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3D NAND

A memory architecture in which memory cells are designed vertically instead of using a traditional floating gate.

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DESCRIPTION

Thanks to 193nm immersion and multiple patterning, flash vendors have extended planar NAND down to the 1xnm node regime. Planar NAND involves the production of horizontal strips of polysilicon. The strips are used to make the wordlines. These, in turn, connect the control gates of the memory cells.

But at the 1xnm node, vendors are struggling to scale the critical element in a NAND device—the floating gate. In fact, the floating gate is seeing an undesirable reduction in the control gate to capacitive coupling ratio.

Realizing that planar NAND is on its last legs, Samsung in 2013 got a jump on its rivals and introduced the industry's first 3D NAND device. Samsung's V-NAND device is a 128 Gbit chip, which stacks 24 vertical layers and consists of 2.5 million channels. More recently, Samsung introduced a 32-layer device and SSDs based on its chips.

In addition, Micron, SK Hynix and Toshiba are also developing 3D NAND.

In 3D NAND, the polysilicon strips are stretched, folded over and stood up vertically. Instead of using a traditional floating gate, 3D NAND uses charge trap technology. Based on silicon nitride films, charge-trap stores the charge on opposite sides of a memory.

One way to illustrate the manufacturing challenges for 3D NAND is to examine Samsung's V-NAND device. Using 30nm to 40nm design rules and a gate-last flow, Samsung's 3D NAND technology is called the Terabit Cell Array Transistor (TCAT). TCAT is a gate-all-around device, where the gate surrounds the channel.

The TCAT flow starts with a CMOS substrate. Then, alternating layers of silicon nitride and silicon dioxide are deposited on the substrate

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step—staircase etch. Using an etcher, the idea is to etch a staircase pattern into the side of the device.

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