

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: August 15, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00034
Patent 10,879,254

**DECLARATION OF STEPHEN CAMPBELL
IN SUPPORT OF
PATENT OWNER'S RESPONSE**

Table of Contents

I.	Introduction	3
II.	Qualifications	4
III.	Understanding of Legal Standards.....	7
A.	Interpreting Claims in an <i>Inter Partes</i> Review Proceeding (Claim Construction)	7
B.	Invalidity by Obviousness	8
IV.	Summary Of Materials Reviewed And Considered	14
V.	Level of Ordinary Skill in the Art.....	18
VI.	Claim Construction	19
VII.	Background	20
A.	Only Claims 2, 7, 8, 11-15, and 17 are at Issue.....	20
B.	3D NAND Memory Technology	20
C.	Overview of the '254 patent (Ex. 1001).....	22
VIII.	A POSITA would not have found claims 2, 7, 8, 11-15, and 17 obvious in view of Nakajima and the knowledge of a POSITA.....	26
A.	Nakajima and the POSITA's knowledge do not render obvious a "dummy channel ... through the stack" (claims 2, 11-15, 17).....	27
1.	A POSITA would not be motivated to replace Nakajima's active channels with dummy channels	29
2.	Petitioner's cited references do not disclose replacing active channels with dummy channels	41
3.	Forming a "dummy channel" is not "unusually simple" and 3D NAND technology is not "particularly straightforward"	47
B.	Nakajima and the POSITA's knowledge do not render obvious "forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening" (claims 7, 8, 14, 15).....	56

1.	Ground 1 fails under Petitioner's first claim construction that requires "undetectable and unintentional recesses"	57
2.	Ground 1 fails under Petitioner's second claim construction that requires "intentional" formation of "actual recesses"	62
3.	Forming "shallow recesses" is not "unusually simple" and 3D NAND technology is not "particularly straightforward"	67
C.	Nakajima and the POSITA's knowledge do not render obvious "simultaneously etching a first opening through the stack and a second opening outside of the stack" (claims 11-15 and 17).	70
1.	Nakajima's "C4" depicted outside the stack in Figure 2 is an obvious error and thus not prior art	71
2.	Nakajima does not disclose "a second opening outside the stack"	73
3.	Nakajima and the POSITA's knowledge do not disclose or render obvious "simultaneously etching"	77
4.	"Simultaneously etching" multiple openings is not "unusually simple" and 3D NAND technology is not "particularly straightforward"	84
IX.	CONCLUSION	87

I. Introduction

1. I have been retained by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) to provide my opinion concerning the validity of U.S. Patent No. 10,879,254 (Ex. 1001, “’254 Patent”). I have been asked to consider the scope and content of the prior art, and respond to certain allegations regarding the prior art, presented by Micron Technology, Inc., (“Petitioner”) in its petition for *inter partes* review of the ’254 patent (“Petition”) and the October 11, 2024, Declaration of Dr. Jack Lee (Ex. 1003). The arguments raised in Dr. Lee’s declaration are similar to those raised in the Petition. Unless otherwise noted, my opinions with respect to the Petition also apply to the corresponding section of Dr. Lee’s declaration, and vice-versa. As explained below (discussing the Grounds raised in the Petition), the invalidity arguments raised in the Petition do not show the prior art in view of the knowledge of a person of ordinary skill in the art (“POSITA”) renders obvious any of the Challenged Claims, and the arguments raised in Dr. Lee’s declaration are insufficient for similar reasons.

2. I have previously rendered my opinion in support of the Patent Owners Preliminary Responses. While I believe that declaration is accurate in all respects, **this new Declaration represents my considered opinion and supersedes my previous Declaration.** There are no substantive differences between the two but any ambiguities should be resolved in favor of this declaration.

3. Where possible, I have used the exhibit numbers connected to the Petition for *Inter Partes* Review of the '254 Patent (IPR2025-00034).

4. I am being compensated for my time at my usual consulting rate of \$450 per hour, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with Patent Owner ("PO") in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

5. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

II. Qualifications

6. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Exhibit 2006. Here, I provide a brief summary of my qualifications.

7. I received my Bachelor's degree in Physics from the University of St. Thomas (St. Paul, Minnesota) in 1975, and my M.S. and Ph.D. in Physics from Northwestern University (Evanston, Illinois) in 1978 and 1981, respectively. I then joined Sperry, now called Unisys, in 1981 as a CMOS process development engineer. In 1982, I was assigned the lead engineer for the 1.2 μm technology

process development effort. In 1984 I was promoted to head of silicon research for the company. This involved a wide variety of process technologies for submicron CMOS.

8. In 1986, I joined the University of Minnesota as an Assistant Professor in the Electrical Engineering Department. My research at the University involved semiconductor processing, materials, and device structures. I raised more than \$100M in various grants and successful submissions to companies and industry consortiums such as the Semiconductor Research Association, as well as State and US government agencies including DARPA and the National Science Foundation. The first ten years of my career at the University concentrated on the development of rapid thermal annealing for 200 mm wafers, particle control in CVD systems, and the development of high uniformity rapid wafer annealing systems. The next ten years were dedicated to the invention and development of high permittivity (aka high-k) films for use as gate insulators. This is necessary to allow the development of deeply scaled CMOS devices. This technology has been widely adopted for nanoscale CMOS devices. In the last fifteen years at the University, my work involved the development of low-cost tandem photovoltaics and micro electromechanical systems (MEMS). The latter included a chronic deep brain sense/stimulation system and very high-speed mechanical switches. Finally, I developed processes for the fabrication of novel 2D materials such as black

arsenic, and fabricated transistors using these materials. I retired from the University in 2021.

9. A brief summary of my work at the University would include:

- Approximately 200 publications
- The leading textbook on semiconductor technology. Currently in its fourth edition, Fabrication Engineering at the Micro and Nanoscale (Oxford 1996, 2000, 2008, 2013) is the dominant text on the topic.
- Honors from outside the University such as being named a Presidential Young Investigator by the National Science Foundation and a Life Fellow by the Institute of Electrical and Electronic Engineers (IEEE).
- Honors within the University including outstanding service and outstanding teaching.
- As the Director of the University's Nanofabrication Center, I increased lab usage from 30 to more than 300 users, enabling millions of dollars research awards annually by Minnesota faculty, and leading to the construction of a new \$80M building with an expansive cleanroom facility.

10. Since retiring from the University, I have consulted with semiconductor companies, including regarding patent litigation.

11. Additional information regarding my education, technical experience and publications, including a list of the U.S. patents of which I am an inventor/coinventor, is included in my *Curriculum Vitae* (Exhibit 2006).

III. Understanding of Legal Standards

12. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

13. My understanding of the pertinent law is outlined below and is the result of explanations provided by counsel. I have applied this understanding in my analysis.

A. Interpreting Claims in an *Inter Partes* Review Proceeding (Claim Construction)

14. I understand that an *Inter Partes* Review is a proceeding before the United States Patent & Trademark Office (“USPTO”) for evaluating the validity of one or more claims of an issued patent.

15. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim

terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary.

16. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the USPTO. I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Invalidity by Obviousness

17. I understand that a patent claim is unpatentable if it is obvious in view of the prior art. I further understand that a claim is unpatentable if it is obvious

from the perspective of a person of ordinary skill in the relevant art (“POSA”), at the time the invention was made.

18. It is my understanding that a claimed invention is unpatentable as obvious under 35 U.S.C. § 103 if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

19. I have been informed that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of the claimed subject matter. I understand that several of these rationales are: 1) combining prior art elements according to known methods to yield predictable results; 2) simple substitution of one known element for another to obtain predictable results; 3) use of a known technique to improve a similar device (method or product) in the same way; 4) applying a known technique to a known device (method or product) ready for improvement to yield predictable results; 5)

choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, 6) and some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. Such a teaching, suggestion, or motivation to combine the prior art references may be explicit or implicit in the prior art, or may be found in other evidence of the level of skill and knowledge of the ordinary artisan.

20. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

21. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have known

the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

22. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are

entirely different from motivation to combine particular references to reach the particular claimed invention.

23. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated to make a combination includes whether he/she would select particular references in order to combine their elements.

24. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

25. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient

reasoning. But, knowledge of a POSITA can only be used to supply a limitation missing from the prior art where recited limitation is unusually simple and the relevant technology particularly straightforward.

26. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness. I have also been informed by counsel that where a prior art reference contains an error that is obvious to a POSITA, that reference cannot be said to describe or suggest the information subject to the error. That is, if a prior art document contains an error that would be immediately apparent to a POSITA, and the correct information is also readily apparent, that erroneous information is not considered part of the prior art that can be used to invalidate a patent.

IV. Summary Of Materials Reviewed And Considered

27. I have been asked to provide analysis and explain the subject matter of the '254 Patent, including the state of the art when the application underlying the '254 Patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '254 Patent including how that art relates to claims 2, 7, 8, 11-15, and 17 (which I refer to as the "challenged claims") of the '254 Patent and to provide my opinions regarding whether that art invalidates the challenged claims. I understand that the Petition challenged more than the challenged claims, but Patent Owner disclaimed a portion of the originally challenged claims. A

28. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the challenged claims of the '254 Patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

29. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '254 Patent.

30. All of the opinions contained in this Declaration are based on the documents I reviewed and my education, experience, knowledge, and professional judgment. In forming the opinions expressed in this Declaration, while drawing on

my experience in the field of semiconductor fabrication, I reviewed the following documents:

Ex.	Description
1001	United States Patent No. 10,879,256 (“the ’254 patent”)
1002	File History for the ’254 patent (“’254 FH”)
1003	Declaration of Jack C. Lee (“Lee”)
1004	Curriculum Vitae of Jack C. Lee
1005	U.S. Patent 10,777,501 to Nakajima et al. (“Nakajima”)
1008	Michelsoni, “3D Flash Memories” (2016)
1010	U.S. Patent 10,354,980 to Mushiga et al. (“Mushiga”)
1015	U.S. Patent 10,290,643 to Kai et al. (“Kai”)
1016	U.S. Patent 9,859,297 to Park et al. (“Park”)
1017	U.S. Patent Appl. Publ. 2018/0308559 to Kim et al. (“Kim”)
1020	U.S. Patent No. 5,945,717 to Chevallier
1021	U.S. Patent No. 10,347,487 to Lee et al.
1022	Ronse, “Optical lithography—a historical perspective,” C. R. Physique 7 (2006) (“Ronse”)
1023	U.S. Patent Appl. Publ. 2019/0081061 to Tessariol et al. (“Tessariol”)
1030	U.S. Patent No. 11,075,084 to Shen et al.
1031	U.S. Patent 10,304,852 to Cui et al. (“Cui”)
2005	Statutory Disclaimer of Claims 1, 5, and 6 of U.S. Patent 10,879,254 Under 37 C.F.R. § 1.321(a) (Filed Feb. 21, 2025)
2008	Michelsoni et al., <i>Inside Solid State Drives (SSDs)</i> (2nd Ed. 2018), as-filed by Petitioner as Exhibit 1014 in IPR2025-00035
2009	Statutory Disclaimer of Claims 3, 4, 9, 10, 18, and 20 of U.S. Patent 10,879,254 Under 37 C.F.R. § 1.321(a), filed May 23, 2025

Ex.	Description
2010	Mark Lapedus, <i>3D NAND Race Faces Huge Tech and Cost Challenges: Shakeout Looms as Vendors Struggle to Find Ways to Add More Layers and Increase Density</i> , Semiconductor Eng'g (May 23, 2019), https://semiengineering.com/3d-nand-race-faces-huge-tech-and-cost-challenges/
2011	Mark Lapedus, <i>3D NAND Metrology Challenges Growing: Rising Costs and Gaps in Equipment Emerge as Technology Scales; New Tools Under Development</i> , Semiconductor Eng'g (Apr. 9, 2019), https://semiengineering.com/3d-nand-metrology-challenges-growing/
2012	Harmeet Singh, <i>Overcoming Challenges in 3D NAND Volume Manufacturing</i> , 60 Solid State Tech. 18 (July 2017) (excerpt)
2013	Declaration of Dr. Jack C. Lee in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,581,322 (Ex. 1003), <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00191 (P.T.A.B. Dec. 2, 2024) (excerpt)
2014	Transcript of the Deposition of Jack C. Lee, Ph.D., taken July 30, 2025, <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00034 ("Lee Dep.")
2015	Timothy Yang, <i>Creating Higher Density 3D NAND Structures: Identify the Manufacturing Issues Associated With Increased 3D NAND Density to Make the Best Tradeoffs and Avoid Structural Collapse</i> , Semiconductor Eng'g (Feb. 21, 2019), https://semiengineering.com/creating-higher-density-3d-nand-structures/
2016	Entegris, <i>White Paper: Considerations for Improving 3D NAND Performance, Reliability, and Yield</i> , https://www.entegris.com/content/dam/web/resources/white-papers/whitepaper-improving-3d-nand-performance-8443.pdf (last visited Aug. 5, 2025)
2017	Yongsik Yu, <i>Tech Brief: Memory "Grows Up" with 3D NAND</i> , Lam Rsch. Newsroom (Apr. 16, 2016), https://newsroom.lamresearch.com/Tech-Brief-Memory-Grows-Up-with-3D-NAND

Ex.	Description
2018	Mark Lapedus, <i>3D NAND's Vertical Scaling Race: More Competition, Business Uncertainty, and Much More Difficult Manufacturing Processes</i> , Semiconductor Eng'g (Dec. 17, 2020), https://semiengineering.com/3d-nands-vertical-scaling-race/
2019	Thermo Fisher Scientific, <i>White Paper: The Challenge of Measuring Buried Critical Dimensions in High-Aspect-Ratio Structures: How Busy Fab Process Owners Can Reduce Time-to-Data in 3D NAND Metrology</i> , https://assets.thermofisher.com/TFS-Assets/MSD/Reference-Materials/helios-5-pxl-3d-nand-whitepaper-wp0025.pdf (last visited Aug. 5, 2025)
2020	Seong Jae Yoo et al., <i>Highly Selective Etching of SiN_x Over SiO₂ Using ClF₃/Cl₂ Remote Plasma</i> , 34 Nanotechnology 465302 (2023)
2022	Jim Handy, <i>3D NAND: How Do You Access the Control Gates</i> , The Memory Guy (Nov. 15, 2013), https://web.archive.org/web/20180513075820/https://thememoryguy.com/3d-nand-how-do-you-access-the-control-gates/#expand
2023	Mark Lapedus, <i>How to Make 3D NAND: Foundries Progress With Complex Combination of High-Aspect Ratio Etch, Metal Deposition and String Stacking</i> , Semiconductor Eng'g (May 23, 2016), https://semiengineering.com/how-to-make-3d-nand/
2028	Mark Shirey, <i>Digging Deep Into High Aspect Ratio Process Control for Memory Technology</i> , Semiconductor Eng'g (Oct. 18, 2018), https://web.archive.org/web/20250621011306/https://semiengineering.com/digging-deep-into-high-aspect-ratio-process-control-for-memory-technology/ (last visited Aug. 15, 2025)
2029	3D Nand, Semiconductor Eng'g (Feb. 13, 2017), https://web.archive.org/web/20180203171844/https://semiengineering.com/kc/knowledge_center/3D-NAND/208 (last visited Aug. 15, 2025)
2030	Mark Lapedus, <i>NAND Market Hits Speed Bump: Transition from Planar to 3D NAND is Harder and More Time-Consuming Than Expected</i> , Semiconductor Eng'g (June 21, 2017), https://web.archive.org/web/20180625071314/https://semiengineering.com/nand-market-hits-speed-bump/ (last visited Aug. 15, 2025)

Ex.	Description
2031	Mark Lapedus, 3D NAND Flash Wars Begin: Market Overcrowding, More Efficient Manufacturing, and Browning List of Scaling Issues Create a Challenging Competitive Landscape, Semiconductor Eng'g (Aug. 20, 2018), https://web.archive.org/web/20180822030129/https://semiengineering.com/3d-nand-flash-wars-begin/ (last visited Aug. 15, 2025)
2032	Mark Lapedus, What's Next for NAND?: Vendors Pin Hopes on 3D Memory, Raising Specter of 2D NAND Shortages; Other Memory Types Add to Uncertainty, Semiconductor Eng'g (May 19, 2016), https://web.archive.org/web/20161127122539/https://semiengineering.com/whats-next-for-nand/ (last visited Aug. 15, 2025)

31. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the '254 patent at the time of the invention, which I have been asked to assume is August 21, 2018.

V. Level of Ordinary Skill in the Art

32. I understand that certain issues relating to validity must be judged from the perspective of a person of ordinary skill in the relevant art at the time of the invention, which I have been told is August 21, 2018.

33. Dr. Lee defines a POSITA as a person having “a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and

experience (*e.g.*, an advanced degree may replace some of the professional experience).” Ex. 1003, ¶36.

34. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art. In view of my educational background and work experience, I was at least a POSITA under Dr. Lee's definition, and was so before August 21, 2018. Regardless of the precise definition of a POSITA, Ground 1 of the Petition does not show the challenged claims obvious. I reserve the right to opine as to an alternative level of a POSITA in this or other proceedings.

VI. Claim Construction

35. Petitioner alleges in its claim construction section that “the terms of the '254 Patent's claims do not require further construction and should receive their plain and ordinary meaning.” Pet. 25 (citing Lee, ¶¶69-72). Dr. Lee similarly states that “the challenged claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.” Lee, ¶72.

36. However, when Petitioner and Dr. Lee analyze the '254 Patent claims reciting the forming of “shallow recesses,” they allege that Nakajima and the knowledge of a POSITA render obvious these limitations under two different claim constructions: (1) by inherent “unintentional recesses” formed by the typical

etching process (Pet. 49-50), and (2) by an “intentional etch that forms actual recesses” (*id.*, 50-52). Pet. 50 (describing the first claim construction as “PO’s Incorrect Claim Interpretation” and the second claim construction as “The Correct Claim Interpretation”); Lee, ¶127.

37. The prior art relied on in the Petition fails to disclose the subject matter of the remaining challenged claims under any reasonable construction, including their plain and ordinary meaning. It is my opinion that no claim construction is necessary to determine that the challenged claims are valid in this proceeding.

VII. Background

A. Only Claims 2, 7, 8, 11-15, and 17 are at Issue

38. I understand that Micron challenged claims 1-15, 17-18, and 20 of the '254 Patent on a single ground as obvious based on Nakajima and the knowledge of a POSITA. Pet. 9. I have been informed by counsel that on February 21, 2025, YMTC disclaimed claims 1, 5, and 6 before the Board's institution decision. Ex. 2005; ID, 3. I have also been informed by counsel that on May 23, 2025, YMTC disclaimed claims 3, 4, 9, 10, 18, and 20. Ex. 2009. I understand that only claims 2, 7, 8, 11-15, and 17 remain at issue in this proceeding.

B. 3D NAND Memory Technology

39. 3D NAND memory devices are a type of non-volatile flash memory that stacks memory cells vertically in multiple layers, unlike traditional 2D NAND

which lays them out horizontally. Memory cells can be written or read by applying a voltage to corresponding conductors that run horizontally across the memory array, called “wordlines.” 3D NAND offers fast read and write speeds due to shorter connection paths between layers, leading to reduced latency and increased performance. As seen below in Figure 5.20 of Exhibit 2008, an exemplary 3D NAND memory depicts a series of vertically stacked memory cells, each controlled by a “Control Gate” (the wordline) shown in red as “CG0” through “CG3.” Ex. 2008, 134. The ends of the “Control Gates” are staggered to form a staircase that allows vertical vias to access and contact each wordline (CG0 to CG3) and connect them to peripheral devices.

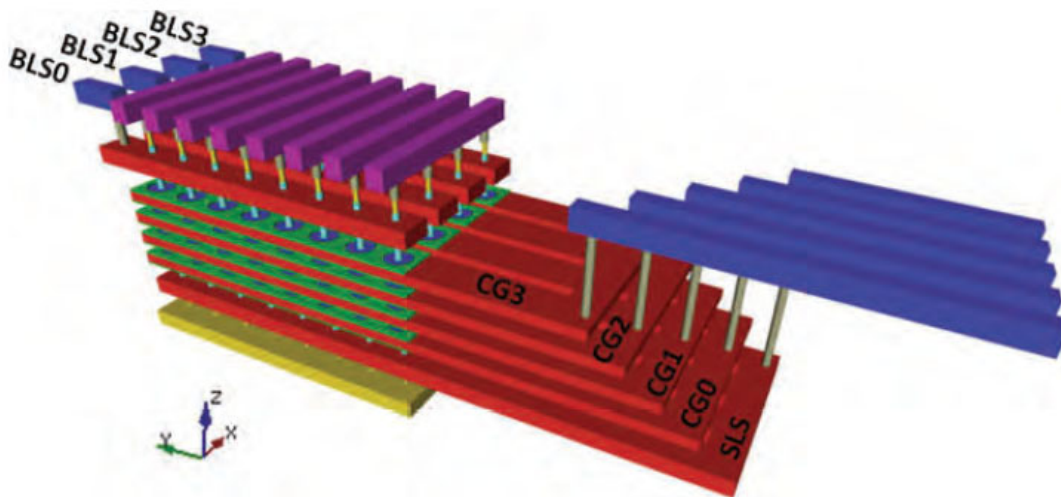


Fig. 5.20 C-FG NAND Flash array with fan-out

Ex. 2008, Fig. 5.20.

C. Overview of the '254 patent (Ex. 1001)

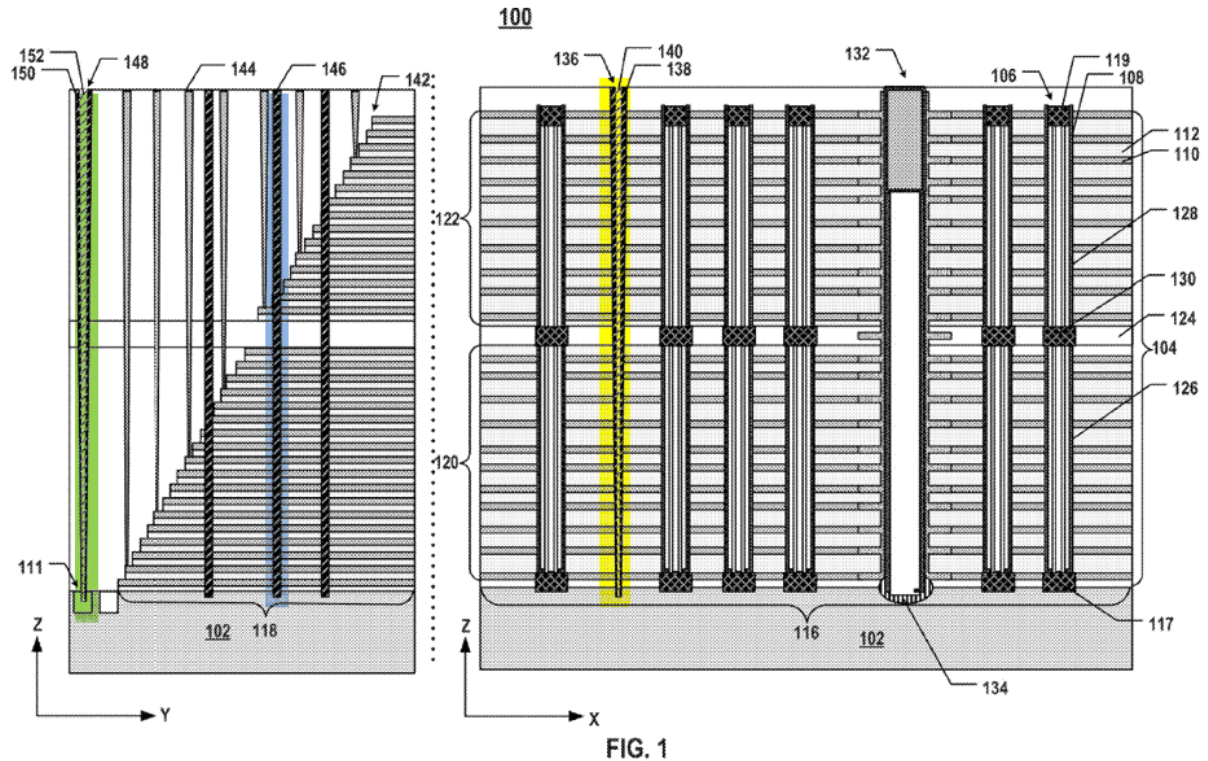
40. The '254 patent is titled "Three-Dimensional Memory Devices Having Through Array Contacts and Methods for Forming Same." Ex. 1001, 1. The '254 patent issued on December 29, 2020, from Application No. 16/745,343, filed on January 17, 2020, and is a continuation of U.S. Application Number 16/149,103, filed on October 1, 2018, which in turn is a continuation of Application Number PCT/CN2018/101482, filed on August 21, 2018. *Id.*

41. The '254 Patent teaches how 3D memory devices require contacts that go vertically through the memory stack called "through array contacts" or "TACs" for "providing vertical interconnects between the stacked memory array device and peripheral device (e.g., for power bus and metal routing)." '254 Patent 4:55-59. In the past, these TACs were formed within a "dielectric stack region within a memory stack," also referred to as a "barrier structure[]." *Id.*, 4:59-62. The drawbacks of a "barrier structure[]" is that "the regions enclosed by the barrier structures take up large area in the core array region where memory strings can be formed." *Id.* at 4:59-65. TACs within a barrier structure "also have a negative impact on the resistance of word lines." *Id.* "Moreover, the existing fabrication processes for forming the barrier structures become more challenging for the next generation 3D memory devices" which "have less process margin." *Id.*, 4:66-5:2.

42. The '254 Patent discloses a unique “3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures.” *Id.*, 5:3-6. The '254 Patent explains that “by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost.” *Id.*, 5:6-9. Also, “[m]ore process margin”—i.e., room for error—may “be obtained due to the elimination of etching and alignment steps for making the barrier structures.” *Id.*, 5:11-15. To “further simplify the fabrication flow and reduce process cost,” the '254 Patent teaches that the non-barrier structure TACs can be “formed in the same fabrication process(es) for making other structures” such as “peripheral contacts” outside the memory stack. *Id.*, 5:15-20.

43. Figure 1, reproduced below with annotations, illustrates a cross-section of an embodiment of a “memory stack 104” and a “staircase structure” 142. *Id.*, 5:32-37, 8:61-63. As shown below, the memory device 100 includes a TAC 136 (yellow) that extends vertically through the stack to carry electrical signals to/from the memory device 100. *Id.*, 8:28-39. Unlike the prior art, TAC 136 is not “enclosed by barrier structures.” *Id.*, 5:3-20. This allows the TACs to be “formed in the same fabrication process(es) for making other structures,” including those *outside* the memory array such as “peripheral contact[]” 148 (green). *Id.*, 5:3-20, 12:24-45. Also, “dummy channel structures 146” (blue) are “disposed in outer

region 118 of memory stack 104 as shown in FIG. 1” to “provide mechanical support to the memory array structures, e.g., memory stack 104.” *Id.*, 9:39-49.



'254 Patent, Fig. 1 (annotated).

44. The '254 Patent describes forming the claimed TACs, which are not enclosed by a “barrier structure.” Rather than forming the TACs in a “barrier structure” to isolate the TACs from other electrical components, the process for forming the TACs begins by forming openings in the memory stack itself for the TAC and then depositing “spacer[s]” on the sidewalls of the openings. *Id.*, 12:64-67. Figure 7B, reproduced below, is a flowchart of an exemplary method for forming such a spacer for the first opening. *Id.*, 13:34-40. The method includes

forming a plurality of shallow recesses by removing parts of the sacrificial layers the memory stack abutting the sidewall of the first opening. *Id.*, 13:36-40.

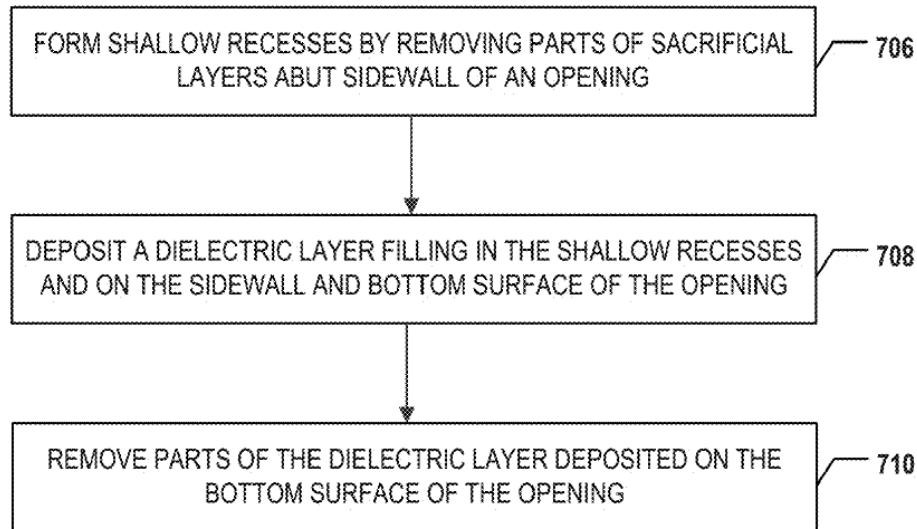


FIG. 7B

'254 Patent, Fig. 7B.

45. As an example, shallow recesses 312 are shown in Figure 3D, annotated below. '254 Patent, 13:52-57. These shallow recesses provide space for a thicker dielectric spacer deposition in step 708, resulting in improved electrical isolation, even without a barrier structure. '254 Patent, 13:59-61, 14:6-12.

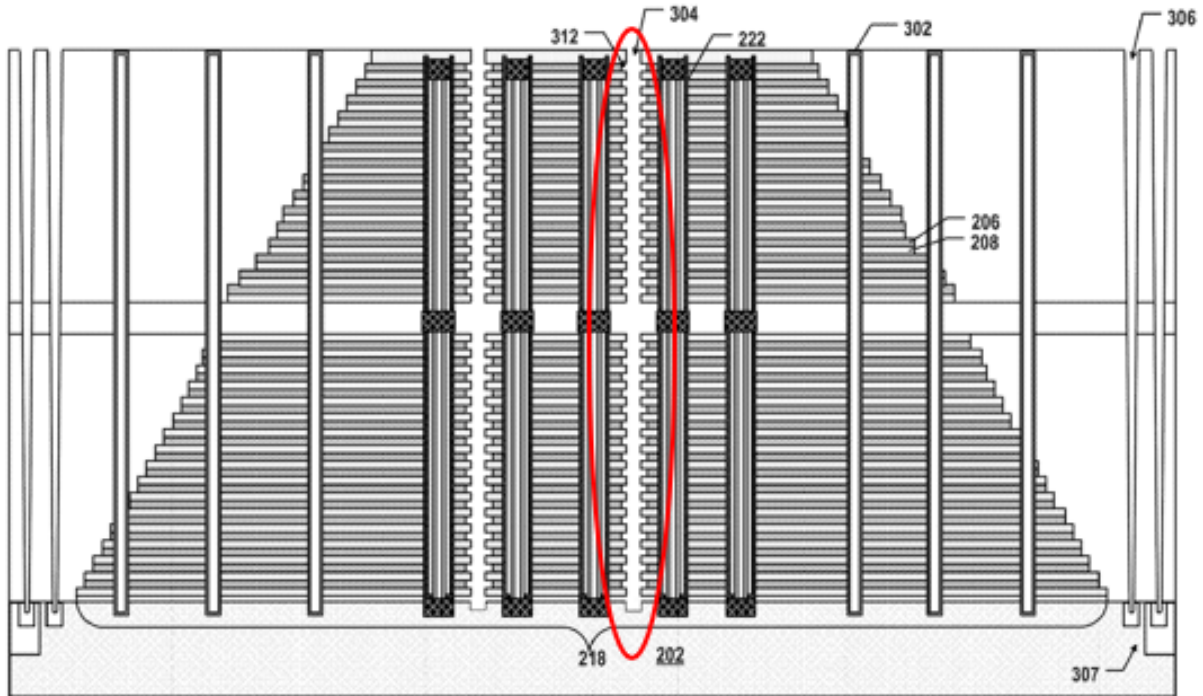


FIG. 3D

'254 Patent, Fig. 3D (annotated).

VIII. A POSITA would not have found claims 2, 7, 8, 11-15, and 17 obvious in view of Nakajima and the knowledge of a POSITA.

46. As a general matter, Dr. Lee relies on the knowledge of a POSITA to supply at least three features missing from Nakajima in relation to the challenged claims. *See* Lee Dep. Tr. 31:9-15 (Dr. Lee admitting that his obviousness positions are not based solely on prior art patents or publications). In doing so, he relies on several patent documents from around the same time as the '254 patent. As I discuss further below, I do not agree that the references cited by Dr. Lee supply the missing “dummy channel,” “shallow recesses,” and “simultaneously etching” features as recited.

47. In my opinion, for the reasons explained in detail below, the recited forming of “dummy channels,” forming of “shallow recesses,” and “simultaneously etching” features are not unusually simple nor is 3D NAND technology particularly straightforward. In fact, forming these components is a challenging and complex process, and the field of 3D NAND memory manufacturing is multifaceted, as it pushes the limits of semiconductor fabrication in terms of size and complexity, wherein even seemingly small modifications can result in unforeseen problems.

A. Nakajima and the POSITA's knowledge do not render obvious a “dummy channel ... through the stack” (claims 2, 11-15, 17).

48. Claim 2 recites “prior to forming the first opening, forming a dummy channel structure extending vertically through the stack.”

49. Claim 11 similarly recites “forming a dummy channel structure extending vertically through the stack.” Claims 12-15 and 17 depend from claim 11.

50. Dr. Lee opines that “it would have been understood and certainly obvious (a POSITA would have been motivated with a reasonable expectation of success) that Nakajima also forms dummy channels for several reasons.” Ex. 1003 ¶ 101. However, in his subsequent discussion (¶¶ 102-109) he does not cite to any portion of Nakajima that discloses forming dummy channels. As Dr. Lee admitted, Nakajima does not disclose “forming a dummy channel structure extending

vertically through the stack,” as claimed. Lee Dep. Tr. at 61:5-8 (admitting Nakajima does not by itself disclose the recited “dummy channel”). Instead Dr. Lee asserts that aspects of dummy channels were known to a POSITA (¶¶ 102-104) and disclosed in other patent literature (¶¶ 105-108). As the Board recognized, Petitioner asserts that Nakajima discloses forming a channel structure through the stack before forming the first opening, but does not argue that Nakajima discloses dummy channels. ID, 15; *see* Pet. 32, 39.

51. The Petition also does not cite to any passage of Nakajima as disclosing formation of a dummy channel structure. Pet., 38-41. Rather, the Petition states that “[i]n view of the knowledge of a POSA, it would have been obvious to implement some of Nakajima’s channels as dummy channels.” *Id.*, 39.

52. Based on the above, I understand the Petition to be proposing a modification of Nakajima to “implement some of Nakajima’s channels as dummy channels” based on the supposed “knowledge of a POSA.” Pet., 39. In my opinion, none of the prior art references cited by Dr. Lee to support the supposed “knowledge of a POSA” disclose forming the “dummy channels” “prior to forming the first opening,” as recited.

53. Petitioner’s proposed modification of Nakajima fails.

54. First, Petitioner fails to establish that a POSITA would have been motivated to modify Nakajima to convert its functional channels into “dummy

channels” as it proposes. To the contrary, in my opinion a POSITA would have understood there would be no advantage—and several meaningful disadvantages—of Petitioner’s proposed modification to Nakajima. Indeed, replacing functional channels with dummy channels would decrease the memory’s storage capacity.

55. Second, Petitioner errs in its attempt to supply a missing limitation by relying on knowledge of a POSITA because forming the recited “dummy channels” is not unusually simple and 3D NAND technology is not particularly straightforward. Both are complex, as described in detail below.

1. A POSITA would not be motivated to replace Nakajima’s active channels with dummy channels

56. Petitioner asserts that it would have been obvious to “implement some of Nakajima’s channels as dummy channels” to provide “structural support.” Pet. 39; *see also id.*, 40 (repeatedly asserting that the dummy channels provide structural support); ID, 15. As depicted below, Petitioner’s annotation of Figure 2 of Nakajima identifies the channels “CL” in region 100a (depicted in the purple box below) that Petitioner proposes converting into “dummy channels.” Pet. 42. Nakajima’s pillar structure CLs are channels with “a core layer 50, a semiconductor layer 20, and a memory layer 30,” forming part of a memory cell. Nakajima, 5:16-66; *see id.* at 5:49-58 (memory cell constitutes semiconductor layer 20 functioning as a channel, memory layer 30, and conductive layer 70

functioning as a control gate (word line)). The semiconductor layer 20 “functions as a channel.” Nakajima 5:55-56. Together, the “semiconductor layer 20, the memory layer 30, and the conductive layer 70 constitute a memory cell MC.” Nakajima 5:49-50. In other words, the channels CL include functional components of the memory cells, and have vital roles in the device.

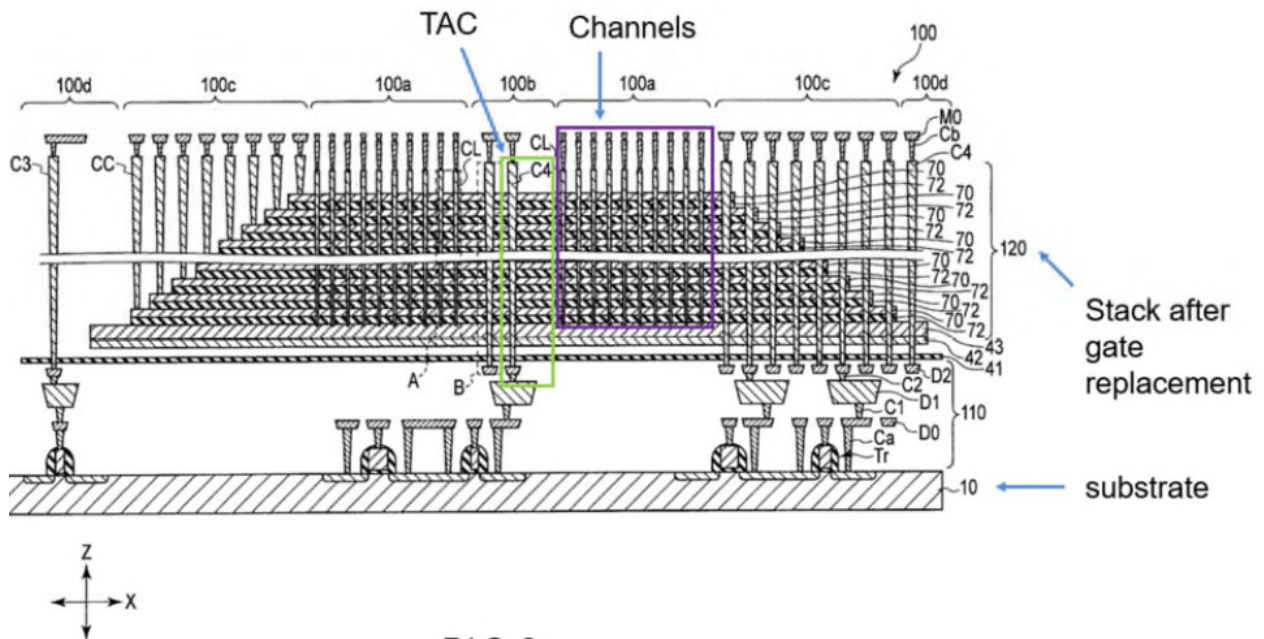


FIG. 2

57. However, I agree with the Board’s finding in its Institution Decision, that “no advantage is clearly shown by replacing some of Nakajima’s active channels with dummy channels.” ID, 16.

58. **First**, as the Board found, “the record does not support Petitioner’s assertion that replacing Nakajima’s active channels with dummy channels would provide additional structural support.” ID, 16-17. Dr. Lee asserts that “dummy channels provide structure support, which is important during the gate line

replacement process (because that process forms voids where the sacrificial gates were, necessitating support members to prevent the stack from collapsing).” Ex. 1003 ¶ 104. But Dr. Lee omits that Nakajima discloses that the pillar structures CL—which are not dummy structures—already provide this support. Specifically, Nakajima discloses that after “the sacrifice layers 71 are removed,” the remaining “insulation layers 72 of the layer stack” are “*supported by physical joints with such pillar structures CL*, and thereby the *gaps 73 between the insulation layers 72 are maintained.*”¹ Nakajima, 8:24-29. As a result, in my opinion a POSITA would understand that Nakajima’s “channels” (“pillar structures CL”) already provide “structural support,” even without modifying them to become “dummy channels” as Petitioner proposes. *See id.*; Pet. 39.

59. Petitioner even admits that “Nakajima describes that the channel pillars support the structure during the gate replacement process.” Pet. 32. Petitioner provides no reason that a POSITA would think Nakajima’s “pillar structures CL” are inadequate for their expressly stated purpose of “suppor[ting]” the “layer stack”—and it is my understanding on reading Nakajima that a POSITA would view Nakajima’s “pillar structures CL” as adequate support. *See* Nakajima, 8:24-29. Moreover, as the Board recognized, Petitioner has not asserted that dummy channels are more supportive than active channels, or “how any tradeoffs

¹ Emphasis is added throughout my declaration unless I state otherwise.

with reduce memory capability or additional processing would be viewed as desirable by a [POSITA].” ID, 16-17. In my opinion, for example, a POSITA would not be motivated reduce memory capability as Petitioner proposes even if it provided a minimal advantage in support (which Petitioner fails to establish is the case), at least because doing so would be contrary to one of the main goals of 3D NAND to increase memory density. Petitioner's suggestion that a POSITA would have been motivated to modify Nakajima as it proposes to use “dummy channels as support structures” is incorrect. *See* Pet. 40; ID, 16-17.

60. So far as Petitioner argues that modifying Nakajima's active channels to become dummy channels involves simply disconnecting them at the top, Petitioner contradicts its argument that a POSITA would be motivated by some structural support advantage. In other words, a POSITA would recognize that disconnecting Nakajima's active channels to make them dummy channels would have no impact on the support provided by these channels—the support would remain unchanged. Moreover, a POSITA would recognize that any alleged space saved by not connecting dummy channels would pale in comparison to the reduction in memory storage. A POSITA would recognize that increased density of memory storage is one of the principal goals of 3D NAND design, as explained further in the next paragraph. I agree with the Board's recognition that Petitioner's

proposed modification provides no structural advantage and would reduce memory storage capability. ID, 17.

61. **Second**, in my opinion, a POSITA would recognize that Petitioner's proposed modification would reduce Nakajima's memory storage capability and reduce integration density in the memory (i.e., the amount of data (bits) that can be stored per unit area on a 3D NAND chip). A POSITA would understand and be motivated to design a 3D NAND chip with a higher memory integration density because it can store more data in the same physical space compared to a chip with lower memory integration density. Ex. 2013, ¶165 (Dr. Lee testifying "[t]he driving force in manufacturing memory is to create as dense as an array as possible" and "a large focus of design efforts for memory revolves around fabricating a dense array"); Kim, [0003] ("Semiconductor devices have been highly integrated for satisfying high performance and low manufacture costs which are desired by users."). Dr. Lee admitted in his deposition that "[memory] density is *one of the most important aspect[s] in designing memory*," and that "we always want to have as high density as possible; for lower cost, higher yield, and at the end, you know, with lower cost per bit, higher yield, [a] company would ... make a lot more money per chip." Lee Dep. Tr. 44:8-11, 48:1-6.

62. In my opinion, a POSITA would have understood that increasing memory density has been the goal throughout the development of NAND memory,

including 3D NAND memory. *See, e.g.*, Ex. 2018, 5 (“In 3D NAND, the ultimate goal is to stack more layers on a substrate, enabling more density.”); Ex. 2011, 3 (“To continue increasing density, the industry is moving to 3D NAND, which stacks the memory cells in the vertical direction.”); Ex. 2012, 1 (“3D NAND has become a mainstream technology because of its ability to increase bit density in memory devices.”); Ex. 2016, 2 (“The promise of 3D NAND is higher density and lower cost per bit.”); Ex. 2017, 1 (recognizing that “different design concepts and manufacturing methods are needed to continue increasing memory density”); *id.*, 2 (recognizing that 3D NAND design is “all in pursuit of higher memory density”); Ex. 2019, 1 (recognizing that to meet “data demands of applications like IoT, artificial intelligence, ADAS, and big data analysis,” “memory manufacturers are striving to increase the bit-density of their products”). As a result, in my opinion a POSITA would not have been motivated to reduce memory density.

63. A POSITA would not be motivated to replace Nakajima's active channel with a dummy channel because it would be contrary to “achiev[ing] higher density,” which is “one of the goal[s] of designing 3D NAND” and “designing a memory chip,” as Dr. Lee admitted. *See* Lee Dep. Tr. 48:10-17, 49:8-14.

64. Petitioner also does not explain how the Nakajima memory device can still operate as intended if “some of Nakajima's channels” are changed into non-functional “dummy channels” that only provide mechanical support. Lee ¶108

(dummy channels “do not store data”). But even if Nakajima's memory device is still operable as intended, replacing channels with dummy structures will lower the memory's storage capacity because the number of active channels will be decreased—a result that a POSITA would view as undesirable and one Petitioner does not address.

65. **Third**, in my opinion, a POSITA would also recognize that decreasing memory density would make the memory less cost effective, as Dr. Lee has testified before. Ex. 2013, ¶165 (Dr. Lee testifying that “[a]s density increases, the memory design becomes more cost effective.”); Kim, [0003] (“Semiconductor devices have been highly integrated for satisfying high performance and low manufacture costs which are desired by users.”). Petitioner's expert further admitted that the less dense the memory array, the more silicon is needed to create a given memory size. Lee Dep. Tr. 48:18-49:2; Ex. 2013, ¶165 (Dr. Lee testifying: “The driving force in manufacturing memory is to create as dense as an array as possible for two reasons. First, memory capacity is obvious [sic] a key element of a memory. Second, the denser the array, the less silicon is necessary to create a given memory size. As density increases, the memory design becomes more cost effective.”). As a result, a POSITA would understand that the less dense the memory array, the more silicon is needed to form a given memory size, and as the less cost effective the memory array.

66. **Fourth**, Petitioner alleges that dummy channels were “commonplace” and argues their attributes were “well known.” Pet. 40-41. In particular, Petitioner states it was well known “to include dummy support members, including ones that travel through the entire stack or partially through the stack.” *Id.* at 40. But this shows, at best, that a POSITA could have made dummy channels, not that a POSITA would have been motivated to modify Nakajima as proposed by Petitioner. To the contrary, for the reasons stated in this declaration, a POSITA would not have been motivated to replace Nakajima's active channels with dummy channels.

67. **Fifth**, Petitioner's remaining arguments are also incorrect. Petitioner points to various alleged reasons why dummy channels are suitable to use as “support structures”—e.g., that they “can be made by the same process and at the same time as the active channels,” “do not require connections to the upper-level devices,” “provide[] additional structural support,” were “well known,” and improve “uniform[ity].” Pet. 40-41. Petitioner misses the point. As discussed, Nakajima already discloses that its active channels, the “pillar structures CL,” provide adequate structural support for the memory array. *See* Nakajima 8:27-29. Petitioner does not (as it cannot) argue that those pillar structures CL do not serve their intended purpose of providing structural support. Thus, even if dummy channels may be suitable “support structures,” Petitioner fails to provide any

reason why a POSITA would be motivated by a support advantage to implement them in Nakajima as proposed—especially given the disadvantage in memory capacity. *See* Nakajima, 8:24-29.

68. Petitioner also fails to show that Nakajima's memory array would suffer from a "likelihood of defective bits on the edge of the memory cell region." *See* Pet. 40-41. Petitioner fails to show how this "likelihood" applies to Nakajima's structure. In addition, the references Dr. Lee relies on do not support that "edge of the array" issues are a concern in 3D NAND, or that adding dummy channels would resolve it. *See, e.g.*, Ex. 1020, 8:47-53 (patent filed in 1998 referring to a "typical flash cell array" at that time, not 3D NAND); Ex. 1021, 2:20-43 (indicating edge of array issues "**may** typically occur at the boundary ... an abnormal edge pattern at the edge of array **may** be controlled by adding a dummy pattern region"). Moreover, a POSITA would not be motivated to remove active memory channels from a memory array on a possibility of some defective bits. Although Petitioner's expert attests that "it is common to refrain from using the cells at the array edge," which are "sometimes referred to as dummy cells," due to "processing variations" (Lee, ¶102 (citing Ex. 1020)), this does not show an advantage to adding dummy channels. And Petitioner's expert recognized that such a dummy region at the edge of the array is "later sacrificed in processing," which would not result in the claimed limitation of a "dummy channel structure

extending vertically through the stack,” undermining Petitioner’s other rationale that the dummy channels would provide additional support. Lee, ¶102 (citing Ex. 1021, 2:20-43); *see* ID, 18 (Board recognizing same). Moreover, a POSITA would understand that process and control issues near the edge of the wafer can be addressed by “monitoring and control of the wafer edge, imposing denser sampling compared to the rest of the wafer.” Ex. 2028, 4.

69. Although Dr. Lee asserts that dummy channels can be employed “at the edge of the array” to provide support to mitigate against abnormalities (Ex. 1003, ¶102), this is not a concern in Nakajima (nor does Dr. Lee allege it would be one). For example, Nakajima’s through-array contacts (TACs) in the staircase region 100c provide structural support at the edge of the array *without* the use of dummy structures. *See, e.g.*, Nakajima, Fig. 2. Regardless, Dr. Lee does not explain why this would motivate a POSITA to modify the functional channels of Nakajima into non-functional dummy channels.

70. Petitioner also does not explain where or how dummy channels would be placed at “the edge of the memory cell region” to extend the memory cell pattern in such a manner as to “result in an overall more uniform feature pattern” (Pet. 40-41), especially given there is no room at the edge of Nakajima’s memory cell array area 100a. *See, e.g.*, Nakajima, Fig. 2. In my opinion, a POSITA would agree with the Board’s recognition that Petitioner does not show that such placement is known

in the prior art such that it would be implemented in Nakajima without further explanation. ID, 18. For example, Petitioner errs in relying on Exhibit 1022, which, as the Board recognized, merely “discusses advantages of quadrupole illumination for photolithography, lacks an explanation of its connection to the channels at issue in the claimed invention, and therefore does not meaningfully support Petitioner’s obviousness assertion.” ID, 18 n.9; *see* Pet. 41. Petitioner also fails to cite anything in Kai, Kim, Park, or any other reference that discloses “addition of the additional rows” that “extend[] the memory cell pattern.” Pet. 40. To the contrary, as discussed, those references do not disclose dummy structures in the memory cell area at all; they disclose only dummy channels *outside* the memory cell array. *See below* Section VIII.A.2. Further, Kim and Park disclose that the dummy channels *should not* be within the memory cell array. Kim, [0047]; Park (Ex. 1016), 7:38-42.

71. The Petition also does not suggest that Nakajima should be modified to *add* dummy channels to the existing active channels. Instead, the Petition states “[i]n view of the knowledge of a POSA, it would have been obvious to implement some of Nakajima’s channels as dummy channels” (Pet. 39), before citing “several reasons” (Pet. 40) for making that modification. *See also* ID, 16 (Petitioner’s combination does not add new channels, but instead, “implement[s] some of Nakajima’s channels as dummy channels.”) (citing Pet., 39). But even if Petitioner

had made that argument (and it did not), a POSITA would have no reason to make the modification to add dummy channels to the existing active channels, and Petitioner provides none. A POSITA would understand that adding dummy channels would increase materials and processing cost, reduce memory cell density, and increase the footprint of the 3D NAND memory without a corresponding increase in memory or any discernable benefit—none of which would have been desirable to a POSITA. *See* Kim, [0003] (“Semiconductor devices have been highly integrated for satisfying high performance and low manufacture costs which are desired by users.”); Ex. 2013, ¶165 (Dr. Lee testifying that “[a]s density increases, the memory design becomes more cost effective.”). It is also inconsistent with Petitioner’s argument that dummy channels “do not require connections to the upper-level devices, thereby not consuming space above the structures while also serving as support structures,” because additional dummy channels would consume significant space around the memory array. *See* Pet. 40. Moreover, Petitioner fails to address, and provides no evidence to support, that adding dummy channels to the current array occurs “prior to the forming the first opening” of the TAC, as recited. Petitioner only relies on Nakajima’s active channel being formed “prior to” the TAC. Pet. 38-39 (citing Pet. 30-32).

2. Petitioner's cited references do not disclose replacing active channels with dummy channels

72. The Petition cites to three references (Kai, Kim, and Park) that purportedly “confirm[] the knowledge of a POSITA” regarding the recited “dummy channels.” Pet. at 39. None of these references disclose dummy structures within the memory array, as the Petition and Dr. Lee propose. At best, these references disclose forming dummy channels outside a memory array. As a result none of them motivate a POSITA to implement “some” of Nakajima's active channels CLs within the memory array as dummy structures. Nakajima, 2:54-55 (Nakajima's channel structures (CLs) are within the “memory cell array areas 100a”).

73. The Kai, Kim, and Park references fail to show that a POSITA would have the “knowledge” to change functional channels *within a memory array* into dummy channels, as in Petitioner's proposed modification of Nakajima. Instead, they each disclose dummy structures formed *outside* the memory array, where active channels are not present. In my opinion, such disclosures would not motivate a POSITA to convert Nakajima's channel structures (CLs) *within* the “memory cell array areas 100a” into dummy structures as Petitioner proposes. See Nakajima, 2:41-43; Pet., 30-32, 39.

74. The Kai reference (Ex. 1015) discloses “support pillar structure 20” (Petitioner's dummy channel; blue) in a “*contact region 300*” (yellow) that is

between memory array region 100 (orange) and the peripheral device region 200. Kai, 6:2-5, 16:28-31, Fig. 6A (annotated below); *see also id.*, Fig. 15A (showing “support pillar structure 20” only in the connection region); Pet. 39. Memory opening fill structure 58 (green), where memory elements reside, is formed in memory array region 100 (orange). Kai, 16:19-23 (memory opening fill structure 58 includes at least memory stack structure 55, dielectric core 62, and a drain region 63 within a memory opening 49), 9:20-28 (memory opening 49 houses memory elements and is formed in memory array region 100).

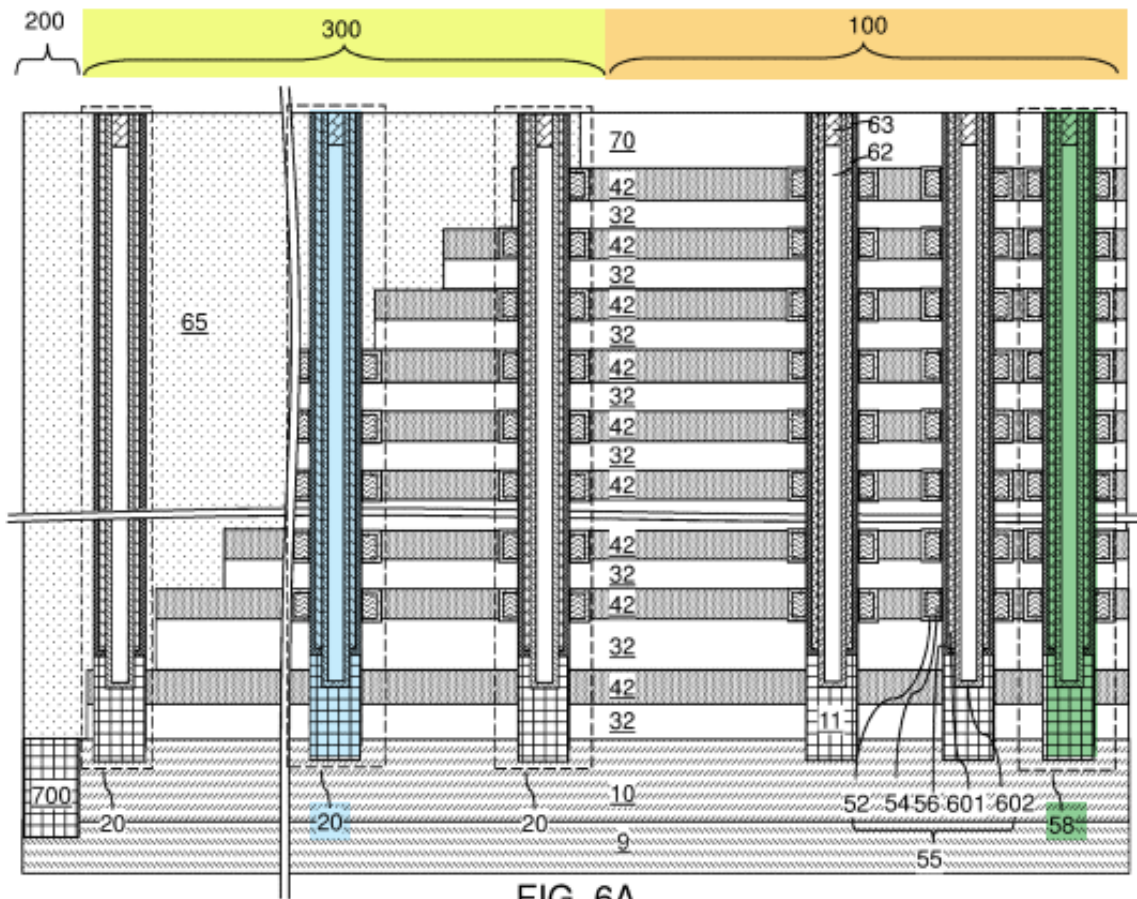


FIG. 6A

Kai, Fig. 6A (annotated). The “memory array region 100” includes what the Petition calls “active channel structures (55)” that “include contacts (88)” to the upper level, as shown in Figure 15A. Kai, 16:28-38, 25:58-63.

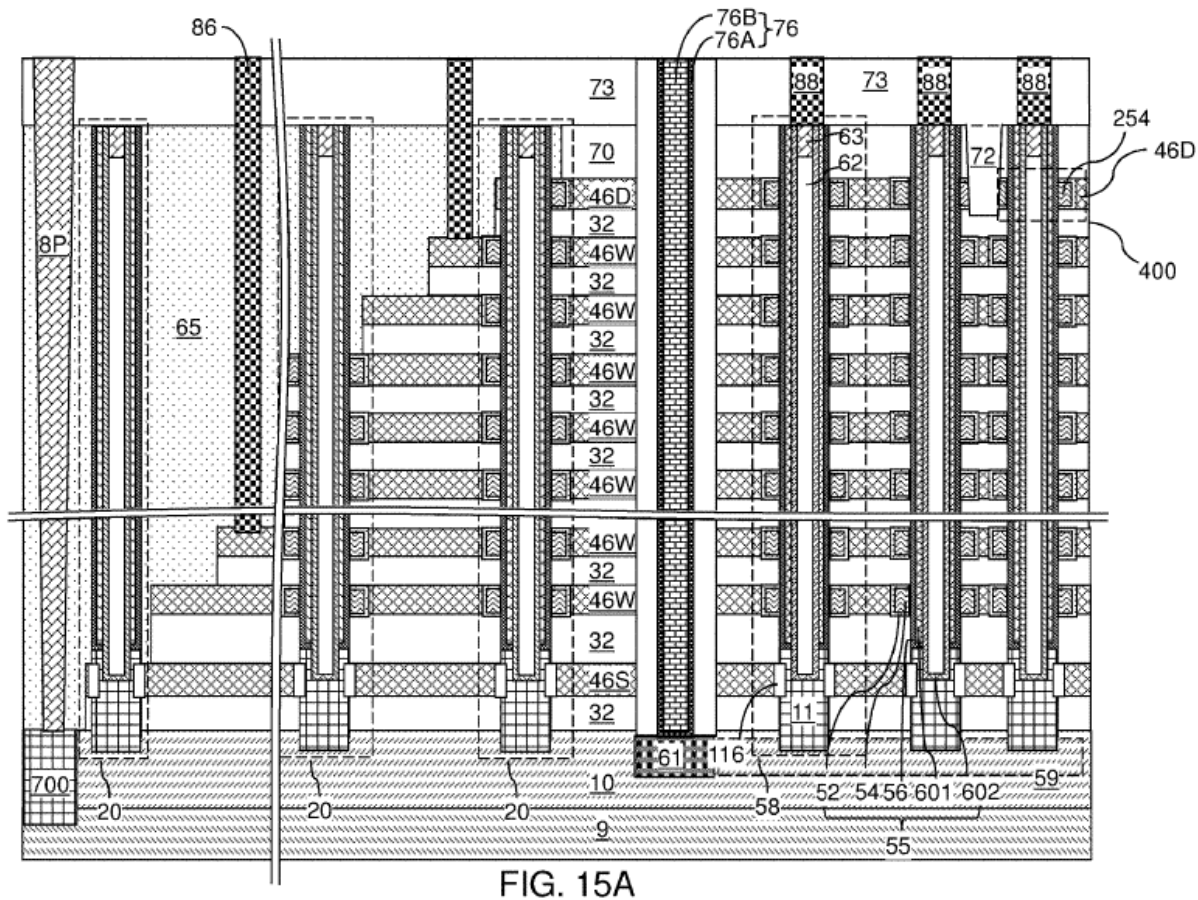
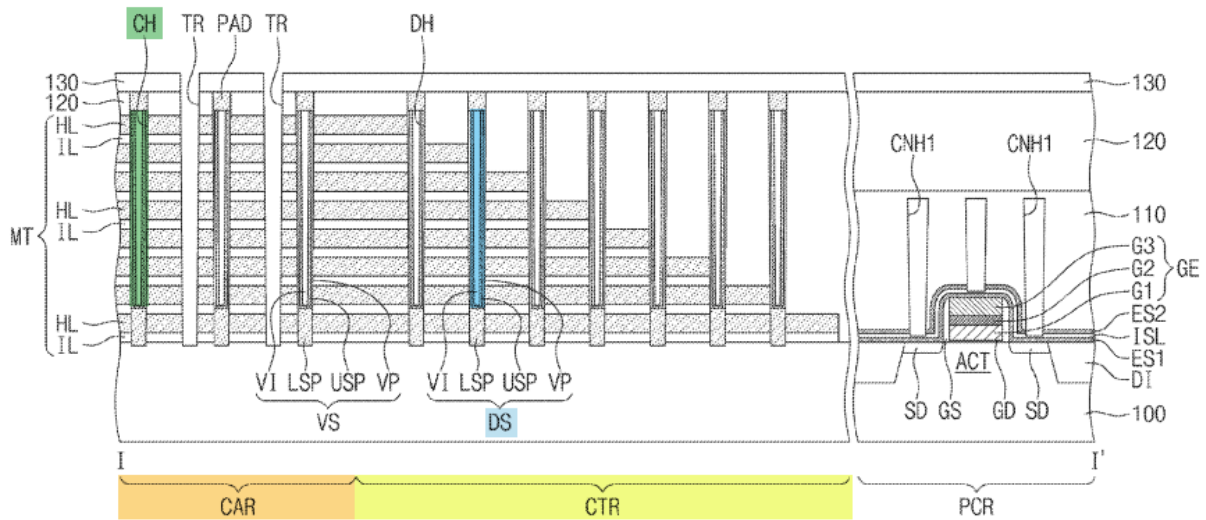


FIG. 15A

Kai, Fig. 15A.

75. Similarly, the Kim reference (Exhibit 1017) discloses “dummy structures DS” in a “connection region CTR”—not the “cell array region CAR” where the memory array is located. Kim (Ex. 1017), [0047] (dummy structures DS formed in the connection region CTR), [0070] (“[o]n the connection region CTR, a plurality of dummy holes DH may be formed”); *see* Pet., 39. As seen

below, dummy structures DS (blue) are located in the connection region CTR (yellow), not the cell array region CAR (orange) that includes channel holes (CH) (green) housing memory cells. Kim, [0037] (channel holes CH formed in the cell array region CAR; vertical structures VS formed in the channel holes CH), [0018] (cell array region CAR includes a memory cell array), [0023] (vertical structures VS (or semiconductor pillars) are memory cells), Fig. 1.



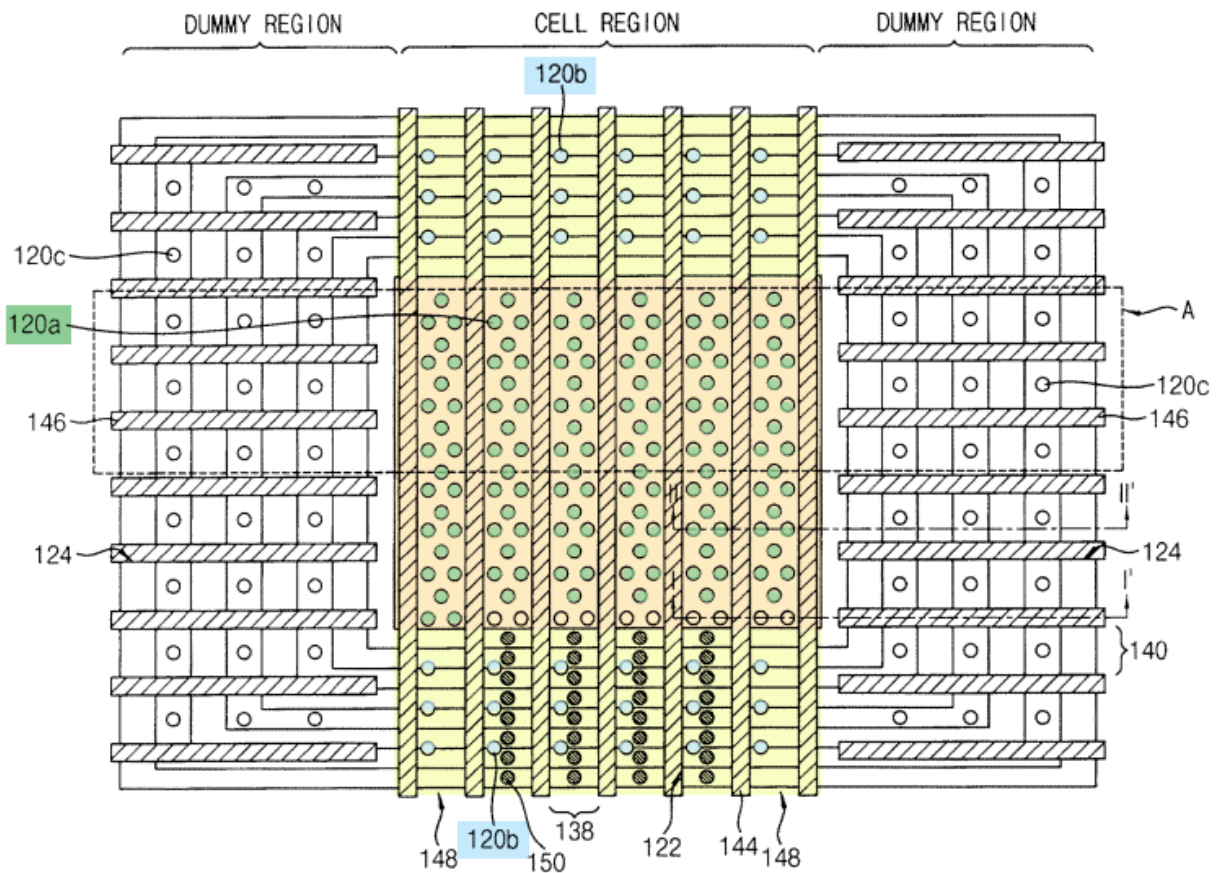
Kim, Fig. 13 (annotated); *see* Pet. 39-40 (Petitioner relying on Kim's Fig. 13).

76. Moreover, Kim teaches away from forming dummy channels in the memory array region, stating that “dummy structures DS may be selectively provided **only** on the connection region CTR and **not** on the cell array region CAR.” Kim, [0047].

77. For its part, Petitioner asserts only that Park (Exhibit 1016) “discloses active and dummy, supporting channels.” Pet. 39. But, like Kai and Kim, Park's dummy channels (second channel structure 120b) are outside the main cell region

where active memory channels (channel structure 120a) reside. Park discloses “second channel structure[s] 120b” (blue below) that are dummy channels “disposed on the wiring region” (yellow)—not the “main cell region” (orange) housing active channel structures 120a (green). Park, 7:32-35 (identifying main cell region in the center and adjacent wiring region having a stepped shape), 7:38-42 (“The first channel structure 120a may be disposed on the main cell region, and may be provided as a portion of a memory cell. The second channel structure 120b may be disposed on the wiring region, and may not be provided as the portion of the memory cell.”), 10:37-47; Pet. 39 (referring to second channel structures 120b as “dummy, supporting channels”) (citing Park, 7:45-51)).

FIG. 1



Park, Fig. 1 (annotated).

78. Like Kim, Park teaches away from forming dummy channels in the memory array region, stating that “[t]he second channel structure 120b may be disposed on the wiring region, and *may not be provided* as the portion of the memory cell” where “first channel structure 120a” resides. *Id.*, 7:38-42.

79. To summarize, none of Kai, Kim, or Park, disclose forming dummy channels in the memory array as Petitioner proposes, let alone changing functional channels that store data in the memory array into non-functional dummy channels.

Instead, each of these references disclose forming dummy channels in a “contact region” (Kai), “connector region CTR” (Kim), or “a wiring region” (Park) *separate* from the memory array. Those disclosures would not have motivated a POSITA to change Nakajima’s active “pillar structures CL” that are in the “memory cell array area 100a” into dummy structures—especially because modifying active channels within the memory cell array to become dummy channels would provide no support advantage, reduce storage capacity, and increase cost as discussed above.

80. Although I focused on claim 2 above, these opinions also apply to claim 11 for the same reasons as claim 2, because claim 11 similarly recites “forming a dummy channel structure extending vertically through the stack.” Claims 12-15 and 17 depend from claim 11.

3. Forming a “dummy channel” is not “unusually simple” and 3D NAND technology is not “particularly straightforward”

81. Petitioner’s arguments as to claims 2, 11-15, 17 fail for another independent reason. As the Board found (ID, 18-19), Petitioner errs by relying on a POSITA’s general knowledge to supply the “dummy channel” limitation missing in Nakajima because Petitioner failed to demonstrate or support that the “dummy channel” limitation missing from Nakajima is unusually simple and that 3D NAND technology is particularly straightforward.

a. **3D NAND is complex technology**

82. A POSITA would understand that 3D NAND technology, including manufacturing relevant components, is not particularly straightforward. Instead, a POSITA would understand that 3D NAND is described as “**very complex**” and including “complex device structures.” Ex. 1008, 293; Ex. 2012, 3; Ex. 1008, 212 (“3D NAND architectures need to be proved cost effective in terms of process costs and product yield because the process complexity is not trivial if compared to 2D NAND.”); Ex. 2012, 4 (“[T]he overall complexity and capital intensity of 3D NAND manufacturing add significantly to the challenges fabs are facing in terms of process control, yield, and economics.”); *see also* Ex. 2019, 5 (“With each generation, the fabrication of 3D NAND becomes more complex.”).

83. In my opinion, a POSITA would also understand that manufacturing 3D NAND “involves a number of new and **complex process steps**.” Ex. 2032, 4; Ex. 2012, 4-5 (recognizing “[a]n incredible level of precision and repetition is required in defining complex 3D structures with extremely high aspect ratio (HAR) features,” including “alternating film deposition” and formation of “staircase,” “wordline,” “contact,” and “channel” features), Fig. 1; Ex. 2028, 1 (“3D NAND has led to complex deposition and etch with angstrom-level precision requirements.”); Ex. 2031, 8 (describing removal of nitride layers and forming a wordline as a “complex process”); *see also* Ex. 2011, 3 (“[M]aking 3D NAND is

a complex process” that requires “using a deposition tool” to deposit layers of material on a substrate); *id.*, 2 (“The big challenge is to characterize the inner portions of a 3D NAND device, which consists of complex materials, multiple layers and tiny channel holes.”); Ex. 2018, 5 (“3D NAND is a complex technology”); *id.*, 6 (“In all cases, the 3D NAND process flow is complex.”). A POSITA would understand that forming the critical staircase pattern, for example, requires a “highly controlled etch process” and “extreme accuracy” to “maintain the stair CD thus avoiding misaligned contacts.” Ex. 2012, 7. “If the CD for a pad is off by a few percent, that error will propagate through subsequent pads defined within the same lithography pass.” Ex. 2012, 7; Ex. 2029, 2 (describing the staircase etch as “another difficult step”). As I discuss elsewhere in my declaration, other features of 3D NAND are complex and challenging for the reasons in Sections VIII.A.3.b, VIII.B.3, and VIII.C.4, supporting 3D NAND technology is not particularly straightforward.

b. Forming the recited “dummy channel” is a complex process

84. In my opinion, a POSITA would also understand that the etching process is “the most critical and challenging step in 3D NAND because it is key to achieving uniform hole size through multiple layers to define the channel of memory cells,” as well as dummy channels. Ex. 2012, 6; Ex. 1008, 218 (“One of the issues is related to yield loss derived from complexity of vertical trench or hole

etching with many layers.”); Ex. 2030, 6; *see also* Ex. 2010, 6 (describing the etching process as “the hardest part of the flow” because “the etch tool must drill tiny circular holes or channels from the top of the device stack to the bottom substrate”—“[e]ach channel must be parallel and uniform”); Ex. 2011, 4 (describing the etching process as “the most difficult step in 3D NAND”); *id.*, 6 (describing the HAR etch process is conducted using reactive ion etch (RIE) systems). “More than a trillion holes must be etched simultaneously and uniformly on every wafer, each with an aspect ratio of more than 40:1.” Ex. 2012, 6; *id.*, 4-5 (“An incredible level of precision and repetition is required in defining complex 3D structures with extremely high aspect ratio (HAR) features.”); Ex. 2032, 6 (recognizing the challenge in forming 3D NAND of 64 or more layers because “the aspect ratios are too complex and difficult”).

85. In my opinion, a POSITA would understand that forming these channels is not simple—“[d]eep etch on these multilayer stacks can ***push the limits of physics*** to achieve uniformity from top to bottom.” Ex. 2012, 6; Ex. 2023, 4 (“This etch is really complex.”); Ex. 2031, 6 (describing HAR etching as the “hardest part of the flow” and “very difficult and very time-consuming”); Ex. 2032, 6 (recognizing the challenge in forming 3D NAND of 64 or more layers because “the aspect ratios are too complex and difficult”); Ex. 2012, 4 (Figure 1 depicting a “3D NAND architecture showing some of the most challenging and critical

deposition and etch processes”); *see also* Ex. 2010, 7 (recognizing “[t]he memory hole etch is probably the most difficult step in 3D NAND manufacturing” because “[y]ou need to etch many microns deep and you need to be able to tightly maintain the profiles to very specific dimensions”); Ex. 2019, 2 (“The etch process to create these channels is also one of the main challenges for current and future 3D NAND designs” because “variations in the channel holes can have drastic effects on the performance of 3D NAND devices.”). A POSITA would know that forming a dummy channel structure involves complex semiconductor manufacturing processes, including “etching an opening through dielectric stack 218 and/or one or more dielectric layers using wet etching, and/or dry etching, such as DRIE” and “thin film deposition processes, such as ALD, CVD, [and] PVD.” ’254 Patent, 12:7-23.

86. The deeper the etch, the harder it is to maintain a continuous etch rate and unwanted variations can occur, such as bowing or twisting within the channel, an incomplete etch, or variation between the top and bottom of the channel. Ex. 2012, 6, Fig. 3; *id.* (“channel hole etching becomes increasingly challenging due to higher aspect ratios”); 2030, 6-7, Fig. 7; Ex. 2017, 3 (“The channel hole etch is one of the most challenging processes” because “[t]ight control is needed to minimize bowing and twisting of the channel, which could lead to shorts or interference between neighboring memory strings.”); *see also* Ex. 2019, 2-3

("[T]he channel hole HAR etch is arguably the most difficult step and adds considerable challenges ... [a]ny variations in channel hole width from top to bottom need to be characterized, and problems such as bow CD, twist, and tilt need to be identified. To further complicate this process, as the etch depth increases, etch rates tend to decrease, which can exacerbate these problems.").

87. Although some of these statements refer to memory channels, they equally apply to etching dummy channels through the stack, which are sometimes formed by the same process as memory channels. *See, e.g.*, '254 Patent, 12:18-23 ("In some embodiments, dummy channel structures 302 are formed simultaneously with channel structures 222 in the same fabrication steps, such that the opening of each dummy channel structure 302 is filled with at least some of the materials filling in channel structures 222."); Kim (Ex. 2017), ¶[0071] ("The channel holes CH and the dummy holes DH may be formed at the same time.").

88. Moreover, a POSITA would understand that forming dummy channels is not unusually simple because dummy channels do not have a standard, predictable structure. Dummy channel structure ranges from using the same materials as channel structures to being "fully filled with dielectric materials" like "silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof." '254 Patent, 9:27-37.

89. Petitioner's cited prior art confirms forming a dummy channel structure is not unusually simple and this technology is not particularly straightforward.

90. For example, the Kai reference describes the process of forming a support pillar structure 20 (Petitioner's "dummy channel" (Pet. 39)) in support opening 19 by referencing Figures 5A-5L. Kai (Ex. 1015), 10:20-26 ("FIGS. 5A-5L illustrate structural changes during formation of a memory stack structure, an optional dielectric core, and a drain region in a memory opening, ... *[t]he same structural change occurs* simultaneously in each of the other memory openings 49 and *in each support opening 19.*"), 16:28-31 (support pillar structure 20 formed in support opening 19), Figs. 5A-5L, 6A, 6B.

91. Kai's process to form a support pillar structure 20 (i.e., dummy channel) includes at least forming a recess (Kai, 10:27-42, Fig. 5A), laterally recessing sidewalls of sacrificial material by isotropic etching (*id.*, 11:9-34, Fig. 5C), depositing and etching a blocking dielectric layer 52L on exposed surfaces of the support openings 19 to form blocking dielectric 52 (*id.*, 11:35-53, Fig. 5D), depositing and etching a floating gate material layer 54L in the annular recesses formed in the sidewalls to form a vertical stack of floating gate electrodes 54 (*id.*, 12:20-13:47, Figs. 5E, 5F), depositing a tunneling dielectric layer 56 and optional first semiconductor channel layer 601 before performing another anisotropic etch

(*id.*, 13:48-14:64, Figs. 5G, 5H), depositing a second semiconductor channel layer 602 (*id.*, 14:65-15:26, Fig. 5I), depositing and etching dielectric core layer 62L to form a dielectric core 62 (*id.*, 15:27-59, Figs. 5J, 5K), and depositing a doped semiconductor material to form a drain region 63 (*id.*, 15:60-16:12, Fig. 5L). Kai is clear: the “support pillar structure 20” is a combination of at least “a memory film 50,² a vertical semiconductor channel 60,³ a dielectric core 62, and a drain region 63 within each support opening 19.” Kai, 16:23-27.

92. Petitioner's Park reference describes an entirely distinct method to form a “dummy channel” (second channel structure 120b according to Petitioner (Pet. 39)), further confirming that forming a dummy channel structure is not “unusually simple” and this technology is not “particularly straightforward.” Park describes forming channel holes (Park, 11:47-58, 10:11-61), performing a silicon epitaxial growth process to form semiconductor patterns 110 (*id.*, 10:62-67), forming a dielectric layer structure 112 on the sidewalls of the channel holes (*id.*, 11:1-23), forming a channel layer 114 on top of dielectric layer structure 112 as

² Memory film 50 includes blocking dielectric 52, vertical stack of floating gate electrodes 54, tunneling dielectric layer 56. Kai, 14:57-60, Figs. 5G, 5H.

³ Vertical semiconductor channel 60 includes first semiconductor channel layer 601 and second semiconductor channel layer 602. Kai, 16:52-54, Figs. 5K, 5L.

well as forming a filling pattern 116 within the channel layer 114 (*id.*, 11:24-33), and forming a pad 118 disposed on top of etched-back portions of dielectric layer 112, channel layer 114, and filling pattern 116 (*id.*, 11:34-46). *See also id.* at 11:46-51, 6:19-26, Fig. 6.

93. Petitioner's other cited reference Kim also describes a complex process for forming a dummy channel. Kim discloses forming a dummy structure ("DS") within dummy holes ("DH") by making a lower semiconductor pattern ("LSP") by an epitaxial growth process, covering an inner sidewall with a vertical insulation layer ("VP") and an upper semiconductor pattern ("USP") using atomic layer deposition or chemical vapor deposition, filling the dummy hole with a buried insulation pattern ("VI"), and forming a pad ("PAD") on the upper portion of the dummy structure. Ex. 1017, Kim (Ex. 1017), [0047], [0073]-[0074]. Each of these dummy holes may have a diameter that "gradually increases" with increasing depth. *Id.*, [0070].

94. Given the complexities described above, including those highlighted in Petitioner's references and other mentioned references, forming a dummy channel structure is not unusually simple and 3D NAND technology is not particularly straightforward. As a result, Petitioner is in error by relying on a POSITA's "general knowledge" to supply the missing "dummy channel" limitation. As the Board found, "the lack of record support for Petitioner's reliance

on the knowledge of a person having ordinary skill in the art undermines Petitioner's obviousness showing." ID, 18-19. For this reason alone, Petitioner's arguments as to claims 2, 11-15, and 17 fail.

B. Nakajima and the POSITA's knowledge do not render obvious "forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening" (claims 7, 8, 14, 15).

95. Claim 7 recites "forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening." '254 Patent, cl. 7. Claim 8 depends from claim 7. Claim 14 depends from claim 11, which is valid for at least the reasons shown above with respect to the recited "dummy channel," as well as the reasons discussed below with respect to the "simultaneously etching" limitation. Also, claim 14 recites "forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening." *Id.*, cl. 14. Claim 15 depends from claim 14. "The first opening" recited in claims 7 and 14 is the opening through which the "through array contact (TAC)" is formed in independent claims 1 and 11, respectively.

96. Although Petitioner asserts that the '254 Patent claims "do not require further construction and should receive their plain and ordinary meaning" (Pet. 25), Petitioner alleges that Nakajima and knowledge of a POSITA render obvious the recited forming of "shallow recesses" under two different claim constructions: (1) by inherent "unintentional recesses" formed by the typical etching process (Pet.

49-50; Ex. 1003 ¶¶ 126-127), and (2) by an “intentional etch that forms actual recesses” (Pet. 50-52; Ex. 1003 ¶ 128). In my opinion, Petitioner fails to render obvious the “shallow recesses” limitation under either interpretation.

1. Ground 1 fails under Petitioner's first claim construction that requires “undetectable and unintentional recesses”

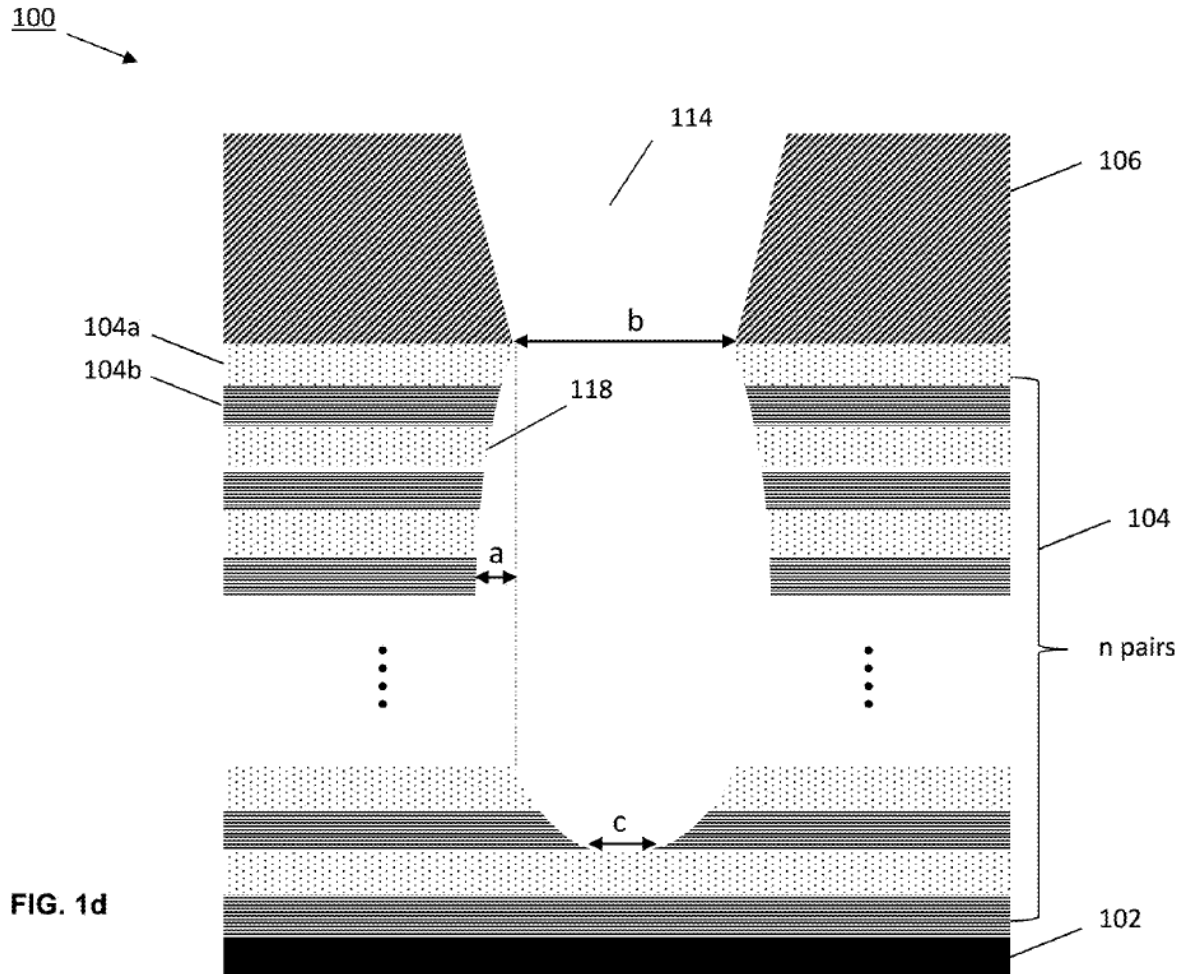
97. Petitioner and its expert assert that the '254 Patent does not support that the claims cover unintentional recesses, but “makes clear that these limitations relate to an intentional etch that forms actual recesses in the sacrificial layers.” Pet. 49 (citing Ex. 1001, 13:47-61, Fig. 3D); Lee, ¶126 (citing same). Petitioner and its expert cite no other intrinsic evidence to support this interpretation should be adopted. As such, Petitioner's arguments under this construction must fail.

98. In my opinion, Petitioner's arguments under this construction also fail on the merits. Petitioner asserts that “typical prior art etches ... were also known to result in lateral recesses in either the dielectric spacers or sacrificial layers.” Pet. 50. But for support, Petitioner cites a patent that says the opposite: “In 3D NAND memory, it is important to have an etching gas which etch both SiO₂ and SiN layers ... without selectivity.” Pet. 49 (quoting Ex. 1030, 2:59-67). In my opinion, a POSITA would understand that etching gasses “without selectivity” etch the layer stack evenly resulting in vertical sidewalls—without recesses. As such, etching would not inherently produce the claimed “shallow recesses” even under Petitioner's “undetectable and unintentional recesses” construction.

99. Petitioner relies on a lone statement from Cui (Exhibit 1031) that “it is a challenge to find” a gas that can etch “without selectivity” (Pet. 49-50), but that does not mean a POSITA would have understood Nakajima to use an etch gas with selectivity that would result in unintentional recesses (let alone be motivated to do so). Thus, as the Board correctly found, “because Petitioner’s evidence indicates that a smooth sidewall can be obtained with the proper etch gas, Petitioner has not shown that a non-smooth sidewall would have been understood by a [POSITA] as the result of etching in Nakajima.” ID, 24; *see, e.g.*, Ex. 1030, 24:3-11, 24:33-37.

100. Dr. Lee cites Exhibit 1030 for support that “typical prior art etches that effectively create a hole through the stack result in very small lateral recesses in either the dielectric spacers or sacrificial layers.” Ex. 1003 ¶ 127. The cited passage of 1030 says no such thing. Rather, the passage describes “a lack of etching a plurality of alternating layers of SiO and SiN layers in a 3D NAND application using a nontraditional hydrofluorocarbon etching gas.” Ex. 1030 2:56-58. “Although there are numbers of prior arts for SiO₂ etching with high selectivity to SiN, for certain applications, it is important to have an etching gas which can etch both SiO₂ and SiN layers...without selectivity.” Ex. 1030 2:59-63. “In another word, it is a challenge to find an etch gas that has similar high etch rates of SiO₂ and SiN in terms of getting a smooth sidewall of high aspect ratio holes in 3D

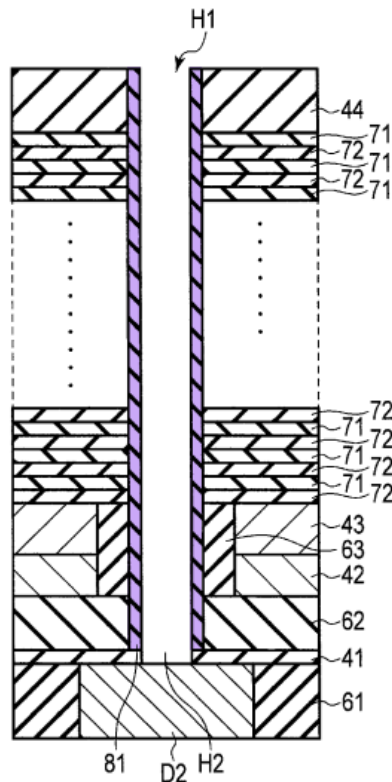
NAND memory.” Ex. 1030 2:63-67. This passage describes that it is important to have an etching gas without selectivity (which etches the layers evenly) and the patent itself purports to provide a solution. As Exhibit 1030 further explains, its proposed solution mitigates against sidewall bowing or barreling as depicted in Figure 1d, below. Ex. 1030, 18:38-63. Exhibit 1030 further describes bowing as undesirable, and does not motivate or inform a POSITA that such a pattern would be formed in Nakajima. Ex. 1030 18:42-44. Nor does it suggest forming a plurality of shallow recesses.



Ex. 1030, Fig. 1d.

101. In my opinion, Petitioner fails to provide any evidence that Nakajima uses a “typical etch” that allegedly inherently forms “lateral recesses in either the dielectric spacers or sacrificial layers.” *See* Pet. 49-50. Nor has Petitioner provided any evidence to establish that even if Nakajima used this “typical etch,” that Petitioner’s asserted “unintentional recesses [that] would naturally result” would be in the “sacrificial layers” as recited (rather than, for example, in the

insulation layers, or spread across both sacrificial and insulation layers). To the contrary, Nakajima's Figure 8 shows no such lateral recesses are formed when forming hole H1 through both the insulation layers 72 and sacrificial layers 71 (collectively, the layer stack 120)—the hole in which the C4 structure is fashioned. Nakajima, 7:28-31, 7:37-43, Fig. 8; *see* Pet. 32-34. And Petitioner's expert Dr. Lee admits that Nakajima's hole H1 is formed "extending *vertically* through the stack" using an anisotropic reactive ion etching (RIE) process, which "aims to remove material in a specific direction" i.e., the vertical direction without forming lateral recesses. Lee, ¶¶89, 123. Dr. Lee also admitted that the silicon oxide layer 81 (in purple below), which is deposited on the side wall of hole H1 consisting of insulation layers 72 and sacrificial layers 71 as seen below in Nakajima's Figure 10, has "the *same thickness* along the side wall." Lee Dep. Tr. 38:16-39:9. This supports that there are no inherent "shallow recesses" in the sacrificial layers 71, which if present, would result in varying thickness in the silicon oxide layer 81.



Nakajima, Fig. 10 (annotated).

102. As a result, in my opinion, Petitioner failed to meet its burden to show that a POSITA would understand that Nakajima inherently has non-smooth sidewalls. To the contrary, a POSITA reading Nakajima would understand that it has smooth sidewalls in the layer stack (i.e., no “shallow recesses” in the sacrificial layers).

2. Ground 1 fails under Petitioner's second claim construction that requires “intentional” formation of “actual recesses”

103. Petitioner next argues this limitation would have been obvious under Petitioner's second “interpretation” of the claim that requires the “intentional” forming of “actual recesses.” Pet. 50-52. Petitioner does not argue that Nakajima

discloses this limitation under this interpretation. *See id.*, 49-50; Lee Dep., 62:21-63:6 (Petitioner's expert admitting he relied on "knowledge of a POSITA" to disclose the "shallow recesses" limitation). Under this interpretation, Petitioner does not combine Nakajima with other references like Cui (Exhibit 1031) or Kai (Exhibit 1015). In my opinion, Petitioner has not argued, let alone established, that a POSITA would have combined Nakajima with Cui or would have used the disclosure of Cui to modify Nakajima. *See* Pet. 9, 51. Instead, Petitioner relies on the "knowledge of a POSITA" to supply the missing "shallow recesses" limitation and asserts that "[i]t was well known that an option for a TAC or other through-memory structures was to have a ribbed shape, that is, forming recesses in one of the stack layers." *Id.*, 50; *see* Lee Dep. Tr. at 62:14-63:6 (admitting reliance on knowledge of a POSITA to disclose the recited "shallow recesses"). Petitioner's argument fails.

104. Dr. Lee asserts that intentional lateral recesses in a hole "for a contact" was also known. Ex. 1003 ¶¶ 128-131. For support, Dr. Lee relies on Cui (Ex. 1031) and Kai (Ex. 1015). However, neither Cui nor Kai disclose or suggest forming shallow recesses by removing parts of the *sacrificial layers* abutting the sidewall of an opening for a "through array contact (TAC)" as required by claim 7.

105. **First**, Cui discloses “large recesses,” not the recited “shallow recesses.” According to Petitioner, Cui discloses an embodiment that—using Petitioner’s own words—“intentionally creates large recesses in the conductor layers.” Pet. 51 (citing Cui (Ex. 1031), Fig. 16A, 26:23-33 (“[A]n isotropic etch process can be performed to laterally recess the *insulating layers* (132, 232) with respect to the spacer material layers such as the first and second sacrificial material layers (142, 242).”)). Dr. Lee similarly testifies that Cui discloses “large recesses in the conductor layers (‘ribbed via cavity’).” Lee, ¶128. Cui’s “*large* recesses” are the opposite of the recited “*shallow* recesses.” Neither Petitioner nor Dr. Lee attempts to explain why Cui’s “large recesses” somehow render obvious forming “shallow recesses” in Nakajima. As the Board found, “Petitioner’s asserted combination would result in ‘large recesses,’ not the claimed shallow recesses.” ID, 26.

106. **Second**, Cui creates recesses in *insulating* layers, not the recited “*sacrificial* layers.” See Cui 26:23-27 (“[A]n isotropic etch process can be performed to laterally recess the insulating layers (132, 232) with respect to the spacer material layers such as the first and second sacrificial material layers (142, 242).”), Fig. 16A. The claims recite forming the “shallow recesses” by “removing parts of the sacrificial layers”—the claims do not recite removing part of the “insulating layers.” As seen below, Cui’s etching by design does not form

“shallow recesses” in the sacrificial layers 142 as required by the claims of the '254 Patent. *See id.*, 26:23-27, Fig. 16A.

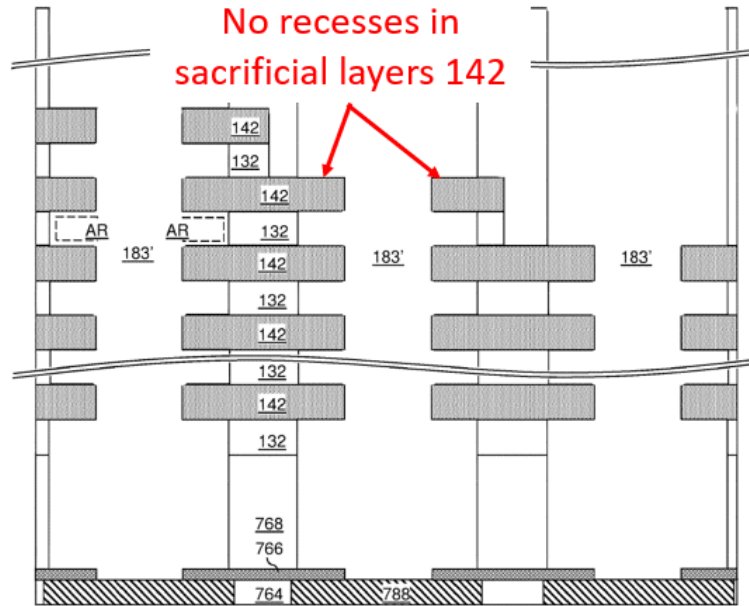


FIG. 16A

Cui, Fig. 16A (annotated).

107. **Third**, Kai does not make up for the deficiencies of Cui. As the Board recognized (ID, 26), Petitioner does not assert that Kai's disclosure of lateral recesses are part of its combination, that they disclose “shallow recesses” as recited in claim 7, or that they would result in the “rib regions” that Petitioner asserts to be the advantage exhibited by Cui's large recesses. *See* Pet. 50-52; Kai, 11:9-34. Further, Petitioner merely cites Kai for disclosure of forming “recesses in sacrificial **gates**.” Pet. 52 (citing Kai, 11:9-34). Petitioner says nothing about Kai disclosing forming recesses in the “sacrificial **layers**” of an alternating stack of dielectric and sacrificial layers for openings associated with a TAC as claimed

(because Kai does not disclose this). Moreover, Petitioner's cursory citation to Kai with a parenthetical stating "recesses in sacrificial gates" fails to establish that a POSITA would implement the claimed "shallow recesses" formed by "removing parts of the sacrificial layers" in Nakajima.

108. Also, Kai does not disclose a "ribbed via cavity" that provides "additional area for the dielectric liner" (Pet. 51) by "travel[ing] into and out of the lateral recesses" (Lee, ¶129)—the foundation of Petitioner's argument for why to modify Nakajima. *See* Pet. 51; Cui 27:40-57, Fig. 17A. Instead, Kai discloses that its recesses are filled with blocking dielectric 52 and a floating gate electrode 54 before tunneling dielectric layer 56 is deposited. Kai, 11:35-39, 12:20-23, 12:47-49, 12:56-61, Figs. 5C-5F. Kai says nothing about forming recesses in the sacrificial layers of an alternating stack of dielectric and sacrificial layers for openings associated with a TAC as claimed.

109. **Fourth**, Petitioner's provided motivation to modify Nakajima to form the claimed "shallow recesses" is "purely derived from hindsight," as the Board noted in its institution decision. ID, 26. Petitioner used hindsight to select the "ribbed via cavity" of Cui and allege that a POSITA would combine it with Nakajima because it "*serves the same purpose as the '254 Patent*, namely, providing additional area for the dielectric liner." Pet. 51. Petitioner cites the '254 Patent's disclosures and, in the next sentence, concludes: "Accordingly, in view of

the knowledge of a POSITA, it would have been obvious, and a POSITA would have been motivated to, create a ribbed via cavity in Nakajima's C4 holes." *Id.* That is hindsight.

110. As the Board noted, "Petitioner presents no particular advantage to the combination except through reference to the '254 patent," that is, hindsight. ID, 26. Neither Petitioner nor Dr. Lee explain why the hindsight motivation of "providing additional area for the dielectric liner" is advantageous, only that it creates a longer spacer—the same purpose of the lateral recesses in the '254 Patent. *Id.*; see Pet. 51-52; Lee, ¶¶129-130. In my opinion, Petitioner's improper reliance on the '254 Patent is underscored by its admission that the '254 Patent "provides virtually no explanation on creating these known rib regions." Pet. 52. Overall, Petitioner's motivation to combine fails because it is derived solely from the challenged '254 Patent—a fatal flaw that is dispositive for claim 7. Petitioner's assertions as to claims 8, 14, and 15 likewise fail by relying on the same assertions as claim 7.

3. Forming "shallow recesses" is not "unusually simple" and 3D NAND technology is not "particularly straightforward"

111. As with the "dummy channel" limitation, Petitioner's reliance on knowledge of a POSITA to supply the "shallow recesses" limitation missing in Nakajima is in error. Petitioner failed to demonstrate or support that the missing

limitation in question is **unusually simple and** the technology **particularly straightforward**.

112. First, as discussed above (Section VIII.A.3.a), 3D NAND technology is plainly not particularly straightforward.

113. Second, the recited forming “shallow recesses” in “sacrificial layers” during the manufacture of 3D NAND devices is not unusually simple because it requires, among other things, that “the lateral dimension of shallow recess” be “controlled by the etching rate and/or etching time.” ’254 Patent, 13:48-61; *see also* Ex. 2015, 2 (“An additional challenge is posed by the removal, in certain types of 3D NAND, of sacrificial layers in between the ‘steps’ of the staircase.”); Ex. 2018, 5-6 (describing the removal of nitride layers as part of a “complex” process); Ex. 2020, 1 (“because of miniaturization and complexity of structures,” 3D NAND “fabrication requires various highly selective etch processes not only for anisotropic etching but also for isotropic etching”). In my opinion, a POSITA would understand that forming shallow recesses cannot be simplified to etchant selection because control of the etchant chemistry, surrounding material, and complex process conditions are all key. *See, e.g.*, Ex. 1010, 1:17-28 (describing the high density and multi-tier 3D NAND flash memory structures “increase[] the complexity of the etch process for forming memory openings and the metal replacement process employed to form the word lines”), 6:10-13 (reaching depth

uniformity using reactive ion etching (RIE) “increases process complexity”); Ex. 2031, 8-9 (describing removal of nitride layers in the stack and forming wordlines as “a complex process”); Ex. 2012, 6 (describing forming wordlines as “particularly challenging because of the need to achieve void-free fill of complex, narrow, lateral structures with minimal stress on the memory stack”). Because of the isotropic nature of the etch (i.e., etching in all directions unlike an anisotropic (directional) etch), controlling the exact lateral recess distance is critical because over-etching could compromise the structural integrity of the device, while under-etching would fail to effectively create recesses. Ex. 2017, 3 (describing replacement-gate schemes as “particularly challenging because of the complex geometries involved”). Further, a POSITA would understand that it is increasingly complex and challenging to achieve consistent etch profiles at the top and bottom of the holes in a memory array as the height of 3D NAND increases, especially when trying to reach a certain shallow depth. Ex. 2016, 3-4, Fig. 3. Also, the choice of material for both the target and non-target layers must be highly compatible with the selective etch chemistry because any incompatibility could lead to non-uniform etching, structural defects, or failure to form the intended structure. *See, e.g.,* Kai, 11:16-20 (“For example, if the sacrificial material layers 42 include silicon nitride, the insulating layers 32 include silicon oxide, and the

epitaxial channel portions 11 include silicon, the isotropic etch process can include a wet etch process employing hot phosphoric acid as an etchant.”).

114. That a POSITA would be “generally knowledgeable about 3D NAND’s structure[and] how it is manufactured” does not impact this analysis. *See ID, 25.* If it did, a Petitioner could supply any missing limitation so long as a POSITA was “generally knowledgeable” about it. My understanding is that a missing limitation can be supplied by a POSITA’s knowledge only when the missing limitation is unusually simple and the technology is particularly straightforward. Petitioner and Dr. Lee have failed to establish either.

115. The recited forming of “shallow recesses” is a highly technical and complex process—not simple, let alone unusually simple. And 3D NAND technology is not straightforward, let alone particularly straightforward. Petitioner thus cannot rely on a POSITA’s general knowledge to supply the missing “shallow recesses” limitation.

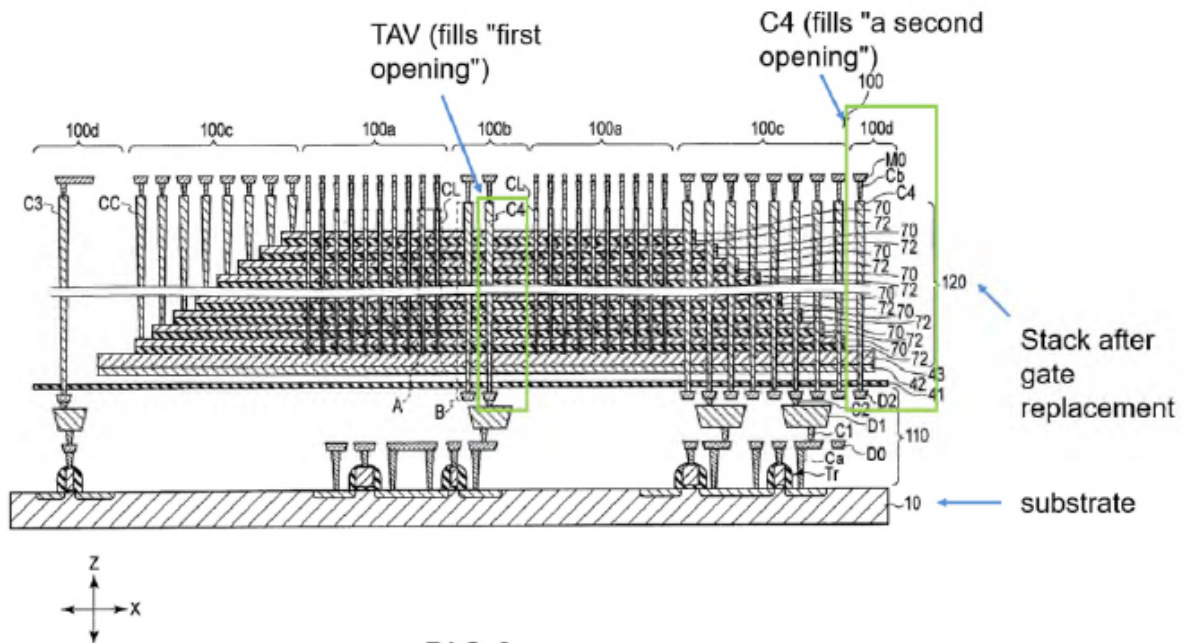
C. Nakajima and the POSITA’s knowledge do not render obvious “simultaneously etching a first opening through the stack and a second opening outside of the stack” (claims 11-15 and 17).

116. Claim 11 recites “simultaneously etching a first opening through the stack and a second opening outside of the stack.” ’254 Patent, cl. 11. Claims 12-15 and 17 depend from claim 11.

117. Petitioner asserted that this limitation is (1) disclosed by Nakajima or (2) obvious over Nakajima in view of the knowledge of a POSITA. Pet., 9, 41-43, 60.

1. Nakajima's "C4" depicted outside the stack in Figure 2 is an obvious error and thus not prior art

118. In my opinion, a POSITA reasonably considering Nakajima's entire disclosure would have noticed an *obvious error* in Figure 2 (below with Petitioner's annotations)—the component in area 100d identified as "C4" should be "C3."



Nakajima, Fig. 2 (as annotated by Petitioner); Pet., 42.

119. In my opinion, Nakajima's written disclosure would leave no doubt in a POSITA's mind that this is an obvious error. When describing Figure 2,

Nakajima states that “the contacts C3 are provided in the peripheral area 100d,” such that “[a]n upper end of a contact C3 is coupled to an interconnect M0 via a contact Cb.” Nakajima, 4:57-60; *see id.*, 3:59 (disclosing that “area 100d includes contacts C3,” not C4). Nakajima also discloses that “[t]he contacts C4 are provided in the layer stack 120 in the staircase area 100c on the other side and in the contact area 100b,” not the peripheral area 100d. Nakajima, 4:49-51, 3:23-30; *see id.*, Fig. 1. A POSITA would also recognize that there is no textual disclosure in Nakajima that describes contacts C4 in peripheral area 100d. In view of these disclosures, in my opinion a POSITA would readily understand the “C4” component identified in area 100d of Figure 2 to be an obvious error and mentally substitute the incorrect “C4” for the correct “C3,” as supported by Nakajima’s entire disclosure.

120. As a result, because Nakajima contains an obvious error, Nakajima does not disclose as prior art a contact C4 in the peripheral area 100d in Figure 2. I understand that, as a result, Petitioner thus cannot rely on the “C4” of area 100d as depicted in Figure 2 as prior art to form the basis of its obviousness ground for claim 11 of the ’254 Patent. *See Pet.*, 41-42, 60.

121. I further understand that Petitioner also cannot rely on the “C4” of area 100d in Figure 2 as prior art to support its obviousness positions regarding limitations [11.E], reciting forming “a second spacer on a sidewall of the second opening,” and [11.F], reciting “filling in the second opening to form a peripheral

contact.” *Id.*, 60. For both limitations, Petitioner relies on the “C4” of area 100d in Figure 2 and features of the C4 contact as described in Nakajima—disclosures that are not prior art for the above reasons. *Id.*, 60 (citing to analysis at *id.*, 41-44).

2. Nakajima does not disclose “a second opening outside the stack”

122. Petitioner alleges that Nakajima teaches forming holes H1 through its stack for its TAVs (C4), and that one C4 structure is outside of the stack. Pet., 41-42. Petitioner proposes that because one C4 is shown “outside the stack” in area 100d of Figure 2 below (as annotated by Petitioner), Nakajima discloses the claimed step of simultaneously etching one opening “through the stack” and another “outside of the stack.” Pet., 42. As the Board noted, “Petitioner requires us to assume that the step of etching H1 holes is performed when the structure has both stack and non-stack areas for hole etching; i.e., when the structure appears as in Figure 2 of Nakajima.” ID, 20. But Petitioner’s reliance on Figure 2 is in error. Petitioner’s arguments fail because they rely on an obvious error, as explained above. Even if that was not the case, Petitioner’s arguments also fail on the merits

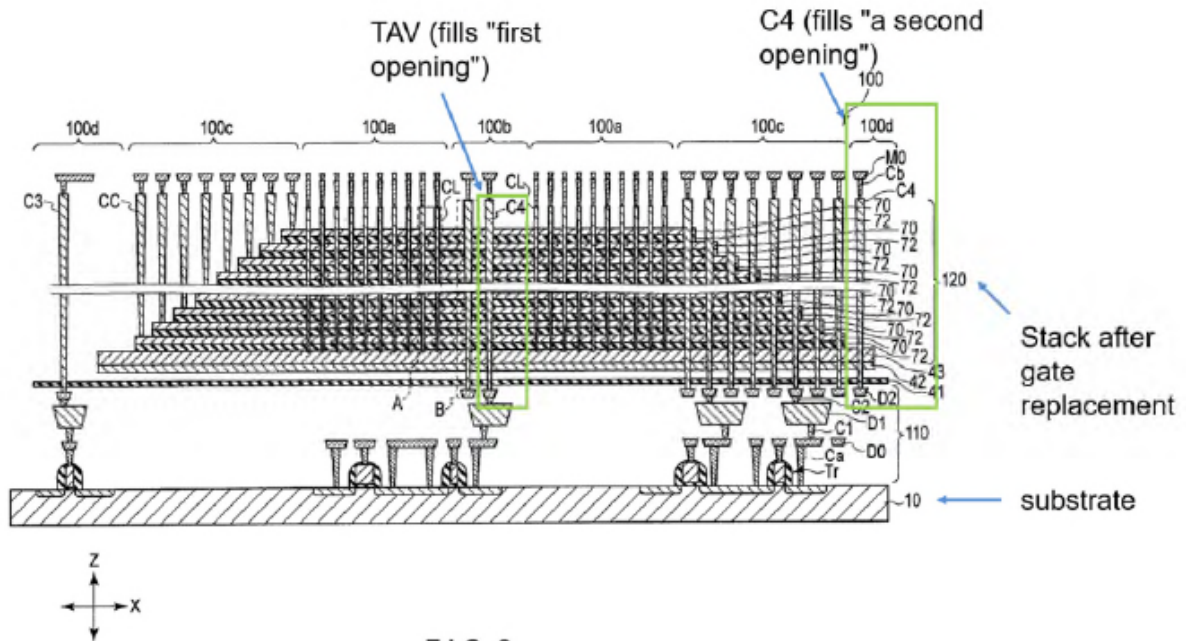
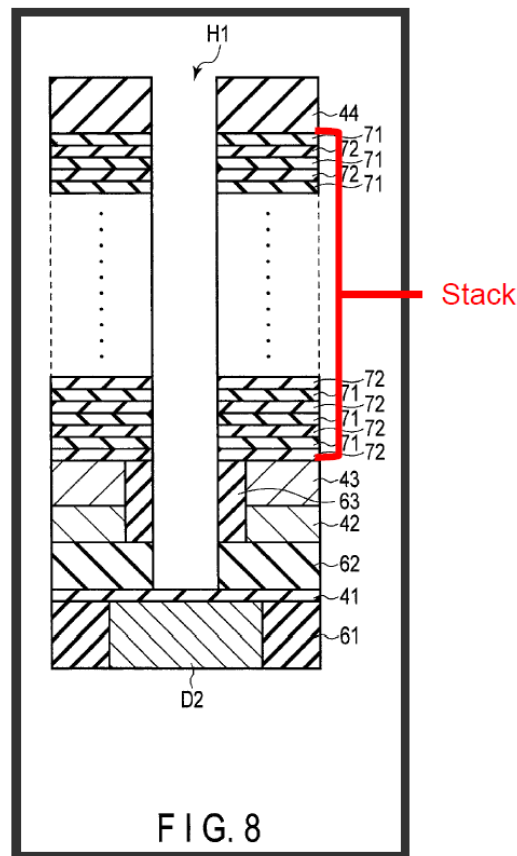


FIG. 2

Nakajima, Fig. 2 (as annotated by Petitioner); Pet., 42. A POSITA would recognize that the depiction of a C4 structure outside the stack in Figure 2 of Nakajima does not mean that the hole for that C4 structure was etched “outside the stack” during Nakajima’s manufacturing process. Nakajima’s express disclosure, which Petitioner ignores and does not address, describes the opposite. Nakajima, 7:37-39, 7:41-43.

123. As a POSITA would recognize, Nakajima discloses that all H1 holes for the C4 structures are etched ***through the stack***. See ID, 20 (“We agree with Patent Owner that Petitioner has not shown that Nakajima’s disclosure of a single step of creating H1 holes would be understood as resulting from simultaneous etching of a hole through the stack and a hole outside the stack.”). Nakajima’s Figure 8, reproduced below, illustrates that the hole H1 is always formed through

the stack—i.e., the alternating layers 71 and 72 that comprise “the stack.” *See also* Nakajima, Fig. 7 (illustrating layer stack 120 comprises alternating layers 71 and 72), 7:28-31 (“[A]lternately stacking the insulation layer 72 and the sacrifice layer 71 is repeated, so that the layer stack 120 ... is formed.”); Pet., 28 (identifying layer stack 120 as the recited “stack” for limitation 1.A), 59 (citing to limitation 1.A for limitation 11.A).



Nakajima, Fig. 8 (annotated). According to Nakajima, “hole H1” is “formed in the insulation layers ... *and the layer stack 120* as shown in FIG. 8.” *Id.*, 7:37-39.

The “hole H1 penetrates the insulation layers ... *and the layer stack 120*, to reach the silicon nitride layer 41.” *Id.*, 7:41-43.

124. Petitioner ignores that a C4 structure formed through the stack may nevertheless be located outside the stack in the final structure shown in Figure 2 if, for example, portions of the stack are removed *after* holes H1 are etched through the stack. *See* Nakajima, 7:37-43. Petitioner's reliance on Figure 2 (which is silent about the timing of when the H1 holes are formed) is in error because it contradicts Nakajima's express teachings about forming H1 through the stack (which Petitioner ignores). *See* Nakajima, 7:37-43. A POSITA reading Nakajima would understand that Nakajima's holes H1 are formed through the stack because Nakajima describes that the layer stack 120 (layers 71 and 72), acts as a framework for forming C4 components, including, for example, forming silicon oxide layer 81 on the inner surfaces of the layer stack 120. Nakajima, 7:44-49 (“Next, the silicon oxide layer 81 is formed *on the inner surfaces of the layer stack 120* and the insulation layers 44, 62, and 63 in the hole H1, and on the silicon nitride layer 41, as shown in FIG. 9. The silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1.”), Fig. 9. In contrast, Nakajima describes that holes for contacts CC and C3 are formed “in the silicon oxide layer 65 by the RIE method using a mask layer, as shown in FIG. 29”—i.e., etched outside of the stack. Nakajima, 17:38-40, Fig. 29; *see* Pet., 43 (citing same).

125. As the Board found, Petitioner fails to disclose this limitation because the cited two C4 holes are both formed *through the stack*. ID, 20-21. A POSITA would recognize that Nakajima does not disclose or suggest forming hole H1 outside the stack, let alone doing so simultaneously with an opening through the stack. Petitioner cannot contest this point given it admits “Nakajima only discloses one step for creating the H1 holes” and “Nakajima only discloses one set of steps for forming the C4 contacts.” Pet., 42 (citing the same portions of Nakajima referenced above); Lee, ¶112 (“Nakajima discloses only one step for creating the H1 holes for the C4 structures.”). As a result, Petitioner’s remaining arguments for why Nakajima discloses, or alternatively why it would have been obvious, to etch these two C4 holes “simultaneously” also fail. See Pet., 42-43. The fact that Nakajima’s two C4 holes are both formed *through the stack* remains true even if they are formed at the same time.

3. Nakajima and the POSITA’s knowledge do not disclose or render obvious “simultaneously etching”

126. Petitioner argues that (1) Nakajima’s two C4 structures are formed at the same time, and (2) it would have been obvious to form the two C4 structures at the same time. Pet., 42. Petitioner is incorrect on both accounts.

127. **First**, Petitioner argues that “[i]t would have been understood” that Nakajima’s H1 holes for the two C4 structures are formed at the same time because Nakajima only discloses one step for forming H1 holes and one set of steps for

forming C4 contacts. Pet., 42. But this reasoning fails because, as mentioned, the contact Petitioner relies on in Figure 2 marked “C4” is actually a “C3” contact based on Nakajima’s disclosure. *See* Section VIII.C.1 above; Nakajima, 3:59, 4:57-58, 4:49-51. By Petitioner’s own logic, a C4 and C3 contact would not be formed at the same time. *See* Pet., 42 (alleging that C4 holes would have been formed at the same time because they are the same type). Moreover, Nakajima describes that contacts C4 are formed *before* slits in the layer stack 120 and removing sacrifice layers 71 (Nakajima, 7:5-8:23), whereas contacts C3 are formed *after* those steps (*id.*, 17:19-45, 18:1-7).

128. **Second**, Petitioner argues that “forming both [C4] holes simultaneously would have been obvious, because it would reduce processing time.” Pet., 42-43. According to Petitioner, “all the structural elements of the C4s are the same, so using a single set of processing steps to make all C4s would be straightforward.” Pet., 42. This supports Patent Owner’s position. Etching processes generally etch different materials at different rates. Thus, “using a single set of processing steps to make all C4s” require the holes to be etched through the same material—e.g., the stack. Under Petitioner’s incorrect interpretation of Nakajima, simultaneously etching one C4 hole “through the stack” and another C4 hole “outside the stack” using “a single set of processing steps” would result in the C4 structures having *different* depths, contrary to Figure 2 of Nakajima. Petitioner

does not address this at all. Moreover, even if one of the C4 holes were formed outside the stack (which is not the case), simultaneous etching would not save processing time because the CC/C3 holes are later etched outside the stack. Nakajima, 7:5-8:23 (C4 formed before slits and removal of sacrifice layers 71), 17:19-45, 18:1-7 (CC/C3 etched through silicon oxide layer 65 after those steps).

129. **Third**, Petitioner is in error by relying on CC/C3 contacts to argue the C4 contacts would be formed at the same time. *See* Pet., 43. Petitioner states “Nakajima discloses etching contact CC (which travel partially through the stack) and C3 (which do not travel through the stack) at the same time.” *Id.* At the outset, Petitioner is wrong about contact CC traveling “partially through the stack.” Contact CC (in purple below) stops at the staircase—it does not “travel partially through the stack” as Petitioner alleges. *See id.*; Nakajima, 17:38-45 (“The holes for the contacts CC penetrate the silicon oxide layer 65, *to reach each terrace.*”), Fig. 29.

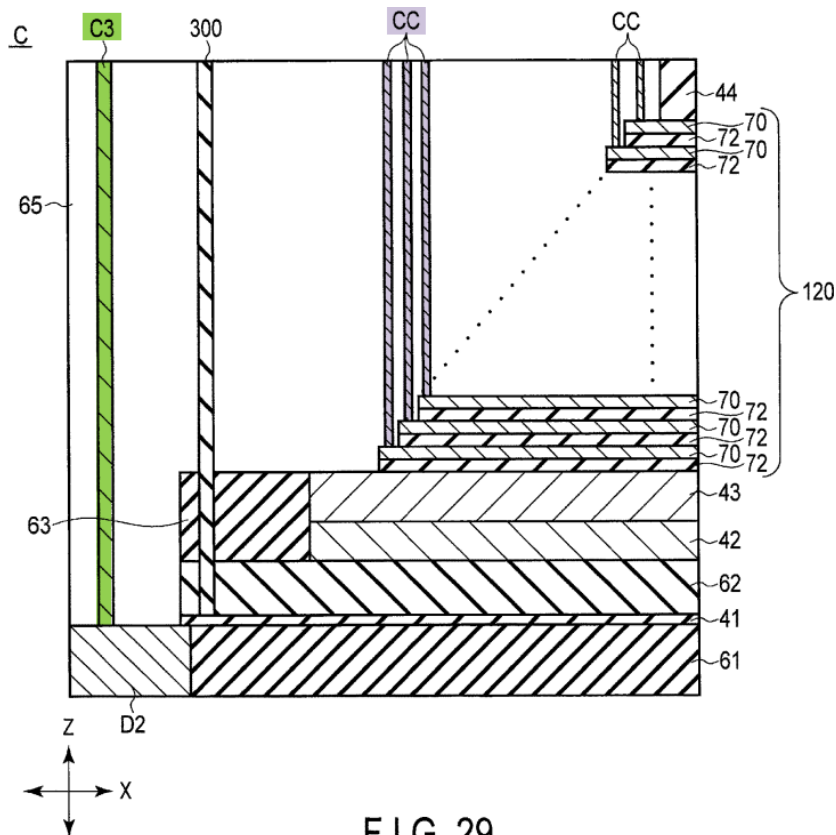


FIG. 29

Nakajima, Fig. 29 (annotated). And as Petitioner admits, contact C3 (in green above) “do[es] not travel through the stack.” Pet., 43; *see also* Nakajima, 17:37-45. At best, Nakajima discloses that the two contacts CC and C3 are formed *outside the stack* at the same time. And Petitioner relies on C4 contacts—not CC/C3 contacts—to allegedly disclose the limitation (which fails for the above reasons). *See* Pet., 41-43.

130. In addition, as shown in annotated Figure 2 above, when C3 (green) and CC (purple) are etched “simultaneously” through the same material (according to Petitioner), they end up with different depths because the etchant used cannot penetrate through the layer stack under CC (but absent from C3). As a result, the

hole for C4 stops when it hits the staircase, while C3 continues to be etched. Because the C4 structures are all etched to the same depth, a POSITA would understand that they are all etched through the same material—namely, the stack, as Nakajima expressly discloses. Nakajima, 7:37-39, 7:41-43.

131. **Fourth**, Petitioner's conclusory assertion that "Nakajima's process is already able to etch the C4 holes in various places, regardless of whether the holes extend through all or only a portion of the stack" is unsupported attorney argument and contrary to Nakajima's explicit disclosure. *See* Pet., 42-43. As addressed above, Nakajima only discloses etching holes H1 for the C4 structures through the stack—portions of the stack are subsequently removed. *See* Section VIII.C.2 above.

132. **Fifth**, Petitioner relies on two patent publications Tessariol and Mushiga to argue it would be obvious to modify Nakajima's two C4 holes to be etched at the same time, stating "it was known and routine to etch holes at the same time through either the full stack or only small portions of the stack, because it saves processing time." Pet., 43 (citing Tessariol (Ex. 1023) and Mushiga (Ex. 1010)). A POSITA would recognize that neither publications support this proposition.

133. A POSITA would recognize that Tessariol, just like Nakajima, merely discloses two holes that are both formed "through the stack," not the claimed

“simultaneously etching” of one opening through the stack and another outside the stack. Ex. 1023, [0037]. In particular, as seen below in Figure 9, Petitioner pointed to the dummy-structure openings 56 (blue) and via openings 54 (green) that are both formed *through the stack* (red box):

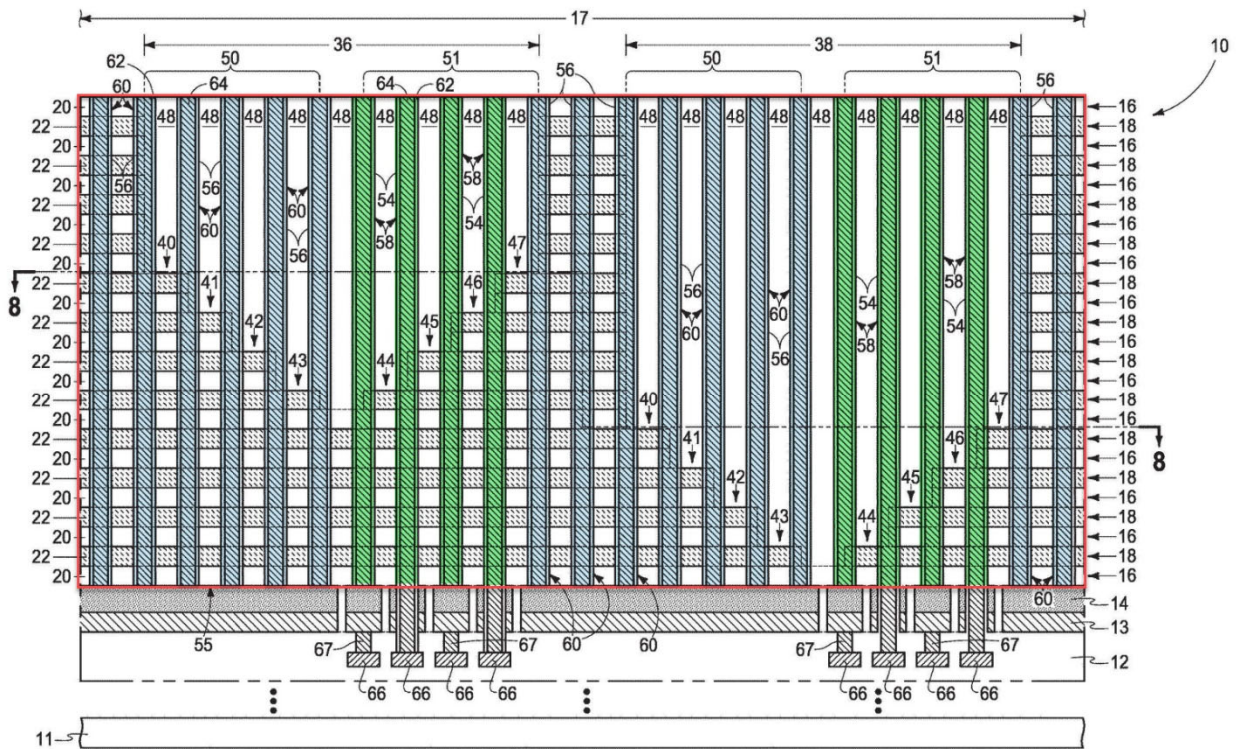


FIG. 9

Ex. 1023, Fig. 9 (annotated); *see* Pet., 43 (citing Ex. 1023, [0037], Fig. 9). Petitioner confirmed as much, admitting that Tessariol supports that “it was known and routine to etch holes at the same time through either *the full stack* or only small *portions of the stack.*” Pet., 43. Thus, like Nakajima, Tessariol only discloses etching different holes “through the stack.”

134. A POSITA would also understand that Mushiga does not support Petitioner's premise that "it was known and routine to etch holes at the same time through either the full stack or only small portions of the stack, because it saves processing time." Pet., 43 (citing Mushiga (Ex. 1010)). Petitioner cites Figure 5 of Mushiga, which shows structures 588 inside and outside the stack. *Id.* Petitioner argues structures 588 are formed "at the same time," but Mushiga does not disclose anything about the timing of forming the cavities that become structures 588—let alone teach that the cavities are etched "simultaneously." Pet., 43 (citing Mushiga, Fig. 5, 10:31-58). Mushiga at most discloses the timing of the formation of the cavities in relation to the formation of the conductive layers 146, 246, but this does not teach simultaneous formation of cavities both through and outside the stack. Mushiga, 10:49-57. By Petitioner's reasoning, all of the semiconductor devices 600 shown in Figure 4 are also formed "simultaneously" by a single process merely because they are discussed at the same time, including an two tiers of alternating stacks of insulating layers (132, 232), electrically conductive layers (146, 246), and memory stack structures 58. Mushiga, 8:62-9:7, Fig. 4.

135. Neither Tessariol nor Mushiga remedy the fact that Petitioner relies on Nakajima's two C4 components that are both formed *through the stack*. See Section VIII.C.2 above. Thus, even if Petitioner were correct that these references

support that “forming both holes simultaneously would have been obvious” (not the case), Petitioner's position remains fatally flawed. *See* Pet., 42

4. “Simultaneously etching” multiple openings is not “unusually simple” and 3D NAND technology is not “particularly straightforward”

136. In my opinion, the missing “simultaneously etching” limitation is neither unusually simple nor involves particularly straightforward technology such that the general knowledge of a POSITA could supply it. Petitioner never alleged that to be the case here, much less provided adequate support for using knowledge of a POSITA to supply a limitation missing from Nakajima.

137. In my opinion, a POSITA would agree with the Board when it found the claimed “complex semiconductor manufacturing processes,” including “wet etching, and/or dry etching, such as DRIE,” are not “unusually simple” and that 3D NAND technology is not “particularly straightforward.” *See* ID, 18-19 (regarding “forming a dummy channel structure extending vertically through the stack” as recited in claims 2, 11-15, and 17). As discussed above in my declaration, 3D NAND technology is plainly not “particularly straightforward.” *See* Section VIII.A.3.a. A POSITA would understand that etching openings through the stack cannot become unusually simple by “simultaneously” performing an additional etching outside the stack.

138. A POSITA would also recognize that etching channels in 3D NAND is described as “the most critical and challenging step”—“[m]ore than a trillion holes must be *etched simultaneously* and uniformly on every wafer.” Ex. 2012, 6. Numerous problems can arise if etching holes through the stack does not go well, including an “incomplete etch wherein some holes don’t reach the bottom, bowing, twisting, and CD variation between the top and bottom of the stack,” which can lead to “shorts, interference between neighboring memory strings, and other performance issues.” Ex. 2012, 6; Ex. 2017, 2; *see also* Ex. 2018, 5, 8; Ex. 2019, 2-3.

139. In addition, a POSITA would recognize that etching channels outside of the stack is a complicated process. For example, the etching of vias that extend down to each stairstep is “yet another very difficult and new process that must be managed to successfully mass produce 3D NAND. Ex. 2022, 2; Ex. 2012, 4, Figure 1 (describing contacts etched outside of the stack as part of “some of the most challenging and critical deposition and etch processes”). “The vias must land precisely on their designated stairstep and not on any others, or the wordlines will be shorted to each other,” yet if there is no solid connection it “may prevent that entire wordline from working properly.” Ex. 2022, 2; Ex. 2012, 7 (“Extreme accuracy is required to maintain the stair CD, thus avoiding misaligned contacts. If the CD for a pad is off by a few percent, that error will propagate through

subsequent pads defined within the same lithography pass.”); Ex. 2028, 2 (describing connecting contacts to the staircase as one of “the high priority process challenges with 3D NAND”). Moreover, “the process of getting to the wordlines rivals the complexity of making the vertical bit strings themselves.” Ex. 2022, 2. And Nakajima describes that contacts CC/C3 formed outside the stack use the same RIE etching method and mask process that the Board found to support that forming “dummy channels” was not “unusually simple.” Nakajima, 17:38-45; ID, 18-19.

140. In my opinion, the recited “simultaneously etching” limitation is a highly technical and complex process—not simple, let alone unusually simple. And 3D NAND technology is not straightforward, let alone particularly straightforward. Petitioner thus cannot rely on a POSITA’s general knowledge to supply the missing “simultaneously etching” limitation. Petitioner’s arguments as to claims 11-15 and 17 fail for this reason alone.

IX. CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on August 15, 2025, in Arden Hills, Minnesota.

Stephen Campbell

Stephen Campbell