

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00035
U.S. Patent No. 11,450,604
Issue Date: September 20, 2022

Title: STAIRCASE STRUCTURE IN THREE-DIMENSIONAL
MEMORY DEVICE AND METHOD FOR FORMING THE SAME

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,450,604**

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37 C.F.R. §42.108(a).....5

LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,450,604 to Wang et al. (the “’604 patent”)
1002	File History of U.S. Patent No. 11,450,604 to Wang et al.
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	<i>Curriculum Vitae</i> of Dr. Sanjay Banerjee
1005	U.S. Patent No. 10,515,973 to Thimmegowda et al. (“Thimmegowda”)
1006	U.S. Patent Publ. No. 2019/006275 to Kobayashi et al. (“Kobayashi”)
1007	U.S. Patent Publ. No. 2016/0027730 to Lee (“Lee”)
1008	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1009	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1010	U.S. Patent Publ. No. 2021/0193676 to Zhang et al. (“Zhang”)
1011	U.S. Patent No. 9,029,938 to Nakaki (“Nakaki”)
1012	Aritome, “NAND Flash Memory Technologies” (2016)
1013	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers (2017)
1014	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)

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1015	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.’s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1016	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL
1017	U.S. Patent Publ. No. 2017/0256551 to Lee
1018	Michelsoni, “3D Flash Memories” (2016)
1019	U.S. Patent Publ. No. 2019/0139977 to Lee
1020	INTENTIONALLY OMITTED
1021	U.S. Patent No. 11,239,248 to Xu et al.
1022	U.S. Patent No. 11,217,601 to Luo et al.
1023	U.S. Patent No. 12,087,572 to van Schravendijk et al.
1024	U.S. Patent Publ. No. 2021/0193536 to Kris et al.
1025	U.S. Patent No. 10,475,737 to Tang et al.
1026	U.S. Patent No. 10,381,369 to Kim et al.
1027	Certified English Translation of Chinese Patent Application Publ. No. CN108766971 to Liu
1028	Chinese Patent Application Publ. No. CN108766971 to Liu
1029	U.S. Patent Publ. No. 2012/0070944 to Kim et al.
1030	U.S. Patent No. 10,026,692 to Chen

I. INTRODUCTION

Petitioner Micron Technology, Inc. (“Micron” or “Petitioner”) respectfully requests *Inter Partes* Review (“IPR”) of claims 1-5, 8-13, and 15 (“the Challenged Claims”) of U.S. Pat. 11,450,604 (Ex. 1001, the “’604 patent”). There is more than a reasonable likelihood Petitioner will prevail on at least one claim.

The ’604 patent’s title is “Staircase Structure in Three-Dimensional Memory Device and Method for Forming the Same.” Most elements of the Challenged Claims are conventional for 3D NAND memory devices (*e.g.*, “a memory array structure,” “a staircase structure,” “a plurality of stairs,” etc.), which existed long before the ’604 patent’s priority date.

The alleged novelty of the ’604 patent, as its title suggests, focuses on a “staircase structure” in a 3D NAND device that comprises two primary elements: (1) a so-called “bridge”; and (2) thin conductive fingers connected thereto. *See* §V.B. But neither concept was new.

Thimmegowda (Ex. 1005) disclosed using a wordline bridge in 3D NAND memory years before the ’604 patent’s priority date. *See* §VI.A. And using thin conductive fingers as landing pads for wordline contacts was disclosed even earlier by both Lee (Ex. 1007) and Kobayashi (Ex. 1006). *See* §VI.B and §VI.C.

Modifying Thimmegowda’s bridge in accordance with the teachings of either Lee (Ground 1) or Kobayashi (Ground 2) renders the Challenged Claims obvious,

and doing so solves an alleged punch-through problem and provides other benefits. Indeed, as the Supreme Court has recognized, “if a technique has been used to improve one device, and a [POSITA] would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). That is precisely the case here.

In sum, because the Challenged Claims recite well-known prior art 3D NAND elements, and are nothing more than a routine, predictable combination of those elements, Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable as obvious.

II. REQUIREMENTS FOR INTER PARTES REVIEW

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies the ’604 patent is available for IPR and no law bars Petitioner from requesting IPR of the Challenged Claims on the grounds identified herein.

B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a))

Pursuant to 37 C.F.R. §§42.8(b)(3-4) and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	Back-Up Counsel
Jeremy Jason Lang Registration No. 73,604 (jlang@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025-1015 T: 650-614-7400; F: 650-614-7401	Travis Jensen Reg. No. 60,087 (tjensen@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025-1015 T: 650-614-7400; F: 650-614-7401 Jared Bobrow <i>Pro Hac Vice</i> to be submitted (jbobrow@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025-1015 T: 650-614-7400; F: 650-614-7401

Petitioner consents to service by electronic mail at the following addresses:

PTABDocketJJL2@orrick.com, T61PTABDocket@orrick.com,
PTABDocketJ3B3@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to
37 C.F.R. §42.10(b), Petitioner attaches a Power of Attorney.

C. Notice of Real-Parties-in-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Micron Technology, Inc., and its subsidiaries, including Micron Consumer Products Group LLC, are the real-parties in interest. No other parties exercised or could have exercised control over this petition. No other parties funded or directed this Petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

D. Notice of Related Matters (37 C.F.R. §42.8(b)(2))

According to USPTO assignment records, the '604 patent is currently assigned to Yangtze Memory Technologies Co., Ltd. (“YMTC” or “Patent Owner”). On July 12, 2024, YMTC asserted the '604 patent and U.S. Patent Nos. 10,672,711, 10,879,164, 10,879,254, 10,886,291, 11,101,276, 11,145,666, 11,482,532, 11,568,941, 11,581,322, and 12,010,838 against Micron (the “YMTC2 case”). On August 21, 2024, the litigation was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”).

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Patent	PTAB Proceeding	Wave
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	

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Patent	PTAB Proceeding	Wave
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	
10,672,711	IPR2025-TBD	Wave 3 Petitions
10,879,164	IPR2025-TBD	
10,879,254	IPR2025-00034	
10,886,291	IPR2025-TBD	
11,101,276	IPR2025-TBD	
11,145,666	IPR2025-TBD	
11,450,604	IPR2025-00035	
11,482,532	IPR2025-TBD	
11,568,941	IPR2025-TBD	
11,581,322	IPR2025-TBD	
12,010,838	IPR2025-TBD	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a).

E. Fee for *Inter Partes* Review

The USPTO is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

F. Proof of Service

Petitioner has attached proof of service of this Petition on the Patent Owner at the correspondence addresses of record for the '604 patent.

III. IDENTIFICATION OF GROUNDS AND CLAIMS BEING CHALLENGED (§42.104(B))

This Petition assumes the earliest possible priority date (PCT filing date) of June 5, 2020 (“Priority Date”).

Petitioner relies on the following references: (1) U.S. Pat. 10,515,973 (Ex. 1005, “Thimmegowda”); (2) U.S. Pub. 2016/0027730 (Ex. 1007, “Lee”); and (3) U.S. Pub. 2019/0006275 (Ex. 1006, “Kobayashi”).

Petitioner asserts two grounds:

Ground 1: Claims 1-5, and 8-13 are obvious in view of Thimmegowda, Lee, and a POSITA’s knowledge.

Ground 2: Claims 1-5, 8-13, and 15 are obvious in view of Thimmegowda, Kobayashi, and a POSITA’s knowledge.

The Declaration of Dr. Sanjay Banerjee (Ex. 1003, “Banerjee”) supports these grounds.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There are No Grounds for a §314 Discretionary Denial in this Case

There is a pending district court action involving the '604 Patent. Petitioner submits that it “presents compelling evidence of unpatentability” and the Board should not discretionarily deny institution. 6/21/22 Interim Procedure, 2, 4-5. Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential).

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24, 7 (PTAB June 16, 2020) (informative); *Fintiv*, 6-9, 12 (similar).

2. Proximity of the Court’s Trial Date

On September 18, 2024, the district court entered a scheduling order which set a trial date of June 15, 2026. *See* Ex. 1008. As a result, if IPR proceedings are instituted, they should be completed before the scheduled trial date. *See also* Ex. 1009 (statistics indicating that it takes on average 48.9 months to reach trial in district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

Regarding the Co-Pending Litigation, to date, the parties and the district court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. *See* §II.B. Virtually no progress has been on the Wave 3 patents (which includes the '604 patent). The parties are over a month away from completing the exchange of contentions for the Wave 3 patents (from the YMTC2 case) and have not taken any depositions in the entire Co-Pending Litigation. Fact discovery is in its infancy. No claim construction positions have been exchanged for the Wave 3 patents, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution*, 10-11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv*, 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner—asserting 149 claims for the Wave 3 patents. Ex. 1015. Petitioner proceeded with diligence, starting the filing of eleven petitions approximately three months after being served with the YMTC2 complaint. Ex 1016. This also weighs strongly in favor of institution.

4. Issue Overlap

Should the Board institute, Micron stipulates that it will not advance in District Court any ground asserted in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution*, 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. Thus, this factor also weighs in favor of institution.

B. Denial Under §325(d) Is Unwarranted

The two-part *Advanced Bionics* framework weighs against §325(d) denial. At the outset, it bears noting that all '604 patent claims resulted from a first-action allowance. *See generally* §V.C; Ex. 1002.

As in *Advanced Bionics* Part I, none of the references in Petitioner's grounds was before the Examiner. Ex. 1002. With respect to Lee, Patent Owner cited TW201605015, which is a Taiwanese foreign language version of Lee, in an IDS. *See id.*, 180. But Patent Owner did **not** submit an English language counterpart or translation. *Id.* Thus, Lee was not before the Examiner. *See* 37 C.F.R.

§1.98(a)(3)(ii) (information in an IDS shall include “the translation if . . . readily available”).

This is analogous to *Mianyang BOE Optoelectronics Tech. Co. Ltd., et al., v. Samsung Display Co. Ltd.*, where the patent owner submitted a Japanese language version of the Kimura reference, which formed the basis of petitioner’s IPR challenge. IPR2023-00941, Paper 12 (Institution Decision), 60-62 (PTAB Dec. 15, 2023). In its §325(d) analysis, the Board in *BOE* stated that “it appears that no English translation of the full document was ever provided to the Examiner.” *Id.* The Board explained that “[d]espite the fact that the figures of JP Kimura appear to be the same as the figures in Kimura, we find that the quality of the substantive disclosures to the Office of JP Kimura in Japanese, together with the English abstract [], are not the same as the version of Kimura asserted in this case” and “would [not] convey a substantially equal understanding of the disclosures.” *Id.* On this basis, the Board concluded “Kimura was not previously considered by the Office.” *Id.* The same result should inure here where Patent Owner chose not to submit an English translation, even though Lee had published in English and was readily available to Patent Owner.

Regardless, at Part II, to the extent any disclosure similar to Thimmegowda, Kobayashi, or Lee was before the Examiner, the Examiner erred by failing to reject the claims in light of such references. “[I]f the record of the Office’s previous

consideration of the art is not well developed or silent, then a petitioner may show the Office erred by overlooking something persuasive.” *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, 10 (PTAB Feb. 13, 2020) (precedential).

The record here is silent as to what, if any, substantive consideration the Examiner gave reference other than Zhang (Ex. 1010), which is the only reference even mentioned by the Examiner. *See* Ex. 1002, 657-660. Even then, it was not the basis for rejection because all ’604 patent claims resulted from a first action allowance. *See generally* §V.C; Ex. 1002, 657. Accordingly, the record is not well-developed, which favors the Board not exercising discretion to deny institution. *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8, 22-23 (factor (c)) (PTAB Dec. 15, 2017).

To the extent any subject matter in the asserted references was before the Examiner, this Petition demonstrates the Examiner erred by overlooking such teachings. *Becton*, 24-25 (factor (e)). In particular, the Examiner stated for all independent claims that “the closest prior art of record [was] Zhang et al. to US 2021/0193676.” Ex. 1002, 658-660. Regarding claim 1, the Examiner stated that Zhang “failed to teach that the stair comprises a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure, and a dielectric portion at a same level and in contact with the conductor portion and

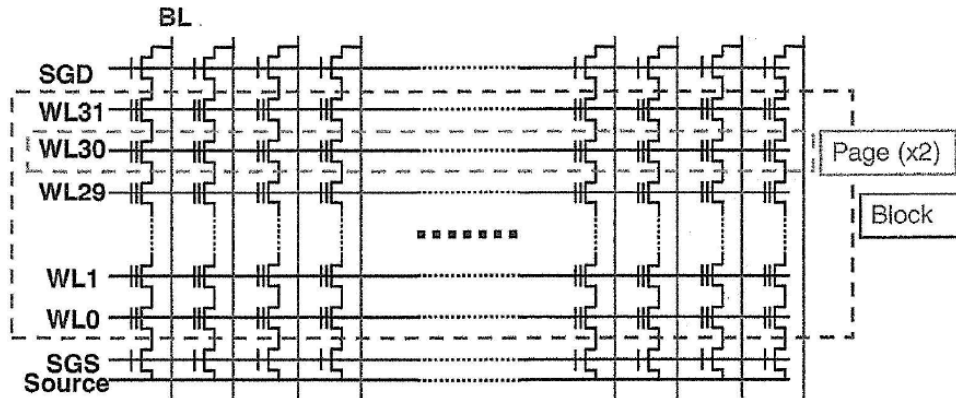
Moreover, this Petition provides additional evidence not before the Examiner, *e.g.*, the testimony of Dr. Banerjee explaining how a POSITA would have understood the teachings of Thimmegowda in view of Lee and Kobayashi. *See* §§IX and X; *Becton*, 25-28 (factor (f)). The Examiner was apparently unaware of a POSITA's understanding of implementing the conductive fingers of Lee and Kobayashi with a bridge structure, *e.g.*, Thimmegowda. Thus, the Petition includes evidence material to patentability the Examiner did not consider.

Because the Examiner was unaware of and/or overlooked specific teachings in Lee that disclose the very thing the Examiner considered the Challenged Claims' point of novelty, the Board should not deny institution under §325(d).

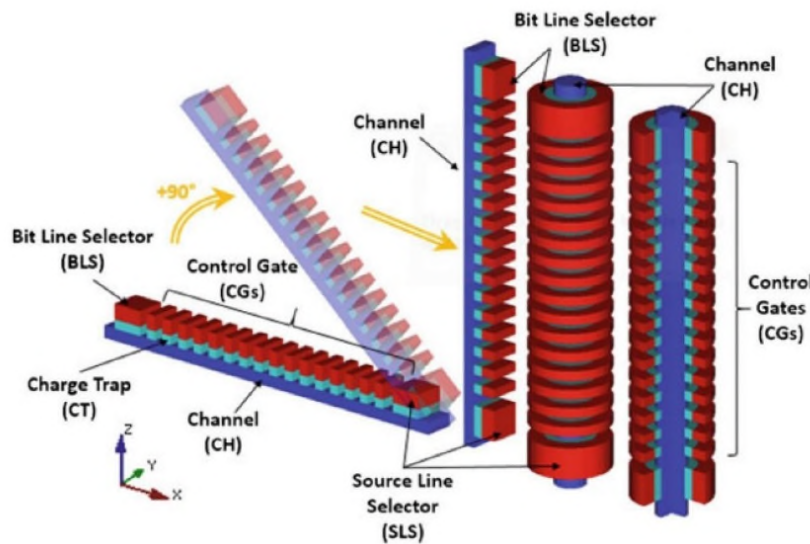
V. THE '604 PATENT

A. Technology Background

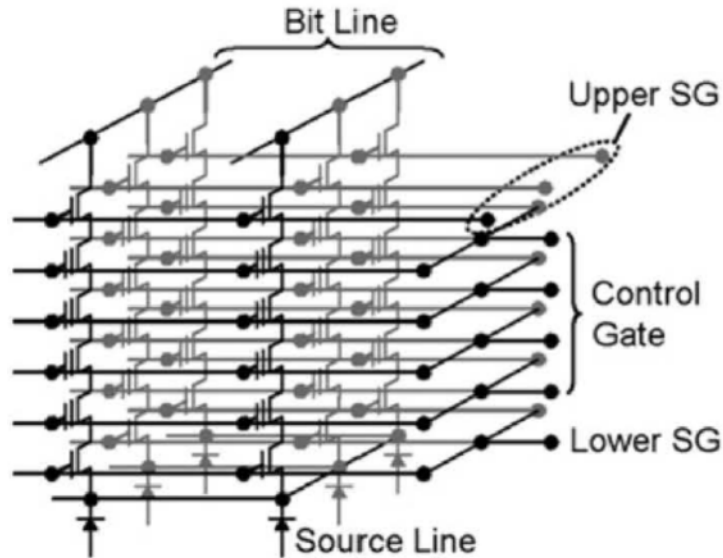
The '604 patent and the prior art discussed in this Petition relate to three-dimensional (3D) memory devices, *e.g.*, 3D NAND memory devices. Early NAND devices were formed as two-dimensional memory arrays. *Id.*, 58.



Id., 40. “[T]o further scale down the memory cell size,” “three- dimensional (3D) NAND flash cells” were developed. *Id.*, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1013, 3.



Ex. 1014, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



Ex. 1012, 296; *see also* Banerjee, ¶¶ 46-54.

The stacked structure in 3D NAND devices typically include one or more memory arrays and a connection region known as a staircase. Ex. 1017 (U.S. Pub. 2017/0256551), Fig. 1F. Staircase structures were well-known and provide conductive landing areas on the individual stair steps 116 (connected to the wordlines in the memory array) for contacts 114. *Id.*, [0052]-[0053].

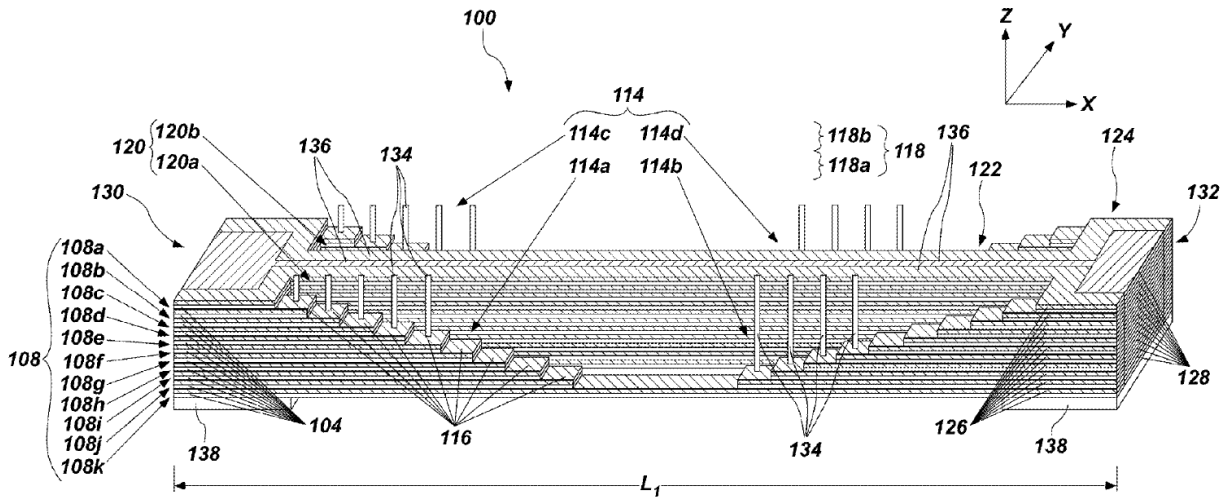


FIG. 1F

Id., Fig. 1F; Banerjee, ¶ 53.

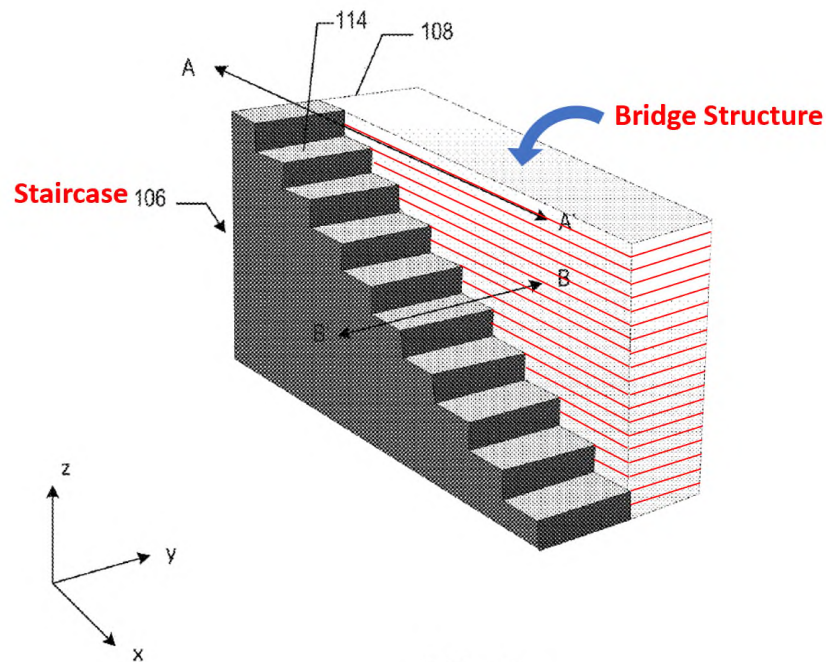
Traditionally, the vertical memory strings, staircase structures, etc., in 3D NAND devices were formed from alternating layers of dielectric and doped polysilicon (which acted as a conductive wordline). But by the '604 patent's priority date in 2020, it was common (and beneficial) to form 3D NAND memory devices using a "gate replacement" process, which involved initially forming an alternating stack of dielectric and sacrificial gate layers, and then replacing the sacrificial gate layers with conductive metal layers to form wordlines for accessing the memory cells. *See, e.g.*, Ex. 1010, [0015], [0050]. Indeed, prior art textbooks taught that one "big advantage" of the metal gate resulting from a gate replacement process is "reduced parasitic resistance of the wordline, which translates into faster operations." Ex. 1018, 132; *see also id.* (explaining additional benefits).

In sum, basic structures like memory strings, staircases, and techniques for manufacturing 3D NAND memory devices (such as gate replacement) were well-known in the art before the '604 patent's priority date. Banerjee, ¶¶ 55-60.

B. The '604 Patent

The '604 patent describes a “3D memory device” with a “staircase structure” that “divides the memory array structure into a first memory array structure and a second memory array structure along a lateral direction.” Ex. 1001, 1:42-47. In other words, the '604 patent discloses two memory arrays with a staircase region in between them.

As shown below, the '604 patent explains the staircase structure is comprised of two main parts: (1) a staircase 106; and (2) a bridge structure 108. *See id.*, 7:42-43, Fig. 1B. The red lines have been added to reflect that bridge 108 is formed of alternating layers of materials in contact with corresponding staircase layers. *Id.*, 5:66-6:1 (“The staircase structure can include a bridge structure that has interleaved a plurality of conductor layers and dielectric layers.”); *id.*, 7:42-43 (“staircase 106 and [] bridge structure 108 [are] in contact with each other.”). Indeed, the '604 patent discloses that the corresponding staircase and bridge layers can be the same material. *Id.*, 8:36-42.



Id., Fig. 1B¹. The bridge connects (or ‘bridges’) memory arrays on either end.
Banerjee, ¶¶ 61-62.

Each staircase step serves as a landing pad for a wordline VIA contact, as Fig. 3A below shows. See Ex. 1001, 10:39-47.

¹ Annotations added throughout unless noted.

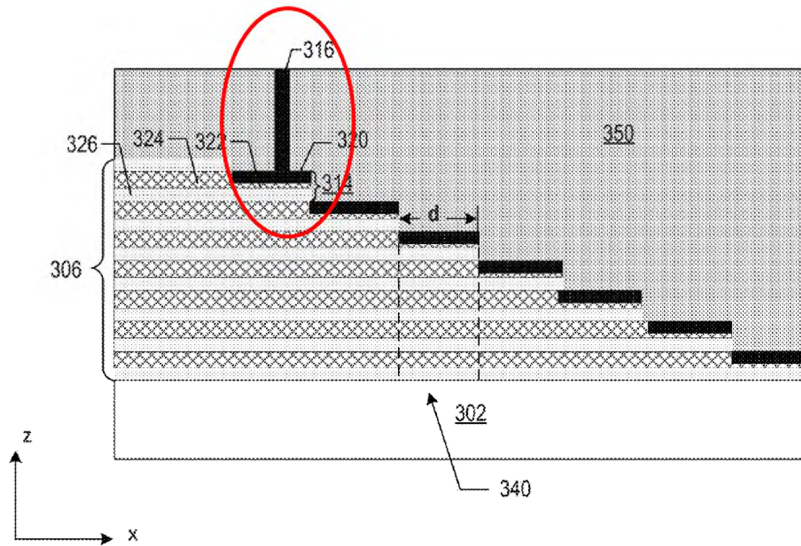


FIG. 3A

Id., Fig. 3A.

The '604 patent purports to solve the “punch-through” problem. *Id.*, 4:58-5:24. The '604 patent explains that as “the number of vertical levels of the stacked storage structure also increases, and it has become more difficult to form the word line VIA contacts on the stairs without **punching through** the contacts and causing short circuits.” *Id.*² The '604 patent further explains:

[W]ord line VIA contacts are often formed by forming openings in contact with the stairs (e.g., the landing area of the stairs) in an insulating structure in which the staircase structure is placed, and filling the openings with a conductive material. Conventionally, these openings, formed to be in contact with stairs at different depths/heights, are formed in the same etching process. Because of the variation in

² Emphasis added throughout unless noted.

opening depths, the openings are often not etched evenly or desirably. For example, the openings in contact with lower stairs (e.g., the deeper openings) and the openings in contact with higher stairs (e.g., the shallower openings) undergo the same etching time, resulting the openings in contact with the higher stairs to be over etched. The over-etching can cause the conductor layers (e.g., word lines) on the top surfaces of the higher stairs to be undesirably damaged or even etched through. The word line VIA contacts can undesirably be in contact with other conductor layers underlying the respective conductor layers, causing a punch-through that leads to short circuits.

Id.

To address this, the '604 patent discloses placing dielectric material underneath the landing area of each stair. *See id.*, 5:25-62. This is accomplished by employing a so-called “conductor portion” (e.g., a narrow conductive finger) that “covers at least the landing area of the respective stair (e.g., a portion of the stair) such that a word line VIA contact can be in contact with and electrically connected to the respective stair.” *Id.* “[T]he dimension of the conductor portion, along the direction the stairs extend, [may be] the same as the dimension of the stair” and “does not laterally extend under [] the conductor portion of any upper stair.” *Id.* In this manner, the “conductor portion” of each stair is in contact with the horizontally adjacent “dielectric portion at the same level” of the stair. *Id.* This results in a staircase where all layers under the landing area of any given step are comprised solely of dielectric. *Id.*

As shown in the modified version of Fig. 3A (on the left), the conductive wordlines (shown in black) underneath any given step extend horizontally to the left where they intersect the memory strings (not shown). In the unmodified version of Fig. 3A (on the right) which employs the '604 patent's purported solution, the conductive portion of each step does **not** extend horizontally to the left.

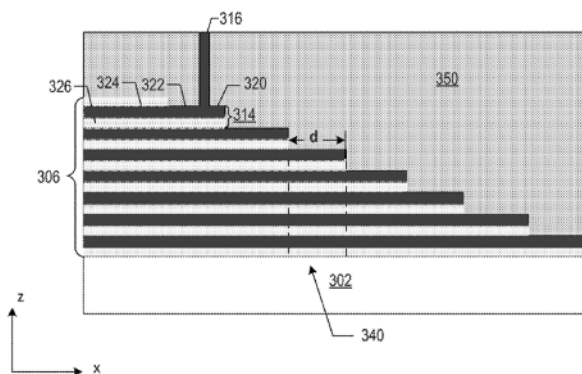


FIG. 3A (modified)

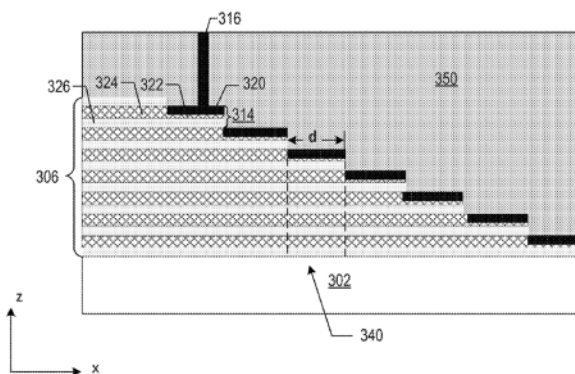


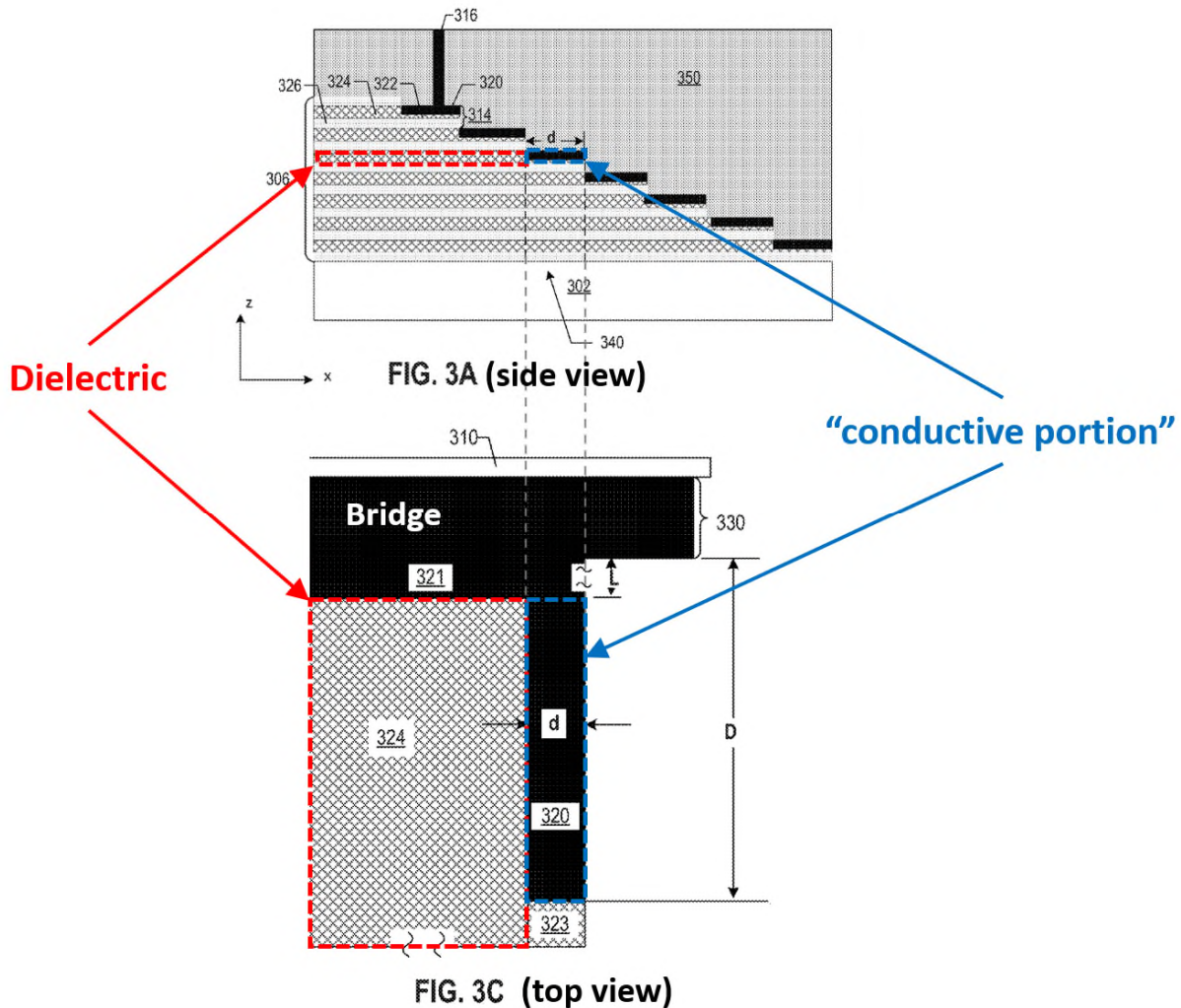
FIG. 3A (unmodified)

Id., Fig. 3A; see also *id.*, 12:8-13.

While the finger approach does not stop over-etching from occurring, it mitigates the consequences. *Id.* In particular, the '604 patent discloses that “[e]ven if a punch-through occurs on any conductor portion, the word line VIA contact has no contact on the ... word line[] of any lower stairs, and leakage or short circuits can be reduced/eliminated.” *Id.*, 5:58-62.

Of course, each “conductor portion” needs to electrically connect to the respective wordline in the memory to provide the appropriate voltages to read/write the memory cells. The '604 patent discloses using the “bridge” to accomplish this. In particular, as discussed *supra*, the bridge “has interleaved a plurality of conductor

layers and dielectric layers” (*id.*, 5:66-6:1) that contact the corresponding staircase layer (*id.*, 7:42-43). The annotated versions of Figs. 3A and 3C below illustrate how a “conductive portion” of a given step in the staircase physically and electrically connects to its corresponding layer in the bridge.



Id., Figs. 3A and 3C. The bridge, in turn, physical and electrically connects to the corresponding wordline in the memory array (not shown). *Id.*, 6:1-2. Thus, the

wordline vias 316 electrically control the corresponding wordlines in the memory array. *Id.*, 6:2-7.

When the staircase structure is located in between two memory arrays, “[e]ach word line thus can be bilaterally driven (in both positive and negative x-directions) from a respective word line VIA contact 116 in the intermediate of 3D memory device 100 through bridge structures 108.” *Id.*, 9:9-13; Banerjee, ¶¶ 63-71.

C. Prosecution History

Prosecution of the ’604 patent was short. *See generally* Ex. 1002. All claims were found allowable in the first (and only) office action. *Id.*, 657-664. The Examiner made no prior art rejections, or any other invalidity rejection. *Id.*

The Examiner did, however, state that “the closest prior art of record [was] Zhang [Ex. 1010].” Ex. 1002, 657-664. In short, the Examiner stated Zhang failed to teach the “conductor portion” and “dielectric portion” at the “same level.” *Id.*, 658-659. It appears that the Examiner found that Zhang lacked the “finger” approach disclosed in the ’604 patent. *See* §V.B.

Throughout prosecution, Patent Owner submitted five Information Disclosure Statements (IDS) containing dozens of references. *See* Ex. 1002, 77, 180, 304, 410, and 740. One IDS identified TW201605015, which is the Taiwanese version of Lee. *Id.*, 180. But Patent Owner never submitted the English-language version (*id.*, 234-

301), even though it was readily available to Patent Owner. *See* Lee, cover (listing publication date of January 28, 2016).

The Examiner never employed any prior art reference in any rejection. As the Petition explains, Thimmegowda in combination with Lee and/or Kobayashi teaches or renders obvious the claim elements that led to allowance, and all other elements of the Challenged Claims. Banerjee, ¶¶ 72-75.

VI. PRIOR ART SUMMARIES

A. Thimmegowda

Thimmegowda (Ex. 1005), assigned to Intel, was filed November 30, 2017, and published February 7, 2019. Thimmegowda is prior art to the '604 patent under at least 35 U.S.C. §§102(a)(1) and 102(a)(2).

Thimmegowda is titled “Wordline Bridge in a 3D Memory Array.” Thimmegowda, cover. Thimmegowda discloses conventional 3D memory device features, including an alternating conductor/dielectric layer stack, memory strings extending through the alternating stack, staircase structures and wordline contacts for accessing the memory strings, etc. *See, e.g., id.*, 1:10-25.

Thimmegowda observes that forming a separate staircase to access the wordlines in each memory array “consumes silicon real estate.” Thimmegowda, 1:20-25. Thus, Thimmegowda discloses a “wordline bridge” that physically and electrically connects the respective wordlines of two memory arrays and allows a

single staircase to access both memory arrays. *Id.*, Abstract; *see also, e.g., id.* (“wordline bridge between wordlines of adjacent tiles of memory cells [] reduce[s] the number wordline staircases in 3D memory arrays.”), 6:33-35, 9:62-66; Banerjee, ¶¶ 78-80.

Thimmegowda discloses a “wordline bridge 306” as shown in blue below.

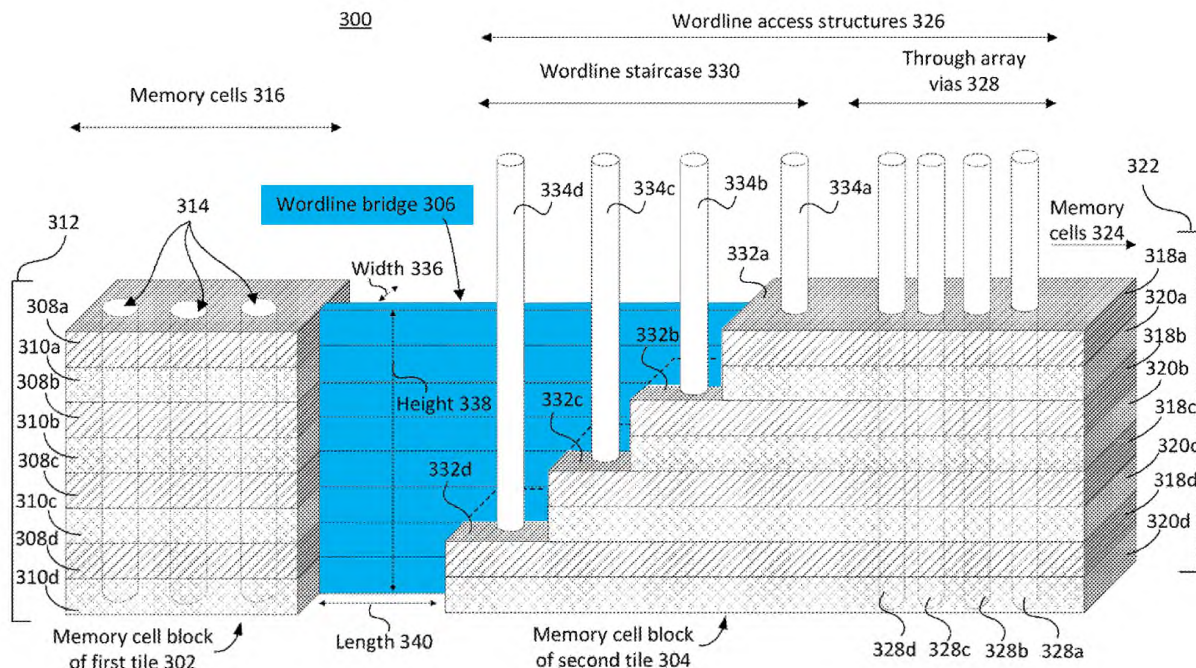


FIG. 3

Thimmegowda, Fig. 3. “The wordline bridge 306 electrically couples the wordlines 308” for the left memory block “to the wordlines 318” for the right memory block “to enable the wordline access structures 326 to access the wordlines 308.” *Id.*, 9:46-51; *see also id.*, 8:25-31.

Additionally, between the memory blocks and connected to the wordline bridge is a “wordline staircase 330,” which includes “staircase step[s]” (332) that provides access to respective “wordline[s]” (318). Thimmegowda, 9:27-45. “The wordline staircase 330 provides access to the wordlines 318 for metal contacts 334.” *Id.*, 9:42-45.

Just like the ’604 patent’s bridge, Thimmegowda’s wordline bridge (which is connected to the staircase steps) enables a single conductive contact (*e.g.*, 334a) to bidirectionally drive memory cells in the memory arrays on either side of the bridge (*viz.*, the memory cell block of first memory tile 302 on the left of Fig. 3 and memory cell block of second memory tile 304 on the right) of the 3D memory device. Thimmegowda, 9:49-51; 7:61-64; Banerjee, ¶¶ 81-83.

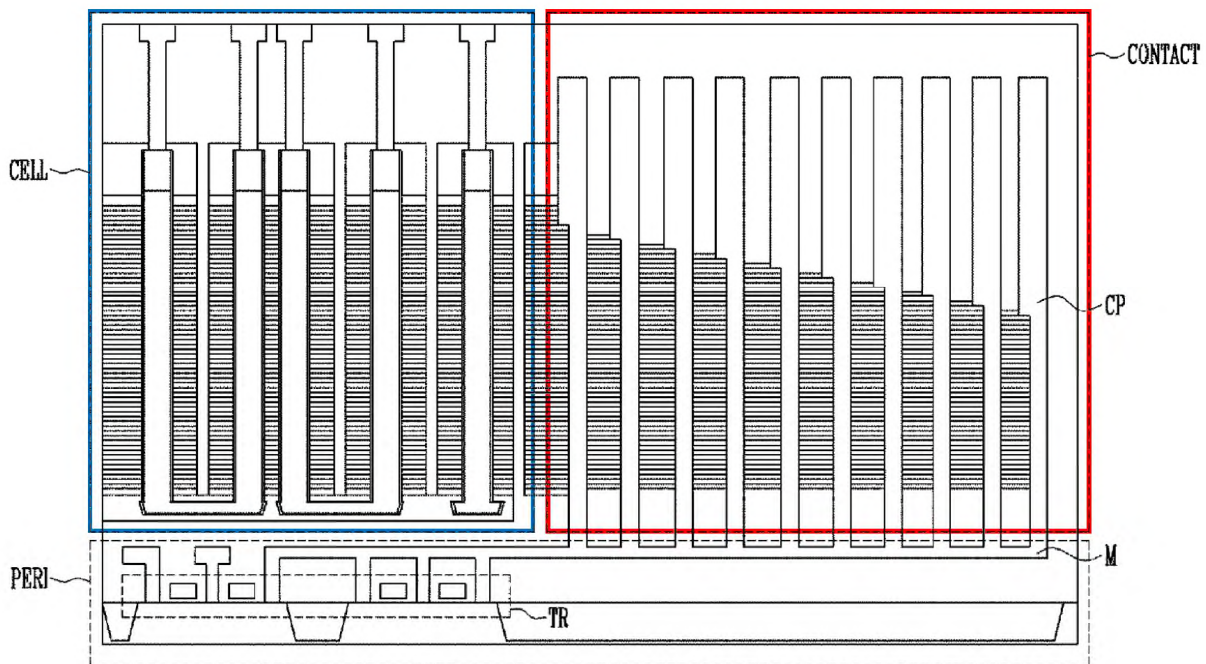
B. Lee

Lee (Ex. 1007) was published on January 28, 2016. Lee is prior art to the ’604 patent under at least 35 U.S.C. §§102(a)(1) and 102(a)(2).

Lee discloses conventional 3D memory device features, including an alternating conductor/dielectric layer stack, memory strings, staircases, staircase contacts (which Lee refers to as “contact plugs”), etc. *See, e.g.*, Lee, [0005]-[0006].

The memory device includes a “cell” region (with memory strings) and a “contact” region (with a staircase). Lee, [0063]-[0064].

FIG. 14A

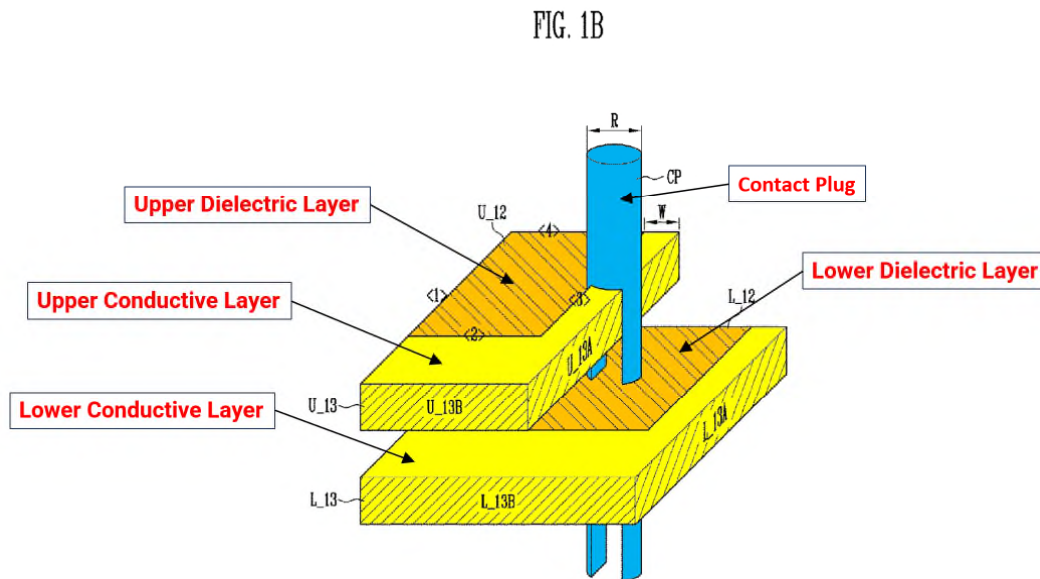


Id., Fig. 14A.

Like the '604 patent, Lee recognizes that “the contact plugs” for connecting to the wordlines in the staircase region “are to be formed with varying depths ... [which] may make it more difficult to manufacture the memory device.” Lee, [0007]. In particular, “the contact plugs may pass through the word lines to form a bridge³ [*i.e.*, a short].” *Id.*

³ Lee uses the term “bridge” differently than the '604 patent to indicate a short circuit due to punch through.

Lee discloses an “interconnection structure” comprised of alternating insulating and dielectric layers “stacked stepwise,” with “conductive layers interposed between the insulating layers and surrounding sidewalls of the dielectric layers.” Lee, [0008]. As shown below, Lee’s interconnection structure includes contact plugs coupled to the conductive layers that “may at least partially pass through the dielectric layers.” *Id.* Notably, both steps shown in Fig. 1B include a dielectric layer (U_12 and L_12, respectively) with two “sidewalls ... surrounded by [] conductive layers” U_13 and L_13, respectively. *Id.*, [0028]. Lee describes the distinctive conductive structures (highlighted in yellow) as “L-shape[d].” *Id.*, [0029].

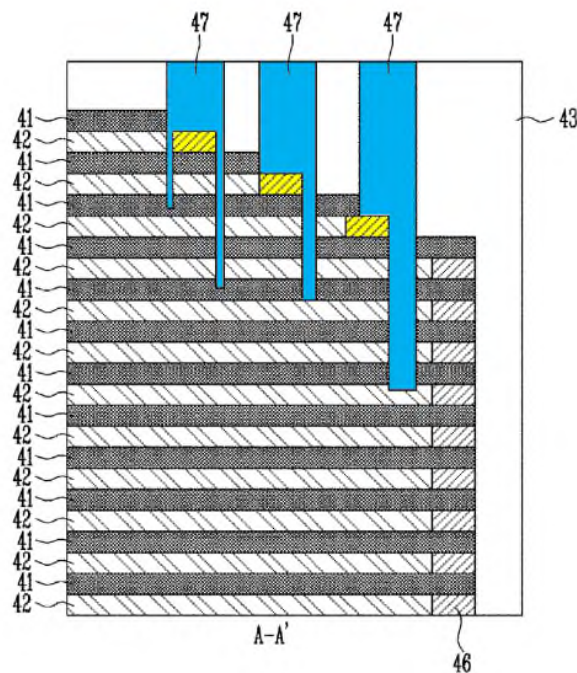


Id., Fig. 1B. Lee explains that “insulating layers 11” are also present “between [the horizontal layers in Fig. 1B],” but are not shown “for convenience of explanation.” *Id.*, [0028].

As also illustrated in Fig. 1B, the contact plug (highlighted in blue) extends through an underlying step without causing a short circuit to another wordline because the step below includes a dielectric region (highlighted in orange). Lee, [0031]. Thus, Lee solved the purported “punch through” problem using the same technique described in the ’604 patent, but Lee did it more than 6-years earlier.

In fact, Lee illustrates the over-etch punch through scenario in Fig. 10A, where various contact plugs 47 (highlighted in blue) are over-etched past the conductive landing pads (highlighted in yellow) through underlying insulating layers 41 and sacrificial layers 42 with no negative effects. Lee, [0056].

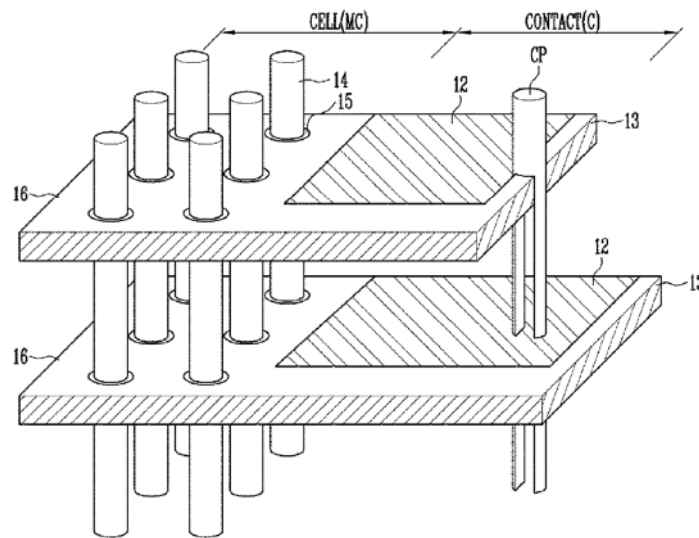
FIG. 10A



Id., Fig. 10A; *see also id.*, [0056].

When implemented in a 3D memory device, it is apparent how the contact plugs connect (physically and electrically) to the conductive layers 13 to access and control the memory strings in the cell region. Lee, [0033].

FIG. 1C



Id., Fig. 1C; Banerjee, ¶¶ 85-92.

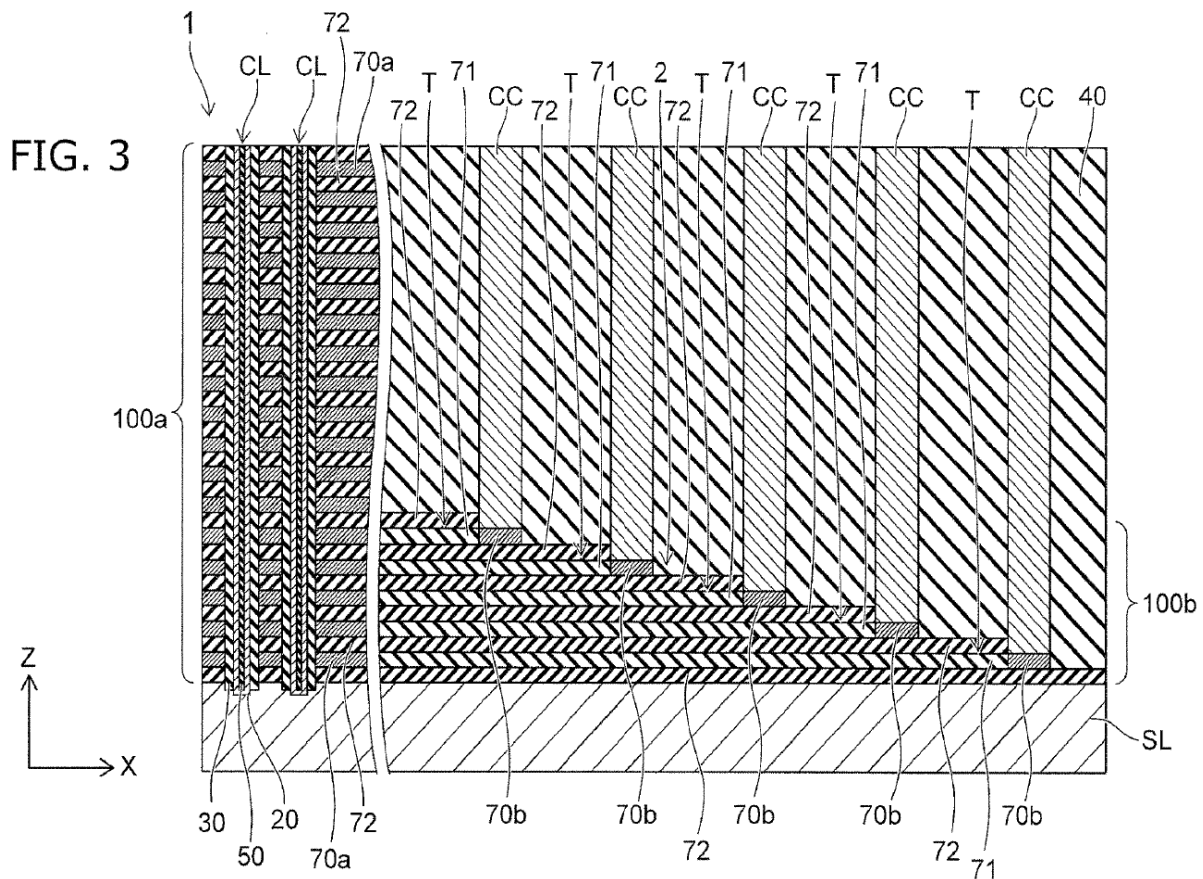
C. Kobayashi

Kobayashi (Ex. 1006), assigned to Toshiba, has a U.S. filing date of January 5, 2018 and was published on January 3, 2019. Kobayashi, cover. Kobayashi is prior art to the '604 patent under at least 35 U.S.C. §§102(a)(1) and 102(a)(2).

Kobayashi discloses various features of conventional 3D memory devices, including memory cell arrays with “memory strings” extending through alternating layers of conductors and insulators, a staircase region, wordline contacts, etc. *Id.*,

Fig. 3, [0029] (wordlines), [0042] (memory strings), [0046] (staircase), [0085] (wordline contacts). Kobayashi's conductive layers 70a are the wordlines.

To provide access to the wordlines, as shown below, Kobayashi discloses “contacts CC extending in the Z-direction” that “reach the terrace portions T” (*i.e.*, landing pads) of the staircase. Kobayashi, [0085]-[0086].



Kobayashi, Fig. 3.

One notable feature present in Fig. 3, but more easily seen in Figs. 1 and 5 below, is a thin conductor 70b (yellow) horizontally adjacent to a dielectric “spacer 71” (orange) on the stairstep terrace T. Kobayashi, [0069]-[0072], [0079]-[0082].

The conductor 70b serves as the landing pad connection point for the wordline contacts CC (shown in Figs. 1 and 3).

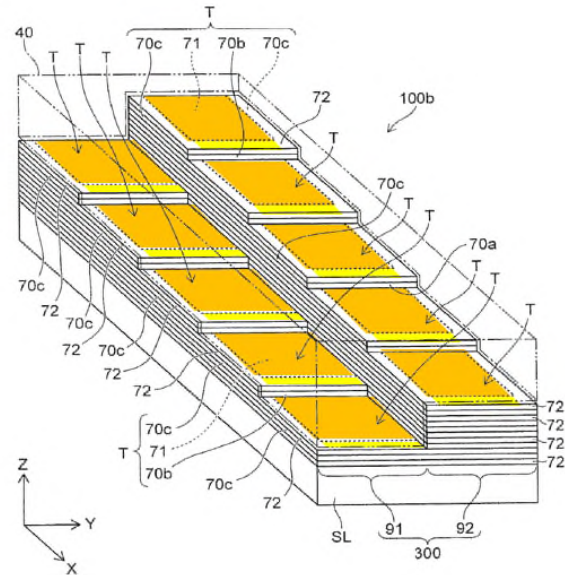
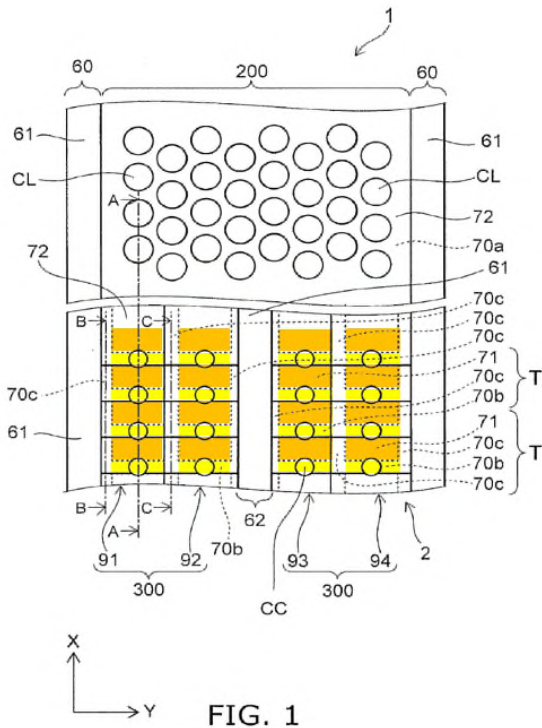


FIG. 5

Id., Figs. 1 and 5. When connected to conductive portion 70c (which effectively forms a bridge), the conductive portions 70b form an “L-shaped” conductor that is physically and electrically connected to the respective wordlines in the memory array. *Id.*, [0029], [0073] (“One end portion of the second conductive portion 70c extending in the X-direction is connected to the first conductive portion 70b provided at the tip of the terrace portion T; and the other end portion is connected to the conductive layer 70a of the first stacked portion 100a. The first conductive portion 70b and the second conductive portion 70c are connected in an L-shaped configuration”), [0079].

As noted, the interior of the L-shaped conductors comprises a dielectric “spacer portion 71.” Kobayashi, [0069]-[0072], [0079]-[0082] (“The spacer portion 71 is provided on the inner side of the first conductive portion 70b and the second conductive portion 70c forming the L-shape.”). As described in [0139]-[0144] and shown in Fig. 33B, just like the ’604 patent, the use of dielectric spacer 71 solves the same punch-through problem, where over-etching will not result in a short to an underlying layer.

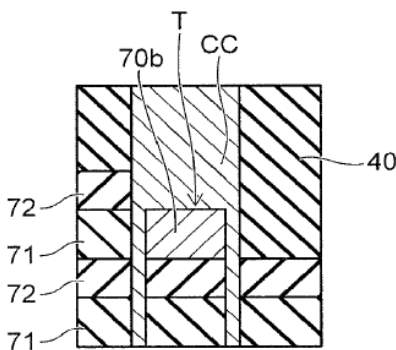


FIG. 33B

Id., Fig. 33B. As described in [0141], “[b]ecause the spacer portions 71 are silicon nitride layers and are insulating bodies, the contact CC is not shorted to the first conductive portions 70b of the other layers even when the contact CC reaches the spacer portions 71 of the other layers lower than the first conductive portion 70b to be connected.” Banerjee, ¶¶ 94-99.

VII. CLAIM CONSTRUCTION

For purposes of this Petition, Petitioner submits the Challenged Claims do not require further construction and should receive their plain and ordinary meaning.

VIII. LEVEL OF SKILL IN THE ART

A POSITA in the field of the '604 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, its component parts, how it operates, and how it is controlled. Banerjee, ¶¶ 40-43.

IX. GROUND 1: THIMMEGOWDA IN VIEW OF LEE AND A POSITA'S KNOWLEDGE

Thimmegowda in view of the teachings of Lee and a POSITA's knowledge renders claims 1-5 and 8-13 obvious.

A. Motivation to Combine

A POSITA would have been motivated to combine the teachings of Thimmegowda and Lee with a reasonable expectation of success. At the outset, it is important to note that Petitioner is **not** proposing to bodily incorporate Lee into Thimmegowda, or vice versa. Rather, Petitioner is combining Thimmegowda's

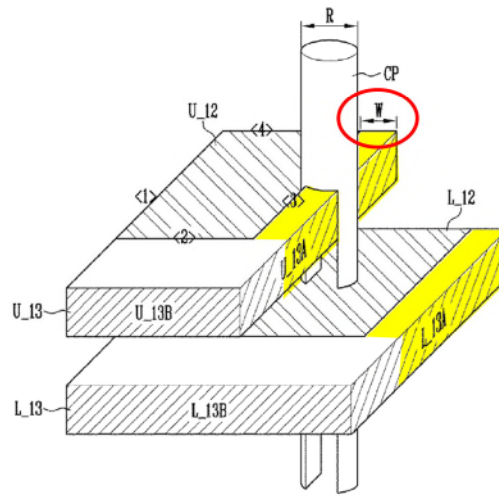
bridge and array architecture teachings that enables a single staircase to bidirectionally drive two arrays and Lee's stairstep teachings that mitigate punch through. *See, e.g., In re Keller*, 642 F.2d 413, 425 (CCPA 1981) ("The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference Rather, ***the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art.***"). Put another way, Petitioner's analysis (and conclusion of obviousness) is the same were one to frame the combination as Lee's stairstep finger approach in view of Thimmegowda's bridge and array architecture teachings.

A POSITA would have been motivated to apply Lee's teaching of non-overlapping conductive fingers to ameliorate the known problems (*e.g.*, short circuits) associated with punch through in Thimmegowda's staircase. Banerjee, ¶¶ 101-03. The problem of overetching wordline via holes in 3D NAND staircase structures was well-known in the art. *See, e.g.*, Ex. 1021, 13:2-11 ("forming electrically conductive contact structures . . . may undesirably punch through the one or more of the electrically conductive materials"); Ex. 1022, 1:66-2:1 (discussing "undesirable defect[]" of "word line contact punch through"), 9:62-10:6; Ex. 1023, 3:52-58 (describing "punch through" problem that causes "yield loss."), 7:42-46 (discussing "undesirable" "punchthrough" problem), 7:61-63 (same); Ex. 1024, Fig. 5, [0061] (same), [0079]-[0080] (same).

A POSITA would naturally look to existing solutions, such as that proposed by Lee, to address the punch-through problem (*e.g.*, to improve yield). As discussed §VI.B, Lee discloses using non-overlapping conductive fingers to mitigate the effects of punch-through. Lee, [0037]-[0038], [0056]. Both Thimmegowda and Lee disclose 3D NAND memory devices that utilize a staircase structure to provide wordline contacts for accessing the memory arrays. While Lee discloses forming multiple sets of staircases (labeled “interconnection structures C1 to C3”), all of which employ the “finger” approach (*see* Lee, Fig. 1), Lee’s finger approach is readily applicable to the single staircase illustrated in Thimmegowda Fig. 3. Banerjee, ¶ 104.

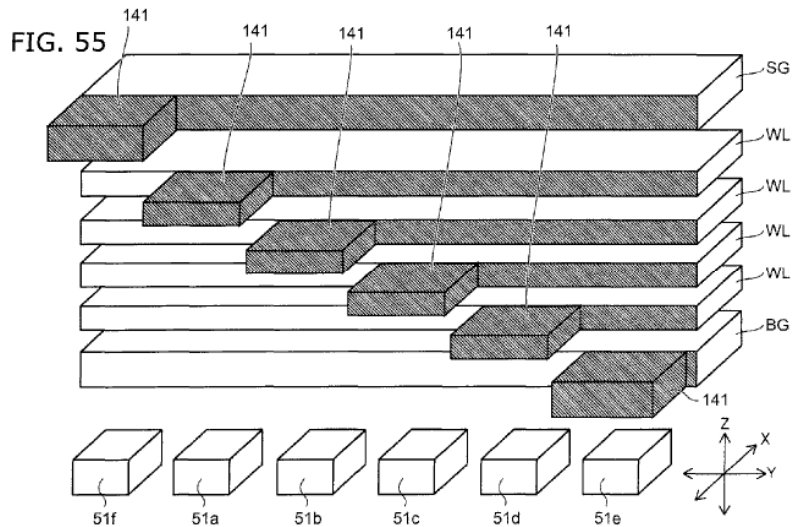
In view of the combined teachings of Lee and Thimmegowda, two implementations of Lee’s finger approach would have been obvious to a POSITA. First, it would have been obvious to a POSITA to use a “thin” finger narrower (in the x-direction) than the width of a step as Lee Fig. 1B expressly discloses.

FIG. 1B



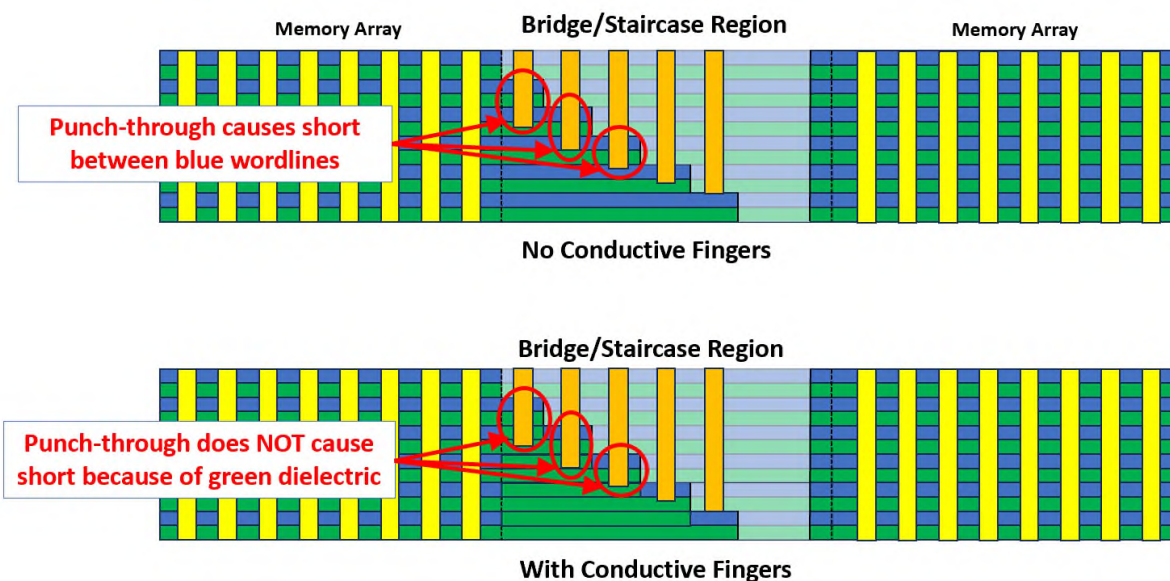
Lee, Fig. 1B (showing finger with width “W” less than step width); Banerjee, ¶ 105.

Second, it would also have been obvious to a POSITA to make the conductive finger cover the full width of the step, especially given that Thimmegowda’s landing pad already did so. Banerjee, ¶ 106. Further, other 3D NAND references, like Nakaki Fig. 55 below, already disclosed non-overlapping conductive fingers (which solved punch through) that covered the full exposed surface area of each stairstep. Ex. 1011, 14:64-65 (“the end parts 141 of the aforementioned staircase structure section 140 are provided as contact parts”), 15:10-11 (“The contact parts 141 do not overlap each other in the Z-direction.”).



Id., Fig. 55; see also *id.*, Fig. 56.

A POSITA would have readily understood that a conductive finger covering the full exposed area of a stair step mitigates the deleterious effects of punch through. This is illustrated, at a conceptual level, by the demonstrative cross-section figures below. The blue layers represent conductive wordlines, the green layers are dielectric, the orange pillars are wordline vias, and the yellow pillars are memory strings.



In the top figure, which does not employ a “finger” approach, the wordline vias “punch through” the intended wordline to an underlying wordline and electrically short the two wordlines together. The lower figure employs conductive fingers that cover the full width of each exposed step. Significantly, adjacent to each step (in the x-direction) is green dielectric material, instead of conductor. Thus, even though the wordline vias “punch through” the intended wordline, they merely extend in the z-direction through additional dielectric and do not create a short to another wordline. Especially given that Thimmegowda’s wordline via landing area already covered the full step width and placed the wordline via in the center of the landing pad (see, e.g., Thimmegowda, Fig. 3), a POSITA would have found it obvious to use a full step-width conductive finger in view of the combined teachings of Lee and Thimmegowda to mitigate punch through. Banerjee, ¶¶ 107-10.

Additionally, Lee discloses using the well-known gate-replacement process (see §V.A), which provides additional motivation to combine Lee and Thimmegowda. In particular, Lee discloses forming its conductive fingers (and the memory device at large) using gate-replacement, which would benefit Thimmegowda's bridge and array architecture. Lee, [0044] (replacing "sacrificial layers"). For example, using metal wordlines (instead of, *e.g.*, polysilicon wordlines), substantially lowered wordline resistance and resulted in faster read/write operations, as described in textbooks published several years before the '604 patent's priority date. See Ex. 1018, 131-32; Banerjee, ¶ 111.

Moreover, employing bridge and architecture in Lee would have provided the advantage of bidirectionally driving two arrays (§VI.A) using a single staircase (which saves space), and would be complementary to Lee's lower resistance from metal gates (via gate replacement). Banerjee, ¶ 112.

Reasonable Expectation of Success. A POSITA would have had a reasonable expectation of success in combining the teachings of Thimmegowda's bridge and array architecture (to drive two memory arrays with one wordline via) with Lee's staircase finger approach (to mitigate punch through). Banerjee, ¶¶ 113-14. To begin, both Thimmegowda and Lee relate to 3D NAND memory devices with memory arrays whose memory strings are accessed using wordline vias in contact with individual staircase steps. See Thimmegowda, Fig. 3; Lee, Fig. 1C.

Thus, the references share a number of key architectural similarities. In particular, combining Lee's finger approach with Thimmegowda's bridge would not change the functionality of how wordline vias read/write the memory cells (*viz.*, there would still be an electrically conductive path to the memory arrays). Likewise, applying Thimmegowda's bidirectional wordline bridge teachings to Lee would not have any impact on how Lee's finger approach mitigates punch through.

And Thimmegowda's wordline bridge architecture is entirely compatible with Lee's gate replacement manufacturing process. Banerjee, ¶ 113, Indeed, a POSITA would not be able to tell by looking at Thimmegowda Fig. 3 what type of manufacturing process (*e.g.*, gate replacement) was used, and would have understood that no particular manufacturing process was required (*e.g.*, the wordline could be made of doped polysilicon or metal such as tungsten). Concerning manufacturing, Lee provides detailed teachings regarding a gate replacement process for forming the fingers, and explains in detail how to manufacture the conductive fingers 13 and adjacent dielectric portions 12. *See* Lee, Figs. 4-13B (and accompanying discussion at [0043]-[0062] describing the gate replacement manufacturing process in detail, especially [0044]-[0045], [0048], [0050], and [0053]-[0055]). More generally, gate replacement techniques were well-known and well within the knowledge and skill of a POSITA, and could readily be applied to form the bridge/staircase structure in Thimmegowda. *See also, e.g.*, Ex. 1017, Figs.

1A-1F (illustrating formation of 3D NAND bridge using gate-replacement process). Accordingly, a POSITA would have had a reasonable expectation of success in combining the teachings of Lee and Thimmegowda. Banerjee, ¶¶ 113-14.

B. Claim 1:

Ground 1 renders claim 1 obvious.

1. [1.PRE] “A three-dimensional (3D) memory device, comprising:”

To the extent the preamble is limiting, Thimmegowda discloses *[a] three-dimensional (3D) memory device*. Thimmegowda’s title is “Wordline Bridge in a *3D Memory Array*.” Thimmegowda, cover; *see also id.*, Abstract, Fig. 3, 1:11-12, 1:64-66; Banerjee, ¶ 116.

2. [1.A] “a memory array structure; and”

Thimmegowda discloses *a memory array structure*. Thimmegowda, Abstract (“The present disclosure relates to providing a wordline bridge ... *in 3D memory arrays. An apparatus may include a memory array having memory cells*. The memory array includes a first block of pages of the memory cells in a first tile and a second block of pages of the memory cells in a second tile.”); 2:57-65 (“memory array”).

Fig. 2 below shows “[t]he memory die 200 includes a memory array 202 ... [which] includes memory cells 205 and memory cells 206.” Thimmegowda, 7:7-11.

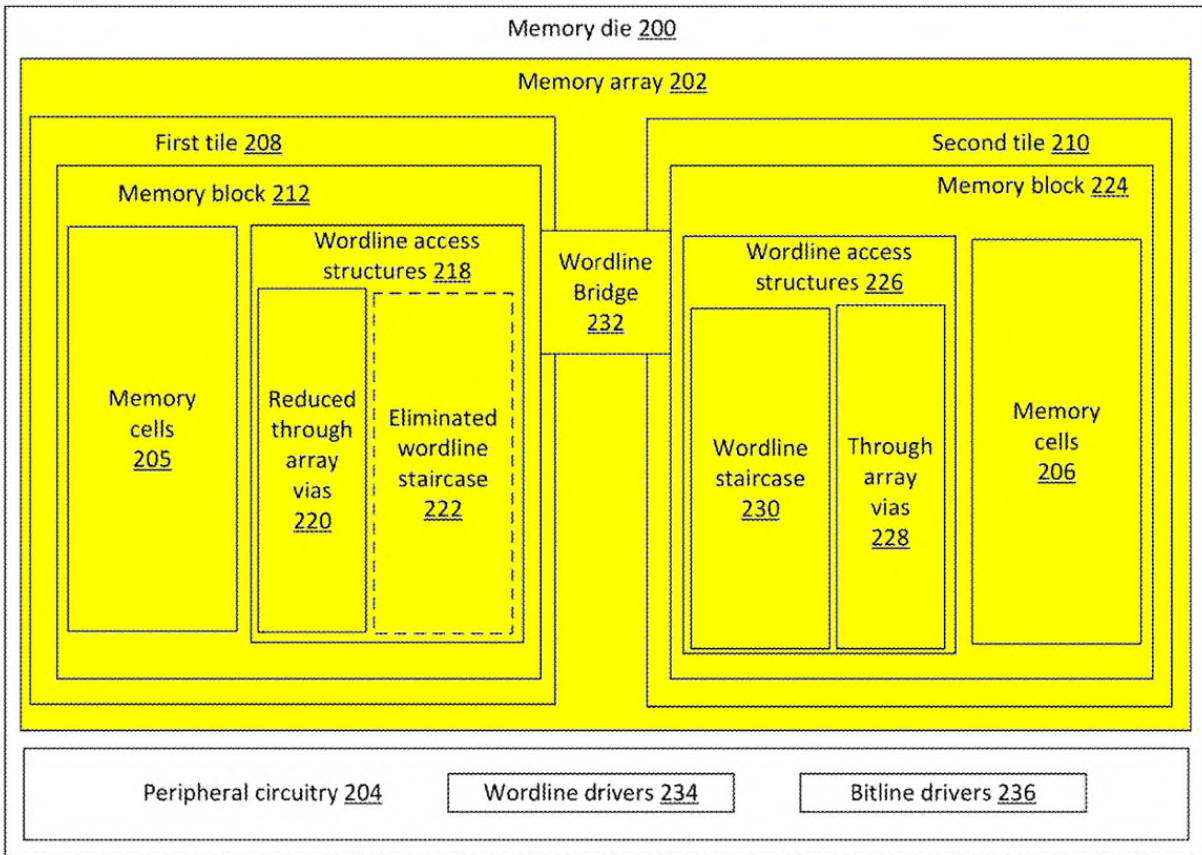


FIG. 2

Id., Fig. 2; *see also* Fig. 3; Banerjee, ¶¶ 117-18.

3. [1.B] “a staircase structure in an intermediate of the memory array structure and dividing the memory array structure into a first memory array structure and a second memory array structure along a lateral direction, the staircase structure comprising”

Thimmegowda discloses element 1[b]. Thimmegowda discloses its “memory arrays are terminated with one or more staircase structures, to allow connection metal contact structures to be connected to the wordlines. The staircase structures include a step or landing for each wordline, to connect each wordline to a metal contact.” Thimmegowda, 1:12-17. Thimmegowda’s wordline staircase 330 (shown

in Fig. 3 below) is the claimed *staircase structure* (subsequent limitations discuss obvious modifications in view of Lee).

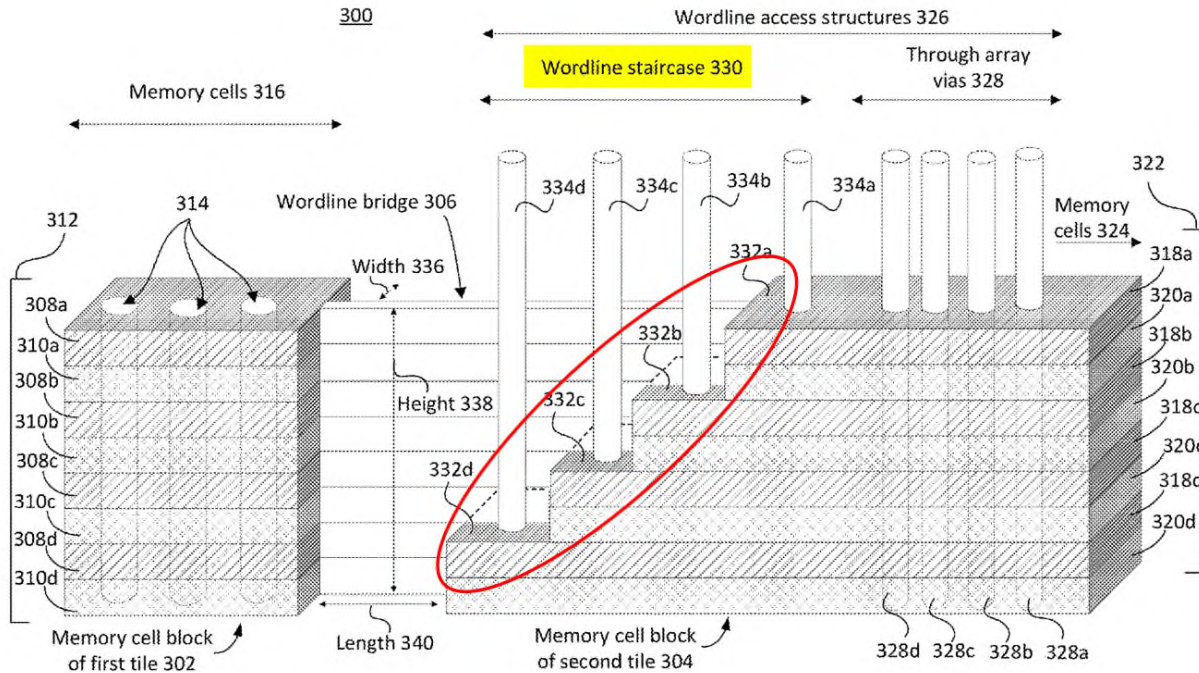


FIG. 3

Id., Fig. 3; see also *id.*, Fig. 2. Fig. 3 also shows that the staircase structure is located *in an intermediate of the memory array structure and dividing the memory array structure into a first memory array structure and a second memory array structure along a lateral direction*. In particular, the staircase 330 sits in between the memory cell block of first tile 302 (located on the left in the lateral x-direction) and the memory cell block of the second tile 304 (located on the right in the lateral x-direction). *Id.*, 7:16-17 (“The memory array 202 is segmented into a first tile 208 and a second tile 210”), 8:27-31; Banerjee, ¶ 119.

4. [1.C] “the staircase structure comprising (i) a plurality of stairs extending along the lateral direction, and”

Thimmegowda discloses element 1[c]. As noted for element 1[b], the claimed *lateral direction* is the x-direction in Thimmegowda Fig. 3. As Fig. 3 shows, the staircase 330 comprises a *plurality of stairs* in the x-direction. For example, Thimmegowda discloses that “[t]he wordline staircase 330 includes a wordline staircase step 332a that provides access to the wordline 318a” Thimmegowda, 9:27-38, 1:12-17 (“a step or landing for each wordline”).

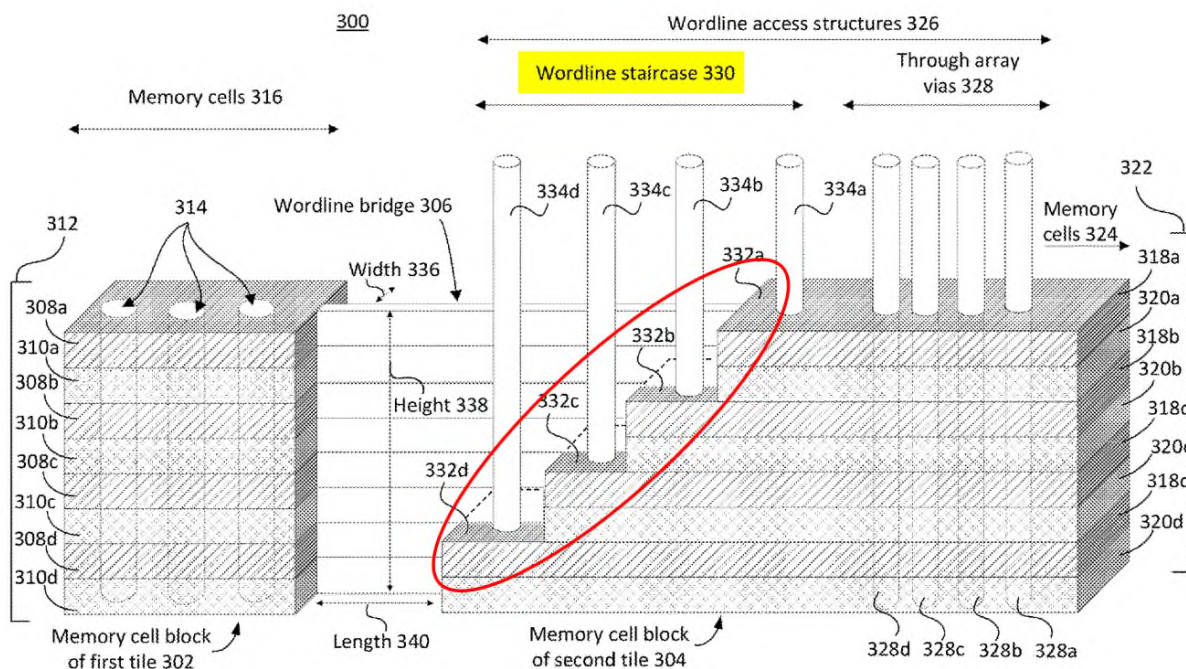


FIG. 3

Id., Fig. 3; Banerjee, ¶ 120.

5. [1.D] “the staircase structure comprising ... (ii) a bridge structure in contact with the first memory array structure and the second memory array structure,”

As an initial matter, the '604 specification explains a *bridge structure* “can include vertically interleaved conductor layers and dielectric layers (not shown), and the conductor layers (e.g., metal layers or polysilicon layers) can function as part of word lines.” Ex. 1001, 7:66-8:2. The '604 patent illustrates an exemplary bridge structure 108 in Fig. 1B. In the annotated version of Fig. 1B below (left), red lines have been added to reflect that bridge 108 is formed of alternating layers of materials. *Id.*, 5:66-6:1 (“conductor layers and dielectric layers.”). And, as shown in the top-down view of Fig. 1C below (right), the bridge structure 108 extends horizontally in the x-direction between two memory arrays (bridging them together).

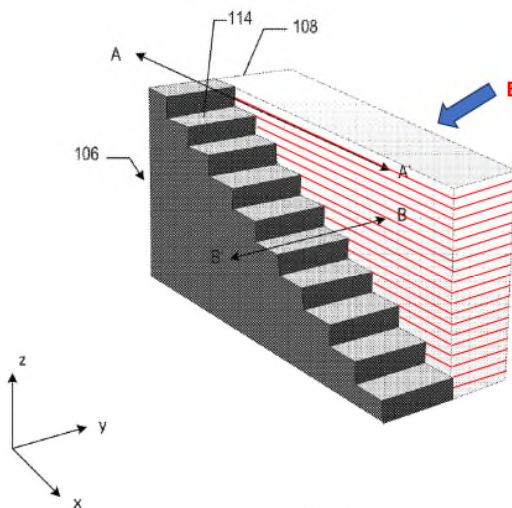


FIG. 1B

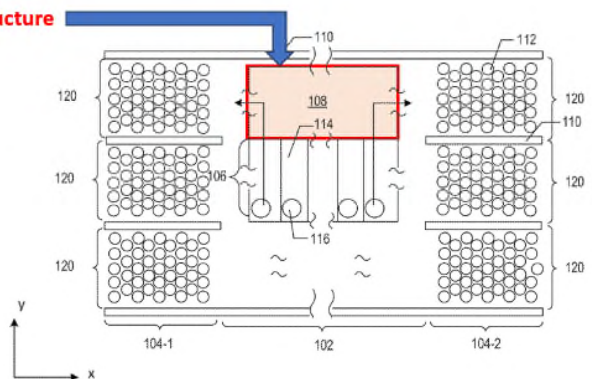


FIG. 1C

Id., Fig. 1B and 1C. At least one example of a “bridge structure” is an alternating

300

Memory cells 316

Wordline access structures 326

Wordline staircase 330

Through array vias 328

312

314

Wordline bridge 306

Width 336

Height 338

334d

334c

334b

334a

332a

332b

332c

332d

Memory cell block of first tile 302

Memory cell block of second tile 304

322

Memory cells 324

318a

320a

318b

320b

318c

320c

318d

320d

328d

328c

328b

328a

308a

310a

308b

310b

308c

310c

308d

310d

Thimmegowda, Fig. 3; *see also id.*, Figs. 1 and 2 (showing wordline bridge in electrical and physical contact with two memory arrays). “The wordline bridge 306 electrically couples the wordlines 308 to the wordlines 318 to enable the wordline access structures 326 to access the wordlines 308, ... The wordline bridge 306

includes the same layers as the wordline stacks 312, 322.” *Id.*, 9:46-60; *see also id.*, 2:35-44; Banerjee, ¶ 122.

Thimmegowda explains its wordline bridge enables a single staircase to bidirectionally drive memory arrays on either side of the bridge. *See, e.g.*, Thimmegowda, 7:61-64.

For example, the claimed *first memory array structure* corresponds to “memory cell block of first tile 302” and the claimed *second memory array structure* corresponds to “memory cell block of second tile 304” in Fig. 3. A POSITA would have understood that wordline staircase 330, via the wordline bridge, (and/or the wordline access structure 326 which include staircase 330) is *in contact with* each memory block, as the bridge enables the staircase contact to bidirectionally drive each array. Thimmegowda, 6:48-60, 7:61-64. The presence of through array vias 328 in Fig. 3 does not change that Thimmegowda discloses *a bridge structure in contact with the first memory array structure and the second memory array structure*. Banerjee, ¶¶ 123-24.

A POSITA would further understand Thimmegowda’s wordline bridge is part of the claimed *staircase structure* as used in the ’604 patent. Banerjee, ¶ 126; Ex. 1001, Fig. 1A and 1B (showing “staircase structure 102” comprising both a “plurality of stairs 114” and a “bridge structure 108”), 2:51-54, 7:42-43 (“FIG. 1B

depicts staircase structure 102 having a staircase 106 and a bridge structure 108, in contact with each other.”).

6. [1.E] “the plurality of stairs comprising a stair above one or more dielectric pairs,”

As an initial matter, regarding *dielectric pairs*, the ’604 specification explains that “[i]n some embodiments, each stair 414 includes a pair of sacrificial layer 429 and an underlying dielectric layer 426 (e.g., one sacrificial/dielectric pair).” Ex. 1001, 14:36-39. In other words, the combination of one sacrificial layer and its corresponding dielectric layer together comprises a “dielectric pair.” *See also id.*, 1001, 5:50-53, 18:48-53. At least one example of a dielectric pair within the meaning of the claims is a sacrificial layer and its corresponding dielectric layer. Banerjee, ¶ 127.

Thimmegowda in view of the teachings of Lee discloses element 1[e]. To begin, Thimmegowda discloses “steps 332” that form part of the staircase as Fig. 3 below shows:

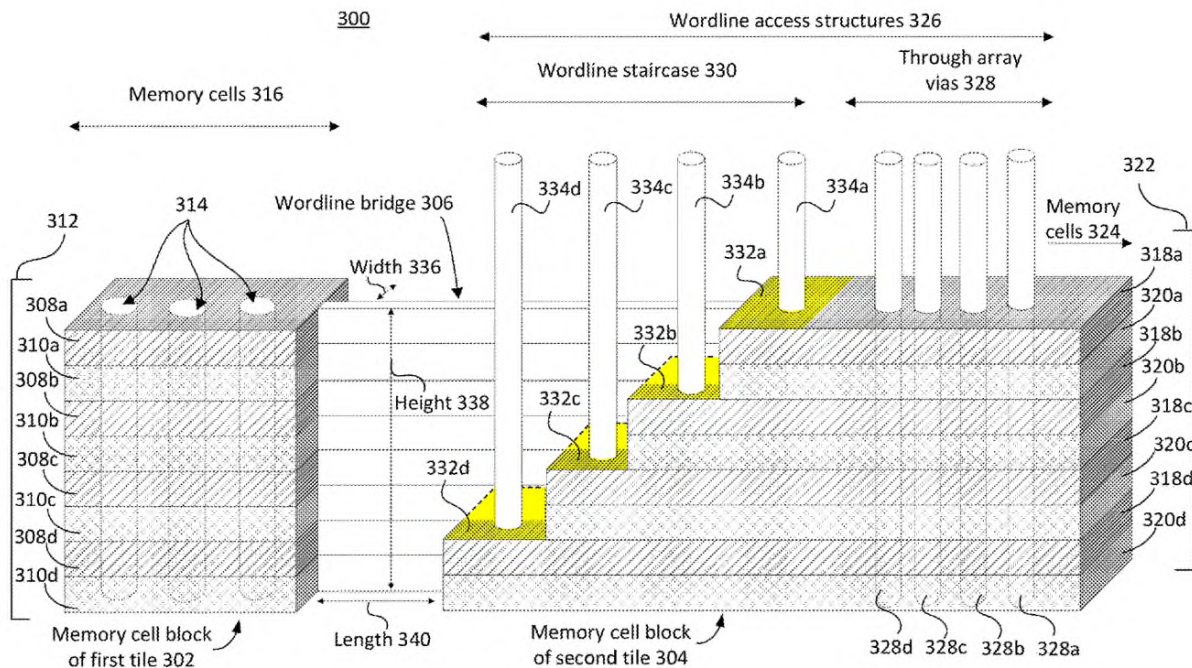
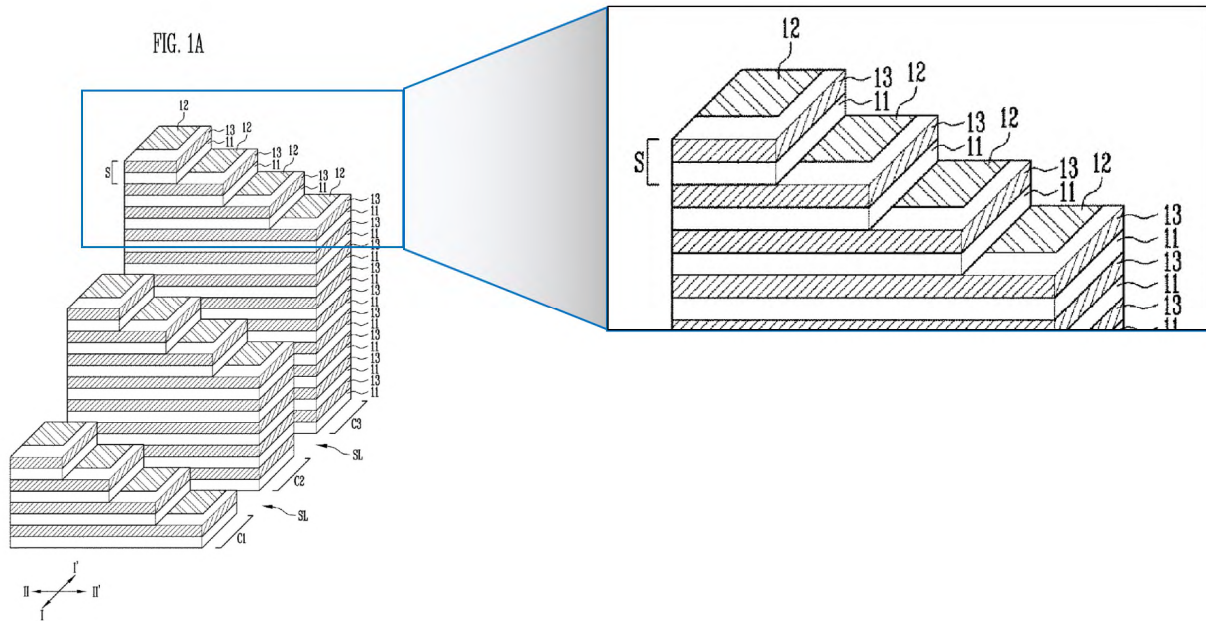


FIG. 3

Thimmegowda, Fig. 3; *see also id.*, 9:27-38. Thimmegowda discloses that layers 310a-d and 320a-d are dielectric layers. *Id.*, 8:34-38, 8:4-50, 8:57-61, 8:67-9:6. These dielectric layers extend horizontally to form corresponding dielectric layers in the wordline staircase 330 and wordline bridge 306. Thus, for example, layers 310d (and corresponding layer 320d) form one layer of the claimed *dielectric pair*. *Id.* The same is true for layers 310c/320c and 310b/310b. *Id.*; Banerjee, ¶¶ 127-28.

Applying Lee’s “finger” approach to Thimmegowda’s staircase/bridge architecture (*see* §IX.A), provides the other layer of the *dielectric pair*. In particular, Lee’s Fig. 1A discloses a step “S” comprised of a lower insulating layer 11 beneath a dielectric layer 12 and conductive finger 13. Lee, [0022]. The combination of

dielectric layers 11 and 12 form a *dielectric pair*. As shown below, each step S in Lee is *above one or more dielectric pairs*. *Id.*



Id., Fig. 1A. Lee further discloses that “in order that the pad region U_13A of the upper conductive layer U_13A may not overlap with the pad region L_13A of the lower conductive layer L_13, the dielectric layer L_12 may be located under the pad region U_13A of the upper conductive layer U_13.” *Id.*, [0031]; Banerjee, ¶ 129.

In like manner, applying Lee's finger approach to Thimmegowda also results in a staircase structure that maintains *a stair above one or more dielectric pairs*, where the *dielectric pair* comprises one dielectric layer 310/320 in combination with the dielectric layer 12 from Lee. Thus, in the modified version of Thimmegowda, each stair (except for the bottom stair) is *a stair above one or more dielectric pairs*. Banerjee, ¶ 130.

7. **[1.F] “wherein: the stair comprises a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure, and”**

As an initial matter, as to *conductor portion*, the ’604 specification states that it “covers at least the landing area of the respective stair (e.g., a portion of the stair)” for a staircase contact. Ex. 1001, 5:25-62. “[T]he dimension of the conductor portion, along the direction the stairs extend ... does not laterally extend under [] the conductor portion of any upper stair.” *Id.* But the ’604 specification also teaches that “along the x-direction, a width d of conductor portion 320 may be equal to *or less than* the dimension of stair 314.” *Id.*, 11:19-21. Either way, the result is a staircase where all layers under the landing area of any given step are comprised solely of dielectric. *Id.* The ’604 specification teaches that the thickness of the “conductor portion” (in the z-direction) may be the full depth of the sacrificial gate replacement layer 324. *See, e.g., id.*, 11:36-40 (“Along the z-direction, a thickness of conductor portion 320 may be equal to or less than that of dielectric portion 324.”); *id.*, 10:65-11:6.

Thimmegowda discloses a *stair compris[ing] a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure*. In particular, as highlighted by representative examples in Thimmegowda Fig. 3 below, the top/exposed surface of steps 332a-d are the *conductor portions* and

connect to respective conductive metal layers in wordline bridge 306. Banerjee, ¶¶ 131-32.

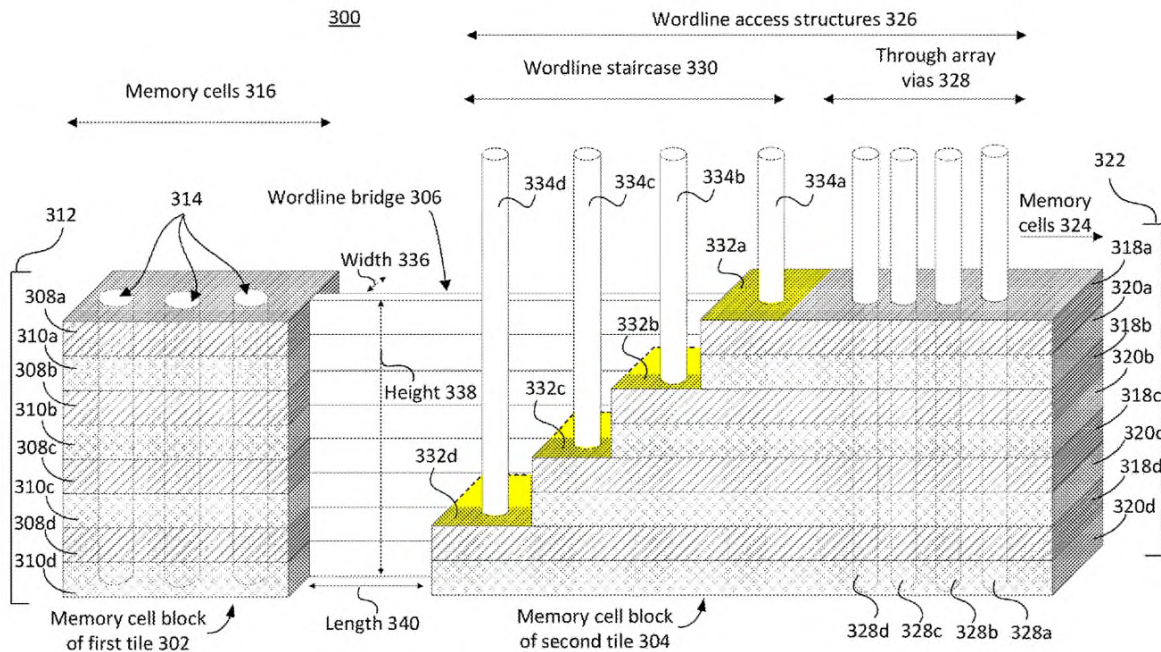


FIG. 3

Thimmegowda, Fig. 3.

Thimmegowda’s “wordline staircase 330 provides access to the wordlines 318 for metal contacts 334.” Thimmegowda, 9:42-45. “The wordline bridge 306 electrically couples the wordlines 308 to the wordlines 318 to enable the wordline access structures 326 to access the wordlines 308.” *Id.*, 9:46-48. Thus, Thimmegowda satisfies element 1[f]. *Id.*, 9:27-48; Banerjee, ¶ 133.

Moreover, Thimmegowda in view of Lee’s “finger” teachings also satisfies element 1[f]. Specifically, in view of these teachings, the landing pads of

Thimmegowda are in direct contact with the bridge, similar to how Lee’s “upper conductive layer U_13 [] include[s] a pad region U_13A surrounding the terminal third sidewall <3>” that is in physical contact with the “connection region U_13B” (analogous to Thimmegowda’s wordline bridge) for connecting to the wordlines in the memory array as shown in Figs. 1B and 1C. Lee, [0030]. In view of these teachings, it would have been obvious for “fingers” (as Lee teaches) to flow into the Thimmegowda bridge (in the Y direction) to enable the wordline contacts to couple to the bridge. Banerjee, ¶ 134; §IX.A.

FIG. 1B

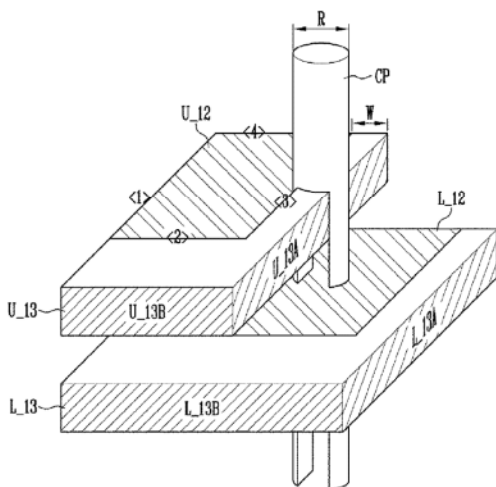
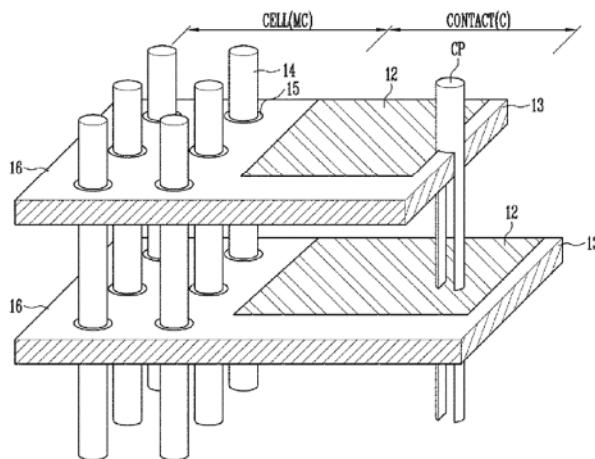


FIG. 1C



Lee, Figs. 1B and 1C. Regardless of whether the conductor portion in the modified version of Thimmegowda covers the entire step surface (as Thimmegowda itself discloses) or is modified to a narrower profile akin to that shown above in Lee (both

of which are obvious), Thimmegowda in view of Lee satisfies element 1[f]. Banerjee, ¶ 134.

8. **[1.G] “wherein: the stair comprises ... a dielectric portion at a same level and in contact with the conductor portion, the stair being electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure; and”**

For the reasons described for element 1[f], Thimmegowda discloses that the stair is *electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure*. See, e.g., Thimmegowda, 12:50-13:2, 9:27-49. That is what allows the metal contacts 334 to drive the memory arrays on both the left and right sides of the staircase structure. *Id.*, 7:61-64. The modified version of Thimmegowda’s bridge structure is no different in this regard (the fingers electrically connect the stairsteps to the bridge and in turn to the arrays). Banerjee, ¶ 135; Claim 1[F].

But Thimmegowda alone does not disclose the balance of element [1.G]. However, the same obvious modification to Thimmegowda discussed in claims [1.E-F] (employing Lee’s finger approach) does satisfy all aspects of element [1.G]. As an initial matter, Fig. 3A illustrates the meaning of *a dielectric portion at a same level and in contact with the conductor portion*. Annotated Fig. 3A below shows alternating layers of dielectric layer 326 and dielectric portion 324 that form stairs 314. The “dielectric portion 324” is located immediately adjacent to (in the x-

direction), and in contact with, conductor portion 320. The '604 patent explains that “[c]onductor portion 320 may be in contact with a dielectric portion 324 (e.g., extending along the x-direction) **of the same level.**” Ex. 1001, 10:60-61.

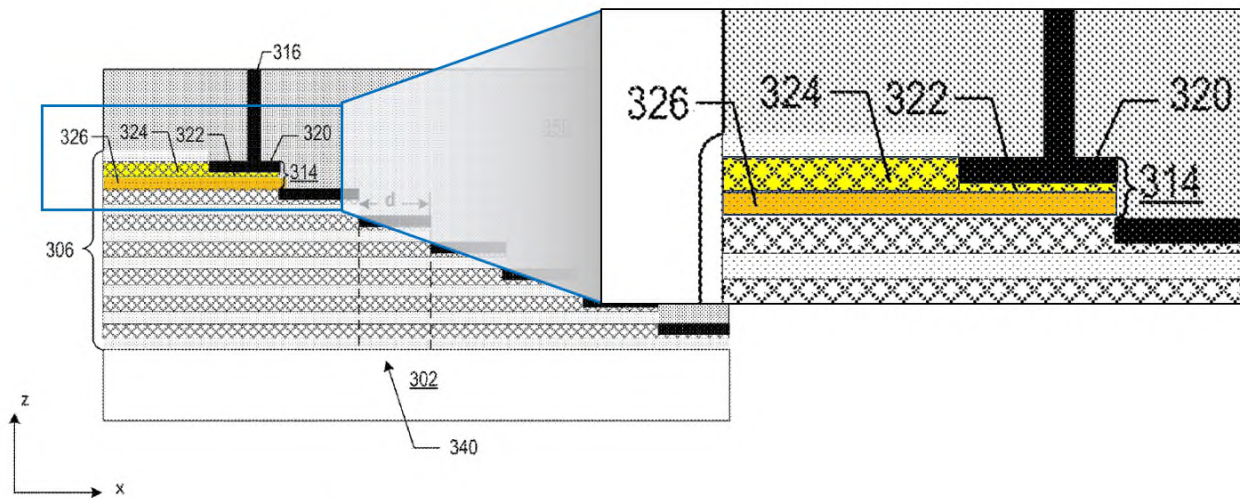


FIG. 3A

Id., Fig. 3A. While dielectric portion 324 also extends underneath conductor portion 320 in the example above, that is not the case when conductor portion 320 extends further in the z-direction. The '604 patent expressly (and repeatedly) discloses that the conductor portion can be the same depth as the sacrificial gate replacement layer 324. *See, e.g., id.*, 11:36-40 (“Along the z-direction, a thickness of conductor portion 320 may be equal to or less than that of dielectric portion 324.”); *id.*, 10:65-11:1 (“conductor portion 320 may be on and in contact with dielectric layer 326 without any second dielectric portion 322 in between.”); Banerjee, ¶ 136.

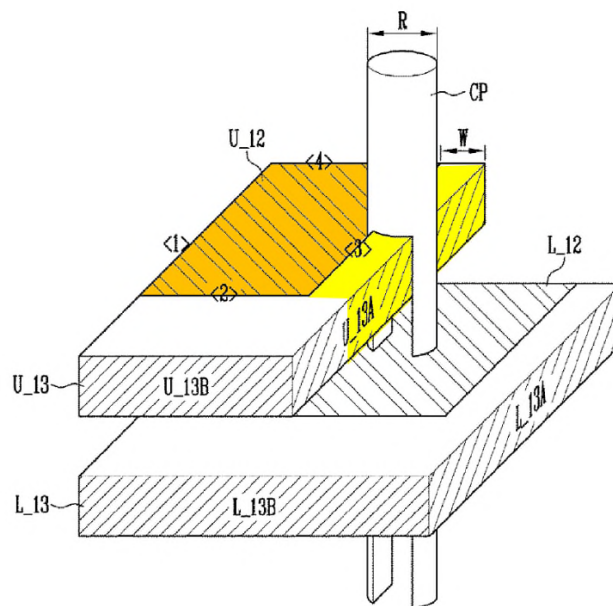
In both the unmodified and modified version of Thimmegowda, the *conductor portion* extends in the z-direction substantially the full depth of the conductive wordline layers 308a-d and 318a-d. See Thimmegowda, Fig. 3, 9:49-51 (“The wordline bridge 306 includes the same layers as the wordline stacks 312, 322”); Lee, Fig. 1A (conductor 13), Fig. 1B (conductors U_13A and L_13A); Claim [1.E-F]; Banerjee, ¶ 137.

And, as claims [1.E-F] explain, in the modified version of Thimmegowda the resulting conductors on staircase steps 332a-d are approximately the width of the step (as shown in Thimmegowda Fig. 3) or narrower (as shown in Lee Fig. 1B) and extend laterally in the y-direction to directly contact the wordline bridge 306. This is similar to how Lee’s conductive strips (*e.g.*, U_13A and L_13A in Fig. 1B) are in physical and electrical contact with the wordlines. See Lee, Fig. 1C; §IX.A. In modified Thimmegowda, the area immediately adjacent to the finger (in the x-direction toward the righthand memory array) is an insulator (*viz.*, *dielectric portion*), similar to what Lee illustrates (and describes) in Fig. 1B. Lee, [0028]; *id.*, [0029] (“[T]he upper dielectric layer U_12 may include four sidewalls <1> to <4>. ... The third sidewall <3> may be ... surrounded by the upper conductive layer U_13.”); Banerjee, ¶ 138.

Lee Fig. 1B below shows *a dielectric portion* [insulating portion U_12, highlighted in orange] which was not replaced during the gate replacement process

at a same level and in contact with the conductor portion [landing pad U_{13A}, highlighted in yellow]. Lee, [0028], [0048]. Applying this teaching to Thimmegowda, the dielectric material remaining after replacing portions of the sacrificial layer with the conductive finger is *at a same level and in contact with the conductor portion* [the finger]. See Claims [1.E-F]; §IX.A. This is true regardless of whether the *conductor portion* (viz., the finger) in modified Thimmegowda is the full width of the exposed landing pad area of a step or a narrower conductive strip (as in Lee). Banerjee, ¶ 139.

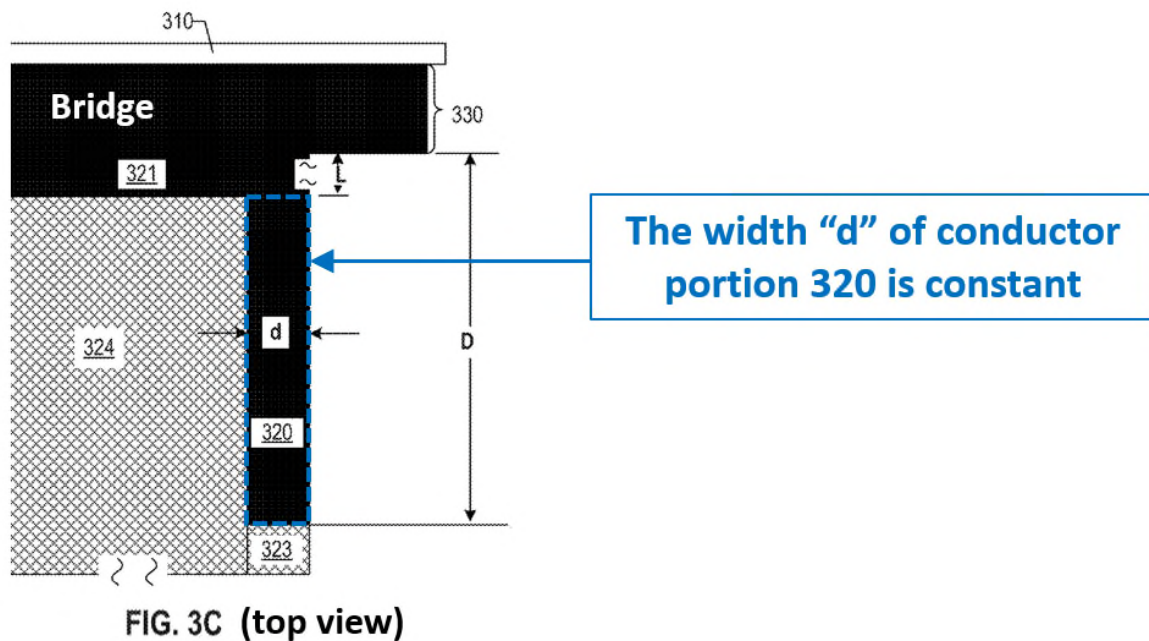
FIG. 1B



Lee, Fig. 1B.

9. [1.H] “along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.”

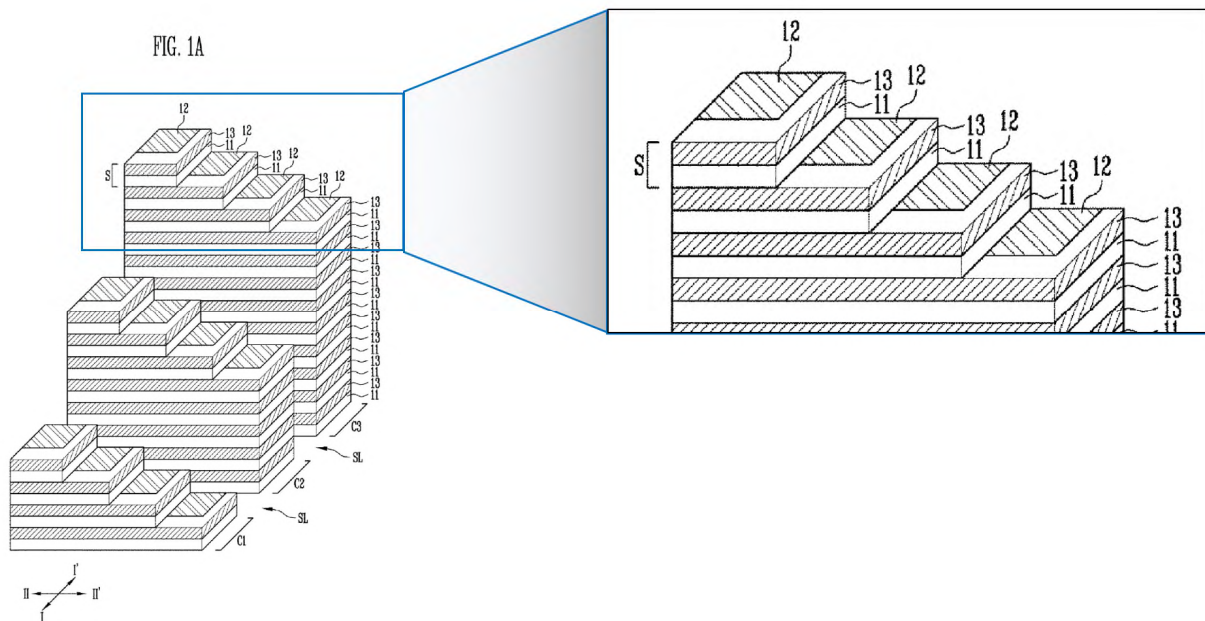
A POSITA would have understood the claimed *second lateral direction perpendicular to the lateral direction* at least includes the y-direction. Banerjee, ¶ 140. In other words, element 1[h] requires that the width of the *conductor portion* in the x-direction remains unchanged as the conductor portion extends in the y-direction toward the bridge. *Id.*; Ex. 1001, 11:19-24. This is illustrated in '604 patent Fig. 3C below, which is a top view showing the dimensions of the conductor portion in the x- and y-directions.



Id., Fig. 3C; see also *id.*, 13:10-14 (“th[e] width d of conductor portion 320 may be unchanged along the y-direction.”).

C. Claim 2 “The 3D memory device of claim 1, wherein the stair further comprises: a dielectric layer under the conductor portion and the dielectric portion.”

Thimmegowda in view of Lee’s teachings of a conductive finger renders obvious claim 2. As shown below in Lee Fig. 1A, each step “S” has an insulating layer 11 (*a dielectric layer*) beneath a conductive finger 13 (*the conductor portion*) and dielectric 12 (*the dielectric portion*). Lee, [0022].



Id., Fig. 1A. In similar fashion, when applying these teaching to Thimmegowda, each step has a *dielectric layer* (e.g., dielectric 310a-d and 320a-d) under the *conductor portion* (the conductive finger on steps 332a-d) and *the dielectric portion* (the remaining sacrificial material on steps 332a-d). Banerjee, ¶ 143; *see also* claim [1.E] (showing arrangement of dielectric pair).

E. Claim 4 “The 3D memory device of claim 2, wherein along the lateral direction, a width of the conductor portion is equal to a dimension of the stair.”

Modified Thimmegowda satisfies claim 4. In one obvious modification of Thimmegowda (discussed in §IX.A), the conductive finger width in the x-direction is co-extensive with the exposed surface area of the step (instead of the narrow finger), and thus the *width of the conductor portion* in the x-direction (viz., *the lateral direction*) *is equal to a dimension of the stair* (viz., the width of the step in the x-direction). See §IX.A; Banerjee, ¶ 146.

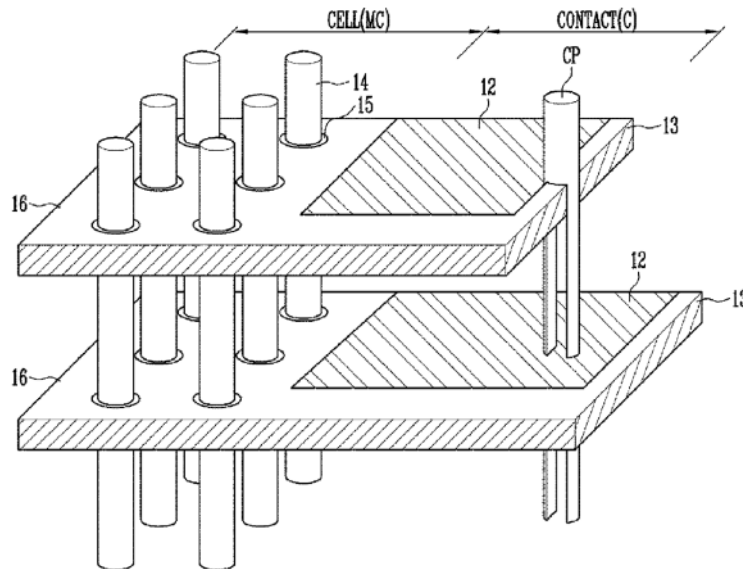
F. Claim 5 “The 3D memory device of claim 1, wherein along the second lateral direction perpendicular to the lateral direction, a length of the conductor portion is equal to or less than a second dimension of the stair.”

The *second lateral direction* is the y-direction in the '604 patent (see element [1.H]). A POSITA would have understood that the *second dimension of the stair* refers to the length of the step in the y-direction toward the bridge. Thimmegowda in view of Lee's finger teaching renders obvious claim 5. In this combination, the conductive finger in modified Thimmegowda extends the full length of the step (in the y-direction toward wordline bridge 306), and is thus *equal to ... a second dimension of the stair* (i.e., the length of the step in the y-direction). See [1.H] and §IX.A; Banerjee, ¶ 147.

Lee Fig. 1C shows the “finger” (conducting layer 13) extends the full step length (i.e., it reaches the wordline bridge running horizontally in the x-direction

toward the memory array), reinforcing that modifying Thimmegowda's bridge structure in view of Lee's teachings satisfies claim 5. Banerjee, ¶¶ 148-49.

FIG. 1C



Lee, Fig. 1C.

G. Claim 8

Thimmegowda in view of Lee renders obvious claim 8 (including each element).

1. **[8.A] “The 3D memory device of claim 1, wherein: the conductor portion comprises at least one of tungsten, cobalt, copper, aluminum, silicides, or polysilicon;”**

Thimmegowda discloses polysilicon gate layers. Thimmegowda, 5:63-66. However, §IX.A demonstrates that it would have been obvious to use the gate line replacement process of Lee to form the conductive gates, and it was well-known

when using gate replacement processes to use conductive materials such as tungsten, copper, and aluminum. Ex. 1017, [0049]. And Lee discloses tungsten gate layers. Lee, [0023], [0044]; Banerjee, ¶ 150.

2. [8.B] “the dielectric portion comprises silicon nitride; and”

The *dielectric portion* in Thimmegowda and Lee combination was discussed in connection with element [1.G] (which is the remaining portion of the sacrificial gate). And it would have been obvious to employ a gate replacement process. See element [8.A]. It was well-known that a common sacrificial material used as part of a gate replacement process was silicon nitride. See Ex. 1018, 132 (“sacrificial nitride layers.”); Ex. 1019, [0050] (“[T]he additional insulating structures 106 are formed of and include silicon nitride (Si₃N₄).”); Banerjee, ¶ 151.

This comports with Lee’s process for forming the “L-shaped” fingers. See Lee, [0048]-[0055]. Lee discloses that “first openings OP1 may be formed by partially removing the sacrificial layers 42 exposed on a sidewall of the stacked structure ST,” resulting in “an L shape.” *Id.*, [0048]. Subsequently, “conductive layers 46 are formed” in the openings and “have substantially an L shape.” *Id.*, [0055]. And Lee expressly discloses that “sacrificial layers 42 which are not removed” remain as part of the overall interconnection structure. *Id.*

Lee further discloses that “the sacrificial layers 42 may *include a nitride*.” *Id.*, [0044]; see also *id.*, [0023] (“[T]he dielectric layers 12 [which also map to the

claimed *dielectric portion*] may be formed of the remaining portions of sacrificial layers used in the manufacturing process, and include a nitride.”). Lee’s express disclosure of a dielectric portion that includes a nitride further renders obvious a *dielectric portion compris[ing] silicon nitride*, as such a material was a well-known and commonly used insulator in semiconductor chips and 3D NAND memory devices. Banerjee, ¶ 152-53; *see, e.g.*, Ex. 1011, 2:58-59 (“The insulating layer 42 is a layer primarily including silicon nitride.”); Kobayashi, [0093] (same).

3. [8.C] “a dielectric layer is arranged under the conductor portion and the dielectric portion, the dielectric layer comprising silicon oxide.”

The only part of element 8[c] that is different than claim 2 is that *the dielectric layer comprising silicon oxide*.

The claimed *dielectric layer* in Thimmegowda (modified or unmodified) is the insulating layer 310a-d/320a-d. Thimmegowda, 9:49-50, 8:34-38, 8:57-60. And Thimmegowda discloses “[t]he dielectrics 310 are oxide layers, ... The *dielectrics 310 are silicon dioxide layers*, ... The dielectrics 320 are oxide layers, ... The *dielectrics 320 are silicon dioxide layers*.” *Id.*, 8:44-9:6; Banerjee, ¶¶ 154-55.

H. Claim 9

Thimmegowda in view of Lee renders claim 9 obvious. As noted below, claim 9 is similar to, and broader than, claim 1 in several respects.

1. **[9.PRE] “A three-dimensional (3D) memory device, comprising:”**

If limiting, the preamble of claim 9 is satisfied for the same reasons as claim 1’s preamble.

2. **[9.A] “a memory array structure; and”**

Element 9[a] is met for the same reasons as element 1[a].

3. **[9.B] “a staircase structure comprising a plurality of stairs extending along a lateral direction,”**

Elements 1[b] and 1[c] collectively require everything recited by element 9[b]. Accordingly, element 9[b] is satisfied for the same reasons as elements 1[b] and 1[c].

1. **[9.C] “a stair comprising a conductor portion on a top surface of the stair and a dielectric portion at a same level and in contact with the conductor portion, the conductor portion being electrically connected to the memory array structure,”**

Elements 1[f] and 1[g] collectively require everything recited by element 9[c], except that 9[c] requires the *conductor portion* (instead of just *the stair*) be *electrically connected to the memory array structure*. As explained for element 1[g], in modified Thimmegowda the *conductor portion* of the stair (not the dielectric or insulator portion of the stair) electrically connects the stair to the memory array. Accordingly, Thimmegowda in view of Lee satisfies element 9[c] for the same reasons elements 1[f] and 1[g] are satisfied. Banerjee, ¶ 160. A comparison of

element 9[c] with elements 1[f] and 1[g] is provided below, with corresponding elements shown in the same colors.

Element 9[c]	Elements 1[f] and [g]
a stair comprising a conductor portion on a top surface of the stair and	the stair comprises a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure, and
a dielectric portion at a same level and in contact with the conductor portion,	a dielectric portion at a same level and in contact with the conductor portion,
the conductor portion being electrically connected to the memory array structure	the stair being electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure; and

2. [9.D] “wherein along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.”

Element 9[d] is the same as element 1[h] and is satisfied for the same reasons.

I. Claims 10-13

Claim 10-13 add the same limitations as claims 2-5, respectively, and are satisfied for the same reasons.

X. GROUND 2: THIMMEGOWDA IN VIEW OF KOBAYASHI AND A POSITA’S KNOWLEDGE

Thimmegowda in view of Kobayashi and the knowledge of a POSITA renders all Challenged Claims obvious.

A. Motivation Combine

A POSITA would have been motivated to combine the teachings of Thimmegowda with Kobayashi with a reasonable expectation of success. At the outset, it is important to note Petitioner is **not** proposing to bodily incorporate Kobayashi into Thimmegowda, or vice versa. Rather, Petitioner is combining Thimmegowda's bridge and array architecture teachings that enables a single staircase to bidirectionally drive two arrays and Lee's stairstep teachings that mitigate punch through. *See, e.g., In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Stated another way, obviousness ensues whether the combination is framed as Thimmegowda in view of Kobayashi or Kobayashi in view of Thimmegowda.

A POSITA would have been motivated to apply Kobayashi's teaching of non-overlapping conductive fingers to ameliorate the known problems (*e.g.*, short circuits) associated with punch through in Thimmegowda's staircase. As explained in §IX.A, the problem of overetching wordline via holes in 3D NAND staircase structures was well-known in the art. A POSITA would naturally look to existing solutions, like that proposed by Kobayashi, to address the punch-through problem (*e.g.*, to improve yield). Banerjee, ¶ 168. As discussed in §VI.C, Kobayashi discloses just such a solution using non-overlapping conductive fingers. Kobayashi, [0139]-[0145] ("Because the spacer portions 71 [] are insulating bodies, the contact CC is not shorted ... even when the contact CC reaches the spacer portions 71 of the

other layers lower than the [desired wordline]”). Both Kobayashi and Thimmegowda disclose 3D NAND memory devices that utilize a staircase structure to provide wordline contacts for accessing the memory arrays. See §§VI.A and VI.B. While Kobayashi discloses forming multiple “columns” of staircases (labeled columns 91-94), all of which employ the “finger” approach (see Kobayashi, Fig. 5), Kobayashi’s finger approach is readily applicable to the single staircase illustrated in Thimmegowda Fig. 3. Banerjee, ¶ 168.

In view of the combined teachings of Kobayashi and Thimmegowda, two implementations of Kobayashi’s finger approach would have been obvious to a POSITA. First, it would have been obvious to a POSITA to use a “thin” finger narrower (in the x-direction) than the width of a step since Kobayashi expressly discloses that approach. Kobayashi, Fig. 5, [0069] (“first conductive portion 70b”); Banerjee, ¶ 169.

Second, it would also have been obvious to a POSITA to make the conductive finger cover the full width of the step, especially given that Thimmegowda’s landing pad already did so. Thimmegowda, Fig. 3 (steps 332). As explained in §IX.A, other 3D NAND references like Nakaki already disclosed non-overlapping conductive fingers for accessing wordline. Ex. 1011, Fig. 55, 14:64-65. Also as explained in §IX.A, a POSITA would have readily understood that a conductive finger covering the full stair width mitigates the effects of punch through. Accordingly, a POSITA

would have found it obvious to use a full step-width conductive finger in view of the combined teachings of Kobayashi and Thimmegowda. Banerjee, ¶ 170.

Additionally, Kobayashi discloses using the well-known gate-replacement process (see §V.A), which provides additional motivation to combine Kobayashi and Thimmegowda. In particular, Kobayashi discloses forming its conductive fingers (and the memory device at large) using gate-replacement, which would benefit Thimmegowda's bridge and array architecture. Kobayashi, Figs. 7-33B, [0010]-[0012], [0087]-[0145]. For example, Kobayashi discloses using tungsten wordlines (Kobayashi, [0074], [0135]) which were known to substantially lower wordline resistance and provide faster memory read/write operations. See Ex. 1018, 131-32; Banerjee, ¶ 171. Moreover, employing Thimmegowda's bridge and architecture in Kobayashi would have provided the advantage of bidirectionally driving two arrays (§VI.A) using a single staircase, and would be complementary to Kobayashi's lower resistance from metal gates (via gate replacement). *Id.*

Reasonable Expectation of Success. A POSITA would have had a reasonable expectation of success in combining the teachings of Thimmegowda's bridge and array architecture (to drive two memory arrays with one wordline via) with Kobayashi's staircase finger approach (to mitigate punch through). Banerjee, ¶ 172. To begin, both Thimmegowda and relate to 3D NAND memory devices with memory arrays whose memory strings are accessed using wordline vias in contact

with individual steps in a staircase. *See* Thimmegowda, Fig. 3; Kobayashi, Figs. 1 and 29. Thus, the references share a number of key architectural similarities. In particular, combining Kobayashi's finger approach with Thimmegowda's bridge would not change the functionality of how wordline vias read/write memory cells (*viz.*, there would still be an electrically conductive path to the memory arrays). Likewise, applying Thimmegowda's bidirectional wordline bridge teachings to Kobayashi would not have any impact on how Kobayashi's finger approach mitigates punch through. Banerjee, ¶ 172.

And Thimmegowda's wordline bridge/staircase architecture is entirely compatible with Kobayashi's gate replacement manufacturing process. *Id.* Indeed, a POSITA would not be able to tell by looking at Thimmegowda Fig. 3 what type of manufacturing process (*e.g.*, gate replacement) was used, and would understand that no particular manufacturing process was required (*e.g.*, the wordline could be made of doped polysilicon or metal such as tungsten). Concerning manufacturing, Kobayashi provides detailed teachings regarding a gate replacement process for forming the fingers, and explains in how to manufacture the conductive fingers 70b and adjacent "spacer portions 71" formed of sacrificial dielectric material. *See* Kobayashi, Figs. 7-33B (and accompanying discussion at [0087]-[0144] describing the gate replacement manufacturing process in detail). More generally, gate replacement techniques well-known and well within the knowledge and skill of a

POSITA, and could readily be applied to form the bridge/staircase structure in Thimmegowda. Banerjee, ¶ 172; *see also, e.g.*, Ex. 1017, Figs. 1A-1F (illustrating formation of 3D NAND bridge using gate-replacement process). Accordingly, a POSITA would have had a reasonable expectation of success in combining the teachings of Kobayashi and Thimmegowda.

B. Claim 1:

Thimmegowda in view of Kobayashi renders claim 1 obvious.

1. Claim 1 Preamble and Elements 1[a]-[d].

Thimmegowda discloses the preamble and elements 1[a]-1[d] for the same reasons explained for Ground 1. Banerjee, ¶ 174.

2. [1.E] “the plurality of stairs comprising a stair above one or more dielectric pairs,”

Thimmegowda in view of Kobayashi renders this limitation obvious.

Thimmegowda discloses “steps 332” that form part of the staircase. *See* §IX.B.6; Thimmegowda, Fig. 3.

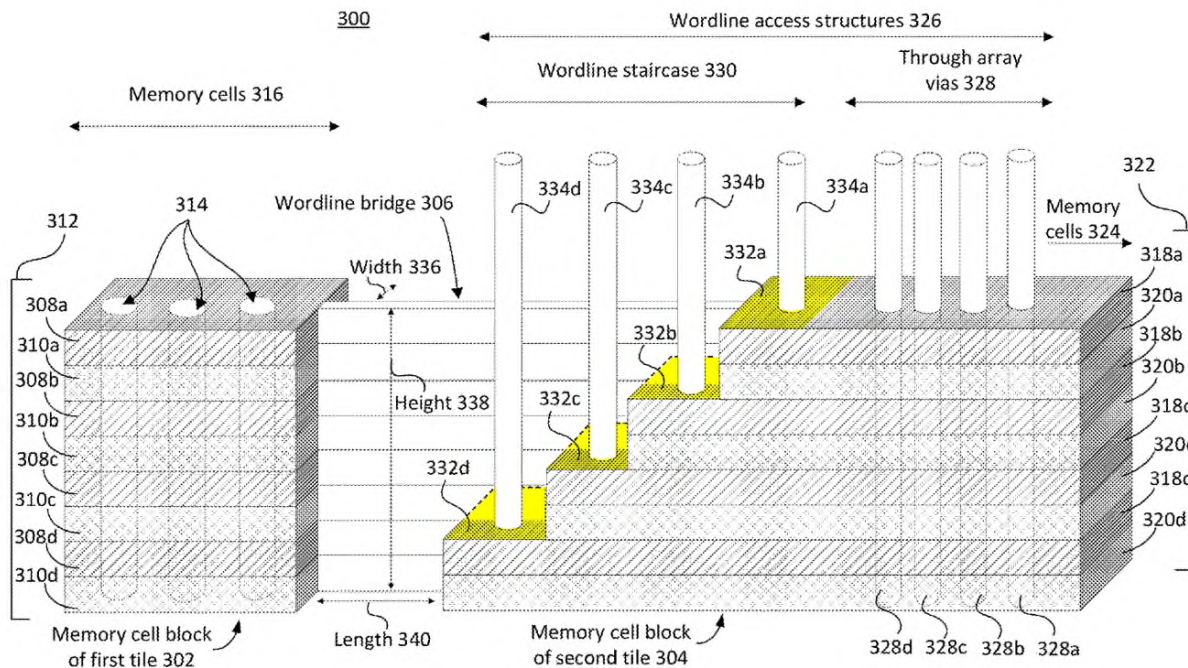
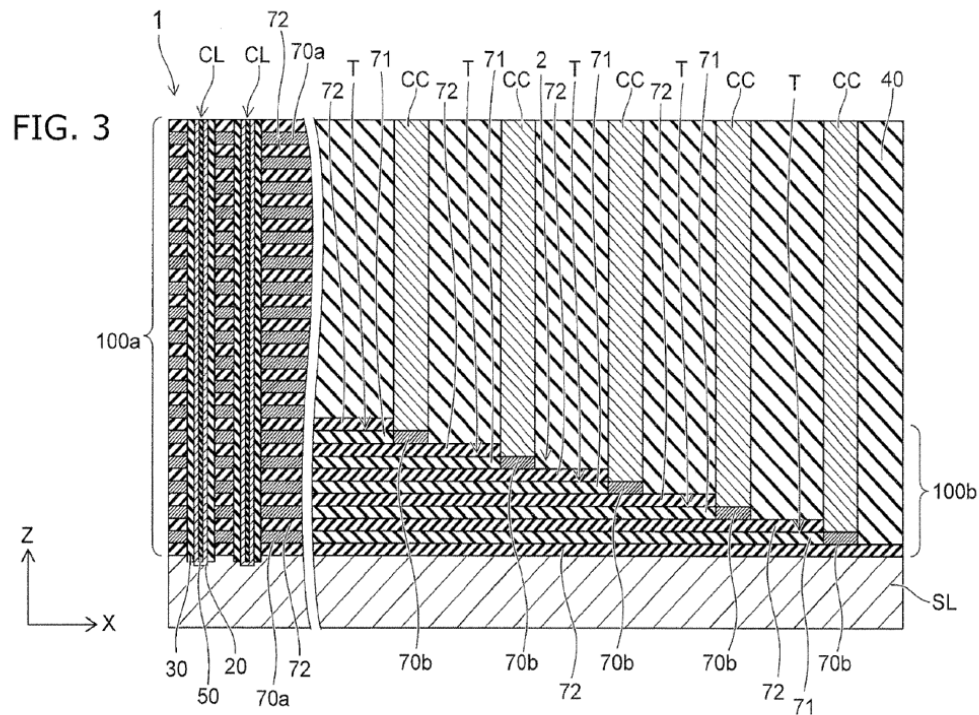


FIG. 3

Id., Fig. 3; *see also id.*, 9:27-38. Thimmegowda discloses that layers 310a-d and 320a-d are dielectric layers. *Id.*, 8:34-38, 8:4-50, 8:57-61, 8:67-9:6. These dielectric layers extend horizontally to form corresponding dielectric layers in the wordline staircase 330 and wordline bridge 306. Thus, for example, layers 310d (and corresponding layer 320d) form one layer of the claimed *dielectric pair*. *Id.*; Banerjee, ¶¶ 175-76.

Applying Kobayashi's "finger" approach to Thimmegowda's staircase/bridge as described in §X.A, provides the other layer of the *dielectric pair*. In Kobayashi's Fig. 3, for example, each step (except for the bottom step) is above a dielectric pair (comprised of sacrificial layer 71 and insulating layer 72) of a lower step. See

Kobayashi, [0070]-[0071], [0139] (“the sacrificial layers (the spacer portions) 71 and the insulating layers 72 [] are positioned at the portions lower than the upper surface of the first conductive portion 70b of the terrace portion T”). The combination of sacrificial spacer portion 71 and insulator 72 form a *dielectric pair*. Banerjee, ¶ 177.



Kobayashi, Fig. 3, Fig. 33A. As shown above, each step in Kobayashi is *above one or more dielectric pairs*. *Id.* Kobayashi further discloses that this arrangement avoids short circuits from punch through. *Id.*, [0141] (“the contact CC is not shorted . . . when the contact CC reaches the spacer portions 71 of the other layers.” *Id.*, [0141]; Banerjee, ¶ 177.

Applying Kobayashi’s finger approach to Thimmegowda results in a staircase structure maintaining *a stair above one or more dielectric pairs*, where the *dielectric pair* comprises a dielectric layer 310/320 in combination with the spacer 71 (*i.e.*, remaining sacrificial dielectric) from Kobayashi. Thus, in modified Thimmegowda, each stair (except for the bottom stair) is *a stair above one or more dielectric pairs*. Banerjee, ¶ 178.

3. [1.F] “wherein: the stair comprises a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure, and”

As Ground 1 explains for element 1[f], Thimmegowda discloses a *stair compris[ing] a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure*.

Thimmegowda in view of Kobayashi’s “finger” teachings and the knowledge of a POSITA also satisfies element 1[f]. In view of Kobayashi’s teaching, Thimmegowda’s landing pads are in direct contact with the bridge, similar to how Kobayashi’s finger-like “first conductive portion 70b” is in physical and electrical contact with the “second conductive portion 70c” (analogous to Thimmegowda’s bridge) for connecting to the wordlines in the memory array as shown in Figs. 1 and 5. Kobayashi, [0069]-[0074] (“The conductive layer 70a [*i.e.*, the wordline], the first conductive portion 70b, and the second conductive portion 70c are provided to

be continuous as one body of the same material [, such as] a metal layer including mainly tungsten.”). Banerjee, ¶¶ 179-81.

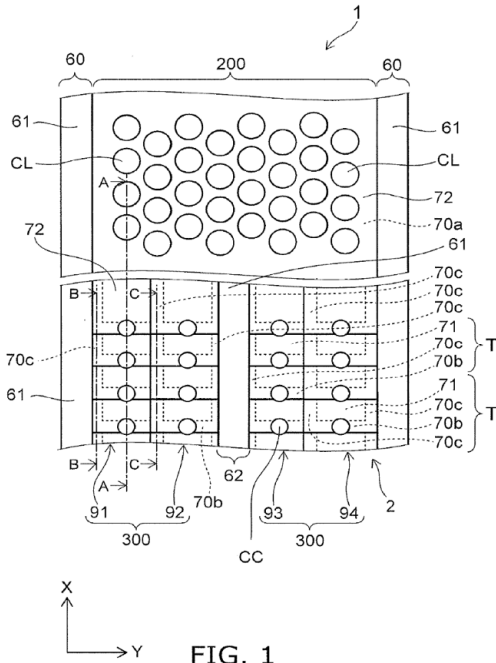


FIG. 1

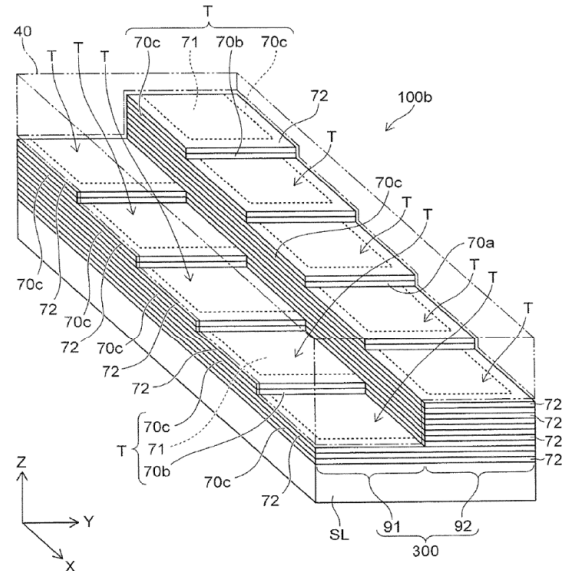


FIG. 5

Lee, Figs. 1 and 5. Regardless of whether the conductor portion in the modified version of Thimmegowda covers the entire step surface (as Thimmegowda itself discloses) or is modified to a narrower profile akin to that shown above in Kobayashi (both of which are obvious), modified Thimmegowda satisfies element 1[f]. §X.A; Banerjee, ¶ 182.

Note that Kobayashi’s top stair portion is the oxide layer of the stack, whereas the bottom comprises the conductor and dielectric portions. Kobayashi, Fig. 3, [0029]. However, it was widely known that when forming a staircase, interchangeable options include having the top or bottom portion the oxide layer,

and this grounds applies the obvious variation in which the oxide is on the bottom of the step. *E.g.*, Ex. 1029, (U.S. Pub. 2012/0070944), [0090] (“each of top surfaces of the insulating layers . . . constituting the stepwise stacked layer . . . may be partially exposed in the word line contact region WCTR. In other embodiments, each of top surfaces of the sacrificial layers . . ., not the top surfaces of the insulating layers . . ., may be partially exposed”), [0091] (same), [0240] (similar); Ex. 1030. (U.S. Pat. 10,026,692), Figs. 7A, 7B (showing each alternative). Further, it was known how to create the finger with the conductive layer on top, as Lee demonstrates. *See* § VI.B. Each arrangement is simply a choice among two options, both of which provide the beneficial staircase and finger structure, and the only difference is a minor change in manufacturing the staircase and finger. As Lee and the above reference demonstrate, it was well within a POSITA’s knowledge how to form the staircase and finger with the conductor portion on top. Banerjee, ¶ 182.

4. **[1.G] “wherein: the stair comprises ... a dielectric portion at a same level and in contact with the conductor portion, the stair being electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure; and”**

For the reasons described above in connection with element 1[f], Thimmegowda discloses that the stair is *electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure*. *See, e.g.*, Thimmegowda, 12:50-13:2, 9:27-48. That is what allows

the metal contacts 334 to drive the memory arrays on both the left and right sides of the staircase structure. *Id.*, 7:61-64. The modified version of Thimmegowda is no different in this regard. Banerjee, ¶¶ 183-84; §X.A.

Thimmegowda in view of Kobayashi renders obvious this limitation. In both the unmodified and modified version of Thimmegowda, the *conductor portion* extends in the z-direction substantially the full depth of the conductive wordline layers 308a-d and 318a-d. See Thimmegowda, Fig. 3, 9:49-51; Kobayashi, Fig. 3 (conductor 70b); §X.A; Banerjee, ¶ 185.

And, as §X.A explains, it would have been obvious in view of Kobayashi for the Thimmegowda conductors on staircase steps 332a-d to be approximately the width of the step (as shown in Thimmegowda Fig. 3) or narrower (as shown in Kobayashi Fig. 3 and Fig. 5) and extend laterally in the y-direction to directly contact the wordline bridge 306. Banerjee, ¶ 185. This is similar to how Kobayashi's conductive fingers (first conductive portions 70b) are in physical and electrical contact with the wordlines. See Kobayashi, Fig. 1, Fig. 3, [0073]-[0074] (“The conductive layer 70a, the first conductive portion 70b, and the second conductive portion 70c are provided to be continuous as one body of the same material.”).

In modified Thimmegowda, the area immediately adjacent to the finger (in the x-direction toward the righthand memory array) is an insulator, e.g., silicon nitride (*dielectric portion*), similar to Kobayashi's “spacer 71” illustrated in Figs. 1,

3, and 5. Kobayashi, [0069]-[0072], [0079]-[0082] (“The spacer portion 71 is provided on the inner side of the first conductive portion 70b and the second conductive portion 70c forming the L-shape. The spacer portion 71 is an insulating portion.”); Banerjee, ¶ 186.

As is readily apparent in Kobayashi Fig. 1 and 5 below, there is *a dielectric portion* [spacer portion 71 highlighted in orange] *at a same level and in contact with the conductor portion* [first conductive portion 70b, highlighted in yellow]. Applying these teachings to Thimmegowda, the dielectric material left after replacing portions of the sacrificial layer with metal is *at a same level and in contact with the conductor portion* [the finger]. *Id.*; §X.A. This is true regardless of whether the *conductor portion* (i.e., the finger) in modified Thimmegowda is the full width of the exposed landing pad area of a step or a narrower conductive strip (as in Lee). Banerjee, ¶ 186.

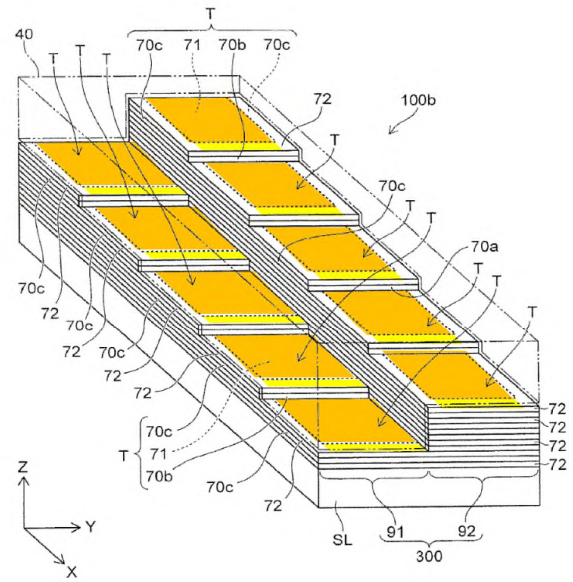
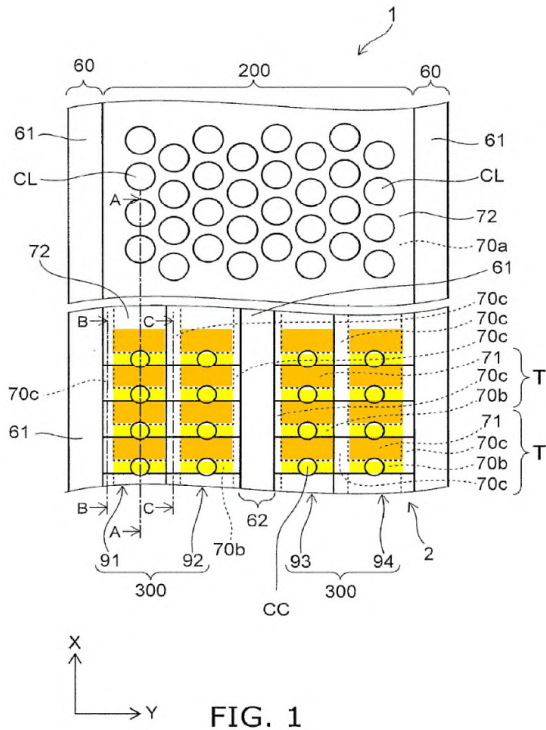


FIG. 5

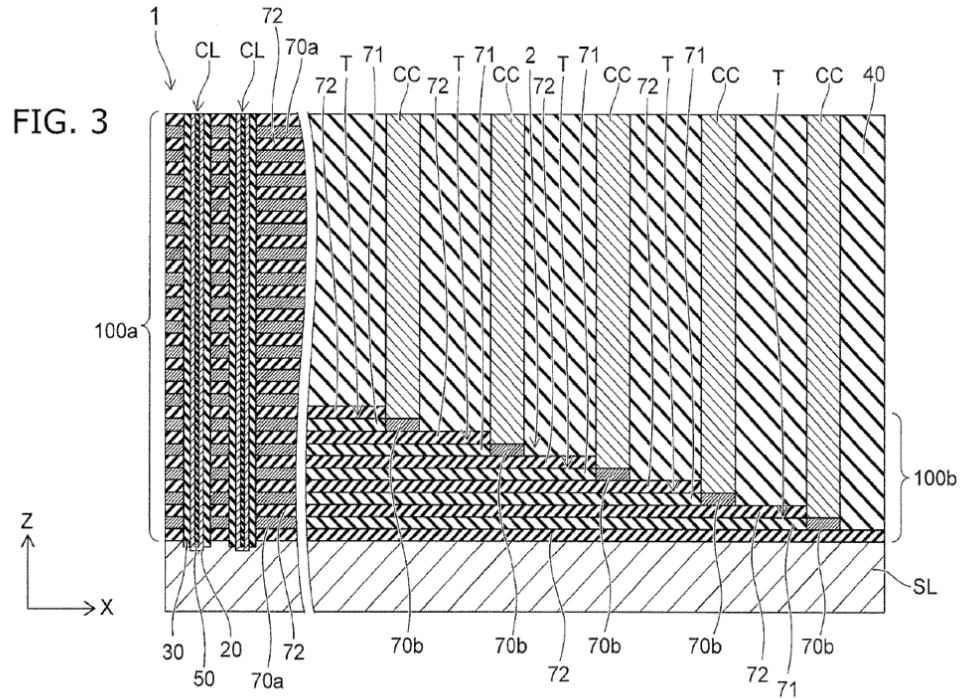
Id., Figs. 1 and 5.

Thimmegowda in view of Kobayashi renders obvious element 1[h]. Applying Kobayashi's teachings, the conductive finger in Thimmegowda's staircase maintains the same width (in the x-direction) as it proceeds in the y-direction to connect to wordline bridge 306 (the *bridge*). This is true regardless of whether the width of the conductor portion is narrow (as shown in Kobayashi) or covers the entire surface area of the step. See §X.A; Banerjee, ¶¶ 187-89.

C. Claim 2 “The 3D memory device of claim 1, wherein the stair further comprises: a dielectric layer under the conductor portion and the dielectric portion.”

Thimmegowda in view of Kobayashi's finger teachings renders obvious claim 2. Kobayashi's Fig. 3 shows each step (except the bottom step) has a *dielectric layer*

(insulating layer 72) under *the conductor portion* (first conductive portion 70b) and *the dielectric portion* (spacer 71). See Kobayashi, [0139]-[0143].

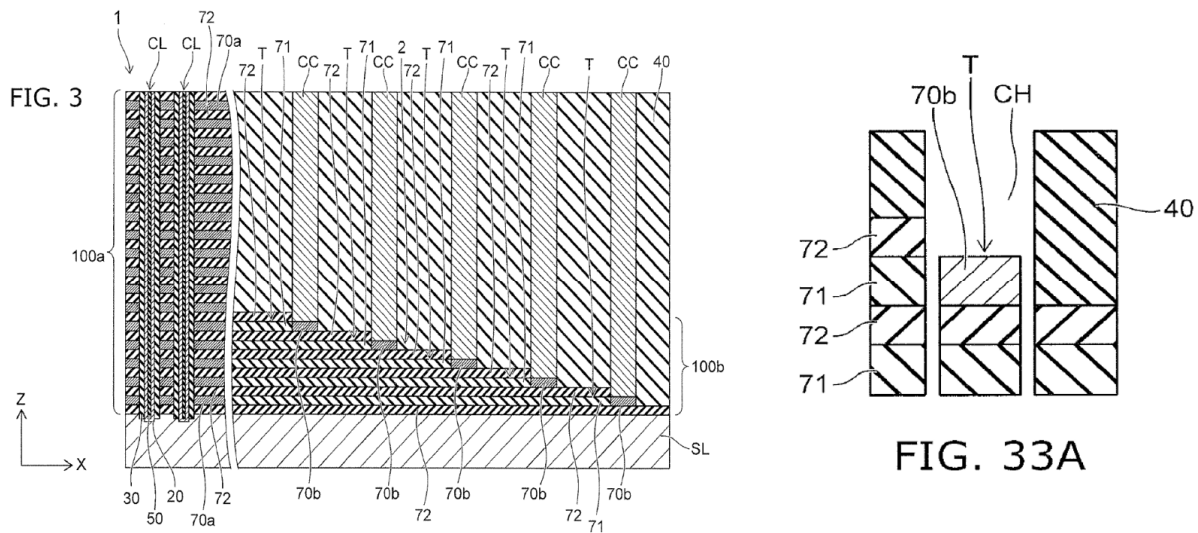


Id., Fig. 3, Fig. 33A. When applying these teaching to Thimmegowda, each step has a *dielectric layer* (e.g., dielectric 310a-d and 320a-d) under the *conductor portion* (the conductive finger on steps 332a-d, akin to Kobayashi’s first conductive portion 70b) and *the dielectric portion* (the remaining sacrificial material on steps 332a-d, akin to Kobayashi’s spacer 71). Banerjee, ¶ 190; §X.A.

D. Claim 3 “The 3D memory device of claim 2, wherein the conductor portion and the dielectric layer are each above the one or more dielectric pairs.”

For the same reasons explained in connection with element 1[e], Thimmegowda in view of Kobayashi satisfies claim 3. §X.B.2. As Kobayashi’s

Figs. 3 and 33 demonstrate, each step (except the bottom step) has a conductive portion 70b (*the conductor portion*) and insulating layer 72 (*the dielectric layer*) that are *above the one or more dielectric pairs* (i.e., the combination of spacer 71 and insulating layer 72 in the underlying step(s)). See Kobayashi, [0138]-[0142]; Banerjee, ¶ 191.



Kobayashi, Fig. 3, Fig. 33A. When applying these teaching to Thimmegowda, *the conductor portion* (the conductive finger on steps 332a-d) *and the dielectric layer* (dielectric layers 310a-c and 320a-c) *are each above the one or more dielectric pairs* (viz., the combination of the remaining sacrificial material on steps 332b-d and their respective insulating layer 310b-d/320b-d in the underlying step(s)). Banerjee, ¶ 191.

E. Claim 4 “The 3D memory device of claim 2, wherein along the lateral direction, a width of the conductor portion is equal to a dimension of the stair.”

Thimmegowda in view of Kobayashi renders obvious claim 4. In one obvious modification of Thimmegowda (see §X.A), the width of the conductive finger in the x-direction is co-extensive with the exposed surface area of the step, and thus the *width of the conductor portion* in the x-direction (viz., *the lateral direction*) *is equal to a dimension of the stair* (viz., the width of the step in the x-direction). Banerjee, ¶ 192.

F. Claim 5 “The 3D memory device of claim 1, wherein along the second lateral direction perpendicular to the lateral direction, a length of the conductor portion is equal to or less than a second dimension of the stair.”

Element 1[h] explains that the *second lateral direction* is the y-direction and the *second dimension of the stair* is the y-direction toward the bridge. Thimmegowda in view of Kobayashi renders obvious claim 5. In view of Kobayashi’s teaching, the conductive finger extends the full length of the step (in the y-direction toward wordline bridge 306), and is thus *equal to ... a second dimension of the stair* (i.e., the length of the step in the y-direction). See §X.A; Banerjee, ¶ 194.

Moreover, the highlighted portions of Kobayashi Figs. 1 and 5 illustrate protruding “finger” (first conductive portion 70b) extends the full step length (i.e., until it reaches the wordline bridge running horizontally in the x-direction toward

the memory array), reinforcing that modifying Thimmegowda's staircase structure in accordance with Kobayashi's teachings satisfies claim 5. See §X.A; Banerjee, ¶ 194.

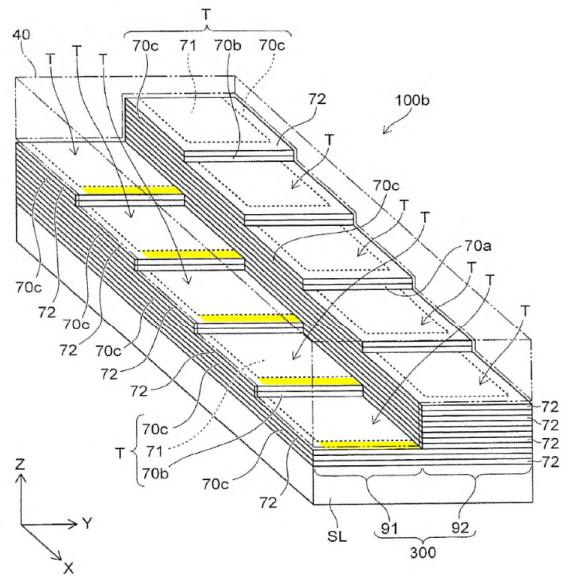
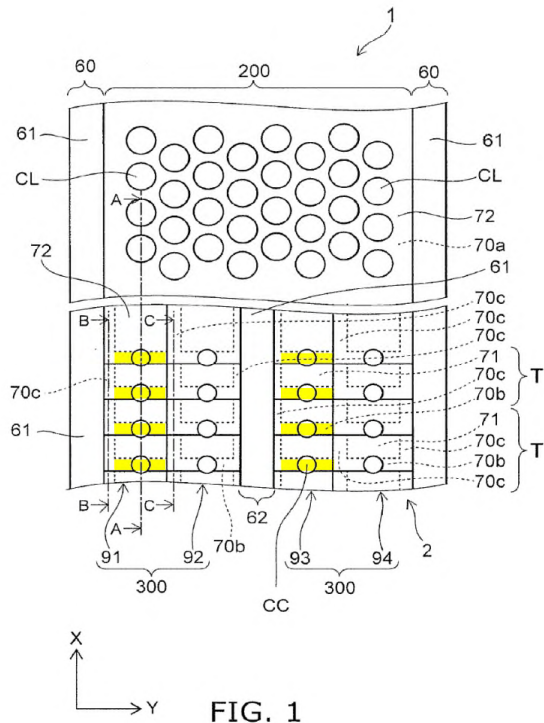


FIG. 5

Kobayashi, Figs. 1 and 5.

G. Claim 8

Thimmegowda in view of Kobayashi renders claim 8 obvious (including each element).

1. [8.A] “The 3D memory device of claim 1, wherein: the conductor portion comprises at least one of tungsten, cobalt, copper, aluminum, silicides, or polysilicon;”

Thimmegowda discloses that its wordlines are polysilicon. Thimmegowda, 5:63-66. However, §X.A demonstrates that in view of Kobayashi, it would have

been obvious to use a gate replacement process in the Thimmegowda and Kobayashi ground, and thus the conductive portions are the replacement gates. And Kobayashi discloses its “first conductive portion 70b ... [is] a metal layer including mainly tungsten,” which is from the gate replacement process. Kobayashi, [0074]; *see also id.*, [0135] (similar), [0133] (replacement). Tungsten was the typical metal for the gate replacement process. *See, e.g.*, Ex. 1017, [0049]; Banerjee, ¶ 196.

2. [8.B] “the dielectric portion comprises silicon nitride; and”

The *dielectric portion* in modified Thimmegowda in view of Kobayashi was discussed in connection with element 1[g] (§X.B.4). And the obvious use of a gate replacement process (like that described in Kobayashi) for this combination was discussed in §§X.A, X.G.1. Kobayashi discloses that “the sacrificial layer 71,” which is used to form the spacer portion 71, “is, for example, a silicon nitride layer” (the typical sacrificial gate material). Kobayashi, [0080]; [0093], [0096], [0113], [0117], [0122], [0141] (“silicon nitride”); Banerjee, ¶ 197.

3. [8.C] “a dielectric layer is arranged under the conductor portion and the dielectric portion, the dielectric layer comprising silicon oxide.”

The only part of element 8[c] that is different than claim 2 is that *the dielectric layer comprising silicon oxide*. The claimed *dielectric layer* in Thimmegowda (modified or unmodified) is the insulating layer 310a-d/320a-d. *See* §IX.G.C; Banerjee, ¶ 198.

H. Claim 9

Thimmegowda in view of Kobayashi renders claim 9 obvious. As noted below, claim 9 is similar to, and broader than, claim 1 in several respects.

1. **[9.PRE] “A three-dimensional (3D) memory device, comprising:”**

If limiting, the preamble of claim 9 is satisfied for the same reasons as claim 1’s preamble.

2. **[9.A] “a memory array structure; and”**

Element 9[a] is met for the same reasons as element 1[a].

3. **[9.B] “a staircase structure comprising a plurality of stairs extending along a lateral direction,”**

Elements 1[b] and 1[c] collectively require everything recited by element 9[b]. Accordingly, element 9[b] is satisfied for the same reasons as elements 1[b] and 1[c].

4. **[9.C] “a stair comprising a conductor portion on a top surface of the stair and a dielectric portion at a same level and in contact with the conductor portion, the conductor portion being electrically connected to the memory array structure,”**

As explained in connection with Ground 1, elements 1[f] and 1[g] collectively require everything recited by element 9[c], except that 9[c] requires the *conductor portion* (instead of just *the stair*) be *electrically connected to the memory array structure*. But, as explained in connection with element 1[g], in modified Thimmegowda the *conductor portion* of the stair (not the dielectric or insulator

portion) electrically connects the stair to the memory array. Accordingly, modified Thimmegowda satisfies element 9[c] for the same reasons as 1[f] and 1[g]. Banerjee, ¶ 203.

5. [9.D] “wherein along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.”

Element 9[d] is the same as element 1[h] and is satisfied for the same reasons.

I. Claims 10-13

Claim 10-13 add the same limitations as claims 2-5, respectively, and are satisfied for the same reasons.

XI. SECONDARY CONSIDERATIONS

There is no evidence in the prosecution history of this or any related application or patent that any arguments regarding secondary considerations exist. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XII. CONCLUSION

Petitioner respectfully requests the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

Dated: October 11, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,938 words.

Dated: October 11, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated documents and exhibits were caused to be served on October 11, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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Petition for *Inter Partes* Review of U.S. Patent No. 11,450,604

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