

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00035
U.S. Patent No. 11,450,604
Issue Date: September 20, 2022

Title: STAIRCASE STRUCTURE IN THREE-DIMENSIONAL
MEMORY DEVICE AND METHOD FOR FORMING THE SAME

**DECLARATION OF SANJAY BANERJEE, Ph.D., IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 11,450,604**

	<u>TABLE OF CONTENTS</u>	<u>Page</u>
I.	INTRODUCTION	8
II.	QUALIFICATIONS.....	9
III.	COMPENSATION	13
IV.	MATERIALS CONSIDERED	13
V.	UNDERSTANDING OF THE GOVERNING LAW.....	15
	A. Claim Construction.....	15
	B. Obviousness.....	17
VI.	LEVEL OF SKILL IN THE ART	22
VII.	THE '604 PATENT'S EFFECTIVE FILING DATE.....	23
VIII.	TECHNOLOGY OVERVIEW	23
IX.	THE '604 PATENT	35
	A. Summary of Patent	35
	B. Prosecution History of the '604 Patent	42
X.	CLAIM CONSTRUCTION	43
XI.	OVERVIEW OF THE PRIOR ART	44
	A. Thimmegowda.....	44
	B. Lee	46
	C. Kobayashi	51
XII.	GROUND 1: THIMMEGOWDA IN VIEW OF LEE AND A POSITA'S KNOWLEDGE	55
	A. Motivation to Combine	55
	B. Claim 1:	64
	1. [1.PRE] "A three-dimensional (3D) memory device, comprising:"	64
	2. [1.A] "a memory array structure; and"	64

3. [1.B] “a staircase structure in an intermediate of the memory array structure and dividing the memory array structure into a first memory array structure and a second memory array structure along a lateral direction, the staircase structure comprising” 65
4. [1.C] “the staircase structure comprising (i) a plurality of stairs extending along the lateral direction, and” 67
5. [1.D] “the staircase structure comprising ... (ii) a bridge structure in contact with the first memory array structure and the second memory array structure,” 68
6. [1.E] “the plurality of stairs comprising a stair above one or more dielectric pairs,” 72
7. [1.F] “wherein: the stair comprises a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure, and” 75
8. [1.G] “wherein: the stair comprises ... a dielectric portion at a same level and in contact with the conductor portion, the stair being electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure; and” 79
9. [1.H] “along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.” 84
- C. Claim 2 “The 3D memory device of claim 1, wherein the stair further comprises: a dielectric layer under the conductor portion and the dielectric portion.” 87
- D. Claim 3 “The 3D memory device of claim 2, wherein the conductor portion and the dielectric layer are each above the one or more dielectric pairs.” 88
- E. Claim 4 “The 3D memory device of claim 2, wherein along the lateral direction, a width of the conductor portion is equal to a dimension of the stair.” 90
- F. Claim 5 “The 3D memory device of claim 1, wherein along the second lateral direction perpendicular to the lateral direction, a length of the conductor portion is equal to or less than a second dimension of the stair.” 90

G.	Claim 8	92
1.	[8.A] “The 3D memory device of claim 1, wherein: the conductor portion comprises at least one of tungsten, cobalt, copper, aluminum, silicides, or polysilicon;”	92
2.	[8.B] “the dielectric portion comprises silicon nitride; and”	92
3.	[8.C] “a dielectric layer is arranged under the conductor portion and the dielectric portion, the dielectric layer comprising silicon oxide.”	94
H.	Claim 9	95
1.	[9.PRE] “A three-dimensional (3D) memory device, comprising:”	95
2.	[9.A] “a memory array structure; and”	95
3.	[9.B] “a staircase structure comprising a plurality of stairs extending along a lateral direction,”	95
1.	[9.C] “a stair comprising a conductor portion on a top surface of the stair and a dielectric portion at a same level and in contact with the conductor portion, the conductor portion being electrically connected to the memory array structure,”	95
2.	[9.D] “wherein along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.”	96
I.	Claim 10: “The 3D memory device of claim 9, wherein the staircase structure further comprises a dielectric layer under the conductor portion and the dielectric portion.”	97
J.	Claim 11: “The 3D memory device of claim 10, wherein: the conductor portion and the dielectric layer are each above one or more dielectric pairs.”	97
K.	Claim 12: “The 3D memory device of claim 9, wherein along the lateral direction, a width of the conductor portion is equal to a dimension of the stair.”	97

L.	Claim 13: “The 3D memory device of claim 9, wherein along the second lateral direction perpendicular to the lateral direction, a length of the conductor portion is equal to or less than a second dimension of the stair.”	97
XIII.	GROUND 2: THIMMEGOWDA IN VIEW OF KOBAYASHI AND THE KNOWLEDGE OF A POSITA	98
A.	Motivation to Combine	98
B.	Claim 1:	101
1.	Claim 1 Preamble and Elements 1[a]-[d].	101
2.	[1.E] “the plurality of stairs comprising a stair above one or more dielectric pairs,”	101
3.	[1.F] “wherein: the stair comprises a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure, and”	105
4.	[1.G] “wherein: the stair comprises ... a dielectric portion at a same level and in contact with the conductor portion, the stair being electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure; and”	109
5.	[1.H] “along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.”	111
C.	Claim 2 “The 3D memory device of claim 1, wherein the stair further comprises: a dielectric layer under the conductor portion and the dielectric portion.”	114
D.	Claim 3 “The 3D memory device of claim 2, wherein the conductor portion and the dielectric layer are each above the one or more dielectric pairs.”	115
E.	Claim 4 “The 3D memory device of claim 2, wherein along the lateral direction, a width of the conductor portion is equal to a dimension of the stair.”	116
F.	Claim 5 “The 3D memory device of claim 1, wherein along the second lateral direction perpendicular to the lateral direction, a length of the conductor portion is equal to or less than a second dimension of the stair.”	117

G.	Claim 8	118
1.	[8.A] “The 3D memory device of claim 1, wherein: the conductor portion comprises at least one of tungsten, cobalt, copper, aluminum, silicides, or polysilicon;” ..	118
2.	[8.B] “the dielectric portion comprises silicon nitride; and”	119
3.	[8.C] “a dielectric layer is arranged under the conductor portion and the dielectric portion, the dielectric layer comprising silicon oxide.”	119
H.	Claim 9	120
1.	[9.PRE] “A three-dimensional (3D) memory device, comprising:”	120
2.	[9.A] “a memory array structure; and”	120
3.	[9.B] “a staircase structure comprising a plurality of stairs extending along a lateral direction,”	120
1.	[9.C] “a stair comprising a conductor portion on a top surface of the stair and a dielectric portion at a same level and in contact with the conductor portion, the conductor portion being electrically connected to the memory array structure,”	120
2.	[9.D] “wherein along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.”	121
I.	Claim 10: “The 3D memory device of claim 9, wherein the staircase structure further comprises a dielectric layer under the conductor portion and the dielectric portion.”	121
J.	Claim 11: “The 3D memory device of claim 10, wherein: the conductor portion and the dielectric layer are each above one or more dielectric pairs.”	121
K.	Claim 12: “The 3D memory device of claim 9, wherein along the lateral direction, a width of the conductor portion is equal to a dimension of the stair.”	122

L.	Claim 13: “The 3D memory device of claim 9, wherein along the second lateral direction perpendicular to the lateral direction, a length of the conductor portion is equal to or less than a second dimension of the stair.”	122
XIV.	SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS.....	122
XV.	DECLARATION	123

I, Dr. Sanjay Banerjee, hereby declare as follows:

I. INTRODUCTION

1. My name is Sanjay Banerjee. I have been retained on behalf of Petitioner Micron Technology, Inc. (“Micron”) to provide this Declaration concerning technical subject matter relevant to the *inter partes* review petition (“Petition”) concerning claims 1-5 and 8-13 (“the Challenged Claims”) of U.S. Patent No. 11,450,604 (Ex. 1001, the “’604 patent”).

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration. I reserve the right to supplement this Declaration in response to additional evidence that may come to light.

3. If requested, I am prepared to explain (in a deposition or at a trial before the Patent Trial and Appeal Board (the “Board”)) the technology disclosed in the Challenged Patents—including the state of the art in the relevant timeframe. Similarly, I am prepared to explain the technology disclosed in the prior art references cited herein. This may include, among other things, background information on 3D NAND technology.

4. I am over 18 years of age and competent to testify to the matters addressed in this Declaration.

II. QUALIFICATIONS

5. I currently serve as the Cockrell Family Regents Chair Professor of Electrical and Computer Engineering and Director of the Microelectronics Research Center at the University of Texas at Austin (“UT”). Prior to this position, I was first an Assistant Professor (September 1987-August 1990) and later an Associate Professor (September 1990-August 1993) at UT, before being named a Professor in September 1993. Prior to starting my academic work at UT, I was a member of the technical staff at Texas Instruments (Corporate R&D) from the time I completed my doctoral studies in 1983 until August 1987. I worked on vertical 3D Dynamic Random Access Memory (DRAM) cells (*see* S. Banerjee and M. Bordelon, “A Model for the Trench Transistor,” *IEEE Trans. Elec. Dev.*, 34 (12), 2485-2493, December 1987).

6. In addition to my academic work at UT, I was also the Director of the South West Academy of Nanoelectronics, one of three centers created by the Semiconductor Research Corporation Nanoelectronics Research Initiative in 2006 to research and develop a replacement for conventional metal oxide semiconductor field effect transistors (“MOSFETs”) during the entire program.

7. I received my Ph.D. in Electrical Engineering from the University of Illinois in 1983. I also received an M.S. in Electrical Engineering from the

University of Illinois in 1981. I received a B. Tech. in Electronics from the Indian Institute of Technology at Kharagpur in 1979.

8. As described in my *curriculum vitae* (Ex. 1004), I have more than 40 years of experience in the field of electrical engineering, including extensive experience in semiconductor development and fabrication including that of flash memory, 3-Dimensional Dynamic Random Access Memory (“DRAM”) cells, MOSFETs, and complementary metal-oxide-semiconductor (“CMOS”) transistors. My work in these fields has resulted in thirty-five United States patents related to methods of forming polysilicon and novel transistors, flash memory, and vertical DRAM cells. I have been elected a Fellow of the National Academy of Inventors.

9. Much of my research and experience has related to methods for MOSFET and polysilicon FET fabrication and design, including deposition of thin films of poly/amorphous Si, high-k gate dielectrics and metals by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), patterning using photolithography and etching using plasma-based Reactive Ion Etching (RIE) which are some of the processing techniques used to make 3D NAND flash. I have worked extensively on polysilicon thin film transistors similar to the ones used in the channel of NAND flash memory cells, high-k and other dielectrics used for charge storage, and for tunneling. A number of the sponsored research grants on which I have been a principal or coinvestigator have related to

chemical deposition methods and/or ultra-shallow source/drain junction technology, including “Transport in MOSFETs” (Motorola, August 1993-August 1994), “Ultra Shallow Junction Technology” (SEMATECH January 1994-December 1996), and “Vertical Si-Ge-C MOSFETS” (Semiconductor Research Corporation September 2000-August 2003). In addition, I am an author on over forty publications relating to flash memory cells, including vertical 3D memory that can be used in NAND flash (e.g., Sarkar J, Dey S, Shahrjerdi D, Banerjee SK, Vertical Flash memory cell with nanocrystal floating gate for ultradense integration and good retention, IEEE Electron Device Letters 28 (5): 449-451 MAY 2007). One of my papers on flash memory was given a Best Paper Award by the SRC.

10. I am a Fellow of the Institute of Electrical and Electronics Engineers (“IEEE”), the American Physical Society (“APS”), and the American Association for the Advancement of Science (“AAAS”). I have served on numerous professional and government committees in the electrical engineering field, including chairing multiple IEEE committees, meetings, and programs, serving on Morgan & Claypool’s editorial board, and serving as a member on the International Technology Roadmap for Semiconductors (“ITRS”).

11. I have taught courses in Semiconductor Physics, Solid State Electronic Devices, and Microelectronic and VLSI Device Fabrication at UT. In addition, I have delivered many courses to industry on Semiconductor Devices and Memory

and Semiconductor Processing. I have taught courses that cover 3D memories, such as 3D NAND (Ultra Large Scale Integration Techniques and Solid State Electronic Devices). As a principal investigator, I have been the advisor to over 80 Doctoral and Masters students.

12. I am the co-author of several books and invited book chapters covering the area of electronic and semiconductor devices, including: Dopant Diffusion, Solid State Electronic Devices (three editions), Silicon-germanium Devices, and Novel 3D CMOS. I have authored or co-authored more than 1,000 papers and presentations in the areas of semiconductor devices and electronics development over the course of my career.

13. I have been the recipient of fifty grants to fund my research from a variety of funding agencies including the National Science Foundation (“NSF”), DARPA, the Department of Energy, Semiconductor Research Corporation, the Department of Defense-Multidisciplinary University Research Initiative, and the Office of Naval Research.

14. I have received numerous awards for my work, including the NSF Presidential Young Investigator Award. The NSF Presidential Young Investigator

Award was¹ a highly competitive honor and grant bestowed annually upon recognized young academic leaders in science and engineering. I have received numerous other awards, including some the highest honors for semiconductor devices such as the Andrew Grove Award from IEEE, and the Semiconductor Industry Association/Semiconductor Research Corporation University Researcher Award, for my work in semiconductor memory and transistors, which are described in more detail in my CV (Ex. 1004).

III. COMPENSATION

15. I am being compensated for my work in this matter at an hourly rate of \$650.00 for consulting services. My compensation is not based on the outcome of this matter or on the substance of my opinions.

IV. MATERIALS CONSIDERED

16. In preparing this declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my declaration:

¹ The NSF Presidential Young Investigator Award was an award given out by the NSF until 1991, at which time it was replaced with the NSF Young Investigator Awards and Presidential Faculty Fellows Program.

Petition for *Inter Partes* Review of U.S. Patent No. 11,450,604
Declaration of Dr. Sanjay Banerjee

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 11,450,604 to Wang et al. (the “’604 patent”)
1002	File History of U.S. Patent No. 11,450,604 to Wang et al.
1005	U.S. Patent No. 10,515,973 to Thimmegowda et al. (“Thimmegowda”)
1006	U.S. Patent Publ. No. 2019/006275 to Kobayashi et al. (“Kobayashi”)
1007	U.S. Patent Publ. No. 2016/0027730 to Lee (“Lee”)
1010	U.S. Patent Publ. No. 2021/0193676 to Zhang et al. (“Zhang”)
1011	U.S. Patent No. 9,029,938 to Nakaki (“Nakaki”)
1012	Aritome, “NAND Flash Memory Technologies” (2016)
1013	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers (2017)
1014	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1017	U.S. Patent Publ. No. 2017/0256551 to Lee
1018	Micheloni, “3D Flash Memories” (2016)
1019	U.S. Patent Publ. No. 2019/0139977 to Lee
1021	U.S. Patent No. 11,239,248 to Xu et al.
1022	U.S. Patent No. 11,217,601 to Luo et al.
1023	U.S. Patent No. 12,087,572 to van Schravendijk et al.
1024	U.S. Patent Publ. No. 2021/0193536 to Kris et al.
1025	U.S. Patent No. 10,475,737 to Tang et al.

EXHIBIT NO.	DESCRIPTION
1026	U.S. Patent No. 10,381,369 to Kim et al.
1027	Certified English Translation of Chinese Patent Application Publ. No. CN108766971 to Liu
1028	Chinese Patent Application Publ. No. CN108766971 to Liu
1029	U.S. Patent Publ. No. 2012/0070944 to Kim et al.
1030	U.S. Patent No. 10,026,692 to Chen

V. UNDERSTANDING OF THE GOVERNING LAW

17. I am not an attorney but have been instructed in and applied the law as described in this section.

A. Claim Construction

18. I understand that the first step in determining whether a patent claim would have been anticipated or obvious is to ascertain how a person of ordinary skill in the art (“POSITA”) would have understood the claim terms.

19. I have been instructed by counsel on the law regarding claim construction and patent claims, and I understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim, or it can further depend from another dependent claim.

I understand that a dependent claim includes all the limitations that it recites, in addition to all the limitations recited in the claim(s) from which it depends.

20. It is my understanding that in proceedings before the USPTO, the claims of a patent are to be construed under what is referred to as the “*Phillips* standard.” I understand that this means that claim terms of a patent are given the ordinary and customary meaning they would have to a POSITA in view of the description provided in the patent itself and the patent’s file history.

21. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood the disputed claim language to mean. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent specification, and the patent’s prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

22. I understand that words or terms should be given their ordinary and accepted meaning unless it clearly appears that the inventors were using them to mean something else. In making this determination, the claims, the remainder of the patent, and the prosecution history are of paramount importance. Additionally, the

patent and its prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (*i.e.*, provided its own special meaning to any disputed terms) or intentionally disclaimed, disavowed, or surrendered any claim scope.

23. I further understand that in proceedings before the PTAB, claim terms need only be construed to the extent necessary to resolve any controversy that may arise.

24. In comparing the claims of the Challenged Patent to the prior art, I have considered the '604 patent and its file history in light of the understanding of a POSITA at the time of the alleged invention.

B. Obviousness

25. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious under 35 U.S.C. §103(a) to a person of ordinary skill in the art of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed. I also understand that the Board considers certain objective factors if they are present, generally

referred to as “secondary considerations” or “objective indicia” of nonobviousness, as further discussed below in this section.

26. I have been informed that there are two ways to determine whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee’s endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee’s endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee’s attention in considering his or her problem.

27. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there generally must have been some reason or motivation for one of

ordinary skill in the art to combine the teachings of the prior art references to arrive at the claimed subject matter.

28. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a person of ordinary skill in the art at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

29. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine, but that other times the motivation linking two or more prior art references is common sense to a POSITA at the time of the invention.

30. I understand that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. I have further been informed and understand that a POSITA combines the teachings of the prior art references and does not necessarily combine the embodiments of those teachings physically.

31. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

32. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all of the elements of a claim are used in substantially the same manner in devices in the same field of endeavor, the claim is likely obvious.

33. Additionally, I understand that a patent is likely to be invalid for obviousness if a person of ordinary skill can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

34. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

35. I also understand that one of ordinary skill in the art must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

36. I have been informed and I understand that factors referred to as “objective indicia of non-obviousness” or “secondary considerations” are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

37. I also understand that evidence of objective indicia of nonobviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a “nexus,” between any such secondary indicia and the claimed invention. I also have been informed that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (*e.g.*, motivation to combine with predictable results) that is sufficiently strong.

38. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

39. I provide my opinions in this declaration based on the guidelines set forth above.

VI. LEVEL OF SKILL IN THE ART

40. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

41. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a POSITA is also a person of ordinary creativity.

42. A POSITA in the field of the '604 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill,

knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, its component parts, how it operates, and how it is controlled.

43. In view of my educational background and work experience, I am a person of more than the ordinary level of skill in the art of the '604 patent and was so by June 5, 2020. In forming my opinions, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of a POSITA.

VII. THE '604 PATENT'S EFFECTIVE FILING DATE

44. I understand that the '604 patent claims priority to an earlier-filed PCT publication No. PCT/CN2020/094658, filed June 5, 2020.

45. For purposes of this declaration, I have been instructed to use June 5, 2020, as the priority date of the '604 patent. My opinions in this declaration were formed from the perspective of a POSITA as of June 5, 2020, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

VIII. TECHNOLOGY OVERVIEW

46. The '604 patent and the prior art discussed in this Petition relate to three-dimensional (3D) memory devices, *e.g.*, 3D NAND memory devices. The

basic building block of the non-volatile semiconductor memory is the memory cell, a structure that stores one or more bits of data. These memory cells are based on the Metal Oxide Semiconductor Field Effect Transistor, or MOSFET. This overview is for N-channel MOSFET-based 3D NAND flash devices. When the proper voltage conditions are applied, (1) electrons are attracted to the surface of the semiconductor device in the channel region forming a conductive path between source and drain and (2) electrons flow through the channel from the source to the drain when a drain voltage is applied. The flow of electrons through the channel is electrically controlled by the gate. The voltage on the gate needed to cause significant conduction in the channel is known as the threshold voltage.

47. A traditional type of non-volatile semiconductor memory can store information using a MOSFET that includes an extra “floating” gate. Floating gates were historically made out of conductive electrodes that were not electrically connected to the external terminals such as source, drain and control gate of the memory cell. But charges can also be stored in charge traps in the gate dielectric, where these act as the “floating gates.” The shapes of the energy band diagrams in the two cases are somewhat different, but the overall charge storage mechanisms have similarities. I will discuss charge-trap memories in more detail shortly. The floating gate stores the charge that is used to represent the data. A floating gate is surrounded by electrical insulators on all sides - it electrically “floats” in the

insulation - and therefore has no direct electrical contact to the rest of the device. Instead, the floating gate is capacitively coupled to the various electrodes. Electrically Erasable Programmable Read Only Memory (EEPROM) can both store and *erase* data electrically. In EEPROM devices, the insulator, or dielectric, between the floating gate and the channel is known as the tunnel dielectric, while the dielectric between the floating gate and the control gate is known as the control dielectric. Flash memory is a type of EEPROM where a large number of memory cells can be erased very quickly - that is, in a “flash.” Flash memory cells are not erased individually like other EEPROMs, but rather in a group called a “block.”

48. The two most common memory cell architectures used for flash EEPROMs are NOR and NAND. The conditions that must be applied to a memory cell in a NOR or NAND architecture in order to program, erase or read the cell are discussed below. Conditions for programming, reading, and erasing memory cells in the various cell architectures were known to those of ordinary skill in the field at the time the '604 patent was filed. The logic value associated with the “erased” and “programmed” states of a memory cell is a matter of convention. In some sources, the logic value “1” denotes the erased state and “0” denotes the programmed state - in others, the reverse is true. Either of these conventions is appropriate. For this background discussion of NAND architecture, I will use the convention where “1” represents the logic value of the erased state and “0” represents the logic value of

the programmed state. In the NOR architecture, a single memory cell exists at each intersection of a bit line (drain) and a word line (control gate). In the NAND memory cell architecture, groups of cells are connected together in series between source and drain (*i.e.*, the bit line). This group of cells, is known as a NAND string. The control gates of these cells are the word lines.

49. One generally programs the cells using tunneling of electrons from the substrate into the floating gate by applying a high positive voltage to the control gate. One gets Fowler-Nordheim tunneling through triangular barriers for thicker tunnel dielectrics, or direct tunneling through trapezoidal barriers for thinner tunneling layers. This high voltage applied to the control gate increases the electric field across the tunnel dielectric and narrows the triangular potential barrier for Fowler Nordheim tunneling, thereby making it easier for electrons to quantum mechanically tunnel through the dielectric. There is also an increase of tunneling current for direct tunneling. These tunneled electrons are stored (trapped) on the floating gate. This results in the high threshold voltage state, generally known as the “0” state. One also erases the NAND cell by tunneling, by either applying a high positive voltage to the substrate electrode, or applying a negative voltage to the control gate. This increases the electric field across the tunnel dielectric, reduces the barrier width and thus increases the probability of tunneling (*i.e.*, removing charge from the floating gate). This results in the low threshold voltage state, generally known as the “1”

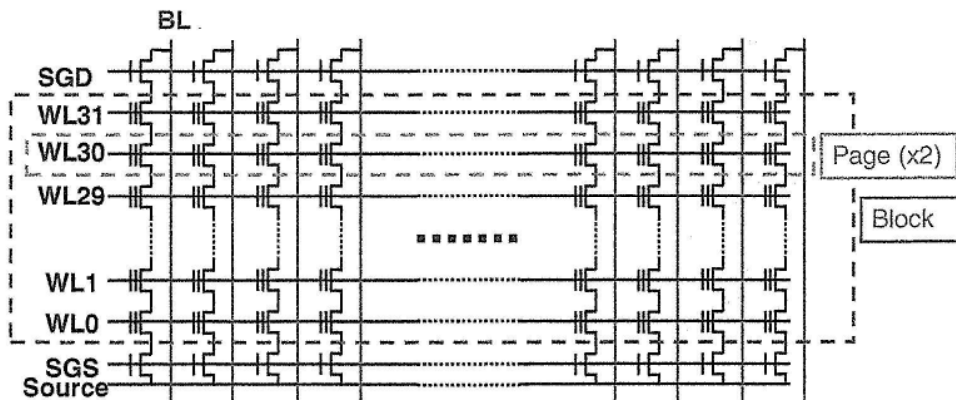
state. For metallic or semiconducting floating gates, the electrons are trapped at the same energy at the Fermi level, or bottom of the conduction band, respectively, and the carriers pile up next to the tunnel dielectric interface. This also makes it necessary to pattern the conducting floating gate to isolate them between adjacent cells. On the other hand, if the charges are trapped in a charge trap layer, there is no need to pattern and etch the layer because the traps states are already isolated from each other. In this case, the electrons can be trapped at multiple trap energy levels and slightly different distances from the tunnel dielectric and channel depending on the spatial distribution of the traps, making the threshold voltage distribution wider than for conducting floating gates. The trap potentials are also different. Instead of a trapezoidal well, traps have a Coulombic well that is subject to Poole-Frenkel barrier lowering upon application of a field.

50. NAND cells are read by applying a high voltage (V_{PASS}) to all the word lines in the NAND string except the cell that is being read. This ensures that all other cells in the string will conduct current. The conduction of the cell being read will depend on whether it is in the “0” or “1” state. This conduction can be determined through the use of a sense amplifier, which may sense either voltage or current on the bit line.

51. NAND memories are more compact than NOR memories because NAND cells are connected in a string. Adjacent NOR cells need to be isolated from

each other, which is accomplished using isolation regions which consume “silicon real estate.” For NAND architectures, individual cells in a string do not need such isolation -- one only needs to isolate one string from the adjacent strings. This consumes less surface space for isolation and makes the NAND architectures more attractive for mass storage applications. Ex. 1012, 38.

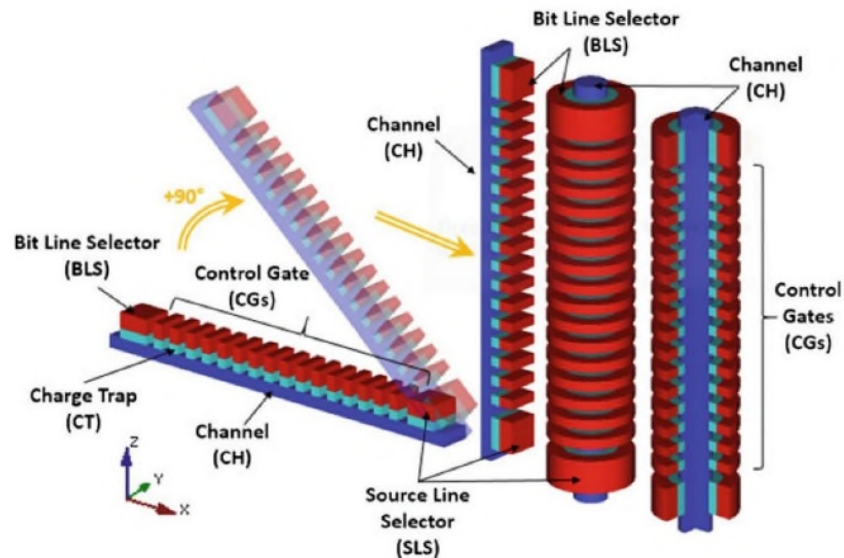
52. In the early days, NAND devices were formed as two-dimensional arrays of cells on a substrate surface (*viz.*, only in the horizontal X- and Y-directions). Ex. 1012, 58. The example below from a NAND flash memory textbook is a schematic showing a 2D NAND memory architecture where cells grouped into “page[s]” and “block[s],” which are only fabricated in the X- and Y-directions.



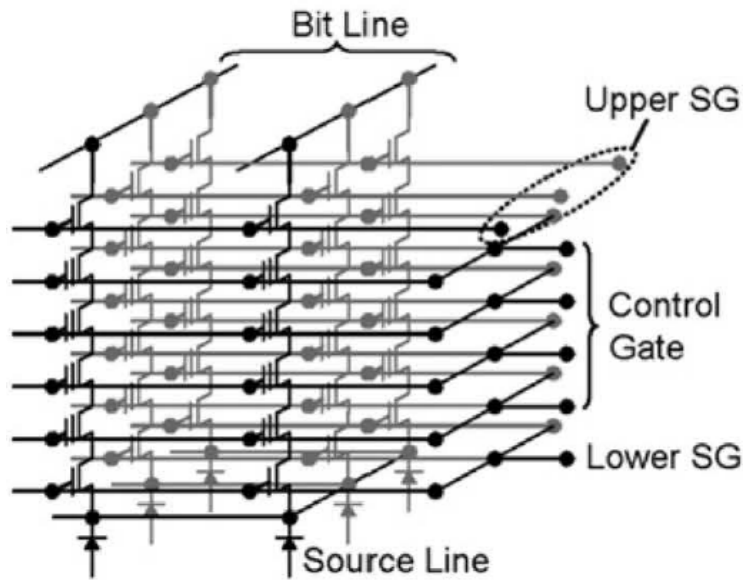
Id., 40.

53. “[T]o further scale down the memory cell size” and achieve higher memory densities, “three-dimensional (3D) NAND flash cells” were developed. Ex.

1012, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1013, 3. The evolution of NAND architectures from 2D to 3D led to further savings of silicon real estate. The image below illustrates the concept of rotating a NAND memory string on its side (*i.e.*, placing it in the vertical dimension on the z-axis).



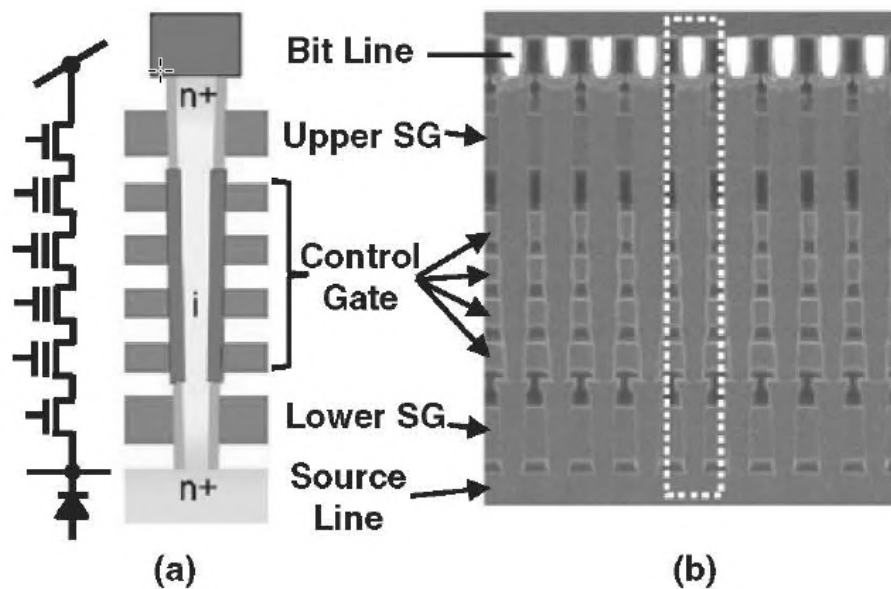
Ex. 1014, 122. The vertical memory cell strings can then be repeated numerous times to form a three-dimensional memory array:



Ex. 1012, 296. This is structurally different than simply stacking various 2D NAND memory arrays on top of one another, because the memory channels/strings in a 3D NAND run in the vertical (not horizontal) direction which has important implications for semiconductor fabrication of the 3D NAND structures.

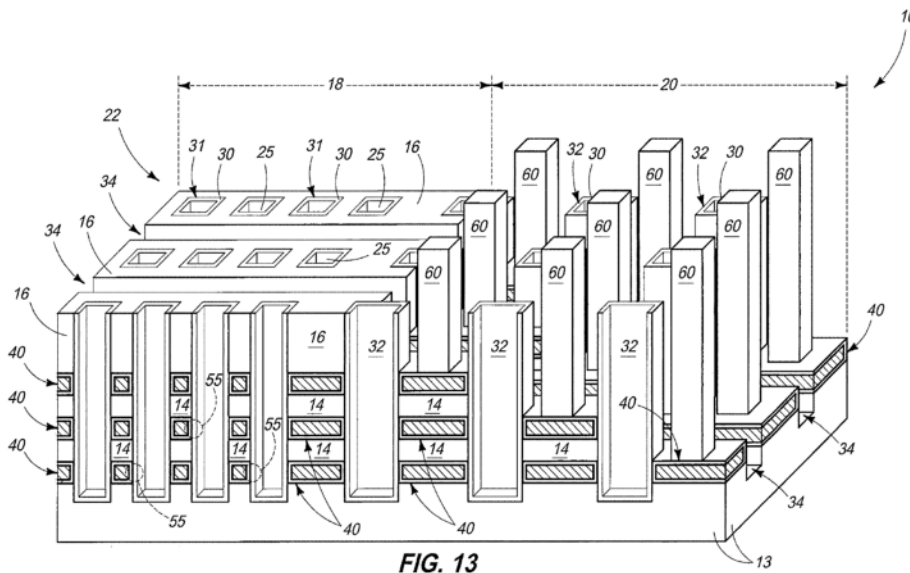
54. 3D NAND memory devices typically include alternating horizontal layers of conductors and dielectric in a “[s]tack.” Ex. 1012, 294. A vertically aligned “through-hole[.]” channel (also known as a channel structure) “filled by memory film ... and channel poly-Si” passes through the layers to form the vertical memory cell strings. *Id.*, 295. Control gates for the memory cells are formed where the wordlines (formed by the horizontal conduction layers) intersect the vertical memory strings and act as a control gate. *Id.*, 295-296. A particular vertical memory cell “string is selected by a bit line and an upper select gate (upper SG).” *Id.* The

lowest layer is a “select gate (lower SG)” that allows the strings to connect to a lower “common source.” *Id.*, 295, 297. An example 3D NAND vertical memory cell string is shown below.



Id., 296.

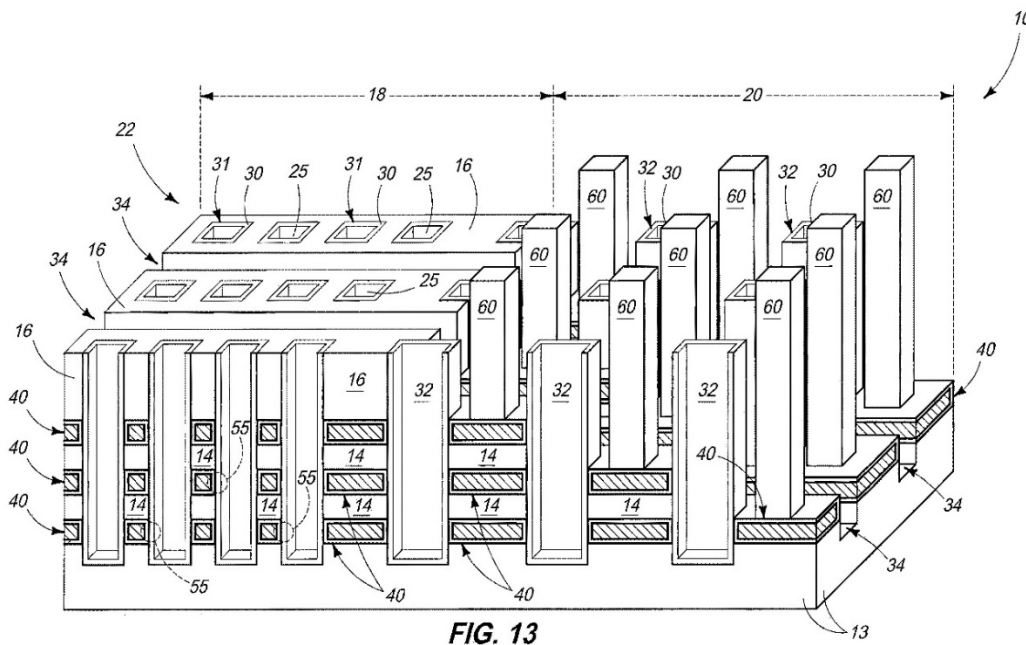
55. It was well known to POSITAs to use so-called “staircase structures” to provide electrical access points for the various wordlines. For example, as illustrated below, each subsequent wordline (40) progressively extends further in the horizontal X-direction to provide landing pads for the contacts 60.



Ex. 1025 (U.S. Pat. No. 10,475,737), Fig. 13, 4:56-64, 8:45-56.

56. To manufacture such 3D NAND devices, it was known in the art to utilize sacrificial layers. Rather than simply depositing alternating layers of dielectric and conductor, the “sacrificial” approach entailed first creating an alternating stack of dielectric layers and interim “sacrificial layers,” which are subsequently removed and replaced with conductive control gate layers. Ex. 1025 (U.S. Pat. No. 10,475,737), 4:25-55. Due to the increased number of layers in 3D NAND relative to 2D NAND, there was a greater need for vertical stability, and it was known to use supporting pillars that extend through the stack to provide mechanical support during the process of replacing the sacrificial gate layers with conductive gate layers. *Id.*, 7:44-8:3.

57. The stacked structure in 3D NAND devices typically include a core region, which includes the memory cells, and a peripheral region, which includes a connection region known as the staircase region. Ex. 1026 (U.S. Pat. No. 10,381,369), 5:43-6:11, 12:20-27. Staircase structures were well known and structurally provide landing areas for contacts to the control gates or wordlines (below, the contacts 60 connect to different control gates or wordlines):



Ex. 1025 (U.S. Pat. No. 10,475,737), Fig. 13, 4:56-64, 8:45-56.

58. One method of forming 3D NAND memory devices is to form the alternating stack of sacrificial gate layers and dielectric layers, and then replace the sacrificial gate layers with metal layers. Ex. 1027 (CN Patent Appl. Publ. No. CN108766971), [0062]. This is known as a gate replacement or gate last process.

The advantage of this process compared to the older scheme where alternating layers of polysilicon (which functions as the wordlines) separated by layers of dielectric to isolate adjacent wordlines is that the replacement gate can be made of more conductive metal. This leads to shorter RC time constant wordline delays and faster memory.

59. One problem with the staircase contacts is that it wastes silicon real estate. A possible solution is to share the staircase contacts with two adjacent memory arrays and use a “bridge” to connect the wordline contacts to access both arrays via bidirectional driving.

60. Another challenge is that the different wordline contact vias are of different lengths along the staircase. Hence, while trying to etch the deepest vias at the bottom of the staircase, one ends up overetching the shorter vias near the top of the staircase. While etch barriers and highly selective etches are one solution, that is often not a panacea. An elegant solution is to stagger the wordline contact conductive landing pads in each staircase such that they do not spatially overlap in the depth direction. That way, even if a shallower via is overetched, it will not electrically short out the lower lying conductive landing pads. Instead, it will terminate on non-conducting insulators.

IX. THE '604 PATENT

A. Summary of Patent

61. The '604 patent describes a 3D memory device with a “staircase structure” that “divides the memory array structure into a first memory array structure and a second memory array structure along a lateral direction.” Ex. 1001, 1:42-47. As I describe in Section VIII, staircase structures were well known. Here, the '604 patent is describing two memory arrays with a staircase region in between them.

62. As shown below, the '604 patent discloses a staircase with two primary features: (1) a staircase 106; and (2) a bridge structure 108. *See* Ex. 1001, 7:42-43. The red lines indicate that bridge 108 is formed of alternating layers of materials in contact with corresponding staircase layers. *Id.*, 5:66-6:1 (“The staircase structure can include a bridge structure that has interleaved a plurality of conductor layers and dielectric layers.”); *id.*, 7:42-43 (“staircase 106 and [] bridge structure 108 [are] in contact with each other.”). In other words, the bridge includes an alternating stack, like a memory stack, such that there are alternating dielectric and conductive layers. The '604 patent discloses that the corresponding staircase and bridge layers can be the same material. *Id.*, 8:36-42.

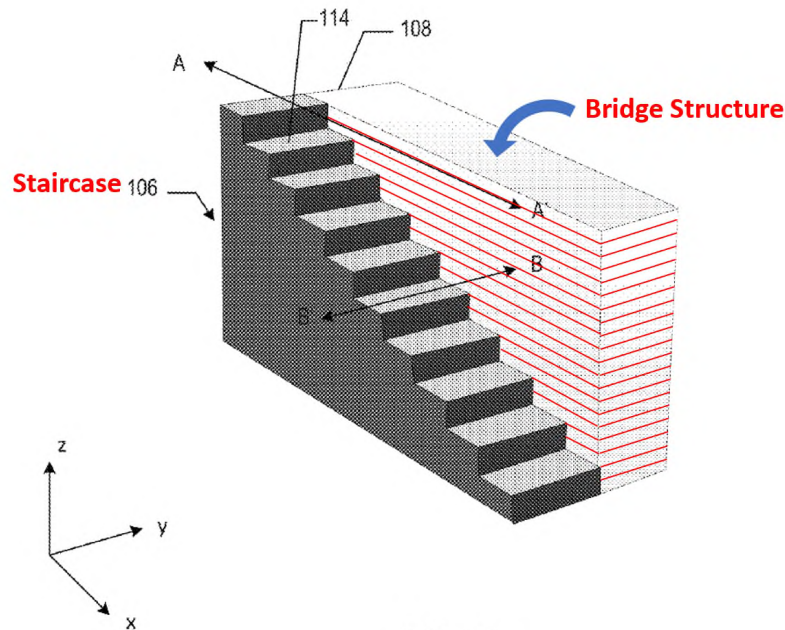


FIG. 1B

Id., Fig. 1B (annotated). The bridge, as its name suggests, connects (or ‘bridges’) memory arrays on either end. This bridge, as I explain below, provides a conductive path for the stairsteps to electrically couple to the arrays on both ends.

63. Each staircase step serves as a landing pad for a wordline VIA contact, as Fig. 3A below shows. See Ex. 1001, 10:39-47. Landing pads were common elements and as the name implies, provide a landing area for a staircase contact.

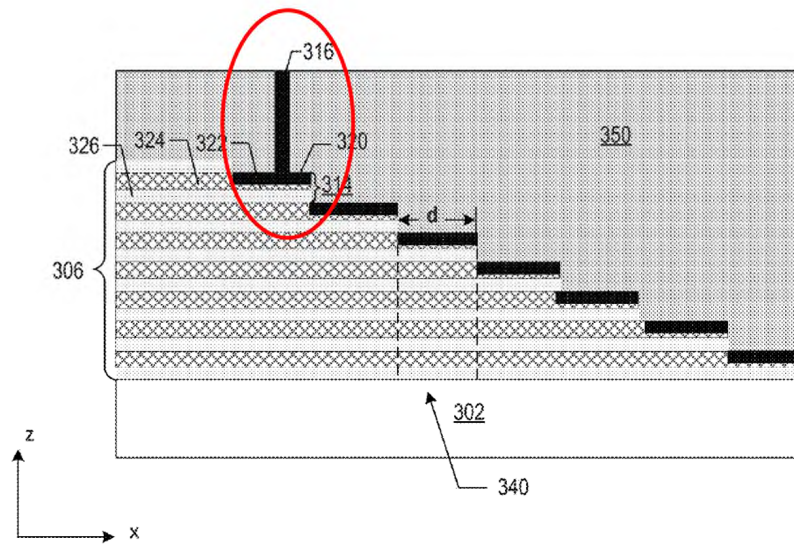


FIG. 3A

Id., Fig. 3A (annotated).

64. The '604 patent purports to solve a “punch-through” in forming staircase contacts on the stairsteps. Ex. 1001, 4:58-5:24. The '604 patent discloses as “the number of vertical levels of the stacked storage structure also increases, and it has become more difficult to form the word line VIA contacts on the stairs without **punching through** the contacts and causing short circuits.” *Id.* (emphasis added).

Punching through refers to etching through the stairstep to underlying layers.

65. The '604 patent further explains:

[W]ord line VIA contacts are often formed by forming openings in contact with the stairs (e.g., the landing area of the stairs) in an insulating structure in which the staircase structure is placed, and filling the openings with a conductive material. Conventionally, these openings, formed to be in contact with stairs at different depths/heights,

are formed in the same etching process. Because of the variation in opening depths, the openings are often not etched evenly or desirably. For example, the openings in contact with lower stairs (e.g., the deeper openings) and the openings in contact with higher stairs (e.g., the shallower openings) undergo the same etching time, resulting the openings in contact with the higher stairs to be over etched. The over-etching can cause the conductor layers (e.g., word lines) on the top surfaces of the higher stairs to be undesirably damaged or even etched through. The word line VIA contacts can undesirably be in contact with other conductor layers underlying the respective conductor layers, causing a punch-through that leads to short circuits.

Id.

66. To address this, the '604 patent discloses placing dielectric material underneath the landing area of each stair. See Ex. 1001, 5:25-62. That way, punching through will result in only penetrating into dielectric material, which would not create an issue with the conductive contact inadvertently punching through to another conductive layer. The '604 patent accomplishes this by employing a “conductor portion” (e.g., a narrow conductive finger) that “covers at least the landing area of the respective stair (e.g., a portion of the stair) such that a word line VIA contact can be in contact with and electrically connected to the respective stair.” *Id.* In particular, “the dimension of the conductor portion, along the direction the stairs extend, [may be] the same as the dimension of the stair” and

“does not laterally extend under [] the conductor portion of any upper stair.” *Id.* In this manner, the “conductor portion” of each stair is in contact with the horizontally adjacent “dielectric portion at the same level” of the stair. *Id.* This results in a staircase where all layers under the landing area of any given step are comprised solely of dielectric. *Id.* Again, the point of this is that there is not underlying conductive elements, because staircase contact must not electrically couple to underlying conductive layer (other gate layers).

67. I will illustrate this point with two versions of Fig. 3A. In the modified version of Fig. 3A (on the left), the conductive wordlines (shown in black) underneath any given step extend horizontally to the left where they intersect the memory strings (not shown). In the unmodified version of Fig. 3A (on the right) which employs the '604 patent's purported solution, the conductive portion of each step does **not** extend horizontally to the left. Thus, on the right, there are not underlying conductive portions of any gate layers.

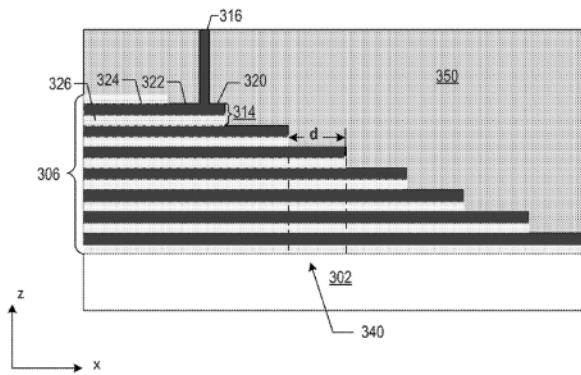


FIG. 3A (modified)

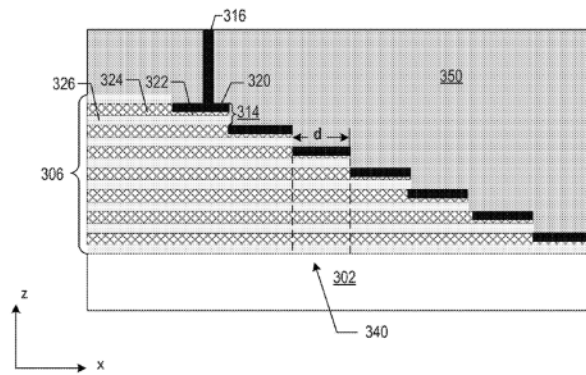


FIG. 3A (unmodified)

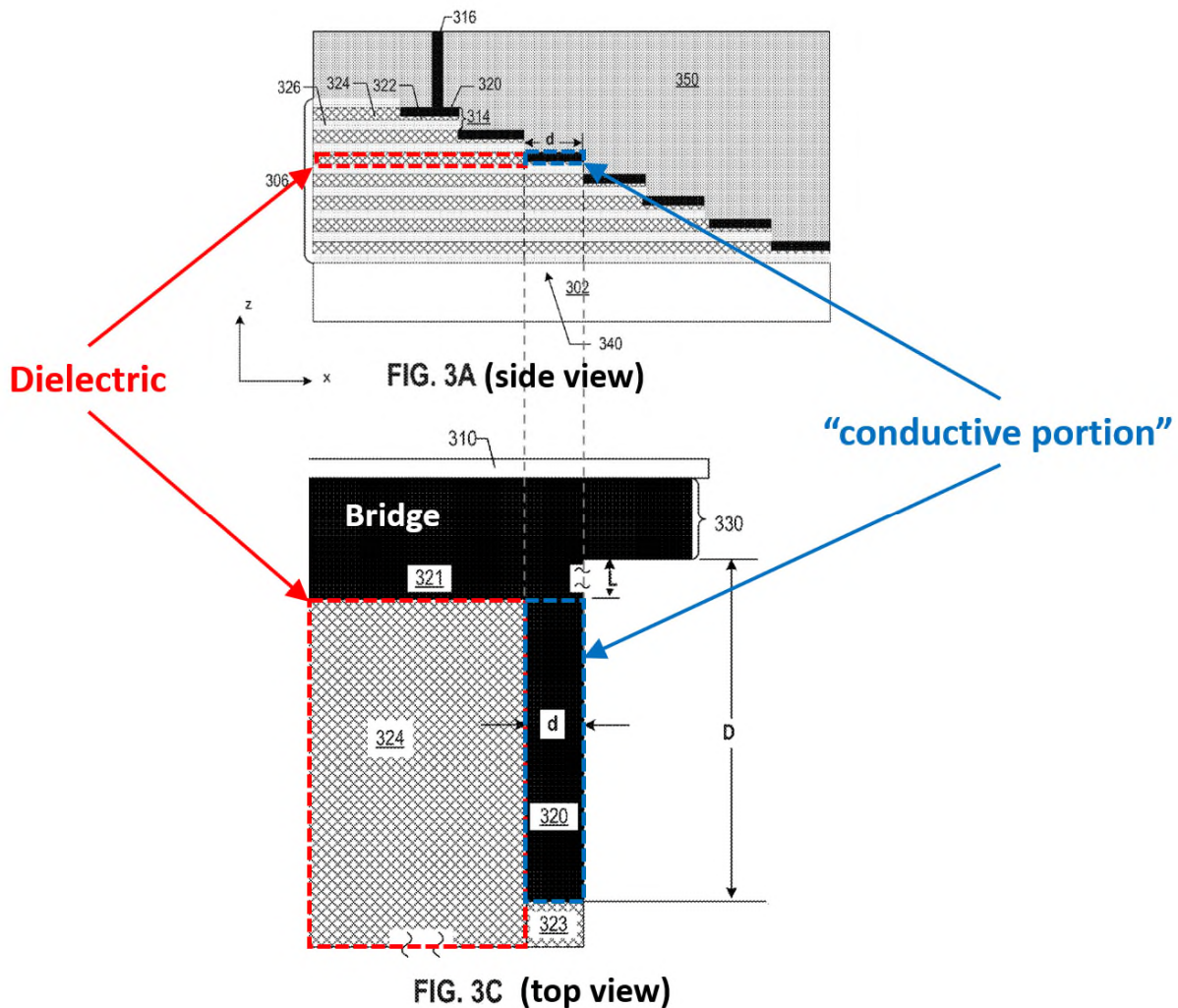
Ex. 1001, Fig. 3A; *see also id.*, 12:8-13.

68. The '604 patent discloses that “[e]ven if a punch-through occurs on any conductor portion, the word line VIA contact has no contact on the ... word line[] of any lower stairs, and leakage or short circuits can be reduced/eliminated.” Ex. 1001, 5:58-62.

69. Each “conductor portion” must electrically connect to the respective wordline in the memory to provide the appropriate voltages to read/write the memory cells. In other words, that conductive portion must electrically couple to the respective wordline layer of the memory stack. The '604 patent discloses a “bridge” to accomplish this. The bridge “has interleaved a plurality of conductor layers and dielectric layers” (Ex. 1001, 5:66-6:1) that contact the corresponding staircase layer (*id.*, 7:42-43).

70. The annotated versions of Figs. 3A and 3C below illustrate how a “conductive portion” of a given step in the staircase physically and electrically

connects to its corresponding layer in the bridge. In effect, there is a conductive layer path from the staircase contact landing pad to a respective wordline layer of the memory stack through the finger and the bridge.



Ex. 1001, Figs. 3A and 3C (annotated). The bridge provides the path from the finger to the corresponding wordline in the memory array (not shown above). *Id.*, 6:1-2. Thus, the wordline vias 316 (a staircase contact) electrically control the

corresponding wordlines in the memory array, because of the path through the finger and the bridge. *Id.*, 6:2-7.

71. When the staircase structure is located in between two memory arrays (*e.g.*, between the memory array structures 104-1 and 104-2 as shown in Fig. 1A), “[e]ach word line thus can be bilaterally driven (in both positive and negative x-directions) from a respective word line VIA contact 116 in the intermediate of 3D memory device 100 through bridge structures 108.” Ex. 1001, 9:9-13. In alternative designs, with reference to Fig. 3A above, the contacts would not connect to the array on the right, because there would not be a conductive path to the right (rather, insulator fill 350 is between the contact and an array on the right).

B. Prosecution History of the ’604 Patent

72. I note that all ’604 patent claims were found allowable in the first (and only) office action. Ex. 1002, 657-664.

73. The Examiner states that “the closest prior art of record [was] Zhang,” U.S. Pat. Pub. No. 2021/0193676 (Ex. 1010). Ex. 1002, 657-664. The Examiner stated Zhang “failed to teach that the stair comprises a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure, and a dielectric portion at a same level and in contact with the conductor portion and along a second lateral direction perpendicular to the lateral direction, a

width of the conductor portion is unchanged.” *Id.*, 658-659 (emphasis in original).

The Examiner made similar remarks for independent claims 9 and 15. *Id.*, 659-660.

74. It appears from these comments that the Examiner found that Zhang lacked the “finger” approach of the ’604 patent. *See* Section IX.A.

75. Throughout prosecution, I understand that Patent Owner submitted five Information Disclosure Statements (IDS), meaning statements that identify prior art references, containing dozens of references. *See* Ex. 1002, 77, 180, 304, 410, and 740. I understand that one IDS reference that was identified was TW201605015, which is the Taiwanese version of Lee. *Id.*, 180. I further understand that Patent Owner did not submit an English-language version (*id.*, 234-301). *See* Ex. 1007, cover page (listing publication date of January 28, 2016). In my opinion, having a translation of the text is important, which is evident from reading the ’604 patent, because fully understanding the figures requires the textual description.

X. CLAIM CONSTRUCTION

76. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. In my opinion, the challenged claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

XI. OVERVIEW OF THE PRIOR ART

A. Thimmegowda

77. I understand that Thimmegowda (Ex. 1005) is prior art to the '604 patent.

78. Thimmegowda is titled “Wordline Bridge in a 3D Memory Array.” Ex. 1005, cover page. Its focus is on disclosing a bridge. Thimmegowda discloses the basic building blocks of a 3D memory device: an alternating conductor/dielectric layer stack (known as a memory stack), memory strings extending through the alternating stack (that is, channel structures), staircase structures (which provide landing spots for contacts to control the wordlines), and wordline contacts (also known as staircase contacts) for accessing the memory strings. *See, e.g., Id.*, 1:10-25. These were all known 3D memory elements at the time.

79. Thimmegowda notes that forming a separate staircase to access the wordlines in each memory array “consumes silicon real estate.” Ex. 1005, 1:20-25. Thimmegowda is referring to the fact that in some designs, one side of the staircase does not electrically couple the memory stack, and thus in these designs, it was common to include a staircase on each side of the memory array.

80. To solve this problem, Thimmegowda discloses a “wordline bridge” that physically and electrically connects the respective wordlines of two memory arrays the staircase, thereby allowing a single staircase to access both memory

arrays. Ex. 1005, Abstract; *see also, e.g., id.* (“wordline bridge between wordlines of adjacent tiles of memory cells [] reduce[s] the number wordline staircases in 3D memory arrays.”), 6:33-35, 9:62-66.

81. Fig. 3 illustrates “wordline bridge 306” shown in blue below.

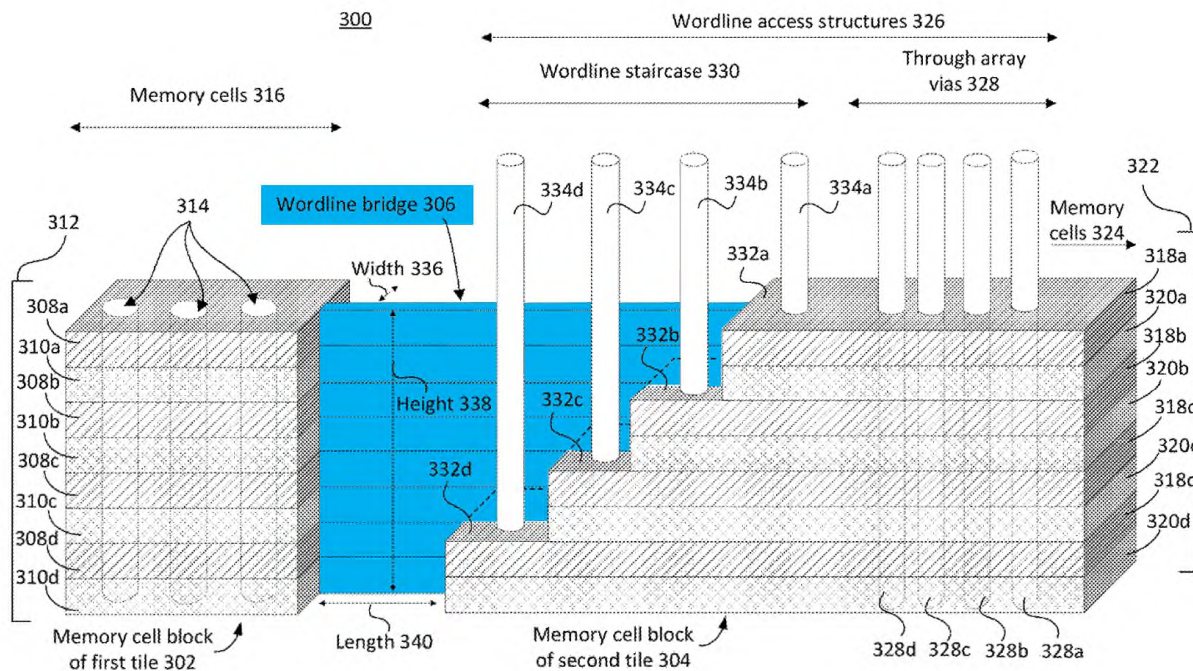


FIG. 3

Ex. 1005, Fig. 3 (annotated). “The wordline bridge 306 electrically couples the wordlines 308” for the left memory block “to the wordlines 318” for the right memory block “to enable the wordline access structures 326 to access the wordlines 308.” *Id.*, 9:46-51; *see also id.*, 8:25-31 (“wordline bridge system 300 includes a memory cell block of the first [memory] tile 302 and a memory cell block of a second [memory] tile 304 electrically coupled together with a wordline bridge 306,

according to one embodiment.”). As can be seen by the arrow pointing to memory cells 324, there is an array (block) to the right that is not shown in the figure.

82. “[W]ordline staircase 330” is between the two memory blocks. The staircase “includes a wordline staircase step 332a that provides access to the wordline 318a, a wordline staircase step 332b that provides access to the wordline 318b,” and so forth.” Ex. 1005, 9:27-45. “The wordline staircase 330 provides access to the wordlines 318 for metal contacts 334.” *Id.*, 9:42-45.

83. Thimmegowda’s wordline bridge enables a single conductive contact (*e.g.*, 334a) to bidirectionally drive memory cells in the memory arrays on either side of the bridge (*viz.*, the memory cell block of first memory tile 302 on the left of Fig. 3 and memory cell block of second memory tile 304 on the right) of the 3D memory device. Ex. 1005, 9:49-51; 7:61-64. Thus, a stairstep electrically couples to a respective gate layer (wordline) in both of the blocks on the right and left. This bridge provides the same bidirectional driving of memory cells as the ’604 patent’s bridge.

B. Lee

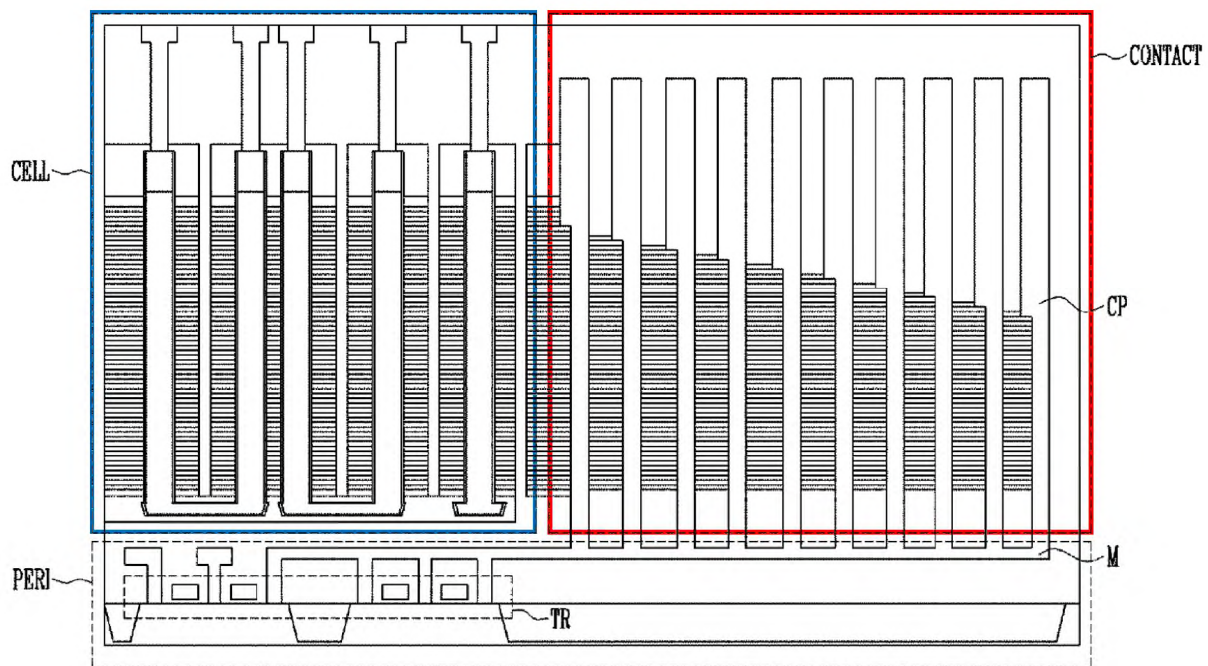
84. I understand that Lee is prior art.

85. Lee also discloses conventional 3D memory device features, including an alternating conductor/dielectric layer stack (memory stack_), memory strings

extending therethrough that form memory strings (channel structures), staircase, staircase contacts, etc. *See, e.g.*, Ex. 1007, [0005]-[0006].

86. Lee discloses a “cell” region (where the memory strings are located, which is also known as the cell region or array) and a “contact” region (the staircase region). Ex. 1007, [0063]-[0064].

FIG. 14A



Id., Fig. 14A (annotated).

87. Lee discloses that “the contact plugs” (staircase contacts) “are to be formed with varying depths ... [which] may make it more difficult to manufacture the memory device.” Ex. 1007, [0007]. This is because the staircase contacts must extend to different steps (to each step for a connection to a respect wordline). Lee

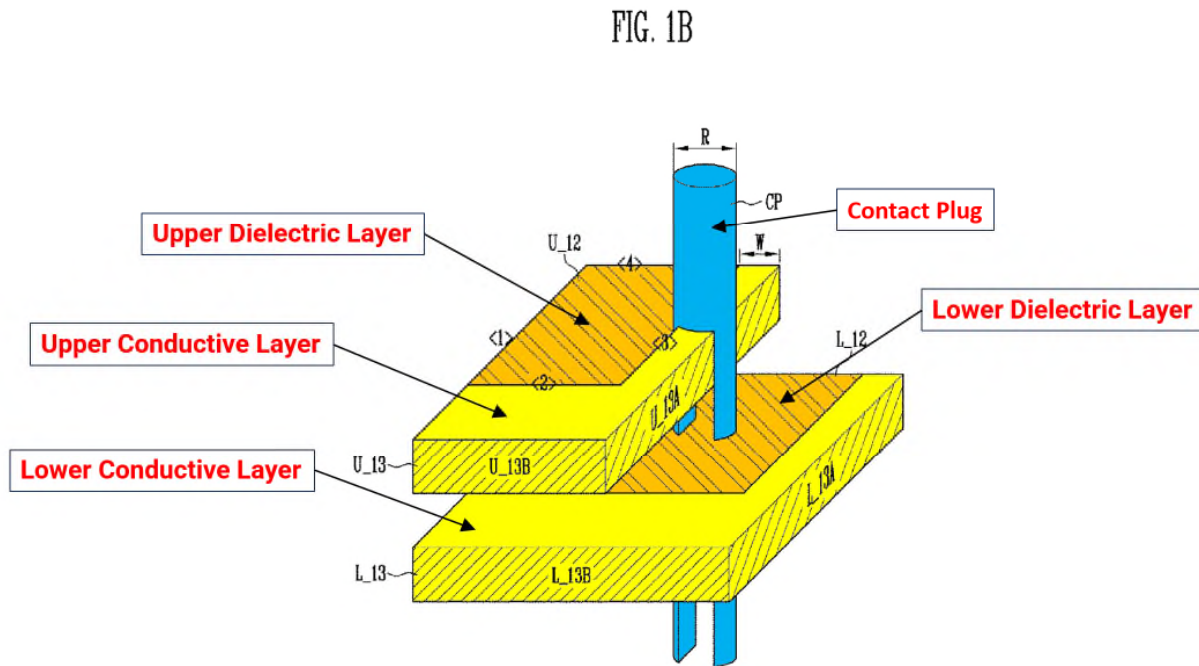
discloses that “the contact plugs may pass through the word lines to form a bridge² [*i.e.*, a short].” *Id.*

88. Lee solves the punch through issue by teaching an “interconnection structure” that includes alternating insulating and dielectric layers “stacked stepwise,” with “conductive layers interposed between the insulating layers and surrounding sidewalls of the dielectric layers.” Ex. 1007, [0008]. Lee’s interconnection structure includes contact plugs coupled to the conductive layers that “may at least partially pass through the dielectric layers.” *Id.* Like the ’604 patent, the contact plugs (staircase contacts) may extend past the target gate layer because under that structure, is not a dielectric layer and then conductive layer (like some alternative designs).

89. As shown below, both steps in Lee’s interconnection structure include a dielectric layer (U₁₂ and L₁₂, respectively) with two “sidewalls ... surrounded by [] conductive layers” U₁₃ and L₁₃, respectively. Ex. 1007, [0028]. Lee

² Lee uses the term “bridge” differently than the ’604 patent to indicate a short circuit due to punch through. Basically, the staircase contact would contact multiple conductive gate layers and “bridge” those conductive elements.

describes the distinctive conductive structures (highlighted in yellow) as “L-shape[d].” *Id.*, [0029].

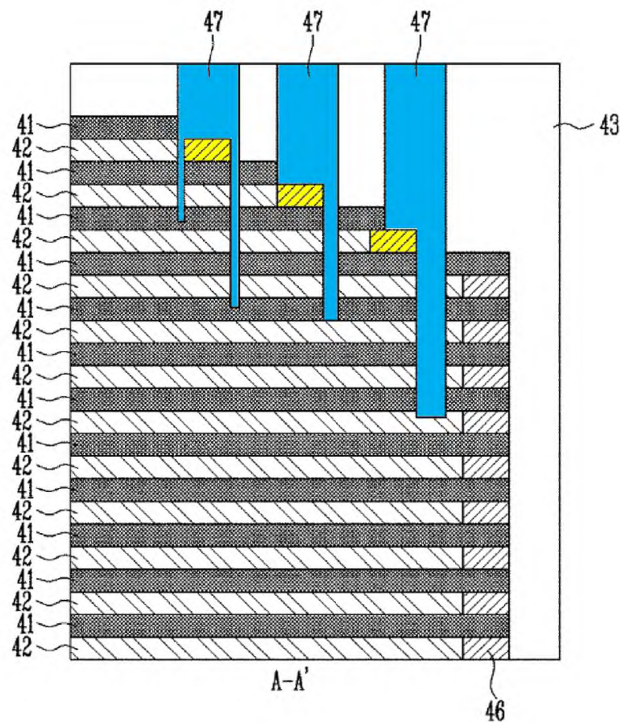


Id., Fig. 1B (annotated). Lee explains that “insulating layers 11” are also present “between [the horizontal layers in Fig. 1B],” but are not shown “for convenience of explanation.” *Id.*, [0028].

90. As shown above, the contact plug (highlighted in blue) extends through an underlying step without causing a short circuit to another wordline because the step below includes a dielectric region (highlighted in orange). Ex. 1007, [0031]. Again, this this is known as punch through, because the staircase punches through the target landing spot. Thus, Lee solved the purported “punch through” problem using the same technique described in the ’604 patent.

91. Lee also illustrates the over-etch punch through scenario in Fig. 10A. Here, various contact plugs 47 (highlighted in blue) punch through the target landing pads (highlighted in yellow) through underlying insulating layers 41 and sacrificial layers 42 with no negative effects. Ex. 1007, [0056].

FIG. 10A

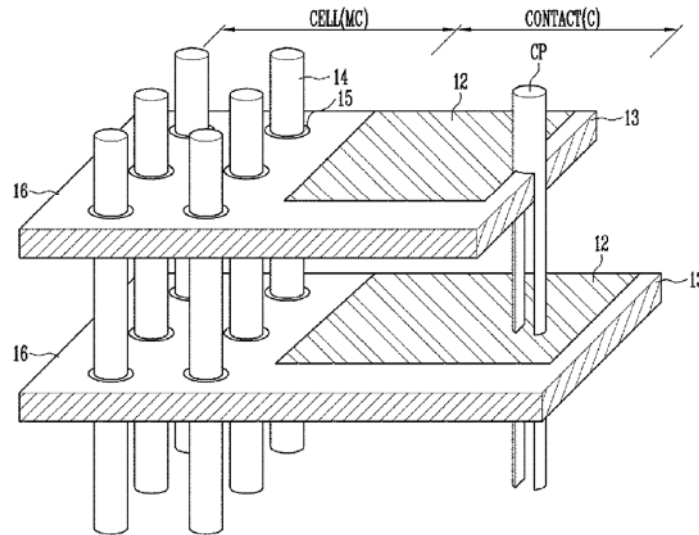


Id., Fig. 10A (annotated); *see also id.*, [0056].

92. When implemented in a 3D memory device, it is apparent how the contact plugs connect (physically and electrically) to the conductive layers 13 to access and control the memory strings in the cell region. Ex. 1007, [0033]. Specifically, as shown below, there is a conductive path from the contact landing

spot on the conductive gate step to the cell area, thus electrically coupling the staircase contact the respective gate layer.

FIG. 1C



Id., Fig. 1C.

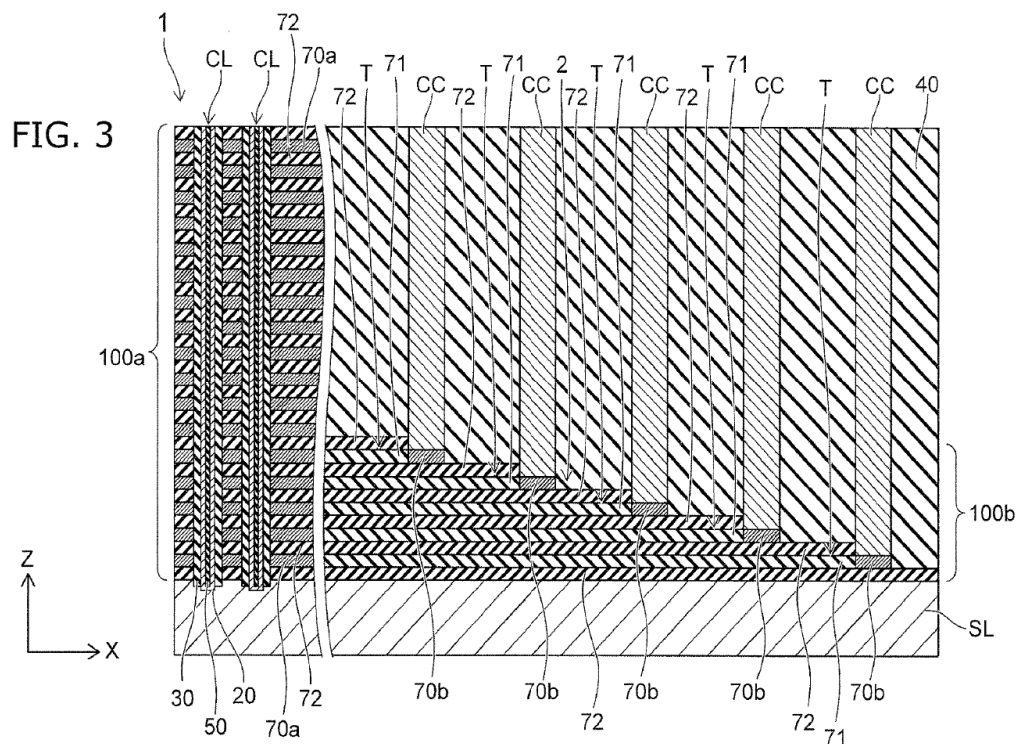
C. Kobayashi

93. I understand that Kobayashi (Ex. 1006) is prior art.

94. Kobayashi relates to a “three-dimensional memory device.” Ex. 1006, [0003]. Kobayashi, like Thimmegowda and Lee, discloses the basic features of conventional 3D memory devices, including memory cell arrays with “memory strings” (channel structures) extending through alternating layers of conductors and insulators (the memory stack), a staircase region, wordline contacts (staircase contacts), etc. *Id.*, Fig. 3, [0029] (wordlines), [0042] (memory strings), [0046]

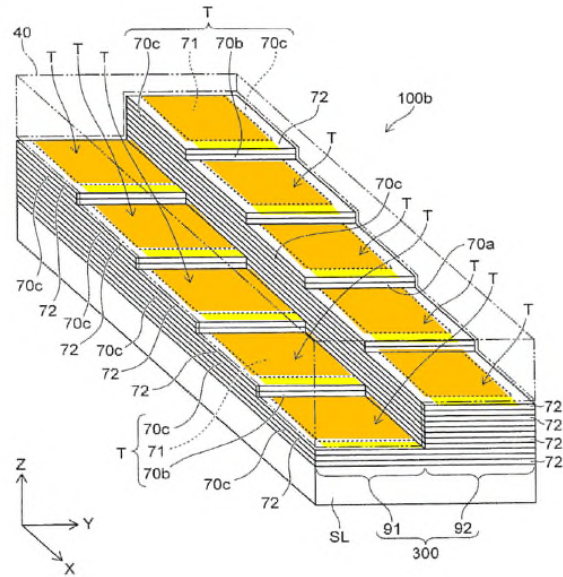
(staircase), [0085] (wordline contacts). Kobayashi's conductive layers 70a are the wordlines.

95. To provide access to the wordlines, Kobayashi proposes “contacts CC extending in the Z-direction” that “reach the terrace portions T” (*i.e.*, landing pads) of the staircase. Ex. 1006, [0085]-[0086]. The contacts are widely known as staircase contacts. Fig. 3 illustrates these contacts that extend down to stairs.



Id., Fig. 3.

96. As shown above in Fig. 3, the entire step is not conductive. This is better seen in Figures 1 and 5 below. Instead, each step includes a thin conductor 70b (yellow) portion horizontally adjacent to a dielectric “spacer portion 71”



Id., Figs. 1 and 5.

53

portion 70b and the second conductive portion 70c are connected in an L-shaped configuration”), [0079].

98. These two conductive portions effectively form a bridge, because it creates a conductive path between the staircase landing pad and the respective gate layer in the array.

99. Recall that the interior of the L-shaped conductors comprises a dielectric “spacer 71.” Ex. 1006, [0069]-[0072], [0079]-[0082] (“The spacer portion 71 is provided on the inner side of the first conductive portion 70 b and the second conductive portion 70 c forming the L-shape. The spacer portion 71 is an insulating portion.”). Kobayashi, like Lee, uses this approach to solve the punch through problem. As shown in Fig. 33B below, the use of dielectric spacer 71 creates the same underlying dielectric layers. *Id.*, [0139]-[0144]. Thus, this solves the same punch-through problem as the ’604 patent, because over-etching (punch through) will not result in the staircase contact inadvertently electrically coupling to a conductive layer underlying the target gate layer.

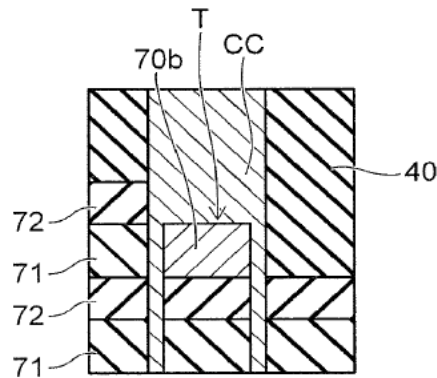


FIG. 33B

Id., Fig. 33B, [0141] (“[b]ecause the spacer portions 71 are silicon nitride layers and are insulating bodies, the contact CC is not shorted to the first conductive portions 70 b of the other layers even when the contact CC reaches the spacer portions 71 of the other layers lower than the first conductive portion 70 b to be connected.”).

XII. GROUND 1: THIMMEGOWDA IN VIEW OF LEE AND A POSITA’S KNOWLEDGE

100. Thimmegowda in view of the teachings of Lee and a POSITA’s knowledge renders claims 1-5 and 8-13 obvious.

A. Motivation to Combine

101. A POSITA would have been motivated to combine the teachings of Thimmegowda and Lee with a reasonable expectation of success for several reasons.

102. My analysis focuses on the combination of Thimmegowda’s bridge and array architecture teachings that enables a single staircase to bidirectionally drive two arrays and Lee’s stairstep teachings that mitigate punch through.

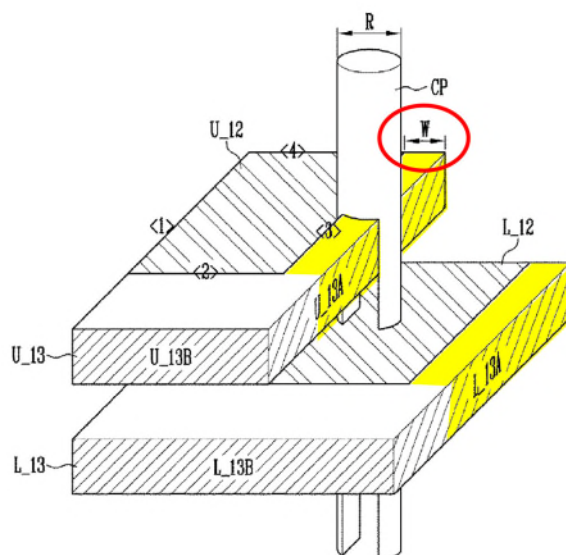
103. A POSITA would have been motivated to apply Lee’s teaching of non-overlapping conductive fingers to mitigate the well-known punch through problem in Thimmegowda’s staircase. This problem was well known. Specifically, because of the radically shrinking dimensions of 3D memories, such as NAND, it was challenging to etch a hole precisely to the appropriate landing spot for a staircase contact. In other words, punch through refers to punching through (below) the target landing spot. *See, e.g.*, Ex. 1021 (U.S. Pat. No. 11,239,248), 13:2-11 (“forming electrically conductive contact structures . . . may undesirably punch through the one or more of the electrically conductive materials”); Ex. 1022 (U.S. Pat. No. 11,217,601), 1:66-2:1 (discussing “undesirable defect[]” of “word line contact punch through”), 9:62-10:6; Ex. 1023 (U.S. Pat. No. 12,087,572), 3:52-58 (describing “punch through” problem that causes “yield loss.”), 7:42-46 (discussing “undesirable” “punchthrough” problem), 7:61-63 (same); Ex. 1024 (U.S. Pat. Pub. No. 2021-0193536), Fig. 5, [0061] (same), [0079]-[0080] (same).

104. For an issue such as punch through, a POSITA would look to known solutions (or mitigating techniques). Lee, for example, proposes such a solution. I discuss Lee extensively at Section XI.B. Lee discloses using non-overlapping conductive fingers to mitigate the effects of punch-through. Ex. 1007, [0037]-[0038], [0056]. That is, below a finger, dielectric layers exist, such that a punch through results in the hole extending into dielectric. A POSITA would have known

this solution was applicable to Thimmegowda, because both Thimmegowda and Lee disclose 3D NAND memory devices with the basic staircase structure that includes steps for the staircase contacts. Lee discloses forming multiple sets of staircases (labeled “interconnection structures C1 to C3”) that all employ the “finger” approach (see Ex. 1007, Fig. 1). But Lee’s finger approach is readily applicable to the single staircase, because it is simply a technique that uses the dielectric portions on the conductive levels to form a staircase such that dielectric layers are below the respective landing pads for staircase contacts.

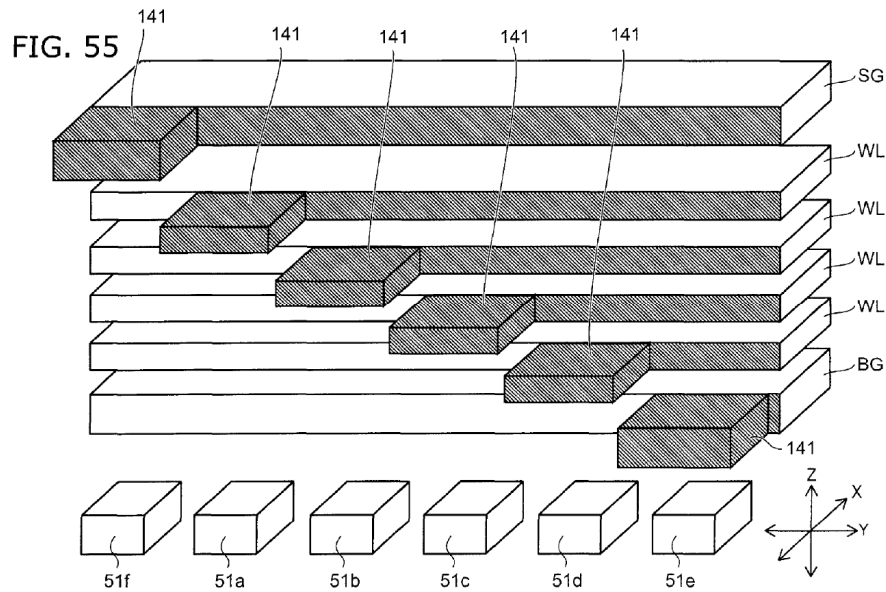
105. I note that two implementations of Lee’s finger approach would have been obvious to a POSITA. First, it would have been obvious to use a “thin” finger narrower (in the x-direction) than the width of a step. Lee, for example at Fig. 1B, expressly discloses. Again, the dielectric portion at the conductive level (the non-finger portion at that level) mitigates the punch through problem.

FIG. 1B



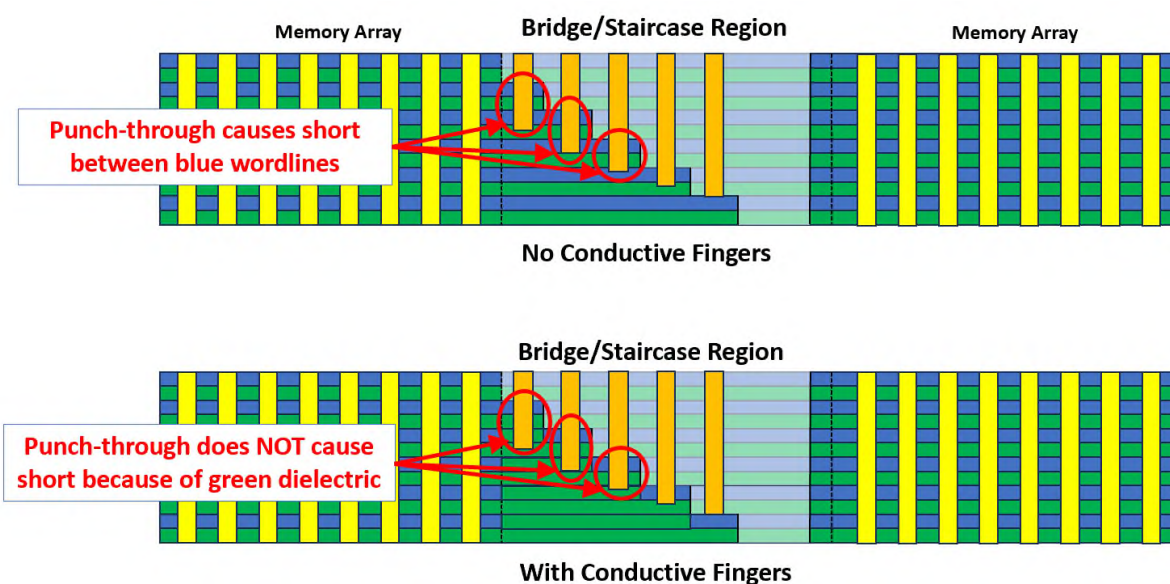
Ex. 1007, Fig. 1B (annotated) (showing finger with width “W” less than step width).

106. Second, it would also have been obvious to make the conductive finger cover the full width of the step. Thimmegowda, for example, includes landing pads like this. Using such wider fingers was also a known solution to punch through. Nakaki, for example at Fig. 55 below, discloses non-overlapping conductive fingers that cover the full exposed surface area of each stairstep. Ex. 1011 (U.S. Pat. No. 9,029,938), 14:64-65 (“the end parts 141 of the aforementioned staircase structure section 140 are provided as contact parts”), 15:10-11 (“The contact parts 141 do not overlap each other in the Z-direction.”).



Id., Fig. 55; *see also id.*, Fig. 56. This likewise solves the punch through problem, because as can be seen, dielectric layers will be under the landing pads.

107. I illustrate this below. The blue layers represent conductive wordlines, the green layers are dielectric, the orange pillars are wordline vias, and the yellow pillars are memory strings.



108. The top figure does not employ a “finger” approach, and as can be seen, the blue conductive layers extend all the way to the staircase landing spots for each respective stairstep. As a result, underneath each landing spot, there are conductive step portions from underlying steps. If when forming the staircase contacts (also known as wordline vias) the etch punches through the target landing spot on a step, the hole will extend to underlying conductive portions. After forming the staircase contact, that contact will electrically short the two wordlines (gate layers) together.

109. The lower figure from above employs conductive fingers that cover the full width of each exposed step. But adjacent to each step (in the x-direction) is green dielectric material, instead of conductor, e.g., that is left from a sacrificial gate. This is the approach that mitigates the punch through issue. Even though the staircase contacts (or wordline vias) “punch through” the target landing area, they

extend in the z-direction through additional dielectric and do not create a short to another wordline. Again, punch through actually refers to the etch that creates the hole, which the contact later fills. .

110. Recall that Thimmegowda's staircase case landing area already covers the full step width and the staircase contact lands in the middle of the step (*see* Ex. 1005, Fig. 3). Thus, the second figure below is illustrative of this approach in combination with employing a dielectric portion at the same level of the conductive portion, like Lee teaches. This mitigates the punch through problem with steps like Thimmegowda.

111. Lee discloses using the well-known gate-replacement process, and the remaining portions of the sacrificial gates form the dielectric portions on the same level of fingers. This provides additional motivation to combine Lee's finger (and more generally gate replacement teachings) with Thimmegowda. I discuss above how the fingers mitigate the punch through problem. But the gate replacement process more generally provides another strong motivation to include Lee's teachings. In short, the gate replacement process enables metal gate layers (wordlines), typically tungsten, instead of, typically, polysilicon gate layers. A major advantage of tungsten gate layers is lowering the resistance or capacitance load when driving a wordlines (corresponding to a conductive gate layer in the

stack). This enables, for example, faster read and write operations. This was textbook material before the '604 patent's priority date. See Ex. 1018, 131-32.

112. I also note that employing the bridge and staircase architecture of Lee was separately beneficial. As I discuss in Section XI.A., this eliminates the need for a staircase per array, because it enables a staircase contact on a single side of a staircase to bidirectionally drive two arrays. Thus, Lee's teachings and Thimmegowda's teachings are complementary to one another.

113. A POSITA would have had a reasonable expectation of success in combining the teachings of Thimmegowda's bridge and array architecture (to drive two memory arrays with one wordline via) with Lee's staircase finger approach (to mitigate punch through). Thimmegowda and Lee relate to 3D NAND memory devices and share the basic building blocks of a memory stack, staircase, and staircase contacts. Recall the memory stack is a stack of alternating gate (wordlines) and dielectric layers. The staircase provides the landing spots for staircase contacts, which are the contacts to the gate layers (wordlines). See Ex. 1007, Fig. 1C; Ex. 1005, Fig. 3. Implementing Lee's finger approach with Thimmegowda's bridge does not change other areas of the 3D NAND device, for example, the circuitry that drives voltages to the staircase contacts to effectuates access operations, e.g., read and writes. Similarly, employing Thimmegowda's bidirectional bridge teachings to

Lee would not have any impact on how Lee's finger approach mitigates punch through.

114. Thimmegowda's bridge architecture is fully compatible with Lee's gate replacement manufacturing process. A key building block of a 3D NAND is the memory stack. Portions of that memory stack become the staircase and the bridge. The stack is simply alternating layers of conductive gate layers and dielectric layers. That Thimmegowda forms the stack without gate replacement is irrelevant to its bridge teachings. Specifically, whether that bridge is made with or without gate replacement, it performs the same exact function. Indeed, when viewing simply the Thimmegowda figures, one would not be able to tell whether that structure was made with gate replacement. As I describe above, the gate replacement process was textbook material. And as to the Lee fingers specifically, Lee details that process. See Ex. 1007, Figs. 4-13B (and accompanying discussion at [0043]-[0062] describing the gate replacement manufacturing process in detail, especially [0044]-[0045], [0048], [0050], and [0053]-[0055]). Thus, a POSITA would have had a reasonable expectation of success in combining the above teachings from Thimmegowda and Lee.

B. Claim 1:

115. Ground 1 renders claim 1 obvious.

1. [1.PRE] “A three-dimensional (3D) memory device, comprising:”

116. I form no opinion regarding whether the preamble is limiting. But Thimmegowda discloses *[a] three-dimensional (3D) memory device*. Ex. 1005, Title (“Wordline Bridge in a **3D Memory Array**”) (emphasis added); *see also id.*, Abstract, Fig. 3, 1:11-12, 1:64-66.

2. [1.A] “a memory array structure; and”

117. Thimmegowda discloses *a memory array structure*. Ex. 1005, Abstract (“The present disclosure relates to providing a wordline bridge ... **in 3D memory arrays. An apparatus may include a memory array having memory cells.**”) (emphasis added); 2:57-65 (“The memory array includes a plurality of memory cells.”).

118. Fig. 2 below shows “[t]he memory die 200 includes a memory array 202 ... [which] includes memory cells 205 and memory cells 206 that are accessed (e.g., read/write) with the peripheral circuitry 204.” Ex. 1005, 7:7-11. As can be seen, there are memory arrays on the left (205) and on the right (206) in respective memory blocks (212) and (224).

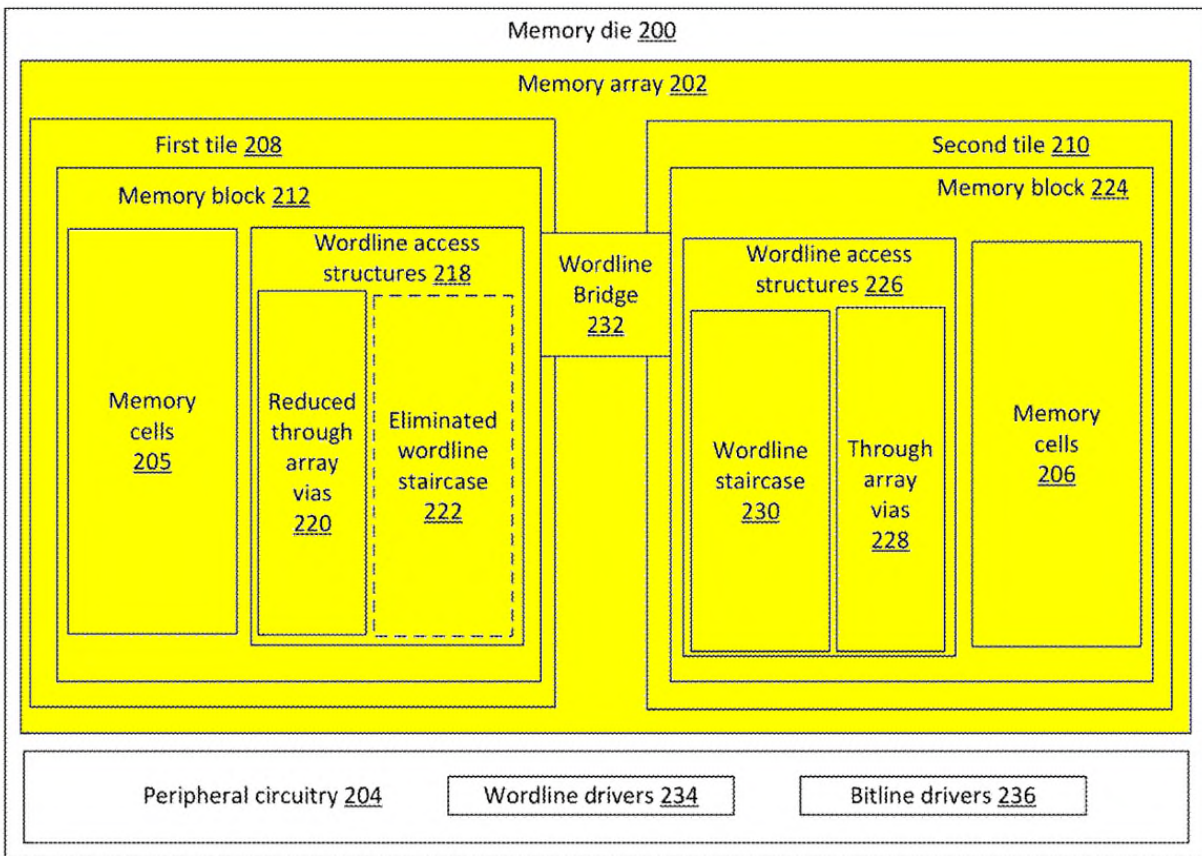


FIG. 2

Id., Fig. 2 (annotated); *see also* Fig. 3.

3. [1.B] “a staircase structure in an intermediate of the memory array structure and dividing the memory array structure into a first memory array structure and a second memory array structure along a lateral direction, the staircase structure comprising”

119. Thimmegowda discloses element 1[b]. Thimmegowda discloses its “memory arrays are terminated with one or more staircase structures, to allow connection metal contact structures to be connected to the wordlines. The staircase structures include a step or landing for each wordline, to connect each wordline to a metal contact.” Ex. 1005, 1:12-17. Thimmegowda’s wordline staircase 330 (shown

in Fig. 3 below) is the claimed *staircase structure*. Note the arrow pointing to the right under “memory cells 324” that points to the right memory block.

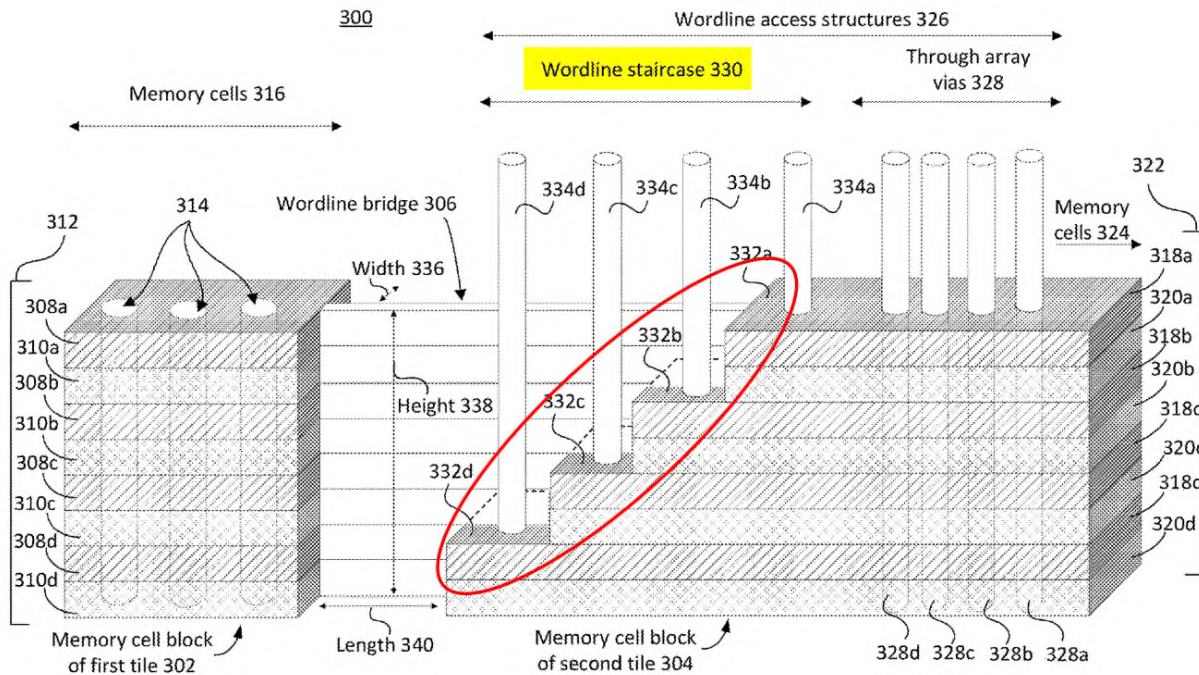


FIG. 3

Id., Fig. 3 (annotated); *see also id.*, Fig. 2. Fig. 3 also shows that the staircase structure is located *in an intermediate of the memory array structure and dividing the memory array structure into a first memory array structure and a second memory array structure along a lateral direction*. In other words, the staircase 330 is between the memory cell block of first tile 302 (located on the left in the lateral x-direction) and the memory cell block of the second tile 304 (located on the right in the lateral x-direction). *See also id.*, 7:16-17 (“The memory array 202 is segmented into a first tile 208 and a second tile 210”), 8:27-31. The staircase divides the

memory array structure into first and second memory array structures, because for example, the bridge is necessary to connect the respective gate layers of each first and second memory array structures.

4. [1.C] “the staircase structure comprising (i) a plurality of stairs extending along the lateral direction, and”

120. Thimmegowda discloses element 1[c]. Recall that the claimed *lateral direction* is the x-direction in Thimmegowda Fig. 3 (left and right on the page). As Fig. 3 shows, the staircase 330 comprises a *plurality of stairs* in the x-direction. Each stair providing a landing spot for a staircase contact. For example, Thimmegowda discloses that “[t]he wordline staircase 330 includes a wordline staircase step 332a that provides access to the wordline 318a, a wordline staircase step 332b that provides access to the wordline 318b,” and so forth. Ex. 1005, 9:27-38; *see also id.*, 1:12-17 (“The staircase structures include a step or landing for each wordline, to connect each wordline to a metal contact.”).

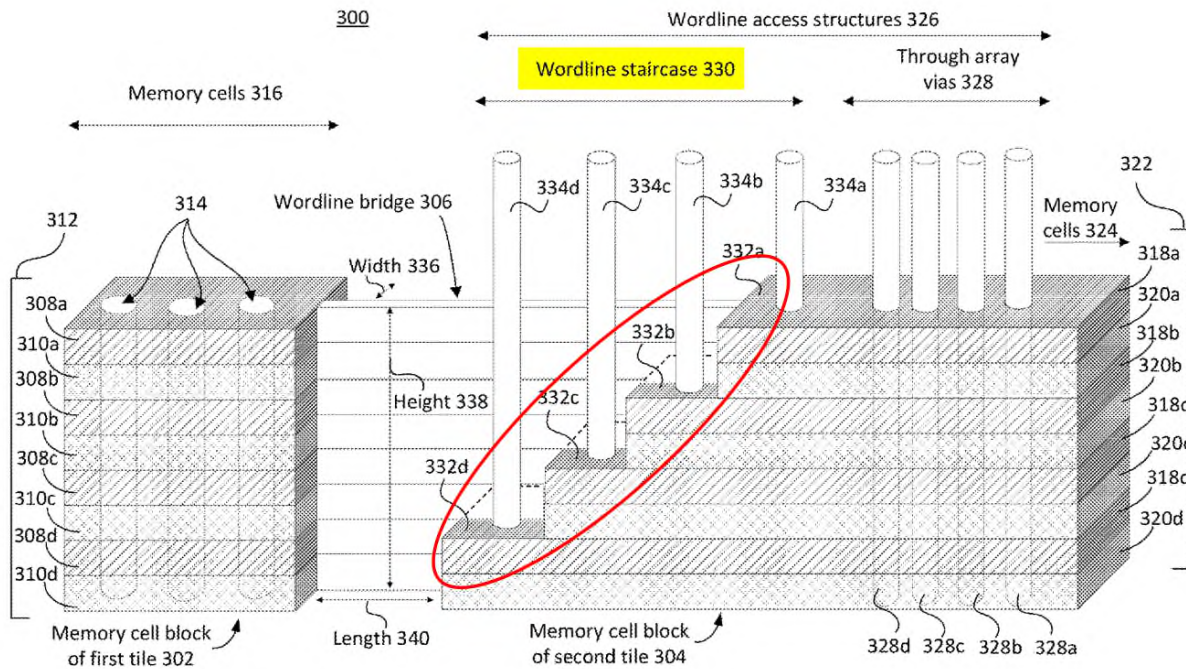


FIG. 3

Id., Fig. 3 (annotated).

5. [1.D] “the staircase structure comprising ... (ii) a bridge structure in contact with the first memory array structure and the second memory array structure,”

121. As an initial matter, I will describe how the '604 patent uses the term *bridge structure*. In short, the bridge provides a conductive path between the arrays, such that a staircase contact can bidirectionally drive both arrays. The '604 patent specification explains a bridge structure “can include vertically interleaved conductor layers and dielectric layers (not shown), and the conductor layers (e.g., metal layers or polysilicon layers) can function as part of word lines.” Ex. 1001, 7:66-8:2. The '604 patent illustrates an exemplary bridge structure 108 in Fig. 1B.

In the annotated version of Fig. 1B below (left), red lines have been added to reflect that bridge 108 is formed of alternating layers of materials. *Id.*, 5:66-6:1 (“The staircase structure can include a bridge structure that has interleaved a plurality of conductor layers and dielectric layers.”). And, as shown in the top-down view of Fig. 1C below (right), the bridge structure 108 extends horizontally in the x-direction between two memory arrays (*viz.*, bridging them together). This enables the stairsteps of each the staircase to electrically couple to each memory array.

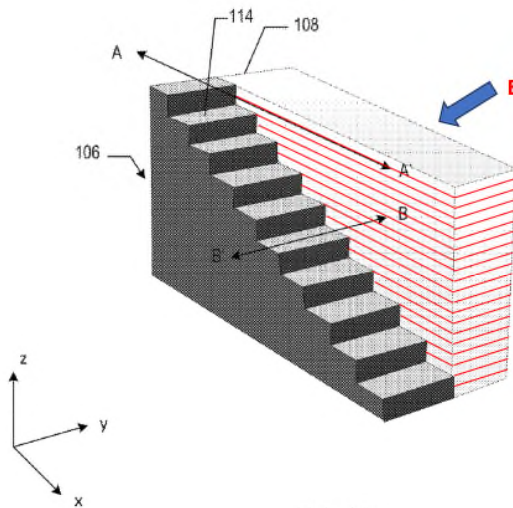


FIG. 1B

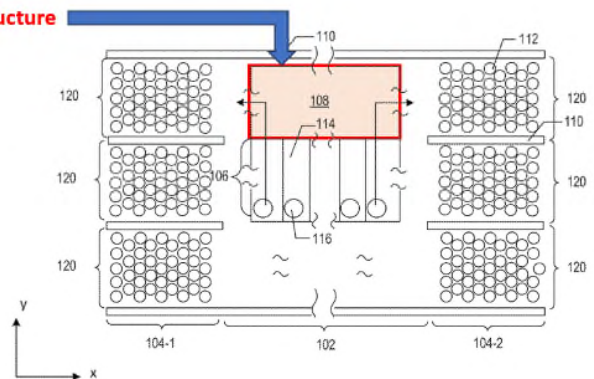


FIG. 1C

Id., Fig. 1B and 1C (annotated). Accordingly, one example of a “bridge structure” is an alternating stack of dielectric and conductive layers connecting two memory arrays.

122. Thimmegowda satisfies element 1[d]. Thimmegowda discloses a “wordline bridge 306,” shown in blue below in Fig. 3, which comprises the claimed *bridge structure*. Fig. 3 also shows the bridge structure in contact with the two

memory array structures. Viewing the figure below, the bridge extends to the back side of the staircase (going into the page in the Y-direction), and thus the gate layers in each array on the left and right electrically couple together. In other words, behind the staircase (in the Y direction) the bridge extends to both memory blocks.

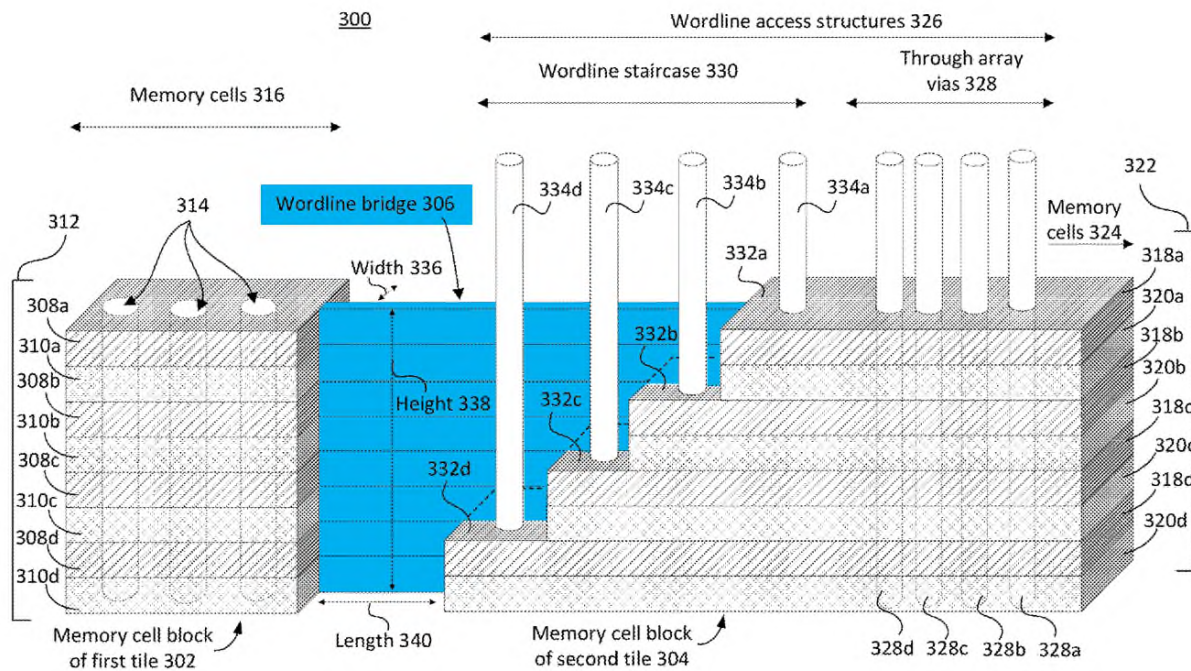


FIG. 3

Ex. 1005, Fig. 3 (annotated); *see also id.*, Figs. 1 and 2 (showing wordline bridge in electrical and physical contact with two memory arrays). As previously explained, “[t]he wordline bridge 306 electrically couples the wordlines 308 to the wordlines 318 to enable the wordline access structures 326 to access the wordlines 308, ... The wordline bridge 306 includes the same layers as the wordline stacks 312, 322.” *Id.*, 9:46-60; *see also id.*, 2:35-44.

123. Thimmegowda explains its wordline bridge enables a single staircase to bidirectionally drive memory arrays on either side of the bridge. *See, e.g.*, Ex. 1005, 7:61-64. This refers to the conductive portion of the stairsteps electrically coupling to each array on the left and right, and the bridge enables the electrical coupling from a single staircase.

124. For example, the claimed *first memory array structure* corresponds to “memory cell block of first tile 302” and the claimed *second memory array structure* corresponds to “memory cell block of second tile 304” in Fig. 3. Wordline staircase 330 (and/or the wordline access structure 326 which include staircase 330) is *in contact with* each memory block. Ex. 1005, 6:48-60. Again, each step has a conductive path through the bridge to respective wordlines in the memory stack in each memory block.

125. Through array vias 328 in Fig. 3 do not change that Thimmegowda discloses *a bridge structure in contact with the first memory array structure and the second memory array structure*. The through array vias are vertical pillars that extend through a portion of the layers and a conductive path still exists.

126. Thimmegowda’s wordline bridge is part of the claimed *staircase structure* as that term is used in the ’604 patent. Ex. 1001, Fig. 1A and 1B (showing “staircase structure 102” comprising both a “plurality of stairs 114” and a “bridge structure 108”), 2:51-54, 7:42-43 (“FIG. 1B depicts staircase structure 102 having a

staircase 106 and a bridge structure 108, in contact with each other.”). The ’604 patent considers the bridge part of the staircase structure because it electrically couples the stairsteps to the memory arrays. *Id.*

6. [1.E] “the plurality of stairs comprising a stair above one or more dielectric pairs,”

127. As an initial matter, I will describe how the ’604 patent uses the term *dielectric pairs*. The ’604 patent specification explains that “[i]n some embodiments, each stair 414 includes a pair of sacrificial layer 429 and an underlying dielectric layer 426 (e.g., one sacrificial/dielectric pair).” Ex. 1001, 14:36-39. In other words, the combination of one sacrificial layer and its corresponding dielectric layer together for a single stair level comprise a “dielectric pair.” This is consistent with other teachings of the ’604 patent, which state that “the conductor portion is over one or more dielectric pairs, each including a dielectric portion and a dielectric layer in a lower stair,” where “the number of dielectric pairs under the conductor portion of a respective stair is equal to the number of stairs/levels under the stair.” *Id.*, 5:50-53; *see also id.*, 18:48-53 (“In some embodiments, the conductor portion and the dielectric layer are each above the one or more dielectric pairs.”). Thus, at least one example of a dielectric pair within the meaning of the claims is a sacrificial layer and its corresponding dielectric layer.

128. Thimmegowda, in view of Lee's teachings, discloses claim element 1[e]. Thimmegowda discloses "steps 332" that form part of the staircase. Ex. 1005, Fig. 3.

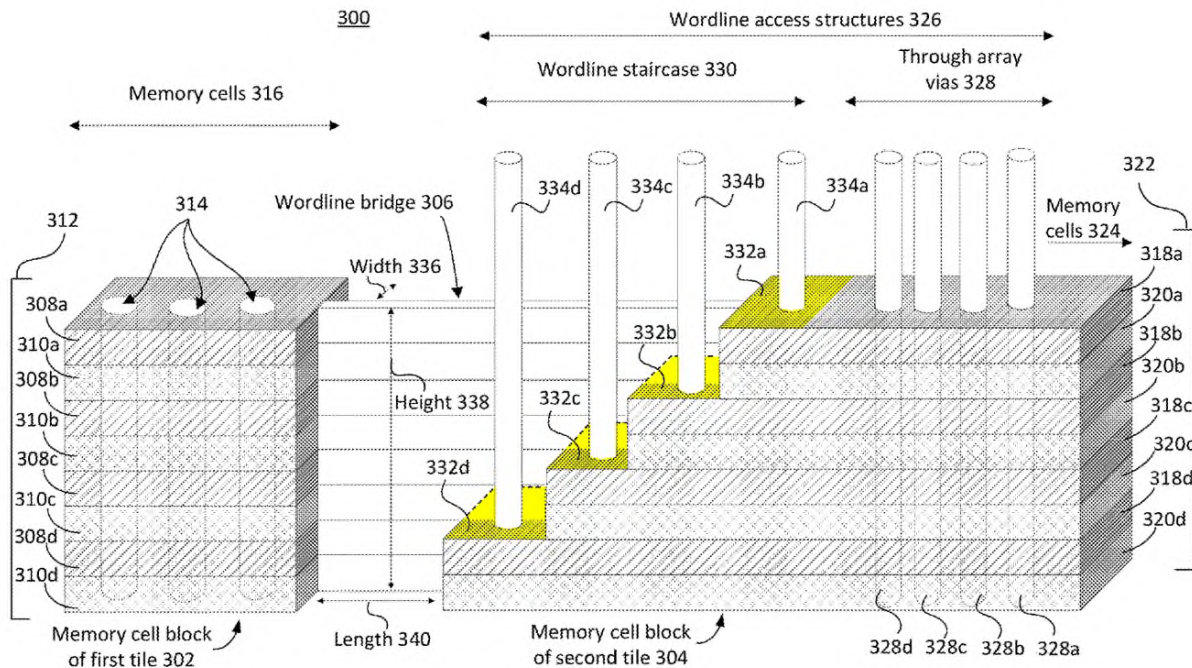
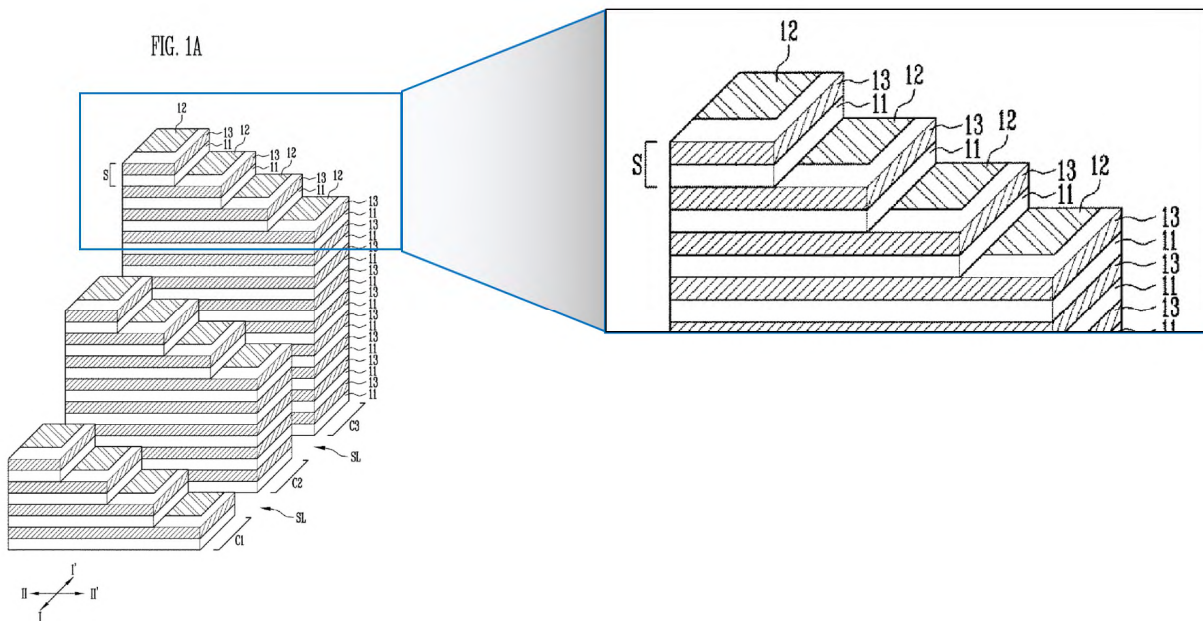


FIG. 3

Ex. 1005, Fig. 3 (annotated); *see also id.*, 9:27-38. Thimmegowda discloses that layers 310a-d and 320a-d are dielectric layers. *Id.*, 8:34-38, 8:4-50, 8:57-61, 8:67-9:6. These dielectric layers extend horizontally to form corresponding dielectric layers in the wordline staircase 330 and wordline bridge 306. These are the standard dielectric layers of a memory stack. Layers 310d (and corresponding layer 320d) form one layer of the claimed *dielectric pair*. *Id.* The same is true for layers 310c/320c and 310b/310b. *Id.*

129. Lee’s “finger” approach provides the other layer of the *dielectric pair*.

Lee Fig. 1A discloses a step “S” comprised of a lower insulating layer 11 beneath a dielectric layer 12 and conductive finger 13. See Ex. 1007, [0022]. The combination of dielectric layers 11 and 12 form a *dielectric pair*. These are two dielectric layers within a staircase level. And each step S in Lee is *above one or more dielectric pairs*, that is, above dielectric layers 11 and 12. *Id.*



Id., Fig. 1A (annotated). Lee further discloses that “in order that the pad region U_13A of the upper conductive layer U_13A may not overlap with the pad region L_13A of the lower conductive layer L_13, the dielectric layer L_12 may be located under the pad region U_13A of the upper conductive layer U_13.” *Id.*, [0031].

130. In sum, applying Lee’s finger approach to Thimmegowda results in a staircase structure that maintains *a stair above one or more dielectric pairs*, where the *dielectric pair*³ comprises one dielectric layer 310/320 (a dielectric layer of a conventional stack) in combination with the dielectric layer 12 from Lee. Thus, in the modified version of Thimmegowda’s bridge and array architecture, each stair (except for the bottom stair) is *a stair above one or more dielectric pairs*. This, in particular, solves the punch through problem that I discuss earlier.

7. **[1.F] “wherein: the stair comprises a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure, and”**

131. I will first describe the ’604 patent’s use of the term *conductor portion*. The ’604 patent specification states that the “conductor portion” “covers at least the landing area of the respective stair (e.g., a portion of the stair) such that a word line VIA contact can be in contact with and electrically connected to the respective stair.”

³ The ’604 patent discloses that “all the dielectric portions 324 and dielectric layers 326 underlying conductor portion 320 may be referred to as a dielectric structure 340, of which a thickness along the z-direction is equal to the distance between the bottom surface of the respective conductor portion 320 and the top surface of substrate 302.” Ex. 1001, 12:8-13.

Ex. 1001, 5:25-62. In other words, the conductive portion provides for a landing spot for the staircase contact. The '604 patent also notes that “the dimension of the conductor portion, along the direction the stairs extend ... does not laterally extend under [] the conductor portion of any upper stair.” *Id.* This refers to the solving the punch through problem with the dielectric pairs under the conductive portion of the gate. The '604 patent specification also teaches that “along the x-direction, a width d of conductor portion 320 may be equal to **or less than** the dimension of stair 314.” *Id.*, 11:19-21 (emphasis added). In other words, the conductive portion may extend the entire length of the stairstep in the X direction. The '604 patent specification also teaches that the thickness of the “conductor portion” (in the z-direction) may be the full depth of the sacrificial gate replacement layer 324. *See, e.g., id.*, 11:36-40 (“Along the z-direction, a thickness of conductor portion 320 may be equal to or less than that of dielectric portion 324.”); *id.*, 10:65-11:6 (“In some embodiments, in a respective stair 314, conductor portion 320 may be on and in contact with dielectric layer 326 without any second dielectric portion 322 in between.”). In other words, the conductive finger may be the same depth of the step.

132. Thimmegowda discloses a *stair compris[ing] a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure*. Shown below, the top/exposed surface of steps 332a-d are the *conductor portions* and connect to respective conductive metal layers in wordline bridge 306.

Again, this ultimately electrically couples the staircase with both arrays, thereby enabling the single staircase to drive both arrays on the left and the right.

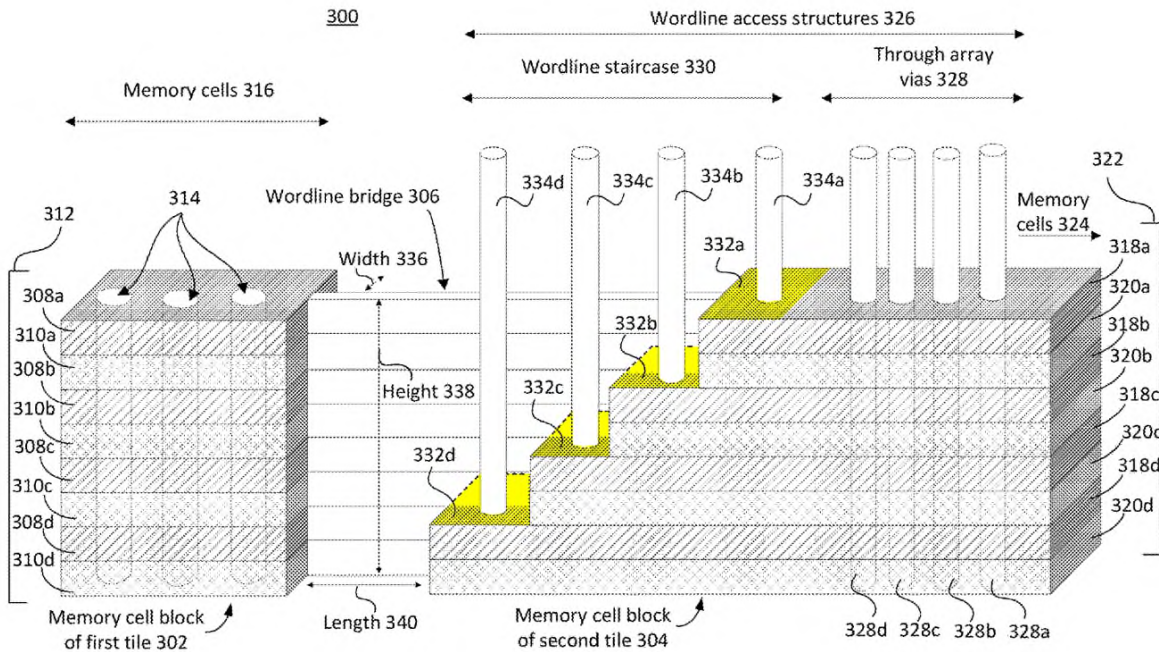


FIG. 3

Ex. 1005, Fig. 3 (annotated).

133. Specifically, Thimmegowda’s “wordline staircase 330 provides access to the wordlines 318 for metal contacts 334 (individually, metal contact 334 a, 334 b, 334 c, and 334 d).” Ex. 1005, 9:42-45. Put another way, the steps include landing spots for the staircase contacts. Then, “[t]he wordline bridge 306 electrically couples the wordlines 308 to the wordlines 318 to enable the wordline access structures 326 to access the wordlines 308.” *Id.*, 9:46-48. In sum, the staircase step includes a

conductive portion, including where the staircase contact lands, and there is a conductive path from that point to bridge and both array structures.

134. Applying Lee's "finger" approach to Thimmegowda also satisfies element 1[f]. In view of these teachings, the landing pads are in direct contact with the bridge, similar to how Lee's "upper conductive layer U_13 [] include[s] a pad region U_13A surrounding the terminal third sidewall <3>" that is in physical contact with the "connection region U_13B" (analogous to Lee's middle section 120) for connecting to the wordlines in the memory array as shown in Figs. 1B and 1C. Ex. 1007, [0030]. In other words, the conductive fingers extend into the bridge and electrically couples to each array, thereby driving both arrays.

FIG. 1B

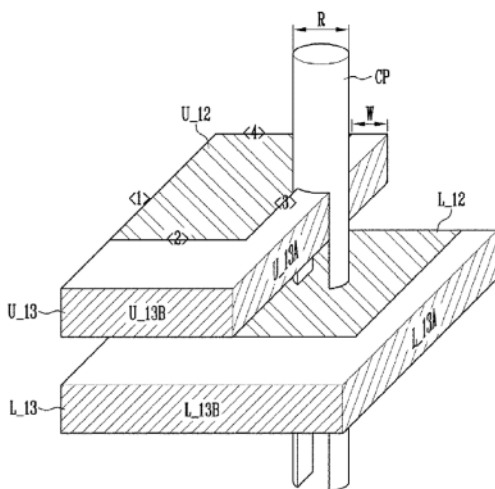
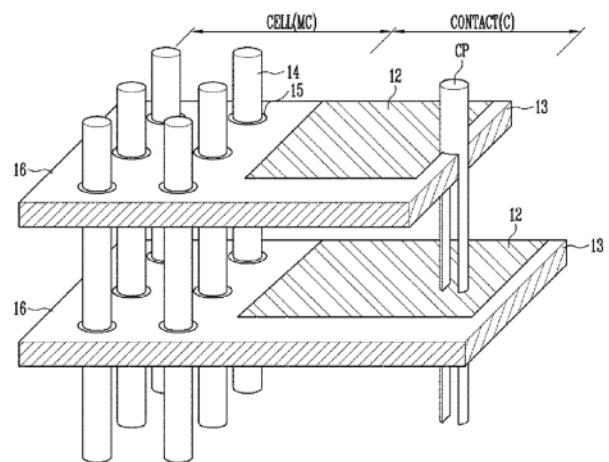


FIG. 1C



Id., Figs. 1B and 1C. I describe Lee's teachings further below. In Lee, the conductive portion has a narrower profile, which solves the punch through problem.

But importantly, that narrower profile extends into the bridge, directly contacting and bidirectionally driving both arrays.

8. **[1.G] “wherein: the stair comprises ... a dielectric portion at a same level and in contact with the conductor portion, the stair being electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure; and”**

135. My analysis under claim element 1[f] demonstrates that Thimmegowda discloses that the stair is *electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure*. See, e.g., Ex. 1005, 12:50-13:2 (“[T]he wordline bridge includes a plurality of polysilicon layers and a plurality of oxide layers. ... [E]ach of the plurality of polysilicon layers is connected to a wordline of the first block of the first ones of the plurality of memory cells and to a wordline of the second block of the second ones of the plurality of memory cells.”), 9:27-49. That is what allows the staircase contacts 334 to drive the memory arrays on both the left and right sides of the staircase structure, i.e., the conductive portion electrically couples to both array structures and uses the bridge to electrically couple to the left array. *Id.*, 7:61-64 (“The second tile 210 is electrically coupled to the first tile 208 through a wordline bridge 232, to facilitate sharing wordline access structures between the memory block 212 and the memory block 224”). Applying Lee teachings does not change

this, because the finger physically connects to the bridge, thereby electrically coupling to the bridge and each array. See claim [1.F].

136. Thimmegowda alone does not disclose the balance of element 1[g]. As I discuss, however, it would have been obvious to apply Lee’s finger approach, which discloses all aspects of element 1[g]. First, I will address the term: *a dielectric portion at a same level and in contact with the conductor portion*. As shown below, there are alternating layers of dielectric layer 326 and dielectric portion 324 that form stairs 314. That is, on each stair level there is a dielectric pair. The “dielectric portion 324” is located immediately adjacent to (in the x-direction), and in contact with, conductor portion 320. The ’604 patent expressly explains that “[c]onductor portion 320 may be in contact with a dielectric portion 324 (e.g., extending along the x-direction) **of the same level.**” Ex. 1001, 10:60-61 (emphasis added). In other words, this departs from an alternative approach wherein the entire conductive portion extends the entire X-length of the step.

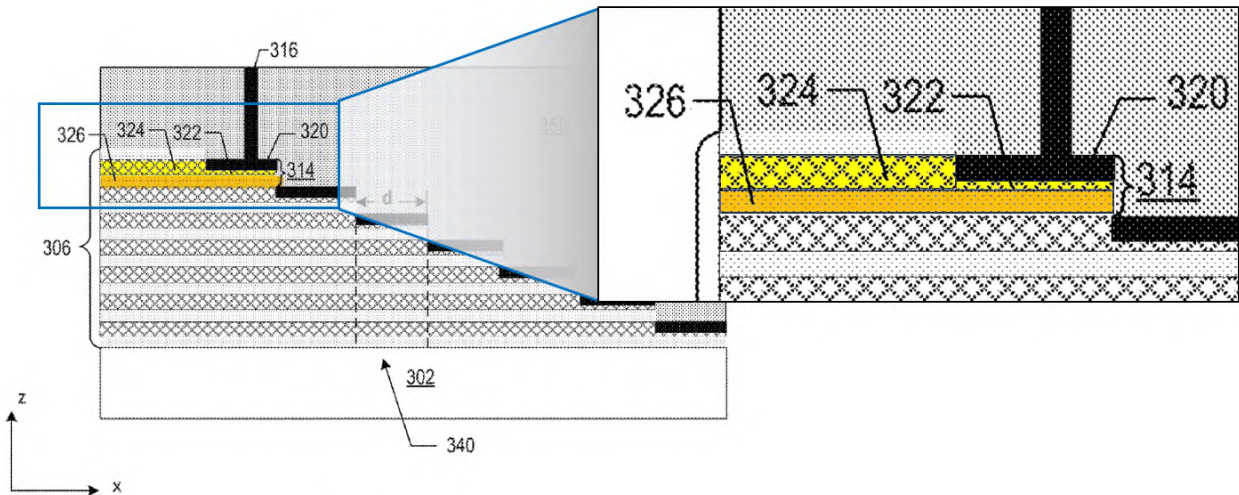


FIG. 3A

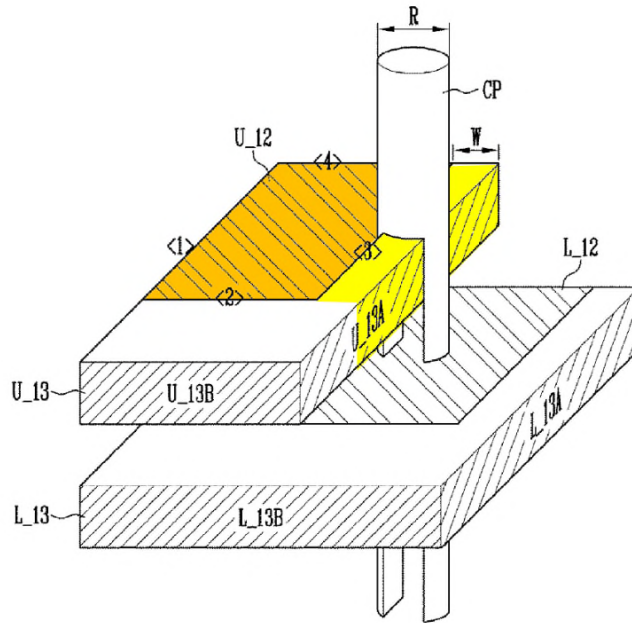
Id., Fig. 3A (annotated). While dielectric portion 324 also extends underneath conductor portion 320 in the example above, as I describe earlier, the '604 patent states the conductive portion may extend the entire Z-direction height of that portion of the step. *See, e.g., id.*, 11:36-40 (“Along the z-direction, a thickness of conductor portion 320 may be equal to or less than that of dielectric portion 324.”); *id.*, 10:65-11:1.

137. In both the unmodified and modified version of Thimmegowda, the *conductor portion* extends in the z-direction substantially the full depth of the conductive wordline layers 308a-d and 318a-d. *See* Ex. 1005, Fig. 3, 9:49-51 (“The wordline bridge 306 includes the same layers as the wordline stacks 312, 322”); Ex. 1007, Fig. 1A (conductor 13), Fig. 1B (conductors U_13A and L_13A).

138. As I explain for limitation [1.E]-[1.F], applying Lee teachings to Thimmegowda's bridge and array architecture results in conductors on staircase steps 332a-d that are approximately the width of the step (as shown in Thimmegowda Fig. 3) or narrower (as shown in Lee Fig. 1B) and extend laterally in the y-direction to directly contact the wordline bridge 306. In the parlance of the '604 patent, these conductive portions are the fingers that extend into the bridge. This is similar to how Lee's conductive strips (*e.g.*, U_13A and L_13A in Fig. 1B) that are in physical and electrical contact with the wordlines, except that they extend in the Y direction. See Ex. 1007, Fig. 1C; Section XII.A. In modified Thimmegowda bridge and array architecture, the area immediately adjacent to the finger (in the x-direction toward the righthand memory array) is an insulator (*viz.*, *dielectric portion*), similar to what Lee illustrates (and describes) in Fig. 1B. *Id.*, [0028] ("Referring to FIG. 1B, sidewalls of an upper dielectric layer U_12 may be surrounded by an upper conductive layer U_13, and sidewalls of a lower dielectric layer L_12 may be surrounded by a lower conductive layer L_13."); *id.*, [0029] ("[T]he upper dielectric layer U_12 may include four sidewalls <1> to <4>. ... The third sidewall <3> may be ... surrounded by the upper conductive layer U_13."). As I discuss when describing Lee, this is what solves the punch through problem (as Lee teaches), i.e., because the respective insulator portions are underneath landing pads above.

139. In Lee Fig. 1B below, there is *a dielectric portion* [insulating portion U_12, highlighted in orange] *at a same level and in contact with the conductor portion* [landing pad U_13A, highlighted in yellow] which was not replaced during the gate replacement process. Lee, [0028], [0048]. Again, this is what solves the punch through problem, as one can see below the staircase contact extending into a dielectric portion on the underlying stairstep. In view of applying these teachings of Lee to Thimmegowda, the dielectric material that is left after replacing portions of the sacrificial layer with a conductor is *at a same level and in contact with the conductor portion* [the finger]. Again, Lee intentionally creates this dielectric portion such that underlying a staircase contact, there are these dielectric portions to avoid the punch through problem. That is *at a same level and in contact with the conductor portion* is met is true regardless of whether the *conductor portion* (i.e., the finger) in modified Thimmegowda is the full width of the exposed landing pad area of a step or a narrower conductive strip (as in Lee).

FIG. 1B

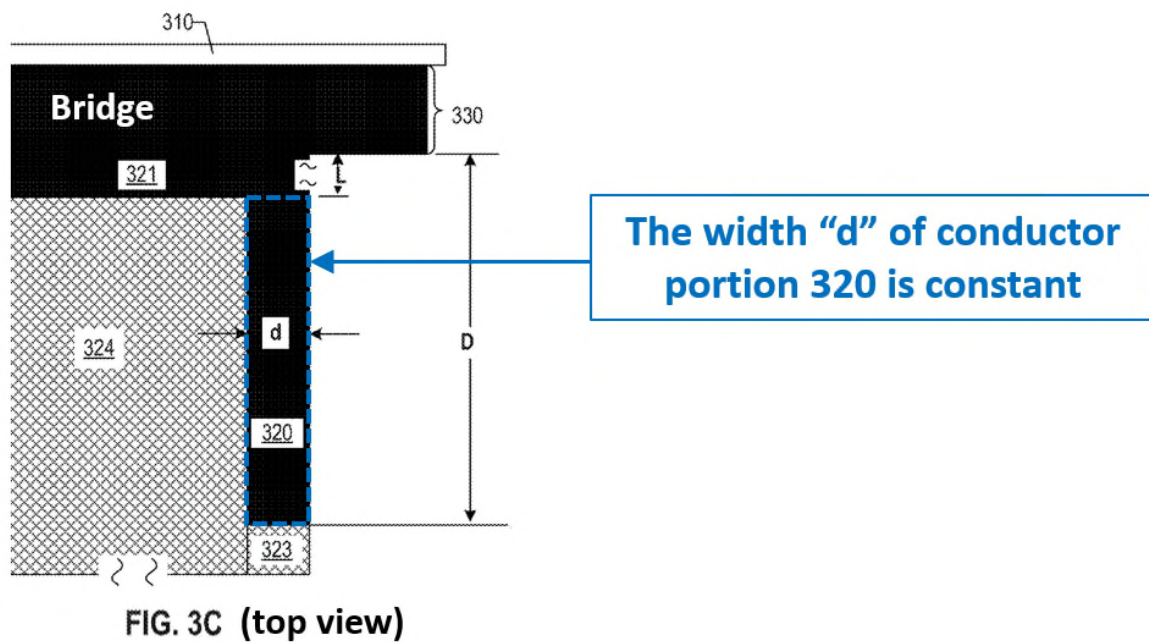


Ex. 1007, Fig. 1B (annotated).

9. [1.H] “along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.”

140. The term *second lateral direction perpendicular to the lateral direction* includes the y-direction, because “the lateral direction” is the x-direction. Ex. 1001, 1:58-60; *see also id.*, 2:4-6 (same), 2:16-18 (same), 18:44-46 (same), 18:55-58 (same), 19:28-30 (same), 19:41-44 (same), 20:15-17 (same), and 20:26-29 (same). Thus, this limitation requires that the width of the *conductor portion* in the x-direction remains unchanged as the conductor portion extends in the y-direction toward the bridge. *Id.*; *see also id.*, 11:19-24 (“along the x-direction, a width d of

conductor portion 320 may be equal to or less than the dimension of stair 314. In some embodiments, width d of conductor portion 320 is equal to the dimension of stair 314 along the x-direction and is nominally unchanged along the y-direction.”). In other words, the finger is the same width travelling to bridge, as shown below:



Id., Fig. 3C (annotated); *see also id.*, 13:10-14 (“th[e] width d of conductor portion 320 may be unchanged along the y-direction.”).

141. Lee Fig. 1B discloses the width of the conductive finger (labelled “W”) as constant until it reaches the “connection region U_13B.” Ex. 1007, [0030]-[0031]. In Lee, the connection region connects to the wordlines as shown in Fig. 1C. *Id.*, [0006]. By analogy, connection region U_13B acts as a bridge of sorts to the array, and the finger travels to that region.

FIG. 1B

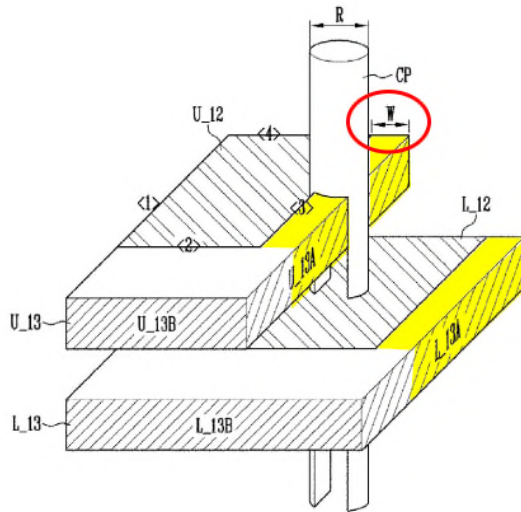
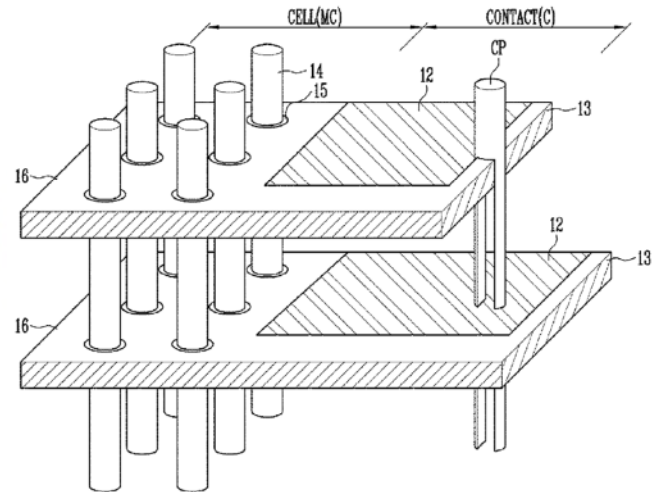


FIG. 1C

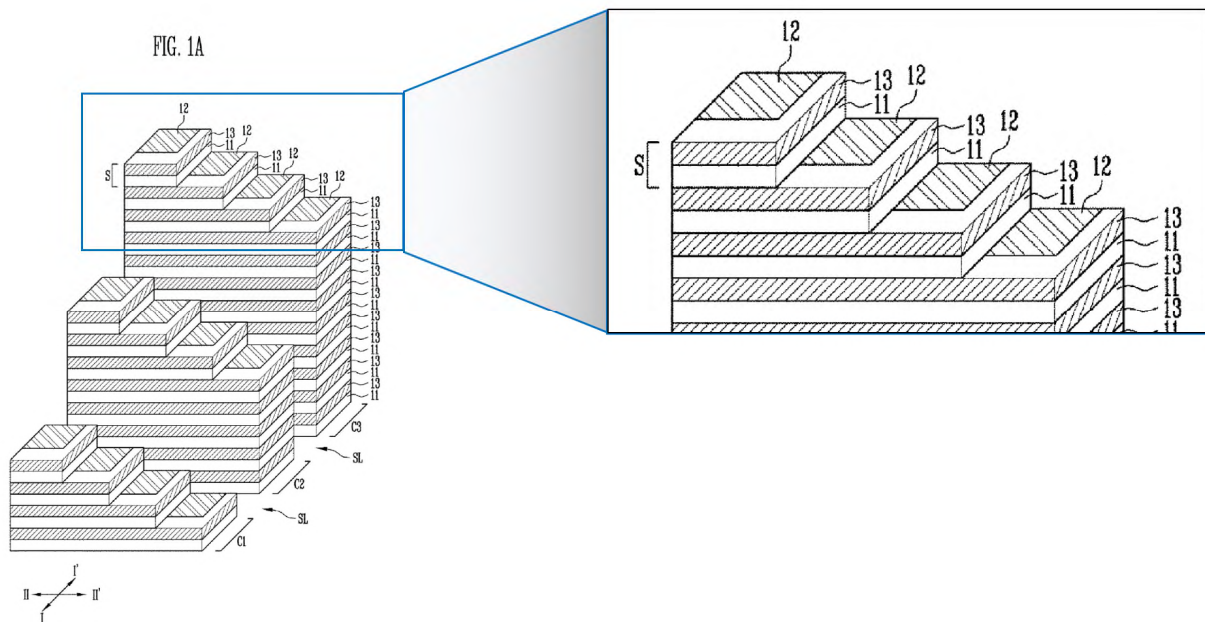


Id., Fig. 1B (annotated) and Fig. 1C.

142. Thimmegowda, in view of Lee, renders obvious claim element 1[h]. In particular, in the modified version of Thimmegowda in view of Lee's teachings, the conductor portion maintains the same width (in the x-direction) as it proceeds in the y-direction to connect to wordline bridge 306 (the *bridge*). In other words, the constant width finger, shown in yellow above, flows into the Thimmegowda bridge just it flows into, e.g., U_13B above. Regardless of whether the width of the conductor portion is narrow (as shown in Lee Fig. 1B) or covers the entire surface area of the step, it would flow into the bridge so that it electrically couples to bridge and bidirectionally drive both arrays.

C. Claim 2 “The 3D memory device of claim 1, wherein the stair further comprises: a dielectric layer under the conductor portion and the dielectric portion.”

143. As I describe below, Thimmegowda in view of Lee’s teachings of a conductive finger on the stair steps satisfies claim 2. As shown below in Lee Fig. 1A, each step “S” has an insulating layer 11 (*a dielectric layer*) beneath a conductive finger 13 (*the conductor portion*) and a dielectric 12 (*the dielectric portion*). See Ex. 1007, [0022]. As I describe when I summarize Lee, that pairing of the dielectric portion 12 and conductive finger 13 solves the punch through problem. Imagine a staircase contact landing on the top conductive landing spot 13, and one sees that underneath that top landing spot, is dielectric pair 12 and 11. Yet the finger enables that staircase contact to still couple to the memory arrays.

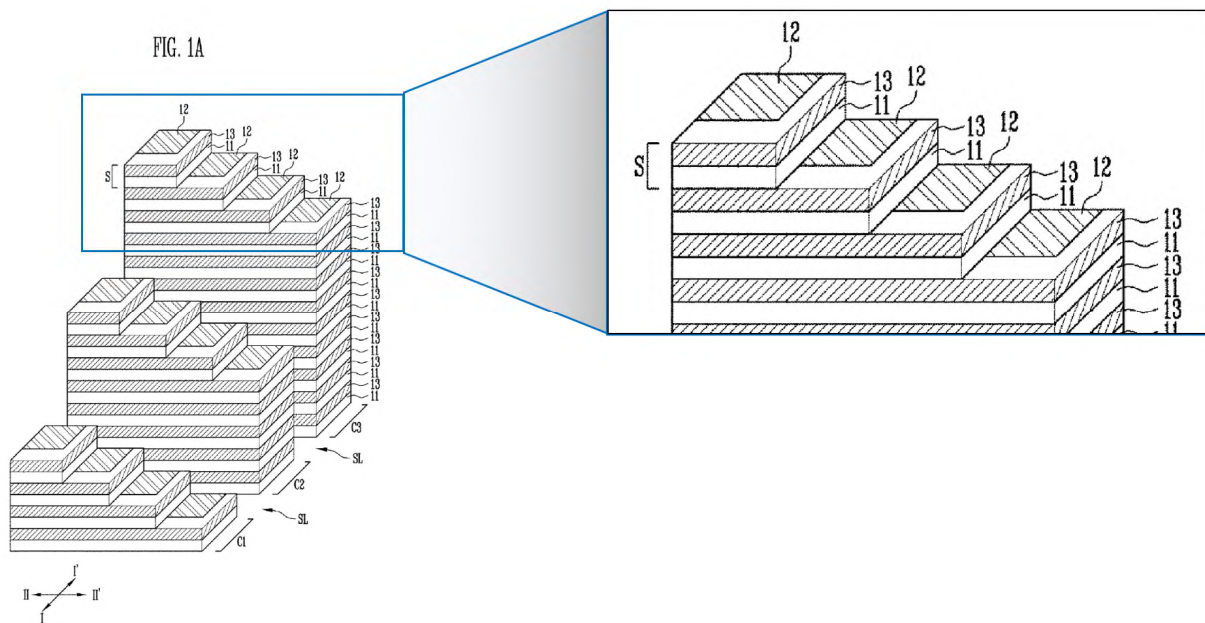


Id., Fig. 1A. Applying these teaching to Thimmegowda, each step has a **dielectric layer** (e.g., dielectric 310a-d and 320a-d) under the **conductor portion** (the conductive finger on steps 332a-d) and **the dielectric portion** (the remaining sacrificial material on steps 332a-d). Again, this solves the punch through problem that Thimmegowda's staircase and bridge structure would otherwise have.

D. Claim 3 “The 3D memory device of claim 2, wherein the conductor portion and the dielectric layer are each above the one or more dielectric pairs.”

144. As my analysis for elements 1[e] and [2], Thimmegowda in view of Lee's teachings satisfies claim 3. Specifically, as shown below in Lee Fig. 1A, each step “S” has a conductive finger 13 (**the conductor portion**) and dielectric layer 11 (**the dielectric layer**) that are **above the one or more dielectric pairs** (i.e., the combination of dielectric 12 and insulating layer 11 in the underlying step(s)). See

Ex. 1007, [0022]. As I explain for claim 2, this is the key Lee teaching that solves the punch through problem, because these dielectric pairs sit under a conductive landing spot (finger) in stair level above.



Id., Fig. 1A.

145. When applying these teachings to Thimmegowda, *the conductor portion* (the conductive finger on steps 332a-d) *and the dielectric layer* (dielectric layers 310a-c and 320a-c) *are each above the one or more dielectric pairs* (viz., the combination of the remaining sacrificial material on steps 332b-d and their respective insulating layer 310b-d/320b-d in the underlying step(s)). This simply modifies the staircases to include these dielectric pairs and conductive fingers to mitigate the punch through problem.

E. Claim 4 “The 3D memory device of claim 2, wherein along the lateral direction, a width of the conductor portion is equal to a dimension of the stair.”

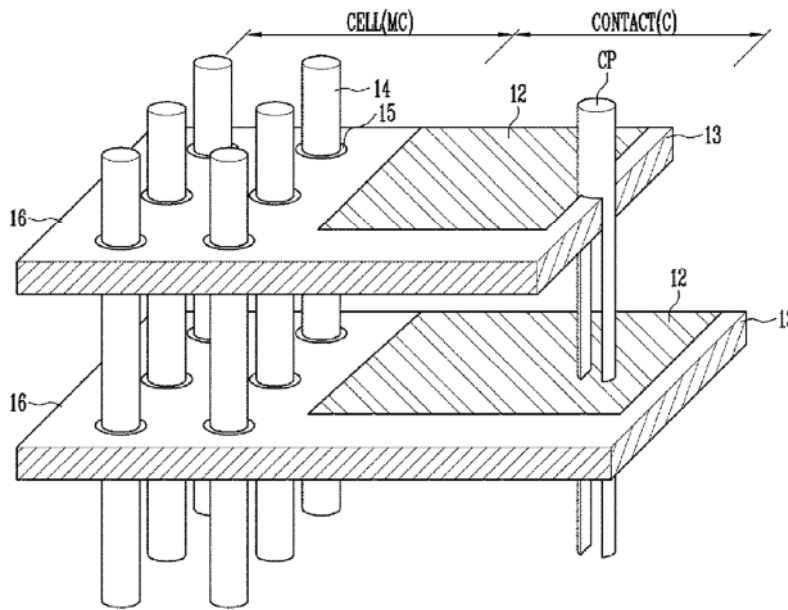
146. Thimmegowda in view of Lee’s teachings satisfies claim 4. In one obvious modification of Thimmegowda’s staircase and bridge architecture, as I explain for element [1.F], fingers extend into the bridge. It would have been obvious for the width of the conductive finger in the x-direction to be co-extensive with the exposed surface area of the step, and thus the *width of the conductor portion* in the x-direction (viz., *the lateral direction*) *is equal to a dimension of the stair* (viz., the width of the step in the x-direction) as I describe in Section XII.A.

F. Claim 5 “The 3D memory device of claim 1, wherein along the second lateral direction perpendicular to the lateral direction, a length of the conductor portion is equal to or less than a second dimension of the stair.”

147. The *second lateral direction* is the y-direction in the ’604 patent (see claim element 1[h]). Thus, the *second dimension of the stair* refers to the length of the step in the y-direction toward the bridge. As my analysis for claim [1.F] demonstrates, Thimmegowda in view of Lee renders obvious that the conductive finger extends the full length of the step (in the y-direction toward wordline bridge 306), and is thus *equal to ... a second dimension of the stair* (i.e., the length of the step in the y-direction).

148. Moreover, Lee Fig. 1C illustrates that the length of the protruding “finger” (*viz.*, conducting layer 13) extends the full length of the step (*i.e.*, to the point where it reaches the wordline bridge running horizontally in the x-direction toward the memory array). Note that the conductive portion towards the screen is the connection region to the cell area.

FIG. 1C



Ex. 1007, Fig. 1C.

149. Further, as I demonstrate for claim 4, it would have been obvious for the conductor portion to extend the less than the full length in the Y-direction as the stair steps go from top to bottom.

G. Claim 8

1. **[8.A] “The 3D memory device of claim 1, wherein: the conductor portion comprises at least one of tungsten, cobalt, copper, aluminum, silicides, or polysilicon;”**

150. Lee discloses tungsten conductive portions that Lee deposits versus the well-known gate replacement process. Ex. 1007, [0023], [0044]. It would have been obvious to use tungsten gates via a gate replacement process in the Thimmegowda in view of the Lee combination. It was well known when using gate replacement processes to use conductive materials such as “tungsten (W).” Ex. 1017 (U.S. Pat. Pub. No. 2017/0256551), [0049]. I discuss in the motivation section the many benefits of tungsten gates.

2. **[8.B] “the dielectric portion comprises silicon nitride; and”**

151. As I discuss above for claim [8.A], the Thimmegowda in view of Lee combination renders obvious using Lee’s gate replacement process. The *dielectric portion* in modified Thimmegowda was discussed in connection with claim element 1[g]. It was well known that a common sacrificial material used as part of a gate replacement process was silicon nitride. See Ex. 1018, 132 (“Multiple layers of oxide and *sacrificial nitride layers* are initially deposited.”) (emphasis added); Ex. 1019, [0050] (“[T]he additional insulating structures 106 are formed of and include silicon nitride (Si₃N₄).”).

152. Lee would have been understood to disclose, and certainly renders obvious, sacrificial silicon nitride layers, which remains in after the gate replacement process. *See* Ex. 1007, [0048]-[0055]. Lee discloses that “first openings OP1 may be formed by partially removing the sacrificial layers 42 exposed on a sidewall of the stacked structure ST. For example, the sacrificial layers 42 may be removed by 400 to 600 Å. Since the sacrificial layers 42 are removed along the sidewall patterned stepwise, the sacrificial layers 42 may be removed in an L shape on the respective layers.” *Id.*, [0048]. Subsequently, “conductive layers 46 are formed” in the openings and “have substantially an L shape.” *Id.*, [0055]. And Lee expressly discloses that “the sacrificial layers 42 which are not removed” remain in place as part of the overall interconnection structure. *Id.*

153. Lee further discloses that “[t]he sacrificial layers 42 may include materials having a high etch selectivity with respect to the insulating layers 41. For example, the sacrificial layers 42 may ***include a nitride.***” Ex. 1007, [0044] (emphasis added); *see also id.*, [0023] (“[T]he dielectric layers 12 [which also map to the claimed ***dielectric portion***] may be formed of the remaining portions of sacrificial layers used in the manufacturing process, and include a nitride.”). Lee’s express disclosure of a dielectric portion that includes a nitride further renders obvious the use of a ***dielectric portion compris[ing] silicon nitride***, as such a material was well known and commonly used as an insulator in semiconductor chips and 3D

NAND memory devices. *See, e.g.*, Ex. 1011, 2:58-59 (“The insulating layer 42 is a layer primarily including silicon nitride.”), Ex. 1006, [0093] (same).

3. [8.C] “a dielectric layer is arranged under the conductor portion and the dielectric portion, the dielectric layer comprising silicon oxide.”

154. The modified version of Thimmegowda renders obvious claim element 8[c]. The only part of element 8[c] that is different than claim 2 is that *the dielectric layer comprising silicon oxide*.

155. The claimed *dielectric layer* in Thimmegowda (modified or unmodified) is the insulating layer 310a-d/320a-d. That is, the dielectric layer of the memory stack. Ex. 1005, 9:49-50 (“The wordline bridge 306 includes the same layers as the wordline stacks 312, 322”), 8:34-38 (“The memory cell block of a first tile 302 includes a wordline 308 a, a dielectric 310a, a wordline 308b, a dielectric 310b, a wordline 308c, a dielectric 310c, a wordline 308d, a dielectric 310d (collectively, a wordline stack 312).”), 8:57-60. And Thimmegowda discloses that “[t]he dielectrics 310 are oxide layers, according to one embodiment. The **dielectrics 310 are silicon dioxide layers**, according to one embodiment. ... The dielectrics 320 are oxide layers, according to one embodiment. The **dielectrics 320 are silicon dioxide layers**, according to one embodiment.” *Id.*, 8:44-9:6. Silicon oxide was the typical dielectric layer for the memory stack.

H. Claim 9

156. Claim 9 is similar to, and broader than, claim 1 in a number of respects, and obvious for the same reasons that I provide for claim 1.

1. [9.PRE] “A three-dimensional (3D) memory device, comprising:”

157. If limiting, the preamble of claim 9 is satisfied for the same reasons as the claim 1 preamble.

2. [9.A] “a memory array structure; and”

158. Claim element 9[a] is met for the same reasons as claim element 1[a].

3. [9.B] “a staircase structure comprising a plurality of stairs extending along a lateral direction,”

159. Claim elements 1[b] and 1[c] collectively require everything recited by claim element 9[b]. Accordingly claim element 9[b] is satisfied for the same reasons as claim elements 1[b] and 1[c].

1. [9.C] “a stair comprising a conductor portion on a top surface of the stair and a dielectric portion at a same level and in contact with the conductor portion, the conductor portion being electrically connected to the memory array structure,”

160. Claim elements 1[f] and 1[g] collectively require everything recited by claim element 9[c], except that element 9[c] requires the *conductor portion* (instead of just *the stair*) be *electrically connected to the memory array structure*. But, as explained in connection with element 1[g], in the modified version of Thimmegowda

it is the **conductor portion** of the stair (not the dielectric or insulator portion of the stair) that electrically connects the stair to the memory array. Accordingly, modified Thimmegowda satisfies claim element 9[c] for the same reasons explained in connection with elements 1[f] and 1[g]. A comparison of element 9[c] with elements 1[f] and 1[g] is provided in the table below, with corresponding elements shown in the same colors.

Element 9[c]	Elements 1[f] and [g]
a stair comprising a conductor portion on a top surface of the stair and	the stair comprises a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure, and
a dielectric portion at a same level and in contact with the conductor portion,	a dielectric portion at a same level and in contact with the conductor portion,
the conductor portion being electrically connected to the memory array structure	the stair being electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure; and

2. [9.D] “wherein along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.”

161. Claim element 9[d] is the same as element 1[h] and is satisfied for the same reasons.

- I. Claim 10: “The 3D memory device of claim 9, wherein the staircase structure further comprises a dielectric layer under the conductor portion and the dielectric portion.”**

162. Claim 10 adds the same limitation as claim 2 and is met for the same reasons.

- J. Claim 11: “The 3D memory device of claim 10, wherein: the conductor portion and the dielectric layer are each above one or more dielectric pairs.”**

163. Claim 11 adds the same limitation as claim 3 and is met for the same reasons.

- K. Claim 12: “The 3D memory device of claim 9, wherein along the lateral direction, a width of the conductor portion is equal to a dimension of the stair.”**

164. Claim 12 adds the same limitation as claim 4 and is met for the same reasons.

- L. Claim 13: “The 3D memory device of claim 9, wherein along the second lateral direction perpendicular to the lateral direction, a length of the conductor portion is equal to or less than a second dimension of the stair.”**

165. Claim 13 adds the same limitation as claim 5 and is met for the same reasons.

XIII. GROUND 2: THIMMEGOWDA IN VIEW OF KOBAYASHI AND THE KNOWLEDGE OF A POSITA

A. Motivation to Combine

166. A POSITA would have been motivated to combine the teachings of Thimmegowda with Kobayashi with a reasonable expectation of success for several reason.

167. My analysis focuses on the combination of Thimmegowda's bridge and array architecture and Kobayashi's stairstep teachings that mitigate punch through.

168. A POSITA would have been motivated to apply Kobayashi's teaching of non-overlapping conductive fingers to mitigate the well-known punch through problem in Thimmegowda's staircase. I explain the punch through problem in detail in Section XII.A. Again, a POSITA would look to known solutions. As I describe in Section XI.C, Kobayashi provides such a solution. Kobayashi's finger teachings are applicable to a staircase, and that is precisely what Thimmegowda relies on for connections to the gate layers. Kobayashi discloses forming multiple "columns" of staircases (labeled columns 91-94), and each of the columns employ Kobayashi's finger approach. That finger approach is applicable to the steps whether they are in a single column or multiple columns. That is because the purpose is creating dielectric pairs under respective staircase contact landing areas. That approach applies equally to one or more columns.

169. I note that two implementations of Kobayashi's finger approach would have been obvious to apply to Thimmegowda. First, it would have been obvious to a POSITA to use a "thin" finger narrower (in the x-direction) than the width of a step, because Kobayashi expressly discloses that narrow finger approach. Ex. 1006, Fig. 5, [0069] ("first conductive portion 70b").

170. Second, it would also have been obvious to make the conductive finger cover the full width of the step. Thimmegowda, for example, includes landing pads like this. Using such wider fingers was also a known solution to punch through. Nakaki, for example at Fig. 55 below, discloses non-overlapping conductive fingers that cover the full exposed surface area of each stairstep. Ex. 1011 (U.S. Pat. No. 9,029,938), 14:64-65 ("the end parts 141 of the aforementioned staircase structure section 140 are provided as contact parts"), 15:10-11 ("The contact parts 141 do not overlap each other in the Z-direction."). I discuss this approach in greater detail in Section XII.A.

171. Kobayashi discloses using the well-known gate-replacement process, and the remaining portions of the sacrificial gates form the dielectric portions on the same level of fingers. See Section XI.C. The gate replacement process more generally provides another strong motivation to include Kobayashi's teachings. In short, the gate replacement process enables metal gate layers (wordlines), typically tungsten, instead of, typically, polysilicon gate layers. A major advantage of

tungsten gate layers is lowering the resistance or capacitance load when driving a wordlines (corresponding to a conductive gate layer in the stack). This enables, for example, faster read and write operations. This was textbook material before the '604 patent's priority date. See Ex. 1018, 131-32. As I describe for Lee, Thimmegowda's bridge teachings would likewise be beneficial for Kobayashi.

172. A POSITA would have had a reasonable expectation of success in combining the teachings of Thimmegowda's bridge and array architecture (to bidirectionally drive two memory arrays with one wordline via) with Kobayashi's staircase finger approach (to mitigate punch through). A key building block of a 3D NAND is the memory stack. Portions of that memory stack become the staircase and the bridge. The stack is simply alternating layers of conductive gate layers and dielectric layers. That Thimmegowda forms the stack without gate replacement is irrelevant to its bridge teachings. Specifically, whether that bridge is made with or without gate replacement, it performs the same exact function. Indeed, when viewing simply the Thimmegowda figures, one would not be able to tell whether that structure was made with gate replacement. As I describe above, the gate replacement process was textbook material. And as to the Kobayashi's fingers specifically, Kobayashi details that process. See Ex. 1006, Figs. 7-33B (and accompanying discussion at [0087]-[0144]). Thus, a POSITA would have had a

reasonable expectation of success in combining the above teachings from Thimmegowda and Lee.

B. Claim 1:

173. As I explain below, Thimmegowda in view of Kobayashi renders claim 1 obvious.

1. Claim 1 Preamble and Elements 1[a]-[d].

174. I demonstrate that Thimmegowda discloses the preamble and elements 1[a]-1[d] in Ground 1.

2. [1.E] “the plurality of stairs comprising a stair above one or more dielectric pairs,”

175. As I explain in Ground 1, at least one example of a *dielectric pair* within the meaning of the claims is a sacrificial layer and its corresponding dielectric layer.

176. Thimmegowda in view of Kobayashi renders this limitation obvious. Recall that Thimmegowda discloses “steps 332” that form part of the staircase. Ex. 1005, Fig. 3.

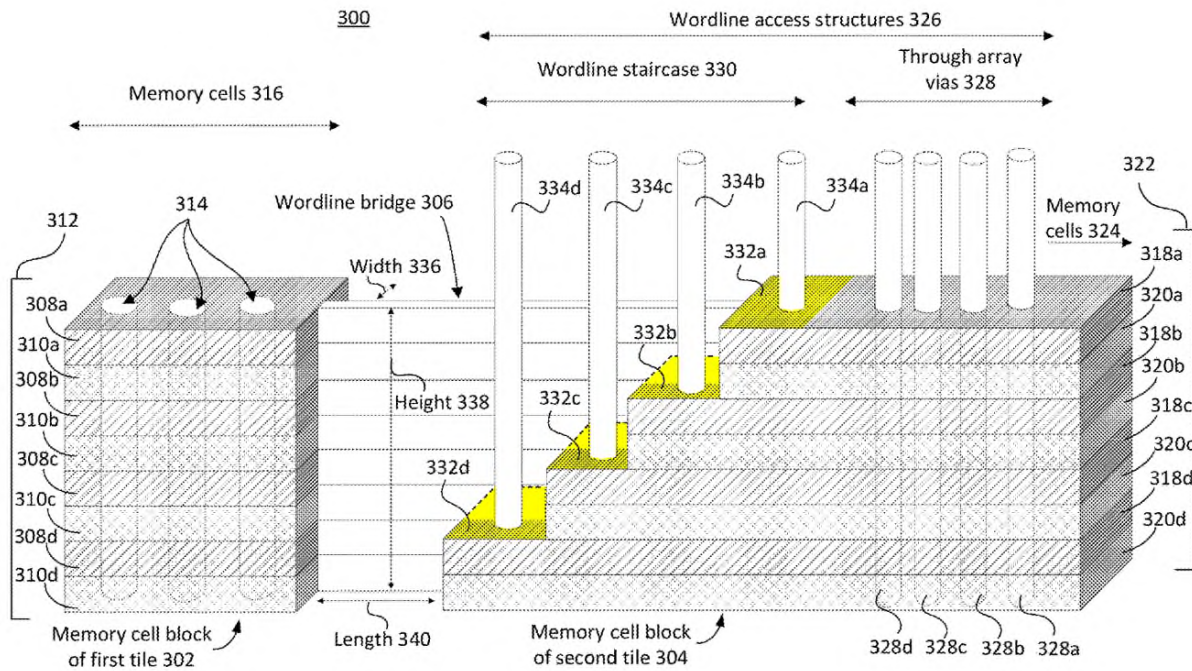


FIG. 3

Ex. 1005, Fig. 3 (annotated); *see also id.*, 9:27-38. Thimmegowda discloses that layers 310a-d and 320a-d are dielectric layers. *Id.*, 8:34-38, 8:4-50, 8:57-61, 8:67-9:6. These dielectric layers extend horizontally to form corresponding dielectric layers in the wordline staircase 330 and wordline bridge 306. That is, these are the typical oxide layers of a 3D memory stack. Thus, for example, layers 310d (and corresponding layer 320d) form one layer of the claimed *dielectric pair*. *Id.* The same is true for the oxide layers, e.g., layers 310c/320c and 310b/310b.

177. As the motivation section explains, it would have been obvious to apply Kobayashi's "finger" approach to Thimmegowda's staircase/bridge architecture, which provides the other layer of the *dielectric pair*. Kobayashi's Fig. 3 (and Fig.

sacrificial spacer portion 71 and insulator 72 forms a *dielectric pair*.



or more dielectric pairs. *Id.* With this arrangement, under a staircase landing pad,

nitride layers and are insulating bodies, the contact CC is not shorted to the first conductive portions 70 b of the other layers even when the contact CC reaches the spacer portions 71 of the other layers lower than the first conductive portion 70 b to be connected.” *Id.*, [0141].

178. Applying Kobayashi’s finger approach to Thimmegowda results in a staircase structure that maintains *a stair above one or more dielectric pairs*, where the *dielectric pair*⁴ comprises a dielectric layer 310/320 in combination with the spacer 71 (*i.e.*, remaining sacrificial dielectric) from Kobayashi. Thus, in the modified version of Thimmegowda’s bridge and staircase structure, each stair (except for the bottom stair) is *a stair above one or more dielectric pairs*.

⁴ The ’604 patent discloses that “all the dielectric portions 324 and dielectric layers 326 underlying conductor portion 320 may be referred to as a dielectric structure 340, of which a thickness along the z-direction is equal to the distance between the bottom surface of the respective conductor portion 320 and the top surface of substrate 302.” Ex. 1001, 12:8-13.

3. [1.F] “wherein: the stair comprises a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure, and”

179. Recall that one example of a conductor portion is a conductive finger that is less than or equal to the depth (in the z-direction) of the sacrificial layer. Again, the finger physically and electrically connects to bridge, thereby bidirectionally driving the two arrays.

180. Recall that Thimmegowda discloses a *stair compris[ing] a conductor portion on a top surface of the stair and in contact with and electrically connected to the bridge structure*. As shown below, the highlighted, top/exposed surface of steps 332a-d are the *conductor portions* and connect to respective conductive metal layers in wordline bridge 306. Thus, the staircase contact lands on a step and is able to bidirectionally drive both arrays.

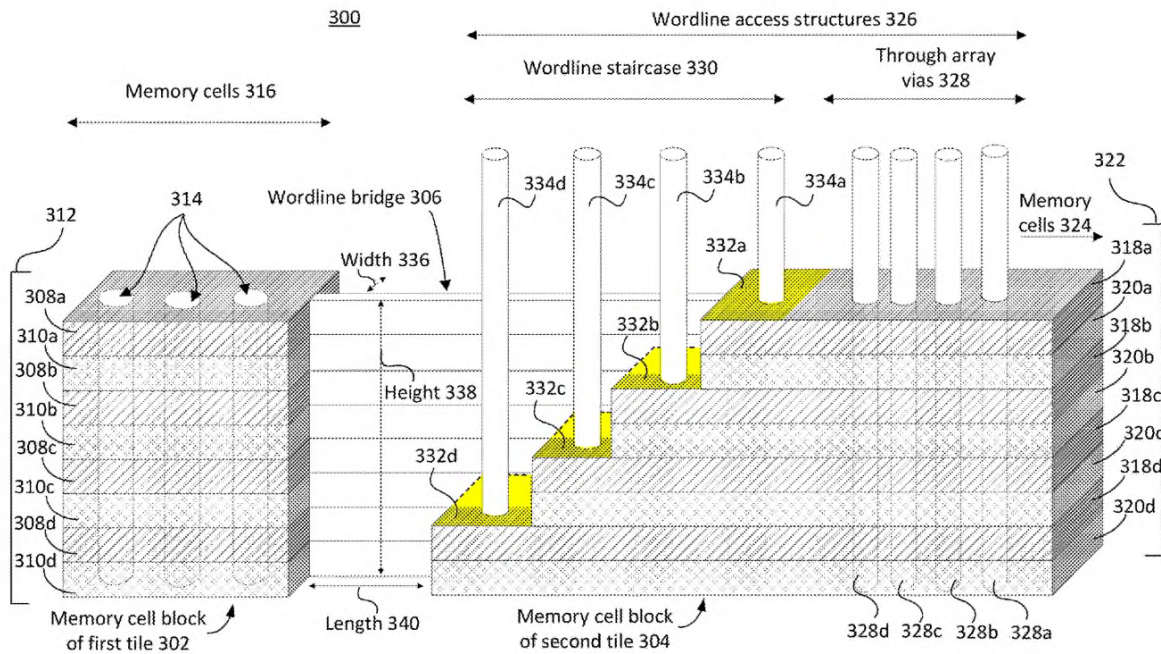


FIG. 3

Ex. 1005, Fig. 3 (annotated); *see also id.*, 9:27-49.

181. Thimmegowda in view of Kobayashi’s “finger” teachings also satisfies element 1[f]. In particular, in the modified version of Thimmegowda, the landing pads are in direct contact with the bridge, as taught by Kobayashi’s finger-like “first conductive portion 70b” that is in physical and electrical contact with the “second conductive portion 70c” (analogous to Thimmegowda’s bridge) for connecting to the wordlines in the memory array as shown in Figs. 1 and 5. Ex. 1006, [0069]-[0074] (“The conductive layer 70a [*i.e.*, the wordline], the first conductive portion 70b, and the second conductive portion 70c are provided to be continuous as one body of the same material [, such as] a metal layer including mainly tungsten.”).

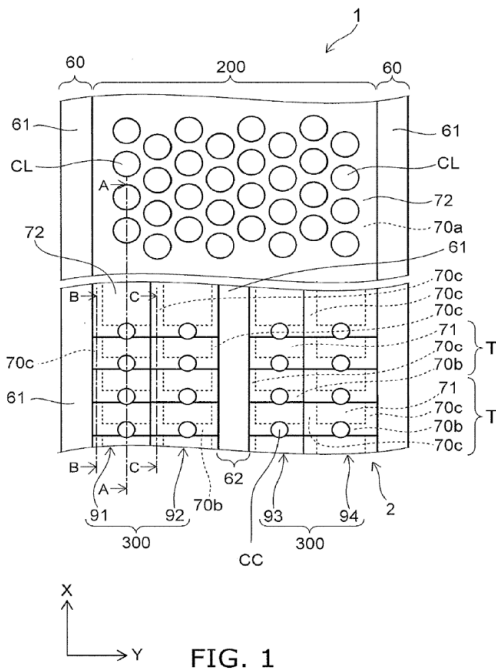


FIG. 1

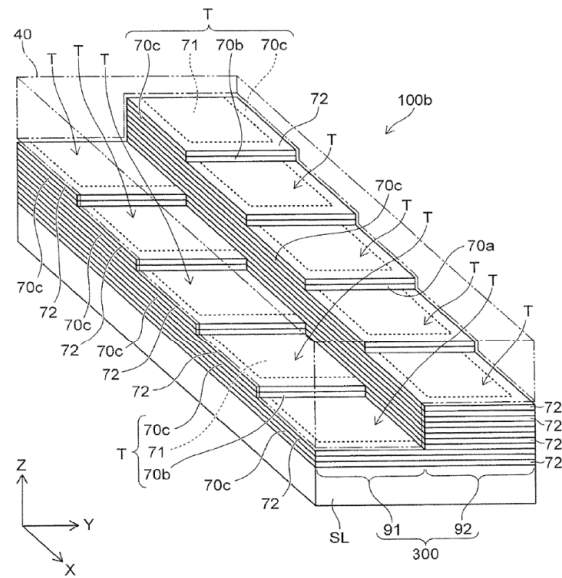


FIG. 5

Ex. 1006, Figs. 1 and 5.

182. Regardless of whether the conductor portion in the modified version of Thimmegowda covers the entire surface (as Thimmegowda itself discloses) or is modified to a narrower profile akin to that shown above in Kobayashi (both of which are obvious), Thimmegowda in view of Kobayashi satisfies claim element 1[f]. Again, a major benefit of Kobayashi is that it mitigates the punch through problem. Applying its teachings to Thimmegowda has this benefit. Note that Kobayashi's top stair portion is the oxide layer of the stack, whereas the bottom comprises the conductor and dielectric portions. Kobayashi, Fig. 3, [0029]. In other words, when first forming the staircase, each step includes a top oxide layer and bottom sacrificial gate layer (silicon nitride). Kobayashi then forms the finger in the

bottom portion, such the bottom portion includes the conductor portion (e.g., tungsten) and the dielectric portion (the remaining silicon nitride). However, it was well known that when forming a staircase, two interchangeable options for each step were: (1) the top portion is the sacrificial gate layer and bottom portion is the oxide layer and (2) the top portion is the oxide layer and the bottom portion is the sacrificial gate layer. *E.g.*, Ex. 1029, (U.S. Pat. Pub. No. 20120070944), [0090] (“each of top surfaces of the insulating layers . . . constituting the stepwise stacked layer . . . may be partially exposed in the word line contact region WCTR. In other embodiments, each of top surfaces of the sacrificial layers . . ., not the top surfaces of the insulating layers . . ., may be partially exposed”), [0091] (same), [0240] (similar); Ex. 1030 (U.S. Pat. No. 10,026,692), Figs. 7A, 7B (showing each alternative). It was also known how to create the finger with the conductive layer on top, and I detail this with respect to Lee. See § VI.B. Each alternative is design choice among two options, and both provide the beneficial staircase and finger structure. The only difference is a minor change in the manufacturing process for the staircase and finger. The above references and Lee demonstrate that it was well within a POSITA’s knowledge how to form the staircase and finger with the conductor portion on top, and a POSITA would have a reasonable expectation of success in forming Kobayashi’s conductive finger portion and remaining sacrificial gate layer on the top of the stairstep.

4. [1.G] “wherein: the stair comprises ... a dielectric portion at a same level and in contact with the conductor portion, the stair being electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure; and”

183. As I discuss for claim element 1[f], Thimmegowda discloses that the stair is *electrically connected to at least one of the first memory array structure or the second memory array structure through the bridge structure*. See, e.g., Ex. 1005, 12:50-13:2, 9:27-48. This allows the staircase contacts to bidirectionally drive the memory arrays on both the left and right sides of the staircase structure. *Id.*, 7:61-64. The Thimmegowda in view of Kobayashi ground includes this feature.

184. The same obvious modification to Thimmegowda staircase and bridge architecture, as I describe in [1.F], renders the remaining portion of the claim obvious.

185. In Thimmegowda alone, and in view of Kobayashi’s teachings, the *conductor portion* extends in the z-direction substantially the full depth of the conductive wordline layers 308a-d and 318a-d. See Ex. 1005, Fig. 3, 9:49-51 (“The wordline bridge 306 includes the same layers as the wordline stacks 312, 322”); Ex. 1006, Fig. 3 (conductor 70b). And as I explain in claim [1.F], Thimmegowda in view Kobayashi renders obvious the resulting conductors on staircase steps 332a-d to be approximately the width of the step (as shown in Thimmegowda Fig. 3) or narrower (as shown in Kobayashi Fig. 3 and Fig. 5) and extend laterally in the y-

direction to directly contact the wordline bridge 306. This is similar to how Kobayashi's conductive fingers (*viz.*, first conductive portions 70b) are in physical and electrical contact with the wordlines. *See* Ex. 1006, Fig. 1, Fig. 3, [0073]-[0074]. Applying Kobayashi's teaching to Thimmegowda results in the finger extending into Thimmegowda's bridge to bidirectionally drive the two arrays.

186. Further, in view Kobayashi's teaching, in Thimmegowda's staircase structure, the area immediately adjacent to the finger (in the x-direction toward the righthand memory array) is an insulator (*viz.*, *dielectric portion*), similar to Kobayashi's "spacer 71" illustrated in Figs. 1, 3, and 5. Ex. 1006, [0069]-[0072], [0079]-[0082]. This enables mitigating the punch through problem, as Kobayashi teaches, while driving both arrays (as taught by Thimmegowda). Thus, there is *a dielectric portion* [spacer portion 71 highlighted in orange] *at a same level and in contact with the conductor portion* [first conductive portion 70b, highlighted in yellow]. Applying this to Thimmegowda, the dielectric material that is left after replacing portions of the sacrificial layer with a conductor is *at a same level and in contact with the conductor portion* [the finger]. *Id.* This is true regardless of whether the *conductor portion* (*i.e.*, the finger) in modified Thimmegowda is the full width of the exposed landing pad area of a step or a narrower conductive strip (as in Lee).

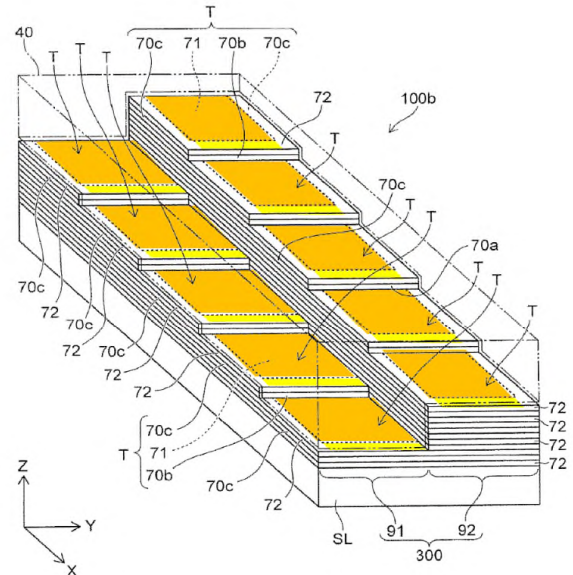
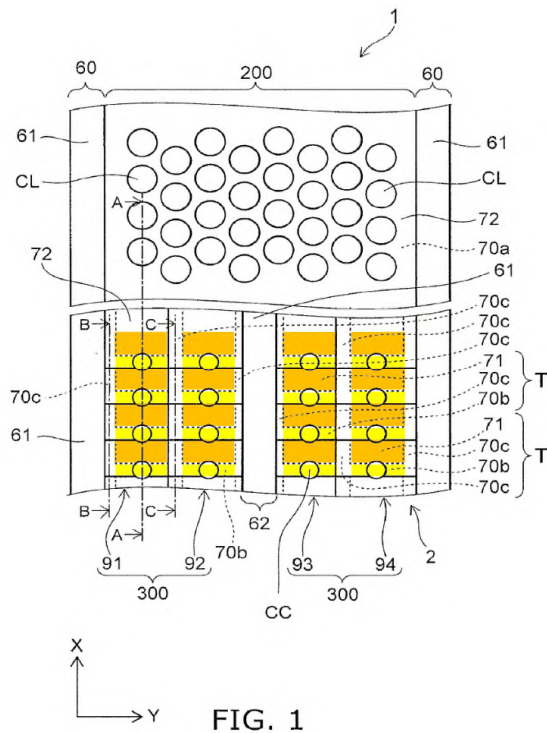
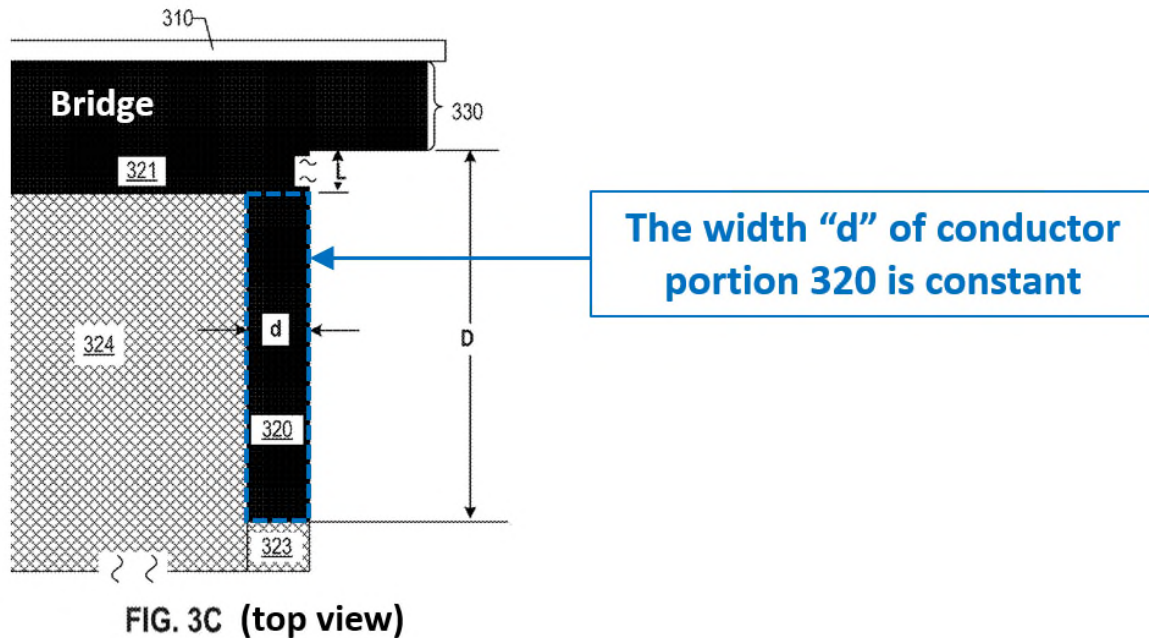


FIG. 5

Ex. 1006, Figs. 1 and 5 (annotated).

5. [1.H] “along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.”

187. Recall that the claimed *second lateral direction perpendicular to the lateral direction* at least includes the y-direction. As shown below, claim element 1[h] requires that the width of the *conductor portion* in the x-direction remains unchanged as the conductor portion extends in the y-direction toward the bridge:

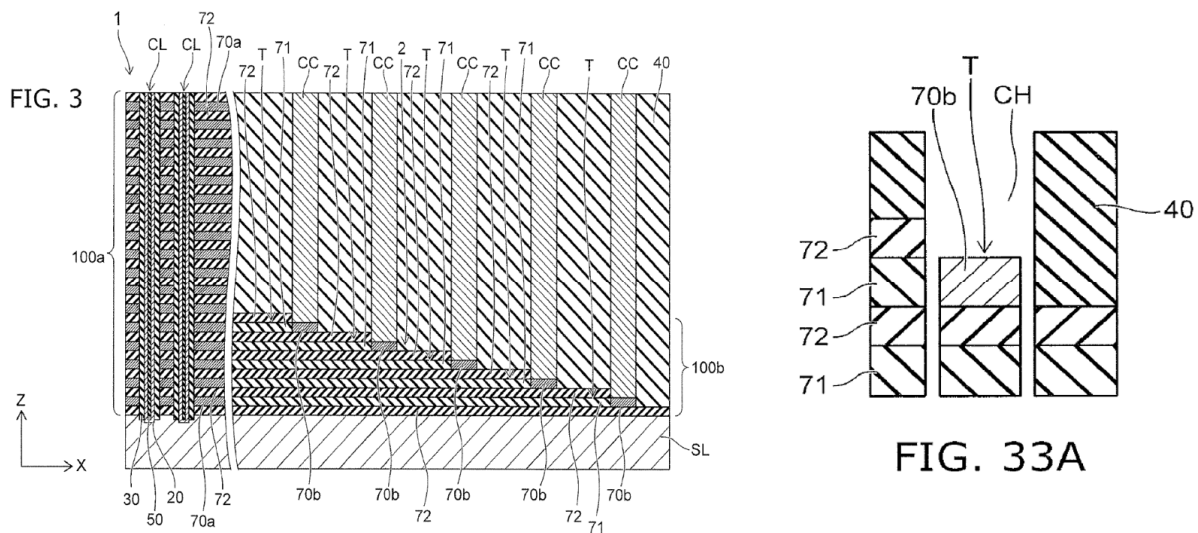


Ex. 1001, Fig. 3C (annotated).

188. As shown in Kobayashi's Figs. 1 and 5 below, the width of first conductive portion 70b remains unchanged until it connects with the second conductive portion 70c. Ex. 1006, [0069]-[0074]. In Kobayashi, the second conductive portion 70c connects to the wordlines. *Id.*, [0074]. Kobayashi's second conductive portion 70c is analogous to Thimmegowda's wordline bridge 306 (the *bridge*), because it provides the conductive path from the finger (which connects to the staircase contact landing pad) to gate layer of the memory stack.

C. Claim 2 “The 3D memory device of claim 1, wherein the stair further comprises: a dielectric layer under the conductor portion and the dielectric portion.”

190. Thimmegowda in view of Kobayashi’s teachings of a conductive finger on the stair steps satisfies claim 2. As shown below in Kobayashi’s Fig. 3 (and Fig. 33A), each step (except the bottom step) has *a dielectric layer* (insulating layer 72) under *the conductor portion* (first conductive portion 70b) and *the dielectric portion* (spacer 71). See Ex. 1006, [0139]-[0143]. This is because for a step with a landing pad, part of that step in the X direction is the conductive portion and part is the dielectric portion. Under those portions is the dielectric layer (silicon oxide).



Ex. 1006, Fig. 3, Fig. 33A. When applying these teachings to Thimmegowda, each step has a *dielectric layer* (e.g., dielectric 310a-d and 320a-d) under the *conductor portion* (the conductive finger on steps 332a-d, akin to Kobayashi’s first conductive

portion 70b) and *the dielectric portion* (the remaining sacrificial material on steps 332a-d, akin to Kobayashi's spacer 71). I discuss how this mitigates punch through problem through this declaration, but again, this arrangement provides for a plurality of dielectric layers to be under a staircase contact landing pad.

D. Claim 3 “The 3D memory device of claim 2, wherein the conductor portion and the dielectric layer are each above the one or more dielectric pairs.”

191. Thimmegowda in view of Kobayashi renders this limitation obvious for the reasons that I explain in claim element 1[E]. Kobayashi Figs. 1 and 33 demonstrate that each step (except the bottom step) has a conductive portion 70b (*the conductor portion*) and insulating layer 72 (*the dielectric layer*) that are *above the one or more dielectric pairs* (i.e., the combination of spacer 71 and insulating layer 72 in the underlying step(s)). See Ex. 1006, [0138]-[0142]. Thus, when viewing Figure 3, for example, there are dielectric pairs under each staircase contact (except the right most).

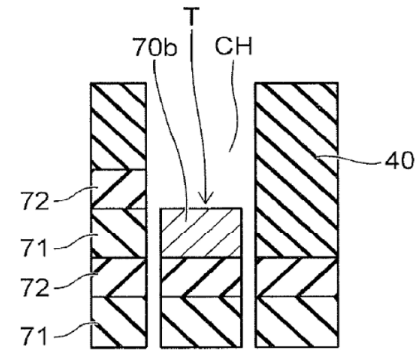
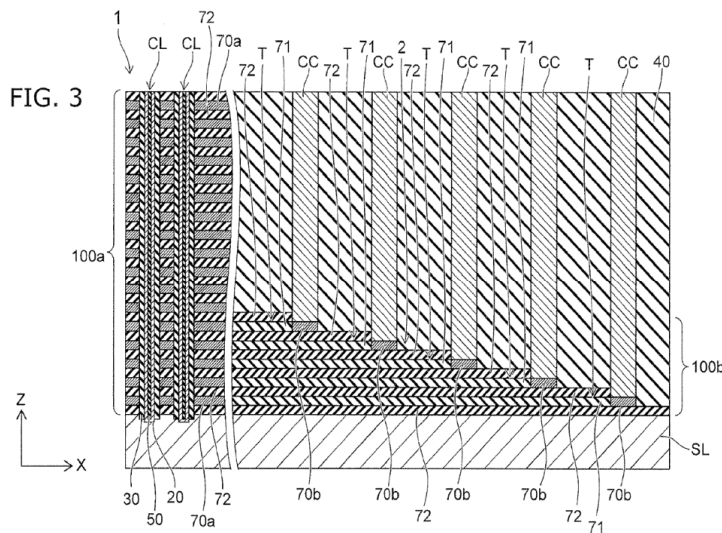


FIG. 33A

Id., Fig. 3, Fig. 33A. When applying these teaching to Thimmegowda, *the conductor portion* (the conductive finger on steps 332a-d) *and the dielectric layer* (dielectric layers 310a-c and 320a-c) *are each above the one or more dielectric pairs* (the combination of the remaining sacrificial material on steps 332b-d and their respective insulating layer 310b-d/320b-d in the underlying step(s)). This beneficially solves the punch through problem.

E. Claim 4 “The 3D memory device of claim 2, wherein along the lateral direction, a width of the conductor portion is equal to a dimension of the stair.”

192. Thimmegowda in view of Kobayashi renders this limitation obvious. For the same reasons that I discuss in Ground 1, it would be obvious for the width of the conductive finger in the x-direction can be co-extensive with the exposed surface area of the step, and thus the *width of the conductor portion* in the x-direction

(viz., *the lateral direction*) *is equal to a dimension of the stair* (viz., the width of the step in the x-direction).

F. Claim 5 “The 3D memory device of claim 1, wherein along the second lateral direction perpendicular to the lateral direction, a length of the conductor portion is equal to or less than a second dimension of the stair.”

193. Recall that the *second lateral direction* is the y-direction in the '604 patent. The *second dimension of the stair* refers to the length of the step in the y-direction toward the bridge. Thimmegowda in view Kobayashi renders obvious claim 5. Thimmegowda in view of Kobayashi renders obvious that the conductive finger extends the full length of the step (in the y-direction toward wordline bridge 306), and is thus *equal to ... a second dimension of the stair* (i.e., the length of the step in the y-direction).

194. Kobayashi's Figs. 1 and 5 illustrate that the length of the protruding “finger” (viz., first conductive portion 70b) extends the full length of the step (i.e., to the point where it reaches the wordline bridge running horizontally in the x-direction toward the memory array). That is, it extends to where it reaches the element that connects to the memory stack. Applying that teaching to Thimmegowda results in this finger, which equals the second dimension of the stair, flowing into the bridge, such that the staircase contact can bidirectionally drive both arrays.

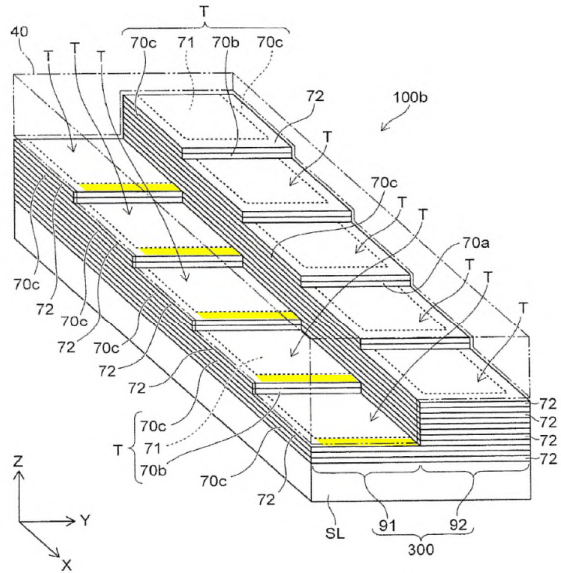
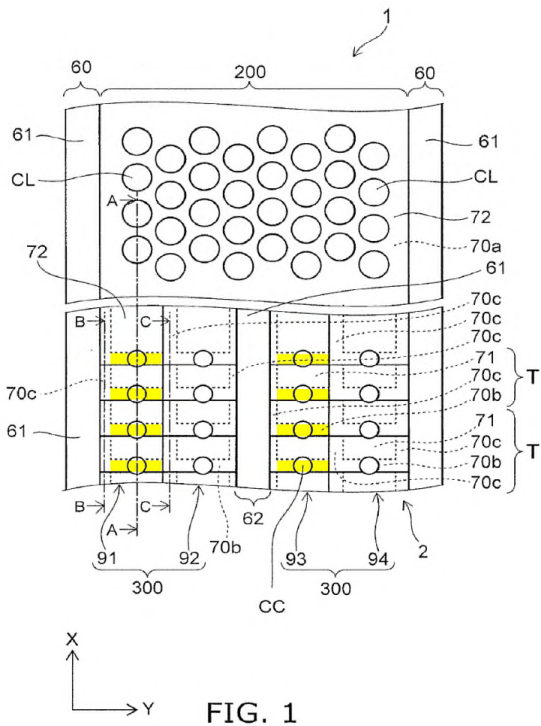


FIG. 5

Ex. 1006, Figs. 1 and 5 (annotated).

G. Claim 8

195. Thimmegowda in view of Kobayashi renders obvious claim 8.

1. [8.A] “The 3D memory device of claim 1, wherein: the conductor portion comprises at least one of tungsten, cobalt, copper, aluminum, silicides, or polysilicon;”

196. Thimmegowda in view of Kobayashi renders obvious this limitation.

Recall that Thimmegowda discloses that its wordlines are polysilicon. However, using a gate replacement process, as taught by Kobayashi, was obvious. Kobayashi discloses that “the first conductive portion 70b ... are, for example, a metal layer including mainly tungsten.” Ex. 1006, [0074]; *see also id.*, [0135] (similar). I

discuss the benefits of the gate replacement process in Claim [8.A] of Ground 1. The same benefits equally apply here.

2. [8.B] “the dielectric portion comprises silicon nitride; and”

197. Thimmegowda in view of Kobayashi renders obvious this limitation. I discuss the *dielectric portion* of this grounds for Thimmegowda and Kobayashi combination. That portion is a remaining part of the sacrificial gates. Kobayashi discloses that “the sacrificial layer 71,” which is used to form the spacer portion 71, “is, for example, a silicon nitride layer.” Ex. 1006, [0080]; *see also id.*, [0093], [0096], [0113], [0117], [0122], [0141] (“the spacer portions 71 are silicon nitride layers and are insulating bodies”). Silicon nitride was the typical composition for sacrificial gates.

3. [8.C] “a dielectric layer is arranged under the conductor portion and the dielectric portion, the dielectric layer comprising silicon oxide.”

198. Thimmegowda in view of Kobayashi renders obvious this limitation. The only part of element 8[c] that is different than claim 2 is that *the dielectric layer comprising silicon oxide*. The claimed *dielectric layer* in Thimmegowda (modified or unmodified) is the insulating layer 310a-d/320a-d. Ex. 1005, 9:49-50, 8:34-38, 8:57-60. These insulating layers are “silicon dioxide.” *Id.*, 8:44-67. This is the most common insulating layer of a 3D memory stack. Kobayashi employs silicon oxide insulating layers as well. Ex. 1006, [0003].

H. Claim 9

199. Recall that the individual claim elements of claim 9 are similar to, and broader than, claim 1 in a number of respects, and my analysis of claim 1 equally apply here.

1. [9.PRE] “A three-dimensional (3D) memory device, comprising:”

200. If limiting, the preamble of claim 9 is satisfied for the same reasons as the claim 1 preamble.

2. [9.A] “a memory array structure; and”

201. Claim element 9[a] is met for the same reasons as claim element 1[a].

3. [9.B] “a staircase structure comprising a plurality of stairs extending along a lateral direction,”

202. Claim elements 1[b] and 1[c] collectively require everything recited by claim element 9[b]. Accordingly claim element 9[b] is satisfied for the same reasons as claim elements 1[b] and 1[c].

1. [9.C] “a stair comprising a conductor portion on a top surface of the stair and a dielectric portion at a same level and in contact with the conductor portion, the conductor portion being electrically connected to the memory array structure,”

203. As explained in connection with Ground 1, claim elements 1[f] and 1[g] collectively require everything recited by claim element 9[c], except that element 9[c] requires the *conductor portion* (instead of just *the stair*) be *electrically*

connected to the memory array structure. As I explain for element 1[g], Thimmegowda in view of Kobayashi discloses that the *conductor portion* of the stair electrically connects the stair to the memory array, thereby enabling the staircase contact to electrically couple to the gate layer of the memory stack. Thus, my analysis of 1[F] and 1[G] demonstrates that claim element 9[c] is obvious.

2. [9.D] “wherein along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged.”

204. Claim element 9[d] is the same as element 1[h] and is satisfied for the same reasons.

I. Claim 10: “The 3D memory device of claim 9, wherein the staircase structure further comprises a dielectric layer under the conductor portion and the dielectric portion.”

205. Claim 10 adds the same limitation as claim 2 and is met for the same reasons.

J. Claim 11: “The 3D memory device of claim 10, wherein: the conductor portion and the dielectric layer are each above one or more dielectric pairs.”

206. Claim 11 adds the same limitation as claim 3 and is met for the same reasons.

K. Claim 12: “The 3D memory device of claim 9, wherein along the lateral direction, a width of the conductor portion is equal to a dimension of the stair.”

207. Claim 12 adds the same limitation as claim 4 and is met for the same reasons.

L. Claim 13: “The 3D memory device of claim 9, wherein along the second lateral direction perpendicular to the lateral direction, a length of the conductor portion is equal to or less than a second dimension of the stair.”

208. Claim 13 adds the same limitation as claim 5 and is met for the same reasons.

XIV. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

209. During my review of the materials discussed herein, I did not become aware of any evidence suggesting the existence of any secondary indicia or considerations of non-obviousness. In the event that Patent Owner proffers any such evidence, I shall provide my opinions on such evidence in a reply declaration.

XV. DECLARATION

210. In signing this declaration, I realize that this declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the USPTO.

211. I am aware that willfully false statements and the like made by me in connection with this declaration are punishable by fine or imprisonment, or both (18 U.S.C. § 1001) and may jeopardize the validity of the Petition. All statements herein made by me of my own knowledge are true and all statements made on information and belief are believed to be true. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 11th day of October 2024 at Austin, Texas.



Sanjay Banerjee, Ph.D.