

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: February 21, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00035
Patent 11,450,604

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

I.	Introduction.....	1
II.	Background.....	3
	A. 3D NAND Memories	3
	B. The '604 Patent (Ex. 1001)	5
	C. Prosecution History	9
	D. Person of Ordinary Skill in the Art	10
	E. Claim Construction	11
III.	Overview of the Asserted Art.....	11
	A. Thimmegowda (Ex. 1005).....	11
	B. Lee (Ex. 1007) and Kobayashi (Ex. 1006).....	14
IV.	Grounds 1 and 2: Claims 1-5 and 8-13 are not obvious based on Thimmegowda, Lee/Kobayashi, and the knowledge of a POSITA.	17
	A. A POSITA Would Not Have Been Motivated To Modify The Stairsteps Of Lee (Ground 1) or Kobayashi (Ground 2) To Render Obvious “a width of the conductor portion is unchanged” In Combination With Thimmegowda	18
	B. A POSITA Would Not Have Been Motivated To Combine Thimmegowda with Lee or Kobayashi	24
V.	Ground 2: Petitioner failed to meet its burden for claim 15.....	28
VI.	The Board should exercise its discretion and deny institution under 35 U.S.C. § 314.....	29
	A. Factor 1 favors denial because a stay is unlikely.	29
	B. Factor 2 is neutral because the trial date is less than a month after Final Written Decision.	30

C.	Factor 3 favors denial because substantial effort will have been expended by the deadline for institution.	31
D.	Factor 4 favors denial because there is significant overlap between the issues raised in the Petition and the district court proceeding.	33
E.	Factor 5 favors denial because Micron is the defendant in the district court proceeding.	34
F.	Factor 6: The limited resources of the Board favors denial.	34
VII.	Conclusion	35

TABLE OF AUTHORITIES**Page(s)****CASES**

<i>10x Genomics, Inc. v. President & Fellows of Harvard Coll.</i> , IPR2023-01299, Paper 15, 2024 WL 993828	31, 32, 34
<i>Apple Inc. v. Fintiv, Inc.</i> , IPR2020-00019, Paper 11 (Mar. 20, 2020)	27, 29, 33
<i>Boe Tech. Grp. Co. v. Element Cap. Com. Co. Pte. Ltd.</i> , IPR2023-00808, Paper 9, 2023 WL 7715885	31, 33, 34
<i>Catalyst Orthoscience Inc. v. Shoulder Innovations, Inc.</i> , PGR2024-00042, Paper 17 (Dec. 19, 2024)	29
<i>Comcast Cable Commc'ns, LLC v. Touchstream Techs., Inc.</i> , IPR2024-00323, Paper 13, 2024 WL 3530021	31, 32, 33
<i>Entangled Media, LLC v. Dropbox Inc.</i> , 732 F. Supp. 3d 1120 (N.D. Cal. 2024)	28
<i>In re Fritch</i> , 972 F.2d 1260 (Fed. Cir. 1992)	26
<i>Skillz Platform Inc. v. Aviagames Inc.</i> , No. 21-cv-02436-BLF, 2022 WL 1189882 (N.D. Cal. Apr. 21, 2022)	28

STATUTES

35 U.S.C. § 314	27
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Exhibit List

Ex.	Description
2001	Micron's Motion to Stay the Case Pending Inter Partes Review and Post Grant Review Proceedings, <i>Yangtze Memory Technology Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 16, 2025), ECF No. 200
2002	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending Inter Partes Review and Post-Grant Proceedings, <i>Yangtze Memory Technology Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3 2025), ECF No. 221
2003	RESERVED
2004	U.S. District Courts–Time Intervals from Filing Date to Beginning Date for Completed Civil Trials, by District, During the 12-Month Period Ending September 30, 2024 (https://www.uscourts.gov/sites/default/files/2025-01/jb_t3_0930.2024.pdf)
2005	RESERVED
2006	Curriculum Vitae of Konstantinos Giapis, Ph.D.
2007	Declaration of Konstantinos Giapis, Ph.D. (“Giapis”)

I. Introduction

Patent Owner Yangtze Memory Technology Company, Ltd. (“YMTC”) respectfully submits this Preliminary Response to the Petition for *inter partes* review of U.S. Patent 11,450,604 (“’604 patent”). As explained below, Petitioner has failed to carry its burden to show a reasonable likelihood that at least one of the challenged claims is unpatentable. Thus, the Board should deny the Petition and no IPR proceeding should be instituted.

The ’604 patent describes and claims an innovative staircase and bridge structure for 3D NAND memories. The ’604 patent’s staircase structure includes steps with (i) a conductive portion having a width that is “***unchanged***” along the x-direction length of the step, and (ii) dielectric material both below and “***at a same level***” as the conductive portion. Among other advantages, the aforementioned features help avoid short circuits when contact structures (shown as 316 below) over-etch and inadvertently “punch through” the conductive step 320 (blue) as it will hit only dielectric materials (green). This is shown below in annotated Figure 3A of the ’604 patent.

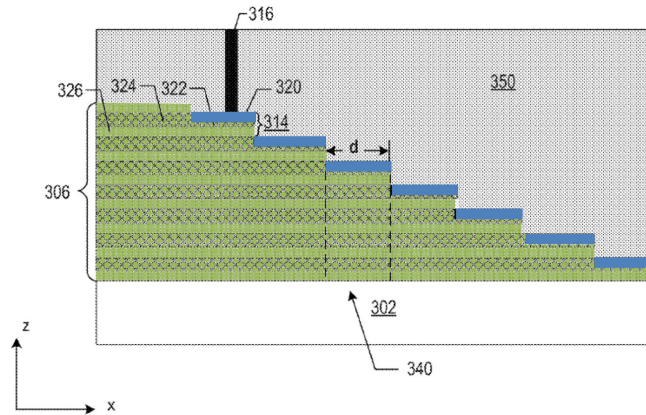


FIG. 3A

But because of the dielectric materials that prevent punch through, the conductive portions of the staircase (blue) are, by themselves, electrically isolated from the memory arrays to the left and right (in the x-direction) of the staircase structure.¹ The '604 patent thus teaches a “bridge structure” that connects the blue conductive portion to both memory arrays. Figures 1C and 1B show a bird’s eye view and a side view, respectively, of the novel staircase and bridge structures of the '604 patent. As shown annotated below, a bridge structure 108 (turquoise) runs along the staircase structure 106 (blue) and electrically connects (maroon arrows) conductive portions 114 (blue) of the staircase to memory structures 120 on the right (pink, positive x direction) and on the left (orange, negative x direction).

¹ Figure 3A does not show the memory arrays to the left and right of the staircase structure. Those are shown in, for example, Figure 1C.

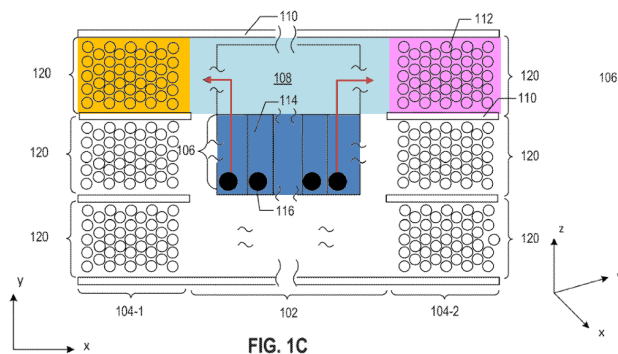


FIG. 1C

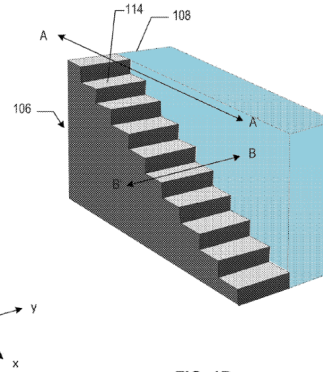


FIG. 1B

The Petition presents two grounds of purported invalidity. Both are based on combining Thimmegowda's "bridge and array architecture teachings" with the "stairstep teachings" of either Lee or Kobayashi. Pet. 34-35, 69. Thimmegowda, however, discloses a bridge that connects a staircase structure to *one* memory array situated next to the staircase in *one* direction. And Lee and Kobayashi's steps are deliberately designed to have varying width to connect to a memory structure without an intervening bridge. A POSITA would not have been motivated to combine Thimmegowda with either Lee or Kobayashi as Petitioner proposes. In fact, combining Thimmegowda with Lee or Kobayashi as proposed results in an inoperable device as explained in greater detail below.

The Board should deny the Petition.

II. Background

A. 3D NAND Memories

3D NAND memory devices are memory arrays with memory cells stacked one on top of the other. '604 patent 4:58-60. Memory cells can be written or read

by applying a voltage to corresponding conductors, called “word lines,” that run horizontally across the memory array. Giapis (Ex. 2007) ¶23.

An exemplary 3D NAND memory is shown in Figure 5.20 of Petitioner's Exhibit 1014, which depicts a series of vertically stacked memory cells, each controlled by a “Control Gate”—the word lines—shown in red as “CG0” through “CG3.” Ex. 1014 at 119; Giapis ¶23.

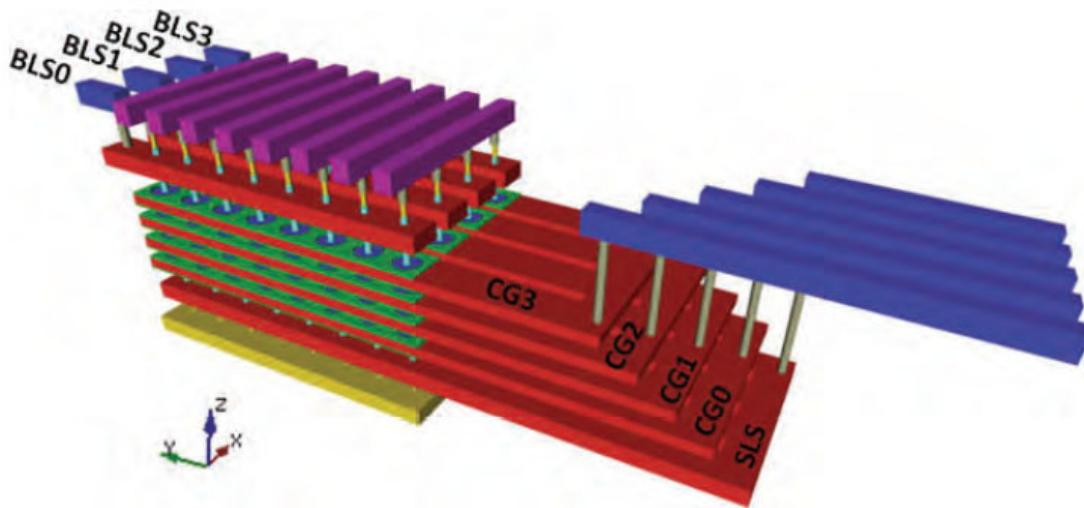


Fig. 5.20 C-FG NAND Flash array with fan-out

The word lines (CG0, CG1, CG2, and CG3) need to be accessed externally to the memory device in order to control the memory. Giapis ¶24. In the prior art, the word lines extend out of one memory array in a staggered manner as shown above. Ex. 1014 at 119. That way, the word lines can then be separately accessed through the vertical vias (shown in tan) connected to external conductive lines

(shown in blue). Ex. 1014 at 119. But if a word line via is over-etched, it will hit a lower word line below (red), causing a short circuit. Giapis ¶25.

B. The '604 Patent (Ex. 1001)

The '604 patent recognized that one problem with the “word line fan-out” of the prior art is that the etching process for the vertical via contacts can result in over-etching. '604 patent 5:1-20. That will cause the vias to penetrate below (or “punch through”) the desired conductor into lower conductor layers, resulting in short circuits. '604 patent 5:1-20.

The '604 patent describes that “[a]s the demand for higher storage capacity continues to increase, the number of vertical levels of the stacked storage structure also increases.” '604 patent 4:63-65. With increasing number of vertical levels, “it has become more difficult to form the word line VIA contacts on the stairs without punching through the contacts and causing short circuits.” '604 patent 4:65-5:1. Previous attempts to solve the punch-through problem involved thickening the conductor layers, resulting in a more challenging fabrication process and not satisfactorily reducing the possibility of punch-through. '604 patent 5:20-24.

The '604 patent discloses an innovative solution to the punch-through problem. As shown in Figure 3A annotated below, the staircase comprises dielectric layers (green) on the same level as conductor portions (blue) corresponding to the word lines. Giapis ¶¶28-29; '604 patent 10:60-11:6. The

conductive portion at the ends of the staircase form a conductive portion for connection to the vias, enabling word line access. Giapis ¶28; '604 patent 10:39-42. This way, as shown below, the conductive portions (blue) do not overlap with one another vertically. Giapis ¶28; '604 patent 11:7-15. And if punch-through occurs, it would only penetrate the dielectric layers (green) below the contact pad, thereby avoiding short circuits. '604 patent 5:58-62.

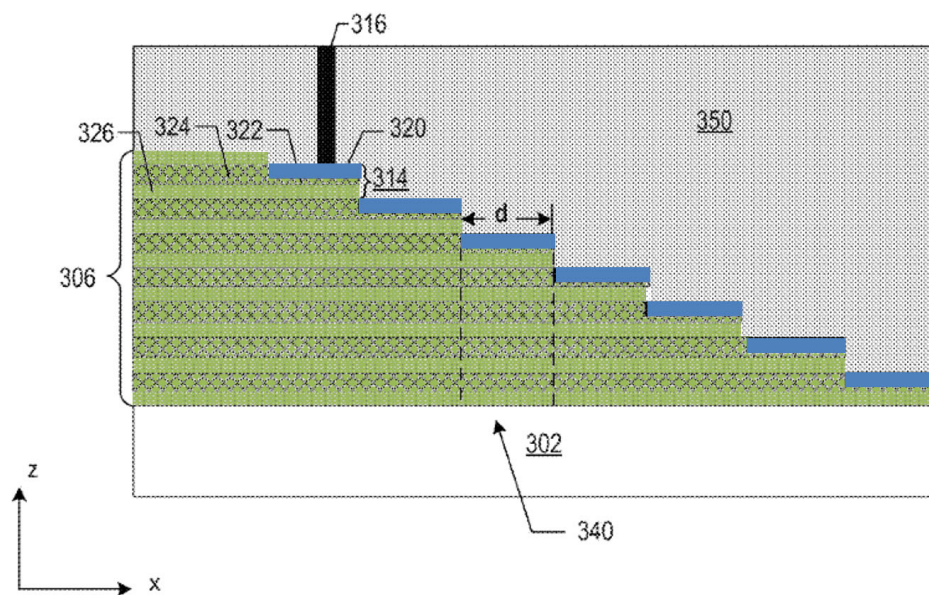


FIG. 3A

But by placing dielectric materials (green) on the same level as the conductive portions 320 (blue), those conductive portions are not, on their own, electrically connected to any memory structures or word lines along which the dielectric materials are placed. Giapis ¶29. To connect the contact pads to their respective word lines, the '604 patent teaches a bridge structure that runs along the side of the staircase, connecting the word lines to memory arrays both to the left

and to the right of the staircase. Giapis ¶29; '604 patent 7:42-43; 7:66-8:30. The perspective view of Figure 1B, annotated below, illustrates the bridge 108 in contact with the staircase structure 108 (turquoise), omitting the memory structures.

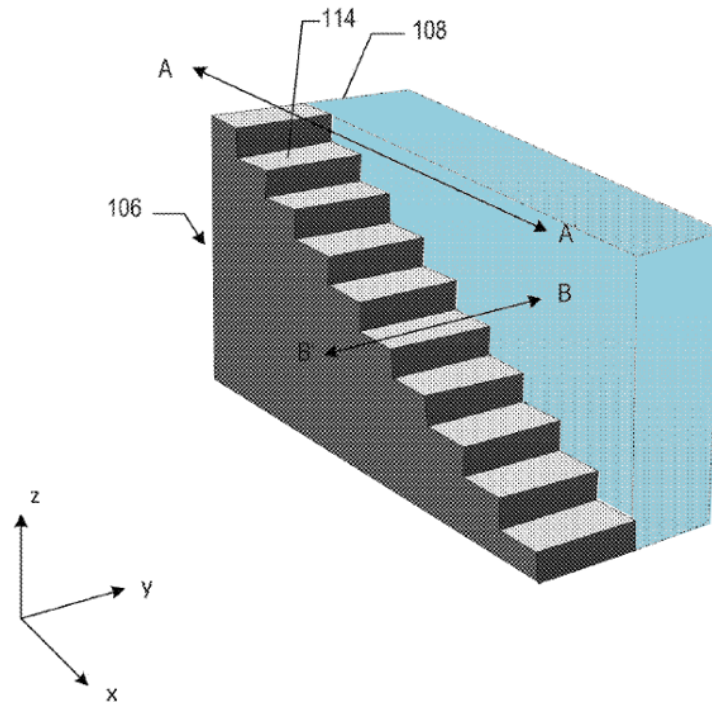
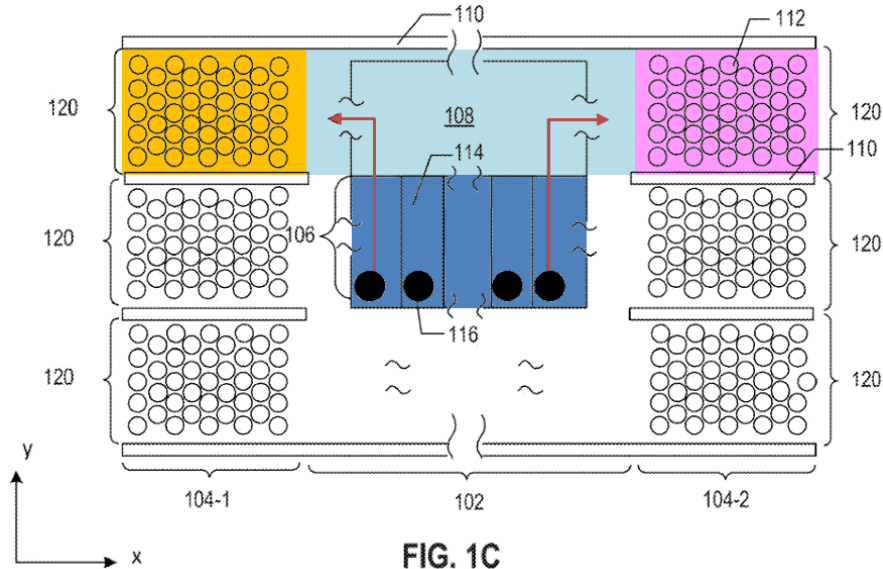


FIG. 1B

Specifically, the bridge structure includes conductive layers (not shown in Figure 1B) that connect the staircase landing pads physically and electrically to memory array structures in both the positive x direction *and* the negative x direction. '604 patent 7:18-25. For example, the top view of Figure 1C (shown annotated below) shows that bridge structure 108 (turquoise) electrically connects (maroon arrows) conductive portions 114 (blue) of the stairs to memory structures

120 on the right (pink, positive x direction) and on the left (orange, negative x direction). '604 patent 8:43-9:17.



Thus, without bridge structure 108, the conductive portions of the '604 patent's claimed staircase 116 would be electrically isolated, and not connected to any memory structure or any other portion of the device via the staircase. Giapis ¶31; *see also* '604 patent 9:4-9. To help connect the contact pads to the bridge structure of the '604 patent, the claims require that the width of the conductor portion of step is "unchanged" in along a "lateral direction perpendicular to" the lateral direction in which the plurality of stairs extend. Giapis ¶31. For example, if the plurality of stairs extends along the x axis in Figures 1B and 1C, reproduced below, then the width of the conductor portion is unchanged along the y axis, as annotated by the red arrows. Giapis ¶31.

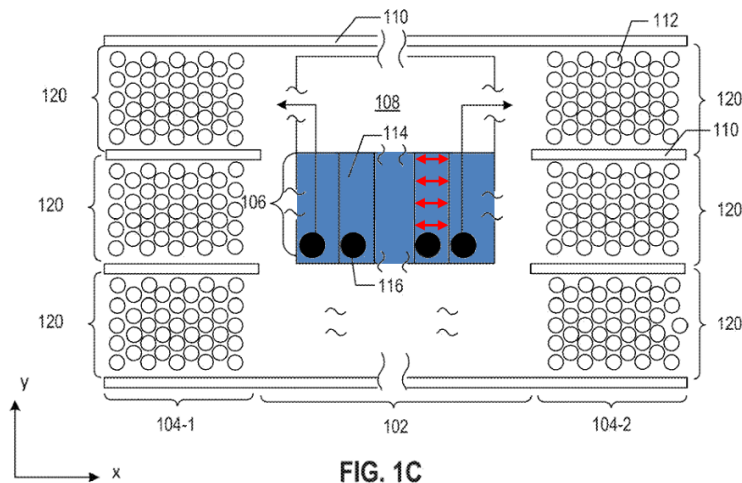


FIG. 1C

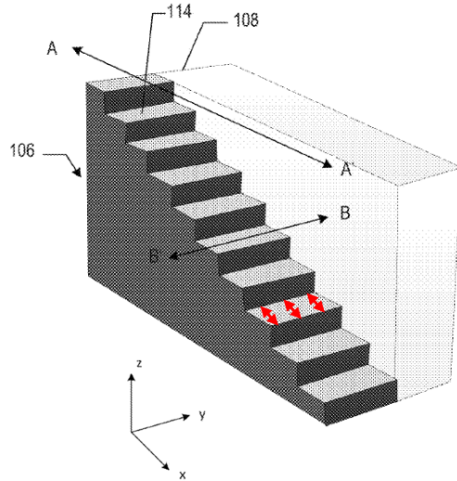
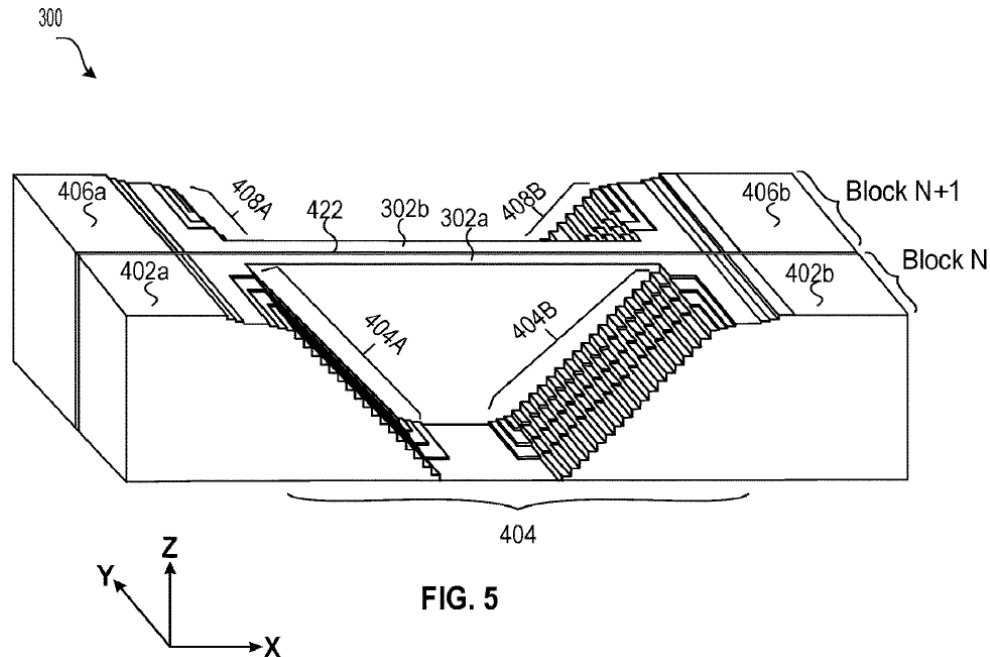


FIG. 1B

C. Prosecution History

The '604 patent was filed July 31, 2020, and issued September 20, 2022. It claims priority to a PCT application (PCT/CN2020/094658) filed June 5, 2020. After several information disclosure statements providing art to the Examiner, the Examiner allowed the claims on March 21, 2022. The Examiner noted that the closest prior art of record was Zhang (Ex. 1010), another YMTC patent application. Ex. 1002 657-58.

As shown in Figure 5 below, and correctly observed by the Examiner, Zhang discloses a staircase structure 404 and a bridge structure 302, but does not disclose at least a dielectric portion at a same level and in contact with the conductor portion and along a second lateral direction perpendicular to the lateral direction, a width of the conductor portion is unchanged. Ex. 1002 at 659.



After a minor amendment, and an after-issue-fee IDS, the Examiner allowed the claims on April 21, 2022. Ex. 1002 at 709, 756.

D. Person of Ordinary Skill in the Art

YMTC takes no position on the level of ordinary skill in the art for the purposes of this Preliminary Response, as the Petition has failed to establish a reasonable likelihood of prevailing under any reasonable definition of POSITA.

E. Claim Construction

The prior art relied on in the Petition fails to disclose the subject matter of the challenged claims under any reasonable construction, including their plain meaning.²

III. Overview of the Asserted Art**A. Thimmegowda (Ex. 1005)**

Thimmegowda discloses a 3D NAND memory that does not address the punch-through problem at all. There is no dispute, for example, that Thimmegowda's stairs do not have a dielectric material at the same level as and in contact with the conductor portion of the stair. Pet. 55. Instead, as annotated below, Thimmegowda discloses alternating conductor (blue) and dielectric (green) layers. Giapis ¶32; Thimmegowda 8:34-9:9. If over-etching occurs, the vias of Thimmegowda will contact a lower conductive portion (blue), resulting in a short circuit. Giapis ¶32.

² Patent Owner reserves the right to advocate for claim constructions in the event the Board institutes review in this case.

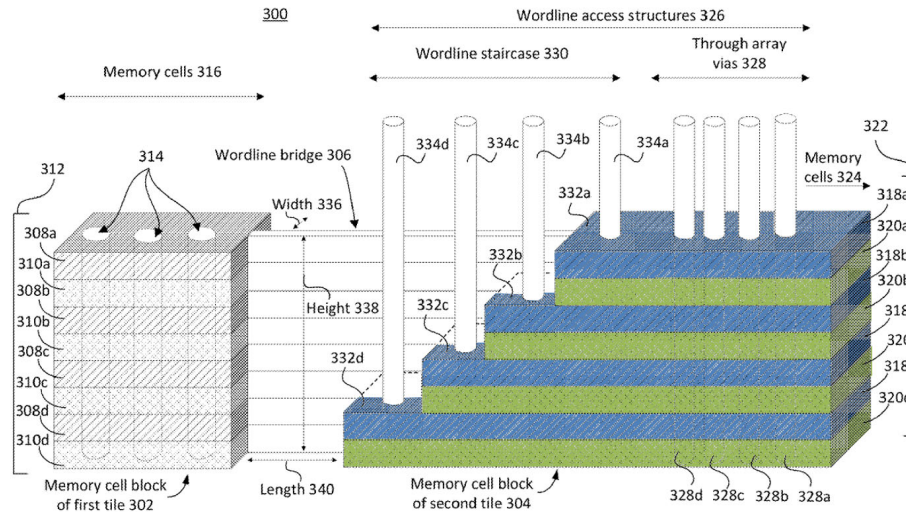


FIG. 3

Petitioner nevertheless relies on Thimmegowda’s disclosure of a “wordline bridge 306.” *E.g.*, Pet. 47. But, unlike the bridge of the ’604 patent, Thimmegowda’s bridge does not run along the staircase. Instead, Thimmegowda’s bridge extends from one end of the staircase to connect the staircase to *one* memory array in *one* x-direction as shown below. Thimmegowda 8:25-33.

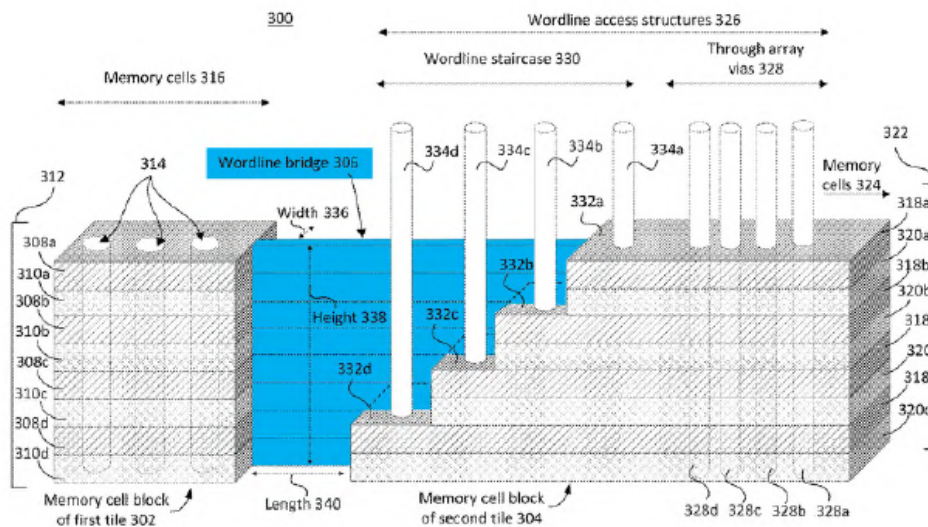


FIG. 3

Notably, as shown in Figure 1B of the '604 patent, the '604 patent bridge structure runs *alongside* the staircase in order to connect it to two memory structures in *both* the positive-x *and* negative-x directions. Pet. 22-23; '604 patent 7:42-43. Thimmegowda's bridge, on the other hand, extends from *one end* of the staircase structure, running up the middle of the stairs, to connect the staircase to *one* memory structure (memory cells 316) in only *one* x-direction. The Petition ignores and does not address these differences.

'604 Patent (annotated)

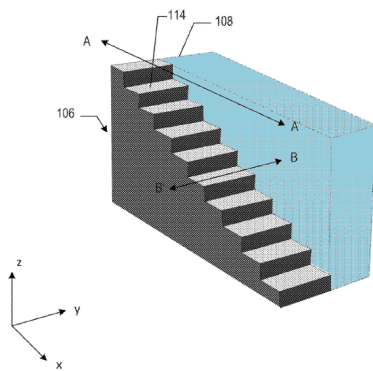


FIG. 1B

Thimmegowda (annotated)

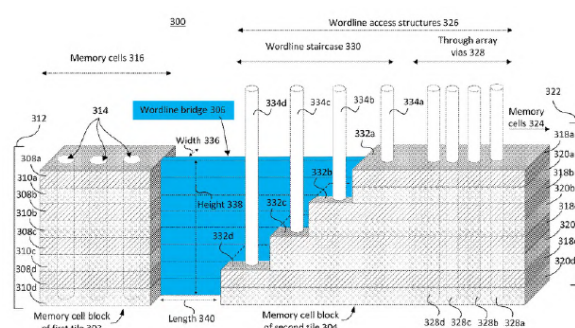


FIG. 3

The differences between the '604 patent bridge and the Thimmegowda bridge are not surprising because the purpose of Thimmegowda's bridge is merely to reduce the number of staircase structures. Giapis ¶¶35-36. Thimmegowda states that increasing density of memory arrays meant "increase in size of the staircase," which "consumes silicon real estate and interferes with the goal of shrinking die sizes or increasing die densities." Thimmegowda 1:20-25; *see also id.* 2:28-34. As a means for reducing the number of staircases, Thimmegowda

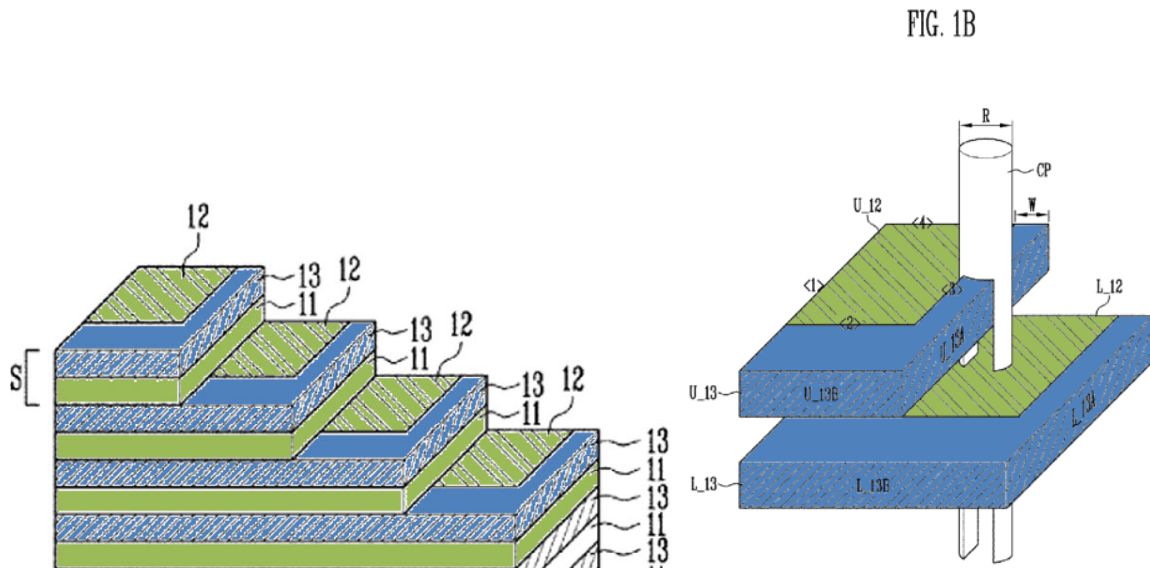
discloses a “wordline bridge that enables blocks of memory cells from one tile to share the wordline access structures of another tile,” i.e., the “staircase structure.” Thimmegowda 2:35-40.

B. Lee (Ex. 1007) and Kobayashi (Ex. 1006)

Petitioner relies on two references, Lee and Kobayashi, for their “stairstep teachings.” Pet. 34-35, 69. But unlike the ’604 patent, each stairstep in Lee and Kobayashi use conductor portions with *varying* width that directly connect to a memory structure, with no need for a bridge. Giapis ¶38.

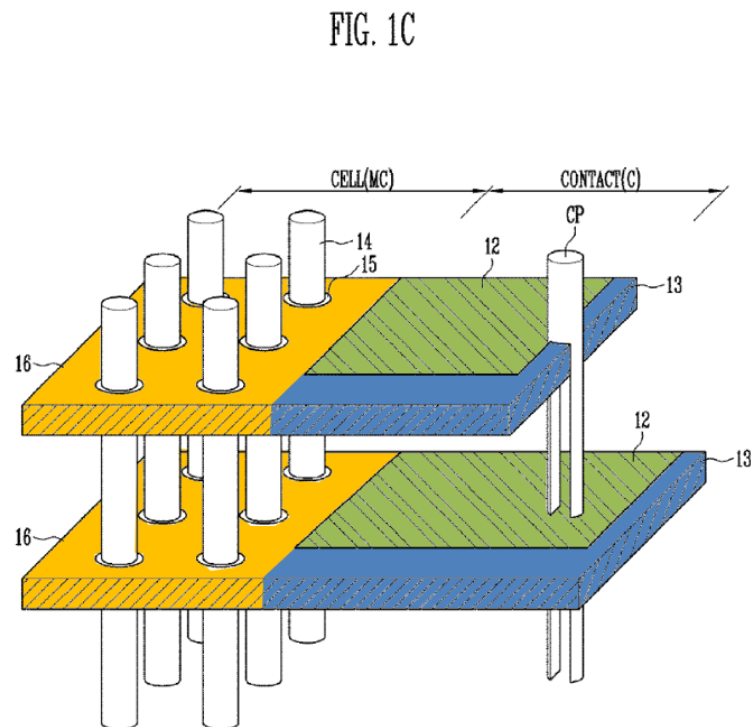
For example, in Figures 1A and 1B of Lee, excerpted and annotated below, the conductor portion 13 (cross-hatched blue side with solid blue top) extends back to connect the conductor portion to the memory array.³ See Lee Abstract (disclosing an “interconnection structure” that includes “conductive layers ... surrounding sidewalls of the dielectric layers”); [0022]-[0023], [0028]. Thus, Lee discloses an L-shape conductor portion. Lee [0022], [0028].

³ Note: in Figure 1B, the insulating layer 11 is omitted for illustrative purposes. Lee [0028].

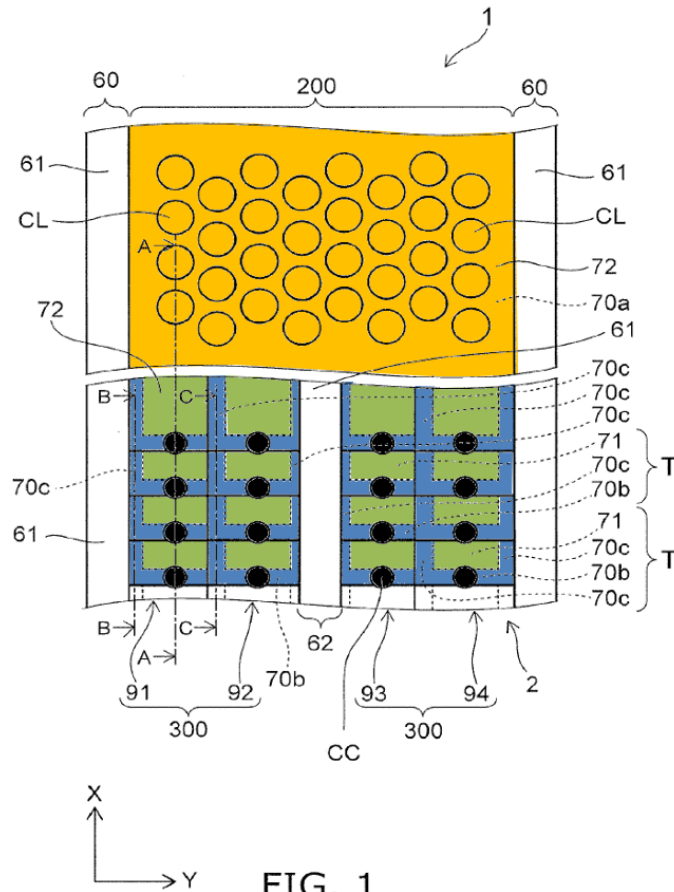


Lee Fig. 1A (left, excerpt) and Fig. 1B (right)

Figure 1C, annotated below, further illustrates that the conductor portion extends back to a memory cell structure, MC (orange). Lee [0032].

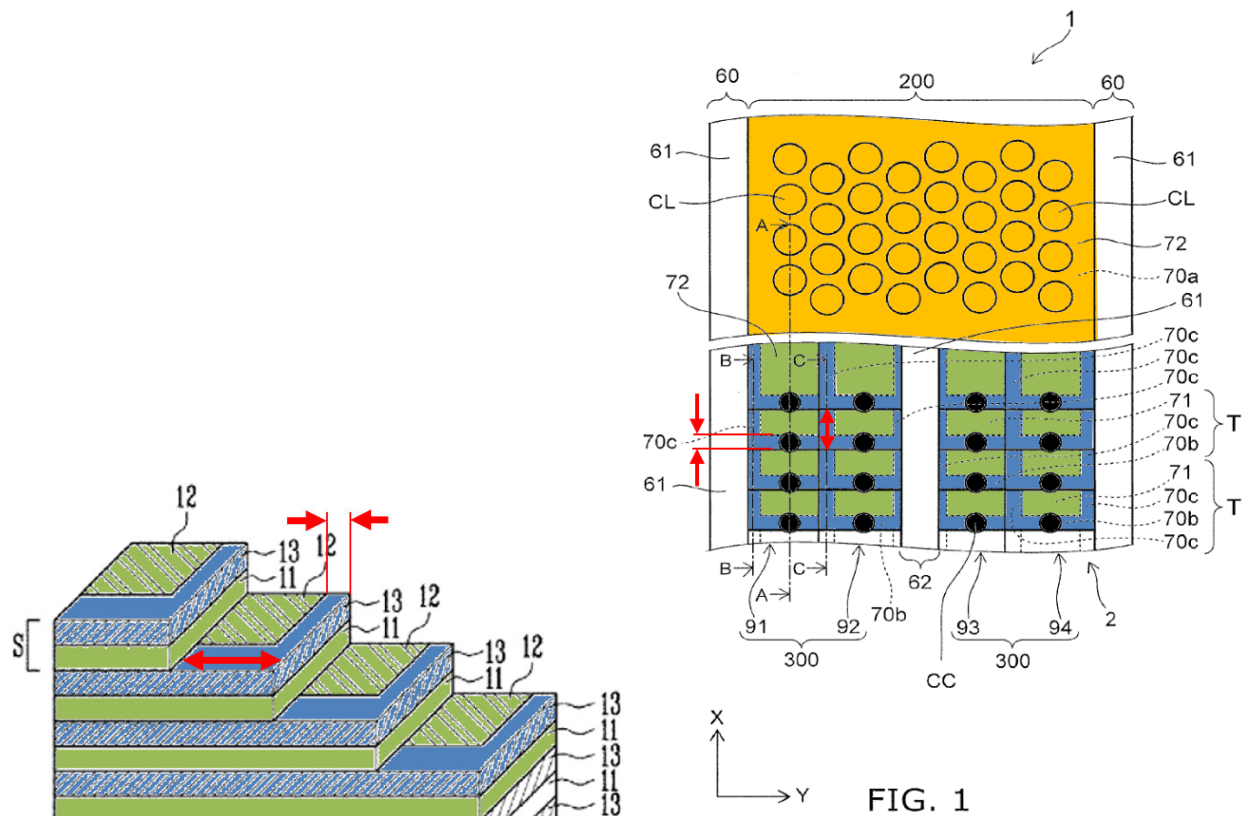


Kobayashi uses a similar design. Figure 1 of Kobayashi, annotated below, shows a top view of two staircase structures 300 with conductive portions 70b/70c (blue) that each extend back to connect to a block 200 (orange) of the memory cell array. Kobayashi [0069], [0071]-[0074], [0079].



Unlike the '604 patent, the stairstep designs of Lee and Kobayashi require conductor portions that do **not** have an unchanged width. Lee [0022], [0028], [0030]; Kobayashi [0069], [0071]-[0074], [0079]. Instead, the conductor portions in both Lee and Kobayashi are deliberately designed to **change** widths in order to extend back and connect to the memory cell array. Lee [0022], [0028]; Kobayashi

[0069], [0079]. This is shown below in annotated Figure 1A of Lee and Figure 1 of Kobayashi.



Lee Fig. 1A (left, excerpt) and Kobayashi Fig. 1 (right)

IV. Grounds 1 and 2: Claims 1-5 and 8-13 are not obvious based on Thimmegowda, Lee/Kobayashi, and the knowledge of a POSITA.

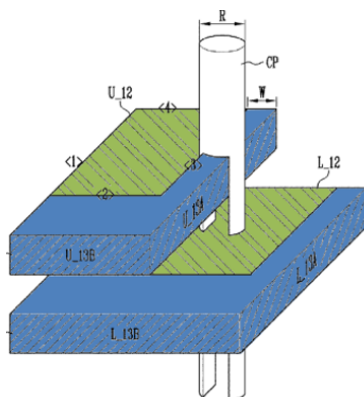
Petitioner proposes to combine Thimmegowda with Lee (Ground 1) or Kobayashi (Ground 2). For the reasons discussed below, Petitioner has not shown a reasonable likelihood that a combination of Thimmegowda and Lee (Ground 1) or a combination of Thimmegowda and Kobayashi (Ground 2) render obvious claims 1-5 and 8-13 of the '604 patent.

A. A POSITA Would Not Have Been Motivated To Modify The Stairsteps Of Lee (Ground 1) or Kobayashi (Ground 2) To Render Obvious “a width of the conductor portion is unchanged” In Combination With Thimmegowda

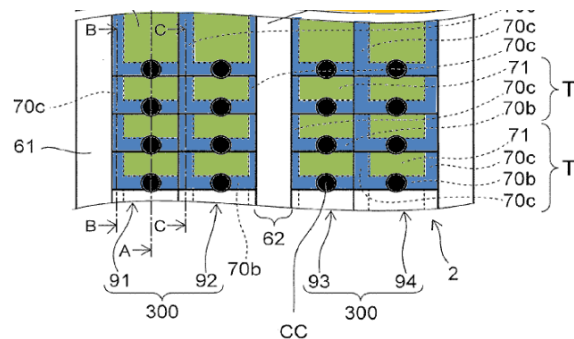
The challenged claims (1-5 and 8-13) require a “conductor portion on a top surface of the stair” where “a width of the conductor portion is unchanged.”

Petitioner proposes “combining Thimmegowda’s bridge and array architecture teachings” with Lee or Kobayashi’s “stairstep teachings.” Pet., 34-35, 69. But the “stairstep teachings” of Lee and Kobayashi do not disclose a “conductor portion” where “a width of the conductor portion is unchanged.” See Lee [0022], [0028], Fig. 1A; Kobayashi [0069], [0079], Fig. 1. To the contrary, the “stairsteps” of both Lee and Kobayashi include an L-shaped “conductor portion” (in blue) with varying widths as shown below (see Giapis ¶¶44, 38-42; Lee [0022], [0028], Fig. 1b; Kobayashi [0069], [0071]-[0074], [0079], Fig. 1):

Lee, Fig. 1b



Kobayashi, Fig. 1

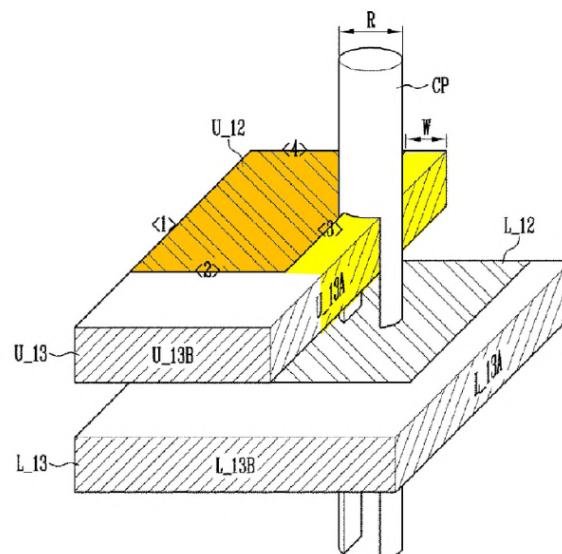


To overcome this deficiency, Petitioner proposes two modifications to the stairstep of Lee (Ground 1) and Kobayashi (Ground 2) to render obvious a

“conductor portion” where “a width of the conductor portion is unchanged.” Both fail.

First, Petitioner asserts that a POSITA would use a “thin finger” of Lee and Kobayashi as the “conductive portion” of a staircase (highlighted in yellow by Petitioner, reproduced below), with the remaining portion being dielectric material (orange). Pet. 36-37 (Ground 1), Pet. 70-71 (Ground 2). As such, other (not highlighted) conductive material of the same staircase is not used by the POSITA in the combination. A POSITA would not have been motivated to make this modification because it would result in an inoperable device. Giapis ¶48.

FIG. 1B



Pet. 58 (annotating Lee, Fig. 1B)

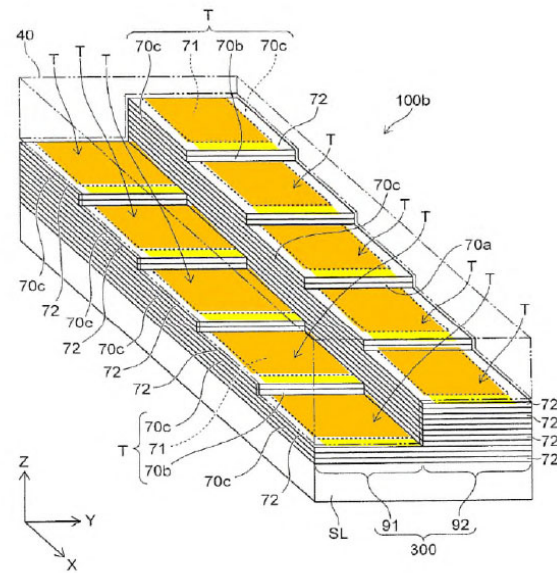
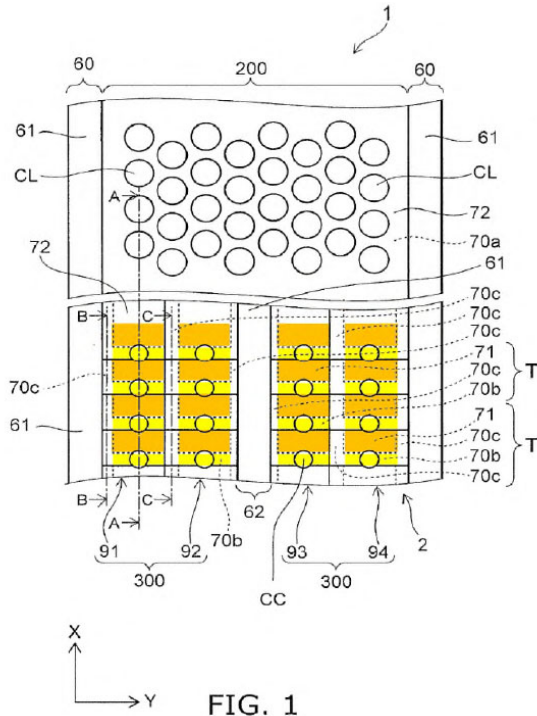


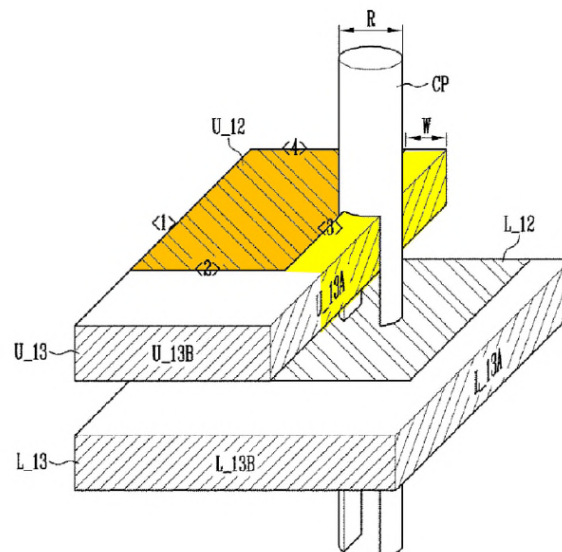
FIG. 5

Pet. 81 (annotating Kobayashi, Figs. 1 and 5)

Specifically, Petitioner’s proposal arbitrarily omits the wider portions of the “conductive portion” of Lee and Kobayashi to meet the limitation of the challenged claims requiring the width of the “conductive portion” to be “unchanged.” That is the definition of impermissible hindsight. Lee and Kobayashi *require* the wider portion of the staircase to electrically connect the landing portion to the memory array. Giapis ¶48; Lee [0030] (“The *connection region* U_13B may couple the pad region U_13A and the gate electrode included in the memory cell structure”) (emphasis added), [0031]; Kobayashi [0073] (“The *second conductive portion 70c ... connects the first conductive portion 70b and the conductive layer 70a* of the first stacked portion 100a”) (emphasis added).

As shown in Petitioner’s own annotated figures below, without the wider portion (U13B in Lee and 70c in Kobayashi), the “thin fingers” (yellow) in both Lee and Kobayashi are “floating” conductors next to a dielectric (orange), and not connected to the memory array, resulting in an inoperative device; this is why the conductive portion must be set in an L-shape with *differing* widths in Lee and Kobayashi. Lee [0030]-[0031]; Kobayashi [0073] (“The second conductive portion 70c...connects the first conductive portion 70b and the conductive layer 70a of the first stacked portion 100a.... The first conductive portion and the second conductive portion 70c are connected in an L-shaped configuration....”). A POSITA would not be motivated to modify the conductive portions to use only a “thin finger” that is electrically disconnected from the rest of the memory device.

FIG. 1B



Pet. 58 (annotating Lee, Fig. 1B)

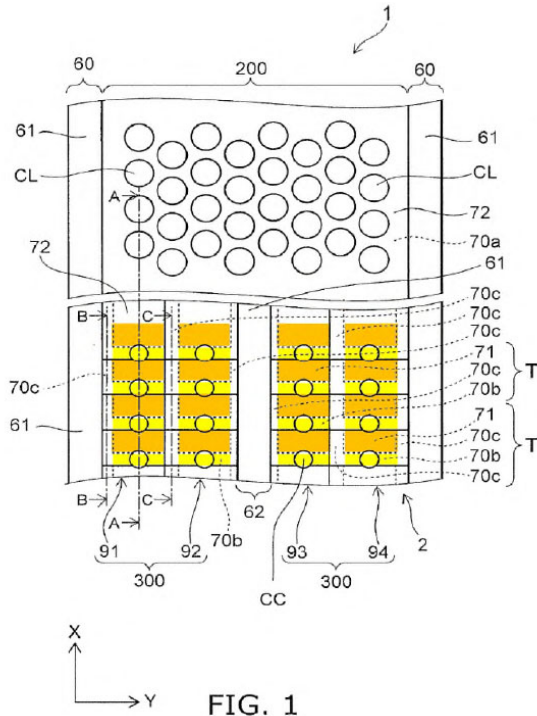


FIG. 1

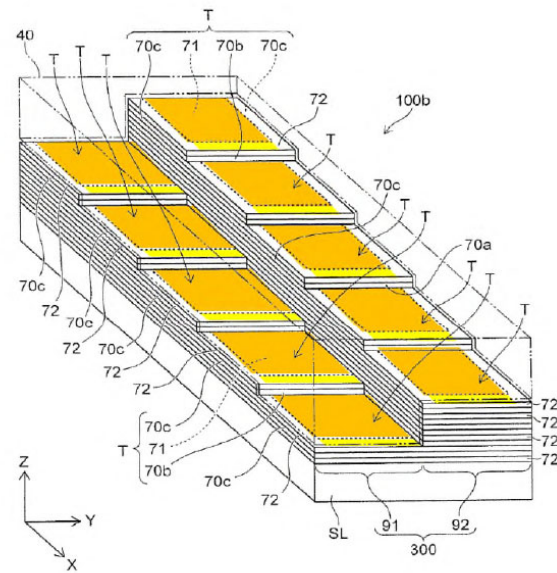


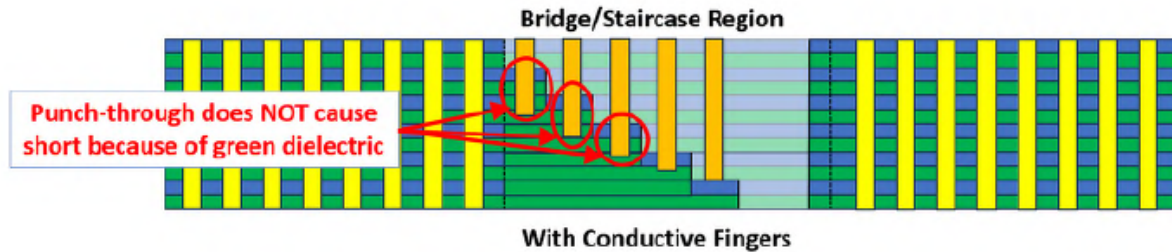
FIG. 5

Pet. 81 (annotating Kobayashi, Figs. 1 and 5)

Put differently, the yellow “thin finger” conductive landing area proposed by Petitioner would be electrically isolated from the array in both the Lee and Kobayashi combinations with Thimmegowda. Giapis ¶48; *e.g.* Lee [0030], Kobayashi [0073] (both describing the connection between the highlighted conductor portion and the memory cells). Petitioner ignores this flaw and provides no explanation as to how the memory array can be electrically connected to the “thin finger” conductor without the wider conductive portion of the step. There is none: the omitted structure provides an essential electrical connection to the memory array.

Second, Petitioner asserts that “it would also have been obvious to a POSITA to make the conductive finger cover the full width of the step” so that its width is “unchanged.” Pet. 37 (Lee), 70 (Kobayashi). But this modification would also result in an inoperable device when combined with Thimmegowda’s bridge and array architecture teachings as proposed.

Petitioner’s own illustration below of its proposed combination confirms its inoperability. Pet. 38-39. In this combination, as described by Petitioner, “adjacent to each step (in the x-direction) is green dielectric material, instead of conductor.” *Id.*; *see also id.* at 79-80. Thus, as shown below in Petitioner’s own illustration, the blue “conductive fingers” of each staircase (blue) are isolated from the memory array to the left of the staircase structure by the newly added green dielectric material in Petitioner’s Thimmegowda/Lee and Thimmegowda/Kobayashi combinations. Giapis ¶49. Such a device would be inoperable because the word lines of the leftmost memory array would not be connected to the staircase or vias for external word line access. *Id.* Petitioner does not address this flaw in its proposed modification.



Pet. 39

Thus, a POSITA would not have been motivated to modify the staircase teachings of Lee or Kobayashi as Petitioner proposes to render obvious a “conductor portion” where “a width of the conductor portion is unchanged.”

B. A POSITA Would Not Have Been Motivated To Combine Thimmegowda with Lee or Kobayashi

Even if a POSITA would have been motivated to modify the stairsteps of Lee or Kobayashi as Petitioner proposes, a POSITA still would not have been motivated to combine Thimmegowda’s “bridge and array architecture teachings” with Lee or Kobayashi’s “stairstep teachings.”

With respect to both grounds, Petitioner asserts that “[i]n modified Thimmegowda, the area immediately adjacent to the finger (in the x-direction toward the righthand memory array) is an insulator.” Pet. 57, 79. But, as discussed, using dielectric material next to each stairstep of Thimmegowda as Petitioner proposes will leave the “conductive fingers” of Petitioner’s proposed combinations electrically and physically isolated from the memory to the right of the staircase. Giapis ¶50; *see* Thimmegowda 9:27-38 (the wordline staircase

“provides access to the wordline[s]”). This is true in both proposed modifications to the Lee and Kobayashi stairsteps discussed above. *Id.* ¶54.

Thimmegowda's “bridge” does not remedy this fatal deficiency. Modified Figure 3 of Thimmegowda below shows Petitioner's proposed combinations. Thimmegowda's bridge only connects the staircase to *one* memory array (on the left). The memory cells 324 to the right of the staircase comprising wordlines 318b, 318c, and 318d (pink) would be electrically cut off from the stairsteps (blue) if “the area immediately adjacent to the finger ... is an insulator” (green) as Petitioner proposes. Giapis ¶¶50, 54. Contrary to Petitioner's suggestions, Thimmegowda's “wordline bridge 306” does not connect wordlines 318b, 318c, and 318d to the staircase once Petitioner's proposed modification is implemented. Giapis ¶¶51-53; *see* Thimmegowda 9:10-13, 9:27-32, 9:42-45.

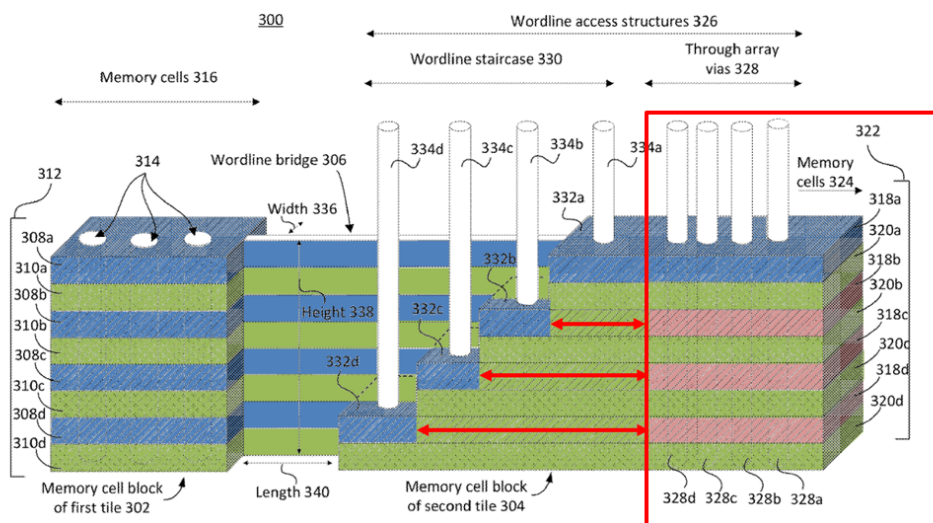


FIG. 3

Petitioner's error results from ignoring fundamental differences between Thimmegowda's bridge and the bridge structure disclosed in the '604 patent. Giapis ¶53. As shown in Figure 1B of the '604 patent, the '604 patent bridge structure runs *alongside* the staircase in order to connect it to two memory structures in *both* the positive-x *and* negative-x directions. Pet. 22-23. This enables the '604 patent's staircase to use conductor portions and dielectrics on the same level that avoid the punch through problem, while still maintaining electrical connection with the memory arrays. Giapis ¶¶53, 29-30. Thimmegowda's bridge, on the other hand, extends from *one end* of the staircase structure, running up the middle of the stairs, to connect the staircase to *one* memory structure (memory cells 316) in *one* x-direction. Giapis ¶¶52-53; Thimmegowda Fig. 3 (showing "length 340" of the wordline bridge as between memory cells 316 and wordline staircase 330). It is not bidirectional, and Petitioner does not show otherwise. *Id.*⁴

⁴ To the extent Petitioner suggests Thimmegowda's bridge can simply supply the electrical connections that would be cut by using the Lee and Kobayashi stairsteps with Thimmegowda as discussed above, Petitioner is wrong as well for the same reasons. Giapis ¶53. In any event, Petitioner has failed to show how such electrical connections would be implemented in either of its proposed combinations.

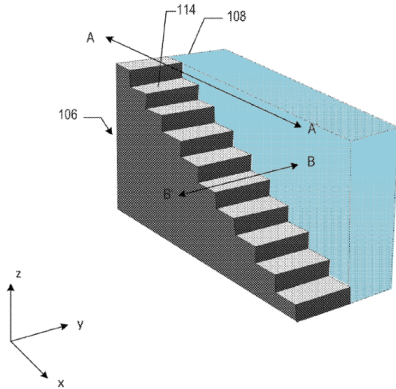
'604 Patent (annotated)

FIG. 1B

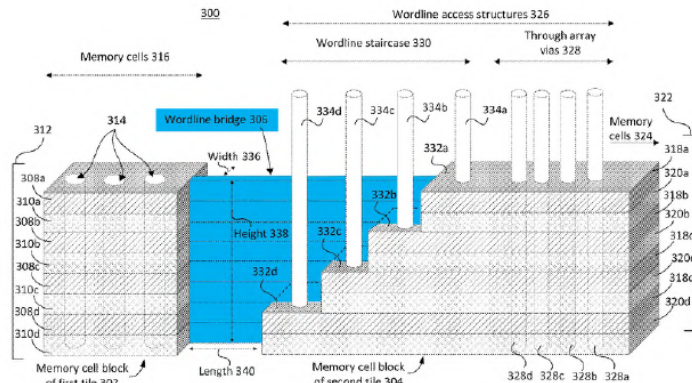
Thimmegowda (annotated)

FIG. 3

Because of this fundamental difference (which the Petition ignores and does not address), a POSITA would not have been motivated to combine Thimmegowda with Lee (Ground 1) or Kobayashi (Ground 2) as Petitioner proposes. The resulting device would be inoperable. *Giapis* ¶54. Petitioner's approach of cherry-picking elements from Lee and Kobayashi (i.e., the staircase) to combine with Thimmegowda (i.e., the wordline bridge) in order to arrive at the claimed invention is the definition of impermissible hindsight.

In view of the foregoing, Petitioner's conclusion that "combining Lee's finger approach with Thimmegowda's bridge would not change the functionality of how wordline vias read/write the memory cells" is plainly incorrect. *Pet.* 40. There is no reasonable expectation of success. *Cf.* *Pet.* 41. Without additional, unaddressed and unmotivated modifications to Thimmegowda's bridge, the proposed modifications of both asserted grounds would render Thimmegowda

inoperable for its intended purpose. *In re Fritch*, 972 F.2d 1260, 1265 n.12 (Fed. Cir. 1992).

The Board should deny the Petition.

V. Ground 2: Petitioner failed to meet its burden for claim 15.

Ground 2 should additionally be denied because Petitioner has failed to meet its burden with respect to claim 15. The Petition defines “the Challenged Claims” as “claims 1-5, 8-13, *and 15*” of the ’604 patent. Pet. 1 (emphasis added). The Petition requests that the Board “find the Challenged Claims unpatentable as obvious.” Pet. 2. In the “Identification of Grounds and Claims Being Challenged,” Petitioner asserts that Ground 2 challenges “[c]laims 1-5, 8-13, *and 15*” as “obvious in view of Thimmegowda, Kobayashi, and a POSITA’s knowledge.” Pet. 6 (emphasis added). In the Board’s P-TACTS system, Petitioner identified claim 15 as challenged by its Petition, mirroring its “Identification of Grounds and Claims Being Challenged” in the Petition.

Total claims: 12

  Updated: 12/19 3:42PM 

Challenged claim number ↑ 2	Ground ↑ 1	Prior art
1-5,8-13	35 U.S.C 103	Obvious in view of U.S. Patent No. 10,515,973 (“Thimmegowda”), U.S. Patent Publ. No. 2016/0027730 (“Lee”) and a POSITA’s knowledge
1-5,8-13,15	35 U.S.C 103	Obvious in view of Thimmegowda, U.S. Patent Publ. No. 2019/006275 (“Kobayashi”) and a POSITA’s knowledge

Thus, the Petition clearly challenges claim 15 in Ground 2. However, Petitioner presents no argument or evidence that claim 15 is obvious. *See* Pet. at iv-v (table of contents of Ground 2); 89 (finishing Ground 2 analysis with claims 10-13).

Accordingly, Petitioner has failed to meet its burden with respect to independent claim 15.

VI. The Board should exercise its discretion and deny institution under 35 U.S.C. § 314.

Institution of an IPR is always discretionary. 35 U.S.C. § 314(a). Here, the Board should exercise its discretion to deny institution because the Petition will not serve as an effective and efficient alternative to litigation. Rather, the overall balance of the *Fintiv* factors shows that “efficiency, fairness, and the merits support the exercise of authority to deny institution.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (Mar. 20, 2020) (precedential).

A. Factor 1 favors denial because a stay is unlikely.

The Parallel Proceeding⁵ has not been stayed, and a stay is unlikely. The Parallel Proceeding presently involves 70 asserted claims from 19 patents. Ex. 2002 at 006. Of those, IPR has been instituted against 23 claims from 8 patents, with 11 claims from one patent have had IPR institution denied across the board.

⁵ *Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.).

Ex. 2002 at 006. Although Petitioner has moved for a stay in the Parallel Proceeding pending resolution of IPRs (Ex. 2001), a stay is unlikely. *See, e.g., Entangled Media, LLC v. Dropbox Inc.*, 732 F. Supp. 3d 1120, 1124 (N.D. Cal. 2024) (characterizing arguments about simplification as “premature” “[b]ecause the PTO has not yet instituted proceedings,” and denying motion to stay); *Skillz Platform Inc. v. Aviagames Inc.*, No. 21-cv-02436-BLF, 2022 WL 1189882, at *3–4, *5 (N.D. Cal. Apr. 21, 2022) (denying motion to stay, stating that any simplification from IPRs “is purely *speculative at this stage*,” and “*the cost of non-institution would be delay without benefit*”).

For these reasons, this factor favors discretionary denial of institution.

B. Factor 2 is neutral because the trial date is less than a month after Final Written Decision.

Trial is set to begin in the Parallel Proceeding on June 15, 2026.⁶ Ex.1008 at 002. That is less than one month after the statutory deadline for a Final Written Decision in this case (May 21, 2026). And, it is *well before* the expected Final Written Decisions that would issue in *eight* other proceedings filed by Micron

⁶ Petitioner's assertion of a 48.9-month median time to trial (Pet. 7 (citing Ex. 1009) misleadingly includes non-jury trials, which have a significantly longer time-to-trial. *See* Ex. 2004 at 003. The corresponding number for jury trials is 32.8 months. Ex. 2004 at 003.

against patents at issue in the Parallel Proceeding. *See* IPR2025-00190, -00191, -00228, -00229, -00244, -00245, -00294, and PGR2025-00021. This factor is therefore neutral. *Fintiv*, IPR2020-00019, Paper 11 at 9 (“If the court’s trial date is at or around the same time as the projected statutory deadline, ... the decision whether to institute will likely implicate other factors”); *Catalyst Orthoscience Inc. v. Shoulder Innovations, Inc.*, PGR2024-00042, Paper 17 at 12-14 (Dec. 19, 2024) (finding Factor 2 neutral where scheduled trial was “just weeks” after the scheduled conclusion of the PGR). A Final Written Decision here would issue after expert discovery, after dispositive motions, and after the pretrial conference. Ex.1008 at 002.

C. Factor 3 favors denial because substantial effort will have been expended by the deadline for institution.

The parties have expended, and continue to expend, substantial resources into the Parallel Proceeding. In that case, the parties have collectively propounded, responded to, and supplemented responses to 38 interrogatories and 117 requests for production. The parties have already produced over 113,000 pages of documents and are continuing to produce thousands more pages of documents. Ex.2002 at 012. They have also engaged in extensive source code discovery, which has involved 14 days of YMTC expert and/or attorney review of code in this District and, more recently, three weeks and counting of code review at Micron’s headquarters in Boise, ID. Ex.2002 at 012. And upon order of the Court, YMTC

has narrowed its claims of infringement to 70 asserted claims, which has required extensive analysis of infringement, validity, and damages issues. Ex.2002 at 012.

The parties have also devoted, and continue to devote, substantial effort to claim construction. The *Markman* hearing is scheduled for April 24—a month *before* institution in this case. Ex.1008 at 002. Claim construction briefing will be finished weeks before then.

Petitioner's assertion that the parties and district court have invested "very little" in the Parallel Proceeding is both wrong and, at the time of this filing and the institution decision, outdated. Pet.10. Petitioner does not even address the substantial effort invested in the Parallel Proceeding in the more than 7 months between filing and the Board's institution decision. Because the parties and the Court will expend significant effort in the parallel litigation *before institution*, this factor favors discretionary denial of institution. *See, e.g., Comcast Cable Commc'ns, LLC v. Touchstream Techs., Inc.*, IPR2024-00323, Paper 13 at 9-10, 2024 WL 3530021, at *4 ("Factor 3 favor[ed] denial" where "substantial work on claim construction [had] happened," and "the related district court litigation ha[d] progressed in other aspects as well," including with respect to contentions); *10x Genomics, Inc. v. President & Fellows of Harvard Coll.*, IPR2023-01299, Paper 15 at 18, 2024 WL 993828, at *8 (similar, noting that the parties had exchanged contentions, "completed claim construction briefing," and that the "district court

ha[d] also considered two motions to dismiss and presided over several discovery disputes”); *Boe Tech. Grp. Co. v. Element Cap. Com. Co. Pte. Ltd*, IPR2023-00808, Paper 9 at 23, 2023 WL 7715885, at *8 (finding “the parties and the District Court ha[d] invested substantial resources in th[e] litigation” because, among other things, “[s]ignificant discovery ha[d] been completed, including the exchange of infringement and invalidity contentions, document requests and interrogatories, and proposed claim terms for construction”).

D. Factor 4 favors denial because there is significant overlap between the issues raised in the Petition and the district court proceeding.

Petitioner Micron has served invalidity contentions identifying the same art from its Petition, and explicitly incorporating its IPR petition by reference.

Although Petitioner stipulates in its Petition that “[s]hould the Board institute, it will not advance in District Court on any ground asserted in this Petition,” no such stipulation has been made in the district court. Pet. 9. Such a narrow stipulation runs the risk of significant overlap both in consideration of the same evidence and arguments framed as “different grounds” than the Petition. Because such a narrow stipulation risks having the district court address substantially the same evidence and arguments that the Board will have to address should it institute an IPR, and on a similar timeline, an IPR of the ’604 patent would be an inefficient use of the Board’s resources and would risk conflicting decisions. *See 10x Genomics*, IPR2023-01299, Paper 15 at 20, 2024 WL 993828, at *9 (“In the absence of a

Sotera stipulation,” “we agree with Patent Owner that the overlapping art and arguments presented in the parallel proceeding weigh in favor of exercising our discretion to deny institution.”) (footnote omitted); *see also Comcast*, IPR2024-00323, Paper 13 at 12, 2024 WL 3530021, at *5 (questioning whether a narrower stipulation “not to pursue in the District Court any ground that utilizes the same combination of prior art references relied upon in the instituted petition” adequately addressed “concerns of inefficiency and the possibility of conflicting decisions”).

E. Factor 5 favors denial because Micron is the defendant in the district court proceeding.

Petitioner is the defendant and counterclaimant in the parallel district court case and, as such, will have a full and fair opportunity to litigate its (overlapping) invalidity contentions in that forum. Thus, this factor favors discretionary denial. *Comcast*, IPR2024-00323, Paper 13 at 13, 2024 WL 3530021, at *5 (“Petitioner is the defendant in the related district court case.... We find that this factor favors denial.”) (citations omitted); *Boe Tech.*, IPR2023-00808, Paper 9 at 24-27, 2023 WL 7715885, at *9.

F. Factor 6: The limited resources of the Board favors denial.

“The sixth *Fintiv* factor takes into account other circumstances that may bear on the decision to exercise discretion to deny, such as the merits of the patentability challenges.” *Comcast*, IPR2024-00323, Paper 13 at 13, 2024 WL

3530021, at *5 (citation omitted). For the reasons explained in Sections IV-VI, below, the Petition fails on the merits for numerous reasons and thus does not present the “particularly strong” or “compelling” showing that can tip the scales in favor of institution. *Fintiv*, IPR2020-00019, Paper 11 at 14-15 (“[I]f the merits of a ground raised in the petition seem particularly strong on the preliminary record, this fact has favored institution.... [I]f the merits of the grounds raised in the petition are a closer call, then that fact has favored denying institution when other factors favoring denial are present.”) (citations omitted); *Comcast*, IPR2024-00323, Paper 13 at 22, 2024 WL 3530021, at *9 (assessing Factor 6, concluding that “Petitioner’s obviousness challenges ... do not meet the compelling merits standard”); *10x Genomics*, IPR2023-01299, Paper 15 at 21-22, 2024 WL 993828, at *10 (same); *Boe Tech.*, IPR2023-00808, Paper 9 at 33-35, 2023 WL 7715885, at *12 (same).

As five of the six *Fintiv* factors favor discretionary denial of institution, and the remaining factor is, at worst, neutral, Patent Owner respectfully requests that the Board exercise its discretion to deny institution.

VII. Conclusion

For the reasons set forth above, the Board should deny the Petition for Inter Partes Review.

Respectfully submitted,

Dated: February 21, 2025

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Preliminary Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(1) because the Patent Owner's Preliminary Response contains 5,466 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Preliminary Response exempted by 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 21st day of February, 2025, a true and correct copy of the foregoing **Patent Owner's Preliminary Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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