

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: February 21, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00035
Patent 11,450,604

**DECLARATION OF KONSTANTINOS GIAPIS
IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE**

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I. Introduction and Qualifications

1. I have been retained by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Petitioner”) to provide my opinion concerning the validity of U.S. Patent No. 11,450,604 (Ex. 1001).

2. I am a professor of chemical engineering at the California Institute of Technology (“Caltech”). I have held a professorial position at Caltech since 1993.

3. My primary research relates to processing of semiconductors, dielectrics, and metals, as performed in the fabrication of semiconductor devices, including microprocessors and digital memories. In particular, my work has focused upon experimental and computational studies of depositing and patterning of layers of electronic materials to fabricate sub-micron features such as transistor gates, vias, and interconnect channels found in VLSI circuits and digital storage. My research group has contributed to the understanding of the evolution of such features (profiles) in single-crystalline silicon, poly-silicon, metal, and dielectric layers subjected to plasma processing (etching and deposition). Since the start of my graduate career in 1985, I have accumulated over 40 years of experience on the processing of semiconductor materials and devices.

4. In my professorial duties at Caltech, I have developed and taught new undergraduate and graduate level courses on semiconductor device physics, processing, and fabrication. These innovative courses combined solid state physics and electronic materials processing technologies with the more traditional chemical engineering subjects of transport phenomena and chemical thermodynamics. The courses have prepared several generations of students for successful careers in the semiconductor industry.

5. During my research career, I have authored or co-authored 100 peer-reviewed papers, 12 refereed conferences proceedings, and two book chapters. Most of my publications relate to basic aspects of semiconductor device processing and, in particular, the interaction dynamics of plasma ions with surfaces of materials used in semiconductor manufacturing. My papers on charging damage during plasma-processing of high-density integrated devices such as microprocessors, and digital memories are highly cited. The latter work includes studies of charging effects during the plasma deposition of interlevel dielectrics on patterned metal interconnects. My laboratory has also extensively used and studied plasma-deposited silicon oxide layers from silane and TEOS precursors. I have also been granted 14 patents.

6. Additional information regarding my education, technical experience and publications, including a list of the U.S. patents of which I am an

inventor/co-inventor, is included in my *Curriculum Vitae*, which I understand is attached at Exhibit 2006.

II. Summary Of Materials Reviewed And Considered

7. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor fabrication, I reviewed the following documents:

Ex.	Description
1001	United States Patent No. 11,450,604 (“the ’604 patent”)
1002	File History for the ’604 patent (“’604 FH”)
1003	Declaration of Sanjay Banerjee
1004	Curriculum Vitae of Dr. Banerjee
1005	U.S. Patent 10,515,973 to Thimmegowda et al. (“Thimmegowda”)
1006	U.S. Patent Application Publication 2019/0006275 to Kobayashi et al. (“Kobayashi”)
1007	U.S. Patent Application Publication 2016/0027730 to Lee (“Lee”)
1012	Aritome, “NAND Flash Memory Technologies” (2016)
1014	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)

8. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the ’604 patent at the time of the invention, which I have been asked to assume is June 5, 2020.

III. Understanding of Legal Standards

9. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

10. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

A. Claim construction

11. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary.

12. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office ("USPTO"). I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Obviousness

13. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is

consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

14. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

15. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

16. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine

references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

17. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated to make a combination includes whether he/she would select particular references in order to combine their elements.

18. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a

full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

19. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

20. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a

reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness.

IV. Level of Ordinary Skill in the Art

21. Dr. Banerjee defines a person of ordinary skill in the art (“POSITA”) as a person having “a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience).” Ex. 1003 ¶ 42.

22. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art. In view of my educational background and work experience, I surpass Dr. Banerjee’s definition of a POSITA, and did so before June 5, 2020. Regardless of the precise definition of a POSITA, Grounds 1 and 2 of the Petition do not show the challenged claims obvious. I reserve the right to opine as to an alternative level of a POSITA in other proceedings or if the Board institutes review in this proceeding.

V. Overview of 3D NAND Memories

23. 3D NAND memory devices include “memory stacks” where memory cells are vertically stacked one on top of the other. ’604 patent, 4:58-60. Memory cells can be written or read by applying a voltage to corresponding conductors, called “word lines,” that run horizontally across the memory array. *E.g.*, Thimmegowda 4:60-5:4. For example, the figure below, from Exhibit 1014, shows vertically stacked memory cells on the left hand side, each controlled by a Control Gate (CG) accessible electrically by means of word lines. Ex.1014 at 134; *see also* Ex.1012 at 62, Fig. 3.4 (equating “Control Gate” with “Word Line”).¹

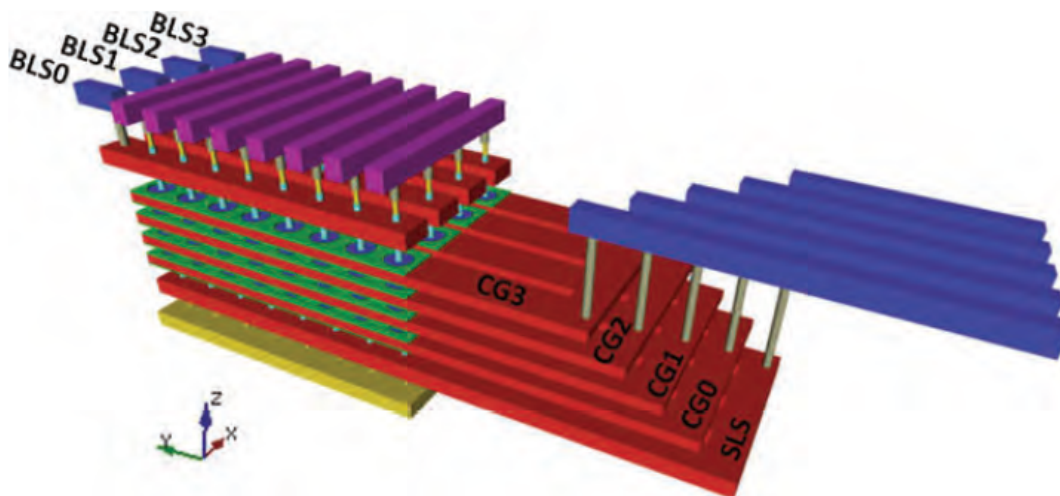


Fig. 5.20 C-FG NAND Flash array with fan-out

¹ Unless otherwise noted my citations are to page numbers in captions added by the parties.

24. The word lines (CG0, CG1, CG2, and CG3) themselves need to be accessed externally to the memory device in order to control the memory. To enable such access, word lines can be “fanned out” in an area adjacent to the memory array ending in conductive portions similar to stair steps arranged in a staircase pattern, as shown above. Ex. 1014, 119; '604 patent 4:60-63. That way, the word lines can then be separately accessed through vertical metal columns (tan) connecting the conductive steps electrically to external conductive lines (blue). Ex. 1014, 119. The metal columns are formed by first drilling channels, called “vias”, in the interlevel dielectric material covering the steps, then filling the vias with metal.

25. The '604 patent recognized that one problem with the “word line fan-out” of the prior art is that the etching process to open the vertical via channels can result in over-etching of the steps. '604 patent 5:1-20. Over-etching means penetration of the vias (or “punch through”) below the desired conductor step into lower conductor layers, resulting in electrical short circuits when those vias are filled with metal. '604 patent 5:1-20. To be clear, if a word line via is over-etched, the via contact may reach a lower word line below (red in the figure above), connecting the two word lines electrically and thus causing a malfunction.

26. The '604 Patent describes that “[a]s the demand for higher storage capacity continues to increase, the number of vertical levels of the stacked storage structure also increases.” '604 patent 4:63-65. With increasing number of vertical levels, “it has become more difficult to form the word line via contacts on the stairs without punching through the contacts and causing short circuits.” '604 patent 4:65-5:1. Previous attempts to solve the punch-through problem involved thickening the conductor layers, resulting in a more challenging fabrication process and not satisfactorily reducing the possibility of punch-through. '604 patent 5:20-24.

VI. Overview of the '604 patent

27. The '604 patent discloses an innovative solution to the punch-through problem. As shown in Figure 3A below, the staircase is not a mere fan-out extension of the memory stack.

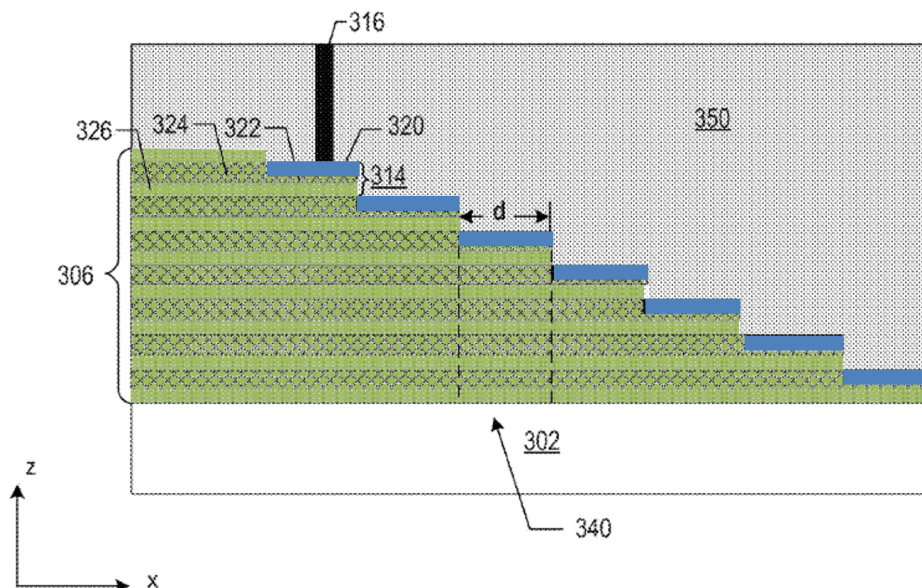


FIG. 3A

28. The conductive portion on each stairstep can be thought of as a “contact pad” (320 in the figure above) for connection to the vias (316), enabling word line access. Instead of the fan-out extension of conductive word lines, the ‘604 patent places a dielectric layer (324) next to every contact pad at each step level. This way, no conductive portion of a word line is located directly underneath any contact pad, as shown in Figure 3A (dashed vertical lines). Thus, punch-through through a pad would not result in a short circuit, no matter how deep the punch-through extends.

29. But by placing dielectric materials (green) on the same level as the conductive portions 320 (blue), those conductive portions are not, on their own, electrically connected to any memory structures or word lines. To connect the contact pads to their respective word lines, the ‘604 patent teaches a bidirectional

bridge structure that runs along the side of the staircase, connecting the word lines to memory arrays *both* to the left and to the right of the staircase. The perspective view of Figure 1B, below, illustrates the bridge 108 in contact with the staircase structure 108 (turquoise), omitting the memory structures.

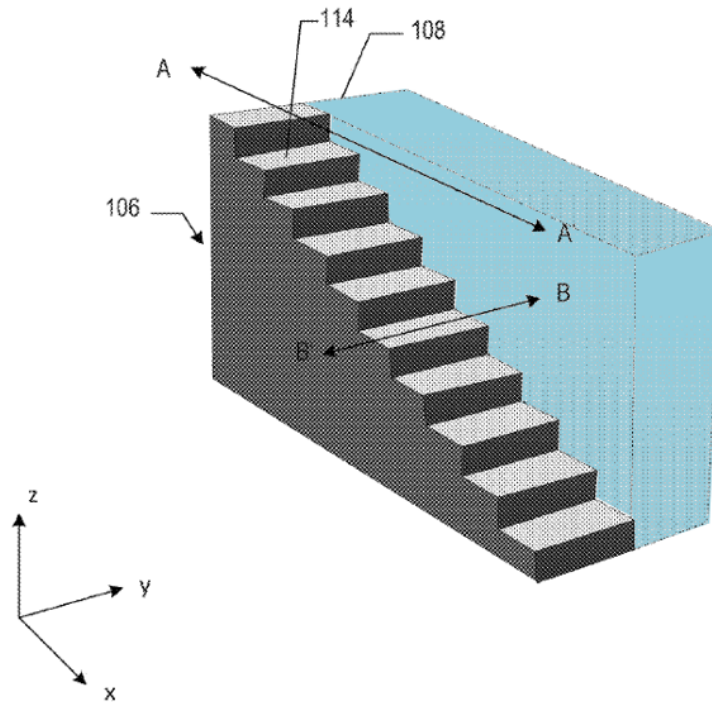
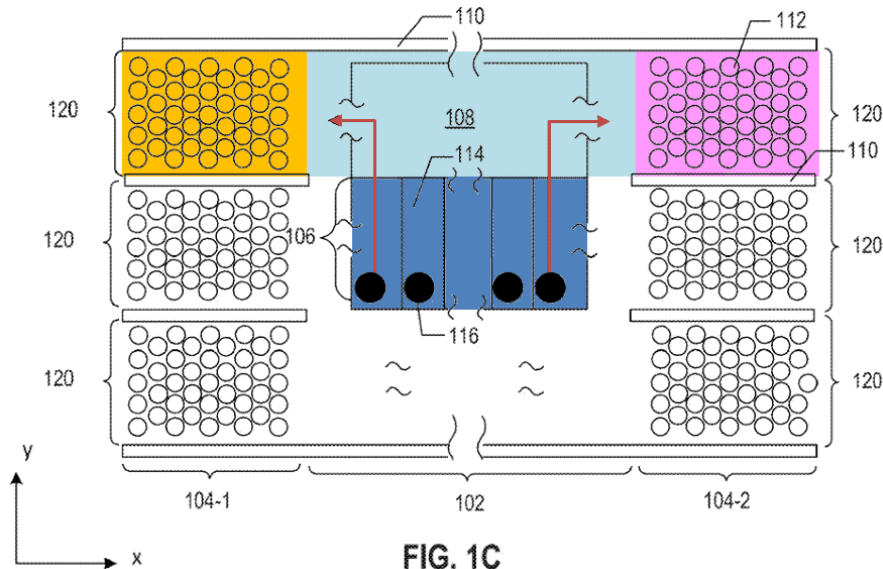


FIG. 1B

30. The bridge structure includes conductive layers (not shown in Figure 1B) that connect the staircase landing pads physically and electrically to memory array structures in both the positive x direction *and* the negative x direction. '604 patent 7:18-25; *see, e.g.*, Ex.1003 ¶ 121 (annotating Fig. 1B to add layers). For example, the top view of Figure 1C (shown below) shows that bridge structure 108 (turquoise) electrically connects (maroon arrows) conductive portions 114

(blue) of the stairs to memory structures 120 on the right (pink, positive x direction) and on the left (orange, negative x direction).



31. Without bridge structure 108, the conductive portions of the '604 patent's claimed staircase 116 would be electrically isolated because they do not extend from the memory cells like the prior art staircase structure discussed above in Section V. All '604 patent claims require that the width of the conductor portion of each step is "unchanged" along a "lateral direction perpendicular to" the lateral direction in which the plurality of stairs extend, which can help simplify formation of the stairstep (compared to designs of variable width) and its connection to the bridge structure. For example, if the plurality of stairs extends along the x-axis in Figures 1B and 1C, reproduced below, then the width of the conductor portion is unchanged along the y-axis, as annotated by the red arrows.

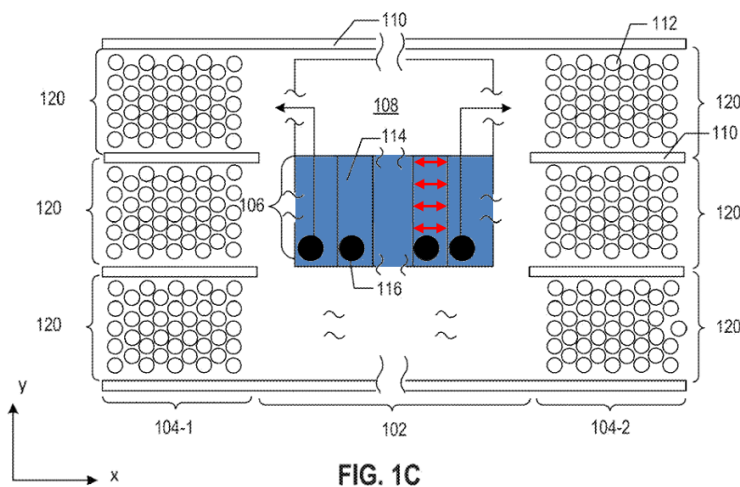


FIG. 1C

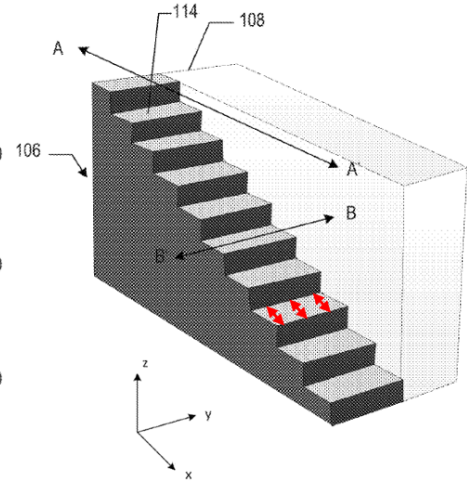


FIG. 1B

VII. A POSITA would not have found claims 1-5 and 8-13 obvious based on Grounds 1 or 2.

A. Overview of Thimmegowda

32. Thimmegowda discloses a 3D NAND memory structure that purports to reduce the number of staircases in the chip, but does not address the punch-through problem. Figure 3, annotated below, illustrates alternative conductor (blue) and dielectric (green) layers in a staircase structure. If over-etching (punch-through) occurs, the vias 334b-334d will contact a lower conductive portion (blue), resulting in a short circuit.

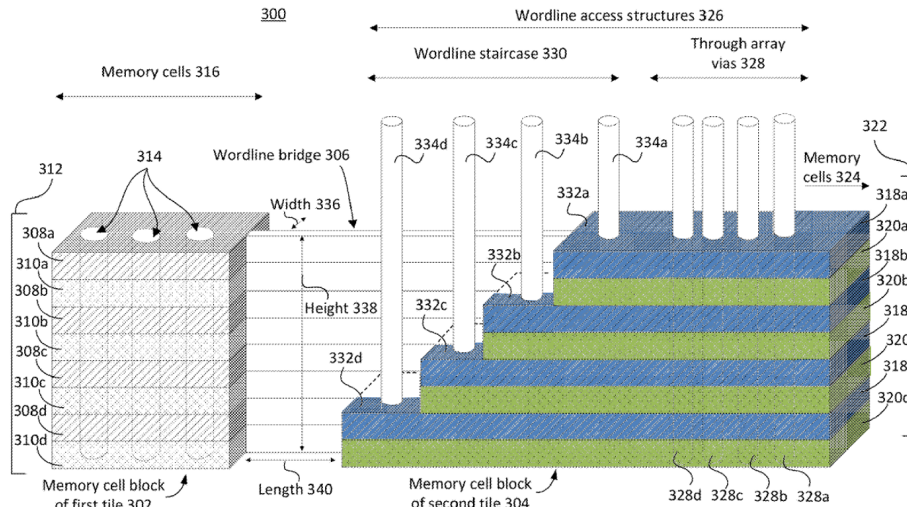


FIG. 3

33. Thimmegowda uses a wordline bridge 306 to connect staircase 330 to memory cells 316, such that the single staircase 330 can drive not only wordlines 318b-318d, but also 308b-308d. Unlike the bridge of the '604 patent, Thimmegowda's bridge does not run alongside the staircase, but rather runs up the middle of the staircase, extending from the end of the staircase to connect the staircase to *one* memory array (memory cells 316, or "memory cell block 302) in *one* direction (left, from the view in Figure 3).

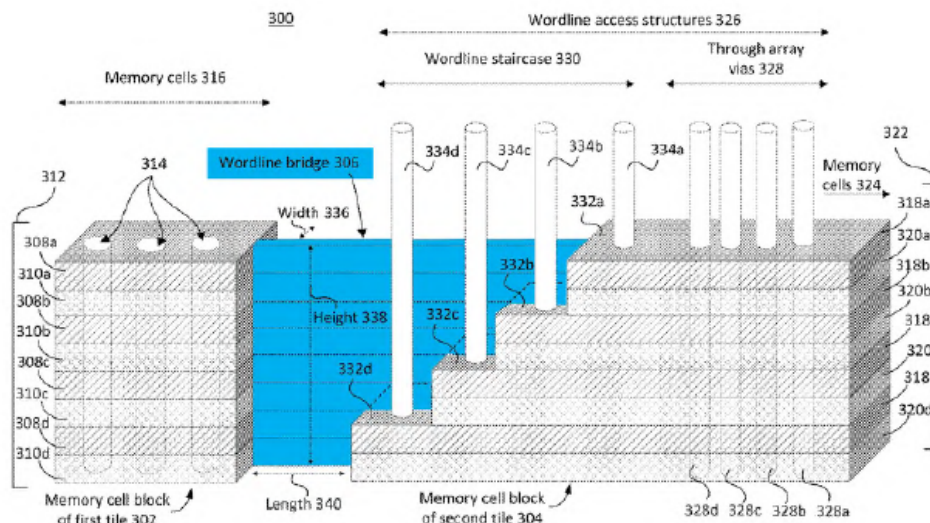


FIG. 3

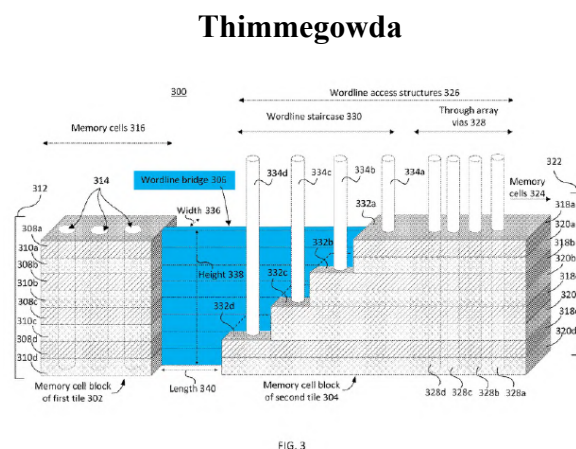
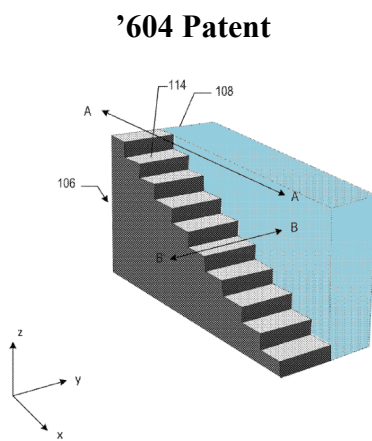
Ex.1003 ¶ 122 (annotating Thimmegowda Fig. 3)

34. The bridge structure does not connect the staircase to memory cells 324, or wordlines 318b-318d. Rather, the staircase would be connected to wordlines 318b-318d regardless of the wordline bridge 306. As shown in the annotation above, the stairsteps extend from (and therefore are directly connected to) word lines 318b-318d of the memory cell block 304 on the right of Figure 3. The bridge only provides the connection to memory cell block 302, on the left.

35. In this way, Thimmegowda's bridge is functionally and structurally different from the bridge disclosed in the '604 patent. The bridge in Figure 1B (annotated below) of the '604 patent provides a connection for each stairstep to wordlines in both directions. Structurally, the '604 patent discloses in Figure 1B a bridge running alongside the staircase in order to provide these connections.

36. In contrast, Thimmegowda's bridge only provides a connection to one set of wordlines in order to reduce the number of staircases, and it does so by running up the middle of the staircase. Thimmegowda states that increasing density of memory arrays meant "increase in size of the staircase," which "consumes silicon real estate and interferes with the goal of shrinking die sizes or increasing die densities." Thimmegowda 1:20-25; *see also* 2:28-34. As a means for reducing the number of staircases, Thimmegowda discloses a "wordline bridge that enables blocks of memory cells from one tile to share the wordline access structures of another tile," i.e., the "staircase structure." Thimmegowda 2:35-40.

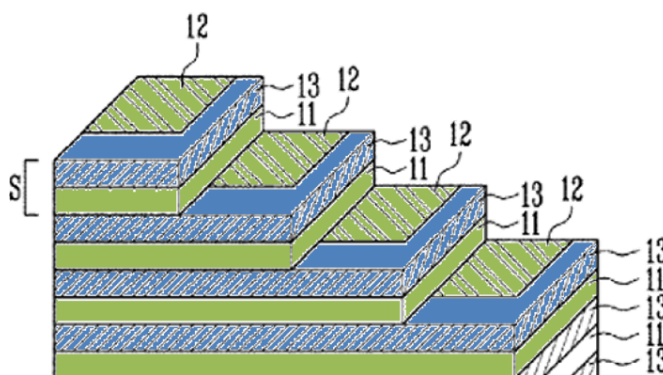
37. The figures below contrast the distinct structures of Figure 1B of the '604 patent (left) versus Figure 3 of Thimmegowda (right).



B. Overview of Lee and Kobayashi

38. Lee and Kobayashi both disclose similar staircase structures to address the punch-through problem. Unlike the staircase structure in the '604

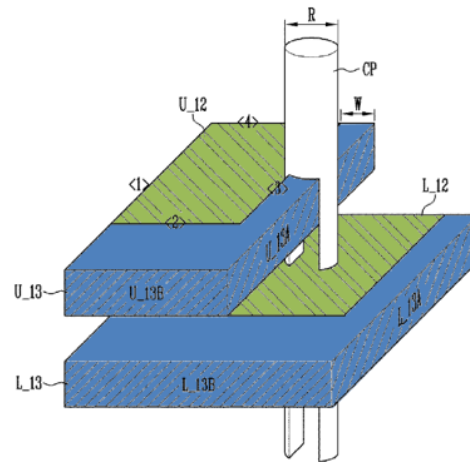
patent, each stairstep in Lee and Kobayashi has conductor portions with varying width and has no need for a bridge. The variable width of the conductor portion allows the conductor to connect to the memory structure. *See* Lee Abstract (disclosing an “interconnection structure” that includes “conductive layers . . . surrounding sidewalls of the dielectric layers”). For example, in Figure 1A of Lee, excerpted and annotated below, the conductor portion 13 (solid blue top with cross-hatched blue sidewall) has varying width in order to extend back towards the memory array, connecting the stairstep to the memory array.



Lee, Figure 1A (excerpt and annotated)

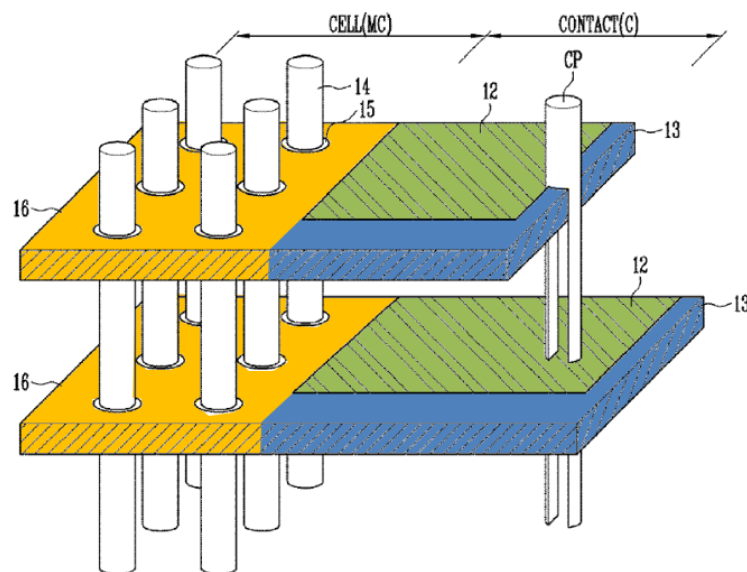
39. Figure 1B, annotated below, shows a closer view of the varying-width conductor portion on each step, with a via contact punching through to a lower step and the insulating layer 11 omitted for clarity.

FIG. 1B

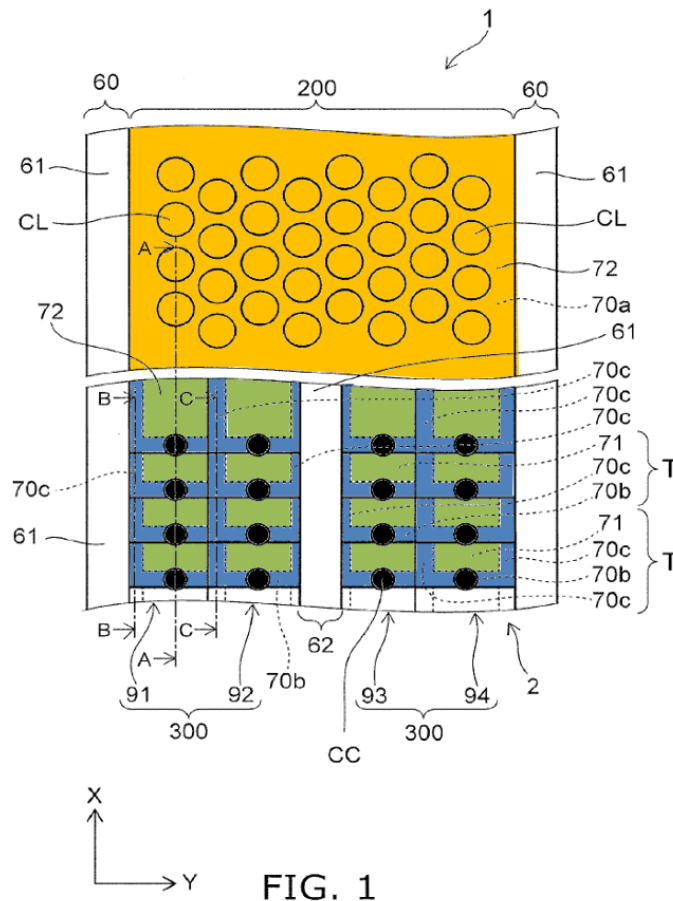
**Lee, Figure 1B (annotated)**

40. Figure 1C, annotated below, further illustrates that the conductor portion extends back to a memory cell structure, MC (orange). Lee [0032].

FIG. 1C

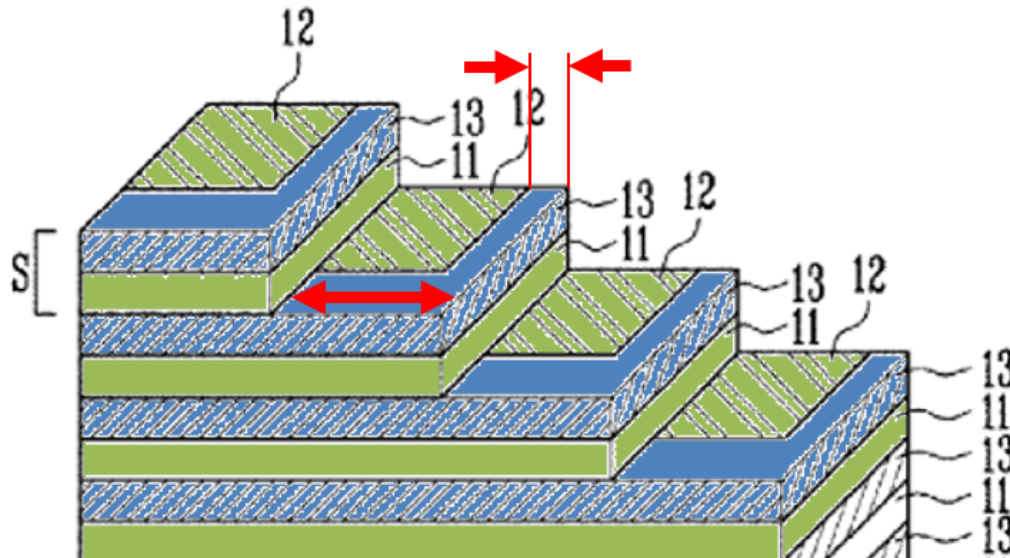


41. Kobayashi uses a similar design. Figure 1 of Kobayashi, annotated below, shows a top view of two double-staircase structures 300 with conductive portions (blue) that each extend back to connect to a block 200 (orange) of the memory cell array.



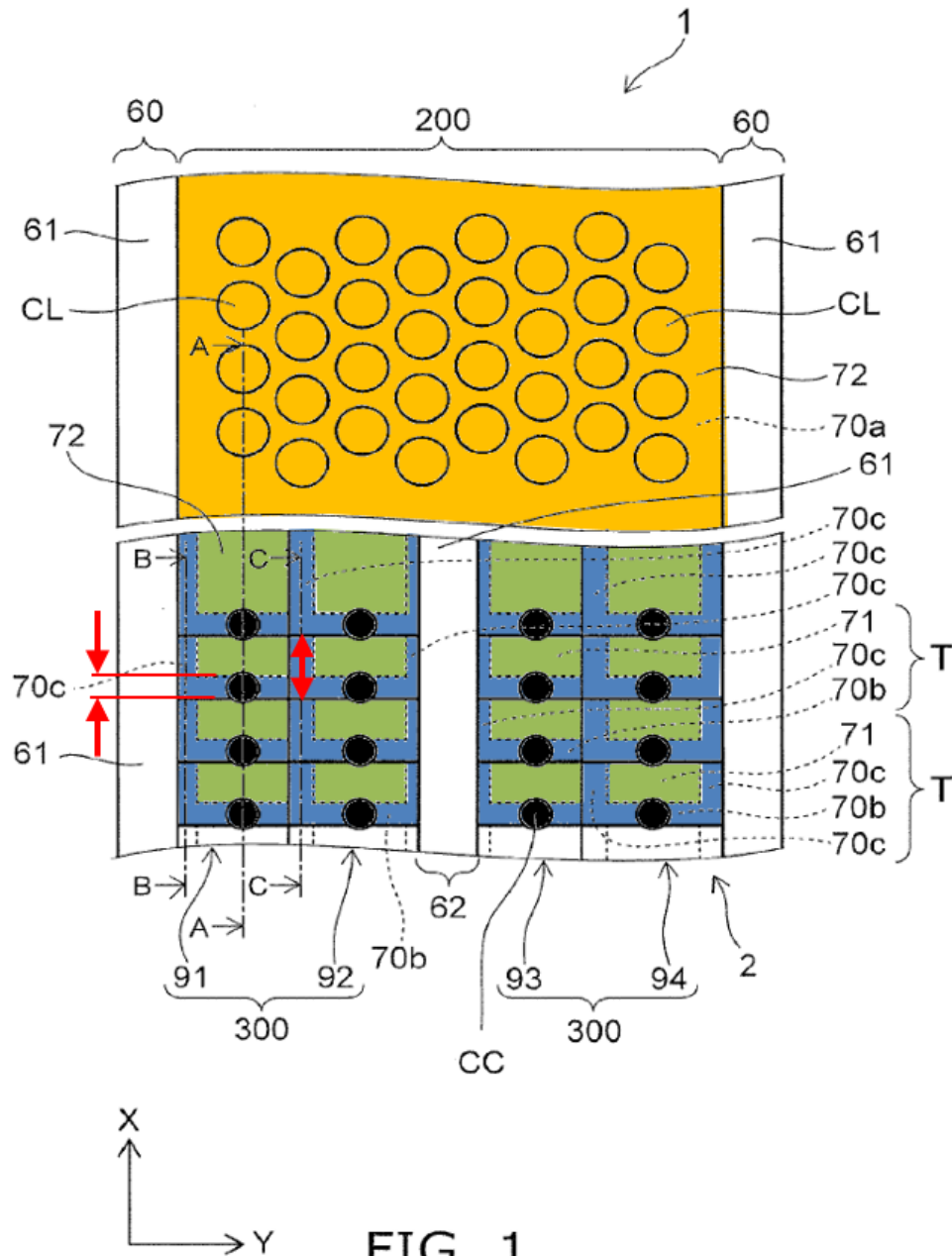
42. Unlike the '604 patent, the stairstep designs of Lee and Kobayashi require conductor portions that do *not* have an unchanged width. Instead, the conductor portions in both Lee and Kobayashi are deliberately designed to *change* widths in order to extend back and connect to the memory cell array. As shown by the red arrows in annotated Figure 1A of Lee, below, the conductor

portion has a narrower width at one end of the step, and a much wider width at the other end of the step.



Lee Fig. 1A (annotated)

The same is true for Kobayashi, as shown by the red arrows annotated Figure 1, below.



Kobayashi Fig. 1 (annotated)

C. A POSITA would not have combined Thimmegowda and Lee (Ground 1) or Kobayashi (Ground 2) in the proposed manner.

43. Dr. Banerjee's analysis is largely the same for Grounds 1 and 2, and thus I have considered them together. For example, Dr. Banerjee "focuses on the

combination of Thimmegowda's bridge and array architecture teachings that enable a single staircase to bidirectionally drive two arrays and Lee's stairstep teachings that mitigate punch through." Ex.1003 ¶ 102; *see also* Ex.1003 ¶ 167 ("My analysis focuses on the combination of Thimmegowda's bridge and array architecture and Kobayashi's stairstep teachings that mitigate punch through."). Specifically, Dr. Banerjee asserts that "[a] POSITA would have been motivated to apply Lee's teaching of non-overlapping fingers to mitigate the well-known punch through problem in Thimmegowda's staircase." Ex.1003 ¶ 103. Dr. Banerjee makes the same assertion for Kobayashi. Ex.1003 ¶ 168 ("A POSITA would have been motivated to apply Kobayashi's teaching of non-overlapping conductive fingers to mitigate the well-known punch through problem in Thimmegowda's staircase.").

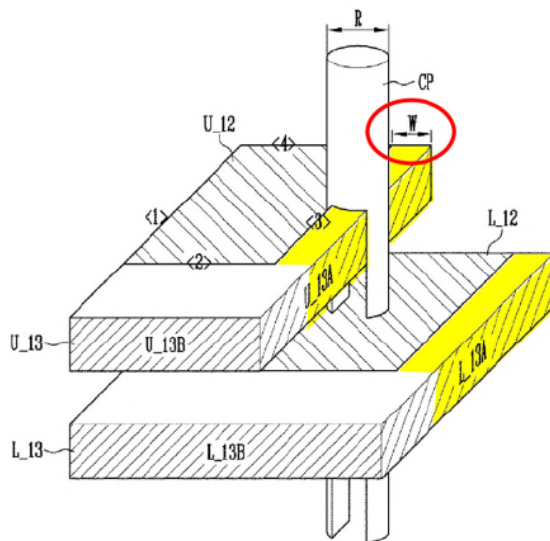
1. **A POSITA would not have been motivated to modify the stairsteps of Lee (Ground 1) or Kobayashi (Ground 2) to make "a width of the conductor portion [to be] unchanged" in the combination with Thimmegowda.**

44. As I discussed above in Section VII.B, Lee and Kobayashi's solution to the punch-through problem did not include stairsteps with conductive portions that have unchanged widths along the length of the step. Instead, both Lee and Kobayashi disclosed stairsteps with variable-length conductor portions that allowed the conductor to connect to a respective wordline.

45. In order to match the claims, Dr. Banerjee attempts to bypass this problem by incorporating only a “finger” portion of the Lee/Kobayashi staircase conductor in the combination references. Ex.1003 ¶ 103 (Lee), ¶ 168 (Kobayashi). In my opinion a POSITA would not have made such a modification of Lee and Kobayashi.

46. For both grounds, Dr. Banerjee asserts two alternative combinations. First, he asserts that a POSITA would have used a “thin finger” of Lee and Kobayashi as the “conductive portion” of a staircase (highlighted in yellow), with the remaining portion of the staircase being dielectric material, and apparently not using the rest of Lee/Kobayashi’s staircase conductor. Ex.1003 ¶¶ 105 (Lee), 169 (Kobayashi).

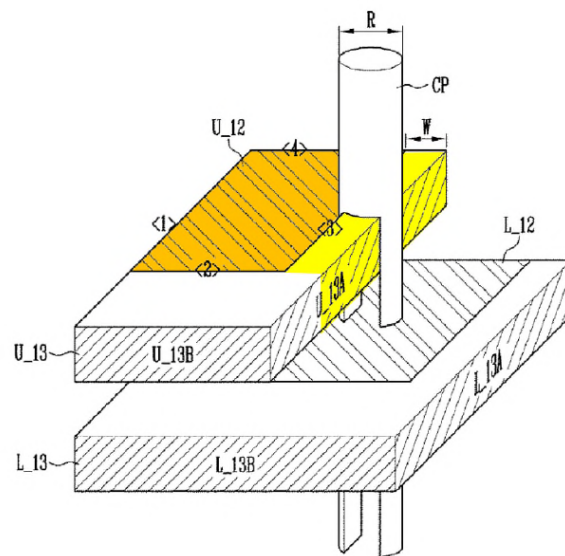
FIG. 1B



Ex.1003 ¶ 105 (annotating Lee Fig. 1B)

47. Below I reproduce Dr. Banerjee's annotations of the dielectric (orange) portions and conductive (yellow) portions of a staircase, taken from Lee (top) and Kobayashi (bottom).

FIG. 1B



Ex.1003 ¶ 139 (annotating Lee, Fig. 1B)

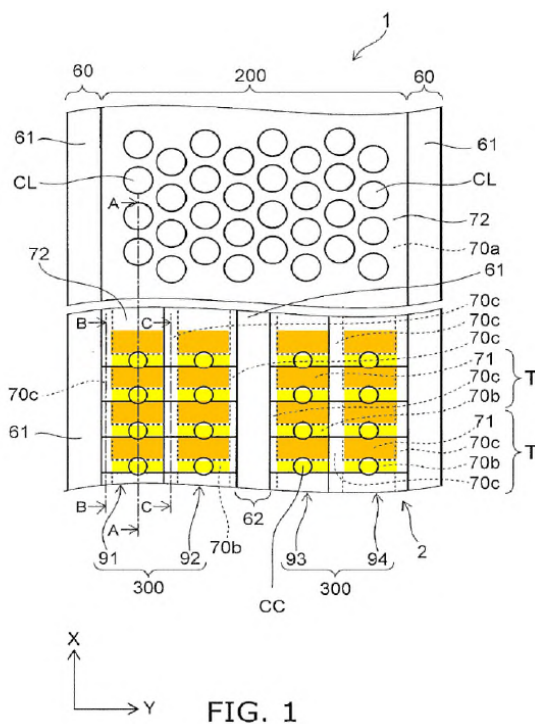


FIG. 1

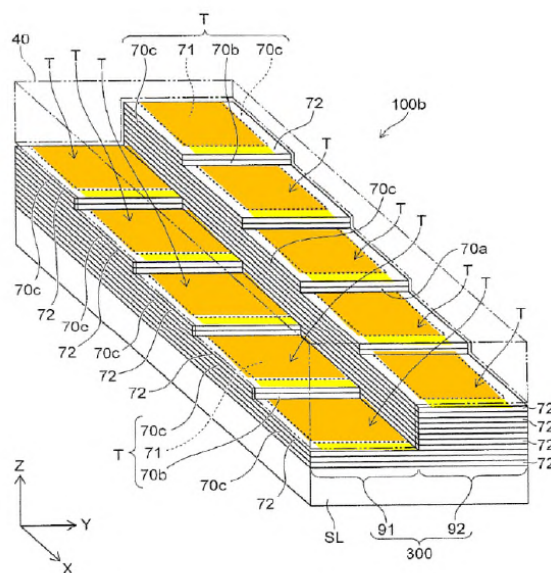
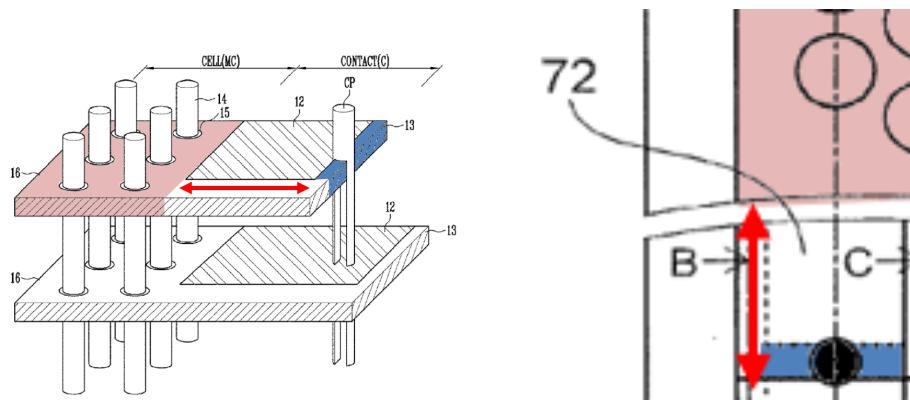


FIG. 5

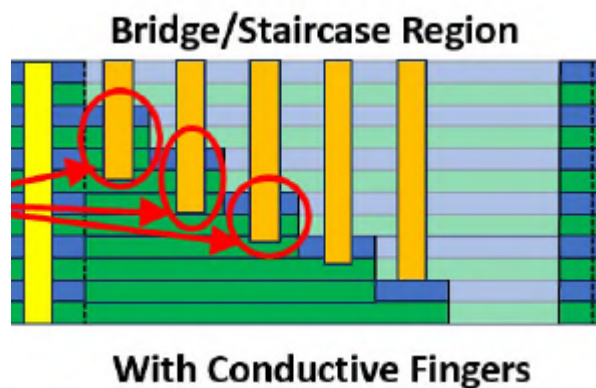
Ex.1003 ¶ 188 (annotating Kobayashi, Figs. 1 and 5)

48. A POSITA would not have picked only the highlighted conductor portions to combine with Thimmegowda. Specifically, the wider portions, which Dr. Banerjee discards, are required in both Lee and Kobayashi to electrically connect the landing portion (i.e., the portion that touches the contact) to the memory array. The figures below from Lee and Kobayashi have been annotated to show that omitting the wider conductor portions (uncolored with red arrow) results in a disconnect between the “thin fingers” (blue) and the memory array (pink), resulting in “floating” conductors and an inoperative device. (I discuss below that the combination with Thimmegowda does not account for this missing connection and would therefore be inoperable to drive the wordlines.)

FIG. 1C

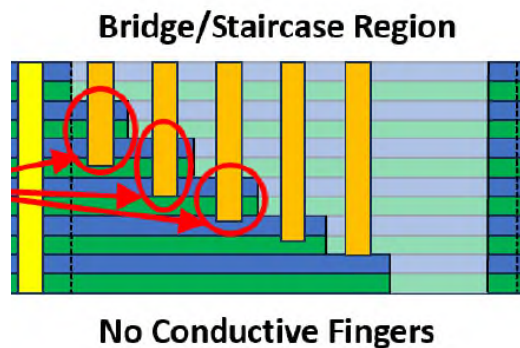
**Lee Fig. 1C (left) and Kobayashi Fig. 1 excerpt (right)**

49. Dr. Banerjee's second proposal is to "make the conductive finger cover the full width of the step." Ex.1003 ¶ 106 (Lee), ¶ 170 (Kobayashi). In this combination, like the "thin finger" proposal, Dr. Banerjee omits the portion of the Lee/Kobayashi conductor that connects to the memory cells. Below I have reproduced a portion of Dr. Banerjee's illustration of this combination.

**Ex.1003 ¶ 107 (excerpt)**

The conductive stairsteps are shown in blue, which is adjacent to a green dielectric material that runs underneath higher layers. Ex.1003 ¶ 109 ("[A]djacent

to each step (in the x-direction) is green dielectric material....”). Similar to the “thin finger” combination, the stairs are not connected to the wordlines/memory cells shown in blue on the far left of the figure. This is in contrast to Dr. Banerjee’s characterization of an unmodified Thimmegowda, reproduced below. Here, the staircase conductor extends all the way back to the memory array on the left side of the drawing, providing an electrical connection and allowing the contacts to drive the respective wordlines.



By removing the conductor, Dr. Banerjee’s combination renders this device inoperable for its intended purpose—i.e., it can no longer drive the wordlines.

2. A POSITA would not have been motivated to combine Thimmegowda’s bridge architecture with Lee or Kobayashi’s stairsteps.

50. Even if a POSITA cherry-picks only a “finger” portion of Lee/Kobayashi’s conductors, the POSITA would not have been motivated to apply that finger portion to Thimmegowda’s architecture because it would render Thimmegowda inoperable. Below I illustrate this principle as applied to

Thimmegowda's Figure 3. Here, the staircase includes a conductor (blue) along the full width, and it has a dielectric material (green) at the same level along the x-direction. But as shown by the red arrows, this dielectric material disconnects the staircase from the wordlines 318b, 318c, and 318d (pink). As such, the wordline staircase 330 does not drive the wordlines, rendering it inoperable for its intended purpose.

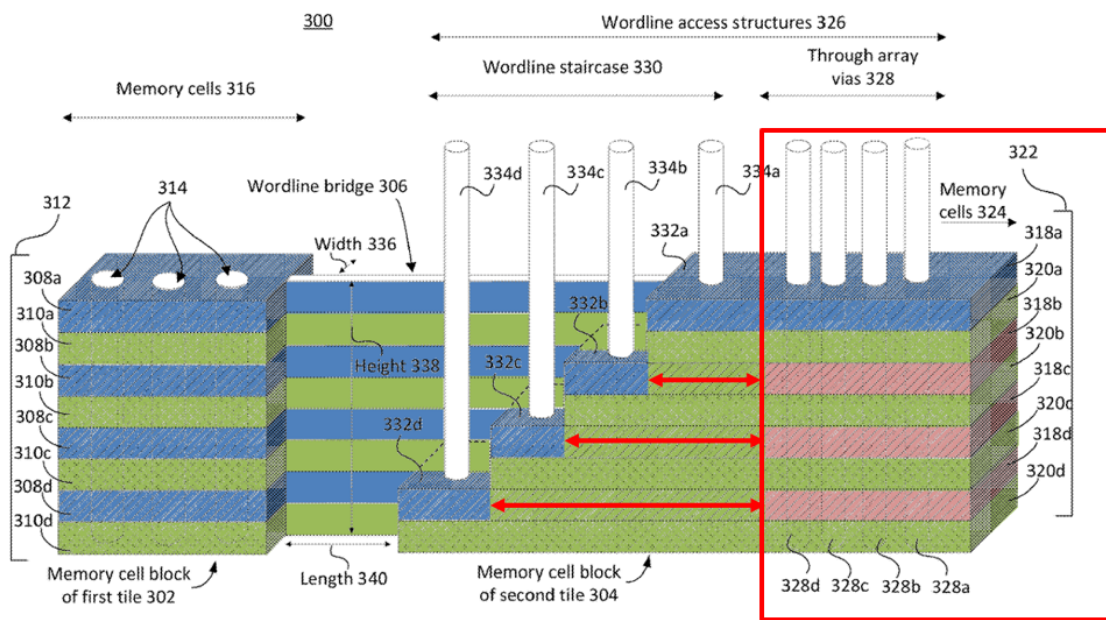


FIG. 3

51. Dr. Banerjee does not directly address the disconnection of the wordlines resulting from his proposed combinations. Where Dr. Banerjee describes the electrical coupling of wordlines, however, Dr. Banerjee either seems to assume that Thimmegowda's structure will somehow provide the electrical connection to wordlines 318b-318d. As discussed further below, however, Thimmegowda's structure *doesn't* provide any other electrical

connection to wordlines 318b-318d—it didn't need to because of the conductors that Dr. Banerjee explicitly removed in the combination when attempting to reconstruct the claims.

52. For example, Dr. Banerjee refers to “employing Thimmegowda’s *bidirectional bridge* teachings to Lee.” Ex.1003 ¶ 113. But as I explained above in Section VII.A, Thimmegowda’s *bridge* is *not* bidirectional. To the contrary, and as shown below in annotated Thimmegowda Figure 3, Thimmegowda’s bridge only provides a connection to wordlines in one direction (to the left, in Figure 3).

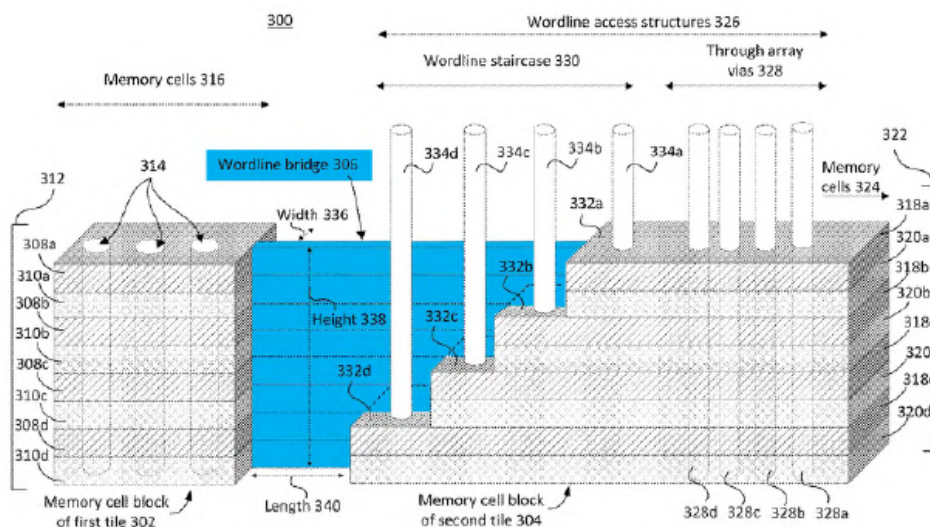


FIG. 3

In the other direction (to the right in Figure 3), Thimmegowda’s wordlines are connected to the stairstep by conductive layers that Dr. Banerjee explicitly removes in his combination—and Dr. Banerjee does not describe or motivate any

modification of Thimmegowda to account for this removal. Thus, although Thimmegowda's staircase can drive memory arrays in two directions, the bridge structure does not connect the stairsteps to the memory array to the right of the Thimmegowda staircase, comprising word lines 318b-318d, as shown boxed in red below.

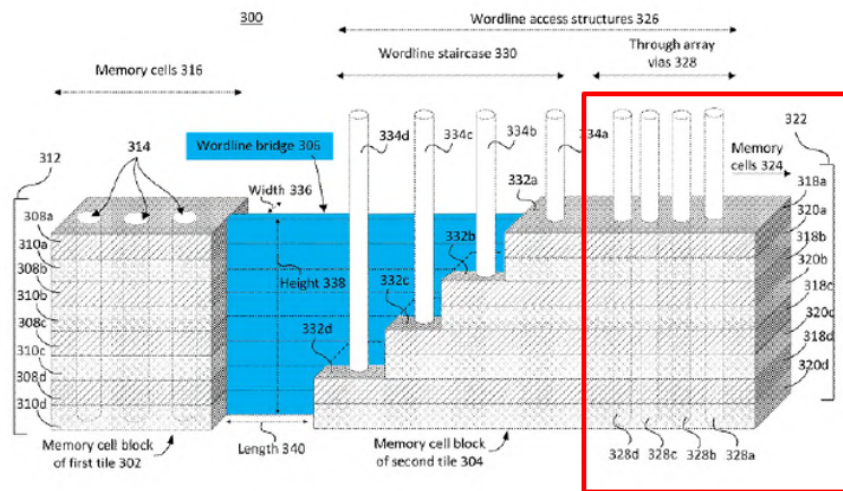


FIG. 3

53. Despite Thimmegowda clearly illustrating wordline bridge 306 as running up the middle of the staircase 330, Dr. Banerjee asserts that in Figure 3, “the bridge extends to the back side of the staircase (going into the page in the Y-direction), and thus the gate layers in each array on the left and right electrically couple together. In other words, behind the staircase (in the Y direction) the bridge extends to both memory blocks.” Ex.1003 ¶ 122. I disagree. Dr. Banerjee seems to be trying to make Thimmegowda's bridge equivalent to the bridge

disclosed in Figure 1B of the '604 patent (below), which runs bidirectionally alongside the staircase as I discussed above in Section VI.

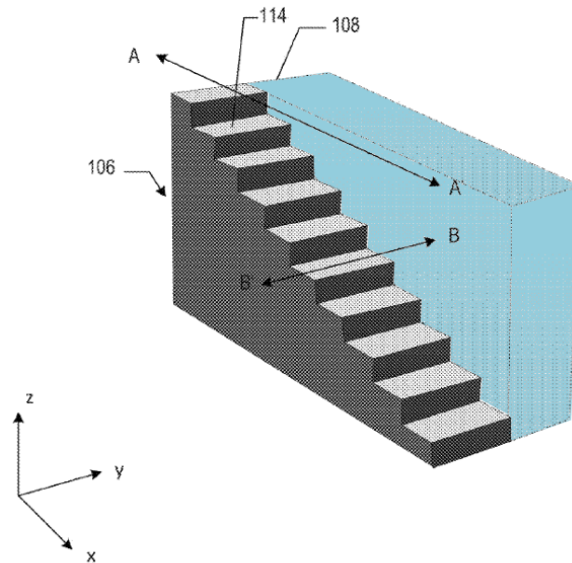


FIG. 1B

'604 Patent, Fig. 1B

But Thimmegowda's bridge is not the same as the Figure 1B bridge in the '604 patent, because Thimmegowda's bridge only needs to connect the staircase in one direction. Dr. Banerjee's own annotation of Figure 3, reproduced below, clearly shows the bridge running up the middle of the staircase and not extending "to the back side of the staircase (going into the page in the Y-direction)." Ex.1003

¶ 122.

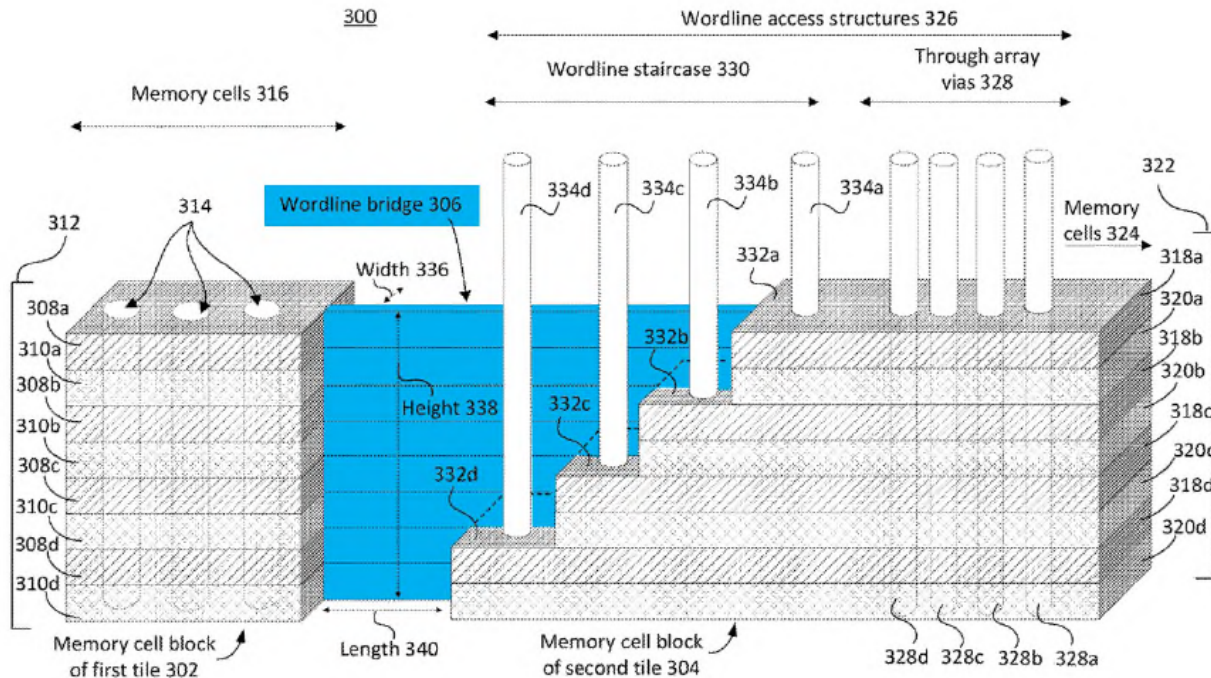


FIG. 3

Ex.1003 ¶ 122 (annotating Thimmegowda Fig. 3)

Dr. Banerjee further cites to Thimmegowda's Figures 1 and 2 as "showing wordline bridge in electrical and physical contact with two memory arrays."

Ex.1003 ¶ 122. I disagree. Figures 1 and 2 are high-level diagrams that do not show "physical contact." Nevertheless, neither figure shows the wordline bridge connecting "to the back of the staircase." The only figure that shows details of the actual connections between a staircase and memory cells is Figure 3, which Dr. Banerjee mischaracterizes as discussed above.

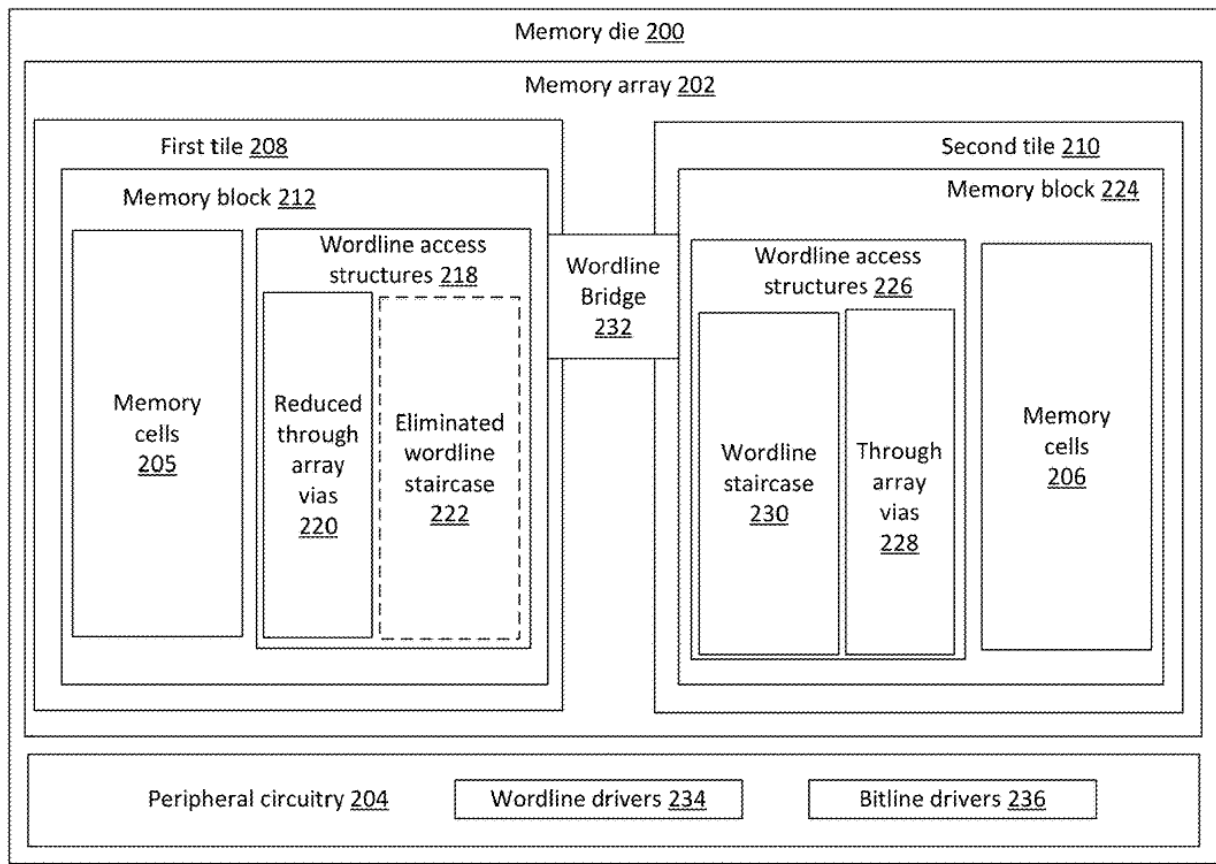


FIG. 2

54. Thus, as shown below, replacing Thimmegowda's conductors with dielectric material (green) next to each staircase leaves the so-called "conductive fingers" (blue) of Dr. Banerjee's proposed combinations electrically and physically isolated from the memory cells to the right of the staircase (shown boxed in red). This is true in both proposed combinations. Wordlines 318b-318d would be cutoff from the staircase structure, thus not allowing them to be driven by the contacts 334b-334d and rendering them (and the memory cells they control) inoperable.

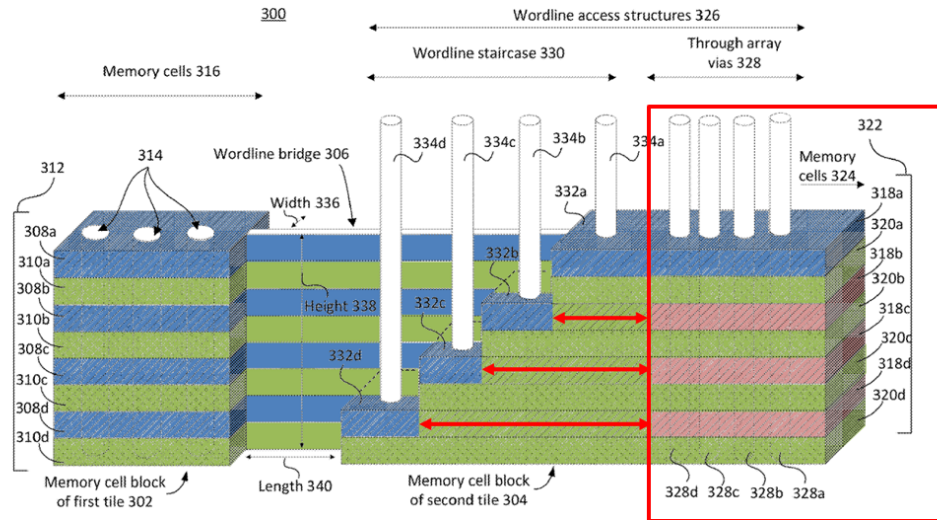


FIG. 3

VIII. CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on February 21, 2025, in Pasadena, CA.

A handwritten signature in black ink, appearing to read 'Konstantinos Giapis', written over a horizontal line.

Konstantinos Giapis