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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/746,333	12/23/2003	Richard V. Orlando	PHL19002USU	3420
8791	7590	11/17/2023		
WOMBLE BOND DICKINSON (US) LLP			EXAMINER	
ATTN: IP DOCKETING			SHENG, TOM V	
P.O. Box 570489				
ATLANTA, GA 30357-0037				
			ART UNIT	PAPER NUMBER
			2628	
			NOTIFICATION DATE	DELIVERY MODE
			11/17/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing@wbd-us.com



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Patent No. 7,233,305

Issue Date: June 19, 2007

Application No. 10/746,333

Filing or 371(c) Date: December 23, 2003

Attorney Docket No. **PHL19002USU**

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DECISION ON PETITION

This is a Notice regarding the request for acceptance of a fee deficiency submission under 37 CFR 1.28(c) filed October 5, 2023.

The Office no longer investigates or rejects original or reissue applications under 37 CFR 1.56. 1098 Off. Gaz. Pat. Office 502 (January 3, 1989). Therefore, nothing in this Notice is intended to imply that an investigation was done.

The fee deficiency submission under 37 CFR 1.28(c) is **ACCEPTED**. Accordingly, status as a small entity has been removed and any future fee(s) submitted must be paid at the undiscounted rate.

Inquiries related to this communication should be directed to the undersigned at (571) 272-0986.

/FELICIA ALLEN-JENKINS/
Paralegal Specialist, OPET



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/746,333	12/23/2003	Richard V. Orlando	PHL19002USU

CONFIRMATION NO. 3420

POWER OF ATTORNEY NOTICE



OC000000063282002

116438
Apogee Law Group
26895 Aliso Creek Road
Suite 104
Aliso Viejo, CA 92656

Date Mailed: 10/17/2023

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/06/2023.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/dmbaines/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/746,333	12/23/2003	Richard V. Orlando	PHL19002USU

CONFIRMATION NO. 3420

POA ACCEPTANCE LETTER



OC00000063282059

8791
WOMBLE BOND DICKINSON (US) LLP
ATTN: IP DOCKETING
P.O. Box 570489
ATLANTA, GA 30357-0037

Date Mailed: 10/17/2023

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/06/2023.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/dmbaines/

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**PATENT - POWER OF ATTORNEY
OR
REVOCATION OF POWER OF ATTORNEY
WITH A NEW POWER OF ATTORNEY
AND
CHANGE OF CORRESPONDENCE ADDRESS**

Patent Number	7,233,205
Issue Date	June 19, 2007
First Named Inventor	Richard V. ORLANDO
Title	GAMMA REFERENCE VOLTAGE GENERATOR
Attorney Docket No.	115G13P001

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR
☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

8791

OR
☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or
☐ Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the:

☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/AIA/96) submitted herewith or filed on _____

SIGNATURE of Applicant or Patent Owner

Signature

Name

Date

Telephone

Title and Company

PHENIX LERNERHORN LLC

NOTE: Signatures of all the applicants or patent owners of the entire interest of their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☒ A total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	48691075
Application Number:	10746333
International Application Number:	
Confirmation Number:	3420
Title of Invention:	GAMMA REFERENCE VOLTAGE GENERATOR
First Named Inventor/Applicant Name:	Richard V. Orlando
Customer Number:	116438
Filer:	Lester Vincent/Linda Quintana
Filer Authorized By:	Lester Vincent
Attorney Docket Number:	PHL19002USU
Receipt Date:	06-OCT-2023
Filing Date:	23-DEC-2003
Time Stamp:	17:31:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73	115013P001_373cStatement-AppendixA.pdf	2004400	no	4
			ff9c460ef465e925744f0b99ffb583ea51ce3ce		

Warnings:

Information:					
2	Power of Attorney	PhenixLonghornP001POAExecuted.pdf	654724	no	1
			195a0ee0b7335f64aa7eb7ae2d5a97bbd28b994d		
Warnings:					
Information:					
Total Files Size (in bytes):				2659124	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: PHENIX LONGHORN, LLCApplication No./Patent No.: 7,233,305Filed/Issue Date: June 19, 2007Titled: GAMMA REFERENCE VOLTAGE GENERATORPHENIX LONGHORN, LLC, a company

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Richard V. ORLANDO and Trevor A. BLYTH To: ALTA ANALOG, INC.The document was recorded in the United States Patent and Trademark Office at
Reel 014849, Frame 0662, or for which a copy thereof is attached.2. From: ALTA ANALOG, INC. To: COMERICA BANKThe document was recorded in the United States Patent and Trademark Office at
Reel 024630, Frame 0270, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Innolux Corporation Exhibit 1002, Page 8

STATEMENT UNDER 37 CFR 3.73(c)

3. From: ALTA ANALOG, INC. To: Richard ORLANDO and AVM CAPITAL LP

The document was recorded in the United States Patent and Trademark Office at
Reel 033360, Frame 0474, or for which a copy thereof is attached.

4. From: AVM CAPITAL LP To: Maury DOMENGEAUX

The document was recorded in the United States Patent and Trademark Office at
Reel 036114, Frame 0576, or for which a copy thereof is attached.

5. From: ALTA ANALOG, INC. To: Richard V. ORLANDO and AVM CAPITAL LP

The document was recorded in the United States Patent and Trademark Office at
Reel 036142, Frame 0214, or for which a copy thereof is attached.

6. From: COMERICA BANK To: ALTA ANALOG, INC.

The document was recorded in the United States Patent and Trademark Office at
Reel 036067, Frame 0288, or for which a copy thereof is attached.

☒ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Lester J. Vincent/

Signature

Lester J. Vincent

Printed or Typed Name

October 6, 2023

Date

31,460

Title or Registration Number

APPENDIX A TO STATEMENT UNDER 37 CFR 3.73(c)

A chain of title of the patent application/patent identified above to the current assignee (continued):

7. From: Richard V. ORLANDO and Maury DOMENGEAUX To: PHENIX, LLC

The document was recorded in the United States Patent and Trademark Office at

Reel 036114, Frame 0930, or for which a copy thereof is attached.

8. From: AVM CAPITAL LP To: Maury DOMENGEAUX

The document was recorded in the United States Patent and Trademark Office at

Reel 037961, Frame 0726, or for which a copy thereof is attached.

9. From: ALTA ANALOG, INC. To: Richard V. ORLANDO and AVM CAPITAL LP

The document was recorded in the United States Patent and Trademark Office at

Reel 037960, Frame 0875, or for which a copy thereof is attached.

10. From: Richard V. ORLANDO and Maury DOMENGEAUX To: PHENIX, LLC

The document was recorded in the United States Patent and Trademark Office at

Reel 037961, Frame 0718, or for which a copy thereof is attached.

11. From: PHENIX, LLC To: PHENIX LONGHORN, LLC

The document was recorded in the United States Patent and Trademark Office at

Reel 040834, Frame 0069, or for which a copy thereof is attached.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

CERTIFICATE OF EFS-WEB TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Linda Quintana
(Name)

/Linda Quintana/
(Signature)

October 5, 2023
(Date)

Attorney Docket No.: 115013P001

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor : Richard V. ORLANDO
Appl. No. : 10/746,333
Filed : December 23, 2003
For : GAMMA REFERENCE
VOLTAGE GENERATOR
U.S. Patent No. : 7,233,305

Examiner: Tom V. SHENG
Art Unit: 2628
Confirmation No.: 3420

E-Filed via EFS Web
Mail Stop: Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION UNDER 37 CFR 1.28(C) FOR FEE DEFICIENCY PAYMENT

Petition Examiner:

I. Notification of Loss of Small Entity Status

Patentee hereby notifies the United States Patent and Trademark Office (PTO) that small entity status is no longer appropriate for this patent. Patentee asserts that Patentee will pay undiscounted fees for this patent.

II. Fee Deficiency Payment

Patentee asserts that small entity status was previously established in good faith and that the PTO was through error not notified of a loss of small entity status. See 37 CFR 1.28(c).

Pursuant to 37 CFR § 1.28(c), please charge our Deposit Account No. 09-0528 in the amount of the fee deficiency, representing the difference in fees originally paid as a small entity and the current large-entity fees. The following chart itemizes the amounts for the above-identified patent and sets forth the total deficiency owed.

III. Chart of Itemization of Fee Deficiency Owed

Fee Description or Type	Current Fee Amount	Amount Previously Paid	Date Previously Paid	Deficiency Owed
11.5 Year Maintenance Fee	\$7,700.00	\$3,700.00	11/13/2018	\$4,000.00
Total Deficiency Owed (sum of all entries in "Deficiency Owed" column)				\$4,000.00

Please charge the total fee deficiency owed of \$4,000.00 to Deposit Account No. 09-0528.

If there are any additional fees owed, please charge Deposit Account No. 09-0528.

Respectfully submitted,

WOMBLE BOND DICKINSON (US) LLP

Date: October 5, 2023

/Lester J. Vincent/
Lester J. Vincent
Reg. No. 31,460

Attn: IP Docketing
P.O. Box 570489
Atlanta, GA 30357
(408) 720-8300

Electronic Acknowledgement Receipt

EFS ID:	48686564
Application Number:	10746333
International Application Number:	
Confirmation Number:	3420
Title of Invention:	GAMMA REFERENCE VOLTAGE GENERATOR
First Named Inventor/Applicant Name:	Richard V. Orlando
Customer Number:	116438
Filer:	Lester Vincent/Linda Quintana
Filer Authorized By:	Lester Vincent
Attorney Docket Number:	PHL19002USU
Receipt Date:	05-OCT-2023
Filing Date:	23-DEC-2003
Time Stamp:	19:28:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition for review by the Office of Petitions	115013P001_PetitionForFeeDeficiencyPayment.pdf	215684	no	2
			6b3535054c7366921c30686f1dfd542a34c174f4		

Warnings:

Information:	
Total Files Size (in bytes):	215684
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 2:18-cv-00020	DATE FILED 1/22/2018	U.S. DISTRICT COURT Eastern District of Texas, Marshall Division
PLAINTIFF PHENIX LONGHORN, LLC		DEFENDANT TEXAS INSTRUMENTS, INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,233,305	6/19/2007	Phenix Longhorn, LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT ORDERED that all of Phenix's claims against TI in Case No. 2:18-cv-00020 are DISMISSED WITH PREJUDICE. It is further ORDERED that all of TI's counterclaims against Phenix in Case No. 2:18-cv-00020 are DISMISSED WITHOUT PREJUDICE.
--

CLERK <i>David A. O'Toole</i>	(BY) DEPUTY CLERK	DATE 8/27/19
----------------------------------	-------------------	------------------------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

Innolux Corporation Exhibit 1002, Page 16

Print

Save As...

Reset

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 2:17-cv-00711	DATE FILED 10/25/2017	U.S. DISTRICT COURT Eastern District of Texas, Marshall Division
PLAINTIFF PHENIX LONGHORN, LLC		DEFENDANT WISTRON CORPORATION
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,233,305	6/19/2007	Phenix Longhorn, LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT ORDERED that all of Phenix's claims against Wistron Corporation in Civil Action No. 2:17-CV-00711-RWS are hereby DISMISSED WITH PREJUDICE. It is further ORDERED that all of Wistron's counterclaims against Phenix in Civil Action No. 2:17-CV-00711-RWS are hereby DISMISSED WITH PREJUDICE. I

CLERK <i>David A. O'Toole</i>	(BY) DEPUTY CLERK ch	DATE 9/9/19
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Format m/d/yyyy

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

Innolux Corporation Exhibit 1002, Page 17

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/746,333	12/23/2003	Richard V. Orlando	ALTA-P007

PHENIX LONGHORN, LLC
2325 OAK ALLEY
TYLER, TX 75703

CONFIRMATION NO. 3420
POWER OF ATTORNEY NOTICE



Date Mailed: 02/22/2019

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/15/2019.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/deelliott/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/746,333	12/23/2003	Richard V. Orlando	

116438
Apogee Law Group
26895 Aliso Creek Road
Suite 104
Aliso Viejo, CA 92656

CONFIRMATION NO. 3420
POA ACCEPTANCE LETTER



Date Mailed: 02/22/2019

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/15/2019.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/deelliott/

Under the Paperwork Reduction Act of 1995, no person is required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 116438

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒ The address associated with Customer Number: 116438

OR

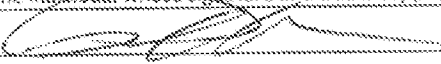
Firm or individual name		
Address		
City	State	Zip
Country		
Telephone		Email

Assignee name and address: Phenix Longhorn, LLC, 2325 Oak Alley, Tyler, TX 75703

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature 	Date 2/14/19
Name Richard V. Orlando	Telephone (408) 499-8455
Title President - Phenix Longhorn, LLC	

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 18 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Phenix Longhorn, LLCApplication No./Patent No.: 10/746,333 / 7,233,305Filed/Issue Date: 12/23/03 / 6/19/07Titled: Gamma Reference Voltage GeneratorPhenix Longhorn LLC, a Limited Liability Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Orlando, Richard V & Blyth, Trevor A To: Alta Analog, IncThe document was recorded in the United States Patent and Trademark Office at
Reel 014849, Frame 0662, or for which a copy thereof is attached.2. From: Alta Analog, Inc. To: Comerica BankThe document was recorded in the United States Patent and Trademark Office at
Reel 024630, Frame 0270, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Innolux Corporation Exhibit 1002, Page 21

STATEMENT UNDER 37 CFR 3.73(c)

3. From: Alta Analog, Inc To: Orlando, Richard

The document was recorded in the United States Patent and Trademark Office at
Reel 033360, Frame 0474, or for which a copy thereof is attached.

4. From: AVM Capital LP To: Domengeaux, Maury

The document was recorded in the United States Patent and Trademark Office at
Reel 036114, Frame 0576, or for which a copy thereof is attached.

5. From: Alta Analog, Inc. To: Orlando, Richard

The document was recorded in the United States Patent and Trademark Office at
Reel 036142, Frame 0214, or for which a copy thereof is attached.

6. From: Comerica Bank To: Alta Analog, Inc.

The document was recorded in the United States Patent and Trademark Office at
Reel 036067, Frame 0288, or for which a copy thereof is attached.

☒ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Francisco A. Rubio-Campos, Reg. No. 45,358/

2/14/19

Signature

Date

Francisco A. Rubio-Campos

USPTO Reg. No. 45,358

Printed or Typed Name

Title or Registration Number

STATEMENT UNDER 37 CFR 3.73(c)
(Continued)

7. From: Orlando, Richard & Domengeaux, Maury
To: Phenix LLC

The document was recorded in the United States Patent and Trademark Office at
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8. From: AVM Capital, LP
To: Domengeaux, Maury

The document was recorded in the United States Patent and Trademark Office at
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9. From: Alta Analog, Inc.
To: Orlando, Richard

The document was recorded in the United States Patent and Trademark Office at
Reel: 037960, Frame: 0875

10. From: Orlando, Richard
To: Phenix, LLC

The document was recorded in the United States Patent and Trademark Office at
Reel: 037961, Frame: 0718

11. From: Phenix, LLC
To: Phenix Longhorn , LLC

The document was recorded in the United States Patent and Trademark Office at
Reel: 040834, Frame: 0069

Electronic Acknowledgement Receipt

EFS ID:	35159423
Application Number:	10746333
International Application Number:	
Confirmation Number:	3420
Title of Invention:	GAMMA REFERENCE VOLTAGE GENERATOR
First Named Inventor/Applicant Name:	Richard V. Orlando
Correspondence Address:	PHENIX LONGHORN, LLC - 2325 OAK ALLEY - TYLER TX 75703 US - -
Filer:	Francisco A. Rubio-Campos
Filer Authorized By:	
Attorney Docket Number:	ALTA-P007
Receipt Date:	15-FEB-2019
Filing Date:	23-DEC-2003
Time Stamp:	00:06:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	PLL19003USU_POA.pdf	365539	no	1
			2ba963a19a9c1b67d8c0e01bc22b25f3af304464		
Warnings:					
Information:					
2	Assignee showing of ownership per 37 CFR 3.73	PLL19003USU_37CFR3-37.pdf	2618609	no	3
			7bf485475342136827d9c786a45d69e4584acb75		
Warnings:					
Information:					
Total Files Size (in bytes):			2984148		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WISTRON CORPORATION,
Petitioner,

v.

PHENIX LONGHORN, LLC,
Patent Owner.

Case IPR2018-01255
Patent 7,233,305 B1

Before DENISE M. POTHIER, DAVID C. McKONE, and
KAMRAN JIVANI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314(a)

I. INTRODUCTION

Wistron Corporation (“Petitioner”)¹ filed a Petition requesting an *inter partes* review of claims 1, 2, 4, and 5 of U.S. Patent No. 7,233,305 B1 (Ex. 1001, “the ’305 patent”). Paper 1 (“Pet.”), 1. Phenix Longhorn, LLC (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 10 (“Prelim. Resp.”). Patent Owner filed two, separate motions to seal Exhibits 2001 and 2009 as well as its Preliminary Response, each in its entirety. Papers 7, 11. These motions will be addressed in a separate order.²

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons stated below, we determine that the “information presented” does not “show[] there is a reasonable likelihood that . . . [P]etitioner would prevail with respect to at least 1 of the claims challenged.” *See id.* Accordingly, we do “not authorize an *inter partes* review to be instituted.” *See id.*

A. Related Proceedings

Petitioner and Patent Owner submit the ’305 patent is presently being asserted against Petitioner in Eastern District of Texas Case No. 2:17:cv-00711-RWS and against Texas Instruments in Eastern District of Texas Case

¹ Petitioner Wistron Corporation identifies itself as a real party-in-interest and states Wistron InfoComm (Zhongshan) Corporation, Zhongshan Torch Development Zone, and Wistron Mexico S.A. de C.V. “may be real parties-in-interest.” Paper 3, 2.

² This Decision does not reproduce or discuss any material the Motions to Seal identify as confidential. Accordingly, this Decision need not be sealed.

No. 2:18-cv-00020-RWS. Pet. viii; Paper 4, 2.³ Petitioner also identifies two actions in which Patent Owner asserted the '305 patent against multiple parties. Pet. viii..

B. The '305 Patent

The '305 patent is titled “Gamma Reference Voltage Generator” and is used with Liquid Crystal Displays (LCDs). Ex. 1001, Title, 1:12–14. Petitioner explains the brightness versus input voltage curve for a display’s image does not match those of a human’s vision and establishes a non-linear behavior called “gamma.” See Pet. 1–2 (citing Ex. 1002 ¶ 25); see also Pet. 2–3 (reproducing Ex. 1008, Fig. 6); see also Prelim. Resp. 5 (stating “the brightness of the LCD pixel is not a linear or straight-line function of the voltages applied” and “the human eye’s sensitivity to light is also not linear”) Due to this mismatch, the curve needs to be adjusted using gamma correction. See Pet. 1–2 (citing Ex. 1002 ¶ 25); see also Prelim. Resp. 5 (discussing controlling gamma reference voltages). The '305 patent indicates gamma correction has been a problem for Thin Film Transistor (TFT) flat panel displays. Ex. 1001, 1:19–21. Often, each display has a different response to the gamma correction reference voltages, which results in a need to generate specific gamma reference voltages for each display’s model. Ex. 1001, 1:22–25.

Traditionally, this problem has been solved using Select-On-Test Resistors, allowing reference voltages (e.g., GM_{1-16} of Fig. 1) to be fine-tuned to the display’s requirements using specific resistors (e.g., R_{1-17} of Fig. 1). Ex. 1001, 1:27–34, 1:46–2:3, Fig. 1. However, this process

³ Patent Owner mistakenly lists “2:18-cv-00720-RWS” rather than 2:18-cv-00020-RWS.

prohibits automatic assembly and testing and requires resistors to be tested, selected, and mounted manually. Ex. 1001, 1:31–34. The '305 patent's invention is “a programmable buffer integrated circuit which can be programmed to output a set of gamma correction reference voltages to be used in Liquid Crystal Displays (LCDs).” Ex. 1001, 2:16–19; *see also id.* at 2:45–51, Figs. 2–3. The described invention includes “automated assembly of an entire PC board” (Ex. 1001, 2:29–30), “automated test and gamma adjustment” (Ex. 1001, 2:30–31, 3:38–41, Fig. 2), and reprogramming gamma characteristics using gamma reference controllers (e.g., 210 and 220) (Ex. 1001, 2:32–33, 3:41–47, Fig. 2).

The '305 patent further states that the integrated circuit can store and retrieve reference voltages' banks using address inputs B0, B1, and B2. Ex. 1001, 5:50–53, 6:41. These inputs allow gamma voltages to be changed and can be used to switch between different gamma settings. Ex. 1001, 5:53–62, Fig. 6. “Having bank switching capability ensures that the optimum gamma curve is used for each individual display and eliminates the need for re-work due to display manufacturing process variations.” Ex. 1001, 7:9–12.

C. Illustrative Claim

Petitioner challenges claims 1, 2, 4, and 5 of the '305 patent. Claim 1 is representative and is reproduced below with bracketing added by Petitioner:

1. An integrated circuit for producing voltage signals on a plurality of outputs comprising:

[a] a plurality of non-volatile storage cells;

[b] circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs;

[c] drivers connected to said multiplexer for addressing said storage cells; and

[d] the plurality of inputs connected to said multiplexer for addressing said storage cells;

[e] wherein said voltage signals are gamma reference voltage signals for determining actual driving voltages of columns of a display,

[f] wherein said non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and

[g] means to switch between the banks based on one or more external signals is provided on said integrated circuit.

Pet. 68; Ex. 1010, 7:45–62 (the above limitations are referred to as “limitation [a],” “limitation [b],” “limitation [c],” “limitation [d],” “limitation [e],” “limitation [f],” and “limitation [g]” throughout the Decision).

D. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1, 2, 4, and 5 of the '305 patent on the following grounds (Pet. 17):

Reference(s)	Basis	Claims challenged
Kang ⁴ (Ex. 1007)	§ 103(a) ⁵	Claims 1, 2, 4, and 5
Da Costa ⁶ (Ex. 1008)	§ 103(a)	Claims 1, 2, 4, and 5
Petropoulos ⁷ (Ex. 1009)	§ 103(a)	Claims 1, 2, and 5
Tanaka ⁸ (Ex. 1010)	§ 103(a)	Claims 1, 2, 4, and 5
Da Costa and Tsai ⁹ (Ex. 1011)	§ 103(a)	Claims 1, 2, 4, and 5
Tanaka and Tsai	§ 103(a)	Claims 1, 2, 4, and 5
Petropoulos and Kang	§ 103(a)	Claims 1, 2, 4, and 5

Petitioner also relies on the Declaration of Thomas L. Credelle.

Ex. 1002. Patent Owner relies on the Declaration of Robert J. Murphy.

Ex. 2010.

⁴ U.S. Patent Application Publication No. 2002/0063666 A1 ("Kang").

⁵ The Leahy-Smith America Invents Act (AIA), which amended 35 U.S.C. § 103, was signed into law in 2011. The AIA's amendments to § 103 apply to applications filed on or after March 16, 2013. Because the '305 patent's filing date is prior to March 16, 2013, we refer to the pre-AIA version of § 103.

⁶ U.S. Patent No. 6,100,879 ("Da Costa").

⁷ U.S. Patent Application Publication No. 2003/0090580 A1 ("Petropoulos").

⁸ U.S. Patent Application Publication No. 2003/0132906 A1 ("Tanaka").

⁹ U.S. Patent No. 5,974,528 ("Tsai").

II. ANALYSIS

A. Person of Ordinary Skill in the Art (“POSITA”)

Petitioner asserts that a person of ordinary skill in the art at the time of the invention “would have had at least a bachelor of science degree in physics, electrical engineering, or the equivalent thereof and three (3) years of experience in circuit design or display technologies.” Pet. 13 (citing Ex. 1002 ¶ 21). Petitioner adds, “[s]uch a POSA¹⁰ would have had knowledge of integrated circuits, gamma correction, and storage of gamma correction voltage values within memory, and would have understood how to search available literature for relevant publications.” Pet. 13–14 (citing Ex. 1002 ¶¶ 21–22). Petitioner support its position with Mr. Credelle’s testimony. Ex. 1002 ¶¶ 21–22, *cited in* Pet. 13–14.

Patent Owner describes the ordinary artisan similarly, indicating the artisan would have had “at least a bachelor’s of science degree in electrical engineering or physics or a related field, with at least three years of experience in the design of floating gate nonvolatile memory integrated circuits either as memory chips or embedded technology or floating gate analog design or technology.” Prelim. Resp. 16–17. Patent Owner adds “[t]his person would be aware of the state of the art in floating gate non-volatile technology and circuits by reading articles published in” various journals and patents and by attending presentations at conferences. Prelim. Resp. 17. Mr. Murphy reiterates Patent Owner’s summary. Ex. 2020 ¶ 28.

¹⁰ Like POSITA, POSA also stands for a person of ordinary skill in the art. Petitioner and Mr. Credelle use this acronym and POSITA interchangeably.

Upon review, the parties present similar skill levels for an ordinary artisan. Neither party asserts the differences in the proposed skill level would impact what an ordinary artisan would have known or recognized in the cited prior art. *See generally* Pet.; Prelim. Resp. Under either proposed skill level, our conclusions related to the proposed grounds remain the same. We further note that the prior art itself demonstrates the level of skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown”) (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

B. Claim Construction

For petitions filed before November 13, 2018, the Board interprets claim terms in an unexpired patent according to the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 100(b) (2016); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (affirming applicability of broadest reasonable construction standard to *inter partes* review proceedings). Under that standard, and absent any special definitions, we generally give claim terms their ordinary and customary meaning as would be understood by one of ordinary skill in the art at the time of the invention. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

1. “Non-volatile storage cells”

Petitioner and Patent Owner agree the phrase “non-volatile storage cells” in claim 1 means “computer memory that retains its stored data after power is removed and restores the data when power is returned to the system, such as, for example, the following: analog floating gate

non-volatile memory, Electrically Erasable Programmable Read Only Memory (EEPROM), Flash EEPROM, Ultraviolet EPROM (UVEPROM), and Non-Volatile Random Access Memory (NOVRAM).” Pet. 15–16 (citing Ex. 1002 ¶¶ 45–47); Prelim. Resp. 17. For purposes of this Decision, we adopt the parties’ agreed construction.

2. Limitation [g]
“Means to switch between the banks
based on one or more external signals”
a. 37 C.F.R. § 42.104(b)(3)

37 C.F.R. § 42.104(b)(3) recites, in relevant part, that an *inter partes* petition must provide a statement of the precise relief requested for each claim challenged and that the statement must identify “[h]ow the challenged claim is to be construed” and “[w]here the claim to be construed contains a means-plus-function . . . limitation as permitted under 35 U.S.C. 112[, sixth paragraph], the construction of the claim must identify the specific portions of the specification that describe the structure, material, or acts corresponding to the each claimed function.”¹¹

As explained below, we determine the “means to switch” limitation of claim 1 contains a means-plus-function limitation invoking 35 U.S.C. § 112, sixth paragraph. Petitioner does not provide a claim construction for this phrase. *See* Pet. 14–16. Patent Owner notes Petitioner’s failure to construe this phrase. Prelim. Resp. 18. At best, Petitioner indicates “each term of the Challenged Claims of the ’305 Patent [should] have its ordinary and customary meaning.” Pet. 14.

¹¹ As previously discussed, the pre-AIA statutes are applicable to the ’305 patent.

Because Petitioner has not presented a claim construction for the recited “means to switch” limitation, including identifying portions of the Specification that describe its structure, material, or acts corresponding to its claimed function as set forth in 37 C.F.R. § 42.104(b)(3), we deny institution of the Petition on this basis. Nevertheless, we proceed to construe this term and address the merits of the Petition, and, as discussed below, find additional grounds for denial.

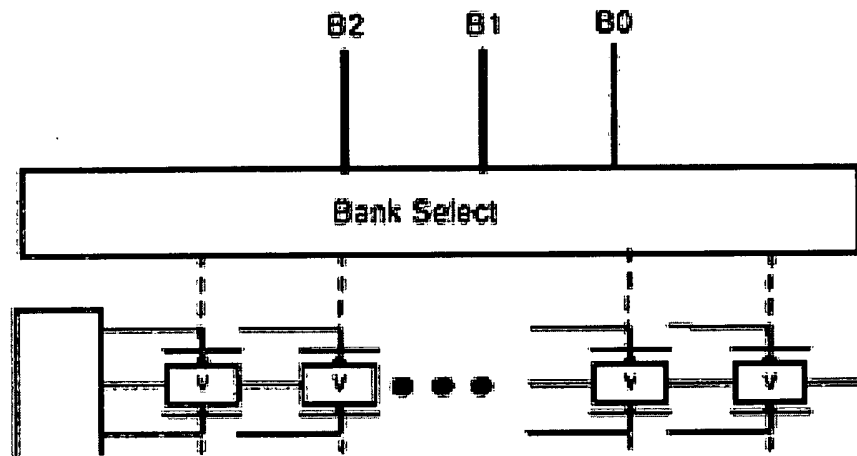
b. Provided Claim Construction

Patent Owner asserts that the “means” phrase in claim 1 “recites a means for performing a specified function” and “must be construed as a means-plus-function limitation under 35 U.S.C. § 112[, sixth paragraph].” Prelim. Resp. 18. As noted above, Petitioner does not provide a claim construction for this phrase (*see* Pet. 14–16) but indicates “each term of the Challenged Claims of the ’305 Patent [should] have its ordinary and customary meaning.” Pet. 14.

Patent Owner states “[t]he function for th[e] limitation [[g]] is switching between the banks based on one or more external signals” and identifies the function’s “corresponding structure” to include (1) the “B0-B2 address inputs” (Prelim. Resp. 18 (citing Ex. 1001, 5:50–63, Figs. 4A-B)), (2) pins for these inputs, and (3) an internal damping circuit referred to as “Bank Switch Damp Time” (Prelim. Resp. 19 (citing Ex. 1001, 5:62–66, Fig. 5)). More specifically, Patent Owner asserts the structure is shown in (1) Figure 4A as pins B0–B2 (the “Bank Select”) corresponding to Figure 4B’s pins 20, 22, and 23 and (2) Figure 6, depicting the Bank Select block with inputs B0, B1, and B2. Prelim. Resp. 18–19 (citing Ex. 1001, 5:50–63, Figs. 4A– 6).

We agree with Patent Owner that the recited phrase “means to switch between the banks based on one or more external signals” in claim 1 invokes 35 U.S.C. § 112, sixth paragraph. A phrase that uses the term “means” creates a presumption that § 112, sixth paragraph applies. *TriMed, Inc. v. Stryker Corp.*, 514 F.3d 1256, 1259 (Fed. Cir. 2008). Also, “[m]eans-plus-function claiming applies only to purely functional limitations that do not provide the structure that performs the recited function.” *Phillips v. AWH Corp.*, 415 F.3d at 1311 (Fed. Cir. 2005); *see also Welker Bearing Co. v. PHD, Inc.*, 550 F.3d 1090, 1095–96 (Fed. Cir. 2008). The recited functional limitation of “switch[ing] between the banks based on one or more external signals” in claim 1 does not provide the structure that performs this recited function. For example, claim 1 does not recite a specific circuit, algorithm, or damping circuit involved in performing the claimed function. Thus means-plus-function claiming applies to limitation [g].

The '305 patent describes an integrated circuit “termed the AG1818” having the capacity to retrieve eight independent banks. Ex. 1001, 5:30–31, 5:50–52. The '305 patent states the AG 1818’s “banks of gamma voltage are . . . selected through the three address inputs B0, B1, and B2” (Ex. 1001, 5:52–53) and “the bank [is] selected by the B0-B2 address inputs” (Ex. 1001, 5:61–62). Address signals B0 through B2 are shown in Figure 6. Ex. 1001, Fig. 6. Part of Figure 6’s block diagram is reproduced below with address signals, B0, B1, and B2 entering a “Bank Select” block:



Part of Figure 6's Block Diagram of an Alternative Embodiment
Ex. 1001, 2:56–57, 5:58–59. The '305 patent further states, “This feature can also be used to switch between different gamma settings based on the information to be displayed for implementing dynamic gamma correction.” Ex. 1001, 5:56–58. Figure 4A further describes B0 through B2 as “Bank Select” signals (Ex. 1001, Fig. 4A), later explaining “the particular bank is addressed through B0-B2” (Ex. 1001, 6:41). Based on this description, we agree with Patent Owner that the structure corresponding to the means to switch is the B0–B2 address inputs, pins for these inputs, the bank select box, and equivalents thereof.

Additionally, the '305 patent describes “an internal damping circuit” that can be used during “read mode” to “create[] a slow transition, about 10 msec., between banks to prevent disruptive display artifacts.” Ex. 1001, 5:60, 5:62–64, Fig. 5 (showing and describing “Tdamp” and “Bank Switch Damp Time”); *see also* Ex. 1001, 5:66–6:2. We agree with Patent Owner that the described internal damping circuit in the '305 patent, and equivalents thereof, are additional structure corresponding to performing the function of switching between the banks based on external signals.

Although neither party construes the following terms, we present a claim construction to address the grounds presented in the Petition.

c. “a multiplexer”

The '305 patent discusses and shows a multiplexer (e.g., mux 320) that connects signals from programming engine 310 to “any one of the programmable analog floating gate memory cells 330 through 337, depending on three address inputs (A_0 , A_1 , and A_2).” Ex. 1001, 3:56–4:3, Fig. 3; Ex. 1002 ¶ 30 (citing same). Although this describes the recited “multiplexer,” this discussion and Mr. Credelle’s accompanying testimony (Ex. 1002 ¶ 30 (stating “the multiplexer . . . is a device used to select which memory cell is addressed by the ‘plurality of inputs’ A_0 , A_1 , and A_2 ”)) merely address the result of using a multiplexer rather than what a multiplexer is. Thus, we consult a dictionary for a customary understanding of “multiplexer” to an ordinarily skilled artisan.

THE AUTHORITATIVE DICTIONARY OF IEEE STANDARD TERMS defines a “multiplexer” as:

multiplexer (A) (supervisory control, data acquisition, and automatic control) A device that allows the interleaving of two or more signals to a single line or terminal. (B) (supervisory control, data acquisition, and automatic control) A device for selecting one of a number of inputs and switching its information to the output.

(2) (A) A device that allows the transmission of a number of different signals simultaneously over a single channel or transmission facility. Synonym: multiplexor. (B) A device capable of interleaving the events of two or more activities or of distributing the events of an interleaved sequence to their respective activities. Contrast: demultiplexer

THE AUTHORITATIVE DICTIONARY OF IEEE STANDARD TERMS 716 (Kim Breitfelder & Don Messina eds., St'd Info. Network IEEE Press 7th ed. 2000).

Figure 3 of the '305 patent shows six signals entering multiplexer 320 and three exit to "any one of the programmable analog floating gate memory cells 330 through 337, depending on three address inputs (A_0 , A_1 , and A_2)."

Ex. 1001, 3:56–4:3, Fig. 3. This multiplexer arrangement is more than a device that allows simultaneous transmission of different signals over a single channel like above definition (2). Rather, the description in the specification is most consistent with the first definition quoted above.

Accordingly, consistent with the '305 patent's Specification, we determine the recited "multiplexer" includes a device that interleaves signals to a single line, or selects one input and switches its information to the output.

d. "banks of cells"

The '305 patent states the integrated circuit, termed the AG1818, has the capacity for eight banks, which are selected through three address signals B0 through B2 (not shown). Ex. 1001, 5:30–31, 50–53, Fig. 4. But, the '305 patent does not show or define a cell's bank. *See generally* Ex. 1001. Given the absence of any explicit definition, we generally give the term "bank" its ordinary and customary meaning as would be understood by one of ordinary skill in the art at the time of the invention.

Consulting THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS, the definition of "bank" most relevant to this proceeding is the following:

(2) (A) One or more disk drives lined up in a row. (B) Any group of similar devices that are connected together for use as a single

device. For example, a row of light-emitting diodes connected to form a display. (C) A contiguous section of addressable memory. For example, eight memory devices, each of which is 64 kB by 1; forming a 64 kB X 8 memory bank.

THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS 85 (Kim Breitfelder & Don Messina eds., St'd Info. Network IEEE Press 7th ed. 2000) (def. 2).

Because, as noted above, both Petitioner and Patent Owner agree the recited “storage cells” relate to computer memory, we conclude definition 2(C) is the most relevant to the phrase “banks of cells.” Thus, we determine the claimed “banks of cells” are contiguous sections of addressable, computer memory.

No other claim term requires express construction.

C. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.¹² *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

¹² Neither party presents arguments regarding objective evidence of nonobviousness here.

D. Obviousness Grounds

Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over seven grounds. Pet. 17–66. Patent Owner present arguments contending the grounds do not teach or suggest claim 1’s preamble and limitations [b]–[d], [f] and [g]. Prelim. Resp. 22–62 . Having reviewed Petitioner’s assertions, Patent Owner’s arguments, and the references, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing the unpatentability of the challenged claims based on any of the above-identified grounds. We focus on independent claim 1 for each of the proposed grounds.

1. Kang (Ex. 1007)

Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over Kang under 35 U.S.C. § 103(a). Pet. 18–30. To support its contentions, Petitioner cites to Mr. Credelle’s declaration testimony (Ex. 1002). Patent Owner presents several arguments, including that Kang does not teach or suggest claim 1’s preamble and limitations [b], [d], [f], and [g]. Prelim. Resp. 22–27. Patent Owner cites to Mr. Murphy’s declaration testimony (Ex. 2010).

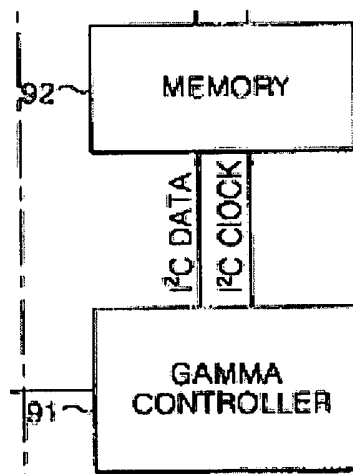
For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Kang renders claim 1 obvious. We focus on limitations [b], [f], and [g].

As background, Kang discusses “[a] gamma voltage and video data correcting apparatus and method in a liquid crystal display . . . , wherein the gamma data for controlling the gamma voltage is stored for each of at least two modes.” Ex. 1007, Abstract.

a. Limitation [b]

*“circuits for programming coupled to a multiplexer
for addressing and programing said storage cells”*

For this limitation, Petitioner maps Kang’s gamma controller 91 to a “circuit for programming.”¹³ Pet. 24–25 (citing Exs. 1007 ¶ 52 and 1002 ¶ 55). Petitioner states the gamma controller circuit is coupled to storage cells (e.g., memory 92 in Fig. 9) through an I²C interface, which Petitioner contends is “a common serial interface.” Pet. 24 (citing Exs. 1007 ¶ 52 and 1002 ¶ 55). Petitioner argues Kang’s I²C interface provides instructions as to where in the memory the data is to be written. *Id.* (citing Exs. 1007 ¶ 52 and 1002 ¶ 55). Kang’s I²C interface, shown in Figure 9, follows:



Partial View of Kang’s Figure 9 showing an I²C interface.

Petitioner concludes an ordinarily skilled artisan “would have understood that the use of a serial interface over a multiplexer is an obvious modification . . . because, since a multiplexer and an I²C serial interface perform identical functions within an integrated circuit, these commodity components are replaceable and do not alter the operation of the device.”

¹³ Claim 1 recites “circuits for programming” not “circuit for programming.” Ex. 1001, 7:48 (emphasis added).

Pet. 24 (citing Ex. 1002 ¶ 55 and *In re Japikse*, 181 F.2d 1019 (CCPA 1950)).

Patent Owner rebuts. Prelim. Resp. 23–25. Patent Owner argues Petitioner “does not explain where Kang discloses a multiplexer because Kang does not.” Prelim. Resp. 24 (citing Ex. 1002 ¶ 57). Petitioner does not contend otherwise. Pet. 24 (noting Kang discloses an I²C serial interface and proposing to modify the serial interface with a multiplexer). That is, Kang discloses that an I²C connects gamma controller 91 to memory 92 and transmits I²C data and clock data to memory 92. Ex. 1007 ¶ 52, Fig. 9. On the current record, Kang does not disclose the recited “multiplexer” of claim 1.

Patent Owner also contends Petitioner provides no support through its expert or documentary evidence for the statement that an artisan would have understood that the use of a serial interface instead of a multiplexer is an obvious modification. Prelim. Resp. 24. Patent Owner argues that “a multiplexer and an I²C serial interface do not perform the same function within an integrated circuit and therefore are not interchangeable.” Prelim. Resp. 25 (citing Ex. 2010 ¶¶ 39–40). We agree with Patent Owner for the following reasons.

Mr. Credelle testifies that an I²C serial interface is a common serial interface. Ex. 1002 ¶ 55 (citing Ex. 1013¹⁴). We agree Exhibit 1013 supports that an I²C bus, which is shown in Kang’s Figure 9, includes a serial data line and serial clock line. Ex. 1013, p. 1 § 1.0. Exhibit 1013 also outlines various “features of the I²C bus,” including having two bus lines

¹⁴ Philips Semiconductors, THE I²C-BUS AND HOW TO USE IT (INCLUDING SPECIFICATIONS) 1–24 (1995).

(data and clock), data corruption properties (e.g., collision detection and arbitration), bidirectional data transfer, and on-chip filtering. Ex. 1013, p. 1 § 1.0.

Comparing the above understandings of “multiplexer” with an I²C bus, we disagree the two perform identical functions as Petitioner asserts. Pet. 24. A multiplexer functions to interleave signals to a single line or to select one input and switch its information to the output. *Id.* An I²C bus, like that in Kang and like that discussed in Exhibit 1013, does not discuss interleaving signals to a single line (e.g., the I²C data with I²C clock), or selecting one input and switching its information to the output. For example, Kang shows and describes that its I²C lines separately enter memory 92 but does not discuss interleaving signals or switching its information. Ex. 1007 ¶ 52, Fig. 9. Nor does our understanding of a multiplexer’s functions include performing data corruption, bidirectional data transfer, and on-chip filtering, like that of an I²C bus. Ex. 1013, p. 1 § 1.0. Mr. Murphy also testifies an ordinary artisan would not understand an I²C interface is equivalent to a multiplexer. Ex. 2010 ¶ 39.

Moreover, Petitioner’s evidence does not support its contention that a skilled artisan would have made the “simple . . . design choice” of modifying Kang with a multiplexer. Pet. 24; *see Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”). Petitioner cites Mr. Credelle’s testimony. Pet. 24 (citing Ex. 1002 ¶ 55). Mr. Credelle, however, does not testify that it would have been obvious to modify Kang. Rather, Mr. Credelle testifies that Kang discloses a multiplexer, which, as noted above, is not Petitioner’s contention.

Ex. 1002 ¶ 55 (“As already discussed, flash memory includes multiplexers, e.g., row and column decoders, to determine where to write data.”). Thus, the Petition is deficient for failing to identify a reason to modify Kang.

As to Mr. Credelle’s testimony that flash memory includes multiplexers to determine where to write data, Mr. Credelle cites, without specificity, to Exhibit 1014. Ex. 1002 ¶ 55 n.6 (citing Ex. 1014¹⁵). Exhibit 1014 discusses flash memory and non-volatile memory, such as EEPROM, EEPROM, and Flash (Ex. 1014, pp. 1–2), and Kang discloses that memory 92 can be EEPROM or EPROM (Ex. 1007 ¶ 53, *noted in* Ex. 1002 ¶ 61). However, Mr. Credelle does not identify where Exhibit 1014 discusses or addresses multiplexers. Thus, just as Petitioner or its expert has not identified where Exhibit 1014 demonstrates flash memory includes a multiplexer, one skilled in the art would not have recognized that Kang’s memory includes a multiplexer.

As for Mr. Credelle testimony that “[a]s already discussed, flash memory includes multiplexers, e.g., row and column decoders, to determine where to write data,” Mr. Credelle does not cite to any particular support for this statement. Ex. 1002 ¶ 55. Presuming he refers to paragraphs 30 through 32 under Section C, titled “Multiplexer for Addressing Memory” (Ex. 1002, p. 12),¹⁶ this testimony merely supports Petitioner’s argument that a multiplexer is any device used to select a memory cell addressed by a plurality of address inputs, an argument we reject above.

¹⁵ Roberto Bez et al., *Introduction to Flash Memory*, 91 PROC. OF THE IEEE 1–14 (2003).

¹⁶ Mr. Credelle first discusses a flash memory cell that uses row and column decoders under this section.

In paragraphs 30 through 32, Mr. Credelle discusses how the '305 patent describes a multiplexer that connects signals from an engine to storage cells. Ex. 1002 ¶ 30 (citing Ex. 1001, 3:56–4:3). From this discussion, Mr. Credelle defines a “multiplexer” in claim 1 as “a device used to select which memory cell is addressed by the ‘plurality of inputs’ A₀, A₁, and A₂.” Ex. 1002 ¶ 30. But, as noted above, a multiplexer is not simply any device that selects a memory cell based on a plurality of address inputs. Rather, it is a device that interleaves signals to a single line or selects one input and switches its information to the output.

Lastly, we note the proposed ground relies on Kang alone, not Kang and Fazio,^{17,18} to teach claim 1’s limitation [b]. Pet. 18, 24–25. As proposed, we determine an ordinary artisan would not have understood that using a multiplexer over Kang’s I²C bus interface “is an obvious modification” and that the an I²C bus interface is replaceable by the multiplexer without altering Kang’s device. Pet. 24.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Kang renders obvious limitation [b] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. See Pet. 28–30.

¹⁷ Ex. 1012 (U.S. Patent No. 5,677,869 (Oct. 14, 1997) (“Fazio”), *noted in* Ex. 1002 ¶¶ 31–32.

¹⁸ *In re Hoch*, 428 F.2d 1341, 1342 n.3 (CCPA 1970) (“Where a reference is relied on to support a rejection, whether or not in a ‘minor capacity,’ there would appear to be no excuse for not positively including the reference in the statement of the rejection.”).

*b. Limitation [f]
“said non-volatile storage cells are organized
into two or more banks of cells”*

For this limitation, Petitioner points to two passages in Kang. Pet. 27–28. Petitioner notes Kang discloses a gamma voltage correcting apparatus includes memory “for storing gamma data for controlling a gamma voltage for each of at least two modes.” Pet. 27 (citing Ex. 1007 ¶ 22 and Ex. 1002 ¶ 59). Petitioner further indicates Kang discloses four modes with different gamma voltages. Pet. 27–28 (citing Ex. 1007 ¶ 59 (Table I) and Ex. 1002 ¶ 59); Ex. 1002 ¶ 61 (citing Ex. 1007 ¶¶ 59–60). Petitioner asserts an ordinary artisan would have understood the two or more modes as disclosed by Kang demonstrates Kang’s gamma generator has two or more banks. Pet. 28 (citing Ex. 1002 ¶ 59).

Patent Owner disagrees. Prelim. Resp. 26. Patent Owner argues Kang discloses memory block 92 with no details how the memory is organized. Prelim. Resp. 26. We agree. Kang discloses multi-mode gamma voltage generator 84 having memory 92, which can be an EEPROM or EPROM. Ex. 1007 ¶¶ 51–53, Figs. 8–9. No further information related to memory 92’s design or architecture is provided. *See* Ex. 1007 ¶¶ 51–53, Figs. 8–9. Even more, Kang does not teach or suggest that the modes are organized in memory as contiguous sections of addressable, computer memory (i.e., as “banks” as construed above).

Kang also discusses “storing a gamma data for controlling a gamma voltage for each of at least two modes.” Ex. 1007 ¶ 22, Abstract. Kang addresses “gamma reference voltages . . . for each mode, Modes A to D” and provides TABLE 1, showing modes A to D. Ex. 1007 ¶ 59. Quoting from these same passages, Mr. Credelle determines “Kang clearly teaches that the

multi-mode gamma generator has two or more banks that contain predetermined gamma reference voltages.” Ex. 1002 ¶ 59. Relying on Mr. Credelle’s testimony and Kang’s multi-mode discussion, Petitioner concludes an ordinary skilled artisan would have understood this discussion of “modes” equates to banks. *See* Ex. 1002 ¶ 59. We find this position unpersuasive.

As noted above, Kang does not discuss organizing its memory using banks of two or more contiguous memory portions. Ex. 1007 ¶¶ 51–53, Figs. 8–9. Additionally, Kang does not discuss how the mode’s data would be stored in memory, such that they suggest, to one skilled in the art, organizing the cells into “two or more banks” as recited. Ex. 1007 ¶¶ 22, 59, Abstract. Mr. Credelle’s testimony on this feature relies on the same passages without further explanation of how Kang’s modes suggest organizing Kang’s memory into two or more banks. Ex. 1002 ¶ 59.

For the previous reasons, Petitioner does not show sufficiently for institution purposes that Kang renders obvious limitation [f]. Claims 2, 4, and 5 depend respectively from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 28–30.

c. Limitation [g]

“means to switch between the banks based on one or more external signals”

Petitioner contends the gamma generator switches between modes using the disclosed control means that accesses data, and a LCD receives an external mode signal to select gamma data from memory. Pet. 28 (citing Exs. 1007 ¶ 22 and 1002 ¶ 60). Petitioner argues an ordinary artisan would

have understood this control means provides the external signal to switch between modes (e.g., banks). Pet. 28 (citing Ex. 1002 ¶ 60).

Kang describes a “control means for accessing the gamma data in response to an instruction” and “a mode selected by the control means.” Ex. 1007 ¶¶ 22, 49; Ex. 1002 ¶ 60. But, any details of how the control means selects a mode is lacking, such that Kang fails to teach or suggest the structure that controls how the control means switches between modes. As previously discussed, Kang’s modes do not clearly correspond to the recited “banks” (e.g., contiguous sections of addressable, computer memory).

Furthermore, Petitioner has not explained further how Kang’s “control means” teaches an equivalent to the recited “means to switch between banks” in claim 1. Pet. 27–28.

Mr. Credelle further discusses Kang’s claim 29 and paragraphs 59, and 60 to teach limitation [g]. Ex. 1002 ¶¶ 60–61. Kang discusses outputting specified mode gamma reference voltages, shown in Table I, “in accordance with a logical value of the gamma data” (Ex. 1007 ¶¶ 59–60) or setting gamma data in response to modes corresponding to peripheral equipment (Ex. 1007 ¶ 66). Lacking, however, is a discussion of structure to switch between memory banks. Notably, Kang’s discussion addresses (1) what happens at multi-channel DAC (digital to analog converter) 93, which interprets gamma data *from* memory 92 (Ex. 1007 ¶ 54), and (2) what is outputted from DAC 93 (e.g., gamma reference voltages in accordance with a logical value). Ex. 1007 ¶ 60, Figs. 9–10. This does not relate to how to switch any banks within memory 92, such that the DAC’s output switches between storage cells’ banks. *See* Ex. 1007 ¶¶ 60, 66, Figs. 9–10.

Claim 29 in Kang also recites storing gamma data in memory and selecting specific gamma data in memory based on a received external mode

signal. Ex. 1007, claim 29. Although this might suggest selecting data associated with a specific mode from memory based on an external signal, the claim does not recite or suggest the corresponding structure to switch between memory banks (e.g., a circuit, algorithm, and/or damping circuit that uses at least one bank address signal). Petitioner also fails to address adequately how the selections within memory in Kang are achieved such that Kang suggests to one skilled in the art the noted structure (e.g., a bank select circuit, algorithm, pins, and/or damping circuit that uses at least one bank address signal) for switching between memory or “storage cells” banks based on at least one received external signal as recited in claim 1.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Kang renders obvious limitation [g]. Claims 2, 4, and 5 depend respectively from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 28–30.

d. Conclusion

Having reviewed Petitioner’s and Patent Owner’s assertions related to Kang, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Kang renders the challenged claims 1, 2, 4, and 5 of the ’305 patent obvious.

2. Da Costa (Ex. 1008)

Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over Da Costa under 35 U.S.C. § 103(a). Pet. 17, 30–37. To support its contentions, Petitioner cites Mr. Credelle’s testimony. Ex. 1002. Patent Owner presents several arguments, including that Da Costa does not teach or suggest claim 1’s preamble and limitations [b]–[d], [f] and [g]. Prelim. Resp. 29–35. Patent Owner cites Mr. Murphy’s testimony. Ex. 2010.

For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Da Costa renders the challenged claims obvious. We focus on claim 1's limitations [b], [f], and [g].

Da Costa discusses “[a] smart controller chip for controlling an active matrix display.” Ex. 1008, Abstract. “The combination of D/A [digital/analog] analog circuitry and standard digital logic makes the controller uniquely suited for addressing all the panel control needs both for the normal digital functions but also for control of the analog aspects of the panel, like display gamma.” Ex. 1008, 2:37–41.

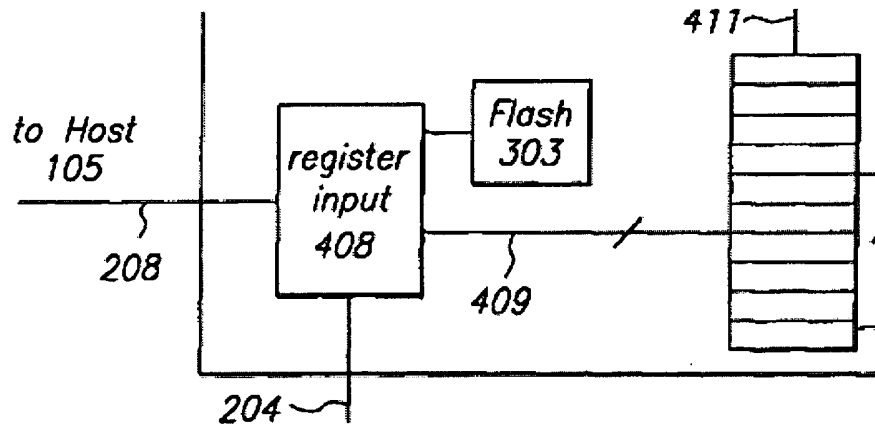
a. Limitation [b]

For this limitation, Petitioner states Da Costa's multiple address lines are used to write the data within memory and registers program the memory with a serial bus. Pet. 33 (citing Exs. 1008, 6:56–60, 11:29–32 and 1002 ¶¶ 77–78). Petitioner contends “a serial bus is an addressing circuit that is interchangeable with a multiplexer,” rendering this limitation obvious. Pet. 33 (citing Ex. 1002 ¶ 55). Petitioner also states Da Costa “does not explicitly describe programming the flash memory 303” but such an arrangement would be obvious to an ordinary artisan. Pet. 33 (citing Ex. 1002 ¶ 78).

Patent Owner argues Petitioner does not explain what in Da Costa provides the multiplexer and disputes that a serial bus is interchangeable with a multiplexer. Prelim. Resp. 31.

Da Costa discloses that register input circuitry 408 receives digital values (e.g., signals) through first serial bus 204 and second serial bus 208 from host system 105 in Figure 4A. Ex. 1008, 6:56–58, Fig. 4A. Da Costa's Figure 4A, partially shown below, illustrates a smart controller chip

(e.g., 202) with serial buses 204 and 208 (discussed in column 6 as cited) entering register input 408.



Partial View of Da Costa's Figure 4A with serial buses.

Ex. 1003, 3:29–30. Da Costa teaches flash memory (e.g., 303 in Figure 4A) integrated into a smart controller chip (e.g., 202), the flash memory being mapped to the recited “non-volatile storage cells.” Pet. 32–33 (citing Exs. 1008, 2:55–59 and 1002 ¶¶ 76–77).

Although Da Costa's Figure 4A may suggest to an ordinary artisan using inputs from the host and/or register inputs to program flash memory 303 (Pet. 33), Petitioner has not demonstrated sufficiently that Da Costa's serial buses act as an addressing circuit that is interchangeable with a multiplexer. Pet. 33. As previously discussed, claim 1 requires “a multiplexer” separate from and coupled to the “circuits for programming.” Pet. 68. For reasons similar to those discussed above when addressing Kang, the record does not demonstrate sufficiently that (1) a serial bus is interchangeable with a multiplexer or performs the identical function of a multiplexer, (2) Da Costa's flash memory includes or suggests a multiplexer, (3) Da Costa teaches or suggests using decoders somewhere between its host and its flash memory (e.g., 303), or (4) a structure connected to flash

memory 303 that behaves like a device that interleaves signals into a single line, or selects one input and switches its information to the output, which is the customary understanding of a multiplexer. We refer to our discussion of this limitation for Kang, above, for more details.

Mr. Credelle cites to other passages in Da Costa to teach limitation [b]. Ex. 1002 ¶ 84 (citing Ex. 1008, 2:47–49, 6:41–49, 6:62–67). Da Costa states a smart controller chip includes registers that contain values but fails to discuss a multiplexer. Ex. 1008, 2:47–49. Da Costa further discusses the structure within Figure 4A’s block diagram, which includes multiplexer circuitry 413. Ex. 1008, 6:41–49, 62–67, Fig. 4A. However, multiplexer circuitry 413 is located after flash memory 303 and registers 410, not connected to the mapped storage cells (e.g., flash memory 303). Ex. 1008, Fig. 4A. The proposed grounds fails to explain sufficiently how this multiplexer is involved in “addressing and programming said storage cells,” which is mapped to flash memory 303. Pet. 33.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Da Costa renders obvious limitation [b] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. See Pet. 36–37.

b. Limitation [f]

For limitation [f], Petitioner states Da Costa teaches ten separate gamma curves in flash memory and one skilled in the art would have understood storing the curves in multiple banks. Pet. 35 (citing Exs. 1007, Figs. 4A and 7A and 1002 ¶ 82). Patent Owner argues Da Costa fails to discuss how its memory is organized, including organized in banks, and one

skilled in the art would not have understood its memory is organized in banks. Prelim. Resp. 32–33 (citing Exs. 1008, 8:48–50, Fig. 7A and 2010 ¶ 43).

Da Costa discloses flash memory 303 with no details of how the memory is organized. Ex. 1008, Fig. 4A. Figure 7A shows the details of registers 410, lines 412, multiplexer circuit 413, lines 415, and high-power analog output circuitry 416 or low-power analog output circuitry 450 in Figure 4A, which are located after register input 408 and flash memory 303. Ex. 1008, 3:29–30, 3:38–42, 6:62–67, 7:38–39, 8:48–51, Figs. 4A–B, 7A. As discussed above, Petitioner has mapped the storage cells to flash memory 303, not to other structure, such as registers 410. Pet. 32–33 (citing Exs. 1008, 2:55–59 and 1002 ¶¶ 76–77). Also, the order in which these components are arranged does not demonstrate specifically how the “non-volatile storage cells are organized,” as recited in claim 1 and as mapped by Petitioner. Prelim. Resp. 33.

Mr. Credelle testifies, “The gamma curves are stored in flash memory 303 and transmitted to registers 410 through bus 409.” Ex. 1002 ¶ 82 (citing Ex. 1008, Fig. 4A) (bolding omitted). Assuming Mr. Credelle is correct, this fails to disclose *how* the stored curves are arranged in memory, such that its storage cells “are organized into two or more banks of cells” (i.e., into contiguous sections of addressable, computer memory) as claim 1 requires.

Mr. Credelle further maps limitation [f] to various passages in Da Costa. Ex. 1002 ¶ 84 (citing Ex. 1008, 9:1–16, 11:29–33, Figs. 7A–B). Figure 7B is similar to Figure 7A and suffers from the problems previously identified for Figure 7A. Ex. 1008, Fig. 7B. The remaining cited passages fail to discuss memory banks, and Mr. Credelle provides no further explanations of these passages. Ex. 1002 ¶ 84.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Da Costa renders obvious limitation [f] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 36–37.

c. Limitation [g]

We agree with Patent Owner that limitation [f], the banks, are not taught or suggested by Da Costa. Prelim. Resp. 33. Moreover, even if Da Costa did teach the recited “banks,” Petitioner has not shown that it teaches limitation [g].

Petitioner further states Da Costa teaches registers 410 connected to chip control circuitry and multiplexer circuitry and the multiplexer circuitry is connected to chip control circuitry and the high-power analog output circuitry. Pet. 35 (citing Exs. 1008, 7:1–9 and 1002 ¶ 83). Da Costa describes and shows chip register 410 connected to MUX 413 and control circuitry 406 and MUX 413 connected to high-power analog output 416. Ex. 1008, 6:62–7:9, Figs. 4A, 7A. As noted above, these circuits are located after flash memory 303. Like Patent Owner, we are not convinced that how these components are connected to each other or how these components would be involved in switching between any purported banks located in Da Costa's storage cells (e.g., 303) to demonstrate limitation [g]. Prelim. Resp. 34.

Petitioner further contends Da Costa's serial bus 208 is used to communicate information between first smart controller 202 and host system 105, which allegedly allows for dynamic modification of the analog reference levels and column/row control signal output by the first smart controller 202. Pet. 35–36 (citing Ex. 1008, 5:1–6). Petitioner states an

ordinary artisan “would have understood this disclosure to describe means to switch between banks using control circuitry 406” based on external input from host 105. Pet. 36 (citing Ex. 1002 ¶ 83). Once again, control circuit 406 is located after flash memory 303. Ex. 1008, Fig. 4A. Petitioner does not establish how this circuit is involved in switching between any purported banks of the storage cells.

The cited passages of Da Costa fail to describe sufficiently structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses at least one bank address signal) corresponding to the recited means in claim 1, including any structure that permits switching between any alleged banks located within Da Costa’s flash memory 303 based on received signals communicated over bus 208. Prelim. Resp. 33–35.

Mr. Credelle further maps limitation [g] to column 11 in Da Costa. Ex. 1002 ¶ 84 (citing Ex. 1008, 11:29–33, 11:41–46). Besides quoting passages from column 11, Mr. Credelle provides no further explanation. Ex. 1002 ¶ 84. Da Costa discusses host system 105 may have software to select between different preprogrammed curves. Ex. 1008, 11:29–33, 41–46. However, selecting between curves fails to teach or suggest a corresponding structure for switching between storage cells’ banks, as claim 1 requires, or its equivalent.

Lastly, Petitioner has not further elaborated on how Da Costa’s purported “means” teaches an equivalent to the recited “means to switch between banks” in claim 1. Pet. 27–28.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Da Costa renders obvious limitation [g] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the

dependent claims does not cure the deficiency of its showing for claim 1.
See Pet. 36–37.

d. Conclusion

Having reviewed Petitioner’s and Patent Owner’s assertions related to Da Costa, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Da Costa renders the challenged claims 1, 2, 4, and 5 of the ’305 patent obvious.

3. Petropoulos (Ex. 1009)

Petitioner also challenges claims 1, 2, and 5 as being unpatentable over Petropoulos under 35 U.S.C. § 103(a). Pet. 17, 37–45. To support its contentions, Petitioner cites Mr. Credelle’s testimony (Ex. 1002). Patent Owner presents several arguments, including Petropoulos does not teach or suggest claim 1’s preamble and limitations [b], [d], and [g]. Prelim. Resp. 39–40. Patent Owner cites Mr. Murphy’s testimony (Ex. 2010).

For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Petropoulos renders claim 1 obvious. We focus on limitations [b] and [g].

Petropoulos discusses “a programmable analog/multi-level memory array for modifying individual outputs . . . in order to obtain a desired sensor array output.” Ex. 1009, Abstract. “The memory array can be programmed with data corresponding to desired modifications, such as . . . gamma correction.” Ex. 1009, Abstract.

a. Limitation [b]

For limitation [b], Petitioner states Petropoulos discloses an address signal generator that provides address signals indicative of row/column addresses, for selecting one of memory cells C11 to CMN to write data values. Pet. 41 (citing Exs. 1009 ¶ 31 and 1002 ¶ 102). Petitioner further

states an address signal generator can be a buffer circuit for generating address signals from addresses provided by external circuitry. Pet. 42 (citing Exs. 1009 ¶ 31 and 1013 ¶ 103). Without stating what circuitry maps to the multiplexer, Petitioner contends an ordinary artisan would have understood the address signal generator programs and addresses storage cells based on multiple inputs (Pet. 41–42 (citing Exs. 1009, Fig. 3 and 1002 ¶ 102)) and that “the decoder tree and other elements within memory are circuits for programming” (Pet. 42 (citing Ex. 1002 ¶ 103)).

Patent Owner contends Petitioner does not explain or specify where the multiplexer is in Petropoulos. Prelim. Resp. 39. We agree. The Petition discusses an “address signal generator” for selecting a memory cell and a buffer circuit for generating address signals but never states the generator or buffer circuit is a multiplexer. Pet. 41–42. Likewise, the Petition states the decoder tree and other elements within memory are circuits for programming but does not explain adequately how these components are a multiplexer as claim 1 requires. Pet. 42.

Cited paragraph 31 of Petropoulos does not assist in clarifying the mapping. Ex. 1009 ¶ 31. Petropoulos discusses address signal generator 320, which can be a buffer circuit, provides address signals for a selected memory cell (e.g., C11–CMN) to which the data value will be written. Ex. 1009 ¶ 31, Fig. 3; Ex. 1002 ¶ 102 (citing Ex. 1009 ¶ 31, Fig. 3). Petropoulos does not discuss how address signal generator 320 behaves like a multiplexer as commonly understood by an ordinary skilled artisan (i.e., a device that interleaves signals to a single line, or selects an input and switches its information to the output). Ex. 1009 ¶ 31, Fig. 3.

Likewise, Petitioner and Mr. Credelle have not explained sufficiently how Figure 3’s decoder tree and “other elements within memory” suggests a

multiplexer to one skilled in the art. Pet. 42; Ex. 1002 ¶¶ 102–103. We emphasize the phrase “other elements” (Pet. 42; Ex. 1002 ¶ 103) does not sufficiently map the recited “multiplexer” to Petropoulos’s components. To the extent Petitioner contends that any circuit that receives address signals and outputs other signals is a multiplexer, we disagree for reasons previously presented.

Mr. Credelle maps limitation [b] to yet further passages in Petropoulos. Ex. 1002 ¶ 110 (citing Ex. 1009 ¶¶ 12–13). Other than quoting from these paragraphs, which do not discuss or suggest a multiplexer, Mr. Credelle provides no further explanation of how these paragraphs teach or suggest “a multiplexer” as claim 1 recites. Ex. 1002 ¶ 110.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Petropoulos renders obvious limitation [b]. Claims 2 and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 45.

b. Limitation [g]

Petitioner asserts Petropoulos teaches “a desired one of the memory arrays 210 is selected for a particular modification.” Pet. 44 (quoting Ex. 1009 ¶ 51 and citing Ex. 1002 ¶ 108). In particular, Petitioner states routing circuit 220 selects a desired modification and that one skilled in the art would have understood the decoder, which accesses the desired voltage from a memory array, maps to the recited “means to switch between banks based on external signals, i.e., the routing circuit.” Pet. 44–45 (citing Exs. 1009 ¶¶ 27, 53 and 1002 ¶ 109).

Cited paragraph 27 summarizes what is shown in Figure 2 below.

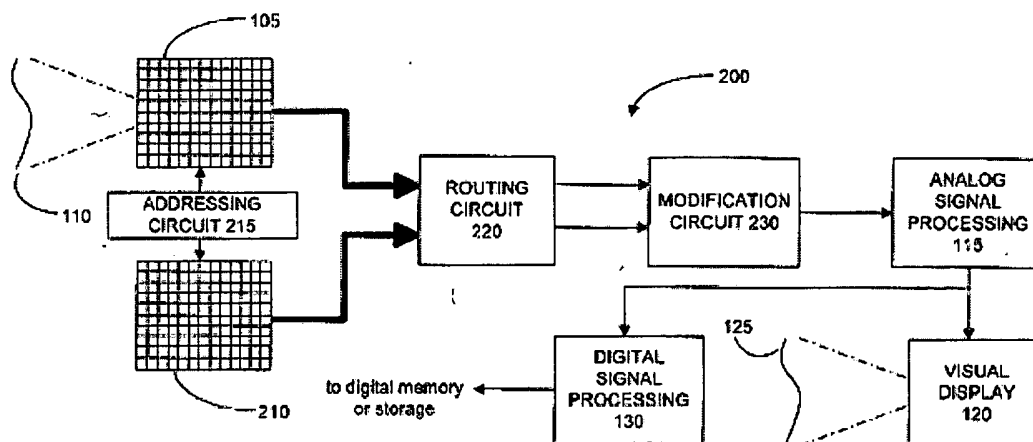
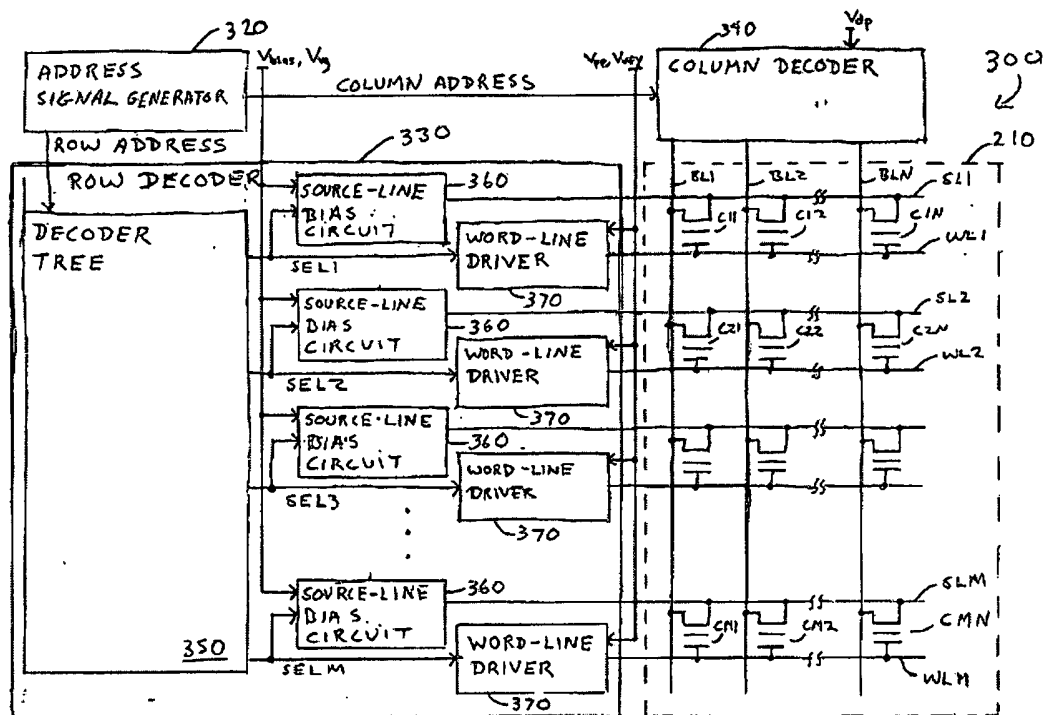


FIG. 2

Petropoulos's Figure 2 Showing an Imaging System

Figure 2's imaging system includes (1) image sensor 105, (2) addressing circuit 215 reading out voltages from image sensor 105 and memory 210, (3) routing circuit 220, and (4) analog signal processing circuit 115 for processing reconstructed image 125. Ex. 1009 ¶¶ 27–28, Fig 2. There is no accompanying discussion of a corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) to limitation [g] in Figure 2.

Figure 3 below shows more detail of the multi-memory 210 in above Figure 2.



Petropoulos's Figure 3 Showing Memory

The above Figure 3's memory shows address signal generator 320 coupled to column decoder 340 and row decoder 330, the decoders coupled to multi-level memory 210. Ex. 1009 ¶ 19, Fig. 3.

Although this figure shows decoders 330 and 340, Petitioner does not explain sufficiently or identify adequately how Petropoulos's decoder is a corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) to limitation [g]. See Prelim. Resp. 40. For example, Petropoulos's Figure 3 has two decoders (e.g., row decoder 330 and column decoder 340). Ex. 1009, Fig. 3. But, Petitioner does not explain whether both of these decoders, or which portions of these decoders, are being mapped to limitation [g]. Pet. 44–45.

Petropoulos discusses a desired memory is selected for a particular modification (Ex. 1009 ¶ 51, *cited in* Pet. 44) and the memory array and

decoder are collectively used for the modifications (Ex. 1009 ¶ 53, *noted in* Pet. 44). Regardless, Petitioner fails to explain how this teaches or suggests the structure corresponding to limitation [g] (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal).

Petropoulos discusses that a multi-level memory array can be used with a decoder for multiple modification types. Ex. 1009 ¶ 53, *noted in* Pet. 44. Petropoulos states, “The memory array is programmed with data corresponding to the desired types of modifications in various portions of the array” and “[t]he decoder then determines the type of modification . . . and accesses the desired voltage from the memory array” (Ex. 1009 ¶ 53). Petitioner fails to explain sufficiently how “the decoder” determining the modification type and accessing the memory array’s desired voltage teaches or suggests to the corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) of limitation [g].

Petitioner further cites paragraph 108 of Mr. Credelle’s testimony as support for Petropoulos teaching limitation [g]. Pet. 44. Mr. Credelle, however, does not persuasively explain how the portions of Petropoulos he cites teach or suggest a corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) to a means for switching between banks as claim 1 requires.

Petitioner further states that the decoder “selects a location in the memory array” (Pet. 44), turning to Mr. Credelle’s testimony for support (Pet 45 (citing Ex. 1002 ¶ 109)). In paragraph 109, Mr. Credelle discusses memory arrays 210, routing circuit 220, and modification circuitry block 230 (shown in Figure 2) are used to select and perform memory array modification and teach “a means to select gamma data from the memory

arrays and a routing circuit 220 to select the modifications.” Ex. 1002 ¶ 109 (citing Ex. 1009 ¶¶ 27, 51). Thus, Mr. Credelle concludes that the “means to select gamma data” and the routing circuit 220—not the previously discussed decoder—are a “means to switch between banks.” Ex. 1009 ¶ 109.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Petropoulos renders obvious claim 1’s limitation [g]. Claims 2 and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 45.

c. Conclusion

Having reviewed Petitioner’s and Patent Owner’s assertions, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Petropoulos renders challenged claims 1, 2, and 5 of the ’305 patent obvious.

4. Tanaka (Ex. 1010)

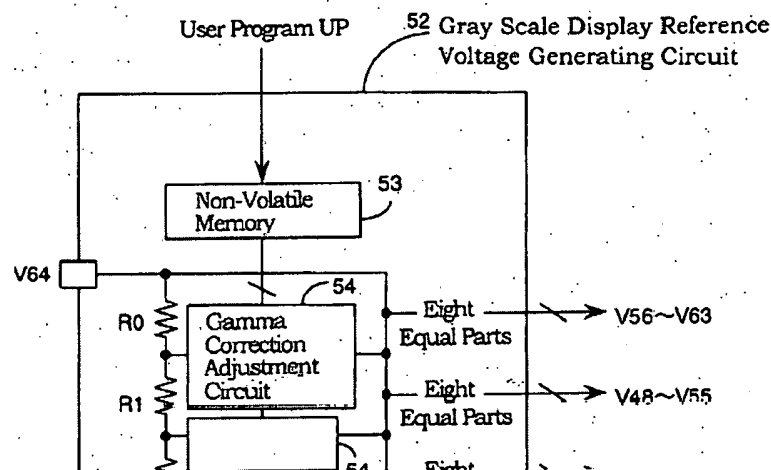
Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over Tanaka under 35 U.S.C. § 103(a). Pet. 17, 45–53. To support its contentions, Petitioner cites to Mr. Credelle’s testimony (Ex. 1002). Patent Owner presents several arguments, including Tanaka does not teach or suggest claim 1’s preamble and limitations [b], [d], [f], and [g]. Prelim. Resp. 41–47. Patent Owner cites to Mr. Murphy’s testimony (Ex. 2010).

Having reviewed Petitioner’s and Patent Owner’s assertions related to Tanaka, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Tanaka renders challenged claim 1 obvious for the following reasons. We focus on claim 1’s limitations [b], [f], and [g].

Tanaka discusses “a gray scale display reference voltage generating circuit” for use with a LCD device that includes “a reference voltage generating section for producing reference voltages of a plurality of levels” and “an adjustment section for adjusting the reference voltages based upon the quantity of adjustment stored in the correction information storing section.” Ex. 1010, Abstract, ¶¶ 32–33.

a. Limitation [b]

Petitioner admits Tanaka “does not explicitly disclose the use of a multiplexer” but contends Tanaka’s user interface must provide data and gamma locations to select memory locations. Pet. 50 (citing Exs. 1010 ¶¶ 102, 143 and 1002 ¶ 123). In particular, Tanaka teaches voltage generating circuit 52 produces reference voltages and uses a basis voltage VR supplied from an external power source and a user program (UP) given by a user program such as an external control device. Ex. 1010 ¶ 102, Fig. 3; Ex. 1002 ¶ 123. A portion of Figure 3 is reproduced below to illustrate.



Partial Figure 3 Showing Memory receiving UP data.

Notably, other than a data line between the UP and memory 53 or between gamma correction adjustment circuit 54 and memory 53 in Tanaka's partial Figure 3, there is no other interface and, more specifically, no multiplexer.

Tanaka discusses storing addresses in memory 53 (Ex. 1010 ¶ 140) and how addresses are stored using "the external control device by the user" (Ex. 1010 ¶ 143). *See* Ex. 1002 ¶ 123 (quoting from Ex. 1010 ¶ 143). More specifically, Tanaka discusses that a user's operation changes the gamma correction adjustment. Ex. 1010 ¶ 143. Tanaka does not discuss or suggest using any particular interface or the recited "multiplexer" to address or program its memory (e.g., 53). Additionally, Petitioner does not explain sufficiently how these teachings map to both the "circuits for programming" and the "multiplexer" coupled to the "circuits for programming" as claim 1 requires. *See* Prelim. Resp. 43.

Petitioner also asserts that "as discussed above," an ordinary artisan would have known "one of a limited number of components would have performed this function," and thus employing a multiplexer would have been obvious. Pet. 50 (citing Ex. 1002 ¶ 123). This theory that any of a limited number of components perform Tanaka's interface function that provides data and gamma locations to memory is similar to an "obvious to try" rationale.

But, Petitioner fails to support this rationale adequately. More specifically, neither Petitioner (Pet. 49–50) nor its expert, Mr. Credelle, (Ex. 1002 ¶ 123) has identified a finite number of predictable solutions for providing Tanaka's interface or shown that an ordinary artisan would have good reasons to pursue using a multiplexer as a predictable solution for Tanaka's interface. *See KSR*, 550 U.S. at 421. In fact, Mr. Credelle testifies flash memory is programmed using decoders and gamma data. Ex. 1002

¶ 123 (referring to Section V.C. of his declaration). Mr. Credelle appears to assert Tanaka teaches its memory already has a multiplexer—not that an ordinary skilled artisan would have good reason to pursue modifying Tanaka’s memory with a multiplexer. *See* Ex. 1002 ¶ 123. Also, even assuming, without agreeing, that “*Tanaka* must necessarily provide address data and gamma locations to selected locations within the memory” (Pet. 50), this is insufficient to demonstrate one skilled in the art would have recognized trying a multiplexer for this purpose.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Tanaka renders obvious limitation [b]. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 52–53.

b. Limitations [f] and [g]

With respect to limitation [f], Petitioner contends Tanaka’s elements 51-1, 51-2, and 52-3 are the cells’ banks. Pet. 51 (citing Exs. 1010, Fig. 10 and 1002 ¶ 127). Notably, this mapping of the storage cells’ banks to element 51 is inconsistent with Petitioner’s earlier mapping of the storage cells to element 53. *Compare* Pet. 49, *with* Pet. 51. Additionally, Petitioner’s mapping to element 51 is inconsistent with Mr. Credelle’s testimony. *Compare* Pet. 51, *with* Ex. 1002 ¶ 127.

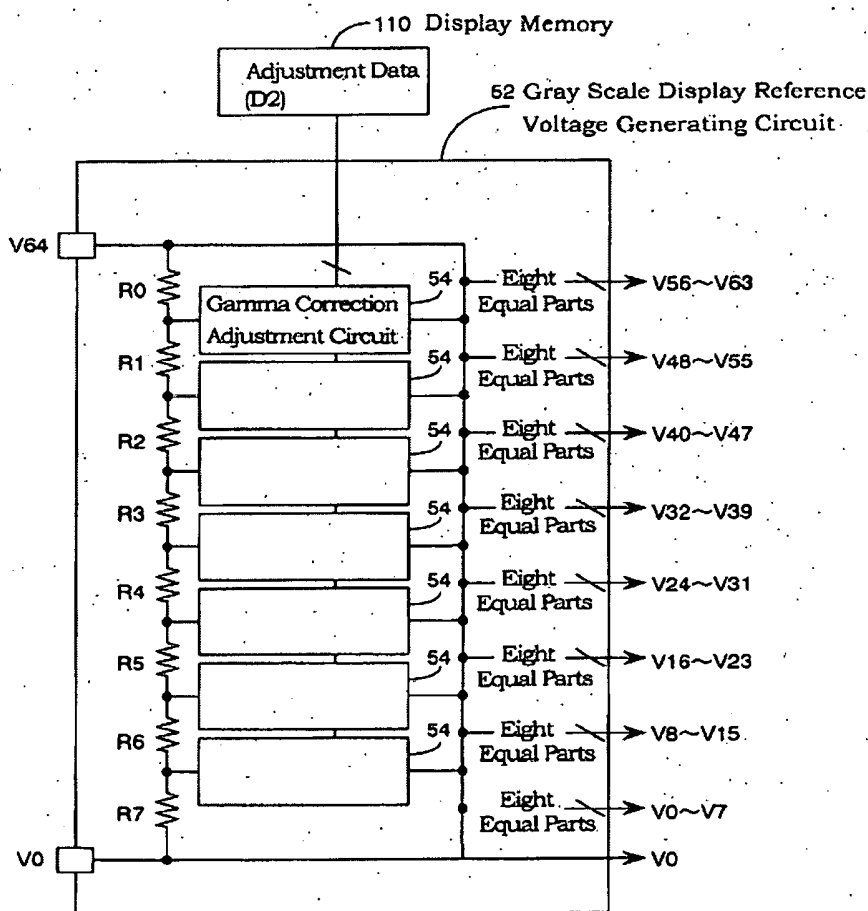
Regarding limitation [g], Petitioner asserts Tanaka teaches selecting banks based on the data’s color. Pet. 51 (citing Ex. 1002 ¶ 128). Petitioner also states Tanaka teaches multiple gamma correction curves stored in display memory and a means to switch between gamma curves depending on a row number. Pet. 51–52 (citing Exs. 1010, Fig. 20 and 1002 ¶ 128). Although indicating Tanaka uses external memory, Petitioner determines “it would have been obvious to a POSA to enlarge the memory 53 to contain

multiple sets of gamma curves.” Pet. 52 (citing Exs. 1010 ¶¶ 243–45, Fig. 33 and 1002 ¶ 130). Lastly, Petitioner states a POSA “would have understood the[three] control signals are external signals to control which bank of gamma correction data is selected from memory.” Pet. 52 (citing Exs. 1010 ¶¶ 243–245 and 1002 ¶¶ 130–131).

Patent Owner rebuts, challenging the multiple bases for concluding Tanaka teaches or suggests limitations [f] and [g]. Prelim. Resp. 45–47.

We disagree with Petitioner (Pet. 51 (citing Exs. 1010, Fig. 10 and 1002 ¶ 127)) and agree with Patent Owner (Prelim. Resp. 45–46) that Tanaka’s reference voltage generating circuits (e.g., 51-1, 51-2, and 52-3) are not banks of cells as understood by an ordinary artisan (e.g., contiguous sections of addressable, computer memory). *See* Ex. 2010 ¶ 47. Rather, they are shown as separate components from memory 53 in Tanaka’s Figure 10. Ex. 1010, Fig. 10.

Also, Tanaka’s Figure 20 below shows an alternative embodiment of gray scale display reference voltage generating circuit 52 from that in Figure 3:



Tanaka's Figure 20 Showing an Alternative Gray Scale Display Reference Voltage Generating Circuit

The above Figure 20's gray scale display reference voltage generating circuit 52 includes seven gamma correction adjustment circuits 54 generating eight equal part voltages (i.e., 64 reference voltages V0-V63) using voltage input terminals V0 and V64 and eight resistors R0 through R7. Ex. 1010 ¶¶ 109, 187, Fig. 20.

Contrary to Petitioner's assertion (Pet. 51-52), this figure does not show or suggest memory banks or a means to switch between gamma curves depending on a row number as part of "[a]n integrated circuit." See Prelim. Resp. 46. Moreover, memory 53, shown in Figure 3 and Figure 10, *noted in*

Ex. 1002 ¶ 127, is not found in Figure 20. In fact, as noted by both Petitioner (Pet. 52) and Patent Owner (Prelim. Resp. 46), display memory 110 in Figure 20 is external to circuit 52. Ex. 1010, Fig. 20. An external memory does not teach or suggest “an integrated circuit” comprising “non-volatile storage cells” along with recited limitations [b]–[g]. *See* Ex. 2010 ¶ 46.

Discussing Figure 20, Mr. Credelle quotes from Tanaka’s paragraph 186, which states adjustment data is stored in memory 110 and adjustment data type read out is varied for every gate signal line by control C. Ex. 1002 ¶ 128 (quoting Ex. 1010 ¶ 186). This teaching does not identify sufficiently a corresponding structure (i.e., a circuit, algorithm, and/or damping circuit that uses at least one bank address signal) to limitation [g]. *See* Prelim. Resp. 46.

Accordingly, Petitioner has not demonstrated adequately that Tanaka’s Figure 20 shows an integrated circuit comprising both “non-volatile storage cells” (limitation [a]) and a “means to switch between the banks [of the storage cells] based on one or more external signals” (limitation [g]) as claim 1 recites.

Petitioner further asserts an ordinary artisan would have known to enlarge memory 53 to contain Tanaka’s gamma curves. Pet. 52 (citing Exs. 1010 ¶¶ 243–245, Fig. 33 and 1002 ¶ 130); Ex. 1002 ¶ 129 (showing gamma curves in Figure 25). Cited paragraphs 243 through 245, which address Figure 32, fail to discuss enlarging memory (e.g., 53) to contain gamma curves. Exs. 1010 ¶¶ 243–245. Thus, although these passages discuss reading out data from display memory using control signals (e.g., C and C1) and cited Figure 33 shows a similar arrangement, there is insufficient evidence that Tanaka suggests to one skilled in the art enlarging

memory 53, which is mapped to the recited “non-volatile cells” in claim 1. Pet. 49 (citing Ex. 1010 ¶¶ 76, 144); *see* Ex. 2010 ¶ 49 (discussing Tanaka does not demonstrate that it would be obvious to enlarge memory to contain gamma curves).

Also, Petitioner has not sufficiently explained or identified the “rows” discussed in paragraphs 203 and 204, *noted in* Ex. 1002 ¶ 129, are storage cells’ banks, such that there is a suggestion to include a “means to switch between banks,” as claim 1 further recites. Because Petitioner does not provide sufficient evidence to have banks within memory 53 and to enlarge Tanaka’s memory 53, Petitioner has not demonstrated sufficiently to include claim 1’s limitation [g].

Mr. Credelle discusses Figure 33 and discusses three external control signals used “to control which bank of gamma correction data is selected from non-volatile display memory 110 and 137.” Ex 1002 ¶ 130. Figure 33 does not show banks in memory 110 and 137, such that Tanaka’s Figure 33 teaches or suggests to an ordinary artisan a “means to switch between banks based on one or more external signals,” as recited. Ex. 1010, Fig. 33; *see also* Ex. 1010 ¶ 241. That is, a corresponding structure to limitation [g] (i.e., a circuit, algorithm, and/or damping circuit that uses at least one bank address signal) is not shown or described. Mr. Credelle’s discussion in paragraph 132, previously addressed above, does not cure this deficiency. Ex. 1002 ¶ 132 (citing Ex. 1010 ¶¶ 243–245).

For the above reasons, Petitioner does not show sufficiently for institution purposes that Tanaka renders obvious limitations [f] and [g]. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 52–53.

d. Conclusion

Having reviewed Petitioner's and Patent Owner's assertions, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Tanaka renders challenged claims 1, 2, 4, and 5 of the '305 patent obvious.

5. Da Costa and Tsai (Ex. 1011)

Petitioner also challenges claims 1, 2, 4, and 5 as being unpatentable over Da Costa and Tsai under 35 U.S.C. § 103(a). Pet. 17, 53–58. Petitioner explains this ground is “presented to address a potential argument that *Da Costa* and/or *Tanaka* do not render obvious the claims' recitation of a ‘multiplexer.’ *Tsai*, which is combinable with *Da Costa* and with *Tanaka* for the reasons discussed below, explicitly discloses the use of a multiplexer, and the combination plainly meets this limitation.” Pet. 18, 57–58. For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Da Costa and Tsai render the challenged claims obvious.

Tsai discusses a microcomputer having embedded flash memory, which allows for (1) programming data into the memory and (2) reprogramming (e.g., update or change) data in memory without external programming tools or on-chip. Ex. 1011, Abstract, *cited in* Pet. 54. Tsai's microcomputer (e.g., 310) includes a bus multiplexer (e.g., 350) connecting a register set (e.g., 340) to flash memory (e.g., 330). Ex. 1011, 7:2–9, 49–67, Fig. 3; Pet. 54–55.

Petitioner proposes to combine Tsai with Da Costa. Pet. 55–57. In particular, Petitioner states, “A POSA reading *Tsai* would have understood that the memory programming method described therein could be used to program the integrated flash memory as disclosed by *Da Costa*” (Pet. 56–

57) (citing Ex. 1002 ¶ 149) and “would have understood that the programming process it describes would provide the memory programming details that Da Costa lacked” (Pet. 57) (citing Ex. 1002 ¶ 149).

As explained above, Petitioner does not show sufficiently for institution purposes that the proposed ground based only on Da Costa under 35 U.S.C. § 103 teaches or suggests limitations [f] and [g]. The proposed ground to combine Da Costa and Tsai does not address how Tsai would have further taught or suggested limitations [f] and [g]. Thus, the proposed ground does not rely on Tsai to teach or suggest claim 1’s limitations [f] and [g], which as previously stated are not sufficiently taught or suggested by Da Costa. We refer above for more details.

Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 36–37.

Having reviewed Petitioner’s and Patent Owner’s assertions related to Da Costa and Tsai, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Da Costa and Tsai render challenged claims 1, 2, 4, and 5 of the ’305 patent obvious.

6. Tanaka and Tsai

Petitioner also challenges claims 1, 2, 4, and 5 as being unpatentable over Tanaka and Tsai under 35 U.S.C. § 103(a). Pet. 17, 58–62. Like the proposed ground based on Da Costa and Tsai, Petitioner explains this ground is “presented to address a potential argument that” Tanaka alone does not render obvious claim 1’s “multiplexer,” asserting the combination of Tanaka and Tsai meets this limitation. Pet. 18; Pet. 60–61.

As explained above, Petitioner does not show sufficiently for institution purposes that the proposed ground based only on Tanaka under

35 U.S.C. § 103 teaches or suggests limitations [f] and [g]. The proposed ground to combine Tanaka and Tsai does not address how Tsai would have further taught or suggested limitations [f] and [g]. In fact, Petitioner states this ground is presented to address “a potential argument” (Pet. 18) that Tanaka does not render a multiplexer obvious (Pet. 18, 58). Thus, this proposed ground does not rely on Tsai to teach or suggest claim 1’s limitations [f] and [g], which as previously stated are not sufficiently taught or suggested by Tanaka. We refer above for more details.

Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. See Pet. 52–53.

Having reviewed Petitioner’s and Patent Owner’s assertions related to Tanaka and Tsai, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Tanaka and Tsai render challenged claims 1, 2, 4, and 5 of the ’305 patent obvious.

7. Petropoulos and Kang

Lastly, Petitioner also challenges claims 1, 2, 4, and 5 as being unpatentable over Petropoulos and Kang under 35 U.S.C. § 103(a). Pet. 17, 62–66. Petitioner explains, “To the extent the Board finds Ground 3 [(grounds based on Petropoulos alone)] to be lacking regarding the claimed gamma reference voltage signals in *Petropoulos*, Petitioner submits that *Kang* in combination with *Petropoulos* renders obvious the claimed gamma reference voltage signals.” Pet. 62; Pet. 18. Petitioner states, “[T]hose descriptions [of a relatively more limited discussion of gamma reference voltage signals in *Petropoulos*] would be a motivation to combine *Petropoulos* with *Kang*, which plainly discloses the gamma correction voltage-related limitations of the Challenged Claims.” Pet. 18, 62.

As explained above, Petitioner has not shown sufficiently for institution purposes that the proposed grounds based on Kang or Petropoulos alone teach certain limitations of the challenged claims. We explained above the proposed ground based only on Petropoulos does not teach or suggest limitations [b] and [g] and the proposed ground based only on Kang does not teach or suggest limitations [b], [f], and [g]. Thus, this proposed ground to combine Petropoulos and Kang does not address how the combination teaches or suggests limitations [b] and [g]. In fact, Petitioner states this ground is presented if “Petropoulos’ relatively more limited discussion of gamma reference voltage signals is deficient” (Pet. 18, 66). That is, the proposed ground does not turn to Kang to teach or suggest limitations [b] and [g], which as previously stated are not sufficiently taught or suggested by Petropoulos. We refer above for more details.

Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 28–30, 45¹⁹.

Having reviewed Petitioner’s and Patent Owner’s assertions related to Petropoulos and Kang, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Petropoulos and Kang render challenged claims 1, 2, 4, and 5 of the ’305 patent obvious.

Because this determination disposes of the Petition, no need exists to reach Patent Owner’s other arguments regarding Petitioner’s showing.

¹⁹ The proposed ground based on Petropoulos alone does not include claim 4. Pet. 17, 45.

E. Conclusions Based on Cited References

Petitioner has not established a reasonable likelihood of prevailing in challenging the following: (1) claims 1, 2, 4, and 5 as obvious over Kang; (2) claims 1, 2, 4, and 5 as obvious over Da Costa; (3) claims 1, 2, and 5 as obvious over Petropoulos; (4) claims 1, 2, 4, and 5 as obvious over Tanaka; (5) claims 1, 2, 4, and 5 as obvious over Da Costa and Tsai; (6) claims 1, 2, 4, and 5 as obvious over Tanaka and Tsai, and (7) claims 1, 2, 4, and 5 as obvious over Petropoulos and Kang.

III. CONCLUSION

For the above reasons, we determine that Petitioner has failed to demonstrate a reasonable likelihood of prevailing at trial as to any challenged claim. Accordingly, we deny institution of an *inter partes* review.

IV. ORDER

For the above reasons, it is

ORDERED that the Petition is *denied* as to the challenged claims of the '305 patent, and no *inter partes* review is instituted.

IPR2018-01255
Patent 7,233,305 B1

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WISTRON CORPORATION,
Petitioner,

v.

PHENIX LONGHORN, LLC,
Patent Owner.

Case IPR2018-01255
Patent 7,233,305 B1

Before DENISE M. POTHIER, DAVID C. McKONE, and
KAMRAN JIVANI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314(a)

I. INTRODUCTION

Wistron Corporation (“Petitioner”)¹ filed a Petition requesting an *inter partes* review of claims 1, 2, 4, and 5 of U.S. Patent No. 7,233,305 B1 (Ex. 1001, “the ’305 patent”). Paper 1 (“Pet.”), 1. Phenix Longhorn, LLC (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 10 (“Prelim. Resp.”). Patent Owner filed two, separate motions to seal Exhibits 2001 and 2009 as well as its Preliminary Response, each in its entirety. Papers 7, 11. These motions will be addressed in a separate order.²

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons stated below, we determine that the “information presented” does not “show[] there is a reasonable likelihood that . . . [P]etitioner would prevail with respect to at least 1 of the claims challenged.” *See id.* Accordingly, we do “not authorize an *inter partes* review to be instituted.” *See id.*

A. Related Proceedings

Petitioner and Patent Owner submit the ’305 patent is presently being asserted against Petitioner in Eastern District of Texas Case No. 2:17:cv-00711-RWS and against Texas Instruments in Eastern District of Texas Case

¹ Petitioner Wistron Corporation identifies itself as a real party-in-interest and states Wistron InfoComm (Zhongshan) Corporation, Zhongshan Torch Development Zone, and Wistron Mexico S.A. de C.V. “may be real parties-in-interest.” Paper 3, 2.

² This Decision does not reproduce or discuss any material the Motions to Seal identify as confidential. Accordingly, this Decision need not be sealed.

No. 2:18-cv-00020-RWS. Pet. viii; Paper 4, 2.³ Petitioner also identifies two actions in which Patent Owner asserted the '305 patent against multiple parties. Pet. viii..

B. The '305 Patent

The '305 patent is titled “Gamma Reference Voltage Generator” and is used with Liquid Crystal Displays (LCDs). Ex. 1001, Title, 1:12–14. Petitioner explains the brightness versus input voltage curve for a display’s image does not match those of a human’s vision and establishes a non-linear behavior called “gamma.” See Pet. 1–2 (citing Ex. 1002 ¶ 25); see also Pet. 2–3 (reproducing Ex. 1008, Fig. 6); see also Prelim. Resp. 5 (stating “the brightness of the LCD pixel is not a linear or straight-line function of the voltages applied” and “the human eye’s sensitivity to light is also not linear”) Due to this mismatch, the curve needs to be adjusted using gamma correction. See Pet. 1–2 (citing Ex. 1002 ¶ 25); see also Prelim. Resp. 5 (discussing controlling gamma reference voltages). The '305 patent indicates gamma correction has been a problem for Thin Film Transistor (TFT) flat panel displays. Ex. 1001, 1:19–21. Often, each display has a different response to the gamma correction reference voltages, which results in a need to generate specific gamma reference voltages for each display’s model. Ex. 1001, 1:22–25.

Traditionally, this problem has been solved using Select-On-Test Resistors, allowing reference voltages (e.g., GM_{1-16} of Fig. 1) to be fine-tuned to the display’s requirements using specific resistors (e.g., R_{1-17} of Fig. 1). Ex. 1001, 1:27–34, 1:46–2:3, Fig. 1. However, this process

³ Patent Owner mistakenly lists “2:18-cv-00720-RWS” rather than 2:18-cv-00020-RWS.

prohibits automatic assembly and testing and requires resistors to be tested, selected, and mounted manually. Ex. 1001, 1:31–34. The '305 patent's invention is “a programmable buffer integrated circuit which can be programmed to output a set of gamma correction reference voltages to be used in Liquid Crystal Displays (LCDs).” Ex. 1001, 2:16–19; *see also id.* at 2:45–51, Figs. 2–3. The described invention includes “automated assembly of an entire PC board” (Ex. 1001, 2:29–30), “automated test and gamma adjustment” (Ex. 1001, 2:30–31, 3:38–41, Fig. 2), and reprogramming gamma characteristics using gamma reference controllers (e.g., 210 and 220) (Ex. 1001, 2:32–33, 3:41–47, Fig. 2).

The '305 patent further states that the integrated circuit can store and retrieve reference voltages' banks using address inputs B0, B1, and B2. Ex. 1001, 5:50–53, 6:41. These inputs allow gamma voltages to be changed and can be used to switch between different gamma settings. Ex. 1001, 5:53–62, Fig. 6. “Having bank switching capability ensures that the optimum gamma curve is used for each individual display and eliminates the need for re-work due to display manufacturing process variations.” Ex. 1001, 7:9–12.

C. Illustrative Claim

Petitioner challenges claims 1, 2, 4, and 5 of the '305 patent. Claim 1 is representative and is reproduced below with bracketing added by Petitioner:

1. An integrated circuit for producing voltage signals on a plurality of outputs comprising:

- [a] a plurality of non-volatile storage cells;
- [b] circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs;
- [c] drivers connected to said multiplexer for addressing said storage cells; and
- [d] the plurality of inputs connected to said multiplexer for addressing said storage cells;
- [e] wherein said voltage signals are gamma reference voltage signals for determining actual driving voltages of columns of a display,
- [f] wherein said non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and
- [g] means to switch between the banks based on one or more external signals is provided on said integrated circuit.

Pet. 68; Ex. 1010, 7:45–62 (the above limitations are referred to as “limitation [a],” “limitation [b],” “limitation [c],” “limitation [d],” “limitation [e],” “limitation [f],” and “limitation [g]” throughout the Decision).

D. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1, 2, 4, and 5 of the '305 patent on the following grounds (Pet. 17):

Reference(s)	Basis	Claims challenged
Kang ⁴ (Ex. 1007)	§ 103(a) ⁵	Claims 1, 2, 4, and 5
Da Costa ⁶ (Ex. 1008)	§ 103(a)	Claims 1, 2, 4, and 5
Petropoulos ⁷ (Ex. 1009)	§ 103(a)	Claims 1, 2, and 5
Tanaka ⁸ (Ex. 1010)	§ 103(a)	Claims 1, 2, 4, and 5
Da Costa and Tsai ⁹ (Ex. 1011)	§ 103(a)	Claims 1, 2, 4, and 5
Tanaka and Tsai	§ 103(a)	Claims 1, 2, 4, and 5
Petropoulos and Kang	§ 103(a)	Claims 1, 2, 4, and 5

Petitioner also relies on the Declaration of Thomas L. Credelle.

Ex. 1002. Patent Owner relies on the Declaration of Robert J. Murphy.

Ex. 2010.

⁴ U.S. Patent Application Publication No. 2002/0063666 A1 (“Kang”).

⁵ The Leahy-Smith America Invents Act (AIA), which amended 35 U.S.C. § 103, was signed into law in 2011. The AIA’s amendments to § 103 apply to applications filed on or after March 16, 2013. Because the ’305 patent’s filing date is prior to March 16, 2013, we refer to the pre-AIA version of § 103.

⁶ U.S. Patent No. 6,100,879 (“Da Costa”).

⁷ U.S. Patent Application Publication No. 2003/0090580 A1 (“Petropoulos”).

⁸ U.S. Patent Application Publication No. 2003/0132906 A1 (“Tanaka”).

⁹ U.S. Patent No. 5,974,528 (“Tsai”).

II. ANALYSIS

A. Person of Ordinary Skill in the Art (“POSITA”)

Petitioner asserts that a person of ordinary skill in the art at the time of the invention “would have had at least a bachelor of science degree in physics, electrical engineering, or the equivalent thereof and three (3) years of experience in circuit design or display technologies.” Pet. 13 (citing Ex. 1002 ¶ 21). Petitioner adds, “[s]uch a POSA¹⁰ would have had knowledge of integrated circuits, gamma correction, and storage of gamma correction voltage values within memory, and would have understood how to search available literature for relevant publications.” Pet. 13–14 (citing Ex. 1002 ¶¶ 21–22). Petitioner support its position with Mr. Credelle’s testimony. Ex. 1002 ¶¶ 21–22, *cited in* Pet. 13–14.

Patent Owner describes the ordinary artisan similarly, indicating the artisan would have had “at least a bachelor’s of science degree in electrical engineering or physics or a related field, with at least three years of experience in the design of floating gate nonvolatile memory integrated circuits either as memory chips or embedded technology or floating gate analog design or technology.” Prelim. Resp. 16–17. Patent Owner adds “[t]his person would be aware of the state of the art in floating gate non-volatile technology and circuits by reading articles published in” various journals and patents and by attending presentations at conferences. Prelim. Resp. 17. Mr. Murphy reiterates Patent Owner’s summary. Ex. 2020 ¶ 28.

¹⁰ Like POSITA, POSA also stands for a person of ordinary skill in the art. Petitioner and Mr. Credelle use this acronym and POSITA interchangeably.

Upon review, the parties present similar skill levels for an ordinary artisan. Neither party asserts the differences in the proposed skill level would impact what an ordinary artisan would have known or recognized in the cited prior art. *See generally* Pet.; Prelim. Resp. Under either proposed skill level, our conclusions related to the proposed grounds remain the same. We further note that the prior art itself demonstrates the level of skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown”) (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

B. Claim Construction

For petitions filed before November 13, 2018, the Board interprets claim terms in an unexpired patent according to the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 100(b) (2016); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (affirming applicability of broadest reasonable construction standard to *inter partes* review proceedings). Under that standard, and absent any special definitions, we generally give claim terms their ordinary and customary meaning as would be understood by one of ordinary skill in the art at the time of the invention. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

1. “Non-volatile storage cells”

Petitioner and Patent Owner agree the phrase “non-volatile storage cells” in claim 1 means “computer memory that retains its stored data after power is removed and restores the data when power is returned to the system, such as, for example, the following: analog floating gate

non-volatile memory, Electrically Erasable Programmable Read Only Memory (EEPROM), Flash EEPROM, Ultraviolet EPROM (UVEPROM), and Non-Volatile Random Access Memory (NOVRAM).” Pet. 15–16 (citing Ex. 1002 ¶¶ 45–47); Prelim. Resp. 17. For purposes of this Decision, we adopt the parties’ agreed construction.

*2. Limitation [g]
“Means to switch between the banks
based on one or more external signals”
a. 37 C.F.R. § 42.104(b)(3)*

37 C.F.R. § 42.104(b)(3) recites, in relevant part, that an *inter partes* petition must provide a statement of the precise relief requested for each claim challenged and that the statement must identify “[h]ow the challenged claim is to be construed” and “[w]here the claim to be construed contains a means-plus-function . . . limitation as permitted under 35 U.S.C. 112[, sixth paragraph], the construction of the claim must identify the specific portions of the specification that describe the structure, material, or acts corresponding to the each claimed function.”¹¹

As explained below, we determine the “means to switch” limitation of claim 1 contains a means-plus-function limitation invoking 35 U.S.C. § 112, sixth paragraph. Petitioner does not provide a claim construction for this phrase. *See* Pet. 14–16. Patent Owner notes Petitioner’s failure to construe this phrase. Prelim. Resp. 18. At best, Petitioner indicates “each term of the Challenged Claims of the ’305 Patent [should] have its ordinary and customary meaning.” Pet. 14.

¹¹ As previously discussed, the pre-AIA statutes are applicable to the ’305 patent.

Because Petitioner has not presented a claim construction for the recited “means to switch” limitation, including identifying portions of the Specification that describe its structure, material, or acts corresponding to its claimed function as set forth in 37 C.F.R. § 42.104(b)(3), we deny institution of the Petition on this basis. Nevertheless, we proceed to construe this term and address the merits of the Petition, and, as discussed below, find additional grounds for denial.

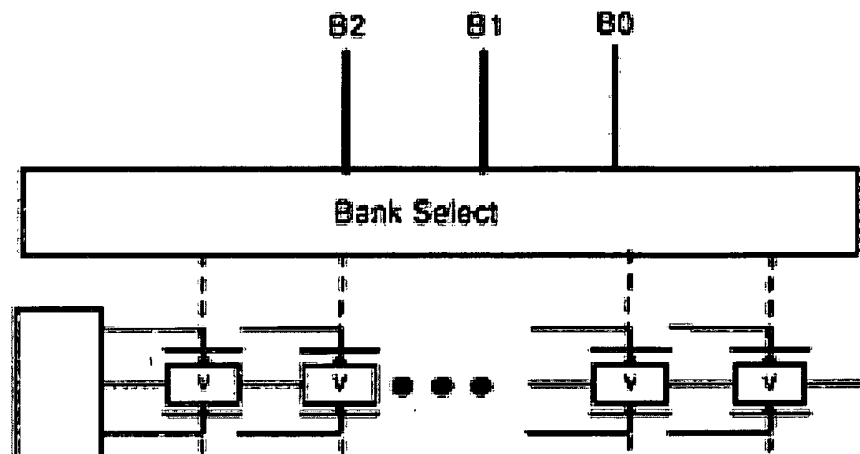
b. Provided Claim Construction

Patent Owner asserts that the “means” phrase in claim 1 “recites a means for performing a specified function” and “must be construed as a means-plus-function limitation under 35 U.S.C. § 112[, sixth paragraph].” Prelim. Resp. 18. As noted above, Petitioner does not provide a claim construction for this phrase (*see* Pet. 14–16) but indicates “each term of the Challenged Claims of the ’305 Patent [should] have its ordinary and customary meaning.” Pet. 14.

Patent Owner states “[t]he function for th[e] limitation [[g]] is switching between the banks based on one or more external signals” and identifies the function’s “corresponding structure” to include (1) the “B0-B2 address inputs” (Prelim. Resp. 18 (citing Ex. 1001, 5:50–63, Figs. 4A-B)), (2) pins for these inputs, and (3) an internal damping circuit referred to as “Bank Switch Damp Time” (Prelim. Resp. 19 (citing Ex. 1001, 5:62–66, Fig. 5)). More specifically, Patent Owner asserts the structure is shown in (1) Figure 4A as pins B0–B2 (the “Bank Select”) corresponding to Figure 4B’s pins 20, 22, and 23 and (2) Figure 6, depicting the Bank Select block with inputs B0, B1, and B2. Prelim. Resp. 18–19 (citing Ex. 1001, 5:50–63, Figs. 4A– 6).

We agree with Patent Owner that the recited phrase “means to switch between the banks based on one or more external signals” in claim 1 invokes 35 U.S.C. § 112, sixth paragraph. A phrase that uses the term “means” creates a presumption that § 112, sixth paragraph applies. *TriMed, Inc. v. Stryker Corp.*, 514 F.3d 1256, 1259 (Fed. Cir. 2008). Also, “[m]eans-plus-function claiming applies only to purely functional limitations that do not provide the structure that performs the recited function.” *Phillips v. AWH Corp.*, 415 F.3d at 1311 (Fed. Cir. 2005); *see also Welker Bearing Co. v. PHD, Inc.*, 550 F.3d 1090, 1095–96 (Fed. Cir. 2008). The recited functional limitation of “switch[ing] between the banks based on one or more external signals” in claim 1 does not provide the structure that performs this recited function. For example, claim 1 does not recite a specific circuit, algorithm, or damping circuit involved in performing the claimed function. Thus means-plus-function claiming applies to limitation [g].

The '305 patent describes an integrated circuit “termed the AG1818” having the capacity to retrieve eight independent banks. Ex. 1001, 5:30–31, 5:50–52. The '305 patent states the AG 1818’s “banks of gamma voltage are . . . selected through the three address inputs B0, B1, and B2” (Ex. 1001, 5:52–53) and “the bank [is] selected by the B0-B2 address inputs” (Ex. 1001, 5:61–62). Address signals B0 through B2 are shown in Figure 6. Ex. 1001, Fig. 6. Part of Figure 6’s block diagram is reproduced below with address signals, B0, B1, and B2 entering a “Bank Select” block:



Part of Figure 6's Block Diagram of an Alternative Embodiment
Ex. 1001, 2:56–57, 5:58–59. The '305 patent further states, "This feature can also be used to switch between different gamma settings based on the information to be displayed for implementing dynamic gamma correction." Ex. 1001, 5:56–58. Figure 4A further describes B0 through B2 as "Bank Select" signals (Ex. 1001, Fig. 4A), later explaining "the particular bank is addressed through B0-B2" (Ex. 1001, 6:41). Based on this description, we agree with Patent Owner that the structure corresponding to the means to switch is the B0–B2 address inputs, pins for these inputs, the bank select box, and equivalents thereof.

Additionally, the '305 patent describes "an internal damping circuit" that can be used during "read mode" to "create[] a slow transition, about 10 msec., between banks to prevent disruptive display artifacts." Ex. 1001, 5:60, 5:62–64, Fig. 5 (showing and describing "Tdamp" and "Bank Switch Damp Time"); *see also* Ex. 1001, 5:66–6:2. We agree with Patent Owner that the described internal damping circuit in the '305 patent, and equivalents thereof, are additional structure corresponding to performing the function of switching between the banks based on external signals.

Although neither party construes the following terms, we present a claim construction to address the grounds presented in the Petition.

c. “a multiplexer”

The '305 patent discusses and shows a multiplexer (e.g., mux 320) that connects signals from programming engine 310 to “any one of the programmable analog floating gate memory cells 330 through 337, depending on three address inputs (A_0 , A_1 , and A_2).” Ex. 1001, 3:56–4:3, Fig. 3; Ex. 1002 ¶ 30 (citing same). Although this describes the recited “multiplexer,” this discussion and Mr. Credelle’s accompanying testimony (Ex. 1002 ¶ 30 (stating “the multiplexer . . . is a device used to select which memory cell is addressed by the ‘plurality of inputs’ A_0 , A_1 , and A_2 ”)) merely address the result of using a multiplexer rather than what a multiplexer is. Thus, we consult a dictionary for a customary understanding of “multiplexer” to an ordinarily skilled artisan.

THE AUTHORITATIVE DICTIONARY OF IEEE STANDARD TERMS defines a “multiplexer” as:

multiplexer (A) (supervisory control, data acquisition, and automatic control) A device that allows the interleaving of two or more signals to a single line or terminal. (B) (supervisory control, data acquisition, and automatic control) A device for selecting one of a number of inputs and switching its information to the output.

(2) (A) A device that allows the transmission of a number of different signals simultaneously over a single channel or transmission facility. Synonym: multiplexor. (B) A device capable of interleaving the events of two or more activities or of distributing the events of an interleaved sequence to their respective activities. Contrast: demultiplexer

THE AUTHORITATIVE DICTIONARY OF IEEE STANDARD TERMS 716 (Kim Breitfelder & Don Messina eds., St'd Info. Network IEEE Press 7th ed. 2000).

Figure 3 of the '305 patent shows six signals entering multiplexer 320 and three exit to "any one of the programmable analog floating gate memory cells 330 through 337, depending on three address inputs (A_0 , A_1 , and A_2)."

Ex. 1001, 3:56–4:3, Fig. 3. This multiplexer arrangement is more than a device that allows simultaneous transmission of different signals over a single channel like above definition (2). Rather, the description in the specification is most consistent with the first definition quoted above.

Accordingly, consistent with the '305 patent's Specification, we determine the recited "multiplexer" includes a device that interleaves signals to a single line, or selects one input and switches its information to the output.

d. "banks of cells"

The '305 patent states the integrated circuit, termed the AG1818, has the capacity for eight banks, which are selected through three address signals B0 through B2 (not shown). Ex. 1001, 5:30–31, 50–53, Fig. 4. But, the '305 patent does not show or define a cell's bank. *See generally* Ex. 1001. Given the absence of any explicit definition, we generally give the term "bank" its ordinary and customary meaning as would be understood by one of ordinary skill in the art at the time of the invention.

Consulting THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS, the definition of "bank" most relevant to this proceeding is the following:

(2) (A) One or more disk drives lined up in a row. (B) Any group of similar devices that are connected together for use as a single

device. For example, a row of light-emitting diodes connected to form a display. (C) A contiguous section of addressable memory. For example, eight memory devices, each of which is 64 kB by 1; forming a 64 kB X 8 memory bank.

THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS 85 (Kim Breitfelder & Don Messina eds., St'd Info. Network IEEE Press 7th ed. 2000) (def. 2).

Because, as noted above, both Petitioner and Patent Owner agree the recited “storage cells” relate to computer memory, we conclude definition 2(C) is the most relevant to the phrase “banks of cells.” Thus, we determine the claimed “banks of cells” are contiguous sections of addressable, computer memory.

No other claim term requires express construction.

C. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.¹² *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

¹² Neither party presents arguments regarding objective evidence of nonobviousness here.

D. Obviousness Grounds

Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over seven grounds. Pet. 17–66. Patent Owner present arguments contending the grounds do not teach or suggest claim 1’s preamble and limitations [b]–[d], [f] and [g]. Prelim. Resp. 22–62 . Having reviewed Petitioner’s assertions, Patent Owner’s arguments, and the references, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing the unpatentability of the challenged claims based on any of the above-identified grounds. We focus on independent claim 1 for each of the proposed grounds.

1. Kang (Ex. 1007)

Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over Kang under 35 U.S.C. § 103(a). Pet. 18–30. To support its contentions, Petitioner cites to Mr. Credelle’s declaration testimony (Ex. 1002). Patent Owner presents several arguments, including that Kang does not teach or suggest claim 1’s preamble and limitations [b], [d], [f], and [g]. Prelim. Resp. 22–27. Patent Owner cites to Mr. Murphy’s declaration testimony (Ex. 2010).

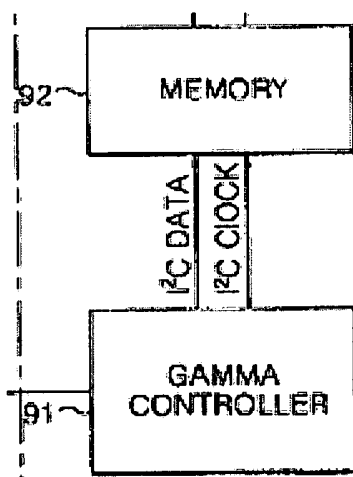
For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Kang renders claim 1 obvious. We focus on limitations [b], [f], and [g].

As background, Kang discusses “[a] gamma voltage and video data correcting apparatus and method in a liquid crystal display . . . , wherein the gamma data for controlling the gamma voltage is stored for each of at least two modes.” Ex. 1007, Abstract.

a. Limitation [b]

*“circuits for programming coupled to a multiplexer
for addressing and programing said storage cells”*

For this limitation, Petitioner maps Kang’s gamma controller 91 to a “circuit for programming.”¹³ Pet. 24–25 (citing Exs. 1007 ¶ 52 and 1002 ¶ 55). Petitioner states the gamma controller circuit is coupled to storage cells (e.g., memory 92 in Fig. 9) through an I²C interface, which Petitioner contends is “a common serial interface.” Pet. 24 (citing Exs. 1007 ¶ 52 and 1002 ¶ 55). Petitioner argues Kang’s I²C interface provides instructions as to where in the memory the data is to be written. *Id.* (citing Exs. 1007 ¶ 52 and 1002 ¶ 55). Kang’s I²C interface, shown in Figure 9, follows:



Partial View of Kang’s Figure 9 showing an I²C interface.

Petitioner concludes an ordinarily skilled artisan “would have understood that the use of a serial interface over a multiplexer is an obvious modification . . . because, since a multiplexer and an I²C serial interface perform identical functions within an integrated circuit, these commodity components are replaceable and do not alter the operation of the device.”

¹³ Claim 1 recites “circuits for programming” not “circuit for programming.” Ex. 1001, 7:48 (emphasis added).

Pet. 24 (citing Ex. 1002 ¶ 55 and *In re Japikse*, 181 F.2d 1019 (CCPA 1950)).

Patent Owner rebuts. Prelim. Resp. 23–25. Patent Owner argues Petitioner “does not explain where Kang discloses a multiplexer because Kang does not.” Prelim. Resp. 24 (citing Ex. 1002 ¶ 57). Petitioner does not contend otherwise. Pet. 24 (noting Kang discloses an I²C serial interface and proposing to modify the serial interface with a multiplexer). That is, Kang discloses that an I²C connects gamma controller 91 to memory 92 and transmits I²C data and clock data to memory 92. Ex. 1007 ¶ 52, Fig. 9. On the current record, Kang does not disclose the recited “multiplexer” of claim 1.

Patent Owner also contends Petitioner provides no support through its expert or documentary evidence for the statement that an artisan would have understood that the use of a serial interface instead of a multiplexer is an obvious modification. Prelim. Resp. 24. Patent Owner argues that “a multiplexer and an I²C serial interface do not perform the same function within an integrated circuit and therefore are not interchangeable.” Prelim. Resp. 25 (citing Ex. 2010 ¶¶ 39–40). We agree with Patent Owner for the following reasons.

Mr. Credelle testifies that an I²C serial interface is a common serial interface. Ex. 1002 ¶ 55 (citing Ex. 1013¹⁴). We agree Exhibit 1013 supports that an I²C bus, which is shown in Kang’s Figure 9, includes a serial data line and serial clock line. Ex. 1013, p. 1 § 1.0. Exhibit 1013 also outlines various “features of the I²C bus,” including having two bus lines

¹⁴ Philips Semiconductors, THE I²C-BUS AND HOW TO USE IT (INCLUDING SPECIFICATIONS) 1–24 (1995).

(data and clock), data corruption properties (e.g., collision detection and arbitration), bidirectional data transfer, and on-chip filtering. Ex. 1013, p. 1 § 1.0.

Comparing the above understandings of “multiplexer” with an I²C bus, we disagree the two perform identical functions as Petitioner asserts. Pet. 24. A multiplexer functions to interleave signals to a single line or to select one input and switch its information to the output. *Id.* An I²C bus, like that in Kang and like that discussed in Exhibit 1013, does not discuss interleaving signals to a single line (e.g., the I²C data with I²C clock), or selecting one input and switching its information to the output. For example, Kang shows and describes that its I²C lines separately enter memory 92 but does not discuss interleaving signals or switching its information. Ex. 1007 ¶ 52, Fig. 9. Nor does our understanding of a multiplexer’s functions include performing data corruption, bidirectional data transfer, and on-chip filtering, like that of an I²C bus. Ex. 1013, p. 1 § 1.0. Mr. Murphy also testifies an ordinary artisan would not understand an I²C interface is equivalent to a multiplexer. Ex. 2010 ¶ 39.

Moreover, Petitioner’s evidence does not support its contention that a skilled artisan would have made the “simple . . . design choice” of modifying Kang with a multiplexer. Pet. 24; *see Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”). Petitioner cites Mr. Credelle’s testimony. Pet. 24 (citing Ex. 1002 ¶ 55). Mr. Credelle, however, does not testify that it would have been obvious to modify Kang. Rather, Mr. Credelle testifies that Kang discloses a multiplexer, which, as noted above, is not Petitioner’s contention.

Ex. 1002 ¶ 55 (“As already discussed, flash memory includes multiplexers, e.g., row and column decoders, to determine where to write data.”). Thus, the Petition is deficient for failing to identify a reason to modify Kang.

As to Mr. Credelle’s testimony that flash memory includes multiplexers to determine where to write data, Mr. Credelle cites, without specificity, to Exhibit 1014. Ex. 1002 ¶ 55 n.6 (citing Ex. 1014¹⁵). Exhibit 1014 discusses flash memory and non-volatile memory, such as EEPROM, EEPROM, and Flash (Ex. 1014, pp. 1–2), and Kang discloses that memory 92 can be EEPROM or EPROM (Ex. 1007 ¶ 53, *noted in* Ex. 1002 ¶ 61). However, Mr. Credelle does not identify where Exhibit 1014 discusses or addresses multiplexers. Thus, just as Petitioner or its expert has not identified where Exhibit 1014 demonstrates flash memory includes a multiplexer, one skilled in the art would not have recognized that Kang’s memory includes a multiplexer.

As for Mr. Credelle testimony that “[a]s already discussed, flash memory includes multiplexers, e.g., row and column decoders, to determine where to write data,” Mr. Credelle does not cite to any particular support for this statement. Ex. 1002 ¶ 55. Presuming he refers to paragraphs 30 through 32 under Section C, titled “Multiplexer for Addressing Memory” (Ex. 1002, p. 12),¹⁶ this testimony merely supports Petitioner’s argument that a multiplexer is any device used to select a memory cell addressed by a plurality of address inputs, an argument we reject above.

¹⁵ Roberto Bez et al., *Introduction to Flash Memory*, 91 PROC. OF THE IEEE 1–14 (2003).

¹⁶ Mr. Credelle first discusses a flash memory cell that uses row and column decoders under this section.

In paragraphs 30 through 32, Mr. Credelle discusses how the '305 patent describes a multiplexer that connects signals from an engine to storage cells. Ex. 1002 ¶ 30 (citing Ex. 1001, 3:56–4:3). From this discussion, Mr. Credelle defines a “multiplexer” in claim 1 as “a device used to select which memory cell is addressed by the ‘plurality of inputs’ A₀, A₁, and A₂.” Ex. 1002 ¶ 30. But, as noted above, a multiplexer is not simply any device that selects a memory cell based on a plurality of address inputs. Rather, it is a device that interleaves signals to a single line or selects one input and switches its information to the output.

Lastly, we note the proposed ground relies on Kang alone, not Kang and Fazio,^{17,18} to teach claim 1’s limitation [b]. Pet. 18, 24–25. As proposed, we determine an ordinary artisan would not have understood that using a multiplexer over Kang’s I²C bus interface “is an obvious modification” and that the an I²C bus interface is replaceable by the multiplexer without altering Kang’s device. Pet. 24.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Kang renders obvious limitation [b] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. See Pet. 28–30.

¹⁷ Ex. 1012 (U.S. Patent No. 5,677,869 (Oct. 14, 1997) (“Fazio”), *noted in* Ex. 1002 ¶¶ 31–32.

¹⁸ *In re Hoch*, 428 F.2d 1341, 1342 n.3 (CCPA 1970) (“Where a reference is relied on to support a rejection, whether or not in a ‘minor capacity,’ there would appear to be no excuse for not positively including the reference in the statement of the rejection.”).

*b. Limitation [f]
“said non-volatile storage cells are organized
into two or more banks of cells”*

For this limitation, Petitioner points to two passages in Kang. Pet. 27–28. Petitioner notes Kang discloses a gamma voltage correcting apparatus includes memory “for storing gamma data for controlling a gamma voltage for each of at least two modes.” Pet. 27 (citing Ex. 1007 ¶ 22 and Ex. 1002 ¶ 59). Petitioner further indicates Kang discloses four modes with different gamma voltages. Pet. 27–28 (citing Ex. 1007 ¶ 59 (Table I) and Ex. 1002 ¶ 59); Ex. 1002 ¶ 61 (citing Ex. 1007 ¶¶ 59–60). Petitioner asserts an ordinary artisan would have understood the two or more modes as disclosed by Kang demonstrates Kang’s gamma generator has two or more banks. Pet. 28 (citing Ex. 1002 ¶ 59).

Patent Owner disagrees. Prelim. Resp. 26. Patent Owner argues Kang discloses memory block 92 with no details how the memory is organized. Prelim. Resp. 26. We agree. Kang discloses multi-mode gamma voltage generator 84 having memory 92, which can be an EEPROM or EPROM. Ex. 1007 ¶¶ 51–53, Figs. 8–9. No further information related to memory 92’s design or architecture is provided. *See* Ex. 1007 ¶¶ 51–53, Figs. 8–9. Even more, Kang does not teach or suggest that the modes are organized in memory as contiguous sections of addressable, computer memory (i.e., as “banks” as construed above).

Kang also discusses “storing a gamma data for controlling a gamma voltage for each of at least two modes.” Ex. 1007 ¶ 22, Abstract. Kang addresses “gamma reference voltages . . . for each mode, Modes A to D” and provides TABLE 1, showing modes A to D. Ex. 1007 ¶ 59. Quoting from these same passages, Mr. Credelle determines “Kang clearly teaches that the

multi-mode gamma generator has two or more banks that contain predetermined gamma reference voltages.” Ex. 1002 ¶ 59. Relying on Mr. Credelle’s testimony and Kang’s multi-mode discussion, Petitioner concludes an ordinary skilled artisan would have understood this discussion of “modes” equates to banks. See Ex. 1002 ¶ 59. We find this position unpersuasive.

As noted above, Kang does not discuss organizing its memory using banks of two or more contiguous memory portions. Ex. 1007 ¶¶ 51–53, Figs. 8–9. Additionally, Kang does not discuss how the mode’s data would be stored in memory, such that they suggest, to one skilled in the art, organizing the cells into “two or more banks” as recited. Ex. 1007 ¶¶ 22, 59, Abstract. Mr. Credelle’s testimony on this feature relies on the same passages without further explanation of how Kang’s modes suggest organizing Kang’s memory into two or more banks. Ex. 1002 ¶ 59.

For the previous reasons, Petitioner does not show sufficiently for institution purposes that Kang renders obvious limitation [f]. Claims 2, 4, and 5 depend respectively from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. See Pet. 28–30.

c. Limitation [g]
“means to switch between the banks based on one or more external signals”

Petitioner contends the gamma generator switches between modes using the disclosed control means that accesses data, and a LCD receives an external mode signal to select gamma data from memory. Pet. 28 (citing Exs. 1007 ¶ 22 and 1002 ¶ 60). Petitioner argues an ordinary artisan would

have understood this control means provides the external signal to switch between modes (e.g., banks). Pet. 28 (citing Ex. 1002 ¶ 60).

Kang describes a “control means for accessing the gamma data in response to an instruction” and “a mode selected by the control means.” Ex. 1007 ¶¶ 22, 49; Ex. 1002 ¶ 60. But, any details of how the control means selects a mode is lacking, such that Kang fails to teach or suggest the structure that controls how the control means switches between modes. As previously discussed, Kang’s modes do not clearly correspond to the recited “banks” (e.g., contiguous sections of addressable, computer memory).

Furthermore, Petitioner has not explained further how Kang’s “control means” teaches an equivalent to the recited “means to switch between banks” in claim 1. Pet. 27–28.

Mr. Credelle further discusses Kang’s claim 29 and paragraphs 59, and 60 to teach limitation [g]. Ex. 1002 ¶¶ 60–61. Kang discusses outputting specified mode gamma reference voltages, shown in Table I, “in accordance with a logical value of the gamma data” (Ex. 1007 ¶¶ 59–60) or setting gamma data in response to modes corresponding to peripheral equipment (Ex. 1007 ¶ 66). Lacking, however, is a discussion of structure to switch between memory banks. Notably, Kang’s discussion addresses (1) what happens at multi-channel DAC (digital to analog converter) 93, which interprets gamma data *from* memory 92 (Ex. 1007 ¶ 54), and (2) what is outputted from DAC 93 (e.g., gamma reference voltages in accordance with a logical value). Ex. 1007 ¶ 60, Figs. 9–10. This does not relate to how to switch any banks within memory 92, such that the DAC’s output switches between storage cells’ banks. *See* Ex. 1007 ¶¶ 60, 66, Figs. 9–10.

Claim 29 in Kang also recites storing gamma data in memory and selecting specific gamma data in memory based on a received external mode

signal. Ex. 1007, claim 29. Although this might suggest selecting data associated with a specific mode from memory based on an external signal, the claim does not recite or suggest the corresponding structure to switch between memory banks (e.g., a circuit, algorithm, and/or damping circuit that uses at least one bank address signal). Petitioner also fails to address adequately how the selections within memory in Kang are achieved such that Kang suggests to one skilled in the art the noted structure (e.g., a bank select circuit, algorithm, pins, and/or damping circuit that uses at least one bank address signal) for switching between memory or “storage cells” banks based on at least one received external signal as recited in claim 1.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Kang renders obvious limitation [g]. Claims 2, 4, and 5 depend respectively from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 28–30.

d. Conclusion

Having reviewed Petitioner’s and Patent Owner’s assertions related to Kang, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Kang renders the challenged claims 1, 2, 4, and 5 of the ’305 patent obvious.

2. Da Costa (Ex. 1008)

Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over Da Costa under 35 U.S.C. § 103(a). Pet. 17, 30–37. To support its contentions, Petitioner cites Mr. Credelle’s testimony. Ex. 1002. Patent Owner presents several arguments, including that Da Costa does not teach or suggest claim 1’s preamble and limitations [b]–[d], [f] and [g]. Prelim. Resp. 29–35. Patent Owner cites Mr. Murphy’s testimony. Ex. 2010.

For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Da Costa renders the challenged claims obvious. We focus on claim 1's limitations [b], [f], and [g].

Da Costa discusses “[a] smart controller chip for controlling an active matrix display.” Ex. 1008, Abstract. “The combination of D/A [digital/analog] analog circuitry and standard digital logic makes the controller uniquely suited for addressing all the panel control needs both for the normal digital functions but also for control of the analog aspects of the panel, like display gamma.” Ex. 1008, 2:37–41.

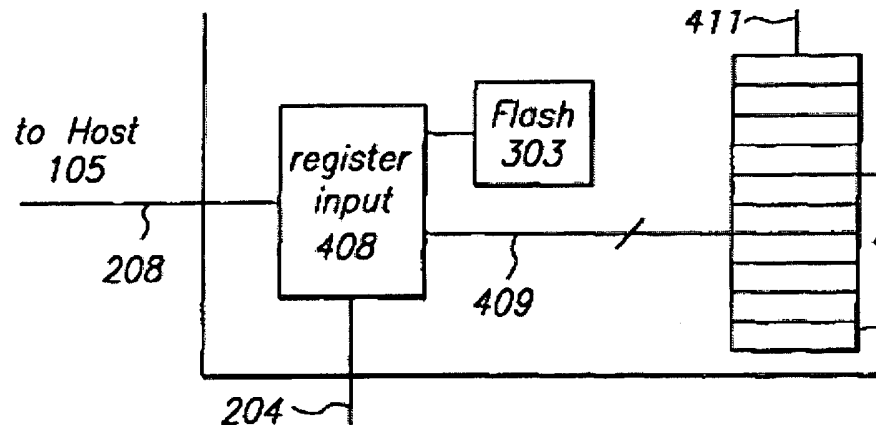
a. Limitation [b]

For this limitation, Petitioner states Da Costa's multiple address lines are used to write the data within memory and registers program the memory with a serial bus. Pet. 33 (citing Exs. 1008, 6:56–60, 11:29–32 and 1002 ¶¶ 77–78). Petitioner contends “a serial bus is an addressing circuit that is interchangeable with a multiplexer,” rendering this limitation obvious. Pet. 33 (citing Ex. 1002 ¶ 55). Petitioner also states Da Costa “does not explicitly describe programming the flash memory 303” but such an arrangement would be obvious to an ordinary artisan. Pet. 33 (citing Ex. 1002 ¶ 78).

Patent Owner argues Petitioner does not explain what in Da Costa provides the multiplexer and disputes that a serial bus is interchangeable with a multiplexer. Prelim. Resp. 31.

Da Costa discloses that register input circuitry 408 receives digital values (e.g., signals) through first serial bus 204 and second serial bus 208 from host system 105 in Figure 4A. Ex. 1008, 6:56–58, Fig. 4A. Da Costa's Figure 4A, partially shown below, illustrates a smart controller chip

(e.g., 202) with serial buses 204 and 208 (discussed in column 6 as cited) entering register input 408.



Partial View of Da Costa's Figure 4A with serial buses.

Ex. 1003, 3:29–30. Da Costa teaches flash memory (e.g., 303 in Figure 4A) integrated into a smart controller chip (e.g., 202), the flash memory being mapped to the recited “non-volatile storage cells.” Pet. 32–33 (citing Exs. 1008, 2:55–59 and 1002 ¶¶ 76–77).

Although Da Costa's Figure 4A may suggest to an ordinary artisan using inputs from the host and/or register inputs to program flash memory 303 (Pet. 33), Petitioner has not demonstrated sufficiently that Da Costa's serial buses act as an addressing circuit that is interchangeable with a multiplexer. Pet. 33. As previously discussed, claim 1 requires “a multiplexer” separate from and coupled to the “circuits for programming.” Pet. 68. For reasons similar to those discussed above when addressing Kang, the record does not demonstrate sufficiently that (1) a serial bus is interchangeable with a multiplexer or performs the identical function of a multiplexer, (2) Da Costa's flash memory includes or suggests a multiplexer, (3) Da Costa teaches or suggests using decoders somewhere between its host and its flash memory (e.g., 303), or (4) a structure connected to flash

memory 303 that behaves like a device that interleaves signals into a single line, or selects one input and switches its information to the output, which is the customary understanding of a multiplexer. We refer to our discussion of this limitation for Kang, above, for more details.

Mr. Credelle cites to other passages in Da Costa to teach limitation [b]. Ex. 1002 ¶ 84 (citing Ex. 1008, 2:47–49, 6:41–49, 6:62–67). Da Costa states a smart controller chip includes registers that contain values but fails to discuss a multiplexer. Ex. 1008, 2:47–49. Da Costa further discusses the structure within Figure 4A’s block diagram, which includes multiplexer circuitry 413. Ex. 1008, 6:41–49, 62–67, Fig. 4A. However, multiplexer circuitry 413 is located after flash memory 303 and registers 410, not connected to the mapped storage cells (e.g., flash memory 303). Ex. 1008, Fig. 4A. The proposed grounds fails to explain sufficiently how this multiplexer is involved in “addressing and programming said storage cells,” which is mapped to flash memory 303. Pet. 33.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Da Costa renders obvious limitation [b] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. See Pet. 36–37.

b. Limitation [f]

For limitation [f], Petitioner states Da Costa teaches ten separate gamma curves in flash memory and one skilled in the art would have understood storing the curves in multiple banks. Pet. 35 (citing Exs. 1007, Figs. 4A and 7A and 1002 ¶ 82). Patent Owner argues Da Costa fails to discuss how its memory is organized, including organized in banks, and one

skilled in the art would not have understood its memory is organized in banks. Prelim. Resp. 32–33 (citing Exs. 1008, 8:48–50, Fig. 7A and 2010 ¶ 43).

Da Costa discloses flash memory 303 with no details of how the memory is organized. Ex. 1008, Fig. 4A. Figure 7A shows the details of registers 410, lines 412, multiplexer circuit 413, lines 415, and high-power analog output circuitry 416 or low-power analog output circuitry 450 in Figure 4A, which are located after register input 408 and flash memory 303. Ex. 1008, 3:29–30, 3:38–42, 6:62–67, 7:38–39, 8:48–51, Figs. 4A–B, 7A. As discussed above, Petitioner has mapped the storage cells to flash memory 303, not to other structure, such as registers 410. Pet. 32–33 (citing Exs. 1008, 2:55–59 and 1002 ¶¶ 76–77). Also, the order in which these components are arranged does not demonstrate specifically how the “non-volatile storage cells are organized,” as recited in claim 1 and as mapped by Petitioner. Prelim. Resp. 33.

Mr. Credelle testifies, “The gamma curves are stored in flash memory 303 and transmitted to registers 410 through bus 409.” Ex. 1002 ¶ 82 (citing Ex. 1008, Fig. 4A) (bolding omitted). Assuming Mr. Credelle is correct, this fails to disclose *how* the stored curves are arranged in memory, such that its storage cells “are organized into two or more banks of cells” (i.e., into contiguous sections of addressable, computer memory) as claim 1 requires.

Mr. Credelle further maps limitation [f] to various passages in Da Costa. Ex. 1002 ¶ 84 (citing Ex. 1008, 9:1–16, 11:29–33, Figs. 7A–B). Figure 7B is similar to Figure 7A and suffers from the problems previously identified for Figure 7A. Ex. 1008, Fig. 7B. The remaining cited passages fail to discuss memory banks, and Mr. Credelle provides no further explanations of these passages. Ex. 1002 ¶ 84.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Da Costa renders obvious limitation [f] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 36–37.

c. Limitation [g]

We agree with Patent Owner that limitation [f], the banks, are not taught or suggested by Da Costa. Prelim. Resp. 33. Moreover, even if Da Costa did teach the recited “banks,” Petitioner has not shown that it teaches limitation [g].

Petitioner further states Da Costa teaches registers 410 connected to chip control circuitry and multiplexer circuitry and the multiplexer circuitry is connected to chip control circuitry and the high-power analog output circuitry. Pet. 35 (citing Exs. 1008, 7:1–9 and 1002 ¶ 83). Da Costa describes and shows chip register 410 connected to MUX 413 and control circuitry 406 and MUX 413 connected to high-power analog output 416. Ex. 1008, 6:62–7:9, Figs. 4A, 7A. As noted above, these circuits are located after flash memory 303. Like Patent Owner, we are not convinced that how these components are connected to each other or how these components would be involved in switching between any purported banks located in Da Costa's storage cells (e.g., 303) to demonstrate limitation [g]. Prelim. Resp. 34.

Petitioner further contends Da Costa's serial bus 208 is used to communicate information between first smart controller 202 and host system 105, which allegedly allows for dynamic modification of the analog reference levels and column/row control signal output by the first smart controller 202. Pet. 35–36 (citing Ex. 1008, 5:1–6). Petitioner states an

ordinary artisan “would have understood this disclosure to describe means to switch between banks using control circuitry 406” based on external input from host 105. Pet. 36 (citing Ex. 1002 ¶ 83). Once again, control circuit 406 is located after flash memory 303. Ex. 1008, Fig. 4A. Petitioner does not establish how this circuit is involved in switching between any purported banks of the storage cells.

The cited passages of Da Costa fail to describe sufficiently structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses at least one bank address signal) corresponding to the recited means in claim 1, including any structure that permits switching between any alleged banks located within Da Costa’s flash memory 303 based on received signals communicated over bus 208. Prelim. Resp. 33–35.

Mr. Credelle further maps limitation [g] to column 11 in Da Costa. Ex. 1002 ¶ 84 (citing Ex. 1008, 11:29–33, 11:41–46). Besides quoting passages from column 11, Mr. Credelle provides no further explanation. Ex. 1002 ¶ 84. Da Costa discusses host system 105 may have software to select between different preprogrammed curves. Ex. 1008, 11:29–33, 41–46. However, selecting between curves fails to teach or suggest a corresponding structure for switching between storage cells’ banks, as claim 1 requires, or its equivalent.

Lastly, Petitioner has not further elaborated on how Da Costa’s purported “means” teaches an equivalent to the recited “means to switch between banks” in claim 1. Pet. 27–28.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Da Costa renders obvious limitation [g] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the

dependent claims does not cure the deficiency of its showing for claim 1.
See Pet. 36–37.

d. Conclusion

Having reviewed Petitioner’s and Patent Owner’s assertions related to Da Costa, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Da Costa renders the challenged claims 1, 2, 4, and 5 of the ’305 patent obvious.

3. Petropoulos (Ex. 1009)

Petitioner also challenges claims 1, 2, and 5 as being unpatentable over Petropoulos under 35 U.S.C. § 103(a). Pet. 17, 37–45. To support its contentions, Petitioner cites Mr. Credelle’s testimony (Ex. 1002). Patent Owner presents several arguments, including Petropoulos does not teach or suggest claim 1’s preamble and limitations [b], [d], and [g]. Prelim. Resp. 39–40. Patent Owner cites Mr. Murphy’s testimony (Ex. 2010).

For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Petropoulos renders claim 1 obvious. We focus on limitations [b] and [g].

Petropoulos discusses “a programmable analog/multi-level memory array for modifying individual outputs . . . in order to obtain a desired sensor array output.” Ex. 1009, Abstract. “The memory array can be programmed with data corresponding to desired modifications, such as . . . gamma correction.” Ex. 1009, Abstract.

a. Limitation [b]

For limitation [b], Petitioner states Petropoulos discloses an address signal generator that provides address signals indicative of row/column addresses, for selecting one of memory cells C11 to CMN to write data values. Pet. 41 (citing Exs. 1009 ¶ 31 and 1002 ¶ 102). Petitioner further

states an address signal generator can be a buffer circuit for generating address signals from addresses provided by external circuitry. Pet. 42 (citing Exs. 1009 ¶ 31 and 1013 ¶ 103). Without stating what circuitry maps to the multiplexer, Petitioner contends an ordinary artisan would have understood the address signal generator programs and addresses storage cells based on multiple inputs (Pet. 41–42 (citing Exs. 1009, Fig. 3 and 1002 ¶ 102)) and that “the decoder tree and other elements within memory are circuits for programming” (Pet. 42 (citing Ex. 1002 ¶ 103)).

Patent Owner contends Petitioner does not explain or specify where the multiplexer is in Petropoulos. Prelim. Resp. 39. We agree. The Petition discusses an “address signal generator” for selecting a memory cell and a buffer circuit for generating address signals but never states the generator or buffer circuit is a multiplexer. Pet. 41–42. Likewise, the Petition states the decoder tree and other elements within memory are circuits for programming but does not explain adequately how these components are a multiplexer as claim 1 requires. Pet. 42.

Cited paragraph 31 of Petropoulos does not assist in clarifying the mapping. Ex. 1009 ¶ 31. Petropoulos discusses address signal generator 320, which can be a buffer circuit, provides address signals for a selected memory cell (e.g., C11–CMN) to which the data value will be written. Ex. 1009 ¶ 31, Fig. 3; Ex. 1002 ¶ 102 (citing Ex. 1009 ¶ 31, Fig. 3). Petropoulos does not discuss how address signal generator 320 behaves like a multiplexer as commonly understood by an ordinary skilled artisan (i.e., a device that interleaves signals to a single line, or selects an input and switches its information to the output). Ex. 1009 ¶ 31, Fig. 3.

Likewise, Petitioner and Mr. Credelle have not explained sufficiently how Figure 3’s decoder tree and “other elements within memory” suggests a

multiplexer to one skilled in the art. Pet. 42; Ex. 1002 ¶¶ 102–103. We emphasize the phrase “other elements” (Pet. 42; Ex. 1002 ¶ 103) does not sufficiently map the recited “multiplexer” to Petropoulos’s components. To the extent Petitioner contends that any circuit that receives address signals and outputs other signals is a multiplexer, we disagree for reasons previously presented.

Mr. Credelle maps limitation [b] to yet further passages in Petropoulos. Ex. 1002 ¶ 110 (citing Ex. 1009 ¶¶ 12–13). Other than quoting from these paragraphs, which do not discuss or suggest a multiplexer, Mr. Credelle provides no further explanation of how these paragraphs teach or suggest “a multiplexer” as claim 1 recites. Ex. 1002 ¶ 110.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Petropoulos renders obvious limitation [b]. Claims 2 and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 45.

b. Limitation [g]

Petitioner asserts Petropoulos teaches “a desired one of the memory arrays 210 is selected for a particular modification.” Pet. 44 (quoting Ex. 1009 ¶ 51 and citing Ex. 1002 ¶ 108). In particular, Petitioner states routing circuit 220 selects a desired modification and that one skilled in the art would have understood the decoder, which accesses the desired voltage from a memory array, maps to the recited “means to switch between banks based on external signals, i.e., the routing circuit.” Pet. 44–45 (citing Exs. 1009 ¶¶ 27, 53 and 1002 ¶ 109).

Cited paragraph 27 summarizes what is shown in Figure 2 below.

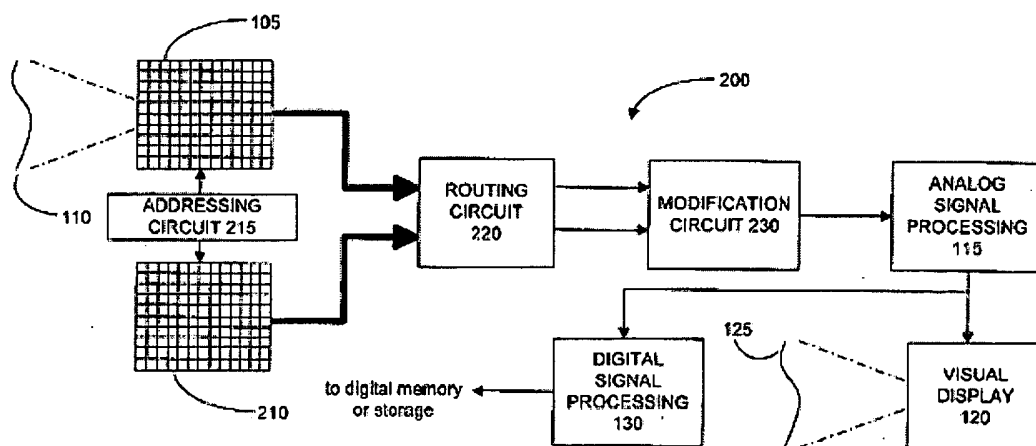
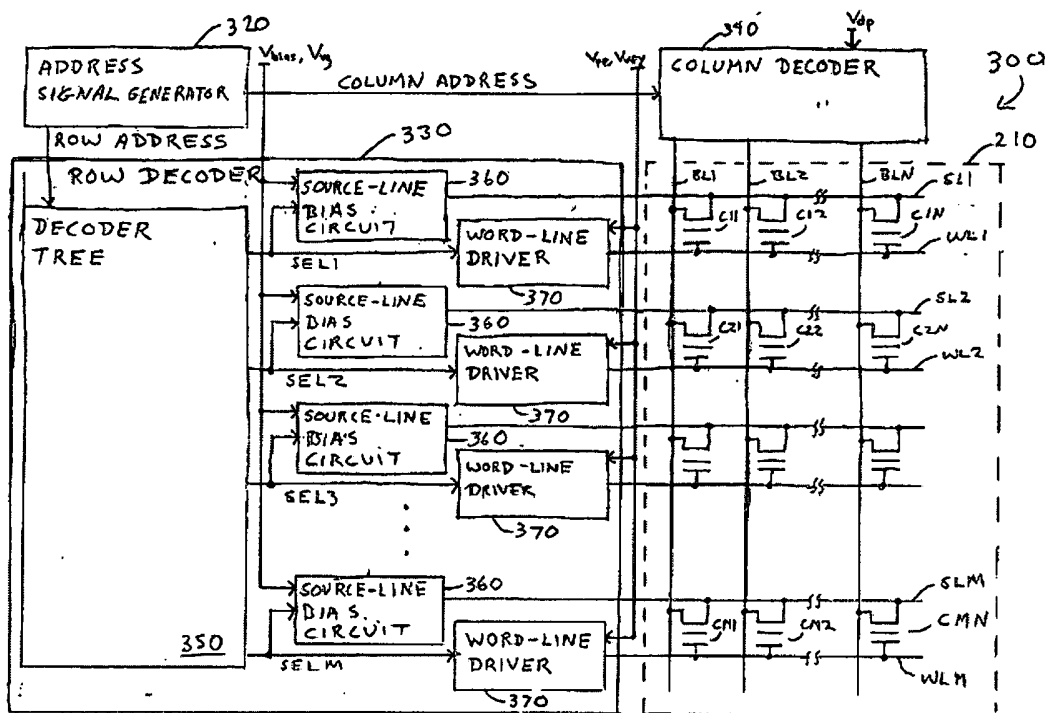


FIG. 2

Petropoulos's Figure 2 Showing an Imaging System

Figure 2's imaging system includes (1) image sensor 105, (2) addressing circuit 215 reading out voltages from image sensor 105 and memory 210, (3) routing circuit 220, and (4) analog signal processing circuit 115 for processing reconstructed image 125. Ex. 1009 ¶¶ 27–28, Fig 2. There is no accompanying discussion of a corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) to limitation [g] in Figure 2.

Figure 3 below shows more detail of the multi-memory 210 in above Figure 2.



Petropoulos's Figure 3 Showing Memory

The above Figure 3's memory shows address signal generator 320 coupled to column decoder 340 and row decoder 330, the decoders coupled to multi-level memory 210. Ex. 1009 ¶ 19, Fig. 3.

Although this figure shows decoders 330 and 340, Petitioner does not explain sufficiently or identify adequately how Petropoulos's decoder is a corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) to limitation [g]. See Prelim. Resp. 40. For example, Petropoulos's Figure 3 has two decoders (e.g., row decoder 330 and column decoder 340). Ex. 1009, Fig. 3. But, Petitioner does not explain whether both of these decoders, or which portions of these decoders, are being mapped to limitation [g]. Pet. 44–45.

Petropoulos discusses a desired memory is selected for a particular modification (Ex. 1009 ¶ 51, *cited in* Pet. 44) and the memory array and

decoder are collectively used for the modifications (Ex. 1009 ¶ 53, *noted in* Pet. 44). Regardless, Petitioner fails to explain how this teaches or suggests the structure corresponding to limitation [g] (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal).

Petropoulos discusses that a multi-level memory array can be used with a decoder for multiple modification types. Ex. 1009 ¶ 53, *noted in* Pet. 44. Petropoulos states, “The memory array is programmed with data corresponding to the desired types of modifications in various portions of the array” and “[t]he decoder then determines the type of modification . . . and accesses the desired voltage from the memory array” (Ex. 1009 ¶ 53). Petitioner fails to explain sufficiently how “the decoder” determining the modification type and accessing the memory array’s desired voltage teaches or suggests to the corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) of limitation [g].

Petitioner further cites paragraph 108 of Mr. Credelle’s testimony as support for Petropoulos teaching limitation [g]. Pet. 44. Mr. Credelle, however, does not persuasively explain how the portions of Petropoulos he cites teach or suggest a corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) to a means for switching between banks as claim 1 requires.

Petitioner further states that the decoder “selects a location in the memory array” (Pet. 44), turning to Mr. Credelle’s testimony for support (Pet 45 (citing Ex. 1002 ¶ 109)). In paragraph 109, Mr. Credelle discusses memory arrays 210, routing circuit 220, and modification circuitry block 230 (shown in Figure 2) are used to select and perform memory array modification and teach “a means to select gamma data from the memory

arrays and a routing circuit 220 to select the modifications.” Ex. 1002 ¶ 109 (citing Ex. 1009 ¶¶ 27, 51). Thus, Mr. Credelle concludes that the “means to select gamma data” and the routing circuit 220—not the previously discussed decoder—are a “means to switch between banks.” Ex. 1009 ¶ 109.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Petropoulos renders obvious claim 1’s limitation [g]. Claims 2 and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 45.

c. Conclusion

Having reviewed Petitioner’s and Patent Owner’s assertions, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Petropoulos renders challenged claims 1, 2, and 5 of the ’305 patent obvious.

4. Tanaka (Ex. 1010)

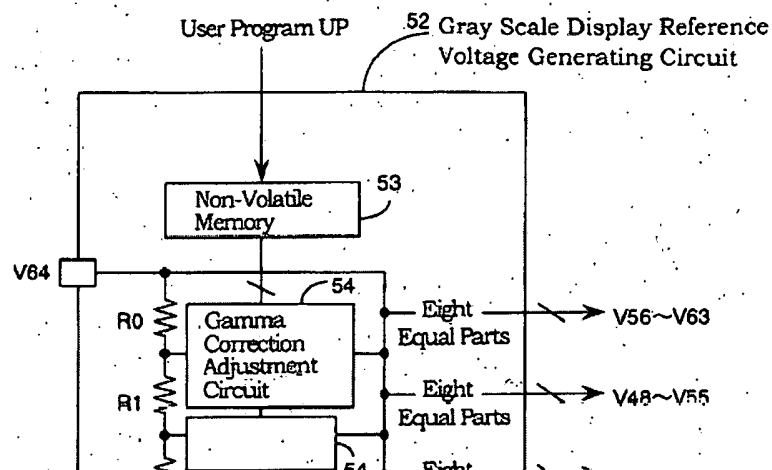
Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over Tanaka under 35 U.S.C. § 103(a). Pet. 17, 45–53. To support its contentions, Petitioner cites to Mr. Credelle’s testimony (Ex. 1002). Patent Owner presents several arguments, including Tanaka does not teach or suggest claim 1’s preamble and limitations [b], [d], [f], and [g]. Prelim. Resp. 41–47. Patent Owner cites to Mr. Murphy’s testimony (Ex. 2010).

Having reviewed Petitioner’s and Patent Owner’s assertions related to Tanaka, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Tanaka renders challenged claim 1 obvious for the following reasons. We focus on claim 1’s limitations [b], [f], and [g].

Tanaka discusses “a gray scale display reference voltage generating circuit” for use with a LCD device that includes “a reference voltage generating section for producing reference voltages of a plurality of levels” and “an adjustment section for adjusting the reference voltages based upon the quantity of adjustment stored in the correction information storing section.” Ex. 1010, Abstract, ¶¶ 32–33.

a. Limitation [b]

Petitioner admits Tanaka “does not explicitly disclose the use of a multiplexer” but contends Tanaka’s user interface must provide data and gamma locations to select memory locations. Pet. 50 (citing Exs. 1010 ¶¶ 102, 143 and 1002 ¶ 123). In particular, Tanaka teaches voltage generating circuit 52 produces reference voltages and uses a basis voltage VR supplied from an external power source and a user program (UP) given by a user program such as an external control device. Ex. 1010 ¶ 102, Fig. 3; Ex. 1002 ¶ 123. A portion of Figure 3 is reproduced below to illustrate.



Partial Figure 3 Showing Memory receiving UP data.

Notably, other than a data line between the UP and memory 53 or between gamma correction adjustment circuit 54 and memory 53 in Tanaka's partial Figure 3, there is no other interface and, more specifically, no multiplexer.

Tanaka discusses storing addresses in memory 53 (Ex. 1010 ¶ 140) and how addresses are stored using "the external control device by the user" (Ex. 1010 ¶ 143). *See* Ex. 1002 ¶ 123 (quoting from Ex. 1010 ¶ 143). More specifically, Tanaka discusses that a user's operation changes the gamma correction adjustment. Ex. 1010 ¶ 143. Tanaka does not discuss or suggest using any particular interface or the recited "multiplexer" to address or program its memory (e.g., 53). Additionally, Petitioner does not explain sufficiently how these teachings map to both the "circuits for programming" and the "multiplexer" coupled to the "circuits for programming" as claim 1 requires. *See* Prelim. Resp. 43.

Petitioner also asserts that "as discussed above," an ordinary artisan would have known "one of a limited number of components would have performed this function," and thus employing a multiplexer would have been obvious. Pet. 50 (citing Ex. 1002 ¶ 123). This theory that any of a limited number of components perform Tanaka's interface function that provides data and gamma locations to memory is similar to an "obvious to try" rationale.

But, Petitioner fails to support this rationale adequately. More specifically, neither Petitioner (Pet. 49–50) nor its expert, Mr. Credelle, (Ex. 1002 ¶ 123) has identified a finite number of predictable solutions for providing Tanaka's interface or shown that an ordinary artisan would have good reasons to pursue using a multiplexer as a predictable solution for Tanaka's interface. *See KSR*, 550 U.S. at 421. In fact, Mr. Credelle testifies flash memory is programmed using decoders and gamma data. Ex. 1002

¶ 123 (referring to Section V.C. of his declaration). Mr. Credelle appears to assert Tanaka teaches its memory already has a multiplexer—not that an ordinary skilled artisan would have good reason to pursue modifying Tanaka’s memory with a multiplexer. *See* Ex. 1002 ¶ 123. Also, even assuming, without agreeing, that “*Tanaka* must necessarily provide address data and gamma locations to selected locations within the memory” (Pet. 50), this is insufficient to demonstrate one skilled in the art would have recognized trying a multiplexer for this purpose.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Tanaka renders obvious limitation [b]. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 52–53.

b. Limitations [f] and [g]

With respect to limitation [f], Petitioner contends Tanaka’s elements 51-1, 51-2, and 52-3 are the cells’ banks. Pet. 51 (citing Exs. 1010, Fig. 10 and 1002 ¶ 127). Notably, this mapping of the storage cells’ banks to element 51 is inconsistent with Petitioner’s earlier mapping of the storage cells to element 53. *Compare* Pet. 49, *with* Pet. 51. Additionally, Petitioner’s mapping to element 51 is inconsistent with Mr. Credelle’s testimony. *Compare* Pet. 51, *with* Ex. 1002 ¶ 127.

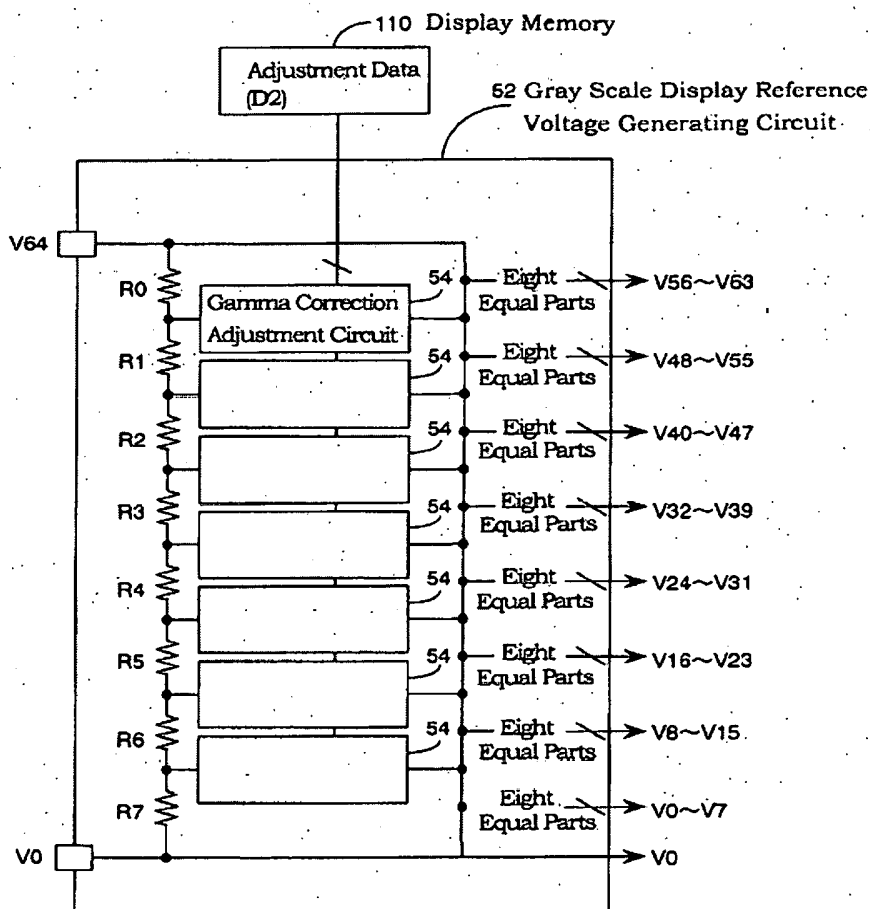
Regarding limitation [g], Petitioner asserts Tanaka teaches selecting banks based on the data’s color. Pet. 51 (citing Ex. 1002 ¶ 128). Petitioner also states Tanaka teaches multiple gamma correction curves stored in display memory and a means to switch between gamma curves depending on a row number. Pet. 51–52 (citing Exs. 1010, Fig. 20 and 1002 ¶ 128). Although indicating Tanaka uses external memory, Petitioner determines “it would have been obvious to a POSA to enlarge the memory 53 to contain

multiple sets of gamma curves.” Pet. 52 (citing Exs. 1010 ¶¶ 243–45, Fig. 33 and 1002 ¶ 130). Lastly, Petitioner states a POSA “would have understood the[three] control signals are external signals to control which bank of gamma correction data is selected from memory.” Pet. 52 (citing Exs. 1010 ¶¶ 243–245 and 1002 ¶¶ 130–131).

Patent Owner rebuts, challenging the multiple bases for concluding Tanaka teaches or suggests limitations [f] and [g]. Prelim. Resp. 45–47.

We disagree with Petitioner (Pet. 51 (citing Exs. 1010, Fig. 10 and 1002 ¶ 127)) and agree with Patent Owner (Prelim. Resp. 45–46) that Tanaka’s reference voltage generating circuits (e.g., 51-1, 51-2, and 52-3) are not banks of cells as understood by an ordinary artisan (e.g., contiguous sections of addressable, computer memory). *See* Ex. 2010 ¶ 47. Rather, they are shown as separate components from memory 53 in Tanaka’s Figure 10. Ex. 1010, Fig. 10.

Also, Tanaka’s Figure 20 below shows an alternative embodiment of gray scale display reference voltage generating circuit 52 from that in Figure 3:



Tanaka's Figure 20 Showing an Alternative Gray Scale Display Reference Voltage Generating Circuit

The above Figure 20's gray scale display reference voltage generating circuit 52 includes seven gamma correction adjustment circuits 54 generating eight equal part voltages (i.e., 64 reference voltages V0-V63) using voltage input terminals V0 and V64 and eight resistors R0 through R7. Ex. 1010 ¶¶ 109, 187, Fig. 20.

Contrary to Petitioner's assertion (Pet. 51–52), this figure does not show or suggest memory banks or a means to switch between gamma curves depending on a row number as part of "[a]n integrated circuit." See Prelim. Resp. 46. Moreover, memory 53, shown in Figure 3 and Figure 10, *noted in*

Ex. 1002 ¶ 127, is not found in Figure 20. In fact, as noted by both Petitioner (Pet. 52) and Patent Owner (Prelim. Resp. 46), display memory 110 in Figure 20 is external to circuit 52. Ex. 1010, Fig. 20. An external memory does not teach or suggest “an integrated circuit” comprising “non-volatile storage cells” along with recited limitations [b]–[g]. *See* Ex. 2010 ¶ 46.

Discussing Figure 20, Mr. Credelle quotes from Tanaka’s paragraph 186, which states adjustment data is stored in memory 110 and adjustment data type read out is varied for every gate signal line by control C. Ex. 1002 ¶ 128 (quoting Ex. 1010 ¶ 186). This teaching does not identify sufficiently a corresponding structure (i.e., a circuit, algorithm, and/or damping circuit that uses at least one bank address signal) to limitation [g]. *See* Prelim. Resp. 46.

Accordingly, Petitioner has not demonstrated adequately that Tanaka’s Figure 20 shows an integrated circuit comprising both “non-volatile storage cells” (limitation [a]) and a “means to switch between the banks [of the storage cells] based on one or more external signals” (limitation [g]) as claim 1 recites.

Petitioner further asserts an ordinary artisan would have known to enlarge memory 53 to contain Tanaka’s gamma curves. Pet. 52 (citing Exs. 1010 ¶¶ 243–245, Fig. 33 and 1002 ¶ 130); Ex. 1002 ¶ 129 (showing gamma curves in Figure 25). Cited paragraphs 243 through 245, which address Figure 32, fail to discuss enlarging memory (e.g., 53) to contain gamma curves. Exs. 1010 ¶¶ 243–245. Thus, although these passages discuss reading out data from display memory using control signals (e.g., C and C1) and cited Figure 33 shows a similar arrangement, there is insufficient evidence that Tanaka suggests to one skilled in the art enlarging

memory 53, which is mapped to the recited “non-volatile cells” in claim 1. Pet. 49 (citing Ex. 1010 ¶¶ 76, 144); *see* Ex. 2010 ¶ 49 (discussing Tanaka does not demonstrate that it would be obvious to enlarge memory to contain gamma curves).

Also, Petitioner has not sufficiently explained or identified the “rows” discussed in paragraphs 203 and 204, *noted in* Ex. 1002 ¶ 129, are storage cells’ banks, such that there is a suggestion to include a “means to switch between banks,” as claim 1 further recites. Because Petitioner does not provide sufficient evidence to have banks within memory 53 and to enlarge Tanaka’s memory 53, Petitioner has not demonstrated sufficiently to include claim 1’s limitation [g].

Mr. Credelle discusses Figure 33 and discusses three external control signals used “to control which bank of gamma correction data is selected from non-volatile display memory 110 and 137.” Ex 1002 ¶ 130. Figure 33 does not show banks in memory 110 and 137, such that Tanaka’s Figure 33 teaches or suggests to an ordinary artisan a “means to switch between banks based on one or more external signals,” as recited. Ex. 1010, Fig. 33; *see also* Ex. 1010 ¶ 241. That is, a corresponding structure to limitation [g] (i.e., a circuit, algorithm, and/or damping circuit that uses at least one bank address signal) is not shown or described. Mr. Credelle’s discussion in paragraph 132, previously addressed above, does not cure this deficiency. Ex. 1002 ¶ 132 (citing Ex. 1010 ¶¶ 243–245).

For the above reasons, Petitioner does not show sufficiently for institution purposes that Tanaka renders obvious limitations [f] and [g]. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 52–53.

d. Conclusion

Having reviewed Petitioner's and Patent Owner's assertions, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Tanaka renders challenged claims 1, 2, 4, and 5 of the '305 patent obvious.

5. Da Costa and Tsai (Ex. 1011)

Petitioner also challenges claims 1, 2, 4, and 5 as being unpatentable over Da Costa and Tsai under 35 U.S.C. § 103(a). Pet. 17, 53–58. Petitioner explains this ground is “presented to address a potential argument that *Da Costa* and/or *Tanaka* do not render obvious the claims' recitation of a ‘multiplexer.’ *Tsai*, which is combinable with *Da Costa* and with *Tanaka* for the reasons discussed below, explicitly discloses the use of a multiplexer, and the combination plainly meets this limitation.” Pet. 18, 57–58. For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Da Costa and Tsai render the challenged claims obvious.

Tsai discusses a microcomputer having embedded flash memory, which allows for (1) programming data into the memory and (2) reprogramming (e.g., update or change) data in memory without external programming tools or on-chip. Ex. 1011, Abstract, *cited in* Pet. 54. Tsai's microcomputer (e.g., 310) includes a bus multiplexer (e.g., 350) connecting a register set (e.g., 340) to flash memory (e.g., 330). Ex. 1011, 7:2–9, 49–67, Fig. 3; Pet. 54–55.

Petitioner proposes to combine Tsai with Da Costa. Pet. 55–57. In particular, Petitioner states, “A POSA reading *Tsai* would have understood that the memory programming method described therein could be used to program the integrated flash memory as disclosed by *Da Costa*” (Pet. 56–

57) (citing Ex. 1002 ¶ 149) and “would have understood that the programming process it describes would provide the memory programming details that Da Costa lacked” (Pet. 57) (citing Ex. 1002 ¶ 149).

As explained above, Petitioner does not show sufficiently for institution purposes that the proposed ground based only on Da Costa under 35 U.S.C. § 103 teaches or suggests limitations [f] and [g]. The proposed ground to combine Da Costa and Tsai does not address how Tsai would have further taught or suggested limitations [f] and [g]. Thus, the proposed ground does not rely on Tsai to teach or suggest claim 1’s limitations [f] and [g], which as previously stated are not sufficiently taught or suggested by Da Costa. We refer above for more details.

Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 36–37.

Having reviewed Petitioner’s and Patent Owner’s assertions related to Da Costa and Tsai, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Da Costa and Tsai render challenged claims 1, 2, 4, and 5 of the ’305 patent obvious.

6. Tanaka and Tsai

Petitioner also challenges claims 1, 2, 4, and 5 as being unpatentable over Tanaka and Tsai under 35 U.S.C. § 103(a). Pet. 17, 58–62. Like the proposed ground based on Da Costa and Tsai, Petitioner explains this ground is “presented to address a potential argument that” Tanaka alone does not render obvious claim 1’s “multiplexer,” asserting the combination of Tanaka and Tsai meets this limitation. Pet. 18; Pet. 60–61.

As explained above, Petitioner does not show sufficiently for institution purposes that the proposed ground based only on Tanaka under

35 U.S.C. § 103 teaches or suggests limitations [f] and [g]. The proposed ground to combine Tanaka and Tsai does not address how Tsai would have further taught or suggested limitations [f] and [g]. In fact, Petitioner states this ground is presented to address “a potential argument” (Pet. 18) that Tanaka does not render a multiplexer obvious (Pet. 18, 58). Thus, this proposed ground does not rely on Tsai to teach or suggest claim 1’s limitations [f] and [g], which as previously stated are not sufficiently taught or suggested by Tanaka. We refer above for more details.

Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. See Pet. 52–53.

Having reviewed Petitioner’s and Patent Owner’s assertions related to Tanaka and Tsai, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Tanaka and Tsai render challenged claims 1, 2, 4, and 5 of the ’305 patent obvious.

7. Petropoulos and Kang

Lastly, Petitioner also challenges claims 1, 2, 4, and 5 as being unpatentable over Petropoulos and Kang under 35 U.S.C. § 103(a). Pet. 17, 62–66. Petitioner explains, “To the extent the Board finds Ground 3 [(grounds based on Petropoulos alone)] to be lacking regarding the claimed gamma reference voltage signals in *Petropoulos*, Petitioner submits that *Kang* in combination with *Petropoulos* renders obvious the claimed gamma reference voltage signals.” Pet. 62; Pet. 18. Petitioner states, “[T]hose descriptions [of a relatively more limited discussion of gamma reference voltage signals in *Petropoulos*] would be a motivation to combine *Petropoulos* with *Kang*, which plainly discloses the gamma correction voltage-related limitations of the Challenged Claims.” Pet. 18, 62.

As explained above, Petitioner has not shown sufficiently for institution purposes that the proposed grounds based on Kang or Petropoulos alone teach certain limitations of the challenged claims. We explained above the proposed ground based only on Petropoulos does not teach or suggest limitations [b] and [g] and the proposed ground based only on Kang does not teach or suggest limitations [b], [f], and [g]. Thus, this proposed ground to combine Petropoulos and Kang does not address how the combination teaches or suggests limitations [b] and [g]. In fact, Petitioner states this ground is presented if “Petropoulos’ relatively more limited discussion of gamma reference voltage signals is deficient” (Pet. 18, 66). That is, the proposed ground does not turn to Kang to teach or suggest limitations [b] and [g], which as previously stated are not sufficiently taught or suggested by Petropoulos. We refer above for more details.

Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 28–30, 45¹⁹.

Having reviewed Petitioner’s and Patent Owner’s assertions related to Petropoulos and Kang, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Petropoulos and Kang render challenged claims 1, 2, 4, and 5 of the ’305 patent obvious.

Because this determination disposes of the Petition, no need exists to reach Patent Owner’s other arguments regarding Petitioner’s showing.

¹⁹ The proposed ground based on Petropoulos alone does not include claim 4. Pet. 17, 45.

E. Conclusions Based on Cited References

Petitioner has not established a reasonable likelihood of prevailing in challenging the following: (1) claims 1, 2, 4, and 5 as obvious over Kang; (2) claims 1, 2, 4, and 5 as obvious over Da Costa; (3) claims 1, 2, and 5 as obvious over Petropoulos; (4) claims 1, 2, 4, and 5 as obvious over Tanaka; (5) claims 1, 2, 4, and 5 as obvious over Da Costa and Tsai; (6) claims 1, 2, 4, and 5 as obvious over Tanaka and Tsai, and (7) claims 1, 2, 4, and 5 as obvious over Petropoulos and Kang.

III. CONCLUSION

For the above reasons, we determine that Petitioner has failed to demonstrate a reasonable likelihood of prevailing at trial as to any challenged claim. Accordingly, we deny institution of an *inter partes* review.

IV. ORDER

For the above reasons, it is

ORDERED that the Petition is *denied* as to the challenged claims of the '305 patent, and no *inter partes* review is instituted.

IPR2018-01255
Patent 7,233,305 B1

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Patent Number	7,233,305
Issue Date	June 19, 2007
Application Number	10/746,333
Filing Date	December 23, 2003
First Named Inventor	Richard V. Orlando
Attorney Docket Number	ALTA-P007

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EFS ID:	34056348
Application Number:	10746333
International Application Number:	
Confirmation Number:	3420
Title of Invention:	GAMMA REFERENCE VOLTAGE GENERATOR
First Named Inventor/Applicant Name:	Richard V. Orlando
Customer Number:	22877
Filer:	Dennis Fernandez/Constance Jacobs
Filer Authorized By:	Dennis Fernandez
Attorney Docket Number:	ALTA-P007
Receipt Date:	19-OCT-2018
Filing Date:	23-DEC-2003
Time Stamp:	09:00:45
Application Type:	Utility under 35 USC 111(a)

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1	Change of Address	2018_10_19_ALTA_P007_Change_of_Address.pdf	186734	no	2
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PLAINTIFF PHENIX LONGHORN, LLC		DEFENDANT TEXAS INSTRUMENTS, INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,233,305	6/19/2007	Phenix Longhorn, LLC
2		
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5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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DOCKET NO. 2:17-cv-00711	DATE FILED 10/25/2017	U.S. DISTRICT COURT Eastern District of Texas, Marshall Division
PLAINTIFF PHENIX LONGHORN, LLC		DEFENDANT WISTRON CORPORATION
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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PLAINTIFF PHENIX LONGHORN, LLC		DEFENDANT WISTRON CORPORATION
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,233,305	6/19/2007	Phenix Longhorn, LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Tyler Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. <u>6:17-cv-00010</u>	DATE FILED <u>1-5-2017</u>	U.S. DISTRICT COURT Eastern District of Texas, Tyler Division
PLAINTIFF PHENIX LONGHORN, LLC		DEFENDANT VIZIO, INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,233,305	6/19/2007	Phenix Longhorn, LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Tyler Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Eastern District of Texas, Tyler Division
PLAINTIFF PHENIX LONGHORN, LLC		DEFENDANT VIZIO, INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,233,305	6/19/2007	Phenix Longhorn, LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/746,333	12/23/2003	Richard V. Orlando	ALTA-P007	3420

22877 7590 03/14/2016
FERNANDEZ & ASSOCIATES, LLP
1175 Osborn Avenue
Atherton, CA 94027

EXAMINER

SHENG, TOM V

ART UNIT	PAPER NUMBER
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2628

NOTIFICATION DATE	DELIVERY MODE
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03/14/2016

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

legalassistant@iploft.com
jmharris@iploft.com



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Patent No. 7233305
Issued Date: 19 June, 2007
Appl. No: 10/746,333
Filed.: 23 December 2003

PART (A) RESPONSE FOR CERTIFICATES OF CORRECTION

This is a decision on the Certificate of Correction request filed 02 December 2015.

The request for issuance of Certificate of Correction for the above-identified correction(s) under the provisions of 37 CFR 1.322 and/or 1.323 is hereby:

(Check one)

☒ Approved ☐ Approved in Part ☐ Denied

Comments:

PART (B) PETITION UNDER 37 CFR 1.324 OR 37 CFR 1.48

This is a decision on the petition filed to correct inventorship under 37 CFR 1.324.

This is a decision on the request under 37 CFR 1.48, petition filed . In view of the fact that the patent has already issued, the request under 37 CFR 1.48 has been treated as a petition to correct inventorship under 37 CFR 1.324.

The petition is hereby: ☐ Granted ☐ Dismissed

The patented filed is being forwarded to Certificate of Corrections Branch for issuance of a certificate naming only the actual inventor or inventors.

/NITIN (Kumar) PATEL/
Supervisory Patent Examiner, Art Unit 2628
Technology Center 2600
Phone: 571-272-2600

Certificates of Correction Branch email: CustomerServiceCoC@uspto.gov CoC Central Phone Number: (703) 756-1814

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,233,305 B1
APPLICATION NO. : 10/746333
DATED : June 19, 2007
INVENTOR(S) : Richard V. Orlando et al.

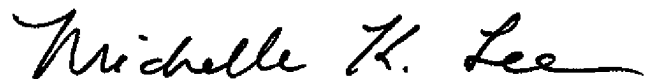
Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

Column 8, line 5 (claim 5): please change “the” to “a”. Line 5 should read “for programming require an external source for a high voltage programming means”.

Signed and Sealed this
First Day of March, 2016

A handwritten signature in black ink, reading "Michelle K. Lee". The signature is fluid and cursive, with the first letters of each name being capitalized and prominent.

Michelle K. Lee
Director of the United States Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Richard V. Orlando et al.	Attorney Docket No.:	ALTA-P007
Serial No.:	10/746,333	Patent No.:	7,233,305
Filed:	12/23/2003	Issued:	06/19/2007
Title	Gamma Reference Voltage Generator		

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
Certificates of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The above-referenced patent issued on June 19, 2007 and contains a typographical error. Applicant respectfully request that the patent be corrected as follows:

- Column 8, line 5 (claim 5): please change “the” to “a”. Line 5 should read “for programming require an external source for a high voltage programming means”

This Request is to correct an error incurred through a typographical error. Applicant submits the \$100.00 certificate of correction filing fee.

Respectfully submitted,

Dated: December 2, 2015

/Dennis S. Fernandez/
Dennis S. Fernandez, Esq.
Reg. No. 34,160

Address: **FERNANDEZ & ASSOCIATES, LLP**
Patent Attorneys
Customer No: **22877**

Phone: (650) 325-4999
Fax: (650) 325-1203
Email: iploft@iploft.com

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 7,233,305

APPLICATION NO.: 10/746,333

ISSUE DATE : 06/19/2007

INVENTOR(S) : Richard V. Orlando, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

- Column 8, line 5 (claim 5): please change "the" to "a". Line 5 should read "for programming require an external source for a high voltage programming means"

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Fernandez & Associates, LLP
1175 Osborn Avenue
Atherton, CA 94027

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		10746333		
Filing Date:		23-Dec-2003		
Title of Invention:		GAMMA REFERENCE VOLTAGE GENERATOR		
First Named Inventor/Applicant Name:		Richard V. Orlando		
Filer:		Dennis Fernandez/Kathryn Pritchard		
Attorney Docket Number:		ALTA-P007		
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of Correction	1811	1	100	100

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				100

Electronic Acknowledgement Receipt

EFS ID:	24247316
Application Number:	10746333
International Application Number:	
Confirmation Number:	3420
Title of Invention:	GAMMA REFERENCE VOLTAGE GENERATOR
First Named Inventor/Applicant Name:	Richard V. Orlando
Customer Number:	22877
Filer:	Dennis Fernandez/Kathryn Pritchard
Filer Authorized By:	Dennis Fernandez
Attorney Docket Number:	ALTA-P007
Receipt Date:	02-DEC-2015
Filing Date:	23-DEC-2003
Time Stamp:	20:44:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 100
RAM confirmation Number	20828
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	2015_12_02_ALTA-P007_Request_Certificate_Correction.pdf	18196	no	1
			c622932805b7a5fa32693dcccdf134c85163dae3		
Warnings:					
Information:					
2	Request for Certificate of Correction	2015_12_02_ALTA-P007_Certificate_Correction.pdf	164667	no	2
			645d73254a53037cdced3da9436f4090f92a1db5		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	29904	no	2
			d88acb3a89ce1d3234aed5c981d4b1b59e530b5f		
Warnings:					
Information:					
Total Files Size (in bytes):			212767		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

AO 120 (Rev. 08/10)

TO: **Mail Stop 8
Director of the U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450**

**REPORT ON THE
FILING OR DETERMINATION OF AN
ACTION REGARDING A PATENT OR
TRADEMARK**

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Tyler Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 6:15-cv-00436	DATE FILED 4/17/2015	U.S. DISTRICT COURT Eastern District of Texas, Tyler Division
PLAINTIFF PHENIX, LLC		DEFENDANT INTEGRATED MEMORY LOGIC, LTD. and EXAR CORPORATION
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,233,305 B1	6/19/2007	Phenix, LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY	
	☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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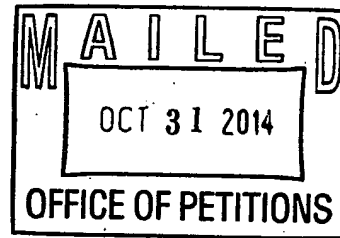
Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy
Innolux Corporation Exhibit 1002, Page 147



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

FERNANDEZ & ASSOCIATES, LLP
1175 Osborn Avenue
Atherton CA 94027



In re Patent No. 7,233,305
Issue Date: June 19, 2007
Application No. 10/746,333
Filed: December 23, 2003

ON PETITION

This is a decision on the renewed petition under 37 CFR 1.378(b), filed October 15, 2014, to accept the delayed payment of a maintenance fee for the above-identified patent.

The petition for delayed payment of the maintenance fee is **GRANTED**.

This patent expired on June 19, 2011 for failure to pay the 3½ year maintenance fee. The 3½ year maintenance fee is hereby accepted and the above-identified patent is reinstated as of the mail date of this decision.

Any questions concerning this matter may be directed to the undersigned at (571) 272-6692.

Christopher Bottorff
Petitions Examiner
Office of Petitions

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Richard V. Orlando et al. Attorney Docket No.: ALTA-P007
Serial No.: 10/746,333 Patent No.: 7,233,305
Filed: 12/23/2003 Issued: June 19, 2007
Title: GAMMA REFERENCE VOLTAGE GENERATOR

**PETITION TO ACCEPT UNINTENTIONALLY DELAYED PAYMENT OF
MAINTENANCE FEE IN AN EXPIRED PATENT (37 CFR 1.378(b))**

Mail Stop: Petitions
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby re-submits this Petition to Accept Unintentionally Delayed Payment of Maintenance Fee in an Expired Patent pursuant to the provisions of 37 CFR 1.378(b).

The required maintenance fee for small entity \$800.00 and petition fee of \$850.00 has been previously paid.

The delay in payment of the maintenance fee was unintentional, and Applicant provides the following:

On or about May 30, 2014, Applicant became aware that the above-referenced patent had expired for non-payment of maintenance fees. Applicant immediately contacted counsel Fernandez & Associates, LLP to inquire if any notifications from the U.S. Patent and

Trademark Office had been received and to begin the petition process to reinstate the expired patent.

On May 8, 2007, counsel Fernandez & Associates, LLP submitted a Change of Correspondence Address to the United States Patent & Trademark Office. The Change of Correspondence Address provided Alta Analog, Inc., 1737 N. First Street, #620, San Jose, CA 95112 as the new correspondence address. A copy of the Change of Correspondence Address is attached hereto and incorporated herein by reference as Exhibit "1".

On or about June 19, 2007, Alta Analog received the Issue Notification from the U.S. Patent & Trademark Office at the new correspondence address of 1737 N. First Street, #620, San Jose, CA 95112. A copy of the Issue Notification is attached hereto and incorporated herein by reference as Exhibit "2".

On or about May 22, 2009, Fernandez & Associates, LLP received Correspondence Address / Fee Address Change from the United States Patent & Trademark Office. A copy of the Notice is attached hereto and incorporated herein by reference as Exhibit "3". This Notice appears to indicate a change of address for customer number 22877 and was filed in U.S. Patent No. 7,233,305. The address appearing on the Notice for Fernandez & Associates, LLP was 1047 El Camino Real, Suite 201, Menlo Park, CA 94025. It was the intention of Fernandez & Associates to change the correspondence address for its customer number and not U.S. Patent No. 7,233,305.

The undersigned tracks payment due dates, including Patent Office maintenance fees, using Microsoft Outlook. During the approximate time line of September, 2010, the Outlook Calendar and computer failed and approximately four months of calendar inputs, data and emails were lost.

Neither Alta Analog nor Fernandez & Associates, LLP received the courtesy maintenance fee reminder or patent expiration notice from the United States Patent & Trademark Office. A telephone call to the Maintenance Fee Branch was placed on May 30, 2014 inquiring as to the address to which the expiration notice was mailed and resulted in another correspondence address of 1175 Osborn Avenue, Atherton, CA 94027. Fernandez & Associates, LLP was advised by “Glenda” that she was unable to confirm the address where the expiration notice was sent and that the physical file could be pulled from storage to determine the mailing address on the expiration notice and/or if the expiration notice was returned to the United States Patent & Trademark Office.

If any additional information is required, the undersigned can be reached at (650) 325-4999.

Applicant respectfully requests that the Petition to Accept Unintentionally Delayed Payment of Maintenance Fee in the above-referenced expired patent be granted.

Respectfully submitted,

Dated: October 15, 2014

/Dennis S. Fernandez/
Dennis S. Fernandez, Esq.
Reg. No. 34,160

Address: **FERNANDEZ & ASSOCIATES, LLP**
Patent Attorneys
Customer No: **22877**
Phone: (650) 325-4999
Fax: (650) 325-1203
Email: iploft@iploft.com



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**CHANGE OF
CORRESPONDENCE ADDRESS
Application**Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/746,333
Filing Date	12/23/2003
First Named Inventor	Richard V. Orlando
Art Unit	2629
Examiner Name	Torn V Sheng
Attorney Docket Number	ALTA-P007

Please change the Correspondence Address for the above-identified patent application to:

☐ The address associated with
Customer Number:

OR

☒ Firm or
Individual Name Alta Analog, Inc. Attn: Richard V. Orlando

Address 1737 North First Street, Suite 620

City San Jose

State CA

Zip 95112

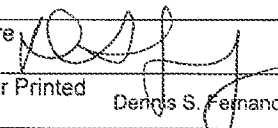
Country U.S.A.

Telephone (408) 441-9600 Ext. 301

Email
rorlando@alta-analog.comThis form cannot be used to change the data associated with a Customer Number. To change the
data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

I am the:

- ☐ Applicant/Inventor
- ☐ Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).
- ☒ Attorney or agent of record. Registration Number 34,160
- ☐ Registered practitioner named in the application transmittal letter in an application without an
executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number _____

Signature 
Typed or Printed
Name Dennis S. Fernandez

Date 05/04/2007

Telephone (650) 325-4999

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple
forms if more than one signature is required, see below.☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/746,333	06/19/2007	7233305	ALTA-P007	3420

7590 05/30/2007
ALTA ANALOG, INC.
ATTN: RICHARD V. ORLANDO
1737 NORTH FIRST STREET,
SUITE 620
SAN JOSE, CA 95112

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 540 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Richard V. Orlando, Los Gatos, CA;
Trevor A. Blyth, Sandy, UT;



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/746,333	7233305	2629	9200



Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 22877 on 05/22/2009

- Correspondence Address
- Power of Attorney Address

The address of record for Customer Number 22877 is:

22877
FERNANDEZ & ASSOCIATES LLP
1047 EL CAMINO REAL
SUITE 201
MENLO PARK, CA 94025

Electronic Acknowledgement Receipt

EFS ID:	20421685
Application Number:	10746333
International Application Number:	
Confirmation Number:	3420
Title of Invention:	GAMMA REFERENCE VOLTAGE GENERATOR
First Named Inventor/Applicant Name:	Richard V. Orlando
Correspondence Address:	ALTA ANALOG, INC. RICHARD V. ORLANDO 1737 NORTH FIRST STREET SUITE 620 SAN JOSE, CA 95112 US 408 441-9600 rorlando@alta-analog.com
Filer:	Dennis Fernandez/Kathryn Pritchard
Filer Authorized By:	Dennis Fernandez
Attorney Docket Number:	ALTA-P007
Receipt Date:	15-OCT-2014
Filing Date:	23-DEC-2003
Time Stamp:	14:17:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition for review by the Office of Petitions.	2014_10_15_ALTA-P007_Maintenance_Fee_Petition.pdf	327268 9e45e3fdcd53df43c4498ec0c7fb7d9fb424751e	no	6
Warnings:					
Information:					
Total Files Size (in bytes):			327268		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Organization _____ Bldg./Room _____

Organization _____
UNITED STATES PATENT AND TRADEMARK OFFICE

P.O. Box 1450

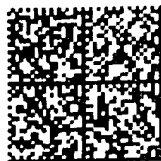
Alexandria, VA. 22313-1450

If Undeliverable Return In Ten Days

Official Business

Penalty For Private Use, \$300

AN EQUAL OPPORTUNITY EMPLOYER



STATES POSTAGE



PITNEY BOWES

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0004244975 AUG27 2014

MAILED FROM ZIP CODE 22314

RECEIVED

SEP 12 2014

USPTO MAIL CENTER

TEXT

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RETURN TO SENDER
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UNABLE TO FORWARD

HC: 22313145050

1892-08429-27-42

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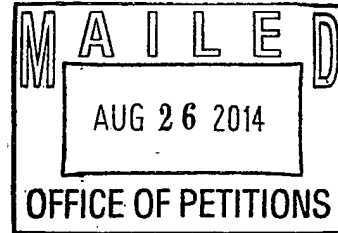


UNITED STATES PATENT AND TRADEMARK OFFICE



Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Alta Analog, Inc.
Attn: Richard V. Orlando
1737 North First Street
Suite 620
San Jose CA 95112



In re Patent No. 7,233,305
Issue Date: June 19, 2007
Application No. 10/746,333
Filed: December 23, 2003

ON PETITION

This is a decision on the petition under 37 CFR 1.378(b), filed June 19, 2014, to accept the delayed payment of a maintenance fee for the above-identified patent.

The petition is **DISMISSED**.

A petition to accept the unintentionally delayed payment of a maintenance fee under 35 U.S.C. 41(c) and 37 CFR 1.378(b) must be accompanied by: (1) a statement that the delay was unintentional; (2) payment of the appropriate maintenance fee, unless previously submitted; (3) payment of the petition fee set forth in 37 CFR 1.17(m). Where there is a question as to whether the delay in payment of the maintenance fee under 35 U.S.C. 41(c) and 37 CFR 1.378(b) was unintentional, the Director may require additional information. This change went into effect on December 18, 2013, the effective date of the Patent Law Treaties Implementation Act, and applies to this petition. This petition lacks item (1) above.

As to item (1), the statement of unintentional delay is not considered to be a properly submitted statement as it is provided by one of the two inventors, Richard V. Orland. Petitioner's attention is directed to 37 CFR 1.33(b), which states.

Amendments and other papers. Amendments and other papers, except for written assertions pursuant to § 1.27(c)(2)(iii) or (c)(2)(iv), filed in the application must be signed by:

- (1) A patent practitioner of record;
- (2) A patent practitioner not of record who acts in a representative capacity under the provisions of § 1.34; or
- (3) The applicant (§ 1.42). Unless otherwise specified, all papers submitted on behalf of a juristic entity must be signed by a patent practitioner.

Moreover, 37 CFR 1.31 states:

An applicant for patent may file and prosecute the applicant's own case, or the applicant may give power of attorney so as to be represented by one or more patent practitioners or joint inventors, except that a juristic entity (e.g., organizational assignee) must be represented by a patent practitioner even if the juristic entity is the applicant. The Office cannot aid in the selection of a patent practitioner.

See Changes To Implement the Inventor's Oath or Declaration Provisions of the Leahy-Smith America Invents Act, 77 Fed. Reg. 48776 (August 14, 2012).

An unsigned amendment (or other paper) or one not properly signed by a person having authority to prosecute the application is not entered. This applies, for instance, where the amendment (or other paper) is signed by less than all of the inventors or is signed on behalf of an assignee but not by a patent practitioner.

Therefore, as the petition containing the statement of unintentional delay is not signed by all of the inventors or a patent practitioner acting on behalf of the assignee pursuant to 37 CFR 3.71 with a statement under 37 CFR 3.73(c), the petition is considered to not contain a proper statement of unintentional delay. If a renewed petition is filed, the renewed petition must contain a statement of unintentional delay signed by all of the inventors or a registered patent practitioner.

Also, the file does not indicate a change of address has been submitted, although the address given on the petition differs from the address of record. If appropriate, a change of address should be filed in accordance with MPEP 601.03. A courtesy copy of this decision is being mailed to the address given on the petition; however, the Office will mail future correspondence to the address of record.

Further correspondence with respect to this matter should be delivered as follows:

By mail: Mail Stop PETITIONS
 Commissioner for Patents
 Post Office Box 1450
 Alexandria, VA 22313-1450

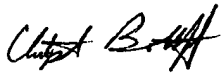
By hand: Customer Service Window
 Mail Stop Petitions
 Randolph Building
 401 Dulany Street
 Alexandria, VA 22314

By fax: (571) 273-8300
 ATTN: Office of Petitions

By internet: EFS-Web¹

¹ www.uspto.gov/ebc/efs_help.html (for help using EFS-Web call the Patent Electronic Business Center at (866) 217-9197)

Any questions concerning this matter may be directed to the undersigned at (571) 272-6692.

A handwritten signature in black ink, appearing to read "Chris Bottorff", written in a cursive style.

Christopher Bottorff
Petitions Examiner
Office of Petitions

cc: Richard V. Orlando
Alta Analog, Inc.
24020 Summit Woods Drive
Los Gatos, CA 95033

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

CHANGE OF CORRESPONDENCE ADDRESS *Patent*

Address to:
Mail Stop Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Patent Number	7,233,305
Issue Date	2007-06-19
Application Number	10/746,333
Filing Date	2003-12-23
First Named Inventor	Richard V. Orlando
Attorney Docket Number	ALTA-P007

Please change the Correspondence Address for the above-identified patent to:

☐ The address associated with Customer Number:

OR

☒ **Firm or Individual Name** Richard Orlando / Alta Analog, Inc.

24020 Summit Woods Drive

Address

City Los Gatos	State CA	ZIP 95033
-----------------------	-----------------	------------------

Country US

Telephone	Email
------------------	--------------

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTO/SB/47).

I am the:

- ☐ Patentee.
- ☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).
- ☒ Attorney or agent of record. Registration Number 34,160.

Signature /Dennis S. Fernandez/

Typed or Printed Name Dennis S. Fernandez

Date September 9, 2014	Telephone (650) 325-4999
-------------------------------	---------------------------------

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of one forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Post Issue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	20097174
Application Number:	10746333
International Application Number:	
Confirmation Number:	3420
Title of Invention:	GAMMA REFERENCE VOLTAGE GENERATOR
First Named Inventor/Applicant Name:	Richard V. Orlando
Correspondence Address:	Alta Analog, Inc. Attn:Richard V. Orlando 1737 North First Street Suite 620 San Jose CA 95112 US 408-441-9600 RORLANDO@ALTA-ANALOG.COM
Filer:	Dennis Fernandez/Kathryn Pritchard
Filer Authorized By:	Dennis Fernandez
Attorney Docket Number:	ALTA-P007
Receipt Date:	10-SEP-2014
Filing Date:	23-DEC-2003
Time Stamp:	13:04:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Change of Address	2014_09_09_ALTA-P007_Address_Change.pdf	124560 5d30a26ae787f9f99127f7a0c168159d81a18a1c	no	1

Warnings:

Information:

Total Files Size (in bytes):	124560
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

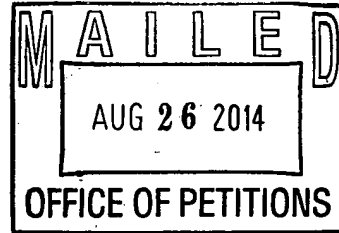
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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Alta Analog, Inc.
Attn: Richard V. Orlando
1737 North First Street
Suite 620
San Jose CA 95112



In re Patent No. 7,233,305
Issue Date: June 19, 2007
Application No. 10/746,333
Filed: December 23, 2003

ON PETITION

This is a decision on the petition under 37 CFR 1.378(b), filed June 19, 2014, to accept the delayed payment of a maintenance fee for the above-identified patent.

The petition is **DISMISSED**.

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As to item (1), the statement of unintentional delay is not considered to be a properly submitted statement as it is provided by one of the two inventors, Richard V. Orland. Petitioner's attention is directed to 37 CFR 1.33(b), which states.

Amendments and other papers. Amendments and other papers, except for written assertions pursuant to § 1.27(c)(2)(iii) or (c)(2)(iv), filed in the application must be signed by:

- (1) A patent practitioner of record;
- (2) A patent practitioner not of record who acts in a representative capacity under the provisions of § 1.34; or
- (3) The applicant (§ 1.42). Unless otherwise specified, all papers submitted on behalf of a juristic entity must be signed by a patent practitioner.

Moreover, 37 CFR 1.31 states:

An applicant for patent may file and prosecute the applicant's own case, or the applicant may give power of attorney so as to be represented by one or more patent practitioners or joint inventors, except that a juristic entity (*e.g.*, organizational assignee) must be represented by a patent practitioner even if the juristic entity is the applicant. The Office cannot aid in the selection of a patent practitioner.

See Changes To Implement the Inventor's Oath or Declaration Provisions of the Leahy-Smith America Invents Act, 77 Fed. Reg. 48776 (August 14, 2012).

An unsigned amendment (or other paper) or one not properly signed by a person having authority to prosecute the application is not entered. This applies, for instance, where the amendment (or other paper) is signed by less than all of the inventors or is signed on behalf of an assignee but not by a patent practitioner.

Therefore, as the petition containing the statement of unintentional delay is not signed by all of the inventors or a patent practitioner acting on behalf of the assignee pursuant to 37 CFR 3.71 with a statement under 37 CFR 3.73(c), the petition is considered to not contain a proper statement of unintentional delay. If a renewed petition is filed, the renewed petition must contain a statement of unintentional delay signed by all of the inventors or a registered patent practitioner.

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Further correspondence with respect to this matter should be delivered as follows:

By mail: Mail Stop PETITIONS
 Commissioner for Patents
 Post Office Box 1450
 Alexandria, VA 22313-1450

By hand: Customer Service Window
 Mail Stop Petitions
 Randolph Building
 401 Dulany Street
 Alexandria, VA 22314

By fax: (571) 273-8300
 ATTN: Office of Petitions

By internet: EFS-Web¹

¹ www.uspto.gov/ebs/efs_help.html (for help using EFS-Web call the Patent Electronic Business Center at (866) 217-9197)

Any questions concerning this matter may be directed to the undersigned at (571) 272-6692.

A handwritten signature in black ink, appearing to read "Christopher Bottorff".

Christopher Bottorff
Petitions Examiner
Office of Petitions

cc: Richard V. Orlando
Alta Analog, Inc.
24020 Summit Woods Drive
Los Gatos, CA 95033



M &

Alta Analog Inc
24020 Summit Woods Dr.
Los Gatos, CA 95033

July 17, 2014

Mail Stop Petitions
Commissioner for Patents,
P.O. Box 1450,
Alexandria, VA 22313-1450

To Whom it May Concern:

Please expedite the petition I have filed for reinstatement of patent 7,233,305, application # 10/746,333. I filed the original petition around June 26th and it was received by the patent office on July 9th.

I have enclosed a check for \$200.00 for the expedite fee.

Sincerely,

Rick Orlando
CEO/President
Alta Analog, Inc.

ENCLOSURE CHECK # 3656

2014 JUL 23 PM 2:50
USPTO
RECEIPTS ACCOUNTING
DIVISION

07/25/2014 DALLEN 00000003 7233305

01 FC:1463

200.00 OP

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT2945585

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST
CONVEYING PARTY DATA	
Name	Execution Date
ALTA ANALOG INC	06/27/2014
RECEIVING PARTY DATA	
Name:	RICHARD ORLANDO
Street Address:	24020 SUMMIT WOODS DR
City:	LOS GATOS
State/Country:	CALIFORNIA
Postal Code:	95033
Name:	AVM CAPITAL LP
Street Address:	14375 SARATOGA AVENUE
Internal Address:	SUITE 104
City:	SARATOGA, CA
State/Country:	CALIFORNIA
Postal Code:	95070
PROPERTY NUMBERS Total: 8	
Property Type	Number
Patent Number:	8194015
Patent Number:	8188952
Patent Number:	7557788
Patent Number:	7554843
Patent Number:	7233305
Patent Number:	7061380
Patent Number:	6985372
Patent Number:	6693828
CORRESPONDENCE DATA	
Fax Number:	(408)353-8707
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
Phone:	408-499-8455
Email:	rorlando@alta-analog.com
Correspondent Name:	RICHARD V ORLANDO

Address Line 1:	24020 SUMMIT WOODS DR
Address Line 4:	LOS GATOS, CALIFORNIA 95033

NAME OF SUBMITTER:	RICHARD V ORLANDO
---------------------------	-------------------

SIGNATURE:	/Richard V. Orlando/
-------------------	----------------------

DATE SIGNED:	07/18/2014
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	This document serves as an Oath/Declaration (37 CFR 1.63).
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Total Attachments: 5

source=Alta Notice of Default#page1.tif

source=Alta Demand for Delivery#page1.tif

source=Alta Demand for Delivery#page2.tif

source=Alta Demand for Delivery#page3.tif

source=Alta Demand for Delivery#page4.tif

June 17, 2014

VIA HAND DELIVERY

Attn: Richard Orlando, President
Alta Analog, Inc.
24020 Summit Woods Drive
Los Gatos, CA 95033

Re: Notice of Default Under Provisions of Security Agreement Between Richard Orlando and AVM Capital LP, as secured parties, and Alta Analog, Inc., as debtor

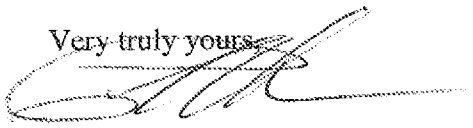
Dear Alta Analog, Inc.:

This is to advise you that you are in default under the terms of the security agreement between Richard Orlando and AVM Capital LP, on the one hand, and Alta Analog, Inc., on the other hand, dated June 30, 2010, and as amended by the Modification One To The Third Amended Security Agreement And The Reimbursement Agreement dated October 31, 2011 ("Security Agreement"). You are in default of the Security Agreement because failure to pay sums when due. As of June 1, 2014, the amount due Richard Orlando was \$409,799.39.

If you have not cured this default by June 27, 2014, we will take all appropriate steps to enforce our security interest, including without limitation giving notice to account debtors pursuant to U.C.C. § 9607(a)(1), repossession of the collateral pursuant to U.C.C. § 9609, public or private sale of the collateral pursuant to U.C.C. § 9610, and strict foreclosure of the collateral under U.C.C. § 9622.

If you have any questions regarding this notice or the nature of your default, please contact the undersigned immediately. We look forward to your prompt response.

Very truly yours,

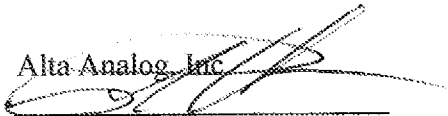


RICHARD ORLANDO

Acknowledgment of Receipt:

Dated: 6/17/2014

Alta Analog, Inc.



Richard Orlando
President

June 27, 2014

VIA HAND DELIVERY

Attn: Richard Orlando, President
Alta Analog, Inc.
24020 Summit Woods Drive
Los Gatos, CA 95033

Re: Demand for Delivery of Possession of Collateral

Dear Alta Analog, Inc.:

This is to advise you that you are in default under the terms of the security agreement between Richard Orlando and AVM Capital LP, on the one hand, and Alta Analog, Inc., on the other hand, dated June 30, 2010, and as amended by the Modification One To The Third Amended Security Agreement And The Reimbursement Agreement dated October 31, 2011 ("Security Agreement"). Further, you have failed to cure the default within the period specified in the Security Agreement.

Pursuant to California U.C.C. § 9609, this letter constitutes written demand that you turn over possession of the following collateral to the secured party:

- PATENT NO. 8,194,015 (Reduction of the effect of AVDD power supply variation on gamma reference voltages and the ability to compensate for manufacturing variations);
- PATENT No. 8,188,952 (System and method for reducing LCD flicker);
- PATENT NO. 7,557,788 (Gamma reference voltage generator);
- PATENT NO. 7,554,843, Serial bus incorporating high voltage programming signals);
- PATENT NO. 7,233,305 (Gamma reference voltage generator);
- PATENT NO. 7,061,380 (Monitoring and recording tag with RF interface and indicator for fault event);

Attn: Richard Orlando, President

Alta Analog, Inc.

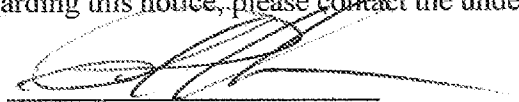
Page 2 of 2

- PATENT NO. 6,985,372 (Analog content addressable memory (CAM) employing analog nonvolatile storage);
- PATENT NO. 6,693,828 (Method for compensating field-induced retention loss in non-volatile storage with reference cells); and
- Various Product Inventory (Wafer and Packaged)

If you fail to deliver possession of the collateral to the undersigned on or before June 27, 2014, and we are forced to file a lawsuit to obtain possession of the collateral, all attorney's fees we incur in obtaining possession of the collateral will be included in the debt secured by the collateral pursuant to the terms of the Security Agreement.

If you have any questions regarding this notice, please contact the undersigned.

Dated: June 27, 2014



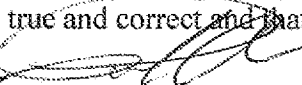
Richard Orlando

I, Richard Orlando, declare and state that:

1. I am the President of the Debtor Alta Analog, Inc. ("Debtor") and am duly authorized to make this declaration and take the actions described herein on the Debtor's behalf.
2. Richard Orlando and AVM Capital LP are the secured parties under the terms of a security agreement between Richard Orlando and AVM Capital LP, on the one hand ("Secured Party"), and Alta Analog, Inc., on the other hand, dated June 30, 2010, and as amended by the Modification One To The Third Amended Security Agreement And The Reimbursement Agreement dated October 31, 2011 ("Security Agreement"), pursuant to which the Debtor granted to Secured Party a security interest in the following collateral:
 - PATENT NO. 8,194,015 (Reduction of the effect of AVDD power supply variation on gamma reference voltages and the ability to compensate for manufacturing variations);
 - PATENT No. 8,188,952 (System and method for reducing LCD flicker);
 - PATENT NO. 7,557,788 (Gamma reference voltage generator);
 - PATENT NO. 7,554,843, Serial bus incorporating high voltage programming signals);
 - PATENT NO. 7,233,305 (Gamma reference voltage generator);
 - PATENT NO. 7,061,380 (Monitoring and recording tag with RF interface and indicator for fault event);
 - PATENT NO. 6,985,372 (Analog content addressable memory (CAM) employing analog nonvolatile storage);
 - PATENT NO. 6,693,828 (Method for compensating field-induced retention loss in non-volatile storage with reference cells); and
 - Various Product Inventory (Wafer and Packaged)
3. The Debtor has defaulted in its obligations under the Security Agreement.
4. Pursuant to the provisions of Division 9 of the California Uniform Commercial Code, the Debtor renounces its rights to require that the Secured Party comply with the provisions in Chapter 6 of Division 9 relating to disposition of the collateral.
5. The Debtor waives any and all rights the Debtor may have to redeem the collateral under both the terms of the Security Agreement and the provisions of California U.C.C. § 9623.

6. In accordance with the provisions of California U.C.C. § 9629, in consideration of the Debtor's renunciation of its rights under Chapter 6 of Division 9 of the California Uniform Commercial Code, Secured Party waives any right to a deficiency on the debt secured by the collateral.

I declare under penalty of perjury under the laws of the State of California that the foregoing is true and correct and that this declaration was executed on June 27, 2014 at Los Gatos, California.


Richard Orlando

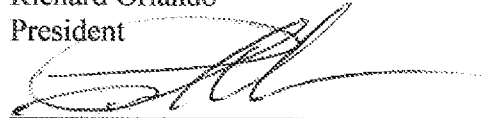
IT IS SO AGREED

Dated: 6/27/2014

Alta Analog, Inc.


Richard Orlando
President

Dated: 6/27/2014


Richard Orlando



CHANGE OF CORRESPONDENCE ADDRESS Application

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/746,333
Filing Date	12/23/2003
First Named Inventor	Richard V. Orlando
Art Unit	2629
Examiner Name	Tom V Sheng
Attorney Docket Number	ALTA-P007

Please change the Correspondence Address for the above-identified patent application to:

☐ The address associated with
Customer Number:

OR

☒ Firm or
Individual Name Alta Analog, Inc. Attn: Richard V. Orlando

Address 1737 North First Street, Suite 620

City San Jose

State CA

Zip 95112

Country U.S.A

Telephone (408) 441-9600 Ext. 301

Email rorlando@alta-analog.com

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

I am the:

☐ Applicant/Inventor

☐ Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 34,160

☐ Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number _____

Signature

Typed or Printed
Name Dennis S. Fernandez

Date 05/04/2007

Telephone (650) 325-4999

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/746,333	7233305	2629	9200



Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 22877 on 05/22/2009

- Correspondence Address
- Power of Attorney Address

The address of record for Customer Number 22877 is:

22877

**FERNANDEZ & ASSOCIATES LLP
1047 EL CAMINO REAL
SUITE 201
MENLO PARK, CA 94025**

USPTO
ACQUISITION
DIVISION

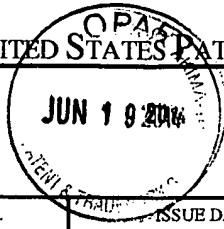
2014 JUN 23 PM 1:30

PART 1 - ATTORNEY/APPLICANT COPY

page 1 of 1



UNITED STATES PATENT AND TRADEMARK OFFICE



UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/746,333	06/19/2007	7233305	ALTA-P007	3420

7590 05/30/2007
ALTA ANALOG, INC.
ATTN: RICHARD V. ORLANDO
1737 NORTH FIRST STREET,
SUITE 620
SAN JOSE, CA 95112

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 540 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

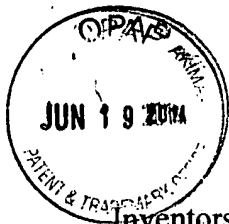
Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Richard V. Orlando, Los Gatos, CA;
Trevor A. Blyth, Sandy, UT;

2007 JUN 23 PM 1:30
UNITED STATES PATENT AND TRADEMARK OFFICE
DIVISION



PATENT
U.S. Pat. No. 7,233,305
Atty. Dkt. No. ALTA-P007

121
9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Richard V. Orlando et al. Attorney Docket No.: ALTA-P007
Serial No.: 10/746,333 Patent No.: 7,233,305
Filed: 12/23/2003 Issued: June 19, 2007
Title: GAMMA REFERENCE VOLTAGE GENERATOR

**PETITION TO ACCEPT UNINTENTIONALLY DELAYED PAYMENT OF
MAINTENANCE FEE IN AN EXPIRED PATENT (37 CFR 1.378(b))**

Mail Stop: Petitions
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

USPTO
RECEIPTS ACCOUNTING
DIVISION
2014 JUN 23 PM 1:29

Sir:

Applicant hereby submits this Petition to Accept Unintentionally Delayed Payment of Maintenance Fee in an Expired Patent pursuant to the provisions of 37 CFR 1.378(b).

The required maintenance fee for small entity \$800.00 and petition fee of \$850.00 is attached.

The delay in payment of the maintenance fee was unintentional, and Applicant provides the following evidence in support thereof:

On or about May 30, 2014, Applicant became aware that the above-referenced patent had expired for non-payment of maintenance fees. Applicant immediately contacted counsel Fernandez & Associates, LLP to inquire if any notifications from the U.S. Patent and

Trademark Office had been received and to begin the petition process to reinstate the expired patent.

On May 8, 2007, counsel Fernandez & Associates, LLP submitted a Change of Correspondence Address to the United States Patent & Trademark Office. The Change of Correspondence Address provided Alta Analog, Inc., 1737 N. First Street, #620, San Jose, CA 95112 as the new correspondence address. A copy of the Change of Correspondence Address is attached hereto and incorporated herein by reference as Exhibit "1".

On or about June 19, 2007, Alta Analog received the Issue Notification from the U.S. Patent & Trademark Office at the new correspondence address of 1737 N. First Street, #620, San Jose, CA 95112. A copy of the Issue Notification is attached hereto and incorporated herein by reference as Exhibit "2".

On or about May 22, 2009, Fernandez & Associates, LLP received Correspondence Address / Fee Address Change from the United States Patent & Trademark Office. A copy of the Notice is attached hereto and incorporated herein by reference as Exhibit "3". This Notice appears to indicate a change of address for customer number 22877 and was filed in U.S. Patent No. 7,233,305. The address appearing on the Notice for Fernandez & Associates, LLP was 1047 El Camino Real, Suite 201, Menlo Park, CA 94025. The undersigned understands that it was the intention of Fernandez & Associates to change the correspondence address for its customer number and not U.S. Patent No. 7,233,305.

The undersigned tracks payment due dates, including Patent Office maintenance fees, using Microsoft Outlook. During the approximate time line of September, 2010, the Outlook

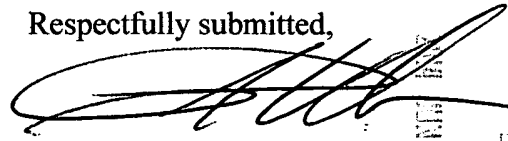
Calendar and computer failed and approximately four months of calendar inputs, data and emails were lost.

After Applicant and its attorneys reviewed their respective records, neither Alta Analog nor Fernandez & Associates, LLP received the courtesy maintenance fee reminder or patent expiration notice from the United States Patent & Trademark Office. A telephone call to the Maintenance Fee Branch was placed on May 30, 2014 inquiring as to the address to which the expiration notice was mailed and resulted in another correspondence address of 1175 Osborn Avenue, Atherton, CA 94027. Fernandez & Associates, LLP was advised by "Glenda" that she was unable to confirm the address where the expiration notice was sent and that the physical file could be pulled from storage to determine the mailing address on the expiration notice and/or if the expiration notice was returned to the United States Patent & Trademark Office.

If any additional information is required, the undersigned can be reached at (408) 499-8455.

Applicant respectfully requests that the Petition to Accept Unintentionally Delayed Payment of Maintenance Fee in the above-referenced expired patent be granted.

Respectfully submitted,



Richard V. Orlando
Alta Analog, Inc.
24020 Summit Woods Drive
Los Gatos, CA 95033
(408) 499-8455

| Dated: June 16, -2014

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Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 08/27/2014

GARIAS	ADJ #00000001	Mailroom Dt: 06/19/2014	
	Seq No: 9	Sales Acctg Dt: 06/27/2014	10746333
	01 FC : 1599	-1685.00 OP	

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 08/27/2014

GARIAS	SALE	#00000001	Mailroom Dt:	06/19/2014	10746333
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		02	FC : 2558	850.00	OP
		03	FC : 1599	35.00	OP



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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/746,333	7233305	2629	9200



Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 22877 on 05/22/2009

- Correspondence Address
- Power of Attorney Address

The address of record for Customer Number 22877 is:

22877
FERNANDEZ & ASSOCIATES LLP
1047 EL CAMINO REAL
SUITE 201
MENLO PARK, CA 94025



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/746,333	06/19/2007	7233305	ALTA-P007	3420

7590 05/30/2007

ALTA ANALOG, INC.
ATTN: RICHARD V. ORLANDO
1737 NORTH FIRST STREET,
SUITE 620
SAN JOSE, CA 95112

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 540 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

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APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Richard V. Orlando, Los Gatos, CA;
Trevor A. Blyth, Sandy, UT;



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
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 Alexandria, Virginia 22313-1450
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BIBDATASHEET

CONFIRMATION NO. 3420

Bib Data Sheet

SERIAL NUMBER 10/746,333	FILING OR 371(c) DATE 12/23/2003 RULE	CLASS 345	GROUP ART UNIT 2629	ATTORNEY DOCKET NO. ALTA-P007	
APPLICANTS Richard V. Orlando, Los Gatos, CA; Trevor A. Blyth, Sandy, UT;					
** CONTINUING DATA ***** This appln claims benefit of 60/477,680 06/11/2003					
** FOREIGN APPLICATIONS *****					
IF REQUIRED, FOREIGN FILING LICENSE GRANTED** SMALL ENTITY ** ** 09/03/2004					
Foreign Priority claimed ☐ yes ☐ no 35 USC 119 (a-d) conditions ☐ yes ☐ no ☐ Met after met Allowance Verified and Acknowledged _____ Examiner's Signature Initials		STATE OR COUNTRY CA	SHEETS DRAWING 6	TOTAL CLAIMS 22	INDEPENDENT CLAIMS 7
ADDRESS ALTA ANALOG, INC. ATTN: RICHARD V. ORLANDO 1737 NORTH FIRST STREET, SUITE 620 SAN JOSE, CA95112					
TITLE GAMMA REFERENCE VOLTAGE GENERATOR					
FILING FEE RECEIVED 575	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. Further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590

02/21/2007

Fernandez & Associates, LLP
PO Box D
Menlo Park, CA 94026-6402

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

05/09/2007 HVUONG2 00000072 10746333

01 FC:2501

700.00 DP

SHENG ELIZONDO	(Depositor's name)
	(Signature)
05/04/2007	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/746,333

12/23/2003

Richard V. Orlando

ALTA-P007

3420

TITLE OF INVENTION: GAMMA REFERENCE VOLTAGE GENERATOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$0	\$0	\$700	05/21/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
SHENG, TOM V	2629	345-089000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☒ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

FERNANDEZ & ASSOCIATES, LLP

2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Alta Analog, Inc.

San Jose, Inc.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☒ A check is enclosed. No. 1875
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 500482 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Date 05/04/2007

Typed or printed name

DENNIS S. FERNANDEZ

Registration No. 34,160

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Certificate of Mailing By "U.S. Certified Mail" Under 37 C.F.R. 1.8	
CERTIFIED MAIL" Mailing Label Number: <u>7006 2150 0000 0447 4839</u>	Date of Deposit: <u>05/04/2007</u>
I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "CERTIFIED MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.8 on the date indicated above and is addressed to the Commissioner For Patents, Alexandria, VA 22313-1450.	
Name: <u>Feng Elizondo</u>	<u>05/04/2007</u>
Signature	Date

Docket No. : **ALTA-P007B**

TRANSMITTAL LETTER

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
ATTN: MAIL STOP ISSUE FEE

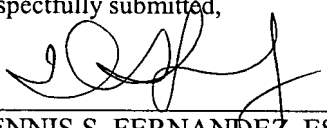
Sir:

Transmitted herewith is the issue fee for patent application 10/746,333, filed 12/23/2003 of:
Inventor(s): **Orlando, et al.**
Entitled: **Gamma Reference Voltage Generator**
Confirmation No. **3420**

Also enclosed are:

- ☒ Part B – Fee(s) Transmittal
- ☒ Change of Correspondence Address PTO/SB/122
- ☒ Return Postcard
- ☒ Check # 1875 in the amount of \$ 700.00 for Small Entity Issue Fee. However, in case Applicant inadvertently miscalculated any required fee, the Commissioner is hereby authorized to charge the necessary additional amount associated with this communication or credit any overpayment to **Deposit Account No: 500482**. A duplicate copy of this authorization is enclosed.

Respectfully submitted,


DENNIS S. FERNANDEZ, ESQ.
Reg. No. 34,160

05/04/2007

Date

CUSTOMER NO: 22877

FERNANDEZ & ASSOCIATES, LLP
PATENT ATTORNEYS
(650) 325-4999
(650) 325-1203: FAX
EMAIL: iploft@iploft.com



PTO/SB/122 (01-06)

Approved for use through 12/31/2008. OMB 0651-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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**CHANGE OF
CORRESPONDENCE ADDRESS
Application**

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/746,333
Filing Date	12/23/2003
First Named Inventor	Richard V. Orlando
Art Unit	2629
Examiner Name	Tom V Sheng
Attorney Docket Number	ALTA-P007

Please change the Correspondence Address for the above-identified patent application to:

☐ The address associated with
Customer Number:**OR**☒ Firm or
Individual Name Alta Analog, Inc. Attn: Richard V. Orlando

Address 1737 North First Street, Suite 620

City San Jose

State CA

Zip 95112

Country U.S.A

Telephone (408) 441-9600 Ext. 301

Email
rorlando@alta-analog.com

This form cannot be used to change the data associated with a Customer Number. To change the
data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

I am the:

☐ Applicant/Inventor☐ Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).☒ Attorney or agent of record. Registration Number 34,160☐ Registered practitioner named in the application transmittal letter in an application without an
executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number _____

Signature

Typed or Printed
Name

Dennis S. Fernandez

Date 05/04/2007

Telephone (650) 325-4999

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple
forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 02/21/2007

Fernandez & Associates, LLP
PO Box D
Menlo Park, CA 94026-6402

EXAMINER

SHENG, TOM V

ART UNIT

PAPER NUMBER

2629

DATE MAILED: 02/21/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/746,333	12/23/2003	Richard V. Orlando	ALTA-P007	3420
TITLE OF INVENTION: GAMMA REFERENCE VOLTAGE GENERATOR				

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$0	\$0	\$700	05/21/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

7590 02/21/2007

Fernandez & Associates, LLP
PO Box D
Menlo Park, CA 94026-6402

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/746,333	12/23/2003	Richard V. Orlando	ALTA-P007	3420

TITLE OF INVENTION: GAMMA REFERENCE VOLTAGE GENERATOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$0	\$0	\$700	05/21/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
SHENG, TOM V	2629	345-089000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
 1 _____
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/746,333	12/23/2003	Richard V. Orlando	ALTA-P007	3420

7590 02/21/2007

Fernandez & Associates, LLP
PO Box D
Menlo Park, CA 94026-6402

EXAMINER

SHENG, TOM V

ART UNIT	PAPER NUMBER
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2629

DATE MAILED: 02/21/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 540 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 540 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability

Application No.

10/746,333

Applicant(s)

ORLANDO ET AL.

Examiner

Art Unit

Tom V. Sheng

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 12/26/2006.
2. ☒ The allowed claim(s) is/are 1,2,4,5,7 and 14-22.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney Dennis S. Fernandez on 2/9/2007.

The application has been amended as follows:

Claim 1, line 11, before ".", insert --, wherein said non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and means to switch between the banks based on one or more external signals is provided on said integrated circuit--.

Claim 7, line 1, replace "claim 6" with --claim 2--.

Claim 14, lines 11 and 14, replace "programming line" with --programming pin--.

Claim 16, line 11, replace "all output" with --said plurality of outputs--.

Claim 16, line 13, replace "the programming mode" with --a programming mode to program said storage cells--.

Claim 21, line 2, replace "one" with --two--.

Please cancel claims 3, 6 and 8-13.

2. Claims 1, 2, 4, 5, 7 and 14-22 are allowed.

The following is an examiner's statement of reasons for allowance:

The invention is directed to a buffered integrated circuit programmable to output a set of gamma correction reference voltages to the source drivers in LCD displays. Once programmed, the buffers will continuously output the programmed value. The integrated circuit incorporates a programming interface to allow the programming of the buffer outputs to the desired values during manufacturing and test of the display panel. Multiple sets of gamma values can be programmed to provide different gamma correction curves for different user or application requirements.

Independent claim 1 identifies, inter alia, the uniquely distinct features “wherein said non-volatile storage cells are organized into one or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and means to switch between the banks based on one or more external signals is provided on said integrated circuit.”

Independent claim 14 identifies, inter alia, the uniquely distinct features “selecting a predetermined group of storage addresses using a predetermined subset of the address lines; taking the programming pin high to latch the predetermined group of storage addresses; selecting a predetermined storage cell address using all of the address lines; programming an applied gamma voltage in the selected storage cell by applying incremental voltage pulses from the programming pin.”

Independent claim 16 identifies, inter alia, the uniquely distinct features “an output pin connected to an output through a second multiplexer connected to said plurality of outputs wherein said output pin is at an output buffer voltage level of said

Art Unit: 2629

output when said integrated circuit is in a programming mode to program said storage cells for said output.”

Steffensmeier teaches a column driver for providing grayscale voltage signal to the column lines. The column driver includes analog memory devices for data storage, a graphics processor and a programmable logic device for programming, a multiplexer bus circuit for addressing one of the analog memory devices, and buffers for buffering outputs of the analog memory devices. However, Steffensmeier does not teach or suggest above claimed features.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V. Sheng whose telephone number is (571) 272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2629

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tom Sheng

AMR A. AWAD
SUPERVISORY PATENT EXAMINER



Search Notes 	Application/Control No. 10746333	Applicant(s)/Patent Under Reexamination ORLANDO ET AL.
	Examiner Sheng, Tom V	Art Unit 2629

SEARCHED			
Class	Subclass	Date	Examiner
345	89, 690	8/15/06, 8/22/06, 2/7/07	TS
348	254, 674		
358	519		

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search	8/15/06, 8/22/06, 2/7/07	TS
Inventor Search	8/15/06	TS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
345	89, 690	2/10/2007	TS
348	254, 674		
358	519		



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Bib Data Sheet

CONFIRMATION NO. 3420

SERIAL NUMBER 10/746,333	FILING OR 371(c) DATE 12/23/2003 RULE	CLASS 345	GROUP ART UNIT 2629	ATTORNEY DOCKET NO. ALTA-P007
APPLICANTS Richard V. Orlando, Los Gatos, CA; Trevor A. Blyth, Sandy, UT;				
** CONTINUING DATA ***** This appln claims benefit of 60/477,680 06/11/2003 <i>YES TS</i> ** FOREIGN APPLICATIONS ***** <i>NO TS</i>				
IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 09/03/2004 ** SMALL ENTITY **				
Foreign Priority claimed ☐ yes ☒ no 35 USC 119 (a-d) conditions met ☐ yes ☒ no ☐ Met after Allowance Verified and Acknowledged <i>[Signature]</i> <i>TS</i> Examiner's Signature Initials		STATE OR COUNTRY CA	SHEETS DRAWING 6	TOTAL CLAIMS 22
INDEPENDENT CLAIMS 7				
ADDRESS Fernandez & Associates, LLP PO Box D Menlo Park, CA94026-6402				
TITLE Gamma reference voltage generator				
FILING FEE RECEIVED 575	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit	

Index of Claims 	Application/Control No. 10746333	Applicant(s)/Patent Under Reexamination ORLANDO ET AL.
	Examiner Sheng, Tom V	Art Unit 2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	02/10/2007									
1	1	=									
2	2	=									
	3	-									
4	4	=									
5	5	=									
	6	-									
3	7	=									
	8	-									
	9	-									
	10	-									
	11	-									
	12	-									
	13	-									
6	14	=									
7	15	=									
8	16	=									
9	17	=									
12	18	=									
13	19	=									
14	20	=									
10	21	=									
11	22	=									

Update Search
EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1234	gamma adj3 voltage	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2007/02/07 14:51
S2	55109	(multiplex\$3 or encod\$3) same address\$3 same (memory or storage or register)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2007/02/07 14:58
S3	3072	345/89,690.ccls. or 348/254,674.ccls. or 358/519.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2007/02/07 14:53
S4	1	S1 same S2	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2007/02/07 14:56
S5	1	S1 and S2 and S3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2007/02/07 14:57
S6	112	(multiplex\$3 or encod\$3) same address\$3 same (memory or storage or register) same gamma	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2007/02/07 14:58
S7	5	S6 and S3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2007/02/07 14:58

Interference Search
EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	5519	(address\$3 same (memory or storage or register) same (bank or group or set or sub adj set or subset)).clm.	US-PGPUB	OR	ON	2007/02/10 14:33
L3	919	345/89,690.ccls. or 348/254,674. ccls. or 358/519.ccls.	US-PGPUB	OR	ON	2007/02/10 14:34
L4	10	2 and 3	US-PGPUB	OR	ON	2007/02/10 14:40
L5	7	(multiplex\$3 same buffer\$2 same address\$3 same program\$4).clm.	US-PGPUB	OR	ON	2007/02/10 14:41



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Orlando, *et al.*

Attorney Docket No.: ALTA-P007

Serial No.: 10/746,333

Group Art Unit: 2629

Filed: 12/23/2003

Examiner: Sheng, Tom V.

Title: GAMMA REFERENCE VOLTAGE GENERATOR

AMENDMENT

The Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In Response to the Office communication of September 6, 2006, please amend the above-identified application as follows:

Amendments to the Drawings begins on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

Conclusion begins on page 11 of this paper.

Amendments to the Drawings:

Figure 1 has been amended to add the legend "-- Prior Art --" as suggested by Examiner.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application.

Listing of Claims:

1. (Currently Amended) An integrated circuit for producing voltage signals on a plurality of outputs comprising:
 - a plurality of non-volatile storage cells;
 - circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs;
 - drivers connected to said storage cells and to the plurality of outputs; and
 - the plurality of inputs connected to said multiplexer for addressing said storage cells,

wherein said voltage signals are gamma reference voltage signals for
determining actual driving voltages of columns of a display.

2. (Original) The integrated circuit of claim 1 wherein said non-volatile storage cells are reprogrammable.
3. (Withdrawn) The integrated circuit of claim 1 wherein said voltage signals are gamma reference voltage signals for driving columns of a display.
4. (Original) The integrated circuit of claim 1 wherein said non-volatile storage cells hold analog voltage values which are a constant fraction of said gamma reference voltage signals.
5. (Original) The integrated circuit of claim 1 wherein said circuits for programming require an external source for the high voltage programming means.
6. (Original) The integrated circuit of claim 2 wherein said reprogrammable, non-volatile storage cells are organized into one or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and means to switch between the banks based on one or more external signals is provided on said integrated circuit.
7. (Original) The integrated circuit of claim 6 wherein said means to switch between banks can have a switching time from about 10 msec to about one second.
8. (Withdrawn) A method of testing a liquid crystal display requiring gamma reference voltage correction comprising the steps:

- a. manufacturing said display with gamma reference control capability
which is electrically reprogrammable and non-volatile;
- b. testing said display with at least one sensor with optical input;
- c. varying gamma reference voltage levels on columns of said display;
- d. using a predetermined algorithm to optimize said gamma reference
voltage levels to criteria sensed by said at least one sensor; and
- e. storing said gamma reference voltage levels in said gamma reference
control capability.

9. (Withdrawn) The method of claim 8 wherein the method is repeated more than once under different ambient or display conditions to generate at least one different set of gamma reference voltage levels stored in said gamma reference control capability.

10. (Withdrawn) A method of adjusting a liquid crystal display with gamma reference voltage correction capability comprising the steps:

- a. manufacturing said display with gamma reference control capability which is
electrically reprogrammable and non-volatile and including at least one
sensor on said display to sense at least one ambient condition and means
to adjust the gamma reference level based on the output of the sensor;
- b. said sensor sensing at least one ambient condition;
- c. said adjusting means selecting a set of gamma reference voltage levels based
on said sensor output and predetermined instructions; and

- d. storing said set of gamma reference voltage levels in said electrically reprogrammable and non-volatile gamma reference control capability.

11. (Withdrawn) A method of programming one or more gamma reference voltage generator integrated circuits attached to a liquid crystal display comprising the steps:

- a. selecting one or more columns on said liquid crystal display;
- b. applying one or more different gamma voltages to said liquid crystal display columns;
- c. storing said applied gamma voltages in reprogrammable, nonvolatile storage cells in said gamma reference voltage generator integrated circuits appropriate to said selected columns;
- d. applying one or more optimization criteria algorithms to said selected column optical emission;
- e. modifying said one or more different applied gamma voltages based on said one or more optimization criteria algorithms;
- f. programming said applied gamma voltages in storage cells in said gamma reference voltage generator integrated circuits appropriate to said selected columns; and
- g. repeating steps (d) through (f) until said one or more optimization criteria have been satisfied.

12. (Withdrawn) The method of claim 11 wherein said gamma reference voltage generator integrated circuit requires an external source for the high voltage programming means.
13. (Withdrawn) A liquid crystal display with gamma reference voltage correction capability which is electrically reprogrammable and non-volatile wherein the gamma reference voltage correction capability contains one or more sets of analog voltage levels for optimizing the column voltages under one or more display conditions.
14. (Currently Amended) A method of programming a gamma reference voltage generator integrated circuit comprising the steps:
- a. selecting a predetermined address using all address lines;
 - b. taking ~~the~~ a programming pin high;
 - c. selecting a predetermined group of storage addresses using a predetermined subset of the address lines;
 - d. taking the programming pin high to latch the predetermined group of storage address;
 - e. selecting a predetermined storage cell address using all of the address lines;
 - f. programming ~~said~~ an applied gamma voltage[[s]] in the selected storage cell by applying incremental voltage pulses from the programming line;
 - g. monitoring the result of said incremental voltage pulses by reading ~~the~~ an output buffer line associated with said selected storage cell; and



h. continuing the incremental voltage pulses from the programming line until the output buffer line associated with said selected storage cell achieves a predetermined value.

15. (Currently Amended) The method of claim 14 wherein said gamma reference voltage generator integrated circuit requires an external source for the supplying high voltage to the programming pin means.

16. (Currently Amended) An integrated circuit for producing voltage signals on a plurality of outputs comprising:

a plurality of non-volatile storage cells;

circuits for programming coupled to a multiplexer for addressing and

programming said storage cells, wherein the addressing is based on a plurality of inputs;

drivers connected to said storage cells and to the plurality of outputs;

the plurality of inputs connected to said multiplexer for addressing said storage cells; and

an output pin connected to an output ~~buffer~~ through a second multiplexer connected to all output ~~buffers~~ wherein said output pin is at an ~~the~~ output buffer voltage level of said output when said integrated circuit is in the programming mode for said output ~~buffer~~.

17. (Original) The integrated circuit of claim 16 wherein said non-volatile storage cells are reprogrammable.

18. (Original) The integrated circuit of claim 16 wherein said voltage signals are gamma reference voltage signals for driving columns of a display.
19. (Original) The integrated circuit of claim 16 wherein said non-volatile storage cells hold analog voltage values which are a constant fraction of said gamma reference voltage signals.
20. (Currently Amended) The integrated circuit of claim 16 wherein said circuits for programming require an external source for ~~the~~ supplying high voltage ~~programming~~ means.
21. (Original) The integrated circuit of claim 17 wherein said reprogrammable, non-volatile storage cells are organized into one or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and means to switch between the banks based on one or more external signals is provided on said integrated circuit.
22. (Original) The integrated circuit of claim 21 wherein said means to switch between banks can have a switching time from about 10 msec to about one second.

Remarks/Arguments

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application and indicating that claims 3, 4, 6, 7 and 14-22 contain allowable subject matter.

Claim Amendments

Claim 1 has been amended to include the allowable subject matter of dependent claim 3 and to eliminate the insufficient antecedent issue of claim 4 and the indefinite issue of claim 1.

Claims 3 and 8-13 have been withdrawn from further consideration

Claim 14 has been amended to eliminate the insufficient antecedent basis issue.

Claim 15, 16 and 20 have been amended to eliminate the indefinite issue.

No new matter has been added in any of the aforementioned amendments.

Claim Rejections – 35 USC §112

Claims 4, 12 and 14 are rejected under 35 USC 112, second paragraph, for insufficient antecedent basis. Claim 4 depends from claim 1 which has been amended to eliminate the insufficient antecedent basis issue. Claim 12 has been withdrawn and the rejection is moot. Claim 14 has been amended to eliminate the insufficient antecedent basis issue. Accordingly, the withdrawal of the rejection is respectfully requested.

Claims 1-7, 12 and 16-22 are rejected under 35 USC 112, second paragraph, as being indefinite. Claims 1 and 16 have been amended to eliminate the indefinite issue. Claims 3 and 12 have been withdrawn and the rejection is moot. Claims 2, 4-7 depend, directly or indirectly,

from claim 1. Claims 17-22 depend, directly or indirectly, from claim 16. Accordingly, the withdrawal of the rejection is respectfully requested.

Claim Rejections – 35 USC §102

Claims 1, 2 and 5 are rejected under 35 USC 102(b) as being anticipated by US Patent to Steffensmeier, number 6,373,478 B1 (Steffensmeier). As discussed above, independent claim 1 has been amended to include the allowable subject matter of cancelled dependent claim 3. Thus, amended independent claim 1 is now allowable. Further, dependent claims 2 and 4-7 are also allowable for at least the same reasons as the amended independent claim 1. In view of the above, the aforementioned rejection is now moot. Accordingly, withdrawal of this rejection is respectfully requested.

Claim Rejections – 35 USC §103

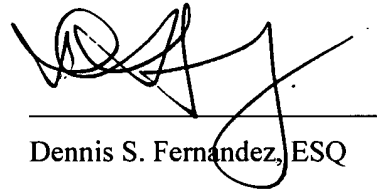
Claims 8-13 are rejected under 35 USC 103(a) as being unpatentable. Claims 8-13 have been withdrawn from further consideration therefore the rejection is now moot. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

In view of the foregoing, Applicants believe that all of the claims 1, 2, 4-7 and 14-22 are now in condition for allowance and respectfully request the Examiner to issue a timely Notice of Allowance. If for any reason, the Examiner believes any of the claims are not in condition for allowance, he is encouraged to phone the undersigned at (650) 325-4999 so that any remaining issues may be resolved.

The above changes are believed not to add new matter, as support is found in the specification.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Dennis S. Fernandez', is written over a horizontal line.

Dennis S. Fernandez, ESQ

Reg. No. 34,160

Date: 12/14/2006

Address: **FERNANDEZ & ASSOCIATES, LLP**
Patent Attorneys

Customer No: **22877**

Phone: (650) 325-4999
Fax: (650) 325-1203
Email: iploft@iploft.com



REPLACEMENT SHEET

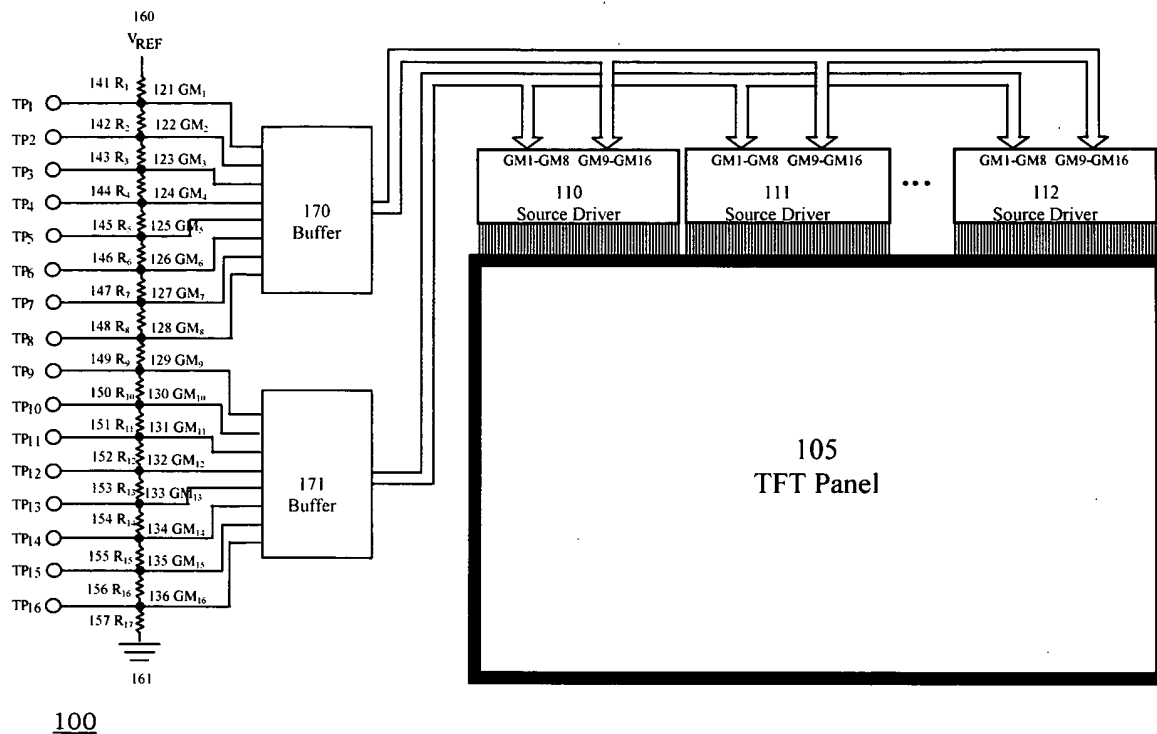


FIG. 1 -- Prior Art --



1507

Certificate of Mailing By "U.S. Certified Mail" Under 37 C.F.R. 1.8
"CERTIFIED MAIL" Mailing Label Number: 7006 2150 0000 0447 4228 Date of Deposit: 12/14/2006
I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "CERTIFIED MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.8 on the date indicated above and is addressed to the Commissioner For Patents, Alexandria, VA 22313-1450.
Name: Feng Elizondo
Signature: [Signature]
Date: 12/14/2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Orlando, et al.
Serial No.: 10/746,333
Filed: 12/23/2003
For: Gamma Reference Voltage Generator

Attorney Docket No. ALTA-P007
Examiner: Sheng, Tom V
Art Unit: 2629

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTN: Mail Stop Amendment

AMENDMENT TRANSMITTAL LETTER

Dear Sir:

1. **TRANSMITTED DOCUMENTS:** the following documents relating to the above-identified patent application are being transmitted herewith.

- ☒ a. An Amendment for this application: 11 pages.
☒ b. Substituted Drawings: 1 sheets.
☐ c. A Petition For Extension of Time For Response under 37 CFR 1.136(a) incorporated herein.
☐ d. An Information Disclosure Statement under 37 CFR 1.97(b) ☒ 1.97(c)
☒ e. A stamped, self-addressed, return postcard.
☒ f. A Check (# 1735) for \$ 60.00 to cover required fees of this correspondence.

2. **APPLICANT FILING STATUS:**

- ☐ a. Applicant is a Large Entity.
☒ b. Applicant is a Small Entity.

3. **EXTENSION OF TIME:**

- ☒ a. Applicant petitions for an extension of time under 37 C.F. R. 1.136 for the total number of months checked below (fees pursuant to 37 C.F.R. 1.17(a)-(d).

Extension of Time	Large Entity Fee	Small Entity Fee
i. One (1) month .	\$ 120.00	☒ \$ 60.00
ii. Two (2) month .	\$ 450.00	\$ 225.00
iii. Three (3) month .	\$ 1,020.00	\$ 510.00

Extension Time Fee Total: \$ 60.00

- ☐ b. Applicant believes that no extension of time is required. However, this conditional petition is being made in case Applicant has inadvertently overlooked the need for a petition for extension of time, the Commissioner is hereby authorized to charge any necessary amount associated with this communication or credit any overpayment to Deposit Account No: 500482.

12/28/2006 AWONDAF1 00000002 10746333

01 FC:2251

60.00 0P

4. FEE CALCULATION:

The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid	Present Extra Claims	Fee Rate	Total
a. Total Claims	15	- 22 =	0	x \$ 50.00 Large Entity x \$ 25.00 Small Entity	\$0.00
b. Independent Claims	3	- 7 =	0	x \$200.00 Large Entity x \$100.00 Small Entity	\$0.00
c. Multiple Dependent Claims Added By This Amendment				x 360.00 Large Entity x 180.00 Small Entity	\$0.00
d. Extension of Time Fee Total, if any, from above EXTENSION OF TIME section 3a.					\$60.00
e. Additional Fees Required With This Correspondence i) 1.17 (p) Fee for Information Disclosure under 1.97(c)					\$0.00
f. Total Fees					\$60.00

5. PAYMENT OF FEES

The full fee due in connection with this communication is provided as follows:

X The Commissioner is hereby authorized to charge the fees associated with this communication or credit any overpayment to **Deposit Account No: 500482**. A duplicate copy of this authorization is enclosed.

X A Check # 1735 for \$ 60.00 for the above specified Total Fee is enclosed. However, should Applicant inadvertently miscalculated the required fee, the Commissioner is hereby authorized to charge the necessary additional amount associated with this communication or credit any overpayment to **Deposit Account No: 500482**.

 Applicant does not believe that any payment of fee is needed in association with this communication. However, should Applicant inadvertently miscalculated the required fee, the Commissioner is hereby authorized to charge any necessary amount associated with this communication or credit any overpayment to **Deposit Account No: 500482**.

Please direct all correspondence concerning the above-identified application to the following address:

CUSTOMER NO: 22877

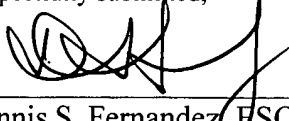
FERNANDEZ & ASSOCIATES, LLP

Patent Attorneys

Phone: (650) 325-4999

Fax: (650) 325-1203

Respectfully submitted,


Dennis S. Fernandez ESQ
Registration No. 34,160

12/14/2006
Date

Substitute for Form PIO-875

Application of Duquenois Number

10/746333

(Column 1)

(Column 2)

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Or

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* If the difference in column 1 is less than zero, enter "0" in column 2.

(Column 1)

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(Column 3)

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b. The entry in column 1 is less than the entry in column 2, write 0 in column 3.
 c. If the Highest Number Previously Paid For of HHS 506C(1) is less than 25, enter 25.
 d. If the Highest Number Previously Paid For of HHS 506C(1) is less than 1, enter 1.
 e. The Highest Number Previously Paid For (Total or Independently) is the highest number

This collection of information is required by 37 CFR 1.65. The information is required to obtain or retain a benefit by the public which is, by law (and by the USPTO) in part at least, non-derogable. Confidentiality is governed by 35 USC § 122 and 37 CFR 1.65. This collection is shown and retained 12 months to complete inclusion of allowing, preparing, and submitting the completed application form by the USPTO. There will vary depending upon the individual case. Any comments on the subject of how you respond to complete this form and suggestions for improving the form should be sent to your local Information Office or US Patent and Trademark Office or US Department of Commerce, P.O. Box 1450 Alexandria, VA 22314; (703) 835-9300; (703) 835-9301; (703) 835-9302; (703) 835-9303; (703) 835-9304; (703) 835-9305; (703) 835-9306; (703) 835-9307; (703) 835-9308; (703) 835-9309; (703) 835-9310; (703) 835-9311; (703) 835-9312; (703) 835-9313; (703) 835-9314; (703) 835-9315; (703) 835-9316; (703) 835-9317; (703) 835-9318; (703) 835-9319; (703) 835-9320; (703) 835-9321; (703) 835-9322; (703) 835-9323; (703) 835-9324; (703) 835-9325; (703) 835-9326; (703) 835-9327; (703) 835-9328; (703) 835-9329; (703) 835-9330; (703) 835-9331; (703) 835-9332; (703) 835-9333; (703) 835-9334; (703) 835-9335; (703) 835-9336; (703) 835-9337; (703) 835-9338; (703) 835-9339; (703) 835-9340; (703) 835-9341; (703) 835-9342; (703) 835-9343; (703) 835-9344; (703) 835-9345; (703) 835-9346; (703) 835-9347; (703) 835-9348; (703) 835-9349; (703) 835-9350; (703) 835-9351; (703) 835-9352; (703) 835-9353; (703) 835-9354; (703) 835-9355; (703) 835-9356; (703) 835-9357; (703) 835-9358; (703) 835-9359; (703) 835-9360; (703) 835-9361; (703) 835-9362; (703) 835-9363; (703) 835-9364; (703) 835-9365; (703) 835-9366; (703) 835-9367; (703) 835-9368; (703) 835-9369; (703) 835-9370; (703) 835-9371; (703) 835-9372; (703) 835-9373; (703) 835-9374; (703) 835-9375; (703) 835-9376; (703) 835-9377; (703) 835-9378; (703) 835-9379; (703) 835-9380; (703) 835-9381; (703) 835-9382; (703) 835-9383; (703) 835-9384; (703) 835-9385; (703) 835-9386; (703) 835-9387; (703) 835-9388; (703) 835-9389; (703) 835-9390; (703) 835-9391; (703) 835-9392; (703) 835-9393; (703) 835-9394; (703) 835-9395; (703) 835-9396; (703) 835-9397; (703) 835-9398; (703) 835-9399; (703) 835-9400; (703) 835-9401; (703) 835-9402; (703) 835-9403; (703) 835-9404; (703) 835-9405; (703) 835-9406; (703) 835-9407; (703) 835-9408; (703) 835-9409; (703) 835-9410; (703) 835-9411; (703) 835-9412; (703) 835-9413; (703) 835-9414; (703) 835-9415; (703) 835-9416; (703) 835-9417; (703) 835-9418; (703) 835-9419; (703) 835-9420; (703) 835-9421; (703) 835-9422; (703) 835-9423; (703) 835-9424; (703) 835-9425; (703) 835-9426; (703) 835-9427; (703) 835-9428; (703) 835-9429; (703) 835-9430; (703) 835-9431; (703) 835-9432; (703) 835-9433; (703) 835-9434; (703) 835-9435; (703) 835-9436; (703) 835-9437; (703) 835-9438; (703) 835-9439; (703) 835-9440; (703) 835-9441; (703) 835-9442; (703) 835-9443; (703) 835-9444; (703) 835-9445; (703) 835-9446; (703) 835-9447; (703) 835-9448; (703) 835-9449; (703) 835-9450; (703) 835-9451; (703) 835-9452; (703) 835-9453; (703) 835-9454; (703) 835-9455; (703) 835-9456; (703) 835-9457; (703) 835-9458; (703) 835-9459; (703) 835-9460; (703) 835-9461; (703) 835-9462; (703) 835-9463; (703) 835-9464; (703) 835-9465; (703) 835-9466; (703) 835-9467; (703) 835-9468; (703) 835-9469; (703) 835-9470; (703) 835-9471; (703) 835-9472; (703) 835-9473; (703) 835-9474; (703) 835-9475; (703) 835-9476; (703) 835-9477; (703) 835-9478; (703) 835-9479; (703) 835-9480; (703) 835-9481; (703) 835-9482; (703) 835-9483; (703) 835-9484; (703) 835-9485; (703) 835-9486; (703) 835-9487; (703) 835-9488; (703) 835-9489; (703) 835-9490; (703) 835-9491; (703) 835-9492; (703) 835-9493; (703) 835-9494; (703) 835-9495; (703) 835-9496; (703) 835-9497; (703) 835-9498; (703) 835-9499; (703) 835-9500; (703) 835-9501; (703) 835-9502; (703) 835-9503; (703) 835-9504; (703) 835-9505; (703) 835-9506; (703) 835-9507; (703) 835-9508; (703) 835-9509; (703) 835-9510; (703) 835-9511; (703) 835-9512; (703) 835-9513; (703) 835-9514; (703) 835-9515; (703) 835-9516; (703) 835-9517; (703) 835-9518; (703) 835-9519; (703) 835-9520; (703) 835-9521; (703) 835-9522; (703) 835-9523; (703) 835-9524; (703) 835-9525; (703) 835-9526; (703) 835-9527; (703) 835-9528; (703) 835-9529; (703) 835-9530; (703) 835-9531; (703) 835-9532; (703) 835-9533; (703) 835-9534; (703) 835-9535; (703) 835-9536; (703) 835-9537; (703) 835-9538; (703) 835-9539; (703) 835-9540; (703) 835-9541; (703) 835-9542; (703) 835-9543; (703) 835-9544; (703) 835-9545; (703) 835-9546; (703) 835-9547; (703) 835-9548; (703) 835-9549; (703) 835-9550; (703) 835-9551; (703) 835-9552; (703) 835-9553; (703) 835-9554; (703) 835-9555; (703) 835-9556; (703) 835-9557; (703) 835-9558; (703) 835-9559; (703) 835-9560; (70



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/746,333	12/23/2003	Richard V. Orlando	ALTA-P007	3420

7590 09/06/2006
Fernandez & Associates, LLP
PO Box D
Menlo Park, CA 94026-6402

EXAMINER

SHENG, TOM V

ART UNIT PAPER NUMBER

2629

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/746,333	Applicant(s) ORLANDO ET AL.	
	Examiner Tom V. Sheng	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 December 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application (PTO-152) |
| 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/23/2003</u> . | 6) ☐ Other: _____ |

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 4 recites the limitation "said gamma reference voltage signals" in lines 2-3.

There is insufficient antecedent basis for this limitation in the claim.

4. Claim 12 recites the limitation "the high voltage programming means" in lines 2-3 and claim 15 also recites the limitation "the high voltage programming means" in lines 2-

3. There are insufficient antecedent bases for this limitation in the claims.

5. Claim 14 recites the limitation "the programming line" in line 11. There is insufficient antecedent basis for this limitation in the claim.

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6. Claims 1-7, 12 and 16-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, lines 5-6, it is unclear which “outputs” and “inputs” the claim is referring to. Please clarify by designating the relevant units being related to. Claims 2-7 are dependent on claim 1.

As for claim 3, lines 2, it is unclear as to the meaning of “gamma reference voltage signals for driving columns of a display”, since it is well known that gamma reference voltage signals are used in a source/column driver in determining the actual driving voltages of columns of a display. That is, gamma reference voltage signals do not drive the columns of a display.

As for claim 12, lines 2-3, it is unclear to one of ordinary skill in the art on how an external source and a high voltage programming means interact in order to program the gamma reference voltages.

As for claim 16, lines 5 and 8-9, it is unclear how as to the scope of the output buffers as there is no reference or relation stated between the output buffers and the outputs of the drivers. Claims 17-22 are dependent on claim 16.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 2 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Steffensmeier (US 6,373,478 B1).

As for claim 1, Steffensmeier teaches an integrated circuit for producing voltage signals (fig. 2; column driver 22 for providing grayscale voltage signal to the column lines) comprising:

a plurality of non-volatile storage cells (analog memory devices 50);

circuits for programming (a graphics processor, a programmable logic device or an application-specific integrated circuit; column 4, lines 55-60) coupled to a multiplexer (device 54, which can be a multiplexer bus circuit, and control circuit 56; column 4, lines 3-5) for addressing and programming said storage cells (device 54 provides an analog voltage to one of the analog memory device 50 while control circuit 56 controls the reception and provision of signals by and from analog devices 50; column 3, line 61 through column 4, line 12);

drivers (buffers 42) connected to said storage cells and to outputs (connected to analog devices 50 as shown); and

inputs (address and data bus 84) connected to said multiplexer for addressing said storage cells (address signal provided from control circuit 56 to device 54; column 3, lines 65-66). See column 3, line 50 through column 4, line 65.

As for claim 2, since the column driver 22 is used for driving a LCD, the voltages stored in the analog memory devices 50 change with each image change. Thus, the analog memory devices 50 are meant to be reprogrammable.

As for claim 5, the column driver 22 inherently relies on an external voltage source, such as Vcc, in order to drive the column lines with appropriate voltages.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liaw et al. (US 6,593,934 B1), hereinafter Liaw.

As for claim 8, Liaw teaches a method of testing a liquid crystal display requiring gamma reference voltage correction comprising the steps:

manufacturing said display (fig. 7A or 7B; display 10) with gamma reference control capability (by CPU 22 and memory 21 using coupled sensors 11, 12 and 13; column 6, lines 2-7; column 8, lines 40-48) which is electrically reprogrammable and non-volatile (gamma reference voltages are automatically evaluated by CPU 22 and updated in memory 21; column 6, lines 7-36; column 8, line 67 through column 9, line 2);

testing said display with at least one sensor with optical input (occurs during correction operation with sensors 11-13 as light sensors; column 6, lines 7-16; column 8, lines 49-56);

varying gamma reference voltage levels on columns of said display (evaluated

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and optimized in step 150; fig. 14; column 10, lines 18-23);

using a predetermined algorithm to optimize said gamma reference voltage levels to criteria sensed by said at least one sensor (optimized by computer software; column 10, lines 18-23); and

storing said gamma reference voltage levels in said gamma reference control capability (optimized gamma reference voltages are loaded into the display circuit, that is, the memory 21; column 10, lines 18-23).

Liaw does not teach that the display is a liquid crystal display and that the memory is non-volatile. On the other hand, one of ordinary skill in the art would recognize that LCD also has a non-uniform gamma characteristics that would require gamma correction and that a non-volatile memory would serve to avoid the need to setting gamma reference voltages every time the display is powered up.

Therefore, it would have been obvious to have a liquid crystal display with automatic gamma correction as above and with a non-volatile memory for storing the reference gamma voltages because of the applicability in LCD and the convenience of using a non-volatile memory.

11. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liaw as applied to claim 8 above, and further in view of Stessen et al. (US 7,038,721 B2), hereinafter Stessen.

As for claim 9, Liaw's gamma correction is performed to obtain the voltage-to-luminance curve so as to evaluate the gamma reference voltages for the display being

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utilized. Thus, Liaw does not teach generating gamma reference voltages based on ambient or display conditions. Further, Liaw does not teach storing all these different sets in the memory. Stressen teaches further the need for gamma correction based on ambient light condition since the optimum value of the overall gamma depends on ambient light conditions (column 1, lines 31-38). Moreover, expanding the memory for storing multiple sets of gamma reference voltages serve to save time and involvement in doing gamma correction in the field/home

Therefore, it would have been obvious to one of ordinary skill in the art to do these corrections for different ambient conditions because of optimal gamma correction and be able to correct beforehand prior to shipping out to stores.

Claims 10, 11 and 13's limitations correspond to those of claims 8 and 9 and are rejected accordingly.

As for claim 12, a regular voltage source, such as Vcc, reads on claimed external source.

Allowable Subject Matter

12. Claims 14-15 and 16-22 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

13. Claim 3, 4, 6 and 7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

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14. The following is a statement of reasons for the indication of allowable subject matter: none of the prior arts of record teaches the limitations "wherein said voltage signals are gamma reference voltage signals for driving columns of a display" of claim 3, "wherein said non-volatile storage cells hold analog voltage values which are a constant fraction of gamma reference voltage signals" of claim 4, "wherein said reprogrammable, non-volatile storage cells are organized into one or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and means to switch between the banks based on one or more external signals is provided on said integrated circuit" of claim 6, the programming method as cited in claim 14, and "an output pin connected to an output buffer through a second multiplexer connected to all output buffers wherein said output pin is at the output buffer voltage level when said integrated circuit is in the programming mode for said output buffer" of claim 16. Claim 7, 15 and 17-22 are dependent on claim 6, 14, and 16 respectively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V. Sheng whose telephone number is (571) 272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tom Sheng
August 22, 2006

AMR A. AWAD
PRIMARY EXAMINER



U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Complete if Known

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	2
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Application Number	Not yet assigned
Filing Date	12/23/2003
First Named Inventor	Orlando, et al.
Art Unit	Not yet assigned
Examiner Name	Not yet assigned
Attorney Docket Number	ALTA-P007

[illegible][illegible]

Examiner Signature	/Tom Sheng/	Date Considered	08/15/2006
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Complete if Known		
			Application Number	Not yet assigned	
			Filing Date	12/23/2003	
			First Named Inventor	Orlando, et al.	
			Art Unit	Not yet assigned	
			Examiner Name	Not yet assigned	
			Attorney Docket Number	ALTA-P007	
Sheet	2	of	2		

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Examiner Signature	<i>Tom Sherr</i>	Date Considered	<i>8/15/06</i>
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Notice of References Cited	Application/Control No. 10/746,333	Applicant(s)/Patent Under Reexamination ORLANDO ET AL.	
	Examiner Tom V. Sheng	Art Unit 2629	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,373,478	04-2002	Steffensmeier, Martin J.	345/204
*	B	US-7,038,721	05-2006	Stessen et al.	348/254
*	C	US-2002/0063666	05-2002	Kang et al.	345/87
*	D	US-6,680,733	01-2004	Woo et al.	345/212
*	E	US-6,756,961	06-2004	Hector et al.	345/98
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims



Application/Control No.

10/746,333

Examiner

Tom V. Sheng

Applicant(s)/Patent under Reexamination

ORLANDO ET AL.

Art Unit

2629

✓	Rejected
=	Allowed

—	(Through numeral) Cancelled
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N	Non-Elected
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A	Appeal
O	Objected

Claim		Date			
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Tom V. Sheng

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INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST Search See printout	8/11/06 8/22/06	TS
Inventor Search See printout	8/15/06	TS

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	300	(first adj3 (multiplexer or mux)) same (second adj3 (multiplexer or mux)) same output same program\$4	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2006/08/22 16:28
L2	2849	345/89,690.ccls. or 348/254,674. ccls. or 358/519.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/22 16:03
L3	0	1 and L2	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2006/08/22 16:03
L4	2	(first adj3 (multiplexer or mux)) same (second adj3 (multiplexer or mux)) same feedback same program\$4	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2006/08/22 16:04
L6	19	(first adj3 (multiplexer or mux)) same (second adj3 (multiplexer or mux)) same (output near2 buffer) same program\$4	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2006/08/22 16:29

Search Note

EAST Search History

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S1	0	10/746333	US-PGPUB; USPAT	OR	ON	2006/08/15 13:14
S2	3522963	(storage or memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 13:58
S4	46715	(multiplexer or encoder) same address\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 14:00
S5	54049	(programming or programmable) same voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 14:01
S6	17112	S2 and S3 and S4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 14:02
S7	1934	S2 same S3 same S4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 14:24
S8	218	S7 same driver	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 15:36
S9	2839	345/89,690.ccls. or 348/254,674. ccls. or 358/519.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 15:36
S10	3522963	(storage or memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 15:37
S11	489359	(programming or programmable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 15:37
S12	46715	(multiplexer or encoder) same address\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 15:37
S13	1934	S10 same S11 same S12	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 15:37

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S14	1	S9 and S13	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 15:41
S15	17112	S10 and S11 and S12	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 15:41
S16	25	S9 and S15	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/11 15:49
S18	3	program\$4 adj25 (multiplexor or mux) adj25 (memory or RAM or storage) adj25 (driver or buffer)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 11:31
S19	553	program\$4 same (multiplexor or mux) same (memory or RAM or storage) same (driver or buffer)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 11:32
S20	2839	345/89,690.ccls. or 348/254,674.ccls. or 358/519.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 11:31
S21	0	S19 and S20	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 11:31
S22	194	program\$4 same (multiplexor or mux) same (memory or RAM or storage) same (driver or buffer) same address\$3 and display	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 11:33
S23	114	program\$4 same (multiplexor or mux) same (memory or RAM or storage) same (driver or buffer) same address\$3 same (channel or column)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 11:38
S24	6	program\$4 same (multiplexor or mux) same (memory or RAM or storage) same (driver or buffer) same address\$3 same (channel or column) and display.ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 11:46
S25	23	(processor or controller) same (multiplexor or mux) same (memory or RAM or storage) same (driver or buffer) same address\$3 same (channel or column) and display.ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 11:47
S26	2	("6593934" or "6046719").pn.	USPAT	OR	ON	2006/08/14 11:48

EAST Search History

S27	1	"6373478".pn.	US-PGPUB; USPAT	OR	ON	2006/08/14 14:15
S28	10	("3584209" "4114995" "4335393" "4639867" "5347201" "5977942").PN. OR ("6373478"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/08/14 14:16
S29	5	gamma adj reference adj voltage same column	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:01
S30	219164	(LCD or liquid adj crystal adj display).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:35
S31	63	(gamma adj reference adj voltage). ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:36
S32	0	gamma adj reference same \$2program\$5 same optical same (sensor or sensing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:40
S33	0	gamma adj reference same var\$4 same optical same (sensor or sensing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:41
S34	0	gamma adj reference same optical same (sensor or sensing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:42
S35	1	gamma adj reference and optical near5 (sensor or sensing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:44
S36	8	gamma adj reference and optic\$2 near5 (sensor or sensing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:46
S37	0	S30 and S31 and S36	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:44
S38	0	S30 and S36	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:45

EAST Search History

S39	14	gamma adj reference and (sensor or sensing) with display	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/14 16:47
S40	125	gamma same correction same (ambient or ambiance or (display or lighting) adj condition)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2006/08/15 13:27
S41	2840	345/89,690.ccls. or 348/254,674. ccls. or 358/519.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/15 13:27
S42	13	S40 and S41	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2006/08/15 13:27

*Inventor Search***EAST Search History**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7	orlando-richard-v.in. or blyth-trevor-a.in.	US-PGPUB; USPAT	OR	ON	2006/08/15 16:18

US 7061380 B1 USPAT
US 6985372 B1 USPAT
US 6693828 B1 USPAT
US 6421213 B1 USPAT
US 6388928 B1 USPAT
US 6185127 B1 USPAT
US 5963106 A USPAT

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RE: APPLICATION STATUS INQUIRY REQUEST

Attorney Docket No.: ALTA-P007
Application No.: 10/746,333
Filing Date: 12/23/2003
Inventor(s): Orlando, et al.
Entitled: Gamma Reference Voltage Generator

Dear Sirs:

Applicant respectfully requests status information for the above-referenced non-provisional patent application filed with the U.S. Patent and Trademark Office on the date indicated above. As of the date of this mailing, Applicant has not yet received a first official action or any other communication of a substantive nature pertaining to this Application since it's filing.

If an expedited response to this status inquiry is possible, the undersigned attorney for Applicant can be reached by phone at (650) 325-4999 or via facsimile at (650) 325-1203.

Sincerely yours,
FERNANDEZ & ASSOCIATES, LLP

Dennis Fernandez
Customer No.: 22877

Fernandez & Associates, LLP
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RE: APPLICATION STATUS INQUIRY REQUEST

Attorney Docket No.:

ALTA-P007

Application No.:

10/746,333

Filing Date:

12/23/2003

Inventor(s):

Orlando, et al.

Entitled:

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Docket No.: ALTA-P007APPLICATION TRANSMITTAL LETTER

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Transmitted herewith for filing is the patent application of

Inventor(s): **ORLANDO, et al.**Entitled: **"GAMMA REFERENCE VOLTAGE GENERATOR"**

26 No. pages of specification, including title page, claims and abstract
6 No. sheets of X informal, formal drawings

Also enclosed are:

- X Executed Combined Declaration and Power of Attorney for Patent Application
- X An Original Executed Assignment of the Application
- X Form PTO-1595 (Recordation Cover Sheet for Assignment)
- X Request and Certification Form PTO/SB/35 (11-00)
- X Application Data Sheet (4 sheets)
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FEES DUEX Applicant Claims Small Entity Status (37 CFR 1.27)

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CLAIMS					
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Basic Application Fee (\$770.00 large entity; \$385 small entity)					\$ 385.00
Total Claims	22	Minus 20 =	2	X \$18 =	18.00
				X \$ 9 (small) =	
Total Independent Claims	7	Minus 3 =	4	X \$86 =	172.00
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For: **Gamma Reference Voltage Generator**
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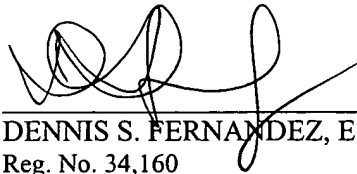
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 - (i) 17 pages prior to the claims, including title page;
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2. An original, executed Combined Declaration and Power of Attorney by named inventors;
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Respectfully submitted,


DENNIS S. FERNANDEZ, ESQ
Reg. No. 34,160

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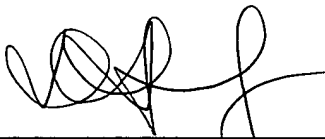
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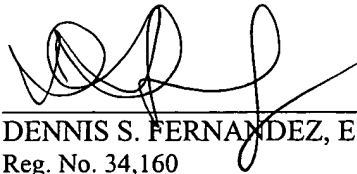
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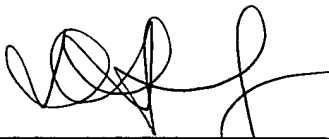
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Reg. No. 34,160

12/23/03

Date

Application

5

for

United States Non-Provisional Utility Patent

Title:

Gamma Reference Voltage Generator

10

Inventors:

Richard V. Orlando, residing at 24020 Summit Woods Drive, Los Gatos, California
95033, a citizen of the United States.

15

Trevor A. Blyth, residing at 8345 South Creek Hollow Cove, Sandy, Utah 84093, a
citizen of the United States.

Gamma Reference Voltage Generator

Cross-Reference to Related Application

This application claims priority from U.S. Provisional Application Serial No. 60/477,680

filed on 06/11/2003

5

Field of the Invention

The invention relates generally to the field of liquid crystal displays, and more particularly to TFT flat panel displays and a method of generating a gamma reference voltage.

10

Description of Related Art

Gamma Correction has long been a problem for the manufacturers of Thin Film Transistor (TFT) Flat Panel Displays. The Gamma Correction curve becomes more complex as the display resolution increases. Each display often has a different response to the gamma correction reference voltages, resulting in the need to generate specific gamma reference voltages for each model of display as well as compensating for display to display variation due to manufacturing process variations.

15

A traditional approach to the Gamma Reference Generation problem has been to use Select-On-Test Resistors. These resistors allow the reference voltages to be fine-tuned to the requirements of the individual display. The testing, selection and mounting of these resistors has become a major production problem since the process is a manual

20

one and prohibits automated assembly and test. In addition, once the resistors are mounted on the display PC board, the resistors cannot be easily changed to meet the growing requirements of individual customers for a specific Gamma characteristic.

Of course, even with the manual labor involved, Select-On-Test resistors are still
5 the least expensive solution to this problem. Devices such as potentiometers, Electrically Erasable Potentiometers (E2POTS), digitally-controlled potentiometers (DCPs) and Digital to Analog Converters (DACs) all could perform this function in some ways better than the Select-On-Test resistors, but the cost is unacceptable.

FIG. 1 is a block diagram illustrating a conventional gamma reference circuit for a
10 TFT display 105 using Select-On-Test-Resistors. In this case, source drivers 110, 111, ... and 112 require a total of 16 gamma reference voltages 121 GM_1 , 122 GM_2 , 123 GM_3 , 124 GM_4 , 125 GM_5 , 126 GM_6 , 127 GM_7 , 128 GM_8 , 129 GM_9 , 130 GM_{10} , 131 GM_{11} , 132 GM_{12} , 133 GM_{13} , 134 GM_{14} , 135 GM_{15} and , 136 GM_{16} . The gamma reference voltages are derived by a resistive divider of 17 resistors 141 R_1 , 142 R_2 , 143 R_3 , 144 R_4 , 145 R_5 ,
15 146 R_6 , 147 R_7 , 148 R_8 , 149 R_9 , 150 R_{10} , 151 R_{11} , 152 R_{12} , 153 R_{13} , 154 R_{14} , 155 R_{15} , 156 R_{16} , 157 R_{17} connected between a reference voltage 160 and ground 161. Since the loading of the source drivers 110, 111, and 112 changes dynamically, it is not possible to simply connect the resistive divider 141 R_1 , 142 R_2 , 143 R_3 , 144 R_4 , 145 R_5 , 146 R_6 , 147 R_7 , 148 R_8 , 149 R_9 , 150 R_{10} , 151 R_{11} , 152 R_{12} , 153 R_{13} , 154 R_{14} , 155 R_{15} , 156 R_{16} , 157
20 R_{17} to the inputs of the source drivers 110, 111, and 112, and some type of buffering are used, such gamma reference buffer ICs 170 and 171.

Initially the PC board is assembled without the resistors. An external test apparatus drives the test points TP1-TP16 until the desired Gamma correction is achieved. The values of the TP voltages are then used to calculate the resistors needed for the particular display under test (DUT) and the resistors are mounted on the PC board.

5 More recently quite complex approaches to Gamma correction have been published. U.S. 6,593,934 (1) and U.S. 6,046,719 (2) are examples of inventions which eliminate the "select-on-test" resistors. Both inventions teach quite complex digital approaches to this "analog" problem; consequently both inventions are quite expensive.

Accordingly, it is desirable to design a gamma reference architecture that automates
10 gamma adjustment and provides reprogrammable capability and achieves acceptable cost.

SUMMARY OF THE INVENTION

The invention is a programmable buffer integrated circuit which can be programmed to output a set of gamma correction reference voltages to be used in Liquid Crystal Displays (LCDs). Once programmed, the buffer will continuously output the programmed value; if
15 power is removed, since the voltage value is stored in non-volatile, programmable memory, the gamma correction is retained. The device incorporates a programming interface to allow the programming of the buffer outputs to the desired values during manufacturing and test of the panel. Multiple sets of gamma values can be programmed and stored to provide optimized gamma correction curves for different user or application
20 requirements.

In the preferred embodiment, the present invention allows automated assembly of an entire PC board, automated test and gamma adjustment, smaller and thinner physical size, lower power consumption, reprogrammable and non-volatile settings. Furthermore, the present invention advantageously allows a stand-alone solution such that it is not
5 necessary to incorporate a micro controller unit (MCU).

Other structures and methods are disclosed in the detailed description below. This summary does not purport to define the invention. The invention is defined by the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

10 FIG. 1 is a prior art block diagram illustrating a conventional gamma reference circuit for a TFT display using Select-On-Test-Resistors.

FIG. 2 is an architectural diagram illustrating a gamma reference circuit employing gamma reference controllers for a TFT display in accordance with one embodiment of the invention.

15 FIG. 3 is a block diagram illustrating one embodiment of a gamma reference controller in accordance with the invention.

FIG.4A and FIG. 4B are descriptions of one alternative pin out.

FIG. 5 shows exemplary electrical parameter specifications of one embodiment.

FIG. 6 is an alternative block diagram of one embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

Figure 2 is an architectural diagram, 200, illustrating a gamma reference circuit implementation employing gamma reference controllers, 210 and 220, for a TFT panel 280. The gamma reference circuit comprises a first gamma reference controller 210, a
5 second gamma reference controller 220, a programming interface 230, source drivers 240, 241, and 242, and a TFT panel 280. The gamma reference controller 210 drives a first set of eight gamma reference voltages GM1 – GM8 to the source drivers 240, 241, ... and 242. The gamma reference controller 220 drives a second set of eight gamma reference voltages GM9 – GM 16 to the source drivers 240, 241, ...and 242.

10 The Programming Interface 230 comprises a common Analog Input (A_{IN}) which will be used to set the reference voltage level, three address inputs (A_0 , A_1 , and A_2) to determine which reference level is being written and a R/W control signal for each of the first gamma reference controller 210 and second gamma reference controller 220, in this case two, that are on the board.

15 During normal operation, the R/W pin is pulled High and the reference voltage outputs will reflect the value last programmed into the nonvolatile memory cells.

The writing or programming operation is accomplished by first selecting the output or channel of the device to be programmed with the A2-A0 inputs. At this point, R/W on the device to be written is driven low and the device enters Tracking Mode.

20 During Tracking Mode, the output of the selected channel tracks the input voltage on the

Analog Input. (An optional internal voltage multiplier converts the 0-3V Analog Input to a 0-10V output.)

Once the desired voltage is found by varying the Analog Input for a particular channel, the R/W signal is driven high and the value on the Analog Input is written into the nonvolatile memory for the output channel selected by the A2-A0 inputs.

In this manner, each of the gamma reference voltages can be written in a sequential manner during display testing.

Alternatively, the first gamma reference controller 210 and second gamma reference controller 220 can be pre-loaded with a default configuration, which is close to historical values for the majority of displays. In this approach, only those parameters that need to be adjusted are changed in testing.

The first gamma reference controller 210 and second gamma reference controller 220 provide the manufacturers of TFT displays a solution to the setting of the gamma reference voltages. Automated testing of the displays and re-programming of the gamma characteristics is enabled, even after the display is completed. The first gamma reference controller 210 and second gamma reference controller 220 provide reduced overall implementation costs, reduced power consumption, reduced physical size and flexibility over the traditional Select-On-Test resistor techniques.

FIG. 3 is a block diagram illustrating one embodiment of a gamma reference controller 300. The gamma reference controller 300 comprises a programming engine or

interface 310, a mux 320, programmable analog floating gate memory cells 330, through 337, and drivers 340 through 347. The programming engine 310, coupled to the mux, comprises an Analog Input which will be used to set the reference voltage level and a R/W control signal for a corresponding gamma reference controller. The mux 320
5 connects signals from the programming engine 310 to any one of the programmable analog floating gate memory cells 330 through 337, depending on three address inputs (A_0 , A_1 , and A_2). Address inputs are used to select which cell is being written to at any time.

Each output is internally connected to an analog storage cell which can be written
10 with analog values, for example, of 1024 step (10 Bit) resolution. The outputs, channel 0 (CH0), channel 1 (CH1), ... channel 6 (CH6), and channel 7 (CH7), are intended to directly drive the reference voltage inputs of the source driver IC. An internal voltage multiplier, having a multiplication factor M, produces an output of zero up to typically 13.5 or alternatively 16 Volts. In FIG. 3, the channel 0, CH0, is driven by a driver 340,
15 which connects to the programmable analog floating gate memory cells 330. The channel 1, CH1, is driven by a driver 341, which connects to the programmable analog floating gate memory cells 331. The channel 6, CH6, is driven by a driver 346, which connects to the programmable analog floating gate memory cells 336. The channel 7, CH7, is driven by a driver 347, which connects to the programmable analog floating gate memory cells
20 337.

- During read mode, all channels continuously output their corresponding stored voltages. Applying a logic “0” to the R/W pin initiates a track and write cycle and the RDY\ pin goes to logic “1”. The addressed channel now outputs a voltage which is equal to the voltage applied to the Vin pin, multiplied by the voltage multiplication factor M.
- 5 The channel address may be changed during tracking mode. At the rising edge of R/W a write cycle is initiated and the present voltage applied to Vin is automatically stored in the analog memory corresponding to the addressed channel. Completion of the write cycle is indicated by a high to low transition at the RDY pin.

Table 1

Name	Description	Value Range	Function
VDD	Supply Input	3V to 5.5V	
Vdisp	Display Supply	10V to 12V	
R/W	Read/Write	CMOS Input	When driven to an active low input, places the selected output into tracking mode. The Rising Edge of R/W writes the voltage on the analog input into the appropriate analog memory location
Rdy	Device Ready	TTL Compatible Output	
VSS	Ground		
CH0-CH7	Analog Outputs	0V –10V	Analog Output Voltage Channels
VIN	Analog Input	0V –3V	Analog Input Voltage
A0-A3	Address Inputs	CMOS Inputs	Selects which output is placed in tracking mode or is written to during a write operation

Table 1 shows an alternative example of the pin descriptions for a gamma reference controller.

Table 2

<u>Symbol</u>	Parameter	Min	Typ	Max	Units	Condition
V_{IL}	Input Low Voltage			$V_{DD} \times 0.3$	V	
V_{IH}	Input High Voltage	$V_{DD} \times 0.7$			V	
V_{OutL}	Analog Output Low Voltage $V_{in}=0.1V$ $V_{disp}=10V$		0.33		V	$I_{OL} = 10mA$
V_{OutH}	Analog Output High Voltage $V_{in}=3V$ $V_{disp}=10V$		10		V	$I_{OH} = -10mA$
V_{OL}	Logic Output Low Voltage			0.4	V	$I_{OL} = 0.3mA$
V_{OH}	Logic Output High Voltage	$V_{DD}-0.8$			V	$I_{OH} = -250\mu A$

<u>Symbol</u>	Parameter	Min	Typ	Max	Units	Condition
I_{IL}	Input Leakage Current			± 1.0	μA	
I_{DD}	V_{DD} Current(Operating)			0.8	mA	$R_{EXT} = \infty$
				1.0	mA	$R_{EXT} = \infty$
				1.5	mA	$R_{EXT} = \infty$
I_{SB}	V_{DD} Current (Standby)			10	μA	
V_{IN}	V_{IN} Range	0		$V_{DD} - 0.8$	V	
R_{IN}	V_{IN} Input Resistance	1.0			M Ω	
AV_{IN}	Channel Gain		3.3		V/V	V_{IN} to V_{OUT}

Table 2 shows an alternative example of the electrical parameters for a gamma reference controller.

5 Examples of eight to eighteen channel Gamma reference controllers have been used; clearly larger ones, 256 channels and higher, are encompassed by the invention. Various output voltage ranges are optional as well, 0 - 5V up to 0 - 16V, depending on the display requirements. Specific ranges or limits of the various parameters are used

herein as examples of different embodiments and are not intended to limit the scope of the invention.

In one embodiment of the invention, the integrated circuit, termed the AG1818, is a programmable gamma reference generator with integrated output buffers to directly drive the source driver inputs of a display; in one embodiment the display is a TFT LCD. The circuit requires a single 3.3 volt supply, 1.5 mA operating current and consumes 10 μ A in standby mode. FIG. 4A and 4B show an alternative pin out of this embodiment.

Eighteen output channels are provided with an output range of 0 to 13.5 Volts and a drive capability of 10 milli-amps. Each output is internally connected to an analog nonvolatile storage cell which can be written with 1,024 analog values, providing 10 bit resolution, or, said another way, to better than 15 mV resolution. The output of these analog nonvolatile memory cells is internally buffered to allow for the high voltages and current needed to directly drive the reference inputs on the source drivers. The outputs can be programmed from 0.2 volts to 0.2 volts below the VREFH value. FIG. 5 shows representative electrical specifications.

In one embodiment the AG1818 has capacity to store and retrieve eight independent banks or groups of reference voltages. The banks of gamma voltages are stored and selected through the three address inputs B0, B1, B2. This allows the gamma voltages to be changed either for dynamic gamma correction or application based gamma variation. This feature can also be used to switch between different gamma settings based

on the information to be displayed for implementing dynamic gamma correction. A block diagram in FIG. 6 illustrates one alternative embodiment.

During read mode, all channels continuously output their corresponding stored
5 voltages based on the bank selected by the B0 - B2 address inputs. When deemed
appropriate an internal damping circuit creates a slow transition, about 10 msec., between
banks to prevent disruptive display artifacts caused by rapid transitions on the gamma
reference voltages during operation. Alternative damping circuits may be employed
which allow the transition between banks to be considerably slower, for instance, one
10 second, as may be required by the display manufacturer's requirements.

An independent programming interface allows the device to be programmed in-
situ thus providing the ability to individually program or adjust the gamma reference
voltages for an individual display. The device can also be programmed prior to mounting
on the pc board or display. The programming interface consists of four signals. The V_{PP}
15 is a high voltage input used to select the programming mode and also provides the high
voltage pulses used to program the individual cells. In the AG1818 embodiment, V_{PP} is
supplied from an external source, an IC or other means. The A_{OUT} analog output is used
to read the cell which is currently being programmed to verify the write operation and
proper output voltage level. The A0 through A1 inputs are used in conjunction with the
20 B0-B2 inputs to select the location to be written.

One alternative method of programming the individual cells starts by placing A0, A1, B0, B1, B2 lines in the (1,1,1,1,1) state and taking the V_{PP} pin high; this places the AG1818 in the Program mode; the read mode is the default mode. Next the particular bank is addressed through B0-B2; V_{PP} is pulsed again, latching the bank address. Next
5 the cell to be programmed in the selected bank is addressed using the A0, A1, B0, B1, B2 lines; V_{PP} is pulsed again, a third time. At this point programming of the selected storage cell is initiated by pulsing V_{PP} with adjustable voltage pulses between approximately 8 and 14 volts. When the selected cell has achieved the desired voltage level the A0, A1, B0, B1, B2 lines are again placed in the (1,1,1,1,1) state; the V_{PP} pin is pulsed; this
10 returns the AG1818 to the read mode. Programming of additional cells proceeds from the beginning sequence; any order of programming storage cells, random or sequential, can be applied.

Key variables in the programming process are programming voltage amplitude, rise and fall time of the pulse, and pulse duration; each of these variables is influenced by
15 design and process parameters of the particular wafer fabrication facility. Real time monitoring of the cell voltage level is accomplished through the A_{OUT} pin which reflects the cell voltage as it is in the output buffer which is the voltage which will be applied to the display column. The use of the A_{OUT} pin provides an essential countermeasure to the vagaries of the design and fabrication processes. Independent of what voltage actually is
20 stored in the cell the Aout pin gives the ability for closed loop programming such that a precise gamma reference voltage is provided to a specific column. As mentioned previously, this programming step can take place prior to mating the gamma reference

chip with a display wherein a predetermined set of voltage values is stored. Alternatively, the programming can take place after the gamma reference chip and display are mated; in this case the display quality can be evaluated as the gamma reference chip is being programmed if required.

5 One knowledgeable in the art that understands that other addressing schemes, such as a serial one, are possible, enabling an overall reduction in the pin count. Having bank switching capability ensures that the optimum gamma curve is used for each individual display and eliminates the need for re-work due to display manufacturing process variations. A PC based programming interface is available for prototyping and
10 gamma optimization. This PC programming interface may be an alternative source of the V_{PP} signals. Display optimization algorithms may be located in such a PC which also may be connected to monitors feeding back data from the display during the optimization tuning at time of manufacture.

 This invention also enables several additional features for the user and
15 manufacturer. Automating the testing of a panel can be achieved with optical sensors and feedback to the gamma correction section of the display. Once the optical sensors have modulated gamma reference voltage levels for the columns to achieve the predetermined light matching for the display these values can be saved in the gamma reference circuitry. In this way different application conditions can be pretested and stored. For the user, a
20 sensor can be supplied with the display which responds to the temperature, lighting or

other conditions present. The output of the sensor can be matched to a predetermined application condition which selects the corresponding gamma value set.

The above embodiments are only illustrative of the principles of this invention and are not intended to limit the invention to the particular embodiments described.

5 Although the above embodiment describes the application of a gamma trimster for a TFT display, one of skill in the art should know that the present invention can be practiced in various types of displays and screens. Accordingly, various modifications, adaptations, and combinations of various features of the described embodiments can be practiced without departing from the scope of the invention as set forth in the appended claims.

10

Claims

What we claim is:

1. An integrated circuit for producing voltage signals comprising:

5 a plurality of non-volatile storage cells;

 circuits for programming coupled to a multiplexer for addressing and

 programming said storage cells;

 drivers connected to said storage cells and to outputs; and

 inputs connected to said multiplexer for addressing said

10 storage cells.

2. The integrated circuit of claim 1 wherein said non-volatile storage cells are reprogrammable.

3. The integrated circuit of claim 1 wherein said voltage signals are gamma reference voltage signals for driving columns of a display.

15 4. The integrated circuit of claim 1 wherein said non-volatile storage cells hold analog voltage values which are a constant fraction of said gamma reference voltage signals.

5. The integrated circuit of claim 1 wherein said circuits for programming require an external source for the high voltage programming means.

6. The integrated circuit of claim 2 wherein said reprogrammable, non-volatile storage cells are organized into one or more banks of cells

5 wherein each bank contains a predetermined gamma reference voltage signal display condition; and

means to switch between the banks based on one or more external signals is provided on said integrated circuit.

7. The integrated circuit of claim 6 wherein said means to switch between

10 banks can have a switching time from about 10 msec to about one second.

8. A method of testing a liquid crystal display requiring gamma reference voltage correction comprising the steps:

a. manufacturing said display with gamma reference control capability which is electrically reprogrammable and non-volatile;

15 b. testing said display with at least one sensor with optical input;

c. varying gamma reference voltage levels on columns of said display;

d. using a predetermined algorithm to optimize said gamma reference voltage levels to criteria sensed by said at least one sensor; and

e. storing said gamma reference voltage levels in said gamma reference control capability.

9. The method of claim 8 wherein the method is repeated more than once under different ambient or display conditions to generate at least one different set of gamma reference voltage levels stored in said gamma reference control capability.

5

10. A method of adjusting a liquid crystal display with gamma reference voltage correction capability comprising the steps:

a. manufacturing said display with gamma reference control capability which is electrically reprogrammable and non-volatile and including at least one

10

sensor on said display to sense at least one ambient condition and means to adjust the gamma reference level based on the output of the sensor;

b. said sensor sensing at least one ambient condition;

15

c. said adjusting means selecting a set of gamma reference voltage levels based on said sensor output and predetermined instructions; and

d. storing said set of gamma reference voltage levels in said electrically

reprogrammable and non-volatile gamma reference control capability.

11. A method of programming one or more gamma reference voltage generator
integrated circuits attached to a liquid crystal display comprising the steps:

a. selecting one or more columns on said liquid crystal display;

b. applying one or more different gamma voltages to said liquid crystal
display columns;

c. storing said applied gamma voltages in reprogrammable, nonvolatile
storage cells in said gamma reference voltage generator integrated
circuits appropriate to said selected columns;

d. applying one or more optimization criteria algorithms to said selected
column optical emission;

e. modifying said one or more different applied gamma voltages based on
said one or more optimization criteria algorithms;

f. programming said applied gamma voltages in storage cells in said
gamma reference voltage generator integrated circuits appropriate
to said selected columns; and

g. repeating steps (d) through (f) until said one or more optimization
criteria have been satisfied.

12. The method of claim 11 wherein said gamma reference voltage generator
integrated circuit requires an external source for the high voltage
programming means.

13. A liquid crystal display with gamma reference voltage correction capability
5 which is electrically reprogrammable and non-volatile wherein the gamma
reference voltage correction capability contains one or more sets of
analog voltage levels for optimizing the column voltages under one
or more display conditions.

14. A method of programming a gamma reference voltage generator
10 integrated circuit comprising the steps:

a. selecting a predetermined address using all address lines;

b. taking the programming pin high;

c. selecting a predetermined group of storage addresses using a
predetermined subset of the address lines;

15 d. taking the programming pin high to latch the group address;

e. selecting a predetermined storage cell address using
all of the address lines;

f. programming said applied gamma voltages in the selected storage cell

by applying incremental voltage pulses from the programming line;

g. monitoring the result of said incremental voltage pulses by reading the

output buffer line associated with said selected storage cell; and

h. continuing the incremental voltage pulses from the programming line

5 until the output buffer line associated with said selected storage

cell achieves a predetermined value.

15. The method of claim 14 wherein said gamma reference voltage generator

integrated circuit requires an external source for the high voltage

programming means.

10 16. An integrated circuit for producing voltage signals comprising:

a plurality of non-volatile storage cells;

circuits for programming coupled to a multiplexer for addressing and

programming said storage cells;

drivers connected to said storage cells and to outputs;

15 inputs connected to said multiplexer for addressing said

storage cells; and

an output pin connected to an output buffer through a second multiplexer

connected to all output buffers wherein said output pin is at the

output buffer voltage level when said integrated circuit is in the programming mode for said output buffer.

17. The integrated circuit of claim 16 wherein said non-volatile storage cells are reprogrammable.

5 18. The integrated circuit of claim 16 wherein said voltage signals are gamma reference voltage signals for driving columns of a display.

19. The integrated circuit of claim 16 wherein said non-volatile storage cells hold analog voltage values which are a constant fraction of said gamma reference voltage signals.

10 20. The integrated circuit of claim 16 wherein said circuits for programming require an external source for the high voltage programming means.

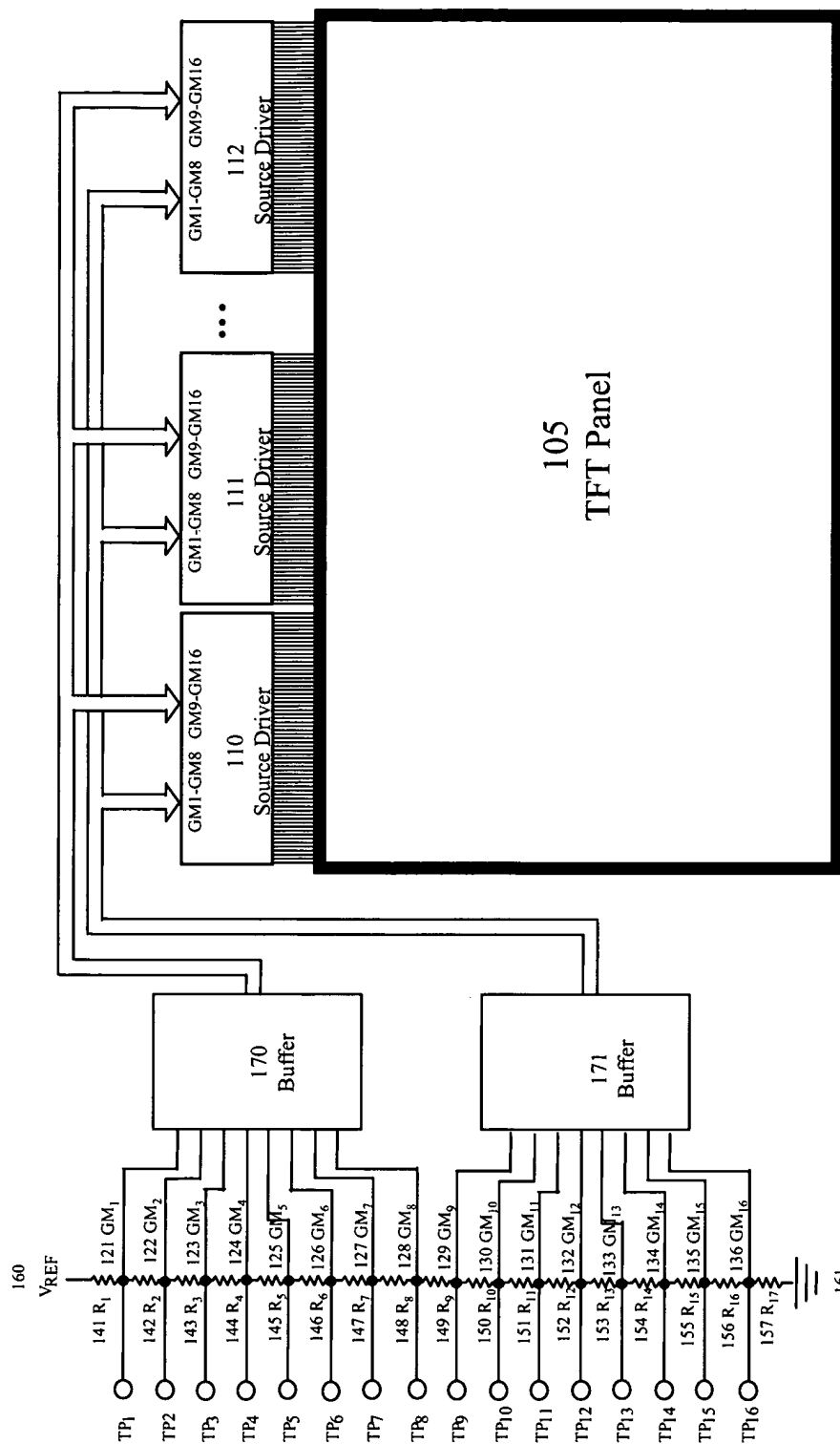
21. The integrated circuit of claim 17 wherein said reprogrammable, non-volatile storage cells are organized into one or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and
15 means to switch between the banks based on one or more external signals is provided on said integrated circuit.

22. The integrated circuit of claim 21 wherein said means to switch between

banks can have a switching time from about 10 msec to about one second.

ABSTRACT

A programmable buffer integrated circuit which can be programmed to output a set of gamma correction reference voltages to be used in LCD displays. Once programmed, the buffers will continuously output the programmed value. The device incorporates a programming interface to allow the programming of the buffer outputs to the desired values during manufacturing and test of the panel. Multiple sets of values can be programmed to provide different gamma correction curves for different user or application requirements.



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FIG. 1

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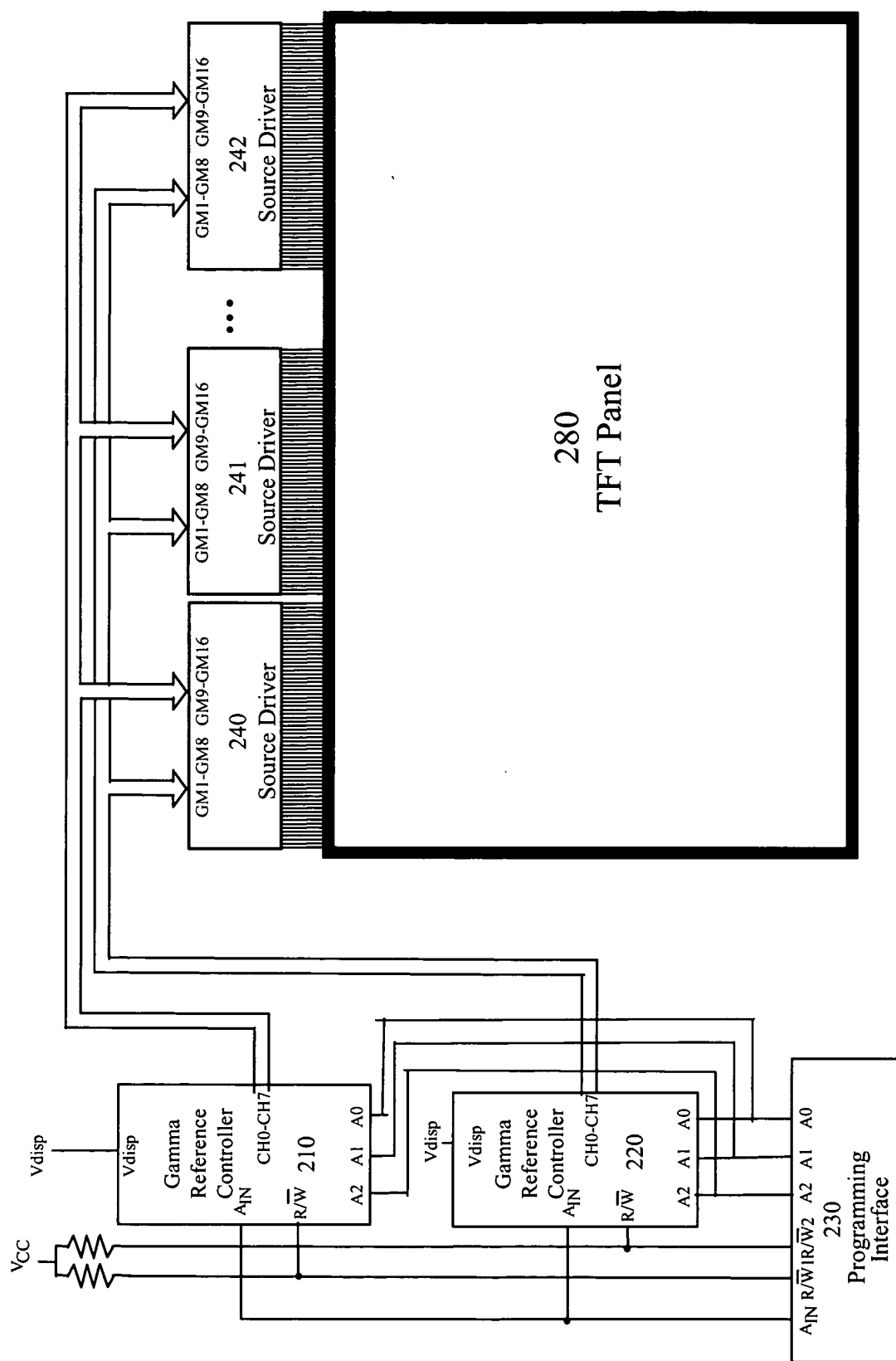
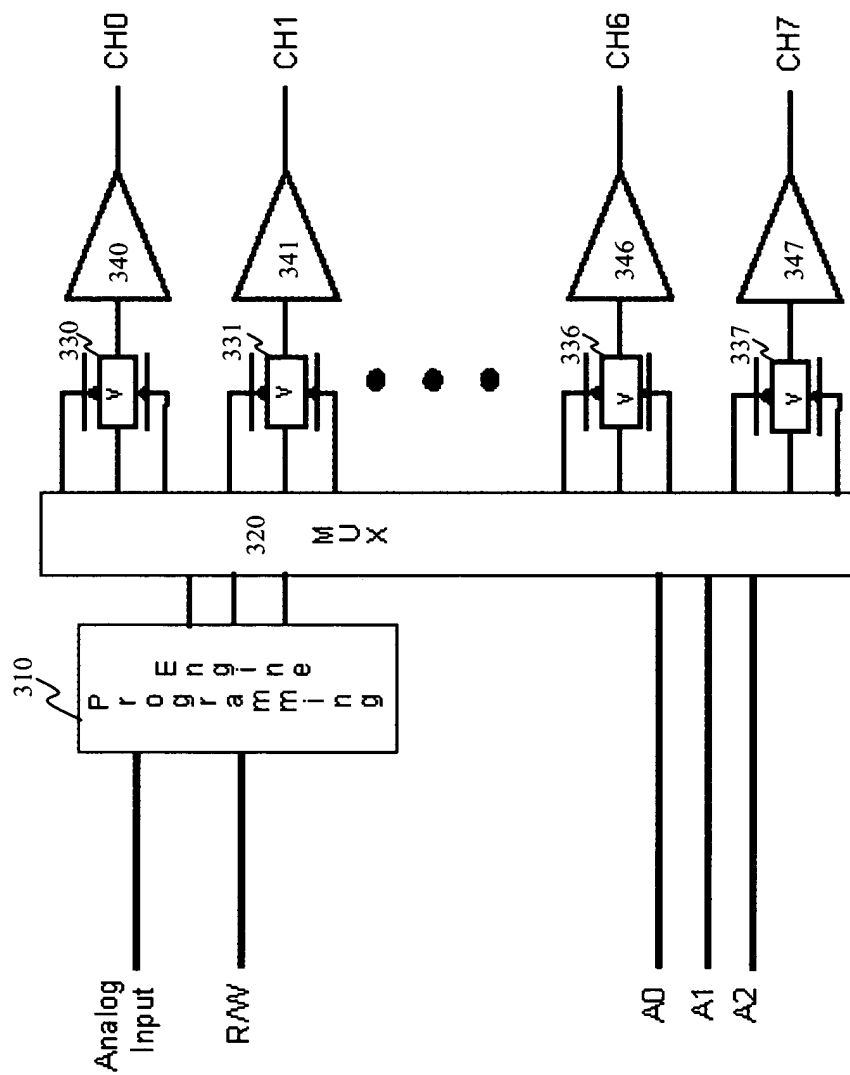


FIG. 2

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FIG. 3

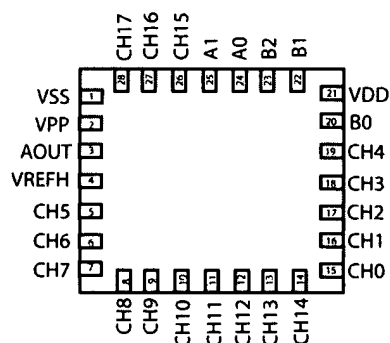
FIG. 4A

PIN DESCRIPTIONS

Name	Description	Value Range	Function
VDD	Digital Supply Input	3V to 3.3V	
CH0-CH17	Analog Outputs	0V –VREF-0.2	Analog Output Voltage Channels
B0-B2	Bank Select	CMOS Inputs	Selects which output is placed in tracking mode or is written to during a write operation
VREFH	Output High Level Reference	5-13.5 Volts	Sets the highest voltage for the output channels.
A _{OUT}	Analog Output	0.2V-VREFH-0.2	Outputs the current value of the selected channel of the selected bank during programming
V _{PP}	Programming Voltage	10-14Volts	Provides the programming voltage and timings needed to program the analog memory cells. Also used to enter operating modes other than read.
A0-A1	Address Inputs	TTL	Used to Select Programming Modes and Locations to be written

FIG. 4B

Pinout



AG1818

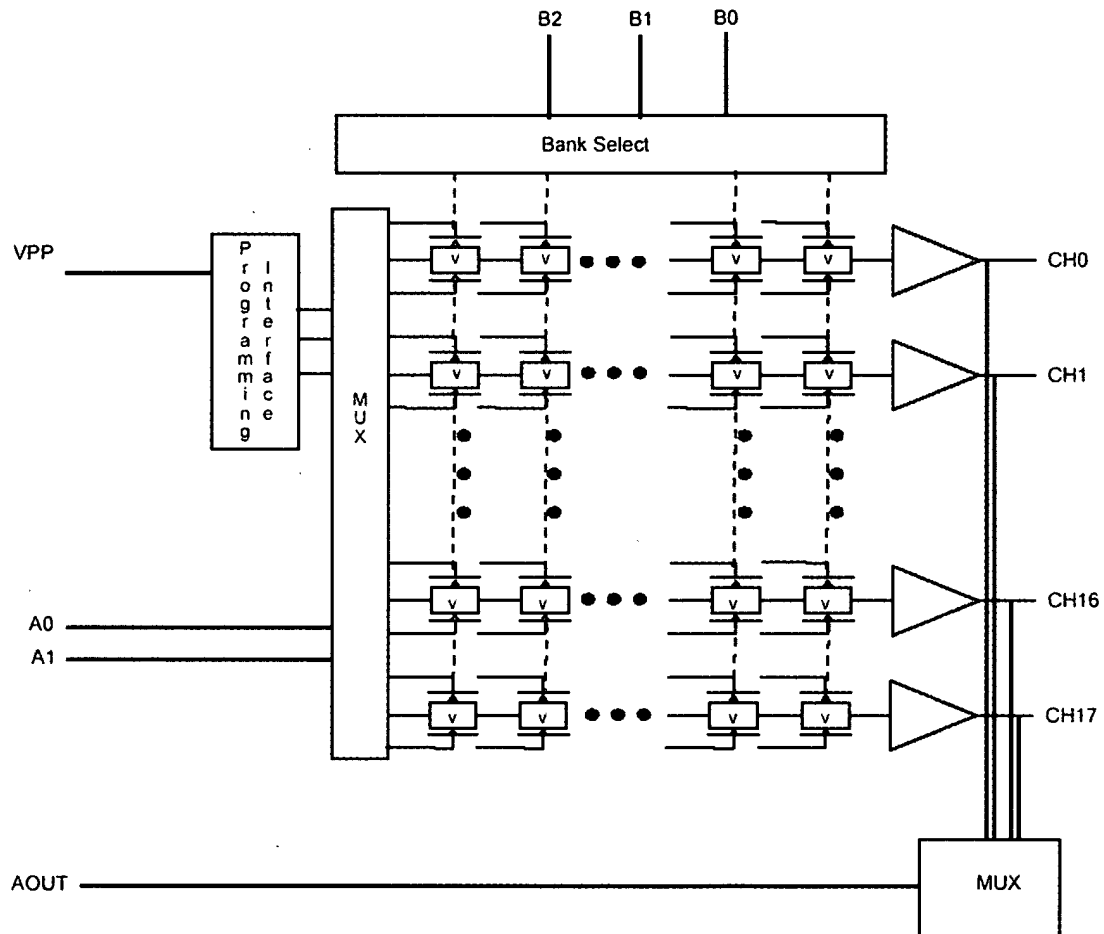
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FIG. 5**ELECTRICAL PARAMETERS**

Symbol	Parameter		Min	Typ	Max	Units	Condition
V_{IL}	Input Low Voltage	A0-A2			V _{DD} x 0.3	V	
V_{IH}	Input High Voltage	A0-A2	V _{DD} x 0.7			V	
V_{OLA}	Output Low Voltage	AOUT, CH0- CH17	0.2			V	I _{OL} = 10mA
V_{OHA}	Output High Voltage	AOUT, CH0- CH17			V _{REFH} - 0.2	V	I _{OH} = - 10mA
I_{IL}	Input Leakage Current				±1.0	µA	
I_{DD}	V _{DD} Current (Operating)				1.5	mA	R _{EXT} = ∞
I_{SB}	V _{DD} Current (Standby)				10	µA	
I_{VREFH}	VREF Current				190	mA	
V_{PP}	VPP Range		10		14	V	
V_{AC}	Accuracy		15			mV	
V_{drift}	Output Drift				70	µV	10 Years at 125 Deg C
PSRR	Power Supply Rejection Ratio		45	60		DB	VDD = 3.3-5.5V
T_{damp}	Bank Switch Damp Time		10			msec	

FIG. 6

BLOCK DIAGRAM (AG1818)



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DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, postal address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original first and joint inventor (if multiple names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

GAMMA REFERENCE VOLTAGE GENERATOR

the specification of which is attached hereto unless the following information is indicated:

_____ was filed on _____;
 as United States Application Number or PCT International Application Number _____;
 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendments referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified, as so indicated below, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)	Priority Claimed
_____	_____ Yes _____ No
(Application No.) (Country)	(Month/Day/Year Filed)

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

<u>60/477,680</u>	<u>06/11/2003</u>
(Application No.)	(Month/Day/Year Filed)

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. 1.56 that became available between the filing date of the prior application and the national or PCT International filing date of this application.

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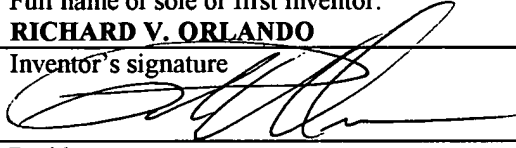
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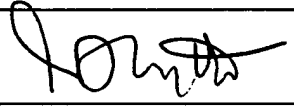
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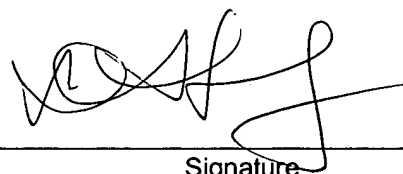
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REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)	First Named Inventor	ORLANDO, et al.
	Title	Gamma Reference Voltage Generator
	Atty Docket Number	ALTA-P007

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

12/23/03

Date



Signature

Dennis S. Fernandez, ESQ. Reg. No. 34,160
Typed or printed name

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Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

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Application Data Sheet

Application Information

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Application Type::	Regular
Subject Matter::	Utility
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Title::	Gamma Reference Voltage Generator
Attorney Docket Number::	ALTA-P007
Request for Early Publication?::	No
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Suggested Drawing Figures::	7
Total Drawing Sheets::	6
Small Entity::	Yes
Petition included?::	No
Secrecy Order in Parent Appl.?::	No

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): **ORLANDO, et al.**

Docket No.: **ALTA-P007**

Serial No.: (Not yet assigned)

Group Art Unit: (Not yet assigned)

Filed: 12/23/2003

Examiner: (Not yet assigned)

Title: **Gamma Reference Voltage Generator**

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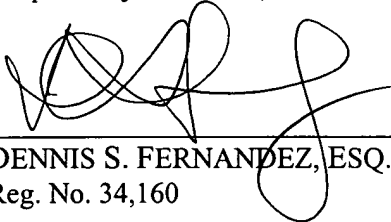
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Applicant respectfully submits that Applicants' claimed invention is patentable over such references. Forms PTO/SB/08A and PTO/SB/08B listing these references are attached. It is understood the Office may find additionally relevant material in these or other references

Respectfully submitted,


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Reg. No. 34,160

12/23/03

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Application Number	Not yet assigned
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Filing Date	12/23/2003
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First Named Inventor	Orlando, et al.
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Art Unit	Not yet assigned
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Examiner Name	Not yet assigned
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Attorney Docket Number	ALTA-P007
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ALTA-P007

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Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

**MULTIPLE DEPENDENT CLAIM
FEE CALCULATION SHEET**

SERIAL NO. 10746337

FILED DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1ST AMENDMENT		AFTER 2ND AMENDMENT	
	IND	DEP	IND	DEP	IND	DEP
1						
2						
3						
4						
5						
6						
7						
8	1					
9		1				
10	1					
11	1					
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50						
TOTAL IND.	7					
TOTAL DEP.						
TOTAL CLAIMS	27					

51						
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100						
TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2003

Application or Docket Number

427,1-2007

CLAIMS AS FILED - PART I

(Column 1)

(Column 2)

TOTAL CLAIMS	22	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	22 minus 20 =	2
INDEPENDENT CLAIMS	7 minus 3 =	4
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

(Column 1)

(Column 2)

(Column 3)

AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20"

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3"

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1

SMALL ENTITY TYPE ☐

OR

OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
XS 9=	18
X43=	172
+145=	
TOTAL	575

OR

OR

OR

OR

OR

RATE	FEE
BASIC FEE	770.00
XS18=	
X86=	
-290=	
TOTAL	

SMALL ENTITY

OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL	
ADDITIONAL FEE	

OR

OR

OR

OR

OR

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL	
ADDITIONAL FEE	

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL	
ADDITIONAL FEE	

OR

OR

OR

OR

OR

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL	
ADDITIONAL FEE	

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL	
ADDITIONAL FEE	

OR

OR

OR

OR

OR

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL	
ADDITIONAL FEE	

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

01/06/2004 WABDELRI 00000016 10746333

01 FC:2001	385.00	OP
02 FC:2201	172.00	OP
03 FC:2202	18.00	OP

PTO-1556
(5/87)