

Exhibit B-1

Phenix Longhorn, LLC v. Innolux Corporation
Civil Action No. 2:23-cv-00478-RWS-RSP
E.D. Tex.

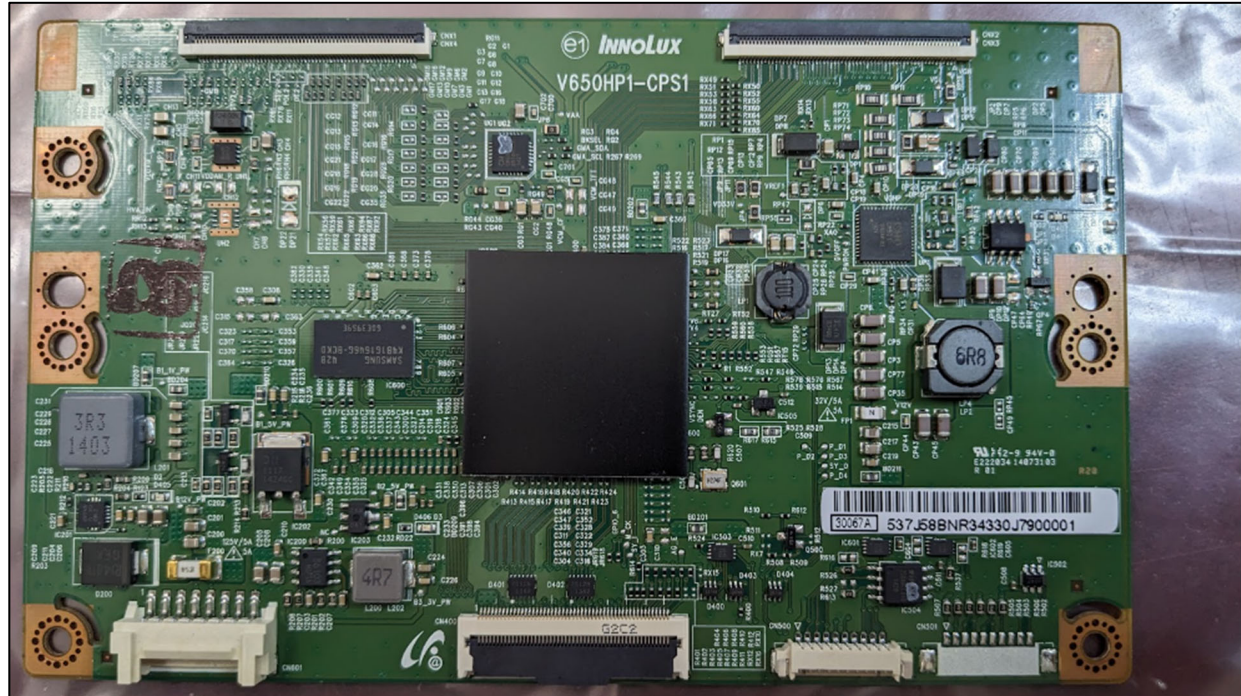
U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
1[pre]: An integrated circuit for producing voltage signals on a plurality of outputs comprising:	The Accused Instrumentalities comprise “[a]n integrated circuit for producing voltage signals on a plurality of outputs.” For example, certain Accused Instrumentalities incorporate one of the CM602 and/or CM603 (collectively, the “Accused Innolux Chips”) programmable gamma integrated circuit, or “Pgamma chip,” which each comprise “[a]n integrated circuit for producing voltage signals on a plurality of outputs,” and is attached to a timing and control (“TCON”) board. Upon information and belief, each television model identified in Exhibit A includes the functionality identified in the exemplary disclosure. Upon information and belief, Innolux and Chimei Innolux refer to the same company, and the Accused Innolux Chips are provided by various suppliers on behalf of Chimei Innolux, including Novatek, Himax and GMT.

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U.S. Patent No. 7,233,305

Exemplary Evidence of Infringement

The photos below show an image of the CM602 chip on the TCON board:



CM602 - V650HP1-CPS1 CONTROLLER BOARD PHOTO

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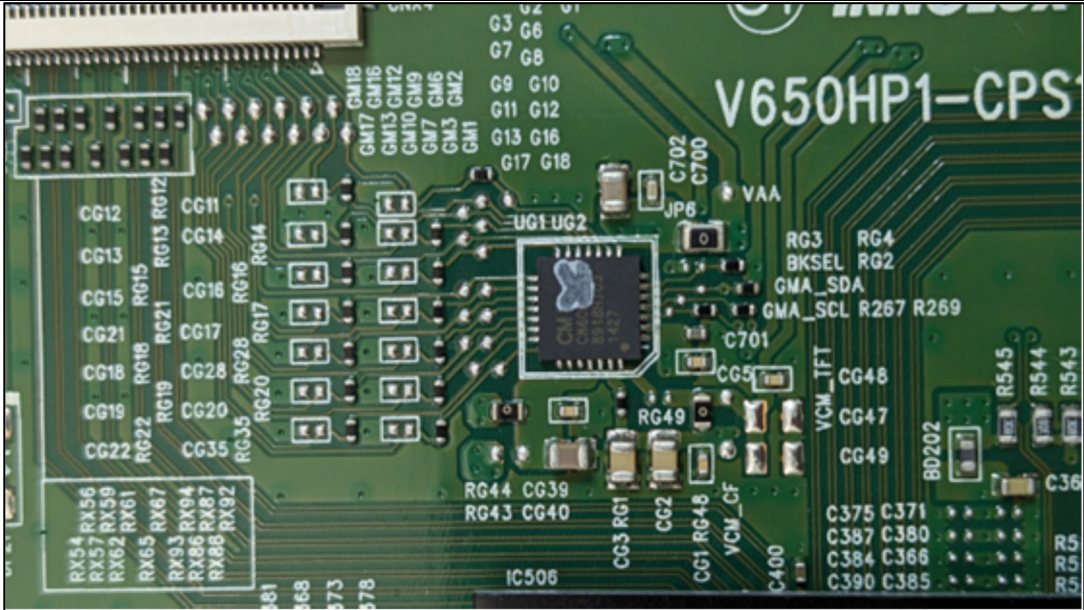
U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
	 CM602 - V650HP1-CPS1 CONTROLLER BOARD PHOTO

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U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
	 CM602 - V650HP1-CPS1 CONTROLLER BOARD PHOTO

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U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
	The photo below shows an enlarged image of the CM603 chip on the TCON board:  CM603 - PGAMMA CHIP CLOSE-UP PHOTO

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U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement																																																												
	The TCON boards each contain test points labeled with the signal names connected to plurality of outputs of the Accused Innolux Chips. Specifically, a plurality of outputs were labeled GM1-GM18 on the CM603 chip. These labels on the plurality of outputs correspond with the industry standard nomenclature for Gamma Reference voltages (<i>e.g.</i>, <1 volt to 16 volts). Preliminary testing of the Accused Innolux Chips was conducted wherein the connections of the pins on the chips were measured using a continuity meter. The results of the continuity meter measurement are summarized below: <table><tr><th colspan="3">Table A – TCON Board Test Point Label</th></tr><tr><th>Pin #</th><th>CM602</th><th>CM603</th></tr><tr><td>1</td><td>V2 through Resistor</td><td>VSS</td></tr><tr><td>2</td><td>VDD</td><td>VDD</td></tr><tr><td>3</td><td>GMA_SCL</td><td>GMA_SCL</td></tr><tr><td>4</td><td>GMA_SDA</td><td>GMA_SDA</td></tr><tr><td>5</td><td>BKSEL</td><td>BKSEL</td></tr><tr><td>6</td><td></td><td>VSS</td></tr><tr><td>7</td><td></td><td>VSS</td></tr><tr><td>8</td><td>AVDD</td><td>AVDD</td></tr><tr><td>9</td><td>GM1 Through Resistor</td><td>GM1 Through Resistor RG11</td></tr><tr><td>10</td><td>GM2 Through Resistor</td><td>GM3 Through Resistor RG12</td></tr><tr><td>11</td><td>GM3 Through Resistor</td><td>GM6 Through Resistor RG13</td></tr><tr><td>12</td><td>GM6 Through Resistor</td><td>GM7 Through Resistor RG14</td></tr><tr><td>13</td><td>GM7 Through Resistor</td><td>GM8 Through Resistor RG15</td></tr><tr><td>14</td><td></td><td>GM9 Through Resistor RG16</td></tr><tr><td>15</td><td>GM9 Through Resistor</td><td></td></tr><tr><td>16</td><td>GM10 Through Resistor</td><td></td></tr><tr><td>17</td><td>GM12 Through Resistor</td><td>GM10 Through Resistor RG17</td></tr><tr><td>18</td><td></td><td>GM11 Through Resistor RG18</td></tr></table>	Table A – TCON Board Test Point Label			Pin #	CM602	CM603	1	V2 through Resistor	VSS	2	VDD	VDD	3	GMA_SCL	GMA_SCL	4	GMA_SDA	GMA_SDA	5	BKSEL	BKSEL	6		VSS	7		VSS	8	AVDD	AVDD	9	GM1 Through Resistor	GM1 Through Resistor RG11	10	GM2 Through Resistor	GM3 Through Resistor RG12	11	GM3 Through Resistor	GM6 Through Resistor RG13	12	GM6 Through Resistor	GM7 Through Resistor RG14	13	GM7 Through Resistor	GM8 Through Resistor RG15	14		GM9 Through Resistor RG16	15	GM9 Through Resistor		16	GM10 Through Resistor		17	GM12 Through Resistor	GM10 Through Resistor RG17	18		GM11 Through Resistor RG18
Table A – TCON Board Test Point Label																																																													
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3	GMA_SCL	GMA_SCL																																																											
4	GMA_SDA	GMA_SDA																																																											
5	BKSEL	BKSEL																																																											
6		VSS																																																											
7		VSS																																																											
8	AVDD	AVDD																																																											
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		19	GM13 Through Resistor	GM12 Through Resistor RG19																																																							
		20	GM16 Through Resistor	GM13 Through Resistor RG20																																																							
		21	GM17 Through Resistor	GM16 Through Resistor RG21																																																							
		22	GM18 Through Resistor	GM18 Through Resistor RG22																																																							
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	Pins 9-14 and 17-22 demonstrate “voltage signals on a plurality of outputs” in the CM603 chip. The table below lists the voltages at each output for BKSEL = 0 and for BKSEL = 1 (3.3V). <table><tr><th colspan="4">Table B.1 – CM602 Chip</th></tr><tr><th>Pin</th><th>GM</th><th>Bank 0 Voltage</th><th>Bank 1 Voltage</th></tr><tr><td>9</td><td>1</td><td>16.57</td><td>16.05</td></tr><tr><td>10</td><td>2</td><td>14.09</td><td>12.86</td></tr><tr><td>11</td><td>3</td><td>13.50</td><td>12.38</td></tr><tr><td>12</td><td>6</td><td>11.65</td><td>11.35</td></tr><tr><td>13</td><td>7</td><td>11.31</td><td>10.45</td></tr><tr><td>15</td><td>9</td><td>9.58</td><td>9.27</td></tr><tr><td>16</td><td>10</td><td>8.05</td><td>8.36</td></tr><tr><td>17</td><td>12</td><td>6.32</td><td>7.17</td></tr><tr><td>19</td><td>13</td><td>5.85</td><td>6.28</td></tr><tr><td>20</td><td>16</td><td>3.80</td><td>4.96</td></tr><tr><td>21</td><td>17</td><td>3.10</td><td>4.38</td></tr><tr><td>22</td><td>18</td><td>0.41</td><td>0.96</td></tr></table>				Table B.1 – CM602 Chip				Pin	GM	Bank 0 Voltage	Bank 1 Voltage	9	1	16.57	16.05	10	2	14.09	12.86	11	3	13.50	12.38	12	6	11.65	11.35	13	7	11.31	10.45	15	9	9.58	9.27	16	10	8.05	8.36	17	12	6.32	7.17	19	13	5.85	6.28	20	16	3.80	4.96	21	17	3.10	4.38	22	18	0.41
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U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement				
		Table B.2 – CM603 Chip			
		Pin	GM	Bank 0 Voltage	Bank 1 Voltage
		9	1	15.56	8.51
		10	3	13.07	8.51
		11	6	11.22	8.51
		12	7	10.91	8.51
		13	8	9.45	8.51
		14	9	9.16	8.51
		17	10	7.63	8.51
		18	11	7.32	8.51
		19	12	5.90	8.51
		20	13	5.38	8.51
		21	16	3.23	8.51
		22	18	0.41	8.51
		Voltage readings were taken with a Tektronix Digital Multi Meter (DMM) and the first few readings are provided below. Readings were rounded to the nearest 1/100 th of a volt.			
In addition to Phenix’s general reservation of the right to supplement, Phenix reserves the right to amend its contentions with respect to this limitation to include or reference nonpublic information about the asserted infringement that was not discovered or located, despite diligent efforts, before the service of these infringement claim charts.					

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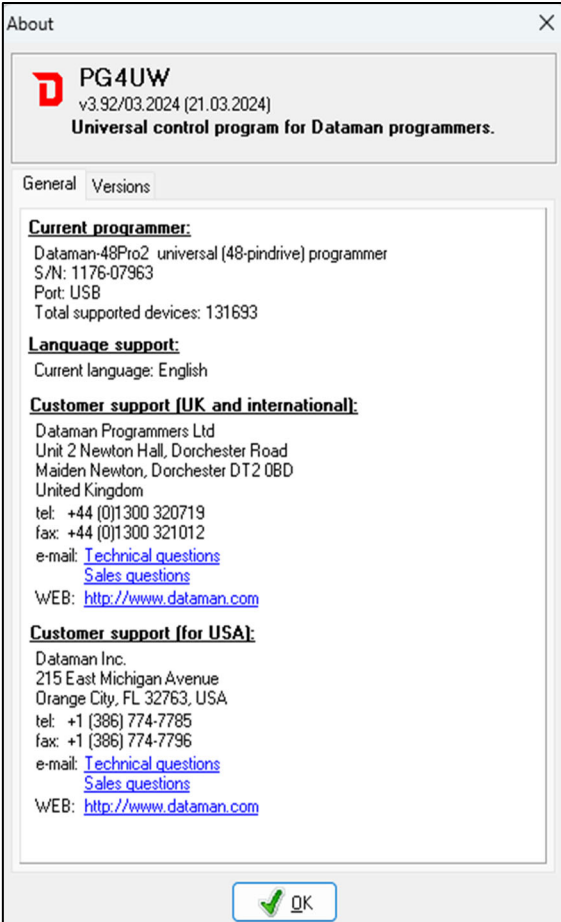
U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
1[a]: a plurality of non-volatile storage cells;	The CM603 chip meets the “a plurality of non-volatile storage cells” element of claim limitation 1[a]. Preliminary testing used a programmer from Dataman to read and write the Accused Innolux Chips’ memory. The Dataman programmer utilized the following software: 

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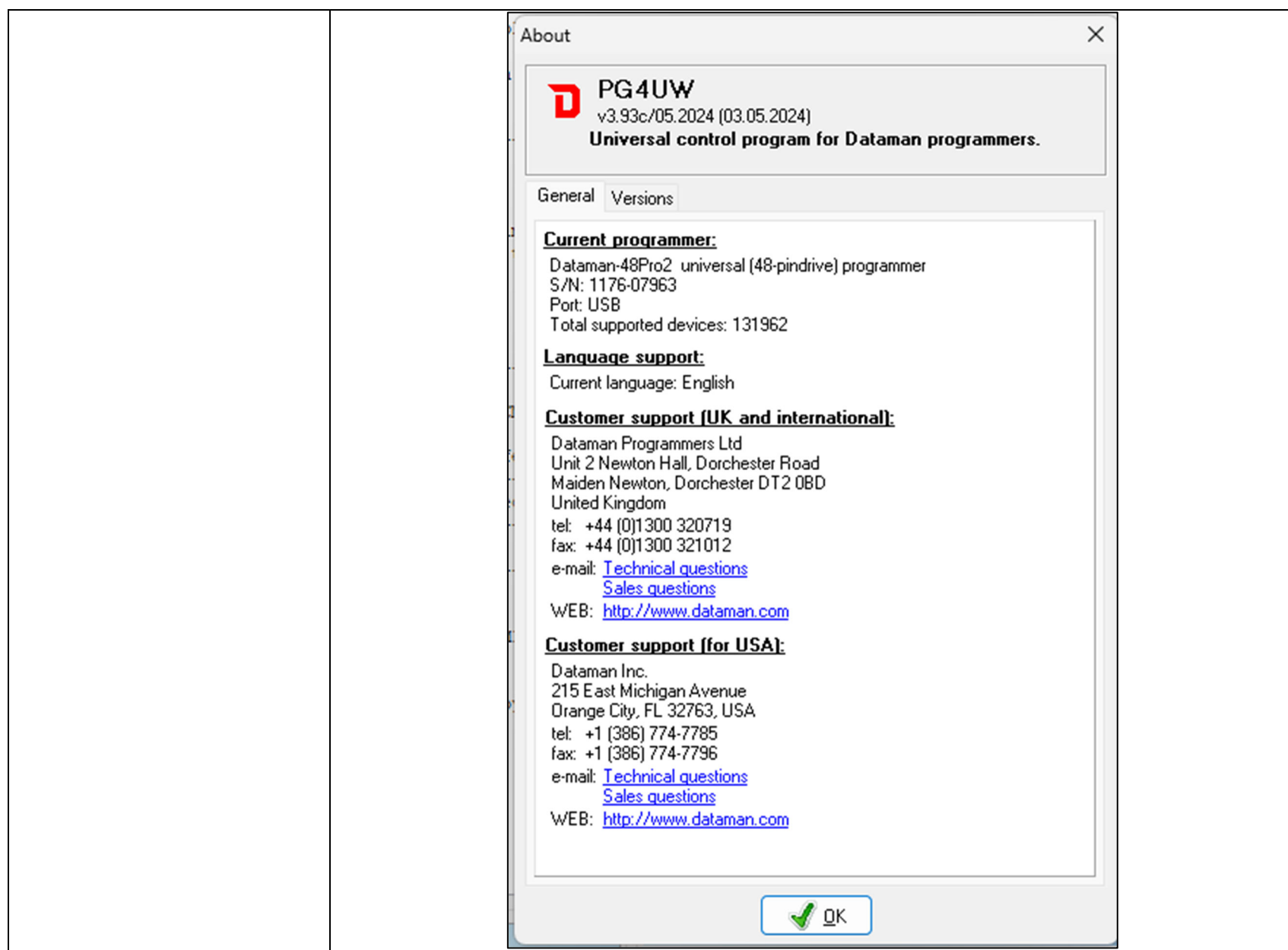


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	The Dataman software supports programming by chip with an adapter or in circuit (ISP) using I2C interface pins. The Dataman software also allows for the selection of the CM602 and CM603 chip as shown below: Select device AllOnly selected typeOnly selected manufacturer <table><thead><tr><th>Manufacturer</th><th>Name</th><th>Adapter/module or note</th><th>Relevance</th></tr></thead><tbody><tr><td>CMI</td><td>CM602 [wQFN28]</td><td>DIL28/QFN28-1 ZIF-CS (id)</td><td>cm602</td></tr><tr><td>Richtek</td><td>CM602 [wQFN28]</td><td>DIL28/QFN28-1 ZIF-CS (id)</td><td>cm602</td></tr></tbody></table> Search suggestions cm602 gives 5 more results cm6 gives 20 more results m60 gives 25 more results 602 gives 144 more results Search: cm602 History Options ☐ Use search pattern exactly as typed (Alt+E) 2 found ☒ Tolerant search and "x" characters replacement (Alt+T) 2 found	Manufacturer	Name	Adapter/module or note	Relevance	CMI	CM602 [wQFN28]	DIL28/QFN28-1 ZIF-CS (id)	cm602	Richtek	CM602 [wQFN28]	DIL28/QFN28-1 ZIF-CS (id)	cm602
Manufacturer	Name	Adapter/module or note	Relevance										
CMI	CM602 [wQFN28]	DIL28/QFN28-1 ZIF-CS (id)	cm602										
Richtek	CM602 [wQFN28]	DIL28/QFN28-1 ZIF-CS (id)	cm602										

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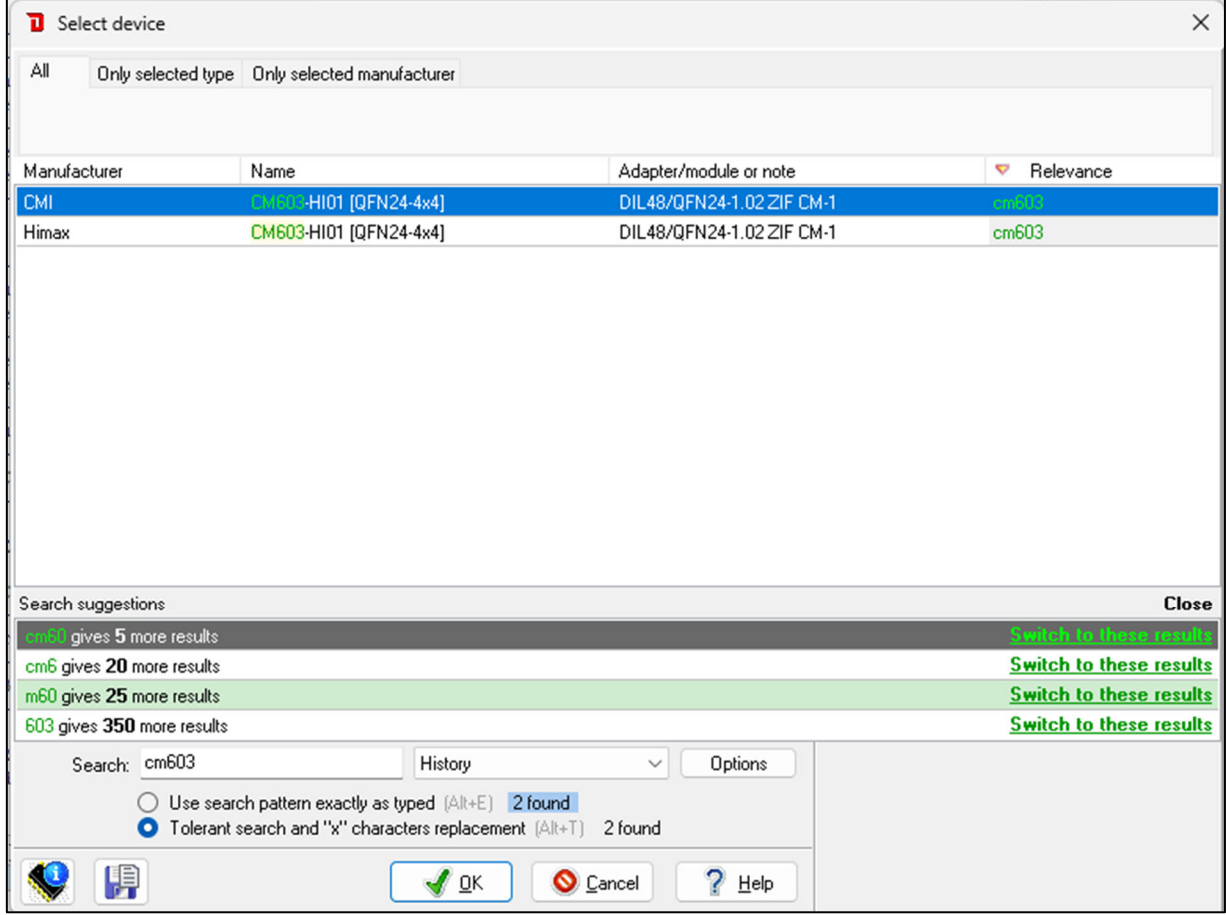
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	 After selecting the CM602 and CM603 chips from its pull-down menus, the Dataman software provided the following information for the Accused Innolux Chips:

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	Device info: Manufacturer: CMI Partname: CM602 [WQFN28] 8-bit bytes: 70h (112 Bytes) Organization: 38h (x16 bit) Algorithm: IIC standard (Byte) Implemented in SW ver. (summary): 3.88 Modified in SW ver. (summary): not modified Implemented in SW ver. (Dataman-48Pro2): 3.88 Modified in SW ver. (Dataman-48Pro2): not modified Package Info: WQFN(28), 5x5x0.8mm Device info: Manufacturer: CMI Partname: CM603-HI01 [QFN24-4x4] 8-bit bytes: 80h (128 Bytes) Organization: 40h (x16 bit) Algorithm: IIC standard (Byte) Implemented in SW ver. (summary): 3.93a Modified in SW ver. (summary): 3.94a Implemented in SW ver. (Dataman-48Pro2): 3.93a Modified in SW ver. (Dataman-48Pro2): 3.94a Package Info: QFN(24), 4x4x0.9mm This chip is based on the EEPROM technology, therefore it can be reprogrammed each byte without previous erase procedure. The erase operation is not available or not necessary (and therefore not supported by our programmers). The blank check operation is also not supported, because erase operation (therefore "erased chip" situation) is not available. Demonstrating evidence of non-volatile (EEPROM) memory, arranged as 40 hex (64 decimal) 16 bit words. Furthermore, the following memory map was provided:

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U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement																																																																																				
	CM602: General Info: Description of registers: <table><tr><th>Registers</th><th>Address range</th><th>Buffer location</th><th>Access options</th></tr><tr><td>GMA1BK1 - GMA16BK1</td><td>00h - 0Fh</td><td>00h - 0Fh</td><td>Read and Write</td></tr><tr><td>CMI01 - CMI02</td><td>10h - 11h</td><td>10h - 11h</td><td>Read and Write</td></tr><tr><td>VCOM1BK1</td><td>12h</td><td>12h</td><td>Read and Write</td></tr><tr><td>VCOM1MINBK1</td><td>18h</td><td>18h</td><td>Read and Write</td></tr><tr><td>VCOM1MAXBK1</td><td>19h</td><td>19h</td><td>Read and Write</td></tr><tr><td>CMI03</td><td>1Ah</td><td>1Ah</td><td>Read and Write</td></tr><tr><td>VCOM2BK1</td><td>1Bh</td><td>1Bh</td><td>Read and Write</td></tr><tr><td>VCOM2MINBK1</td><td>1Ch</td><td>1Ch</td><td>Read and Write</td></tr><tr><td>VCOM2MAXBK1</td><td>1Dh</td><td>1Dh</td><td>Read and Write</td></tr><tr><td>VREF</td><td>1Fh</td><td>1Fh</td><td>Read and Write</td></tr><tr><td>GMA1BK2 - GMA16BK2</td><td>20h - 2Fh</td><td>20h - 2Fh</td><td>Read and Write</td></tr><tr><td>VCOM1BK2</td><td>30h</td><td>30h</td><td>Read and Write</td></tr><tr><td>VCOM1MINBK2</td><td>31h</td><td>31h</td><td>Read and Write</td></tr><tr><td>VCOM1MAXBK2</td><td>32h</td><td>32h</td><td>Read and Write</td></tr><tr><td>VCOM2BK2</td><td>33h</td><td>33h</td><td>Read and Write</td></tr><tr><td>VCOM2MINBK2</td><td>34h</td><td>34h</td><td>Read and Write</td></tr><tr><td>VCOM2MAXBK2</td><td>35h</td><td>35h</td><td>Read and Write</td></tr><tr><td>CMI04</td><td>36h</td><td>36h</td><td>Read and Write</td></tr><tr><td>MOTP Remain Time</td><td>37h</td><td>37h</td><td>Read</td></tr><tr><td>Other locations</td><td>-</td><td>-</td><td>Reserved</td></tr></table>	Registers	Address range	Buffer location	Access options	GMA1BK1 - GMA16BK1	00h - 0Fh	00h - 0Fh	Read and Write	CMI01 - CMI02	10h - 11h	10h - 11h	Read and Write	VCOM1BK1	12h	12h	Read and Write	VCOM1MINBK1	18h	18h	Read and Write	VCOM1MAXBK1	19h	19h	Read and Write	CMI03	1Ah	1Ah	Read and Write	VCOM2BK1	1Bh	1Bh	Read and Write	VCOM2MINBK1	1Ch	1Ch	Read and Write	VCOM2MAXBK1	1Dh	1Dh	Read and Write	VREF	1Fh	1Fh	Read and Write	GMA1BK2 - GMA16BK2	20h - 2Fh	20h - 2Fh	Read and Write	VCOM1BK2	30h	30h	Read and Write	VCOM1MINBK2	31h	31h	Read and Write	VCOM1MAXBK2	32h	32h	Read and Write	VCOM2BK2	33h	33h	Read and Write	VCOM2MINBK2	34h	34h	Read and Write	VCOM2MAXBK2	35h	35h	Read and Write	CMI04	36h	36h	Read and Write	MOTP Remain Time	37h	37h	Read	Other locations	-	-	Reserved
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CM603:

Buffer location	Data	NVM	Register
00h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	-	Soft WP1
01h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	-	Soft WP2
02h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	GMA1BK1
03h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	GMA2BK1
...	...	x	...
0Dh	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	GMA12BK1
10h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	CMI01
11h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	CMI02
12h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	VCOMBK1
18h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	VCOMMINBK1
19h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	VCOMMAXBK1
1Ah	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	CMI03
1Fh	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	VREF
20h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	GMA1BK2
21h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	GMA2BK2
...	...	x	...
2Bh	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	GMA12BK2
30h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	VCOMBK2
31h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	VCOMMINBK2
32h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	VCOMMAXBK2
36h	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	CMI04
...	...	x	...
3Dh	b9 b8 b7 b6 b5 b4 b3 b2 b1 b0	x	CMI010
3Eh	- - - - - - - - b1 b0	x	Control reg.
3Eh	b9 - - - - - b4 b3 b2 b1 b0	-	Status reg.
Other locations	---	-	Reserved

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	For the CM602 Chip, The memory map shows that data is organized as 16 bit words. The first 16 words at address 0 to F (hex) are for Bank 0, and the 16 words at address 20 to 2F (hex) are for Bank 1. For the CM603 Chip, the above memory map shows that locations 02 hex through 0D hex are used for the first Bank of Gamma voltages GMA1BK1 to GMA12BK1, and locations 20 hex through 2B hex are used for the second Bank of Gamma voltages namely GMA1BK2 to GMA12BK2. Dataman software refers to the locations as 1 to 12, but those 12 test points are actually labelled on the board's silkscreen as GM1, 3, 6, 7, 8, 9, 10, 11, 12, 13, 16, and 18. Moreover, the non-volatile memory of the Accused Innolux Chips was demonstrated using the Dataman-40Pro2 programmer, as detailed below. Demonstration of the correlation between the stored EEPROM values and the Gamma voltages was demonstrated by conducting a test of the Accused Innolux Chips. The Accused Innolux Chips were removed from the TCON boards: For example, the Image below shows the CM602 Chip removed from the TCON board.

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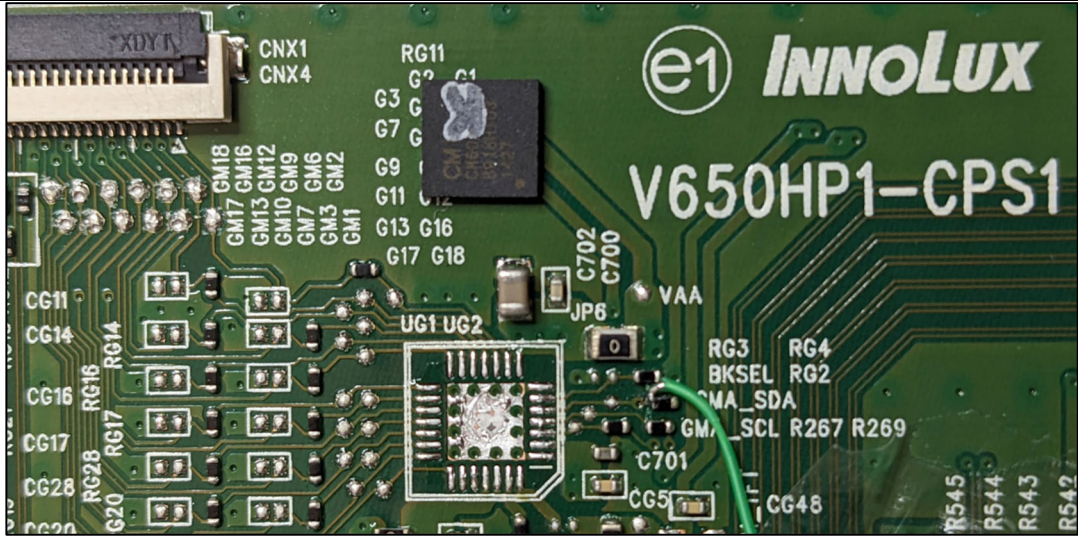
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	 PHOTO OF CM602 DESOLDERED FROM BOARD The Accused Innolux Chips were then placed in a then placed in an adapter in the Dataman-48Pro2 programmer shown below:

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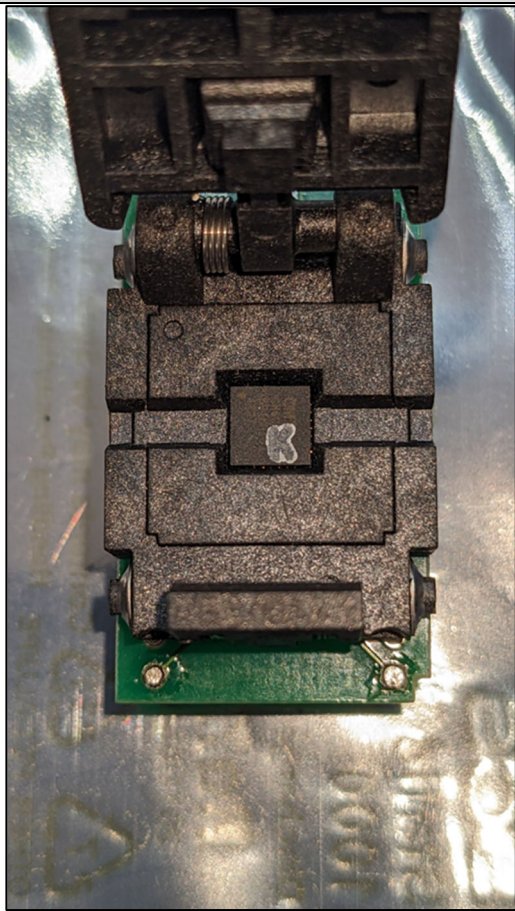
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	 PHOTO OF CM602 PLACED IN PROGRAMMING ADAPTER

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U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
	 PHOTO OF CM602 AND ADAPTER IN DATAMAN PROGRAMMER Using the programmer's software, the contents of the Accused Innolux Chips were read as follows:

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The screenshot shows a 'View/Edit Buffer' window with the following details:

- Title Bar:** View/Edit Buffer
- Buffer size:** 8,192.0 kWords
- Current address:** 000000003F
- hMode:** View (selected), Edit
- Bit Mode:** 8 bit, 16 bit (selected)
- Toolbar:** Includes icons for file operations (open, save, print), editing (copy, paste, undo, redo), and viewing (hex, ASCII, binary).
- Main Display:** A table with columns for Address-hex, hex values, and ASCII values. The address range is 00000000 to 0000006F. The hex values are mostly FFFF, with some non-FFFF values at the beginning (e.g., 03E7, 0352, 032E, 02BE, 02AA, 0253, 0241, 01E6). The ASCII values are mostly dots, with some non-dot values at the beginning (e.g., .Ç, .R, ., .%, .a, .S, .A, .æ).
- Highlight Legend:**
 - ☒ Enabled
 - Recently modified by multi operation (FILL, ERASE)
 - Recently modified by Byte/Word direct edit
 - Older modified by multi operation
 - Older modified by Byte/Word direct edit
- Buttons:** Clear

Exhibit B-1

U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
	efforts, before the service of these infringement claim charts.
1[b]: circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs;	Upon information and belief, the Accused Innolux Chips meet the “circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs” element of claim limitation 1[b]. Interface to the memory locations is accomplished through the I²C serial interface, which consists of a serial data line (SDA or GSDA) and a serial clock line (SCL). Address information is sent to the device in a bit serial fashion, and the data is either read or written in the same bit serial manner. In order to program the storage cells, upon information and belief, a write command is sent to the device by changing the value in the location on the screen. An annotated version of the integrated circuit is provided below, annotated to show certain “circuits for programming.”

Exhibit B-1

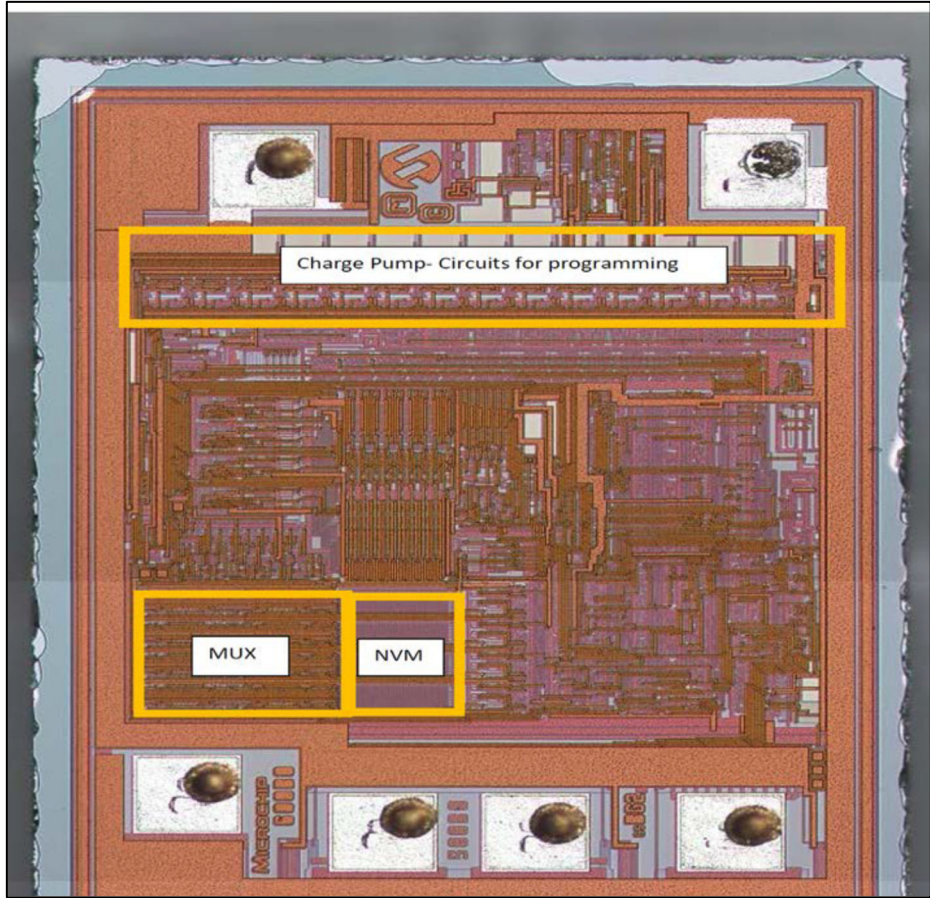
U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
	 CM602 ANNOTATED CHIP DIAGRAM Additional evidence of “circuits for programming” and “multiplexer” in the Accused Innolux Chips will be obtained during discovery of data sheets, schematics, and VHDL code from Innolux.

Exhibit B-1

U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
	In addition to Phenix’s general reservation of the right to supplement, Phenix reserves the right to amend its contentions with respect to this limitation to include or reference nonpublic information about the asserted infringement that was not discovered or located, despite diligent efforts, before the service of these infringement claim charts.
1[c]: drivers connected to said storage cells and to the plurality of outputs; and	Upon information and belief, the Accused Innolux Chips meet the “drivers connected to said storage cells and to the plurality of outputs” element of claim limitation 1[c]. Changes to the storage cells are reflected in the outputs. The drivers are present, as evidenced by the fact that high current and high voltages are required at the output pins for connecting to the source driver inputs. Evidence of “drivers connected to said storage cells and to the plurality of outputs” in the Accused Innolux Chips will be obtained during discovery of data sheets, schematics, and VHDL code from Innolux. In addition to Phenix’s general reservation of the right to supplement, Phenix reserves the right to amend its contentions with respect to this limitation to include or reference nonpublic information about the asserted infringement that was not discovered or located, despite diligent efforts, before the service of these infringement claim charts.

Exhibit B-1

U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
1[d]: wherein said voltage signals are gamma reference voltage signals for determining actual driving voltages of columns of a display	The Accused Innolux Chips meet the “voltage signals [that] are gamma reference voltage signals for determining actual driving voltages of columns of a display” element of claim limitation 1[d]. As described above, the I²C interface includes bits to select which storage cells are being addressed. These address bits are used internally in the device to drive the multiplexer, which then selects the correct storage cells based on said address. The outputs of the Accused Innolux Chips are connected to the GM1-GM18 test points, which are the industry standard nomenclature for gamma reference voltages. These outputs are further connected to the column drivers of the display to set the voltage driven on the columns of the display based on the digital data. In addition to Phenix’s general reservation of the right to supplement, Phenix reserves the right to amend its contentions with respect to this limitation to include or reference nonpublic information about the asserted infringement that was not discovered or located, despite diligent efforts, before the service of these infringement claim charts.
1[e]: wherein said non-volatile storage cells are organized into two or more banks of cells	The Accused Innolux Chips meet the “non-volatile storage cells [that] are organized into two or more banks of cells” element of claim limitation 1[e]. Additionally, the second set of data values in the memory (20-2B hex) of the CM602 and CM603 chips are a second set of gamma voltages reference voltages. Pin 5 of the CM602 and CM603 chip selects between the two banks. A comparison of the data from the Dataman programmer with the voltage readings from the Tektronix DMM, can be seen in the tables below:

Exhibit B-1

U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement				
	Table C.1 – CM602 Chip				
	Address	GM	Bank 0 Data Hex	Bank 0 Data Dec	Bank 0 Voltage
	00	1	03E7	999	16.57
	01	2	0352	850	14.09
	02	3	032E	814	13.50
	03	6	02BE	702	11.64
	04	7	02AA	682	11.31
	05		0253		
	06	9	0241	577	9.58
	07	10	01E6	486	8.05
	08		01D4		
	09	12	017D	381	6.32
	0A	13	0160	352	5.85
	0B	16	00E4	228	3.80
	Table C.2 – CM603 Chip				
	Pin	GM	Bank 0 Data Hex	Bank 0 Data Decimal	Bank 0 Voltage
	9	GM1	3A7	935	15.56

Exhibit B-1

U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement				
	10	GM3	312	786	13.07
	11	GM6	2A3	675	11.22
	12	GM7	290	656	10.91
	13	GM8	239	569	9.45
	14	GM9	227	551	9.16
	17	GM10	1CC	460	7.63
	18	GM11	1BA	442	7.32
	19	GM12	163	355	5.90
	20	GM 13	144	324	5.38
	21	GM16	0C4	196	3.23
	22	GM18	019	25	0.41
	Table D.1 – CM602				
	Address	GM	Bank 1 Data Hex	Bank 1 Data Dec	Bank 1 Voltage
	00	1	3C7	967	16.05
	01	2	307	775	12.86
	02	3	2EA	746	12.38
	03	6	2AC	684	11.35
	04	7	276	630	10.45
	05			0	
	06	9	22E	558	9.27

Exhibit B-1

U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement					
		07	10	1F8	504	8.36
		08			0	
		09	12	1B0	432	7.17
		0A	13	17A	378	6.28
		0B	16	12A	298	4.96
		Table D.2 – CM603				
		Pin	GM	Bank 1 Data Hex	Bank 1 Data Decimal	Bank 1 Voltage
		9	GM1	200	512	8.51
		10	GM3	200	512	8.51
		11	GM6	200	512	8.51
		12	GM7	200	512	8.51
		13	GM8	200	512	8.51
		14	GM9	200	512	8.51
		17	GM10	200	512	8.51
		18	GM11	200	512	8.51
		19	GM12	200	512	8.51
		20	GM 13	200	512	8.51
		21	GM16	200	512	8.51
		22	GM18	200	512	8.51

Exhibit B-1

U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement																																																																																				
	Combining the screen shot above and the memory map, one can see that for the decimal values divided by the voltage, the following values are produced: <table><tr><th colspan="6">Table E.1 – CM602 Chip</th></tr><tr><th>Address</th><th>GM</th><th>Bank 0 Data Hex</th><th>Bank 0 Data Dec</th><th>Bank 0 Voltage</th><th>Data / Voltage</th></tr><tr><td>00</td><td>1</td><td>03E7</td><td>999</td><td>16.57</td><td>60.3</td></tr><tr><td>01</td><td>2</td><td>0352</td><td>850</td><td>14.09</td><td>60.3</td></tr><tr><td>02</td><td>3</td><td>032E</td><td>814</td><td>13.50</td><td>60.3</td></tr><tr><td>03</td><td>6</td><td>02BE</td><td>702</td><td>11.64</td><td>60.3</td></tr><tr><td>04</td><td>7</td><td>02AA</td><td>682</td><td>11.31</td><td>60.3</td></tr><tr><td>05</td><td></td><td>0253</td><td></td><td></td><td></td></tr><tr><td>06</td><td>9</td><td>0241</td><td>577</td><td>9.58</td><td>60.2</td></tr><tr><td>07</td><td>10</td><td>01E6</td><td>486</td><td>8.05</td><td>60.4</td></tr><tr><td>08</td><td></td><td>01D4</td><td></td><td></td><td></td></tr><tr><td>09</td><td>12</td><td>017D</td><td>381</td><td>6.32</td><td>60.3</td></tr><tr><td>0A</td><td>13</td><td>0160</td><td>352</td><td>5.85</td><td>60.2</td></tr><tr><td>0B</td><td>16</td><td>00E4</td><td>228</td><td>3.80</td><td>60.0</td></tr></table>	Table E.1 – CM602 Chip						Address	GM	Bank 0 Data Hex	Bank 0 Data Dec	Bank 0 Voltage	Data / Voltage	00	1	03E7	999	16.57	60.3	01	2	0352	850	14.09	60.3	02	3	032E	814	13.50	60.3	03	6	02BE	702	11.64	60.3	04	7	02AA	682	11.31	60.3	05		0253				06	9	0241	577	9.58	60.2	07	10	01E6	486	8.05	60.4	08		01D4				09	12	017D	381	6.32	60.3	0A	13	0160	352	5.85	60.2	0B	16	00E4	228	3.80	60.0
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0B	16	00E4	228	3.80	60.0																																																																																

Exhibit B-1

U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement						
		Table E.2 – CM603 Chip					
		Pin	GM	Bank 0 Data Hex	Bank 0 Data Decimal	Bank 0 Voltage	Dec Data / Voltage
		9	GM1	3A7	935	15.56	60.1
		10	GM3	312	786	13.07	60.1
		11	GM6	2A3	675	11.22	60.2
		12	GM7	290	656	10.91	60.1
		13	GM8	239	569	9.45	60.2
		14	GM9	227	551	9.16	60.2
		17	GM10	1CC	460	7.63	60.3
		18	GM11	1BA	442	7.32	60.4
		19	GM12	163	355	5.90	60.2
		20	GM 13	144	324	5.38	60.2
		21	GM16	0C4	196	3.23	60.7
		22	GM18	019	25	0.41	61.0

Exhibit B-1

U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement				
		Table F.1 – CM602 Chip			
		Address	GM	Bank 1 Data Hex	Bank 1 Data Dec
		00	1	3C7	967
		01	2	307	775
		02	3	2EA	746
		03	6	2AC	684
		04	7	276	630
		05			0
		06	9	22E	558
		07	10	1F8	504
		08			0
		09	12	1B0	432
		0A	13	17A	378
		0B	16	12A	298

Exhibit B-1

U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement						
		Table F.2 – CM603 Chip					
		Pin	GM	Bank 1 Data Hex	Bank 1 Data Decimal	Bank 1 Voltage	Dec Data / Voltage
		9	GM1	200	512	8.51	60.2
		10	GM3	200	512	8.51	60.2
		11	GM6	200	512	8.51	60.2
		12	GM7	200	512	8.51	60.2
		13	GM8	200	512	8.51	60.2
		14	GM9	200	512	8.51	60.2
		17	GM10	200	512	8.51	60.2
		18	GM11	200	512	8.51	60.2
		19	GM12	200	512	8.51	60.2
		20	GM 13	200	512	8.51	60.2
		21	GM16	200	512	8.51	60.2
		22	GM18	200	512	8.51	60.2
		As can be seen, the formula for producing output voltage from internal values is approximately Voltage = Value / 60.2.					
The Dataman programmer was used to change two values in each bank of the CM602 and CM603 chip as shown highlighted in RED below:							

Exhibit B-1

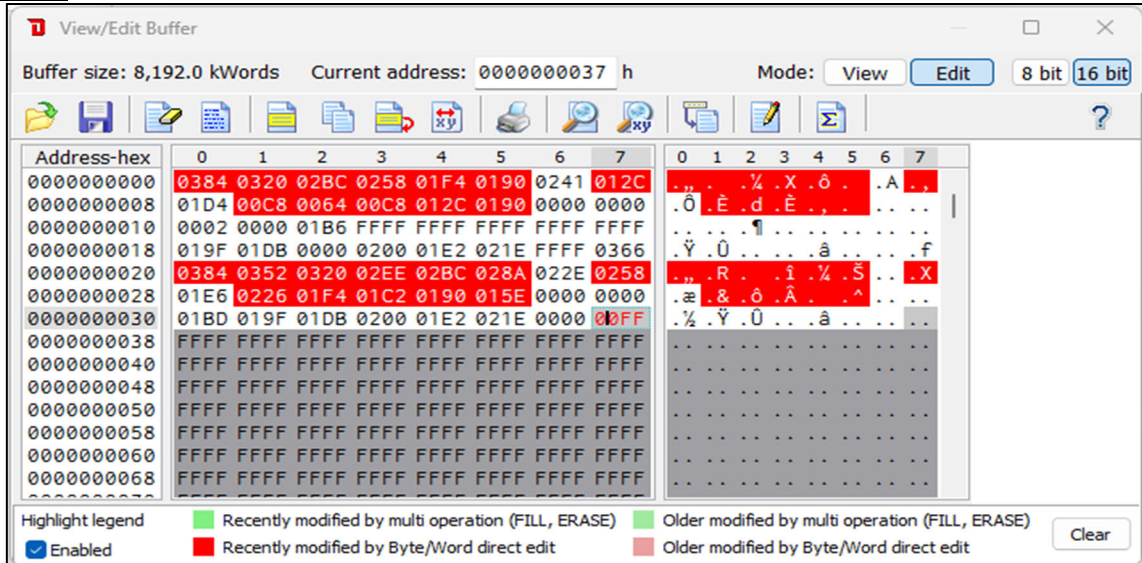
U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement
	CM602: 

Exhibit B-1

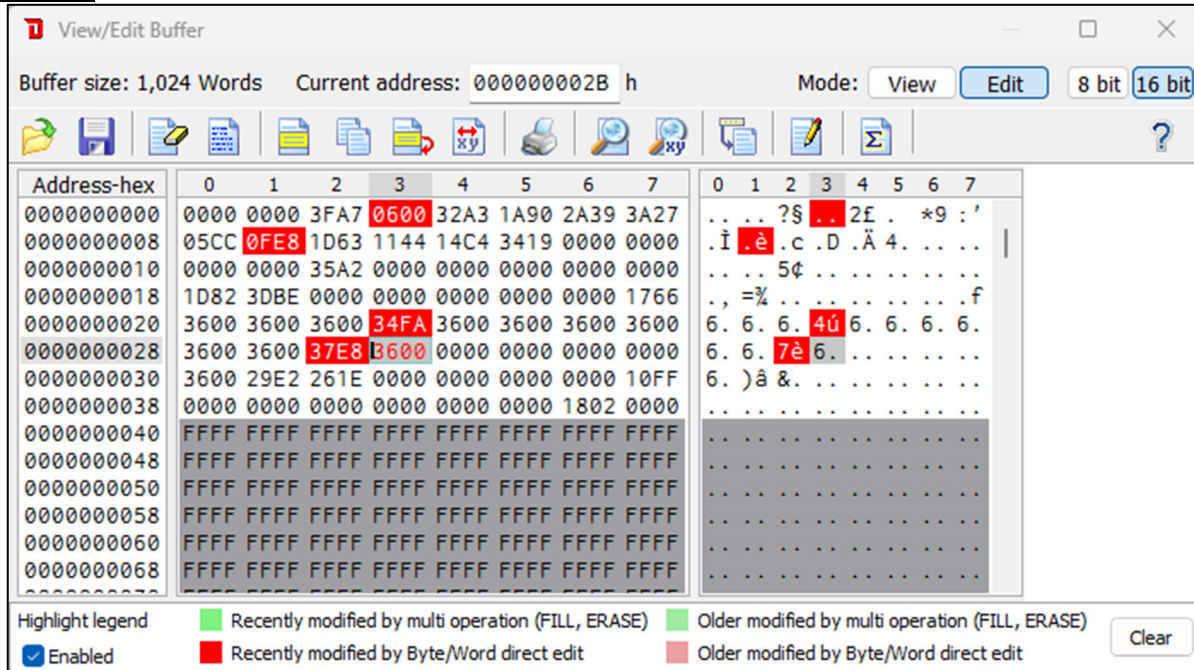
U.S. Patent No. 7,233,305	Exemplary Evidence of Infringement																																																																																																																																																																																																																																																															
	CM603:  View/Edit Buffer Buffer size: 1,024 Words Current address: 000000002B h Mode: View Edit 8 bit 16 bit <table><tr><th>Address-hex</th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr><tr><td>0000000000</td><td>0000</td><td>0000</td><td>3FA7</td><td>0600</td><td>32A3</td><td>1A90</td><td>2A39</td><td>3A27</td><td>..</td><td>..</td><td>?\$</td><td>.</td><td>2f</td><td>.</td><td>*9</td><td>:'</td></tr><tr><td>0000000008</td><td>05CC</td><td>0FE8</td><td>1D63</td><td>1144</td><td>14C4</td><td>3419</td><td>0000</td><td>0000</td><td>.İ</td><td>.è</td><td>.c</td><td>.D</td><td>.Ä</td><td>4.</td><td>..</td><td>..</td></tr><tr><td>0000000010</td><td>0000</td><td>0000</td><td>35A2</td><td>0000</td><td>0000</td><td>0000</td><td>0000</td><td>0000</td><td>..</td><td>..</td><td>5¢</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr><tr><td>0000000018</td><td>1D82</td><td>3DBE</td><td>0000</td><td>0000</td><td>0000</td><td>0000</td><td>0000</td><td>1766</td><td>.,</td><td>=%</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr><tr><td>0000000020</td><td>3600</td><td>3600</td><td>3600</td><td>34FA</td><td>3600</td><td>3600</td><td>3600</td><td>3600</td><td>6.</td><td>6.</td><td>6.</td><td>4ú</td><td>6.</td><td>6.</td><td>6.</td><td>6.</td></tr><tr><td>0000000028</td><td>3600</td><td>3600</td><td>37E8</td><td>B600</td><td>0000</td><td>0000</td><td>0000</td><td>0000</td><td>6.</td><td>6.</td><td>7è</td><td>6.</td><td>..</td><td>..</td><td>..</td><td>..</td></tr><tr><td>0000000030</td><td>3600</td><td>29E2</td><td>261E</td><td>0000</td><td>0000</td><td>0000</td><td>0000</td><td>10FF</td><td>6.</td><td>)â</td><td>&.</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr><tr><td>0000000038</td><td>0000</td><td>0000</td><td>0000</td><td>0000</td><td>0000</td><td>0000</td><td>0000</td><td>1802</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr><tr><td>0000000040</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr><tr><td>0000000048</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr><tr><td>0000000050</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr><tr><td>0000000058</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr><tr><td>0000000060</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr><tr><td>0000000068</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>FFFF</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr></table> Highlight legend - Recently modified by multi operation (FILL, ERASE) - Older modified by multi operation (FILL, ERASE) - Recently modified by Byte/Word direct edit - Older modified by Byte/Word direct edit Enabled Clear	Address-hex	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0000000000	0000	0000	3FA7	0600	32A3	1A90	2A39	3A27	..	..	?\$	.	2f	.	*9	:'	0000000008	05CC	0FE8	1D63	1144	14C4	3419	0000	0000	.İ	.è	.c	.D	.Ä	4.	..	..	0000000010	0000	0000	35A2	0000	0000	0000	0000	0000	..	..	5¢	..	..	..	..	..	0000000018	1D82	3DBE	0000	0000	0000	0000	0000	1766	.,	=%	..	..	..	..	..	..	0000000020	3600	3600	3600	34FA	3600	3600	3600	3600	6.	6.	6.	4ú	6.	6.	6.	6.	0000000028	3600	3600	37E8	B600	0000	0000	0000	0000	6.	6.	7è	6.	..	..	..	..	0000000030	3600	29E2	261E	0000	0000	0000	0000	10FF	6.	)â	&.	..	..	..	..	..	0000000038	0000	0000	0000	0000	0000	0000	0000	1802	..	..	..	..	..	..	..	..	0000000040	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	..	..	..	..	..	..	..	..	0000000048	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	..	..	..	..	..	..	..	..	0000000050	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	..	..	..	..	..	..	..	..	0000000058	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	..	..	..	..	..	..	..	..	0000000060	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	..	..	..	..	..	..	..	..	0000000068	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	..	..	..	..	..	..	..	..
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The chips were then removed from the programmer, reinserted and data was read again as shown below:

CM602:

The screenshot shows a 'View/Edit Buffer' window. The title bar says 'View/Edit Buffer'. Below the title bar, there's a status bar with 'Buffer size: 8,192.0 kWords', 'Current address: 00000003F h', and 'Mode: View Edit 8 bit 16 bit'. The main area is a table with two columns of hex data. The left column is labeled 'Address-hex' and ranges from 00000000 to 00000068. The right column shows hex values. A red highlight is visible on the value 'FFFF' at address 00000038. Below the table is a 'Highlight legend' with four items: 'Recently modified by multi operation (FILL, ERASE)' (green), 'Older modified by multi operation (FILL, ERASE)' (light green), 'Recently modified by Byte/Word direct edit' (red), and 'Older modified by Byte/Word direct edit' (pink). A 'Clear' button is at the bottom right.

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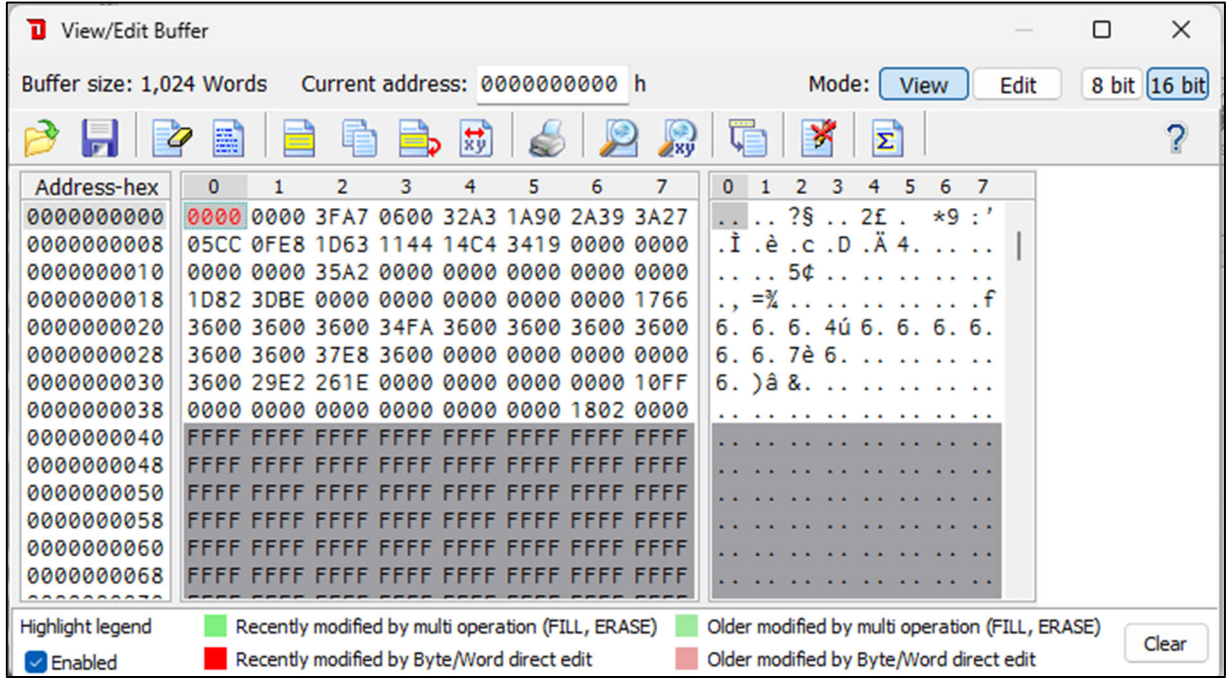
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	CM603:  Upon removal, the values written remain in memory, thus demonstrating the non-volatile nature of the memory. For example, as shown in table regarding the CM603 Chip, the two values changed in each bank are highlighted in blue below. Also, the expected output voltages were calculated using the formula Value / 60.2.

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	<table><tr><th colspan="5">Table G – CM603 Chip</th></tr><tr><th>GM</th><th>Bank 0 Dec</th><th>Bank 0 Hex</th><th>Expected Bank 0 voltage</th><th>Measured Voltage</th></tr><tr><td>GM1</td><td>935</td><td>3A7</td><td>15.53</td><td></td></tr><tr><td>GM3</td><td>512</td><td>200</td><td>8.50</td><td>8.52</td></tr><tr><td>GM6</td><td>675</td><td>2A3</td><td>11.21</td><td></td></tr><tr><td>GM7</td><td>656</td><td>290</td><td>10.90</td><td></td></tr><tr><td>GM8</td><td>569</td><td>239</td><td>9.45</td><td></td></tr><tr><td>GM9</td><td>551</td><td>227</td><td>9.15</td><td></td></tr><tr><td>GM10</td><td>460</td><td>1CC</td><td>7.64</td><td></td></tr><tr><td>GM11</td><td>1000</td><td>3E8</td><td>16.61</td><td>16.67</td></tr><tr><td>GM12</td><td>355</td><td>163</td><td>5.90</td><td></td></tr><tr><td>GM 13</td><td>324</td><td>144</td><td>5.38</td><td></td></tr><tr><td>GM16</td><td>196</td><td>C4</td><td>3.26</td><td></td></tr><tr><td>GM18</td><td>25</td><td>19</td><td>0.42</td><td></td></tr></table> <table><tr><th colspan="5">Table H – CM603 Chip</th></tr><tr><th>GM</th><th>Bank 1 Dec</th><th>Bank 1 Hex</th><th>Expected Bank 0 voltage</th><th>Measured Voltage</th></tr><tr><td>GM1</td><td>512</td><td>200</td><td>8.50</td><td></td></tr></table>	Table G – CM603 Chip					GM	Bank 0 Dec	Bank 0 Hex	Expected Bank 0 voltage	Measured Voltage	GM1	935	3A7	15.53		GM3	512	200	8.50	8.52	GM6	675	2A3	11.21		GM7	656	290	10.90		GM8	569	239	9.45		GM9	551	227	9.15		GM10	460	1CC	7.64		GM11	1000	3E8	16.61	16.67	GM12	355	163	5.90		GM 13	324	144	5.38		GM16	196	C4	3.26		GM18	25	19	0.42		Table H – CM603 Chip					GM	Bank 1 Dec	Bank 1 Hex	Expected Bank 0 voltage	Measured Voltage	GM1	512	200	8.50	
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		GM3	512	200	8.50	
		GM6	512	200	8.50	
		GM7	250	FA	4.15	4.15
		GM8	512	200	8.50	
		GM9	512	200	8.50	
		GM10	512	200	8.50	
		GM11	512	200	8.50	
		GM12	512	200	8.50	
		GM13	512	200	8.50	
		GM16	1000	3E8	16.61	16.62
		GM18	512	200	8.50	
	As can be seen above, after the Accused Innolux Chips were programmed with the new values, it was soldered back on to the board and the above measured values were recorded. As shown, the expected voltages match the measured voltages to within a few hundredths of a volt, demonstrating that the stored data generates the output Gamma voltages.					

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1[f]: wherein each bank contains a predetermined gamma reference voltage signal display condition; and	The Accused Innolux Chips meet the “each bank contains a predetermined gamma reference voltage signal display condition” element of claim limitation 1[f]. The court in EDTX has construed “predetermined gamma reference voltage signal display condition” to mean “a display condition established by the predetermined gamma reference voltage signals based on the application that is being displayed, external environment such as temperature and ambient light, or the personal preference of the user.” For the Accused Innolux Chips, by switching the Banks select pin (Pin 5), two different and distinct gamma reference voltage signals are applied to the column drivers to get a particular display condition. The default position of Bank Select pin is pulled to ground through the resistor, RG3. The PCB is designed to either select Bank 0 with RG3 installed, or select Bank1 by eliminating RG3 and instead placing resistor RG2 which serves as a pullup resistor on the Bank select pin to VDD (3.3 volts). By removing RG3, the Bank select pin can be connected to either VSS or VDD, and select between the two. In addition to Phenix’s general reservation of the right to supplement, Phenix reserves the right to amend its contentions with respect to this limitation to include or reference nonpublic information about the asserted infringement that was not discovered or located, despite diligent efforts, before the service of these infringement claim charts.

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1[g]: means to switch between the banks based on one or more external signals is provided on said integrated circuit.	The Accused Innolux Chips also meet the “means to switch between the banks based on one or more external signals is provided on said integrated circuit” element of claim limitation 1[g]. For example, in the CM602 and CM603, Pin 5 serves as the external structure for supplying the “one or more external signals” for switching between the banks. In addition, a switching circuit composed of one or more gates will be shown to be the internal structure for switching between the two Banks of memory. Upon information and belief, the Accused Innolux Chips including damping circuitry. For example, bench testing of the CM602 confirms damping circuitry. The numbers are <10 nanoseconds for the BKSEL input binary transition from 0 to 1 and 13.9V to 6V in 500 nanoseconds for V3 gamma output. An example of this damping circuitry can be seen in the photo below.

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	 The V650HP1-CPS1 board with CM602 was bench tested as follows. A function generator was fed into the Bank Select pin and the VGA7 pin was measured. Results are shown below. The yellow trace is VGA1 Output and the blue trace is Bank Select Input.

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Therefore the Accused Innolux Chips have a “means to switch between the banks based on one or more external signals is provided on said integrated circuit.”

Additional evidence of “means to switch between the banks based on one or more external signals is provided on said integrated circuit” in the Accused Innolux Chips will be obtained

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	during discovery of data sheets, schematics, and VHDL code from Innolux. In addition to Phenix’s general reservation of the right to supplement, Phenix reserves the right to amend its contentions with respect to this limitation to include or reference nonpublic information about the asserted infringement that was not discovered or located, despite diligent efforts, before the service of these infringement claim charts.
2. The integrated circuit of claim 1 wherein said non-volatile storage cells are reprogrammable.	Upon information and belief, the Accused Innolux Chips meet the “non-volatile storage cells [that] are reprogrammable” element of dependent claim 2. For at least the same reasons that the Accused Innolux Chips infringe claim 1, as described above, the Accused Innolux Chips meet the “non-volatile storage cells [that] are reprogrammable” element of dependent claim 2. Moreover, upon information and belief, alteration of the value of the memory locations may be written to the chip and the data and gamma reference voltages will remain even after conducting a power cycle. <i>See</i> claim 1. In addition to Phenix’s general reservation of the right to supplement, Phenix reserves the right to amend its contentions with respect to this limitation to include or reference nonpublic information about the asserted infringement that was not discovered or located, despite diligent efforts, before the service of these infringement claim charts.

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5. The integrated circuit of claim 1 wherein said circuits for programming require an external source for a high voltage programming means.	Upon information and belief, the Accused Innolux Chips meet the “said circuits for programming require an external source for a high voltage programming means” element of dependent claim 5. For at least the same reasons that the Accused Innolux Chips infringe claim 1, as described above, the Accused Innolux Chips meet the “said circuits for programming require an external source for a high voltage programming means” element of dependent claim 5. Moreover, non-volatile floating gate memories require a high voltage source for programming. Upon information and belief, Pin 8 is a pin for supplying an external high voltage analog supply, typically up to 20 volts, and used for programming. For example, Pin 8 was measured on the on the CM603 chip at voltage of 17.705V. In addition to Phenix’s general reservation of the right to supplement, Phenix reserves the right to amend its contentions with respect to this limitation to include or reference nonpublic information about the asserted infringement that was not discovered or located, despite diligent efforts, before the service of these infringement claim charts.