

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Innolux Corporation

Petitioner,

v.

Phenix Longhorn LLC

Patent Owner.

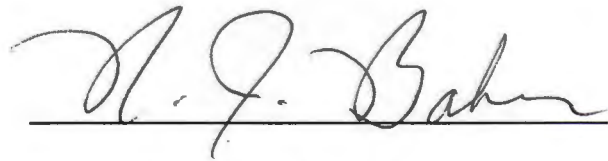
Case No. IPR2025-00043
U.S. Patent No. 7,233,305

**EXPERT DECLARATION OF R. JACOB BAKER, PH.D., P.E., IN
SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 7,233,305**

I declare under penalty of perjury that the following is true and correct. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on October 11, 2024

Liberty, TX

A handwritten signature in black ink, appearing to read "R. J. Baker", is written over a solid horizontal line.

R. Jacob Baker, Ph.D., P.E.

TABLE OF CONTENTS

I.	Introduction.....	4
II.	Qualifications.....	5
III.	Person Of Ordinary Skill In The Art.....	13
IV.	Legal Understanding.....	15
V.	Background.....	22
VI.	The '305 Patent.....	30
VII.	Claim Construction.....	34
VIII.	The State of the Art.....	39
IX.	The Prior Art.....	41
X.	Motivations to Combine	47
XI.	Ground 1: Claims 1-5, and 8-14 are Invalid as Obvious over Nakata	47
XII.	Ground 2: Claims 1-5, and 8-14 are Invalid as Obvious over Nakata, in view of Tsai	60
XIII.	Ground 3: Claims 1-5, and 8-14 are Invalid as Obvious over Petropoulos ..	69
XIV.	Ground 4: Claims 1-5, and 8-14 are Invalid as Obvious over Petropoulos in view of Tsai	77
XV.	Ground 5: Claims 1-5, and 8-14 are Invalid over Nakata, in view of Tsai, in further view of Yamazaki.....	77
XVI.	Ground 6: Claims 1-5, and 8-14 are Invalid as Obvious over Petropoulos in view of Yamazaki.....	88
XVII.	Ground 7: Claims 1-5, and 8-14 are Invalid as Obvious over Petropoulos in view of Tsai in further view of Yamazaki.....	89
XVIII.	Conclusion.....	89

I. Introduction

1. My name is R. Jacob Baker, Ph.D., P.E. I am an emeritus professor of electrical and computer engineering at the University of Nevada, Las Vegas. I have prepared this declaration as an expert witness on behalf of the Petitioner. I submit this declaration in support of a Petition for *Inter Partes* Review of United States Patent No. 7,233,305 (“the ’305 Patent”), owned by Phenix Longhorn LLC (“Phenix” or “Patent Owner”). I have been retained in this matter by Baker Botts LLP (“Counsel”) on behalf of Innolux Corporation (“Innolux” or “Petitioner”).

2. This declaration contains statements of my opinions formed to date and the bases and reasons for those opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses.

3. I make this declaration based upon my personal knowledge. I am over the age of 21 and am competent to make this declaration.

4. The statements herein include my opinions and the bases for those opinions, which are provided in the Exhibit List to the attached Petition.

5. The materials I considered in forming my opinions herein included at least those documents. In forming the opinions expressed in this declaration, I relied upon my knowledge, skill, experience, training, and education in the relevant field of the art, and have considered the viewpoint of a person of ordinary skill in

the art at the time of the alleged invention (“POSITA”), i.e., a POSITA as of January 28, 2004.

6. I am being compensated for my time in connection with this IPR at my standard consulting rate for consulting services. My compensation is not affected by the outcome of this matter. Although I am being compensated for my time in preparing this declaration, the opinions herein are my own.

II. Qualifications

7. My qualifications generally are set forth in my Curriculum Vitae, which has been submitted as Exhibit 1004, also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

A. Educational Background

8. I received a B.S. degree and a M.S. degree in electrical engineering from the University of Nevada, Las Vegas (“UNLV”) in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

9. My doctoral research, culminating in the award of a Ph.D. in Electrical Engineering in 1993, investigated the use of power MOSFETs (metal oxide semiconductor field effect transistors) in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power

MOSFETs to switch higher voltages, that is, greater than 1,000 V at near 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled “Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices,” published in the IEEE Transactions on Power Electronics. The paper received the 2000 Best Paper Award from the Power Electronics Society.

B. Industry Experience

10. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel’s cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

11. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change

Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. (“MTI”) in Boise, Idaho. I am a named inventor on 150 U.S. patents in integrated circuit design including Flash memory, DRAM, and CMOS image sensors. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system’s performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess

communications (IPC) with the memory controller (MC). In addition to work developing these high-speed digital communication systems, I've supervised a half dozen or so master's Theses in high-speed digital communications with focuses ranging from calibration to eliminating slack in digital timing. Further, I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed communications, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

12. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State,

for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density 3D packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc. From 1994 to 1996, I worked on the design of displays at Micron Display and Micron Technology, Inc. ("Micron") in Boise, Idaho. This work was at a time when cathode ray tubes (CRTs) were still the dominant type of display. Flat panel displays were being developed with the hope of replacing CRTs in the consumer market. I worked on flat panel displays which resulted in 5 patents: 5,598,156, 5,638,085, 5,818,365, 5,894,293, and 5,909,201. I worked on the design of the pixels, both active and passive, as well as the supporting electronics for processing video signals. I was involved with the evaluation of display technologies including liquid crystal displays (LCDs), light-emitting diodes, plasma displays, and organic light emitting diode (OLED) displays; the display technologies that were looking to displace CRTs in the consumer market. I was also involved with the packaging of the displays including the vacuum sealing and deposition of the phosphors for

light wavelength conversion. I also taught display design as a topic in my courses and did display design consulting again in industry for Cirque in 2013.

13. Further, I did consulting work in 2009 and 2010 at Sun Microsystems and then Oracle on the design of memory modules. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module at higher speeds.

14. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (Light Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook CMOS Mixed-Signal Circuit Design and a presentation, which I have presented at several universities and companies,

C. Academic Experience

15. I have been teaching electrical engineering since 1991. From 1991-1993, I was an adjunct faculty member in the electrical engineering department of the University of Nevada, Las Vegas and University of Nevada, Reno. From 1993

to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new electrical and computer engineering program at Boise State University (“BSU”) where I served as department chair from 2004 to 2007. At BSU I helped establish graduate programs in electrical and computer engineering including, in 2006, the university’s second Ph.D. degree. In 2012, I re-joined the faculty at UNLV where I am currently a Professor of Electrical and Computer Engineering. Over the course of my career as a professor, I have advised over 100 graduate students.

16. I have been recognized for my contributions as an educator and researcher in electrical and computer engineering. While at Boise State University, I received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the “Father of Silicon Valley”). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession. In 2011 I received the IEEE Circuits and Systems Education Award. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award each year I have been at UNLV.

17. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R. J., Wiley-IEEE, ISBN: 978-0470881323 (3rd ed., 2010)) and CMOS Mixed-Signal Circuit Design (Baker, R. J., Wiley-IEEE, ISBN: 978-0470290262 (2nd ed., 2009) and ISBN: 978-0471227540 (1st ed., 2002)). I co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R. J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 978-0-470-18475-2 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R. J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R. J., Li, H.W., and Boyce, D.E., Wiley-IEEE, ISBN: 978-0780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

D. Other Relevant Experience

18. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities. I am the author and co-author of more than 100 papers and presentations in the areas of solid-state circuit design and packages. A list of my publications and patents are on my curriculum vitae in Appendix B.

19. I currently serve, or have served, as a volunteer on: the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-present). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. In addition to the above, I am an IEEE Fellow and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

20. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

21. During the past several years, I have provided expert testimony, depositions, reports, or declarations in the cases shown in Appendix B.

III. Person Of Ordinary Skill In The Art

22. I have been informed by counsel that the content of a patent (including its claims) and prior art should be interpreted the way a POSITA would have interpreted the material at the time of invention. I understand from counsel

that the person of ordinary skill is a hypothetical person who is assumed to be aware of all the pertinent information that qualifies as prior art. In addition, the POSITA is a person of ordinary creativity who makes inferences and takes creative steps.

23. I have been informed by counsel that the “time of invention” I should use for purposes of this declaration is the date that the applicant for the ’305 Patent filed the earliest parent application in the United States Patent and Trademark Office, namely, June 11, 2003. I have not provided an opinion as to whether the claims of the ’305 Patent are entitled to that priority date.

24. It is my opinion that a POSITA at the time of the alleged invention would have had at least a bachelor of science degree in physics, electrical engineering, or the equivalent thereof and three (3) years of experience in circuit design or display technologies. Such a POSITA would have had knowledge of integrated circuits, gamma correction, and storage of gamma correction voltage values within memory, and would have understood how to search available literature for relevant publications.

25. In addition to my testimony as an expert, I am prepared to testify as someone who actually practiced in the field from 1985 to present, who actually possessed at least the knowledge of a POSITA in that time period, and who

actually worked with others possessing at least the knowledge of a POSITA in that time period.

IV. Legal Understanding

26. I have a general understanding of validity based on my experience with patents and my discussions with counsel.

27. I have a general understanding of prior art and priority date based on my experience with patents and my discussions with counsel.

28. I understand from my discussions with counsel that inventors may be entitled to a priority date earlier than the date of filing to the extent that they can show complete possession of particular claimed inventions at such an earlier priority date and reasonable diligence to reduce the claims to practice between such an earlier priority date and the date of filing of the patent. I understand from my discussions with counsel that if the patent holder contends that particular claims are entitled to an earlier priority date than the date of filing of the patent, then the patent holder has the burden to prove this contention with specificity.

29. I understand that, subject to the next paragraph, the asserted “priority date” of a patent is the earlier of: (a) the date on which a patent application is filed; or (b) the date on which an earlier-filed patent application is filed if the patent holder claims the benefit of priority to that earlier-filed patent application.

30. I understand that it is not enough for a patent to merely claim the benefit of an earlier-filed application, but that additional criteria must be met. In particular, the prior application itself must describe the claimed invention, and must do so in sufficient detail that one skilled in the art can clearly conclude that the inventor invented the claimed invention as of the filing date sought. First, I understand that a priority-date analysis is on a claim-by-claim basis. Second, I understand that, in order for a patent claim to be entitled to the filing date of an earlier patent application, a “Section 112 analysis” must be conducted. I am informed that a “Section 112” analysis encompasses looking to the earlier patent application, and ascertaining whether that earlier patent application meets both the written-description and enablement requirements as of the filing date of the earlier application. I understand that it is not enough that the claim would have been obvious from the earlier application, but that application itself must describe the claimed invention.

31. I understand that in order to satisfy the written description requirement the earlier application must reasonably convey to those skilled in the art that the inventors had possession of the subject matter of the patent as of the filing date of the earlier application. I have been informed that it is the disclosure of the earlier patent application that counts, and that while the meaning of terms, phrases, or diagrams in the earlier patent application must be interpreted from the

vantage point of one skilled in the art, all of the claimed limitations must appear in the specification. Further, I understand that this analysis is not a question of whether one skilled in the art might be able to construct the claimed invention from the teachings of the disclosure. The question is not whether a claimed invention is an obvious variant of that which is disclosed in the specification; rather, I understand that an earlier application must itself describe each of the claim limitations.

32. I also understand that in order to satisfy the enablement requirement, the earlier application must enable a POSITA to practice the claimed invention without undue experimentation.

33. I understand from my discussions with counsel that an invention by another must be made before the priority date of a particular patent claim in order to qualify as “prior art” under 35 U.S.C. § 102 or § 103, that a printed publication or a product usage must be publicly available before the date of invention of a particular patent claim in order to qualify as “prior art” under 35 U.S.C. § 102(a), that a printed publication or a product usage or offer for sale must be publicly available more than one year prior to the date of the application for patent in the United States in order to qualify as “prior art” under 35 U.S.C. § 102(b), or that the invention by another must be described in an application for patent filed in the United States before the priority date of a particular patent claim in order to qualify

as “prior art” under 35 U.S.C. § 102(e). I understand from my discussions with counsel that the Petitioner has the burden of proving that any particular reference or product usage or offer for sale is prior art.

34. I have a general understanding of anticipation based on my experience with patents and my discussions with counsel.

35. I understand that anticipation analysis is a two-step process. The first step is to determine the meaning and scope of the asserted claims. Each claim must be viewed as a whole, and it is improper to ignore any element of the claim. For a claim to be anticipated under U.S. patent law: (1) each and every claim element must be disclosed, either explicitly or inherently, in a single prior art reference; (2) the claim elements disclosed in the single prior art reference must be arranged in the same way as in the claim; and (3) the invention must be disclosed in the single prior art reference, in as complete detail as set forth in the claim. Where even one element is not disclosed in a reference, the anticipation contention fails. Moreover, to serve as an anticipatory reference, the reference itself must be enabled, i.e., it must provide enough information so that a POSITA can practice the subject matter of the reference without undue experimentation.

36. I have a general understanding of obviousness based on my experience with patents and my discussions with counsel.

37. I understand that a patent claim is invalid under 35 U.S.C. § 103 as being obvious only if the differences between the claimed invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in that art. An obviousness analysis requires consideration of four factors: (1) scope and content of the prior art relied upon to challenge patentability; (2) differences between the prior art and the claimed invention; (3) the level of ordinary skill in the art at the time of the invention; and (4) the objective evidence of non-obviousness, such as commercial success, unexpected results, the failure of others to achieve the results of the invention, a long-felt need which the invention fills, copying of the invention by competitors, praise for the invention, skepticism for the invention, or independent development.

38. I understand that a prior art reference is proper to use in an obviousness determination if the prior art reference is analogous art to the claimed invention. I understand that a prior art reference is analogous art if at least one of the following two considerations is met. First, a prior art reference is analogous art if it is from the same field of endeavor as the claimed invention, even if the prior art reference addresses a different problem and/or arrives at a different solution. Second, a prior art reference is analogous art if the prior art reference is reasonably

pertinent to the problem faced by the inventor, even if it is not in the same field of endeavor as the claimed invention.

39. I understand that it must be shown that a POSITA at the time of the invention would have had a reasonable expectation that a modification or combination of one or more prior art references would have succeeded. Furthermore, I understand that a claim may be obvious in view of a single prior art reference, without the need to combine references, if the elements of the claim that are not found in the reference can be supplied by the knowledge or common sense of one of ordinary skill in the relevant art. However, I understand that it is inappropriate to resolve obviousness issues by a retrospective analysis or hindsight reconstruction of the prior art and that the use of “hindsight reconstruction” is improper in analyzing the obviousness of a patent claim.

40. I further understand that the law recognizes several specific guidelines that inform the obviousness analysis. First, I understand that a reconstructive hindsight approach to this analysis, i.e., the improper use of post-invention information to help perform the selection and combination, or the improper use of the listing of elements in a claim as a blueprint to identify selected portions of different prior art references in an attempt to show that the claim is obvious, is not permitted. Second, I understand that any prior art that specifically teaches away from the claimed subject matter, i.e., prior art that would lead a POSITA to a

specifically different solution than the claimed invention, points to non-obviousness, and conversely, that any prior art that contains any teaching, suggestion, or motivation to modify or combine such prior art reference(s) points to the obviousness of such a modification or combination. Third, while many combinations of the prior art might be “obvious to try,” I understand that any obvious-to-try analysis will not render a patent invalid unless it is shown that the possible combinations are: (1) sufficiently small in number so as to be reasonable to conclude that the combination would have been selected; and (2) such that the combination would have been believed to be one that would produce predictable and well understood results. Fourth, I understand that if a claimed invention that arises from the modification or combination of one or more prior art references uses known methods or techniques that yield predictable results, then that factor also points to obviousness. Fifth, I understand that if a claimed invention that arises from the modification or combination of one or more prior art references is the result of known work in one field prompting variations of it for use in the same field or a different one based on design incentives or other market forces that yields predictable variations, then that factor also points to obviousness. Sixth, I understand that if a claimed invention that arises from the modification or combination of one or more prior art references is the result of routine optimization, then that factor also points to obviousness. Seventh, I understand that

if a claimed invention that arises from the modification or combination of one or more prior art references is the result of a substitution of one known prior art element for another known prior art element to yield predictable results, then that factor also points to obviousness.

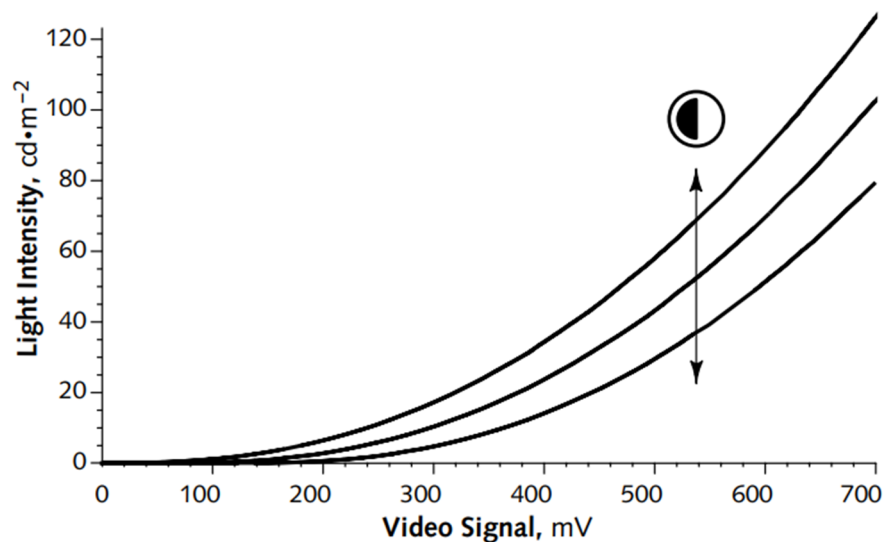
41. I understand from my discussions with counsel that the obviousness analysis should further consider evidence of “secondary considerations” such as commercial success, long-felt but unresolved needs, copying of the invention by competitors, and failures of others.

42. I understand that a dependent claim incorporates each and every limitation of the claim from which it depends. Thus, my understanding is that if a prior art reference fails to anticipate an independent claim, then that prior art reference also necessarily fails to anticipate all dependent claims that depend from the independent claim. Similarly, my understanding is that if a prior art reference or combination of prior art references fails to render obvious an independent claim, then that prior art reference or combination of prior art references also necessarily fails to render obvious all dependent claims that depend from the independent claim.

V. Background

A. Gamma Correction

43. Gamma correction is an important concept in display technology that ensures that images are faithfully rendered on display devices. (EX1009, at 92-93). Gamma correction addresses a mismatch between how electronic devices create images and how our eyes perceive them (EX1009, at 91). Traditional cathode ray tube (CRT) displays are known to have a nonlinear relationship between the input signal and display brightness - when you increase the input signal linearly, the brightness does not increase linearly. (EX1009, at 91). Instead, it follows a curved path (EX1009, at 913). This curve is described by a parameter called “gamma” (EX1009, at 92-93).

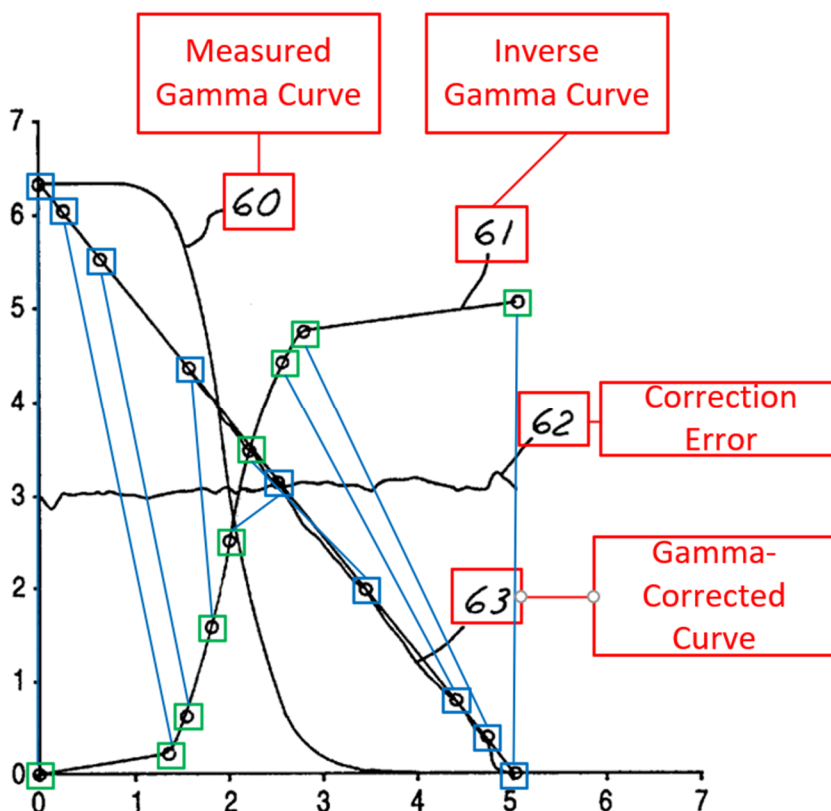


(EX1009, at 93). Human eyes have a similar but opposite curve when perceiving brightness (EX1009, at 93). By applying a gamma correction to adjust the signal

before it reaches the display, the final image matches what our eyes expect to see (EX1009, at 101).

44. Liquid Crystal Display (“LCD”) screens have a similar nonlinear relationship between input voltage and transmittance – how well the LCD panel allows light to pass through it. (EX1011, at 1:10-35). In order to correct this nonlinearity, the voltage-to-transmittance curve for a specific display must be determined, and an inverse transformation applied to accommodate for this nonlinearity (EX1011, at 1:36-60).

45. This is typically done by selecting a number of points (sometimes referred to as channels) on the measured gamma curve, and providing corrections for each of those points to produce an inverse gamma curve. (EX1011, at 3:63-4:16). When that inverse gamma curve is applied to inputs to the display, a linear relationship between input voltage and transmittance can be obtained. (EX1011, at 3:63-4:16). This is illustrated in the figure below, which shows a measured gamma curve 60 for a display, an inverse gamma curve 61 defined by nine points (highlighted in green), and the gamma-corrected curve 63. The annotations further illustrate how the nine points (in green) in the inverse gamma curve 61 map to nine points on the gamma corrected curve 63 (in blue).



(EX1011, at 4:17-23, Fig. 6). As described in EX1011, a common approach to gamma correction in LCD displays in 1997 was to store these nine points in high-speed digital memory, and to use a set of digital to analog converters (DAC's) to apply these gamma correction values to a display. (EX1011, at 4:43-65).

A. Gamma Correction Circuits

46. Many years later, in 2003 – the time of the alleged invention, the state of the art in display technology included sophisticated systems for gamma correction to optimize image quality. Display devices commonly incorporated integrated circuits with dedicated gamma correction functionality, including nonvolatile memory for storing correction data, control circuitry for applying

corrections, and driver circuits for outputting adjusted signals to display pixels. (EX1008, Fig. 1, 3:30-37, 6:10-28) These integrated designs, with components formed on a single substrate, enabled high-speed operations and efficient switching between different gamma correction data sets. (EX1008, 19:56-65)

47. The art recognized the importance of providing independent gamma correction for different color channels to improve overall image quality. Advanced data drivers could generate separate gamma reference voltages for red, green, and blue colors, allowing for optimized color reproduction. (EX1005, 1:61-2:3, Fig. 1) These systems typically employed digital-to-analog converters to transform stored digital gamma data into analog reference voltages, which were then used to convert image data into appropriate driving voltages for the display. (EX1005, 3:15-32, Fig. 1)

48. Flexibility in gamma correction was a key focus, with systems designed to store and apply multiple sets of correction data to accommodate varying display conditions. (EX1005, 2:25-28; EX1006, 2:29-35, 8:58-67) This adaptability was achieved through the use of reprogrammable nonvolatile memory arrays organized in rows and columns, allowing for efficient storage and retrieval of correction values. (EX1006, 4:11-25, 5:19-28, Fig. 3)

49. The art also taught sophisticated memory architectures to enable on-chip programming and flexible data management. Microcomputers with embedded

flash memory could partition storage into separate blocks for loader programs and application data, with shared I/O circuitry and bus multiplexing to efficiently switch between execution and programming modes. (EX1007, 3:5-13, 7:49-67, Fig. 3) This approach allowed for dynamic updating of stored data, including gamma correction values, without the need for external programming tools. (EX1007, Abstract, 2:38-43).

50. Overall, the state of the art demonstrated a clear trend towards integrated, flexible, and dynamically adjustable gamma correction systems in display devices, leveraging advances in memory technology and circuit design to optimize image quality across various operating conditions.

B. Addressing Memory Cells

51. By 2003, it was well known to those of ordinary skill in the art that memory arrays required multiplexers to perform read and write operations on each memory cell within an array of memory cells. For example, U.S. Patent No. 5,602,987 to Harari et al., titled “Flash EEPROM System” (“Harari”), discusses conventional techniques as of 1993 – a decade before the priority date of the ’305 Patent, for addressing digital memory in semiconductor devices. (EX1011). Below is Figure 7, which illustrates the data path for programming memory cells:

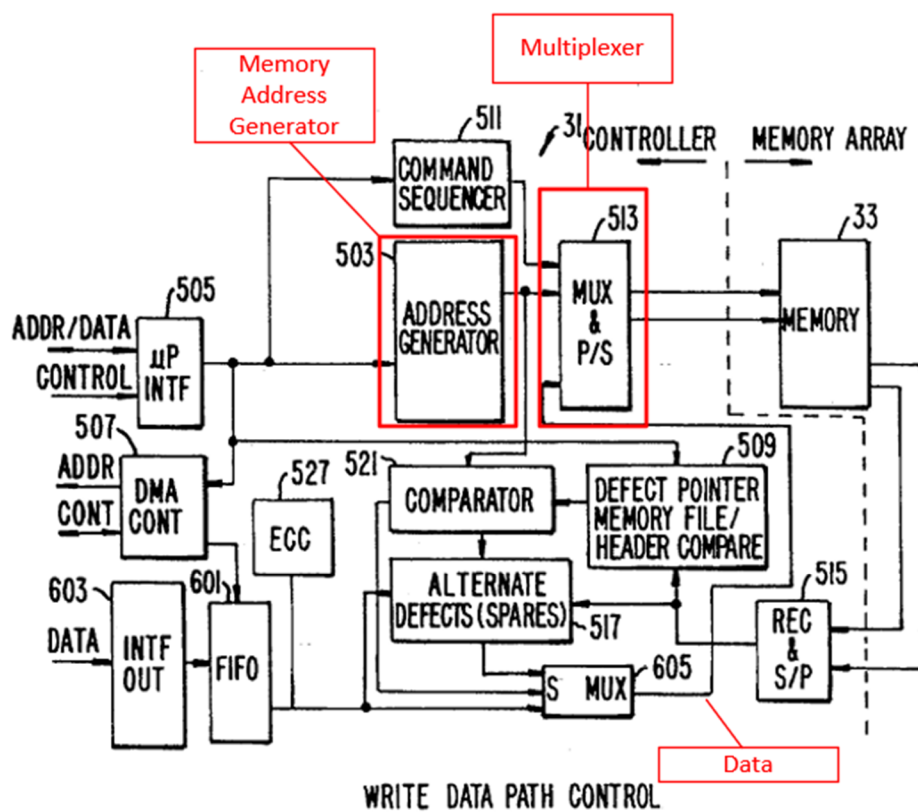


FIG. 7.

52. As Harari describes, “data is [] sent to the memory device through multiplexers 605 and 513” (EX1011, at 11:3-14).

53. As another example, some non-volatile storage systems use row and column select circuits in order to choose what memory cell to send data to. U.S. Patent 5,667,869 to Fazio (“Fazio”) illustrates this means of performing memory addressing:

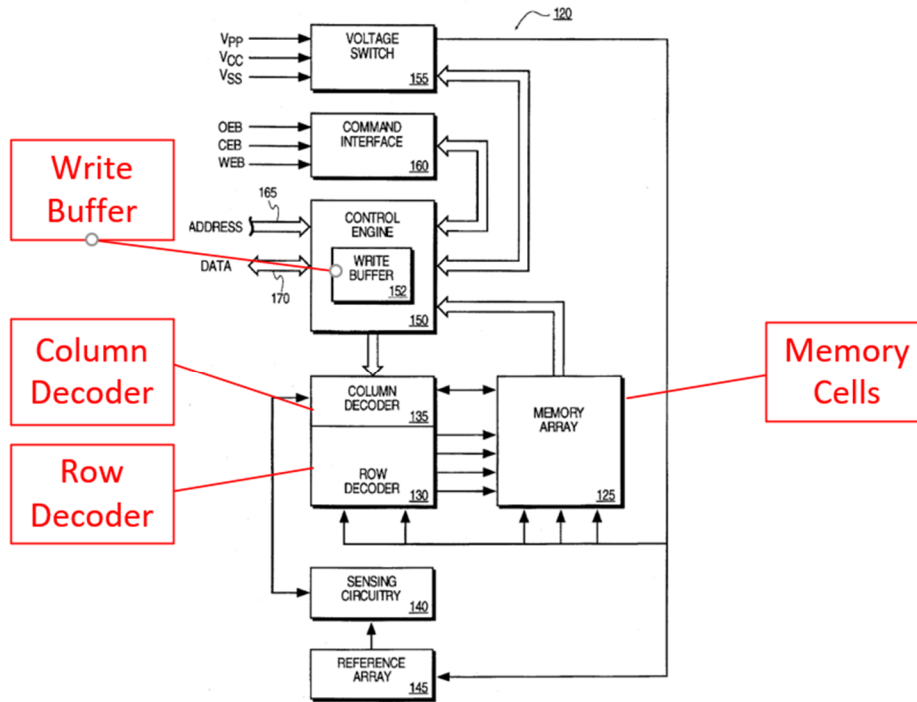


FIG. 8

54. Fazio describes this means of addressing as follows:

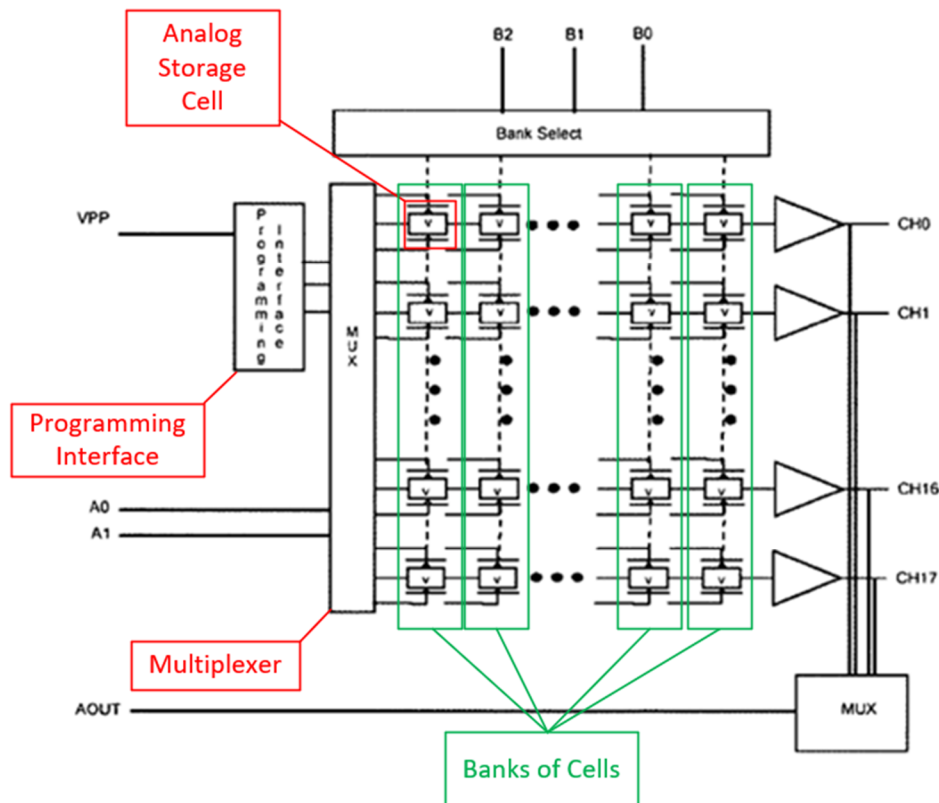
To read data stored in the memory array 125, row decoder 130 and column decoder 135 select a number of memory cells of the memory array 125 in response to a user-provided address received via address lines 165. Row decoder 130 selects the appropriate row of memory array 125, and column decoder 135 selects the appropriate column (or columns) of memory array 12

55. (EX 1012, at 7:17-23). As the figure depicts, the row decoder 130 and column decoder 135 also select rows and columns during write operations, as depicted by the arrow showing data flowing from the write buffer 152 to the column decoder 135 and row decoder 130, and on to the memory array 125.

VI. The '305 Patent

56. U.S. Patent 7,233,305 (“the '305 patent”) describes an integrated circuit for generating gamma reference voltages used in LCD displays. (EX1001, 1:10-15). The '305 patent acknowledges that gamma correction has long been a problem for TFT flat panel display manufacturers, and that existing approaches like select-on-test resistors were already known in the art. (EX1001, 1:19-27) The patent proposes using non-volatile storage cells to store gamma correction data, which can be programmed to output a set of gamma correction reference voltages. (EX1001, 2:16-28)

57. The '305 patent describes organizing the non-volatile storage cells into multiple banks, where each bank contains predetermined gamma reference voltage data for different display conditions. (EX1001, 5:49-58, Fig. 6).



58. (EX1001, Fig. 6). The integrated circuit includes means to switch between these banks based on external signals, such as using the Bank Select shown above. (EX1001, 5:59-6:6). The patent describes using a programming interface to allow programming of the buffer outputs during manufacturing and testing of the display panel. (EX1001, 2:22-28).

59. The '305 patent mentions that the non-volatile storage cells can be reprogrammable, allowing for updates to the stored gamma correction data. (EX1001, 2:29-35) The patent also notes that the storage cells can hold analog voltage values which are a constant fraction of the gamma reference voltage signals. (EX1001, 4:34-44) Additionally, the '305 patent describes using an

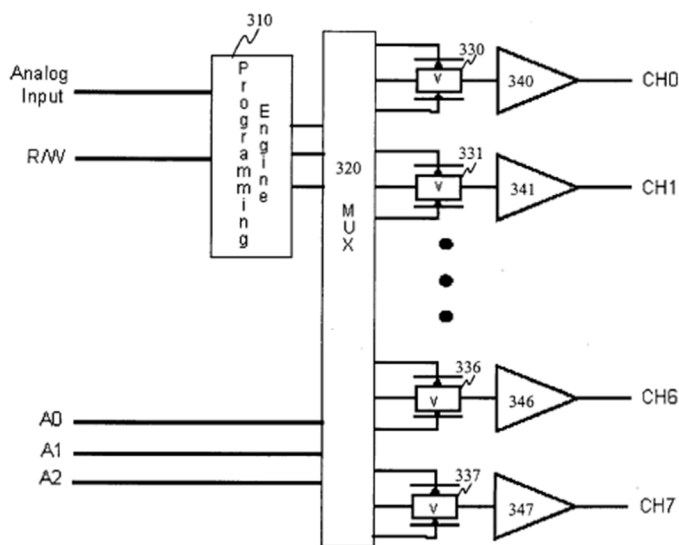
external source for supplying high voltage to the programming circuits. (EX1001, 6:22-36) The patent claims these features allow for automated assembly, automated test and gamma adjustment, and reprogrammable settings in a stand-alone solution. (EX1001, 2:29-38).

A. Priority Date of the '305 Patent

60. The '305 Patent was filed on December 23, 2003, and claims priority through Provisional Application No. 60/477,680, (the '680 Application) filed on June 11, 2003. (EX1001, cover; EX1016). In my opinion, however, the effective filing date of the claims challenged herein is December 23, 2003, because none of them are supported by the '680 Application.

61. The '680 Application entirely omits any specification description of the claimed invention at all. While the Application Data Sheet lists an invention titled "Gamma Trimster and Method for Gamma reference Voltage Generation for Displays", the actual filing contains a specification for a "Haptic Targeting Device." (EX1016, at 4, 8). That specification describes an "Invention [that] relates [to] haptic devices, and in particular to a targeting device providing haptic feedback to a user." (*Id.*). The specification contains no description of displays, gamma correction, or any other feature claimed in the '305 Patent. There appears to have been an error in the filing of the '680 Application, such that the specification of an entirely different application was filed completely unrelated to

gamma correction. The '680 Patent does have three figures that apparently were intended to be part of the filing, but these figures do not include any that show numerous claimed features in the challenged claims. That one figure – Figure 3 – illustrates an embodiment with a single row of non-volatile memory cells, and omits a second output multiplexer:



300

FIG. 3

62. (EX1016, at 3). In my opinion, this figure would not have put a POSITA in possession of the claimed invention. As a result, there is no support for the limitation “said non-volatile storage cells are organized into two or more banks of cells” in Claim 1, or “an output pin connected to an output through a second multiplexer connected to said plurality of outputs” in Claim 8. Therefore, in my opinion, the effective filing date of the claims challenged herein is December 23, 2003.

VII. Claim Construction

63. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a POSITA, at the time of the alleged invention. In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, the prosecution history of record, and the knowledge of a POSITA at the relevant time. I have followed these principles in my analysis.

A. “means to switch between the banks based on one or more external signals”

64. I understand that in the Wistron Litigation, the court ruled that this term was a means-plus-function limitation under § 112(6). (EX1013, at 46). The court further ruled that this term recites the function of “switching between the banks based on one or more external signals,” and referred to the Bank Select components in the '305 Patent, shown in Fig. 4A (B0-B2); Fig. 4B (pins 20, 22, 23), Fig. 5 (Tdamp); Fig. 6 (Bank Select, B0, B1, B2). (EX1012, at 46).

65. In my opinion, this construction is mostly correct, but is incorrect in that it includes the damping functionality. This damping function is not described in the claim limitation, nor is this “damping” circuit a required feature of embodiments of the '305 Patent, which only suggests that such circuits be used “when deemed appropriate.”

66. Further, the inclusion of this “damping” feature would vitiate the scope of Claim 3, which further requires that the “means to switch between banks can have a switching time from about 10msec to about one second.” This Claim 3 additionally requires features which could be embodied by the damping circuit, but their express inclusion in Claim 3 suggests that they are *not* included in the function of Claim 1.

67. Accordingly, it is my opinion that the proper construction of this term is that it recites the function of “switching between the banks based on one or more external signals” as shown in Fig. 4A (B0-B2); Fig. 4B (pins 20, 22, 23), and Fig. 6 (Bank Select, B0, B1, B2). Nonetheless, as a POSITA would recognize, the “damping circuit” described is merely a low-pass filter, a common component well within the knowledge of a POSITA that, as argued below, could easily have been added to any of the prior art described below.

B. “non-volatile storage cell”

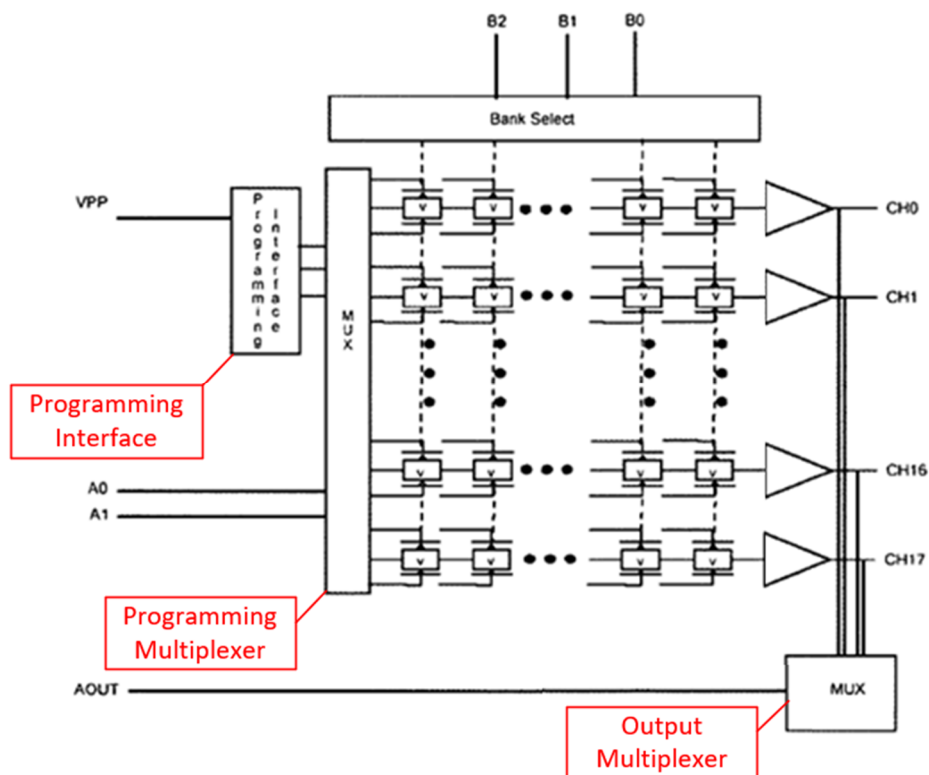
68. The court in the Wistron Litigation ruled that a “non-volatile storage cell” refers to “memory cells which retain stored data even when power is removed,” which can encompass both digital and analog storage cells. (EX1013, at 18-25). I agree with this construction. The term “non-volatile storage cell,” would have been understood by a POSITA to refer to digital or analog storage.

C. “multiplexer”

69. The term “multiplexer” means “one or more circuits that couple (1) one input (or one set of inputs) to one of many outputs (or one of many sets of outputs) [a de-multiplexer] or (2) one of many inputs (or one set of many sets of inputs) to one output (or one set of outputs) [a multiplexer].” (EX1012, at 13).

70. I understand that in a prior IPR proceeding the Board construed “multiplexer” to mean “a device that interleaves signals to a single line, or selects one input and switches its information to the output.” (EX1014, at 14). The Board based this construction on a definition of the term in the Authoritative Dictionary of IEEE Standard Terms. (EX1014, at 13). However, this construction is incorrect and inconsistent with the use of the term as it is used in the ’305 Patent, which makes clear that the term “multiplexer” can refer either to a device that can switch one of many inputs to a single output, *or* switch one input to one of many outputs.

71. Claim 1 explains that the multiplexer is “for addressing and programming said storage cells.” (EX1001, at Claim 1). The multiplexer referred to in the claims is shown below as “Programming Multiplexer”:



(EX1001, Fig. 6).

72. When the multiplexer is used as part of the programming interface to write to the storage cells, the multiplexer is used to allow the programming interface to write to the various storage cells. That is, it takes in a from the programming interface, and can switch that signal to one of many outputs to the storage cells (i.e. a one-to-many multiplexer). Fig. 6 also shows another multiplexer, which is used to switch the gamma correction channels (CH0-17) to the analog output (AOUT), which is therefore switching many input signals to one output (i.e. a many-to-one multiplexer.). This is also consistent with how the term “multiplexer” is used by POSITAs, where the term “multiplexer” can be a generic

term to refer to multiplexers, demultiplexers, or bidirectional multiplexers (that operate as either multiplexers or demultiplexers depending on the operating mode.).

73. I understand that, in the Wistron Litigation, Patent Owner agreed that the term “multiplexer” should be defined as” one or more circuits that couple (1) one input (or one set of inputs) to one of many outputs (or one of many sets of outputs) [a de-multiplexer] or (2) one of many inputs (or one set of many sets of inputs) to one output (or one set of outputs) [a multiplexer].” (EX1012, at 13). I agree that this is the correct construction that is consistent with how the term is used by POSITAs, and how the term is used in the ’305 Patent. (EX1001, at 3:18-31, 3:48-4:3).

D. “two or more banks of cells”

74. In my opinion, the term “two or more banks of cells” should be construed as “two or more separate devices of addressable computer memory.” In the prior proceeding, the Board adopted a similar construction of the term “banks of cells,” which it construed as “contiguous sections of addressable memory” (EX1014, at 15). The Board relied upon the Authoritative Dictionary of IEEE Standards Terms, which in part defined a “bank” as “a contiguous section of addressable memory.” (EX1014, at 15).

75. But in my opinion, this construction is incorrect. I agree that the term “bank” as it is used to refer to a single collection of devices. However, the claim term refers to a plurality of banks of cells, not a single bank. As a result, the term as it is used in the ’305 Patent must refer to separate “banks,” and not a single bank. And if a bank is a “contiguous section of addressable memory,” then the term “two or more banks of cells” must refer to more than one such contiguous sections.

VIII. The State of the Art

76. At the time of the alleged invention, the field of gamma correction for LCD displays was well-developed, with various integrated solutions available to address the challenges of precise voltage generation and dynamic adjustment. The prior art demonstrates that key elements of the claimed invention were already known and combined in similar ways by those skilled in the art.

77. Integrated circuits for producing multiple gamma reference voltages were common, typically incorporating non-volatile storage, programming circuits, and output drivers. For example, Petropoulos discloses an integrated circuit with analog/multi-level non-volatile memory cells, programming circuits coupled to a routing circuit (multiplexer) for addressing, and drivers connected to outputs. (EX1006, 4:11-36, 9:10-17, Fig. 2) Similarly, Nakata teaches a gamma correction voltage generation device with non-volatile registers, a serial interface for

programming, and buffer amplifiers driving multiple outputs. (EX1005, [0017]-[0019], [0028], Fig. 1)

78. The organization of storage cells into multiple banks for different display conditions was also known. Nakata describes multiple sets of registers, each holding different gamma correction patterns that can be switched between based on external signals like scanline information. (EX1005, [0021]-[0024], Fig. 2) This allowed for dynamic gamma adjustment to enhance image quality under varying display conditions.

79. Reprogrammability of non-volatile storage was a standard feature, enabling in-situ optimization of gamma correction values. Yamazaki's system, for instance, allowed for erasing and reprogramming of FAMOS-type TFTs storing gamma correction data. (EX1008, 8:16-34, 9:9-12) This capability facilitated fine-tuning of display characteristics over time.

80. The use of analog voltage storage representing fractional values of gamma reference voltages was also practiced. While some systems like Nakata used digital storage with DAC conversion, others stored analog values directly. A POSITA would recognize the tradeoffs between these approaches and select the appropriate method based on design requirements.

81. In summary, the prior art demonstrates that integrated gamma correction systems with reprogrammable non-volatile storage, multiple voltage

outputs, and dynamic adjustment capabilities were well-established. The claimed invention appears to be, at most, a straightforward combination of known elements performing their expected functions to yield predictable results in display gamma correction.

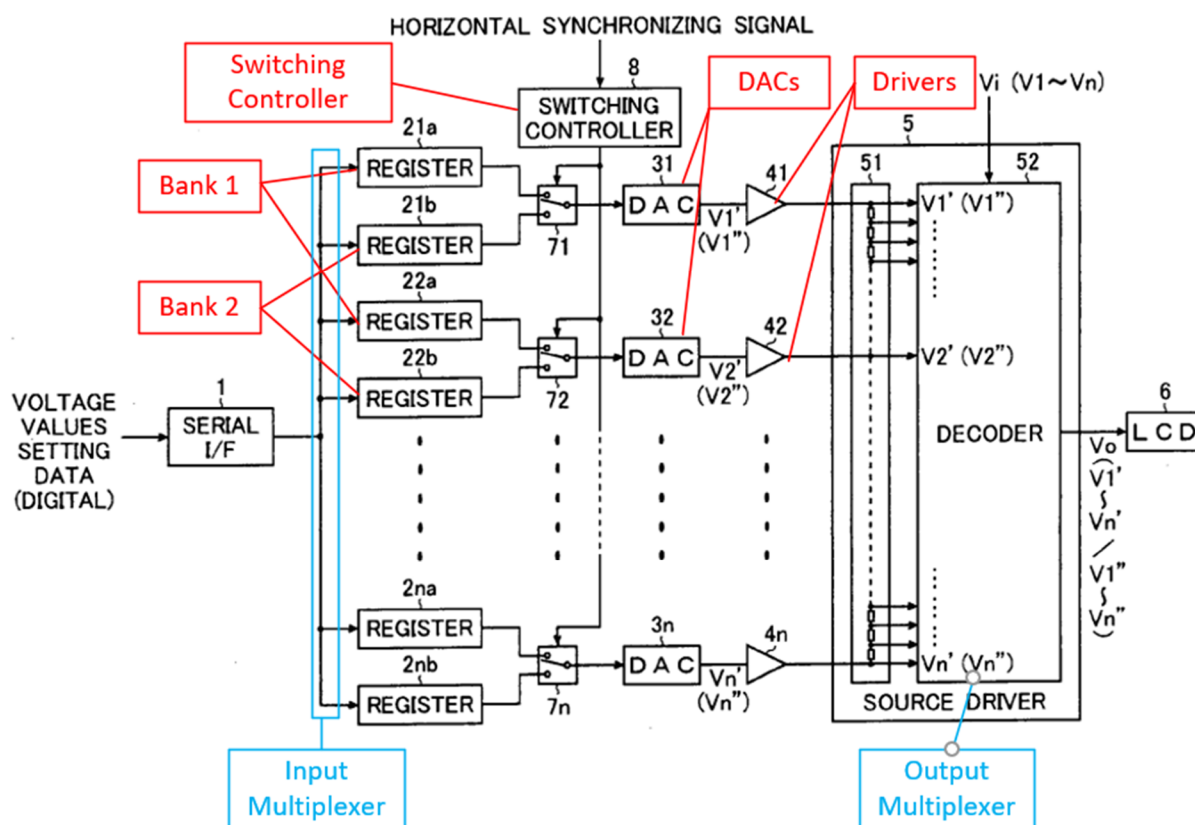
IX. The Prior Art

A. Nakata (EX1005)

82. The Nakata reference discloses a gamma correction voltage generation device for producing gamma reference voltages to drive a liquid crystal display. (EX1005, [0017], Fig. 1). The device comprises multiple sets of registers for holding digital data, digital-to-analog converters (DACs) for converting the digital data to analog voltages, and buffers for amplifying and outputting the analog voltages as gamma correction voltages. (EX1005, [0017]-[0019], Fig. 1). Nakata teaches that the registers can be implemented as non-volatile, reprogrammable memories to easily store and update corrected gamma values. (EX1005, [0019], [0028]).

83. In some embodiments, Nakata discloses organizing the registers into multiple banks, each containing a different pattern of gamma correction data. (EX1005, [0021]-[0024], Fig. 2). A switching controller allows switching between these banks based on external signals like scanline information. (EX1005, [0024], Fig. 2). This reference was selected because it demonstrates that using

reprogrammable non-volatile storage to generate customizable gamma correction voltages was known in the art. The multi-bank organization and switching capabilities further show that dynamically adjustable gamma correction based on display conditions was a known technique for enhancing image quality in LCD devices.

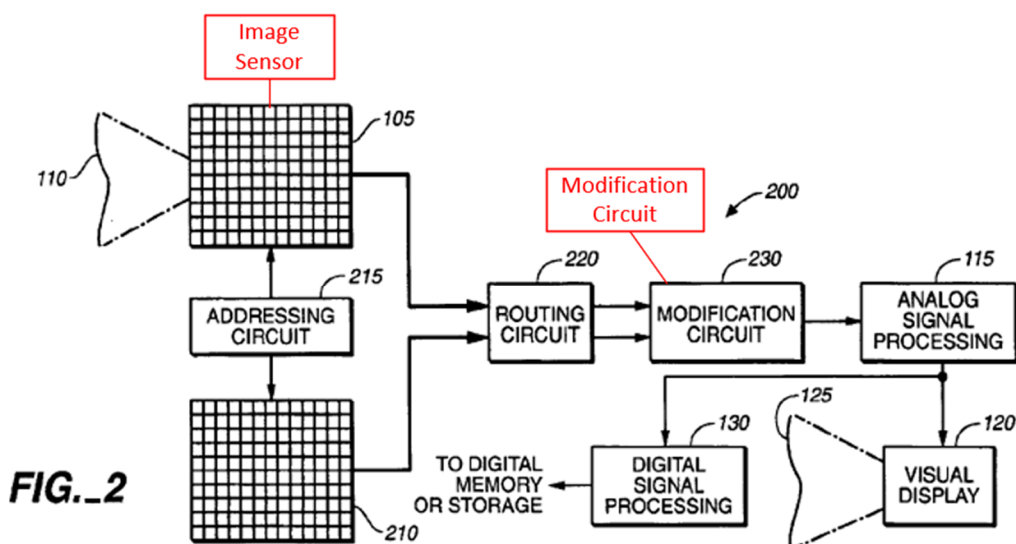


(EX1005, at Fig. 3 (annotated)).

B. Petropoulos (EX1006)

84. The Petropoulos reference discloses an integrated circuit for modifying sensor array outputs using programmable analog/multi-level non-volatile memory. (EX1006, 3:38-47, Fig. 2) The system stores modification

voltages, including gamma correction values, in reprogrammable memory cells organized in rows and columns. (EX1006, 4:11-25, 5:19-28, Fig. 3) These stored values are used to adjust sensor outputs through various modification circuits, such as summing, subtraction, and multiplication. (EX1006, 4:52-64, 7:7-24, Figs. 4-5) The reference also describes using high programming voltages supplied externally to program the non-volatile memory cells. (EX1006, 5:58-64) Petropoulos was selected for this IPR because it demonstrates that storing and applying gamma correction values using reprogrammable non-volatile memory in display driver circuits was known in the art. The reference shows how gamma correction values could be flexibly stored and updated to optimize display output for various conditions.



(EX1006, at Fig. 2)

C. Tsai (EX1007)

85. The Tsai reference discloses a microcomputer with an embedded flash memory unit that enables on-chip programming without external tools. (EX1007, Abstract, 2:38-43). The flash memory is partitioned into a loader block for storing a loader program and a user block for storing application programs, both sharing the same I/O circuit. (EX1007, 3:5-13, Fig. 2). A bus multiplexer selectively connects either block to the microprocessor unit or register set based on memory selection (MSEL) and bus selection (BSEL) signals. (EX1007, 3:23-42, 7:49-67, Fig. 3). This architecture allows for efficient switching between executing the loader program and writing new data to the user block during on-chip programming. (EX1007, 7:49-67). The microprocessor includes a timer to control the programming process, ensuring sufficient time for data transfer while maintaining system responsiveness. (EX1007, 4:41-5:21, Fig. 4). Tsai's reprogrammable memory structure and flexible switching mechanism make it particularly relevant for implementing updateable voltage generation systems, such as those used for gamma correction in displays. The ability to store and switch between multiple sets of programmed data aligns well with the needs of adaptive display systems.

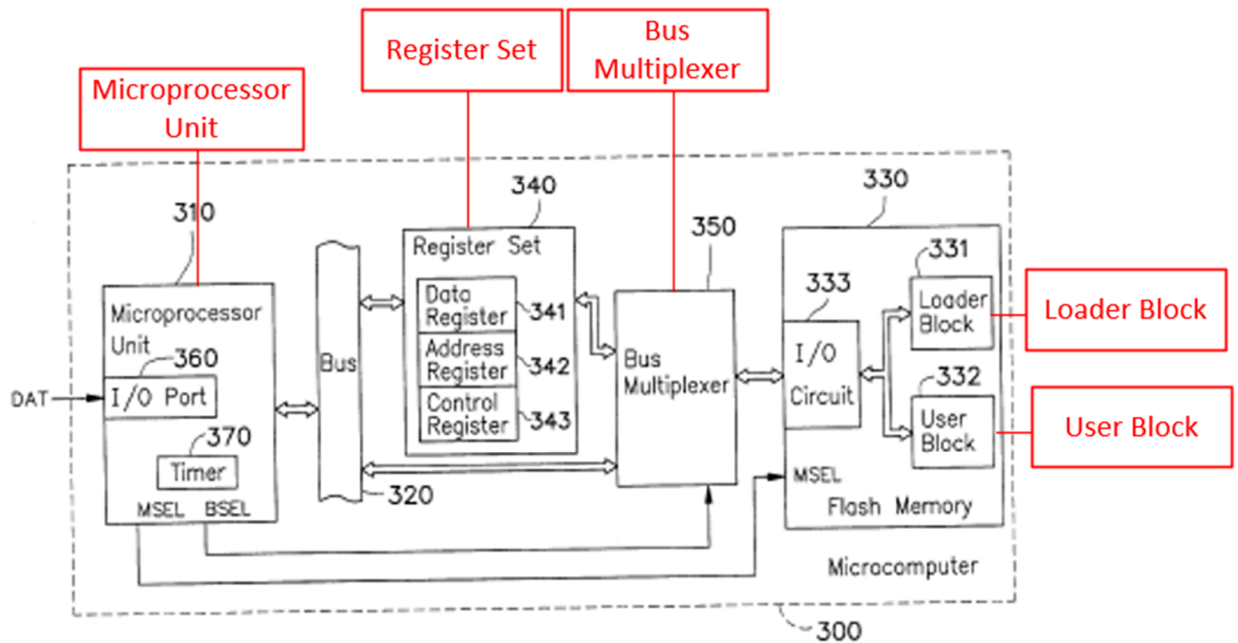


FIG. 3

D. Yamazaki (EX1008)

86. Yamazaki discloses an integrated circuit for gamma correction in a display device. The circuit includes a nonvolatile memory for storing gamma correction data, a control circuit for performing gamma correction, and driver circuits for outputting corrected signals to display pixels. (EX1008, Fig. 1, 3:30-37, 6:10-28) The nonvolatile memory comprises FAMOS-type TFTs with floating gates arranged in a matrix, allowing storage of multiple gamma correction data sets. (EX1008, Fig. 3, 8:16-34) Yamazaki's system enables customized gamma correction for individual displays by storing device-specific correction data. (EX1008, 5:60-6:9)

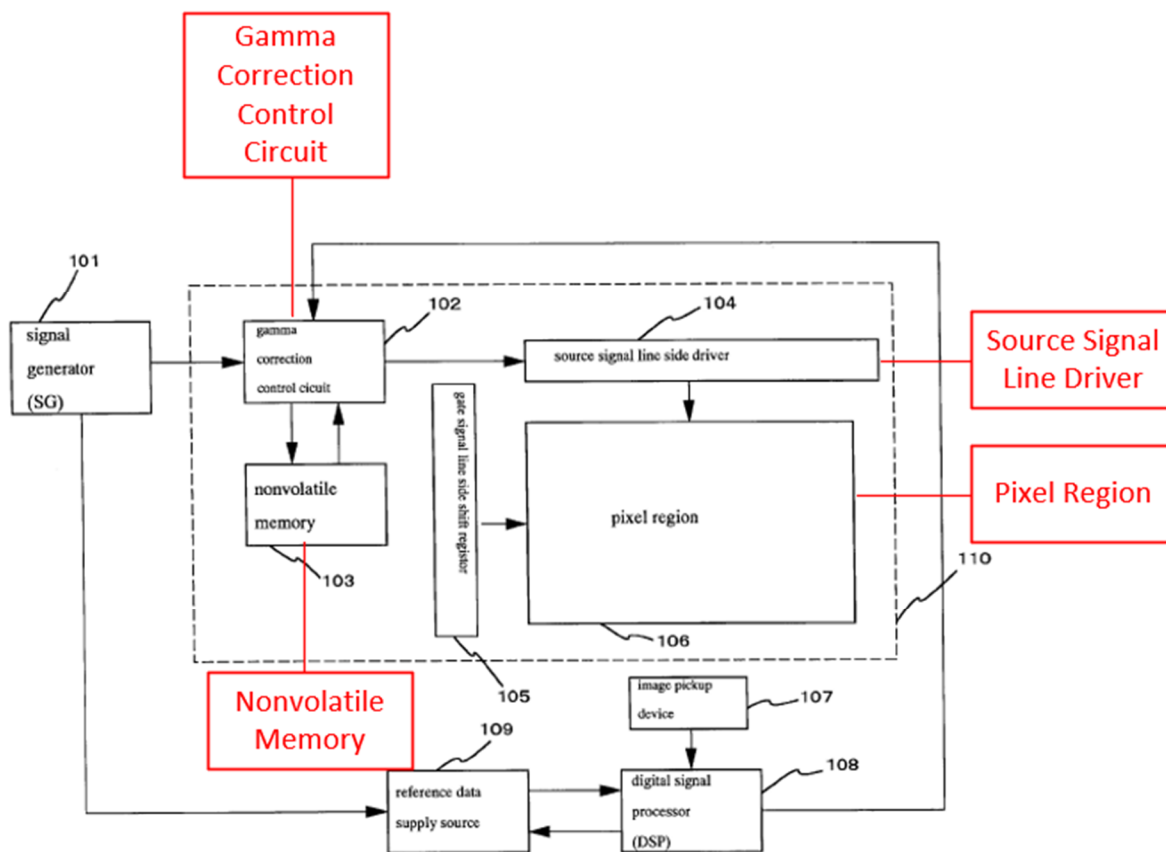


Fig. 1

(EX1008, Fig. 1)

87. The gamma correction control circuit receives input signals and addresses the appropriate memory cells to retrieve correction data. (EX1008, 6:39-46) This data is then used to adjust voltage levels applied to the display columns via the source signal line side driver. (EX1008, 6:14-28) Yamazaki's integrated design, with all components formed on a single substrate, enables high-speed operations and efficient switching between different gamma correction data sets. (EX1008, 19:56-65)

X. Motivations to Combine

88. A POSITA would be motivated to combine each of the asserted combinations here to arrive at the challenged claims. Each of Nakata, Petropoulos, and Yamazaki relate to the field of integrated circuits for producing gamma reference voltages to drive a display. Each also includes programmable non-volatile storage cells for storing the voltage values. Thus, all the references asserted here are analogous art, because they are in the same field of endeavor. Tsai is in the field of memory devices, and thus would also be analogous to the '703 Patent because it is also in the same field of endeavor – related to the storage and use of information – but does not disclose gamma reference voltage correction. Even if Tsai is not in the same field of endeavor, it is reasonably pertinent to the problems to be solved by the '305 Patent, because it discloses a memory device useful for storage and retrieval of information. The specific rationales to combine these references, along with more specific similarities of each, are further provided below.

XI. Ground 1: Claims 1-5, and 8-14 are Invalid as Obvious over Nakata

89. Claims 1-5, and 8-14 are invalid as obvious over Nakata. Below is a limitation-by-limitation analysis of Nakata, showing where each limitation is found in the prior art.

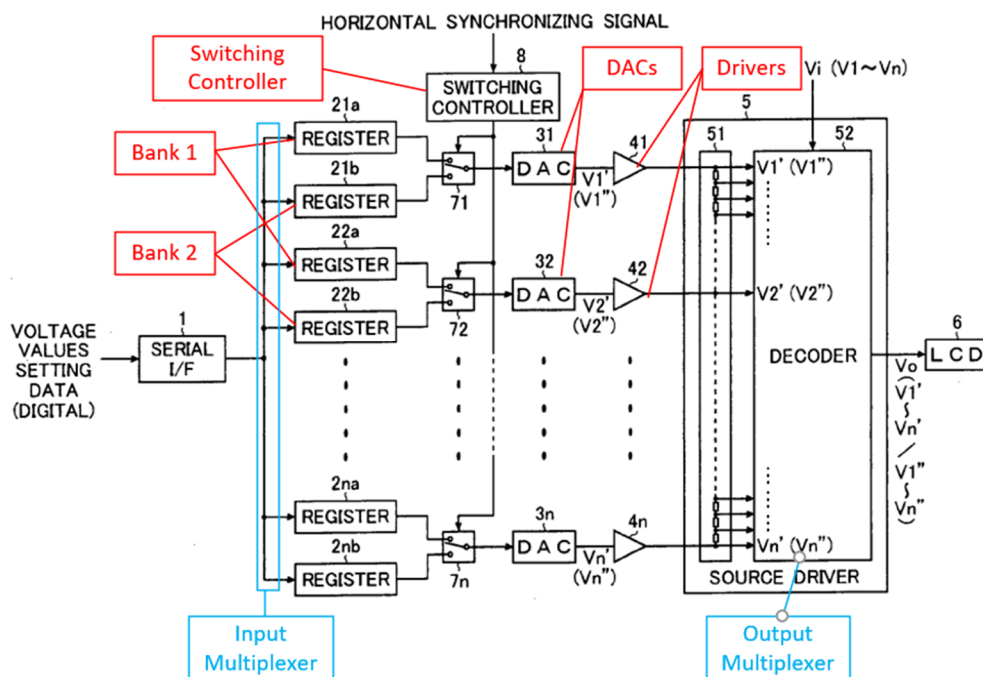
A. Claim 1

1. Limitation 1[0]: An integrated circuit for producing voltage signals on a plurality of outputs comprising:

90. Nakata discloses an integrated circuit for producing voltage signals on a plurality of outputs. Nakata describes a gamma correction voltage generation device that outputs analog voltages V_1' to V_n' as gamma correction voltages on multiple outputs from buffers 41 to 4n. (EX1005, [0017]-[0019], Fig. 1). While not explicitly labeled an “integrated circuit,” a POSITA would understand the gamma correction voltage generation device to be implemented as an integrated circuit, as this was the standard implementation for display driver circuits at the time. (EX1005, [0029]-[0031]).

2. Limitation 1[1]: a plurality of non-volatile storage cells;

91. Nakata discloses a plurality of non-volatile storage cells. Specifically, Nakata describes registers 21 to 2n for holding digital data used to generate gamma correction voltages, shown below as Bank 1 and Bank 2. (EX1005, [0017]-[0019], Fig. 1).



(EX1005, Fig. 3 (annotated)).

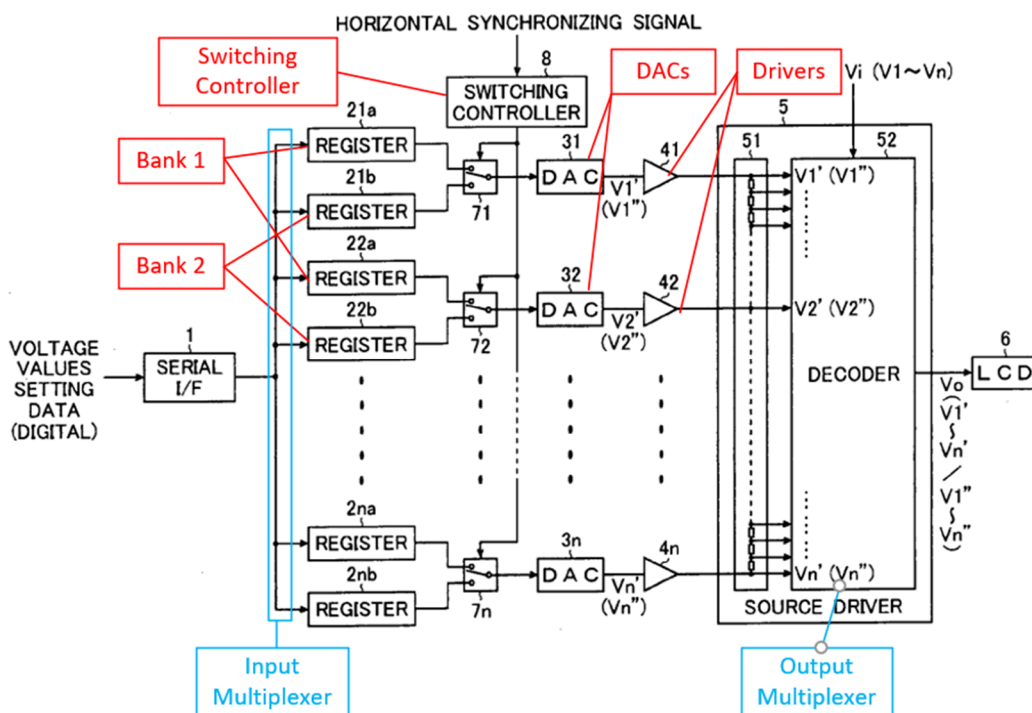
92. Nakata teaches that these registers can be implemented as non-volatile memories to easily store corrected values without a separate memory device. (EX1005, [0028]). While not explicitly called “storage cells,” a POSITA would understand the non-volatile registers to be comprised of storage cells for holding individual digital data bits. Therefore, Nakata’s non-volatile registers correspond to the claimed plurality of non-volatile storage cells.

3. Limitation 1[2]: circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs;

93. Nakata discloses circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based

on a plurality of inputs. Specifically, Nakata describes a serial interface 1 for distributing digital data to registers 21 to 2n. (EX1005, [0017], [0020], Fig. 1).

While not explicitly called a multiplexer, a POSITA would understand the serial interface 1 includes multiplexing functionality to route serial data to multiple registers based on addressing. This can be seen in the figure below, labeled (“Input Multiplexer”), where the output from the Serial I/F component branches out to the various registers for programming, and is thus a “multiplexer:”



(EX1005, Fig. 3 (annotated)).

94. The addressing is based on the serial input data, which comprises a plurality of inputs. (EX1005, [0017], Fig. 1). Therefore, Nakata discloses programming circuits (serial interface 1) coupled to multiplexing functionality for

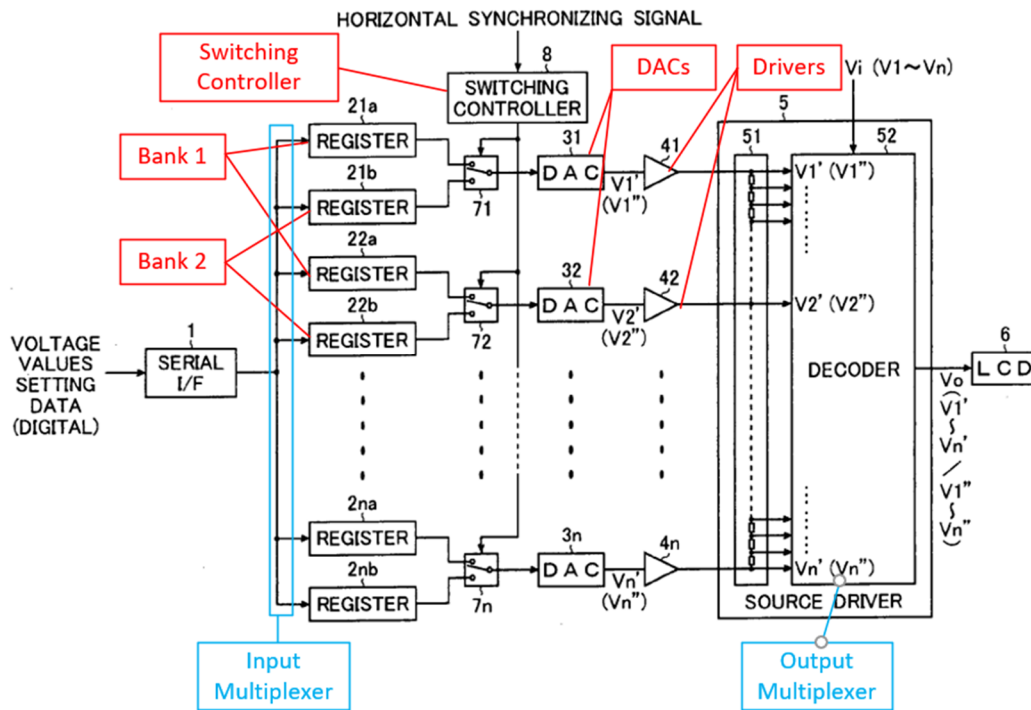
addressing and programming the registers (storage cells) based on plural inputs (serial data).

4. Limitation 1[3]: drivers connected to said storage cells and to the plurality of outputs; and

95. Nakata discloses drivers connected to said storage cells and to the plurality of outputs. Specifically, Nakata discloses DACs 31 to 3n connected to the registers 21 to 2n (storage cells), and buffers 41 to 4n connected to the outputs of the DACs. (EX1005, [0017]-[0019], Fig. 1). The DACs and buffers together form drivers that convert the digital data in the registers to analog voltages and amplify them to drive the plurality of outputs. (EX1005, [0017]-[0019]). Therefore, Nakata clearly discloses the claimed drivers connected to both the storage cells and outputs.

5. Limitation 1[4]: the plurality of inputs connected to said multiplexer for addressing said storage cells, wherein said voltage signals are gamma reference voltage signals for determining actual driving voltages of columns of a display,

96. Nakata discloses the plurality of inputs connected to said multiplexer for addressing said storage cells, wherein said voltage signals are gamma reference voltage signals for determining actual driving voltages of columns of a display. The serial input data (plurality of inputs) is used by the serial interface 1 (which includes multiplexing functionality) to address and program the registers. (EX1005, [0017], [0020], Fig. 1).



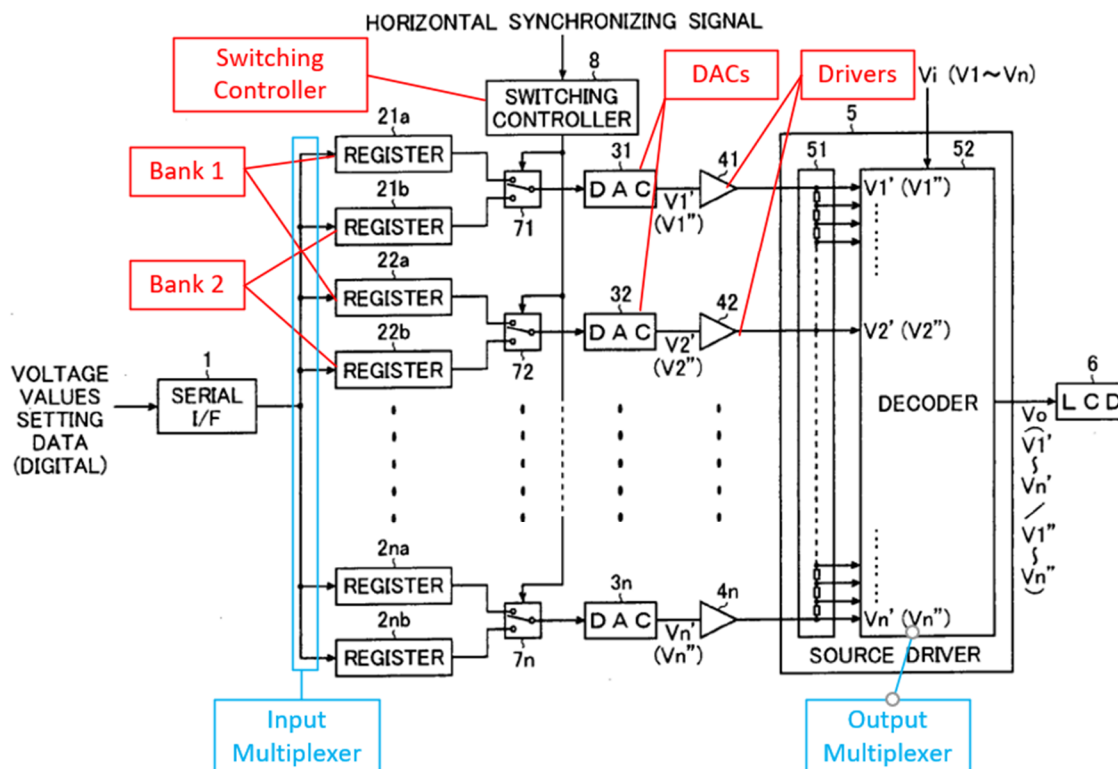
(EX1005, Fig. 3 (annotated)).

97. Nakata explicitly states that the output voltages V_1' to V_n' are gamma correction voltages used for driving a liquid crystal display. (EX1005, [0017]-[0019], Fig. 1). These gamma correction voltages determine the actual driving voltages applied to the LCD columns via the source driver 5. (EX1005, [0018]-[0019], Fig. 1).

6. Limitation 1[5]: wherein said non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and

98. Nakata discloses wherein said non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition. Specifically, Nakata describes

embodiments with multiple sets of registers (e.g. 21a/21b to 2na/2nb), where each set holds a different pattern of digital data for generating gamma correction voltages. (EX1005, [0021]-[0027], Figs. 2-3). These are labeled below as Bank 1 and Bank 2:

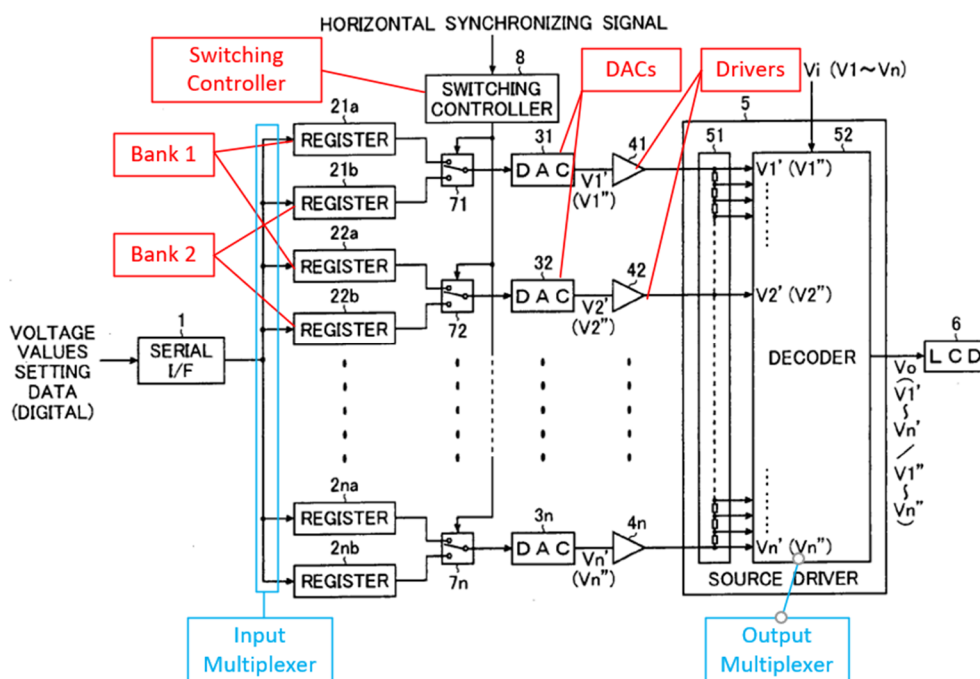


(EX1005, Fig. 3 (annotated)).

99. Each register set corresponds to a bank of storage cells containing data for a predetermined gamma voltage pattern (display condition). Nakata teaches using these different patterns for various display conditions, such as odd vs. even scanlines. (EX1005, [0024]). A POSITA would understand the register sets to be organized banks of non-volatile storage cells as claimed.

7. Limitation 1[6]: means to switch between the banks based on one or more external signals is provided on said integrated circuit.

100. Nakata discloses means to switch between the banks based on one or more external signals provided on said integrated circuit. Specifically, Nakata describes a switching controller 8 that controls selectors 71 to 7n to switch between different sets (banks) of registers. (EX1005, [0022]-[0024], Fig. 2). The switching controller 8 switches banks based on scanline information, which is an external signal indicating which scanline is being driven. (EX1005, [0024]). This can be seen below in Fig. 3, labeled “Switching Controller”:



(EX1005, Fig. 3 (Annotated)).

101. While not explicitly stated, a POSITA would understand the switching controller to be part of the same integrated gamma correction voltage generation device, as integrating all components on a single chip was standard practice for display driver circuits at the time. (EX1005, [0029]-[0031]).

B. Claim 2: The integrated circuit of claim 1 wherein said non-volatile storage cells are reprogrammable.

102. Nakata discloses that the non-volatile storage cells are reprogrammable. Specifically, Nakata teaches that the digital data held in registers 21 to 2n can be rewritten while checking the LCD image in real time. (EX1005, [0019]). Nakata further states that the registers can be implemented as non-volatile memories to easily store corrected values without a separate memory device. (EX1005, [0028]). A POSITA would understand from these disclosures that Nakata's registers are non-volatile reprogrammable storage cells for holding gamma correction data that can be repeatedly updated as needed to optimize display performance.

C. Claim 3: The integrated circuit of claim 2 wherein said means to switch between banks can have a switching time from about 10 msec to about one second.

103. A POSITA would understand that Nakata discloses the claimed switching time range. Nakata describes switching between register banks on a per-scanline basis using switching controller 8 and selectors 71-7n. (EX1005, [0022]-[0024], Fig. 2). While not explicitly stating a time, switching every few scanlines

at typical display refresh rates (e.g. 60 Hz) would fall within the claimed 10 ms to 1 second range. Additionally, Nakata's goal of enhancing image quality (EX1005, [0024]) implies switching fast enough to be imperceptible, which a POSITA would understand to be within the claimed range given standard display timing parameters.

D. Claim 4: The integrated circuit of claim 1 wherein said non-volatile storage cells hold analog voltage values which are a constant fraction of said gamma reference voltage signals.

104. A POSITA would understand that Nakata discloses non-volatile storage cells holding analog voltage values that are a constant fraction of the gamma reference voltage signals. While Nakata describes the registers storing digital data (EX1005, [0017-0019]), a POSITA would recognize this digital data directly represents specific analog voltage levels to be output by the DACs. (EX1005, Fig. 1). Since the DAC outputs are amplified by the buffers to produce the final gamma correction voltages (EX1005, [0017]), the analog values represented by the register data are necessarily a constant fraction (scaled-down version) of the output gamma voltages. Therefore, Nakata's registers hold analog voltage values that are a constant fraction of the gamma reference signals.

E. Claim 5: The integrated circuit of claim 1 wherein said circuits for programming require an external source for the high voltage programming means.

105. A POSITA would understand that Nakata discloses circuits for programming that require an external source for high voltage programming. While Nakata does not explicitly state this, programming non-volatile memory typically requires higher voltages than normal operating voltages. Nakata teaches storing the register data in non-volatile memory after adjustments are completed. (EX1005, [0019]). A POSITA would recognize that programming this non-volatile memory would require an external high voltage source, as this is standard practice for integrated circuits with on-chip non-volatile memory. The serial interface for programming the registers would necessarily include circuitry to interface with this external high voltage source for programming the non-volatile memory. (EX1005, Fig. 1, [0017-0019]).

F. Claim 8

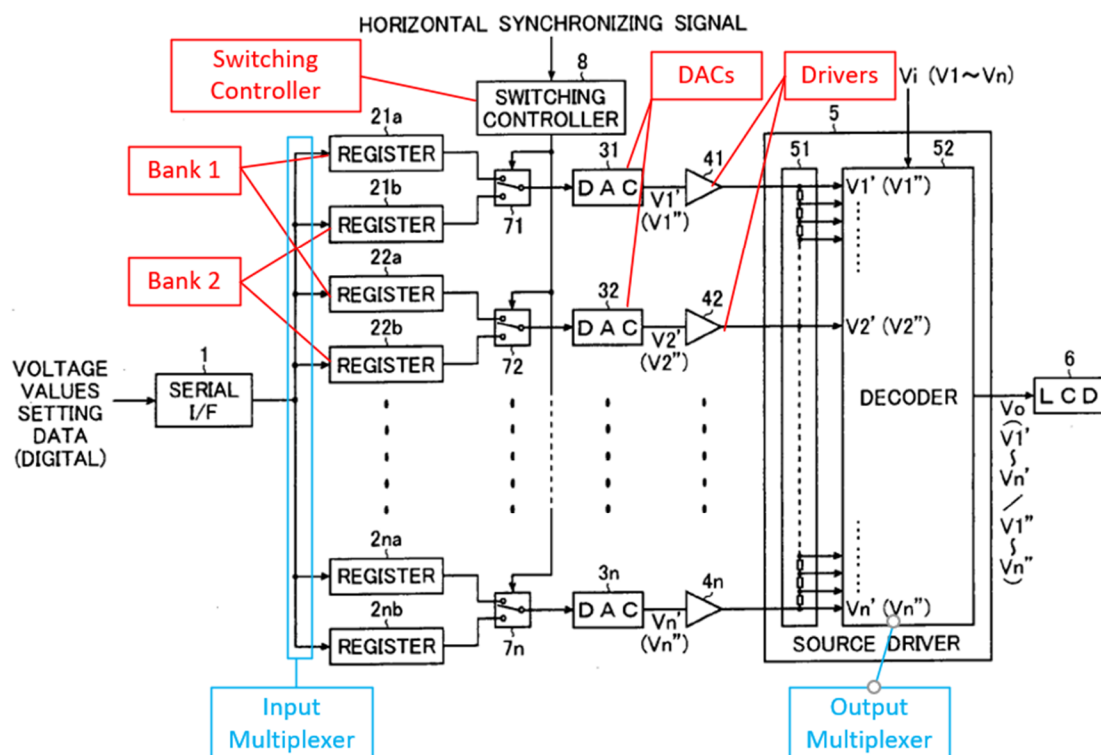
1. Limitations 8[0]-8[4]

106. Limitations 8[0]-8[4] are substantially identical to limitations 8[0]-8[4], and are disclosed in Nakata, as described *supra*, at § XI.A.1-5.

2. Limitation 8[5]: an output pin connected to an output through a second multiplexer connected to said plurality of outputs wherein said output pin is at an output buffer voltage level of said output when said integrated circuit is in a programming mode to program said storage for said output.

107. Nakata this limitation. (EX1005, [0018]). Specifically, Nakata describes a source driver 5 comprising a decoder 52 that selects and outputs a voltage V_o from among the gamma correction voltages V_1' to V_n' or intermediate

voltages generated by the resistance ladder 51. (EX1005, Fig. 1, [0018]). The decoder 52 corresponds to the claimed "second multiplexer." (EX1005, [0018]). This is because the decoder 52 couples one of many input voltages (V_1' to V_n' or intermediate voltages) to one output voltage V_o . (EX1005, [0018]). The output voltage V_o is provided to the LCD 6, which requires an output pin, and this output pin would be at the voltage level of the selected gamma correction voltage or intermediate voltage when the device is in a mode for programming the gamma correction values stored in the registers. (EX1005, [0019]). This is labeled as "Output Multiplexer" in the figure below:



(EX1005, Fig. 3 (annotated)).

108. Therefore, Nakata discloses all elements of the claimed limitation. (EX1005, Fig. 1, [0018]-[0019]).

A. Claim 9

109. Claim 9 is substantially identical to Claim 2. Nakata discloses the features of Claim 9, as described *supra*, at § XI.B.

B. Claim 10

110. Claim 10 is substantially identical to limitations 1[5]-1[6]. Nakata, in view of Tsai, discloses these features, as described *supra*, at § XI.A.6-7.

C. Claim 11

111. Claim 11 is substantially identical to Claim 3. Nakata, in view of Tsai discloses these features, as described *supra*, at § XI.A.6-7.

D. Claim 12

112. Claim 12 is substantially identical to limitation 1[4]. Nakata, in view of Tsai, discloses these features, as described *supra*, at § XI.A.5.

E. Claim 13

113. Claim 13 is substantially identical to Claim 4. Nakata, in view of Tsai, discloses these features as described *supra*, at § XI.D.

F. Claim 14

114. Claim 14 is substantially identical to Claim 5. Nakata discloses these features as described *supra*, at § XI.E.

XII. Ground 2: Claims 1-5, and 8-14 are Invalid as Obvious over Nakata, in view of Tsai

115. A POSITA would have been motivated to combine Nakata with Tsai to arrive at the claimed features. Specifically, a POSITA would have been motivated to modify Nakata's gamma correction voltage generation device to incorporate Tsai's partitioned memory architecture with a loader block and user block. This modification would have been obvious to try, as it would provide a known solution to the problem of efficiently reprogramming gamma correction data. (EX1007, 2:38-43)

116. Nakata discloses the need to rewrite gamma correction data while checking display output in real-time. (EX1005, [0019]) However, Nakata does not provide details on how to implement this reprogramming efficiently. Tsai's partitioned memory architecture, with a loader block for storing a loader program and a user block for application data, offers a predictable solution to this problem. (EX1007, 3:5-13) A POSITA would recognize that incorporating Tsai's memory architecture into Nakata's device would allow for efficient reprogramming of gamma correction data without external tools, while maintaining normal display operation. (EX1007, 2:38-3:4)

117. Furthermore, a POSITA would be motivated to implement Tsai's switching mechanism between memory blocks in Nakata's device. Tsai teaches using memory selection (MSEL) and bus selection (BSEL) signals to control

which memory block is active. (EX1007, 7:49-67) This technique could be readily applied to Nakata's multiple register sets to enable dynamic switching between gamma correction patterns, improving upon Nakata's existing selector mechanism. (EX1005, [0022]-[0024]) This modification would be a use of a known technique to improve a similar device, yielding the predictable result of more flexible gamma correction control.

118. The combination would also benefit from Tsai's teaching of using a timer and interrupt system for managing the reprogramming process. (EX1007, 4:41-5:21) Implementing this feature in Nakata's device would allow for precise timing control when switching between gamma correction patterns, ensuring smooth transitions and enhanced image quality as desired by Nakata. (EX1005, [0024]) This modification would be applying a known technique to a known device ready for improvement to yield predictable results.

119. A limitation-by-limitation analysis of Nakata is provided *supra*, at § XI. A limitation-by-limitation analysis of Tsai is provided below.

A. Claim 1

1. Limitation 1[0]

120. To the extent that the preamble is limiting, Tsai also discloses an integrated circuit for producing voltage signals on a plurality of outputs. Tsai describes a microcomputer implemented as an integrated circuit that includes a

microprocessor unit and embedded flash memory for generating and outputting voltage signals. (EX1007, 2:14-28, Fig. 3) The microcomputer produces gamma reference voltages, which are voltage signals, on multiple outputs to drive source drivers for a display. (EX1007, 1:19-27, 3:1-6, Fig. 3) Figure 3 shows the integrated circuit architecture with multiple output channels (CH0-CH7) for outputting the voltage signals. (EX1007, Fig. 3)

2. Limitation 1[1]

121. Tsai discloses a plurality of non-volatile storage cells. Tsai describes an embedded flash memory unit within the microcomputer. (EX1007, 1:24-33, 3:5-22, Fig. 2). Flash memory is a type of non-volatile memory that retains data without power. A POSITA would have recognized that an embedded flash memory unit necessarily comprises multiple non-volatile storage cells to store data and programs, as individual storage cells are the fundamental building blocks of flash memory. The loader block and user block described by Tsai (EX1007, Fig. 2) would each require numerous storage cells to store their respective programs.

3. Limitation 1[2]

122. Tsai discloses circuits for programming coupled to a multiplexer for addressing and programming storage cells, with addressing based on a plurality of inputs. Tsai describes a microprocessor unit 310 coupled to a bus multiplexer 350 that addresses and programs the loader block 331 and user block 332 of the flash

memory 330 during data reprogramming. (EX1007, 3:2-9, Fig. 3). The addressing is controlled by signals from the microprocessor unit, including a memory selection signal MSEL and bus selection signal BSEL, which determine which block is active and connected to the register set 340 for programming. (EX1007, 3:14-19, 7:49-67, Fig. 3). The MSEL and BSEL signals, along with address values stored in the address register 342, constitute the plurality of inputs for addressing. (EX1007, 3:14-19, 7:41-48, Fig. 3).

4. Limitation 1[3]

123. A POSITA would have understood that Tsai discloses drivers connected to the storage cells and outputs. Tsai describes a microprocessor unit that manages data flow between a register set and flash memory blocks during programming and execution modes. (EX1007, 7:49-67, 8:37-47, Fig. 3). A POSITA would have recognized that drivers are necessary components to interface between the microprocessor and flash memory for reading and writing operations. The drivers are present to buffer and amplify signals between the storage cells in the flash memory and the outputs to the microprocessor and register set, enabling the described data transfer functionality. (EX1007, Fig. 3).

5. Limitation 1[4]

124. Tsai does not expressly disclose gamma reference voltage signals for determining driving voltages of display columns. However, a POSITA would have

found it obvious to adapt Tsai's programmable voltage generation system for this purpose. Tsai discloses an integrated circuit that produces programmable voltage signals on multiple outputs using non-volatile storage cells and drivers. (EX1007, Fig. 3, 3:2-9, 7:10-19) A POSITA would have recognized this architecture could be readily applied to generate gamma reference voltages, which are simply a set of programmable voltages used to drive display columns. The ability to program and store multiple voltage values in Tsai's system (EX1007, 3:23-29) aligns well with the needs of gamma correction, where different voltage levels are required for optimal display performance.

6. Limitation 1[5]

125. Tsai discloses that the non-volatile storage cells are organized into two or more banks. Specifically, Tsai describes partitioning the embedded flash memory into a loader block and a user block. (EX1007, 3:5-13, Fig. 2). The loader block stores a loader program, while the user block stores application programs. (EX1007, 3:14-16, Fig. 2). A POSITA would have understood that these blocks to be analogous to banks containing predetermined display conditions, as the loader and application programs define different operational states of the display system. The blocks can be separately addressed and accessed to retrieve their respective programs for execution. (EX1007, 3:35-47, Fig. 3).

7. Limitation 1[6]

126. Tsai discloses a means to switch between banks based on external signals provided on the integrated circuit. Specifically, Tsai describes a bus multiplexer that selectively connects either the loader block or user block to the microprocessor or register set based on external signals MSEL and BSEL from the microprocessor unit. (EX1007, 3:23-42, 7:49-67, Fig. 3). The MSEL signal selects which memory block is active, while BSEL controls the bus multiplexer connections. (EX1007, Fig. 3). This switching mechanism allows the microcomputer to alternate between executing the loader program and writing new data to the user block during on-chip programming. (EX1007, 7:49-67).

B. Claim 2

127. Tsai discloses that the non-volatile storage cells are reprogrammable. Tsai describes a microcomputer with embedded flash memory that has “on-chip programming capability that allows new data to be reprogrammed by the microcomputer itself into the embedded flash memory” (EX1007, Abstract). The flash memory is partitioned into a loader block and a user block, where the user block stores application programs that can be updated through reprogramming (EX1007, 2:62-3:6, Fig. 2). Tsai details a method for reprogramming data into the flash memory, including receiving new data, temporarily storing it, and writing it into the memory blocks (EX1007, 4:41-57, Fig. 5). This on-chip reprogramming capability is a key feature that allows updating the stored programs without

external tools, clearly indicating the reprogrammable nature of the non-volatile storage cells.

C. Claim 3

128. A POSITA would have found it obvious to configure Tsai's switching time between banks to be from about 10 msec to about one second. While Tsai does not expressly disclose this specific time range, Tsai teaches using a timer to control switching between memory blocks during programming. (EX1007, 4:41-5:21, Fig. 4). Tsai explains that the timer is set based on the time required to program one block of data. (EX1007, 8:30-37). A POSITA would have understood that flash memory programming typically takes on the order of milliseconds to seconds per block, and would have found it obvious to set Tsai's timer within the claimed range to allow sufficient time for programming while maintaining responsive operation. The claimed range represents a straightforward optimization of Tsai's disclosed timing mechanism based on typical flash memory characteristics known to POSITAs.

D. Claim 4

129. A POSITA would have understood that Tsai, in combination with Nakata, discloses non-volatile storage cells holding analog voltage values which are a constant fraction of gamma reference voltage signals. Tsai teaches an embedded flash memory unit partitioned into blocks for storing program data

(EX1007, 6:15-26, Fig. 3). When incorporated into Nakata, the flash memory unit of Tsai would hold values that are analog voltage values which are a constant fraction of a gamma correction value. Specifically, the digital values would be constant, and would correlate to a fraction of a gamma correction value, such that when the digital values are converted to analog values (i.e. by a DAC), it would be a fraction of the gamma reference voltage applied to the DAC. While Tsai does not explicitly describe storing analog voltages, a POSITA would have recognized that flash memory cells store analog charge levels that correspond to discrete digital values. In the context of gamma reference generation for displays, these stored analog levels would necessarily represent fractions of the full gamma reference voltage range. Therefore, the non-volatile cells in Tsai hold analog voltages that are constant fractions of gamma reference signals when used for this purpose.

1. Limitations 8[0]-8[4]

130. Limitations 8[0]-8[4] are substantially identical to limitations 1[0]-1[4]. Nakata, in view of Tsai, discloses these features, as described *supra*, at § X.A.1-5, XI.A.1-5.

2. Limitation 8[5]: an output pin connected to an output through a second multiplexer connected to said plurality of outputs wherein said output pin is at an output buffer voltage level of said output when said integrated circuit is in a programming mode to program said storage for said output.

131. Nakata discloses this feature. *See supra*, § XI.F.2.

E. Claim 9

132. Claim 9 is substantially identical to Claim 2. Nakata, in view of Tsai further discloses the features of Claim 9, as described *supra*, at § XI.B., XII.B

F. Claim 10

133. Claim 10 is substantially identical to limitations 1[5]-1[6]. Nakata, in view of Tsai, discloses these features, as described *supra*, at § XI.A.6-7, XII.A.6-7.

G. Claim 11

134. Claim 11 is substantially identical to Claim 3. Nakata, in view of Tsai discloses these features, as described *supra*, at § XI.A.6-7, XII.A.6-7.

H. Claim 12

135. Claim 12 is substantially identical to limitation 1[4]. Nakata, in view of Tsai, discloses these features, as described *supra*, at § XI.A.5, XII.A.5.

I. Claim 13

Claim 13 is substantially identical to Claim 4. Nakata, in view of Tsai, discloses these features as described *supra*, at § XI.D, XII.D.

J. Claim 14

136. Claim 14 is substantially identical to Claim 5. Nakata discloses these features as described *supra*, at § XI.E.

XIII. Ground 3: Claims 1-5, and 8-14 are Invalid as Obvious over Petropoulos

137. Claims 1-5, and 8-14 are invalid as obvious over Petropoulos. Below is a limitation-by-limitation analysis of Petropoulos, showing where each limitation is found in the prior art.

A. Claim 1

1. Limitation 1[0]

138. Petropoulos discloses a circuit for processing analog signals received from a sensor before outputting the signals to a display or other device. (EX1006 at Abstract). Petropoulos teaches that “[t]he memory array can be programmed with data corresponding to desired modifications, such as low and high offset voltage correction, low gain correction, and gamma correction.” (EX1006 at Abstract). Petropoulos does not explicitly teach that the correction circuitry is integrated onto a single chip, though it does state that the circuitry is “coupled,” (see EX1006 at Claim 9), and it would have been obvious to a POSITA to include the components on a single integrated circuit, because otherwise electrical noise would make high-fidelity output difficult, if not impossible, to achieve. Given Petropoulos’ teaching that “the quality of the reproduced image is particularly important especially in high-end imaging applications,” a POSITA would have been motivated to implement the system of Petropoulos on a single integrated circuit.

2. Limitation 1[1]

139. Petropoulos discloses “a plurality of non-volatile storage cells.” Specifically, Petropoulos describes an “analog/multi-level memory array” containing multiple “memory cells” that retain stored data even when power is removed. (EX1006, 3:9-19, 5:19-28, Fig. 3). These non-volatile memory cells are used to store modification voltages for adjusting sensor array outputs. (EX1006, 4:11-25). Figure 3 shows a memory array 210 with MxN memory cells C11 to CMN, each implemented as a non-volatile floating gate transistor. (EX1006, 5:19-28, Fig. 3). A POSITA would have understood these cells retain their stored analog values when powered off, meeting the non-volatile storage cell limitation.

3. Limitation 1[2]

140. Petropoulos discloses an address signal generator which “provides address signals indicating a row address and a column address for a selected one of memory cells C11 to CMN to which the data value will be written.” (EX1006 at [0031]). A POSITA would have understood that this circuit for programming and addressing storage cells is necessarily based on multiple inputs. (See EX1006 at Fig. 3). Petropoulos teaches that the address signal generator “can be a buffer circuit that generates the address signals from address [sic] provided by circuitry external to memory 300, or . . . can generate sequential addresses for recording analog or multi-level samples of a continuous analog signal.” (EX1006 at [0031]). A POSITA would have understood that the addressing is based on a plurality of

inputs to select any memory cell, and that the decoder tree and other elements within the memory are circuits for programming.

4. Limitation 1[3]

141. Petropoulos discloses a multiplier circuit that applies gamma voltages to the sensor data connected to the memory array, which stores gamma correction values. (EX1006 at Fig. 7, [0050]). The multiplier circuit includes an op amp, which a POSITA would understand is a driver because it “multiplies the input voltage V_s from individual sensor elements in the image sensor by a corresponding gamma correction factor V_{gc} stored in the gamma correction memory array.” (EX1006 at [0050]).

5. Limitation 1[4]

142. As discussed above, Petropoulos discloses an address signal generator that selects where data is written into the storage cells. (EX1006 at [0031]). Petropoulos describes a plurality of inputs connected to a decoder tree which accepts multiple inputs from the address signal generator to address the storage cells. (EX1006 at Fig. 4). Petropoulos teaches that “[w]hen writing a data value, an address signal generator 320 provides address signals indicating a row address and a column address for a selected one of memory cells C_{11} to C_{MN} to which the data value will be written. (EX1006 at [0031]). A POSITA would understand that the use of the plural (i.e., signals), indicates the use of a plurality of inputs.

143. Petropoulos also teaches that the correction signals can be gamma correction values for gamma correction of visual displays. (EX1006 at [0026]). These gamma correction factors are voltages V_{gc} which are combined with the signal voltage V_s by the op amp. (See EX1006 at Fig. 7, [0050]). Because the resultant voltages are output to a visual display device, a POSITA would have understood that these gamma correction factors are used to determine actual driving voltages for columns of the display.

Limitation 1[5]

144. Petropoulos discloses “a plurality of memory arrays 210, each being programmed and stored with voltages for a different modification function, [so that] a variety of modifications to the sensor element voltages can be performed.” (EX1006 at [0051]). Petropoulos further describes other embodiments in which “a single analog/multi-level memory array can be used in conjunction with a decoder for multiple types of modifications.” (EX1006 at [0053]). Petropoulos teaches that in these embodiments, the decoder “determines the type of modification for a particular voltage from an image sensor element and accesses the desired voltage from the memory array,” then supplies the voltages to the appropriate modification circuit. (*Id.*). A POSITA would have understood that multiple memories, or multiple types of modifications within a single memory, correspond to multiple banks of storage cells because different levels correspond to different groups, *i.e.*,

banks. Moreover, a POSITA would have understood that these types of memory could be used for display gamma correction.

Limitation 1[6].

145. Petropoulos discloses the use of a decoder to access the desired voltage from a memory array. (EX1006 at [0053]). Petropoulos teaches that “a desired one of the memory arrays 210 is selected for a particular modification.” (EX1006 at [0051]). A routing circuit 220 selects the desired modification. (EX1006 at [0027]). A POSITA would have understood that a decoder, which selects a location in the memory array, is a means to switch between the banks based on external signals, *i.e.*, the routing circuit.

B. Claim 2

Petropoulos discloses that the non-volatile storage cells, *i.e.*, the memory arrays, “can be reprogrammed.” (EX1006 at [0054]).

C. Claim 3

146. A POSITA would have found it obvious to implement the switching time between banks in Petropoulos to be from about 10 msec to about one second based upon the POSITA’s knowledge that such a switching would be unnoticeable by the viewer of the display. While Petropoulos does not explicitly specify a switching time, it discloses reprogrammable memory arrays that can be updated to correct sensor outputs over time (EX1006, 2:64-3:8, 9:44-51). A POSITA would have understood that switching between banks too quickly could cause display

artifacts, while switching too slowly would be inefficient and may impact display quality. Therefore, a POSITA would have been motivated to implement a switching time in the claimed range to balance smooth transitions with responsiveness, which represents a routine optimization within the prior art. Specifically, a POSITA could have used a low-pass filter – a common and well-understood component in electronic systems – to effectively filter out the harsh transition between banks.

D. Claim 4

147. A POSITA would have understood that Petropoulos discloses non-volatile storage cells holding analog voltage values which are a constant fraction of gamma reference voltage signals. Petropoulos teaches using an analog/multi-level memory array to store voltages for gamma correction of display signals. (EX1006, 2:64-3:8, 4:11-25, Fig. 7). A POSITA would have recognized that gamma correction typically involves multiplying input voltages by constant fractional values to achieve the desired non-linear response. Thus, the analog voltages stored in Petropoulos' memory for gamma correction would necessarily be constant fractions of the gamma reference voltages in order to properly perform the gamma correction function when multiplied with the input signals.

E. Claim 5

148. Petropoulos discloses a programming voltage V_{pp} that is used to program voltages into the memory. (EX1006 at [0032]). Petropoulos also teaches that “[i]f memory array 210 is a Flash memory array, typical programming voltages V_{pp} and V_{dp} are respectively about 12 volts and about 6 volts above voltage V_{ss} . (Id.). A POSITA would have understood that these voltage levels are high voltages. Moreover, it would have been obvious to a POSITA to supply the voltage using an external source. (See EX1006 at Fig. 3).

Claim 8

1. Limitations 8[1]-8[4]

Limitations 8[0] to 8[4] are identical to Limitations 1[0] to 1[4]. Petropoulos discloses these features. *See supra*, § XIII.B.1-5.

2. Limitation 8[5]

149. While Petropoulos does not expressly disclose an output pin connected through a second multiplexer to the plurality of outputs, a POSITA would have found this limitation obvious. Petropoulos teaches using a decoder to selectively route sensor outputs and stored modification values to a modification circuit. (EX1006, 9:38-47, Fig. 8). A POSITA would have understood that implementing this selective routing functionality with a multiplexer connected to an output pin would have been an obvious and straightforward design choice to enable reading out the modified sensor values during programming. Using a multiplexer to selectively output signals was a well-known technique that a

POSITA would have readily applied to achieve the predictable result of selectively outputting the modified sensor values in Petropoulos' system.

F. Claim 9

150. Claim 9 is substantially identical to Claim 2, but differs only in that it depends from Claim 8, rather than Claim 1. Petropoulos further discloses the features of Claim 9, as described *supra*, at § XIII.B.

G. Claim 10

151. Claim 10 is substantially identical to limitations 1[5]-1[6]. Petropoulos discloses these features, as described *supra*, at § XIII.A.6-7.

H. Claim 11

152. Claim 11 is substantially identical to Claim 3. Petropoulos discloses these features, as described *supra*, at § XIII.A.6-7.

I. Claim 12

153. Claim 12 is substantially identical to limitation 1[4]. Petropoulos discloses these features, as described *supra*, at § XIII.A.5.

J. Claim 13

Claim 13 is substantially identical to Claim 4. Petropoulos discloses these features as described *supra*, at § XIII.D.

K. Claim 14

154. Claim 14 is substantially identical to Claim 5. Nakata discloses these features as described *supra*, at § XIII.E.

XIV. Ground 4: Claims 1-5, and 8-14 are Invalid as Obvious over Petropoulos in view of Tsai

155. In the event that the Board finds that Ground 2 is insufficient to show the claimed multiplexer, it is my opinion that Tsai, in combination with Petropoulos, renders obvious the claimed multiplexer. Specifically, a POSITA would have been motivated to incorporate Tsai's bank switching mechanism into Petropoulos' system to enable dynamic selection between multiple sets of gamma correction values. This modification would have been obvious to try, as it would provide the predictable benefit of allowing Petropoulos' system to efficiently switch between different gamma correction curves for various display conditions or user preferences. (EX1006, 2:29-35; EX1007, 3:23-42, 7:49-67; EX1003, ¶ 124).

156. Each of the limitations of the challenged claims are present in Petropoulos, as described *supra*, at § XIII, or in Tsai, as described *supra*, at XII.

XV. Ground 5: Claims 1-5, and 8-14 are Invalid over Nakata, in view of Tsai, in further view of Yamazaki

157. In the event that the Board finds that Ground 1 is insufficient because the combination of Nakata and Tsai does not adequately disclose nonvolatile storage cells, it is my opinion that Yamazaki, which expressly discloses such storage cells, does.

158. A POSITA would have been motivated to combine Nakata with Tsai and Yamazaki to arrive at the claimed features. Specifically, a POSITA would have been motivated to modify Nakata's gamma correction voltage generation device to incorporate the multiple banks of non-volatile storage cells and switching means disclosed in Tsai and Yamazaki.

159. Nakata teaches storing gamma correction data in registers that can be implemented as non-volatile memory. (EX1005, [0028]). However, Nakata lacks explicit disclosure of multiple banks of storage cells. A POSITA would have been motivated to incorporate Tsai's teaching of partitioning memory into multiple blocks, each containing different display conditions, as this would allow for storing multiple gamma correction profiles. (EX1007, 3:5-13). This modification would have been a simple substitution of Tsai's partitioned memory structure for Nakata's single set of registers, yielding the predictable result of increased flexibility in gamma correction.

160. Furthermore, a POSITA would have been motivated to incorporate Yamazaki's teaching of storing multiple sets of gamma correction data and switching between them based on external signals. (EX1008, 7:21-26, 19:35-55). This modification would allow Nakata's device to dynamically adjust gamma correction based on different display conditions, improving image quality. The combination would have been obvious to try, as there are a finite number of ways

to implement multiple gamma correction profiles, and Yamazaki's approach provides clear benefits.

161. Regarding the switching time, while not explicitly disclosed, a POSITA would have found it obvious to implement a switching time between 10 msec and 1 second. Tsai teaches using a timer and interrupt system for memory operations (EX1007, 4:41-5:21), and Yamazaki discloses a high-speed integrated design (EX1008, 19:56-65). A POSITA would have recognized that implementing switching within the claimed range would balance system responsiveness and power efficiency, applying known techniques to yield predictable results.

162. These modifications to Nakata would have been straightforward applications of known techniques in display driver circuits, motivated by the desire to improve display quality and flexibility in gamma correction.

163. A limitation-by-limitation analysis of Nakata and Tsai is provided *supra*, at § XI, XII, and is not repeated here. Below is an analysis of where in Yamazaki each limitation is found.

A. Claim 1

1. Limitation 1[0]

164. Yamazaki discloses an integrated circuit for producing voltage signals on a plurality of outputs. Yamazaki describes a semiconductor display device correcting system that includes a control circuit, memory elements, and other

components for gamma correction integrally formed on an insulating substrate. (EX1008, 8:6-24, Fig. 7B) This integrated system produces voltage signals on multiple outputs to drive the display pixels. (EX1008, 5:60-6:9) Specifically, Yamazaki discloses that the gamma correction control circuit outputs corrected voltage signals to a source signal line side driver, which then selects corresponding pixel TFTs to write picture information. (EX1008, 6:3-9, Fig. 1) This demonstrates an integrated circuit producing voltage signals on multiple outputs to drive the display.

2. Limitation 1[1]

165. Yamazaki discloses a plurality of non-volatile storage cells. Specifically, Yamazaki describes a nonvolatile memory composed of FAMOS type TFTs with floating gates for storing gamma correction data. (EX1008, 8:16-34, 9:16-17) The memory includes multiple storage elements arranged in a matrix, with each element comprising a P-channel FAMOS TFT and an N-channel switching TFT. (EX1008, 8:16-34, Fig. 3) This matrix arrangement of multiple non-volatile memory elements clearly constitutes a plurality of non-volatile storage cells as claimed.

3. Limitation 1[2]

166. Yamazaki discloses circuits for programming coupled to a multiplexer for addressing and programming storage cells based on multiple inputs. The

gamma correction control circuit 102 interacts with nonvolatile memory 103 to adjust voltage levels based on input signals. (EX1008, 5:60-6:9, Fig. 1). This process involves addressing and programming memory cells. The system uses multiple inputs, including digital picture signals from signal generator 101 and feedback signals from digital signal processor 108, to control the addressing and programming. (EX1008, 6:39-46, Fig. 1). The X-address decoder 301 and Y-address decoder 302 act as multiplexers to select specific memory elements for programming based on these inputs. (EX1008, 8:43-49, Fig. 3).

4. Limitation 1[3]

167. Yamazaki discloses drivers connected to storage cells and to the plurality of outputs. Specifically, Yamazaki describes a source signal line side driver 104 and gate signal line side driver 105 that are connected to the nonvolatile memory 103 (storage cells) and to the pixel region 106 (plurality of outputs). (EX1008, Fig. 1, 6:10-28) The source and gate drivers receive gamma-corrected signals from the gamma correction control circuit 102, which retrieves data from the nonvolatile memory 103, and provide those signals to drive the pixels in the pixel region 106. (EX1008, 6:14-28) This configuration directly connects the drivers to both the storage cells and outputs as claimed.

5. Limitation 1[4]

168. Yamazaki discloses the plurality of inputs connected to said multiplexer for addressing said storage cells, wherein said voltage signals are gamma reference voltage signals for determining actual driving voltages of columns of a display. Yamazaki describes a gamma correction control circuit 102 connected to a nonvolatile memory 103 via a multiplexer, where the memory stores gamma correction data used to adjust voltage levels for driving display columns. (EX1008, Fig. 1, 5:60-6:9). The gamma correction control circuit 102 uses inputs to address the storage cells in memory 103 to retrieve the appropriate gamma correction data. (EX1008, 6:10-28). This gamma correction data is then used to generate gamma reference voltages that determine the actual driving voltages applied to the display columns via the source signal line side driver 104. (EX1008, Fig. 1, 6:29-46). I realize we don't have much time, but pictures are useful.

6. Limitation 1[5]

169. Yamazaki discloses non-volatile storage cells organized into two or more banks, each containing a predetermined gamma reference voltage signal display condition. Yamazaki teaches storing "multiple sets of gamma values" to "provide optimized gamma correction curves for different user or application requirements." (EX1008, 2:24-28). These multiple sets correspond to banks of cells, each set providing gamma correction for a different display condition.

Yamazaki further discloses that “when all gamma correction data of gradation signals are stored in the memory 103, the signal generator 101 and the digital signal processor 108 are detached from the liquid crystal panel.” (EX1008, 5:60-63, Fig. 1). This indicates the gamma correction data is organized into multiple sets (banks) in the non-volatile memory 103, allowing different gamma corrections to be applied for various display conditions without external components.

7. Limitation 1[6]

170. Yamazaki does not expressly disclose means to switch between banks based on external signals. However, a POSITA would have found this limitation obvious in view of Yamazaki’s teachings. Yamazaki discloses storing multiple sets of gamma correction data in nonvolatile memory to provide different gamma correction curves for different requirements. (EX1008, 2:24-28, Fig. 3). A POSITA would have understood that to utilize these different stored gamma curves, some means of switching between them based on external signals (e.g. user input or sensor data) would be necessary and obvious to implement on the integrated circuit. This would allow dynamically selecting the appropriate gamma correction for different display conditions or user preferences, as suggested by Yamazaki. (EX1008, 7:20-32).

B. Claim 2

171. Yamazaki discloses that the non-volatile storage cells are reprogrammable. Yamazaki describes a nonvolatile memory comprised of FAMOS (Floating gate Avalanche injection MOS) type TFTs for storing gamma correction data. (EX1008, 8:16-34, Fig. 3) A POSITA would have understood that FAMOS cells are reprogrammable due to their floating gate structure, which allows electrical erasure and reprogramming. Yamazaki further confirms the reprogrammable nature by stating that the storage content of the memory elements “can be erased by irradiation of X-rays, ultraviolet rays, or electron beams, or by application of heat.” (EX1008, 9:9-12) This disclosure of erasure methods indicates the ability to reprogram the non-volatile storage cells.

C. Claim 3

172. A POSITA would have understood that Yamazaki discloses a means to switch between banks with a switching time from about 10 msec to about one second based upon the POSITA’s knowledge that such a switching would be unnoticeable by the viewer of the display. Yamazaki describes integrating a control circuit, nonvolatile memory, and volatile memory on the same substrate to enable “high speed operations” when switching between stored gamma correction data banks. (EX1008, 19:21-34, 19:35-55, 19:56-65). While a specific switching time is not explicitly stated, a POSITA would have recognized that integrating these components on a single substrate to achieve “high speed operations” necessarily

results in switching times within the claimed 10 msec to 1 second range, which was typical for such integrated memory systems at the time of the invention.

D. Claim 4

173. A POSITA would have understood that Yamazaki discloses that the non-volatile storage cells hold analog voltage values which are a constant fraction of the gamma reference voltage signals. Yamazaki discloses that the nonvolatile memory stores gamma correction data used to adjust voltage levels corresponding to image gradations. (EX1008, 3:30-37, 3:52-4:5). The stored gamma correction data represents analog voltage values that are constant fractions of the gamma reference voltages, as this is necessary to achieve the desired gradation adjustments across the full range of reference voltages. A POSITA would have recognized that storing fractional values, rather than absolute voltages, allows the system to flexibly apply gamma correction across different voltage ranges.

E. Claim 5

174. Yamazaki discloses that the circuits for programming require an external source for the high voltage programming means. Specifically, Yamazaki describes that during the writing operation of the memory element, “a high voltage of 50 V is applied to the signal line C1.” (EX1008, 8:54-61). This disclosure of applying a high 50V signal implies the necessity of an external high voltage source, as such a high voltage would not be internally generated within the

integrated circuit itself without special fabrication techniques. A POSITA would have understood that this externally-supplied high voltage is crucial for programming the nonvolatile memory cells described by Yamazaki. (EX1008, 9:6-9).

F. Claim 8

Limitation 8[0]-8[4]

Limitations 8[0] to 8[4] are identical to Limitations 1[0] to 1[4]. The combination of Nakata and Tsai disclose these features. *See supra*, § XI.A.1-5, XII.A.1-5.

1. Limitation 8[5]

175. Yamazaki does not expressly disclose an output pin connected to an output through a second multiplexer, wherein this output pin is at an output buffer voltage level of said output when the integrated circuit is in a programming mode. While Yamazaki discusses output interactions for driving display pixels and signal processing (EX1008, 6:47-57), it does not specifically describe the claimed output pin configuration with a second multiplexer. However, a POSITA would have found it obvious to implement such an output configuration to enable programming and verification of the nonvolatile memory cells while maintaining normal display output functionality. Adding a multiplexed output pin connected to the memory cell outputs would allow for efficient programming and readback without disrupting the display operation. (EX1008, Fig. 3, 6:22-36, 12:26-35)

G. Claim 9

176. Claim 9 is substantially identical to Claim 2. The combination of Nakata and Tsai disclose the features of Claim 9, as described *supra*, at § XI.B, XII.B.

H. Claim 10

177. Claim 10 is substantially identical to limitations 1[5]-1[6]. The combination of Nakata and Tsai disclose these features, as described *supra*, at § XI.A.6-7, XII.A.6-7.

I. Claim 11

178. Claim 11 is substantially identical to Claim 3. The combination of Nakata and Tsai discloses these features, as described *supra*, at § XI.A.6-7, XII.A.6-7.

J. Claim 12

179. Claim 12 is substantially identical to limitation 1[4]. The combination of Nakata and Tsai disclose these features, as described *supra*, at § XI.A.5, XII.A.5.

K. Claim 13

Claim 13 is substantially identical to Claim 4. The combination of Nakata and Tsai disclose these features as described *supra*, at § XI.D, XII.D.

L. Claim 14

180. Claim 14 is substantially identical to Claim 5. Nakata discloses these features as described *supra*, at § XI.E.

XVI. Ground 6: Claims 1-5, and 8-14 are Invalid as Obvious over Petropoulos in view of Yamazaki

181. In the event that the Board finds that Ground 2 is insufficient because Petropoulos does not adequately disclose memory cells stored in banks, it is my opinion that Yamazaki, which expressly discloses such storage cells, does. A POSITA would have been motivated to combine Petropoulos with Yamazaki to arrive at the claimed features. Specifically, a POSITA would have been motivated to modify Petropoulos to include means to switch between banks of gamma reference voltage signals based on external signals, as taught by Yamazaki. This modification would have been obvious to try, as it would allow dynamically selecting appropriate gamma correction for different display conditions or user preferences, providing optimized image quality. (EX1008, 2:24-28, 7:20-32) The combination would have yielded predictable results, as both references relate to gamma correction for displays using stored reference values. (EX1006, 2:29-35; EX1008, 5:60-6:9)

182. A limitation-by-limitation analysis of Petropoulos is provided *supra*, at § XIII, and a limitation-by-limitation analysis of Yamazaki is provided *supra*, at § XV, and they are not repeated here.

XVII. Ground 7: Claims 1-5, and 8-14 are Invalid as Obvious over Petropoulos in view of Tsai in further view of Yamazaki

183. In the event that the Board finds that Grounds 2 and/or 4 are insufficient on their own, it is my opinion that Petropoulos, in view of Tsai, in further view of Yamazaki overcomes these challenges. A motivation to combine Petropoulos with Tsai is provided above *supra*, at § XIV. A further motivation to combine Petropoulos with Yamazaki is provided above, *supra*, at § XV.

184. A limitation-by-limitation analysis of Petropoulos is provided *supra*, at § XIII, a limitation-by-limitation analysis of Tsai is provided *supra*, at § XII, and a limitation-by-limitation analysis of Yamazaki is provided *supra*, at § XV.

XVIII. Conclusion

185. In my opinion, claims 1-5 and 8-14 of the '305 Patent are invalid for at least the reasons stated above.

186. I reserve the right to supplement my opinions in the future to respond to any arguments raised by the owner of the '305 Patent and to take into account new information that becomes available to me.