

CASE IPR2018-01255
U.S. Patent No. 7,233,305

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WISTRON CORPORATION,
Petitioner,

v.

PHENIX LONGHORN, LLC,
Patent Owner.

CASE IPR2018-01255
U.S. Patent No. 7,233,305

PATENT OWNER'S PRELIMINARY RESPONSE TO PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,233,305
[REDACTED]

TABLE OF CONTENTS

TABLE OF ABBREVIATIONS.....	vvi
LIST OF EXHIBITS.....	vii
I. INTRODUCTION.....	1
II. FACTUAL BACKGROUND.	2
III. OVERVIEW OF THE TECHNOLOGY.....	4
A. The Problem To Be Solved.....	4
B. The Pioneering Work Of Alta Analog.	7
IV. U.S. PATENT NO. 7,233,305.	10
V. THE PETITION IS TIME BARRED UNDER 35 U.S.C. § 315(B).....	10
VI. LEGAL PRINCIPLES RELEVANT TO THE CHALLENGE.	16
A. Person Of Ordinary Skill In The Art.....	16
B. Claim Construction.....	17
1. “Non-volatile storage cells.”	17
2. “Means to switch between the banks based on one or more external signals.”	18
VII. GROUNDS 1-4 ARE IMPROPER BECAUSE THEY ASSERT OBVIOUSNESS BASED ON A SINGLE PRIOR ART REFERENCE.	19
VIII. NONE OF THE GROUNDS SHOW A REASONABLE LIKELIHOOD OF PREVAILING ON ANY CHALLENGED CLAIM.....	21
A. Ground 1: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Kang.	22

1. Kang does not disclose the preamble of claim 1.....	22
2. Kang does not disclose part [b] of claim 1.	23
3. Kang does not disclose part [d] of claim 1.	25
4. Kang does not disclose part [f] of claim 1.	26
5. Kang does not disclose part [g] of claim 1.	26
6. Kang does not disclose claim 2.....	27
7. Kang does not disclose claim 4.....	27
8. Kang does not disclose claim 5.....	28
9. Conclusion.....	28
B. Ground 2: The Challenged Claims Are Not Unpatentable Under 35	
U.S.C. § 103(a) As Obvious Over Da Costa.....	29
1. Da Costa does not disclose the preamble of claim 1.	29
2. Da Costa does not disclose part [b] of claim 1.....	30
3. Da Costa does not disclose part [c] of claim 1.	31
4. Da Costa does not disclose part [d] of claim 1.....	32
5. Da Costa does not disclose part [f] of claim 1.....	32
6. Da Costa does not disclose part [g] of claim 1.....	33
7. Da Costa does not disclose claim 2.....	35
8. Da Costa does not disclose claim 4.....	35
9. Da Costa does not disclose claim 5.....	36
10. Conclusion.....	37
C. Ground 3: The Challenged Claims Are Not Unpatentable Under 35	
U.S.C. § 103(a) As Obvious Over Petropoulos.....	37
1. Petropoulos does not disclose the preamble of claim 1.....	38

2. Petropoulos does not disclose part [b] of claim 1.....	39
3. Petropoulos does not disclose part [d] of claim 1.....	39
4. Petropoulos does not disclose part [g] of claim 1.	40
5. Petropoulos does not disclose claim 2.....	41
6. Petropoulos does not disclose claim 5.....	41
7. Conclusion.....	41
D. Ground 4: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Tanaka.	41
1. Tanaka does not disclose the preamble of claim 1.	42
2. Tanaka does not disclose part [b] of claim 1.	43
3. Tanaka does not disclose part [d] of claim 1.	44
4. Tanaka does not disclose part [f] of claim 1.	44
5. Tanaka does not disclose part [g] of claim 1.....	45
6. Tanaka does not disclose claim 2.	47
7. Tanaka does not disclose claim 4.	48
8. Tanaka does not disclose claim 5.	48
9. Conclusion.....	48
E. Ground 5: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Da Costa In View Of Tsai.	48
1. Wistron uses hindsight to achieve the combination of Da Costa and Tsai, which is improper.....	48
2. A POSITA would not be motivated to combine Da Costa with Tsai.....	50
3. The combination of Da Costa and Tsai does not render the challenged claims obvious.....	52

F. Ground 6: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Tanaka In View Of Tsai.....	53
1. Wistron uses hindsight to achieve the combination of Tanaka and Tsai, which is improper.	53
2. A POSITA would not be motivated to combine Tanaka with Tsai.	54
3. The combination of Tanaka and Tsai does not render the challenged claims obvious.....	56
G. Ground 7: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Petropoulos In View Of Kang.	57
1. Ground 7 should be denied because it is redundant of grounds 1 and 3.....	57
2. A POSITA would not be motivated to combine Petropoulos with Kang.....	59
3. The combination of Petropoulos and Kang does not render the challenged claims obvious.....	62
IX. CONCLUSION.....	62

TABLE OF ABBREVIATIONS

Abbreviation	Term
Phenix	Patent Owner Phenix Longhorn, LLC
Wistron	Petitioner Wistron Corporation
Vizio	Vizio, Inc.
POSITA	Person of ordinary skill in the art
The '305 patent	U.S. Patent No. 7,233,305
Kang	U.S. Patent Application Publication No. 2002/0063666
Da Costa	U.S Patent No. 6,100,879
Petropoulos	U.S. Patent Application Publication No. 2003/0090580
Tanaka	U.S. Patent Application Publication No. 2003/0132906
Tsai	U.S. Patent No. 5,974,528

LIST OF EXHIBITS

Exhibit 2001	Supply Agreement
Exhibit 2004	Complaint for Patent Infringement against Vizio, Inc.
Exhibit 2005	Return of Service of Complaint
Exhibit 2006	Order of Dismissal
Exhibit 2007	Complaint for Patent Infringement against Wistron Corporation
Exhibit 2008	Amended Complaint for Patent Infringement against Wistron Corporation
Exhibit 2009	Privilege Log
Exhibit 2010	Declaration of Robert J. Murphy
Exhibit 2011	Curriculum Vitae of Robert J. Murphy

I. INTRODUCTION.

Phenix respectfully requests that the Board deny institution of Wistron's petition because it is time barred under 35 U.S.C. §315(b). Wistron's petition is time barred because it was filed more than one year after the date a privy of Wistron, Vizio, was served with a complaint alleging infringement of the '305 patent. Wistron had [REDACTED] and therefore already had its opportunity to challenge the '305 patent. As such, Wistron is barred from seeking *inter partes* review and the Board has no jurisdiction to institute review.

Even if the Board determines that the Petition is not time barred, which it is, the Board should deny the Petition because Wistron is not reasonably likely to prevail on any challenged claim. None of the grounds show that the challenged claims are unpatentable as obvious under 35 U.S.C. §103(a). Additionally, grounds 1-4 improperly assert obviousness based on a single prior art reference. Grounds 5-7 fail to establish that a POSITA would be motivated to combine the asserted prior art to arrive at the claimed invention. Also, grounds 5-7 are either based on improper hindsight or are redundant. Accordingly, all grounds to institute review should be denied.

II. FACTUAL BACKGROUND.

On January 5, 2017, Phenix filed a complaint for patent infringement against Vizio.¹ Phenix served Vizio with the complaint on January 13, 2017.² The Vizio complaint accuses Vizio television sets with the AUO-1422.J1 integrated circuit (IC) of infringing the '305 patent.³ The AUO-1422.J1 is a programmable gamma ("P-gamma") integrated circuit that improves the quality of a television users' viewing experience on liquid crystal display (LCD) television sets incorporating this IC. On December 27, 2017, Phenix consented to the dismissal of the Vizio case without prejudice and on January 4, 2018 the court dismissed the case.⁴

Before the Vizio case was dismissed, on October 25, 2017, Phenix filed a similar complaint for patent infringement against Wistron.⁵ On June 15, 2018, Phenix amended its complaint to name Wistron InfoComm (Zhongshan) Corporation and Wistron Mexico SA de CV as defendants.⁶ The Wistron amended complaint also accuses the AUO-1422.J1 integrated circuit of infringing the '305 patent.⁷

¹ Exhibit 2004.

² Exhibit 2005.

³ Exhibit 2004 at ¶22.

⁴ Exhibit 2006.

⁵ Exhibit 2007.

⁶ Exhibit 2008.

⁷ *Id.* at ¶30.

As alleged in the amended complaint, Wistron has all its products designed for sale in the United States reviewed by UL LLC (“UL”) formerly known as Underwriters Laboratories, a private product testing and certification company.⁸ According to the UL website, Wistron has manufactured or is manufacturing television sets and other products that were inspected and certified by UL for use in the United States.⁹ According to the UL online certifications directory, one of the television sets made by Wistron and certified by UL is model number E50u-D2, which incorporates the AUO-1422.J1.¹⁰ Wistron model number E50u-D2 corresponds to the identical model number marketed and sold under the Vizio brand and displays the UL certification mark on the rear housing of the television set.¹¹

Not surprisingly, during discovery in the Wistron case, Wistron produced a Supply Agreement between itself and Vizio.¹² Under the Supply Agreement, [REDACTED]

[REDACTED].¹³ [REDACTED]

[REDACTED],

[REDACTED]

⁸ *Id.* at ¶21.

⁹ *Id.* at ¶22.

¹⁰ *Id.* at ¶¶23, 25.

¹¹ *Id.* at ¶24.

¹² Exhibit 2001.

¹³ *Id.*

[REDACTED].¹⁴ [REDACTED]

[REDACTED],

[REDACTED]

[REDACTED].¹⁵

On June 19, 2018, more than one year after Phenix served Vizio with the complaint asserting infringement of the '305 patent, Wistron filed the Petition.¹⁶ Wistron InfoComm and Wistron Mexico were named as potential real parties in interest on July 5, 2018.¹⁷

III. OVERVIEW OF THE TECHNOLOGY.

A. The Problem To Be Solved.

Buyers of consumer electronics products today are accustomed to viewing LCD displays on televisions, computers, and tablets without appreciating the innovations required in making these screens a pleasant viewing experience. Because of variables inherent in the manufacturing technology, LCDs have color consistency issues that have plagued system integrators, such as Wistron, who need to provide a uniform product to its name brand customers.

¹⁴ *Id.* at ¶2.6.

¹⁵ *Id.* at ¶13.2.

¹⁶ Paper 1.

¹⁷ Paper 3.

When fresh off the production line, the color consistency on LCD panels varies not only by batch in a production line, but also from display-to-display within the same batch. The problem is that the brightness of the LCD pixel is not a linear or straight-line function of the voltages applied; *i.e.*, it is not one-to-one. Compounding this problem is the fact that the human eye's sensitivity to light is also not linear. In order to obtain an acceptable LCD picture, a way is needed to drive the pixels with a voltage to correct for the nonlinear anomalies. This correction is controlled by a set of gamma reference voltages applied to each column driver in the LCD panel. The column driver is an IC with two sets of inputs. The first input is for the digital picture data to be converted into analog voltages applied on a display column of pixels. Each physical column of a display requires its own column driver for each red, green, and blue pixel. The second input is for the gamma reference voltages that are used to correct or adjust the conversion occurring on the first input, resulting in the desired display condition.¹⁸

LCD panels have various problems that are corrected by applying gamma reference voltages. For example, one problem is "banding." Banding occurs when colors vary in brightness from side-to-side in the display when there is variation in

¹⁸ Exhibit 1001 at Fig. 2.

the outputs of each individual column driver. The picture below shows an example of banding:



By using a gamma reference voltage generator which is connected in parallel to all of the column drivers in the display, banding can be eliminated.

The gamma correction curve becomes more complicated as the display resolution increases. In today's world where LCD television sets have become large and have very high resolution, gamma correction becomes a necessity.

Gamma correction can be applied to the gamma reference voltages going into a display using various techniques.

The gamma reference voltages produce changes to the display that are shown below in reference to different gamma correction values:



As described in more detail in the '305 patent, in the 2003 timeframe, manufacturers using the prior art inserted into their displays numerous “select-on-test” resistors or other discrete electronic components that had to be manually changed at the factory, or they included expensive devices using microcontrollers to correct LCD display problems. These solutions were unacceptable to LCD manufacturers due to cost, which was and still is a very important consideration in the manufacturing of these products for the consumer market.

B. The Pioneering Work Of Alta Analog.

Alta Analog, Inc. (“Alta”) was a semiconductor company located in Silicon Valley, started in March 2002 by the inventors of the '305 patent, Richard Orlando and Trevor Blyth. The company was a start-up company, originally housed in the residence of Mr. Orlando, the President of Alta. Alta was founded to

commercialize a new fundamental semiconductor technology that held the promise of revolutionizing the implementation of analog functions on integrated circuits.

Alta grew to about 10 employees and contractors, and like many semiconductor companies in Silicon Valley, subcontracted the manufacturing or fabrication step of the integrated circuits designed by Alta. Thus, Alta was a fabless semiconductor company, and most chips were actually made overseas, primarily in Asia.

Alta pioneered the first programmable gamma reference generator integrated circuit capable of generating two or more gamma reference voltage display conditions for LCD displays. As a result of Alta's pioneering research and development, Mr. Orlando and Mr. Blyth filed a provisional patent application on June 11, 2003¹⁹ and then a utility application on December 23, 2003.²⁰ The utility patent application later issued as the '305 patent on June 19, 2007. The inventors assigned the '305 patent to Alta. Alta designed and developed six programmable gamma reference generator ICs: AGN1114, AGT1809, AGP1814, AGN1814, AGB1818, and ATT3209. In particular, the AG1818 is described as one embodiment of the '305 patent.²¹ Between 2010 and 2011, Alta sold over 230,000

¹⁹ Exhibit 1001 (listing U.S. Pat. Appl. No. 60/477,680).

²⁰ *Id.* (listing U.S. Pat. Appl. No. 10/746,333).

²¹ *Id.* at 5:30-33 ("In one embodiment of the invention, the integrated circuit termed the AG1818, is a programmable gamma reference generator with integrated output

units of the AG1818, which is the same in all material respects to the AGB1818, to Sharp Electronics Corporation for inclusion as a component of LCD television sets sold in the Japanese television market.

Alta's pioneering work of led to the creation of a programmable gamma reference voltage generator on a stand-alone integrated circuit, which provided an inexpensive solution to the LCD display problem. The LCD panel market is extremely cost sensitive, and one of the major benefits of the Alta technology was the ability to deliver a solution for the color variation problem at a price point that was acceptable to the market. The Alta devices solved the display variation problem and allowed the panel electronics to compensate for the variations either on a lot-by-lot basis, or even on a panel-by-panel basis. The Alta devices also allowed the panel to adjust using sensors for changing the driving electronics to achieve the optimum image display, even with changes in the operating environment.

In 2014, Phenix, LLC acquired the '305 patent from Alta and then later assigned it to Phenix Longhorn, LLC.

buffers to directly drive the source driver inputs of a display”), Fig. 4B, Fig. 6, and 5:30 – 7:19.

IV. U.S. PATENT NO. 7,233,305.

In general, the '305 patent describes and claims an integrated circuit that sends voltages to an LCD display to correct its appearance to a user. Specifically, the '305 patent addresses the problem of providing a gamma correction solution to LCD monitors by doing away with manually adjusted select-on-test resistors (or other discrete components) or expensive microcontroller-based solutions and replacing these components with a single, stand-alone integrated circuit. Specifically, the '305 patent solves the problem by teaching a programmable integrated circuit that has multiple banks of gamma correction curves stored in non-volatile memory. Non-volatile memory is a computer memory that retains its data when power is removed. The integrated circuit taught by the '305 patent is capable of producing two or more stored sets of voltage signals, representing the programmed gamma correction curves, in the ranges needed for driving the columns of a display.

V. THE PETITION IS TIME BARRED UNDER 35 U.S.C. § 315(B).

Because Wistron filed its Petition more than one year after Phenix served Wistron's privy, Vizio, with a complaint alleging infringement of the '305 patent, Wistron's Petition is time barred. A petition to institute a trial must be filed with the Board consistent with any time period required by statute.²² Otherwise, the

²² 37 C.F.R. § 42.3(b).

Board lacks jurisdiction to consider it.²³ Section 315(b) provides in pertinent part: “[a]n inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.” “The timely filing of a petition under § 315(b) is a condition precedent to the Director’s authority to act”—indeed, it “sets limits on the Director’s statutory authority to institute.”²⁴ As a threshold issue prior to institution, §315(b) time bar determinations are vital because IPRs can deprive a patentee of significant property rights through the cancellation of claims, as in this case.²⁵ The one-year period during which Wistron could file a petition expired on January 13, 2018—one year after Vizio was served in the Vizio case. Because Wistron and Vizio were in privity, the Petition is time-barred and the Board lacks jurisdiction to institute review.²⁶

The general definition of privity is “[t]he connection or relationship between two parties, each having a legally recognized interest in the same subject matter

²³ *Id.*

²⁴ *See Click-To-Call Techs., LP v. Ingenio, Inc.*, Case No. 215-1242, 2018 U.S. App. LEXIS 22839, at *43 (Fed. Cir. 2018) (*citing Wi-Fi One, LLC v. Broadcom Corp.*, 878 F.3d 1364, 1374 (Fed. Cir. 2018)).

²⁵ *See Applications in Internet Time, LLC v. RPX Corp.*, Case No. 2017-1698, 2018 U.S. App. LEXIS 20605, at *69 (Fed. Cir. 2018) (Reyna, J. concurring).

²⁶ *See Click-To-Call Techs.*, 2018 U.S. App. LEXIS 22839, at *2.

(such as a transaction, proceeding, or piece of property).”²⁷ In a unanimous opinion, the Supreme Court in *Taylor v. Sturgell* described a non-exhaustive list of six categories where each alone is sufficient to establish privity between a named party and a nonparty in litigation: (1) an agreement between the parties to be bound; (2) pre-existing substantive legal relationships between the parties; (3) adequate representation by the named party; (4) the nonparty’s control of the prior litigation; (5) where the nonparty acts as a proxy for the named party to relitigate the same issues; and (6) where special statutory schemes foreclose successive litigation by the nonparty (*e.g.*, bankruptcy and probate).²⁸ The Supreme Court noted that this list of six categories “is meant only to provide a framework” for considering privity, “not to establish a definitive taxonomy.”²⁹ The Board has also recognized that each *Taylor* ground alone is sufficient to establish privity between a non-party and a named party in the prior litigation.³⁰

The PTO’s Trial Practice Guide is consistent with *Taylor*.³¹ The Trial Practice Guide provides that the PTO “intends to evaluate what parties constitute ‘privies’ in a manner consistent with the flexible and equitable considerations

²⁷ *Privity*, Black’s Law Dictionary (10th ed. 2014).

²⁸ *See Taylor v. Sturgell*, 553 U.S. 880, 894-95 (2008).

²⁹ *Id.* at 893 n.6.

³⁰ *See Arris International PLC v. Chanbond, LLC*, IPR2018-00570, Paper 21 at 7 (P.T.A.B. Jul. 27, 2018) (citing *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319-20 (Fed. Cir. 2018)).

³¹ *See Office Patent Trial Practice Guide*, 77 Fed. Reg. 48,756 (Aug. 14, 2012).

established under federal caselaw.”³² The Trial Practice Guide adopts *Taylor*’s definition for privity: “[p]rivity is essentially a shorthand statement that collateral estoppel is to be applied in a given case The concept refers to a relationship between the party to be estopped and the unsuccessful party in the prior litigation which is sufficiently close so as to justify application of the doctrine of collateral estoppel.”³³

At a minimum, the second *Taylor* ground is implicated in this matter. The Supply Agreement constitutes a substantive legal relationship sufficient to establish privity between Wistron and Vizio.³⁴ The relationship between Wistron and Vizio goes beyond typical transactions between supplier and buyer. Vizio’s model number E50u-D2 television is a Wistron television.³⁵ In other words, Vizio merely markets the Wistron television under the Vizio brand name.

Moreover, as the Federal Circuit has observed, [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]³⁶ [REDACTED]

³² *Id.* at 48,759.

³³ *Id.* (citations omitted); see *Taylor*, 553 U.S. at 894 n.8 (“The term ‘privity,’ however, has also come to be used more broadly, as a way to express the conclusion that nonparty preclusion is appropriate on any ground.”).

³⁴ See *Taylor*, 553 U.S. at 894.

³⁵ Exhibit 2008 at ¶24.

³⁶ See *Intel Corp. v. U.S. Int’l Trade Comm’n*, 946 F.2d 821, 839 (Fed. Cir. 1991) (finding that “an indemnification agreement, in other cases, has alone been enough to find privity”); see also *SpeedTrack, Inc. v. Office Depot, Inc.*, No. C 07-3602

.³⁷

.³⁸

Further, the fourth ground of *Taylor* is also implicated in this matter because Wistron had the opportunity to control the Vizio litigation. A nonparty will be found to have control if it “has the actual measure of control or opportunity to control that might reasonably be expected between two formal coparties.”³⁹ Moreover, actual control is not required; the opportunity to exert the appropriate level of control is sufficient.⁴⁰ The Board has found that the opportunity to control the prior proceedings was sufficient to establish privity on numerous occasions.⁴¹

PJH, 2014 U.S. Dist. LEXIS 62674, at *6-7 (N.D. Cal. May 6, 2014) (ruling that in view of the indemnification obligations the manufacturer owed to its customer, the manufacturer was in privity with the customer such that claim preclusion could apply), *aff’d*, 791 F.3d 1317, 1324-29 (Fed. Cir. 2015).

³⁷ *Id.*

³⁸ *See Intel*, 946 F.2d at 839.

³⁹ *See* 77 Fed. Reg. at 48,759 (quoting 18A Charles Alan Wright, Arthur R. Miller & Edward H. Cooper, *Federal Practice and Procedure* § 4451 (2d ed. 2011)).

⁴⁰ *Id.* (“A common consideration is whether the non-party . . . could have exercised control”); *see Gonzalez v. Banco Cent. Corp.*, 27 F.3d 751, 758 (1st Cir. 1994) (“[C]ontrol means . . . the power—whether exercised or not—to call the shots.”).

⁴¹ *See, e.g., Arris International PLC v. Chanbond, LLC*, Case IPR2018-00570, Paper 21 at 10-21 (P.T.A.B. Jul. 20, 2018); *General Electric Company v. Transdata, Inc.*, Case IPR2014-1380, Paper 34 at 7-11 (PTAB Apr. 15, 2015);

Here, [REDACTED]

[REDACTED]. [REDACTED]

[REDACTED].⁴² [REDACTED]

[REDACTED]

[REDACTED].⁴³ [REDACTED]

[REDACTED].⁴⁴ [REDACTED]

[REDACTED].⁴⁵ Thus, Wistron was well aware of the Vizio case and

well aware of its opportunity to control the case.

In short, Wistron “has already had his day in court” as it had the opportunity to present proofs and arguments with respect to its own accused product in the Vizio case.⁴⁶ Wistron had the same practical opportunity to control the course of the proceedings as Vizio. As such, Wistron was in privity with Vizio because it had the opportunity to control that might reasonably be expected between formal coparties, even if Wistron elected not to exercise that control. Because Phenix

First Data Corporation v. Cardsoft, Case IPR2014-00715, Paper 9 at 7-10 (PTAB Oct. 17, 2014).

⁴² See Exhibit 2001 at ¶13.2.

⁴³ *Id.* at Schedule B, ¶2.

⁴⁴ Exhibit 2009.

⁴⁵ *Id.*

⁴⁶ See *Taylor*, 553 U.S. at 895 (“Because such a person has had the opportunity to present proofs and argument, he has already had his day in court even though he was not a formal party to the litigation.”) (internal quotation marks and citations omitted).

served Vizio with a complaint more than one year before Wistron filed its Petition, Wistron's Petition is time barred.

VI. LEGAL PRINCIPLES RELEVANT TO THE CHALLENGE.

Even if the Board determines that the Petition is not time barred, which it is, the Board should deny the Petition to institute review of the challenged claims in view of the following legal principles.

A. Person Of Ordinary Skill In The Art.

Under 35 U.S.C. §103(a), obviousness is determined by resolving the level of skill in the pertinent art.⁴⁷ Wistron's definition of a POSITA is flawed because it leaves out certain important qualifications related to experience in the design of non-volatile memory and knowledge of the state of the art.

The filing date of the '305 patent is December 23, 2003, and relates back to a provisional filed on June 11, 2003.⁴⁸ A POSITA of the '305 patent would be someone working in the field in 2003.⁴⁹ This artisan would be a person with at least a bachelor's of science degree in electrical engineering or physics or a related field, with at least three years of experience in the design of floating gate non-volatile memory integrated circuits either as memory chips or embedded

⁴⁷ See *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17 (1966)).

⁴⁸ Exhibit 1001.

⁴⁹ See *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005).

technology or floating gate analog design or technology. This person would be aware of the state of the art in floating gate non-volatile technology and circuits by reading articles published in journals sponsored by the Institute of Electrical and Electronics Engineers, Inc. (“IEEE”), reading or attending presentations at conferences, such as International Solid-State Circuits Conference (“ISSCC”), or by reading published patents.

B. Claim Construction.

Other than the terms specifically addressed below, Phenix assumes that each term of the challenged claims is given its ordinary and customary meaning. Phenix reserves the right to offer additional constructions should a review be instituted on any of the proposed grounds.

1. “Non-volatile storage cells.”

Phenix agrees with Wistron that the term “non-volatile storage cells” should be construed to mean “cells of a computer memory that retain their stored data after power is removed and restores the data when power is returned to the system, such as, for example, the following: analog floating gate non-volatile memory, Electrically Erasable Programmable Read Only Memory (EEPROM), Flash EEPROM, Ultraviolet EPROM (UVEPROM), and Non-Volatile Random Access Memory (NOVRAM).”

2. “Means to switch between the banks based on one or more external signals.”

Wistron fails to provide a construction for the term “means to switch between the banks based on one or more external signals is provided on said integrated circuit.” Because this term recites a means for performing a specified function, this term must be construed as a means-plus-function limitation under 35 U.S.C. § 112(f).⁵⁰ Under 37 C.F.R. § 42.104(b)(3), where the claim to be construed contains a means-plus-function limitation, the construction of the claim must identify the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function.”⁵¹ Thus, even under the broadest reasonable construction standard applied in these proceedings, the Board must construe the means to switch between the bank limitation as a means-plus-function limitation.⁵²

The function for this limitation is switching between the banks based on one or more external signals. The corresponding structure includes the B0-B2 address inputs.⁵³ The structure is described in Figure 4A which shows pins B0-B2 (the “Bank Select”) that corresponds to Figure 4B at pins 20, 22, and 23.⁵⁴ The

⁵⁰ See 35 U.S.C. §112(f).

⁵¹ See 37 C.F.R. § 42.104(b)(3).

⁵² See *IPCom GmbH & Co. v. HTC Corp.*, 861 F.3d 1362, 1370 (Fed. Cir. 2017).

⁵³ Exhibit 1001 at 5:50-63.

⁵⁴ *Id.* at Figs. 4a-4b.

structure also includes an internal damping circuit, which is referred to in Figure 5 as “Bank Switch Damp Time.”⁵⁵ Finally, the corresponding structure is further shown in Figure 6, which depicts the Bank Select block with inputs B0, B1, and B2.

VII. GROUNDS 1-4 ARE IMPROPER BECAUSE THEY ASSERT OBVIOUSNESS BASED ON A SINGLE PRIOR ART REFERENCE.

Grounds 1-4 improperly assert obviousness based on a single prior art reference and therefore are not reasonably likely to prevail. Numerous pre- and post-*KSR v. Teleflex* Federal Circuit decisions rejected the notion that a single reference made an invention obvious.⁵⁶ Put simply, under this line of authority, “common sense” to achieve the claimed invention must have a documentary basis in the record, lest a decision maker use impermissible hindsight reasoning. These holdings take inspiration from Supreme Court directives in *KSR v. Teleflex* to

⁵⁵ *Id.* at 5:62-66 and Fig. 5.

⁵⁶ See *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355 (Fed. Cir. 2016); *K/S HIMPP v. Hear-Wear Techs., LLC*, 751 F.3d 1362 (Fed. Cir. 2014), cert. denied, 135 S. Ct. 1439 (2015); *In re Kotzab*, 217 F.3d 1365 (Fed. Cir. 2000) (reference teaching one sensor per valve did not render obvious claims for one sensor for multiple valves, despite “simplicity” of proposed modification extending a sensor to multiple valves); *In re Laskowsky*, 871 F.2d 115 (Fed. Cir. 1989) (reciting and applying legal standard that, for obviousness over single reference, prior art must “suggest[] the desirability of the modification”).

avoid hindsight.⁵⁷ They also distinguish decisions where all of the claim limitations existed in a proposed multi-reference combination.⁵⁸

For example, in *K/S HIMPP v. Hear-Wear*, a requester in *inter partes* reexamination challenged the decision of the Board holding a hearing aid patent nonobvious. The invention included modules joined by a connector.⁵⁹ The claims required the connector to contain a multi-pronged plug.⁶⁰ No documentary evidence existed in the record of multi-pronged plugs.⁶¹ The Federal Circuit rejected the appellant’s attempt to invoke undocumented “basic knowledge” or “common sense” to modify a single prior art reference, and thus secure a reversal.⁶² The Federal Circuit held that a decision maker may not hold a claimed invention obvious over a single prior art reference that fails to disclose a core structural claim limitation, unless contemporaneous documentary evidence suggested that a POSITA would have modified the reference with the missing item.⁶³

⁵⁷ See *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

⁵⁸ See, e.g., *Hear-Wear*, 751 F.3d at 1366.

⁵⁹ *Id.* at 1363.

⁶⁰ *Id.*

⁶¹ *Id.* at 1365.

⁶² *Id.* at 1366 (“[T]he Board cannot accept general conclusions about what is ‘basic knowledge’ or ‘common sense’ as a replacement for core factual findings in a determination of patentability.”).

⁶³ *Id.*

Hear-Wear specifically discussed why the “flexible approach” to determining obviousness required by the Supreme Court’s *KSR* decision does not weaken the requirement of documentary evidence when dealing with a single-reference modification theory. “In contradistinction to *KSR*, this case involves the lack of evidence of a specific claim limitation, whereas *KSR* related to the combinability of references where the claim limitations were in evidence.”⁶⁴ The same holds true in this case. As discussed further below, Wistron impermissibly seeks to invalidate the ’305 patent by invoking basic knowledge, common sense, or well-known practices to supply a core structure claim limitation otherwise missing from the alleged prior art without documentary evidence or evidence of the desirability of the asserted modification.

**VIII. NONE OF THE GROUNDS SHOW A REASONABLE
LIKELIHOOD OF PREVAILING ON ANY CHALLENGED
CLAIM.**

Review should also not be instituted because none of the seven grounds raised in the Petition provide a basis for the Board to find that there is a reasonable likelihood of prevailing on any claim challenged in the Petition. Below, Phenix provides examples of why these grounds clearly fail to render the challenged claims unpatentable, and expressly reserves the right to provide additional reasons and support should a review be instituted on any proposed ground.

⁶⁴ *Id.*

A. Ground 1: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Kang.

1. Kang does not disclose the preamble of claim 1.

Kang does not disclose the preamble of claim 1 because it does not disclose all of the claimed components on a single integrated circuit. Wistron merely asserts that Kang discloses gamma controller 91 and memory 92 on a single integrated circuit.⁶⁵ Kang does not teach that the other components of the multi-mode gamma voltage generator 84, which Wistron relies on from Figure 9, are also part of the same integrated circuit as gamma controller 91 and memory 92.

In addition, Kang implements the gamma controller 91 using a microcomputer.⁶⁶ The '305 patent, however, expressly teaches against the use of a microcontroller: “the present invention advantageously allows a stand-alone solution such that it is not necessary to incorporate a micro controller unit (MCU)”.⁶⁷ Kang does not disclose how to create the claimed invention without the use of a microcomputer. A POSITA would understand that a microcomputer is a large and expensive component and would defeat the intent of the inventors to create a less expensive, smaller, and thinner gamma reference architecture.⁶⁸ Thus, Kang teaches away from the claimed invention because it would lead a POSITA

⁶⁵ Paper 1 at p. 23.

⁶⁶ Exhibit 1007 at ¶52.

⁶⁷ Exhibit 1001 at 2:33-35.

⁶⁸ Exhibit 2010 at ¶36.

“in a direction divergent from the path that was taken” in the claim.⁶⁹ As such, Kang does not render the claimed invention obvious.

2. Kang does not disclose part [b] of claim 1.

Kang also does not disclose part [b] of claim 1 because it does not disclose “circuits for programming.” Wistron asserts Kang meets this limitation by its disclosure of the gamma controller 91.⁷⁰ But Kang implements the gamma controller 91 using a microcomputer.⁷¹ The broadest reasonable construction of “circuits for programming” in light of the specification would not encompass a microcomputer because, as discussed above, the specification expressly teaches against the use of a microcomputer.⁷² Moreover, the plain claim language requires “circuit for programming coupled to a multiplexer.” A POSITA would not understand the claims to require a microcomputer coupled to a multiplexer because a microcomputer would have no need for a multiplexer—a microcomputer is a large and sophisticated computing device that can perform multiplexing itself.⁷³ Thus, contrary to what Wistron claims, the gamma controller 91 does not teach the circuits for programming limitation of claim 1.

⁶⁹ See *Meiresonne v. Google, Inc.*, 849 F.3d 1379, 1382 (Fed. Cir. 2017) (citing *Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013)).

⁷⁰ Paper 1 at p. 25.

⁷¹ Exhibit 1007 at ¶52.

⁷² Exhibit 1001 at 2:33-35.

⁷³ Exhibit 2010 at ¶38.

In addition, Kang does not disclose part [b] of claim 1 because it does not disclose “a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs.” Wistron asserts that Kang meets this limitation by its disclosure of an I²C serial interface.⁷⁴ But Wistron’s contention is flawed because it claims that the I²C serial interface satisfies the plurality of inputs limitation, not the multiplexer.⁷⁵ Wistron does not explain where Kang discloses a multiplexer because Kang does not.⁷⁶

Moreover, Wistron provides no support for its conclusory statement that a POSITA would have understood that the use of a serial interface instead of a multiplexer is an obvious modification.⁷⁷ Wistron’s expert makes no such statement,⁷⁸ Wistron provides no documentary evidence to support the modification,⁷⁹ and Wistron points to no evidence in the record that shows the desirability of such a modification.⁸⁰ Indeed, Kang suggests that such a modification is not desirable because an I²C interface is necessitated by Kang’s

⁷⁴ Paper 1 at p. 24.

⁷⁵ Exhibit 1002 at ¶57 (“The I²C interface . . . constitutes a ‘plurality of input lines.’”).

⁷⁶ See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”).

⁷⁷ *Id.*

⁷⁸ Exhibit 1002 at ¶55.

⁷⁹ See *Hear Wear*, 751 F.3d at 1365.

⁸⁰ See *In re Laskowsky*, 871 F.2d at 117.

implementation of the gamma controller 91 as a microcomputer, which, as discussed above, teaches away from the claimed invention.

Furthermore, a multiplexer and an I²C serial interface do not perform the same function within an integrated circuit and therefore are not interchangeable.⁸¹ For example, as Wistron's expert contends, the I²C serial interface provides instructions and addresses for where to write the data to the memory.⁸² Thus, Kang leads a POSITA to including structures that provide this intelligence on the integrated circuit, which increases the cost and complexity of the chip.⁸³ The '305 patent, however, uses a multiplexer instead of an I²C serial interface because it merely requires address lines such that the structure needed for providing instructions and addresses can be provided off the chip, which is consistent with the '305 patent goal of providing a smaller and cheaper gamma reference solution.⁸⁴

3. Kang does not disclose part [d] of claim 1.

Kang does not disclose part [d] of claim 1 because Kang does not disclose “the plurality of inputs connected to said multiplexer for addressing said storage

⁸¹ Exhibit 2010 at ¶39.

⁸² Exhibit 1002 at ¶55.

⁸³ Exhibit 2010 at ¶40.

⁸⁴ *Id.*

cells” for the same reasons that Kang does not disclose a multiplexer as discussed with respect to part [b] above.

4. Kang does not disclose part [f] of claim 1.

Kang does not disclose part [f] of claim 1 because it does not disclose “non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition.” Wistron asserts that Kang meets this limitation by its disclosure of a memory “for storing gamma data for controlling a gamma voltage for each or at least two modes.”⁸⁵ Kang, however, merely discloses a memory block 92. Even assuming that memory block 92 consists of memory cells, Kang does not provide any details for how the memory cells are organized. A POSITA would not understand that memory 92 is necessarily organized into two or more banks of cells because it stores gamma voltages for multiple modes.⁸⁶

5. Kang does not disclose part [g] of claim 1.

Kang does not disclose part [g] of claim 1 because Kang does not disclose “means to switch between the banks based on one or more external signals is provided on said integrated circuit” for the same reasons that Kang does not disclose banks of cells as discussed with respect to part [f] above. In addition,

⁸⁵ Paper 1 at p. 27.

⁸⁶ Exhibit 2010 at ¶41.

Kang fails to disclose the structures required by this limitation. Neither Wistron nor its expert identify where Kang discloses inputs B0-B2 and bank select circuitry for switching between two or more banks of cells provided on a single integrated circuit.⁸⁷ Wistron merely asserts that Kang meets this limitation by its disclosure of a control means yet provides no explanation for how the control means corresponds to the structures disclosed in the '305 patent.⁸⁸ Thus, Wistron fails to show that Kang teaches this limitation.

6. Kang does not disclose claim 2.

As noted above, Kang does not disclose all of the limitations of claim 1. Because claim 2 incorporates all of the limitations of claim 1, Kang does not disclose all of the limitations of claim 2 and thus does not render claim 2 obvious.

7. Kang does not disclose claim 4.

As noted above, Kang does not disclose all of the limitations of claim 1. Because claim 4 incorporates all of the limitations of claim 1, Kang does not disclose all of the limitations of claim 4 and thus does not render claim 4 obvious.

⁸⁷ See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”); Paper 1 at p. 28; Exhibit 1002 at ¶60.

⁸⁸ See 37 C.F.R. § 42.22(a)(2) (requiring a detailed explanation of the significance of the evidence); Paper 1 at p. 28; Exhibit 1002 at ¶60.

8. Kang does not disclose claim 5.

As noted above, Kang does not disclose all of the limitations of claim 1. Because claim 5 incorporates all of the limitations of claim 1, Kang does not disclose all of the limitations of claim 5 and thus does not render claim 5 obvious.

In addition, Kang does not disclose claim 5 because it does not disclose “circuits for programming require an external source for the high voltage programming means.” As discussed above, Wistron asserts that the gamma controller 91 constitutes “circuits for programming.” But in its analysis of claim 5, Wistron asserts that an EPROM or an EEPROM, which Kang implements by memory 92, requires high programming voltages, not the gamma controller 91 as required by Wistron’s claim 1 analysis.⁸⁹ Wistron does not specify where Kang discloses that the gamma controller 91 requires high voltage programming and provides no evidence that would support such an assertion.⁹⁰ Thus, Wistron fails to show that Kang teaches this limitation.

9. Conclusion.

For all the reasons set forth above, Wistron fails to show any reasonable likelihood that it will prevail on ground 1. Accordingly, the Petition to institute review on ground 1 should be denied.

⁸⁹ Paper 1 at p. 30.

⁹⁰ See 37 C.F.R. § 42.104(b)(4)-(5); Paper 1 at p. 30; Exhibit 1002 at ¶69.

B. Ground 2: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Da Costa.

1. Da Costa does not disclose the preamble of claim 1.

Da Costa does not disclose the preamble of claim 1 because it does not disclose all of the claimed components on a single integrated circuit. Wistron merely asserts that Da Costa discloses a smart controller and a flash memory on a single integrated circuit.⁹¹ Da Costa does not teach that the other limitations of claim 1 are also on the same integrated circuit. For example, Wistron asserts that column drivers 108 meet the driver limitation of claim 1.⁹² But Figure 4a of Da Costa, which Wistron's expert relies on, shows that column drivers 108 are not part of the same integrated circuit as smart controller 202.⁹³

In addition, a POSITA would understand that Da Costa's smart controller is akin to a microcontroller.⁹⁴ The '305 patent, however, expressly teaches against the use of a microcontroller: "the present invention advantageously allows a stand-alone solution such that it is not necessary to incorporate a micro controller unit (MCU)".⁹⁵ Da Costa does not disclose how to achieve the claimed invention without the use of a microcontroller. A POSITA would understand that a

⁹¹ Paper 1 at p. 23.

⁹² Paper 1 at p. 33.

⁹³ Exhibit 1008 at Fig. 4a; Exhibit 1002 at ¶75.

⁹⁴ Exhibit 2010 at ¶42.

⁹⁵ Exhibit 1001 at 2:33-35.

microcontroller is a large and expensive component and that it would defeat the intent of the inventors to create a less expensive, smaller, and thinner gamma reference architecture.⁹⁶ Thus, Da Costa teaches away from the claimed invention because it would lead a POSITA “in a direction divergent from the path that was taken” in the claim.⁹⁷ As such, Da Costa does not render the claimed invention obvious.

2. Da Costa does not disclose part [b] of claim 1.

Da Costa also does not disclose part [b] of claim 1 because it does not disclose “circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs.” Wistron does not explain where Da Costa discloses “circuits for programming coupled to a multiplexer.”⁹⁸ Wistron does not specify what it contends is the “circuits for programming.”⁹⁹ Even assuming that Wistron contends that the smart controller is the circuits for programming or includes the

⁹⁶ Exhibit 2010 at ¶42.

⁹⁷ See *Meiresonne*, 849 F.3d at 1382 (citing *Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013)).

⁹⁸ See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”); Paper 1 at p. 33; Exhibit 1002 at ¶¶77-78.

⁹⁹ See 37 C.F.R. § 42.22(a)(2) (requiring a detailed explanation of the significance of the evidence); Paper 1 at p. 33; Exhibit 1002 at ¶¶77-78.

circuits for programming, Wistron does not explain how these components are coupled to a multiplexer.

In addition, Da Costa does not disclose part [b] of claim 1 because it does not disclose “a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs.” Wistron states that multiple address lines, which Wistron contends corresponds to the “plurality of inputs,” are required, but does not state what the multiple address lines are.¹⁰⁰ Wistron appears to contend that the serial bus provides the address lines.¹⁰¹ But Wistron does not explain what provides the multiplexer or the circuits for programming coupled to a multiplexer because Da Costa does not.¹⁰² Moreover, as discussed above, a serial bus is not interchangeable with a multiplexer. Thus, Wistron fails to establish that Da Costa teaches this limitation.

3. Da Costa does not disclose part [c] of claim 1.

Da Costa does not disclose part [c] of claim 1 because it does not disclose “drivers connected . . . to the plurality of outputs” on a single integrated circuit. Wistron contends that drivers are met by column drivers 108.¹⁰³ But as noted above, the column drivers 108 are not on the same integrated circuit as the smart

¹⁰⁰ Paper 1 at p. 33; Exhibit 1002 at ¶77.

¹⁰¹ Paper 1 at p. 24.

¹⁰² See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”).

¹⁰³ Paper 1 at p. 33.

controller 202.¹⁰⁴ Alternatively, Wistron contends that drivers are met by the high-power analog output 416.¹⁰⁵ But neither Wistron nor its expert explain where this alleged driver, or column driver 108 for that matter, is connected to a plurality of outputs.¹⁰⁶ Thus, Wistron fails to establish that Da Costa teaches this limitation.

4. Da Costa does not disclose part [d] of claim 1.

Da Costa does not disclose part [d] of claim 1 because Da Costa does not disclose “the plurality of inputs connected to said multiplexer for addressing said storage cells” for the same reasons that Da Costa does not disclose a plurality of inputs or a multiplexer as discussed with respect to part [b] above.

5. Da Costa does not disclose part [f] of claim 1.

Da Costa does not disclose part [f] of claim 1 because it does not disclose “non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition.” Wistron asserts that Da Costa meets this limitation by its disclosure of a flash memory 303.¹⁰⁷ Da Costa, however, merely discloses a flash memory block 303.¹⁰⁸ Even assuming that the flash memory block 303 consists of memory cells, Da Costa does not provide any details for how the memory cells are organized. A

¹⁰⁴ Exhibit 1008 at Fig. 4a.

¹⁰⁵ Paper 1 at p. 34.

¹⁰⁶ *Id.*; Exhibit 1002 at ¶79.

¹⁰⁷ Paper 1 at p. 35; Exhibit 1002 at ¶82.

¹⁰⁸ Exhibit 1008 at Fig. 4a.

POSITA would not understand that flash memory 303 is necessarily organized into two or more banks of cells merely because it stores gamma curves.¹⁰⁹ Wistron's expert also mistakenly claims that a multiple memory bank architecture is shown in Figure 7A.¹¹⁰ But Figure 7A shows the registers 410 located in the high-power analog output circuitry 416 or the low-power output analog circuitry 450, not flash memory 303 or PROM 206.¹¹¹ Thus, contrary to what Wistron claims, a POSITA would not understand Da Costa to store gamma curves in multiple banks of storage cells.¹¹²

6. Da Costa does not disclose part [g] of claim 1.

Da Costa does not disclose part [g] of claim 1 because Da Costa does not disclose “means to switch between the banks based on one or more external signals is provided on said integrated circuit” for the same reasons that Da Costa does not disclose banks of cells as discussed with respect to part [f] above. In addition, Da Costa fails to disclose the structures required by this limitation. Neither Wistron nor its expert identify where Da Costa discloses inputs B0-B2 and bank select

¹⁰⁹ Exhibit 2010 at ¶43.

¹¹⁰ Exhibit 1002 at ¶82.

¹¹¹ Exhibit 1008 at 8:48-50.

¹¹² Exhibit 2010 at ¶43.

circuitry for switching between two or more banks of storage cells provided on a single integrated circuit.¹¹³

First, Wistron asserts that Da Costa meets this limitation by its disclosure of MUX 704 and MUX 706 and chip control circuitry 406.¹¹⁴ Yet, Wistron provides no explanation for how these structures correspond to the structures disclosed in the '305 patent.¹¹⁵ In addition, the structures that Wistron points to do not provide a means to switch between two or more banks of non-volatile storage cells in flash memory 303. As shown in Figure 7A, MUX 704 and MUX 706 and control chip circuitry 406 allow for the selection of digital values in register 410.¹¹⁶ Thus, Wistron fails to show that Da Costa teaches this limitation.

Second, Wistron asserts that Da Costa meets this limitation based on external input from host system 105.¹¹⁷ Yet, Wistron provides no explanation for how the host system 105 corresponds to the structures disclosed in the '305 patent.¹¹⁸ In addition, Wistron provides no evidence as to how the host system 105

¹¹³ See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”); Paper 1 at pp. 35-36; Exhibit 1002 at ¶83.

¹¹⁴ Paper 1 at p. 35.

¹¹⁵ See 37 C.F.R. § 42.22(a)(2) (requiring a detailed explanation of the significance of the evidence); Paper 1 at p. 35; Exhibit 1002 at ¶83.

¹¹⁶ Exhibit 1008 at 9:1-29.

¹¹⁷ Paper 1 at pp. 35-36; Exhibit 1002 at ¶83.

¹¹⁸ See 37 C.F.R. § 42.22(a)(2) (requiring a detailed explanation of the significance of the evidence); Paper 1 at p. 35; Exhibit 1002 at ¶83.

provides a means to switch between two or more banks of non-volatile storage cells in flash memory 303. A POSITA would not understand the use of host system 105 to dynamically modify analog reference levels and the column and row signals output by smart controller 202 as describing a means to switch between banks of non-volatile storage cells.¹¹⁹ Further, host system 105 is external to smart controller 202 whereas claim 1 requires the corresponding structure of the means to switch between the banks to be “provided on said integrated circuit.”¹²⁰ For all the reasons above, Da Costa does not satisfy this limitation.

7. Da Costa does not disclose claim 2.

As noted above, Da Costa does not disclose all of the limitations of claim 1. Because claim 2 incorporates all of the limitations of claim 1, Da Costa does not disclose all of the limitations of claim 2 and thus does not render claim 2 obvious.

8. Da Costa does not disclose claim 4.

As noted above, Da Costa does not disclose all of the limitations of claim 1. Because claim 4 incorporates all of the limitations of claim 1, Da Costa does not disclose all of the limitations of claim 4 and thus does not render claim 4 obvious.

In addition, Da Costa does not disclose claim 4 because Da Costa does not disclose non-volatile storage cells that hold analog voltage values. Wistron even

¹¹⁹ Exhibit 2010 at ¶44.

¹²⁰ Exhibit 1001 at 7:60-62.

states that the flash memory 303 holds a digital representation of analog output voltages, not analog voltage values.¹²¹ Wistron does not even cite any evidence that the flash memory holds analog voltage values.¹²² Thus, Wistron fails to show that Da Costa teaches this limitation.

9. Da Costa does not disclose claim 5.

As noted above, Da Costa does not disclose all of the limitations of claim 1. Because claim 5 incorporates all of the limitations of claim 1, Da Costa does not disclose all of the limitations of claim 5 and thus does not render claim 5 obvious.

In addition, Da Costa does not disclose claim 5 because it does not disclose “circuits for programming require an external source for the high voltage programming means.” Like it does above in connection with claim 1, Wistron does not state what it asserts constitutes “circuits for programming.” Even assuming that Wistron contends that the smart controller 202 is the circuits for programming or includes the circuits for programming, Wistron does not explain where Da Costa discloses that these components require an external source for high voltage programming.¹²³ Wistron’s expert contends that a POSITA would

¹²¹ Paper 1 at p. 36.

¹²² *Id.*; Exhibit 1002 at ¶89; see 37 C.F.R. § 42.104(b)(5)(requiring specific evidence to support challenge).

¹²³ See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”); Paper 1 at p. 37; Exhibit 1002 at ¶93.

know that high voltages are required to program an EEPROM.¹²⁴ But Da Costa discloses flash memory, not EEPROM. Indeed, neither Wistron nor its expert explain where Da Costa discloses EEPROM.¹²⁵ Thus, Wistron fails to show that Da Costa teaches this limitation.

10. Conclusion.

For all the reasons set forth above, Wistron fails to show any reasonable likelihood that it will prevail on ground 2. Accordingly, the Petition to institute review on ground 2 should be denied.

C. Ground 3: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Petropoulos.

Wistron incorrectly states that Petropoulos is prior art under 35 U.S.C. §102(b). Because the '305 patent was filed before March 16, 2003, alleged prior art to the '305 patent is determined by pre-America Invents Act §102.¹²⁶ Under pre-AIA §102(b), Petropoulos, which published May 15, 2003, does not qualify as prior art because it was not published more than one year before the filing date of the '305 patent, which is December 23, 2003.¹²⁷ Accordingly, for the purpose of this Preliminary Response, Phenix assumes that Petropoulos qualifies as prior art

¹²⁴ *Id.*

¹²⁵ See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”); Paper 1 at p. 37; Exhibit 1002 at ¶93.

¹²⁶ See MPEP §2159.01.

¹²⁷ 35 U.S.C. §102(b) (pre-AIA).

under pre-AIA §102 but reserves the right to contest that Petropoulos qualifies as prior art.

1. Petropoulos does not disclose the preamble of claim 1.

Petropoulos does not disclose the preamble of claim 1 because it does not disclose all of the claimed components on a single integrated circuit. Wistron and its expert admit as much.¹²⁸ Contrary to what Wistron claims, it would not have been obvious to a POSITA simply looking at Petropoulos to include the components on a single integrated circuit.¹²⁹ Petropoulos is directed to correcting corrupted elements in signal sensors.¹³⁰ The only evidence in Petropoulos that Wistron claims supports modifying Petropoulos is the observation that the quality of a reproduced image is important in high-end applications.¹³¹ This statement, however, is made in the context of addressing manufacturing variations in sensors.¹³² This observation in no way suggests that a single integrated circuit would be a solution to the problem of correcting corrupted sensor output as addressed by Petropoulos. Further, other than the unsupported and conclusory statement by its expert that it would be difficult to achieve high-fidelity output, Wistron provides no evidence in the record that shows the desirability of

¹²⁸ Paper 1 at p. 40; Exhibit 1002 at ¶¶99.

¹²⁹ Exhibit 2010 at ¶45.

¹³⁰ Exhibit 1009 at ¶[0002].

¹³¹ Paper 1 at p. 41.

¹³² Exhibit 1009 at ¶¶[0008]-[0009].

modifying Petropoulos to be a single integrated circuit.¹³³ Thus, the preamble of claim 1 would not be obvious in light of Petropoulos.

2. Petropoulos does not disclose part [b] of claim 1.

Petropoulos also does not disclose part [b] of claim 1 because it does not disclose “circuits for programming for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs.” Wistron does not explain where Petropoulos discloses “circuits for programming coupled to a multiplexer.”¹³⁴ Wistron does not specify what it contends is the “multiplexer.”¹³⁵ Even accepting Wistron’s contention that Petropoulos discloses an address signal generator as the circuits for programming or as part of the circuits for programming, Wistron does not explain how these components are coupled to a multiplexer. Thus, Wistron fails to establish that Petropoulos teaches this limitation.

3. Petropoulos does not disclose part [d] of claim 1.

Petropoulos does not disclose part [d] of claim 1 because Petropoulos does not disclose “the plurality of inputs connected to said multiplexer for addressing

¹³³ See *In re Laskowsky*, 871 F.2d at 117.

¹³⁴ See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”); Paper 1 at p. 33; Exhibit 1002 at ¶¶77-78.

¹³⁵ See 37 C.F.R. § 42.22(a)(2) (requiring a detailed explanation of the significance of the evidence); Paper 1 at pp. 41-42; Exhibit 1002 at ¶¶102-103.

said storage cells” for the same reasons that Petropoulos does not disclose a multiplexer as discussed with respect to part [b] above.

4. Petropoulos does not disclose part [g] of claim 1.

Petropoulos does not disclose part [g] of claim 1 because Petropoulos does not disclose “means to switch between the banks based on one or more external signals is provided on said integrated circuit” for the same reasons that Petropoulos does not disclose all of the components of claim 1 on a single integrated circuit as discussed with respect to the preamble above. In addition, Petropoulos fails to disclose the structures required by this limitation. Neither Wistron nor its expert identify where Petropoulos discloses inputs B0-B2 and bank select circuitry for switching between two or more banks of storage cells provided on a single integrated circuit.¹³⁶

Wistron asserts that Petropoulos meets this limitation by its disclosure of a decoder. Yet, Wistron provides no explanation for how a decoder corresponds to the structures disclosed in the ’305 patent.¹³⁷ Thus, Wistron fails to show that Petropoulos teaches this limitation.

¹³⁶ See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”); Paper 1 at pp. 44-45; Exhibit 1002 at ¶¶108-109.

¹³⁷ See 37 C.F.R. § 42.22(a)(2) (requiring a detailed explanation of the significance of the evidence); Paper 1 at pp. 44-45; Exhibit 1002 at ¶¶108-109.

5. Petropoulos does not disclose claim 2.

As noted above, Petropoulos does not disclose all of the limitations of claim 1. Because claim 2 incorporates all of the limitations of claim 1, Petropoulos does not disclose all of the limitations of claim 2 and thus does not render claim 2 obvious.

6. Petropoulos does not disclose claim 5.

As noted above, Petropoulos does not disclose all of the limitations of claim 1. Because claim 5 incorporates all of the limitations of claim 1, Petropoulos does not disclose all of the limitations of claim 5 and thus does not render claim 5 obvious.

7. Conclusion.

For all the reasons set forth above, Wistron fails to show any reasonable likelihood that it will prevail on ground 3. Accordingly, the Petition to institute review on ground 3 should be denied.

D. Ground 4: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Tanaka.

Wistron incorrectly states that Tanaka is prior art under 35 U.S.C. §102(b). Because the '305 patent was filed before March 16, 2003, alleged prior art to the '305 patent is determined by pre-AIA §102.¹³⁸ Under pre-AIA §102(b), Tanaka,

¹³⁸ See MPEP § 2159.01.

which published July 17, 2003, does not qualify as prior art because it was not published more than one year before the filing date of the '305 patent, which was filed December 23, 2003. Accordingly, for the purpose of this Preliminary Response, Phenix assumes that Tanaka qualifies as prior art under pre-AIA §102(e)—the other section under which Wistron claims Tanaka qualifies as prior art¹³⁹—but Phenix reserves its right to swear behind Tanaka.

1. Tanaka does not disclose the preamble of claim 1.

Tanaka does not disclose the preamble of claim 1 because it does not disclose all of the claimed components on a single integrated circuit. Wistron merely asserts that Tanaka's source driver 101 is composed of an integrated circuit, not that it is an integrated circuit.¹⁴⁰ Regardless of whether Wistron considers source driver 101 to be a single integrated circuit, Tanaka does not teach that the limitations of claim 1 are also on the same integrated circuit. For example, as discussed below, Wistron does not specify where Tanaka discloses a multiplexer. Indeed, source driver 101 does not contain a multiplexer and therefore cannot be the integrated circuit required by claim 1.¹⁴¹

¹³⁹ Paper 1 at p. 46.

¹⁴⁰ Paper 1 at p. 49.

¹⁴¹ Exhibit 1010 at Fig. 1.

2. Tanaka does not disclose part [b] of claim 1.

Tanaka also does not disclose part [b] of claim 1 because it does not disclose “circuits for programming coupled to a multiplexer for addressing and programming said storage cells, wherein the addressing is based on a plurality of inputs.” Wistron does not explain where Tanaka discloses “circuits for programming coupled to a multiplexer.”¹⁴² Wistron even admits that Tanaka does not disclose a “multiplexer.”¹⁴³ Even assuming that an external control device is what Wistron claims is the circuits for programming, the external control device does not satisfy claim 1 because it is external to source driver 108, which Wistron apparently claims is the integrated circuit.¹⁴⁴ Wistron also does not explain how these components are coupled to a multiplexer. Contrary to what Wistron believes, Wistron’s expert provides no support for its claim that it would have been obvious to a POSITA to employ a multiplexer.¹⁴⁵ Indeed, it would not have been obvious for a POSITA to employ a multiplexer because a POSITA would have no need for a multiplexer given the use of the external control device.¹⁴⁶ Thus, Wistron fails to show that Tanaka renders this limitation obvious.

¹⁴² See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”); Paper 1 at pp. 49-50; Exhibit 1002 at ¶¶77-78.

¹⁴³ Paper 1 at p. 50.

¹⁴⁴ Exhibit 1010 at ¶[0102], ¶[0143], and Fig. 3.

¹⁴⁵ Exhibit 1002 at ¶123.

¹⁴⁶ Exhibit 2010 at ¶46.

3. Tanaka does not disclose part [d] of claim 1.

Tanaka does not disclose part [d] of claim 1 because Tanaka does not disclose “the plurality of inputs connected to said multiplexer for addressing said storage cells” for the same reasons that Tanaka does not disclose a multiplexer as discussed with respect to part [b] above. Again, Wistron’s expert provides no support for Wistron’s claim that it would have been obvious to a POSITA to employ a multiplexer.¹⁴⁷

4. Tanaka does not disclose part [f] of claim 1.

Tanaka does not disclose part [f] of claim 1 because it does not disclose “non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition.” Wistron asserts that Tanaka meets this limitation by its disclosure of reference voltage generating circuits 52-1, 52-2, and 52-3.¹⁴⁸ But these circuits are not non-volatile storage cells. Instead, they are circuits connected to non-volatile memory block 53.¹⁴⁹ Even assuming that non-volatile memory block 53 consists of memory cells, Tanaka does not provide any details for how the memory cells are

¹⁴⁷ Exhibit 1002 at ¶125.

¹⁴⁸ Paper 1 at p. 51; Exhibit 1002 at ¶127.

¹⁴⁹ Exhibit 1010 at Fig. 10.

organized. Thus, a POSITA would not understand that non-volatile memory block is necessarily organized into two or more banks of cells.¹⁵⁰

5. Tanaka does not disclose part [g] of claim 1.

Tanaka does not disclose part [g] of claim 1 because Tanaka does not disclose “means to switch between the banks based on one or more external signals is provided on said integrated circuit” for the same reasons that Tanaka does not disclose all of the components of claim 1 on a single integrated circuit or banks of cells as discussed above. In addition, Tanaka fails to disclose the structures required by this limitation. Neither Wistron nor its expert identify where Tanaka discloses inputs B0-B2 and bank select circuitry for switching between two or more banks of storage cells provided on a single integrated circuit.¹⁵¹

Wistron asserts that Tanaka meets this limitation four different ways but none of those ways teach claim 1. First, Wistron claims that reference voltage generating circuits 52-1, 52-2, and 52-3 are selected based on the color of the data.¹⁵² But as discussed above, the reference voltage generating circuits are not

¹⁵⁰ Exhibit 2010 at ¶47.

¹⁵¹ See 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents.”); Paper 1 at pp. 44-45; Exhibit 1002 at ¶¶108-109.

¹⁵² Paper 1 at p. 51; Exhibit 1002 at ¶128.

banks of cells. Moreover, Wistron fails to identify the structures that switch between these alleged banks of cells.¹⁵³

Second, Wistron claims that multiple gamma correction data is stored in display memory 110 as shown in Figure 20. But again, Wistron fails to identify the structures in Tanaka that provide the means for switching between the stored gamma curves.¹⁵⁴

Third, Wistron claims that multiple gamma data are also shown in Figure 25.¹⁵⁵ Not only does Wistron's expert admit that the gamma data shown in Figure 25 is stored in external memory, he also admits that it is selected by an external controller 105.¹⁵⁶ Thus, it is irrelevant whether it would have been obvious to a POSITA to enlarge memory 53 of the first alternative to include more gamma curves because external controller 105 is not provided on the same integrated circuit. Moreover, to the extent that Wistron claims that the external controller provides a means to switch between the banks, Wistron fails to explain how this controller satisfies the structure required by claim 1.¹⁵⁷

¹⁵³ *Id.*; see 37 C.F.R. § 42.104(b)(5)(requiring specific evidence to support challenge).

¹⁵⁴ *Id.*

¹⁵⁵ Exhibit 1002 at ¶129.

¹⁵⁶ *Id.*

¹⁵⁷ See 37 C.F.R. § 42.22(a)(2) (requiring a detailed explanation of the significance of the evidence).

Finally, Wistron's contention that Tanaka discloses an external controller 105 that provides external control signals to select gamma correction data is also flawed.¹⁵⁸ As discussed above, the use of a controller teaches away from the '305 patent. In addition, as shown in Figure 33, the external controller 105 is not provided on the same integrated circuit as non-volatile display memory 110 and 137. Thus, it is irrelevant whether it would have been obvious to a POSITA to add memory to source driver 101. And even if it was, Tanaka does not teach how external controller 105 switches between gamma curves stored in memory 53.¹⁵⁹ Moreover, to the extent that Wistron claims that the external controller provides a means to switch between the banks, Wistron fails to explain how this controller satisfies the structure required by claim 1.¹⁶⁰

6. Tanaka does not disclose claim 2.

As noted above, Tanaka does not disclose all of the limitations of claim 1. Because claim 2 incorporates all of the limitations of claim 1, Tanaka does not disclose all of the limitations of claim 2 and thus does not render claim 2 obvious.

¹⁵⁸ Paper 1 at p. 52; Exhibit 1002 at ¶¶130-131.

¹⁵⁹ Exhibit 2010 at ¶¶48-49.

¹⁶⁰ See 37 C.F.R. § 42.22(a)(2) (requiring a detailed explanation of the significance of the evidence).

7. Tanaka does not disclose claim 4.

As noted above, Tanaka does not disclose all of the limitations of claim 1. Because claim 4 incorporates all of the limitations of claim 1, Tanaka does not disclose all of the limitations of claim 4 and thus does not render claim 4 obvious.

8. Tanaka does not disclose claim 5.

As noted above, Tanaka does not disclose all of the limitations of claim 1. Because claim 5 incorporates all of the limitations of previously presented claim 1, Tanaka does not disclose all of the limitations of claim 5 and thus does not render claim 5 obvious.

9. Conclusion.

For all the reasons set forth above, Wistron fails to show any reasonable likelihood that it will prevail on ground 4. Accordingly, the Petition to institute review on ground 4 should be denied.

E. Ground 5: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Da Costa In View Of Tsai.

1. Wistron uses hindsight to achieve the combination of Da Costa and Tsai, which is improper.

Ground 5 must be rejected because it is based on impermissible hindsight. Using the '305 patent to identify pieces of prior art and then simply pulling in additional references to fill in the gaps is firmly prohibited as amounting to

hindsight reconstruction by using the invention themselves.¹⁶¹ Impermissible hindsight must be avoided and the Board must be cautious of arguments that rely on such *ex post* reasoning.¹⁶²

Wistron violates these principles by alleging that the only missing element of Da Costa is a multiplexer. Not only does Da Costa fail to disclose much more than just a multiplexer, but the need for a multiplexer only becomes apparent based on facts gleaned from the '305 patent, not the alleged prior art. Indeed, Da Costa teaches away from a multiplexer by its use of a smart controller. A POSITA would not arrive at the claimed invention by combining a smart controller with a multiplexer because the '305 patent teaches against the use of microcontrollers, such as the smart controller disclosed in Da Costa.¹⁶³ A POSITA would further understand that the advantages of the '305 patent are achieved by using a multiplexer instead of a microcontroller, not in conjunction with a microcontroller.¹⁶⁴ A POSITA would only be led to the flawed combination of Da Costa and Tsai if a POSITA starts with the claimed elements of the '305 patent and seeks to find them in the alleged prior art.¹⁶⁵ Because this combination only makes sense in hindsight, it does render the challenged claims obvious.

¹⁶¹ See *KSR*, 550 U.S. at 421.

¹⁶² See *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361 (Fed. Cir. 2016).

¹⁶³ Exhibit 2010 at ¶50.

¹⁶⁴ *Id.*

¹⁶⁵ *Id.* at ¶¶50-51.

2. A POSITA would not be motivated to combine Da Costa with Tsai.

Contrary to what Wistron contends, a POSITA would not be motivated to combine Da Costa and Tsai to arrive at the claimed invention. Wistron merely asserts that a POSITA “would be motivated to search for other references in order to learn how to program the integrated flash memory” and “would have been motivated to look to Tsai when considering the implementation of the display control system.”¹⁶⁶ In essence, Wistron says nothing more than a POSITA, once presented with Da Costa and Tsai, would have understood that they could be combined. That is not enough.¹⁶⁷ “It does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.”¹⁶⁸ Wistron must explain why a POSITA would have been motivated to combine Da Costa and Tsai and how the combination was supposed to work, which Wistron does not do.¹⁶⁹

In fact, a POSITA would have no reason to combine Da Costa and Tsai. Da Costa already discloses internal multiplexers 413 and 754.¹⁷⁰ These multiplexers receive signals from the chip control circuitry 406 to select values from registers

¹⁶⁶ Paper 1 at pp. 56-57.

¹⁶⁷ See *PersonalWeb Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993 (Fed. Cir. 2017).

¹⁶⁸ *Id.*

¹⁶⁹ *Id.* at 994.

¹⁷⁰ Exhibit 1008 at Figs. 4a and 7b.

410. These registers contain digital values that correspond to analog reference levels.¹⁷¹ The register values can be dynamically adjusted by the host system for the smart controller chip 202. A POSITA would understand that the flash memory 303 provides pre-stored values that cannot be adjusted once the chip is made.¹⁷² Thus, Da Costa is not concerned with adding another multiplexer to address and program individual non-volatile storage cells in flash memory 303 because there is no need to address and program the flash memory after the chip is made.¹⁷³ A POSITA would not be motivated to add additional circuitry that they were already aware of to Da Costa for an unnecessary purpose.¹⁷⁴

Moreover, even assuming that a POSITA would be motivated to combine Da Costa and Tsai, which a POSITA would not, a POSITA would not have a reasonable expectation of achieving what is claimed in the '305 patent.¹⁷⁵ As noted above, Da Costa discloses multiplexers that receive signals from the chip control circuitry 406 to select analog reference values from registers 410.¹⁷⁶ Not only does Da Costa not use non-volatile storage cells to store these analog reference values, but Da Costa uses internal control circuitry to access these values

¹⁷¹ *Id.* at 2:47-49.

¹⁷² Exhibit 2010 at ¶53.

¹⁷³ *Id.*

¹⁷⁴ *Id.*

¹⁷⁵ See *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016).

¹⁷⁶ Exhibit 1008 at 9:1-29.

via a multiplexer.¹⁷⁷ A POSITA would not have a reasonable expectation of achieving the '305 patent by combining the additional circuitry disclosed in Tsai because that would defeat the intent of the inventors to create a less expensive, smaller, and thinner gamma reference architecture.¹⁷⁸

The '305 patent, on the other hand, advantageously provides a stand-alone solution such that it is not necessary to incorporate the control circuitry disclosed in Da Costa or the additional programming circuitry allegedly disclosed in Tsai.¹⁷⁹ One of the ways that the inventors of the '305 patent achieved this advantage is by simply using a multiplexer without additional control circuitry to address and program non-volatile storage cells.¹⁸⁰ Because a POSITA taking Da Costa would not be motivated to combine its teachings with Tsai and would not expect to achieve the invention of the '305 patent by the combination, the combined system does not provide a legitimate basis for finding the challenged claims obvious.

3. The combination of Da Costa and Tsai does not render the challenged claims obvious.

Even assuming that a POSITA would have been motivated to combine Da Costa with Tsai, which a POSITA would not, the resulting combination still would not disclose all of the elements of the challenged claims. Da Costa does not

¹⁷⁷ *Id.*

¹⁷⁸ Exhibit 2010 at ¶50.

¹⁷⁹ Exhibit 1001 at 2:33-35.

¹⁸⁰ *Id.* at 3:56-4:3.

merely lack a multiplexer, which Wistron claims is provided by Tsai. As discussed above, Da Costa fails to disclose several other elements of the challenged claims, which Wistron does not address. As such, the combined system of Da Costa in view of Tsai does not render the challenged claims obvious and the Petition to institute review on ground 5 should be denied.

F. Ground 6: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Tanaka In View Of Tsai.

1. Wistron uses hindsight to achieve the combination of Tanaka and Tsai, which is improper.

Ground 6 must be rejected because Wistron again resorts to impermissible hindsight.¹⁸¹ Wistron violates these principles by alleging that the only missing element of Tanaka is a multiplexer. Not only does Tanaka fail to disclose much more than just a multiplexer, but the need for a multiplexer only becomes apparent based on facts gleaned from the '305 patent, not the alleged prior art. Indeed, Tanaka teaches away from a multiplexer by its use of a controller.¹⁸² A POSITA would not arrive at the claimed invention by combining a controller with a multiplexer because the '305 patent teaches against the use of microcontrollers, such as the controller disclosed in Tanaka.¹⁸³ A POSITA would further understand that the advantages of the '305 patent are achieved by using a multiplexer instead

¹⁸¹ See *KSR*, 550 U.S. at 421; *Arendi*, 832 F.3d at 1361.

¹⁸² Exhibit 1010 at Figs. 25 and 33.

¹⁸³ Exhibit 2010 at ¶50.

of a microcontroller, not in conjunction with a microcontroller.¹⁸⁴ A POSITA would only be led to the flawed combination of Tanaka and Tsai if a POSITA starts with the claimed elements of the '305 patent and seeks to find them in the alleged prior art. Because this combination makes sense only in hindsight, it does render the challenged claims obvious.

2. A POSITA would not be motivated to combine Tanaka with Tsai.

Contrary to what Wistron contends, a POSITA would not be motivated to combine Tanaka and Tsai to arrive at the claimed invention. Wistron merely asserts that a POSITA “would be motivated to search for other references in order to learn how to program the non-volatile memory” and “would have been motivated to look to Tsai when considering the implementation of the display control system.”¹⁸⁵ In essence, Wistron says nothing more than a POSITA, once presented with Tanaka and Tsai, would have understood that they could be combined. That is not enough.¹⁸⁶ “It does not imply a motivation to pick out . . . two references and combine them to arrive at the claimed invention.”¹⁸⁷ Wistron must explain why a POSITA would have been motivated to combine Tanaka and

¹⁸⁴ *Id.* at ¶¶51-52.

¹⁸⁵ Paper 1 at p. 60.

¹⁸⁶ *See PersonalWeb*, 848 F.3d at 993.

¹⁸⁷ *Id.* at 993-994.

Tsai and how the combination was supposed to work, which Wistron does not do.¹⁸⁸

In fact, a POSITA would have no reason to combine Tanaka and Tsai. Tanaka discloses a controller that provides display data and control signals to the source driver.¹⁸⁹ Thus, a multiplexer is not needed because Tanaka already has control circuitry for selecting gamma correction data.¹⁹⁰ Also, a POSITA would understand that the non-volatile memory provides pre-stored values that cannot be adjusted once the chip is made.¹⁹¹ Thus, Tanaka is not concerned with adding a multiplexer to address and program the non-volatile memory because there is no need to address and program the memory after the chip is made.¹⁹² A POSITA would not be motivated to add additional circuitry for an unnecessary purpose.¹⁹³

Moreover, even assuming that a POSITA would be motivated to combine Tanaka and Tsai, which a POSITA would not, a POSITA would not have a reasonable expectation of achieving what is claimed in the '305 patent.¹⁹⁴ As noted above, Tanaka uses an external controller, which the '305 patent teaches

¹⁸⁸ *Id.* at 994.

¹⁸⁹ Exhibit 1008 at [0010].

¹⁹⁰ Exhibit 2010 at ¶¶46-47.

¹⁹¹ *Id.* at ¶49.

¹⁹² *Id.*

¹⁹³ *Id.*

¹⁹⁴ *See Intelligent Bio-Sys.*, 821 F.3d at 1367.

against.¹⁹⁵ A POSITA would not have a reasonable expectation of achieving the '305 patent by combining the additional circuitry disclosed in Tsai because that would defeat the intent of the inventors to create a less expensive, smaller, and thinner gamma reference architecture.¹⁹⁶

The '305 patent, on the other hand, advantageously provides a stand-alone solution such that it is not necessary to incorporate the controller disclosed in Tanaka or the additional programming circuitry allegedly disclosed in Tsai.¹⁹⁷ One of the ways that the inventors of the '305 patent achieved this advantage is by simply using a multiplexer without a microcontroller to address and program non-volatile storage cells.¹⁹⁸ Because a POSITA taking Tanaka would not be motivated to combine its teachings with Tsai and would not expect to achieve the invention of the '305 patent by the combination, the combined system does not provide a legitimate basis for finding the challenged claims obvious.

3. The combination of Tanaka and Tsai does not render the challenged claims obvious.

Even assuming that a POSITA would have been motivated to combine Tanaka with Tsai, which a POSITA would not, the resulting combination still would not disclose all of the elements of the challenged claims. Tanaka does not

¹⁹⁵ Exhibit 1001 at 2:33-35.

¹⁹⁶ Exhibit 2010 at ¶¶48-49.

¹⁹⁷ Exhibit 1001 at 2:33-35.

¹⁹⁸ *Id.* at 3:56-4:3.

merely lack a multiplexer, which Wistron claims is provided by Tsai. As discussed above, Tanaka fails to disclose several other elements of the challenged claims, which Wistron does not address. As such, the combined system of Tanaka in view of Tsai does not render the challenged claims obvious and the Petition to institute review on ground 6 should be denied.

G. Ground 7: The Challenged Claims Are Not Unpatentable Under 35 U.S.C. § 103(a) As Obvious Over Petropoulos In View Of Kang.

1. Ground 7 should be denied because it is redundant of grounds 1 and 3.

Ground 7 should be denied because it is redundant of grounds 1 and 3. Wistron fails to explain why ground 1 (Kang) and ground 3 (Petropoulos) are not redundant of ground 7 (Petropoulos in view of Kang). Wistron’s proposed three grounds rely on identical concepts and arguments. Wistron contends that Petropoulos and Kang “teach systems and methods for correcting images on a display.”¹⁹⁹ Wistron also asserts that Kang teaches “a gamma voltage correction apparatus.”²⁰⁰ Wistron further asserts that Petropoulos is “directed to a system for correcting corrupted elements, including gamma,”²⁰¹ and that the combined system contains a “detailed disclosure of the gamma correction process.” Wistron does

¹⁹⁹ Paper 1 at p. 62.

²⁰⁰ Paper 1 at p. 64.

²⁰¹ Paper 1 at p. 62.

not assert that Kang provides any of the claim elements missing from Petropoulos or vice versa. Instead, Wistron merely asserts ground 7 in the event that the Board concludes that “Petropoulos’ disclosure of gamma correction is insufficient to render the Challenged Claims obvious.” As such, Wistron’s grounds 1, 3, and 7 suffer from vertical redundancy.²⁰²

The Board has made clear that in order to ensure “the just, speedy, and inexpensive resolution of every proceeding,” it will not institute *inter partes* review proceedings on cumulative grounds.²⁰³ The Board has instructed parties that it will not “authorize *inter partes* review on certain unpatentability challenges . . . [where] the challenges appear to rely on the same prior art facts as other challenges for which *inter partes* review had been authorized.”²⁰⁴ Doing so “would unnecessarily consume the time and resources of all parties involved.”²⁰⁵

To avoid rejection of a proposed ground of unpatentability, Wistron must “provide a meaningful distinction between the different, redundant rejections.”²⁰⁶ Where multiple references have been cited for the same facts or disclosure,

²⁰² See, e.g., *Liberty Mut. Ins. Co. v. Progressive Casualty Ins. Co.*, CBM-2012-00003, Paper 59 at 3 (P.T.A.B. Oct. 25, 2012) (vertical redundancy “involves a plurality of prior art references applied both in partial combination and in full combination.”).

²⁰³ See, e.g., *Illumina, Inc. v. Trustees of Columbia Univ.*, IPR2012-00006, Paper 43 at 11 (P.T.A.B. May 10, 2013) (citing 37 C.F.R. § 42.1(b)).

²⁰⁴ *Id.*

²⁰⁵ *Id.*

²⁰⁶ *Id.*

Wistron must explain the differences between the references and “how this difference would impact the unpatentability challenge.”²⁰⁷ Specifically, with respect to vertical redundancy, Wistron “must articulate a reasonable basis to believe that from a certain perspective the base ground is stronger, and that from another perspective the ground with the additional reference is stronger.”²⁰⁸ In other words, if either the base ground or the additional ground is stronger from all perspectives, Wistron should only assert the stronger ground, so that the Board is not burdened with considering the weaker ground.²⁰⁹

Here, Wistron fails to provide any explanation as to how differences in the references would impact the unpatentability challenge. Indeed, Wistron fails to explain how Petropoulos combined with Kang is stronger than Petropoulos or Kang alone, or vice versa. As such, the Board should deny at least ground 7 as redundant.

2. A POSITA would not be motivated to combine Petropoulos with Kang.

Even if the Board does not deny ground 7 as redundant, which it should, a POSITA would not be motivated to combine Petropoulos and Kang to arrive at the claimed invention. Wistron merely asserts that a POSITA “would be motivated to

²⁰⁷ *Id.*

²⁰⁸ *See Liberty*, CBM-2012-00003, Paper 59 at 12.

²⁰⁹ *Id.*

search for other references for a more detailed disclosure of the gamma correction process and the process of programming correction value to the memory array” and “would have been motivated to look to Kang when considering the implementation of the display control system.”²¹⁰ In essence, Wistron says nothing more than a POSITA, once presented with Petropoulos and Kang, would have understood that they could be combined. That is not enough.²¹¹ “It does not imply a motivation to pick out . . . two references and combine them to arrive at the claimed invention.”²¹² Wistron must explain why a POSITA would have been motivated to combine Petropoulos and Kang and how the combination was supposed to work, which Wistron does not do.²¹³

In fact, a POSITA would have no reason to combine Petropoulos and Kang. Petropoulos discloses a memory array that can be programmed with data for gamma correction.²¹⁴ Wistron does not assert that Kang provides any of the missing elements of Petropoulos. Instead, Wistron’s arguments amount to nothing more than conclusory statements that a POSITA would have been motivated to combine the prior art references to obtain additional information regarding the gamma correction process and programming correction values to the memory

²¹⁰ Paper 1 at pp. 64-65.

²¹¹ *See PersonalWeb*, 848 F.3d at 993.

²¹² *Id.* at 993-994.

²¹³ *Id.* at 994.

²¹⁴ Exhibit 1009 at Abstract.

array, which are insufficient.²¹⁵ Wistron does not articulate why the additional information would benefit a POSITA when doing gamma correction of programming correction values.²¹⁶ Wistron also fails to explain the type of additional information a POSITA would obtain or how the POSITA would use that information.²¹⁷

Moreover, even assuming that a POSITA would be motivated to combine Petropoulos and Kang, which a POSITA would not, a POSITA would not have a reasonable expectation of achieving what is claimed in the '305 patent.²¹⁸ As noted above, Petropoulos uses an external controller that the '305 patent teaches against. A POSITA would not have a reasonable expectation of achieving the '305 patent by viewing Kang because Kang also teaches the use of a microcontroller to do gamma correction. Thus, both references run counter to the intent of the inventors to create a less expensive, smaller, and thinner gamma reference architecture.²¹⁹

The '305 patent, on the other hand, advantageously provides a stand-alone solution such that it is not necessary to incorporate the controller disclosed in

²¹⁵ See *In re NuVasive, Inc.*, 842 F.3d 1376, 1384 (Fed. Cir. 2016).

²¹⁶ *Id.*

²¹⁷ *Id.*

²¹⁸ See *Intelligent Bio-Sys.*, 821 F.3d at 1367.

²¹⁹ Exhibit 2010 at ¶¶37, 45.

Petropoulos or Kang.²²⁰ One of the ways that the inventors of the '305 patent achieved this advantage is by simply using a multiplexer without a microcontroller to address and program non-volatile storage cells.²²¹ Because a POSITA taking Petropoulos would not be motivated to combine its teachings with Kang and would not expect to achieve the invention of the '305 patent by the combination, the combined system does not provide a legitimate basis for finding the challenged claims obvious.

3. The combination of Petropoulos and Kang does not render the challenged claims obvious.

Even assuming that a POSITA would have been motivated to combine Petropoulos with Kang, which a POSITA would not, the resulting combination still would not disclose all of the elements of the challenged claims. As discussed above, Petropoulos fails to disclose several elements of the challenged claims, which Wistron does not address. As such, the combined system of Petropoulos in view of Kang does not render the challenged claims obvious and the Petition to institute review on ground 7 should be denied.

IX. CONCLUSION.

In conclusion, Wistron's Petition is time barred because it was filed more than one year after the date its privy, Vizio, was served with a complaint alleging

²²⁰ Exhibit 1001 at 2:33-35.

²²¹ *Id.* at 3:56-4:3.

infringement of the '305 patent. Regardless, the Petition is not reasonably likely to prevail on any of the grounds asserted against the challenged claims of the '305 patent. Accordingly, all grounds to institute review should be denied.

Respectfully submitted,

By: /s/ Lewis E. Hudnell, III
Nicolas S. Gikkas, *Lead Counsel*
Reg. No. 46,245
The Gikkas Law Firm, P.C.
530 Lytton Avenue
2nd Floor
Palo Alto, CA 94301
Telephone: (650) 617-3419
Facsimile: (650) 618-2600
nsg@gikkaslaw.com

Lewis E. Hudnell, III
Reg. No. 51,185
Hudnell Law Group P.C.
800 W. El Camino Real
Suite 180
Mountain View, CA 94040
T: (650) 564-7720
F: (347) 772-3034
lewis@hudnelllaw.com

CERTIFICATE OF WORD COUNT

Under 37 C.F.R. § 42.24, I certify that Sections I-IX of this Preliminary Response have a total of 11,646 words according to the word count tool in Microsoft Word™.

By: /s/ Lewis E. Hudnell, III
Lewis E. Hudnell, III
Reg. No. 51,185

CERTIFICATE OF SERVICE

I certify that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE TO PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,233,305 was served on October 29, 2018 on the Petitioner by filing this document through the PTAB's E2E System as well as e-mailing a copy to Benjamin.weed.ptab@klgates.com and jake.vannette@klgates.com.

By: /s/ Lewis E. Hudnell, III
Nicolas S. Gikkas, *Lead Counsel*
Reg. No. 46,245
The Gikkas Law Firm, P.C.
530 Lytton Avenue
2nd Floor
Palo Alto, CA 94301
Telephone: (650) 617-3419
Facsimile: (650) 618-2600
nsg@gikkaslaw.com

Lewis E. Hudnell, III, *Back up Counsel*
Reg. No. 51,185
Hudnell Law Group P.C.

800 W. El Camino Real
Suite 180
Mountain View, CA 94040
T: 650-564-7720
F: 347-772-3034
lewis@hudnelllaw.com