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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WISTRON CORPORATION,
Petitioner,

v.

PHENIX LONGHORN, LLC,
Patent Owner.

Case IPR2018-01255
Patent 7,233,305 B1

Before DENISE M. POTHIER, DAVID C. MCKONE, and KAMRAN JIVANI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314(a)

I. INTRODUCTION

Wistron Corporation ("Petitioner")[1] filed a Petition requesting an *inter partes* review of claims 1, 2, 4, and 5 of U.S. Patent No. 7,233,305 B1 (Ex. 1001, "the '305 patent"). Paper 1 ("Pet."), 1. Phenix Longhorn, LLC ("Patent Owner") filed a Preliminary Response to the Petition. Paper 10 ("Prelim. Resp."). Patent Owner filed two, separate motions to seal Exhibits 2001 and 2009 as well as its Preliminary Response, each in its entirety. Papers 7, 11. These motions will be addressed in a separate order.[2]

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons stated below, we determine that the "information presented" does not "show[] there is a reasonable likelihood that . . . [P]etitioner would prevail with respect to at least 1 of the claims challenged." *See id.* Accordingly, we do "not authorize an *inter partes* review to be instituted." *See id.*

A. Related Proceedings

Petitioner and Patent Owner submit the '305 patent is presently being asserted against Petitioner in Eastern District of Texas Case No. 2:17:cv-00711-RWS and against Texas Instruments in Eastern District of Texas Case

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[1] Petitioner Wistron Corporation identifies itself as a real party-in-interest and states Wistron InfoComm (Zhongshan) Corporation, Zhongshan Torch Development Zone, and Wistron Mexico S.A. de C.V. "may be real parties-in-interest." Paper 3, 2.

[2] This Decision does not reproduce or discuss any material the Motions to Seal identify as confidential. Accordingly, this Decision need not be sealed.

No. 2:18-cv-00020-RWS. Pet. viii; Paper 4, 2.[3] Petitioner also identifies two actions in which Patent Owner asserted the '305 patent against multiple parties. Pet. viii..

B. The '305 Patent

The '305 patent is titled "Gamma Reference Voltage Generator" and is used with Liquid Crystal Displays (LCDs). Ex. 1001, Title, 1:12–14. Petitioner explains the brightness versus input voltage curve for a display's image does not match those of a human's vision and establishes a non-linear behavior called "gamma." *See* Pet. 1–2 (citing Ex. 1002 ¶ 25); *see also* Pet. 2–3 (reproducing Ex. 1008, Fig. 6); *see also* Prelim. Resp. 5 (stating "the brightness of the LCD pixel is not a linear or straight-line function of the voltages applied" and "the human eye's sensitivity to light is also not linear") Due to this mismatch, the curve needs to be adjusted using gamma correction. *See* Pet. 1–2 (citing Ex. 1002 ¶ 25); *see also* Prelim. Resp. 5 (discussing controlling gamma reference voltages). The '305 patent indicates gamma correction has been a problem for Thin Film Transistor (TFT) flat panel displays. Ex. 1001, 1:19–21. Often, each display has a different response to the gamma correction reference voltages, which results in a need to generate specific gamma reference voltages for each display's model. Ex. 1001, 1:22–25.

Traditionally, this problem has been solved using Select-On-Test Resistors, allowing reference voltages (e.g., $GM_{1–16}$ of Fig. 1) to be fine-tuned to the display's requirements using specific resistors (e.g., R_{1-17} of Fig. 1). Ex. 1001, 1:27–34, 1:46–2:3, Fig. 1. However, this process

[3] Patent Owner mistakenly lists "2:18-cv-00720-RWS" rather than 2:18-cv-00020-RWS.

prohibits automatic assembly and testing and requires resistors to be tested, selected, and mounted manually. Ex. 1001, 1:31–34. The ’305 patent’s invention is “a programmable buffer integrated circuit which can be programmed to output a set of gamma correction reference voltages to be used in Liquid Crystal Displays (LCDs).” Ex. 1001, 2:16–19; *see also id.* at 2:45–51, Figs. 2–3. The described invention includes “automated assembly of an entire PC board” (Ex. 1001, 2:29–30), “automated test and gamma adjustment” (Ex. 1001, 2:30–31, 3:38–41, Fig. 2), and reprogramming gamma characteristics using gamma reference controllers (e.g., 210 and 220) (Ex. 1001, 2:32–33, 3:41–47, Fig. 2).

The ’305 patent further states that the integrated circuit can store and retrieve reference voltages’ banks using address inputs B0, B1, and B2. Ex. 1001, 5:50–53, 6:41. These inputs allow gamma voltages to be changed and can be used to switch between different gamma settings. Ex. 1001, 5:53–62, Fig. 6. “Having bank switching capability ensures that the optimum gamma curve is used for each individual display and eliminates the need for re-work due to display manufacturing process variations.” Ex. 1001, 7:9–12.

C. Illustrative Claim

Petitioner challenges claims 1, 2, 4, and 5 of the ’305 patent. Claim 1 is representative and is reproduced below with bracketing added by Petitioner:

> 1. An integrated circuit for producing voltage signals on a plurality of outputs comprising:
>
> [a] a plurality of non-volatile storage cells;
>
> [b] circuits for programming coupled to a multiplexer for addressing and programing said storage cells, wherein the addressing is based on a plurality of inputs;
>
> [c] drivers connected to said multiplexer for addressing said storage cells; and
>
> [d] the plurality of inputs connected to said multiplexer for addressing said storage cells;
>
> [e] wherein said voltage signals are gamma reference voltage signals for determining actual driving voltages of columns of a display,
>
> [f] wherein said non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition; and
>
> [g] means to switch between the banks based on one or more external signals is provided on said integrated circuit.

Pet. 68; Ex. 1010, 7:45–62 (the above limitations are referred to as "limitation [a]," "limitation [b]," "limitation [c]," "limitation [d]," "limitation [e]," "limitation [f]," and "limitation [g]" throughout the Decision).

D. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1, 2, 4, and 5 of the '305 patent on the following grounds (Pet. 17):

Reference(s)	**Basis**	**Claims challenged**
Kang[4] (Ex. 1007)	§ 103(a)[5]	Claims 1, 2, 4, and 5
Da Costa[6] (Ex. 1008)	§ 103(a)	Claims 1, 2, 4, and 5
Petropoulos[7] (Ex. 1009)	§ 103(a)	Claims 1, 2, and 5
Tanaka[8] (Ex. 1010)	§ 103(a)	Claims 1, 2, 4, and 5
Da Costa and Tsai[9] (Ex. 1011)	§ 103(a)	Claims 1, 2, 4, and 5
Tanaka and Tsai	§ 103(a)	Claims 1, 2, 4, and 5
Petropoulos and Kang	§ 103(a)	Claims 1, 2, 4, and 5

Petitioner also relies on the Declaration of Thomas L. Credelle. Ex. 1002. Patent Owner relies on the Declaration of Robert J. Murphy. Ex. 2010.

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[4] U.S. Patent Application Publication No. 2002/0063666 A1 ("Kang").
[5] The Leahy-Smith America Invents Act (AIA), which amended 35 U.S.C. § 103, was signed into law in 2011. The AIA's amendments to § 103 apply to applications filed on or after March 16, 2013. Because the '305 patent's filing date is prior to March 16, 2013, we refer to the pre-AIA version of § 103.
[6] U.S. Patent No. 6,100,879 ("Da Costa").
[7] U.S. Patent Application Publication No. 2003/0090580 A1 ("Petropoulos").
[8] U.S. Patent Application Publication No. 2003/0132906 A1 ("Tanaka").
[9] U.S. Patent No. 5,974,528 ("Tsai").

II. ANALYSIS

A. Person of Ordinary Skill in the Art ("POSITA")

Petitioner asserts that a person of ordinary skill in the art at the time of the invention "would have had at least a bachelor of science degree in physics, electrical engineering, or the equivalent thereof and three (3) years of experience in circuit design or display technologies." Pet. 13 (citing Ex. 1002 ¶ 21). Petitioner adds, "[s]uch a POSA[10] would have had knowledge of integrated circuits, gamma correction, and storage of gamma correction voltage values within memory, and would have understood how to search available literature for relevant publications." Pet. 13–14 (citing Ex. 1002 ¶¶ 21–22). Petitioner support its position with Mr. Credelle's testimony. Ex. 1002 ¶¶ 21–22, *cited in* Pet. 13–14.

Patent Owner describes the ordinary artisan similarly, indicating the artisan would have had "at least a bachelor's of science degree in electrical engineering or physics or a related field, with at least three years of experience in the design of floating gate nonvolatile memory integrated circuits either as memory chips or embedded technology or floating gate analog design or technology." Prelim. Resp. 16–17. Patent Owner adds "[t]his person would be aware of the state of the art in floating gate non-volatile technology and circuits by reading articles published in" various journals and patents and by attending presentations at conferences. Prelim. Resp. 17. Mr. Murphy reiterates Patent Owner's summary. Ex. 2020 ¶ 28.

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[10] Like POSITA, POSA also stands for a person of ordinary skill in the art. Petitioner and Mr. Credelle use this acronym and POSITA interchangeably.

Upon review, the parties present similar skill levels for an ordinary artisan. Neither party asserts the differences in the proposed skill level would impact what an ordinary artisan would have known or recognized in the cited prior art. *See generally* Pet.; Prelim. Resp. Under either proposed skill level, our conclusions related to the proposed grounds remain the same. We further note that the prior art itself demonstrates the level of skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required "where the prior art itself reflects an appropriate level and a need for testimony is not shown") (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

B. Claim Construction

For petitions filed before November 13, 2018, the Board interprets claim terms in an unexpired patent according to the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 100(b) (2016); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (affirming applicability of broadest reasonable construction standard to *inter partes* review proceedings). Under that standard, and absent any special definitions, we generally give claim terms their ordinary and customary meaning as would be understood by one of ordinary skill in the art at the time of the invention. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

1. "Non-volatile storage cells"

Petitioner and Patent Owner agree the phrase "non-volatile storage cells" in claim 1 means "computer memory that retains its stored data after power is removed and restores the data when power is returned to the system, such as, for example, the following: analog floating gate

non-volatile memory, Electrically Erasable Programmable Read Only Memory (EEPROM), Flash EEPROM, Ultraviolet EPROM (UVEPROM), and Non-Volatile Random Access Memory (NOVRAM)." Pet. 15–16 (citing Ex. 1002 ¶¶ 45–47); Prelim. Resp. 17. For purposes of this Decision, we adopt the parties' agreed construction.

2. Limitation [g]
"Means to switch between the banks
based on one or more external signals"
a. 37 C.F.R. § 42.104(b)(3)

37 C.F.R. § 42.104(b)(3) recites, in relevant part, that an *inter partes* petition must provide a statement of the precise relief requested for each claim challenged and that the statement must identify "[h]ow the challenged claim is to be construed" and "[w]here the claim to be construed contains a means-plus-function . . . limitation as permitted under 35 U.S.C. 112[, sixth paragraph], the construction of the claim must identify the specific portions of the specification that describe the structure, material, or acts corresponding to the each claimed function."[11]

As explained below, we determine the "means to switch" limitation of claim 1 contains a means-plus-function limitation invoking 35 U.S.C. § 112, sixth paragraph. Petitioner does not provide a claim construction for this phrase. *See* Pet. 14–16. Patent Owner notes Petitioner's failure to construe this phrase. Prelim. Resp. 18. At best, Petitioner indicates "each term of the Challenged Claims of the '305 Patent [should] have its ordinary and customary meaning." Pet. 14.

[11] As previously discussed, the pre-AIA statutes are applicable to the '305 patent.

Because Petitioner has not presented a claim construction for the recited "means to switch" limitation, including identifying portions of the Specification that describe its structure, material, or acts corresponding to its claimed function as set forth in 37 C.F.R. § 42.104(b)(3), we deny institution of the Petition on this basis. Nevertheless, we proceed to construe this term and address the merits of the Petition, and, as discussed below, find additional grounds for denial.

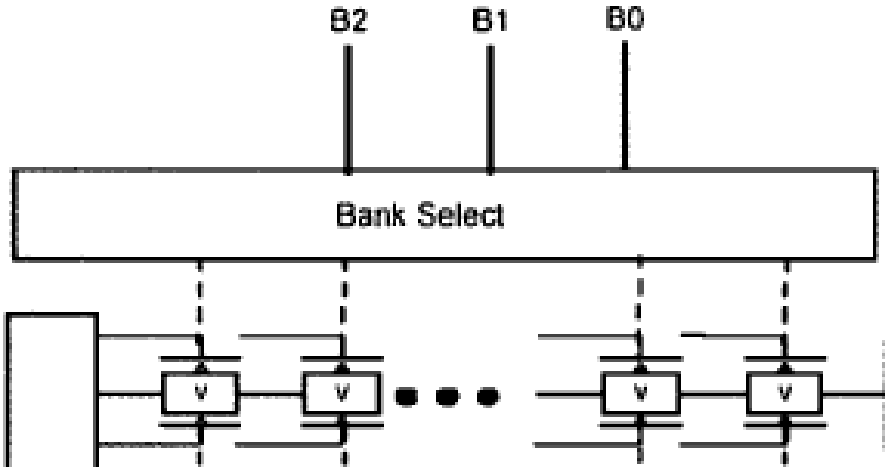
b. Provided Claim Construction

Patent Owner asserts that the "means" phrase in claim 1 "recites a means for performing a specified function" and "must be construed as a means-plus-function limitation under 35 U.S.C. § 112[, sixth paragraph]." Prelim. Resp. 18. As noted above, Petitioner does not provide a claim construction for this phrase (*see* Pet. 14–16) but indicates "each term of the Challenged Claims of the '305 Patent [should] have its ordinary and customary meaning." Pet. 14.

Patent Owner states "[t]he function for th[e] limitation [[g]] is switching between the banks based on one or more external signals" and identifies the function's "corresponding structure" to include (1) the "B0-B2 address inputs" (Prelim. Resp. 18 (citing Ex. 1001, 5:50–63, Figs. 4A-B)), (2) pins for these inputs, and (3) an internal damping circuit referred to as "Bank Switch Damp Time" (Prelim. Resp. 19 (citing Ex. 1001, 5:62–66, Fig. 5)). More specifically, Patent Owner asserts the structure is shown in (1) Figure 4A as pins B0–B2 (the "Bank Select") corresponding to Figure 4B's pins 20, 22, and 23 and (2) Figure 6, depicting the Bank Select block with inputs B0, B1, and B2. Prelim. Resp. 18–19 (citing Ex. 1001, 5:50–63, Figs. 4A– 6).

We agree with Patent Owner that the recited phrase "means to switch between the banks based on one or more external signals" in claim 1 invokes 35 U.S.C. § 112, sixth paragraph. A phrase that uses the term "means" creates a presumption that § 112, sixth paragraph applies. *TriMed, Inc. v. Stryker Corp.*, 514 F.3d 1256, 1259 (Fed. Cir. 2008). Also, "[m]eans-plus-function claiming applies only to purely functional limitations that do not provide the structure that performs the recited function." *Phillips v. AWH Corp.*, 415 F.3d at 1311 (Fed. Cir. 2005); *see also Welker Bearing Co. v. PHD, Inc.*, 550 F.3d 1090, 1095–96 (Fed. Cir. 2008). The recited functional limitation of "switch[ing] between the banks based on one or more external signals" in claim 1 does not provide the structure that performs this recited function. For example, claim 1 does not recite a specific circuit, algorithm, or damping circuit involved in performing the claimed function. Thus means-plus-function claiming applies to limitation [g].

The '305 patent describes an integrated circuit "termed the AG1818" having the capacity to retrieve eight independent banks. Ex. 1001, 5:30–31, 5:50–52. The '305 patent states the AG 1818's "banks of gamma voltage are . . . selected through the three address inputs B0, B1, and B2" (Ex. 1001, 5:52–53) and "the bank [is] selected by the B0-B2 address inputs" (Ex. 1001, 5:61–62). Address signals B0 through B2 are shown in Figure 6. Ex. 1001, Fig. 6. Part of Figure 6's block diagram is reproduced below with address signals, B0, B1, and B2 entering a "Bank Select" block:



Part of Figure 6's Block Diagram of an Alternative Embodiment

Ex. 1001, 2:56–57, 5:58–59. The '305 patent further states, "This feature can also be used to switch between different gamma settings based on the information to be displayed for implementing dynamic gamma correction." Ex. 1001, 5:56–58. Figure 4A further describes B0 through B2 as "Bank Select" signals (Ex. 1001, Fig. 4A), later explaining "the particular bank is addressed through B0-B2" (Ex. 1001, 6:41). Based on this description, we agree with Patent Owner that the structure corresponding to the means to switch is the B0–B2 address inputs, pins for these inputs, the bank select box, and equivalents thereof.

Additionally, the '305 patent describes "an internal damping circuit" that can be used during "read mode" to "create[] a slow transition, about 10 msec., between banks to prevent disruptive display artifacts." Ex. 1001, 5:60, 5:62–64, Fig. 5 (showing and describing "Tdamp" and "Bank Switch Damp Time"); *see also* Ex. 1001, 5:66–6:2. We agree with Patent Owner that the described internal damping circuit in the '305 patent, and equivalents thereof, are additional structure corresponding to performing the function of switching between the banks based on external signals.

Although neither party construes the following terms, we present a claim construction to address the grounds presented in the Petition.

c. "a multiplexer"

The '305 patent discusses and shows a multiplexer (e.g., mux 320) that connects signals from programming engine 310 to "any one of the programmable analog floating gate memory cells 330 through 337, depending on three address inputs (A_0, A_1, and A_2)." Ex. 1001, 3:56–4:3, Fig. 3; Ex. 1002 ¶ 30 (citing same). Although this describes the recited "multiplexer," this discussion and Mr. Credelle's accompanying testimony (Ex. 1002 ¶ 30 (stating "the multiplexer . . . is a device used to select which memory cell is addressed by the 'plurality of inputs' A_0, A_1, and A_2")) merely address the result of using a multiplexer rather than what a multiplexer is. Thus, we consult a dictionary for a customary understanding of "multiplexer" to an ordinarily skilled artisan.

THE AUTHORITATIVE DICTIONARY OF IEEE STANDARD TERMS defines a "multiplexer" as:

> multiplexer (A) (supervisory control, data acquisition, and automatic control) A device that allows the interleaving of two or more signals to a single line or terminal. (B) (supervisory control, data acquisition, and automatic control) A device for selecting one of a number of inputs and switching its information to the output.
>
> (2) (A) A device that allows the transmission of a number of different signals simultaneously over a single channel or transmission facility. Synonym: multiplexor. (B) A device capable of interleaving the events of two or more activities or of distributing the events of an interleaved sequence to their respective activities. Contrast: demultiplexer

THE AUTHORITATIVE DICTIONARY OF IEEE STANDARD TERMS 716 (Kim Breitfelder & Don Messina eds., St'd Info. Network IEEE Press 7th ed. 2000).

Figure 3 of the '305 patent shows six signals entering multiplexer 320 and three exit to "any one of the programmable analog floating gate memory cells 330 through 337, depending on three address inputs (A_0, A_1, and A_2)." Ex. 1001, 3:56–4:3, Fig. 3. This multiplexer arrangement is more than a device that allows simultaneous transmission of different signals over a single channel like above definition (2). Rather, the description in the specification is most consistent with the first definition quoted above.

Accordingly, consistent with the '305 patent's Specification, we determine the recited "multiplexer" includes a device that interleaves signals to a single line, or selects one input and switches its information to the output.

d. "banks of cells"

The '305 patent states the integrated circuit, termed the AG1818, has the capacity for eight banks, which are selected through three address signals B0 through B2 (not shown). Ex. 1001, 5:30–31, 50–53, Fig. 4. But, the '305 patent does not show or define a cell's bank. *See generally* Ex. 1001. Given the absence of any explicit definition, we generally give the term "bank" its ordinary and customary meaning as would be understood by one of ordinary skill in the art at the time of the invention.

Consulting THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS, the definition of "bank" most relevant to this proceeding is the following:

> (2) (A) One or more disk drives lined up in a row. (B) Any group of similar devices that are connected together for use as a single

> device. For example, a row of light-emitting diodes connected to form a display. (C) A contiguous section of addressable memory. For example, eight memory devices, each of which is 64 kB by 1; forming a 64 kB X 8 memory bank.

THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS 85 (Kim Breitfelder & Don Messina eds., St'd Info. Network IEEE Press 7th ed. 2000) (def. 2).

Because, as noted above, both Petitioner and Patent Owner agree the recited "storage cells" relate to computer memory, we conclude definition 2(C) is the most relevant to the phrase "banks of cells." Thus, we determine the claimed "banks of cells" are contiguous sections of addressable, computer memory.

No other claim term requires express construction.

C. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.[12] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

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[12] Neither party presents arguments regarding objective evidence of nonobviousness here.

D. Obviousness Grounds

Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over seven grounds. Pet. 17–66. Patent Owner present arguments contending the grounds do not teach or suggest claim 1's preamble and limitations [b]–[d], [f] and [g]. Prelim. Resp. 22–62 . Having reviewed Petitioner's assertions, Patent Owner's arguments, and the references, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing the unpatentability of the challenged claims based on any of the above-identified grounds. We focus on independent claim 1 for each of the proposed grounds.

1. Kang (Ex. 1007)

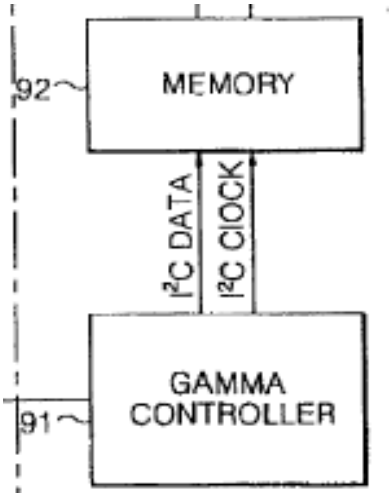
Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over Kang under 35 U.S.C. § 103(a). Pet. 18–30. To support its contentions, Petitioner cites to Mr. Credelle's declaration testimony (Ex. 1002). Patent Owner presents several arguments, including that Kang does not teach or suggest claim 1's preamble and limitations [b], [d], [f], and [g]. Prelim. Resp. 22–27. Patent Owner cites to Mr. Murphy's declaration testimony (Ex. 2010).

For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Kang renders claim 1 obvious. We focus on limitations [b], [f], and [g].

As background, Kang discusses "[a] gamma voltage and video data correcting apparatus and method in a liquid crystal display . . . , wherein the gamma data for controlling the gamma voltage is stored for each of at least two modes." Ex. 1007, Abstract.

a. Limitation [b]
"circuits for programming coupled to a multiplexer for addressing and programing said storage cells"

For this limitation, Petitioner maps Kang's gamma controller 91 to a "circuit for programming."[13] Pet. 24–25 (citing Exs. 1007 ¶ 52 and 1002 ¶ 55). Petitioner states the gamma controller circuit is coupled to storage cells (e.g., memory 92 in Fig. 9) through an I^2C interface, which Petitioner contends is "a common serial interface." Pet. 24 (citing Exs. 1007 ¶ 52 and 1002 ¶ 55). Petitioner argues Kang's I^2C interface provides instructions as to where in the memory the data is to be written. *Id.* (citing Exs. 1007 ¶ 52 and 1002 ¶ 55). Kang's I^2C interface, shown in Figure 9, follows:



Partial View of Kang's Figure 9 showing an I^2C interface.

Petitioner concludes an ordinarily skilled artisan "would have understood that the use of a serial interface over a multiplexer is an obvious modification . . . because, since a multiplexer and an I^2C serial interface perform identical functions within an integrated circuit, these commodity components are replaceable and do not alter the operation of the device."

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[13] Claim 1 recites "circuit*s* for programming" not "circuit for programming." Ex. 1001, 7:48 (emphasis added).

Pet. 24 (citing Ex. 1002 ¶ 55 and *In re Japikse*, 181 F.2d 1019 (CCPA 1950)).

Patent Owner rebuts. Prelim. Resp. 23–25. Patent Owner argues Petitioner "does not explain where Kang discloses a multiplexer because Kang does not." Prelim. Resp. 24 (citing Ex. 1002 ¶ 57). Petitioner does not contend otherwise. Pet. 24 (noting Kang discloses an I^2C serial interface and proposing to modify the serial interface with a multiplexer). That is, Kang discloses that an I^2C connects gamma controller 91 to memory 92 and transmits I^2C data and clock data to memory 92. Ex. 1007 ¶ 52, Fig. 9. On the current record, Kang does not disclose the recited "multiplexer" of claim 1.

Patent Owner also contends Petitioner provides no support through its expert or documentary evidence for the statement that an artisan would have understood that the use of a serial interface instead of a multiplexer is an obvious modification. Prelim. Resp. 24. Patent Owner argues that "a multiplexer and an I^2C serial interface do not perform the same function within an integrated circuit and therefore are not interchangeable." Prelim. Resp. 25 (citing Ex. 2010 ¶¶ 39–40). We agree with Patent Owner for the following reasons.

Mr. Credelle testifies that an I^2C serial interface is a common serial interface. Ex. 1002 ¶ 55 (citing Ex. 1013[14]). We agree Exhibit 1013 supports that an I^2C bus, which is shown in Kang's Figure 9, includes a serial data line and serial clock line. Ex. 1013, p. 1 § 1.0. Exhibit 1013 also outlines various "features of the I^2C bus," including having two bus lines

[14] Philips Semiconductors, THE I^2C-BUS AND HOW TO USE IT (INCLUDING SPECIFICATIONS) 1–24 (1995).

(data and clock), data corruption properties (e.g., collision detection and arbitration), bidirectional data transfer, and on-chip filtering. Ex. 1013, p. 1 § 1.0.

Comparing the above understandings of "multiplexer" with an I^2C bus, we disagree the two perform identical functions as Petitioner asserts. Pet. 24. A multiplexer functions to interleave signals to a single line or to select one input and switch its information to the output. *Id.* An I^2C bus, like that in Kang and like that discussed in Exhibit 1013, does not discuss interleaving signals to a single line (e.g., the I^2C data with I^2C clock), or selecting one input and switching its information to the output. For example, Kang shows and describes that its I^2C lines separately enter memory 92 but does not discuss interleaving signals or switching its information. Ex. 1007 ¶ 52, Fig. 9. Nor does our understanding of a multiplexer's functions include performing data corruption, bidirectional data transfer, and on-chip filtering, like that of an I^2C bus. Ex. 1013, p. 1 § 1.0. Mr. Murphy also testifies an ordinary artisan would not understand an I^2C interface is equivalent to a multiplexer. Ex. 2010 ¶ 39.

Moreover, Petitioner's evidence does not support its contention that a skilled artisan would have made the "simple . . . design choice" of modifying Kang with a multiplexer. Pet. 24; *see Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention."). Petitioner cites Mr. Credelle's testimony. Pet. 24 (citing Ex. 1002 ¶ 55). Mr. Credelle, however, does not testify that it would have been obvious to modify Kang. Rather, Mr. Credelle testifies that Kang discloses a multiplexer, which, as noted above, is not Petitioner's contention.

Ex. 1002 ¶ 55 ("As already discussed, flash memory includes multiplexers, e.g., row and column decoders, to determine where to write data."). Thus, the Petition is deficient for failing to identify a reason to modify Kang.

As to Mr. Credelle's testimony that flash memory includes multiplexers to determine where to write data, Mr. Credelle cites, without specificity, to Exhibit 1014. Ex. 1002 ¶ 55 n.6 (citing Ex. 1014[15]). Exhibit 1014 discusses flash memory and non-volatile memory, such as EEPROM, EEPROM, and Flash (Ex. 1014, pp. 1–2), and Kang discloses that memory 92 can be EEPROM or EPROM (Ex. 1007 ¶ 53, *noted in* Ex. 1002 ¶ 61). However, Mr. Credelle does not identify where Exhibit 1014 discusses or addresses multiplexers. Thus, just as Petitioner or its expert has not identified where Exhibit 1014 demonstrates flash memory includes a multiplexer, one skilled in the art would not have recognized that Kang's memory includes a multiplexer.

As for Mr. Credelle testimony that "[a]s already discussed, flash memory includes multiplexers, e.g., row and column decoders, to determine where to write data," Mr. Credelle does not cite to any particular support for this statement. Ex. 1002 ¶ 55. Presuming he refers to paragraphs 30 through 32 under Section C, titled "Multiplexer for Addressing Memory" (Ex. 1002, p. 12),[16] this testimony merely supports Petitioner's argument that a multiplexer is any device used to select a memory cell addressed by a plurality of address inputs, an argument we reject above.

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[15] Roberto Bez et al., *Introduction to Flash Memory*, 91 PROC. OF THE IEEE 1–14 (2003).

[16] Mr. Credelle first discusses a flash memory cell that uses row and column decoders under this section.

In paragraphs 30 through 32, Mr. Credelle discusses how the ’305 patent describes a multiplexer that connects signals from an engine to storage cells. Ex. 1002 ¶ 30 (citing Ex. 1001, 3:56–4:3). From this discussion, Mr. Credelle defines a “multiplexer” in claim 1 as “a device used to select which memory cell is addressed by the ‘plurality of inputs’ A_0, A_1, and A_2.” Ex. 1002 ¶ 30. But, as noted above, a multiplexer is not simply any device that selects a memory cell based on a plurality of address inputs. Rather, it is a device that interleaves signals to a single line or selects one input and switches its information to the output.

Lastly, we note the proposed ground relies on Kang alone, not Kang and Fazio,[17,18] to teach claim 1’s limitation [b]. Pet. 18, 24–25. As proposed, we determine an ordinary artisan would not have understood that using a multiplexer over Kang’s I^2C bus interface “is an obvious modification” and that the an I^2C bus interface is replaceable by the multiplexer without altering Kang’s device. Pet. 24.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Kang renders obvious limitation [b] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner’s showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 28–30.

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[17] Ex. 1012 (U.S. Patent No. 5,677,869 (Oct. 14, 1997) (“Fazio”), *noted in* Ex. 1002 ¶¶ 31–32.

[18] *In re Hoch*, 428 F.2d 1341, 1342 n.3 (CCPA 1970) (“Where a reference is relied on to support a rejection, whether or not in a ‘minor capacity,’ there would appear to be no excuse for not positively including the reference in the statement of the rejection.”).

b. Limitation [f]
"said non-volatile storage cells are organized into two or more banks of cells"

For this limitation, Petitioner points to two passages in Kang. Pet. 27–28. Petitioner notes Kang discloses a gamma voltage correcting apparatus includes memory "for storing gamma data for controlling a gamma voltage for each of at least two modes." Pet. 27 (citing Ex. 1007 ¶ 22 and Ex. 1002 ¶ 59). Petitioner further indicates Kang discloses four modes with different gamma voltages. Pet. 27–28 (citing Ex. 1007 ¶ 59 (Table I) and Ex. 1002 ¶ 59); Ex. 1002 ¶ 61 (citing Ex. 1007 ¶¶ 59–60). Petitioner asserts an ordinary artisan would have understood the two or more modes as disclosed by Kang demonstrates Kang's gamma generator has two or more banks. Pet. 28 (citing Ex. 1002 ¶ 59).

Patent Owner disagrees. Prelim. Resp. 26. Patent Owner argues Kang discloses memory block 92 with no details how the memory is organized. Prelim. Resp. 26. We agree. Kang discloses multi-mode gamma voltage generator 84 having memory 92, which can be an EEPROM or EPROM. Ex. 1007 ¶¶ 51–53, Figs. 8–9. No further information related to memory 92's design or architecture is provided. *See* Ex. 1007 ¶¶ 51–53, Figs. 8–9. Even more, Kang does not teach or suggest that the modes are organized in memory as contiguous sections of addressable, computer memory (i.e., as "banks" as construed above).

Kang also discusses "storing a gamma data for controlling a gamma voltage for each of at least two modes." Ex. 1007 ¶ 22, Abstract. Kang addresses "gamma reference voltages . . . for each mode, Modes A to D" and provides TABLE 1, showing modes A to D. Ex. 1007 ¶ 59. Quoting from these same passages, Mr. Credelle determines "Kang clearly teaches that the

multi-mode gamma generator has two or more banks that contain predetermined gamma reference voltages." Ex. 1002 ¶ 59. Relying on Mr. Credelle's testimony and Kang's multi-mode discussion, Petitioner concludes an ordinary skilled artisan would have understood this discussion of "modes" equates to banks. *See* Ex. 1002 ¶ 59. We find this position unpersuasive.

As noted above, Kang does not discuss organizing its memory using banks of two or more contiguous memory portions. Ex. 1007 ¶¶ 51–53, Figs. 8–9. Additionally, Kang does not discuss how the mode's data would be stored in memory, such that they suggest, to one skilled in the art, organizing the cells into "two or more banks" as recited. Ex. 1007 ¶¶ 22, 59, Abstract. Mr. Credelle's testimony on this feature relies on the same passages without further explanation of how Kang's modes suggest organizing Kang's memory into two or more banks. Ex. 1002 ¶ 59.

For the previous reasons, Petitioner does not show sufficiently for institution purposes that Kang renders obvious limitation [f]. Claims 2, 4, and 5 depend respectively from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 28–30.

c. Limitation [g]
"means to switch between the banks based on one or more external signals"

Petitioner contends the gamma generator switches between modes using the disclosed control means that accesses data, and a LCD receives an external mode signal to select gamma data from memory. Pet. 28 (citing Exs. 1007 ¶ 22 and 1002 ¶ 60). Petitioner argues an ordinary artisan would

have understood this control means provides the external signal to switch between modes (e.g., banks). Pet. 28 (citing Ex. 1002 ¶ 60).

Kang describes a "control means for accessing the gamma data in response to an instruction" and "a mode selected by the control means." Ex. 1007 ¶¶ 22, 49; Ex. 1002 ¶ 60. But, any details of how the control means selects a mode is lacking, such that Kang fails to teach or suggest the structure that controls how the control means switches between modes. As previously discussed, Kang's modes do not clearly correspond to the recited "banks" (e.g., contiguous sections of addressable, computer memory).

Furthermore, Petitioner has not explained further how Kang's "control means" teaches an equivalent to the recited "means to switch between banks" in claim 1. Pet. 27–28.

Mr. Credelle further discusses Kang's claim 29 and paragraphs 59, and 60 to teach limitation [g]. Ex. 1002 ¶¶ 60–61. Kang discusses outputting specified mode gamma reference voltages, shown in Table I, "in accordance with a logical value of the gamma data" (Ex. 1007 ¶¶ 59–60) or setting gamma data in response to modes corresponding to peripheral equipment (Ex. 1007 ¶ 66). Lacking, however, is a discussion of structure to switch between memory banks. Notably, Kang's discussion addresses (1) what happens at multi-channel DAC (digital to analog converter) 93, which interprets gamma data *from* memory 92 (Ex. 1007 ¶ 54), and (2) what is outputted from DAC 93 (e.g., gamma reference voltages in accordance with a logical value). Ex. 1007 ¶ 60, Figs. 9–10. This does not relate to how to switch any banks within memory 92, such that the DAC's output switches between storage cells' banks. *See* Ex. 1007 ¶¶ 60, 66, Figs. 9–10.

Claim 29 in Kang also recites storing gamma data in memory and selecting specific gamma data in memory based on a received external mode

signal. Ex. 1007, claim 29. Although this might suggest selecting data associated with a specific mode from memory based on an external signal, the claim does not recite or suggest the corresponding structure to switch between memory banks (e.g., a circuit, algorithm, and/or damping circuit that uses at least one bank address signal). Petitioner also fails to address adequately how the selections within memory in Kang are achieved such that Kang suggests to one skilled in the art the noted structure (e.g., a bank select circuit, algorithm, pins, and/or damping circuit that uses at least one bank address signal) for switching between memory or "storage cells" banks based on at least one received external signal as recited in claim 1.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Kang renders obvious limitation [g]. Claims 2, 4, and 5 depend respectively from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 28–30.

d. Conclusion

Having reviewed Petitioner's and Patent Owner's assertions related to Kang, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Kang renders the challenged claims 1, 2, 4, and 5 of the '305 patent obvious.

2. Da Costa (Ex. 1008)

Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over Da Costa under 35 U.S.C. § 103(a). Pet. 17, 30–37. To support its contentions, Petitioner cites Mr. Credelle's testimony. Ex. 1002. Patent Owner presents several arguments, including that Da Costa does not teach or suggest claim 1's preamble and limitations [b]–[d], [f] and [g]. Prelim. Resp. 29–35. Patent Owner cites Mr. Murphy's testimony. Ex. 2010.

For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Da Costa renders the challenged claims obvious. We focus on claim 1's limitations [b], [f], and [g].

Da Costa discusses "[a] smart controller chip for controlling an active matrix display." Ex. 1008, Abstract. "The combination of D/A [digital/analog] analog circuitry and standard digital logic makes the controller uniquely suited for addressing all the panel control needs both for the normal digital functions but also for control of the analog aspects of the panel, like display gamma." Ex. 1008, 2:37–41.

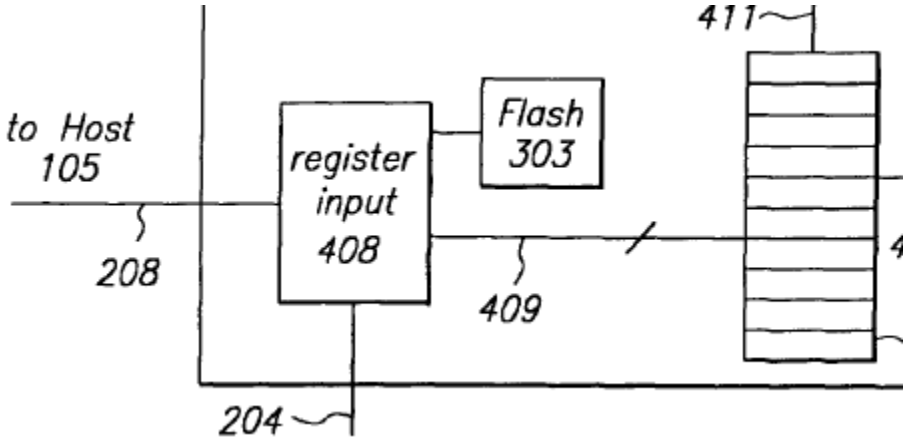
a. Limitation [b]

For this limitation, Petitioner states Da Costa's multiple address lines are used to write the data within memory and registers program the memory with a serial bus. Pet. 33 (citing Exs. 1008, 6:56–60, 11:29–32 and 1002 ¶¶ 77–78). Petitioner contends "a serial bus is an addressing circuit that is interchangeable with a multiplexer," rendering this limitation obvious. Pet. 33 (citing Ex. 1002 ¶ 55). Petitioner also states Da Costa "does not explicitly describe programming the flash memory 303" but such an arrangement would be obvious to an ordinary artisan. Pet. 33 (citing Ex. 1002 ¶ 78).

Patent Owner argues Petitioner does not explain what in Da Costa provides the multiplexer and disputes that a serial bus is interchangeable with a multiplexer. Prelim. Resp. 31.

Da Costa discloses that register input circuity 408 receives digital values (e.g., signals) through first serial bus 204 and second serial bus 208 from host system 105 in Figure 4A. Ex. 1008, 6:56–58, Fig. 4A. Da Costa's Figure 4A, partially shown below, illustrates a smart controller chip

(e.g., 202) with serial buses204 and 208 (discussed in column 6 as cited) entering register input 408.



Partial View of Da Costa's Figure 4A with serial buses.

Ex. 1003, 3:29–30. Da Costa teaches flash memory (e.g., 303 in Figure 4A) integrated into a smart controller chip (e.g., 202), the flash memory being mapped to the recited "non-volatile storage cells." Pet. 32–33 (citing Exs. 1008, 2:55–59 and 1002 ¶¶ 76–77).

Although Da Costa's Figure 4A may suggests to an ordinary artisan using inputs from the host and/or register inputs to program flash memory 303 (Pet. 33), Petitioner has not demonstrated sufficiently that Da Costa's serial buses act as an addressing circuit that is interchangeable with a multiplexer. Pet. 33. As previously discussed, claim 1 requires "a multiplexer" separate from and coupled to the "circuits for programming." Pet. 68. For reasons similar to those discussed above when addressing Kang, the record does not demonstrate sufficiently that (1) a serial bus is interchangeable with a multiplexer or performs the identical function of a multiplexer, (2) Da Costa's flash memory includes or suggests a multiplexer, (3) Da Costa teaches or suggests using decoders somewhere between its host and its flash memory (e.g., 303), or (4) a structure connected to flash

memory 303 that behaves like a device that interleaves signals into a single line, or selects one input and switches its information to the output, which is the customary understanding of a multiplexer. We refer to our discussion of this limitation for Kang, above, for more details.

Mr. Credelle cites to other passages in Da Costa to teach limitation [b]. Ex. 1002 ¶ 84 (citing Ex. 1008, 2:47–49, 6:41–49, 6:62–67). Da Costa states a smart controller chip includes registers that contain values but fails to discuss a multiplexer. Ex. 1008, 2:47–49. Da Costa further discusses the structure within Figure 4A's block diagram, which includes multiplexer circuitry 413. Ex. 1008, 6:41–49, 62–67, Fig. 4A. However, multiplexer circuitry 413 is located after flash memory 303 and registers 410, not connected to the mapped storage cells (e.g., flash memory 303). Ex. 1008, Fig. 4A. The proposed grounds fails to explain sufficiently how this multiplexer is involved in "addressing and programming said storage cells," which is mapped to flash memory 303. Pet. 33.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Da Costa renders obvious limitation [b] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 36–37.

b. Limitation [f]

For limitation [f], Petitioner states Da Costa teaches ten separate gamma curves in flash memory and one skilled in the art would have understood storing the curves in multiple banks. Pet. 35 (citing Exs. 1007, Figs. 4A and 7A and 1002 ¶ 82). Patent Owner argues Da Costa fails to discuss how its memory is organized, including organized in banks, and one

skilled in the art would not have understood its memory is organized in banks. Prelim. Resp. 32–33 (citing Exs. 1008, 8:48–50, Fig. 7A and 2010 ¶ 43).

Da Costa discloses flash memory 303 with no details of how the memory is organized. Ex. 1008, Fig. 4A. Figure 7A shows the details of registers 410, lines 412, multiplexer circuit 413, lines 415, and high-power analog output circuitry 416 or low-power analog output circuitry 450 in Figure 4A, which are located after register input 408 and flash memory 303. Ex. 1008, 3:29–30, 3:38–42, 6:62–67, 7:38–39, 8:48–51, Figs. 4A–B, 7A. As discussed above, Petitioner has mapped the storage cells to flash memory 303, not to other structure, such as registers 410. Pet. 32–33 (citing Exs. 1008, 2:55–59 and 1002 ¶¶ 76–77). Also, the order in which these components are arranged does not demonstrate specifically how the "non-volatile storage cells are organized," as recited in claim 1 and as mapped by Petitioner. Prelim. Resp. 33.

Mr. Credelle testifies, "The gamma curves are stored in flash memory 303 and transmitted to registers 410 through bus 409." Ex. 1002 ¶ 82 (citing Ex. 1008, Fig. 4A) (bolding omitted). Assuming Mr. Credelle is correct, this fails to disclose *how* the stored curves are arranged in memory, such that its storage cells "are organized into two or more banks of cells" (i.e., into contiguous sections of addressable, computer memory) as claim 1 requires.

Mr. Credelle further maps limitation [f] to various passages in Da Costa. Ex. 1002 ¶ 84 (citing Ex. 1008, 9:1–16, 11:29–33, Figs. 7A–B). Figure 7B is similar to Figure 7A and suffers from the problems previously identified for Figure 7A. Ex. 1008, Fig. 7B. The remaining cited passages fail to discuss memory banks, and Mr. Credelle provides no further explanations of these passages. Ex. 1002 ¶ 84.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Da Costa renders obvious limitation [f] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 36–37.

c. Limitation [g]

We agree with Patent Owner that limitation [f], the banks, are not taught or suggested by Da Costa. Prelim. Resp. 33. Moreover, even if Da Costa did teach the recited "banks," Petitioner has not shown that it teaches limitation [g].

Petitioner further states Da Costa teaches registers 410 connected to chip control circuitry and multiplexer circuitry and the multiplexer circuitry is connected to chip control circuitry and the high-power analog output circuitry. Pet. 35 (citing Exs. 1008, 7:1–9 and 1002 ¶ 83). Da Costa describes and shows chip register 410 connected to MUX 413 and control circuitry 406 and MUX 413 connected to high-power analog output 416. Ex. 1008, 6:62–7:9, Figs. 4A, 7A. As noted above, these circuits are located after flash memory 303. Like Patent Owner, we are not convinced that how these components are connected to each other or how these components would be involved in switching between any purported banks located in Da Costa's storage cells (e.g., 303) to demonstrate limitation [g]. Prelim. Resp. 34.

Petitioner further contends Da Costa's serial bus 208 is used to communicate information between first smart controller 202 and host system 105, which allegedly allows for dynamic modification of the analog reference levels and column/row control signal output by the first smart controller 202. Pet. 35–36 (citing Ex. 1008, 5:1–6). Petitioner states an

ordinary artisan "would have understood this disclosure to describe means to switch between banks using control circuity 406" based on external input from host 105. Pet. 36 (citing Ex. 1002 ¶ 83). Once again, control circuit 406 is located after flash memory 303. Ex. 1008, Fig. 4A. Petitioner does not establish how this circuit is involved in switching between any purported banks of the storage cells.

The cited passages of Da Costa fail to describe sufficiently structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses at least one bank address signal) corresponding to the recited means in claim 1, including any structure that permits switching between any alleged banks located within Da Costa's flash memory 303 based on received signals communicated over bus 208. Prelim. Resp. 33–35.

Mr. Credelle further maps limitation [g] to column 11 in Da Costa. Ex. 1002 ¶ 84 (citing Ex. 1008, 11:29–33, 11:41–46). Besides quoting passages from column 11, Mr. Credelle provides no further explanation. Ex. 1002 ¶ 84. Da Costa discusses host system 105 may have software to select between different preprogrammed curves. Ex. 1008, 11:29–33, 41–46. However, selecting between curves fails to teach or suggest a corresponding structure for switching between storage cells' banks, as claim 1 requires, or its equivalent.

Lastly, Petitioner has not further elaborated on how Da Costa's purported "means" teaches an equivalent to the recited "means to switch between banks" in claim 1. Pet. 27–28.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Da Costa renders obvious limitation [g] of claim 1. Claims 2, 4, and 5 depend from claim 1. Petitioner's showing for the

dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 36–37.

d. Conclusion

Having reviewed Petitioner's and Patent Owner's assertions related to Da Costa, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Da Costa renders the challenged claims 1, 2, 4, and 5 of the '305 patent obvious.

3. Petropoulos (Ex. 1009)

Petitioner also challenges claims 1, 2, and 5 as being unpatentable over Petropoulos under 35 U.S.C. § 103(a). Pet. 17, 37–45. To support its contentions, Petitioner cites Mr. Credelle's testimony (Ex. 1002). Patent Owner presents several arguments, including Petropoulos does not teach or suggest claim 1's preamble and limitations [b], [d], and [g]. Prelim. Resp. 39–40. Patent Owner cites Mr. Murphy's testimony (Ex. 2010).

For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Petropoulos renders claim 1 obvious. We focus on limitations [b] and [g].

Petropoulos discusses "a programmable analog/multi-level memory array for modifying individual outputs . . . in order to obtain a desired sensor array output." Ex. 1009, Abstract. "The memory array can be programmed with data corresponding to desired modifications, such as . . . gamma correction." Ex. 1009, Abstract.

a. Limitation [b]

For limitation [b], Petitioner states Petropoulos discloses an address signal generator that provides address signals indicative of row/column addresses, for selecting one of memory cells C11 to CMN to write data values. Pet. 41 (citing Exs. 1009 ¶ 31 and 1002 ¶ 102). Petitioner further

states an address signal generator can be a buffer circuit for generating address signals from addresses provided by external circuitry. Pet. 42 (citing Exs. 1009 ¶ 31 and 1013 ¶ 103). Without stating what circuitry maps to the multiplexer, Petitioner contends an ordinary artisan would have understood the address signal generator programs and addresses storage cells based on multiple inputs (Pet. 41–42 (citing Exs. 1009, Fig. 3 and 1002 ¶ 102)) and that "the decoder tree and other elements within memory are circuits for programming" (Pet. 42 (citing Ex. 1002 ¶ 103)).

Patent Owner contends Petitioner does not explain or specify where the multiplexer is in Petropoulos. Prelim. Resp. 39. We agree. The Petition discusses an "address signal generator" for selecting a memory cell and a buffer circuit for generating address signals but never states the generator or buffer circuit is a multiplexer. Pet. 41–42. Likewise, the Petition states the decoder tree and other elements within memory are circuits for programming but does not explain adequately how these components are a multiplexer as claim 1 requires. Pet. 42.

Cited paragraph 31 of Petropoulos does not assist in clarifying the mapping. Ex. 1009 ¶ 31. Petropoulos discusses address signal generator 320, which can be a buffer circuit, provides address signals for a selected memory cell (e.g., C11–CMN) to which the data value will be written. Ex. 1009 ¶ 31, Fig. 3; Ex. 1002 ¶ 102 (citing Ex. 1009 ¶ 31, Fig. 3). Petropoulos does not discuss how address signal generator 320 behaves like a multiplexer as commonly understood by an ordinary skilled artisan (i.e., a device that interleaves signals to a single line, or selects an input and switches its information to the output). Ex. 1009 ¶ 31, Fig. 3.

Likewise, Petitioner and Mr. Credelle have not explained sufficiently how Figure 3's decoder tree and "other elements within memory" suggests a

multiplexer to one skilled in the art. Pet. 42; Ex. 1002 ¶¶ 102–103. We emphasize the phrase "other elements" (Pet. 42; Ex. 1002 ¶ 103) does not sufficiently map the recited "multiplexer" to Petropoulos's components. To the extent Petitioner contends that any circuit that receives address signals and outputs other signals is a multiplexer, we disagree for reasons previously presented.

Mr. Credelle maps limitation [b] to yet further passages in Petropoulos. Ex. 1002 ¶ 110 (citing Ex. 1009 ¶¶ 12–13). Other than quoting from these paragraphs, which do not discuss or suggest a multiplexer, Mr. Credelle provides no further explanation of how these paragraphs teach or suggest "a multiplexer" as claim 1 recites. Ex. 1002 ¶ 110.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Petropoulos renders obvious limitation [b]. Claims 2 and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 45.

b. Limitation [g]

Petitioner asserts Petropoulos teaches "a desired one of the memory arrays 210 is selected for a particular modification." Pet. 44 (quoting Ex. 1009 ¶ 51 and citing Ex. 1002 ¶ 108). In particular, Petitioner states routing circuit 220 selects a desired modification and that one skilled in the art would have understood the decoder, which accesses the desired voltage from a memory array, maps to the recited "means to switch between banks based on external signals, i.e., the routing circuit." Pet. 44–45 (citing Exs. 1009 ¶¶ 27, 53 and 1002 ¶ 109).

Cited paragraph 27 summarizes what is shown in Figure 2 below.

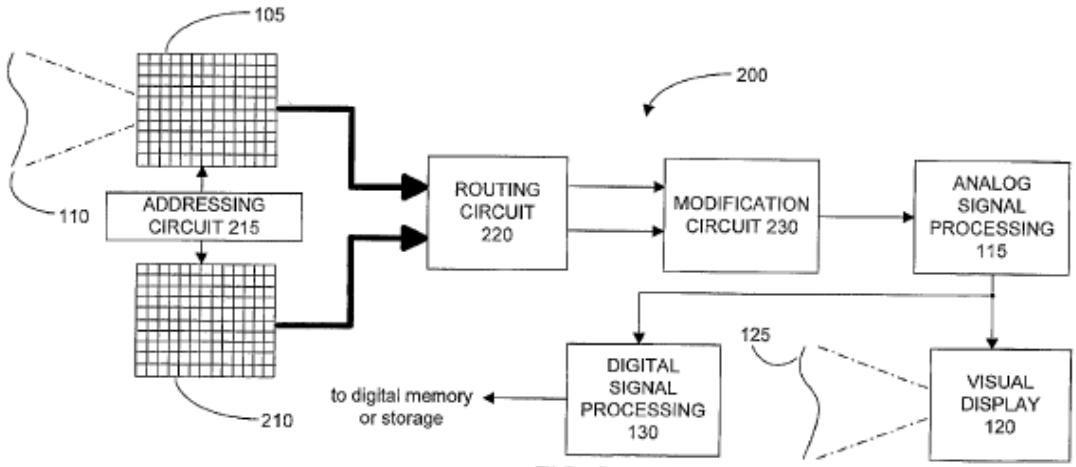
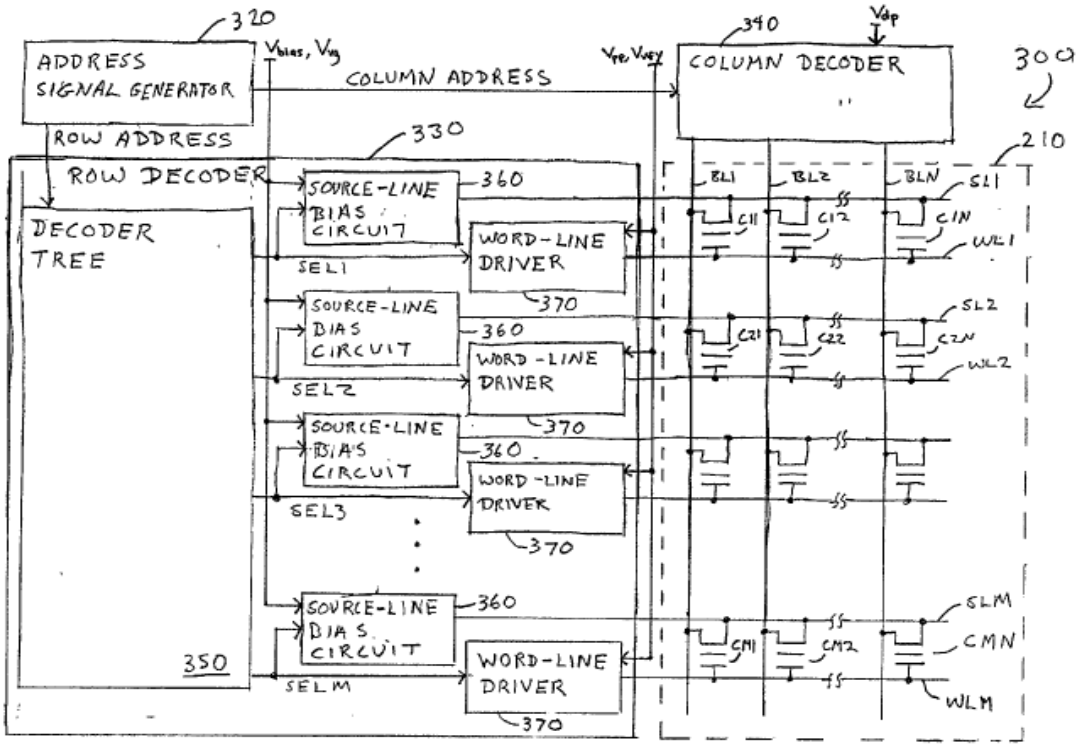


FIG. 2

Petropoulos's Figure 2 Showing an Imaging System

Figure 2's imaging system includes (1) image sensor 105, (2) addressing circuit 215 reading out voltages from image sensor 105 and memory 210, (3) routing circuit 220, and (4) analog signal processing circuit 115 for processing reconstructed image 125. Ex. 1009 ¶¶ 27–28, Fig 2. There is no accompanying discussion of a corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) to limitation [g] in Figure 2.

Figure 3 below shows more detail of the multi-memory 210 in above Figure 2.



Petropoulos's Figure 3 Showing Memory

The above Figure 3's memory shows address signal generator 320 coupled to column decoder 340 and row decoder 330, the decoders coupled to multi-level memory 210. Ex. 1009 ¶ 19, Fig. 3.

Although this figure shows decoders 330 and 340, Petitioner does not explain sufficiently or identify adequately how Petropoulos's decoder is a corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) to limitation [g]. *See* Prelim. Resp. 40. For example, Petropoulos's Figure 3 has two decoders (e.g., row decoder 330 and column decoder 340). Ex. 1009, Fig. 3. But, Petitioner does not explain whether both of these decoders, or which portions of these decoders, are being mapped to limitation [g]. Pet. 44–45.

Petropoulos discusses a desired memory is selected for a particular modification (Ex. 1009 ¶ 51, *cited in* Pet. 44) and the memory array and

decoder are collectively used for the modifications (Ex. 1009 ¶ 53, *noted in* Pet. 44). Regardless, Petitioner fails to explain how this teaches or suggests the structure corresponding to limitation [g] (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal).

Petropoulos discusses that a multi-level memory array can be used with a decoder for multiple modification types. Ex. 1009 ¶ 53, *noted in* Pet. 44. Petropoulos states, "The memory array is programmed with data corresponding to the desired types of modifications in various portions of the array" and "[t]he decoder then determines the type of modification . . . and accesses the desired voltage from the memory array" (Ex. 1009 ¶ 53). Petitioner fails to explain sufficiently how "the decoder" determining the modification type and accessing the memory array's desired voltage teaches or suggests to the corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) of limitation [g].

Petitioner further cites paragraph 108 of Mr. Credelle's testimony as support for Petropoulos teaching limitation [g]. Pet. 44. Mr. Credelle, however, does not persuasively explain how the portions of Petropoulos he cites teach or suggest a corresponding structure (i.e., a bank select circuit, algorithm, pins, and/or damping circuit that uses a bank address signal) to a means for switching between banks as claim 1 requires.

Petitioner further states that the decoder "selects a location in the memory array" (Pet. 44), turning to Mr. Credelle's testimony for support (Pet 45 (citing Ex. 1002 ¶ 109)). In paragraph 109, Mr. Credelle discusses memory arrays 210, routing circuit 220, and modification circuitry block 230 (shown in Figure 2) are used to select and perform memory array modification and teach "a means to select gamma data from the memory

arrays and a routing circuit 220 to select the modifications." Ex. 1002 ¶ 109 (citing Ex. 1009 ¶¶ 27, 51). Thus, Mr. Credelle concludes that the "means to select gamma data" and the routing circuit 220—not the previously discussed decoder—are a "means to switch between banks." Ex. 1009 ¶ 109.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Petropoulos renders obvious claim 1's limitation [g]. Claims 2 and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 45.

c. Conclusion

Having reviewed Petitioner's and Patent Owner's assertions, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Petropoulos renders challenged claims 1, 2, and 5 of the '305 patent obvious.

4. Tanaka (Ex. 1010)

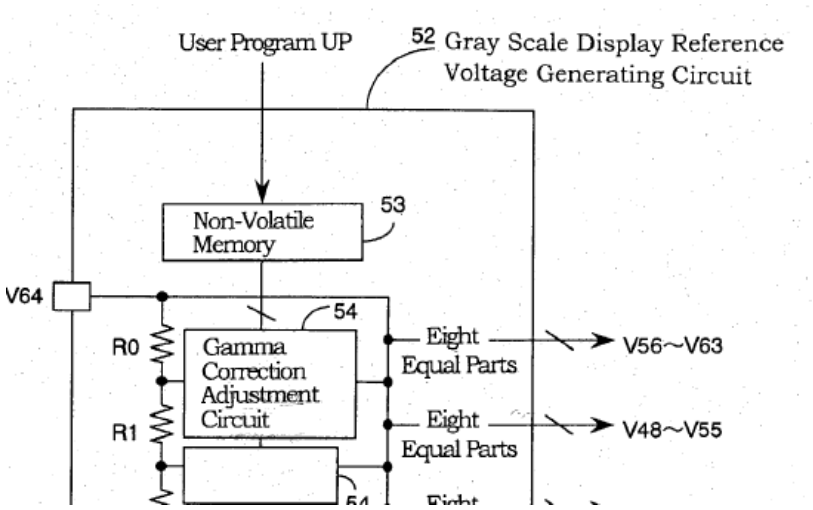
Petitioner challenges claims 1, 2, 4, and 5 as being unpatentable over Tanaka under 35 U.S.C. § 103(a). Pet. 17, 45–53. To support its contentions, Petitioner cites to Mr. Credelle's testimony (Ex. 1002). Patent Owner presents several arguments, including Tanaka does not teach or suggest claim 1's preamble and limitations [b], [d], [f], and [g]. Prelim. Resp. 41–47. Patent Owner cites to Mr. Murphy's testimony (Ex. 2010).

Having reviewed Petitioner's and Patent Owner's assertions related to Tanaka, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Tanaka renders challenged claim 1 obvious for the following reasons. We focus on claim 1's limitations [b], [f], and [g].

Tanaka discusses "a gray scale display reference voltage generating circuit" for use with a LCD device that includes "a reference voltage generating section for producing reference voltages of a plurality of levels" and "an adjustment section for adjusting the reference voltages based upon the quantity of adjustment stored in the correction information storing section." Ex. 1010, Abstract, ¶¶ 32–33.

a. Limitation [b]

Petitioner admits Tanaka "does not explicitly disclose the use of a multiplexer" but contends Tanaka's user interface must provide data and gamma locations to select memory locations. Pet. 50 (citing Exs. 1010 ¶¶ 102, 143 and 1002 ¶ 123). In particular, Tanaka teaches voltage generating circuit 52 produces reference voltages and uses a basis voltage VR supplied from an external power source and a user program (UP) given by a user program such as an external control device. Ex. 1010 ¶ 102, Fig. 3; Ex. 1002 ¶ 123. A portion of Figure 3 is reproduced below to illustrate.



Partial Figure 3 Showing Memory receiving UP data.

Notably, other than a data line between the UP and memory 53 or between gamma correction adjustment circuit 54 and memory 53 in Tanaka's partial Figure 3, there is no other interface and, more specifically, no multiplexer.

Tanaka discusses storing addresses in memory 53 (Ex. 1010 ¶ 140) and how addresses are stored using "the external control device by the user" (Ex. 1010 ¶ 143). *See* Ex. 1002 ¶ 123 (quoting from Ex. 1010 ¶ 143). More specifically, Tanaka discusses that a user's operation changes the gamma correction adjustment. Ex. 1010 ¶ 143. Tanaka does not discuss or suggest using any particular interface or the recited "multiplexer" to address or program its memory (e.g., 53). Additionally, Petitioner does not explain sufficiently how these teachings map to both the "circuits for programming" and the "multiplexer" coupled to the "circuits for programming" as claim 1 requires. *See* Prelim. Resp. 43.

Petitioner also asserts that "as discussed above," an ordinary artisan would have known "one of a limited number of components would have performed this function," and thus employing a multiplexer would have been obvious. Pet. 50 (citing Ex. 1002 ¶ 123). This theory that any of a limited number of components perform Tanaka's interface function that provides data and gamma locations to memory is similar to an "obvious to try" rationale.

But, Petitioner fails to support this rationale adequately. More specifically, neither Petitioner (Pet. 49–50) nor its expert, Mr. Credelle, (Ex. 1002 ¶ 123) has identified a finite number of predictable solutions for providing Tanaka's interface or shown that an ordinary artisan would have good reasons to pursue using a multiplexer as a predictable solution for Tanaka's interface. *See KSR*, 550 U.S. at 421. In fact, Mr. Credelle testifies flash memory is programmed using decoders and gamma data. Ex. 1002

¶ 123 (referring to Section V.C. of his declaration). Mr. Credelle appears to assert Tanaka teaches its memory already has a multiplexer—not that an ordinary skilled artisan would have good reason to pursue modifying Tanana's memory with a multiplexer. *See* Ex. 1002 ¶ 123. Also, even assuming, without agreeing, that "*Tanaka* must necessarily provide address data and gamma locations to selected locations within the memory" (Pet. 50), this is insufficient to demonstrate one skilled in the art would have recognized trying a multiplexer for this purpose.

For the above reasons, Petitioner does not show sufficiently for institution purposes that Tanaka renders obvious limitation [b]. Claims 2, 4, and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 52–53.

b. Limitations [f] and [g]

With respect to limitation [f], Petitioner contends Tanaka's elements 51-1, 51-2, and 52-3 are the cells' banks. Pet. 51 (citing Exs. 1010, Fig. 10 and 1002 ¶ 127). Notably, this mapping of the storage cells' banks to element 51 is inconsistent with Petitioner's earlier mapping of the storage cells to element 53. *Compare* Pet. 49, *with* Pet. 51. Additionally, Petitioner's mapping to element 51 is inconsistent with Mr. Credelle's testimony. *Compare* Pet. 51, *with* Ex. 1002 ¶ 127.

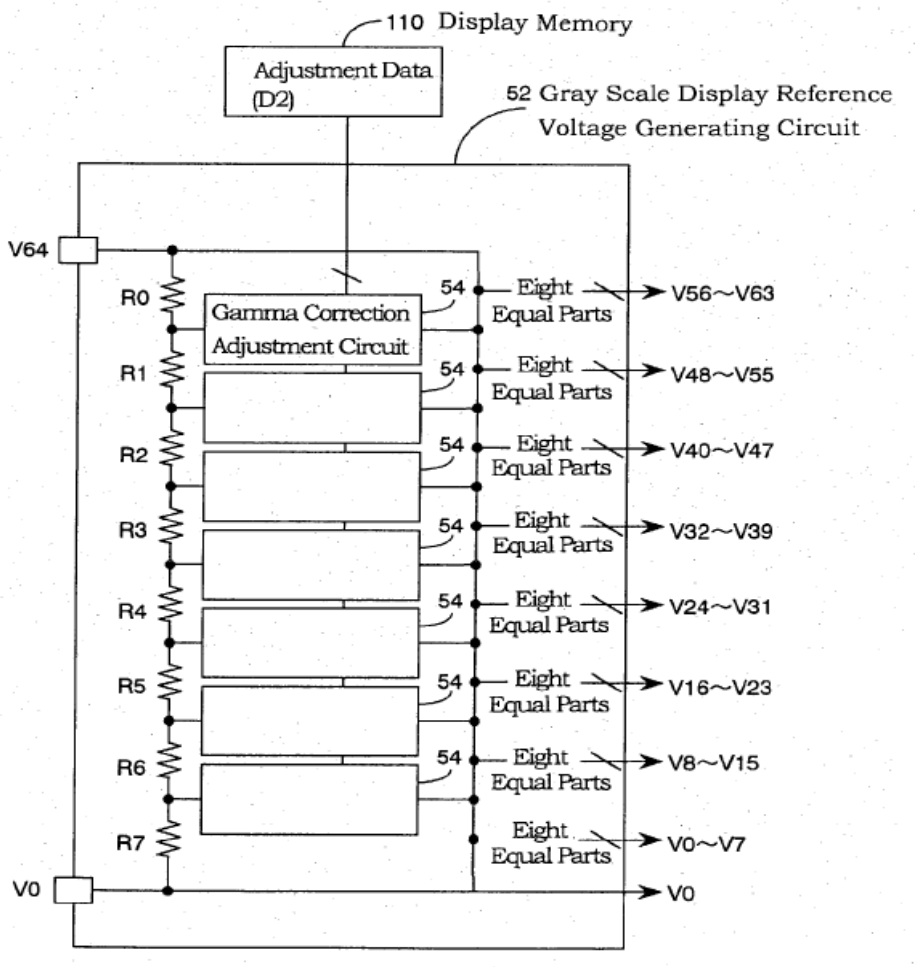
Regarding limitation [g], Petitioner asserts Tanaka teaches selecting banks based on the data's color. Pet. 51 (citing Ex. 1002 ¶ 128). Petitioner also states Tanaka teaches multiple gamma correction curves stored in display memory and a means to switch between gamma curves depending on a row number. Pet. 51–52 (citing Exs. 1010, Fig. 20 and 1002 ¶ 128). Although indicating Tanaka uses external memory, Petitioner determines "it would have been obvious to a POSA to enlarge the memory 53 to contain

multiple sets of gamma curves." Pet. 52 (citing Exs. 1010 ¶¶ 243–45, Fig. 33 and 1002 ¶ 130). Lastly, Petitioner states a POSA "would have understood the[three] control signals are external signals to control which bank of gamma correction data is selected from memory." Pet. 52 (citing Exs. 1010 ¶¶ 243–245 and 1002 ¶¶ 130–131).

Patent Owner rebuts, challenging the multiple bases for concluding Tanaka teaches or suggests limitations [f] and [g]. Prelim. Resp. 45–47.

We disagree with Petitioner (Pet. 51 (citing Exs. 1010, Fig. 10 and 1002 ¶ 127)) and agree with Patent Owner (Prelim. Resp. 45–46) that Tanaka's reference voltage generating circuits (e.g., 51-1, 51-2, and 52-3) are not banks of cells as understood by an ordinary artisan (e.g., contiguous sections of addressable, computer memory). *See* Ex. 2010 ¶ 47. Rather, they are shown as separate components from memory 53 in Tanaka's Figure 10. Ex. 1010, Fig. 10.

Also, Tanaka's Figure 20 below shows an alternative embodiment of gray scale display reference voltage generating circuit 52 from that in Figure 3:



Tanaka's Figure 20 Showing an Alternative Gray Scale Display Reference Voltage Generating Circuit

The above Figure 20's gray scale display reference voltage generating circuit 52 includes seven gamma correction adjustment circuits 54 generating eight equal part voltages (i.e., 64 reference voltages V0-V63) using voltage input terminals V0 and V64 and eight resistors R0 through R7. Ex. 1010 ¶¶ 109, 187, Fig. 20.

Contrary to Petitioner's assertion (Pet. 51–52), this figure does not show or suggest memory banks or a means to switch between gamma curves depending on a row number as part of "[a]n integrated circuit." *See* Prelim. Resp. 46. Moreover, memory 53, shown in Figure 3 and Figure 10, *noted in*

Ex. 1002 ¶ 127, is not found in Figure 20. In fact, as noted by both Petitioner (Pet. 52) and Patent Owner (Prelim. Resp. 46), display memory 110 in Figure 20 is external to circuit 52. Ex. 1010, Fig. 20. An external memory does not teach or suggest "an integrated circuit" comprising "non-volatile storage cells" along with recited limitations [b]–[g]. *See* Ex. 2010 ¶ 46.

Discussing Figure 20, Mr. Credelle quotes from Tanaka's paragraph 186, which states adjustment data is stored in memory 110 and adjustment data type read out is varied for every gate signal line by control C. Ex. 1002 ¶ 128 (quoting Ex. 1010 ¶ 186). This teaching does not identify sufficiently a corresponding structure (i.e., a circuit, algorithm, and/or damping circuit that uses at least one bank address signal) to limitation [g]. *See* Prelim. Resp. 46.

Accordingly, Petitioner has not demonstrated adequately that Tanaka's Figure 20 shows an integrated circuit comprising both "non-volatile storage cells" (limitation [a]) and a "means to switch between the banks [of the storage cells] based on one or more external signals" (limitation [g]) as claim 1 recites.

Petitioner further asserts an ordinary artisan would have known to enlarge memory 53 to contain Tanaka's gamma curves. Pet. 52 (citing Exs. 1010 ¶¶ 243–245, Fig. 33 and 1002 ¶ 130); Ex. 1002 ¶ 129 (showing gamma curves in Figure 25). Cited paragraphs 243 through 245, which address Figure 32, fail to discuss enlarging memory (e.g., 53) to contain gamma curves. Exs. 1010 ¶¶ 243–245. Thus, although these passages discuss reading out data from display memory using control signals (e.g., C and C1) and cited Figure 33 shows a similar arrangement, there is insufficient evidence that Tanaka suggests to one skilled in the art enlarging

memory 53, which is mapped to the recited "non-volatile cells" in claim 1. Pet. 49 (citing Ex. 1010 ¶¶ 76, 144); *see* Ex. 2010 ¶ 49 (discussing Tanaka does not demonstrate that it would be obvious to enlarge memory to contain gamma curves).

Also, Petitioner has not sufficiently explained or identified the "rows" discussed in paragraphs 203 and 204, *noted in* Ex. 1002 ¶ 129, are storage cells' banks, such that there is a suggestion to include a "means to switch between banks," as claim 1 further recites. Because Petitioner does not provide sufficient evidence to have banks within memory 53 and to enlarge Tanaka's memory 53, Petitioner has not demonstrated sufficiently to include claim 1's limitation [g].

Mr. Credelle discusses Figure 33 and discuses three external control signals used "to control which bank of gamma correction data is selected from non-volatile display memory 110 and 137." Ex 1002 ¶ 130. Figure 33 does not show banks in memory 110 and 137, such that Tanaka's Figure 33 teaches or suggests to an ordinary artisan a "means to switch between banks based on one or more external signals," as recited. Ex. 1010, Fig. 33; *see also* Ex. 1010 ¶ 241. That is, a corresponding structure to limitation [g] (i.e., a circuit, algorithm, and/or damping circuit that uses at least one bank address signal) is not shown or described. Mr. Credelle's discussion in paragraph 132, previously addressed above, does not cure this deficiency. Ex. 1002 ¶ 132 (citing Ex. 1010 ¶¶ 243–245).

For the above reasons, Petitioner does not show sufficiently for institution purposes that Tanaka renders obvious limitations [f] and [g]. Claims 2, 4, and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 52–53.

d. Conclusion

Having reviewed Petitioner's and Patent Owner's assertions, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Tanaka renders challenged claims 1, 2, 4, and 5 of the '305 patent obvious.

5. Da Costa and Tsai (Ex. 1011)

Petitioner also challenges claims 1, 2, 4, and 5 as being unpatentable over Da Costa and Tsai under 35 U.S.C. § 103(a). Pet. 17, 53–58. Petitioner explains this ground is "presented to address a potential argument that *Da Costa* and/or *Tanaka* do not render obvious the claims' recitation of a 'multiplexer.' *Tsai*, which is combinable with *Da Costa* and with *Tanaka* for the reasons discussed below, explicitly discloses the use of a multiplexer, and the combination plainly meets this limitation." Pet. 18, 57–58. For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing Da Costa and Tsai render the challenged claims obvious.

Tsai discusses a microcomputer having embedded flash memory, which allows for (1) programming data into the memory and (2) reprogramming (e.g., update or change) data in memory without external programming tools or on-chip. Ex. 1011, Abstract, *cited in* Pet. 54. Tsai's microcomputer (e.g., 310) includes a bus multiplexer (e.g., 350) connecting a register set (e.g., 340) to flash memory (e.g., 330). Ex. 1011, 7:2–9, 49–67, Fig. 3; Pet. 54–55.

Petitioner proposes to combine Tsai with Da Costa. Pet. 55–57. In particular, Petitioner states, "A POSA reading *Tsai* would have understood that the memory programming method described therein could be used to program the integrated flash memory as disclosed by *Da Costa*" (Pet. 56–

57) (citing Ex. 1002 ¶ 149) and "would have understood that the programming process it describes would provide the memory programming details that Da Costa lacked" (Pet. 57) (citing Ex. 1002 ¶ 149).

As explained above, Petitioner does not show sufficiently for institution purposes that the proposed ground based only on Da Costa under 35 U.S.C. § 103 teaches or suggests limitations [f] and [g]. The proposed ground to combine Da Costa and Tsai does not address how Tsai would have further taught or suggested limitations [f] and [g]. Thus, the proposed ground does not rely on Tsai to teach or suggest claim 1's limitations [f] and [g], which as previously stated are not sufficiently taught or suggested by Da Costa. We refer above for more details.

Claims 2, 4, and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 36–37.

Having reviewed Petitioner's and Patent Owner's assertions related to Da Costa and Tsai, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Da Costa and Tsai render challenged claims 1, 2, 4, and 5 of the '305 patent obvious.

6. Tanaka and Tsai

Petitioner also challenges claims 1, 2, 4, and 5 as being unpatentable over Tanaka and Tsai under 35 U.S.C. § 103(a). Pet. 17, 58–62. Like the proposed ground based on Da Costa and Tsai, Petitioner explains this ground is "presented to address a potential argument that" Tanaka alone does not render obvious claim 1's "multiplexer," asserting the combination of Tanaka and Tsai meets this limitation. Pet. 18; Pet. 60–61.

As explained above, Petitioner does not show sufficiently for institution purposes that the proposed ground based only on Tanaka under

35 U.S.C. § 103 teaches or suggests limitations [f] and [g]. The proposed ground to combine Tanaka and Tsai does not address how Tsai would have further taught or suggested limitations [f] and [g]. In fact, Petitioner states this ground is presented to address "a potential argument" (Pet. 18) that Tanaka does not render a multiplexer obvious (Pet. 18, 58). Thus, this proposed ground does not rely on Tsai to teach or suggest claim 1's limitations [f] and [g], which as previously stated are not sufficiently taught or suggested by Tanaka. We refer above for more details.

Claims 2, 4, and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 52–53.

Having reviewed Petitioner's and Patent Owner's assertions related to Tanaka and Tsai, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Tanaka and Tsai render challenged claims 1, 2, 4, and 5 of the '305 patent obvious.

7. Petropoulos and Kang

Lastly, Petitioner also challenges claims 1, 2, 4, and 5 as being unpatentable over Petropoulos and Kang under 35 U.S.C. § 103(a). Pet. 17, 62–66. Petitioner explains, "To the extent the Board finds Ground 3 [(grounds based on Petropoulos alone)] to be lacking regarding the claimed gamma reference voltage signals in *Petropoulos*, Petitioner submits that *Kang* in combination with *Petropoulos* renders obvious the claimed gamma reference voltage signals." Pet. 62; Pet. 18. Petitioner states, "[T]hose descriptions [of a relatively more limited discussion of gamma reference voltage signals in *Petropoulos*] would be a motivation to combine *Petropoulos* with *Kang*, which plainly discloses the gamma correction voltage-related limitations of the Challenged Claims." Pet. 18, 62.

As explained above, Petitioner has not shown sufficiently for institution purposes that the proposed grounds based on Kang or Petropoulos alone teach certain limitations of the challenged claims. We explained above the proposed ground based only on Petropoulos does not teach or suggest limitations [b] and [g] and the proposed ground based only on Kang does not teach or suggest limitations [b], [f], and [g]. Thus, this proposed ground to combine Petropoulos and Kang does not address how the combination teaches or suggests limitations [b] and [g]. In fact, Petitioner states this ground is presented if "Petropoulos' relatively more limited discussion of gamma reference voltage signals is deficient" (Pet. 18, 66). That is, the proposed ground does not turn to Kang to teach or suggest limitations [b] and [g], which as previously stated are not sufficiently taught or suggested by Petropoulos. We refer above for more details.

Claims 2, 4, and 5 depend from claim 1. Petitioner's showing for the dependent claims does not cure the deficiency of its showing for claim 1. *See* Pet. 28–30, 45[19].

Having reviewed Petitioner's and Patent Owner's assertions related to Petropoulos and Kang, we determine that Petitioner has not established a reasonable likelihood that it would prevail in showing Petropoulos and Kang render challenged claims 1, 2, 4, and 5 of the '305 patent obvious.

Because this determination disposes of the Petition, no need exists to reach Patent Owner's other arguments regarding Petitioner's showing.

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[19] The proposed ground based on Petropoulos alone does not include claim 4. Pet. 17, 45.

E. Conclusions Based on Cited References

Petitioner has not established a reasonable likelihood of prevailing in challenging the following: (1) claims 1, 2, 4, and 5 as obvious over Kang; (2) claims 1, 2, 4, and 5 as obvious over Da Costa; (3) claims 1, 2, and 5 as obvious over Petropoulos; (4) claims 1, 2, 4, and 5 as obvious over Tanaka; (5) claims 1, 2, 4, and 5 as obvious over Da Costa and Tsai; (6) claims 1, 2, 4, and 5 as obvious over Tanaka and Tsai, and (7) claims 1, 2, 4, and 5 as obvious over Petropoulos and Kang.

III. CONCLUSION

For the above reasons, we determine that Petitioner has failed to demonstrate a reasonable likelihood of prevailing at trial as to any challenged claim. Accordingly, we deny institution of an *inter partes* review.

IV. ORDER

For the above reasons, it is

ORDERED that the Petition is *denied* as to the challenged claims of the ’305 patent, and no *inter partes* review is instituted.

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