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Handbook of Wafer Bonding



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Wafer Bonding Using Spin-On Glass as Bonding Material

Viorel Dragoi

Among the most used wafer bonding processes, adhesive wafer bonding attracts a high level of interest due to its specific features:

- Compensation of surface defects: if wafer bonding is used to join patterned wafers there is a risk of generating surface defects during wafer preparation (e.g., scratches, local high roughness), which may have an impact on bonding results.
- Compensation of particle contamination: small amounts of particles remaining on the surface can be incorporated in the bonding layer if the particle diameter is smaller than the layer thickness.
- Low processing temperature compared to fusion bonding ($<300^{\circ}\text{C}$).
- Relatively simple process flow (standard sol-gel process) compared with other thin-film deposition methods requiring vacuum deposition (e.g., evaporation, sputtering).

Due to the large variety of polymer materials designed for various microelectronics processes, the selection pool for bonding materials is very broad. However, there is only a small part of this large amount of materials which fulfills the requirements for wafer bonding.

This chapter reviews some basic aspects related to the use of spin-on glass (SOG) materials as bonding layers in adhesive wafer bonding. An SOG-based adhesive wafer bonding process is presented [1].

2.1

Spin-On Glass Materials

Spin-on glasses represent a category of materials used mainly as interlevel dielectrics in microelectronic applications or simply for surface planarization. Typically the material is applied to a substrate using a sol-gel process flow consisting of a deposition step (spin coating or spray coating) followed by a baking step for

removal of solvents and finally a thermal curing step. After cure, SOG films should show good uniformity, crack resistance, low stress, high thermal stability, and good adhesion to the substrate. SOGs can fill narrow spaces in pre-metal and metal levels simultaneously planarizing the surfaces.

The term “surface planarization” may have different meanings depending on the application area: microelectronics or wafer bonding.

In microelectronics the starting semiconductor wafers for device fabrication are ideally flat or planar prior to undergoing various fabrication steps. This series of material growth, deposition, and patterning steps decreases the flatness or planarity of the wafer surface.

The recent trends towards device fabrication that involve an increasing number of metal layers aggravate the problem of wafer nonplanarity. The shift to narrower and narrower metal lines has also prompted the emergence of thicker metal lines in order to meet current device requirements.

At least two major problems arise from the decrease in surface flatness: (i) full step coverage of fine lines so that no breakage in line continuity occurs becomes more difficult and (ii) fine-featured pattern imaging (e.g., in photolithography steps) is more difficult, if not impossible.

There are two categories of planarization techniques: local planarization and global planarization. Local planarization refers to techniques that increase planarity over short distances. Global planarization consists of techniques that decrease long-range variations in wafer surface topology, especially those that occur over the entire image field of the stepper.

Planarization techniques include: (i) oxidation; (ii) chemical etching; (iii) deposition of oxide or nitride layers; (iv) deposition of low-melting-point glass layers; (v) use of polyimide films; (vi) use of resins and low-viscosity liquid epoxies; (vii) use of SOG materials; (viii) sacrificial etch-back; and (ix) as a stand-alone step or associated with layer deposition techniques, mechanical–chemical polishing of wafers.

The use of SOG materials for surface planarization in microelectronics is not new. The early SOG films were typically silicates. Today’s mainstream technologies using multiple interconnect levels employ mainly siloxane SOG films. Siloxanes became mainstream in SOG technology due to their excellent crack resistance and ability to fill gaps as small as $0.1\ \mu\text{m}$ while ensuring complete local planarization. Phosphosilicates can be used as well in order to further improve crack resistance.

Some SOG materials can also be used for new applications as adhesive layers for wafer bonding. One of the main challenges of using such materials for wafer bonding is the ability to obtain a perfectly flat surface of the SOG layer across the entire area that is desired to be bonded.

If in microelectronics manufacturing the term “planar surface” refers to areas as large as a stepper field area which would show a small waviness, for wafer bonding it would refer to a perfectly flat surface across the entire wafer area.

2.2

Wafer Bonding with SOG Layers

An example of wafer bonding process development using a silicate SOG material as bonding layer is now presented. The target for this process was for it to be applicable for bonding Si and GaAs substrates. The challenge in this case was the thermal mismatch illustrated by the significant difference in thermal expansion coefficient ($TEC_{GaAs} \approx 2TEC_{Si}$). It was experimentally determined that a process temperature of 200 °C would be acceptable for the final application if the bond strength achieved would be enough such that a GaAs wafer would survive mechanical thinning (grinding).

2.2.1

Experimental

In order to check the concept of wafer bonding via SOG intermediate layers, the process was first applied to an Si/Si system. The experiments were carried out on p-type, (100)-oriented Si wafers, 100 and 150 mm in diameter. The Si wafers were first cleaned using standard RCA 1 and RCA 2 procedures, followed by a deionized water rinse and drying in nitrogen flow.

Two different processes were used for SOG deposition on substrates: spin coating and spray coating. The most commonly used process is spin coating. In this approach, a liquid precursor is dispensed on the wafer (static—the wafer is not rotated during dispense; or dynamic—the wafer is slowly rotated during dispense). The wafer is then rotated at low speed for uniform spread of the material on the entire wafer surface. Finally the wafer is rotated at high speed to remove excess material and for layer drying. The film thickness is highly dependent on the rotation speed used in the drying step.

Spray coating is an alternative to spin coating and can be especially useful for high-topography wafers, noncircular substrates, or substrates with etched trough via holes. The film thickness achieved in the spray-coating process is dependent on the amount of dispensed material as well as on the programmed motion of the dispense arm (stroke time and arm speed) and spinner chuck (rotation speed). While the wafer rotates slowly at 30–100 rpm, the atomizing nozzle starts spraying right outside the wafer area and moves over the wafer center to the other side. To get a uniform layer thickness over the whole wafer, the speed of the nozzle increases towards the wafer center and decreases from there on outwards according to a controlled speed profile.

SOG films were deposited by spin coating using the following steps:

- dispense of the liquid SOG precursor on the Si surface;
- obtaining the gel film by spinning at low rotation speeds;
- spin-drying of the solvent for solvent evaporation;
- pyrolysis of the gel film onto a hot plate in air at temperatures between 150 and 180 °C.

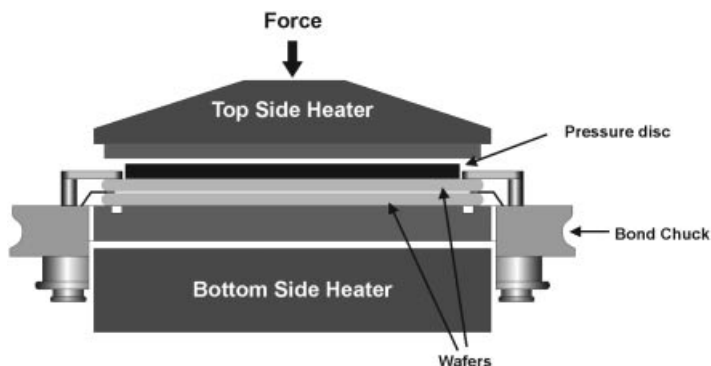


Figure 2.1 Bond chamber setup for adhesive bonding.

For spray coating, the SOG material liquid precursor was diluted with ethanol and the process was optimized for different layer thicknesses.

The thickness of the SOG layers was measured with an Alpha-Step 500 profiler from KLA Tencor.

The wafer bonding step was performed in an EVG®520 semi-automated bonding system. The experimental setup used is shown schematically in Figure 2.1. The two wafers were loaded clamped together onto the bond chuck, with spacers keeping them separated. Mechanical alignment of wafer edges was performed using a chuck with alignment pins. The bond chamber was first evacuated down to a few tens of millibars in order to avoid air being trapped between the wafers when moving them into contact. The wafers were then brought into contact. After contacting the wafers the chamber was purged with nitrogen and the two heaters started to heat the wafer stack. A force of up to 7 kN could be applied using a piston mounted together with the top heater.

SOG-coated Si wafers were bonded at room temperature with clean blank Si wafers using the bonding procedure described above. After bonding, the pairs were annealed at temperatures starting from 200°C in order to optimize the process.

Bonded interface quality was investigated using infrared (IR) transmission with an EVG®20 infrared inspection station and scanning acoustic microscopy (SAM) with a Sonoscan D9000 system. The surface energy was evaluated using the crack-opening method [2] and by tensile testing (Si/GaAs bonds).

2.2.2

Wafer Bonding with Silicate SOG Layers

Spin- and spray-coating methods were evaluated for a silicate SOG material. The film thickness for spin coating varied in the range 280–125 nm for a spin-drying speed range 2000–5000 rpm (500 rpm increments).

Spray-coating tests showed relatively good uniformity for thicker SOG layers (~600 nm) but bond tests showed for spray-coated layers that the uniformity was

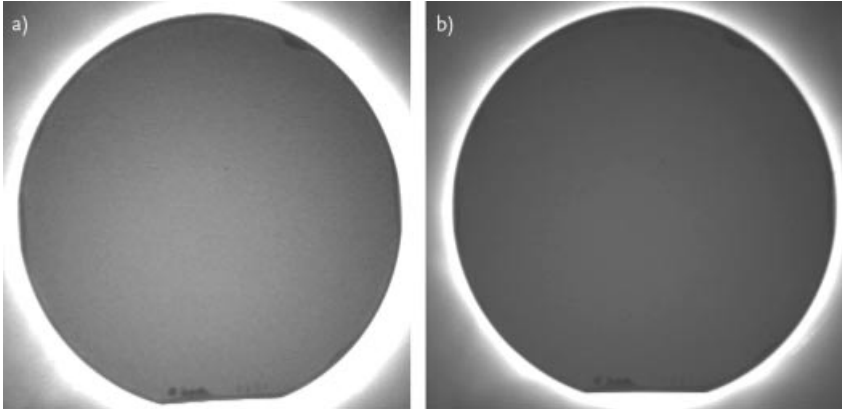


Figure 2.2 IR transmission images of a bonded wafer pair (100 mm in diameter): (a) room temperature bonded; (b) annealed at 200°C for 10h.

not enough for good-quality bonding. In order to improve the quality of the spray-coated layers additional work would be required in studying various precursor dilutions and deposition conditions. As there was no specific need for spray coating in this application (it was investigated here only for comparison with standard spin coating), this method was not further pursued due to the good results obtained for spin coating.

In order to avoid the occurrence of interface defects, the SOG deposition process was optimized for obtaining defect-free layers. Figure 2.2 shows IR images of a bonded wafer pair immediately after room temperature bonding and after annealing at 200°C for 10h. The only defects observed are located around the laser marks of the two wafers (close to the wafer flat), which in this case are in the bonded interface. It can be observed that for one wafer there is an unbonded area around the marks (SOG-coated wafer – “shadow” defect in the SOG layer) while for the other the marked numbers (blank Si) can be clearly observed.

It can be observed that no additional defects are generated, and those existing after room temperature pre-bonding do not increase in size, showing there is no outgassing at the bonded interface. This test reveals the importance of the SOG layer quality for successful bonding.

The bond strength measured after room temperature bonding was found to be in the range $0.4\text{--}0.45\text{ J m}^{-2}$, about 3–4 times higher than for normal hydrophilic Si/Si bonding which is about $0.1\text{--}0.15\text{ J m}^{-2}$ [3]. This very high surface energy can be the result of the chemistry at the SOG–Si interface, which is very different from standard Si–Si bonding. IR spectroscopy measurements (Figure 2.3) revealed the existence of CH_3 radicals in the SOG films baked at temperatures below 200°C. The residual organic radicals remaining from the solvent can easily hydrolyze with the water molecules adsorbed at the GaAs surface and create strong covalent bonds. Even after a baking procedure at 150°C for 5 min the SOG surface also contains silanol groups, which may generate adhesion at room temperature due

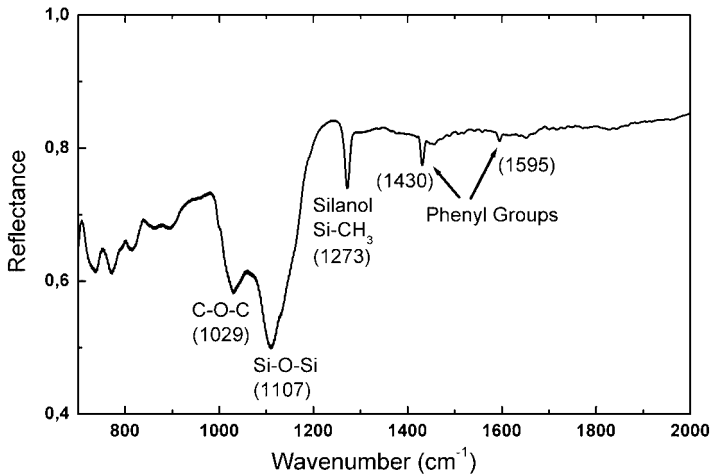


Figure 2.3 IR reflection spectrum of SOG layer.

to their ability to form chemical bonds with molecules from the other surface directly or via water molecules.

Thermal annealing optimization was performed by measuring the dependence of the surface energy on the annealing time at 200°C and by trying different temperatures. To allow the diffusion of the gaseous products generated at the interface, the heating/cooling rate was less than 1°C min⁻¹. A low temperature ramping is also required for the final application (Si/GaAs bonding) in order to avoid thermal shocks which may result in wafer breakage.

Surface energy increased to 1.8 J m⁻² for annealing at 200°C for 6 h, and after 18 h the surface energy reached 2.3 J m⁻², a value close to the fracture energy of Si. An increase of the annealing temperature to 300 and 400°C produced no increase of the surface energy. Further experiments showed that the maximum surface energy value is obtained after a thermal annealing of 10 h at 200°C.

The influence of the SOG thickness on the surface energy was studied by measuring the energy at room temperature and after 200°C/10 h annealing for samples having SOG layers with various thicknesses. A slight increase of the surface energy is observed with increasing SOG thickness for the room temperature bonded pairs (Figure 2.4a). After completion of thermal annealing, no influence of the SOG layer thickness on the surface energy could be observed (Figure 2.4b); all measured values were found to be within the measurement error range.

In order to allow for a qualitative estimation of the bonding strength, bonded pairs were submitted to a mechanical thinning procedure consisting of grinding followed by chemical-mechanical polishing (CMP). One of the Si bonded wafers was thinned down to about 30 μm by grinding and then polished down to 5 μm by CMP. The harsh mechanical thinning process does not affect the quality of the bonded interface.

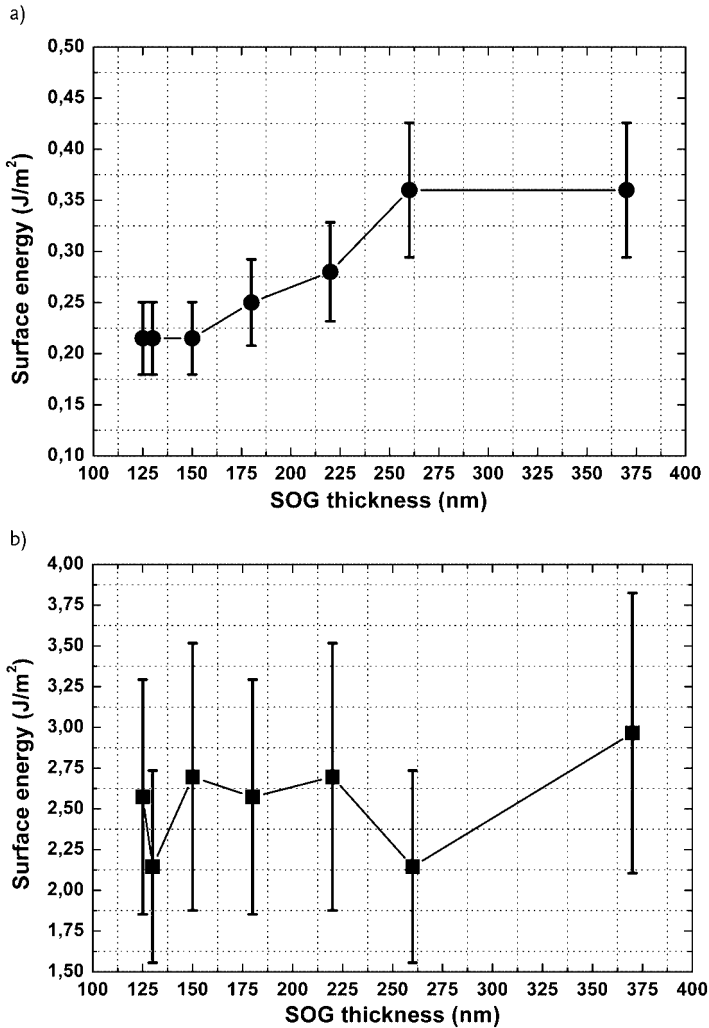


Figure 2.4 Surface energy versus SOG thickness: (a) room temperature bonded wafers; (b) after annealing at 200°C for 10h.

The process described above was further applied for the fabrication of GaAs/Si heterostructures. The main issue in this case is the thermal mismatch of the two materials. Also, GaAs requires processing temperatures below 450°C in ambient air atmosphere or vacuum, or As-rich atmosphere at higher temperatures. The use of a temperature of only 200°C eliminates the complications of using special atmospheres based on toxic gases requiring special handling.

Silicon (p-type, (100)-oriented) wafers were coated with SOG layers and then bonded with semi-insulating (100)-oriented GaAs wafers. The surface energy for

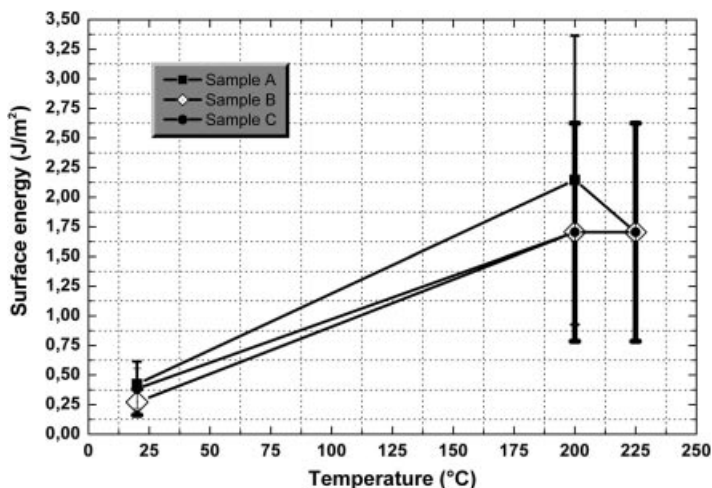


Figure 2.5 Surface energies measured for three different GaAs/Si bonded pairs.

room temperature bonded samples was about 0.4 J m^{-2} , also high if compared to Si/Si hydrophilic bonding.

The bonded pairs were then annealed at 200 and 225 °C for 10 h (increasing the temperature above 225 °C will result in a high stress which leads to debonding and GaAs shattering). Figure 2.5 presents the surface energy for three identically processed GaAs/Si bonded pairs. After annealing at 200 °C, the surface energy reached values of about 2 J m^{-2} . Annealing at 225 °C or increasing the annealing time did not result in any significant increase of the surface energy.

Due to the high thermal mismatch of the two materials, the behavior of the bonded pairs during annealing was investigated by *in situ* measurement of the bow. A large bow developed during heating, reaching 500 μm at 200 °C (with “zero” considered to be the room temperature bow value). On cooling the bonded pair from 200 °C to room temperature, the bow values decreased back to zero following exactly the same path as during heating, showing no hysteresis (Figure 2.6). On repeating the heating/cooling cycle for the same bonded pair, the bow values were found to be the same. No degradation of the bonded interface was observed during this heating/cooling cycling.

This behavior is induced by the SOG layer, which can compensate the high thermally induced mechanical stress. To determine the maximum temperature at which the GaAs/Si heterostructure can be heated, the bow was measured for the heating of the annealed bonded wafers pairs. At temperatures higher than 280 °C the wafers debonded and/or broke. Similar to the Si/Si bonding via SOG intermediate layers, some GaAs/Si bonded pairs were submitted to a mechanical thinning process. The GaAs wafers were thinned by grinding down to 40 μm and then by CMP to 10 μm . This mechanical thinning process did not affect the interface quality, and after thinning the GaAs/Si bonded pairs were heated at 450 °C without any debonding or defect generation. The contribution of the thin wafer to the

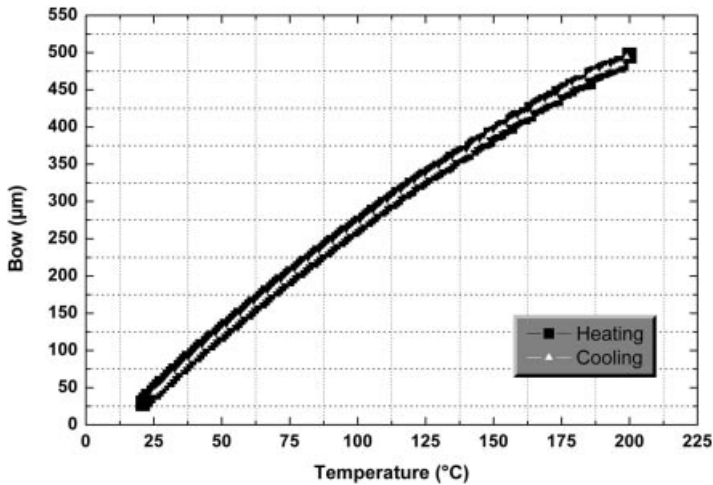


Figure 2.6 Bow measured *in situ* for a GaAs/Si wafer bonded pair during thermal annealing.

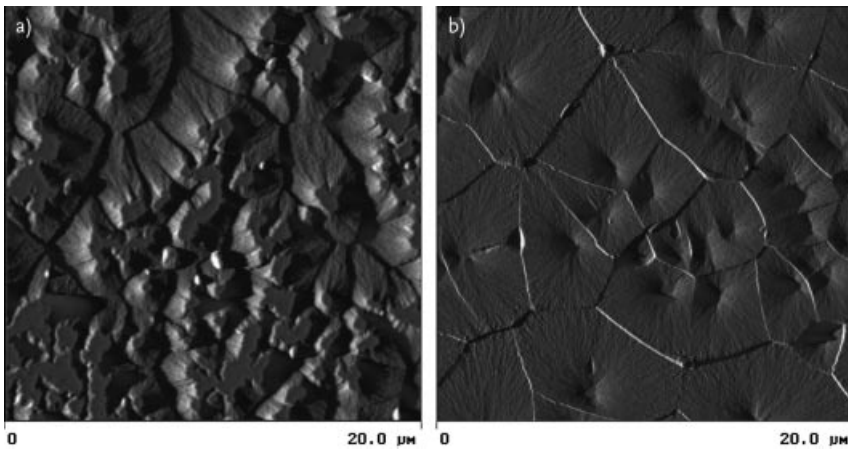


Figure 2.7 AFM images of the two surfaces resulting after separation during tensile tests: (a) SOG on Si; (b) SOG on GaAs.

induced stress became less important and the bonded pair could stand higher temperatures than the initial full-thickness wafers.

Tensile testing was used for bond strength quantification. For this test, $6 \times 6 \text{ mm}^2$ specimens were diced from bonded wafer pairs, which were then loaded in a pulling machine (pull force perpendicular to the bonded interface). After the two wafer pieces were separated it was determined visually that separation occurred due to a crack in the SOG layer and not due to SOG delamination. Further atomic force microscopy (AFM) investigation of the two surfaces resulting after breakage confirmed SOG fracture as the root cause of the separation (Figure 2.7). This result

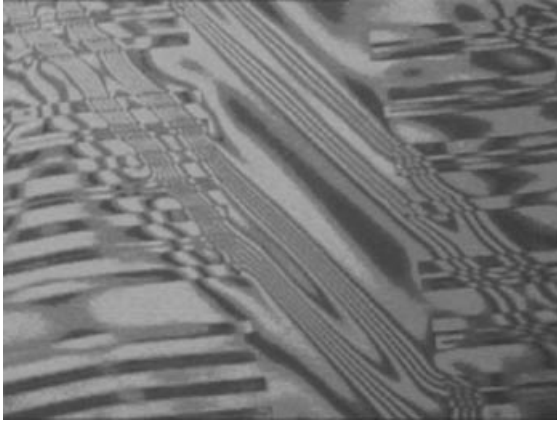


Figure 2.8 Optical photograph of the surface of a planarization SOG layer spin coated on a blank GaAs wafer.

shows the bonding strength is higher than the bulk fracture strength of the SOG material.

2.2.3

Wafer Bonding with Planarization SOG

Despite its flowing properties induced in order to enhance the filling ability of SOG material (crucial for its main function), an integrated circuit (IC) planarization SOG may not be usable for wafer bonding even when deposited on the flat surface of a prime wafer. Figure 2.8 shows a photograph of a planarization SOG spin-coated on a prime-grade GaAs wafer and baked at 180°C. The alternating lines visible in Figure 2.8 are generated by the surface waviness of the SOG layer. Even when coated on a nonpatterned surface, the SOG surface was found not to be flat. In such a case the full area bonding of the two surfaces is not possible. AFM studies were performed on SOG surfaces similar to that in Figure 2.8. The thickness variation of the SOG layer was found to be up to 80 nm for an SOG thickness of ~500 nm. The average microroughness between waves was around 0.5 nm. Similar results were obtained for bonding Si wafers.

Figure 2.9 shows a GaAs/InP (nonpatterned) wafer pair bonded with this type of SOG as adhesive layer. The two wafers are only partially bonded, in some dot-like small areas (dark gray contrast in Figure 2.9), probably only on top of the wave topography of the SOG layer.

A typical procedure for planarization is to perform a CMP planarization step on surfaces with topography too high to be tolerated for wafer bonding. In the particular case of the planarization SOG used, this method was not considered suitable due to the fact the SOG is processed below the curing temperature (<400°C) and CMP was found not to be effective due to material softness. SOG processing

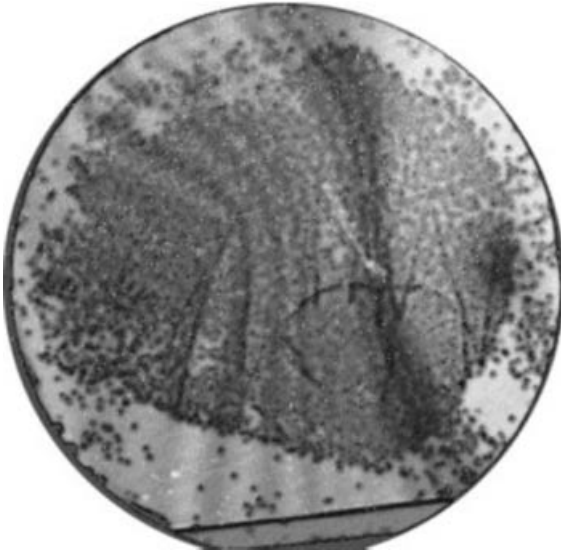


Figure 2.9 SAM image of a GaAs/InP pair bonded with a planarization SOG layer.

above 450°C is not desirable due to the main target of the process development being to set up a low-temperature process. Additionally the thermal curing process of planarization SOG is based on a well-defined thermal profile which would add significant time to the process flow.

The behavior described here is common to various types of materials produced by different vendors. This makes the selection of SOG materials suitable for wafer bonding very difficult, as there are many SOG materials available but only a few types give good bonding results.

2.2.4

Applications of Adhesive Wafer Bonding with SOG Layers

The process development described above was used for an application requiring the transfer of an epitaxial structure grown on a GaAs substrate to a CMOS wafer with the final goal of on-chip optical interconnect fabrication [4]. The bonding process for this application had to be compliant with two requirements:

- low-temperature process imposed by the use of CMOS wafer (<400°C);
- thermal mismatch of the two substrates (Si for CMOS and GaAs).

The process described in the previous sections was found to be compatible with this application.

In the first step, a CMOS wafer was planarized for direct bonding. Planarization consisted of an oxide chemical vapor deposition followed by CMP. After the oxide surface was ready for bonding, a thin SOG layer (~250 nm) was deposited as a

bonding layer. The bonding process was performed as for blank Si and GaAs wafers and thermal annealing was performed at 200 °C.

After the wafer bonding step, the GaAs substrate was removed by etching and the epitaxial structure transferred on the CMOS wafer was patterned for further processing.

In this type of application the SOG material is used for its low-temperature processing and for its ability to provide stress compensation between thermally mismatched substrates.

Besides low-temperature processing, the use of SOG bonding layers is also attractive for nonstandard applications in which the simplicity of SOG processing may be good from both technical and cost perspectives.

Examples of various uses of SOG materials have been reported in the literature: a “compliant layer” between Si and Si_3N_4 [5], a low-temperature silicon-on-insulator manufacturing process with SOG replacing the thermal silicon oxide [6], as well as an intermediate layer allowing anodic bonding of two Si substrates [7].

Due to the increasing amount of wafer bonding-based applications, SOG manufacturers have started to produce materials optimized for wafer bonding. However, not all of these materials are field-proven for wafer bonding applications, and process development is required when starting a new application.

2.2.5

Conclusion

Adhesive wafer bonding based on SOG layers was investigated. The main benefits expected from the use of such bonding layers are low-temperature processing (<400 °C), “clean” process (CMOS-compatible), elastic behavior to allow stress compensation, and compatibility with a wide range of substrate materials.

Tests were performed first using Si wafers and then applied to various compound semiconductors wafers.

Two general types of SOG materials were evaluated: a standard planarization SOG used in IC manufacturing and a silicate SOG material with thermal, optical, and mechanical properties of the cured material similar to those of thermally grown SiO_2 .

The silicate SOG showed good-quality surfaces when spin- or spray-coated on a flat surface and baked in the temperature range 150–300 °C. During process optimization, an optimum baking temperature of 180 °C immediately after substrate coating was determined and a bonding temperature of 200 °C.

Bond tests using Si/Si pairs with a thin SOG layer coated on one of the two wafers were performed for process condition optimization. Process results were evaluated in terms of defects (IR transmission and SAM) and bond strength (crack-opening method and tensile tests). The surface quality of the bonding layers was high enough to allow spontaneous bonding under ambient conditions and defect-free interfaces after thermal annealing. The bond strength obtained after thermal annealing was very high, in the range of the bulk fracture strength of the substrates. Tensile tests revealed no delamination but a fracture into the

bonding layer, showing SOG fracture strength was less than substrates fracture strength.

A final process was applied to bond Si to GaAs wafers in order to check bonding layer behavior for substrate combination with a thermal expansion coefficient ratio of about 2. Silicate SOG exhibited an elastic behavior allowing the two substrates to bend during thermal annealing (bonded pair bow reached about 500 μm) and recover their flat shape once cooled to room temperature. The contribution of wafer thickness to bonded wafer behavior during heating was proven by thinning the GaAs wafer from 625 μm down to 10 μm after annealing at 200 °C. In this case the bonded pair could survive thermal cycling from room temperature to 450 °C, significantly higher compared to “thick” wafer behavior, when GaAs breakage was typically observed at temperatures below 300 °C.

The process was successfully applied for bonding CMOS wafers to compound semiconductor wafers at a maximum temperature of 200 °C [3].

The planarization SOG evaluated showed behavior significantly different from that of the silicate material. Even when coated onto a blank surface this material showed certain waviness of the surface after a baking step. This also showed the major difference between the planarization concept in IC manufacturing, where waviness is acceptable, and the wafer bonding requirement of a perfectly flat surface.

CMP was not effective in this case due to the softness of the SOG material which was only baked for solvent removal (~180 °C) and not fully cured at temperatures greater than 400 °C. Due to the aim of a low-temperature process, fully curing the SOG layer was not an option in this case.

As a result of the surface waviness the bond between the two substrates occurred only partially, proving the material is not suitable for the bonding process.

The results presented in this chapter were obtained using a very small selection of SOG materials from the large variety available. However, the main characteristics of the materials presented here apply to a large number of different SOG materials from various vendors, as the chemistries used are similar in principle.

The choice of a bonding layer material suitable for a specific application is a relatively difficult and requires, in most cases, experimental evaluation and process optimization considering the boundary conditions of each application.

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6

Plasma-Activated Bonding

Maik Wiemer, Dirk Wuensch, Joerg Braeuer, and Thomas Gessner

6.1

Introduction

Several years ago, low-temperature wafer bonding was implemented industrially. In particular, direct wafer bonding or short direct bonding has a major advantage in microelectromechanical systems (MEMS) packaging because no additional intermediate layers, like in eutectic or adhesive bonding, are required. Direct bonding uses the formation of covalent bonds caused by the atomic contact of two clean and smooth surfaces and subsequently annealing at temperatures above 800 °C [1, 2]. As a result of system integration and enhanced packaging density it is essential to reduce these relatively high annealing temperatures. One possibility to reduce these process temperatures is the implementation of plasma activating procedures prior to bonding. Therefore, the bond technique here presented is called plasma-activated bonding (PAB). This activation process is generally employed because various suppliers of wafer bond equipment have offered special plasma-activation tools for several years.

In principle, two solids, regardless of which materials they are, can be bonded using PAB subject to the condition that their surfaces are flat and clean. The implementation of the PAB process requires a special high surface quality of the process wafers. The most important parameters are surface roughness, wafer flatness, and surface contamination caused by technology process steps before the bonding step. Typical values of 4-inch or 6-inch wafers are: surface roughness (root mean square) less than 0.5 nm (measured area $10 \times 10 \mu\text{m}^2$), flatness less than $10 \mu\text{m}$, and total thickness variation less than $2 \mu\text{m}$ [3–5]. In practice, it is expensive and associated with much technical effort to create a smooth and flat bonding surface [3]. Especially, the PAB of silicon is an area that has become of considerable scientific and commercial interest. Many researchers have investigated this bond technique and developed various theoretical models and proved these models with several experiments [2, 4, 6–13].

The system integration and packaging of microelectronic, micromechanical, and microanalysis systems are increasingly affected by three-dimensional chip stacking [14]. The fabrication of bonding on the wafer or chip scale plays a major

role therein [15]. Different functionalities often require the implementation of heterogeneous materials with a large mismatch in coefficient of thermal expansion (CTE) or materials with a low melting point. Therefore the process temperature during wafer bonding is often the limiting factor for the development of MEMS.

The theory of direct bonding and the mechanism of plasma activation processes are presented in this chapter. Furthermore, a classification of PAB is given. Based on this classification, the principle of low- and atmospheric-pressure plasma activation of materials used in the direct bonding process is explained. The process flow of PAB and the characterization of the bonds produced are also introduced. The last section focuses on some applications for PAB.

6.2

Theory

This section describes briefly the theory of direct bonding, the mechanism of plasma activation processes, and the physical definition of plasma to enable an understanding of the PAB technique.

6.2.1

(Silicon) Direct Bonding

Two different methods are known for the direct bonding process. One is hydrophobic direct bonding. The other, and more interesting for plasma activation, is hydrophilic direct bonding. To understand the mechanisms of plasma treatment of a silicon surface, it is necessary to explain the procedure of hydrophilic direct bonding. The process includes pre-bonding at room temperature and annealing at high temperatures in order to develop strong covalent Si-Si bonds.

In the case of hydrophilic direct bonding, the bond process at room temperature occurs after contact of the wafers by hydrogen bonds between the chemisorbed water molecules located on the opposing wafer surfaces [3, 5, 16]. Typically, external pressure is applied to facilitate contact of the wafer surfaces. The bond strength particularly depends on the number of hydrogen bonds and therefore on the number of silanol groups and water molecules. A subsequent heat treatment (annealing) takes place, to increase the strength of the bonded wafers. Thereby the water molecules diffuse out either along the interface to the outside or through the native oxide to the bulk silicon. The wafers move closer together and form hydrogen bonds between the Si-OH groups. With increasing temperature the opposing silanol groups can react with each other to form covalent siloxane bonds (Si-O-Si) [1-3]. This reaction is the following:



The reasons for significant bond strengths on heat treatment at temperatures above 800°C are enhanced water molecule diffusion and increased viscous flow

of the materials. Especially, the increased viscous flow leads to greater surface contact between the wafers. In summary, a high bond strength depends on the cleanness of the silicon surface, the number of hydrogen bonds formed, and the diffusion of water molecules out of the interface during annealing at high temperatures [2, 3].

6.2.2

Mechanisms of Plasma on Silicon Surfaces

Tan *et al.* described the surface and interface effects caused by plasma treatments, which result in an increase of the bond strength of a silicon wafer compound at low temperatures [17]. Those authors propose four mechanisms:

- 1) **Removal of contaminants on the wafer surface.** The plasma treatment removes organic contaminants and adsorbates from the substrate surface. These contaminations increase the surface potential barrier and hinder the formation of strong bonds. The activation process cleans the surface and produces more dangling bonds which can enhance the surface energy.
- 2) **Increase in the number of silanol groups.** The plasma initiates a modification of the surface. Hence, the number of silanol groups on the silicon wafer is increased. As described in the process of hydrophilic direct wafer bonding at the beginning of this chapter, the bond strength of a wafer compound is correlated with the number of siloxane bonds formed, which are generated by the silanol groups on the wafer surface via the chemical reaction shown in Eq. (6.1) [1]. However, the work of Wiegand[2] shows that the density of the OH groups is almost the same as that without plasma treatment. With a method called power spectral density analysis and with the help of atomic force microscopy, he represented each surface's feature frequency or wavelength and verified that the total surface area increases after the plasma treatment. Therefore, the total number of silanol groups on the wafer surface increases, whereas the surface density of the silanol groups remains unchanged. Thus, more silanol groups can react with each other and the silicon surfaces are bonded via an increased number of oxygen bonds. So, more siloxane bonds are formed via the chemical reaction of Eq. (6.1) and the bond strength is finally increased. The increasing amount of silanol groups on the wafer surface is also mentioned in [6–8].
- 3) **Improvement of the diffusivity of water and gas trapped at the interface.** Plasma activation ensures an increased diffusivity and thus enhances the evacuation of water and gas trapped at the interface. Consequently, the reversible chemical reaction of Eq. (6.1) will intensify, so that the bond strength is significantly increased at lower temperatures.
- 4) **Enhancement of viscous flow.** A viscous flow of the surface layer at temperatures above 800°C initiates the mechanism of hydrophilic direct bonding to complete bond formation of the wafer pair. Accordingly, it is necessary that

this viscous flow of the surface layer occurs at lower temperatures. A SiO_2 layer, for example, is damaged by the plasma process and it becomes porous [18]. Thus, the layer contains more water than it does before the plasma treatment, so that the viscosity is much reduced and a viscous flow might take place at lower temperatures. Therefore, a larger contact area can now be available, so that the bond strength is increased.

To sum up, plasma activation enhances the bond strength in comparison to that of conventional direct bonding. This increase in bond strength using plasma treatment is based on cleaning of the wafer surface, an increase in the number of silanol groups, enhanced diffusivity, and lower viscosity of the oxide.

6.2.3

Physical Definition of a Plasma

A physical plasma is an ionized gas with a neutral electrical charge. That means that the density of positive and negative charges is equal [1]. In principle, a plasma consists of electrons, ions, radicals, and photons, for example ultraviolet (UV) radiation [19]. The electrons that are required to ignite the plasma are produced using a high-frequency (HF) alternating electrical field. This field is applied between two electrodes in the reactor chamber. In that field electrons are accelerated and collide with the plasma gas molecules. During this collision more and more electrons are ejected from the gas molecules due to the high kinetic energy of the accelerated electrons. These generated electrons lead to the creation of positively charged ions and radicals. The ions are also accelerated in the HF field. Because of the much higher mass of the ions compared to the electrons, the ions are not able to follow the fast alternating field. This is the reason why ions are accelerated in one direction, that is, towards the wafer. The high kinetic energy of the ions leads to an ion bombardment on the wafer surface and so the activation takes place [20].

6.3

Classification of PAB

The classification of the plasma types for PAB is quite challenging. There are several techniques to achieve plasma activation. These techniques can be subdivided in terms of the gases that are used in the process (oxygen, nitrogen, hydrogen, ammonia, argon, etc.), the atmosphere (low pressure, atmospheric pressure), and the plasma mode (reactive ion etching (RIE), inductively coupled plasma RIE (ICP-RIE), etc.) [21]. The background of the classification for the PAB used herein is the order of the technical development as well as the main parameter “pressure” of the plasma activation for bonding. Figure 6.1 represents this classification.

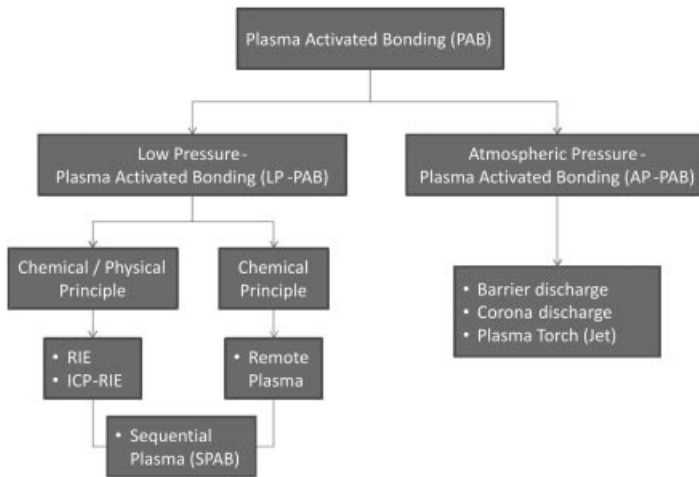


Figure 6.1 Classification of PAB.

6.3.1

Low-Pressure PAB

Low-pressure plasma systems operate in a vacuum, which typically ranges from 0.1 to 100 Pa with a continuous gas flow into the reactor. As mentioned before, there are a multiplicity of plasma modes that can be applied to activate the wafer surface. A commonly used plasma mode is RIE [4, 10, 22]. This RIE mode is usually adopted in dry etching processes. By reducing the plasma parameters, such as the HF power, it can also be used for surface activation. Also a variation of RIE, i.e., ICP-RIE, can be used in the wafer activation process [23].

In both RIE and ICP-RIE plasmas, ions and radicals interact with the surface. In contrast to these chemical/physical methods, another treatment is the so-called remote plasma which only uses chemical components. For the remote plasma, mostly neutral radicals react during the treatment. The advantage of this process is that ion bombardment is avoided so that the surfaces are less damaged. Longer plasma exposure times are possible in comparison to the RIE and ICP-RIE modes mentioned above [11, 24]. A special procedure for the remote plasma is the sequential plasma mode [12, 13]. In this special method the wafers are first activated with a short RIE plasma treatment, directly followed by a radical treatment [12]. Both plasma modes are applied in the same reactor chamber, so that no wafer handling between the two steps is necessary. An additional microwave source and an ion-trapping metal plate are used in the plasma reactor to generate the radicals. After the ion bombardment the radicals are separated from the ions by a trapping plate. The effect of the plasma on the wafer surfaces changes from chemical/physical plasma treatment to a chemical treatment caused by reactions between the radicals and the atoms on the surface [25].

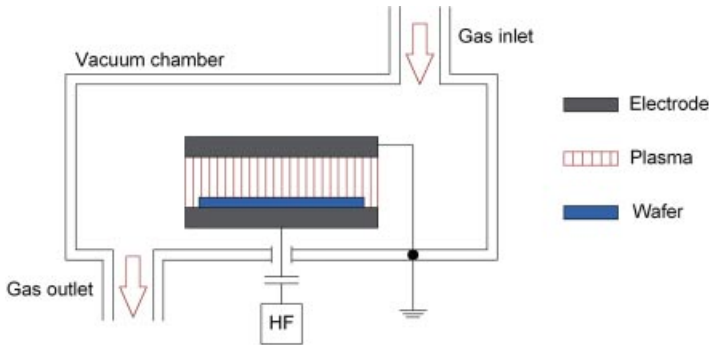


Figure 6.2 Schematic of a plasma reactor for low-pressure plasma activation.

Figure 6.2 shows a typical plasma reactor for low-pressure activation. Low-pressure activation requires a vacuum, additional process gases, and a HF electric field between the two electrodes.

The substrate exposed to the plasma is activated by ion bombardment and chemical reactions caused by radicals. During the period of positive voltage at the HF electrode the electrons move to this electrode. Due to the work function the electrons are not able to leave the electrode within the positive half-wave of the applied voltage. Therefore this electrode is negatively charged up to typically 1000 V (bias voltage). The massive ions are not able to follow the HF field so that they move to the negatively charged electrode where the wafer is placed. In most cases an operation frequency of 13.56 MHz is used [20, 26]. In contrast to conventionally used bias voltage for etching processes, the ions in plasma activation are only accelerated to approximately 100 V [4]. Beside the process gas used, the most important parameters for plasma activation are generator power, chamber pressure, operating distance, process time, and gas flow.

6.3.2

Atmospheric-Pressure PAB

Atmospheric-pressure PAB is a method to ignite plasma without using a low-pressure environment. That means that no expensive equipment for vacuum generation is needed [27].

Gabriel *et al.* reported that there is an important difference between treatments using low- and atmospheric-pressure plasmas [27]. For a plasma process at atmospheric pressure the interaction of ions with the substrate is negligible. In contrast, the low-pressure plasma treatment is dominated by physical processes with highly energetic ions and electrons on the substrate surface. The lifetime of ions in atmospheric-pressure plasma is below 100 μ s. So there is almost no influence on the substrate surface [27, 28]. This is the reason why the surface processes using an atmospheric-pressure plasma can be described by the intense UV radiation,

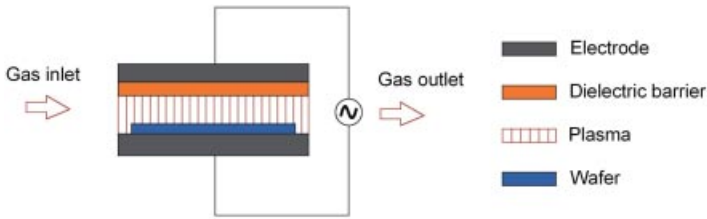


Figure 6.3 Schematic of atmospheric-pressure plasma activation.

which is generated by the dissociation of ions, the chemically active radicals, and the high concentration of electrons (about 10^{14} – 10^{15} cm⁻³) [27, 28].

With an atmospheric-pressure plasma it is possible to ignite the plasma both at specific local areas and the whole surface of the substrate. To generate stable plasma at atmospheric pressure, a method different from that of low-pressure plasma activation is required. Between two electrodes the plasma gas is ignited via an alternating voltage. To avoid sparks a dielectric has to be fixed to one or both of the electrodes. This mode is known as the dielectric barrier discharge (DBD) [9, 27–29]. Originally the DBD, also called silent discharges, was developed by Werner von Siemens (1857) to create ozone. For the DBD the shape of the electrode has to be similar to the substrate geometry to cover the entire surface [30].

The principle of the discharge with one dielectric barrier is shown in Figure 6.3. The electrical discharge between two metallic electrodes is separated by an isolator barrier. As a result of the discharge at atmospheric pressure a plasma is created in the space between the electrode and the isolator barrier.

The DBD uses alternating high voltage (1–10 kV) with frequencies of 0.5–500 kHz. Typical operating distance between the barrier and the ground electrode varies from 0.1 mm to several centimeters. Dielectric materials are often glass, quartz, ceramics, or other materials with high breakdown voltage [31, 32].

As mentioned before, the DBD enables local surface activation. Eichler *et al.* call this method “plasma printing” [29]. An additional mode of local atmospheric-pressure plasma activation is the plasma torch. The plasma torch can be used like a sequential writing method. In this mode the plasma is stable on the top of the nozzle and each geometry can be activated [33, 34].

6.4

Procedure of PAB

6.4.1

Process Flow

A schematic of a typical PAB process flow is shown in Figure 6.4. First, the wafers are often cleaned in deionized water or hydrogen peroxide-based solution (RCA,

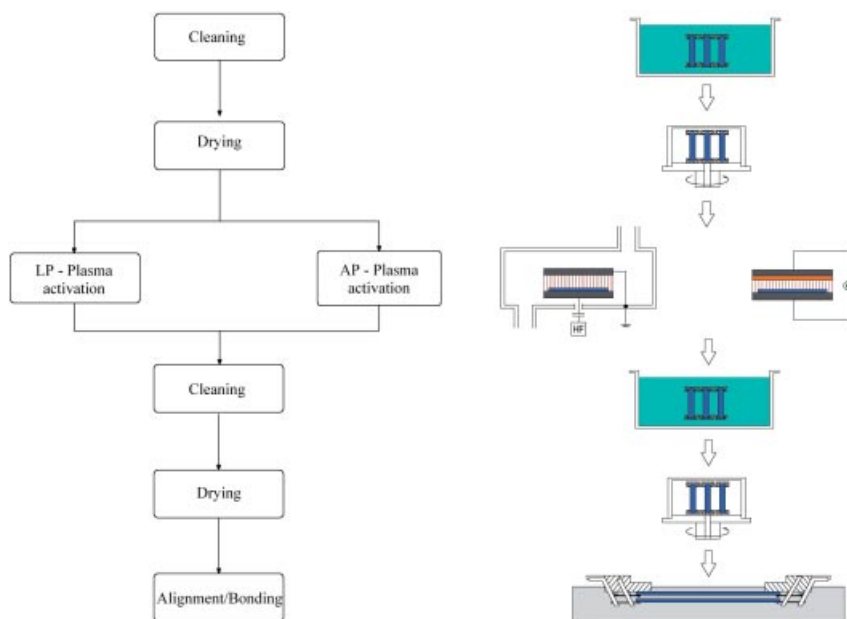


Figure 6.4 Process flow of PAB. (LP, low pressure; AP, atmospheric pressure.)

Piranha). This pretreatment reduces the organic and inorganic contaminations of the surface and creates hydrophilic surfaces. Thereafter the wafers are dried, for example in a spin dryer, and subsequently treated by plasma exposure. After plasma treatment the wafers are dipped in deionized water or hydrogen peroxide-based solution and dried. However, the wet chemical cleaning or the water dip is not essential for a PAB process. The next step is the pre-bonding procedure. Conventionally used bond equipment can be applied, which allows the alignment and the bonding of the wafers as well as the monitoring of all bonding parameters, such as temperature, time, and pressure, during the process. After the pre-bonding process at room temperature an annealing step can be optionally used to increase the bond strength.

6.4.2

Characterization Techniques

The quality of a wafer bond can be described by defect rate, hermeticity, bonding strength, and induced stresses. A number of techniques can be used to characterize a bond. The most important physical parameter of a plasma-activated bond is the bond strength. There are various measurement techniques to characterize the bond strength. A frequently used method is the crack-opening method, which is shown schematically in Figure 6.5a. With this technique a razor blade (thickness

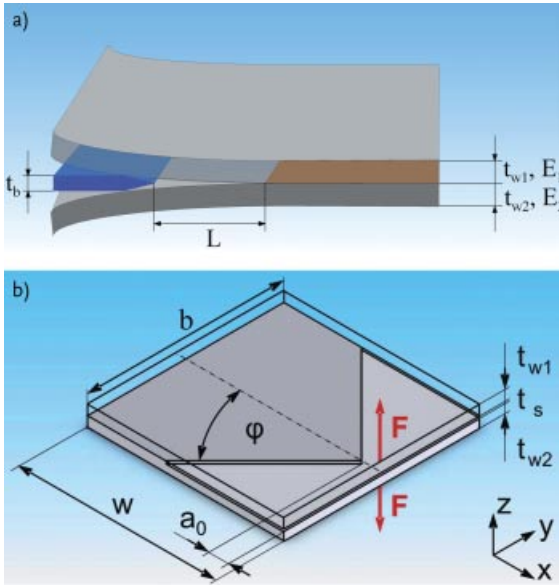


Figure 6.5 Schematics of test methods: (a) crack-opening method; (b) micro-chevron test.

t_b) separates the stacks into two parts (thicknesses t_{w1} , t_{w2} ; Young's moduli E_1 , E_2). The inserted blade creates two new surfaces and forms the equilibrium crack length L . The bond strength is defined by the surface energy γ and is given by

$$\gamma = \frac{3t_b^2 E_1 t_{w1}^3 E_2 t_{w2}^3}{16L^4 (E_1 t_{w1}^3 + E_2 t_{w2}^3)} \quad (6.2)$$

Besides the crack-opening method, tensile or blister tests can be applied for these investigations [3, 35].

The crack-opening method provides no significant bond strengths due to fact that the crack length L is determined very subjectively by the operator. This inherent measurement uncertainty makes it very hard to compare published results between each other.

A much more accurate method to determine the bond strength is the so-called micro-chevron test (MC test). The MC test is a specially adapted method for microsystems technology [36, 37]. In this case the bond strength is determined by the fracture toughness k_{ic} . However, this test requires special sample preparation in an etch process to produce the required geometries (see also Figure 6.5b). Due to the special characteristics of the test, the crack length is not determined experimentally. The maximum force F_{max} is measured in a tensile test. The fracture toughness is calculated using the maximum tensile force, the geometrical parameters (width w , length b), and a specific geometry value γ_{min} , which is specified in numerical analysis [36, 38]. The fracture toughness is determined as

$$k_{ic} = \frac{F_{max}}{b\sqrt{w}} \gamma_{min} \quad (6.3)$$

Besides the characterization of the bond strength, hermeticity is an important aspect for MEMS applications. Visser *et al.* [39] performed leak tests with helium for plasma-activated bonds according to MIL-STD 883. Both the PAB and the direct bonded (annealed at 1100°C) specimen showed a leak rate of less than 5.0×10^{-8} mbar l s⁻¹. Due to the small cavities (typical volume of 0.1 mm³) of MEMS, ultralow leak rates (10⁻¹⁶ mbar l s⁻¹) must be realized. This ultrahigh resolution requires much more sensitive leakage measurements, so that the conventionally used methods like the helium leak tests are not adequate. Millar and Desmulliez described in a review ultralow leak rate detection methods. These methods ensure accurate hermeticity testing of MEMS [40].

6.4.3

Experiments and Results

Single-side-polished 4-inch silicon wafers with a thickness of 525 μm were used. All wafers were p-doped and (100)-orientated. The process flow of the following wafer preparation is based on Figure 6.4. First, all wafers were cleaned, using the RCA procedure. In the next step a low-pressure RIE plasma reactor was applied to activate the wafer surfaces (Figure 6.2). For plasma treatment duration, an optimum of 5 min was determined, which was used in the subsequent experiments. Process gases oxygen and nitrogen were used during the activation process. This activation process was followed by rinsing the wafers for 10 min in deionized water. After the pre-bonding process at room temperature, the wafers were annealed at various temperatures, which ranged from 40 to 200°C. After dicing into single chevron test structures, the bond strength of the silicon–silicon interface was characterized using the MC test. As seen in Figure 6.6a, for all plasma-treated wafer stacks, the fracture toughness is two or three times higher than that for the nonactivated reference wafer stack [41].

Eichler *et al.* [9, 30] reported a dielectric barrier discharge at atmospheric pressure for low-temperature direct silicon wafer bonding (Figure 6.3). The measurement of the surface energy with a modified crack-opening method is realized *in situ* during annealing from room temperature to 200°C. Figure 6.6b presents these results against the process gas variation. The experiments show that at annealing temperatures below 100°C the surface energies are two to three times higher compared to the RCA-cleaned reference silicon wafer stack. By annealing the wafers up to 100°C and treating with synthetic air (80 vol.% N₂ + 20 vol.% O₂) or nitrogen plasma a linear increase of the surface energy can be observed. The highest surface energy at 100°C can be achieved with a synthetic air (N₂/O₂) treatment. The treatment with the process gas oxygen shows no significant increase below 100°C. By annealing at temperatures between 100 and 200°C the surface energy of the oxygen-treated surfaces rises strongly. After annealing at 200°C the oxygen plasma-treated wafers achieve the highest final value among all process gases [9, 30].

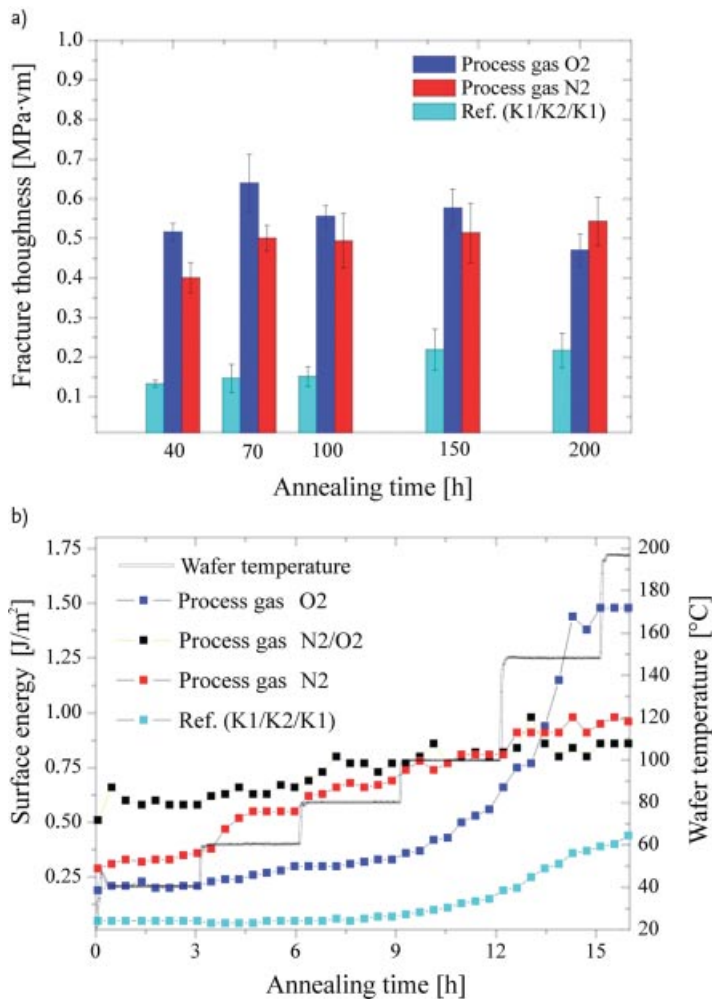


Figure 6.6 Fracture toughness and surface energy during annealing for various activated silicon wafer stacks: (a) low-pressure PAB; (b) atmospheric-pressure PAB.

6.5 Applications for PAB

Some selected applications are discussed in the following subsections. Some sensors are introduced: a pressure sensor and an image sensor. An optical microsystem and microfluidic packaging are also presented. At the end of this section the compatibility of PAB with the complementary metal–oxide–semiconductor (CMOS) standard process is illustrated. The applications described here are each representative for one of the different plasma modes mentioned above, for example, ICP-RIE, DBD, and sequential plasma treatment.

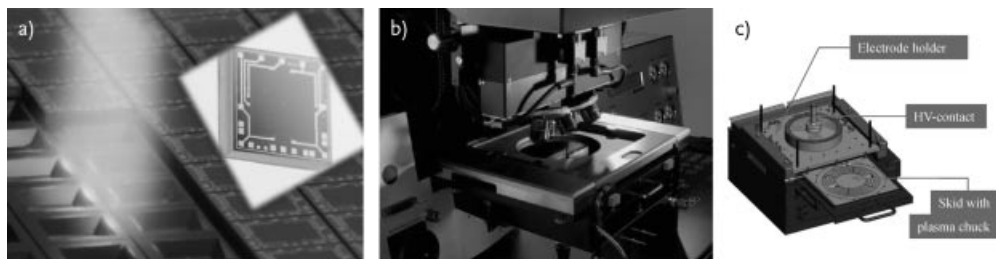


Figure 6.7 (a) Pressure sensor (in cooperation with EPCOS AG). (b) Mask aligner. (c) Tool for an atmospheric-pressure plasma activation system (upgradable in the SUSS Mask Aligner) [42].

6.5.1

Pressure Sensor

Figure 6.7a shows a pressure sensor (EPCOS AG) used as a demonstrator for atmospheric-pressure PAB. Here, a DBD activation of silicon wafers was applied at the Fraunhofer Institute for Surface Engineering and Thin Films. A grounded chuck acting as wafer carrier and an indium tin oxide (ITO)-coated high-voltage glass electrode are used for the activation equipment. In this case the ITO layer is the real electrode and the 750 μm thick glass substrate is the dielectric barrier. The gas-flushed gap between the substrate surface and the counter electrode has an operating distance of 500 μm . The discharge is powered by a corona generator which operates at a frequency of 28.5 Hz. The transfer of this technique within a mask aligner is currently planned (Figures 6.7b and c).

Before low-temperature bonding of the pressure sensor at the Fraunhofer Research Institution for Electronic Nano Systems, the ideal plasma parameters have to be determined. Hence, the process gases nitrogen and synthetic air (80 vol.% N_2 + 20 vol.% O_2) and a process time of 40 s were chosen. Before and after the atmospheric-pressure plasma treatment a cleaning step using deionized water was applied [30]. To increase the bonding strength an annealing at 350 $^{\circ}\text{C}$ for 6 h in nitrogen atmosphere was carried out. After dicing the sensors were characterized by burst tests. The bond strength of a synthetic air plasma-activated specimen was two times higher than that of nonactivated ones [42, 43].

6.5.2

Optical Microsystem

The development of a high-density optical microsystem applied to laser Doppler velocimeter sensors is presented by Higurashi and coworkers [39, 44]. Here, a two-step PAB technique is used as an alternative to eutectic AuSn or Au–Au thermocompression bonding.

Due to the high process temperatures (above 300 $^{\circ}\text{C}$) of AuSn and Au–Au thermocompression bonding, Higurashi and coworkers developed an Au–Au surface-

activated bonding technique. To clean the surfaces, low-pressure plasma activation with argon as process gas is applied. Subsequently Au–Au chip bonding takes place by contacting the substrates in ambient air for 30 s at temperatures below 250 °C [45]. Higurashi [44] asserted that an Au–Au bonded laser diode did not show any significant changes in electrical and optical performance compared with an unbonded one. After the first bonding step a further surface-activated bonding step is introduced to fabricate the microsystem (Figure 6.8). In this step, the optical bench including the bonded laser diode, micromirrors, and electrodes onto patterned silicon and a glass substrate including a photodiode, electrical interconnections, and microlenses are bonded at 150 °C.

6.5.3

Microfluidics Packaging

Howlader *et al.* developed a room temperature PAB technique using sequential plasma activation [25]. At first the wafers are exposed to an oxygen RIE treatment. After this process a microwave nitrogen radical treatment is applied. By using the sequential plasma activation as an *in situ* process, contamination is negligible. The implemented ion trap has two main functions. First, in the RIE mode the ion trap works as the counter electrode. Second, during the microwave treatment the trap operates as a filter to separate the uncharged radicals. The typical parameters for the oxygen RIE treatment are 13.56 MHz, 30 Pa chamber pressure, 200 W generator power, and 60 s process time. For the microwave plasma typical parameters are 2.45 GHz, 100 Pa chamber pressure, and 2000 W generator power. After the plasma activation the wafers were pre-bonded and kept in atmospheric air. Howlader *et al.* characterizes the bond strength by tensile testing. With this sequential plasma activation bond strengths similar to those of the bulk material (silicon or glass) could be achieved. To test the hermeticity a krypton-85 leak test was applied. The sealed cavities were placed in a high-pressure chamber with radioisotope krypton-85 gas mixture. To measure the radiation coming out of the specimen a scintillation counter was used. With this method the leak rate was determined to be lower than $1 \times 10^{-9} \text{ Pa m}^3 \text{ s}^{-1}$.

Howlader *et al.* used the technique described above to produce a glass–glass microfluidic device. Based on the high bonding strength, and the hermetic sealing behavior, this technique can be used for such microfluidic applications. Furthermore, the low bonding temperature guarantees the survival of living cells in the microchip.

6.5.4

Backside-Illuminated CMOS Image Sensor

Optical devices such as image sensors are another application for PAB. Dragoi *et al.* [46] bonded a fully processed CMOS wafer to a blank one using PAB. First, the CMOS wafer was polished to achieve a flat surface which corresponds to the requirements of direct bonding. After that, plasma-enhanced chemical vapor

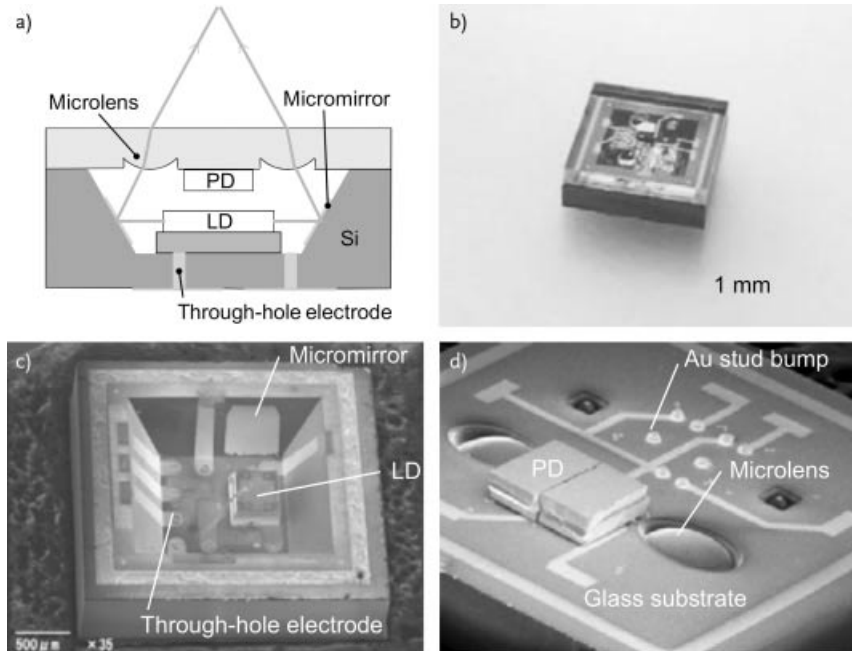


Figure 6.8 High-density optical microsystem: (a) cross-sectional assembly; (b) fabricated system; (c) integrated laser diode (LD) on optical bench; (d) integrated photodiode (PD) on Pyrex glass [44].

deposition was applied to form a silicon dioxide coating on both wafers. Subsequently an oxide layer densification was used to remove gas from the oxide layer. The oxide was then polished using standard chemical mechanical polishing (CMP). In the second step both wafers were plasma-activated and aligned by edge-to-edge alignment and optical alignment followed by spontaneous pre-bond at room temperature. After pre-bonding, the wafer stacks were annealed at 200–400°C. The CMOS substrate was back-thinned by grinding and etching. The final technology step for processing the CMOS image sensor was adhesive wafer bonding of the optical elements like filters, lenses, and spacers.

6.5.5

CMOS Compatibility of Low-Pressure PAB

Sanz-Velasco *et al.* [47] determined the compatibility to the CMOS process with an oxygen plasma treatment prior to direct bonding. This is difficult because the impact of the plasma treatment on the electrical properties of the bonded interface and on the reliability of standard electronics is unclear. The plasma can have an influence on the components by contaminations or radiation damage. Here, contamination can be induced by the deposition of nonvolatile contaminants from the sputtering procedures or mobile ion contamination. The potential difference

between the plasma and the wafer and the plasma and the chamber walls justifies this sputtering procedure. For RIE, the wafer is exposed to a bombardment by energetic ions, electrons, and photons, for example UV radiation. The photons can cause radiation damage in the materials. Such damage can be in the form of electron traps in gate oxides which are the reason for shifts in the threshold voltages of MOS devices. Atoms in the surface can also be displaced and implanted. Furthermore, destruction of the gate oxide can occur.

In order to test CMOS compatibility, Sanz-Velasco *et al.* investigated the influence of plasma activation on application-specific integrated circuits. For this they manufactured test structures using the CMOS CYE 0.8 μm process from Austria Mikro Systeme International AG. According to the CYE process a top passivation layer, consisting of 1 μm silicon oxynitride and 1 μm silicon nitride, is superimposed on the electronics to protect them during the plasma treatment. Only the contact pads are treated. ICP-RIE was used with a gas pressure of 40 mtorr, a radio-frequency power of 15 W, and a coil power of 800 W to expose the components for 30 s to the oxygen plasma [47].

To characterize the various influences, Sanz-Velasco *et al.* measured the I - V characteristics of MOS transistors, the C - V characteristics of MOS gate capacitances, and the frequency of oscillators prior and after the plasma treatment. All measurements showed no significant change. Thus, the authors concluded that the oxygen plasma treatment in ICP-RIE can be used for CMOS applications.

6.6

Conclusion

PAB is a fully CMOS-compatible technology that provides unique possibilities for fabrication and improvement of three-dimensional integrated microsystems. Process flow, limitations, and parameters for PAB at low and atmospheric pressure with sufficient bond strength, packaging reliability, and defect-free bonding interfaces are readily available in the literature. The main advantages of PAB are the low bonding temperature, the compatibility with standard integrated wafer processing, and the wafer bonding of heterogeneous materials with a high CTE mismatch or temperature-sensitive materials. However, PAB requires special wafer surface preparation such as CMP to reduce surface roughness, wafer flatness, and minimal surface contamination. For defect-free PAB, cleanliness prior to bonding should be at a very high level. In conclusion, PAB is a well-known technology and one possibility for three-dimensional wafer stacking used in MEMS packaging.

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12

Cu/SiO₂ Hybrid Bonding

Léa Di Cioccio

12.1

Introduction

Bonding of metal surfaces is extensively used for microelectromechanical system sealing, power devices, heat dissipation or three-dimensional interconnections. For these applications, techniques such as thermocompression, with or without eutectic alloys or adhesives layers, bumps with low-temperature solders, or direct bonding have been implemented [1–4].

Moreover, for more Moore and more than Moore applications, low-temperature bonding and metal bonding are becoming the main drivers of the latest developments. As copper is the main metal used for CMOS interconnects, a high-density copper interconnection between layer structures is expected to be important for future three-dimensional integration of discrete electronic devices fabricated on the basis of various technology/design concepts.

To address that, copper/oxide surface direct bonding presents many attractive advantages: compatibility with front-end or back-end requirements for a sequential approach, low-temperature process, through-interconnect layer compatibility, high accuracy of alignment during bonding, as the surfaces are bonded at room temperature no underfill is needed, and a very high interconnect density is possible.

Direct wafer bonding refers to a process by which two mirror-polished wafers are put into contact and held together at room temperature by adhesive forces, without any additional intermediate materials [5]. Direct wafer bonding can be achieved in clean rooms at room temperature with ambient air, without any pressure and without any adhesive materials. However, high bond strength and a void-free bonding interface are required in order to provide reliable and high-performance devices.

Copper/oxide surface direct bonding is a technology that enables three-dimensional metal interconnects at the same time as a bond between two piled

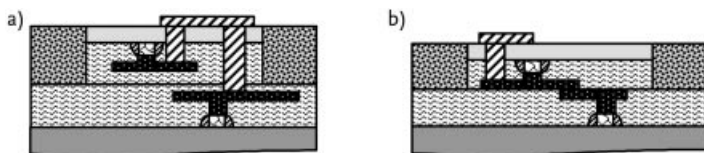


Figure 12.1 (a) Die-to-wafer integration scheme with oxide bonding. This bonding technology needs two through-silicon vias. (b) Die-to-wafer integration scheme with patterned copper bonding.

up two-dimensional processed strata. Otherwise, with an insulating layer at the bonding interface, two through-silicon vias (TSVs) of different depths are needed to connect the upper and the lower layer. A single TSV technology is feasible because of localized electrical conductive pads at the bonding interface obtained with copper/oxide surface direct bonding (Figure 12.1).

Direct copper bonding experiments have led to 8 μm pitch interconnections of thin copper electrodes at around 350 $^{\circ}\text{C}$ using oxide bonding technologies for local copper thermocompression bonding [6]. The diffusion of copper atoms across a thick adsorbate (mainly oxide) layer was obtained after long-time annealing in order to obtain sufficient bonding strength and electrical conductivity. Bumpless copper electrodes with a pitch of 6 μm fabricated with the applied damascene process were also demonstrated. The surfaces were bonded at room temperature under vacuum after Ar sputtering of the surfaces in order to remove the native copper oxide layer. The use of high-vacuum conditions increased the bonding process complexity, such as difficulties in sample handling and alignment procedure, as well as leading to low manufacturing throughput and high cost. More recently this process was modified allowing bonding at atmospheric pressure in an O₂ atmosphere after the same surface preparation under vacuum [7].

The best process has to be easily integrated into the dual damascene back-end-of-the-line (BEOL) process, using standard BEOL process steps. So we aimed to develop a process based on surface preparation using chemical mechanical polishing (CMP), with bonding at room temperature in ambient air without added bonding pressure during the bonding. The bonding annealing temperature should be in the range allowed by the BEOL requirements, that is, under 400 $^{\circ}\text{C}$. This process is described below.

More recently, we developed a Cu/Cu direct bonding process on either plain or patterned surfaces at room temperature in ambient air without bonding pressure [8–12]. Bonding of 5 and 20 μm copper pads with a pitch of 10 and 40 μm , respectively, was performed with wafer-to-wafer alignment of 0.6 μm (mean value) and a standard deviation of $\sigma = 0.4 \mu\text{m}$. A specific contact resistivity of 1 $\Omega \mu\text{m}^2$ was obtained from a Kelvin structure [13–16] and was reduced to 47 m $\Omega \mu\text{m}^2$ in this work.

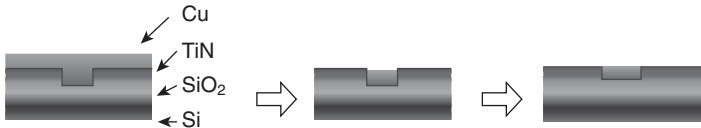


Figure 12.2 Damascene CMP process with dishing controlled on copper pads.

12.2

Blanket Cu/SiO₂ Direct Bonding Principle

12.2.1

Chemical Mechanical Polishing Parameters

Damascene copper CMP is widely used in production lines as an efficient back-end process for copper removal down to the oxide. The standard damascene CMP process is the process most used to planarize metal levels in microelectronics. However, to avoid leakage, the process usually induces a dishing of the copper pads on patterned surfaces. This surface topology leads to important inconveniences: copper pad dishing and oxide erosion. These are critical issues if one wants a direct copper contact between two face-to-face copper pads. At CEA-Leti, an optimized CMP-based process was implemented on patterned surfaces to reach a high surface planarization level (Figure 12.2). The CMP optimization (pad/slurry matching) target is to minimize copper dishing and oxide erosion with respect to the lay-out, and a standard wet cleaning is applied to remove the slurry residues and the remaining particles.

Wafers with 5 μm copper pads and a copper density of 20% were designed to achieve direct Cu/SiO₂ bonding. After CMP-based preparation, a dishing of less than 10 nm was obtained on 5 μm width pads over all of the wafer.

After cleaning, wafers were introduced separately in an EVG SmartView™ alignment tool. Alignment was optically achieved using specific alignment marks. The bonding wave was then initiated with a tip at the center of the wafers. Bonding occurs at room temperature, with ambient air and atmospheric pressure.

An optimized CMP process has been developed to control copper dishing and oxide erosion. The key point is to obtain a perfectly flat surface to enable electrical contact on each copper pad. Copper oxidation during the surface preparation is controlled (Figures 12.3 and 12.4).

For oxide bonding using this CMP process, a bonding energy of 1.4 J m⁻² was measured after a 400 °C annealing step for 30 min, which is compatible with further post-processes such as thinning. Figure 12.5 shows that when using this process, the sealing of the different interfaces is perfect.

Since infrared radiation does not propagate through the copper materials, scanning acoustic microscopy (SAM) has to be used to characterize patterned bonding quality. SAM has the advantage of being a nondestructive technique at the wafer

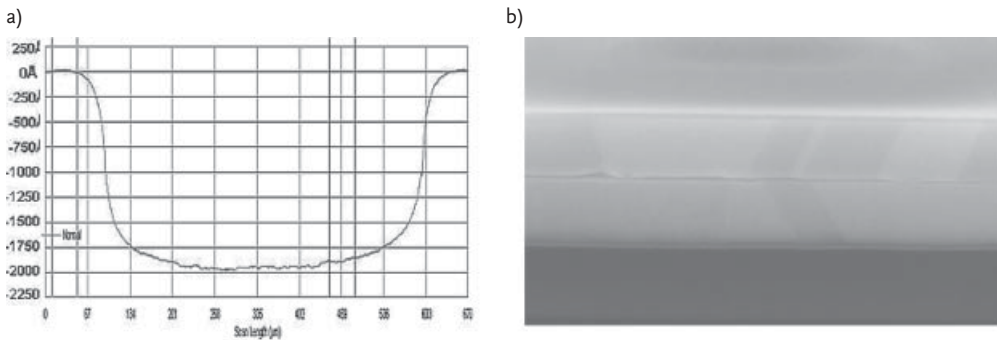


Figure 12.3 (a) Dishing characterized by a profilometer scan of a 500µm copper pad after a standard CMP process. (b) Cu/Cu SEM cross section of two 20µm copper pads bonded with dishing after a 200°C annealing step for 30 min.

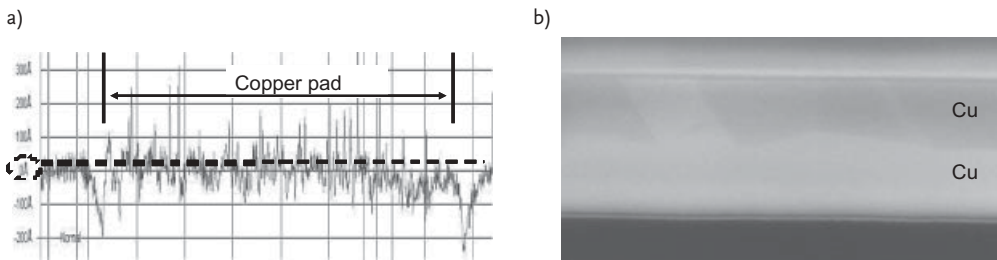


Figure 12.4 (a) Dishing characterized by a profilometer scan of a 500µm copper pad after an optimized CMP process. The maximum roughness is less than 10nm. (b) Cu/Cu SEM cross section of two 20µm wide and 0.5µm high copper pads bonded without dishing after a 200°C annealing step for 30 min.

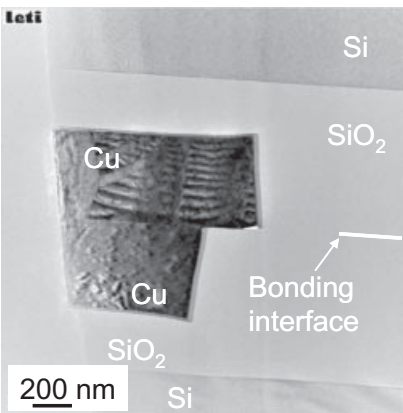


Figure 12.5 TEM image of bonded copper pad. It can be seen that the sealing of the different interfaces is perfect.

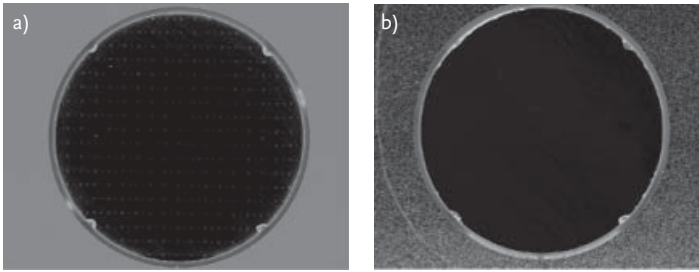


Figure 12.6 SAM images of 200mm direct Cu/SiO₂ bonded pair (a) without post-bonding anneal, and (b) after a post-bonding anneal for 2h.

Table 12.1 Bonding strength ($G = \Gamma_0 + \Gamma_p$) of a bonding pair as a function of post-bond annealing temperature. The duration for the annealing step was 2h.

Annealing temperature (°C)	Bonding strength (J m ⁻²)
200	1.14
400	6.6

scale. Without post-bond annealing, the whole wafer is bonded; no echo is detected from the bonding interface, as shown in Figure 12.6a. The four marks present at the edge of the bonding pair are induced by the bonding tool spacers. After post-bond annealing at up to 400°C for 2h, no bonding degradation is seen (Figure 12.6b). This high bonding quality is reached because of a perfect homogeneity between the center and the edge of the wafer after the CMP process.

After bonding of 5μm patterned copper pads, three kinds of contacts are obtained at the bonding interface: SiO₂/SiO₂, SiO₂/Cu (if misalignment occurs), and Cu/Cu. Since SiO₂/Cu does not allow interdiffusion, its bonding strength is lower than those of SiO₂/SiO₂ and Cu/Cu. For this reason, the SiO₂/Cu contact density at the bonding interface has to be minimized to obtain higher bonding strength.

Bonding strength can be determined using the double cantilever beam (DCB) technique [17]. This technique consists of measuring the debonding length induced by the insertion of a blade at the bonding interface. It is important to note that the interface fracture energy for ductile materials has two major contributions: the chemical work of adhesion Γ_0 and the work of plastic deformation Γ_p . When measurements are done with mode I methods, such as the DCB technique, there is a minimum plasticity contribution [18]. After a post-bond annealing step at 200°C for 2h, the bonding strength obtained is 1.14 J m⁻². When a 400°C post-bond annealing step for 2h is performed on the bonding pair, the bonding strength reaches 6.6 J m⁻² (Table 12.1). This high bonding strength (three times higher than that for blanket SiO₂/SiO₂ bonding; see Figure 12.12) is induced by direct



Figure 12.7 Bonded pair (200mm) with 200°C post-bonding anneal. The top silicon was thinned down to 5 μm with successive coarse and fine grinding.

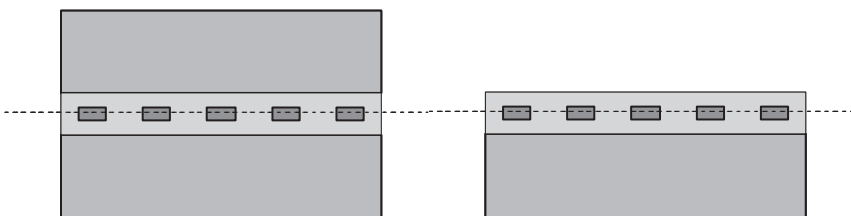


Figure 12.8 Two wafers with mixed copper oxide surfaces bonded face-to-face in an alignment tool. Then, one wafer was ground and its top silicon was removed down to the oxide layer.

copper-to-copper contact zones. Since interdiffusion and copper grain growth can happen in these zones, the bonding strength becomes very important (see Section 12.3).

With a bonding strength of 1.14 J m^{-2} (200°C post-bond anneal), the bonding pair is able to sustain post-processes such as silicon thinning. We have demonstrated the possibility of thinning the top silicon wafer down to 5 μm. The thinning process was performed by successive coarse and fine grinding. With 5 mm edge trimming after grinding, the 5 μm thin silicon substrate was free of delamination (Figure 12.7). A silicon CMP step can then be performed on the top silicon to remove post-grinding residual strain. The thinning process is very important for post-processing such as the formation of TSVs for three-dimensional technology.

Achieving Cu/SiO₂ bonding with this designed surface leads to a bond pitch of less than 10 μm. To allow optical observation of the pad bonding, after thinning down the top silicon wafer to 50 μm, the residual silicon was chemically removed with a tetramethylammonium hydroxide (TMAH) bath (Figure 12.8). Figure 12.9 presents a top view of Cu/SiO₂ bonding with a 10 μm pitch. Since misalignment is less than 1 μm, the bottom pads are barely visible.

A focused ion beam (FIB) was used for cross-sectional secondary electron microscopy (SEM) analyses. The dark area observed above the copper pad in Figure 12.10 is an electron charging effect induced by the presence of silicon oxide at the top of the copper pads. At the bonding interface, after a 300°C post-bond annealing step for 2 h, small voids are observed at the Cu/Cu bonding interface. Regarding

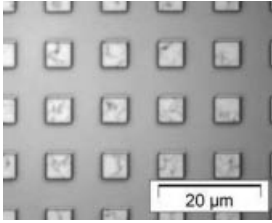


Figure 12.9 top view of a 10μm pitch direct Cu/SiO₂ bonding after total top silicon removal.

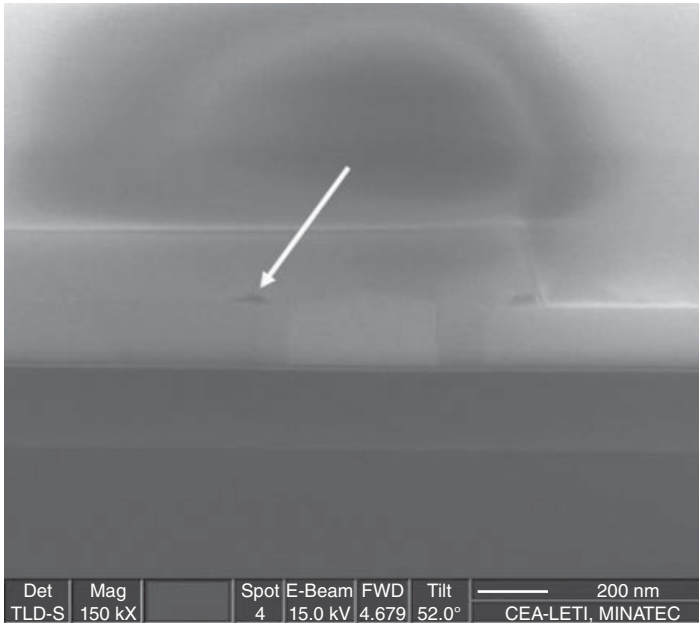


Figure 12.10 FIB-SEM cross section of direct Cu/SiO₂ bonding with 10μm pitch. The Cu/Cu interface is sealed and reveals copper grain growth from one layer to the other. Tiny voids (about 20nm in diameters) are observed at the bonding interface.

the Cu/Cu bonding interface, one can see a zigzag-shaped interface due to growth of copper grains from one layer to the other. The voids might arise from residual surface roughness prior to the bonding or vacancies in the copper layers which would migrate at the bonding interface.

12.2.2

Bonding Quality and Alignment

Bonding of patterned surfaces can be achieved at atmospheric pressure in an EVG SmartView alignment tool. The alignments marks used are standard crosses in a

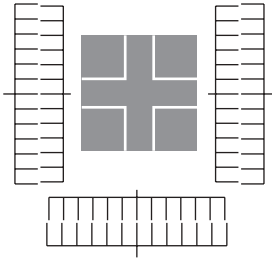


Figure 12.11 Alignment marks after bonding of patterned wafers.

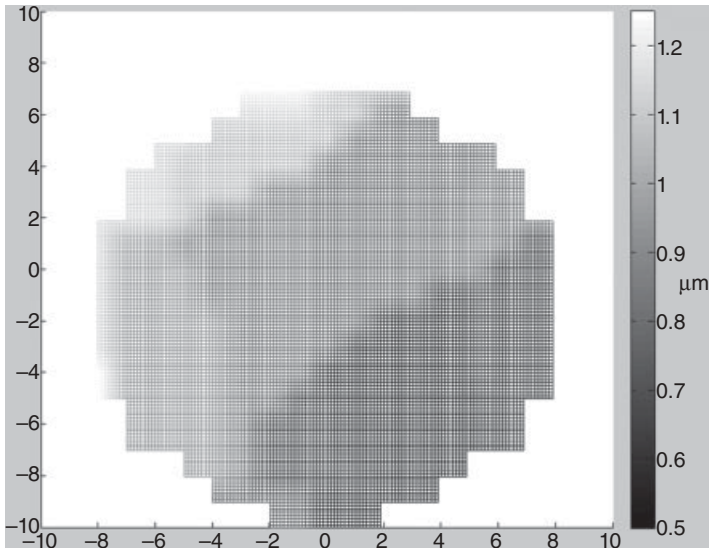


Figure 12.12 Graphical representation of a bonded pair with measured misalignment. The maximum measured misalignment is 1.2 μm all over the bonded pair.

box with verniers allowing measurement accuracy of 0.2 μm or less depending on the specific mark design. Alignment measurements are done with an infrared microscope (Figure 12.11).

Since alignment marks are present in every die of the wafer, it is possible to create a mapping of the misalignment of the bonded pair. Figure 12.12 shows a graphical representation of this misalignment for the whole of a bonded pair. The mean value and standard deviation can be determined using Eqs. (12.1) and (12.2), respectively:

$$\bar{x} = \frac{1}{n} \sum_{i=1}^n x_i \quad (12.1)$$

Table 12.2 Evolution of the mean misalignment and its standard deviation for a Cu/SiO₂ bonded pair after a grinding process. An evolution of 0.1 μm is meaningless as it is the accuracy of the measurement.

Infrared alignment measures after bonding	x (μm)	σ (μm)
Cu/SiO ₂ bonding as bonded	0.6	0.4
Cu/SiO ₂ bonding after grinding down to 50 μm	0.7	0.3
Cu/SiO ₂ bonding after grinding down to 15 μm	0.7	0.3

$$\sigma = \sqrt{\frac{1}{n-1} \sum_{i=1}^n (x_i - \bar{x})^2} \quad (12.2)$$

No misalignment above 1.2 μm was recorded and the mean value was 0.6 μm with $\sigma = 0.4$ μm. These results confirm that since the process is done at room temperature no very large misalignment is induced during the bonding.

The same measurements were done on a bonded pair after a 400°C annealing for 2 h, and also for two subsequent thinning processes to 50 and 15 μm. The measured misalignments were stable as is evident from Table 12.2.

12.3

Blanket Copper Direct Bonding Principle

Blanket copper-to-copper direct bonding can be achieved at room temperature, with ambient air and atmospheric pressure. Evolution of the bonding strength ($G = \Gamma_0 + \Gamma_p$) is characterized by two different techniques: the DCB method and four-point bending. With four-point bending, the angle of mixed modes is higher than with the DCB method. The measured bonding strength with ductile materials such as copper is then expected to be higher with four-point bending than with the DCB method due to an increase of the plastic contribution Γ_p . Figure 12.13 presents the evolution of the bonding strength as a function of 30 min post-bond annealing temperature. At room temperature and without post-bond annealing, bonding strength values of 2.5 and 6.2 J m⁻² are measured with DCB and four-point bending, respectively. With a 100°C annealing step for 30 min, the bonding strength increases and reaches 3 and 12 J m⁻² with DCB and four-point bending, respectively. These bonding strength values are high compared to those of thermal oxide. Above 200°C, for blanket copper bonding, the initiated fracture propagates directly through the silicon bulk. The copper-to-copper bonding strength becomes so high that the sample breaks, making the measurements of bonding strength impossible. As previously mentioned in this chapter the same phenomenon was observed for a patterned surface.

Transmission electron microscopy (TEM) observations of a room temperature Cu/Cu bonding interface reveals a very sharp interface as shown in Figure 12.14.

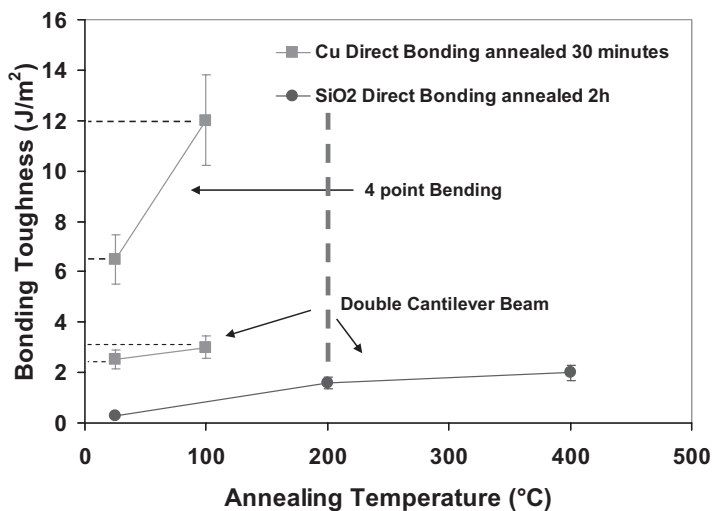


Figure 12.13 Bonding strength ($G = \Gamma_0 + \Gamma_p$) of a bonding pair as a function of the post-bond annealing temperature.

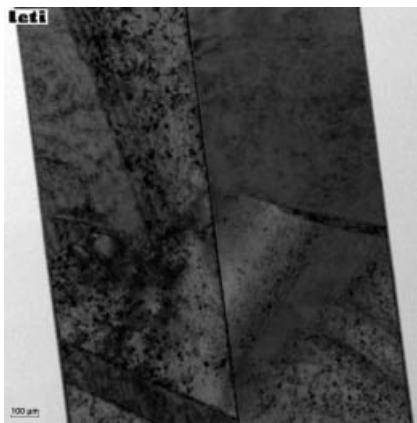


Figure 12.14 TEM cross-sectional image of direct copper bonding without post-bonding anneal. The copper layer thickness is 500 μm.

This is perfectly in accordance with the copper direct bonding process since very flat and low-roughness surfaces are mandatory.

When higher magnification TEM is used to characterize the bonding interface, one can see an interfacial layer with a width of about 4 nm (Figure 12.15). Since the bonding process is perfectly symmetric, a sharp interface is expected rather than a boundary layer. This layer is crystalline with a different orientation from the copper. Since the bonding is done without additive material, at the first stages of bonding, rough surfaces contact theory has to be considered.

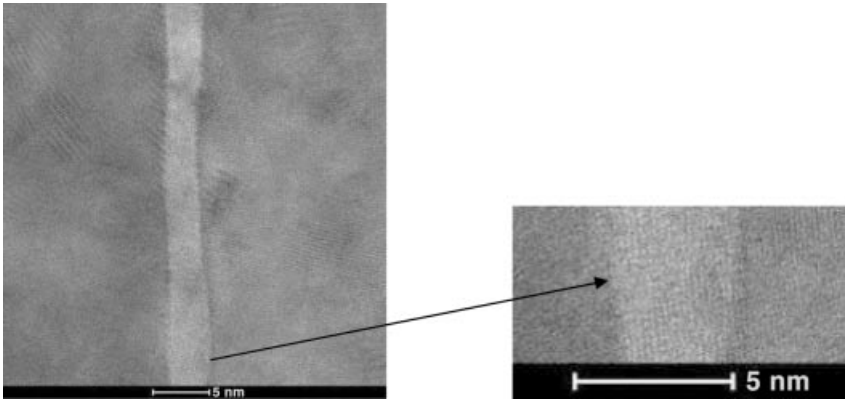


Figure 12.15 High-resolution TEM cross section of direct copper bonding without post-bonding anneal. A 4 nm thick crystalline layer is present at the bonding interface.

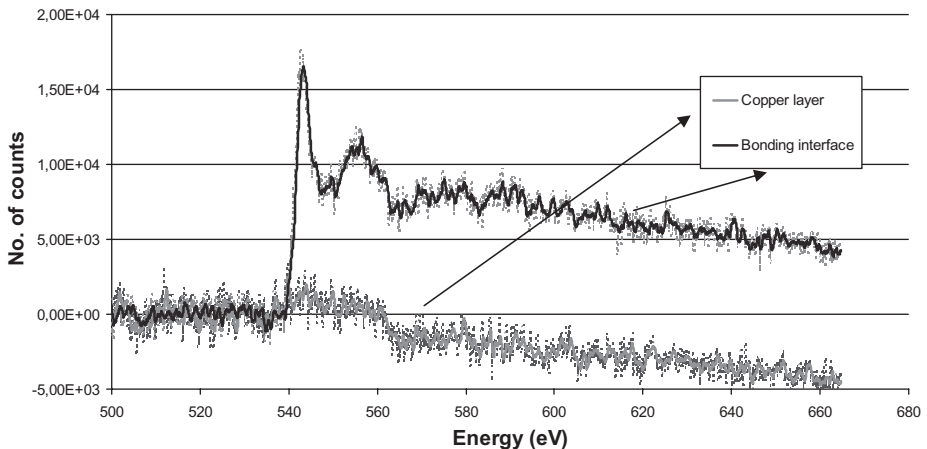


Figure 12.16 Electron energy loss spectra at a bonding interface compared to a copper layer. A peak of oxygen is detected when the analysis is carried out on the bonding interface.

Identification of elements present at the bonding interface was carried out with electron energy loss spectroscopy. Both the copper layer and the interfacial layer were analyzed with this technique. Results are presented in Figure 12.16. A peak is detected at 543 eV for the interfacial layer. This peak indicates the presence of oxygen within the interfacial layer. Since copper oxide has crystalline properties [19], this interfacial layer can be identified as a copper oxide layer.

The high bonding strength achieved at room temperature without additional annealing can be explained by the presence of a homogeneous copper oxide. When a crack is initiated, it has to propagate through a crystalline structure instead of a

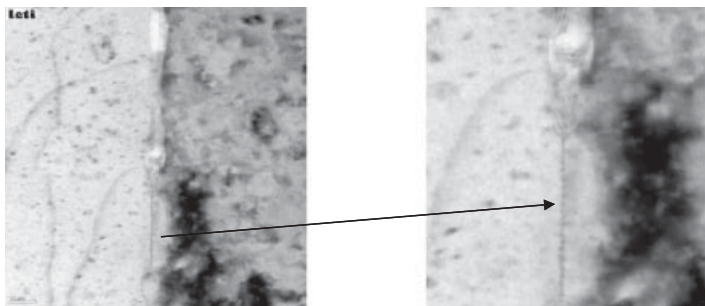


Figure 12.17 High-magnification TEM cross section of direct copper bonding after 30 min post-bond annealing at 200°C. Dislocations are observed at the bonding interface, meaning grain boundary creation and interface sealing.

single interface. This propagation path through the crystalline layer needs more energy and so the measured bonding strength is increased.

Above 200°C post-bond annealing, measurement of the bonding strength of copper direct bonding is impossible. To understand the impact of this thermal treatment on the bonding interface and interfacial layer, TEM was first used to visualize the situation. Figure 12.17 shows TEM images of the bonding interface after a 200°C annealing step. The initial crystalline interfacial layer evolves along the bonding interface and is no longer continuous. Intimate contact between the two copper layers is still possible. From the high-magnification cross-sectional TEM image, one can see dislocations at this new bonding interface. These dislocations are the signature of grain boundary creation between the two layers and the interface sealing.

In situ thermal evolution X-ray reflectivity (XRR) characterization of the bonding interface was performed at the European Synchrotron Radiation Facility with 27 keV X-rays. This technique has already been used for detailed understanding of silicon direct bonding [20]. Thermal cycles from room temperature up to 400°C were used for this experiment. XRR measurements were done every 25°C increment, once the temperature stabilized. Figure 12.18 presents the superposition of the fits of the bonding interface electron density for room temperature and 175, 200, and 225°C. At room temperature, the decreased electron density of the bonding interface is due to copper oxide, residual roughness, or buried nanovoids. Around 200°C, the electron density of the bonding interface increases. At this temperature the bonding interface is becoming closed, that is to say, some parts of the interface are creating true copper-to-copper contact and making the electron density of the bonding interface closer to that of copper.

The sealing of the bonding interface at 200°C may explain the impossibility of characterizing the bonding strength. At this temperature, the two copper layers seem to have created an intimate bond from one layer to the other. That is why during DCB or flexion tests it is easier for the initiated fracture to propagate through the silicon bulk than through a copper grain boundary.

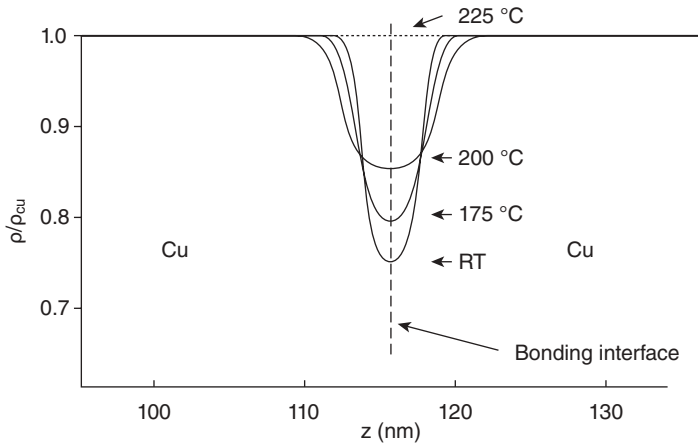


Figure 12.18 XRR fit of electron density close to a bonding interface. At 225 °C, the bonding interface is becoming sealed. (RT, room temperature.)

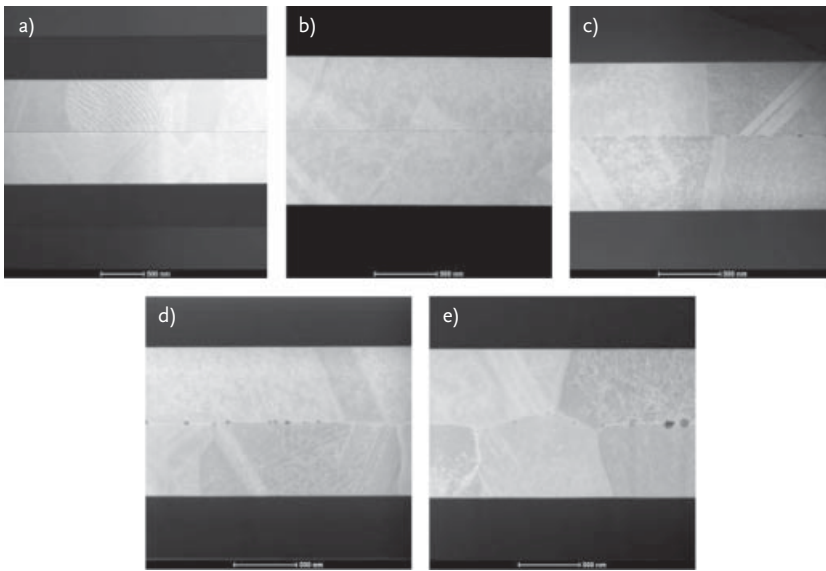


Figure 12.19 TEM cross sections of direct copper bonding with successive 30 min post-bond annealing: (a) room temperature; (b) 100 °C; (c) 200 °C; (d) 300 °C; (e) 400 °C.

Macroscopic evolution of direct copper bonding with temperature has been studied with low-magnification TEM. Figure 12.19 presents copper bonding cross sections at room temperature and after successive 100, 200, 300, and 400 °C annealing steps with an annealing time of 30 min for each step. For each temperature, a sample was taken from the same bonded pair prior to subsequent thermal

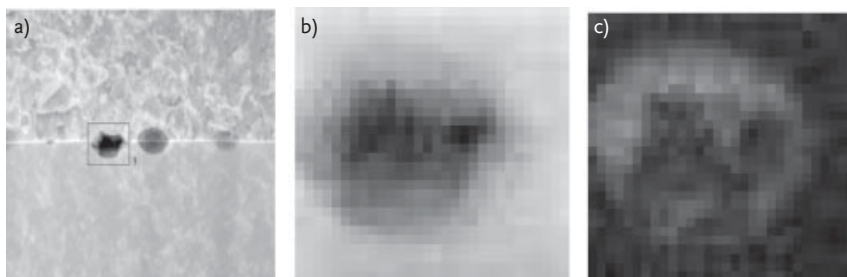


Figure 12.20 (a) Selected zone for EDX analyses. (b) Copper mapping and (c) oxygen mapping.

treatment. Imaging was performed using dark field, which makes less dense constituents appear darker. Since the density of copper oxide is less than that of copper, the interfacial layer appears darker in dark-field TEM cross sections. Even after a 100°C annealing step for 30 min, the oxide at the bonding interface starts to flow and agglomerate. After a 300°C post-bond anneal, copper grains start to grow from one layer to the other. The bonding interface assumes a zigzag shape. During the annealing steps, the copper oxide diffuses and agglomerates along the bonding interface, and then an intimate copper-to-copper bond is created to allow macroscopic copper grain growth.

With post-bond annealing, 20 nm nodules appear at the bonding interface. Characterization of these nodules was carried out with electron dispersive X-ray (EDX) analysis. EDX mapping of a selected zone (Figure 12.20a) was performed. Copper (Figure 12.20b) and oxide (Figure 12.20c) constituents were followed over all of the selected zone. The brighter a pixel, the greater the amount of element is present. For copper mapping, a hole is present at the nodule center with no copper inside it. Looking at the oxygen mapping, a crown of oxide around the nodule is apparent. Nodules seem to be voids covered with copper oxide.

However, after thermal treatments above 200°C, the bonding interface becomes a grain boundary with intimate copper-to-copper contact. This true copper-to-copper bond enables electrons to pass from one copper layer to the other and to reinforce the bonding.

These observations confirm that the sealing of the interface is driven by two physical mechanisms. The first and main one is the direct bonding adhesion of surfaces at room temperature without any pressure or compression. The second mechanism is a modified diffusion bonding.

Diffusion bonding is an extensively studied mechanism in sintering of metals [21] and consists of a plastic deformation of the asperities of both metal films. Such deformation can induce elliptical voids along the bonding interface. In diffusion bonding the strengthening of the bonding interface is obtained by diffusion at the interface, bulk diffusion, grain growth, and power-law creep and is conditioned by temperature, pressure, and initial surface conditions [22].

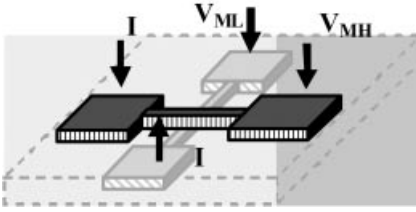


Figure 12.21 Schematic of a Kelvin cross structure.

In our case, we have a modified diffusion bonding since no pressure is applied during bonding and annealing, and the process is driven mainly by temperature, metal oxide thermodynamic instability, and the very small initial roughness.

For patterned surfaces, the oxide zones are bonded at room temperature and the copper might be slightly dished and still unbonded. The mechanism discussed above is, however, still possible. The thermal expansion of the copper pads in the vertical direction (horizontal expansion is impeded by the silicon wafer), greater than that of the oxide, allows the aligned copper pad surfaces to come into contact and bond because of the diffusion bonding.

12.4

Electrical Characterization

Determination of contact resistance is commonly carried out with Kelvin structures. Figure 12.21 shows a schematic representation of such a Kelvin cross where two of the tips force the current to pass through the bonding contact and the other two are used to measure the voltage from both parts of the contact. This technique is widely used because it is a free access resistance method. One branch of the Kelvin cross is designed on the top wafer, while the second is on the bottom wafer. With this configuration, the misalignment will not affect the measured resistance.

To a first approximation, the contact resistance R_C can be directly determined using the relation

$$R_C = \frac{V_{MH} - V_{ML}}{I} \quad (12.3)$$

where V_{MH} and V_{ML} are the electrical potential of the top and bottom layer, respectively. One can then determine the specific contact resistivity:

$$\rho_C = R_C \times A_C \quad (12.4)$$

where ρ_C is the specific contact resistivity and A_C the contact area.

In order to obtain contact resistance at a Cu/Cu direct bonding interface, 200mm silicon wafers were used with 800nm silicon oxide deposited. Kelvin branches (500nm) were dry etched over the wafer and 20nm Ti/TiN (chemical

Table 12.3 Repartition of different contacts at the bonding interface for patterned Kelvin structures.

Contact type	% of the bonding interface
SiO ₂ /SiO ₂	60
Cu/SiO ₂	39.9
Cu/Cu	0.14

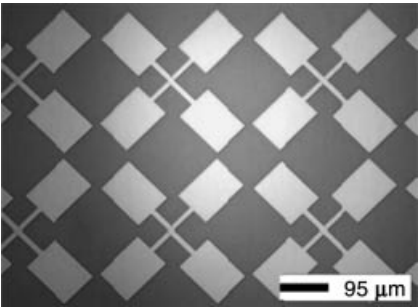


Figure 12.22 Optical microscopy top view of a bonded pair after top wafer substrate removal.

vapor deposition) followed by 1 μm copper (physical vapor + electrochemical deposition) were deposited. Surface preparation was performed by CMP-based activation as described in Section 12.2. Kelvin branches have been designed to obtain a copper surface density of 20%. After bonding, three kinds of contacts are obtained at the bonding interface (Table 12.3).

After room temperature bonding and post-bond annealing, grinding plus TMAH were used to entirely etch the top silicon substrate, as previously explained. A dry silicon oxide etching step is finally used to expose the direct contacts between measurement probes and 75 × 95 μm² copper pads (Figure 12.22).

Measured resistances after 2 h thermal treatment at 200 and 400 °C are presented in Figures 12.23 and 12.24, respectively. Since the Kelvin structure appears over all of the wafer, multiple measurements were possible.

Voltage–current, $V(I)$, curves were obtained with a HP4155 analyzer. The current was varied from –100 up to +100 mA with a step of 1 mA. More than 20 Kelvin structures were characterized over the whole of the wafer.

For all measurements, the obtained curve revealed an ohmic behavior since the voltage is proportional to the current and the curve passes through the origin of the axes. No hysteresis issues were recorded for these electrical measurements. Forward current was exactly the same as reverse current. The resistance R_C was determined by a linear fit of the $V(I)$ curve. For all measurements, the obtained

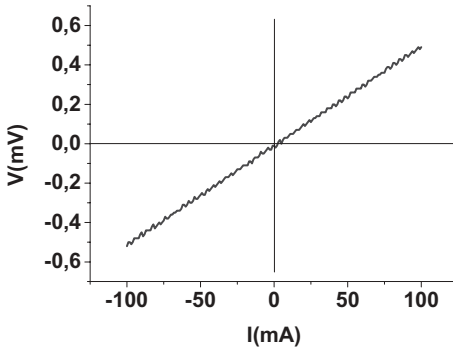


Figure 12.23 Single $V(I)$ curve of wafer-to-wafer $10 \times 10 \mu\text{m}^2$ Cu/Cu contact after post-bonding anneal at 200°C for 2 h. R_c and ρ_c are equal to $5 \text{ m}\Omega$ and $0.5 \Omega \mu\text{m}^2$, respectively.

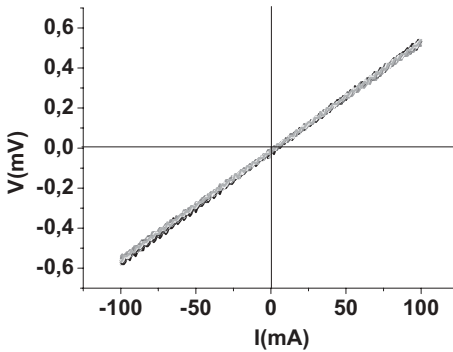


Figure 12.24 Twenty $V(I)$ curves of wafer-to-wafer $10 \times 10 \mu\text{m}^2$ Cu/Cu contact after post-bonding anneal at 400°C for 2 h. R_c and ρ_c are equal to $5 \text{ m}\Omega$ and $0.5 \Omega \mu\text{m}^2$, respectively.

contact resistance was $5 \text{ m}\Omega$ with $\sigma = 0.1 \text{ m}\Omega$. Good electrical property homogeneity was achieved over the whole of the bonded pair with direct Cu/SiO₂ bonding after post-bond annealing.

When the same experiment is carried out on Kelvin structures with different contact areas, after an annealing step at 400°C for 2 h, the measured resistance is always in the region of $5 \text{ m}\Omega$. Table 12.4 summarizes the resistance for contact areas from 3×3 up to $25 \times 25 \mu\text{m}^2$.

Since the contact resistance has to be inversely proportional to the bonding area, second-order effects affect the contact resistance determined using Eq. (12.3). Indeed, with such low resistances, Eq. (12.3) is not accurate enough to describe the electrical behavior of the bonding interface. Furthermore, with the Kelvin crosses used for this study, current is forced to pass across a 90° angle. Figure 12.25 shows a simulation of equipotentials all along the current path. A drop of

Table 12.4 Evolution of measured contact resistance and contact resistivity as a function of contact area.

Contact area (μm ²)	Mean R _C (mΩ)	Mean ρ _c (Ωμm ²)
3 × 3	5.28	0.047
5 × 5	5.18	0.129
7 × 7	5.20	0.255
10 × 10	5.05	0.505
25 × 25	5.40	3.375

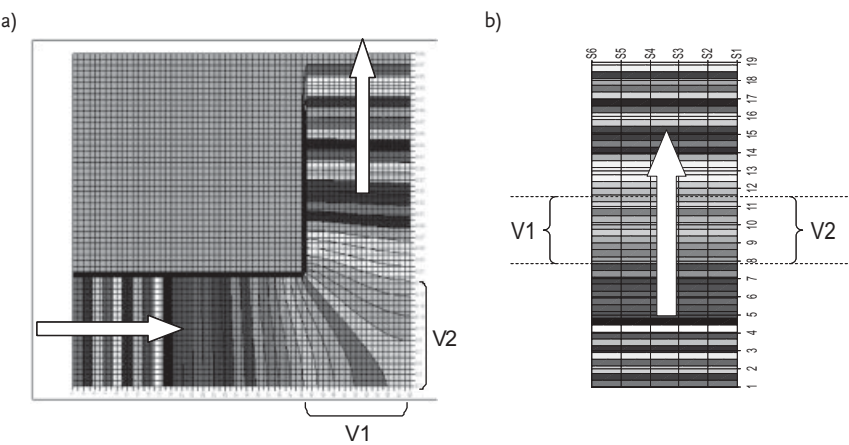


Figure 12.25 Comparison of equipotential simulation all along (a) angular and (b) straight current path during Kelvin measurement. A drop of 2% of the total voltage occurs between each different scale of gray.

2% of the total voltage occurs between each different gray color. For an angular current path, a parasitic voltage drop affects the measured resistance around the contact area.

When the contact resistance becomes negligible compared to the parasitic resistance $(V_1 - V_2)/I$, the measured resistance remains constant. The measured resistance R_M can then be expressed by

$$R_M = R_C + \frac{V_1 - V_2}{I} \tag{12.5}$$

Taking into account this parasitic effect, specific contact resistance cannot be directly determined using Eq. (12.3). When contact resistances are in the region of a few milliohms, Kelvin structures with angular current flow are not accurate enough to obtain a good characterization of the electrical properties of the bonding interface.

12.5

Die-to-Wafer Bonding

The process used for wafer-to-wafer bonding can be adapted to die-to-wafer bonding. After a surface-activation process, dies can be directly bonded onto a host substrate with an SET FC 150 alignment tool. SAM characterization of the bonding interface after a 400°C post-bonding anneal for 2 h reveals only few unbounded zones (Figure 12.26). Defects at the die corner are due to handling issues. A misalignment was found of 0.5 μm after infrared characterization.

Using the same protocol with die-to-wafer bonding, the top silicon die substrate was removed by successive grinding, TMAH treatment, and silicon oxide dry etching. Electrical characterization was performed on a 400°C/2 h annealed Kelvin cross. The very first $I(V)$ curve shows perfect ohmic behavior (Figure 12.27).

The measured resistance was 12 m Ω for a $10 \times 10 \mu\text{m}^2$ contact area. The increase of contact resistance compared to wafer-to-wafer bonding can be explained by the additional steps required for dies or a slight copper oxidation. Ways to improve this electrical behavior are under investigation. However, the Cu/Cu contact resistance obtained remains negligible compare to that of TSV resistance used for three-dimensional IC schemes.



Figure 12.26 SAM image of Cu/SiO₂ die-to-wafer bonding after a 400°C post-bonding anneal for 2 h.

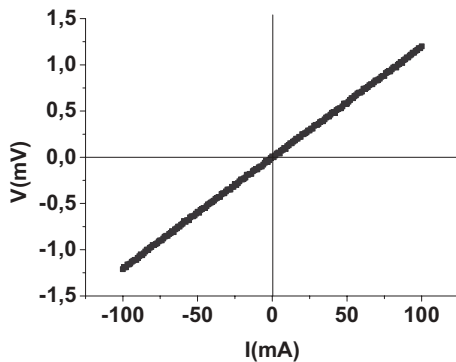


Figure 12.27 $V(I)$ curve of die-to-wafer $10 \times 10 \mu\text{m}^2$ Cu/Cu contact after a post-bonding anneal at 400°C for 2 h. R_c and ρ_c were determined as 12 m Ω and 1.2 $\Omega \mu\text{m}^2$, respectively.

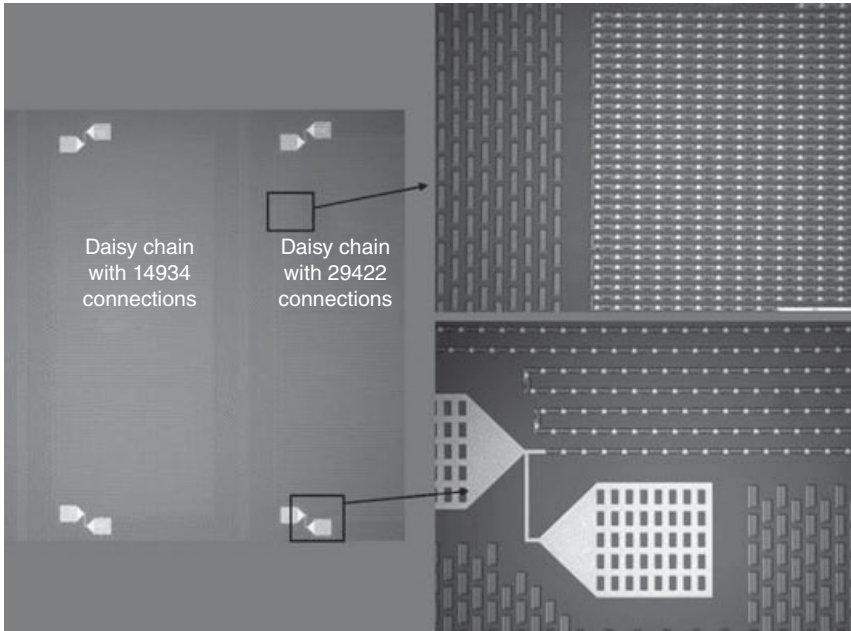


Figure 12.28 Optical observation of daisy chains after the complete removal of top silicon.

12.5.1

Daisy Chain Structures [23]

Daisy chains with up to 29 422 connections have been designed to limit the angular current flow parasitical resistance effect and to demonstrate the reliability copper direct bonding electrical contact. Copper lines were 3 μm wide, 500 nm thick, and 10 μm long. The pitch was 14 μm and contact area was 3 $\times$ 3 μm^2 (Figure 12.28). After annealing the bonded pair at 400 $^{\circ}\text{C}$ for 2 h, the $V(I)$ curve obtained was perfectly ohmic across the 29 422 connections. The total resistance was measured at about 2.34 k Ω . That is to say, the resistance for each “Cu contact + line” element was 79.5 m Ω .

A schematic cross section of the daisy chain is presented in Figure 12.29. A copper film resistivity ρ of $2.1 \times 10^{-2} \Omega\mu\text{m}$ was measured on specific electrical characterization of the structure. The experimentally measured resistance of 79.5 m Ω for “Cu contact + line” can be separated into three different structures (Figure 12.29). Theoretical values for R_1 and R_3 can be obtained using

$$R = \frac{\rho L}{S} \quad (12.6)$$

Using $\rho = 2.1 \times 10^{-2} \Omega\mu\text{m}$, $L = 2 \mu\text{m}$, and $S = 0.5 \times 3 \mu\text{m}^2$, one can obtain a value for R_1 and R_3 of about 28 m Ω . If R_2 were induced only by copper material, the ideal

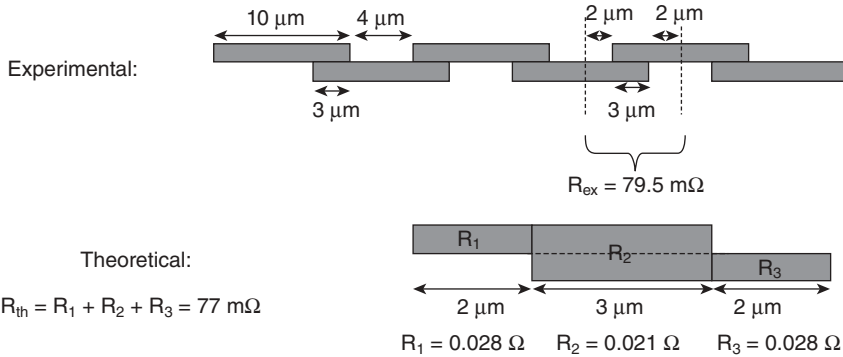


Figure 12.29 Experimental and theoretical measurements for the resistance per node on daisy chain with $3 \times 3 \mu\text{m}^2$ contact area.

resistance would be $R_{2th} = 21 \text{ m}\Omega$. Since the resistance obtained for “Cu contact + line” is $79.5 \text{ m}\Omega$, the resistance $R_{2real} = R - R_1 - R_3 = 23 \text{ m}\Omega$. That is to say, for a daisy chain with 29422 connections, after a 400°C annealing step, the impact of the copper-to-copper bonding interface for $3 \times 3 \mu\text{m}^2$ contact areas is $R_{2real} - R_{2th} = 2.5 \text{ m}\Omega$.

This difference is induced by copper line resistance variations (affecting R_1 , R_2 , and R_3), misalignment error during bonding (affecting mainly the contact area and so R_2), and the real bonding interface resistance R_C . To a first approximation we assume that this difference is the maximum value of R_C , though one can estimate the specific contact resistance ρ_C using Eq. (12.4). The specific contact resistance ρ_C is then about $22.5 \text{ m}\Omega\mu\text{m}^2$.

12.6

Conclusion

Cu/SiO₂ bonding has been demonstrated for wafer-to-wafer bonding as well as die-to-wafer bonding. In both cases, high bonding quality and alignment are evident from SAM and infrared analyses. A very low contact resistance is achieved with multiple contact areas, and the contact resistivity is reduced down to $\rho_C = 47 \text{ m}\Omega\mu\text{m}^2$ for Kelvin structures and down to $\rho_C = 22.5 \text{ m}\Omega\mu\text{m}^2$ for daisy chains with 29422 connections. With post-bond annealing, the bonding interface acts as a copper grain boundary.

Acknowledgment

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13

Metal/Silicon Oxide Hybrid Bonding

Paul Enquist

13.1

Introduction

This chapter describes a metal/silicon oxide hybrid bonding technology that is an ideal solution for the fabrication of three-dimensional (3D) integrated circuits (ICs). This bonding technology is part of a broader class of hybrid bonding technologies that are distinct from conventional bonding technologies in that a heterogeneous bond comprising more than one type of bond component is utilized as opposed to a homogeneous bond that comprises a single type of bond component. The heterogeneous nature of the hybrid bond generally offers advantages over a homogeneous bond. For example, a homogeneous flip-chip bond utilizing solder bumps can result in yield and reliability limitations due to the lack of bonding between the reflowed bumps. Adding a heterogeneous underfill bond component between the reflowed bumps significantly improves the reliability of the solder interconnects at the expense of increased stress in the silicon die [1].

While the flip-chip/underfill hybrid bond is an excellent solution for most 3D packaging applications, the inherent nonplanarity of this bond limits the interconnect pitch and makes it unsuitable for 3D integration applications that require a bond with a micrometer scalable interconnect. Two alternative planar hybrid technologies have been proposed and developed to meet the needs of these 3D IC applications. One of these is a metal/adhesive hybrid technology using copper/benzocyclobutene (BCB) that is the subject of Chapter 11 [2]. The other is a metal/non-adhesive hybrid technology that includes a variety of metal/silicon oxide combinations that is the primary subject of this chapter. The relationship between these hybrid bonding technologies is summarized in Figure 13.1.

13.2

Metal/Non-adhesive Hybrid Bonding—Metal DBI®

The metal/non-adhesive hybrid bonding technology is a class of direct bonding that has been developed at Ziptronix, Inc. and trademarked as Direct

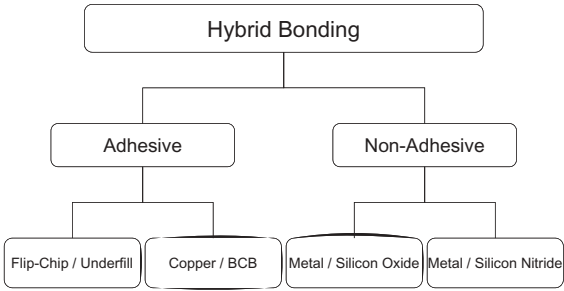


Figure 13.1 Various hybrid bonding technologies.

Bond Interconnect (DBI®) (e.g., [3–7]). DBI® is covered by a number of issued patents and patent applications (e.g., [8, 9]).

A key advantage of the metal/non-adhesive or metal/direct hybrid bonding technology compared to adhesive-based hybrid bond technologies is the breadth of post-bond fabrication processes possible. Adhesive-based hybrid bond technologies have a bond temperature characteristic of the adhesive and are typically limited after bonding to the glass transition temperature which can be close to the bond temperature. In contrast, the non-adhesive or direct hybrid bond technology is capable of achieving high bond energy at low temperatures and is capable of withstanding temperatures after bonding well in excess of that which would damage the materials that are hybrid bonded, for example ICs.

Another advantage of non-adhesive or direct hybrid bonding technology is compatibility with established CMOS wafer foundry volume manufacturing materials and processes. The materials and processes used to implement this hybrid bonding technology can leverage those currently used in volume CMOS wafer manufacture, lowering the barrier for adoption and facilitating process integration of hybrid bonding with CMOS back-end-of-line (BEOL) for lowest cost-of-ownership (CoO) 3D IC manufacture.

13.3 Metal/Silicon Oxide DBI®

The majority of direct hybrid bonding development has focused on the use of metal/silicon oxide hybrid bonding. Many different configurations have been evaluated including various combinations of hybrid bond surface fabrication processes, surface topographies, types of metal, hybrid bond alignment, and hybrid surface contact techniques. These configurations are discussed below in detail.

13.3.1

Metal/Silicon Oxide DBI® Surface Fabrication

The hybrid metal/silicon oxide bonding surface can be fabricated with a number of different process flows. The ability to implement this direct hybrid bonding with a variety of process flows facilitates adoption of the technology in a range of different environments and an assortment of different metals. Damascene, planarized stud, and nonplanar process flows suitable for aluminum, copper, gold, and nickel metals are described below.

13.3.1.1 Damascene Metal/Silicon Oxide DBI® Process Flow

The damascene hybrid bonding process flow is similar to that used in volume CMOS copper BEOL wafer fabrication. A single or dual damascene can be implemented depending on the desired surface patterning as described below. This process flow typically includes deposition of a silicon oxide layer, followed by via etch (single damascene) or via and trench etch (dual damascene) through the silicon oxide layer to a last metal layer. The desired hybrid bond metal can then be deposited in via or via and trench, for example by physical vapor deposition or electroplating. This metal deposition may be preceded by a conductive barrier liner deposition to impede diffusion of the metal into the surrounding silicon oxide and improve reliability. The deposited metal is then polished with chemomechanical polishing (CMP) to the desired surface planarity as discussed below. This process can scale to a submicrometer pitch as demonstrated by interlevel vias in CMOS copper BEOL. This process flow has been proven with both aluminum and copper hybrid bond metals as described in more detail below.

13.3.1.2 Planarized Stud Metal/Silicon Oxide DBI® Process Flow

The planarized stud hybrid bonding process flow differs from the damascene hybrid bonding process flow in that the hybrid bond metal is formed prior to instead of after the hybrid bond silicon oxide. The hybrid bond metal is first deposited on a last metal or via layer, for example using electroplating on a seed layer with a photoresist mask on a tungsten plug CMP surface on a CMOS aluminum BEOL wafer. The seed layer is then etched using the hybrid bond metal or photoresist as a mask, followed by silicon oxide deposition and CMP to the desired surface planarity as discussed below. This process can also scale to a submicrometer pitch. This process flow has been proven using nickel hybrid bond metal as described in more detail below.

13.3.1.3 Nonplanar Metal/Silicon Oxide DBI® Process Flow

The nonplanar hybrid bonding process flow is suitable for hybrid bond metals that are not well suited for CMP in either the damascene or planarized stud process. This process flow can begin with either the damascene or planarized stud process flow wherein the hybrid bond metal is replaced with a metal that is suitable for CMP. The hybrid bond metal can then be selectively deposited or deposited and

patterned on the planar damascene or planarized stud hybrid surface with electrical contact to the CMP-suitable metal. The thickness of the metal is typically kept within 100 nm to minimize the nonplanarity of the hybrid surface and allow high bond energy as described below. This process flow has been proven using gold hybrid bond metal as described in more detail below.

13.3.2

Metal/Silicon Oxide DBI® Surface Patterning

The hybrid bond surface is patterned to define regions of metal and silicon oxide according to the process flow used to define the surface. These regions are designed to mate with another hybrid bond surface after these surfaces are aligned and brought into contact. The surface can be predominantly metal, silicon oxide, or comparable amounts of metal and silicon oxide portions. The geometries defining the metal or silicon oxide portions can be similar to those used in CMOS BEOL wafer fabrication, for example (sub)micrometer-scale inter-level vias or intralevel routing features. Pairs of surfaces consisting of vias and/or routing features with one being a mirror image of the other may be patterned for subsequent flipping of one surface, alignment, and contact to the other surface as described below. Surfaces that are not mirror image pairs may also be patterned for subsequent contact, for example bonding via to routing or crossover routing features.

13.3.3

Metal/Silicon Oxide DBI® Surface Topography

There are basically three DBI® surface topography configurations that can result from the DBI® surface fabrication process flows described above. These are DBI® metal planar with the adjacent silicon oxide, or above or below the adjacent silicon oxide. A planar metal/silicon oxide DBI® surface topography is one where the metal and silicon oxide relative heights are within 1 nm of each other. The metal and silicon oxide relative heights of the nonplanar metal/silicon DBI® surface topographies are typically within about 10 nm. It is also possible to accommodate a larger variation of greater than 100 nm, for example if a larger interconnection pitch is acceptable [3].

13.3.4

Metal/Silicon Oxide DBI® Surface Roughness

The silicon oxide component of the DBI® surface is typically less than 0.5 nm root mean square (RMS) to facilitate high direct bond energy between silicon oxide components of the hybrid bond. A similar low RMS for the metal component is conducive for a direct metal bond and further increase in bond energy. However, high hybrid bond energies and reliable 3D interconnections can be achieved with higher metal component RMS less than about 10 nm as described below. These

roughness values can be readily achieved with commercial CMP tools using the appropriate combination of pads and slurries for the type of metal and silicon oxide, surface patterning, and desired surface topography.

13.3.5

Metal/Silicon Oxide DBI® Surface Activation and Termination

After the appropriate metal/silicon oxide DBI® surface topography and roughness have been met, the surface can be activated and terminated to enable high bond energy at low temperature after alignment and placement of two DBI® surfaces into contact in an ambient manufacturing environment. Effective activation can be achieved with a slight etch that removes contaminants, breaks surface atomic bonds, and maintains or does not significantly increase surface roughness. Terminating this surface allows the surface to be handled in an ambient manufacturing environment before it is aligned and placed into contact with another DBI® surface to form a DBI® bonded pair. The termination may also facilitate a chemical reaction between surfaces placed together that enables high bond energy at low temperature, for example below 200°C. Different types of terminations, for example based on nitrogen and hydroxyl, are possible. Higher bond energies may be obtained if both surfaces are activated and terminated prior to contact. High bond energies may also be obtained if only the silicon oxide is activated and terminated, although both metal and silicon oxide components of the hybrid surface may be exposed to the activation and termination process. The activation and termination can be accomplished with a number of different methods. For example, a plasma process can be used to both activate and terminate or a wet process can be used after a plasma activation process to terminate. These processes can be implemented with a discrete tool set or a cluster tool that includes aligning and placing DBI® bond surfaces together (www.suss.com; www.evgroup.com). The capability of high bond energy at low temperature of the technology enables a low CoO manufacturing solution by eliminating the need for a bond chamber that increases tool cost and lowers tool throughput. Surface activation and termination methods, devices that can be made with these methods, and tools that can be used to implement these methods are described more fully in a number of issued patents and patent applications (e.g., [10–16]).

13.3.6

Metal/Silicon Oxide DBI® Alignment and Hybrid Surface Contact

A number of options are available for the alignment and placement of two DBI® surfaces into contact. The preferred implementation can depend on a variety of requirements including alignment accuracy, surface form factor, and throughput. For example, a pick-and-place tool (www.set-sas.fr) may be preferred for a die-to-wafer application with a less than 10 mm² die size requiring more than 100 placements per wafer and 10 μm alignment accuracy. Alternatively, a high-accuracy wafer alignment and placement tool (www.suss.com; www.evgroup.com) may be

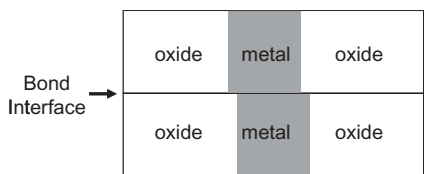


Figure 13.2 Generic metal/silicon oxide DBI[®] hybrid bond cross section showing silicon oxide-to-silicon oxide, metal-to-metal, and silicon oxide-to-metal bond components. The silicon oxide-to-metal bond component(s) may result from misalignment of mirror image patterned wafers.

required for a 200 or 300 mm wafer-to-wafer application requiring submicrometer alignment accuracy.

Different types of bonds are formed when two metal/silicon oxide hybrid surfaces are bonded. Various aspects of how these bonds are formed depend on the properties of the silicon oxide and metal and surface topography. Details of these bonds and how they are formed in the context of bonding hybrid patterned wafers with the metal surface level with, above, or below the silicon oxide surface are described below.

13.3.6.1 DBI[®] Bond Components

There are generally three types of bonds when two hybrid metal/silicon oxide surfaces have been aligned and placed together. These are silicon oxide-to-silicon oxide, metal-to-metal, and silicon oxide-to-metal bonds, as shown in Figure 13.2. These bonds are typically direct bonds without any intervening adhesive material and the metal-to-metal or silicon oxide-to-metal direct bond may be to a native oxide on the metal. The metal-to-metal direct bond can make an electrical interconnection as a result of direct contact or after a temperature cycle as described below. If desired, fusing, melting, or reflow of the metallic bond may also occur after a temperature cycle depending on the metal and temperature cycle used. Some of these features are reviewed below in the context of bonding mirror image patterned wafers with the metal surface height equal to, above, or below the silicon oxide height. The silicon oxide-to-metal bond component may be intentional, for example when bonding a via pattern to a routing pattern or bonding dissimilar routing patterns, or unintentional, for example from misalignment when bonding mirror image via or routing patterns to each other.

The bonding of these various metal/silicon oxide hybrid surfaces results in a wide variety of relative areas of these three different types of bonds. This range is generally limited by the design rules associated with the patterning and alignment accuracy of the surface contact tool and not the DBI[®] technology, assuming the appropriate combination of surface roughness, termination, topography, metal, and silicon oxide is used. For example, when bonding a closest pack density of mirror image vias to form a high-density 3D interconnect, the silicon oxide-to-silicon oxide and metal-to-metal bond can be about 80 and 20%, respectively, of

the hybrid surface if the alignment accuracy is good enough for the misaligned metal-to-silicon oxide area to be negligible. Conversely, the metal-to-metal bond component can be larger than either of the silicon oxide-to-silicon oxide or metal-to-silicon oxide components if a network of power or ground planes are bonded together. The metal-to-silicon oxide component can also be larger than either of the silicon oxide-to-silicon oxide or metal-to-metal components if the misalignment is large or different routing layers are bonded together. The capability of the DBI® technology to accommodate these different types of bonds as part of the hybrid bond enables high bond energy regardless of the hybrid patterning or misalignment and facilitates submicrometer scaling of a 3D interconnect pitch.

13.3.6.2 Metal Surface Planar with Silicon Oxide Surface

Planarity of the metal and silicon oxide components on the hybrid surfaces allows these components to come in direct contact with each other to form direct silicon oxide-to-silicon oxide, metal-to-metal, or silicon oxide-to-metal bonds according to the respective patterns on these surfaces. This allows for a contiguous bond across the entire hybrid bond interface that affords high bond energy and isolated electrical interconnections. Both high bond energy and isolated electrical interconnections can be achieved by simply placing together suitably prepared surfaces with the requisite alignment in an ambient manufacturing environment, for example if the silicon oxide surface is appropriately activated and terminated and the metal does not have a native oxide of an extent that could preclude electrical interconnections. Planarity between the metal and silicon oxide components further enables these electrical interconnections with an interconnection pitch to be realized that is limited only by the patterning of these components and the accuracy with which the hybrid surfaces can be aligned and placed.

It is also possible that electrical interconnections are not formed upon initial placement of the hybrid surfaces together. This can happen, for example, if there is a native oxide of an extent on the metal surface that inhibits the electrical interconnection. The extent of this native oxide can depend on a number of factors including the type of metal and surface preparation or cleaning prior to bonding. Electrical interconnections may then be formed after placement, for example with a temperature cycle that creates pressure at the metal-to-metal bond from high silicon oxide-to-silicon oxide bond strength and a higher coefficient of thermal expansion (CTE) of the metal than the silicon oxide. The temperature cycle resulting in electrical interconnections depends on a number of factors including the type of metal, extent of native oxide, and silicon oxide-to-silicon oxide temperature-dependent bond strength.

13.3.6.3 Metal Surface Above Silicon Oxide Surface

High bond energy and isolated electrical interconnections can also be achieved with hybrid surfaces where the metal component is above the silicon oxide surface. The bond energy of this configuration after placing hybrid surfaces together is not limited to the metal-to-metal bonding if the material on which the hybrid patterns

are built (e.g., CMOS wafers) has sufficiently low Young's modulus to allow the silicon oxide-to-silicon oxide or metal-to-silicon oxide components to come into contact. The Young's modulus required depends on a number of factors including the hybrid surface patterning, interconnection pitch, silicon oxide-to-silicon oxide and metal-to-silicon oxide bond energy, and extent of the metal above the silicon oxide surface. For example, 20 nm of extent may allow a 20 μm pitch, while 100 nm of extent may only allow a 1 mm pitch when DBI® bonding gold/silicon oxide hybrid surfaces [3]. A native oxide on the metal may be present to an extent to further limit the interconnection pitch or metal extent above the silicon oxide by requiring additional silicon oxide-to-silicon oxide or metal-to-silicon oxide bond area to provide adequate bond energy to compress the metal-to-metal during a post-contact heat treatment.

13.3.6.4 Metal Surface Below Silicon Oxide Surface

High bond energy and isolated electrical interconnections can also be achieved with hybrid surfaces where the metal component is below the silicon oxide surface. Electrical connections with this configuration are not made after hybrid surface contact unless the Young's modulus of the material on which the hybrid patterns are built is sufficiently low to allow the metal-to-metal components to come into contact. Electrical interconnections with this configuration can also be made with a post-contact temperature cycle. A larger temperature excursion than that of the other configurations may be required to close the gap formed by thermal expansion between two metal surfaces recessed below silicon oxide surfaces. Alternatively, this gap may be closed by reflow, for example if a suitable solder-based or alloyed metal is used.

This configuration may provide some advantages in volume manufacturability. For example, the surface topography of some combinations of metal/silicon oxide may be easier to control within a specification if a metal recess is allowed to be within a certain range as opposed to a more precise restriction of less than 1 nm recess. This control can be achieved with a small recess less than about 5–10 nm whose gap can be closed with a minor temperature cycle after surface contact. For example, a 1 μm tall copper metal with a recess or CMP dishing maintained within 2 nm below a silicon oxide surface can be expected to have the resulting metal-to-metal gap within 4 nm after silicon oxide-to-silicon oxide contact at ambient to be closed at about 100 °C above ambient. The use of nickel instead of copper is expected to require about 150 °C to close this gap due to the smaller CTE of nickel compared to copper.

13.3.7

Metal Parameters Relevant to DBI® Surface Fabrication and Electrical Interconnection

Metal/silicon oxide hybrid bonding is generically applicable to a wide variety of types of metals. The implementation details for a particular type of metal are typically different for a different type of metal. However, the four properties of metals

summarized below provide some basic guidelines on how to prepare a hybrid surface for bonding and how to achieve isolated electrical interconnections with a scalable pitch within a low thermal budget after bonding.

13.3.7.1 Polishing Rate

The polishing rate of a metal is the rate at which metal is removed from a metal/silicon oxide hybrid surface. It is dependent on a number of factors including the metal hardness, malleability, ductility, surface patterning, and polishing conditions including pad, slurry, downforce, and rotation. A metal polishing rate similar to, lower than, or higher than the silicon oxide polishing rate will tend to yield a DBI® bond surface with metal that is planar, higher than, or lower than, respectively, the silicon oxide. Appropriate selection of polishing conditions will generally result in an appropriate surface topography for DBI® bonding.

13.3.7.2 Native Oxide Stability

Metals that have a stable oxide, like nickel and aluminum, are more likely to have this oxide inhibit electrical interconnections upon initial metal-to-metal contact. An electrically conducting bond may be achieved by removing this oxide prior to bonding or reduction of the oxide interfacial layer after metal-to-metal contact. Removal of the oxide prior to bonding may allow electrical interconnection upon direct metal contact, but may also require handling, alignment, and placement in a non-oxidizing environment to prevent re-oxidation of the metal surface. Reduction of the oxide interfacial layer after metal-to-metal contact eliminates this environmental restriction and can be accomplished with a post-contact process step, for example a temperature cycle that sufficiently compresses the metal-to-metal bond with a combination of high silicon oxide-to-silicon oxide bond energy and metal-to-silicon oxide CTE mismatch. Note that this process step has a very low CoO because the compression is provided intrinsically by the silicon oxide direct bond eliminating the need for external compression tooling and enabling a batch process. It is also possible for this process step to be eliminated completely if this temperature cycle can be provided by a downstream process step.

13.3.7.3 Coefficient of Thermal Expansion

The CTE of a metal can vary by a factor of about two depending on the type of metal. This is about 25–50 times or 12–25 ppm °C⁻¹ greater than that of the silicon oxide. This significant difference in CTE results in considerable compressive stress at the metal-to-metal interface and tensile stress at the silicon oxide-to-silicon oxide interface at low temperatures above the hybrid surface fabrication and bonding ambient. This compressive stress can exceed the yield strength of the metal and facilitate formation of a metal-to-metal direct metallic bond with reliable electrical performance.

13.3.7.4 Yield Strength

The metal yield strength can vary by two or three orders of magnitude depending on the metals selected and their deposition methods. Metals with low yield strength

will typically require less compressive stress to form electrical interconnections than metals with high yield strength and comparable native oxide. This lower stress may or may not occur at lower temperatures depending on the relative metal CTE and topography.

13.3.8

DBI® Metal/Silicon Oxide State of the Art

DBI® is a generic hybrid bonding technology that includes a wide range of metal/silicon oxide combinations. This section reviews four of these combinations as evaluated by a number of independent organizations and summarizes the state-of-the-art capability with regard to interconnect pitch, thermal budget, resistivity, yield, and reliability.

13.3.8.1 Aluminum/Silicon Oxide DBI® Hybrid Bonding

Aluminum/silicon oxide DBI® hybrid bonding has been reported by Edinburgh University [17]. A damascene process was used to build the hybrid surface with 20–40 nm of aluminum CMP dishing. Bonded hybrid wafers were heated to 435 °C to increase the bond strength. About 20 nm of the 40–80 nm metal-to-metal gap after placing hybrid surfaces into contact was closed during the post-contact temperature cycle. The residual gap was closed by stress relief-induced hillock formation resulting in a metal-to-metal bond and electrical interconnections. A minimum metal-to-metal contact area of 10 μm by 10 μm was needed to obtain electrical connections. Contact resistivity was over 1 kΩ μm² and the yield was 20%.

13.3.8.2 Copper/Silicon Oxide DBI® Hybrid Bonding

Copper/silicon oxide DBI® hybrid bonding has been reported by Ziptronix, Inc. and CEA-Leti [7, 18]. Damascene processes were used to build the hybrid surfaces with a copper CMP planar or dished topography of about 2 nm. The Ziptronix process included a TiW via and trench conductive diffusion barrier liner for improved reliability. CEA-Leti reported single connections with a contact resistivity of 0.98 Ω μm² and a 200 °C heat treatment after hybrid surface contact. Ziptronix reported fully functional serial daisy chains with 72 500 elements on a 25 μm pitch with contact resistivity less than 0.45 Ω μm² after a 125 °C heat treatment following hybrid surface contact. These parts exceed the JEDEC temperature cycling and HAST reliability requirement. Ziptronix has also reported scaling of the direct copper DBI® process to smaller pitch and higher yield with fully functional 463 000 element daisy chains on a 10 μm pitch while maintaining contact resistivity less than 0.45 Ω μm² using an alignment/placement pick-and-place tool with ±1 μm over 3σ accuracy. This process is based on existing CMOS industry standard volume production copper BEOL tools and processes.

13.3.8.3 Gold/Silicon Oxide DBI® Hybrid Bonding

Gold/silicon oxide DBI® hybrid bonding has been reported by Ziptronix, Inc. [3]. A nonplanar process was used to build the hybrid surface using 20–100 nm of gold

on top of a planar surface. Direct metal-to-metal bonding at room temperature was reported for 5 mm diameter gold pads on a 6 mm pitch with an unbonded annulus of less than 20 μm around 20 nm pads.

13.3.8.4 Nickel/Silicon Oxide DBI® Hybrid Bonding

Nickel/silicon oxide DBI® hybrid bonding has been reported by Ziptronix, Inc. (e.g., [4–6]). A planarized stud process was used to build the hybrid surface with a nickel CMP planar or dished topography of about 2 nm. Ziptronix reported fully functional serial daisy chains with 1 000 000 elements on an 8 μm pitch with contact resistivity less than 0.5 $\Omega\mu\text{m}^2$ with 300 °C heat treatment subsequent to hybrid surface contact. These parts exceeded ten times the JEDEC temperature cycling and three times the JEDEC HAST reliability requirement. Ziptronix has also reported scaling of the direct nickel DBI® process to 1.5 μm pitch with sub-micrometer pitch capability subject to adequate wafer alignment and placement accuracy. This process has also been used to three-dimensionally integrate industry standard CMOS aluminum and copper BEOL interconnect wafers. Wafer start options for this process include a planarized tungsten plug CMP aluminum BEOL surface and a planarized passivated copper BEOL surface. A lower CoO alternative for implementing nickel direct DBI® process in volume production is replacement of the tungsten plug or copper-filled via with nickel at the end of the BEOL.

13.4

Metal/Silicon Nitride DBI®

Another type of direct hybrid bonding is metal/silicon nitride hybrid bonding. This is of particular interest for applications in which reliability issues result from diffusion of the metal into the surrounding silicon oxide that can be resolved by the use of silicon nitride. An example of a metal for which this can be a concern is copper, as illustrated by the use of silicon nitride capping layers in copper dual damascene CMOS BEOL fabrication.

Figure 13.3 provides an example of a copper/silicon nitride hybrid bonding structure with intrinsically high reliability resulting from complete enclosure of copper with either a conducting barrier liner or insulating silicon nitride barrier. The preparation of this surface can be carried out with the damascene process flow described above with a capping layer of silicon nitride added on top of the silicon oxide prior to trench and/or via etch. The silicon nitride is thick enough to provide sufficient residual silicon nitride diffusion barrier thickness after the DBI® CMP and depends on CMP details, typically 0.1 to 0.5 μm .

This copper/silicon nitride hybrid bond surface is similar to a typical CMOS copper BEOL surface after deposition of silicon nitride on the copper CMP surface. The primary difference is exposed copper on the hybrid bond surface that will be subsequently electrically interconnected to another hybrid surface, for example copper/silicon nitride, as shown in Figure 13.4. Note that in the case of copper/silicon nitride to copper/silicon nitride hybrid bonding, there will generally be



Figure 13.3 Hybrid copper/silicon nitride surface before hybrid bonding.

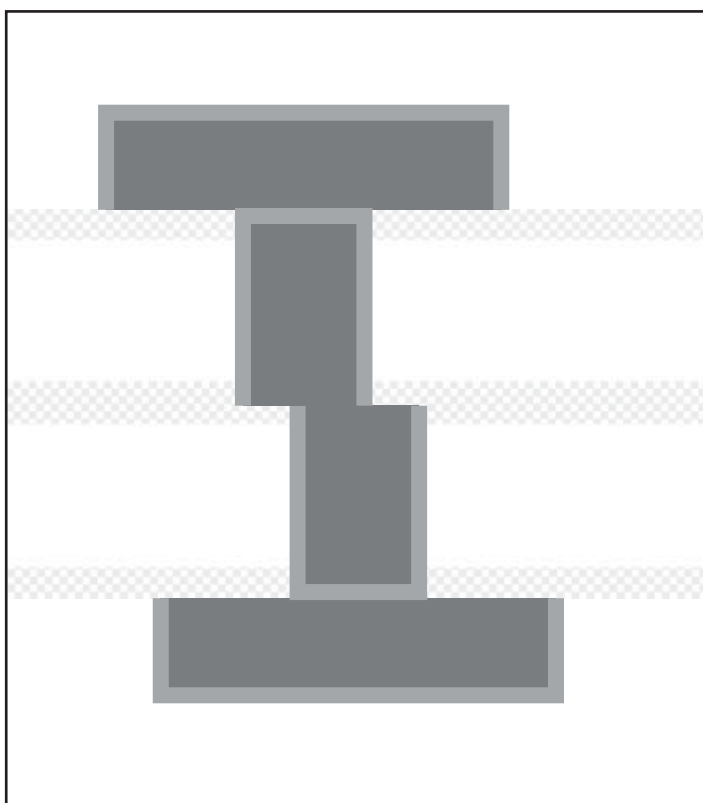


Figure 13.4 Bonded hybrid copper/silicon nitride hybrid surfaces.

some copper that is not bonded to copper due to misalignment resulting from imperfect alignment and placement of the two hybrid bonding surfaces together. The surface silicon nitride effectively caps this misaligned copper allowing a fully encapsulated, reliable 3D IC interconnect.

13.5

Metal/Silicon Oxide DBI® Hybrid Bonding Applications

Metal/silicon oxide DBI® hybrid bonding can be used in a wide variety of 3D packaging and integration applications. This section focuses on those 3D applications that require a process capability beyond that available from technology currently qualified for volume production that can be accommodated by DBI® and are thus likely to drive the adoption of this nascent hybrid technology.

Key distinguishing advantages of the DBI® technology compared to other bonding technologies are the ability to create large arrays of high-density 3D interconnections with high bond energy at low thermal budget with minimal applied external stress. Applications for which these advantages are required include pixelated 3D ICs, 3D heterogeneous integration, and CMOS (ultra) low-*k* 3D integration. The suitability of DBI® for these applications is described in more detail below.

13.5.1

Pixelated 3D ICs

A pixelated 3D IC is a type of 3D IC containing a periodic repetition of standard cells or pixels. Minimizing the pixel size with CMOS scaling reduces die size and cost assuming availability of a likewise scalable 3D interconnect bond technology. The capability of DBI® to support submicrometer 3D interconnect scalability is very well suited for this type of application.

An example of a pixelated 3D IC application is 3D backside illuminated (BSI) CMOS image sensors (CIS). Conventional two-dimensional (2D) BSI-CIS technology, consisting of bonding a CIS to a handle wafer and removing the CIS substrate to allow imaging from the backside, is experiencing rapid adoption due to improved pixel scaling, resolution, quantum efficiency, sensitivity, crosstalk, fill factor, chief ray angle, and module thickness. A 3D BSI-CIS differs from a conventional 2D BSI-CIS in that the handle wafer is a CMOS wafer that contains circuitry otherwise exterior to the pixels, enabling a 50% form factor reduction when stacked underneath the pixels. This standard CMOS handle wafer without the PMOS detectors is considerably less expensive than a conventional CIS CMOS wafer. The combination of reduced CMOS cost and reduced die size enables a 30% cost reduction in a smaller package for a 3D BSI-CIS part compared to a 2D BSI-CIS part with comparable resolution. Alternatively, a 3D BSI-CIS part can have double the pixels or resolution of a 2D BSI-CIS part in the same size package (R. Guidash, personal communication).

Advanced 3D BSI-CIS designs will require at least one 3D interconnection per pixel requiring 3D interconnect that can scale with the pixel pitch. The migration of frontside illuminated (FSI) CIS pixel pitch from the 1.6 to 1.4 μm node and the fundamental capability of BSI to scale better than FSI is expected to result in a required 3D BSI-CIS pixel pitch of 1 μm and below. This submicrometer pitch scalability is within DBI[®] capability.

The suitability of DBI[®] for this application has been investigated by Kodak (unpublished data). A 1.5 megapixel, 1.25 μm pixel pitch, 3D BSI-CIS was designed and constituent 110 nm aluminum BEOL CMOS sensor and circuit wafers built through tungsten plug CMP, as described above, by a commercial foundry. The wafers were then hybrid bonded using a direct nickel DBI[®] planarized stud process and the sensor wafer was thinned to 10 μm using back-grinding and silicon CMP by Ziptronix. Bonded wafers were annealed at about 400 °C to improve dark current. Low sensor wafer distortion was enabled by high DBI[®] bond energy at low temperature that facilitated wafer-scale color filter array fabrication. 3D BSI-CIS parts were then singulated, packaged, and tested yielding the results described below.

A scanning electron micrograph cross section of a single DBI[®] 3D interconnection at the hybrid interface within the 3D BSI-CIS part is shown in Figure 13.5. This micrograph shows the nickel DBI[®] interconnection of metal 4 in the sensor wafer to metal 4 in the circuit wafer using a nickel diameter and thickness of about 3 and 0.5 μm , respectively.

The quantum efficiency of the 1.5 megapixel, 1.25 μm pixel pitch 3D BSI-CIS parts built with nickel DBI[®] and bulk silicon CMOS detector wafers were measured after application of an antireflection coating. Ideal blue response was obtained as shown in Figure 13.6. Lag, linearity, and charge capacity were as good as FSI-CIS parts. Operability of the 1.5 megapixels was 100%. An unfocused image obtained from the prototype parts is shown in Figure 13.7.

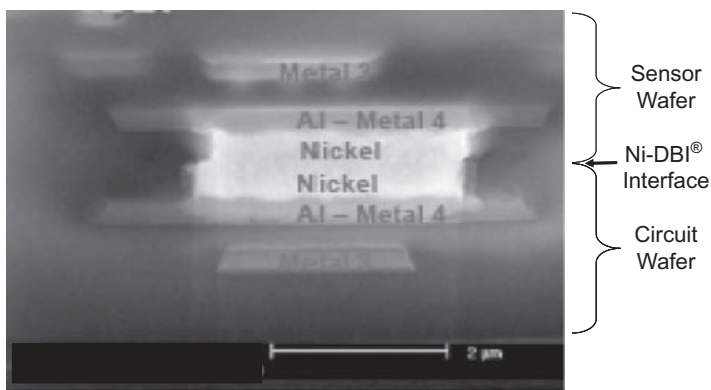


Figure 13.5 Scanning electron micrograph cross section of 3 μm diameter nickel DBI[®] interconnecting CMOS sensor and circuit wafers in prototype 1.5 megapixel, 1.25 μm pitch 3D BSI-CIS.

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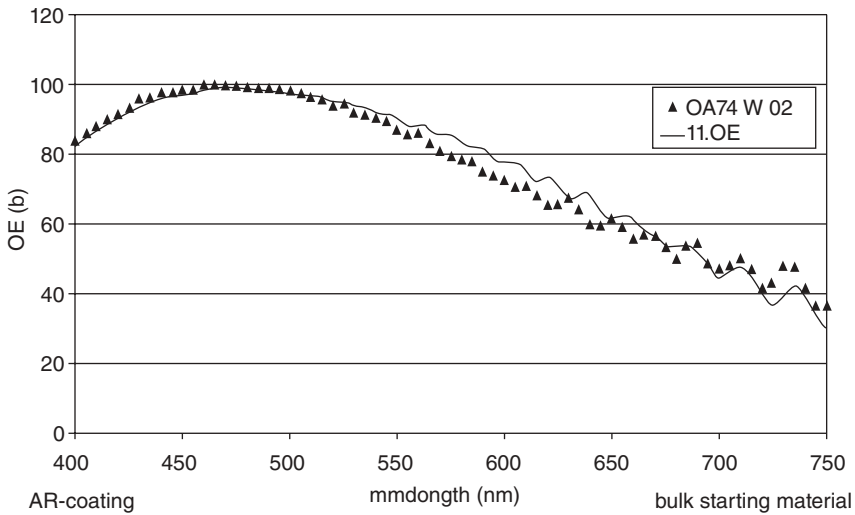


Figure 13.6 Quantum efficiency (QE) versus wavelength for antireflective (AR)-coated 3D BIS-CIS built with a bulk silicon CMOS detector wafer and nickel DBI®.



Figure 13.7 Unfocused image from 1.5 megapixel, 1.25 μm pixel pitch, 3D BIS-CIS built with nickel DBI® hybrid bonding.

Scaling the format to 8 megapixels and the pixel pitch and DBI® interconnect to 1.1 μm pitch is projected to enable a high-resolution 8 megapixel CIS in an industry-standard SMIA-65 package for mobile imaging applications including cell phones. The excellent performance and yield of these prototype 3D BSI-CIS parts indicate that DBI® is a suitable candidate technology for next-generation BSI-CISs.

13.5.2

Three-Dimensional Heterogeneous Integration

Three-dimensional heterogeneous integration (HI) involves bonding of materials like III/V semiconductors that can have significantly lower thermal budgets than

CMOS. These materials also have significantly different CTE that can further limit the thermal budget of a bond or post-bond fabrication process. The precise temperature limit depends on the combination of materials integrated, so the 3D bonding and interconnect technology with the lowest thermal budget will generally be able to accommodate the widest variety of HI. Applications enabled by HI include improved spectral response image sensors by combining non-silicon detector material with CMOS readout integrated circuits and high-resolution pixilated displays by combining nitride-based visible emitting material with CMOS driver circuits.

The fundamental high bond energy at low temperature capability of DBI(R) is ideal for HI. For example, the 125 °C result reported by Ziptronix for direct copper DBI® with 2 nm dishing is well within the thermal budget requirements of most HI combinations. Reduction of this thermal budget to room temperature is possible with the appropriate surface roughness, planarity, and activation and termination as described above.

13.5.3

CMOS (Ultra) Low-k 3D Integration

Advanced CMOS nodes require (ultra) low-dielectric materials to minimize interconnect delays. These materials are very brittle and can be easily damaged due to their poor mechanical properties. A 3D integration technology that applies minimum stress is thus expected to be compatible with advanced CMOS nodes. The capability of DBI® to achieve high bond energy at low temperature by simply placing hybrid surfaces together without any externally applied pressure indicates that this is a suitable technology for this application.

The suitability of DBI® for CMOS low-*k* 3D integration was evaluated by Ziptronix with a direct nickel DBI® process using 300 mm, 65 nm, 12-level metal, copper low-*k* FPGA wafers and a silicon test wafer. After DBI® bonding, the silicon test wafer was thinned to about 25 μm and silicon vias were cut to expose FPGA pads for testing. A scanning electron microscopy cross section showing DBI® integration of the 65 nm, copper low-*k* FPGA wafer to the silicon test wafer is shown in Figure 13.8. Comparison of on-wafer FPGA tests before and after DBI® bonding, test wafer thinning, and FPGA pad cut indicated no degradation in FPGA performance due to the DBI® and post-bond processes. This initial DBI® low-*k* result indicates compatibility of DBI® with CMOS low-*k* 3D integration.

13.6

Summary

Metal/silicon oxide hybrid bonding enables direct bonding between both metal and silicon oxide components with high bond energy and low thermal budget required for 3D IC applications. The technology is robust in that it can be implemented with industry-standard CMOS wafer fabrication tools and processes and

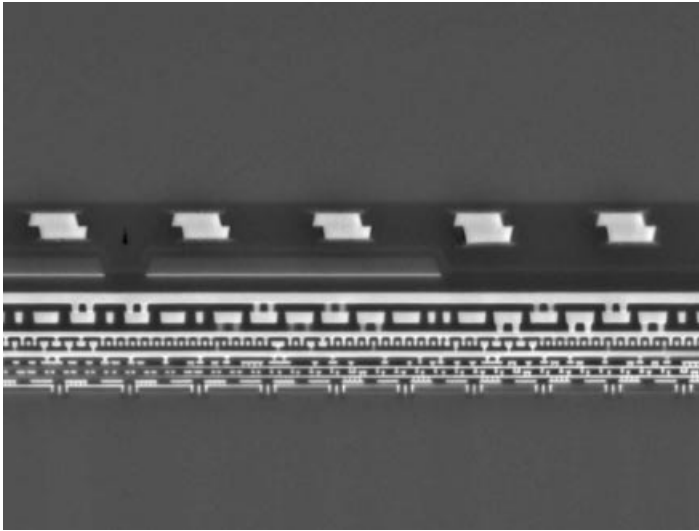


Figure 13.8 Scanning electron micrograph cross section of 10 μ m pitch nickel DBI® 3D interconnecting 65 nm, 12-level metal, copper/low-*k* FPGA CMOS wafer-to-silicon test wafer.

a variety of metals, process flows, surface topographies, surface patterning, and bond configurations. High bond energy with submicrometer 3D interconnect scalability at low or room temperature without externally applied pressure designate this technology as a preferred platform solution for emerging 3D IC applications including pixelated ICs, HI, and copper/low-*k* CMOS.

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