

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co., Ltd.,
Petitioner,

v.

SiOnyx, LLC,
Patent Owner.

Case No. IPR2025-00064
Patent No. 10,347,682

**DECLARATION OF DR. MICHAEL LEBBY IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,347,682**

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I. INTRODUCTION

1. I, Michael Lebby, declare as follows.
2. I have been retained as a technical consultant on behalf of Samsung Electronics Co., Ltd. (“Samsung” or “Petitioner”), which I understand to be the petitioner in the present proceeding. I have been asked to consider whether the references listed as Exhibits 1006, 1007, 1009, 1010, and 1012 below disclose or render obvious the limitations recited in claims 1-44 of U.S. Patent No. 10,347,682 (Ex-1001, “’682 patent”). I have also been asked to consider the state of the art. My opinions are provided in this declaration.
3. I am being compensated at my standard consulting rate for my time. My compensation is in no way contingent on the results of these or any other proceedings relating to the ’682 patent.

II. BACKGROUND AND QUALIFICATIONS

4. A description of my professional background and qualifications is provided below. An additional account of my work experience and qualifications is included in my *curriculum vitae*, which is Ex-1005 (“CV”).
5. I am currently the CEO and CTO at GenusTechnik Inc., which provides consulting services in areas that include image sensors, photonics, optoelectronics, semiconductors as used in image sensors and other optical applications.

6. In addition, I am currently the Chairman, CEO, and Director of the Board of Directors for Lightwave Logic. As CEO, I successfully guided Lightwave Logic to up-list to NASDAQ in September 2021 organically (i.e., without the raising of financing), and I led the company to acceptance in the Russell 3000 index in 2022.

7. I have led and run optoelectronics start-ups, and I have commercialized optoelectronic and photonics technologies into volume manufacturing. I have also worked as a Corporate Venture Capitalist specializing in optical communications, photonics, sensing, electronics, and semiconductors, and I am currently a technical expert advising the European Commission regarding evaluation of numerous photonic technology proposals, including image sensor proposals. I am a Fellow Member of the National Academy of Inventors (NAI), the IEEE, and Optica (OSA), and I was voted Photonic Integrated Circuit (PIC) business leader of the year by the PIC International Conference in 2018.

8. In particular, my technical expertise has included the design of components for photonics technology that can source light as well as receive and detect light. These components include LEDs, ICs, lasers, photodetectors, diodes, image sensors, etc. In many of my industrial and commercial roles in the photonics industry I have used, designed, optimized, and improved photonic materials, components, and packages both through solutions of engineering problems as well as patents and publications.

9. Over the course of my career in photonics, optoelectronics, and optical technology in general, I have worked in nearly every aspect of the field, including optical assembly, laser diodes, photodetectors, image sensors, LEDs, integrated circuits (e.g. drivers, and other basic electronic digital and analog functions), as well as fiber optics. In particular, I have designed optoelectronic devices such as LEDs, laser diodes (VCSELs – vertical cavity surface emitting lasers), photodiodes, image sensors, and solar cells with a focus on efficient optical device design that maximizes device performance. For example, I have worked on improving light extraction efficiency in laser diodes as well as LEDs, where these devices are utilized in modules. I have also worked on arrays of detectors for sensing applications.

10. I started my career in 1977 at the Ministry of Defense (United Kingdom), in the Royal Electrical and Mechanical Engineers as a telecommunications apprentice. At the Ministry of Defence, I studied material and characterization issues relating to Gallium Arsenide (GaAs) and Indium Phosphide (InP) optoelectronic devices, as well as semiconductor device design, fabrication, and characterization, particularly with materials using III-V semiconductors. I also worked with silicon for integrated circuits, silicon photonics, and ceramic-based radio-frequency (RF) electronic packaging that included low-temperature co-fired ceramic. These devices and materials were utilized in photonic-based transceiver packages and modules. I also worked on electronics, motors, sensors, and other technologies that combined photonics with electronics.

11. I attended the University of Bradford, where I obtained a Bachelor's of Engineering (Electrical Engineering), with honors, in 1984, an MBA in 1985 and a Ph.D. (Electrical Engineering) in 1987. My Ph.D. thesis related to the characterization and fabrication of both optoelectronic and electronic semiconductor devices that included the detection of light. In 2004, I was awarded a Doctor of Engineering (a Doctorate degree higher than a Ph.D.) from the University of Bradford for my "Technical Contributions to Optoelectronics." This was only the second time in the University of Bradford's history that a Doctor of Engineering was granted based on industry experience.

12. While attending the University of Bradford and for a few years thereafter, i.e., from 1985 to 1989, I worked as a researcher in the Photonics Research Department of AT&T Bell Labs ("Bell Labs"). At Bell Labs, I focused my research on novel device designs using III-V semiconductor material systems including FETs, bipolar transistors, LEDs, laser diodes, and photodetectors. My research at Bell Labs became the subject of my Ph.D. thesis.

13. After completing my Ph.D. at the University of Bradford and my work at Bell Labs, I became a Research and Development Manager ("R&D Manager") in the photonics division of Motorola's Corporate R&D Labs ("Motorola"). I worked at Motorola from 1989 to 1998, where my responsibilities included research and development in optical interconnects, electrical and fiber optic connectors,

optical/electrical engines, electronic ICs, displays, laser devices, LEDs, optical lenses, image sensors, and optical waveguides, as well as the packaging and reliability of mobile product prototypes. Some of the prototypes on which I worked included moving parts with motors (both standard as well as semiconductor MEMs based), and phased array optical beams that could direct and re-direct optical beams. While at Motorola, I was the inventor or co-inventor on over 150 utility patents, and I received a special award from the Chairman of Motorola in 1998 for exemplary patent accomplishments. At that time, I had the highest number of issued utility patents in the history of Motorola.

14. As an R&D Manager at Motorola, I initiated Motorola's work in optical interconnect technology (known at Motorola as "Optobus"TM) and associated optical connectors, electronics, and photonics components, and I was also involved in research and development on the IC chip designs that this parallel interconnect module utilized. In this project, transparent plastics were developed and molded onto standard metallic lead frames for both light-emitting devices (e.g., LEDs, VCSELs) and photodetectors, which collect light and convert it into an electronic signal. These transparent lead frame packages were developed in volume production at Motorola. I also worked on various techniques to improve both photonics based detectors such as photodetectors, image sensors as well as photonics based emitters such as lasers and LEDs, both as individual components as well as in arrays of multiple components.

15. In 1998, I left Motorola to join TE Connectivity (previously Tyco Electronics) as Director of Technology and Business Development. In that role, I helped develop technology strategy for optical communications, optoelectronic transceivers, and fiber optic connector and adapter products for the Global Optoelectronics Division. My work included designing and characterizing photodetectors, sensors, LEDs, laser-based photonic packages and modules for product manufacturing.

16. In 1999, I joined Intel Capital (“Intel”) as Director of Business Development and as a corporate investor. My work at Intel included sourcing, negotiating, and closing private placement equity deals in the optical networking, photonic component, interconnect, optical lens, image sensor, and semiconductor industries. My work at Intel also included investigating the investment of Intel Capital equity in photonic devices, optical beams, and other technologies to support the physical movement of optical signals. I also was one of the founders of Intel’s silicon photonics division, which worked to establish a fabrication facility in South San Jose to investigate silicon based image sensors and the integration of silicon FET electronics with optoelectronics into the same silicon semiconductor wafer.

17. From 2005 to 2010, I served as the Executive Director, President, and CEO of the Optoelectronic Industry Development Association (OIDA) – a trade association that represented photonics manufacturers in the fields of photonic sensing,

fiber optics, display, defense, aerospace, LED lighting and automotive/motor vehicles.

I was responsible for organizing technical conferences, workshops and forecasts using industry roadmaps, all of which featured a portfolio of photonics technology that included: optical sensors, free-space optics, optical interconnects, fiber optics, optical communications, automotive photonic technologies, wavelength division multiplexing, LEDs, displays and their associated packaging.

18. In 2010, I became the General Manager and CTO of Translucent, Inc., a start-up company that developed and manufactured silicon and rare earth oxide-based epitaxial semiconductor wafers.

19. I was employed by Glyndŵr University from 2013 to 2015 as a Professor of Optoelectronics, where I focused on the design, simulation, and testing of high-speed, low-power photonic integrated circuits, optoelectronic integrated circuits, laser diodes, optics, and solar cells for applications that included communications, automotive, displays, sensing, and energy.

20. From 2013 to 2015, I was also employed as the President and CEO of OneChip Photonics Corporation, where I additionally served as an elected independent board member. In these roles, I focused on technical, business, and operational strategy for fiber optic communications based on InP photonic integrated circuits, as well as optoelectronic integrated circuits for fiber optic transceivers that incorporated electrical and optical multiplexing schemes using fiber optic connectors.

21. Over the course of my career, I have also led panels and given numerous keynote and invited presentations, speeches, and talks at workshops and conferences, including on photonic and optoelectronic materials, devices, components, packages as well as photonics technology in general.

22. Due to my passion for optics, I have been elected to the London Guild of Spectacle Makers. A more detailed description of my education, as well as my training and experience in the relevant technology, is included in my CV.

23. I hold over 340 combined issued USPTO patents and USPTO published patent applications that have been derived from over 230 issued U.S. utility patents, mostly in the field of optoelectronics, photonics, electronics, and semiconductors. I have been cited by the USPTO to be in the most prolific seventy-five inventors in the United States from 1988 to 1997.

24. I have authored approximately sixty-five (65) publications, and have achieved over 400 media events that include: technical articles, books, chapters, invited speaker events at conferences as well as interviews that included TV, video, radio, and social, industrial, professional media in general. This includes technical, business-related, and financial conferences as a contributing, invited, and keynote speaker. Details can be found in my CV. Over the past decade, I have been a project reviewer and technical expert for the European Commission on numerous occasions.

25. I have also served as an expert witness on numerous patent matters, including 50 IPR proceedings and 5 PGR proceedings. I have also served on over 60 oral depositions that include ITC and District court proceedings.

26. A complete listing of these patents, publications, articles, lectures, and other public media is included with my CV.

27. On the basis of my education and the experience described above, I believe I am qualified to give the opinions set out herein.

III. MATERIALS REVIEWED

28. I am not an attorney and offer no legal opinions, but in my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art. *See* Section VI.C below for the level of ordinary skill in the art for this declaration.

29. In preparing this declaration, I reviewed the '682 patent, including the claims of the patent in view of the specification, and I have reviewed the prosecution history of the '682 patent and numerous publications and technical references from and preceding the time of the alleged invention. More specifically, I have reviewed each of the following:

Exhibit	Description
1001	U.S. Patent No. 10,347,682 (the "'682 patent")
1002	File History for U.S. Patent No. 10,347,682
1003	Provisional Application No. 61/841,326
1006	U.S. Patent Application Publication No. 2012/0068289 (Alie)

Exhibit	Description
1007	U.S. Patent Application Publication No. 2006/0081900 (Baggenstoss)
1008	Intentionally Left Blank
1009	U.S. Patent Application Publication No. 2012/0313204 (Haddad204)
1010	U.S. Patent Application Publication No. 2010/0006969 (Park)
1011	U.S. Patent No. 7,928,389 (Yap)
1012	U.S. Patent Application Publication No. 2011/0227138 (Haddad138)
1013	Samsung's Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1014	SiOnyx's Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1015	Email from N. Subhedar re: Claim Construction M&C Follow-Up (Sept. 8, 2024)
1016	U.S. Patent No. 8,680,591 (Haddad138 Issued Patent)
1017	U.S. Patent No. 9,496,308 (Haddad204 Issued Patent)
1018	The Authoritative Dictionary of IEEE Standard Terms (7th ed. 2000)
1019	Stephen Y. Chou et al., <i>Nanoimprint Lithography</i> , J. Vac. Sci. Technol. B 14(6), 4129-33 (1996)
1020	Gary S. May & Simon M. Sze, <i>Fundamentals of Semiconductor Fabrication</i> (2003)
1021	Provisional Application No. 61/311,004 (Haddad138-Provisional004)
1022	Provisional Application No. 61/243,434 (Haddad138-Provisional434)
1023	Provisional Application No. 61/311,107 (Haddad138-Provisional107)
1024	U.S. Patent Application Publication No. 2012/0146172 (Carey)
1025	U.S. Patent No. 7,442,629 (Mazur)
1026	U. Gösele & Q.-Y. Tong, <i>Semiconductor Wafer Bonding</i> (1998)
1027	U.S. Patent Application Publication No. 2011/0304003 (Tanida)
1028	S. Wolf, <i>Microchip Manufacturing</i> (2004)
1029	<i>Encyclopedia of Physical Science and Technology</i> (3rd ed. 2002)
1030	Christoph Posch, <i>Detectors, Pixels, and Signal Processing, in SMART CAMERAS</i> (Ahmed Nabil Belbachir ed., 2010)
1031	E. Fred Schubert, <i>LIGHT-EMITTING DIODES</i> (2nd ed. 2006)
1032	U.S. Patent Application Publication No. 2006/0216904 (Tong)
1033	Provisional Application No. 61/317,147 (Alie-Provisional)
1034	U.S. Patent Application Publication No. 2013/0207168 (Edwards)
1035	Maik Wiemer, et al., <i>Plasma-Activated Bonding, in Handbook of Wafer Bonding</i> (Peter Ramm, et al., eds., 2012)

IV. RELEVANT LEGAL STANDARDS

30. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to forming my opinions. I have applied the following understanding of the law.

31. I have been informed that a patent claim may be “anticipated” if each element of that claim is present either explicitly or inherently in a single prior art reference, and that the elements should be arranged in the reference as in the claim. Petitioner’s counsel has informed me that for a claimed limitation to be inherently present, the prior art need not expressly disclose the limitation, so long as the claimed limitation necessarily flows from a disclosure in the prior art.

32. I have been informed that a patent claim can be considered to have been obvious to a person of ordinary skill in the art at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed.

33. I have been informed that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and

- what differences, if any, existed between the claimed invention and the prior art.

34. I have been informed that a single reference can render a patent claim obvious if any differences between that reference and the claims would have been obvious to a person of ordinary skill in the art. Alternatively, the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider, among other factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, and when combined, would yield predictable results;
- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;

- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

35. Petitioner's counsel has informed me that one of ordinary skill in the art has ordinary creativity and is not an automaton. Petitioner's counsel has informed me that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

36. I understand that various objective or "real world" factors may be indicative of non-obviousness. I understand that such factors include:

- the commercial success of the claimed invention;
- the existence of a long-felt, unresolved need for a solution to the problem solved by the claimed invention;
- failed attempts to solve the problem solved by the claimed invention;
- copying of the claimed invention;
- unexpected results of the claimed invention;
- praise for the claimed invention by others in the relevant field; and
- willingness of others to accept a license under the patent because of the merits of the claimed invention.

V. TECHNOLOGY BACKGROUND

37. Since the early 2000s, digital cameras and camcorders have become increasingly popular, largely due to the development of advanced image sensors. These sensors play a critical role in converting visual information into electrical signals, which are then processed to create digital images or videos. At the heart of an image sensor lies an array of light-sensitive pixels, each of which is a photodiode capable of detecting light. The photodiode's function is to convert incoming light photons into electrons; the quantity of electrons collected at each pixel determines the pixel's brightness. By assembling this data across all pixels, the sensor constructs a coherent image or video corresponding to the captured scene.

38. In an ideal scenario, an image sensor would achieve perfect efficiency, converting every photon that strikes it into a collected electron. However, in practice, some photons are lost during the conversion process. The efficiency of this conversion is quantified by a metric known as external quantum efficiency, or quantum efficiency for short. Quantum efficiency is defined as the percentage of photons incident on an image sensor that are converted into collected electrons. Ex-1030, 60. Some incident photons may be lost because they are reflected off before reaching the semiconductor layer including a photodiode; others may be lost because they pass through the semiconductor layer without being absorbed. To mitigate such losses, it is common practice to include in an image sensor microstructures that let more light into the

semiconductor layer including a photodiode, as well as microstructures that reflect and scatter light that leaves the semiconductor layer back into the semiconductor layer.

39. Photodiodes are typically fabricated by doping a semiconductor layer to create a junction, which is used for sensing light. A photodiode junction is then connected to a neighboring metallization layer, which carries the electrical signal to external circuits that integrate the signals from all pixels to form a complete image. In the design of image sensors, the side of the semiconductor layer where the photodiode junction and the metallization layer are located is referred to as the “front side,” while the opposite side is known as the “backside.” Image sensors can be designed to receive light from either the front side (front side illuminated, or FSI) or the backside (backside illuminated, or BSI), each offering different advantages and trade-offs.

40. Front side illuminated sensors are easier and less costly to manufacture, but they suffer from greater light loss because the incident light must pass through the metallization layer before reaching the photodiode junction. This can reduce the sensor’s overall efficiency and image quality, especially in low-light conditions. Conversely, backside illuminated sensors are more challenging and expensive to produce but offer superior performance because the incident light directly reaches the photodiode junction without passing through the metallization layer. This design reduces light loss and improves the sensor’s quantum efficiency, leading to better image quality, particularly in demanding lighting environments.

VI. OVERVIEW OF U.S. PATENT NO. 10,347,682

A. Summary

41. The '682 patent states that silicon imaging devices were widely used, including in both front side illumination (FSI) and backside illumination (BSI) configurations. '682 patent, 1:16-29. In an FSI device, incident light enters the device by “first passing by transistors and metal circuitry.” '682 patent, 5:60-62. In a BSI device, on the other hand, “incident light enters the device via the light sensitive region opposite the circuitry.” '682 patent, 6:4-6.

42. The '682 patent purports to improve upon traditional optoelectronic devices by adding a textured layer. Figure 2 depicts an FSI embodiment with a textured layer:

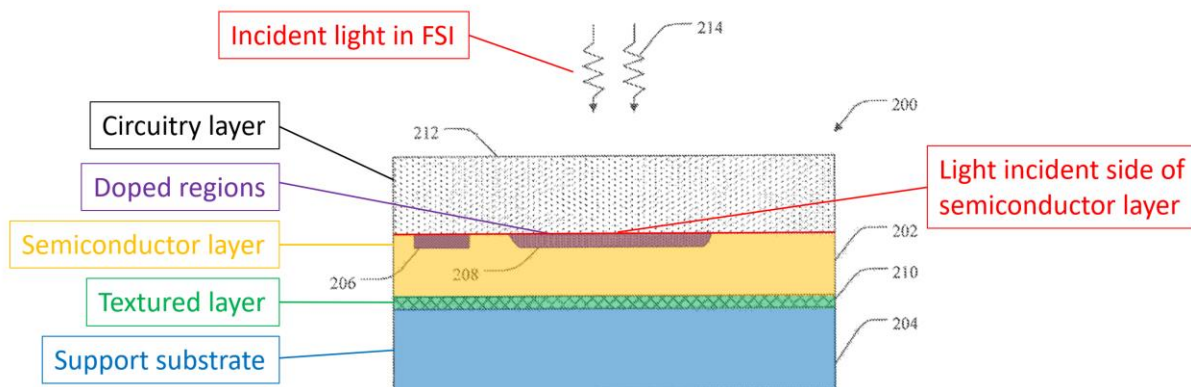


FIG. 2

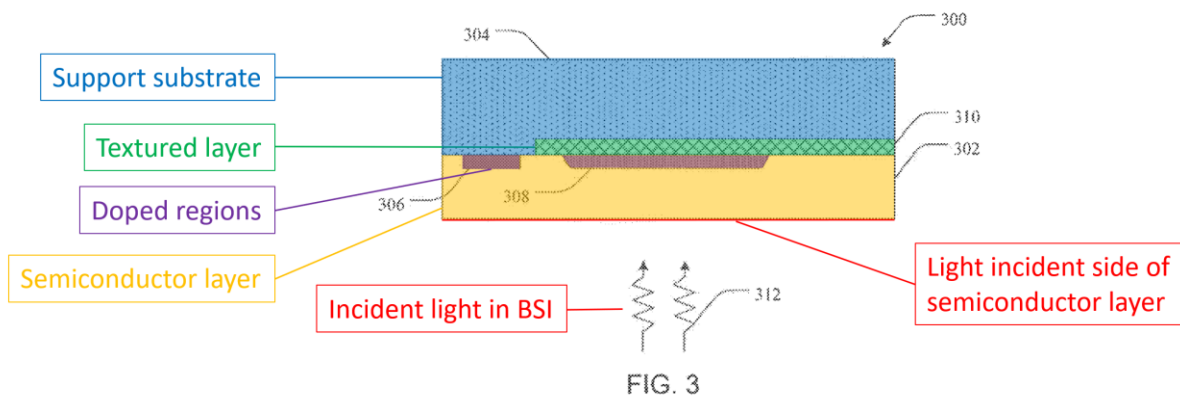
'682 patent, Fig. 2 (annotated).

43. Light 214 comes from the top, passing through a circuitry layer 212 to reach a semiconductor layer 202. '682 patent, 6:44-47. The semiconductor layer 202

has doped regions 206 and 208 that form a junction for sensing light. '682 patent, 6:36-40. On the bottom side of the semiconductor layer is a textured layer containing surface features. '682 patent, 6:40-42. The surface features of a textured layer include shapes such as “cones, pillars, pyramids, inverted features, trenches, gratings, protrusions, and the like.” '682 patent, 9:34-36. The textured layer allegedly functions to “diffuse light, to redirect light, and to thus increase the quantum efficiency.” '682 patent, 9:25-27.

44. The Figure 2 device is an FSI device because light 214 enters the device from the top, first passing through a circuitry layer 212 before reaching a semiconductor layer 202. '682 patent, 6:44-47.

45. Figure 3 depicts a BSI embodiment with a textured layer:



'682 patent, Fig. 3 (annotated).

46. The Figure 3 device is a BSI device because light 312 enters the device from the bottom, reaching a semiconductor layer 302 without passing through a circuitry layer. '682 patent, 6:63-65.

47. Unlike the independent claims of the '682 patent, which all require a textured region **on** the light incident side, both Figures 2 and 3 depict a textured layer (green) on a side of the semiconductor layer (yellow) **opposite** the light incident side. The '682 patent does not include a figure with a textured layer or region **on** the light incident side or identify any advantage to such a configuration. The '682 patent, though, notes that “the textured region can be located on the light incident side of the semiconductor material,” as well as being located “on a side of the semiconductor material opposite the light incident side, or both on the light incident side and opposite the light incident side.” '682 patent, 7:43-48.

B. Prosecution History

48. The '682 patent was filed on June 5, 2017, claiming priority to Provisional Application No. 61/841,326, filed on June 29, 2013.

49. Following an office rejection, the applicant added to claim 1 two limitations in an attempt to overcome the cited prior art: (1) shallow trench isolation surface features being located on the light incident side, and (2) a first bonding layer. Ex-1002 at 70. After another office rejection, the applicant added to claim 1 the limitation of “wherein said optoelectronic device is a photosensitive imager device capable of detecting visible and infrared electromagnetic radiation.” Ex-1002 at 110. The applicant also added to claim 17 (issued as claim 24) the limitation of bonding a first bonding layer to a second bonding layer. Ex-1002 at 111.

50. The examiner issued a notice of allowance, noting that the cited prior art did not disclose “a support substrate coupled to said semiconductor layer and a first bonding layer disposed between the semiconductor layer and the support substrate” and “bonding the first bonding layer to a second bonding layer disposed on the support substrate.” Ex-1002 at 1629.

C. Level of Ordinary Skill in the Art

51. It is my understanding that factors defining the level of ordinary skill in the art include: (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of technology; and (5) the educational level of active workers in the field.

52. A person of ordinary skill in the art (“POSITA”) as of June 2013 would have had a bachelor’s degree in engineering, physics, or a related or equivalent field, and two or more years of experience researching, developing, designing, and/or evaluating image sensors using photonics. A person with less or different education but more relevant practical experience, or vice versa, may also meet this standard.

53. I met this definition of a POSITA as of June 2013. I applied this definition of a POSITA in forming my opinion in this declaration.

54. U.S. Patent No. 11,069,737 (the “’737 patent”) is a continuation of the ’682 patent, and shares the same specification and the same or similar claim terms with

the '682 patent. I understand that SiOnyx, LLC ("SiOnyx" or "Patent Owner") asserted the '737 patent against Petitioner in *Sensors with Pixels and Products Containing the Same*, Inv. No. 337-TA-1403 (ITC) ("737 Case"). I understand that Patent Owner's expert in the 737 Case opined that "[t]he level of ordinary skill for the Asserted Patents should be defined as a person having at least a bachelor's degree in electrical engineering, materials science, or physics, (or an equivalent technical degree), at least two years of experience in optoelectronics, and at least three years of work experience in semiconductor manufacturing. Further, a master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa." I met Patent Owner's definition of a POSITA as of June 2013. My opinions remain the same under Patent Owner's definition.

D. Claim Construction

55. I understand that in this proceeding, the claims should be construed in accordance with their ordinary and customary meaning in light of the specification, as understood by one of ordinary skill in the art. I have therefore applied those plain and ordinary meanings in my analysis.

56. I understand that, in the 737 Case, Petitioner and Patent Owner have proposed competing constructions for certain terms of the '737 patent. See Ex-1013; Ex-1014; Ex-1015.

57. For purposes of my opinions, I was asked to apply the parties' proposed constructions where both parties' proposed constructions were available and consistent with the plain and ordinary meaning. Where Petitioner proposed a certain term was indefinite, I was asked to apply Patent Owner's proposed construction where it did not conflict with the plain and ordinary meaning.

VII. OVERVIEW OF THE PRIOR ART

A. Haddad138 (Ex-1012)

58. I understand that Haddad138 is prior art because it was published on September 22, 2011, which is more than one year before the '682 patent's provisional application filing date of June 29, 2013.

59. Although Haddad138 was listed in an information disclosure statement (IDS) along with almost 900 other documents, it was not discussed during prosecution.

The named inventors of the '682 patent, Homayoon Haddad and Jutao Jiang, are also joint inventors of Haddad138. The '682 patent's provisional application incorporates the Haddad138's patent application by reference, referring to Haddad138 for "[f]urther details regarding both BSI and FSI photodiodes, pixels, imagers, and other optoelectronic devices." Ex-1003, 9:18-20.

Like the '682 patent, Haddad138 discloses an optoelectronic device having a textured region with surface features. Like the textured region of the '682 patent, Haddad138's textured region includes surface features in the shapes of "cones,

pyramids, pillars, protrusions, micro lenses, quantum dots, inverted features and the like.” Haddad138, [0063]. Haddad138’s “textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad138, [0063].

60. Figure 9 depicts an example optoelectronic device with a textured region 90. Haddad138, [0087].

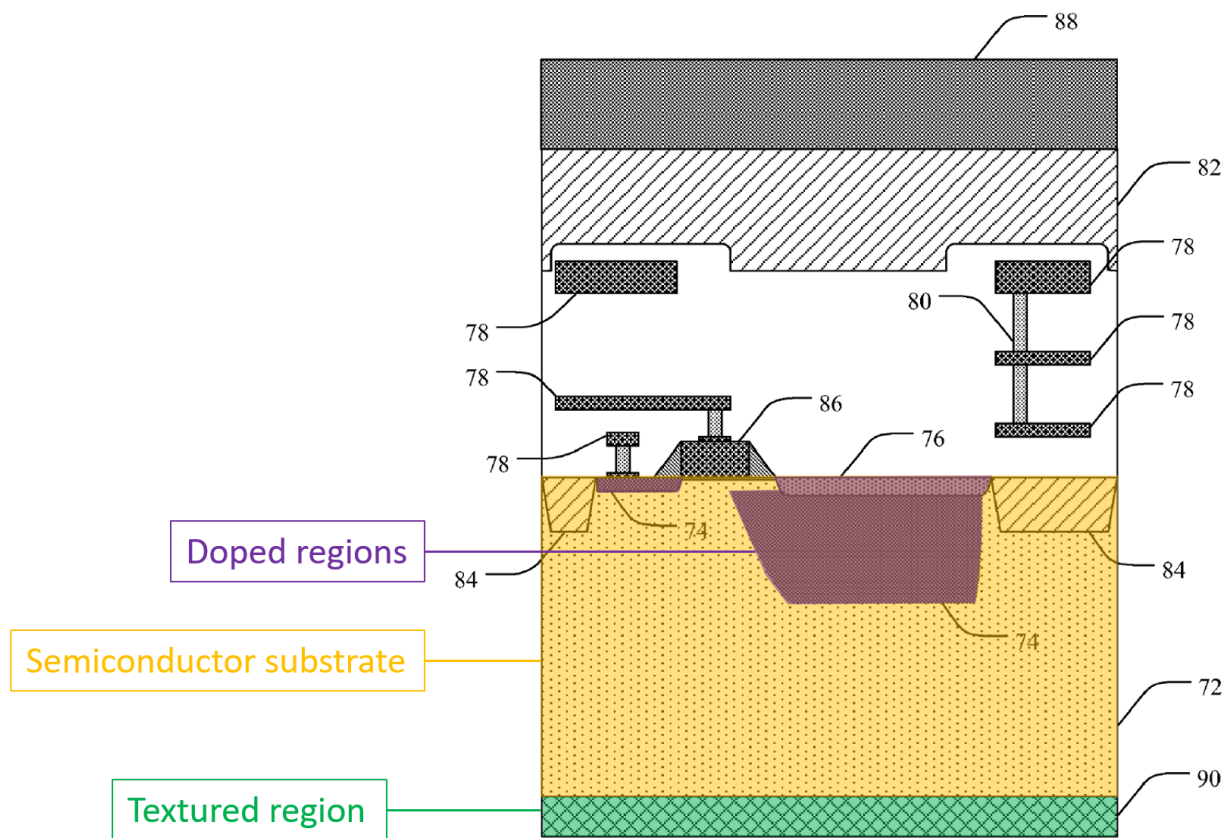


FIG. 9

Haddad138, Fig. 9 (annotated).

Like the '682 patent, Haddad138 discloses that its devices “can be adapted for

either [FSI or BSI] configuration.” Haddad138, [0048]. “In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry.” Haddad138, [0048]. The Figure 9 device has such a metallization layer on the top side of the semiconductor substrate. Haddad138, [0085]. When the Figure 9 device is adapted for an FSI configuration, therefore, incident light would enter from the top, similar to the FSI device depicted in Figure 2 of the ’682 patent. *See* Haddad138, [0048]; *see also* Haddad138, [0049] (explaining that, in an FSI configuration, “light enters the semiconductor substrate from the direction of the multiple doped regions”).

61. When the Figure 9 device is adapted for a BSI configuration, incident light would enter from the bottom, similar to the BSI device depicted in Figure 3 of the ’682 patent. *See* Haddad138, [0048] (disclosing that in BSI imagers incident light is “mostly absorbed prior to reaching the circuitry”). A BSI adaptation of the Figure 9 device is further discussed below regarding limitation 1[b].

B. Baggenstoss (Ex-1007)

62. I understand that Baggenstoss is prior art because it was published on April 20, 2006, which is more than one year before the ’682 patent’s provisional application filing date of June 29, 2013.

63. Baggenstoss was not listed in an IDS and was not discussed during prosecution. A parent application (of which Baggenstoss is a divisional) was listed in

an IDS along with almost 900 other documents, but it was not discussed during prosecution.

64. Baggenstoss discloses an optoelectronic device with a textured region in the form of a grated interface formed by trenches (elements 144 in Figure 4, below). Baggenstoss, [0031]-[0032], [0009].

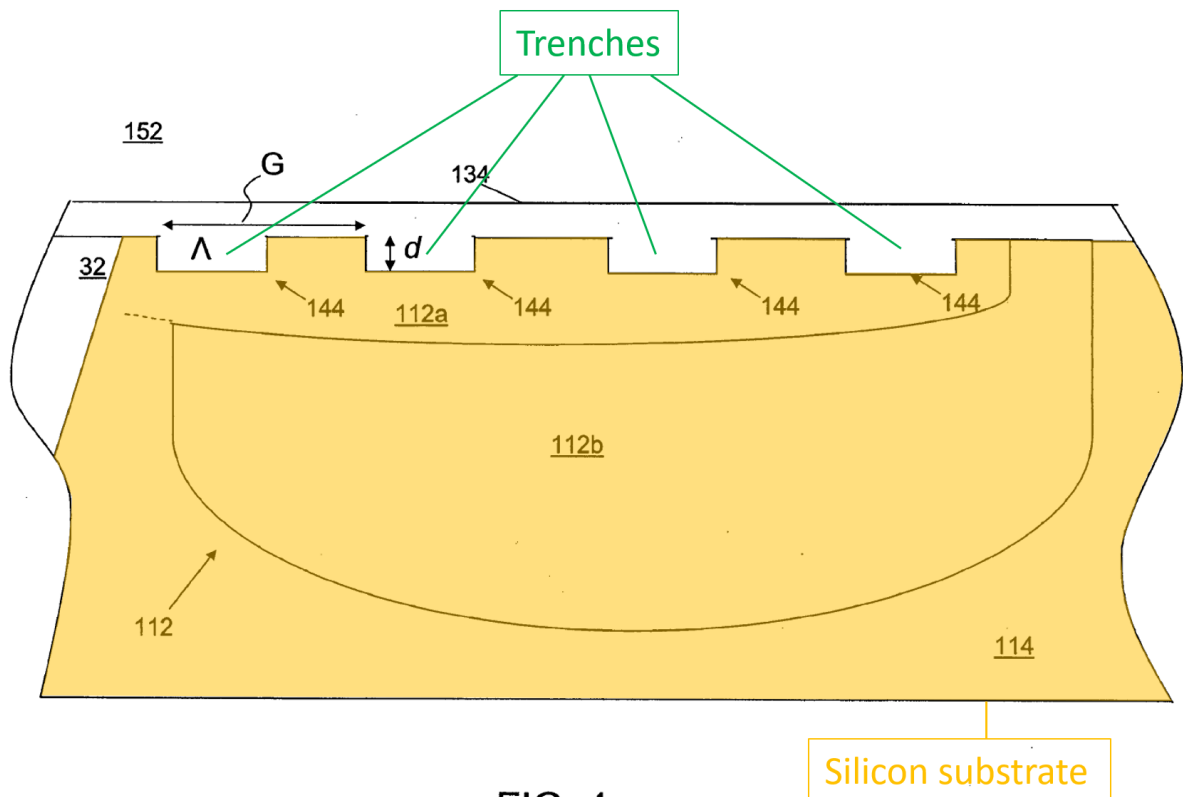


FIG. 4

Baggenstoss, Fig. 4 (annotated).

65. In another embodiment, Baggenstoss discloses an optoelectronic device with a textured region in the form of “blazed (or step-wise)” gratings formed of trenches (elements 244 in Figure 11, below). Baggenstoss, [0042].

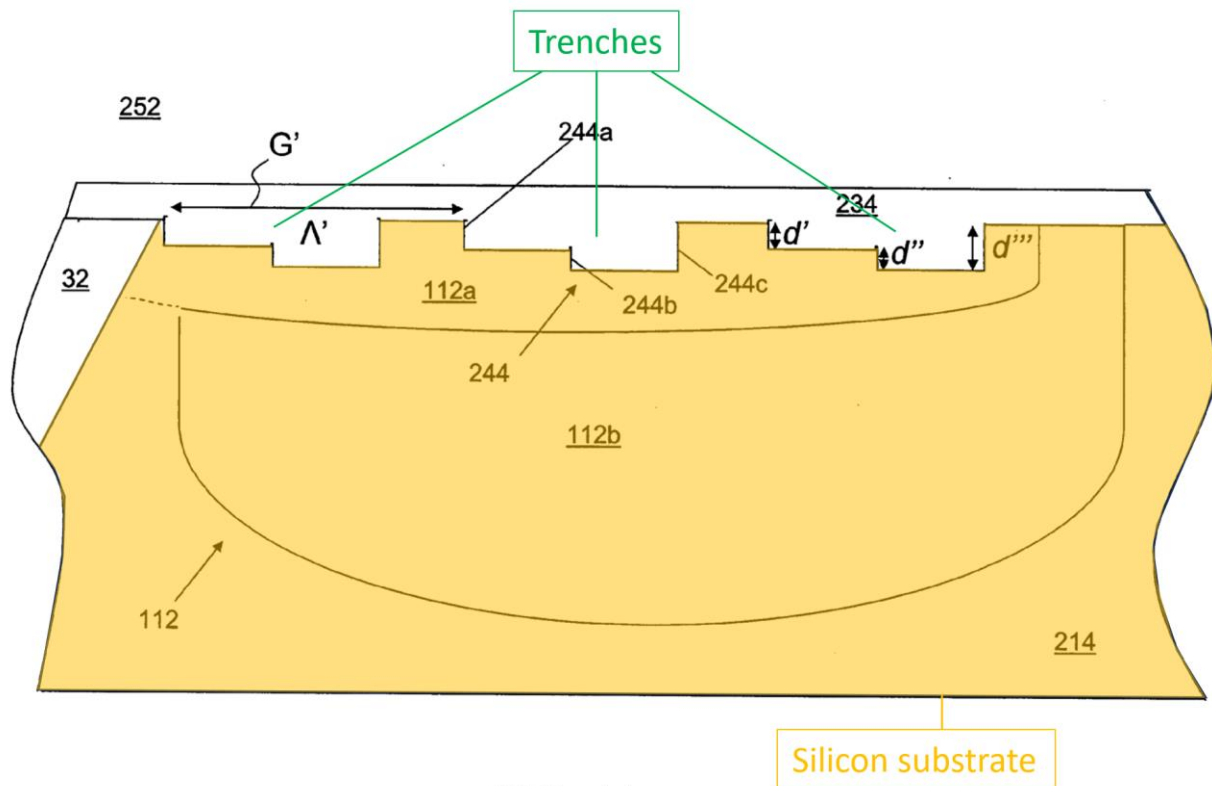


FIG. 11

Baggenstoss, Fig. 11 (annotated).

66. Baggenstoss's grated interface is located on the light incident side of a silicon substrate. Baggenstoss, Fig. 3, [0008]. Baggenstoss teaches that its "grated interface allows a greater percentage of incident light to be captured, which is a vast improvement over the art." Baggenstoss, [0014].

C. Alie (Ex-1006)

67. I understand that Alie is prior art because it was published on March 22, 2012, which is more than one year before the '682 patent's provisional application filing date of June 29, 2013.

68. Alie was not listed in an IDS and was not discussed during prosecution.

69. The '682 patent incorporates by reference—but does not claim priority to—Alie's patent application, referring to Alie for "[f]urther details regarding substrates, bonding, and various imager details." '682 patent, 7:21-24. Like the '682 patent, Alie discloses an optoelectronic device having a textured region with surface features on the light incident side of a semiconductor layer, including to provide additional scattering of incident light. Alie, [0094]. Like the textured region of the '682 patent, Alie's textured region includes surface features in the shapes of "cones, pillars, pyramids, microlenses, quantum dots, inverted features, gratings, protrusions, sphere-like structures, and the like." Alie, [0068]. Alie's "textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device." Alie, [0068].

70. Figure 5 depicts an example optoelectronic device with a textured region
36. Alie, [0096].

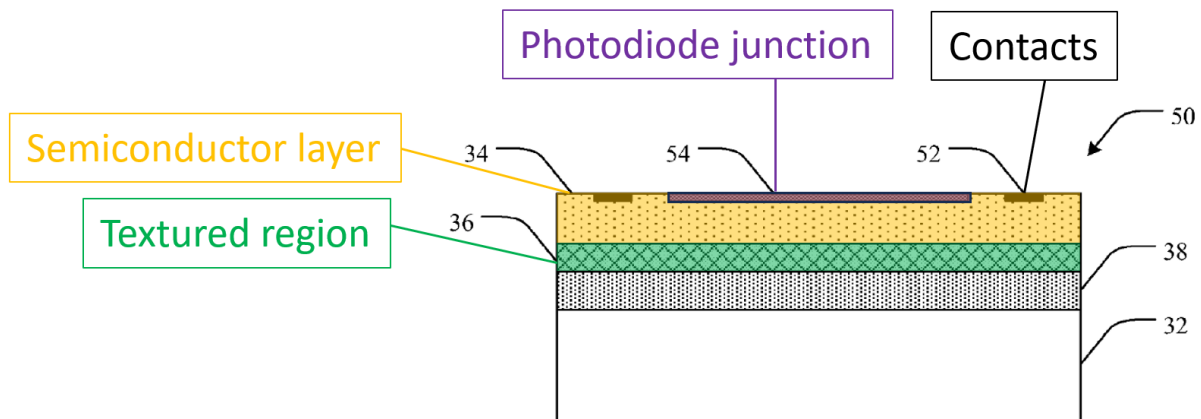


FIG. 5

Alie, Fig. 5 (annotated).

71. Like the '682 patent, Alie discloses that its devices can be adapted for either an FSI architecture or a BSI architecture. Alie, [0053] (“in addition to backside illuminated, front side illuminated architectures are also contemplated to be within the present scope”). When the Figure 5 device is adapted for an FSI architecture, incident light would enter from the top (where photodiode junction 54 is located), similar to the FSI device depicted in Figure 2 of the '682 patent. Alie discloses that a textured forward scattering layer can be added “on the side of the device that receives incident electromagnetic radiation” for additional scattering of incident light. Alie, [0094].

72. When the Figure 5 device is adapted for a BSI architecture, incident light would enter from the bottom (the opposite side of where photodiode junction 54 is located), similar to the BSI device depicted in Figure 3 of the '682 patent.

D. Haddad204 (Ex-1009)

73. I understand that Haddad204 is prior art because it was published on December 13, 2012, which predates the '682 patent's provisional application filing date of June 29, 2013.

74. Although Haddad204 was listed in an IDS along with almost 900 other documents, it was not discussed during prosecution.

75. The named inventors of the '682 patent, Homayoon Haddad and Jutao Jiang, are also joint inventors of Haddad204. Like the '682 patent, Haddad204 discloses an optoelectronic device with a textured region including surface features. Haddad204, [0073], [0053]. In particular, Haddad204 discloses “a plurality of pillars of variable sizes ... arranged in a non-uniform array.” Haddad204, [0112]. Figure 9a shows a top view and Figure 9b shows a cross-sectional view of such “pillars etched into a semiconductor material.” Haddad204, [0112].

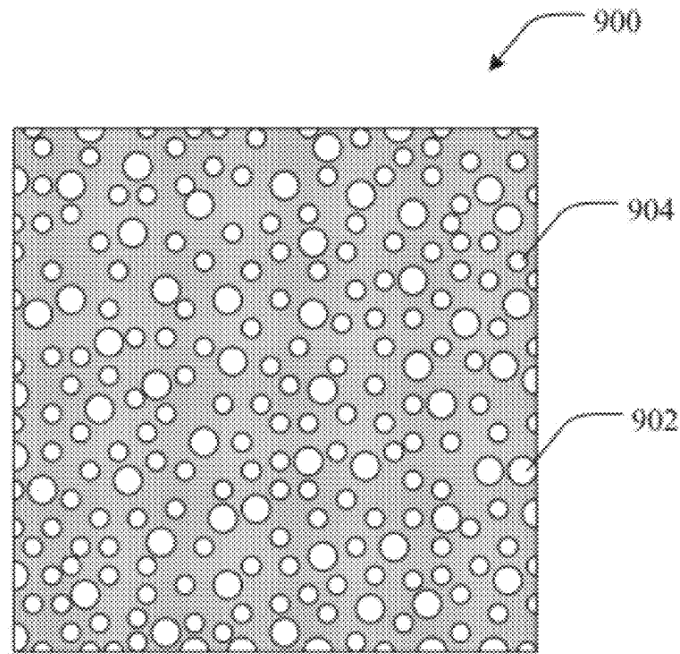


FIG. 9a

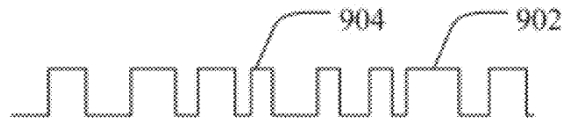


FIG. 9b

Haddad204, Figs. 9a-b.

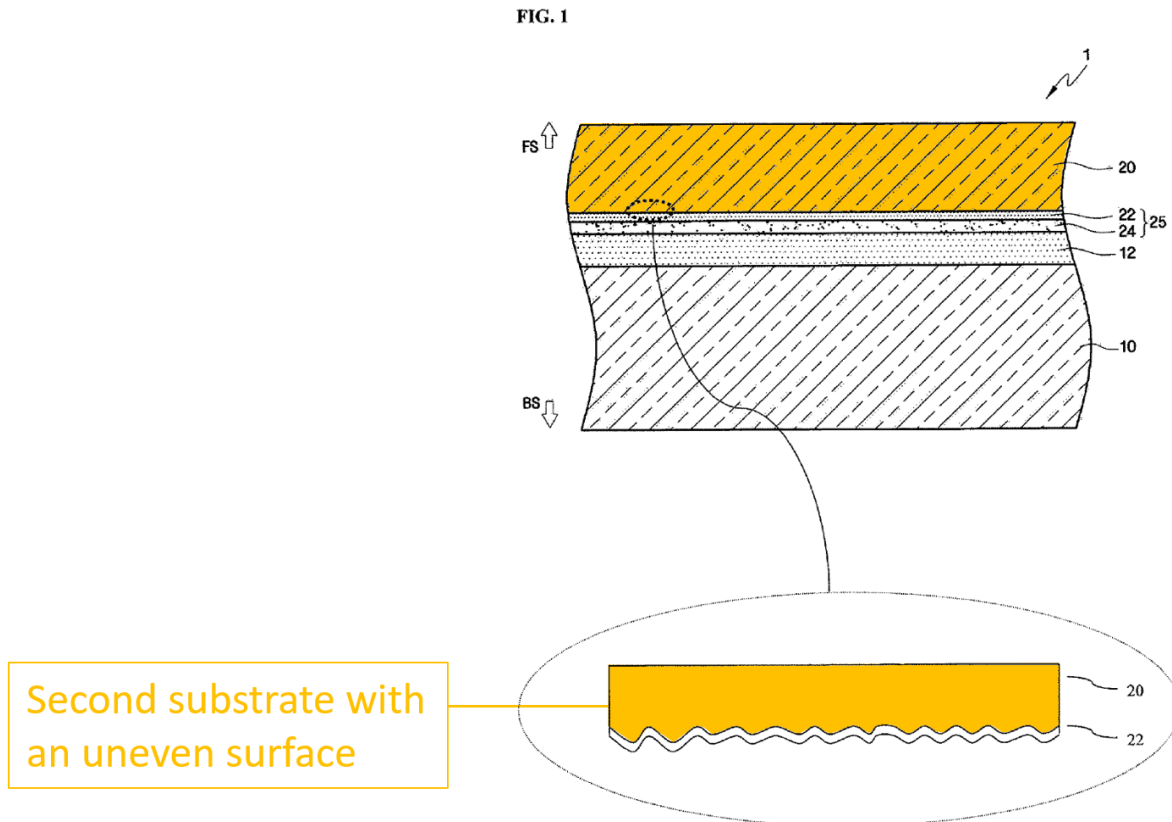
76. Haddad204 discloses that textured regions can be placed on both sides of a semiconductor layer. Haddad204, [0111] (disclosing that in addition to texturing the side opposite the light incident side, “texturing can be applied to the light-incident surface of the semiconductor substrate in order to facilitate additional scattering as light enters the device”).

E. Park (Ex-1010)

77. I understand that Park is prior art because it was published on January 14, 2010, which is more than one year before the '682 patent's provisional application filing date of June 29, 2013.

78. Park was not listed in an IDS and was not discussed during prosecution.

79. Like the '682 patent, Park discloses an optoelectronic device with a textured region including surface features. Park, [0072], [0059].



Park, Fig. 1.

80. Park's uneven surface is located on the light incident side of a semiconductor layer. Park, Figs. 1 & 7. Park teaches that the uneven surface helps with absorbing incident light by reducing reflection. Park, [0072].

VIII. CLAIMS ANALYSIS

A. Ground A-1: Claims 1-3, 6-8, 11-12, 15-18, 21, and 26-27 Are Anticipated, or at a Minimum, Obvious Based on Haddad138

1. Claim 1

a) 1[pre]: “An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:”

81. Haddad138 discloses the preamble to the extent it is limiting.

82. Haddad138 discloses “photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation.” Haddad138, [0045]. Haddad138 explains that its devices have an enhanced ability to absorb electromagnetic radiation compared to “[t]raditional silicon photodetecting imagers [that] have limited light absorption/detection properties.” Haddad138, [0044]. Specifically, Haddad138 discloses a device with a textured region, Haddad138, [0087], which “can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to *absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.*” Haddad138, [0063];¹ see also Haddad138, [0070] (“the

¹ All emphases in quotes have been added, unless otherwise stated.

textured surface can *increase the probability of incident radiation being absorbed by the semiconductor material*").

- b) 1[a]: “a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,”

83. Haddad138 discloses this limitation.

84. Figure 9 depicts a photosensitive pixel device containing a semiconductor substrate 72 (i.e., the claimed semiconductor layer) having multiple doped regions 74 and 76. Haddad138, [0084].

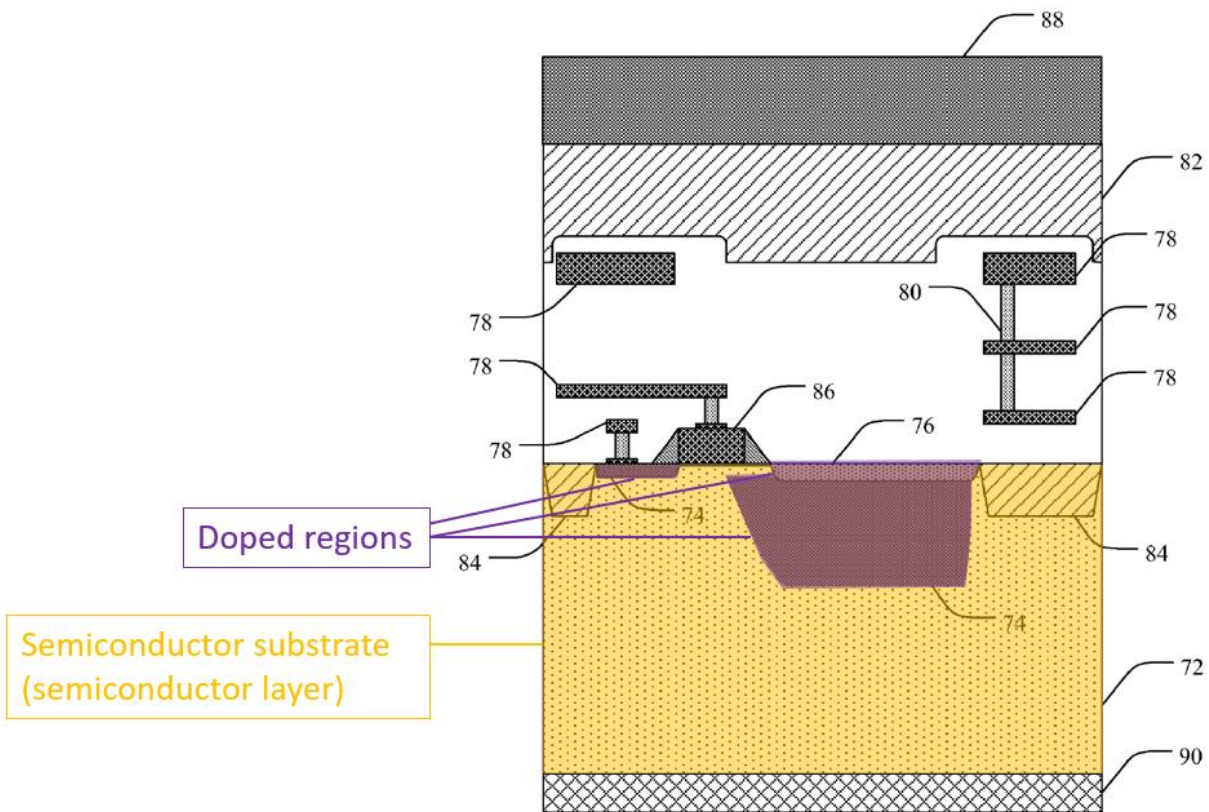


FIG. 9

Haddad138, Fig. 9 (annotated).

85. As shown in Figure 9, the doped regions form at least one junction. As an engineering dictionary from IEEE explains, the term “junction” means “[a] region of transition between semiconductor regions of different electrical properties (for example, n-n⁺, p-n, p-p⁺ conductors).” Ex-1018, 598. Haddad138 discloses that “the semiconductor substrate can be negative in polarity, and the doped region and the highly doped region can be doped with p⁺ and n⁻ dopants respectively.” Haddad138, [0084]. Haddad138 also discloses that the doped regions “create a pinned diode.” Haddad138, [0084]. A POSITA would understand that the diode in this context refers to a p-n junction. Ex-1018, 309 (“diode ... in a more restricted usage, a semiconductor device that has the asymmetrical voltage-current characteristic exemplified by a single p-n junction”). Indeed, Haddad138 expressly states that similar doped regions in Figure 1 “form[] at least one junction.” Haddad138, [0049].

86. As depicted in Figure 9, the semiconductor substrate 72 has a top surface and a bottom surface, which correspond to the claimed light incident side and the opposed side. The surface corresponding to the claimed light incident side depends on whether the Figure 9 device is adapted for an FSI configuration (in which case the top surface is the light incident side) or for a BSI configuration (in which case the bottom surface is the light incident side), as discussed above in Section VII.A.

- c) **1[b]: “a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,”**

87. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious.

- (1) “a textured region comprising a plurality of shallow trench isolation surface features”**

88. Haddad138 discloses a textured region having surface features (i.e., the claimed shallow trench isolation surface features). Haddad138, [0063]. Haddad138’s surface features have the same structures as the shallow trench isolation surface features described in the specification of the ’682 patent. Haddad138 discloses that “nonlimiting examples of [surface feature morphologies] include cones, pillars, pyramids ... inverted features, and combinations thereof.” Haddad138, [0006]. These are the same shapes and configurations that the ’682 patent provides as examples of shallow trench isolation surface features. ’682 patent, 9:34-37 (“Non-limiting examples of such shapes and configurations include cones, pillars, pyramids, inverted features ... and the like, including combinations thereof.”); *see also* ’682 patent, cl. 12 (“shallow trench isolation surface features comprise pyramids”). Haddad138 also discloses that its surface features can have a height of “50 nm to 20 μ m,” Haddad138, [0070], just like the surface features of the ’682 patent, ’682 patent, cl. 11.

89. Both Haddad138 and the '682 patent describe the same or similar processes for creating the shallow trench isolation surface features. Haddad138 discloses forming surface features using “chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, and combinations thereof.” Haddad138, [0006]. These are the same methods used to create shallow trench isolation surface features in the '682 patent, as explained in the provisional application for the '682 patent. Ex-1003, 11:16-22 (“Various methods can be utilized to form shallow trench isolation features.... Non-limiting examples can include chemical etching (e.g. anisotropic etching, isotropic etching) ... nanoimprinting, material deposition....”).

90. Both Haddad138 and the '682 patent explain that their shallow trench isolation surface features serve the same function. Just as the '682 patent states that its “surface features of the textured layer ... facilitate an increase [in] the effective optical path length of the semiconductor layer,” '682 patent, 9:29-31, Haddad138 discloses that its “textured region can include surface features to increase the effective absorption length of the photosensitive pixel,” Haddad138, [0063].

91. Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the surface features and the shallow trench isolation in Haddad138. Haddad138

discloses forming shallow trench isolation. Haddad138, [0085]. The process for creating shallow trench isolation was well known. It involves forming trenches that isolate individual transistors, photodiodes, and other components of a semiconductor device. This isolation is crucial to prevent electrical or optical interference. Because shallow trench isolation offers high-quality isolation with less space compared to older methods like LOCOS (local oxidation of silicon), it is especially useful in high density, modern CMOS technology. It would have been obvious to use the same process to form both the shallow trench isolation and the surface features in Haddad138, or to form both structures in the same manufacturing step. Ex-1034, [0010]-[0012] (disclosing using a shallow trench isolation process to form surface features). Creating the surface features using the same process as the process for the shallow trench isolation would generate predictable results, and reduce the costs associated with developing a new process. This would involve employing a known technique to improve similar devices in the same way. A POSITA would have had a reasonable expectation of success because Haddad138 already discloses using shallow trench isolation in its devices, and it was well known how to use a shallow trench isolation process to form surface features. Haddad138, [0066], [0085]; Ex-1034, [0010]-[0012]. For example, Haddad138 discloses forming surface features “using deep trench isolation and etching techniques.” Haddad138, [0066]. Another prior art publication

also discloses using a shallow trench isolation (STI) process to create a surface grating made of trenches filled with field oxide. Ex-1034, [0010]-[0012].

(2) “located on the light incident side of the semiconductor layer”

92. Haddad138 discloses, or at a minimum, renders obvious locating the claimed shallow trench isolation surface features on the light incident side of the semiconductor layer. Figure 9 depicts a textured region 90 having surface features. Haddad138, [0087], [0063].

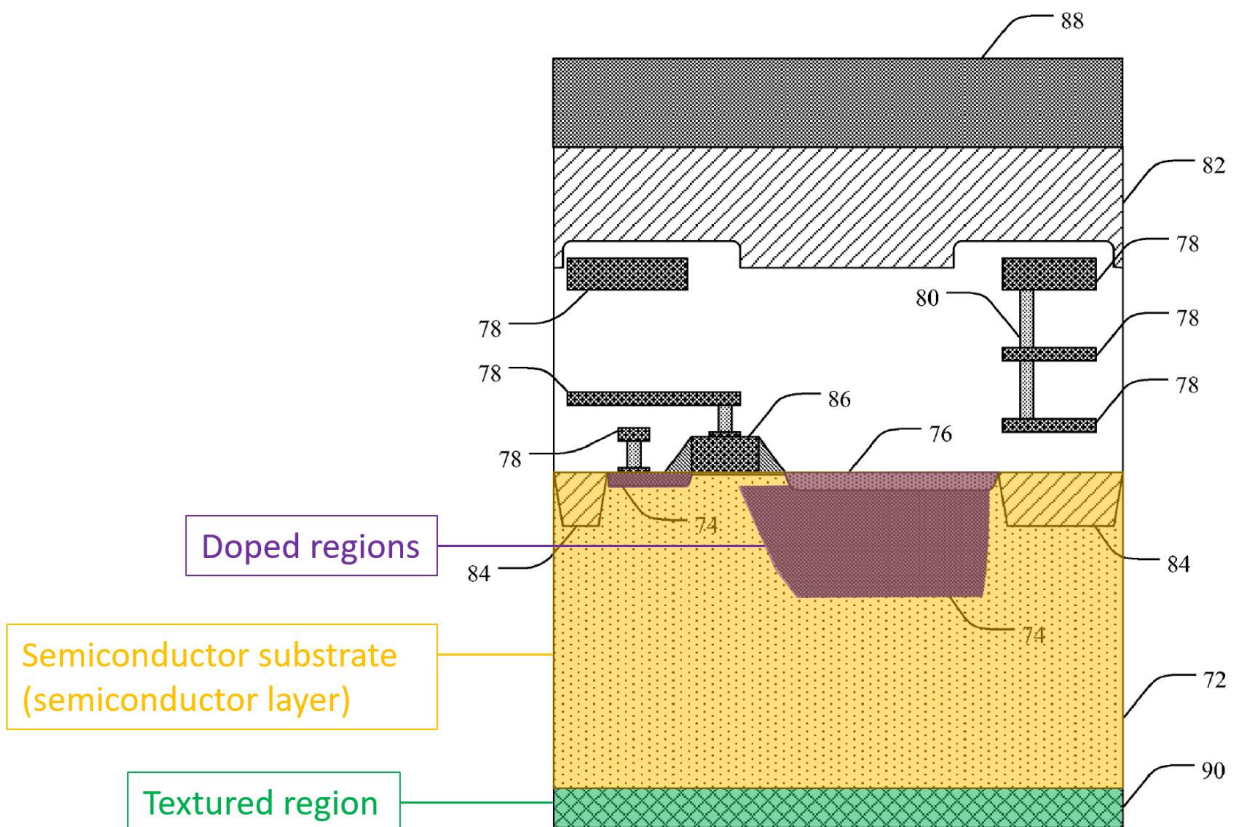


FIG. 9

Haddad138, Fig. 9 (annotated).

93. Haddad138 discloses that its devices “can be adapted for either [FSI or BSI] configuration.” Haddad138, [0048]. Haddad138 illustrates such adaptations with reference to Figure 1, which depicts a semiconductor substrate 12 and a textured region 18, similar to the semiconductor substrate and textured region depicted in Figure 9. Haddad138 explains that the Figure 1 device is “a FSI design where light enters the semiconductor substrate from the direction of the multiple doped regions.” Haddad138, [0049]. In other words, in an FSI configuration, incident light would enter the Figure 1 device from the top.

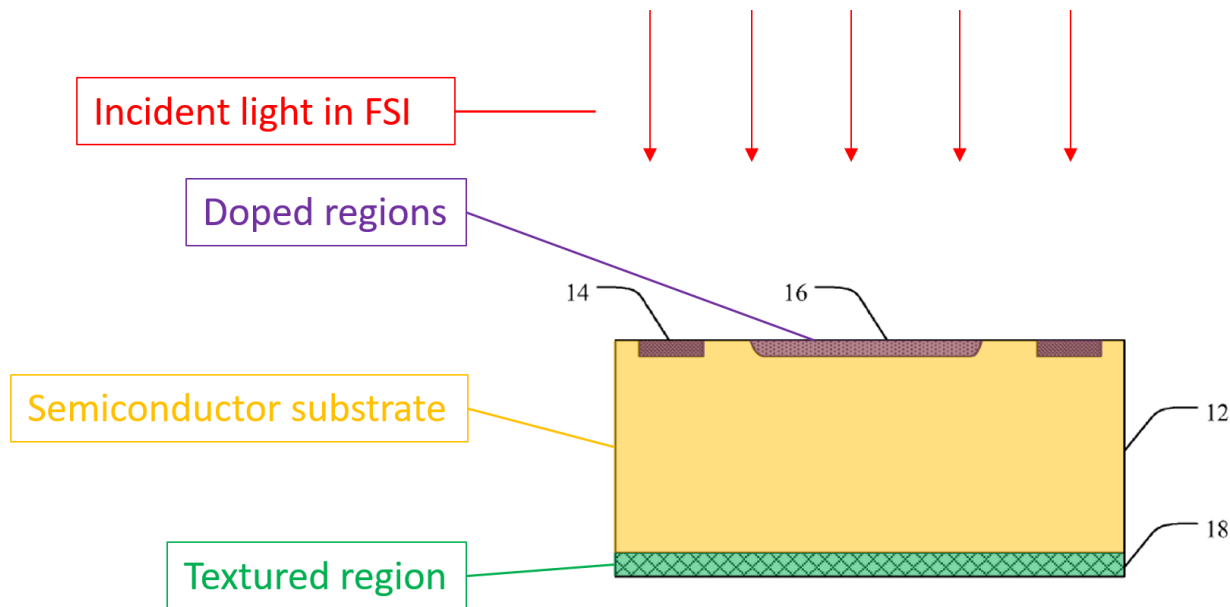
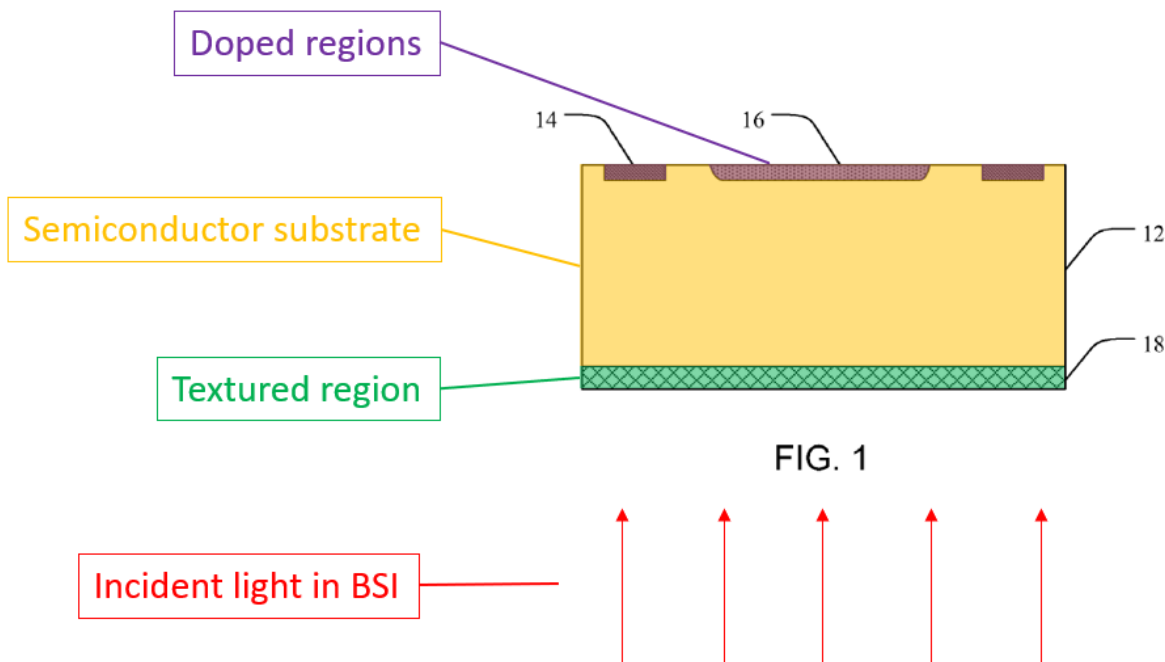


FIG. 1

Ex-1012, Fig. 1 (annotated and modified to show incident light).

94. Haddad138 teaches, however, that the Figure 1 device “can be configured with a BSI architecture, and thus *electromagnetic radiation would enter the*

semiconductor substrate from the direction of the textured region.” Haddad138, [0049]. In other words, in a BSI configuration, incident light would enter the Figure 1 device from the bottom.

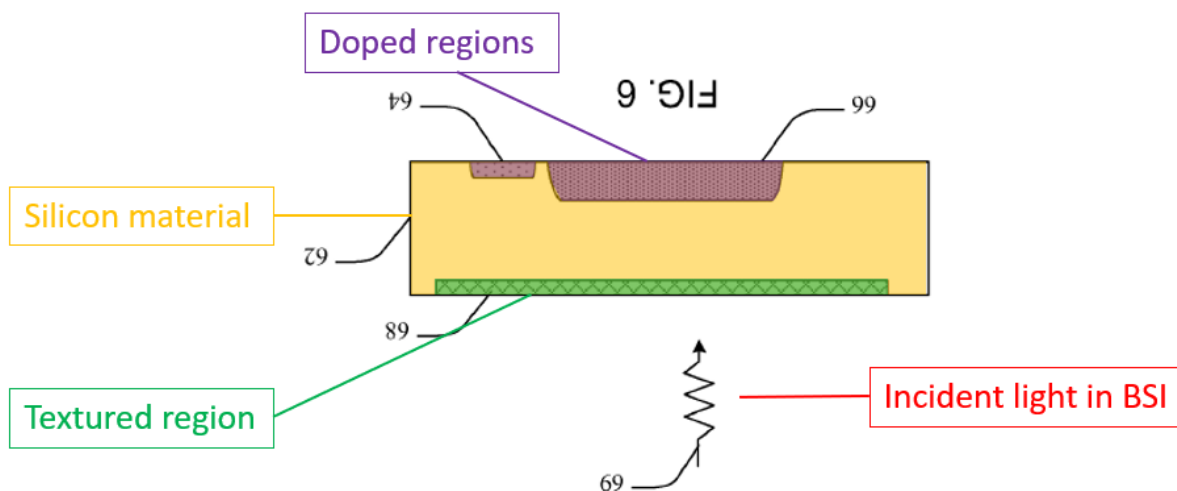


Ex-1012, Fig. 1 (annotated and modified to show incident light).

95. Similarly, when the Figure 9 device is adapted for a BSI configuration (as Haddad138 discloses), incident light would enter the device from the direction of the textured region, i.e., the bottom side. In a BSI configuration of the Figure 9 device, therefore, the surface features of the textured region 90 correspond to the claimed shallow trench isolation surface features located on the light incident side of the semiconductor layer. In this configuration, the textured region located on the light incident side would enable tuning the travel path of incident light. Haddad138, [0079]. One of Haddad138’s provisional applications, to which Haddad138 claims priority and

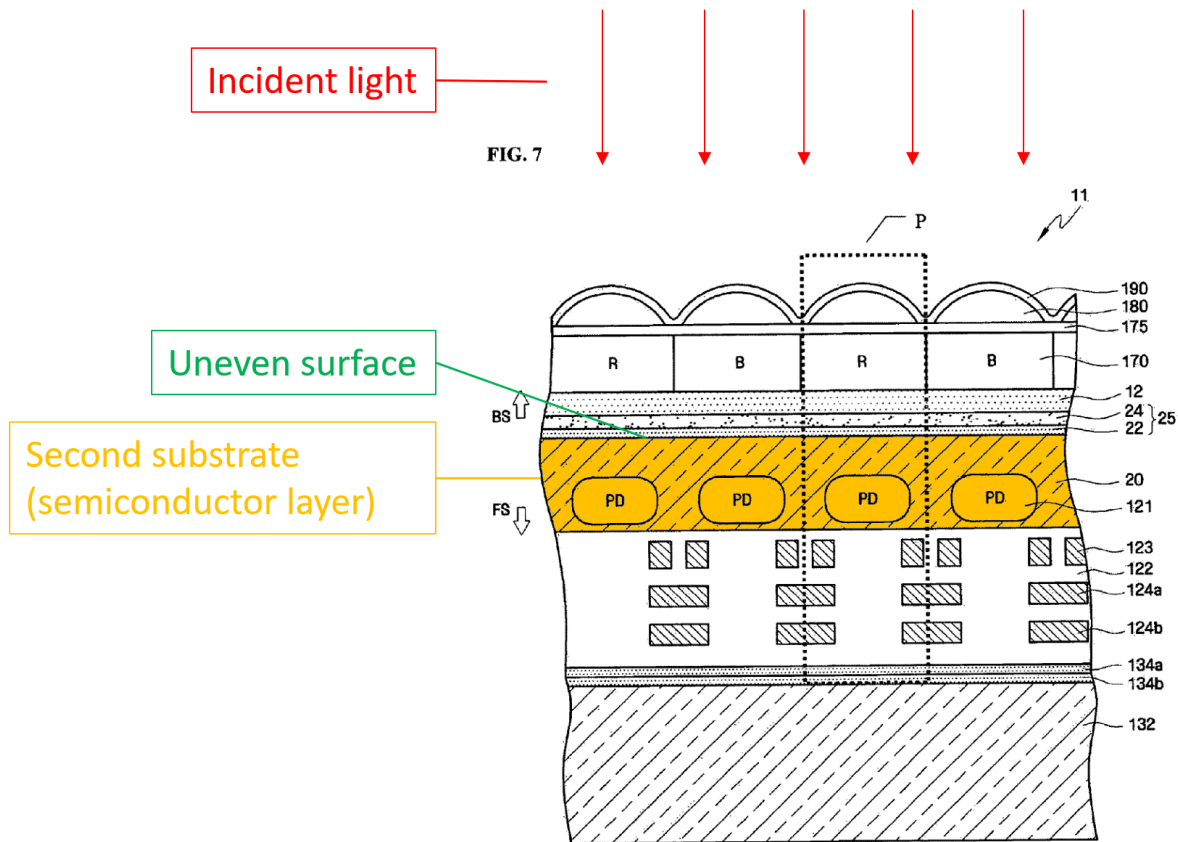
incorporates by reference, also explains that a textured region located on the light incident side can “enhance the absorption properties by reducing the amount of incident electromagnetic radiation that is reflected from the device.” Haddad138-Provisional434, 5.

96. Such BSI devices having a textured region on the light incident side were commonplace. For example, another prior art publication also depicts an example of a BSI device having a textured region on the light incident side. Ex-1024, [0077].



Ex-1024, Fig. 6 (annotated and rotated 180 degrees).

97. Samsung’s own prior art publication also depicts a BSI device having a textured region on the light incident side. Ex-1010, [0059], [0072].



Ex-1012, Fig. 7 (annotated and modified to show incident light).

(3) “configured to interact with incident electromagnetic radiation”

98. Haddad138 discloses that its textured region is “positioned to interact with electromagnetic radiation.” Haddad138, [0003], [0049]. Specifically, Haddad138 discloses that the textured region “can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation.” Haddad138, [0063]. Haddad138 discloses that this interaction is facilitated by surface

features of the textured region, i.e., the surface features are configured to interact with incident electromagnetic radiation. Haddad138, [0063].

d) 1[c]: “a support substrate coupled to said semiconductor layer, and”

99. Haddad138 discloses this limitation.

100. Figure 9 depicts a carrier support substrate 88 (i.e., the claimed support substrate) coupled to a semiconductor substrate 72 (i.e., the claimed semiconductor layer) via a passivation layer 82 and a metallization layer containing metal regions 78. Haddad138, [0086]-[0088].

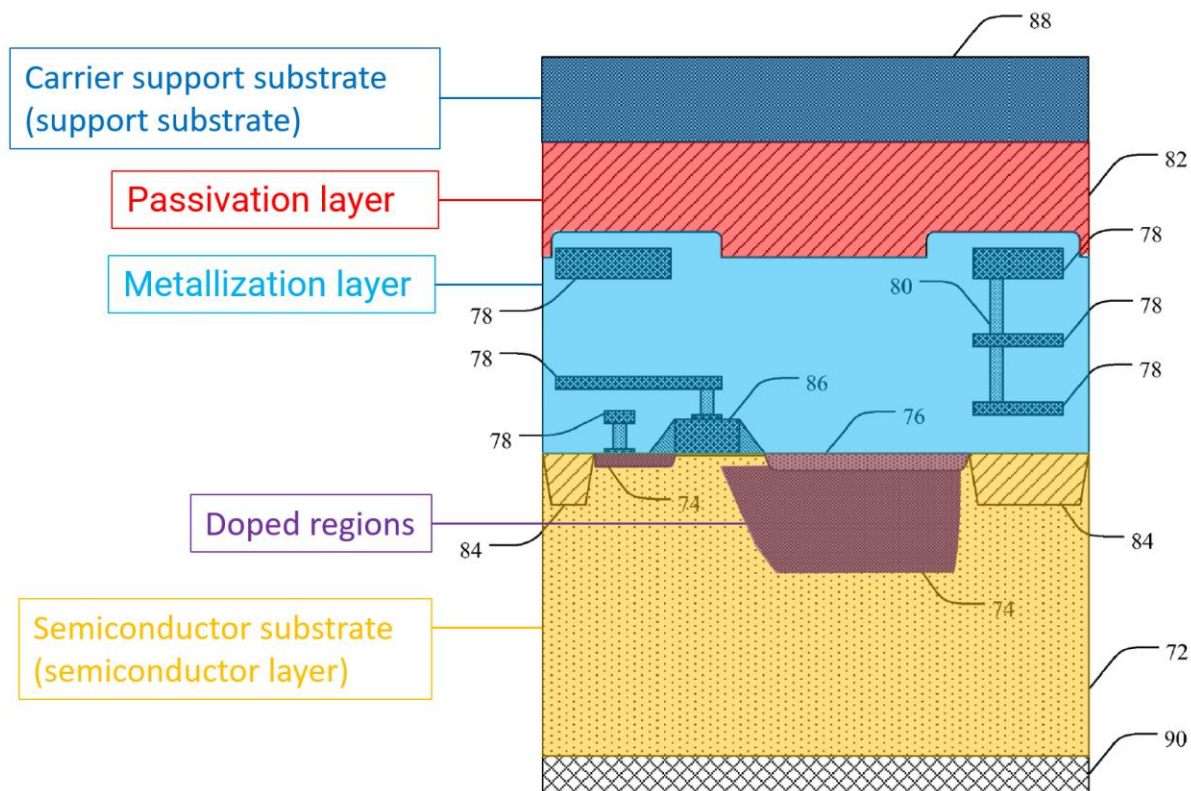


FIG. 9

Haddad138, Fig. 9 (annotated).

101. Haddad138 teaches that the support substrate 88 may be present in the optoelectronic device upon completion of manufacturing. Indeed, Figures 10 and 11 disclose alternatives to the Figure 9 embodiment in which a second carrier support substrate is added or the substrate is removed, respectively. Haddad138, [0088] (“As is shown in FIG. 10, an additional carrier support substrate 100 *can* be coupled.... A reflective layer 102 *can* be disposed....”), [0089] (“As is shown in FIG. 11, the carrier support substrate *can* be removed”). Thus, a POSITA would understand that, in at least some embodiments, Haddad138’s device would include the support substrate.

e) 1[d]: “a first bonding layer disposed between the semiconductor layer and the support substrate,”

102. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious.

103. Haddad138 discloses that “[t]he carrier substrate can be coupled to the photosensing pixel [including the semiconductor layer] by various techniques” including “by way of a bonding layer” (i.e., the claimed first bonding layer). Haddad138, [0086]. One of Haddad138’s provisional applications, to which Haddad138 claims priority and incorporates by reference, illustrates such a bonding layer. Haddad138-Provisional004, 4-5.

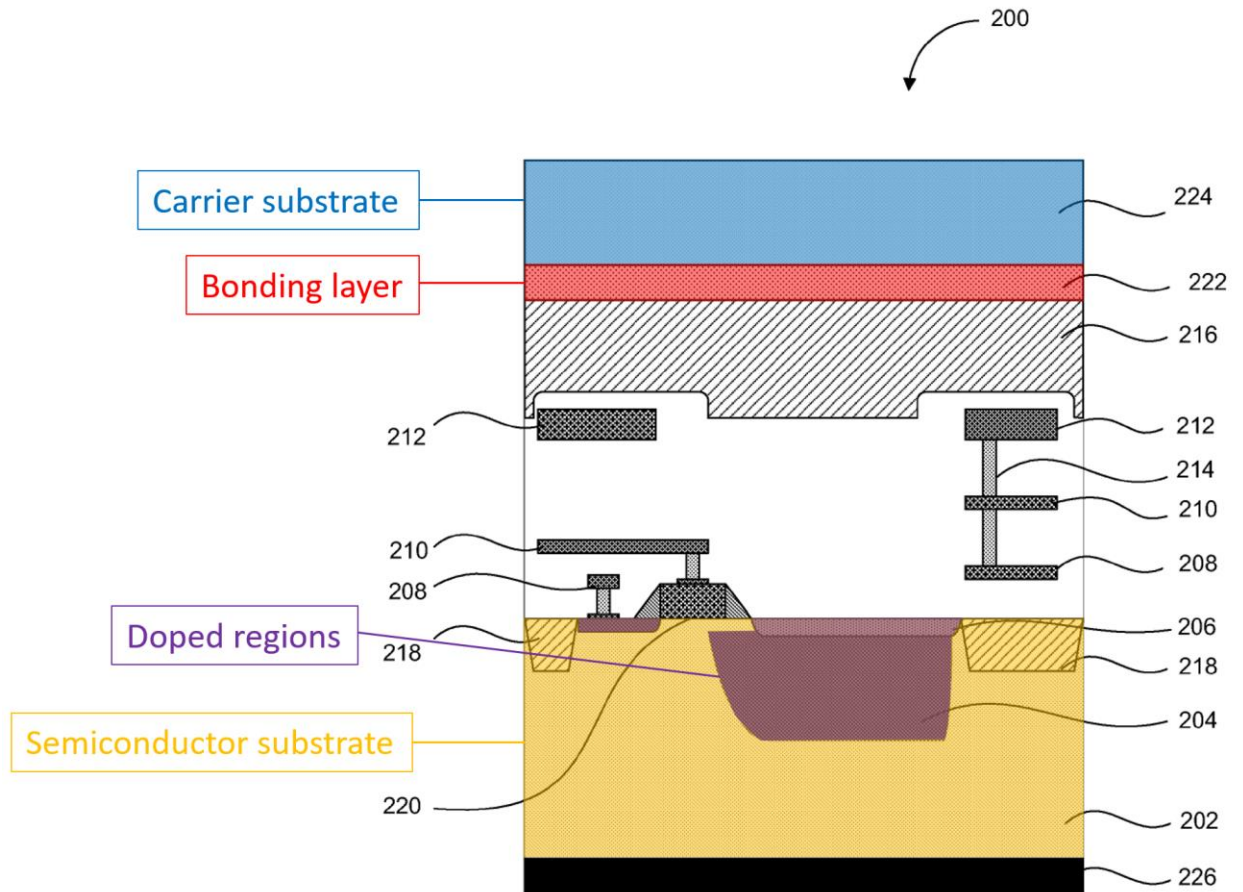


FIG. 4

Haddad138-Provisional004, Fig. 4 (annotated).

f) 1[e]: “wherein said optoelectronic device is a photosensitive imager device capable of detecting visible and infrared electromagnetic radiation.”

104. Haddad138 discloses this limitation under both Petitioner’s and Patent Owner’s proposed constructions in the 737 Case.

105. The preamble of claims 1 and 32 of the ’737 patent has the same recitation of this limitation, “a photosensitive imager device capable of detecting visible and

infrared electromagnetic radiation.” In the 737 Case, Petitioner proposed that the preamble of claims 1 and 32 of the ’737 patent is limiting and means, “An image sensor pixel capable of detecting visible and infrared electromagnetic radiation.” Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning, and that to the extent a construction is required, it means, “A device with multiple pixels arranged to capture an image from visible and/or infrared light.” Ex-1014, 3-4.

106. Haddad138 discloses an image sensor pixel capable of detecting visible and infrared electromagnetic radiation. Haddad138 discloses “pixels ... capable of detecting visible as well as infrared electromagnetic radiation.” Haddad138, [0045]. Haddad138 discloses that its pixels are incorporated into an “imaging array,” i.e., they are image sensor pixels. Haddad138, [0064]; *see also* Haddad138, [0079] (disclosing “4 pixel imagers”), [0095] (“multiple pixels can be associated together to form an imager”).

107. As discussed above, Haddad138 also discloses a device with multiple pixels arranged to capture an image from visible and/or infrared light. Haddad138, [0045], [0064], [0079], [0095].

2. Claim 2

a) **“The device of claim 1, wherein the semiconductor layer is single crystal silicon.”**

108. Haddad138 discloses this limitation.

109. Haddad138 discloses that “[a] variety of semiconductor materials are contemplated for use,” including “monocrystalline silicon” (i.e., the claimed single crystal silicon). Haddad138, [0052].

3. Claim 3

a) **“The device of claim 1, wherein the shallow trench isolation surface features are formed in the semiconductor layer.”**

110. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious.

111. As discussed above for limitation 1[b], Haddad138’s surface features correspond to the claimed shallow trench isolation surface features.

112. Haddad138 discloses that “the textured region can be positioned on a surface of the semiconductor substrate.” Haddad138, [0005]. For a textured region to be positioned on a surface of the semiconductor substrate, the surface of the semiconductor substrate would need to be textured, i.e., the shallow trench isolation surface features are formed in the semiconductor layer. This understanding is consistent with the teaching of one of Haddad138’s provisional applications that a light diffusing region (i.e., a textured region) can be “***formed in*** or near the semiconductor substrate” in the “present invention.” Haddad138-Provisional004, 1-2. Haddad138 also discloses chemically and/or structurally altering “the surface of the semiconductor

material” to form “surface features appearing as microstructures or patterned areas on the surface.” Haddad138, [0070].

4. Claim 6

- a) “The device of claim 1, further comprising a device layer coupled to the semiconductor layer on said side opposed to the light incident side.”**

113. Haddad138 discloses this limitation.

114. Figure 9 depicts a layer containing metal regions 78 (i.e., the claimed device layer) coupled to the top surface of the semiconductor substrate 72 (i.e., the claimed semiconductor layer). Haddad138, [0084]-[0085].

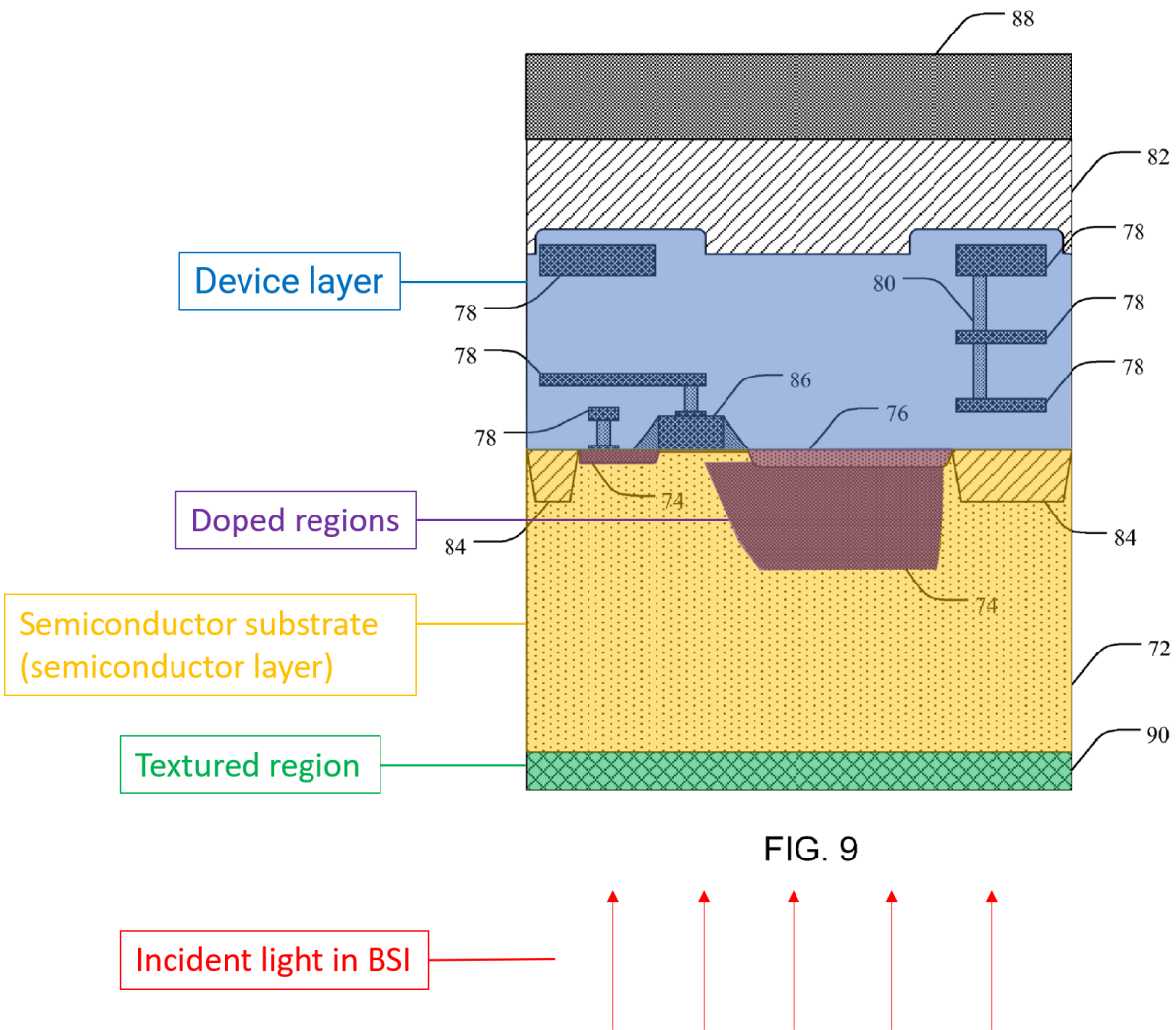


FIG. 9

Haddad138, Fig. 9 (annotated and modified to show incident light). The provisional application to the '682 patent refers to such a metallization layer as a device layer. Ex-1003, Fig. 3.

115. As discussed above in Section VII.A, in a BSI configuration, incident light enters the device from the bottom. See Haddad138, [0048]-[0049]. In this configuration, the bottom surface of the semiconductor substrate 72 corresponds to the claimed light incident side of the semiconductor layer, and the top surface (to which

the device layer is coupled) corresponds to the claimed side opposed to the light incident side.

5. **Claim 7**

- a) **“The device of claim 1, wherein said first bonding layer comprises any of silicon oxide, silicon nitride and amorphous silicon.”**

116. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious.

117. As discussed above regarding limitation 1[d], Haddad138 discloses a bonding layer that is disposed between the semiconductor layer and the support substrate. It would have been obvious to use silicon oxide or silicon nitride as the bonding layer because they can be easily polished and bonded. Ex-1026, 228 (“Materials that are too rough or difficult to polish may be covered by process-compatible intermediate layers such as spun-on or chemical vapor-deposited **silicon dioxide or silicon nitride, which may be easily polished and bonded.**”).

118. It would have been obvious to apply the known technique of using silicon oxide or silicon nitride as bonding layers to Haddad138’s device to yield predictable results. Silicon oxide and silicon nitride were routinely used as bonding layers. Ex-1026, 216 (“SOI [silicon-on-insulator] structures consist of a thin, top layer of single-crystal silicon, a layer of silicon dioxide (SiO₂), and a silicon handle substrate that acts as mechanical support.”); Ex-1027, [0032] (“The bonding layer 9 is, for example,

formed of at least any one of a silicon oxide film (SiO_2), a silicon nitride film (SiN_x)

... as a single layer or a plurality of stacked layers.”); Ex-1028, 317. The use of silicon oxide and silicon nitride would have yielded predictable results because they were commonly used in semiconductor manufacturing and their properties were well known. Ex-1026, 228; Ex-1020, 155-162.

119. A POSITA would have had a reasonable expectation of success. It would have been well within the abilities of a POSITA to use silicon oxide and silicon nitride because the methods of manufacturing them were well known and involved routine semiconductor manufacturing steps. Ex-1020, 155-162.

6. Claim 8

- a) **“The device of claim 1, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.”**

120. Haddad138 discloses this limitation.

121. Haddad138 discloses a semiconductor material (i.e., the claimed semiconductor layer) with “a thickness of from about 1 μm to about 10 μm .” Haddad138, [0055].

7. Claim 11

- a) **“The device of claim 1, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.”**

122. Haddad138 discloses this limitation.

123. Haddad138 discloses that “the [surface] features or microstructures can be on the order of 50 nm to 20 μ m in size.” Haddad138, [0070]. More specifically, Haddad138 discloses that “a surface can be ***several hundred nanometers*** thick,” which is within the claimed range. Haddad138, [0032].

8. Claim 12

a) “The device of claim 1, wherein said shallow trench isolation surface features comprise pyramids.”

124. Haddad138 discloses this limitation.

125. Haddad138 discloses that “[t]he surface features can be ... pyramids.” Haddad138, [0063]; *see also* Haddad138, [0066].

9. Claim 15

a) “The device of claim 1, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.”

126. Haddad138 discloses this limitation.

127. Haddad138 discloses its devices have an enhanced ability to absorb electromagnetic radiation compared to “[t]raditional silicon photodetecting imagers [that] have limited light absorption/detection properties.” Haddad138, [0044]. Specifically, Haddad138 discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to ***absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.***”

Haddad138, [0063]; *see also* Haddad138, [0070] (“the textured surface can ***increase the probability of incident radiation being absorbed by the semiconductor material***”).

10. Claim 16

- a) **“The device of claim 1, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.”**

128. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious.

129. One of Haddad138’s provisional applications, to which Haddad138 claims priority and incorporates by reference, discloses that the “net result” of using its light diffusing regions (i.e., the claimed textured regions) is “the photosensing pixel can absorb light having a wavelength in the range of about 400nm to about 1200nm,” which includes the claimed range of about 700 nm to about 1100 nm. Haddad138-Provisional004, 6. “This is accomplished by internal reflection and increasing the effective absorption length to be greater than the thickness of the semiconductor substrate.” Haddad138-Provisional004, 6.

130. Moreover, Haddad138 discloses that, unlike “[t]raditional silicon photodetecting imagers” that have trouble detecting “photons having wavelengths longer than approximately 700 nm,” Haddad138, [0044], its devices are “able to absorb longer wavelengths (e.g. >1000 nm for silicon).” Haddad138, [0044].

131. Haddad138 also discloses that its textured region increases optical absorption of “infrared,” Haddad138, [0065], whose wavelength range includes the claimed range of about 700 nm to about 1100 nm. Ex-1029, 807.

132. In sum, because Haddad138 discloses that its textured region increases optical absorption over at least “the range of about 400nm to about 1200nm,” more than “700 nm,” and “infrared,” Haddad138 discloses that its textured region increases optical absorption of the spectrum range “of at least about 700 nm to about 1100 nm,” as required by this limitation. Infrared was known to include at least the range of 700 nm to 2500 nm. Ex-1029, 807 (“The region of the near infrared spectrum extends from about 700 nm ($14,000\text{ cm}^{-1}$) near the end of the visible region, to 2500 nm ($4,000\text{ cm}^{-1}$), which is the beginning of the infrared fundamental region.”).

133. In addition, Haddad138 does not teach away from the claimed range and the claimed range does not produce any new or unexpected result.

11. Claim 17

- a) **“The device of claim 1, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.”**

134. Haddad138 discloses this limitation.

135. Haddad138 discloses that its “textured region can include surface features to increase the effective absorption length of the photosensitive pixel,” i.e., increase the effective optical path length of light as it passes through the semiconductor layer.

Haddad138, [0063]. This result is achieved by the textured region “diffus[ing]” and “redirect[ing]” light within the semiconductor layer. Haddad138, [0063].

12. Claim 18

- a) **“The device of claim 1, wherein said textured region allows the semiconductor layer to experience multiple passes of light.”**

136. Haddad138 discloses this limitation.

137. Haddad138 discloses that its textured region “can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared).” Haddad138, [0065].

13. Claim 21

- a) **“The device of claim 1, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

138. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case.

139. In the 737 Case, Petitioner proposed that the term “the surface features are arranged according to a pattern” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning and that, to the extent a construction is required, it means “features coincident with at least one surface that are arranged in a repeating manner.” Ex-1014, 4.

140. As discussed above for limitation 1[b], Haddad138's surface features correspond to the claimed shallow trench isolation surface features. Haddad138 discloses that the surface features are arranged according to a pattern under Patent Owner's proposed construction in the 737 Case. Haddad138 discloses "surface features appearing as microstructures or ***patterned areas on the surface.***" Haddad138, [0070]. Moreover, Haddad138 discloses forming surface features using nanoimprinting, Haddad138, [0006], which involves using a mold to create imprints on the target material, thus resulting in a formation of features coincident with at least one surface that are arranged in a repeating manner. Ex-1019, 4129. Haddad138 also discloses forming surface features using chemical etching, Haddad138, [0006], which involves the use of a mask that results in the formation of features coincident with at least one surface that are arranged in a repeating manner. *See, e.g.*, Ex-1020, 87; Ex-1011, 8:25-29.

14. Claim 26

a) "The device of claim 1, further comprising deep trench isolation for isolating the device."

141. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious.

142. Figure 9 depicts trench isolation 84. Haddad138, [0084]-[0085].

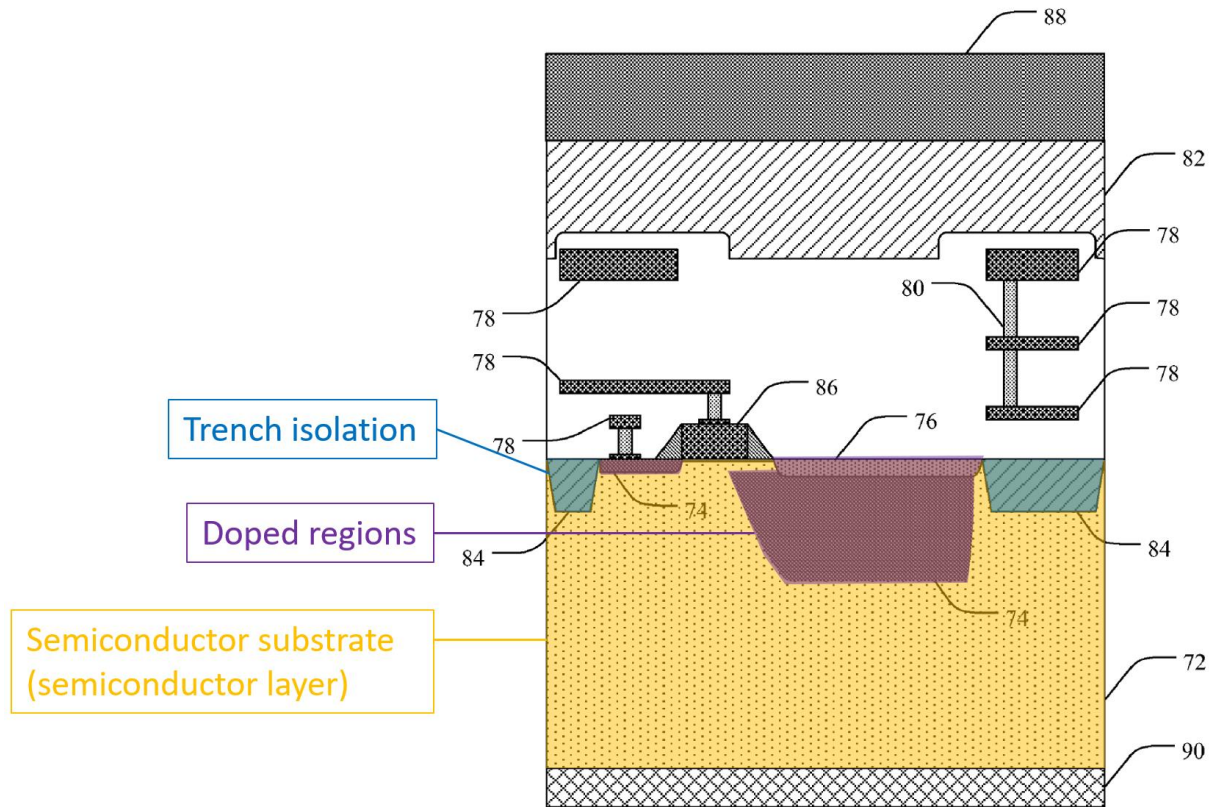


FIG. 9

Haddad138, Fig. 9 (annotated).

143. Haddad138 discloses that the trench isolation can be deep, as required by this limitation. Haddad138, [0085]; *see also* Haddad138-Provisional004, 5 (“The trench isolation can be shallow or deep trench isolation”).

144. Haddad138’s deep trench isolation can reduce optical and electrical crosstalk, i.e., isolate the device, as required by this limitation. Haddad138, [0085]; *see also* Haddad138-Provisional004, 5 (“The isolation layer can be configured to reflect the incident light until it is absorbed, thereby increas[ing] the effective absorption length of the device.”).

15. Claim 27

a) “The device of claim 26, wherein said deep trench isolation provides light trapping functionality.”

145. Haddad138 discloses this limitation.

146. Haddad138’s deep trench isolation can reduce optical crosstalk and “reflect incident light until it is absorbed,” i.e., provide light trapping functionality, as required by this limitation. Haddad138, [0085]; *see also* Haddad138-Provisional004, 5 (“The isolation layer can be configured to reflect the incident light until it is absorbed, thereby increas[ing] the effective absorption length of the device.”).

B. Ground A-2: Claims 4-5, 14, and 21-22 Are Obvious Based on Haddad138 and Baggenstoss

1. The Combination of Haddad138 and Baggenstoss

147. As discussed above regarding limitation 1[b], Haddad138 discloses an optoelectronic device with a textured region. Haddad138, [0084], [0087], [0064]. Haddad138 discloses that its textured region can include surface features. Haddad138, [0063].

148. Similarly, Baggenstoss discloses an optoelectronic device with a grated interface formed by trenches 144. Baggenstoss, [0031]-[0032], [0009].

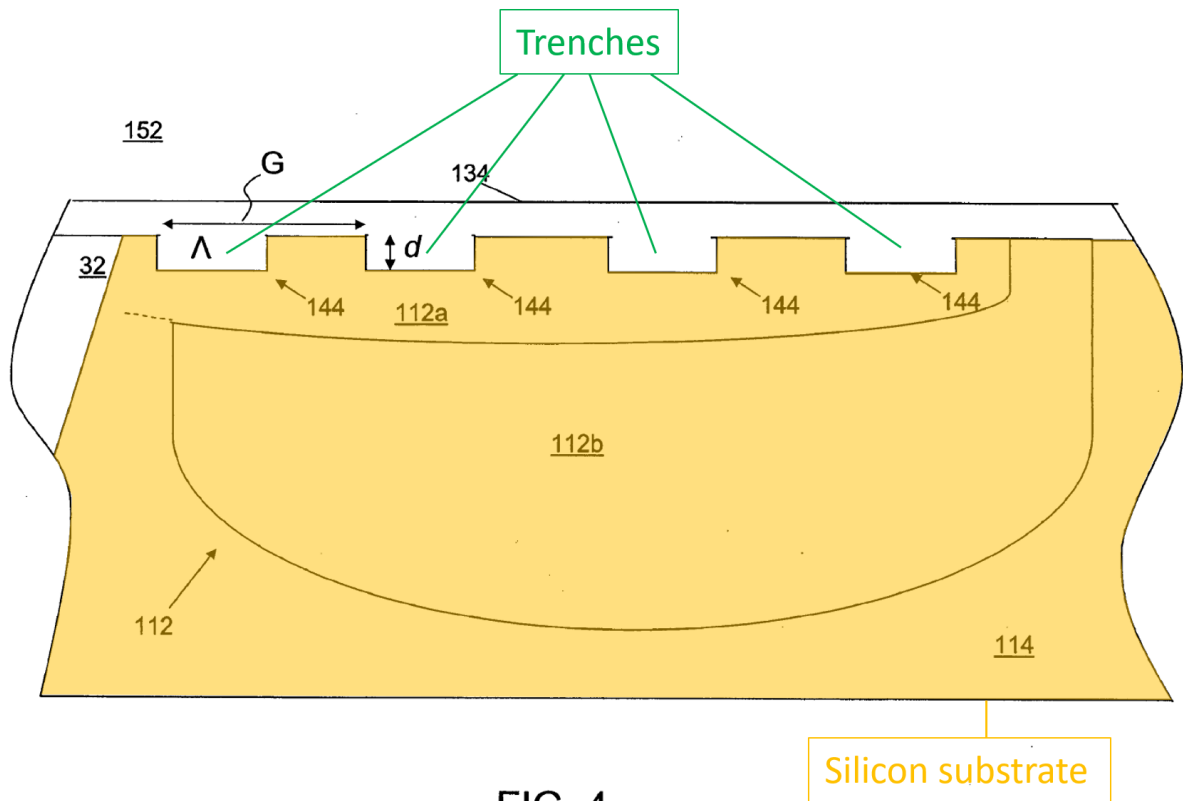


FIG. 4

Baggenstoss, Fig. 4 (annotated).

149. In another embodiment, Baggenstoss discloses an optoelectronic device with a “blazed (or step-wise)” gratings formed of trenches 244. Baggenstoss, [0042].

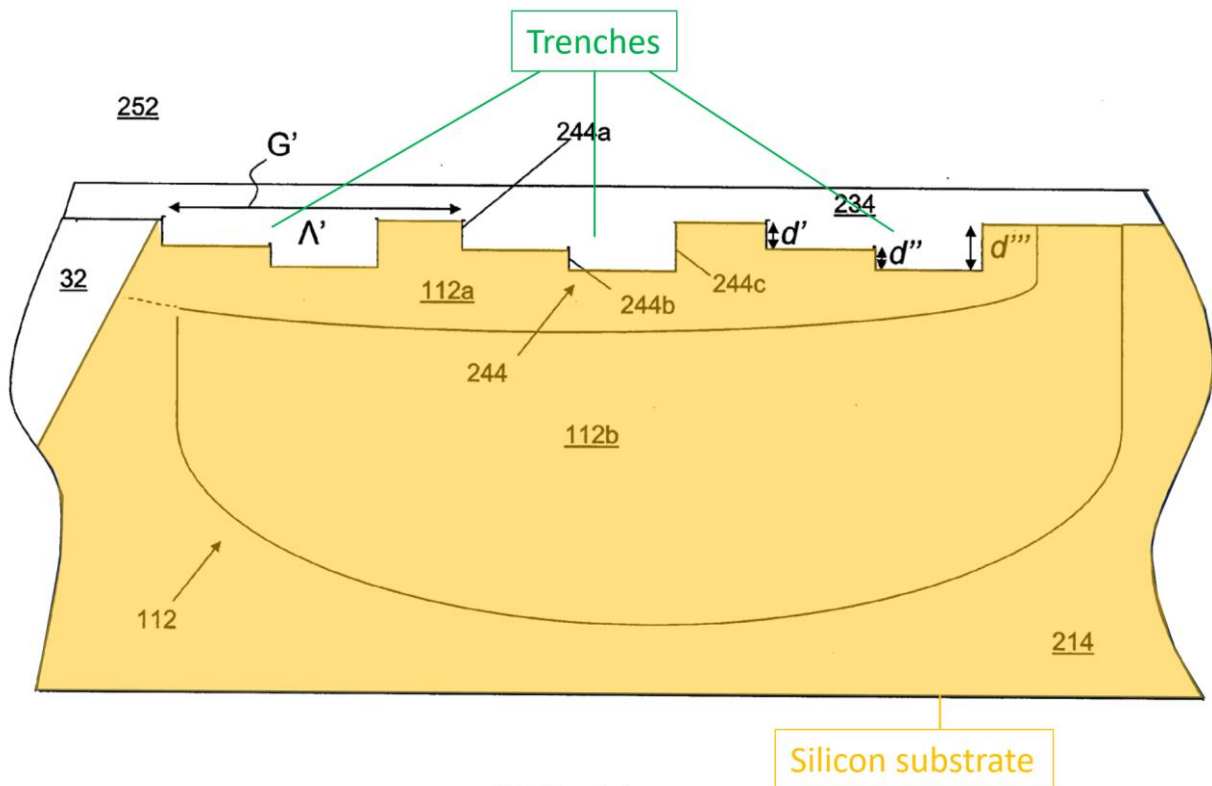


FIG. 11

Baggenstoss, Fig. 11 (annotated).

150. A POSITA would have looked to Baggenstoss's discussion of trenches for more details on how to implement the surface features in Haddad138. Baggenstoss teaches that its grated interface formed of trenches "allows a greater percentage of incident light to be captured, which is a vast improvement over the art." Baggenstoss, [0014]. Baggenstoss explains that its grated interface "serves to create a hybrid index of refraction ... thereby decreasing the percentage of incident light reflection." Baggenstoss, [0031]. With the grated interface formed of trenches 144, the incident light reflection is "nearly eliminated" with a trench depth d of 100 nm. Baggenstoss, [0035]. The "blazed" gratings formed of trenches 244 can decrease the incident light

reflection even further. Baggenstoss, [0042]-[0043]. Whether to use Baggenstoss's trenches 144 or 244 would have depended on the particular design needs regarding the cost of manufacture and the desired amount of reduction in incident light reflection. While Baggenstoss teaches that the blazed gratings formed of trenches 244 decrease the incident light reflection even more than the grated interface formed of trenches 144, such blazed gratings would cost more to manufacture. Two masks would be involved in creating the blazed gratings, and a second mask increases the expense associated with the etching step because each mask needs to be designed, manufactured, and aligned correctly during the etching step. Whether the additional cost is worthwhile would depend on whether a particular design requires the additional decrease in incident light reflection. For example, if the particular design required capturing light with multiple wavelengths, the blazed gratings may enable better quantum efficiency.

151. The use of Baggenstoss's trenches in Haddad138's devices would have involved use of a known technique to improve similar devices in the same way. Both Haddad138 and Baggenstoss disclose photodetectors. Haddad138, [0003], [0064]; Baggenstoss, [0014], [0009]. Both Haddad138 and Baggenstoss have the same goal of improving the efficiency of photodetectors in capturing incident light. Haddad138, [0063]; Baggenstoss, [0014]. Both Haddad138 and Baggenstoss achieve that goal by using a textured region including surface features. Haddad138, [0063], [0087]; Baggenstoss, [0031]-[0032], [0042]. Both Haddad138 and Baggenstoss disclose

placing the textured region on the light incident side. Haddad138, [0049]; Baggenstoss, [0038], Fig. 3. Like the grated interface of Baggenstoss, the textured region of Haddad138 can “enhance the absorption properties by reducing the amount of incident electromagnetic radiation that is reflected from the device.” Haddad138-Provisional434, 5. Both Haddad138 and Baggenstoss disclose forming the surface features using chemical etching. Haddad138, [0006]; Baggenstoss, [0038].

152. In addition, the use of Baggenstoss’s trenches in Haddad138’s devices would have been, at most, a simple substitution of one known element (i.e., Baggenstoss’s trenches) for another (i.e., Haddad138’s surface features) to obtain predictable results. Again, because Haddad138 discloses surface features, a POSITA would have understood that Baggenstoss’s trenches, which are surface features, would work in Haddad138.

153. A POSITA would have had a reasonable expectation of success in arriving at this combination. It would have been well within the abilities of a POSITA to use the implementation details of Baggenstoss’s trenches for Haddad138’s surface features, given that it would have involved routine manufacturing steps, such as chemical etching, that Haddad138 was already using for its surface features. Haddad138, [0006]. The techniques for creating trenches were commonly known and widely used across several fields, including image sensors and semiconductor solutions that manipulate light. For example, Haddad138 discloses forming surface

features “using deep trench isolation and etching techniques.” Haddad138, [0066].

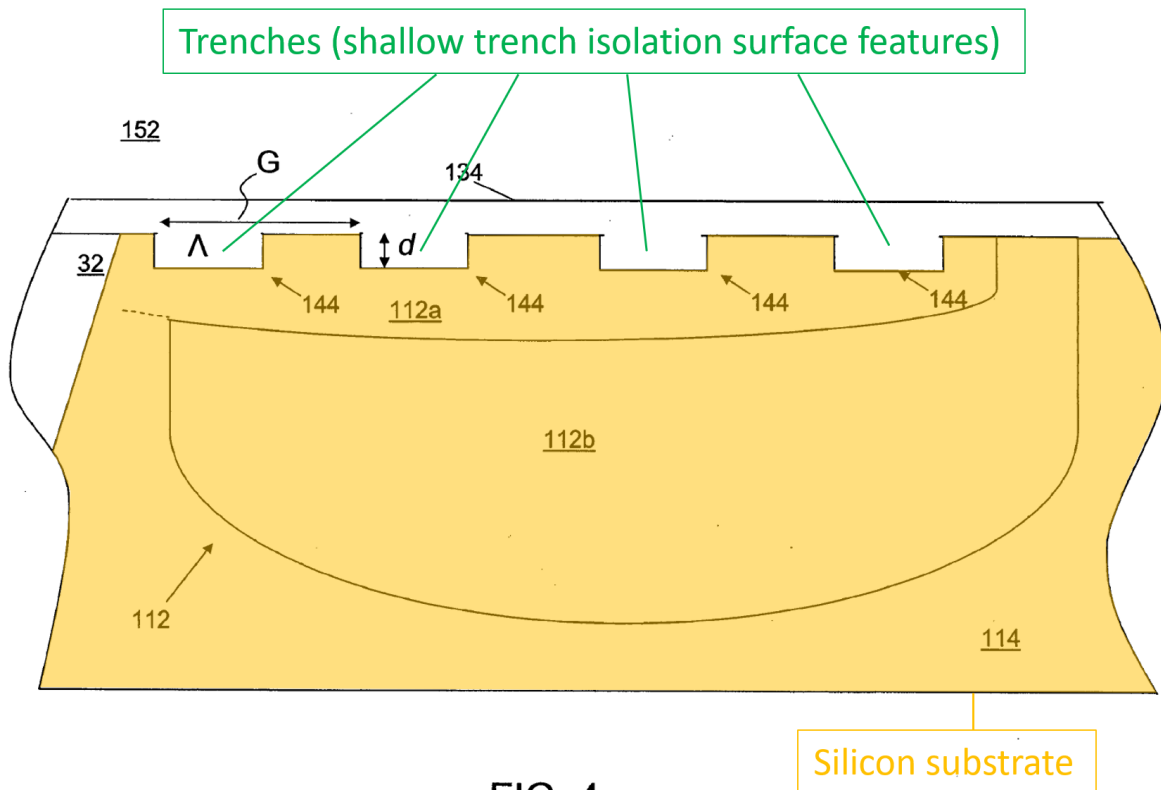
Alie also discloses forming gratings (which are formed of trenches), Alie, [0068], and forming trench isolations. Alie, [0098]. The fabrication and processing of gratings—whether blazed or not—were well known to a POSITA and have been popular.

2. Claim 4

- a) **“The device of claim 1, wherein the shallow trench isolation surface features have a substantially uniform height.”**

154. Haddad138 in view of Baggenstoss renders this limitation obvious.

155. As discussed above in Section VIII.B.1, Baggenstoss discloses an optoelectronic device with a grated interface formed by trenches 144. Baggenstoss, [0031]-[0032], [0009].



Baggenstoss, Fig. 4 (annotated).

156. Baggenstoss's trenches 144 correspond to the claimed shallow trench isolation surface features. Baggenstoss's trenches 144 have the same structures as the shallow trench isolation surface features described in the specification of the '682 patent. Baggenstoss's trenches 144 form a grating, which is the same shape and configuration that the '682 patent provides as an example of shallow trench isolation surface features. '682 patent, 9:34-37 ("Non-limiting examples of such shapes and configurations include ... gratings...."). Baggenstoss also discloses that its trenches 144 can have a depth of 100 nm (i.e., 0.1 micron), Baggenstoss, [0034], similar to the surface features of the '682 patent, '682 patent, 11:27-28.

157. Both Baggenstoss and the '682 patent describe the same or similar processes for creating the shallow trench isolation surface features. Baggenstoss discloses forming its trenches using “chemical etching, reactive ion etching (RIE), or other techniques for creating a recess in the silicon substrate.” Baggenstoss, [0038]. These are the same methods used to create shallow trench isolation surface features in the '682 patent, as explained in the provisional application for the '682 patent. Ex-1003, 11:16-22 (“Various methods can be utilized to form shallow trench isolation features.... Non-limiting examples can include chemical etching (e.g. anisotropic etching, isotropic etching) ... reactive ion etching....”).

158. Both Baggenstoss and the '682 patent explain that their shallow trench isolation surface features serve the same function. Just as the '682 patent states that its “surface features ... interact with light,” '682 patent, 9:9-13, Baggenstoss discloses that its trenches 144 interact with light to decrease incident light reflection, Baggenstoss, [0035].

159. Baggenstoss discloses that the trenches 144 have a predetermined depth (i.e., the claimed height), represented by d in Figure 4. Baggenstoss, [0032]. The predetermined depth d can be, for example, a constant depth of 100 nm. Baggenstoss, [0034]-[0035]. Baggenstoss's shallow trench isolation surface features, therefore, have a substantially uniform height, as required by this limitation.

160. Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the trenches and the shallow trench isolation in Baggenstoss. Baggenstoss discloses forming shallow trench isolation, e.g., element 32 in Figure 4. Baggenstoss, [0009]. The process for creating shallow trench isolation was well known. It involves forming trenches that isolate individual transistors, photodiodes, and other components of a semiconductor device. This isolation is crucial to prevent electrical or optical interference. Because shallow trench isolation offers high-quality isolation with less space compared to older methods like LOCOS (local oxidation of silicon), it is especially useful in high density, modern CMOS technology. It would have been obvious to use the same process to form both the shallow trench isolation and the trenches 144 in Baggenstoss, or to form both structures in the same manufacturing step. Ex-1034, [0010]-[0012] (disclosing using a shallow trench isolation process to form surface features). Creating the surface features using the same process as the process for the shallow trench isolation would generate predictable results, and reduce the costs associated with developing a new process. This would involve employing a known technique to improve similar devices in the same way. A POSITA would have had a reasonable expectation of success because Baggenstoss already discloses using shallow trench isolation in its devices, and it was well known how to use a shallow

trench isolation process to form surface features. Baggenstoss, [0009]; Haddad138, [0066]; Ex-1034, [0010]-[0012]. Haddad138 discloses forming surface features “using deep trench isolation and etching techniques.” Haddad138, [0066]. Another prior art publication also discloses using a shallow trench isolation (STI) process to create a surface grating made of trenches filled with field oxide. Ex-1034, [0010]-[0012].

3. Claim 5

a) “The device of claim 1, wherein the shallow trench isolation surface features are not uniform in height.”

161. Haddad138 in view of Baggenstoss renders this limitation obvious.

162. In another embodiment, Baggenstoss discloses an optoelectronic device with a “blazed (or step-wise)” gratings formed of trenches 244. Baggenstoss, [0042].

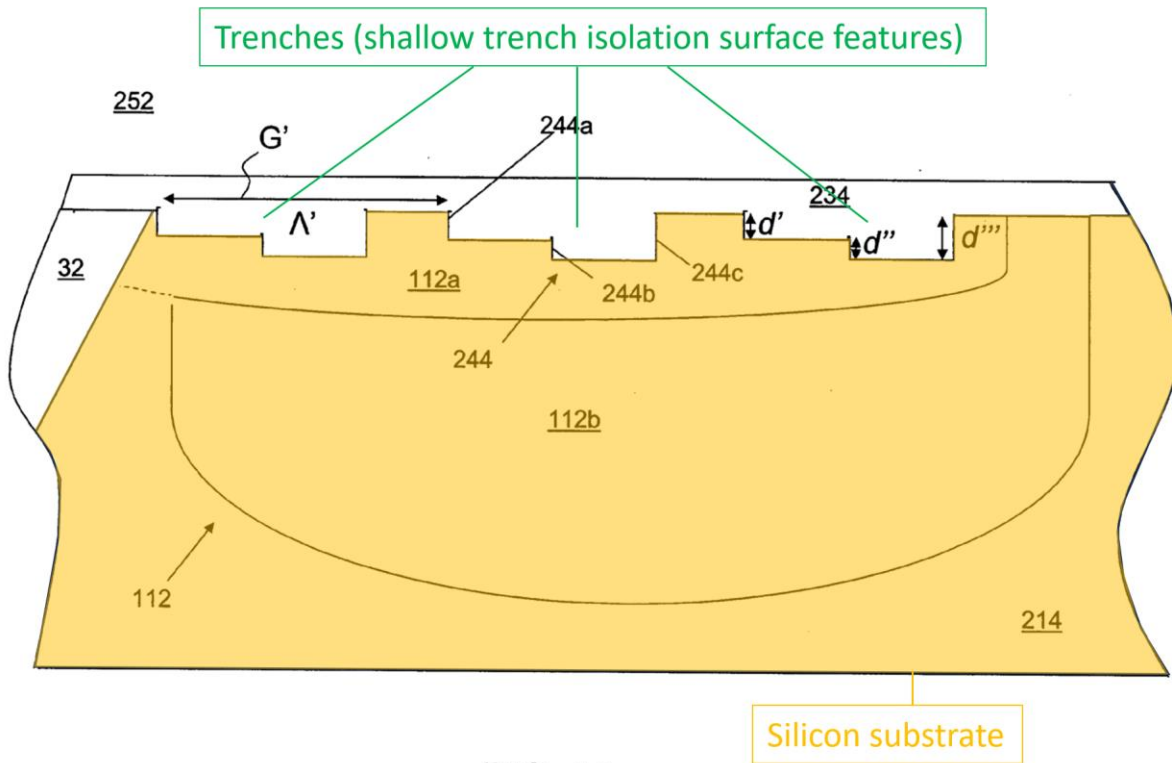


FIG. 11

Baggenstoss, Fig. 11 (annotated).

163. Baggenstoss's trenches 244 correspond to the claimed shallow trench isolation surface features. Baggenstoss's trenches 244 have the same structures as the shallow trench isolation surface features described in the specification of the '682 patent. Baggenstoss's trenches 244 form a grating, which is the same shape and configuration that the '682 patent provides as an example of shallow trench isolation surface features. '682 patent, 9:34-37 ("Non-limiting examples of such shapes and configurations include ... gratings..."). Baggenstoss also discloses that the trenches 244 may have predetermined depths ranging "from about 10 nm to about 250 nm" (i.e.,

0.01 to 0.25 microns). Baggenstoss, [0043], similar to the surface features of the '682 patent, '682 patent, 11:27-28.

164. Both Baggenstoss and the '682 patent describe the same or similar processes for creating the shallow trench isolation surface features. Baggenstoss discloses forming its trenches using “chemical etching, reactive ion etching (RIE), or other techniques for creating a recess in the silicon substrate.” Baggenstoss, [0038]; *see also* Baggenstoss, [0043] (“The trenches 244 could be formed by any of the methods described above with respect to [trenches 144 in] FIG. 4”). These are the same methods used to create shallow trench isolation surface features in the '682 patent, as explained in the provisional application for the '682 patent. Ex-1003, 11:16-22 (“Various methods can be utilized to form shallow trench isolation features.... Non-limiting examples can include chemical etching (e.g. anisotropic etching, isotropic etching) ... reactive ion etching....”).

165. Both Baggenstoss and the '682 patent explain that their shallow trench isolation surface features serve the same function. Just as the '682 patent states that its “surface features ... interact with light,” '682 patent, 9:9-13, Baggenstoss discloses that its trenches 244 interact with light to decrease incident light reflection, Baggenstoss, [0042].

166. As shown in Figure 11, the trenches 244 have two different depths (i.e., the claimed heights). Baggenstoss, [0043]. Thus, the shallow trench isolation surface

features are not uniform in height, as required by this limitation. Baggenstoss discloses that its trenches can be formed by chemical etching. Baggenstoss, [0038], [0043]. Typically, two masks would be required to etch the two different depths of the trenches 244.

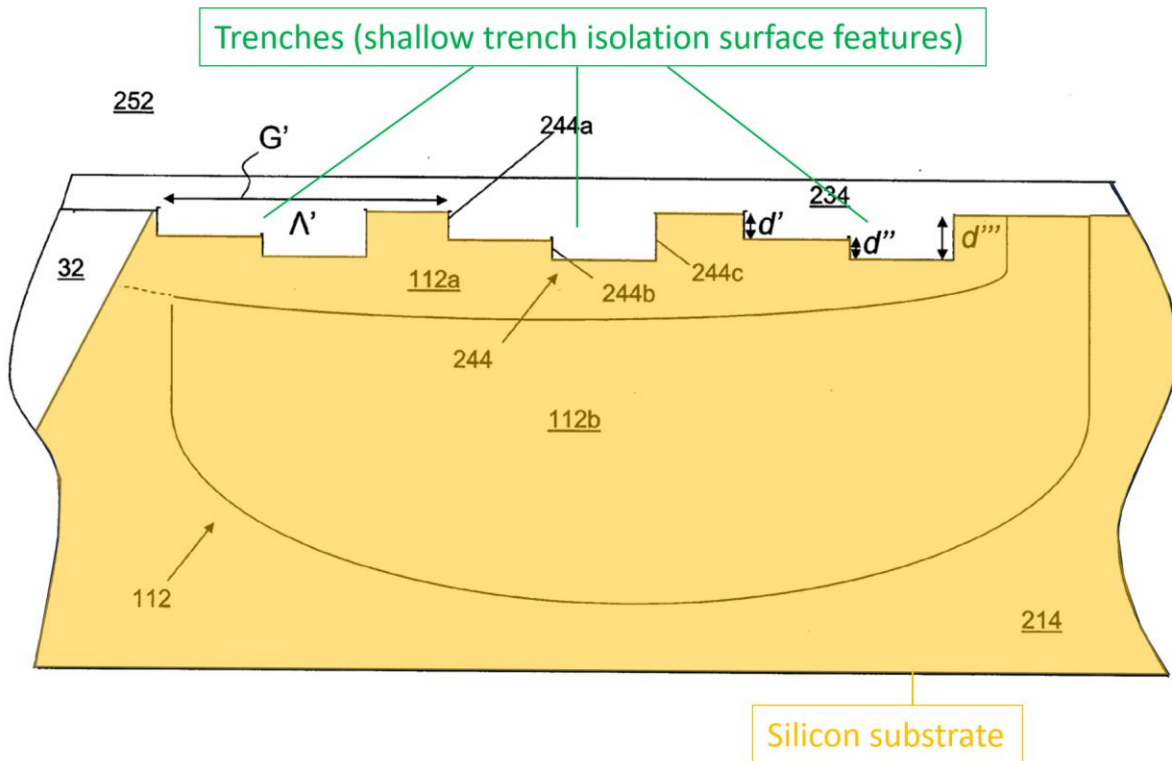
167. Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the trenches and the shallow trench isolation in Baggenstoss, or to form both structures in the same manufacturing step, for the same reason discussed above regarding claim 4.

4. Claim 14

- a) “The device of claim 1, wherein said plurality of shallow trench isolation surface features comprise multiple etched levels.”**

168. Haddad138 in view of Baggenstoss renders this limitation obvious.

169. As discussed above regarding claim 5, Baggenstoss discloses trenches 244 (i.e., the claimed shallow trench isolation surface features) with two different depths. Baggenstoss, [0043].



Baggenstoss, Fig. 11 (annotated).

170. The different depths correspond to the claimed multiple etched levels because Baggenstoss's trenches 244 can be formed via chemical etching. Baggenstoss, [0038], [0043]. Typically, two masks would be required to etch the two different depths of the trenches 244.

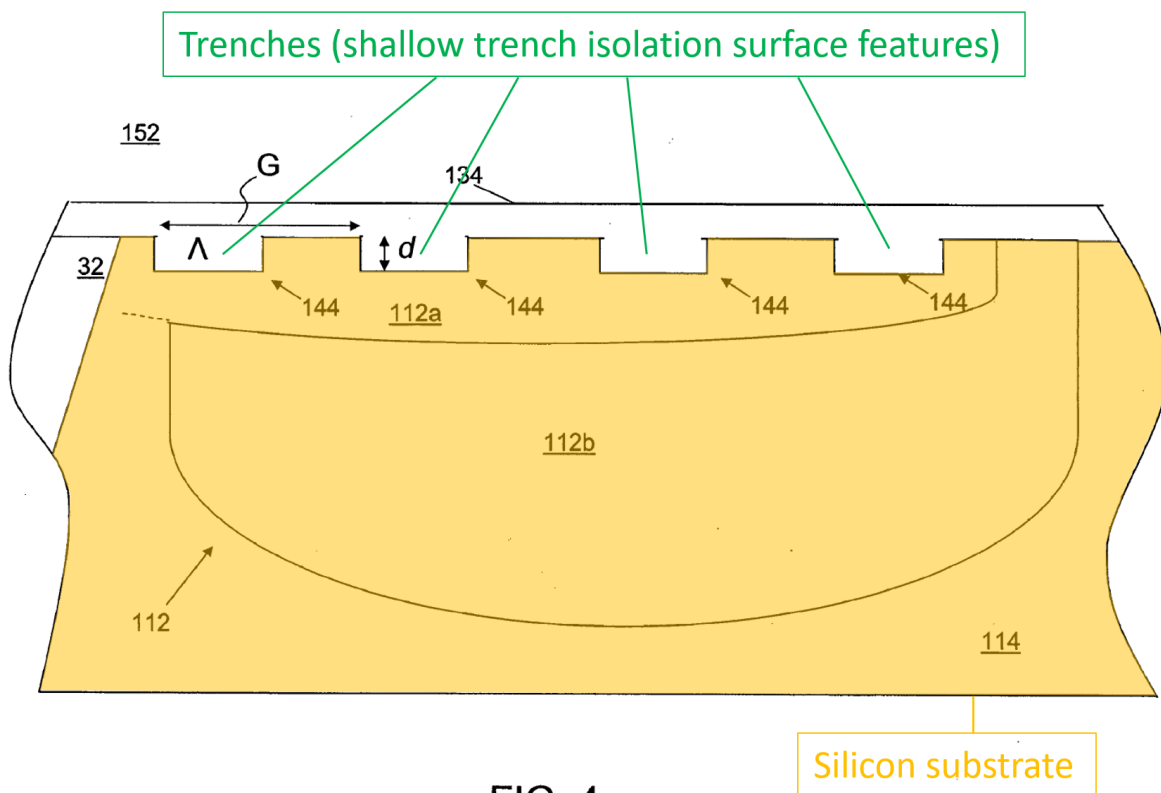
5. Claim 21

- a) **“The device of claim 1, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

171. Haddad138 in view of Baggenstoss renders this limitation obvious under Patent Owner's proposed construction in the 737 Case.

172. In the 737 Case, Petitioner proposed that the '737 patent term "the surface features are arranged according to a pattern" is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning and that, to the extent a construction is required, it means "features coincident with at least one surface that are arranged in a repeating manner." Ex-1014, 4.

173. As discussed above regarding claim 4, Figure 4 of Baggenstoss depicts a grated interface formed by trenches 144 (i.e., the claimed shallow trench isolation surface features). Baggenstoss, [0031]-[0032].



Baggenstoss, Fig. 4 (annotated).

174. “Each grating (measured as the distance from the beginning of one trench 144 to the beginning of the next trench 144 (shown by arrow G)) has a predetermined period that is represented by Λ .” Baggenstoss, [0032]. The predetermined period Λ can be, for example, 340 nm. Baggenstoss, [0034]. Baggenstoss’s trenches are features coincident with at least one surface that are arranged in a repeating manner, and are an example of a pattern provided by the provisional application for the ’682 patent. Ex-1003, 13:2-4 (“[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a **uniform grid pattern** comprised of [trenches] that form **a series of spaces and lines** or pillars.”).

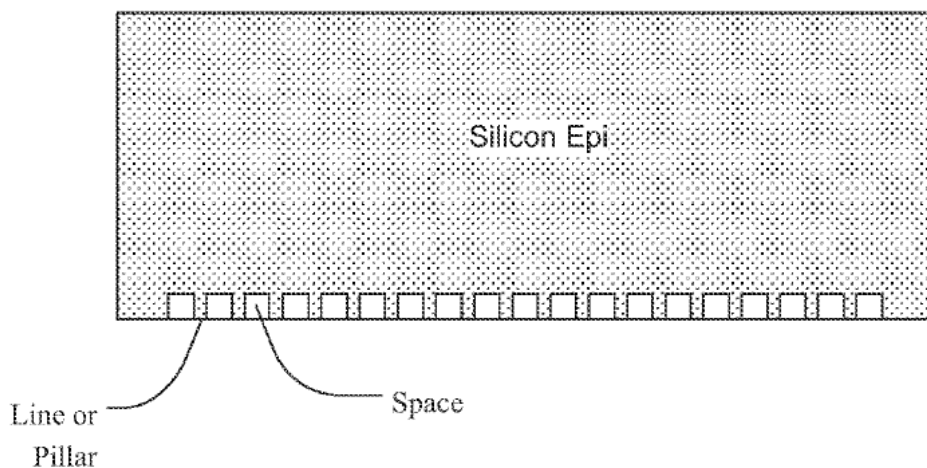


FIG. 5

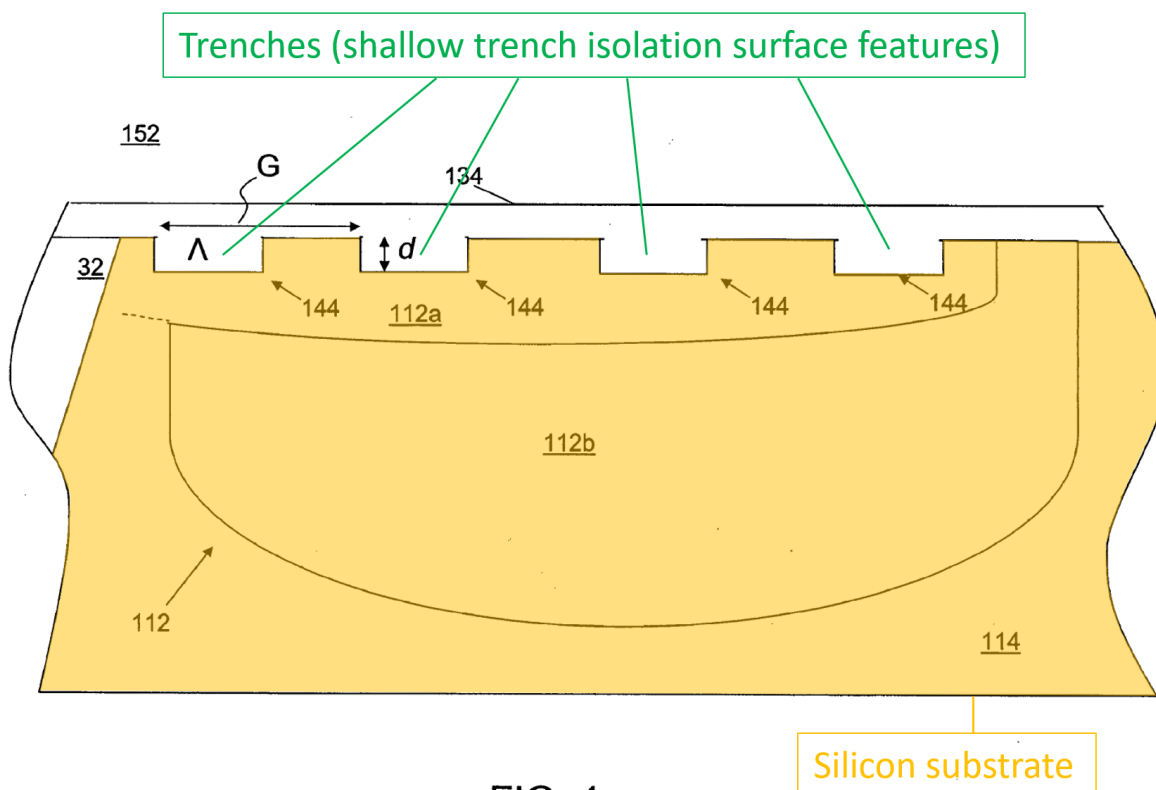
Ex-1003, Fig. 5.

6. Claim 22

- a) “The device of claim 21, wherein the pattern is an at least substantially uniform grid.”

175. Haddad138 in view of Baggenstoss renders this limitation obvious.

176. As discussed above regarding claim 4, Figure 4 of Baggenstoss depicts a grated interface formed by trenches 144 (i.e., the claimed shallow trench isolation surface features). Baggenstoss, [0031]-[0032].



Baggenstoss, Fig. 4 (annotated).

177. “Each grating (measured as the distance from the beginning of one trench 144 to the beginning of the next trench 144 (shown by arrow G) has a predetermined period that is represented by Λ ,” i.e., the trenches form the claimed substantially uniform grid. Baggenstoss, [0032]. The provisional application for the ’682 patent identifies such gratings as an example of a “uniform grid pattern.” Ex-1003, 13:2-4

(“[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a **uniform grid pattern** comprised of [trenches] that form **a series of spaces and lines** or pillars.”).

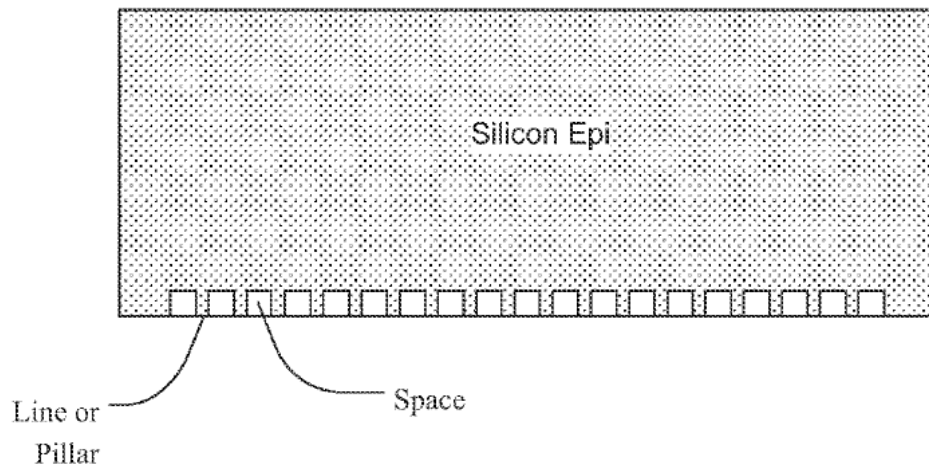


FIG. 5

Ex-1003, Fig. 5.

C. Ground A-3: Claims 9-10, 13, 19-20, 28-31, and 34-42 Are Obvious Based on Haddad138 and Alie

1. The Combination of Haddad138 and Alie

178. Haddad138 discloses a substrate coupled to a semiconductor layer by way of a bonding layer. Haddad138, [0086]. However, it does not disclose the bonding layer thickness, the use of two bonding layers, or the use of a reflector layer.

179. Alie contains additional details about the bonding layer and a reflector layer. In particular, it discloses the use of a dielectric layer as a bonding layer. Alie, [0055], [0087], [0105]. In addition, Alie discloses that its dielectric layer can have “a thickness of from about 500 nm to about 2 microns.” Alie, [0088]. Alie further

discloses that, instead of using just one dielectric layer for bonding, two dielectric layers can be used. Alie, [0059]. Alie also discloses use of a reflector layer. Alie, [0089].

180. Haddad138 also discloses that its surface features can be formed by etching. Haddad138, [0006]. However, it does not expressly mention using a mask and photolithography, followed by etching.

181. Alie contains additional details about etching. In particular, it discloses that surface features can be formed by “a selective etching technique, such as a mask, photolithography, and an etch.” Alie, [0072].

182. A POSITA would have had looked to Alie for additional details about the bonding layer and the etching process, as well as incorporating from Alie the reflector layer.

183. Combining Haddad138 with Alie would have involved use of a known technique (i.e., Alie’s bonding layers, reflector layer, or etching technique) to improve similar devices in the same way. Both Haddad138 and Alie share the same two joint inventors: Jeffrey McKee and Chintamani Palsule. Both Haddad138 and Alie concern photodetectors with textured regions that increase quantum efficiency. Haddad138, [0063]-[0064], [0087]; Alie, [0052], [0096], [0006]. The textured regions in both references include similarly shaped surface features. Haddad138, [0063]; Alie, [0068].

The textured regions in both references can be formed by chemical etching. Haddad138, [0066]; Alie, [0074].

184. Both Haddad138's and Alie's devices use similar materials. *See, e.g.*, Haddad138, [0052]; Alie, [0060]. Both Haddad138's and Alie's devices also share similar dimensions. *See, e.g.*, Haddad138, [0055] ("the semiconductor material has a thickness of from about 1 μm to about 10 μm "); Alie, [0063] ("the semiconductor material has a thickness of from about 1 μm to about 10 μm "). In view of the above, where Haddad138 is silent on certain details regarding the bonding layers, the reflector layer, and the etching technique, a POSITA would have looked to Alie for such details and used them for Haddad138's device with predictable results. A POSITA would have commonly looked to materials such as Alie for implementation details regarding similar devices. Additional motivations for using these elements are explained further below.

185. A POSITA would have had a reasonable expectation of success in making this combination. It would have been well within the abilities of a POSITA to use Alie's bonding layers, reflector layer, and etching technique for Haddad138's device, given that it would have involved routine manufacturing steps that Alie had already used in its devices with predictable results. Bonding layers, reflector layers, and photolithography have all been commonly known and widely used across several fields, including image sensors and semiconductor solutions that manipulate light.

2. Claim 9

- a) **“The device of claim 1, wherein said bonding layer has a thickness in a range of about 30 nm to about 3 microns.”**

186. Haddad138 in view of Alie renders this limitation obvious.

187. Haddad138 discloses that “[t]he carrier substrate can be coupled to the photosensing pixel by various techniques” including “by way of a bonding layer” (i.e., the claimed first bonding layer). Haddad138, [0086].

188. Similarly, Alie discloses the use of a dielectric layer as a bonding layer. Alie, [0055], [0087], [0105]. Alie discloses that its dielectric layer can have “a thickness of from about 500 nm to about 2 microns,” which is a range fully encompassed by the claimed range of about 30 nm to about 3 microns. Alie, [0088]. Alie does not teach away from the claimed range and the claimed range does not produce any new or unexpected result. A POSITA would have known that the ranges of about 30 nm to about 3 microns or about 40 nm to about 2 microns were typical for optoelectronic devices because the thickness of a bonding layer has to balance mechanical stability, electrical insulation, optical properties, surface finish, and temperature management.

3. Claim 10

- a) **“The device of claim 1, wherein said bonding layer has a thickness in a range of about 40 nm to about 2 microns.”**

189. Haddad138 in view of Alie renders this limitation obvious.

190. Haddad138 discloses that “[t]he carrier substrate can be coupled to the photosensing pixel by various techniques” including “by way of a bonding layer” (i.e., the claimed first bonding layer). Haddad138, [0086].

191. Similarly, Alie discloses the use of a dielectric layer as a bonding layer. Alie, [0055], [0087], [0105]. Alie discloses that its dielectric layer can have “a thickness of from about 500 nm to about 2 microns,” which is a range fully encompassed by the claimed range of about 40 nm to about 2 microns. Alie, [0088]. Alie does not teach away from the claimed range and the claimed range does not produce any new or unexpected result. A POSITA would have known that the ranges of about 30 nm to about 3 microns or about 40 nm to about 2 microns were typical for optoelectronic devices because the thickness of a bonding layer has to balance mechanical stability, electrical insulation, optical properties, surface finish, and temperature management.

4. Claim 13

- a) **“The device of claim 1, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.”**

192. Haddad138 in view of Alie renders this limitation obvious.

193. Haddad138 discloses that surface features can be formed by etching. Haddad138, [0006].

194. Alie teaches that using a mask and photolithography to etch surface features allows forming “a specific structure or pattern” over a specific area of a target surface. Alie, [0072]. Masks and photolithography to etch semiconductor materials were and still are standard tools to create regular patterns in the semiconductor industry. With this technique, etched surface features can be created with precision. A POSITA would have been familiar with this well known technique.

5. Claim 19

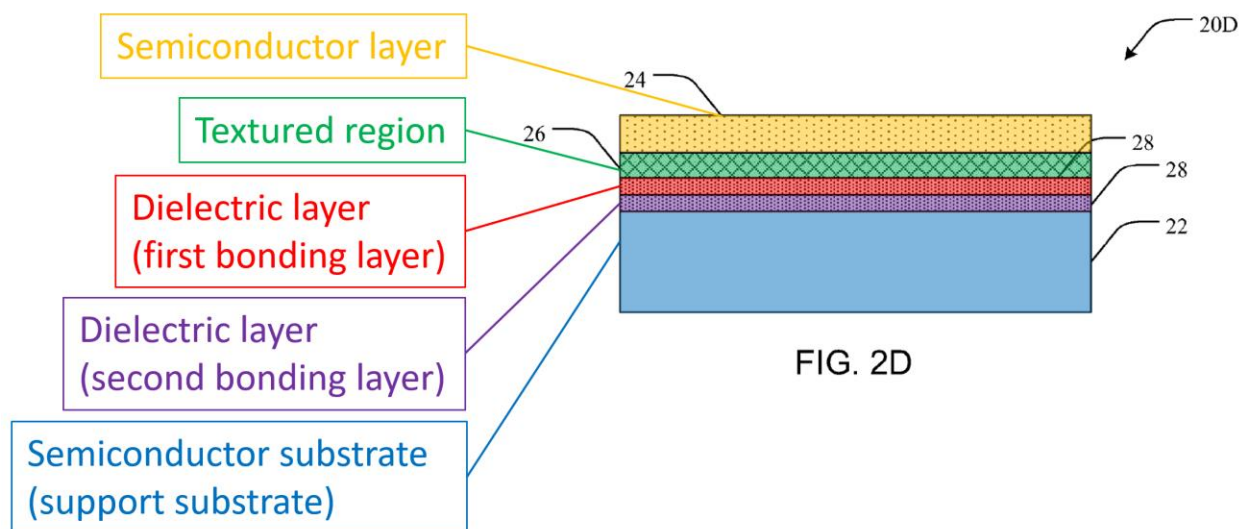
a) **“The device of claim 1, further comprising a second bonding layer positioned between the first bonding layer and the support substrate.”**

195. Haddad138 in view of Alie renders this limitation obvious.

196. Haddad138 discloses that, during the manufacture of an optoelectronic device, “[t]he carrier substrate can be coupled to the photosensing pixel by various techniques” including “by way of a bonding layer” (i.e., the claimed first bonding layer). Haddad138, [0086].

197. Alie also discloses using a dielectric layer as a bonding layer in an optoelectronic device. Alie, [0055], [0006]. Alie further discloses that, instead of using just one dielectric layer for bonding, two dielectric layers can be used. Alie, [0059]. A POSITA would have known that using two bonding layers was a common technique

to ensure the strength, uniformity, thermal performance, and reliability of the bond. See, e.g., Ex-1032, [0041]-[0042]; Ex-1035, 113-14. By using two bonding layers, one can ensure that the two layers that are being bonded have the matching bonding properties. Figure 2D depicts the use of the second bonding layer (purple) positioned between the first bonding layer (red) and the support substrate (blue). Alie, [0059].



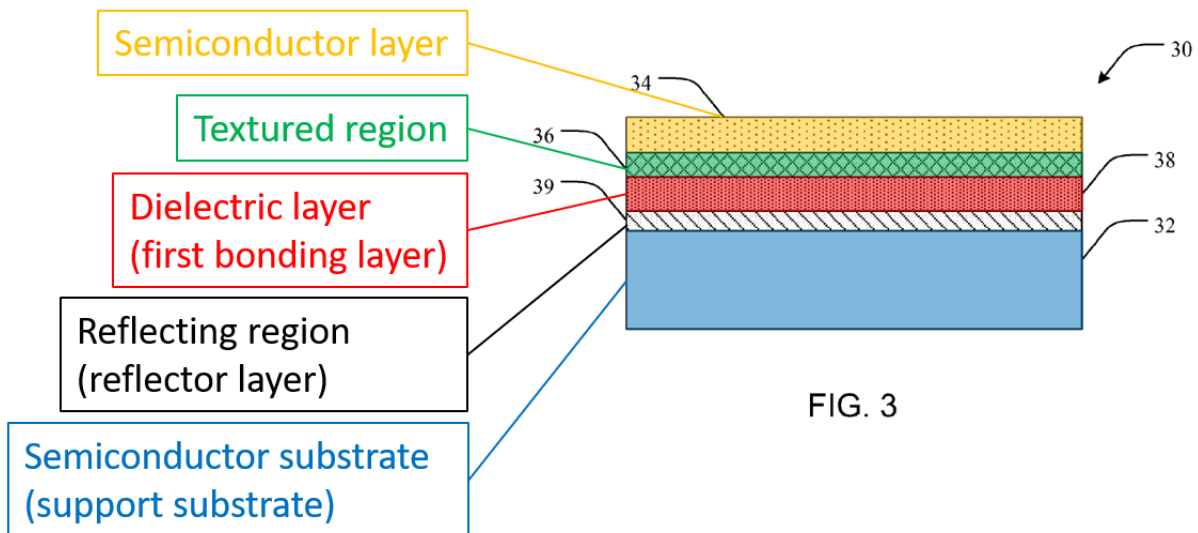
Alie, Fig. 2D (annotated).

6. Claim 20

- a) **“The device of claim 19, further comprising a reflector layer disposed between the first bonding layer and the second bonding layer.”**

198. Haddad138 in view of Alie renders this limitation obvious.

199. Figure 3 of Alie depicts the use of a reflecting region 39 (i.e., the claimed reflector layer) directly beneath the first bonding layer. Alie, [0089].



Alie, Fig. 3 (annotated).

200. In discussing a manufacturing method for a device similar to the Figure 3 device, Alie discloses that there can be “a second dielectric layer formed on the semiconductor substrate (not shown)” in addition to the existing dielectric layer. Alie, [0105]. The second dielectric layer formed on the semiconductor substrate corresponds to the claimed second bonding layer. Arranged as described in Alie, the reflector layer (brown) directly below the first bonding layer (red) would be sandwiched between the first bonding layer (red) and the second bonding layer formed on the semiconductor substrate (not shown).

201. It would have been obvious to modify Haddad138’s device (modified to use Alie’s two bonding layers as discussed above regarding claim 19) by placing Figure 3’s reflector layer between the two bonding layers, as taught by Alie. A known issue in the field is a loss of light due to transmission through a semiconductor layer.

Placing a reflector layer on the side opposite the light incident side of the semiconductor layer addresses this issue by increasing internal reflection of light within the semiconductor layer. Alie teaches that “[s]uch internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer.” Alie, [0070]. Alie further teaches that “[t]his increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.” Alie, [0070]. Given the known challenge of light loss and the established effectiveness of reflectors in improving light absorption, a POSITA would have been motivated to apply this well-understood solution to enhance the performance of Haddad138’s device. A well-known textbook confirms that reflectors are “well suited” for inclusion between a semiconductor layer and a support substrate opposite the light incident side to reflect light back into the semiconductor layer and increase light absorption. Ex-1031, 170. It would have been obvious to place the reflector layer between two bonding layers to ensure strong bonding, given that reflector layers may have poor bonding properties.

7. Claim 28

a) 28[pre]: “An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:”

202. Haddad138 discloses the preamble to the extent it is limiting.

203. See limitation 1[pre] in Ground A-1.

- b) **28[a]: “a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,”**

204. Haddad138 discloses this limitation.

205. See limitation 1[a] in Ground A-1.

- c) **28[b]: “a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,”**

206. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious.

207. See limitation 1[b] in Ground A-1.

- d) **28[c]: “a support substrate coupled to said semiconductor layer, and”**

208. Haddad138 discloses this limitation.

209. See limitation 1[c] in Ground A-1.

- e) **28[d]: “a first bonding layer disposed between the semiconductor layer and the support substrate,”**

210. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious.

211. See limitation 1[d] in Ground A-1.

- f) **28[e]: “a second bonding layer positioned between the first bonding layer and the support substrate, and”**

212. Haddad138 in view of Alie renders this limitation obvious.

213. See claim 19 in Ground A-3.

g) 28[f]: “a reflector layer disposed between the first bonding layer and the second bonding layer.”

214. Haddad138 in view of Alie renders this limitation obvious.

215. See claim 20 in Ground A-3.

8. Claim 29

a) “The device of claim 28, wherein said shallow trench isolation surface features comprise pyramids.”

216. Haddad138 discloses this limitation.

217. See claim 12 in Ground A-1 and claim 28 in Ground A-3.

9. Claim 30

a) “The device of claim 28, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.”

218. Haddad138 in view of Alie renders this limitation obvious.

219. See claims 13 and 28 in Ground A-3.

10. Claim 31

a) “The device of claim 28, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.”

220. Haddad138 discloses this limitation.

221. See claim 8 Ground A-1 and claim 28 in Ground A-3.

11. Claim 34

- a) **“The device of claim 28, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.”**

222. Haddad138 discloses this limitation.

223. See claim 11 in Ground A-1 and claim 28 in Ground A-3.

12. Claim 35

- a) **“The device of claim 28, wherein said photosensitive imager device is capable of detecting visible and infrared electromagnetic radiation.”**

224. Haddad138 discloses this limitation under both Petitioner’s and Patent Owner’s proposed constructions in the 737 Case.

225. See limitation 1[e] in Ground A-1 and claim 28 in Ground A-3.

13. Claim 36

- a) **“The device of claim 28, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.”**

226. Haddad138 discloses this limitation.

227. See claim 15 in Ground A-1 and claim 28 in Ground A-3.

14. Claim 37

- a) **“The device of claim 28, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.”**

228. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious.

229. See claim 16 in Ground A-1 and claim 28 in Ground A-3.

15. Claim 38

- a) **“The device of claim 28, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.”**

230. Haddad138 discloses this limitation.

231. See claim 17 in Ground A-1 and claim 28 in Ground A-3.

16. Claim 39

- a) **“The device of claim 28, wherein said textured region allows the semiconductor layer to experience multiple passes of light.”**

232. Haddad138 discloses this limitation.

233. See claim 18 in Ground A-1 and claim 28 in Ground A-3.

17. Claim 40

- a) **“The device of claim 28, further comprising deep trench isolation for isolating the device.”**

234. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious.

235. See claim 26 in Ground A-1 and claim 28 in Ground A-3.

18. Claim 41

- a) **“The device of claim 40, wherein said deep trench isolation provides light trapping functionality.”**

236. Haddad138 discloses this limitation.

237. See claim 27 in Ground A-1 and claim 28 in Ground A-3.

19. Claim 42

- a) **“The device of claim 28, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

238. Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case.

239. See claim 21 in Ground A-1 and claim 28 in Ground A-3.

D. Ground A-4: Claim 23 Is Obvious Based on Haddad138 and Haddad204

1. Claim 23

- a) **“The device of claim 21, wherein the pattern is a non-uniform arrangement.”**

240. Haddad138 in view of Haddad204 renders this limitation obvious.

241. As discussed above regarding limitation 1[b], Haddad138 discloses an optoelectronic device with a textured region. Haddad138, [0087], [0084], [0064]. Haddad138 discloses that its textured region can include surface features such as pillars. Haddad138, [0006], [0063].

242. Similarly, Haddad204 discloses an optoelectronic device with a textured region including surface features such as pillars. Haddad204, [0073], [0053]. Importantly, Haddad204 discloses “a plurality of pillars of variable sizes ... arranged

in a non-uniform array.” Haddad204, [0112]. Figure 9a shows a top view and Figure 9b shows a cross-sectional view of such “pillars etched into a semiconductor material.” Haddad204, [0112].

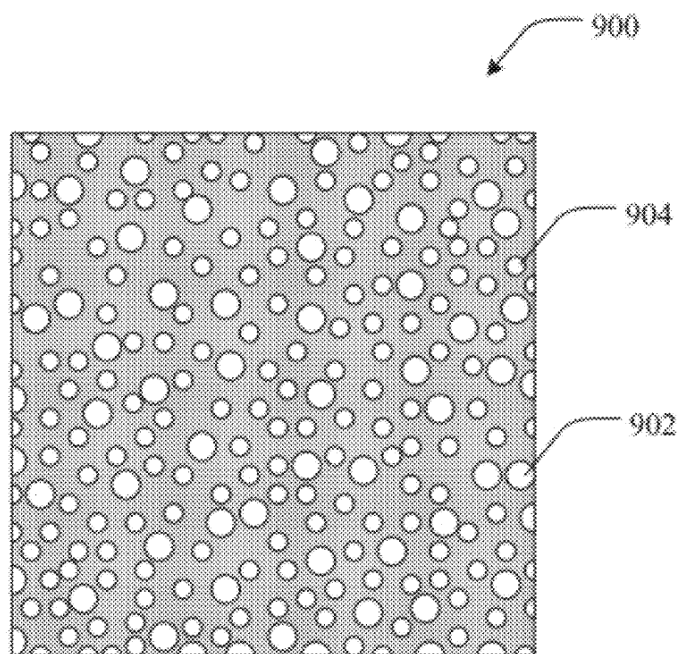


FIG. 9a

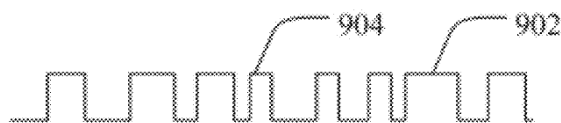


FIG. 9b

Haddad204, Figs. 9a-b.

243. A POSITA would have looked to Haddad204 for more details on how to implement the surface features disclosed in Haddad138. Haddad204 teaches that its surface features “increase the effective absorption length of the photosensitive pixel,”

which in turn, increases the quantum efficiency. Haddad204, [0073], [0076].

Increasing quantum efficiency using surface features is the same goal shared by Haddad138. Haddad138, [0063]. Both Haddad138 and Haddad204 teach that “[a]ny increase in the quantum efficiency makes a large difference in the signal to noise ratio.” Haddad138, [0050], Haddad204, [0058]. Non-uniformly arranged pillars can scatter light at various angles, which can improve light absorption in a semiconductor layer by interacting with more photodiode junction. Moreover, non-uniform pillars can create an irregular refractive index profile, which can reduce reflection over a broad range of incident angles. A POSITA would have been aware of these advantages. It was well known that an irregular pattern creates a good optical scattering effects.

244. Combining Haddad138 with Haddad204 would have involved use of a known technique (i.e., Haddad204’s non-uniform arrangement) to improve similar devices in the same way. Both Haddad138 and Haddad204 share the same joint inventors: Hodayoon Haddad, Jutao Jiang, Jeffrey McKee, Drake Miller, Chintamani Palsule, and Leonard Forbes. Both Haddad138 and Haddad204 concern photodetectors with textured regions that increase quantum efficiency. Haddad138, [0063]-[0064], [0087]; Haddad204, [0073], [0053]. The textured regions in both references include similarly shaped surface features such as pillars. Haddad138, [0063]; Haddad204, [0073]. The textured regions in both references can be formed by chemical etching. Haddad138, [0006]; Haddad204, [0093]. Both Haddad138 and

Haddad204 disclose placing the textured regions on the light incident side. Haddad138, [0049]; Haddad204, [0111].

245. A POSITA would have had a reasonable expectation of success in making this combination. It would have been well within the abilities of a POSITA to use Haddad204's non-uniform arrangement of pillars for Haddad138's arrangement of pillars, given that it would have involved routine manufacturing steps that Haddad204 had already used in its devices with predictable results. Creating pillar structures in a non-uniform arrangement has been commonly known and widely used across several fields, including image sensors and semiconductor solutions that manipulate light.

E. Ground A-5: Claim 23 Is Obvious Based on Haddad138 and Park

1. Claim 23

a) “The device of claim 21, wherein the pattern is a non-uniform arrangement.”

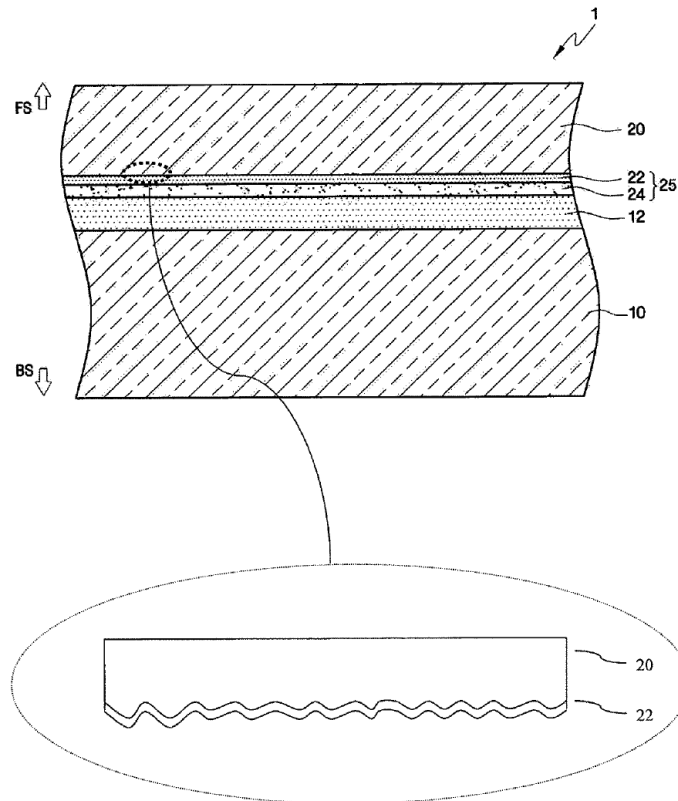
246. Haddad138 in view of Park renders this limitation obvious.

247. As discussed above regarding limitation 1[b], Haddad138 discloses an optoelectronic device with a textured region. Haddad138, [0087], [0084], [0064]. Haddad138 discloses that its textured region can include surface features such as protrusions. Haddad138, [0063].

248. Similarly, Park discloses an optoelectronic device with a textured region including surface features with protrusions. Park, [0072] (“Referring to the inset in FIG. 1 ... reflections may also be reduced by processing the second substrate 20 to

have an *uneven surface* facing the oxide layer 22.”), [0059] (“FIGS. 1 to 7 illustrate cross-sectional views of stages in a method of fabricating an image sensor”).

FIG. 1



Park, Fig. 1. As its name suggests, and as depicted in Figure 1, Park’s uneven surface has protrusions in a non-uniform arrangement.

249. A POSITA would have looked to Park for more details on how to implement the surface features including protrusions disclosed in Haddad138. Park teaches that its uneven surface helps with absorbing incident light by reducing reflection. Park, [0072]. Decreasing reflection of incident light means more light entering the silicon substrate to be absorbed. Haddad138 teaches that increased

absorption of incident light increases quantum efficiency. Haddad138, [0063]. Haddad138 teaches that “[a]ny increase in the quantum efficiency makes a large difference in the signal to noise ratio.” Haddad138, [0050]. An uneven surface can scatter light at various angles, which can improve light absorption in a semiconductor layer. Moreover, an uneven surface can create an irregular refractive index profile, which can reduce reflection over a broad range of incident angles. A POSITA would have been aware of these advantages. It was well known that an irregular pattern creates a good optical scattering effects. Based on the teachings of Park and Haddad138, a POSITA would have been motivated to use Park’s non-uniform arrangement.

250. Combining Haddad138 with Park would have involved use of a known technique (i.e., Park’s non-uniform arrangement) to improve similar devices in the same way. Both Haddad138 and Park concern increasing quantum efficiency of photodetectors. Haddad138, [0050], [0063], [0065]; Park, [0004]-[0005], Fig. 7. To achieve this goal, Haddad138 uses a textured region with protrusions and Park similarly uses an uneven surface with protrusions. Haddad138, [0063]; Park, [0072]. Both Haddad138 and Park disclose placing the textured region or the uneven surface on the light incident side. Haddad138, [0049]; Park, Figs. 1, 7. Like Park’s uneven surface, the Haddad138’s textured region can “enhance the absorption properties by

reducing the amount of incident electromagnetic radiation that is reflected from the device.” Haddad138-Provisional434, 5.

251. A POSITA would have had a reasonable expectation of success in making this combination. It would have been well within the abilities of a POSITA to use Park’s non-uniform arrangement of protrusions for Haddad138’s arrangement of protrusions, given that it would have involved routine manufacturing steps that Park had already used in its devices with predictable results. Creating an uneven surface of a semiconductor layer has been commonly known and widely used across several fields, including image sensors and semiconductor solutions that manipulate light.

F. Ground A-6: Claims 32-33 and 42-43 Are Obvious Based on Haddad138, Alie, and Baggenstoss

1. The Combination of Haddad138, Alie, and Baggenstoss

252. As discussed above in Sections VIII.C.1, 5 & 6, it would have been obvious to combine Haddad138 with Alie, incorporating Alie’s bonding layers and reflector layer in Haddad138’s device.

253. As discussed above in Section VIII.B.1, it would have been obvious to combine Haddad138 with Baggenstoss, incorporating Baggenstoss’s trenches in Haddad138’s device.

254. It further would have been obvious to combine Haddad138 with both Alie and Baggenstoss in order to incorporate Alie’s bonding layers and reflector layer, as

well as Baggenstoss's trenches, into Haddad138's device. The reasons for including such features in an optoelectronic device were well understood for the reasons taught in those references and discussed above in Sections VIII.B.1 and VIII.C.1, 5 & 6.

255. Combining Haddad138 with Alie and Baggenstoss would have involved use of a known technique to improve similar devices in the same way. Haddad138, Alie, and Baggenstoss all disclose photodetectors. Haddad138, [0003], [0019]; Alie, [0052], [0096], [0006]; Baggenstoss, [0014], [0009]. Haddad138, Alie, and Baggenstoss all have the same goal of improving the efficiency of photodetectors in capturing incident light. Haddad138, [0063]; Alie, [0052], Baggenstoss, [0014]. Haddad138, Alie, and Baggenstoss all achieve that goal by using a textured region including surface features. Haddad138, [0063], [0087]; Alie, [0052], Baggenstoss, [0031]-[0032], [0042]. Haddad138, Alie, and Baggenstoss all disclose placing the textured region on the light incident side. Haddad138, [0049]; Alie, [0094]; Baggenstoss, [0038], Fig. 3. Haddad138, Alie, and Baggenstoss all disclose forming the surface features using chemical etching. Haddad138, [0006]; Alie, [0074]; Baggenstoss, [0038].

256. A POSITA would have had a reasonable expectation of success in making this combination. It would have been well within the abilities of a POSITA to use Alie's bonding layers and reflector layer as discussed above in Sections VIII.C.1, 5 & 6 and to use Baggenstoss's trenches as discussed above in Section VIII.B.1. The

bonding layers, reflector layer, and trenches would work together in improving Haddad138's device.

2. Claim 32

- a) **“The device of claim 28, wherein the shallow trench isolation surface features have a substantially uniform height.”**

257. Haddad138 in view of Alie and Baggenstoss renders this limitation obvious.

258. See claim 4 in Ground A-2 and claim 28 in Ground A-3.

3. Claim 33

- a) **“The device of claim 28, wherein the shallow trench isolation surface features are not uniform in height.”**

259. Haddad138 in view of Alie and Baggenstoss renders this limitation obvious.

260. See claim 5 in Ground A-2 and claim 28 in Ground A-3.

4. Claim 42

- a) **“The device of claim 28, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

261. Haddad138 in view of Alie and Baggenstoss renders this limitation obvious under Patent Owner's proposed construction in the 737 Case.

262. See claim 21 in Ground A-2 and claim 28 in Ground A-3.

5. Claim 43

- a) “The device of claim 42, wherein the pattern is an at least substantially uniform grid.”**

263. Haddad138 in view of Alie and Baggenstoss renders this limitation obvious.

264. See claim 22 in Ground A-2 and 28 in Ground A-3.

G. Ground A-7: Claim 44 Is Obvious Based on Haddad138, Alie, and Haddad204

1. Claim 44

- a) “The device of claim 42, wherein the pattern is a non-uniform arrangement.”**

265. Haddad138 in view of Alie and Haddad204 renders this limitation obvious.

266. See claim 23 in Ground A-4 and claim 28 in Ground A-3.

267. As discussed above in Sections VIII.C.1, 5 & 6, it would have been obvious to combine Haddad138 with Alie, incorporating Alie’s bonding layers and reflector layer in Haddad138’s device.

268. As discussed above regarding Ground A-4, it would have been obvious to combine Haddad138 with Haddad204, incorporating Haddad204’s non-uniform arrangement in Haddad138’s device.

269. It further would have been obvious to combine Haddad138 with both Alie and Haddad204 in order to incorporate Alie’s bonding layers and reflector layer, as

well as Haddad204's non-uniform arrangement of surface features, into Haddad138's device. The reasons for including such features in an optoelectronic device were well understood for the reasons taught in those references and discussed above in Section VIII.C.1, 5 & 6 and regarding Ground A-4.

270. Combining Haddad138 with Alie and Haddad204 would have involved use of a known technique to improve similar devices in the same way. Haddad138, Alie, and Haddad204 all concern photodetectors with textured regions that increase quantum efficiency. Haddad138, [0050], [0063], [0065]; Alie, [0052], [0096], [0006]; Haddad204, [0073], [0053]. The textured regions in all three references include similarly shaped surface features such as pillars. Haddad138, [0063]; Alie, [0068]; Haddad204, [0073]. The textured regions in all three references can be formed by chemical etching. Haddad138, [0006]; Alie, [0074]; Haddad204, [0093]. Haddad138, Alie, and Haddad204 all disclose placing the textured regions on the light incident side. Haddad138, [0049]; Alie, [0094]; Haddad204, [0111].

271. A POSITA would have had a reasonable expectation of success in making this combination. It would have been well within the abilities of a POSITA to use Alie's bonding layers and reflector layer as discussed above in Section VIII.C.1, 5 & 6 and to use Haddad204's non-uniform arrangement as discussed above regarding Ground A-4. The bonding layers, reflector layer, and the non-uniform arrangement of surface features would work together in improving Haddad138's device.

H. Ground A-8: Claim 44 Is Obvious Based on Haddad138, Alie, and Park

1. Claim 44

a) “The device of claim 42, wherein the pattern is a non-uniform arrangement.”

272. Haddad138 in view of Alie and Park renders this limitation obvious.

273. See claim 23 in Ground A-5 and claim 28 in Ground A-3.

274. As discussed above in Sections VIII.C.1, 5 & 6, it would have been obvious to combine Haddad138 with Alie, incorporating Alie’s bonding layers and reflector layer in Haddad138’s device.

275. As discussed above regarding Ground A-5, it would have been obvious to combine Haddad138 with Park, incorporating Park’s non-uniform arrangement in Haddad138’s device.

276. It further would have been obvious to combine Haddad138 with both Alie and Park in order to incorporate Alie’s bonding layers and reflector layer, as well as Park’s non-uniform arrangement of surface features, into Haddad138’s device. The reasons for including such features in an optoelectronic device were well understood for the reasons taught in those references and discussed above in Section VIII.C.1, 5 & 6 and regarding Ground A-5.

277. Combining Haddad138 with Alie and Park would have involved use of a known technique to improve similar devices in the same way. Haddad138, Alie, and

Park all concern increasing quantum efficiency of photodetectors. Haddad138, [0050], [0063], [0065]; Alie, [0052], [0096], [0006]; Park, [0004]-[0005], Fig. 7. To achieve this goal, Haddad138 uses a textured region with protrusions and Alie and Park similarly use textured regions with protrusions. Haddad138, [0063]; Alie, [0068]; Park, [0072]. Haddad138, Alie, and Park all disclose placing the textured regions on the light incident side. Haddad138, [0049]; Alie, [0094]; Park, Figs. 1, 7.

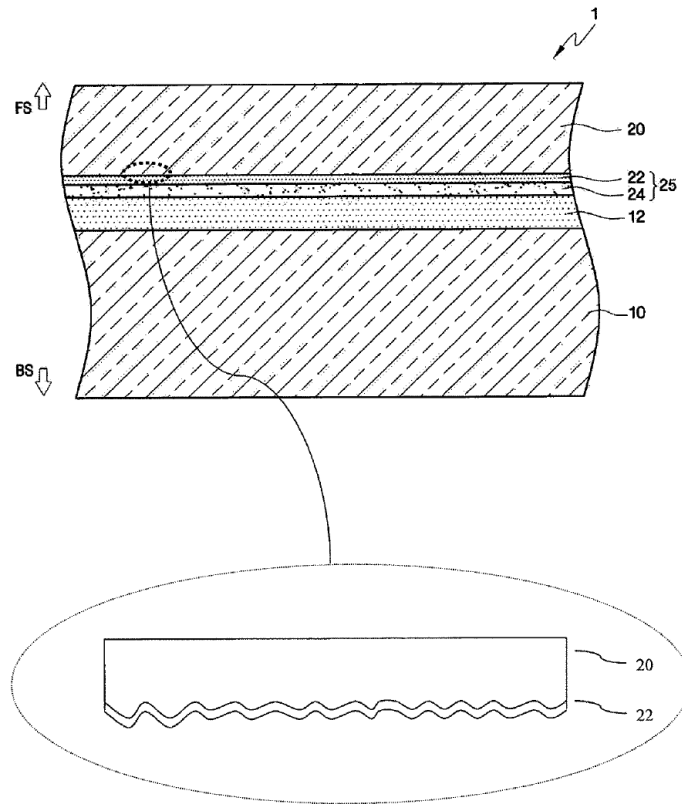
278. A POSITA would have had a reasonable expectation of success in making this combination. It would have been well within the abilities of a POSITA to use Alie's bonding layers and reflector layer as discussed above in Sections VIII.C.1, 5 & 6 and to use Park's non-uniform arrangement as discussed above regarding Ground A-5. The bonding layers, reflector layer, and the non-uniform arrangement of surface features would work together in improving Haddad138's device.

I. Ground B-1: Claims 24-25 Are Obvious Based on Park and Baggenstoss

1. The Combination of Park and Baggenstoss

279. Park discloses forming an uneven surface on a semiconductor layer of an optoelectronic device. Park, [0072], [0059].

FIG. 1



Park, Fig. 1.

280. Similarly, Baggenstoss discloses creating an optoelectronic device with a grated interface formed by trenches 144 (i.e., the claimed plurality of shallow trench isolation surface features). Baggenstoss, [0031]-[0032], [0009].

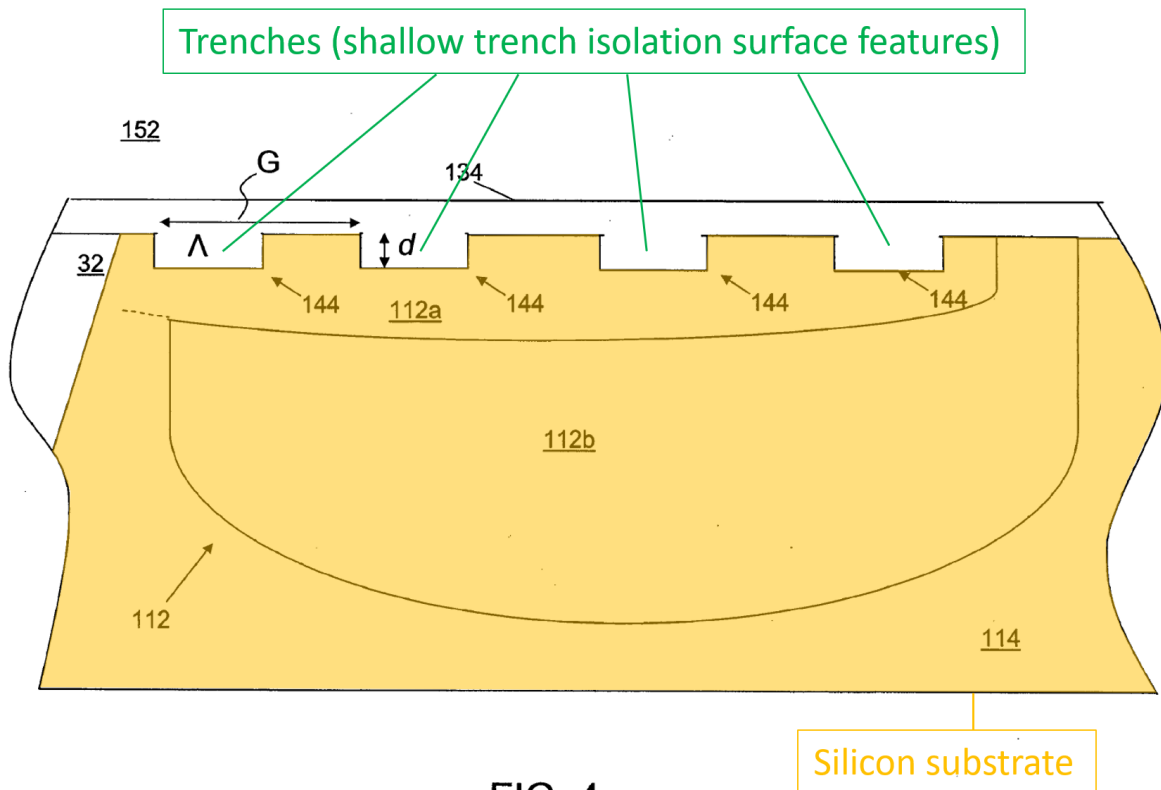


FIG. 4

Baggenstoss, Fig. 4 (annotated).

281. A POSITA would have looked to Baggenstoss's discussion of trenches for more details on how to implement the uneven surface in Park. Baggenstoss teaches that its grated interface formed of trenches "allows a greater percentage of incident light to be captured, which is a vast improvement over the art." Baggenstoss, [0014]. Baggenstoss explains that its grated interface "serves to create a hybrid index of refraction ... thereby decreasing the percentage of incident light reflection." Baggenstoss, [0031]. With the grated interface formed of trenches 144, the incident light reflection is "nearly eliminated" with a trench depth d of 100 nm. Baggenstoss, [0035]. The "blazed" gratings formed of trenches 244 can decrease the incident light

reflection even further. Baggenstoss, [0042]-[0043]. Whether to use Baggenstoss's trenches 144 or 244 would have depended on the particular design needs regarding the cost of manufacture and the desired amount of reduction in incident light reflection. While Baggenstoss teaches that the blazed gratings formed of trenches 244 decrease the incident light reflection even more than the grated interface formed of trenches 144, such blazed gratings would cost more to manufacture. Two masks would be involved in creating the blazed gratings, and a second mask doubles the expense associated with the etching step because each mask needs to be designed, manufactured, and aligned correctly during the etching step. In addition, using two masks usually requires at least two etching steps, which would consume more time and resources, further adding to the cost. Whether the additional cost is worthwhile would depend on whether a particular design requires the additional decrease in incident light reflection.

282. Using Baggenstoss's trenches in Park's method would have involved use of a known technique to improve similar devices in the same way. Both Park and Baggenstoss disclose photodetectors. Park, [0037]; Baggenstoss, [0014], [0009]. Both Park and Baggenstoss have the same goal of improving the efficiency of photodetectors in capturing incident light. Park, [0072]; Baggenstoss, [0014]. Both Park and Baggenstoss achieve that goal by using a textured region including surface features. Park, [0072]; Baggenstoss, [0031]-[0032], [0042]. Both Park and Baggenstoss disclose placing the textured region on the light incident side. Park, Figs.

1, 7; Baggenstoss, [0038], Fig. 3. Like the grated interface of Baggenstoss, Park's uneven surface can "serve to reduce specular reflection." Park, [0072].

283. The use of Baggenstoss's trenches in Park's method would have been a simple substitution of one known element (i.e., Baggenstoss's trenches) for another (Park's uneven surface) to obtain predictable results. Again, because Park discloses an uneven surface, a POSITA would have understood that Baggenstoss's trenches, which form an uneven surface, would work in Park.

284. A POSITA would have had a reasonable expectation of success in using Baggenstoss's trenches in Park's method. It would have been well within the abilities of a POSITA to use the implementation details of Baggenstoss's trenches for Park's uneven surfaces, given that it would have involved routine manufacturing steps that Park was already using. Park, [0065]-[0066]. The techniques for creating trenches were commonly known and widely used across several fields, including image sensors and semiconductor solutions that manipulate light. For example, Haddad¹³⁸ discloses forming surface features "using deep trench isolation and etching techniques." Haddad¹³⁸, [0066]. Alie also discloses forming gratings (which are formed of trenches), Alie, [0068], and forming trench isolations. Alie, [0098].

2. Claim 24

- a) 24[pre]: "A method of making an optoelectronic device, comprising:"**

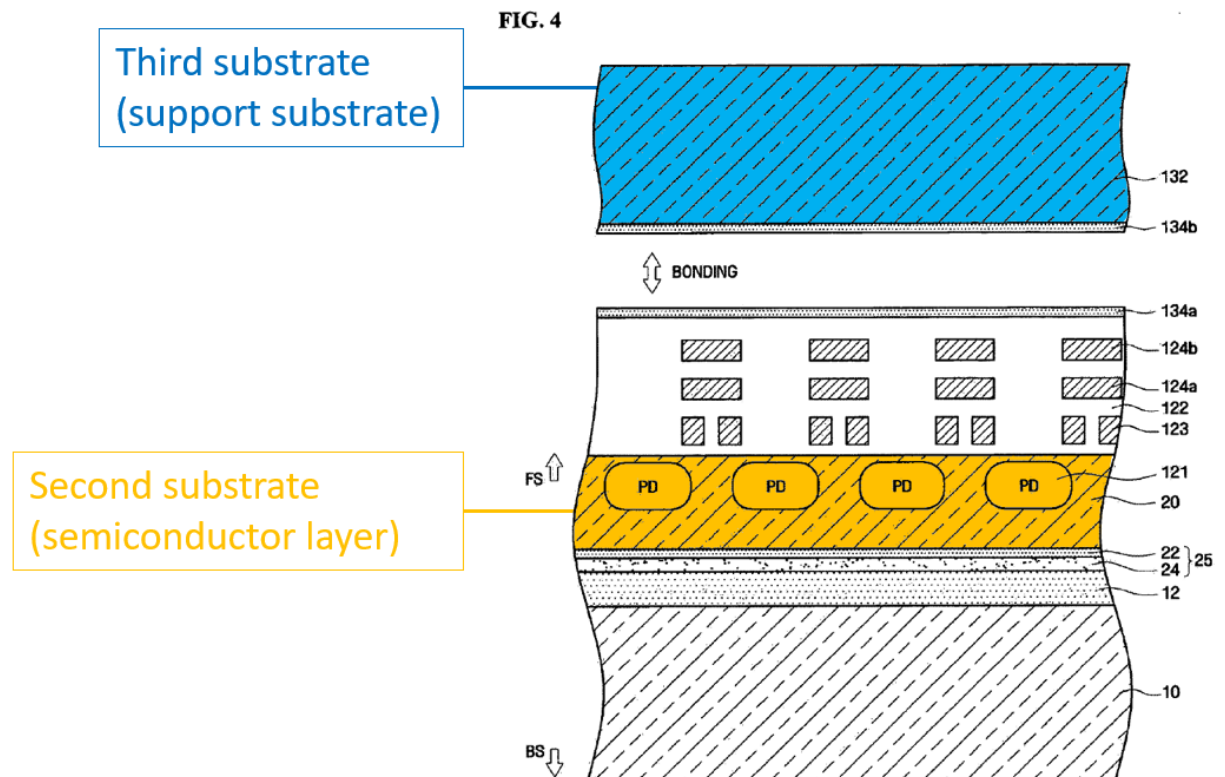
285. Park discloses the preamble to the extent it is limiting.

286. Park discloses that “FIGS. 1 to 7 illustrate cross-sectional views of stages in a method of fabricating an image sensor.” Park, [0037].

b) 24[a]: “bonding a semiconductor layer to a support substrate, wherein bonding the semiconductor layer to the support substrate includes:”

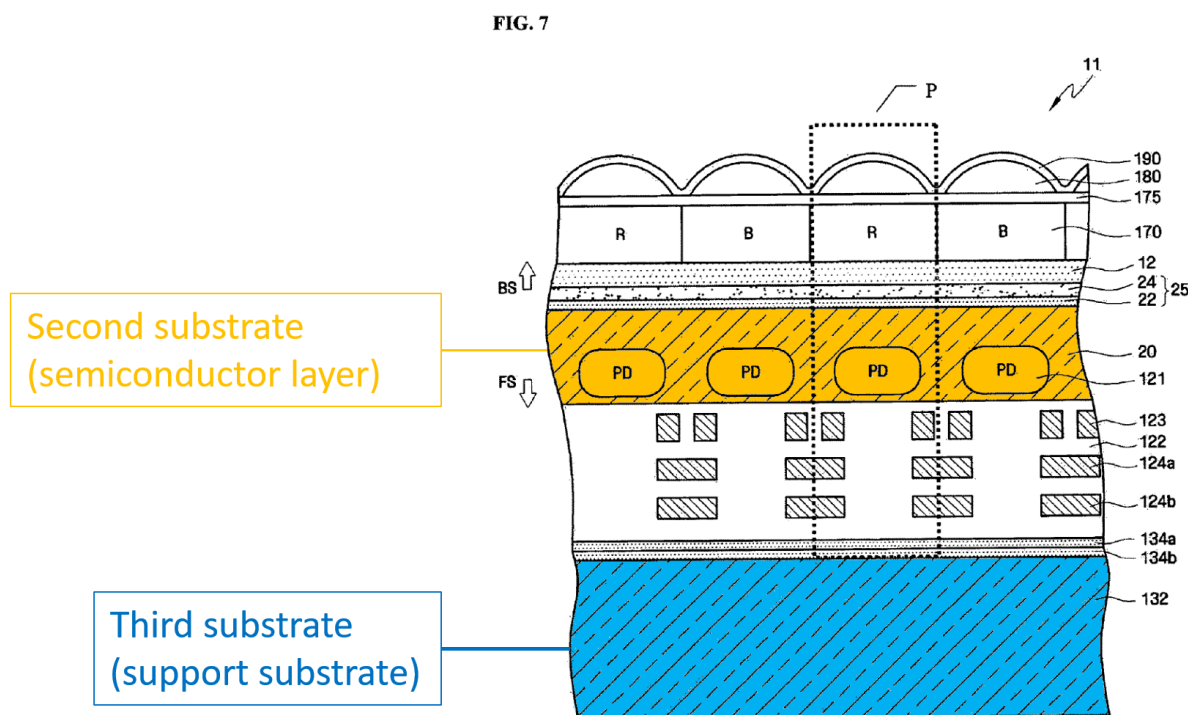
287. Park discloses this limitation.

288. Fig 4 depicts bonding a second substrate 20 (i.e., the claimed semiconductor layer) to a third substrate 132 (the claimed support substrate). Park, [0076].



Park, Fig. 4 (annotated).

289. The second substrate 20 corresponds to the claimed semiconductor layer because Park discloses that the second substrate 20 may be doped silicon with light sensing devices 121. Park, [0064], [0074]. The third substrate 132 corresponds to the claimed support substrate because it supports Park's device, as shown in Figure 7. Park, [0059].

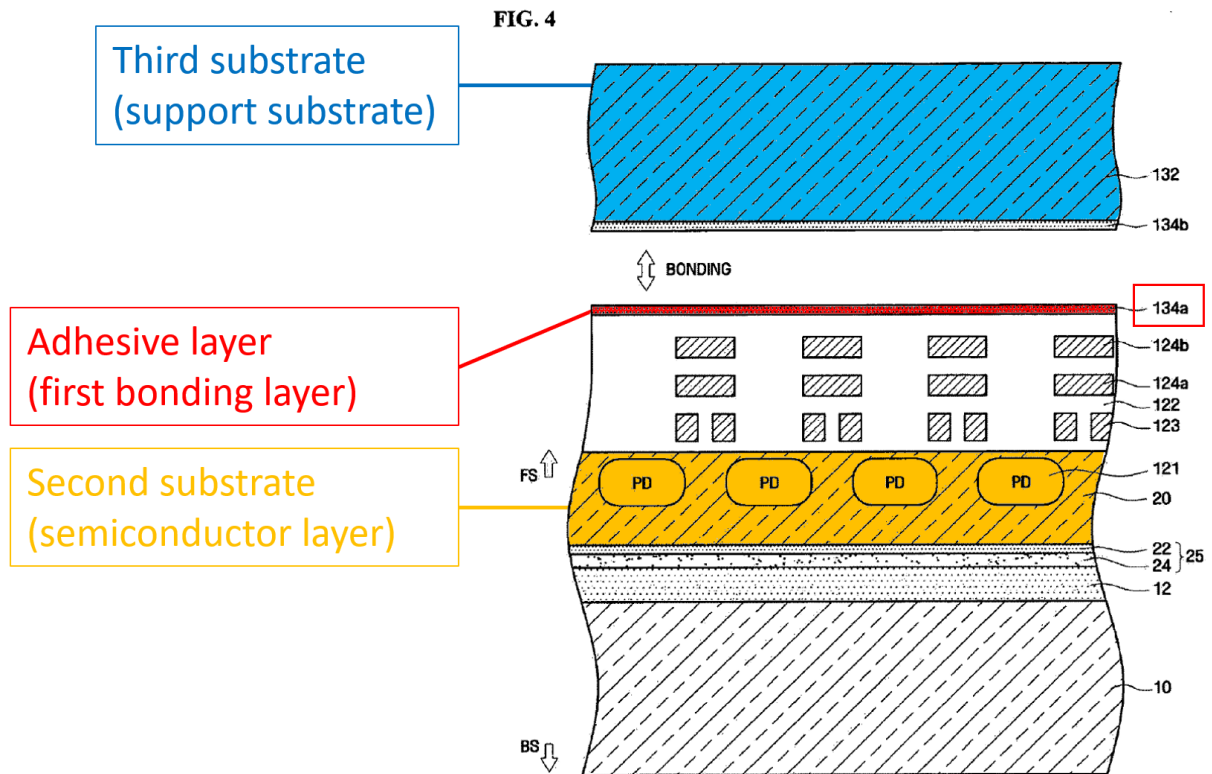


Park, Fig. 7 (annotated).

c) 24[b]: “depositing a first bonding layer onto the semiconductor layer; and”

290. Park discloses this limitation.

291. Park discloses depositing an adhesive layer 134a (i.e., the claimed first bonding layer) onto the semiconductor layer. Park, [0076].

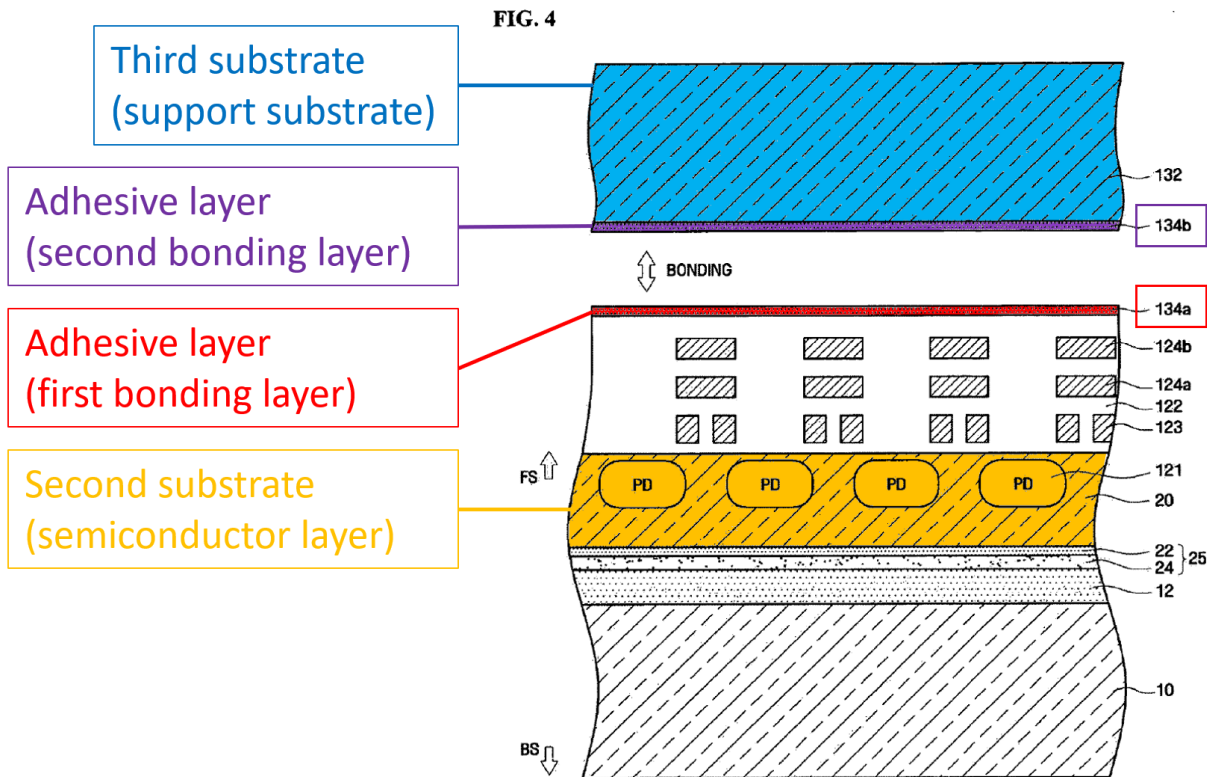


Park, Fig. 4 (annotated).

d) 24[c]: “bonding the first bonding layer to a second bonding layer disposed on the support substrate; and”

292. Park discloses this limitation.

293. Park discloses bonding the first bonding layer to an adhesive layer 134b that is disposed on the substrate 132 (i.e., the claimed second bonding layer disposed on the support substrate). Park, [0076].



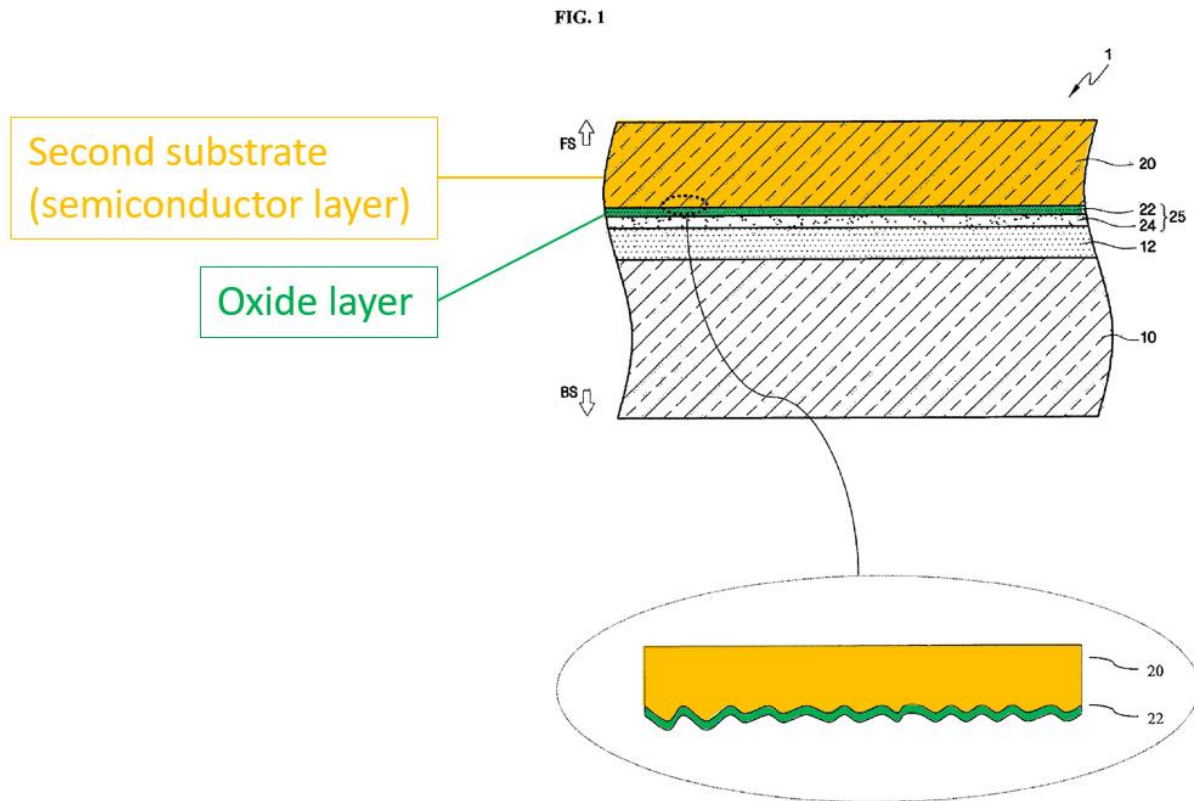
Park, Fig. 4 (annotated).

- e) **24[d]: “creating a plurality of shallow trench isolation surface features on a light incident side of said semiconductor layer.”**

294. Park in view of Baggenstoss renders this limitation obvious.²

295. Park discloses that “reflections may ... be reduced by processing the second substrate 20 to have an uneven surface.” Park, [0072]. Figure 1 depicts the second substrate 20’s uneven surface adjacent to an oxide layer 22. Park, [0060]-[0061].

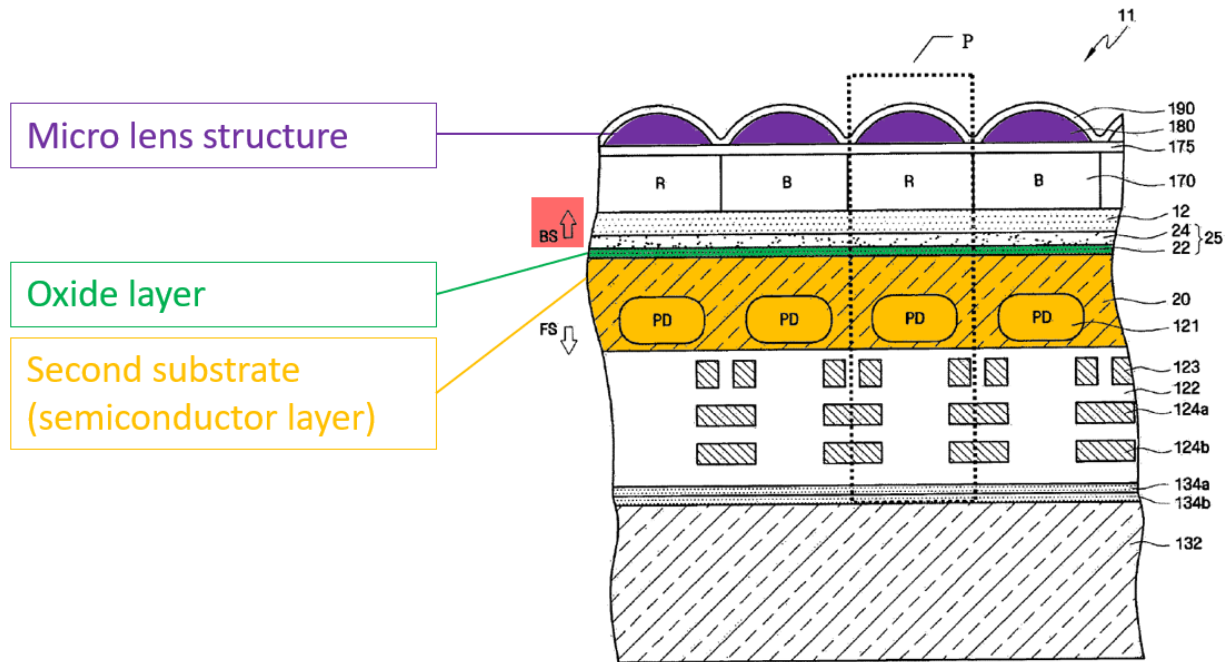
² Claim 24 does not require limitation 24[d] to be performed after limitations 24[a]-[c].



Park, Fig. 1 (annotated).

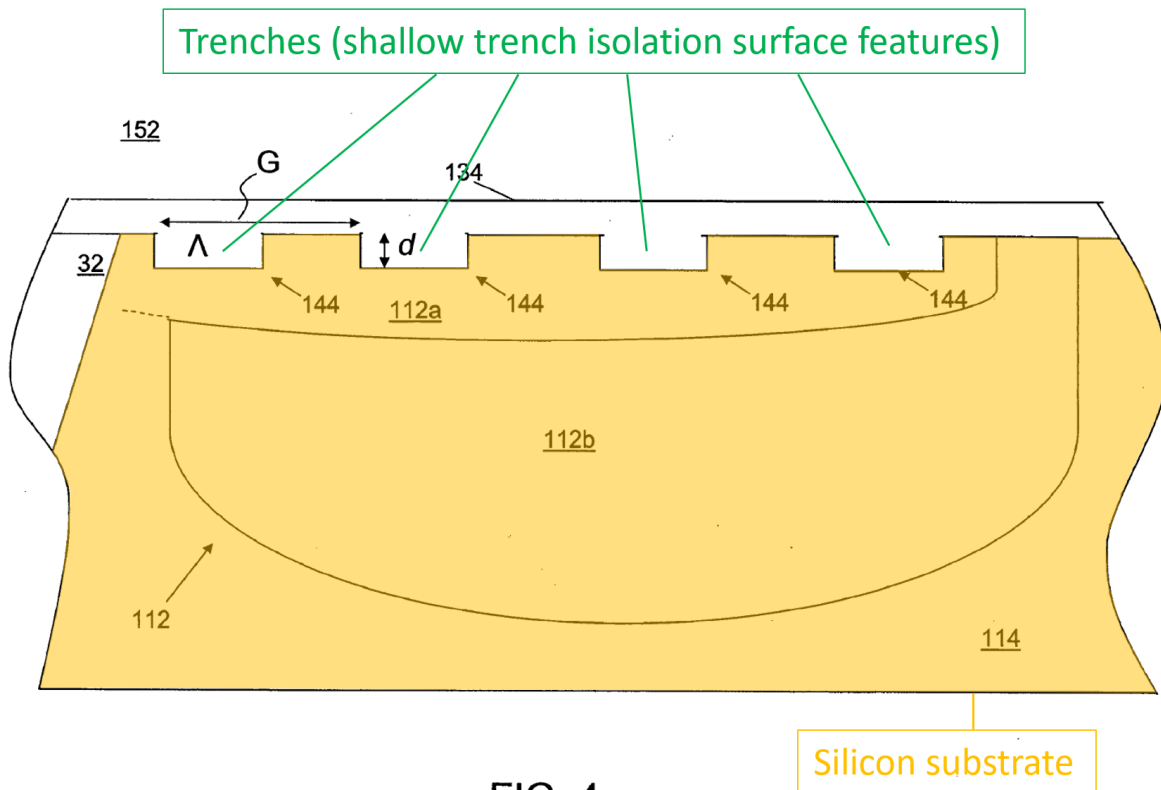
296. Park discloses that the second substrate 20's uneven surface is on the light incident side of the second substrate 20. Figure 7 depicts that the second substrate 20's uneven surface (adjacent to the oxide layer 22) is on the backside (indicated by the label "BS"), which has a micro lens structure 180 for incident light. Park, [0078]; *see also* Park, [0060] (disclosing that Park's image sensor is a backside illuminated device).

FIG. 7



Park, Fig. 7 (annotated).

297. Similarly, Baggenstoss discloses creating an optoelectronic device with a grated interface formed by trenches 144 (i.e., the claimed plurality of shallow trench isolation surface features). Baggenstoss, [0031]-[0032], [0009].



Baggenstoss, Fig. 4 (annotated).

298. Baggenstoss's trenches 144 correspond to the claimed shallow trench isolation surface features for the same reasons discussed above regarding claim 4. And Baggenstoss discloses that the trenches 144 are on the light incident side of a silicon substrate 114. Baggenstoss, Fig. 3, [0031]. It would have been obvious to use Baggenstoss's trenches in connection with Park's process for the reasons discussed above in Section VIII.I.1.

3. Claim 25

- a) **“The method of claim 24, wherein the step of creating the plurality of shallow trench isolation surface**

**features comprises generating an array of surface
features using shallow trench isolation etching.”**

299. Park in view of Baggenstoss renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case.

300. In the 737 Case, Petitioner proposed that the ’737 patent term “shallow trench isolation etching” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning, and to the extent a construction is required, it means, “etching a pattern of shallow trenches.” Ex-1014, 4; Ex-1015, 2-3.

301. Baggenstoss discloses creating an optoelectronic device with a grated interface formed by trenches 144 (i.e., the claimed plurality of shallow trench isolation surface features comprising an array of surface features). Baggenstoss, [0031]-[0032], [0009].

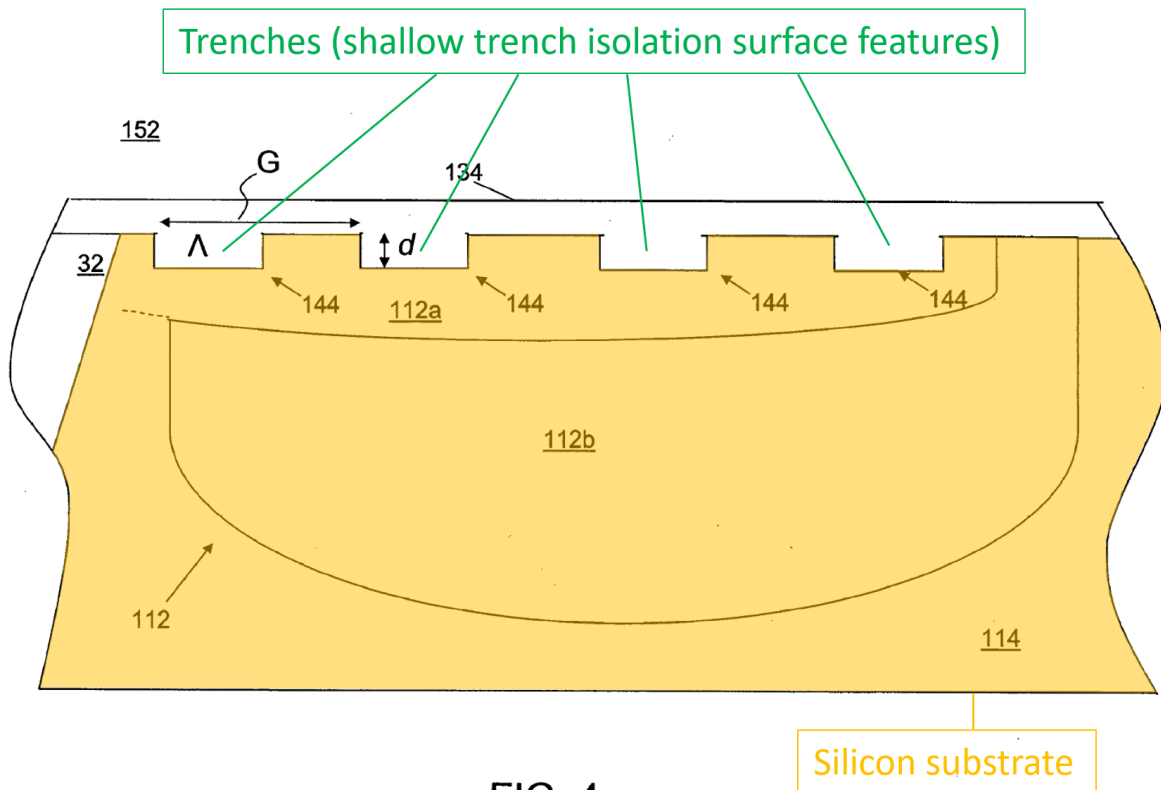


FIG. 4

Baggenstoss, Fig. 4 (annotated).

302. As discussed above regarding claim 4 in Ground A-2, Baggenstoss discloses that its shallow trench isolation surface features are formed by etching a pattern of shallow trenches. Baggenstoss, [0038].

303. Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the trenches and the shallow trench isolation in Baggenstoss, or to form both structures in the same manufacturing step, as discussed above regarding claim 4.

IX. EVIDENCE OF NON-OBVIOUSNESS

304. It is my understanding that in order for evidence of non-obviousness to be relevant, there must be a nexus between the claimed invention and the evidence. I am not aware of any evidence of non-obviousness. I reserve the right to respond to any purported objective evidence of non-obviousness raised by Patent Owner.

X. CONCLUSION

305. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

November 22, 2024
Date



Michael Lebby