

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co., Ltd.,
Petitioner,

v.

SiOnyx, LLC,
Patent Owner.

Case No. IPR2025-00064
Patent No. 10,347,682

**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO.
10,347,682 UNDER 35 U.S.C. §§ 311–319 AND 37 C.F.R. § 42.100 *et seq.***

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List of Exhibits

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1001	U.S. Patent No. 10,347,682 (the “’682 patent”)
1002	File History for U.S. Patent No. 10,347,682
1003	Provisional Application No. 61/841,326
1004	Declaration of Dr. Michael Lebby
1005	Curriculum Vitae of Dr. Michael Lebby
1006	U.S. Patent Application Publication No. 2012/0068289 (Alie)
1007	U.S. Patent Application Publication No. 2006/0081900 (Baggenstoss)
1008	Intentionally Left Blank
1009	U.S. Patent Application Publication No. 2012/0313204 (Haddad204)
1010	U.S. Patent Application Publication No. 2010/0006969 (Park)
1011	U.S. Patent No. 7,928,389 (Yap)
1012	U.S. Patent Application Publication No. 2011/0227138 (Haddad138)
1013	Samsung’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1014	SiOnyx’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1015	Email from N. Subhedar re: Claim Construction M&C Follow-Up (Sept. 8, 2024)
1016	U.S. Patent No. 8,680,591 (Haddad138 Issued Patent)
1017	U.S. Patent No. 9,496,308 (Haddad204 Issued Patent)
1018	The Authoritative Dictionary of IEEE Standard Terms (7th ed. 2000)
1019	Stephen Y. Chou et al., <i>Nanoimprint Lithography</i> , J. Vac. Sci. Technol. B 14(6), 4129-33 (1996)
1020	Gary S. May & Simon M. Sze, <i>Fundamentals of Semiconductor Fabrication</i> (2003)
1021	Provisional Application No. 61/311,004 (Haddad138-Provisional004)
1022	Provisional Application No. 61/243,434 (Haddad138-Provisional434)
1023	Provisional Application No. 61/311,107 (Haddad138-Provisional107)
1024	U.S. Patent Application Publication No. 2012/0146172 (Carey)
1025	U.S. Patent No. 7,442,629 (Mazur)
1026	U. Gösele & Q.-Y. Tong, <i>Semiconductor Wafer Bonding</i> (1998)
1027	U.S. Patent Application Publication No. 2011/0304003 (Tanida)
1028	S. Wolf, <i>Microchip Manufacturing</i> (2004)
1029	<i>Encyclopedia of Physical Science and Technology</i> (3rd ed. 2002)

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Exhibit	Description
1030	Christoph Posch, <i>Detectors, Pixels, and Signal Processing, in SMART CAMERAS</i> (Ahmed Nabil Belbachir ed., 2010)
1031	E. Fred Schubert, <i>LIGHT-EMITTING DIODES</i> (2nd ed. 2006)
1032	U.S. Patent Application Publication No. 2006/0216904 (Tong)
1033	Provisional Application No. 61/317,147 (Alie-Provisional)
1034	U.S. Patent Application Publication No. 2013/0207168 (Edwards)
1035	Maik Wiemer, et al., <i>Plasma-Activated Bonding, in Handbook of Wafer Bonding</i> (Peter Ramm, et al., eds., 2012)

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Samsung” or “Petitioner”) petitions for *inter partes* review seeking cancellation of claims 1-44 (the “Challenged Claims”) of U.S. Patent No. 10,347,682 (Ex. 1001, the “’682 patent”).

The ’682 patent purports to improve upon traditional optoelectronic devices by adding a textured layer. Figure 2 depicts an embodiment:

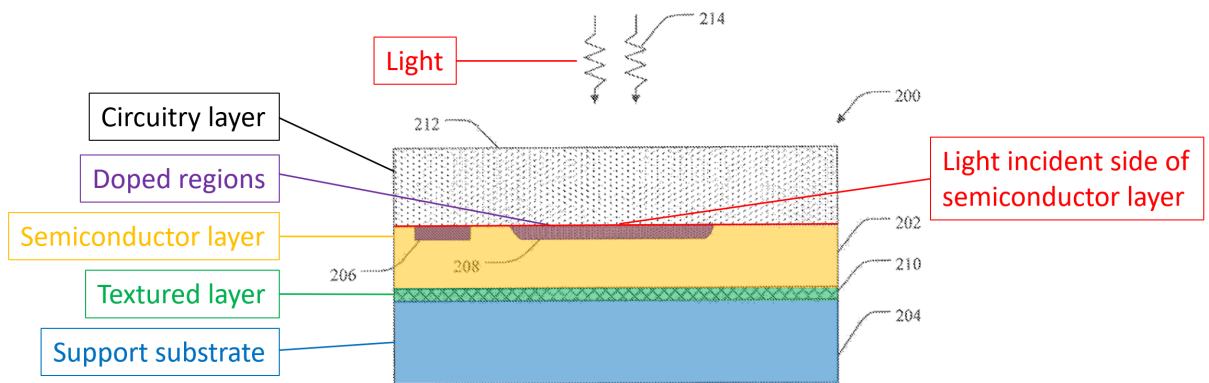


FIG. 2

’682 patent, Fig. 2 (annotated).

Light 214 comes from the top, passing through a circuitry layer 212 to reach a semiconductor layer 202. ’682 patent, 6:44-47. The semiconductor layer 202 has doped regions 206 and 208 that form a junction for sensing light. ’682 patent, 6:36-40. On the bottom side of the semiconductor layer is a textured layer containing surface features. ’682 patent, 6:40-42. The surface features of a textured layer include shapes such as “cones, pillars, pyramids, inverted features, trenches, gratings, protrusions, and the like.” ’682 patent, 9:34-36. The textured layer allegedly

functions to “diffuse light, to redirect light, and to thus increase the quantum efficiency.” ’682 patent, 9:25-27.

Although Figure 2 depicts the textured layer 210 as being located on the side of the semiconductor layer 202 *opposite* the light incident side, the independent claims of the ’682 patent require an optoelectronic device having a textured region with surface features *on* the light incident side or a method of making the same. The ’682 patent does not identify any advantage to having a textured region on the light incident side. This feature, however, was known in the prior art, and all of the prior art references relied on in this Petition explain that having a textured region on the light incident side provides additional scattering of light into the semiconductor layer or reduces reflection away from the semiconductor layer.

For example, Haddad138, which is prior art to the ’682 patent, discloses an optoelectronic device having a textured region with surface features on the light incident side of a semiconductor layer. Like the textured region of the ’682 patent, Haddad138’s textured region includes surface features in the shapes of “cones, pyramids, pillars, protrusions, micro lenses, quantum dots, inverted features and the like.” Haddad138, [0063]. Haddad138’s “textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad138, [0063]. Grounds A-1 to 8 show how Haddad138 alone or in

combination with other references anticipates or renders obvious claims 1-23 and 26-44.

A patent application filed by Petitioner and published before the priority date of the '682 patent also discloses a method of making an optoelectronic device having a textured region with surface features on the light incident side. Park, [0072], Figs. 1, 4, 7. Ground B-1 shows how Park in combination with another reference renders obvious claims 24-25.

II. STANDING, MANDATORY NOTICES, AND FEE AUTHORIZATION

A. Grounds for Standing

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '682 patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the '682 patent on the grounds identified in this petition.

B. Real Parties-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

C. Related Matters

Petitioner identifies the following related matter.

- *SiOnyx, LLC v. Samsung Electronics, Co., Ltd.*, 2:24-cv-00408 (E.D. Tex.)

D. Counsel Information

Petitioner designates the following counsel:

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Pursuant to 37 C.F.R. § 42.10 (b), Petitioner has filed a power of attorney with the above designation of counsel.

E. Service Information

Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail at the email addresses above and at Samsung-SiOnyx-IPR-Cov@cov.com.

F. Payment of Fees Under 37 C.F.R. §42.103

This petition is accompanied by the fees set forth in 37 C.F.R. § 42.15(a). Please charge or credit Deposit Account No. 60-3160 with any shortage or overpayment of fees associated with this petition and any other fees incurred by Petitioner.

III. SUMMARY OF CHALLENGE

- ***Ground A-1:*** Claims 1-3, 6-8, 11-12, 15-18, 21, and 26-27 are anticipated, or at a minimum, obvious based on Haddad138.
- ***Ground A-2:*** Claims 4-5, 14, and 21-22 are obvious based on Haddad138 and Baggenstoss.
- ***Ground A-3:*** Claims 9-10, 13, 19-20, 28-31, and 34-42 are obvious based on Haddad138 and Alie.
- ***Ground A-4:*** Claim 23 is obvious based on Haddad138 and Haddad204.
- ***Ground A-5:*** Claim 23 is obvious based on Haddad138 and Park.
- ***Ground A-6:*** Claims 32-33 and 42-43 are obvious based on Haddad138, Alie, and Baggenstoss.
- ***Ground A-7:*** Claim 44 is obvious based on Haddad138, Alie, and Haddad204.
- ***Ground A-8:*** Claim 44 is obvious based on Haddad138, Alie, and Park.
- ***Ground B-1:*** Claims 24-25 are obvious based on Park and Baggenstoss.

The '682 patent was filed on June 5, 2017 and claims priority to a provisional application filed on June 29, 2013. Each of the asserted references is available as prior art under 35 U.S.C. § 102 (AIA),¹ as shown in the following table.

¹ Because both the application and the provisional application for the '682 patent were filed after March 16, 2013, the AIA conditions for patentability apply.

Exhibit	Reference	Date(s)	Availability as Prior Art
1012	U.S. Patent Application Publication No. 2011/0227138 (Haddad138)	September 22, 2011 (published)	§ 102(a)(1) & (2)
1007	U.S. Patent Application Publication No. 2006/0081900 (Baggenstoss)	April 20, 2006 (published)	§ 102(a)(1) & (2)
1006	U.S. Patent Application Publication No. 2012/0068289 (Alie)	March 22, 2012 (published)	§ 102(a)(1) & (2)
1009	U.S. Patent Application Publication No. 2012/0313204 (Haddad204)	December 13, 2012 (published)	§ 102(a)(1) & (2)
1010	U.S. Patent Application Publication No. 2010/0006969 (Park)	January 14, 2010 (published)	§ 102(a)(1) & (2)

IV. THE '682 PATENT

A. Overview of the '682 Patent

The '682 patent states that silicon imaging devices were widely used, including in both front side illumination (FSI) and backside illumination (BSI) configurations. '682 patent, 1:16-29; *see also* Ex-1004 ¶¶41-47. In an FSI device, incident light enters the device by “first passing by transistors and metal circuitry.” '682 patent, 5:60-62. In a BSI device, on the other hand, “incident light

enters the device via the light sensitive region opposite the circuitry.” ’682 patent, 6:4-6.

The ’682 patent purports to improve upon traditional optoelectronic devices by adding a textured layer, as discussed above in Section I. Figure 2 depicts an FSI embodiment with a textured layer:

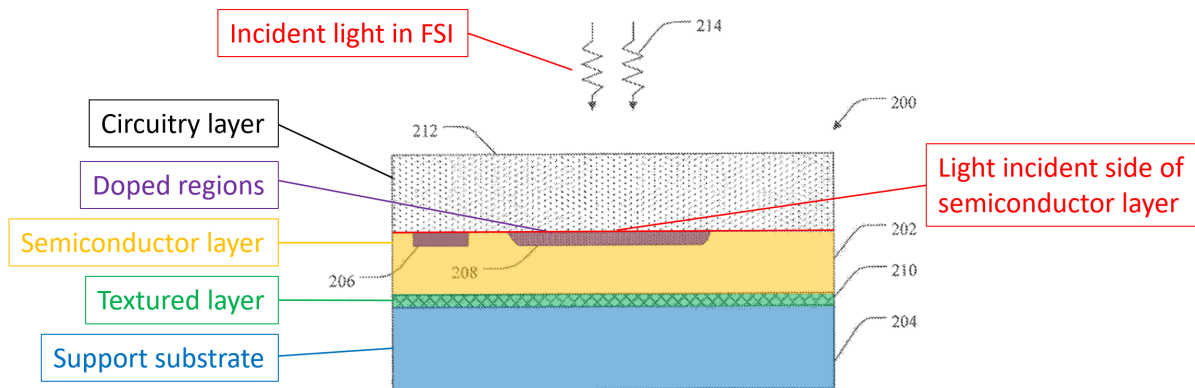
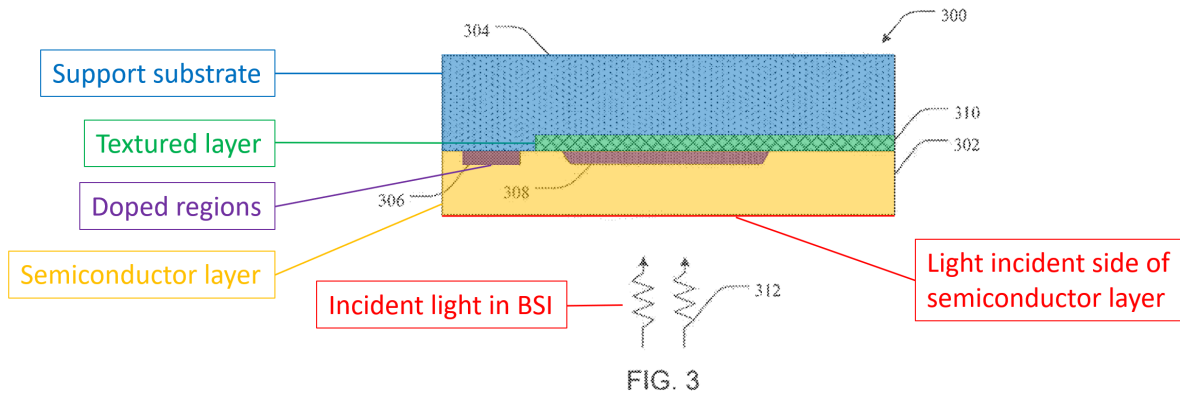


FIG. 2

’682 patent, Fig. 2 (annotated).

The Figure 2 device is an FSI device because light 214 enters the device from the top, first passing through a circuitry layer 212 before reaching a semiconductor layer 202. ’682 patent, 6:44-47.

Figure 3 depicts a BSI embodiment with a textured layer:



'682 patent, Fig. 3 (annotated).

The Figure 3 device is a BSI device because light 312 enters the device from the bottom, reaching a semiconductor layer 302 without passing through a circuitry layer. '682 patent, 6:63-65.

Unlike the independent claims of the '682 patent, which all require a textured region *on* the light incident side, both Figures 2 and 3 depict a textured layer (green) on a side of the semiconductor layer (yellow) *opposite* the light incident side. The '682 patent does not include a figure with a textured layer or region *on* the light incident side or identify any advantage to such a configuration. The '682 patent, though, notes that “the textured region can be located on the light incident side of the semiconductor material,” as well as being located “on a side of the semiconductor material opposite the light incident side, or both on the light incident side and opposite the light incident side.” '682 patent, 7:43-48.

B. Prosecution History

The '682 patent was filed on June 5, 2017, claiming priority to Provisional Application No. 61/841,326, filed on June 29, 2013.

Following an office rejection, the applicant added to claim 1 two limitations in an attempt to overcome the cited prior art: (1) shallow trench isolation surface features being located on the light incident side, and (2) a first bonding layer. Ex-1002 at 70. After another office rejection, the applicant added to claim 1 the limitation of “wherein said optoelectronic device is a photosensitive imager device capable of detecting visible and infrared electromagnetic radiation.” Ex-1002 at 110. The applicant also added to claim 17 (issued as claim 24) the limitation of bonding a first bonding layer to a second bonding layer. Ex-1002 at 111.

The examiner issued a notice of allowance, noting that the cited prior art did not disclose “a support substrate coupled to said semiconductor layer and a first bonding layer disposed between the semiconductor layer and the support substrate” and “bonding the first bonding layer to a second bonding layer disposed on the support substrate.” Ex-1002 at 1629.

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) as of June 2013 would have had a bachelor’s degree in engineering, physics, or a related or equivalent field, and two or more years of experience researching, developing, designing, and/or

evaluating image sensors using photonics. Ex-1004 ¶52. A person with less or different education but more relevant practical experience, or vice versa, may also meet this standard. Ex-1004 ¶52.

VI. CLAIM CONSTRUCTION

In IPR proceedings, claims are construed in accordance with their “ordinary and customary meaning” in light of the specification. 37 C.F.R. § 42.100(b); *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005). For purposes of this petition, Petitioner does not believe that any specialized constructions are necessary.

U.S. Patent No. 11,069,737 (the “’737 patent”) is a continuation of the ’682 patent, and shares the same specification and the same or similar claim terms with the ’682 patent. SiOnyx, LLC (“SiOnyx” or “Patent Owner”) asserted the ’737 patent against Petitioner in *Sensors with Pixels and Products Containing the Same*, Inv. No. 337-TA-1403 (ITC) (“’737 Case”). In the ’737 Case, Petitioner and Patent Owner have proposed competing constructions for certain terms of the ’737 patent. *See* Ex-1013; Ex-1014; Ex-1015. For the limitations of the ’682 patent that include a term that is the same as or similar to a disputed term from the ’737 Case, both Petitioner’s and Patent Owner’s proposed constructions are identified and addressed in Section VIII below.

VII. OVERVIEW OF THE PRIOR ART

A. Haddad138 (Ex-1012)

Haddad138 is prior art because it was published on September 22, 2011, which is more than one year before the '682 patent's provisional application filing date of June 29, 2013.

Although Haddad138 was listed in an information disclosure statement (IDS) along with almost 900 other documents, it was not discussed during prosecution.

The named inventors of the '682 patent, Homayoon Haddad and Jutao Jiang, are also joint inventors of Haddad138. The '682 patent's provisional application incorporates the Haddad138's patent application by reference, referring to Haddad138 for "[f]urther details regarding both BSI and FSI photodiodes, pixels, imagers, and other optoelectronic devices." Ex-1003, 9:18-20.

Like the '682 patent, Haddad138 discloses an optoelectronic device having a textured region with surface features. Ex-1004 ¶¶58-61. Figure 9 depicts an example optoelectronic device with a textured region 90. Haddad138, [0087].

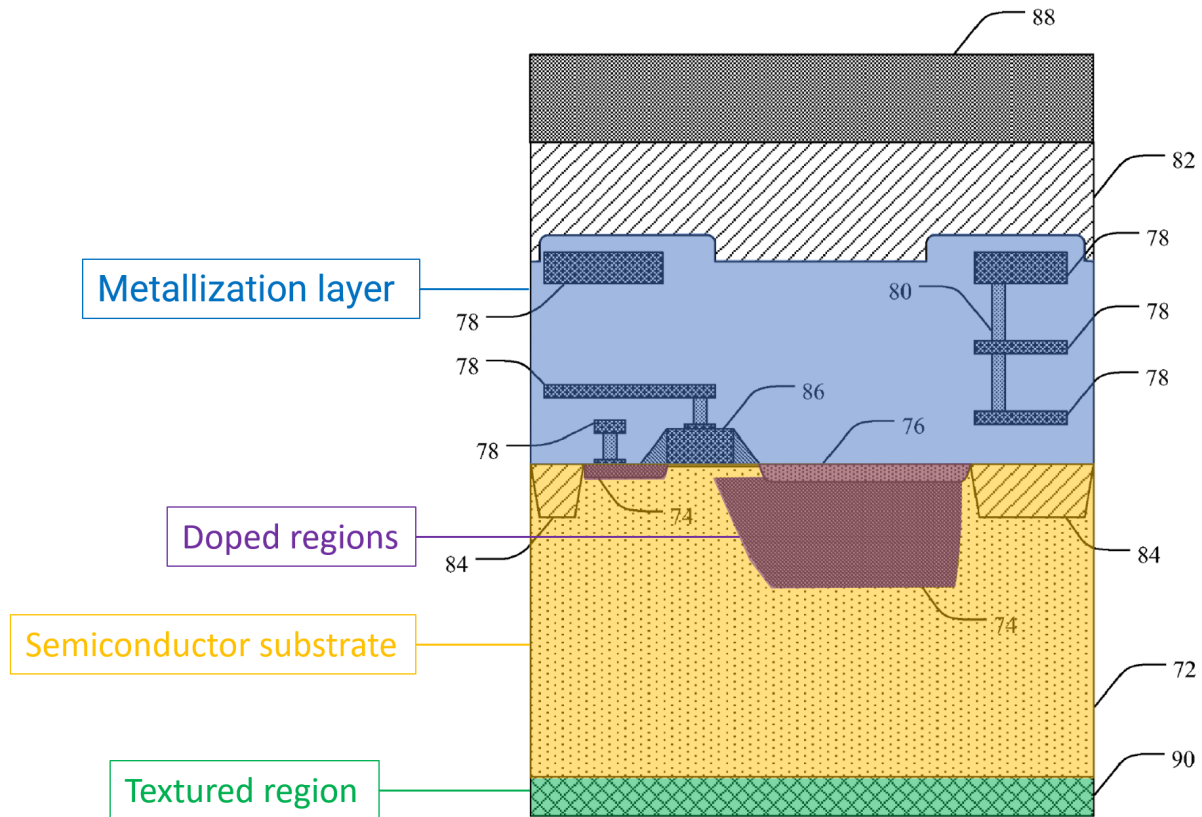


FIG. 9

Haddad138, Fig. 9 (annotated).

Like the '682 patent, Haddad138 discloses that its devices “can be adapted for either [FSI or BSI] configuration.” Haddad138, [0048]. “In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry.” Haddad138, [0048]. The Figure 9 device has such a metallization layer on the top side of the semiconductor substrate. Haddad138, [0085]. When the Figure 9 device is adapted for an FSI configuration, therefore, incident light would enter from the top, similar to the FSI device depicted in Figure 2 of the '682 patent. *See* Haddad138, [0048]; *see also* Haddad138, [0049] (explaining that, in an FSI

configuration, “light enters the semiconductor substrate from the direction of the multiple doped regions”); Ex-1004 ¶¶39-40, 60.

When the Figure 9 device is adapted for a BSI configuration, incident light would enter from the bottom, similar to the BSI device depicted in Figure 3 of the ’682 patent. *See* Haddad138, [0048] (disclosing that in BSI imagers incident light is “mostly absorbed prior to reaching the circuitry”); *see also* Ex-1004 ¶¶39-40, 61. A BSI adaptation of the Figure 9 device is further discussed below regarding limitation 1[b].

B. Baggenstoss (Ex-1007)

Baggenstoss is prior art because it was published on April 20, 2006, which is more than one year before the ’682 patent’s provisional application filing date of June 29, 2013.

Baggenstoss was not listed in an IDS and was not discussed during prosecution. A parent application (of which Baggenstoss is a divisional) was listed in an IDS along with almost 900 other documents, but it was not discussed during prosecution.

Baggenstoss discloses an optoelectronic device with a textured region in the form of a grated interface formed by trenches (elements 144 in Figure 4, below). Baggenstoss, [0031]-[0032], [0009]; *see also* Ex-1004 ¶¶62-66.

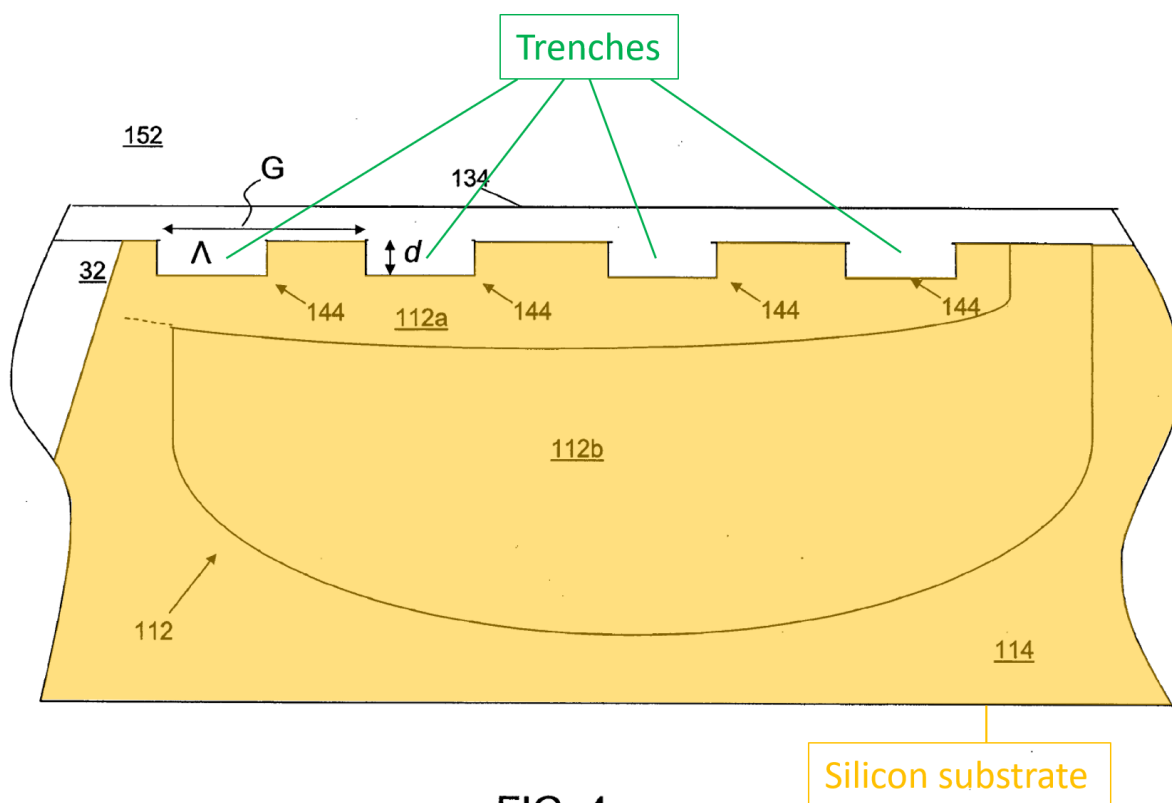


FIG. 4

Baggenstoss, Fig. 4 (annotated).

In another embodiment, Baggenstoss discloses an optoelectronic device with a textured region in the form of “blazed (or step-wise)” gratings formed of trenches (elements 244 in Figure 11, below). Baggenstoss, [0042].

The '682 patent incorporates by reference—but does not claim priority to—Alie's patent application, referring to Alie for "[f]urther details regarding substrates, bonding, and various imager details." '682 patent, 7:21-24.

Figure 5 depicts an example optoelectronic device with a textured region 36. Alie, [0096]; *see also* Ex-1004 ¶¶67-72.

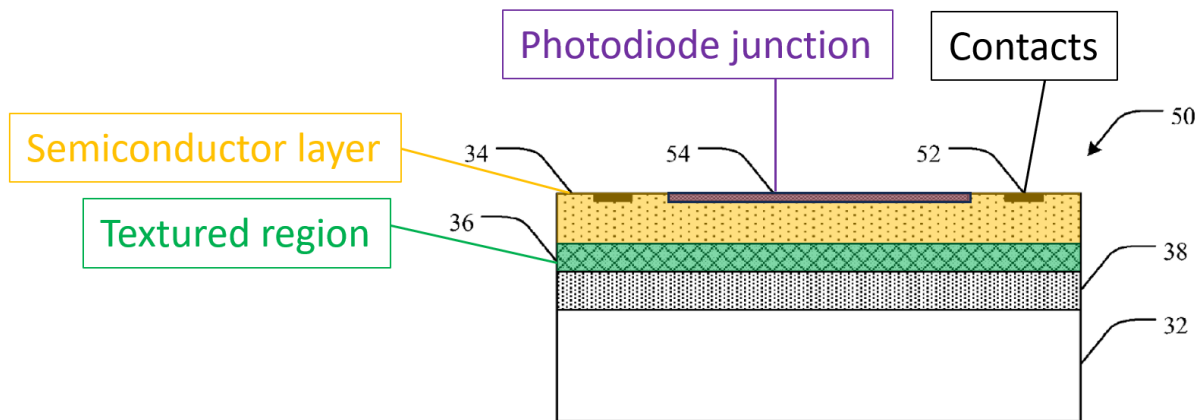


FIG. 5

Alie, Fig. 5 (annotated).

Like the '682 patent, Alie discloses that its devices can be adapted for either an FSI architecture or a BSI architecture. Alie, [0053].

D. Haddad204 (Ex-1009)

Haddad204 is prior art because it was published on December 13, 2012, which predates the '682 patent's provisional application filing date of June 29, 2013.

Although Haddad204 was listed in an IDS along with almost 900 other documents, it was not discussed during prosecution.

Like the '682 patent, Haddad204 discloses an optoelectronic device with a textured region including surface features. Haddad204, [0073], [0053]; *see also* Ex-1004 ¶¶73-76. In particular, Haddad204 discloses “a plurality of pillars of variable sizes ... arranged in a non-uniform array.” Haddad204, [0112]; *see also* Ex-1004 ¶75. Figure 9a shows a top view and Figure 9b shows a cross-sectional view of such “pillars etched into a semiconductor material.” Haddad204, [0112].

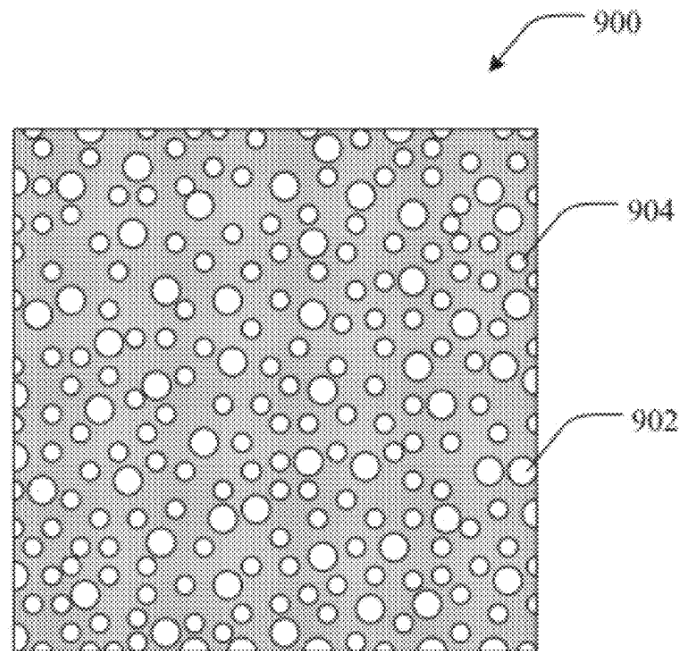


FIG. 9a

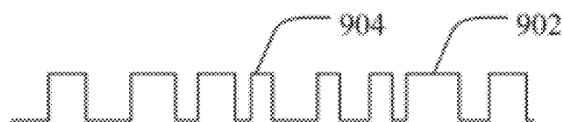


FIG. 9b

Haddad204, Figs. 9a-b.

Haddad204 discloses that textured regions can be placed on both sides of a semiconductor layer, including the light incident side. Haddad204, [0111].

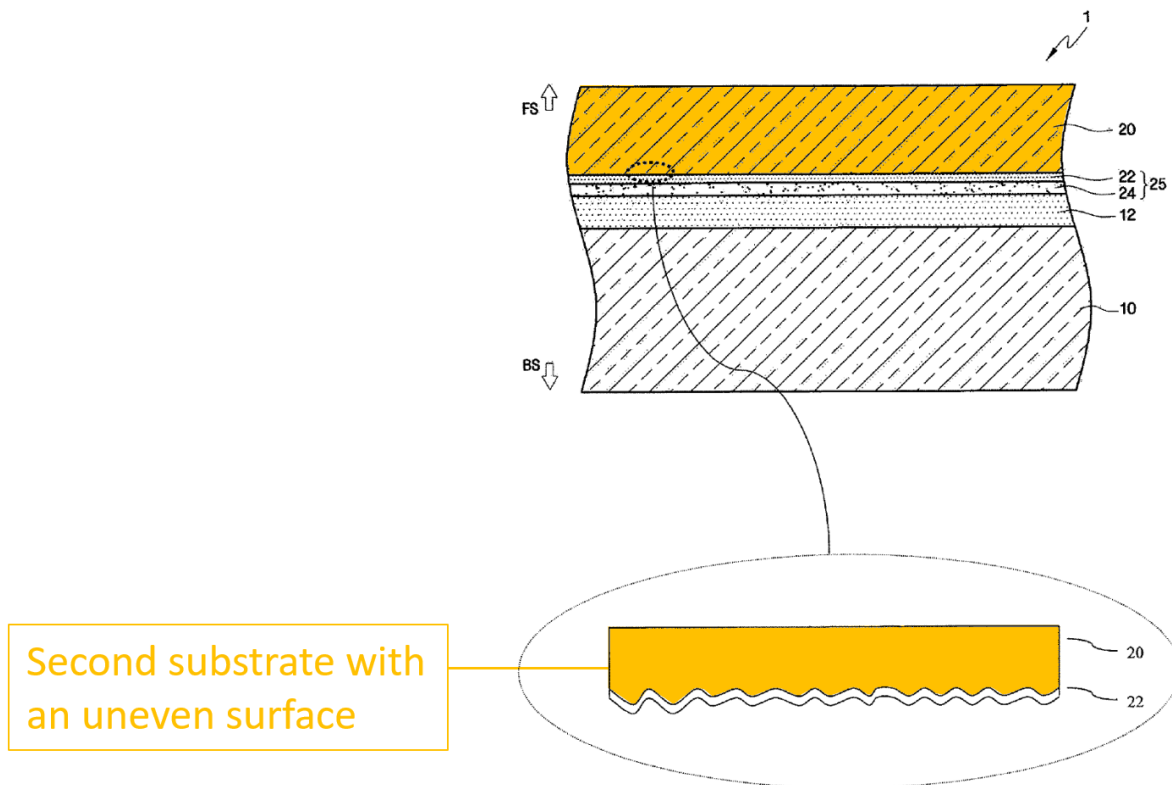
E. Park (Ex-1010)

Park is prior art because it was published on January 14, 2010, which is more than one year before the '682 patent's provisional application filing date of June 29, 2013.

Park was not listed in an IDS and was not discussed during prosecution.

Like the '682 patent, Park discloses an optoelectronic device with a textured region including surface features. Park, [0072], [0059]; *see also* Ex-1004 ¶¶77-80.

FIG. 1



Park, Fig. 1.

Park's uneven surface is located on the light incident side of a semiconductor layer. Park, Figs. 1 & 7.

VIII. APPLICATION OF PRIOR ART TO THE CHALLENGED CLAIMS

A. Ground A-1: Claims 1-3, 6-8, 11-12, 15-18, 21, and 26-27 Are Anticipated, or at a Minimum, Obvious Based on Haddad138

1. Claim 1

a) 1[pre]: “An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:”

Haddad138 discloses the preamble to the extent it is limiting. Ex-1004 ¶¶81-82.

Haddad138 discloses “photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation.” Haddad138, [0045]. Ex-1004 ¶82. Haddad138 explains that its devices have an enhanced ability to absorb electromagnetic radiation compared to “[t]raditional silicon photodetecting imagers [that] have limited light absorption/detection properties.” Haddad138, [0044]. Specifically, Haddad138 discloses a device with a textured region, Haddad138, [0087], which can function to “absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad138, [0063]; *see also* Haddad138, [0070]

(“the textured surface can *increase the probability of incident radiation being absorbed by the semiconductor material*”).²

- b) 1[a]: “a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,”

Haddad138 discloses this limitation. Ex-1004 ¶¶83-86.

Figure 9 depicts a photosensitive pixel device containing a semiconductor substrate 72 (i.e., the claimed semiconductor layer) having multiple doped regions 74 and 76. Haddad138, [0084]; *see also* Ex-1004 ¶84.

² All emphases in quotes have been added, unless otherwise stated.

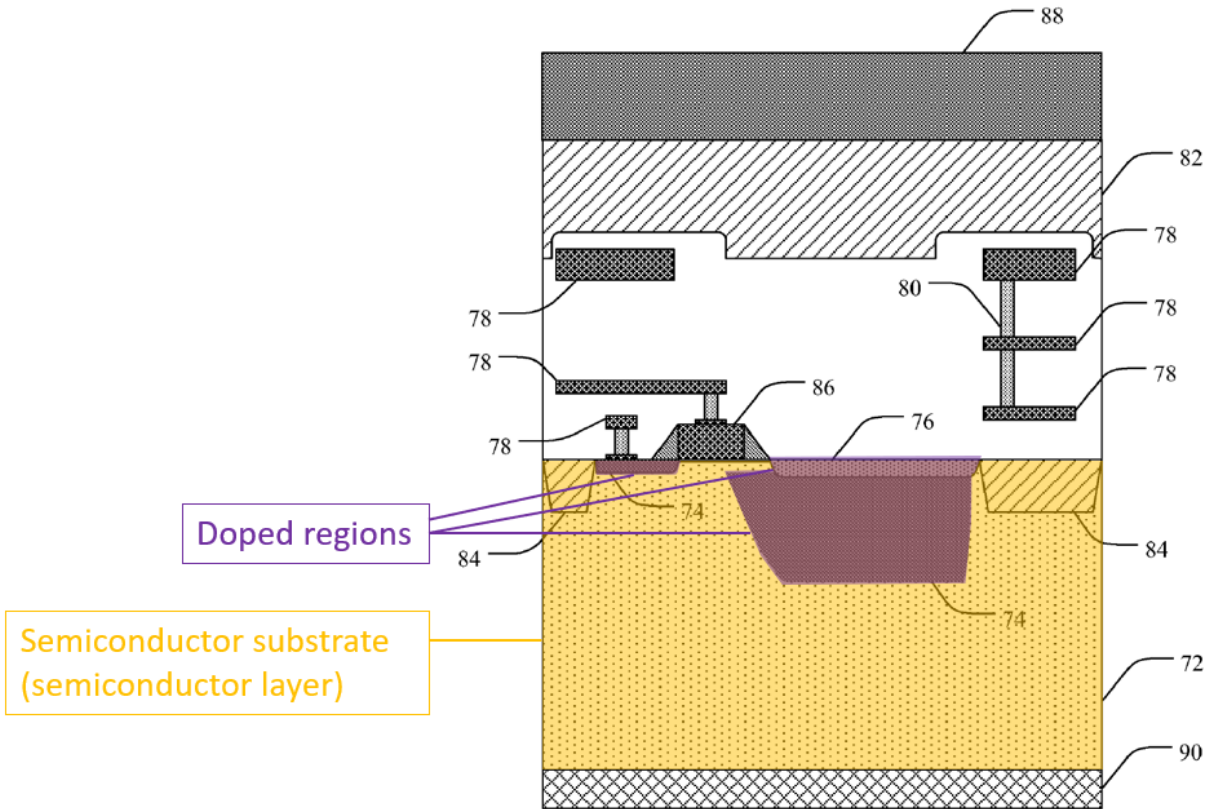


FIG. 9

Haddad138, Fig. 9 (annotated).

As Dr. Lebby explains, the doped regions form at least one junction. Ex-1004 ¶85 (citing Ex-1018, 598; Ex-1018, 309; Haddad138, [0049], [0084]). Indeed, Haddad138 expressly states that similar doped regions in Figure 1 “form[] at least one junction.” Haddad138, [0049].

As depicted in Figure 9, the semiconductor substrate 72 has a top surface and a bottom surface, which correspond to the claimed light incident side and the opposed side. Ex-1004 ¶86. The surface corresponding to the claimed light incident

side depends on whether the Figure 9 device is adapted for an FSI configuration (in which case the top surface is the light incident side) or for a BSI configuration (in which case the bottom surface is the light incident side), as discussed above in Section VII.A. Ex-1004 ¶86.

- c) **1[b]: “a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶87-98.

- (1) **“a textured region comprising a plurality of shallow trench isolation surface features”**

Haddad138 discloses a textured region having surface features (i.e., the claimed shallow trench isolation surface features). Haddad138, [0063]; *see also* Ex-1004 ¶88. As Dr. Lebby explains, Haddad138’s surface features have the same structures as the shallow trench isolation surface features described in the specification of the ’682 patent. Ex-1004 ¶88. Haddad138 discloses that “nonlimiting examples of [surface feature morphologies] include cones, pillars, pyramids, ... inverted features, and combinations thereof.” Haddad138, [0006]. These are the same shapes and configurations that the ’682 patent provides as examples of shallow trench isolation surface features. ’682 patent, 9:34-37 (“Non-limiting examples of such shapes and configurations include cones, pillars, pyramids,

inverted features ... and the like, including combinations thereof.”); *see also* ’682 patent, cl. 12 (“shallow trench isolation surface features comprise pyramids”). Haddad138 also discloses that its surface features can have a height of “50 nm to 20 μ m,” Haddad138, [0070], just like the surface features of the ’682 patent, ’682 patent, cl. 11; *see also* Ex-1004 ¶88. Both Haddad138 and the ’682 patent describe the same or similar processes for creating the shallow trench isolation surface features. Ex-1004 ¶89. Both Haddad138 and the ’682 patent explain that their shallow trench isolation surface features serve the same function. Ex-1004 ¶90.

Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the surface features and the shallow trench isolation in Haddad138. Ex-1004 ¶91. Haddad138 discloses forming shallow trench isolation. Haddad138, [0085]. As Dr. Lebby explains, the process for creating shallow trench isolation was well known. Ex-1004 ¶91. Creating the surface features using the same process as the process for the shallow trench isolation would generate predictable results, and reduce the costs associated with developing a new process. Ex-1004 ¶91. This would involve employing a known technique to improve similar devices in the same way. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007); Ex-1004 ¶91. A POSITA would have had a reasonable expectation of success because Haddad138 already discloses using

shallow trench isolation in its devices, and, as Dr. Lebby discusses, it was well known how to use a shallow trench isolation process to form surface features. Haddad138, [0066], [0085]; Ex-1034, [0010]-[0012]; *see also* Ex-1004 ¶91.

(2) “located on the light incident side of the semiconductor layer”

Haddad138 discloses, or at a minimum, renders obvious locating the claimed shallow trench isolation surface features on the light incident side of the semiconductor layer. Figure 9 depicts a textured region 90 having surface features. Haddad138, [0087], [0063]; *see also* Ex-1004 ¶92.

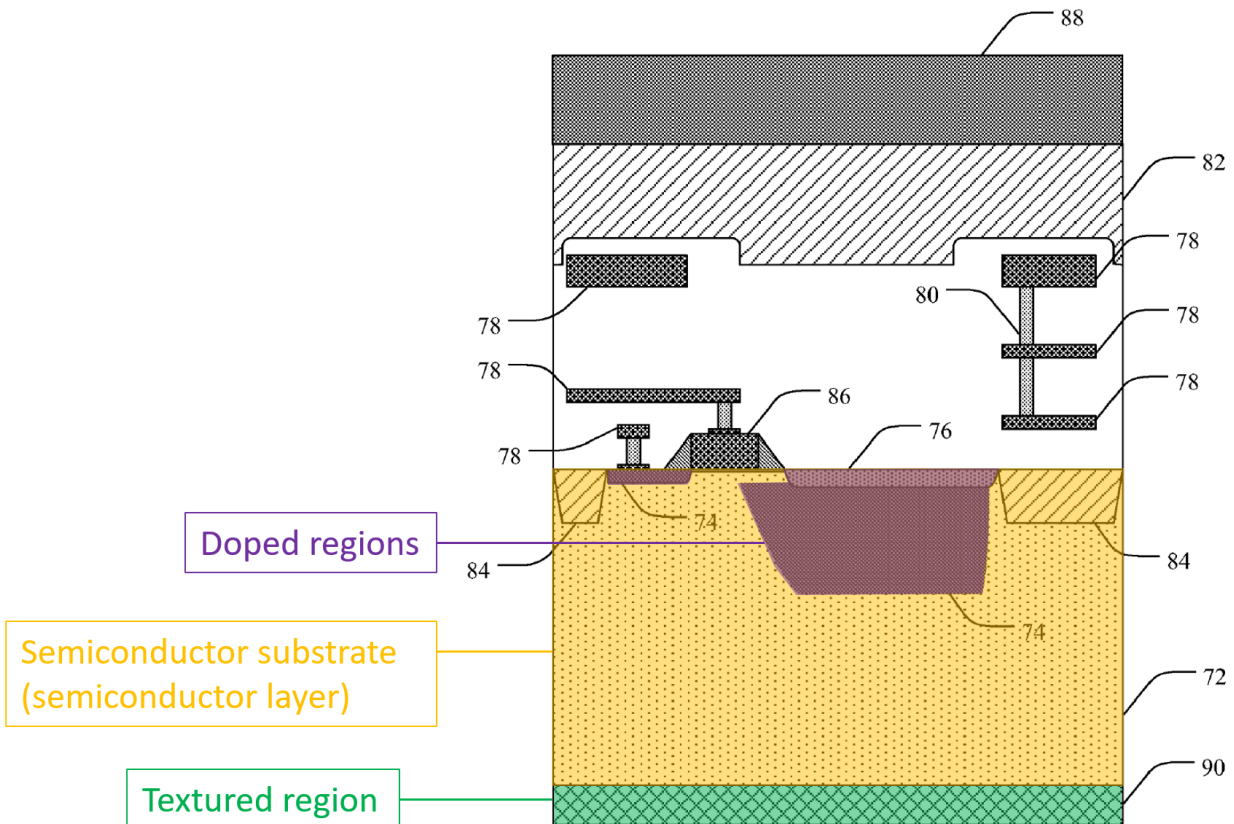
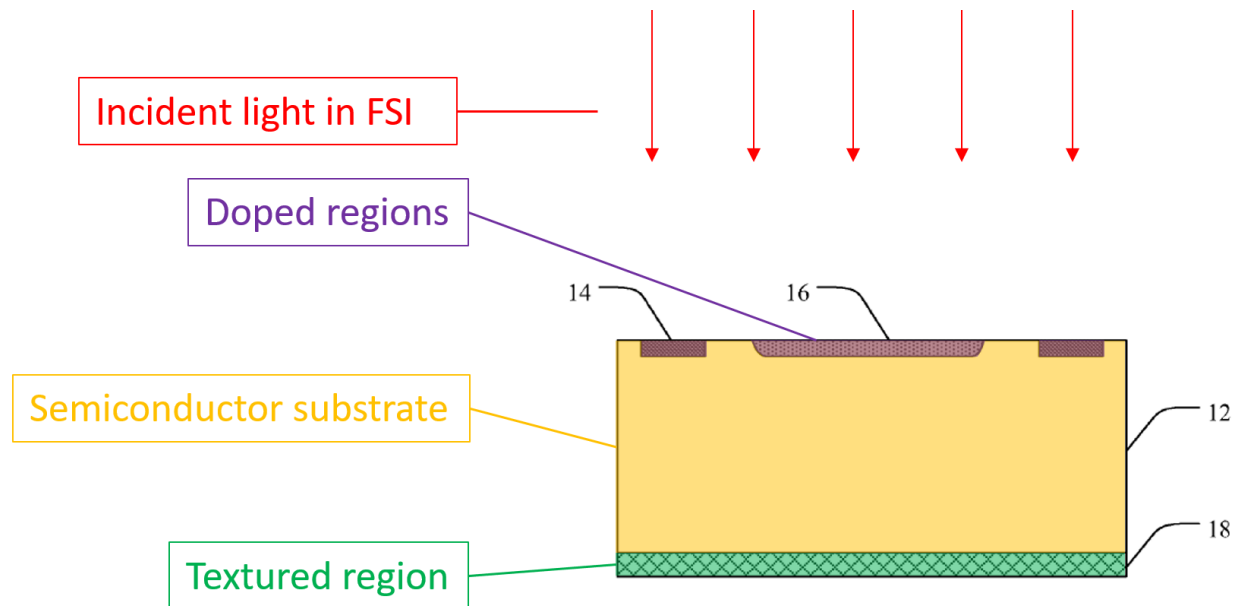


FIG. 9

Haddad138, Fig. 9 (annotated).

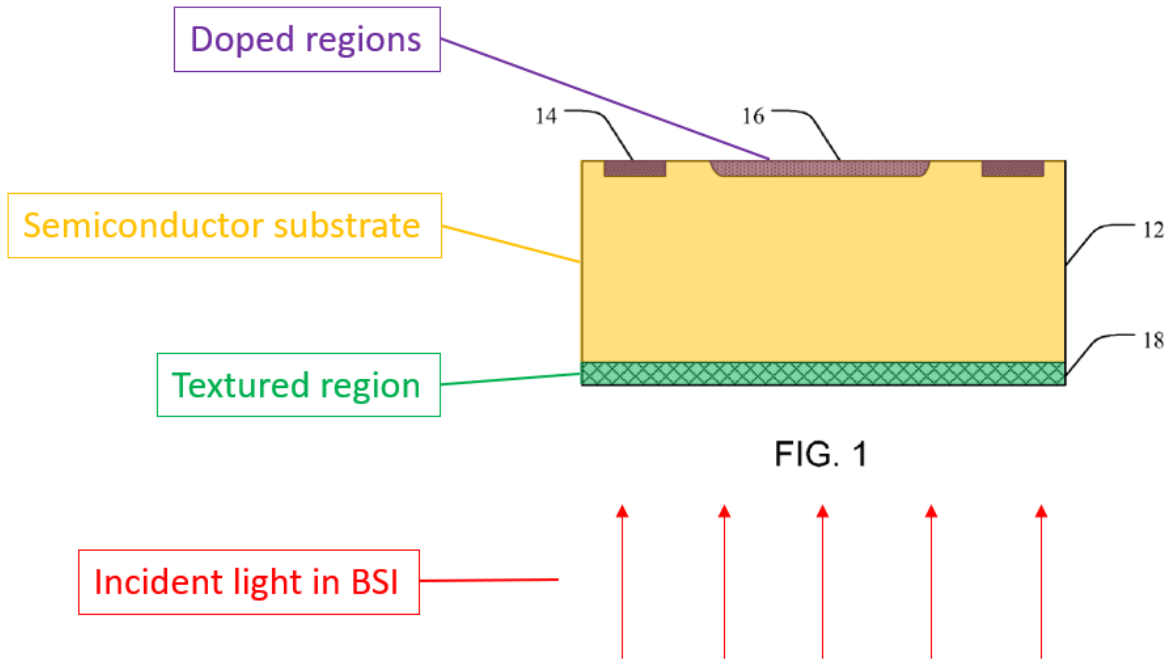
Haddad138 discloses that its devices “can be adapted for either [FSI or BSI] configuration.” Haddad138, [0048]. Haddad138 illustrates such adaptations with reference to Figure 1, which depicts a semiconductor substrate 12 and a textured region 18, similar to the semiconductor substrate and textured region depicted in Figure 9. Haddad138 explains that the Figure 1 device is “a FSI design where light enters the semiconductor substrate from the direction of the multiple doped regions.” Haddad138, [0049]. In other words, in an FSI configuration, incident light would enter the Figure 1 device from the top. Ex-1004 ¶93.



Ex-1012, Fig. 1 (annotated and modified to show incident light).

Haddad138 teaches, however, that the Figure 1 device “can be configured with a BSI architecture, and thus *electromagnetic radiation would enter the semiconductor substrate from the direction of the textured region.*” Haddad138,

[0049]. In other words, in a BSI configuration, incident light would enter the Figure 1 device from the bottom. Ex-1004 ¶94.



Ex-1012, Fig. 1 (annotated and modified to show incident light).

Similarly, when the Figure 9 device is adapted for a BSI configuration (as Haddad138 discloses), incident light would enter the device from the direction of the textured region, i.e., the bottom side. Ex-1004 ¶¶39-40, 95. In a BSI configuration of the Figure 9 device, therefore, the surface features of the textured region 90 correspond to the claimed shallow trench isolation surface features located on the light incident side of the semiconductor layer. Ex-1004 ¶¶95-97.

(3) “configured to interact with incident electromagnetic radiation”

Haddad138 discloses that its textured region is “positioned to interact with electromagnetic radiation.” Haddad138, [0003], [0049]; *see also* Ex-1004 ¶98. Specifically, Haddad138 discloses that the textured region “can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation.” Haddad138, [0063]. Haddad138 discloses that this interaction is facilitated by surface features of the textured region, i.e., the surface features are configured to interact with incident electromagnetic radiation. Haddad138, [0063].

d) 1[c]: “a support substrate coupled to said semiconductor layer, and”

Haddad138 discloses this limitation. Ex-1004 ¶¶99-101.

Figure 9 depicts a carrier support substrate 88 (i.e., the claimed support substrate) coupled to a semiconductor substrate 72 (i.e., the claimed semiconductor layer) via a passivation layer 82 and a metallization layer containing metal regions 78. Haddad138, [0086]-[0088]; *see also* Ex-1004 ¶100.

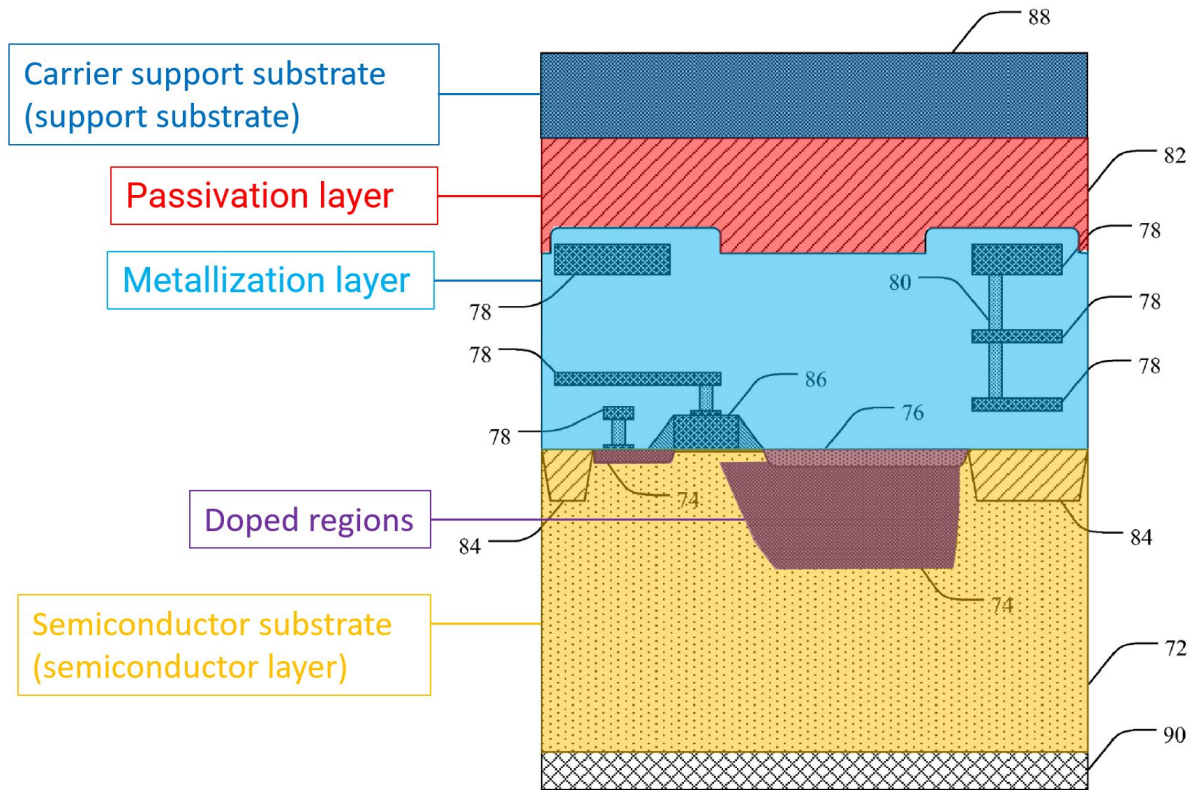


FIG. 9

Haddad138, Fig. 9 (annotated).

Haddad138 teaches that the support substrate 88 may be present in the optoelectronic device upon completion of manufacturing. Ex-1004 ¶101. Indeed, Figures 10 and 11 disclose alternatives to the Figure 9 embodiment in which a second carrier support substrate is added or the substrate is removed, respectively. Haddad138, [0088] (“As is shown in FIG. 10, an additional carrier support substrate 100 *can* be coupled.... A reflective layer 102 *can* be disposed....”), [0089] (“As is shown in FIG. 11, the carrier support substrate *can* be removed”). Thus, a POSITA would understand that, in at least some embodiments, Haddad138’s device would include the support substrate. Ex-1004 ¶101.

e) **1[d]: “a first bonding layer disposed between the semiconductor layer and the support substrate,”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶102-03.

Haddad138 discloses that “[t]he carrier substrate can be coupled to the photosensing pixel [including the semiconductor layer] by various techniques” including “by way of a bonding layer” (i.e., the claimed first bonding layer). Haddad138, [0086]; *see also* Ex-1004 ¶103. One of Haddad138’s provisional applications, to which Haddad138 claims priority and incorporates by reference, illustrates such a bonding layer. Haddad138-Provisional004, 4-5.

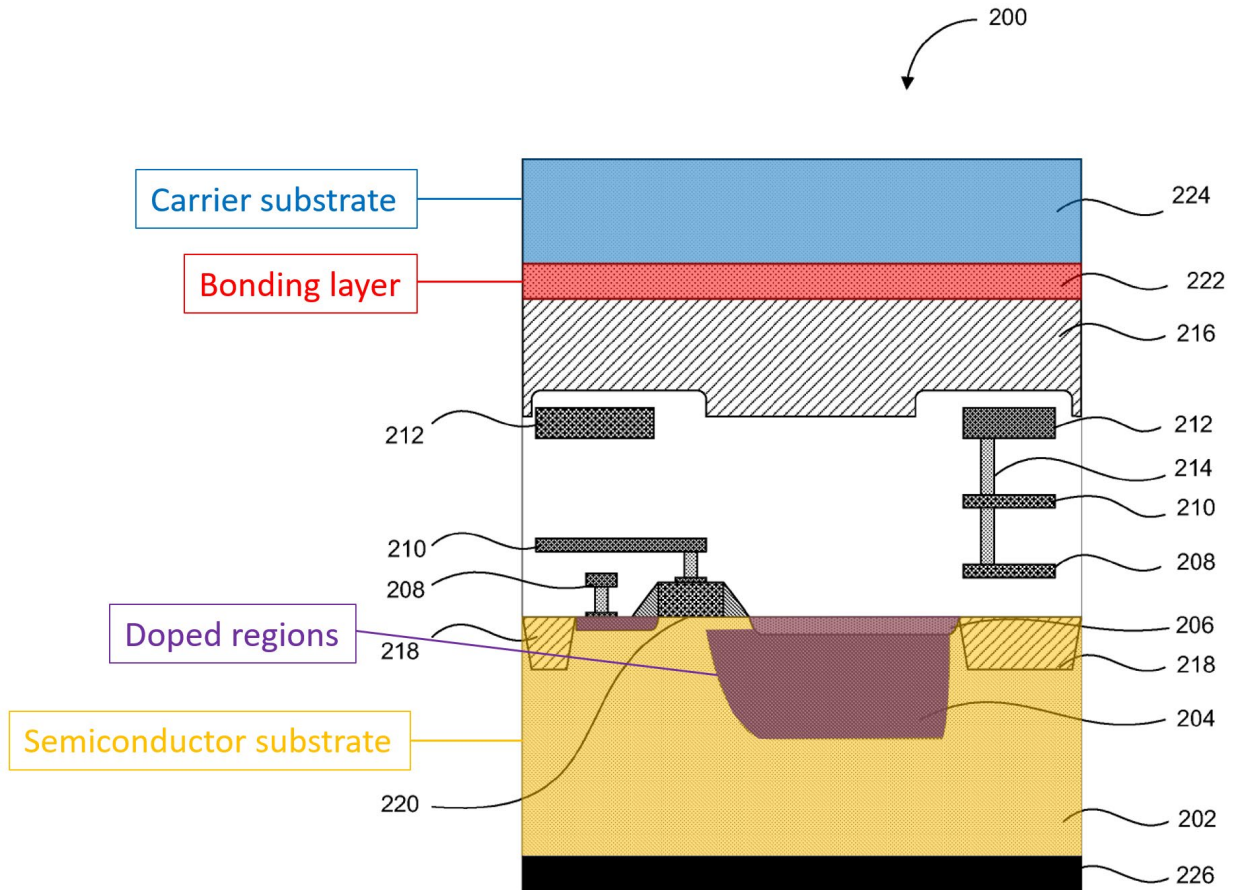


FIG. 4

Haddad138-Provisional004, Fig. 4 (annotated).

- f) 1[e]: “wherein said optoelectronic device is a photosensitive imager device capable of detecting visible and infrared electromagnetic radiation.”

Haddad138 discloses this limitation under both Petitioner’s and Patent Owner’s proposed constructions in the 737 Case. Ex-1004 ¶¶104-07.

The preamble of claims 1 and 32 of the ’737 patent has the same recitation of this limitation, “a photosensitive imager device capable of detecting visible and infrared electromagnetic radiation.” In the 737 Case, Petitioner proposed that the

preamble of claims 1 and 32 of the '737 patent is limiting and means, “An image sensor pixel capable of detecting visible and infrared electromagnetic radiation.” Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning, and that to the extent a construction is required, it means, “A device with multiple pixels arranged to capture an image from visible and/or infrared light.” Ex-1014, 3-4.

Haddad138 discloses an image sensor pixel capable of detecting visible and infrared electromagnetic radiation. Haddad138 discloses “pixels ... capable of detecting visible as well as infrared electromagnetic radiation.” Haddad138, [0045]. Ex-1004 ¶¶37-38, 106. Haddad138 discloses that its pixels are incorporated into an “imaging array,” i.e., they are image sensor pixels. Haddad138, [0064]; *see also* Haddad138, [0079] (disclosing “4 pixel imagers”), [0095] (“multiple pixels can be associated together to form an imager”).

As discussed above, Haddad138 also discloses a device with multiple pixels arranged to capture an image from visible and/or infrared light. Haddad138, [0045], [0064], [0079], [0095]; *see also* Ex-1004 ¶107.

2. Claim 2

a) “The device of claim 1, wherein the semiconductor layer is single crystal silicon.”

Haddad138 discloses this limitation. Ex-1004 ¶¶108-09.

Haddad138 discloses that “[a] variety of semiconductor materials are contemplated for use,” including “monocrystalline silicon” (i.e., the claimed single crystal silicon). Haddad138, [0052]; *see also* Ex-1004 ¶109.

3. Claim 3

a) **“The device of claim 1, wherein the shallow trench isolation surface features are formed in the semiconductor layer.”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶110-12.

As discussed above for limitation 1[b], Haddad138’s surface features correspond to the claimed shallow trench isolation surface features.

Haddad138 discloses that “the textured region can be positioned on a surface of the semiconductor substrate.” Haddad138, [0005]. For a textured region to be positioned on a surface of the semiconductor substrate, the surface of the semiconductor substrate would need to be textured, i.e., the shallow trench isolation surface features are formed in the semiconductor layer. Ex-1004 ¶112. This understanding is consistent with the teaching of one of Haddad138’s provisional applications that a light diffusing region (i.e., a textured region) can be “*formed in* or near the semiconductor substrate” in the “present invention.” Haddad138-Provisional004, 1-2; *see also* Ex-1004 ¶112. Haddad138 also discloses chemically and/or structurally altering “the surface of the semiconductor material” to form

“surface features appearing as microstructures or patterned areas on the surface.”

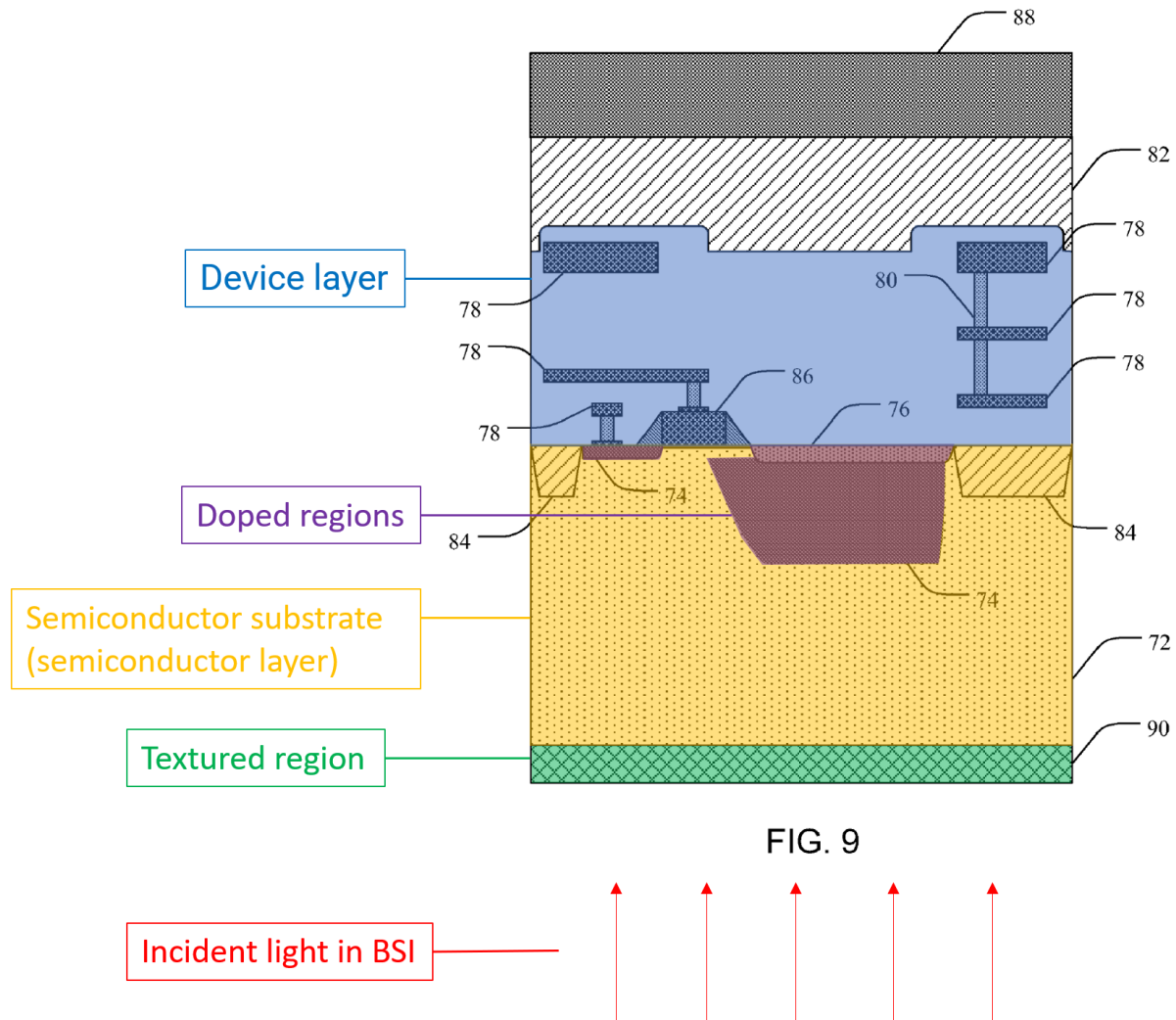
Haddad138, [0070].

4. Claim 6

- a) “The device of claim 1, further comprising a device layer coupled to the semiconductor layer on said side opposed to the light incident side.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶113-15.

Figure 9 depicts a layer containing metal regions 78 (i.e., the claimed device layer) coupled to the top surface of the semiconductor substrate 72 (i.e., the claimed semiconductor layer). Haddad138, [0084]-[0085]; *see also* Ex-1004 ¶114.



Haddad138, Fig. 9 (annotated and modified to show incident light). The provisional application to the '682 patent refers to such a metallization layer as a device layer. Ex-1003, Fig. 3.

As discussed above in Section VII.A, in a BSI configuration, incident light enters the device from the bottom. *See* Haddad138, [0048]-[0049]. In this configuration, the bottom surface of the semiconductor substrate 72 corresponds to the claimed light incident side of the semiconductor layer, and the top surface (to

which the device layer is coupled) corresponds to the claimed side opposed to the light incident side. Ex-1004 ¶115.

5. Claim 7

- a) **“The device of claim 1, wherein said first bonding layer comprises any of silicon oxide, silicon nitride and amorphous silicon.”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶116-19.

As discussed above regarding limitation 1[d], Haddad138 discloses a bonding layer that is disposed between the semiconductor layer and the support substrate. It would have been obvious to use silicon oxide or silicon nitride as the bonding layer because they can be easily polished and bonded. Ex-1026, 228; *see also KSR*, 550 U.S. at 418; Ex-1004 ¶117.

It would have been obvious to apply the known technique of using silicon oxide or silicon nitride as bonding layers to Haddad138’s device to yield predictable results. *KSR*, 550 U.S. at 417; Ex-1004 ¶118. Silicon oxide and silicon nitride were routinely used as bonding layers. Ex-1026, 216; Ex-1027, [0032]; Ex-1028, 317; Ex-1004 ¶118. The use of silicon oxide and silicon nitride would have yielded predictable results because they were commonly used in semiconductor manufacturing and their properties were well known. Ex-1026, 228; Ex-1020, 155-162; Ex-1004 ¶118.

A POSITA would have had a reasonable expectation of success. Ex-1004 ¶119. It would have been well within the abilities of a POSITA to use silicon oxide and silicon nitride because the methods of manufacturing them were well known and involved routine semiconductor manufacturing steps. Ex-1020, 155-162; *see also* Ex-1004 ¶119.

6. Claim 8

- a) **“The device of claim 1, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶120-21.

Haddad138 discloses a semiconductor material (i.e., the claimed semiconductor layer) with “a thickness of from about 1 μm to about 10 μm .” Haddad138, [0055].

7. Claim 11

- a) **“The device of claim 1, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶122-23.

Haddad138 discloses that “the [surface] features or microstructures can be on the order of 50 nm to 20 μm in size.” Haddad138, [0070]. More specifically, Haddad138 discloses that “a surface can be *several hundred nanometers* thick,” which is within the claimed range. Haddad138, [0032].

8. Claim 12

- a) **“The device of claim 1, wherein said shallow trench isolation surface features comprise pyramids.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶124-25.

Haddad138 discloses that “[t]he surface features can be pyramids.”

Haddad138, [0063]; *see also* Haddad138, [0066].

9. Claim 15

- a) **“The device of claim 1, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶126-27.

Haddad138 discloses its devices have an enhanced ability to absorb electromagnetic radiation compared to “[t]raditional silicon photodetecting imagers [that] have limited light absorption/detection properties.” Haddad138, [0044]. Specifically, Haddad138 discloses that its textured region can function to “absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad138, [0063]; *see also* Haddad138, [0070] (“the textured surface can *increase the probability of incident radiation being absorbed by the semiconductor material*”).

10. Claim 16

- a) “The device of claim 1, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶128-33.

One of Haddad138’s provisional applications discloses that the “net result” of using its light diffusing regions (i.e., the claimed textured regions) is “the photosensing pixel can absorb light having a wavelength in the range of about 400nm to about 1200nm,” which includes the claimed range of about 700 nm to about 1100 nm. Haddad138-Provisional004, 6.

Moreover, Haddad138 discloses that, unlike “[t]raditional silicon photodetecting imagers” that have trouble detecting “photons having wavelengths longer than approximately 700 nm,” Haddad138, [0044], its devices are “able to absorb longer wavelengths (e.g. >1000 nm for silicon).” Haddad138, [0044].

Haddad138 also discloses that its textured region increases optical absorption of “infrared,” Haddad138, [0065], whose wavelength range includes the claimed range of about 700 nm to about 1100 nm. Ex-1029, 807; Ex-1004 ¶131.

In sum, because Haddad138 discloses that its textured region increases optical absorption over at least “the range of about 400nm to about 1200nm,” more than

“700 nm,” and “infrared,”³ Haddad138 discloses that its textured region increases optical absorption of the spectrum range “of at least about 700 nm to about 1100 nm,” as required by this limitation.

In addition, Haddad138 does not teach away from the claimed range and the claimed range does not produce any new or unexpected result. Ex-1004 ¶133; *see also UCB v. Actavis*, 65 F.4th 679, 689-90 (Fed. Cir. 2023).

11. Claim 17

- a) **“The device of claim 1, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶134-35.

Haddad138 discloses that its “textured region can include surface features to increase the effective absorption length of the photosensitive pixel,” i.e., increase the effective optical path length of light as it passes through the semiconductor layer. Haddad138, [0063].

12. Claim 18

- a) **“The device of claim 1, wherein said textured region allows the semiconductor layer to experience multiple passes of light.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶136-37.

³ Infrared was known to include at least the range of 700 nm to 2500 nm. Ex-1029, 807; *see also* Ex-1004 ¶132.

Haddad138 discloses that its textured region “can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared).” Haddad138, [0065].

13. Claim 21

- a) **“The device of claim 1, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case. Ex-1004 ¶¶138-40.

In the 737 Case, Petitioner proposed that the term “the surface features are arranged according to a pattern” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning and that, to the extent a construction is required, it means “features coincident with at least one surface that are arranged in a repeating manner.” Ex-1014, 4.

As discussed above for limitation 1[b], Haddad138’s surface features correspond to the claimed shallow trench isolation surface features. Haddad138 discloses that the surface features are arranged according to a pattern under Patent Owner’s proposed construction in the 737 Case. Haddad138 discloses “surface features appearing as microstructures or *patterned areas on the surface*.” Haddad138, [0070]. Moreover, Haddad138 discloses forming surface features using

nanoimprinting, Haddad138, [0006], which involves using a mold to create imprints on the target material, thus resulting in a formation of features coincident with at least one surface that are arranged in a repeating manner. Ex-1019, 4129; *see also* Ex-1004 ¶140. Haddad138 also discloses forming surface features using chemical etching, Haddad138, [0006], which involves the use of a mask that results in the formation of features coincident with at least one surface that are arranged in a repeating manner. *See, e.g.*, Ex-1020, 87; Ex-1011, 8:25-29; *see also* Ex-1004 ¶140.

14. Claim 26

a) “The device of claim 1, further comprising deep trench isolation for isolating the device.”

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶141-44.

Figure 9 depicts trench isolation 84. Haddad138, [0084]-[0085]; *see also* Ex-1004 ¶142.

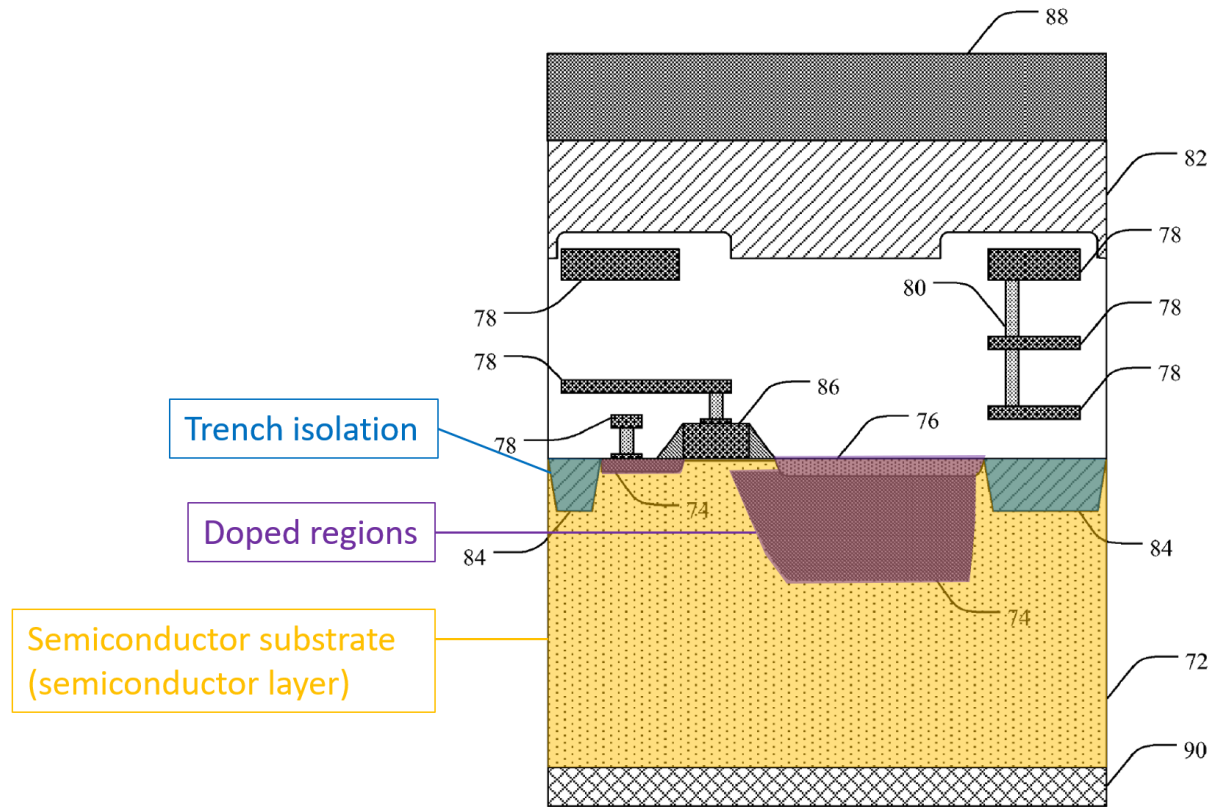


FIG. 9

Haddad138, Fig. 9 (annotated).

Haddad138 discloses that the trench isolation can be deep, as required by this limitation. Haddad138, [0085]; *see also* Haddad138-Provisional004, 5 (“The trench isolation can be shallow or deep trench isolation”); Ex-1004 ¶143.

Haddad138’s deep trench isolation can reduce optical and electrical crosstalk, i.e., isolate the device, as required by this limitation. Haddad138, [0085]; *see also* Haddad138-Provisional004, 5 (“The isolation layer can be configured to reflect the incident light until it is absorbed, thereby increas[ing] the effective absorption length of the device.”); *see also* Ex-1004 ¶144.

15. Claim 27

- a) “The device of claim 26, wherein said deep trench isolation provides light trapping functionality.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶145-46.

Haddad138’s deep trench isolation can reduce optical crosstalk and “reflect incident light until it is absorbed,” i.e., provide light trapping functionality, as required by this limitation. Haddad138, [0085]; *see also* Haddad138-Provisional004, 5 (“The isolation layer can be configured to reflect the incident light until it is absorbed, thereby increas[ing] the effective absorption length of the device.”); Ex-1004 ¶146.

B. Ground A-2: Claims 4-5, 14, and 21-22 Are Obvious Based on Haddad138 and Baggenstoss

1. The Combination of Haddad138 and Baggenstoss

As discussed above regarding limitation 1[b], Haddad138 discloses an optoelectronic device with a textured region. Haddad138, [0084], [0087], [0064]; *see also* Ex-1004 ¶147. Haddad138 discloses that its textured region can include surface features. Haddad138, [0063].

Similarly, Baggenstoss discloses an optoelectronic device with a grated interface formed by trenches 144. Baggenstoss, [0031]-[0032], [0009]; *see also* Ex-1004 ¶148.

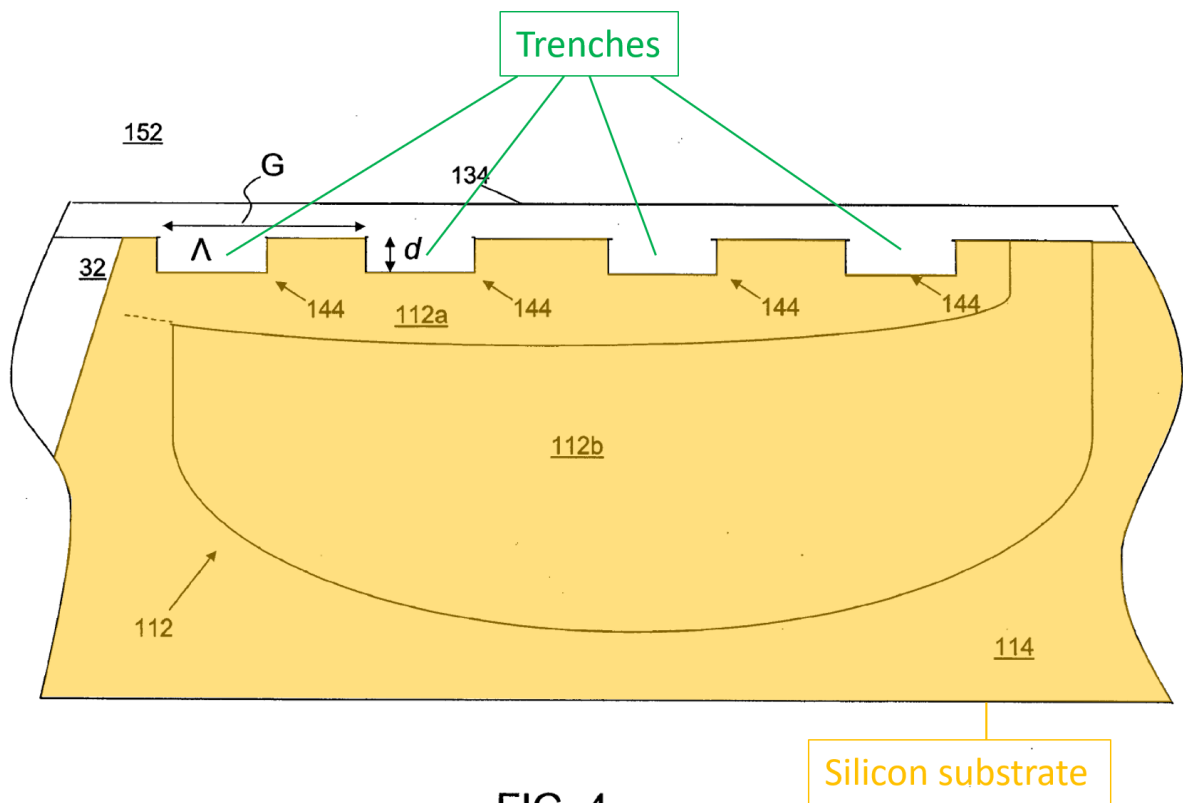


FIG. 4

Baggenstoss, Fig. 4 (annotated).

In another embodiment, Baggenstoss discloses an optoelectronic device with a “blazed (or step-wise)” gratings formed of trenches 244. Baggenstoss, [0042]; *see also* Ex-1004 ¶149.

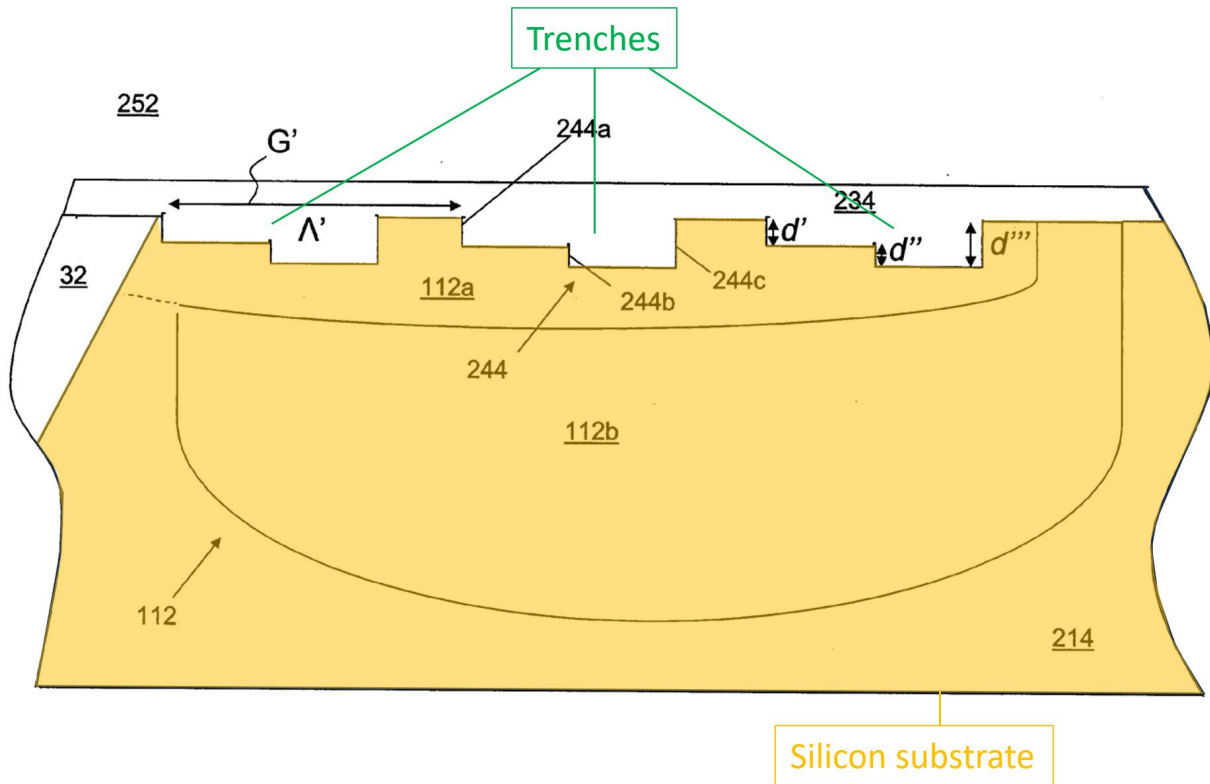


FIG. 11

Baggenstoss, Fig. 11 (annotated).

As Dr. Lebby explains, a POSITA would have looked to Baggenstoss’s discussion of trenches for more details on how to implement the surface features in Haddad138. Ex-1004 ¶150. Baggenstoss teaches that its grated interface formed of trenches “allows a greater percentage of incident light to be captured, which is a vast improvement over the art.” Baggenstoss, [0014]; *see also* KSR, 550 U.S. at 418.

The use of Baggenstoss’s trenches in Haddad138’s devices would have involved use of a known technique to improve similar devices in the same way. KSR, 550 U.S. at 417; Ex-1004 ¶151. Both Haddad138 and Baggenstoss disclose photodetectors. Haddad138, [0003], [0064]; Baggenstoss, [0014], [0009]. Both

Haddad138 and Baggenstoss have the same goal of improving the efficiency of photodetectors in capturing incident light. Haddad138, [0063]; Baggenstoss, [0014]. Both Haddad138 and Baggenstoss achieve that goal by using a textured region including surface features. Haddad138, [0063], [0087]; Baggenstoss, [0031]-[0032], [0042]. Both Haddad138 and Baggenstoss disclose placing the textured region on the light incident side. Haddad138, [0049]; Baggenstoss, [0038], Fig. 3. Like the grated interface of Baggenstoss, the textured region of Haddad138 can “enhance the absorption properties by reducing the amount of incident electromagnetic radiation that is reflected from the device.” Haddad138-Provisional434, 5; *see also* Ex-1004 ¶151. Both Haddad138 and Baggenstoss disclose forming the surface features using chemical etching. Haddad138, [0006]; Baggenstoss, [0038].

In addition, the use of Baggenstoss’s trenches in Haddad138’s devices would have been, at most, a simple substitution of one known element (i.e., Baggenstoss’s trenches) for another (i.e., Haddad138’s surface features) to obtain predictable results. *KSR*, 550 U.S. at 417; Ex-1004 ¶152. Again, because Haddad138 discloses surface features, a POSITA would have understood that Baggenstoss’s trenches, which are surface features, would work in Haddad138. Ex-1004 ¶152.

A POSITA would have had a reasonable expectation of success in arriving at this combination. Ex-1004 ¶153. As Dr. Lebby explains, it would have been well within the abilities of a POSITA to use the implementation details of Baggenstoss’s

trenches for Haddad138's surface features, given that it would have involved routine manufacturing steps, such as chemical etching, that Haddad138 was already using for its surface features. Haddad138, [0006]; *see also* Ex-1004 ¶153.

2. Claim 4

- a) **“The device of claim 1, wherein the shallow trench isolation surface features have a substantially uniform height.”**

Haddad138 in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶154-60.

As discussed above in Section VIII.B.1, Baggenstoss discloses an optoelectronic device with a grated interface formed by trenches 144. Baggenstoss, [0031]-[0032], [0009]; *see also* Ex-1004 ¶155.

the '682 patent, '682 patent, 11:27-28; *see also* Ex-1004 ¶156. Both Baggenstoss and the '682 patent describe the same or similar processes for creating the shallow trench isolation surface features. Ex-1004 ¶157. Both Baggenstoss and the '682 patent explain that their shallow trench isolation surface features serve the same function. Ex-1004 ¶158.

Baggenstoss discloses that the trenches 144 have a predetermined depth (i.e., the claimed height), represented by d in Figure 4. Baggenstoss, [0032]. The predetermined depth d can be, for example, a constant depth of 100 nm. Baggenstoss, [0034]-[0035]. Baggenstoss's shallow trench isolation surface features, therefore, have a substantially uniform height, as required by this limitation. Ex-1004 ¶159.

Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the trenches and the shallow trench isolation in Baggenstoss. Ex-1004 ¶160. Baggenstoss discloses forming shallow trench isolation, e.g., element 32 in Figure 4. Baggenstoss, [0009]. As Dr. Lebby explains, the process for creating shallow trench isolation was well known. Ex-1004 ¶160. Creating the surface features using the same process as the process for the shallow trench isolation would generate predictable results, and reduce the costs associated with developing a new process. Ex-1004 ¶160. This would involve employing a known technique to improve similar

devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶160. A POSITA would have had a reasonable expectation of success because Baggenstoss already discloses using shallow trench isolation in its devices, and, as Dr. Lebby discusses, it was well known how to use a shallow trench isolation process to form surface features. Baggenstoss, [0009]; Haddad138, [0066]; Ex-1034, [0010]-[0012]; *see also* Ex-1004 ¶160.

3. Claim 5

- a) “The device of claim 1, wherein the shallow trench isolation surface features are not uniform in height.”**

Haddad138 in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶161-67.

In another embodiment, Baggenstoss discloses an optoelectronic device with a “blazed (or step-wise)” gratings formed of trenches 244. Baggenstoss, [0042]; *see also* Ex-1004 ¶162.

0.25 microns). Baggenstoss, [0043], similar to the surface features of the '682 patent, '682 patent, 11:27-28; *see also* Ex-1004 ¶163. Both Baggenstoss and the '682 patent describe the same or similar processes for creating the shallow trench isolation surface features. Ex-1004 ¶164. Both Baggenstoss and the '682 patent explain that their shallow trench isolation surface features serve the same function. Ex-1004 ¶165.

As shown in Figure 11, the trenches 244 have two different depths (i.e., the claimed heights). Baggenstoss, [0043]. Thus, the shallow trench isolation surface features are not uniform in height, as required by this limitation. Ex-1004 ¶166. Baggenstoss discloses that its trenches can be formed by chemical etching. Baggenstoss, [0038], [0043]; *see also* Ex-1004 ¶166. Typically, two masks would be required to etch the two different depths of the trenches 244. Ex-1004 ¶166.

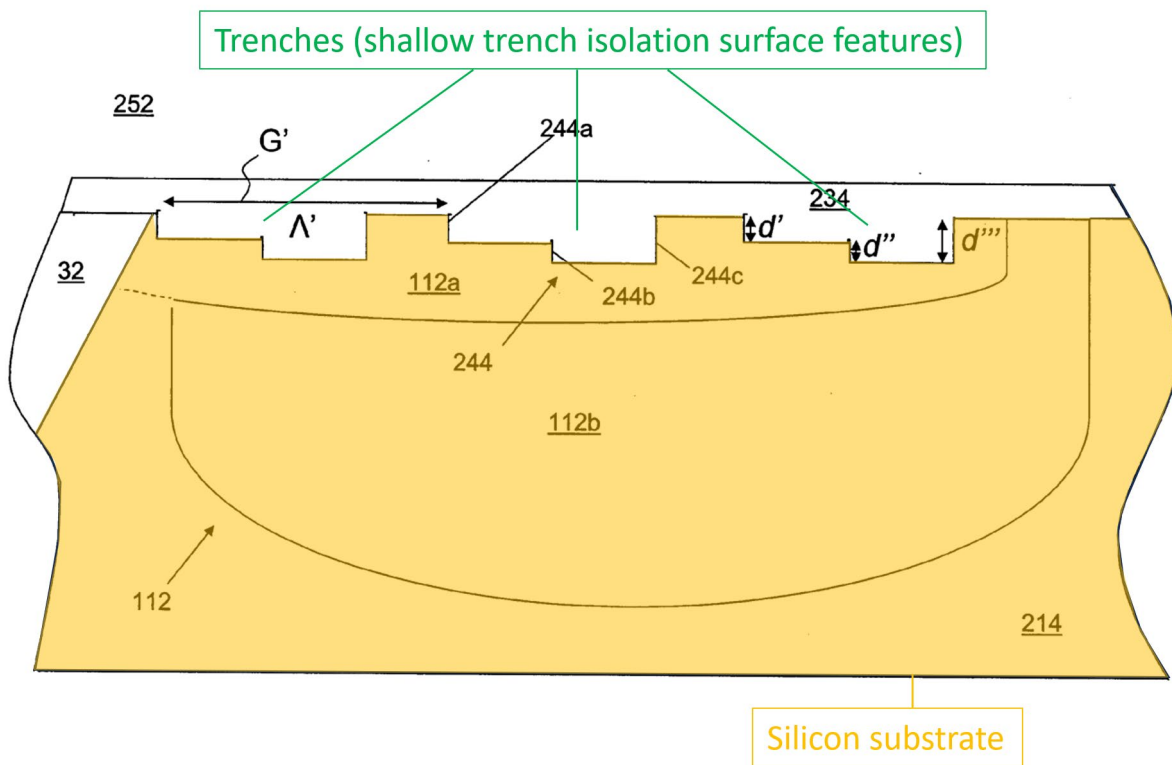
Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the trenches and the shallow trench isolation in Baggenstoss, for the same reason discussed above regarding claim 4. Ex-1004 ¶167.

4. Claim 14

- a) “The device of claim 1, wherein said plurality of shallow trench isolation surface features comprise multiple etched levels.”

Haddad138 in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶168-70.

As discussed above regarding claim 5, Baggenstoss discloses trenches 244 (i.e., the claimed shallow trench isolation surface features) with two different depths. Baggenstoss, [0043]; *see also* Ex-1004 ¶169.



Baggenstoss, Fig. 11 (annotated).

The different depths correspond to the claimed multiple etched levels because Baggenstoss's trenches 244 can be formed via chemical etching. Baggenstoss, [0038], [0043]; *see* Ex-1004 ¶170. Typically, two masks would be required to etch the two different depths of the trenches 244. Ex-1004 ¶170.

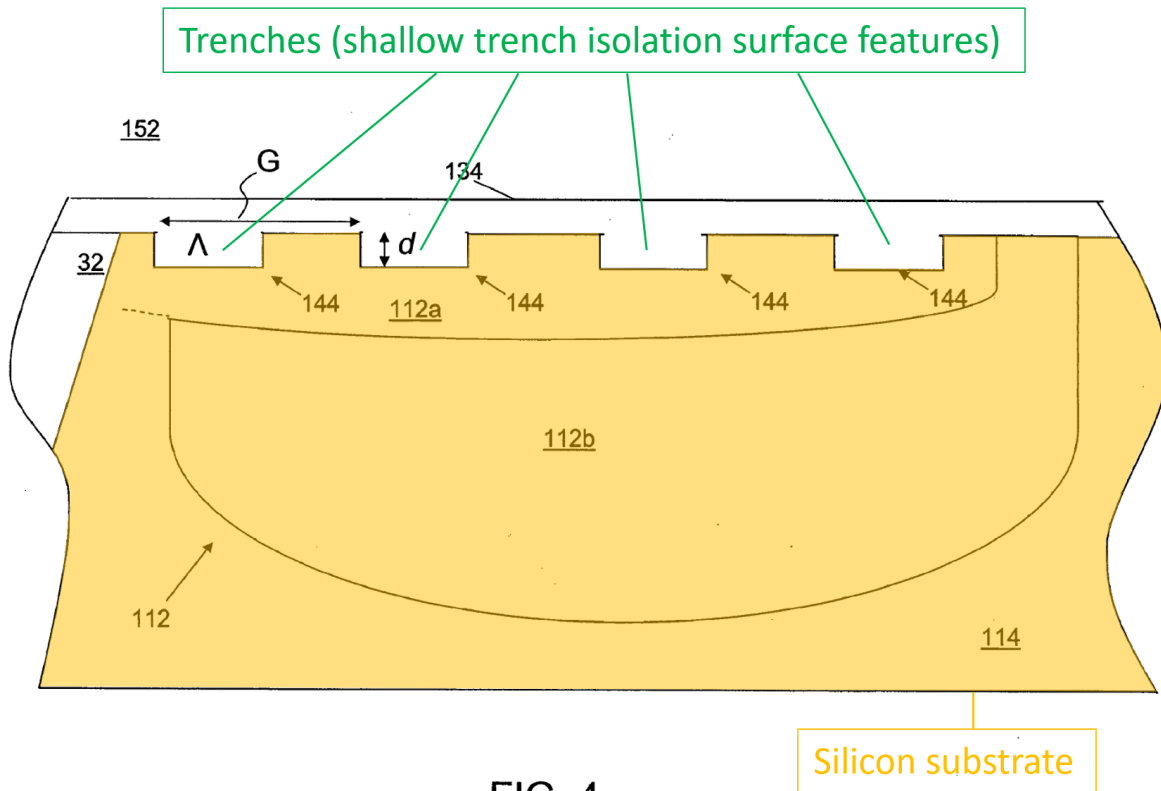
5. Claim 21

- a) “The device of claim 1, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

Haddad138 in view of Baggenstoss renders this limitation obvious under Patent Owner's proposed construction in the 737 Case. Ex-1004 ¶¶171-74.

In the 737 Case, Petitioner proposed that the '737 patent term “the surface features are arranged according to a pattern” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning and that, to the extent a construction is required, it means “features coincident with at least one surface that are arranged in a repeating manner.” Ex-1014, 4.

As discussed above regarding claim 4, Figure 4 of Baggenstoss depicts a grated interface formed by trenches 144 (i.e., the claimed shallow trench isolation surface features). Baggenstoss, [0031]-[0032]; *see also* Ex-1004 ¶173.



Baggenstoss, Fig. 4 (annotated).

“Each grating (measured as the distance from the beginning of one trench 144 to the beginning of the next trench 144 (shown by arrow G)) has a predetermined period that is represented by Λ .” Baggenstoss, [0032]. The predetermined period Λ can be, for example, 340 nm. Baggenstoss, [0034]. Baggenstoss’s trenches are features coincident with at least one surface that are arranged in a repeating manner, and are an example of a pattern provided by the provisional application for the ’682 patent. Ex-1003, 13:2-4 (“[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a *uniform grid pattern* comprised of [trenches] that form *a series of spaces and lines* or pillars.”); see also Ex-1004 ¶174.

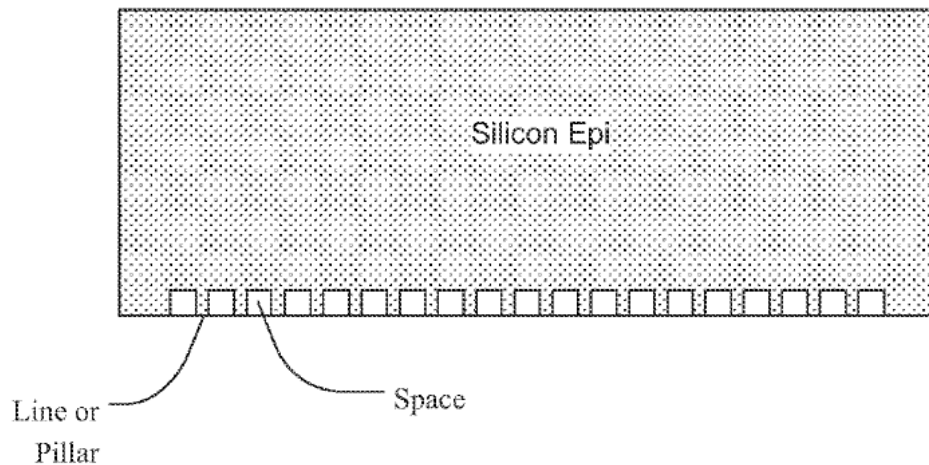


FIG. 5

Ex-1003, Fig. 5.

6. Claim 22

- a) “The device of claim 21, wherein the pattern is an at least substantially uniform grid.”**

Haddad138 in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶175-77.

As discussed above regarding claim 4, Figure 4 of Baggenstoss depicts a grated interface formed by trenches 144 (i.e., the claimed shallow trench isolation surface features). Baggenstoss, [0031]-[0032]; *see also* Ex-1004 ¶176.

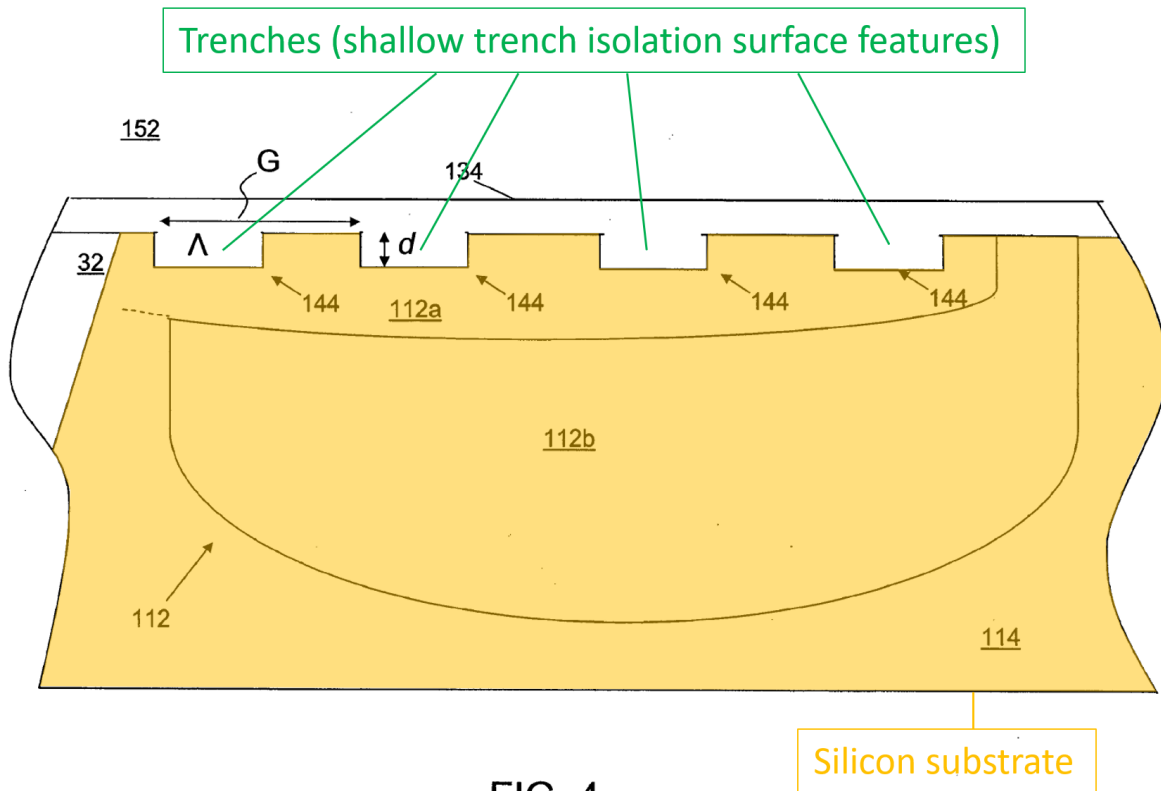


FIG. 4

Baggenstoss, Fig. 4 (annotated).

“Each grating (measured as the distance from the beginning of one trench 144 to the beginning of the next trench 144 (shown by arrow G) has a predetermined period that is represented by Λ ,” i.e., the trenches form the claimed substantially uniform grid. Baggenstoss, [0032]; *see also* Ex-1004 ¶177. The provisional application for the ’682 patent identifies such gratings as an example of a “uniform grid pattern.” Ex-1003, 13:2-4 (“[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a *uniform grid pattern* comprised of [trenches] that form *a series of spaces and lines* or pillars.”).

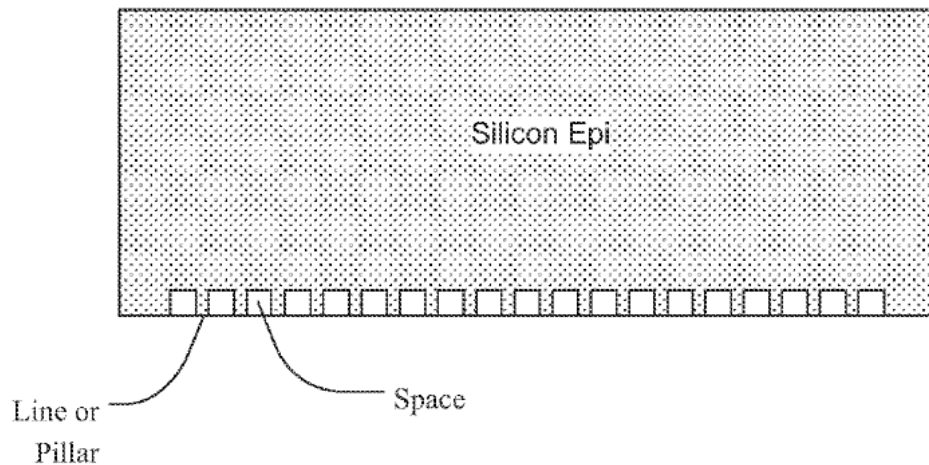


FIG. 5

Ex-1003, Fig. 5.

C. Ground A-3: Claims 9-10, 13, 19-20, 28-31, and 34-42 Are Obvious Based on Haddad138 and Alie

1. The Combination of Haddad138 and Alie

Haddad138 discloses a substrate coupled to a semiconductor layer by way of a bonding layer. Haddad138, [0086]; *see also* Ex-1004 ¶178. However, it does not disclose the bonding layer thickness, the use of two bonding layers, or the use of a reflector layer.

Alie contains additional details about the bonding layer and a reflector layer. In particular, it discloses the use of a dielectric layer as a bonding layer. Alie, [0055], [0087], [0105]; *see also* Ex-1004 ¶179. In addition, Alie discloses that its dielectric layer can have “a thickness of from about 500 nm to about 2 microns.” Alie, [0088]. Alie further discloses that, instead of using just one dielectric layer for bonding, two

dielectric layers can be used. Ex-1004 ¶179. Alie, [0059]. Alie also discloses use of a reflector layer. Alie, [0089].

Haddad138 also discloses that its surface features can be formed by etching. Haddad138, [0006]; *see also* Ex-1004 ¶180. However, it does not expressly mention using a mask and photolithography, followed by etching.

Alie contains additional details about etching. In particular, it discloses that surface features can be formed by “a selective etching technique, such as a mask, photolithography, and an etch.” Alie, [0072]; *see also* Ex-1004 ¶181.

A POSITA would have had looked to Alie for additional details about the bonding layer and the etching process, as well as incorporating from Alie the reflector layer. Ex-1004 ¶182.

Combining Haddad138 with Alie would have involved use of a known technique (i.e., Alie’s bonding layers, reflector layer, or etching technique) to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶183. Both Haddad138 and Alie share the same two joint inventors: Jeffrey McKee and Chintamani Palsule. Both Haddad138 and Alie concern photodetectors with textured regions that increase quantum efficiency. Haddad138, [0063]-[0064], [0087]; Alie, [0052], [0096], [0006]. The textured regions in both references include similarly shaped surface features. Haddad138, [0063]; Alie, [0068]. The textured regions in both references can be formed by chemical etching. Haddad138, [0066]; Alie, [0074].

Both Haddad138's and Alie's devices use similar materials. *See, e.g.*, Haddad138, [0052]; Alie, [0060]. Both Haddad138's and Alie's devices also share similar dimensions. *See, e.g.*, Haddad138, [0055] ("the semiconductor material has a thickness of from about 1 μm to about 10 μm "); Alie, [0063] ("the semiconductor material has a thickness of from about 1 μm to about 10 μm "). In view of the above, where Haddad138 is silent on certain details regarding the bonding layers, the reflector layer, and the etching technique, a POSITA would have looked to Alie for such details and used them for Haddad138's device with predictable results. Ex-1004 ¶184. Additional motivations for using these elements are explained further below.

A POSITA would have had a reasonable expectation of success in making this combination. Ex-1004 ¶185. As Dr. Lebby explains, it would have been well within the abilities of a POSITA to use Alie's bonding layers, reflector layer, and etching technique for Haddad138's device, given that it would have involved routine manufacturing steps that Alie had already used in its devices with predictable results. Ex-1004 ¶185.

2. Claim 9

- a) **“The device of claim 1, wherein said bonding layer has a thickness in a range of about 30 nm to about 3 microns.”**

Haddad138 in view of Alie renders this limitation obvious. Ex-1004 ¶¶186-88.

Haddad138 discloses that “[t]he carrier substrate can be coupled to the photosensing pixel by various techniques” including “by way of a bonding layer” (i.e., the claimed first bonding layer). Haddad138, [0086]; *see also* Ex-1004 ¶187.

Similarly, Alie discloses the use of a dielectric layer as a bonding layer. Alie, [0055], [0087], [0105]; *see also* Ex-1004 ¶188. Alie discloses that its dielectric layer can have “a thickness of from about 500 nm to about 2 microns,” which is a range fully encompassed by the claimed range of about 30 nm to about 3 microns. Alie, [0088]. Alie does not teach away from the claimed range and the claimed range does not produce any new or unexpected result. Ex-1004 ¶188; *see also UCB v. Actavis*, 65 F.4th at 689-90.

3. Claim 10

- a) **“The device of claim 1, wherein said bonding layer has a thickness in a range of about 40 nm to about 2 microns.”**

Haddad138 in view of Alie renders this limitation obvious. Ex-1004 ¶¶189-91.

Haddad138 discloses that “[t]he carrier substrate can be coupled to the photosensing pixel by various techniques” including “by way of a bonding layer” (i.e., the claimed first bonding layer). Haddad138, [0086]; *see also* Ex-1004 ¶190.

Similarly, Alie discloses the use of a dielectric layer as a bonding layer. Alie, [0055], [0087], [0105]; *see also* Ex-1004 ¶191. Alie discloses that its dielectric layer can have “a thickness of from about 500 nm to about 2 microns,” which is a range fully encompassed by the claimed range of about 40 nm to about 2 microns. Alie, [0088]. Alie does not teach away from the claimed range and the claimed range does not produce any new or unexpected result. Ex-1004 ¶191; *see also UCB v. Actavis*, 65 F.4th at 689-90.

4. Claim 13

- a) **“The device of claim 1, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.”**

Haddad138 in view of Alie renders this limitation obvious. Ex-1004 ¶¶192-94.

Haddad138 discloses that surface features can be formed by etching. Haddad138, [0006]; *see also* Ex-1004 ¶193.

Alie teaches that using a mask and photolithography to etch surface features allows forming “a specific structure or pattern” over a specific area of a target surface. Alie, [0072]; *see also* Ex-1004 ¶194.

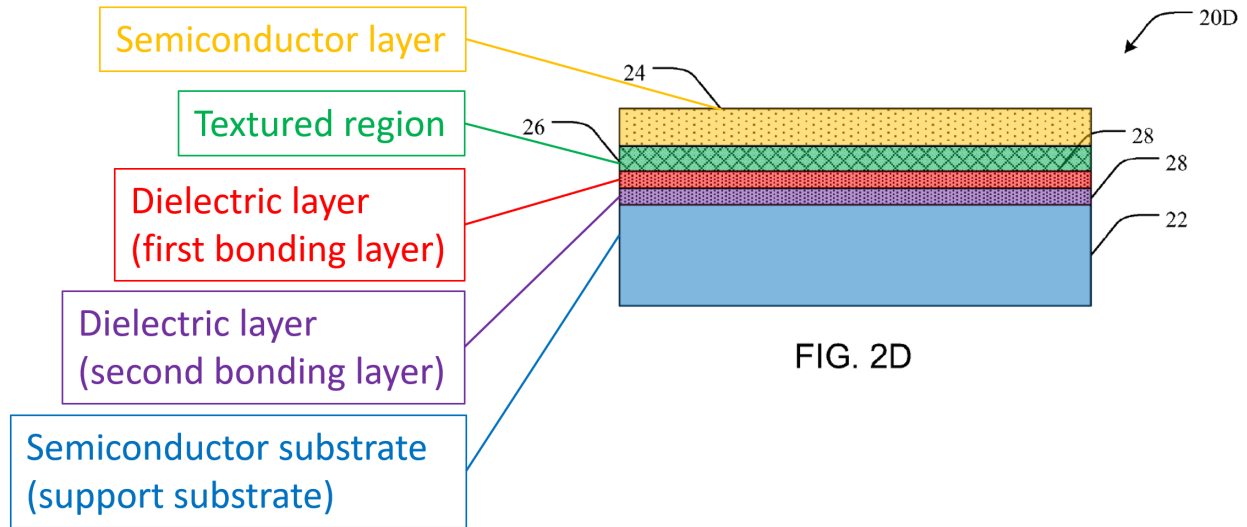
5. Claim 19

- a) “The device of claim 1, further comprising a second bonding layer positioned between the first bonding layer and the support substrate.”**

Haddad138 in view of Alie renders this limitation obvious. Ex-1004 ¶¶195-97.

Haddad138 discloses that, during the manufacture of an optoelectronic device, “[t]he carrier substrate can be coupled to the photosensing pixel by various techniques” including “by way of a bonding layer” (i.e., the claimed first bonding layer). Haddad138, [0086]; *see also* Ex-1004 ¶196.

Alie also discloses using a dielectric layer as a bonding layer in an optoelectronic device. Alie, [0055], [0006]. Alie further discloses that, instead of using just one dielectric layer for bonding, two dielectric layers can be used. Alie, [0059]. A POSITA would have known that using two bonding layers was a common technique to ensure the strength, uniformity, thermal performance, and reliability of the bond. *See, e.g.*, Ex-1032, [0041]-[0042]; Ex-1035, 113-14; *see also* Ex-1004 ¶197. Figure 2D depicts the use of the second bonding layer (purple) positioned between the first bonding layer (red) and the support substrate (blue). Alie, [0059].



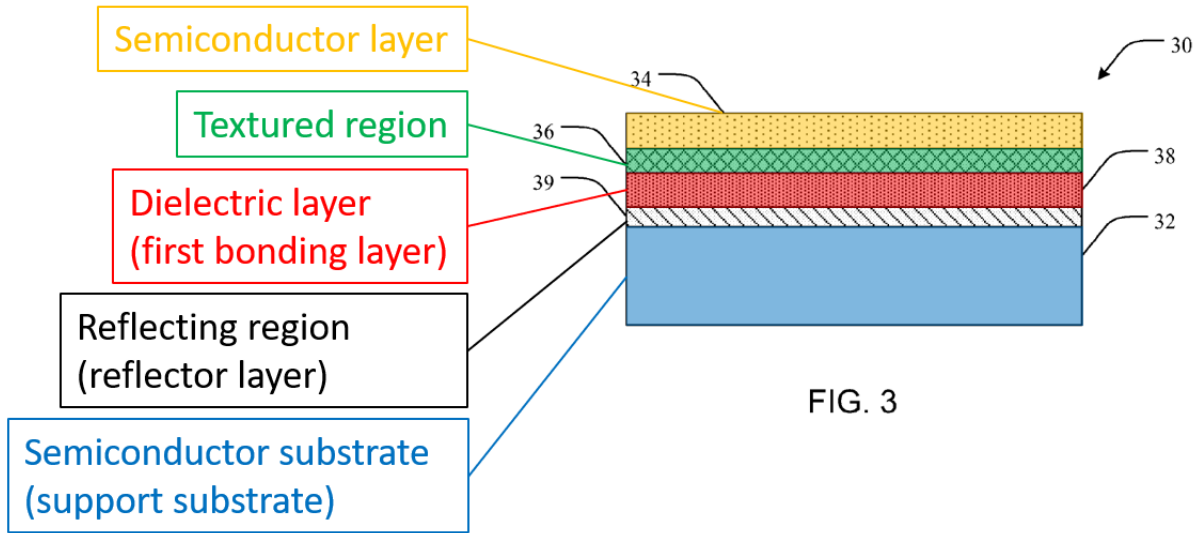
Alie, Fig. 2D (annotated).

6. Claim 20

- a) **“The device of claim 19, further comprising a reflector layer disposed between the first bonding layer and the second bonding layer.”**

Haddad138 in view of Alie renders this limitation obvious. Ex-1004 ¶¶198-201.

Figure 3 of Alie depicts the use of a reflecting region 39 (i.e., the claimed reflector layer) directly beneath the first bonding layer. Alie, [0089]. Ex-1004 ¶199.



Alie, Fig. 3 (annotated).

In discussing a manufacturing method for a device similar to the Figure 3 device, Alie discloses that there can be “a second dielectric layer formed on the semiconductor substrate (not shown)” in addition to the existing dielectric layer. Alie, [0105]. The second dielectric layer formed on the semiconductor substrate corresponds to the claimed second bonding layer. Ex-1004 ¶200. Arranged as described in Alie, the reflector layer (brown) directly below the first bonding layer (red) would be sandwiched between the first bonding layer (red) and the second bonding layer formed on the semiconductor substrate (not shown). Ex-1004 ¶200.

It would have been obvious to modify Haddad138’s device (modified to use Alie’s two bonding layers as discussed above regarding claim 19) by placing Figure 3’s reflector layer between the two bonding layers, as taught by Alie. Ex-1004 ¶201. A known issue in the field is a loss of light due to transmission through a

semiconductor layer. Ex-1004 ¶201. Placing a reflector layer on the side opposite the light incident side of the semiconductor layer addresses this issue by increasing internal reflection of light within the semiconductor layer. Ex-1004 ¶201. Alie teaches that “[s]uch internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer.” Alie, [0070]; *see also KSR*, 550 U.S. at 418; Ex-1004 ¶201. Alie further teaches that “[t]his increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.” Alie, [0070]. Given the known challenge of light loss and the established effectiveness of reflectors in improving light absorption, a POSITA would have been motivated to apply this well-understood solution to enhance the performance of Haddad138’s device. Ex-1004 ¶201. It would have been obvious to place the reflector layer between two bonding layers to ensure strong bonding, given that reflector layers may have poor bonding properties. Ex-1004 ¶201.

7. Claim 28

a) 28[pre]: “An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:”

Haddad138 discloses the preamble to the extent it is limiting. Ex-1004 ¶¶202-03.

See limitation 1[pre] in Ground A-1.

- b) **28[a]: “a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,”**

Haddad138 discloses this limitation. Ex-1004 ¶¶204-05.

See limitation 1[a] in Ground A-1.

- c) **28[b]: “a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶206-07.

See limitation 1[b] in Ground A-1.

- d) **28[c]: “a support substrate coupled to said semiconductor layer, and”**

Haddad138 discloses this limitation. Ex-1004 ¶¶208-09.

See limitation 1[c] in Ground A-1.

- e) **28[d]: “a first bonding layer disposed between the semiconductor layer and the support substrate,”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶210-11.

See limitation 1[d] in Ground A-1.

- f) **28[e]: “a second bonding layer positioned between the first bonding layer and the support substrate, and”**

Haddad138 in view of Alie renders this limitation obvious. Ex-1004 ¶¶212-

13.

See claim 19 in Ground A-3.

- g) **28[f]: “a reflector layer disposed between the first bonding layer and the second bonding layer.”**

Haddad138 in view of Alie renders this limitation obvious. Ex-1004 ¶¶214-

15.

See claim 20 in Ground A-3.

8. Claim 29

- a) **“The device of claim 28, wherein said shallow trench isolation surface features comprise pyramids.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶216-17.

See claim 12 in Ground A-1 and claim 28 in Ground A-3.

9. Claim 30

- a) **“The device of claim 28, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.”**

Haddad138 in view of Alie renders this limitation obvious. Ex-1004 ¶¶218-

19.

See claims 13 and 28 in Ground A-3.

10. Claim 31

- a) **“The device of claim 28, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶220-21.

See claim 8 in Ground A-1 and claim 28 in Ground A-3.

11. Claim 34

- a) **“The device of claim 28, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶222-23.

See claim 11 in Ground A-1 and claim 28 in Ground A-3.

12. Claim 35

- a) **“The device of claim 28, wherein said photosensitive imager device is capable of detecting visible and infrared electromagnetic radiation.”**

Haddad138 discloses this limitation under both Petitioner’s and Patent Owner’s proposed constructions in the 737 Case. Ex-1004 ¶¶224-25.

See limitation 1[e] in Ground A-1 and claim 28 in Ground A-3.

13. Claim 36

- a) **“The device of claim 28, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶226-27.

See claim 15 in Ground A-1 and claim 28 in Ground A-3.

14. Claim 37

- a) **“The device of claim 28, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶228-29.

See claim 16 in Ground A-1 and claim 28 in Ground A-3.

15. Claim 38

- a) **“The device of claim 28, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶230-31.

See claim 17 in Ground A-1 and claim 28 in Ground A-3.

16. Claim 39

- a) **“The device of claim 28, wherein said textured region allows the semiconductor layer to experience multiple passes of light.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶232-33.

See claim 18 in Ground A-1 and claim 28 in Ground A-3.

17. Claim 40

- a) **“The device of claim 28, further comprising deep trench isolation for isolating the device.”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶234-35.

See claim 26 in Ground A-1 and claim 28 in Ground A-3.

18. Claim 41

- a) **“The device of claim 40, wherein said deep trench isolation provides light trapping functionality.”**

Haddad138 discloses this limitation. Ex-1004 ¶¶236-37.

See claim 27 in Ground A-1 and claim 28 in Ground A-3.

19. Claim 42

- a) **“The device of claim 28, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

Haddad138 discloses this limitation, or at a minimum, renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case. Ex-1004 ¶¶238-39.

See claim 21 in Ground A-1 and claim 28 in Ground A-3.

D. Ground A-4: Claim 23 Is Obvious Based on Haddad138 and Haddad204

1. Claim 23

- a) **“The device of claim 21, wherein the pattern is a non-uniform arrangement.”**

Haddad138 in view of Haddad204 renders this limitation obvious. Ex-1004 ¶¶240-45.

As discussed above regarding limitation 1[b], Haddad138 discloses an optoelectronic device with a textured region. Haddad138, [0087], [0084], [0064];

see also Ex-1004 ¶241. Haddad138 discloses that its textured region can include surface features such as pillars. Haddad138, [0006], [0063].

Similarly, Haddad204 discloses an optoelectronic device with a textured region including surface features such as pillars. Haddad204, [0073], [0053]. Importantly, Haddad204 discloses “a plurality of pillars of variable sizes ... arranged in a non-uniform array.” Haddad204, [0112]; *see also* Ex-1004 ¶242. Figure 9a shows a top view and Figure 9b shows a cross-sectional view of such “pillars etched into a semiconductor material.” Haddad204, [0112].

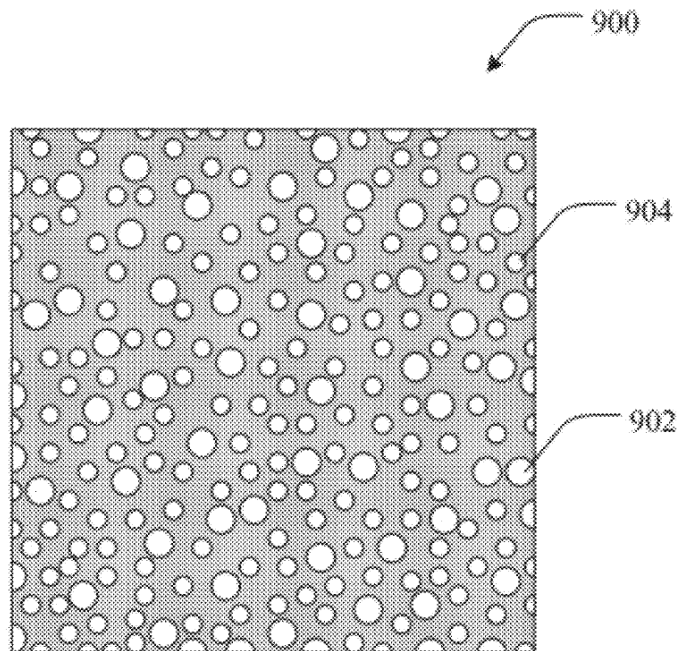


FIG. 9a

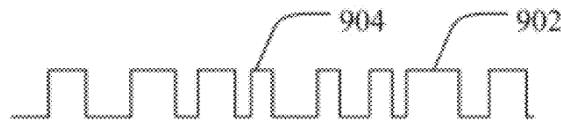


FIG. 9b

Haddad204, Figs. 9a-b.

A POSITA would have looked to Haddad204 for more details on how to implement the surface features disclosed in Haddad138. Haddad204 teaches that its surface features “increase the effective absorption length of the photosensitive pixel,” which in turn, increases the quantum efficiency. Haddad204, [0073], [0076]; *see also KSR*, 550 U.S. at 418; Ex-1004 ¶243. Increasing quantum efficiency using surface features is the same goal shared by Haddad138. Haddad138, [0063]. Both Haddad138 and Haddad204 teach that “[a]ny increase in the quantum efficiency makes a large difference in the signal to noise ratio.” Haddad138, [0050], Haddad204, [0058].

Combining Haddad138 with Haddad204 would have involved use of a known technique (i.e., Haddad204’s non-uniform arrangement) to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶244. Both Haddad138 and Haddad204 share the same joint inventors. Both Haddad138 and Haddad204 concern photodetectors with textured regions that increase quantum efficiency. Haddad138, [0063]-[0064], [0087]; Haddad204, [0073], [0053]. The textured regions in both references include similarly shaped surface features such as pillars.

Haddad138, [0063]; Haddad204, [0073]. The textured regions in both references can be formed by chemical etching. Haddad138, [0006]; Haddad204, [0093]. Both Haddad138 and Haddad204 disclose placing the textured regions on the light incident side. Haddad138, [0049]; Haddad204, [0111].

A POSITA would have had a reasonable expectation of success in making this combination. Ex-1004 ¶245. As Dr. Lebby explains, it would have been well within the abilities of a POSITA to use Haddad204's non-uniform arrangement of pillars for Haddad138's arrangement of pillars, given that it would have involved routine manufacturing steps that Haddad204 had already used in its devices with predictable results. Ex-1004 ¶245.

E. Ground A-5: Claim 23 Is Obvious Based on Haddad138 and Park

1. Claim 23

a) “The device of claim 21, wherein the pattern is a non-uniform arrangement.”

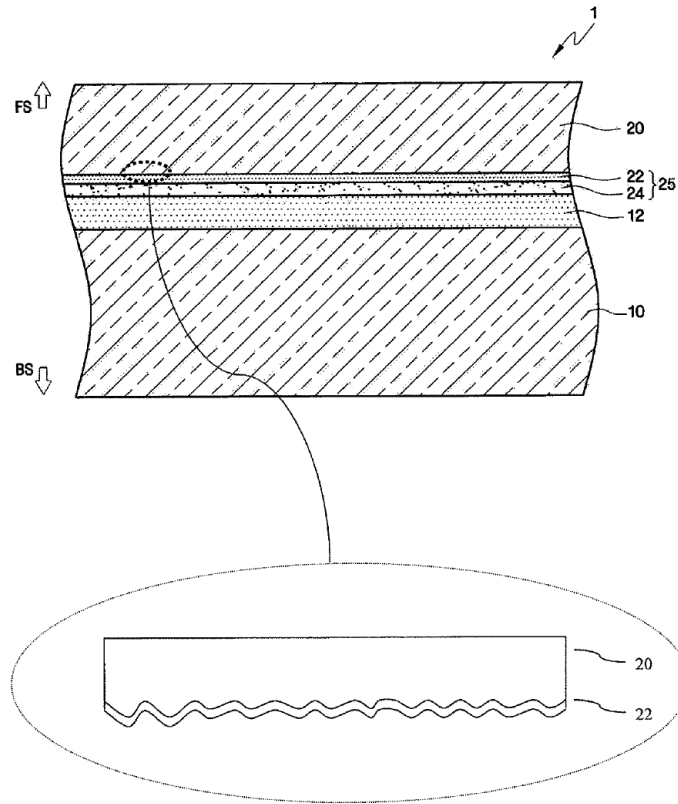
Haddad138 in view of Park renders this limitation obvious. Ex-1004 ¶¶246-51.

As discussed above regarding limitation 1[b], Haddad138 discloses an optoelectronic device with a textured region. Haddad138, [0087], [0084], [0064]; *see also* Ex-1004 ¶247. Haddad138 discloses that its textured region can include surface features such as protrusions. Haddad138, [0063].

Similarly, Park discloses an optoelectronic device with an uneven surface.

Park, [0072], [0059]; *see also* Ex-1004 ¶248.

FIG. 1



Park, Fig. 1. As its name suggests, and as depicted in Figure 1, Park's uneven surface has protrusions in a non-uniform arrangement. Ex-1004 ¶248.

A POSITA would have looked to Park for more details on how to implement the surface features including protrusions disclosed in Haddad138. Park teaches that its uneven surface helps with absorbing incident light by reducing reflection. Park, [0072]; *see also* KSR, 550 U.S. at 418; Ex-1004 ¶249. Decreasing reflection of incident light means more light entering the silicon substrate to be absorbed. Ex-

1004 ¶249. Haddad138 teaches that increased absorption of incident light increases quantum efficiency. Haddad138, [0063]. Haddad138 teaches that “[a]ny increase in the quantum efficiency makes a large difference in the signal to noise ratio.” Haddad138, [0050]. Based on the teachings of Park and Haddad138, a POSITA would have been motivated to use Park’s non-uniform arrangement. Ex-1004 ¶249.

Combining Haddad138 with Park would have involved use of a known technique (i.e., Park’s non-uniform arrangement) to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶250. Both Haddad138 and Park concern increasing quantum efficiency of photodetectors. Haddad138, [0050], [0063], [0065]; Park, [0004]-[0005], Fig. 7. Both Haddad138 and Park disclose placing a textured region or uneven surface on the light incident side. Haddad138, [0049]; Park, Figs. 1, 7. Like Park’s uneven surface, the Haddad138’s textured region can “enhance the absorption properties by reducing the amount of incident electromagnetic radiation that is reflected from the device.” Haddad138-Provisional434, 5; *see also* Ex-1004 ¶250.

A POSITA would have had a reasonable expectation of success in making this combination. Ex-1004 ¶251. As Dr. Lebby explains, it would have been well within the abilities of a POSITA to use Park’s non-uniform arrangement of protrusions for Haddad138’s arrangement of protrusions, given that it would have involved routine

manufacturing steps that Park had already used in its devices with predictable results. Ex-1004 ¶251.

F. Ground A-6: Claims 32-33 and 42-43 Are Obvious Based on Haddad138, Alie, and Baggenstoss

1. The Combination of Haddad138, Alie, and Baggenstoss

As discussed above in Sections VIII.C.1, 5 & 6, it would have been obvious to combine Haddad138 with Alie, incorporating Alie's bonding layers and reflector layer in Haddad138's device. Ex-1004 ¶¶252.

As discussed above in Section VIII.B.1, it would have been obvious to combine Haddad138 with Baggenstoss, incorporating Baggenstoss's trenches in Haddad138's device. Ex-1004 ¶¶253.

It further would have been obvious to combine Haddad138 with both Alie and Baggenstoss in order to incorporate Alie's bonding layers and reflector layer, as well as Baggenstoss's trenches, into Haddad138's device. Ex-1004 ¶¶254-56. The reasons for including such features in an optoelectronic device were well understood for the reasons taught in those references and discussed above in Sections VIII.B.1 and VIII.C.1, 5 & 6.

Combining Haddad138 with Alie and Baggenstoss would have involved use of a known technique to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶255. Haddad138, Alie, and Baggenstoss all disclose photodetectors. Haddad138, [0003], [0019]; Alie, [0052], [0096], [0006]; Baggenstoss, [0014],

[0009]. Haddad138, Alie, and Baggenstoss all have the same goal of improving the efficiency of photodetectors in capturing incident light. Haddad138, [0063]; Alie, [0052], Baggenstoss, [0014]. Haddad138, Alie, and Baggenstoss all achieve that goal by using a textured region including surface features. Haddad138, [0063], [0087]; Alie, [0052], Baggenstoss, [0031]-[0032], [0042]. Haddad138, Alie, and Baggenstoss all disclose placing the textured region on the light incident side. Haddad138, [0049]; Alie, [0094]; Baggenstoss, [0038], Fig. 3. Haddad138, Alie, and Baggenstoss all disclose forming the surface features using chemical etching. Haddad138, [0006]; Alie, [0074]; Baggenstoss, [0038].

A POSITA would have had a reasonable expectation of success in making this combination. Ex-1004 ¶256. It would have been well within the abilities of a POSITA to use Alie's bonding layers and reflector layer as discussed above in Sections VIII.C.1, 5 & 6 and to use Baggenstoss's trenches as discussed above in Section VIII.B.1. Ex-1004 ¶256. The bonding layers, reflector layer, and trenches would work together in improving Haddad138's device. Ex-1004 ¶256.

2. Claim 32

- a) **“The device of claim 28, wherein the shallow trench isolation surface features have a substantially uniform height.”**

Haddad138 in view of Alie and Baggenstoss renders this limitation obvious. Ex-1004 ¶¶257-58.

See claim 4 in Ground A-2 and claim 28 in Ground A-3.

3. Claim 33

- a) **“The device of claim 28, wherein the shallow trench isolation surface features are not uniform in height.”**

Haddad138 in view of Alie and Baggenstoss renders this limitation obvious.

Ex-1004 ¶¶259-60.

See claim 5 in Ground A-2 and claim 28 in Ground A-3.

4. Claim 42

- a) **“The device of claim 28, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

Haddad138 in view of Alie and Baggenstoss renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case. Ex-1004 ¶¶261-62.

See claim 21 in Ground A-2 and claim 28 in Ground A-3.

5. Claim 43

- a) **“The device of claim 42, wherein the pattern is an at least substantially uniform grid.”**

Haddad138 in view of Alie and Baggenstoss renders this limitation obvious.

Ex-1004 ¶¶263-64.

See claim 22 in Ground A-2 and 28 in Ground A-3.

G. Ground A-7: Claim 44 Is Obvious Based on Haddad138, Alie, and Haddad204

1. Claim 44

a) “The device of claim 42, wherein the pattern is a non-uniform arrangement.”

Haddad138 in view of Alie and Haddad204 renders this limitation obvious. Ex-1004 ¶¶265-71.

See claim 23 in Ground A-4 and claim 28 in Ground A-3.

As discussed above in Sections VIII.C.1, 5 & 6, it would have been obvious to combine Haddad138 with Alie, incorporating Alie’s bonding layers and reflector layer in Haddad138’s device. Ex-1004 ¶267.

As discussed above regarding Ground A-4, it would have been obvious to combine Haddad138 with Haddad204, incorporating Haddad204’s non-uniform arrangement in Haddad138’s device. Ex-1004 ¶268.

It further would have been obvious to combine Haddad138 with both Alie and Haddad204 in order to incorporate Alie’s bonding layers and reflector layer, as well as Haddad204’s non-uniform arrangement of surface features, into Haddad138’s device. Ex-1004 ¶¶269-71. The reasons for including such features in an optoelectronic device were well understood for the reasons taught in those references and discussed above in Section VIII.C.1, 5 & 6 and regarding Ground A-4.

Combining Haddad138 with Alie and Haddad204 would have involved use of a known technique to improve similar devices in the same way. *KSR*, 550 U.S. at

417; Ex-1004 ¶270. Haddad138, Alie, and Haddad204 all concern photodetectors with textured regions that increase quantum efficiency. Haddad138, [0050], [0063], [0065]; Alie, [0052], [0096], [0006]; Haddad204, [0073], [0053]. The textured regions in all three references include similarly shaped surface features such as pillars. Haddad138, [0063]; Alie, [0068]; Haddad204, [0073]. The textured regions in all three references can be formed by chemical etching. Haddad138, [0006]; Alie, [0074]; Haddad204, [0093]. Haddad138, Alie, and Haddad204 all disclose placing the textured regions on the light incident side. Haddad138, [0049]; Alie, [0094]; Haddad204, [0111].

A POSITA would have had a reasonable expectation of success in making this combination. Ex-1004 ¶271. It would have been well within the abilities of a POSITA to use Alie's bonding layers and reflector layer as discussed above in Section VIII.C.1, 5 & 6 and to use Haddad204's non-uniform arrangement as discussed above regarding Ground A-4. Ex-1004 ¶271. The bonding layers, reflector layer, and the non-uniform arrangement of surface features would work together in improving Haddad138's device. Ex-1004 ¶271.

H. Ground A-8: Claim 44 Is Obvious Based on Haddad138, Alie, and Park

1. Claim 44

a) “The device of claim 42, wherein the pattern is a non-uniform arrangement.”

Haddad138 in view of Alie and Park renders this limitation obvious. Ex-1004 ¶¶272-78.

See claim 23 in Ground A-5 and claim 28 in Ground A-3.

As discussed above in Sections VIII.C.1, 5 & 6, it would have been obvious to combine Haddad138 with Alie, incorporating Alie’s bonding layers and reflector layer in Haddad138’s device. Ex-1004 ¶274.

As discussed above regarding Ground A-5, it would have been obvious to combine Haddad138 with Park, incorporating Park’s non-uniform arrangement in Haddad138’s device. Ex-1004 ¶275.

It further would have been obvious to combine Haddad138 with both Alie and Park in order to incorporate Alie’s bonding layers and reflector layer, as well as Park’s non-uniform arrangement of surface features, into Haddad138’s device. Ex-1004 ¶¶276-78. The reasons for including such features in an optoelectronic device were well understood for the reasons taught in those references and discussed above in Section VIII.C.1, 5 & 6 and regarding Ground A-5.

Combining Haddad138 with Alie and Park would have involved use of a known technique to improve similar devices in the same way. *KSR*, 550 U.S. at 417;

Ex-1004 ¶277. Haddad138, Alie, and Park all concern increasing quantum efficiency of photodetectors. Haddad138, [0050], [0063], [0065]; Alie, [0052], [0096], [0006]; Park, [0004]-[0005], Fig. 7. To achieve this goal, Haddad138 uses a textured region with protrusions and Alie and Park similarly use textured regions with protrusions. Haddad138, [0063]; Alie, [0068]; Park, [0072]. Haddad138, Alie, and Park all disclose placing the textured regions on the light incident side. Haddad138, [0049]; Alie, [0094]; Park, Figs. 1, 7.

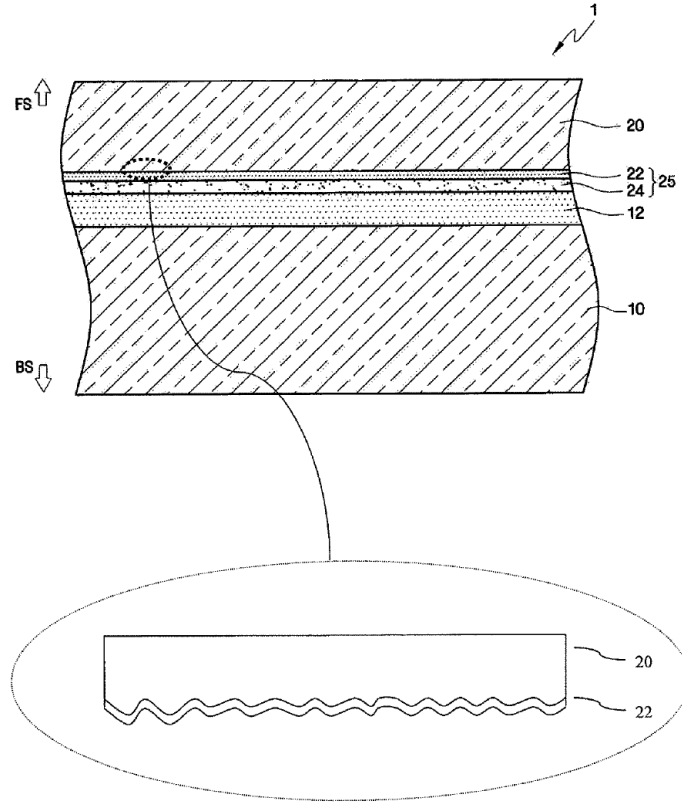
A POSITA would have had a reasonable expectation of success in making this combination. Ex-1004 ¶278. It would have been well within the abilities of a POSITA to use Alie's bonding layers and reflector layer as discussed above in Sections VIII.C.1, 5 & 6 and to use Park's non-uniform arrangement as discussed above regarding Ground A-5. Ex-1004 ¶278. The bonding layers, reflector layer, and the non-uniform arrangement of surface features would work together in improving Haddad138's device. Ex-1004 ¶278.

I. Ground B-1: Claims 24-25 Are Obvious Based on Park and Baggenstoss

1. The Combination of Park and Baggenstoss

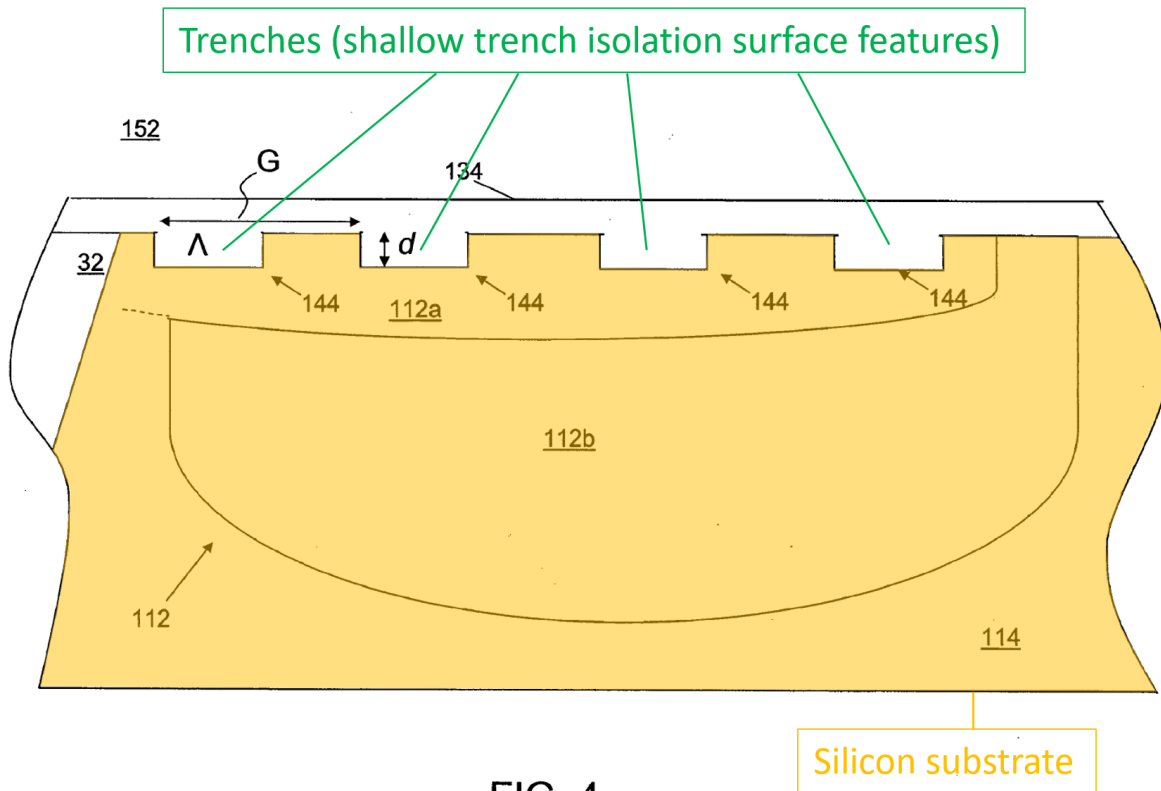
Park discloses forming an uneven surface on a semiconductor layer of an optoelectronic device. Park, [0072], [0059]; *see also* Ex-1004 ¶279.

FIG. 1



Park, Fig. 1.

Similarly, Baggenstoss discloses creating an optoelectronic device with a grating interface formed by trenches 144 (i.e., the claimed plurality of shallow trench isolation surface features). Baggenstoss, [0031]-[0032], [0009]; *see also* Ex-1004 ¶280.



Baggenstoss, Fig. 4 (annotated).

A POSITA would have looked to Baggenstoss’s discussion of trenches for more details on how to implement the uneven surface in Park. Ex-1004 ¶281. Baggenstoss teaches that its grated interface formed of trenches “allows a greater percentage of incident light to be captured, which is a vast improvement over the art.” Baggenstoss, [0014]; *see also KSR*, 550 U.S. at 418. Baggenstoss explains that its grated interface “serves to create a hybrid index of refraction ... thereby decreasing the percentage of incident light reflection.” Baggenstoss, [0031]. With the grated interface formed of trenches 144, the incident light reflection is “nearly eliminated” with a trench depth d of 100 nm. Baggenstoss, [0035]. The “blazed”

gratings formed of trenches 244 can decrease the incident light reflection even further. Baggenstoss, [0042]-[0043]. As Dr. Lebby explains, whether to use Baggenstoss's trenches 144 or 244 would have depended on the particular design needs regarding the cost of manufacture and the desired amount of reduction in incident light reflection. Ex-1004 ¶281.

Using Baggenstoss's trenches in Park's method would have involved use of a known technique to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶282. Both Park and Baggenstoss disclose photodetectors. Park, [0037]; Baggenstoss, [0014], [0009]. Both Park and Baggenstoss have the same goal of improving the efficiency of photodetectors in capturing incident light. Park, [0072]; Baggenstoss, [0014]. Both Park and Baggenstoss achieve that goal by using a textured region including surface features. Park, [0072]; Baggenstoss, [0031]-[0032], [0042]. Both Park and Baggenstoss disclose placing the textured region on the light incident side. Park, Figs. 1, 7; Baggenstoss, [0038], Fig. 3. Like the grated interface of Baggenstoss, Park's uneven surface can "serve to reduce specular reflection." Park, [0072]; *see also* Ex-1004 ¶282.

The use of Baggenstoss's trenches in Park's method would have been, at most, a simple substitution of one known element (i.e., Baggenstoss's trenches) for another (Park's uneven surface) to obtain predictable results. *KSR*, 550 U.S. at 417; Ex-1004 ¶283. Again, because Park discloses an uneven surface, a POSITA would have

understood that Baggenstoss's trenches, which form an uneven surface, would work in Park. Ex-1004 ¶283.

A POSITA would have had a reasonable expectation of success in using Baggenstoss's trenches in Park's method. Ex-1004 ¶284. As Dr. Lebby explains, it would have been well within the abilities of a POSITA to use the implementation details of Baggenstoss's trenches for Park's uneven surfaces, given that it would have involved routine manufacturing steps that Park was already using. Park, [0065]-[0066]; *see also* Ex-1004 ¶284.

2. Claim 24

a) 24[pre]: "A method of making an optoelectronic device, comprising:"

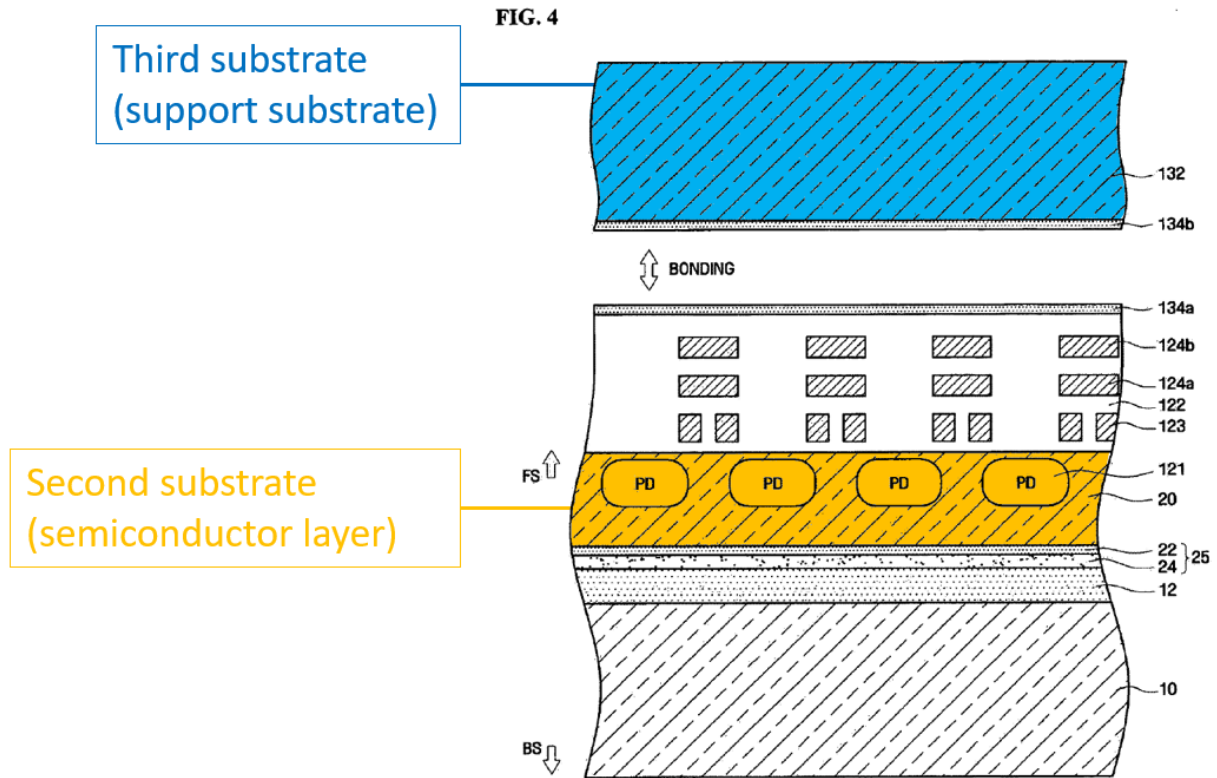
Park discloses the preamble to the extent it is limiting. Ex-1004 ¶¶285-86.

Park discloses that "FIGS. 1 to 7 illustrate cross-sectional views of stages in a method of fabricating an image sensor." Park, [0037].

b) 24[a]: "bonding a semiconductor layer to a support substrate, wherein bonding the semiconductor layer to the support substrate includes:"

Park discloses this limitation. Ex-1004 ¶¶287-89.

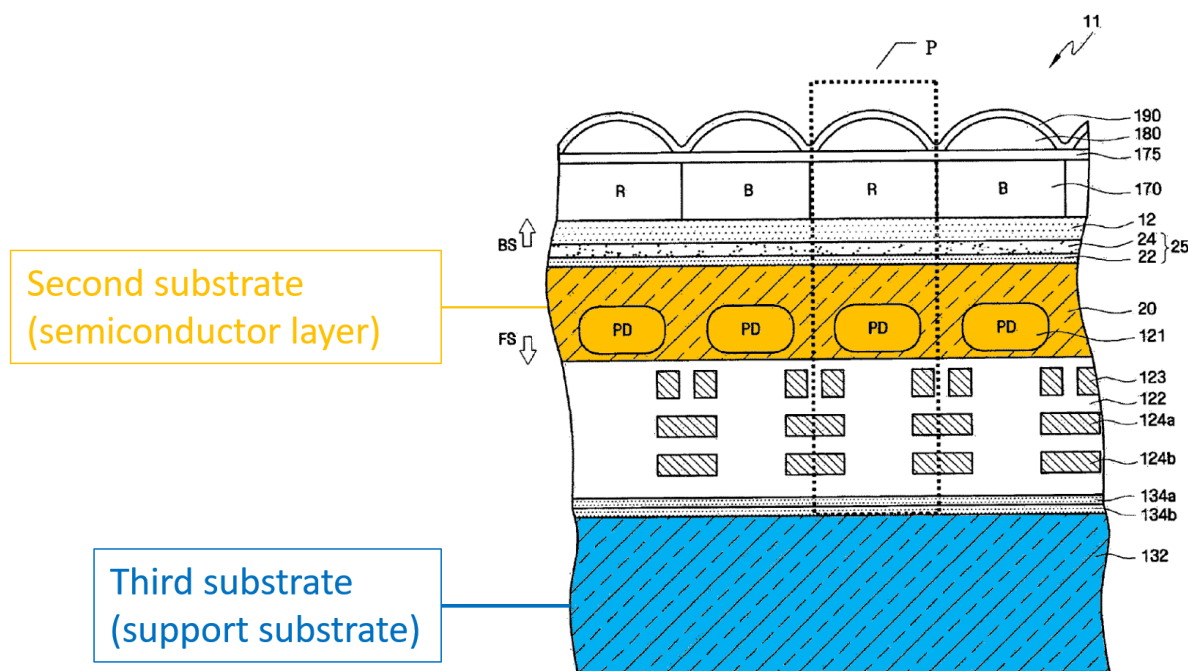
Fig 4 depicts bonding a second substrate 20 (i.e., the claimed semiconductor layer) to a third substrate 132 (the claimed support substrate). Park, [0076].



Park, Fig. 4 (annotated).

The second substrate 20 corresponds to the claimed semiconductor layer because Park discloses that the second substrate 20 may be doped silicon with light sensing devices 121. Park, [0064], [0074]; *see also* Ex-1004, ¶289. The third substrate 132 corresponds to the claimed support substrate because it supports Park's device, as shown in Figure 7. Park, [0059].

FIG. 7

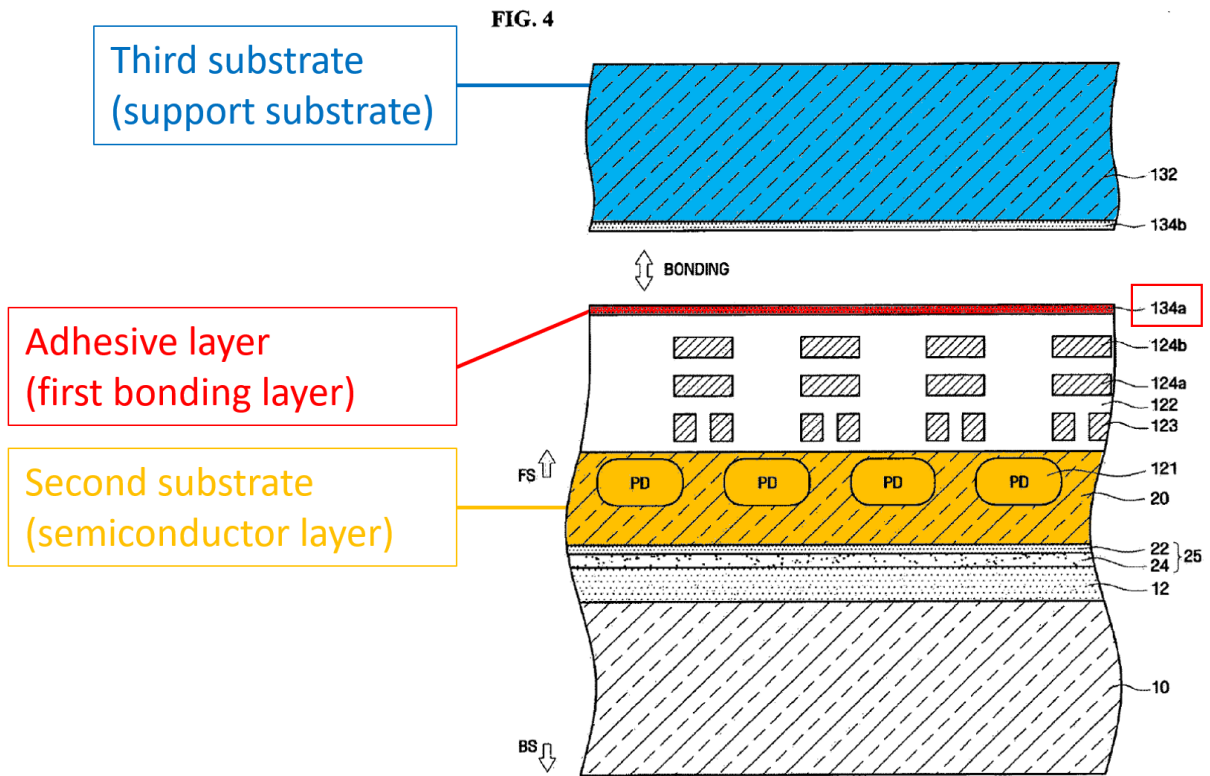


Park, Fig. 7 (annotated).

c) 24[b]: “depositing a first bonding layer onto the semiconductor layer; and”

Park discloses this limitation. Ex-1004 ¶¶290-91.

Park discloses depositing an adhesive layer 134a (i.e., the claimed first bonding layer) onto the semiconductor layer. Park, [0076].

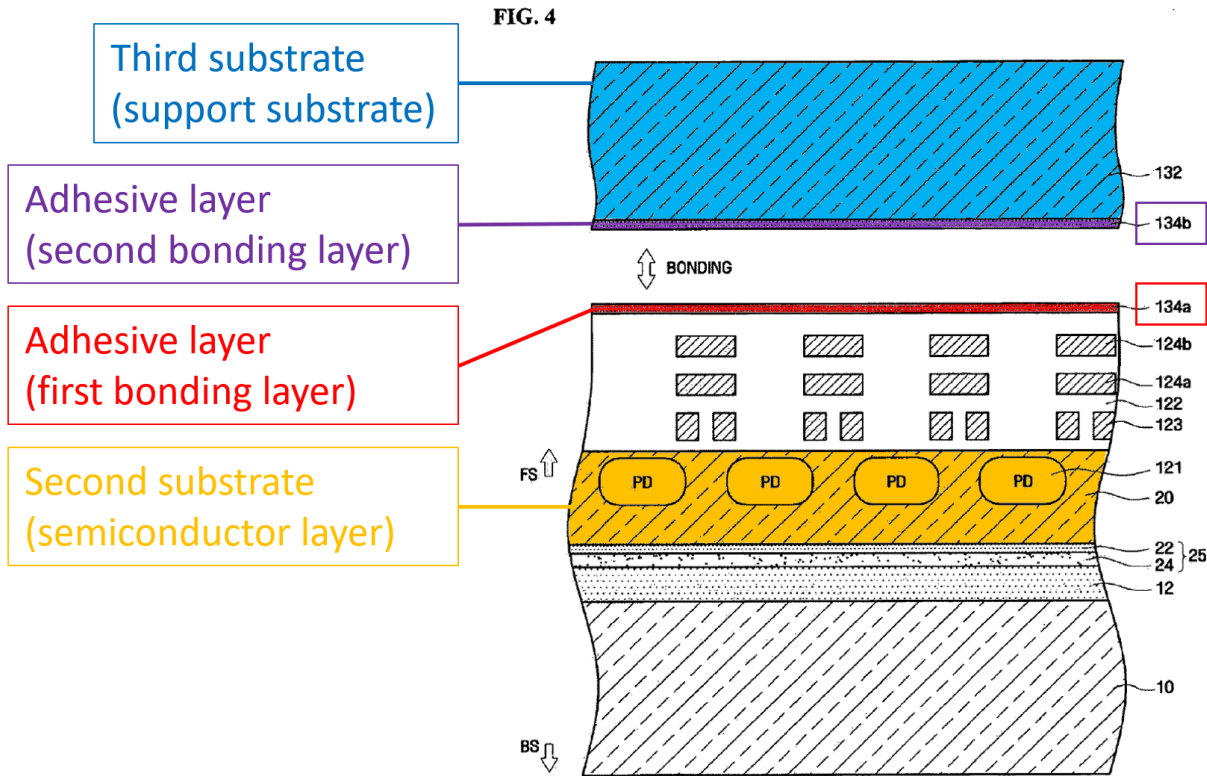


Park, Fig. 4 (annotated).

- d) 24[c]: “bonding the first bonding layer to a second bonding layer disposed on the support substrate; and”

Park discloses this limitation. Ex-1004 ¶¶292-93.

Park discloses bonding the first bonding layer to an adhesive layer 134b that is disposed on the substrate 132 (i.e., the claimed second bonding layer disposed on the support substrate). Park, [0076].



Park, Fig. 4 (annotated).

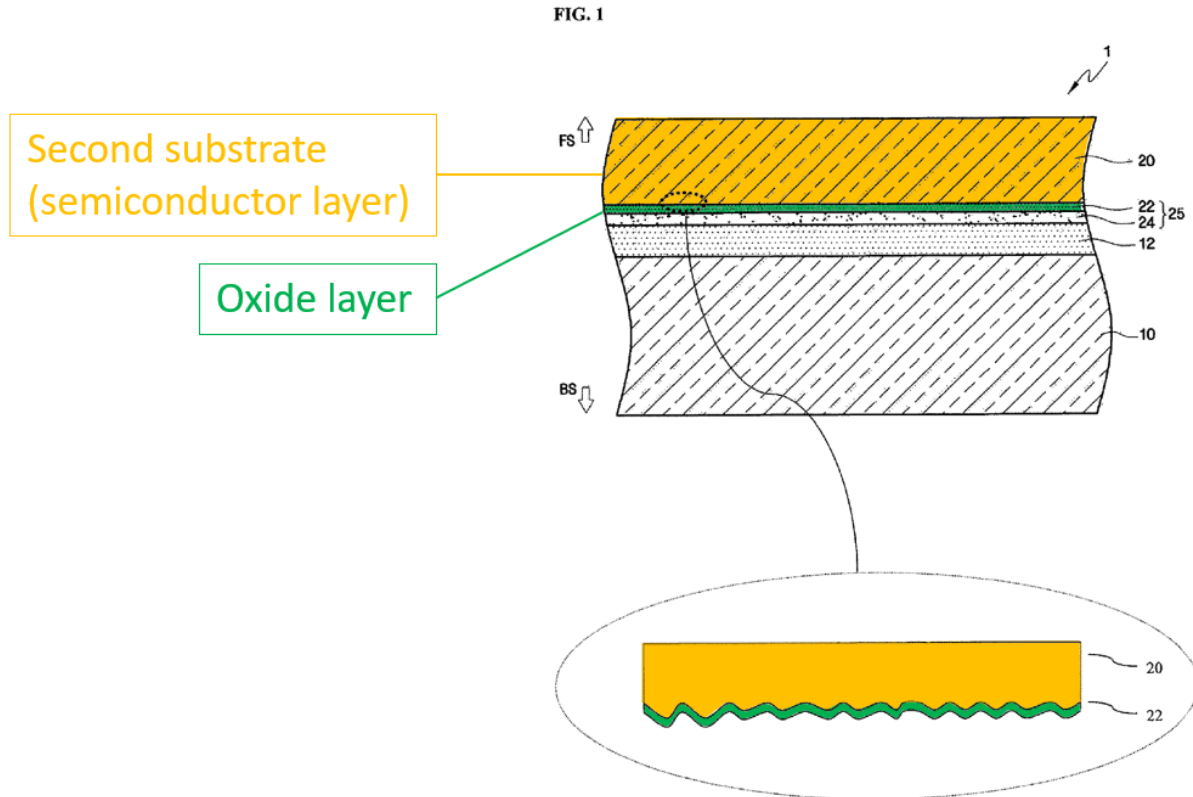
- e) **24[d]: “creating a plurality of shallow trench isolation surface features on a light incident side of said semiconductor layer.”**

Park in view of Baggenstoss renders this limitation obvious.⁴ Ex-1004 ¶¶294-98.

Park discloses that “reflections may ... be reduced by processing the second substrate 20 to have an uneven surface.” Park, [0072]. Figure 1 depicts the second

⁴ Claim 24 does not require limitation 24[d] to be performed after limitations 24[a]-[c]. See *Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1371 (Fed. Cir. 2003).

substrate 20's uneven surface adjacent to an oxide layer 22. Park, [0060]-[0061]; *see also* Ex-1004 ¶295.



Park, Fig. 1 (annotated).

Park discloses that the second substrate 20's uneven surface is on the light incident side of the second substrate 20. Figure 7 depicts that the second substrate 20's uneven surface (adjacent to the oxide layer 22) is on the backside (indicated by the label "BS"), which has a micro lens structure 180 for incident light. Park, [0078]; *see also* Park, [0060] (disclosing that Park's image sensor is a backside illuminated device); Ex-1004 ¶296.

Similarly, Baggenstoss discloses creating an optoelectronic device with a grating interface formed by trenches 144 (i.e., the claimed plurality of shallow trench isolation surface features). Baggenstoss, [0031]-[0032], [0009]; *see also* Ex-1004 ¶297.

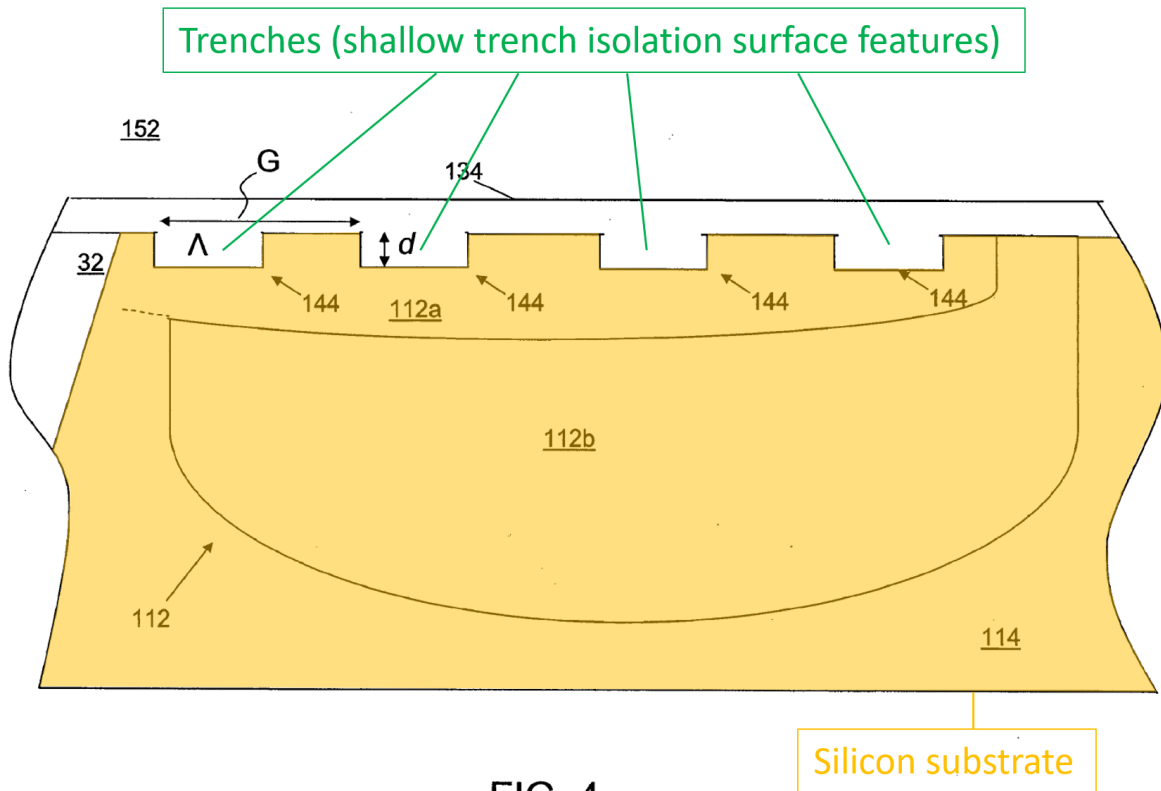


FIG. 4

Baggenstoss, Fig. 4 (annotated).

Baggenstoss's trenches 144 correspond to the claimed shallow trench isolation surface features for the same reasons discussed above regarding claim 4. Ex-1004 ¶298. And Baggenstoss discloses that the trenches 144 are on the light incident side of a silicon substrate 114. Baggenstoss, Fig. 3, [0031]. It would have been obvious to use Baggenstoss's trenches in connection with Park's process for the reasons discussed above in Section VIII.I.1. Ex-1004 ¶298.

3. Claim 25

- a) **“The method of claim 24, wherein the step of creating the plurality of shallow trench isolation surface features comprises generating an array of surface features using shallow trench isolation etching.”**

Park in view of Baggenstoss renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case. Ex-1004 ¶¶299-303.

In the 737 Case, Petitioner proposed that the ’737 patent term “shallow trench isolation etching” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning, and to the extent a construction is required, it means, “etching a pattern of shallow trenches.” Ex-1014, 4; Ex-1015, 2-3.

Baggenstoss discloses creating an optoelectronic device with a grated interface formed by trenches 144 (i.e., the claimed plurality of shallow trench isolation surface features comprising an array of surface features). Baggenstoss, [0031]-[0032], [0009]; *see also* Ex-1004 ¶301.

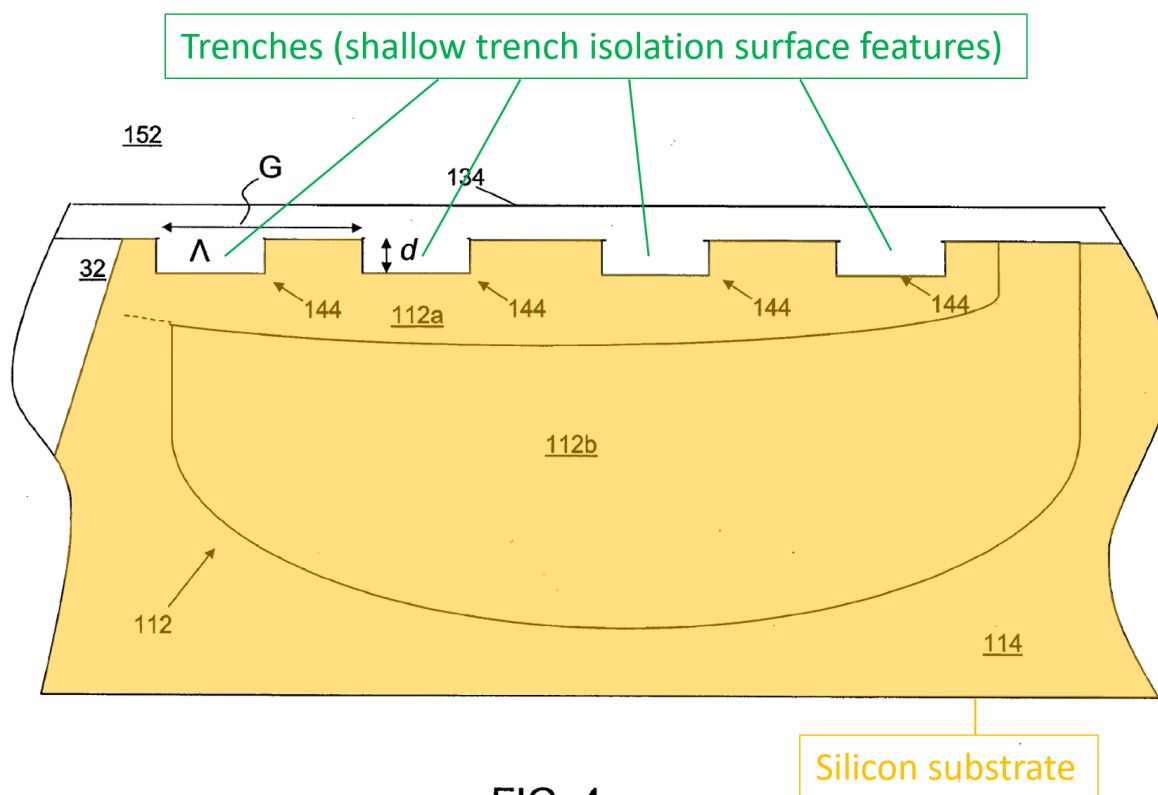


FIG. 4

Baggenstoss, Fig. 4 (annotated).

As discussed above regarding claim 4 in Ground A-2, Baggenstoss discloses that its shallow trench isolation surface features are formed by etching a pattern of shallow trenches. Baggenstoss, [0038]; *see also* Ex-1004 ¶302.

Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the trenches and the shallow trench isolation in Baggenstoss, as discussed above regarding claim 4. Ex-1004 ¶303.

IX. SECONDARY CONSIDERATIONS

Petitioner is unaware of evidence of secondary considerations of non-obviousness. Petitioner reserves the right to rebut any purported objective evidence of non-obviousness raised by Patent Owner.

X. THE BOARD SHOULD NOT USE ITS DISCRETION TO DENY INSTITUTION

A. 35 U.S.C. § 314(a)

The Board should not exercise its discretion to deny institution under 35 U.S.C. §314(a). No other petitions have been filed against the '682 patent and thus the *General Plastic* factors for serial petitions do not weigh against institution. Under *Apple Inc. v. Fintiv, Inc.*, IPR2020-0019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential), the district court litigation is still at an early stage, and trial on issues including the validity of the '682 patent is scheduled for April 2026. In addition, the other *Fintiv* factors would not justify denying institution. By the time of institution, the district court's claim construction briefing would not have even begun, and the fact discovery deadline would be about five months away. Discretionary denial is further inappropriate here because this petition presents compelling evidence of unpatentability. Accordingly, the *Fintiv* factors should not be applied to deny institution of this proceeding.

B. 35 U.S.C. § 325(d)

The Board likewise should not deny institution under §325(d). When evaluating discretionary denial arguments under §325(d), the Board reviews: “(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential).

Here, the first prong of *Advanced Bionics* is not satisfied. One of the two primary references, Park, was not previously presented to the Office, and it does not involve the same or substantially the same arguments previously presented to the Office. (The other primary reference Haddad138, the secondary reference Haddad204, and a parent application of the secondary reference Baggenstoss were listed in an IDS along with almost 900 other documents, but were not substantively argued or otherwise meaningfully addressed during examination.) Accordingly, any analysis by the Board of 325(d) issues should end with prong 1. *See, e.g., Fusion Orthopedics, LLC v. Extremity Medical, LLC*, IPR2023-00894, Paper 15 at 34-35 (P.T.A.B. Nov. 17, 2023).

Even were the Board to reach the second prong, it too is not met. The petition describes the examiner's errors in a manner material to the patentability of the Challenged Claims. The examiner did not consider Park, and the examiner erred by overlooking the materiality of the Haddad138, Haddad204, and a parent application of Baggenstoss to the Challenged Claims during examination.

XI. CONCLUSION

Petitioner respectfully requests *inter partes* review and cancellation of the Challenged Claims of the '682 patent.

Date: November 22, 2024

Respectfully submitted,

By: /Scott C. Weidenfeller/

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CERTIFICATION OF WORD COUNT

I certify that the foregoing complies with the type-volume limitation of 37 C.F.R. § 42.24 and contains 13,967 words based on the word count indicated by the word-processing system used to prepare the paper, and excluding those portions exempted by § 42.24(a).

Date: November 22, 2024

/Scott C. Weidenfeller/

Scott C. Weidenfeller (Reg. No. 54,531)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6 and 42.105, I hereby certify that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,347,682 under U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq.*, together with its supporting exhibits, Petitioner’s Explanation of Parallel Petitions, and Power of Attorney was served by Federal Express for Saturday delivery, a means at least as fast and reliable as Priority Mail Express®, on the following correspondence address of record for patent owner:

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Date: November 22, 2024

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