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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

SIONYX, LLC,
Patent Owner.

Case IPR2025-00064
Patent 10,347,682 B2

PATENT OWNER'S PRELIMINARY RESPONSE

37 C.F.R. § 42.107 and 35 U.S.C. § 313

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LIST OF PATENT OWNER'S EXHIBITS

PO Exhibit Number	Description
	Filed and Served on February 13, 2025 with Patent Owner's Motion for <i>Pro Hac Vice</i> Admission of Andrew P. Zappia Under 37 C.F.R. § 42.10
2001	Declaration of Andrew P. Zappia in Support of Patent Owner's Motion for <i>Pro Hac Vice</i> Admission
	Filed and Served on March 12, 2025 with Patent Owner's Preliminary Response
2002	Second Amended Docket Control Order dated December 27, 2024 (ECF No. 50) in <i>SiOnyx, LLC v. Samsung Electronics, Co., Ltd.</i> , Case No. 2:24-cv-00408-JRG (E.D. Tex.)
2003	Memorandum Opinion and Order dated August 30, 2024 (ECF No. 18) in <i>SiOnyx, LLC v. Samsung Electronics, Co., Ltd.</i> , Case No. 2:24-cv-00408-JRG (E.D. Tex.)
2004	Excerpts of Defendants' P.R. 3-3 Invalidity Contentions served October 30, 2024, in <i>SiOnyx, LLC v. Samsung Electronics, Co., Ltd.</i> , Case No. 2:24-cv-00408-JRG (E.D. Tex.)

CLAIM LISTING FOR U.S. PATENT NO. 10,347,682

1. [1Preamble] An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:
 - [1a] a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,
 - [1b] a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,
 - [1c] a support substrate coupled to said semiconductor layer, and
 - [1d] a first bonding layer disposed between the semiconductor layer and the support substrate,
 - [1e] wherein said optoelectronic device is a photosensitive imager device capable of detecting visible and infrared electromagnetic radiation.
2. The device of claim 1, wherein the semiconductor layer is single crystal silicon.
3. The device of claim 1, wherein the shallow trench isolation surface features are formed in the semiconductor layer.
4. The device of claim 1, wherein the shallow trench isolation surface features have a substantially uniform height.

5. The device of claim 1, wherein the shallow trench isolation surface features are not uniform in height.
6. The device of claim 1, further comprising a device layer coupled to the semiconductor layer on said side opposed to the light incident side.
7. The device of claim 1, wherein said first bonding layer comprises any of silicon oxide, silicon nitride and amorphous silicon.
8. The device of claim 1, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.
9. The device of claim 1, wherein said bonding layer has a thickness in a range of about 30 nm to about 3 microns.
10. The device of claim 1, wherein said bonding layer has a thickness in a range of about 40 nm to about 2 microns.
11. The device of claim 1, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.
12. The device of claim 1, wherein said shallow trench isolation surface features comprise pyramids.

13. The device of claim 1, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.

14. The device of claim 1, wherein said plurality of shallow trench isolation surface features comprise multiple etched levels.

15. The device of claim 1, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.

16. The device of claim 1, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.

17. The device of claim 1, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.

18. The device of claim 1, wherein said textured region allows the semiconductor layer to experience multiple passes of light.

19. The device of claim 1, further comprising a second bonding layer positioned between the first bonding layer and the support substrate.

20. The device of claim 19, further comprising a reflector layer disposed between the first bonding layer and the second bonding layer.

21. The device of claim 1, wherein the shallow trench isolation surface features are arranged according to a pattern.

22. The device of claim 21, wherein the pattern is an at least substantially uniform grid.

23. The device of claim 21, wherein the pattern is a non-uniform arrangement.

24. **[24Preamble]** A method of making an optoelectronic device, comprising:

[24a] bonding a semiconductor layer to a support substrate, wherein bonding the semiconductor layer to the support substrate includes:

[24b] depositing a first bonding layer onto the semiconductor layer; and

[24c] bonding the first bonding layer to a second bonding layer disposed on the support substrate; and

[24d] creating a plurality of shallow trench isolation surface features on a light incident side of said semiconductor layer.

25. The method of claim 24, wherein the step of creating the plurality of shallow trench isolation surface features comprises generating an array of surface features using shallow trench isolation etching.

26. The device of claim 1, further comprising deep trench isolation for isolating the device.

27. The device of claim 26, wherein said deep trench isolation provides light trapping functionality.

28. **[28Preamble]** An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:

[28a] a semiconductor layer having a light incident side and an opposed side,

[28b] said semiconductor layer having multiple doped regions forming at least one junction,

[28c] a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,

[28d] a support substrate coupled to said semiconductor layer,
and

[28e] a first bonding layer disposed between the semiconductor layer and the support substrate,

[28f] a second bonding layer positioned between the first bonding layer and the support substrate, and

[28g] a reflector layer disposed between the first bonding layer and the second bonding layer.

29. The device of claim 28, wherein said shallow trench isolation surface features comprise pyramids.

30. The device of claim 28, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.

31. The device of claim 28, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.

32. The device of claim 28, wherein the shallow trench isolation surface features have a substantially uniform height.

33. The device of claim 28, wherein the shallow trench isolation surface features are not uniform in height.

34. The device of claim 28, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.

35. The device of claim 28, wherein said photosensitive imager device is capable of detecting visible and infrared electromagnetic radiation.
36. The device of claim 28, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.
37. The device of claim 28, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.
38. The device of claim 28, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.
39. The device of claim 28, wherein said textured region allows the semiconductor layer to experience multiple passes of light.
40. The device of claim 28, further comprising deep trench isolation for isolating the device.
41. The device of claim 40, wherein said deep trench isolation provides light trapping functionality.

42. The device of claim 28, wherein the shallow trench isolation surface features are arranged according to a pattern.

43. The device of claim 42, wherein the pattern is an at least substantially uniform grid.

44. The device of claim 42, wherein the pattern is a non-uniform arrangement.

EX1001 ('682 Patent), 13:2-15:23.

I. INTRODUCTION

Pursuant to 37 C.F.R. § 42.107(a) and 35 U.S.C. § 313, SiOnyx, LLC (“Patent Owner”) submits this Preliminary Response to the Petition for *Inter Partes* Review of claims 1-44 of U.S. Patent No. 10,347,682 (“Petition”) (EX1001) (“the ’682 Patent”) filed by Samsung Electronics Co., Ltd. (“Petitioner”) on November 22, 2024, with a filing date accorded of November 22, 2024 (Paper 4). This Preliminary Response is timely filed.

It is Petitioner’s burden to show — by the Petition and its supporting evidence — that there is a reasonable likelihood that at least one of the Challenged Claims (defined below) is unpatentable. 37 C.F.R. § 42.108(c); *see also* 35 U.S.C. § 314(a). Petitioner has failed to meet this burden.

The Petition challenges all 44 claims of the ’682 Patent (the “Challenged Claims”). Claims 1, 24 and 28 are the independent claims.

II. SUMMARY OF ARGUMENTS

As an initial matter, institution should be denied under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020). The ’682 Patent is the subject of a case pending in the Eastern District of Texas (No. 2:24-cv-00408-JRG (“Litigation”)) scheduled for trial in early April 2026. On September 26, 2024, Petitioner filed an Amended Answer and Counterclaims in the Litigation asking for

a declaratory judgment that all claims of the '682 Patent are invalid. Petitioner served Invalidity Contentions in the Litigation on October 30, 2024, before this Petition was filed. The claim construction briefing and hearing will be completed by October 15, 2025, and the case will be tried in April 2026. Here, an institution decision is due by June 12, 2025, and a final written decision would not be expected (if institution is granted) until June 2026, long after the Litigation is concluded. This fact, and the other *Fintiv* factors, strongly support discretionary denial.

Institution should also be denied because Petitioner has failed to meet its burden to show a reasonable likelihood that at least one of the Challenged Claims is unpatentable. Specifically, Petitioner fails to show that Haddad¹³⁸¹ alone (claim 1), or in combination with Alie (claim 28) or Park in combination with Baggenstoss (claim 24) render any independent claim unpatentable. The other combinations directed to dependent claims do not cure these deficiencies as to the independent claims, warranting denial of institution.

Despite casting its Ground A-1 argument as anticipation, Petitioner has not set forth a case for anticipation of any of the Challenged Claims. Specifically,

¹ Reference identifications used herein have the same meaning as ascribed to them in the Petition unless otherwise defined herein.

Haddad138 does not disclose, teach, or suggest “a textured region comprising a plurality of shallow trench isolation surface features,” nor does Haddad138 disclose, teach, or suggest that this claimed textured region is “located on the light incident side of the semiconductor layer.” These limitations are present in each independent claim and missing from Petitioner's Ground references. Recognizing this, Petitioner first attempts to assume away the “shallow trench isolation surface features” aspect of the invention by asserting (without evidence in Haddad138) that the element is present. In apparent recognition that Haddad138 does not anticipate, Petitioner also proposes to modify Haddad138, using pure hindsight, to move the absent “shallow trench isolation surface features” to the “light incident side of the semiconductor layer” so that Haddad138 allegedly matches the claims of the '682 Patent. However, Petitioner fails to offer any showing that a person of ordinary skill in the art (“POSITA”) would have made the proposed modification with a reasonable expectation of success, a required showing for obviousness. Neither the combination of Haddad138 with Alie² (Ground A-3) nor the proposed combination of Park and Baggenstoss (Ground B-1) nor the remaining combinations directed to

² This same Alie reference is the basis for co-pending petition Case No. IPR2025-00065.

dependent claims (Grounds A-2 through A-8), cure this fatal deficiency. The Petition fails for at least these reasons. Institution should therefore be denied.

III. THE BOARD SHOULD EXERCISE ITS DISCRETION AND DENY INSTITUTION

On February 28, 2025, the Patent Office rescinded former Director Kathi Vidal's 2022 memorandum, titled "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation."

("Memorandum"). The Patent Office now directs parties in post-grant proceedings to "refer to [PTAB] precedent for guidance, including *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential)..." ("*Fintiv*"). See USPTO Bulletin Feb 28, 2025 ("Guidance"). The Guidance adds that "[t]o the extent any other PTAB or Director Review decisions rely on the Memorandum, the portions of those decisions relying on the Memorandum shall not be binding or persuasive on the PTAB." *Id.* In view of *Fintiv* and the Guidance, Patent Owner urges the Patent Trial and Appeal Board ("the Board") to deny institution of this Petition because it would cause the parties, the District Court, and the Board to incur significant inefficiencies and risks inconsistent outcomes, which are cautioned against in *Fintiv* and *NHK Spring* (defined below).

On June 3, 2024, Patent Owner filed the Litigation against Petitioner asserting infringement of the '682 Patent. In September of 2024, Petitioner responded by filing a counterclaim asking the District Court to grant a declaratory judgment of

invalidity. Two months later, Petitioner filed this duplicative Petition relying on the same prior art that Petitioner asked the District Court to consider in the Invalidity Contentions filed in support of its counterclaim.³ The invalidity and infringement contentions have already been exchanged in the Litigation, in October 2024 and January 2025, respectively. *See* EX2002 (Second Amended Docket Control Order). Fact discovery will close in November 2025, and expert discovery will close soon after in December 2025. Trial will commence in the beginning of April 2026, well before the Board's deadline to issue a Final Written Decision in this IPR proceeding (if instituted), which would be around June 2026. Also, the Litigation involves the same claim construction standard, invalidity theories, and prior art as the Petition. Under the Board's precedential orders in *Fintiv* and *NHK Spring*, and the new Guidance, the Board should exercise its discretion to deny institution under 35 U.S.C. § 314(a).

A. Institution Should Be Denied Under 35 U.S.C. § 314(a)

Section 314(a) and the Guidance gives the Board discretion to deny institution because of efficiency considerations stemming from parallel proceedings on the same patent. *See NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 19-20 (PTAB Sept. 12, 2018) (precedential, designated

³ Petitioner also relies on a Prior Art Product in its Invalidity Contentions.

May 7, 2019) (“*NHK Spring*”). The Litigation is precisely the parallel proceeding that supports discretionary denial, particularly given the significant resources that the parties and the District Court have already invested in the Litigation to vet the very same issues as presented in this Petition. In the Board’s precedential *Fintiv* decision, the Board set forth six factors for determining “whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5-6 (PTAB Mar. 20, 2020) (precedential). When evaluating these factors, “the Board takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Google LLC v. Personalized Media Commc’ns, LLC*, IPR2020-00720, Paper 16 at 5 (PTAB Aug. 31, 2020) (citing *Fintiv*, IPR2020-00019, Paper 11 at 5-6). Here, all six *Fintiv* factors weigh against institution.

B. The *Fintiv* Factors Strongly Favor Discretionary Denial

First, a discretionary denial may not be appropriate if the District Court or other tribunal granted a stay or evidence exists that one may be granted if the IPR proceeding is instituted. The Petitioner has not moved to stay the Litigation based on this IPR proceeding, nor is there any indication that it will do so. Further, the District Court is very unlikely to grant such a stay at this stage. The District Court in this case has already denied a motion to stay the Litigation in favor of a pending

ITC investigation also filed by Patent Owner against Petitioners.⁴ *See* EX2003 (Memorandum Opinion and Order Denying Stay). The District Court is unlikely to stay the Litigation now, when it has progressed even further into the schedule. This favors denial of institution.

The second *Fintiv* factor addresses the proximity of a trial date to the Board's projected statutory deadline for a final written. Here, the trial date is set for April 2026, and a final written decision would not issue until approximately June 2026, months after the trial. This factor also favors denial of institution.

Third, significant investment in the parallel proceeding by the District Court and the parties favors discretionary denial. It is unquestionable that, nearly one year in, the parties and the District Court have already invested (and will continue to invest) enormous time and resources in the Litigation, and this factor therefore favors denial of institution.

Fourth, the overlap between issues raised in the Petition and in the Litigation favor denial of institution. Here, the issues presented as to the validity of the '682 Patent are nearly identical. The '682 Patent has been challenged by two parallel petitions that set forth a total of thirteen Grounds for invalidity. The Petitioner's

⁴ That ITC case does not involve the '682 Patent. *See Certain Photonics Devices with Pixels and Products Containing the Same*, Inv. No. 337-TA-1403.

counterclaim and supporting Invalidity Contentions, served in the Litigation on October 30, 2024, assert the same prior art references as those that have been asserted in the Petition. *See* EX2004 (Excerpts of Defendants' Invalidity Contentions). In addition to the same prior art references being applied in both tribunals, the Petitioner challenges the '682 Patent claims based on a prior art product. Of course, the Petition cannot challenge the claims based on prior art products, and this also weighs in favor of denying the Petition, as the District Court will consider all the prior art proffered by Petitioner in the Litigation. This factor favors denial of institution.

Fifth, identity of parties favors denial of institution. Here, the Petitioner is the same party as the named Defendant in the Litigation and Patent Owner is the plaintiff in the Litigation. This factor therefore favors denial of institution.

Finally, Patent Owner notes that additional considerations also favor denial. Sections 314(a) and 325(d) and efficiency considerations favor denial because Petitioner's invalidity arguments are already being considered in a parallel proceeding. Patent Owner has undergone significant expense to address the invalidity positions set forth by Petitioner and will have to expend even more resources to substantively address those same invalidity arguments before the Board. This is antithetical to the preservation of the efficiency and consistency of the patent system, which is a key objective of *Fintiv*.

IV. INSTITUTION SHOULD BE DENIED FOR FAILING TO SHOW THAT THERE IS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

Petitioner proffers nine Grounds for attacking claims 1-44:

Ground	[Petition] Challenged Claims	Basis for Rejection
A-1	1-3, 6-8, 11-12, 15-18, 21, 26-27	§102 and/or §103: Haddad138 (EX1012)
A-2	4-5, 14, 21-22	§103: Haddad138 (EX1012) and Baggenstoss (EX1007)
A-3	9-10, 13, 19-20, 28-31, 34-42	§103: Haddad138 (EX1012) and Alie (EX1006)
A-4	23	§103: Haddad138 (EX1012) and Haddad204 (EX1009)
A-5	23	§103: Haddad138 (EX1012) and Park (EX1010)
A-6	32-33, 42-43	§103: Haddad138 (EX1012), Alie (EX1006), and Baggenstoss (EX1007)
A-7	44	§103: Haddad138 (EX1012), Alie (EX1006), and Haddad204 (EX1009)
A-8	44	§103: Haddad138 (EX1012), Alie (EX1006), and Park (EX1010)
B-1	24-25	§103: Park (EX1010) and Baggenstoss (EX1007)

See Petition, 5-6.

As discussed below, Petitioner has failed to meet its burden to show a reasonable likelihood that at least one of the Challenged Claims is unpatentable under these Grounds.

A. Ground A-1: Petitioner Has No Anticipation Position and A POSITA Would Not Have Been Motivated To Modify Haddad138 As Proposed

Among other limitations, claim 1 requires “a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation.” Petitioner asserts that Haddad138 “discloses this limitation, or at a minimum, renders this limitation obvious.” Petition, 22. Petitioner appears to be arguing either anticipation or obviousness. However, all its invalidity arguments for the Challenged Claims depend on, first, reading the “shallow trench isolation surface features” claim language out of the claims, and second, modifying Haddad138 such that the purported textured region in Haddad138 is located on the light incident side of the semiconductor layer. Petition, 24-26.

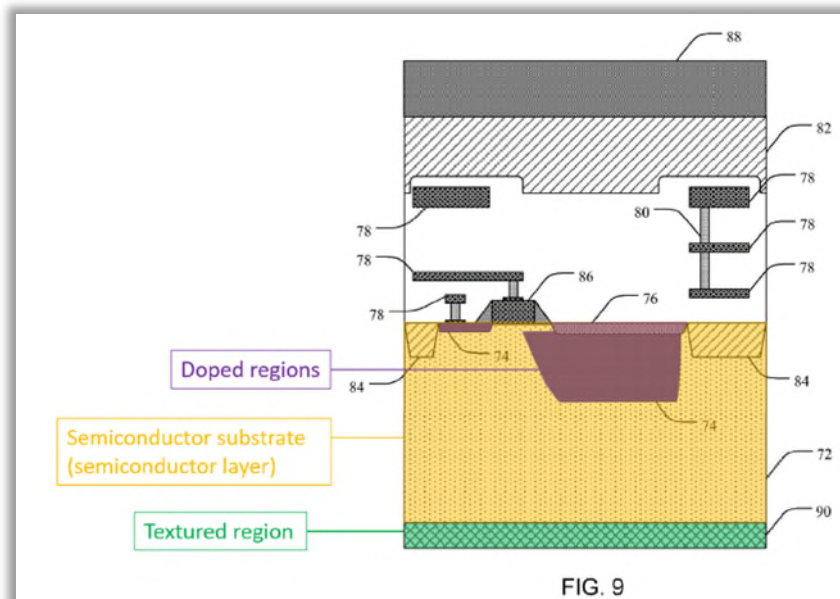
Claim 1 requires “shallow trench isolation surface features.” During prosecution of the '682 Patent, claim 1 was amended to add this and other limitations. Petitioner dismisses this language by equating, without evidence from the reference, structures in Haddad138 with the claimed shallow trench isolation (“STI”) surface features. But Haddad138 does not disclose, teach, or suggest STI surface features comprising a textured region. Haddad138 mentions STI only in the context of using it, or alternatively using deep trench isolation, to reduce

optical and electrical crosstalk between pixels. EX1012 (Haddad138), [0085], [0090]. No other description or mention of shallow trench isolation appears in Haddad138, let alone any suggestion to use shallow trench isolation surface features in a textured region as claimed. Nor is there any teaching or suggestion in Haddad138 that such a solution is needed or desired. Petitioner's expert provides no additional support other than stating that STI was well known. The fact that STI was known (including in Haddad138), but was **not used as part of a textured region**, supports the non-obviousness of such use. Haddad138 fails as an obviousness reference for this reason alone.

Petitioner then relies on its faulty assumption of the presence of STI surface features in Haddad138's textured region to next modify Haddad138 in further support of its invalidity theory. This admission that Haddad138 needs to be modified to support Petitioner's invalidity theory eliminates it as anticipatory art. Further, Petitioner's obviousness theory relies only on an assertion that a POSITA *could* modify the Haddad138 reference. The Petition and its supporting declaration are silent on the critical requirement for showing motivation to combine based on a modification to the prior art: why a POSITA *would have made* the modification. Petitioner's obviousness argument is therefore legally deficient.

1. Petitioner's anticipation argument is unsupported and contrary to the specification

The embodiment in Haddad138 relied upon by Petitioner does not disclose a device with texture comprising a plurality of shallow trench isolation surface features on the light incident side of the semiconductor layer, as required by claim 1. In fact, the opposite is true. Petitioner relies on the embodiment of Haddad138 illustrated in Figure 9, reproduced below:



Petition, 24 (annotated by Petitioner). Claim 1 limits the location of the “textured region” (90, highlighted in green) to “the light incident side of the semiconductor layer” (72, yellow). For this embodiment of Haddad138 to meet that limitation, light would need to be incident on the device from the bottom side of Figure 9.

Figure 9 of Haddad138 illustrates the device of Figure 7 of Haddad138 after the performance of additional manufacturing steps. EX1012 (Haddad138), [0084]

(“FIGS. 7-11 show various steps in the manufacture of a photosensitive pixel.”)

Figures 7 and 9 illustrate a “front side illumination (FSI) photosensitive pixel device,” meaning that “light enters the semiconductor substrate from the direction of the multiple doped regions,” *e.g.*, from the top of Figure 9. *Id.*, [0084], [0087], [0049]. Thus, the relied-upon embodiment of Haddad138 does not anticipate claim 1, because it is configured as an FSI (front side illuminated) device with texture on the opposite side of the semiconductor layer.

While still asserting anticipation, Petitioner acknowledges that Figure 9 must be modified to meet claim 1. Petitioner attempts to modify the figure by describing it as a back side illuminated (BSI) configuration, and states “[i]n a BSI configuration of the Figure 9 device, therefore, the surface features of the textured region 90 correspond to the claimed shallow trench isolation surface features located on the light incident side of the semiconductor layer.” Petition, 26. Setting aside that there are no shallow trench isolation surface features as already discussed, this admission dooms Petitioner’s anticipation argument. Where modification is required to meet the elements of a claim, the argument “invoke[s] the question of obviousness, not anticipation.” *Net MoneyIN, Inc. v. Verisign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008); *see also Enplas Display Device Corp. v. Seoul Semiconductor Co.*, 909 F.3d 398, 405 (Fed. Cir. 2018) (“Prior art that must be modified to meet the disputed claim limitation does not anticipate the

claim.”). Here, the relied-upon Figure 9 meets claim 1 only if it is modified from the disclosed FSI configuration to a BSI configuration. Petitioner's anticipation argument fails.

2. Petitioner offers no motivation to modify Haddad138

While Petitioner attempts to cast its position against claim 1 as anticipation, as discussed above, Petitioner's argument requires hindsight bias and modification of Haddad138. As a result, the only invalidity theory that could be discerned from the Petition might be one of obviousness. However, even if considered an obviousness assertion, Ground A-1 still fails because Petitioner offers no showing on motivation to combine.

“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (emphasis in original). Here, Petitioner does not offer any showing on any motivation to modify Figure 9 of Haddad138 to change the configuration from a FSI to BSI architecture. Rather, Petitioner, at best, presents Haddad138's disclosure as one that could be modified to become a BSI device. Simply creating a BSI version of Haddad138, however, would not result in the claimed invention.

Haddad138 has a disclosure of BSI devices (*e.g.* Figure 15) and a separate disclosure of the Figure 9 FSI device. In both figures, the textured region is opposite the light incident side of the semiconductor layer. *See, e.g.*, EX1012 (Haddad138), [0093] (“[a] textured region 156 can be coupled to the semiconductor substrate 72 **opposite the lens...**”). These two disclosures do not allow Petitioner to modify Figure 9 into a different BSI device than in Figure 15 without showing why a POSITA would have made such a modification. *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (finding a motivation required even when “combining multiple embodiments from a single reference.”)

While the law allows for obviousness arguments based on a single reference, “there must be a showing of a suggestion or motivation to modify the teachings of that reference.” *SIBIA Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1356 (Fed. Cir. 2000). Petitioner offers no showing whatsoever on motivation. Even if Petitioner's arguments are accepted as true, the Petition is deficient because it presents nothing on “showing of a suggestion or motivation to modify” the Haddad138 reference. *Id.* Because Petitioner's arguments are legally insufficient to show obviousness, Ground A-1 fails.

3. Petitioner fails to allege a reasonable expectation of success

Setting aside Petitioner's failure to make a showing on motivation, Petitioner's arguments also fail because Petitioner did not allege a reasonable

expectation of success. The Federal Circuit has held that obviousness only succeeds if a POSITA “can make the combination with a reasonable expectation of success.” *Gen. Elec. Co. v. Raytheon Techs. Corp.*, 983 F.3d 1334, 1352 (Fed. Cir. 2020). Here, Petitioner offers no showing that a POSITA would be able to modify the embodiment of Figure 9 to be back side illuminated with a reasonable expectation of success. *See In re Stepan Co.*, 868 F.3d at 1346 n.1 (“combining multiple embodiments from a single reference” requires “a reasonable expectation that such a combination would be successful.”) Nor does the disclosure of Haddad138 or the expert declaration of Dr. Lebby (EX1004) address reasonable expectation of success. Ground A-1 fails for this additional reason.

B. Ground A-2: Petitioner's Combination Of Haddad138 With Baggenstoss Does Not Address The Shortcomings Of Ground A-1

Petitioner asserts that the combination of Haddad138 with Baggenstoss renders obvious dependent claims 4-5, 14, and 21-22. Ground A-2 relies on the same modification to Haddad138 as discussed above. *See* Petition, 43-58. As a result, Ground A-2 fails for the same reasons as Ground A-1.

C. Ground A-3: Petitioner's Combination Of Haddad138 With Alie Does Not Address The Shortcomings Of Ground A-1

Petitioner asserts that the combination of Haddad138 with Alie renders obvious claims 9-10, 13, 19-20, 28-31, and 34-42. Ground A-3 relies on the same

modification to Haddad138 as discussed above. *See* Petition, 58-71. As a result, Ground A-3 fails for the same reasons as Ground A-1.

D. Ground A-4: Petitioner's Combination Of Haddad138 With Haddad204 Does Not Address The Shortcomings Of Ground A-1

Petitioner asserts that the combination of Haddad138 with Haddad204 renders obvious claim 23. Ground A-4 relies on the same modification to Haddad138 as discussed above. *See* Petition, 71-74. As a result, Ground A-4 fails for the same reasons as Ground A-1.

E. Ground A-5: Petitioner's Combination Of Haddad138 With Park Does Not Address The Shortcomings Of Ground A-1

Petitioner asserts that the combination of Haddad138 with Park renders obvious claim 23. Ground A-5 relies on the same modification to Haddad138 as discussed above. *See* Petition, 74-77. As a result, Ground A-5 fails for the same reasons as Ground A-1.

F. Ground A-6: Petitioner's Combination Of Haddad138 With Alie And Baggenstoss Does Not Address The Shortcomings Of Ground A-1

Petitioner asserts that the combination of Haddad138 with Alie and Baggenstoss renders obvious claims 32-33 and 42-43. Ground A-6 relies on the same modification to Haddad138 as discussed above. *See* Petition, 77-79. As a result, Ground A-6 fails for the same reasons as Ground A-1.

G. Ground A-7: Petitioner's Combination Of Haddad138 With Alie And Haddad204 Does Not Address The Shortcomings Of Ground A-1

Petitioner asserts that the combination of Haddad138 with Alie and Haddad204 renders obvious claim 44. Ground A-7 relies on the same modification to Haddad138 as discussed above. *See* Petition, 80-81. As a result, Ground A-7 fails for the same reasons as Ground A-1.

H. Ground A-8: Petitioner's Combination Of Haddad138 With Alie And Park Does Not Address The Shortcomings Of Ground A-1

Petitioner asserts that the combination of Haddad138 with Alie and Park renders obvious claim 44. Ground A-8 relies on the same modification to Haddad138 as discussed above. *See* Petition, 82-83. As a result, Ground A-8 fails for the same reasons as Ground A-1.

I. Ground B-1: Petitioner's Combination Of Park With Baggenstoss Does Not Address The Shortcomings Of Ground A-1

Park is directed to an optoelectronic device configured to minimize dark current. One embodiment disclosed by Park includes an "uneven surface" designed to reduce reflection. EX1010 (Park), [0072]. Park describes that the uneven surface is made by processing a silicon substrate or oxide layer, which may further include an antireflective layer. *Id.* Notably, this is the only mention of an uneven surface in Park, and no further disclosure is provided as to the structure of

the uneven surface nor how to make it. Figure 1 provides little insight as to the meaning of “uneven surface” as used in Park.

Baggenstoss is directed to a pixel cell for a grated interface for use within the context of imaging devices. Baggenstoss describes that a photosensor is formed within a silicon substrate, and the silicon substrate is covered by an oxide layer arranged to form a grated interface with the silicon substrate. EX1007 (Baggenstoss), [0014]. This grated interface can be formed through a variety of methods including chemical etching and reactive ion etching. EX1007 (Baggenstoss), [0038]. Baggenstoss describes how the grated interface allegedly serves to improve the performance of an image sensor by functioning as an antireflective layer. EX1007 (Baggenstoss), [0031]. Baggenstoss expounds upon the alleged benefits of the antireflective properties of the grated interface, describing how reflection decreases where the period between each grating structure decreases from 1000 nm to 340 nm, wherein the percentage of incident light reflected is nearly eliminated. EX1007 (Baggenstoss), [0034]. In relation to the grated interface, Baggenstoss focuses exclusively upon its antireflective properties, and how to implement the antireflective grated interface.

Petitioner fails to show that a POSITA would have been motivated to combine Park with Baggenstoss to achieve the claimed invention. “[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been*

motivated to make the combinations or modifications of prior art to arrive at the claimed invention.” *Belden*, 805 F.3d at 1073 (emphasis in original). Here, aside from the hindsight use of the claims as a template, Petitioner does not offer any showing on any motivation for why a POSITA would combine Park, directed to the reduction of dark current, with the grated surface of Baggenstoss, and further modify that combination to achieve the claimed invention. Specifically, Petitioner makes no showing as to how the use of the antireflective grated interface of Baggenstoss in place of the antireflective coating in Park would impact Park’s goal of minimizing dark current. Moreover, Petitioner fails to explain how this combination and modification would achieve the “textured region” as claimed in the ’682 Patent.

The Federal Circuit has held that obviousness only succeeds if a POSITA “can make the combination with a reasonable expectation of success.” *Gen. Elec.*, 983 F.3d at 1352. Here, Petitioner offers no showing that a POSITA would be able to combine Park with Baggenstoss with a reasonable expectation of success. Dr. Lebby’s belief that such a combination would have been within the abilities of a POSITA does not show how or why such a combination would have been successful. Ground B-1 fails for this additional reason.

V. CONCLUSION

For the reasons set forth above, Petitioner has failed to demonstrate a reasonable likelihood that it would prevail with respect to any of the Challenged Claims. Thus, *inter partes* review of the '682 Patent should be denied.

Respectfully submitted,

Date: March 12, 2025

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this preliminary response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains **4,305** words, according to the word-processing system used to prepare this preliminary response, excluding the parts of this preliminary response that are exempted by 37 C.F.R. § 42.24(c) (including the table of contents, a table of authorities, an exhibits list, a listing of facts, a certificate of service or this certificate of word count, or appendix of exhibits).

Date: March 12, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), this is to certify that on this 12th day of March, 2025, I caused to be served a true and correct copy of the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE (with EX2002-2004)** by e-mail (as agreed in the Service Information section of the Petition):

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