ABSTRACT OF THE DISCLOSURE

Photosensitive devices and associated methods are provided. In one aspect, for example, a photosensitive imager device can include a semiconductor layer having multiple doped regions forming a least one junction, a textured region coupled to the semiconductor layer and positioned to interact with electromagnetic radiation. The textured region can be formed from a series of shallow trench isolation features.

SAMSUNG EX. 1002 - 1/1684

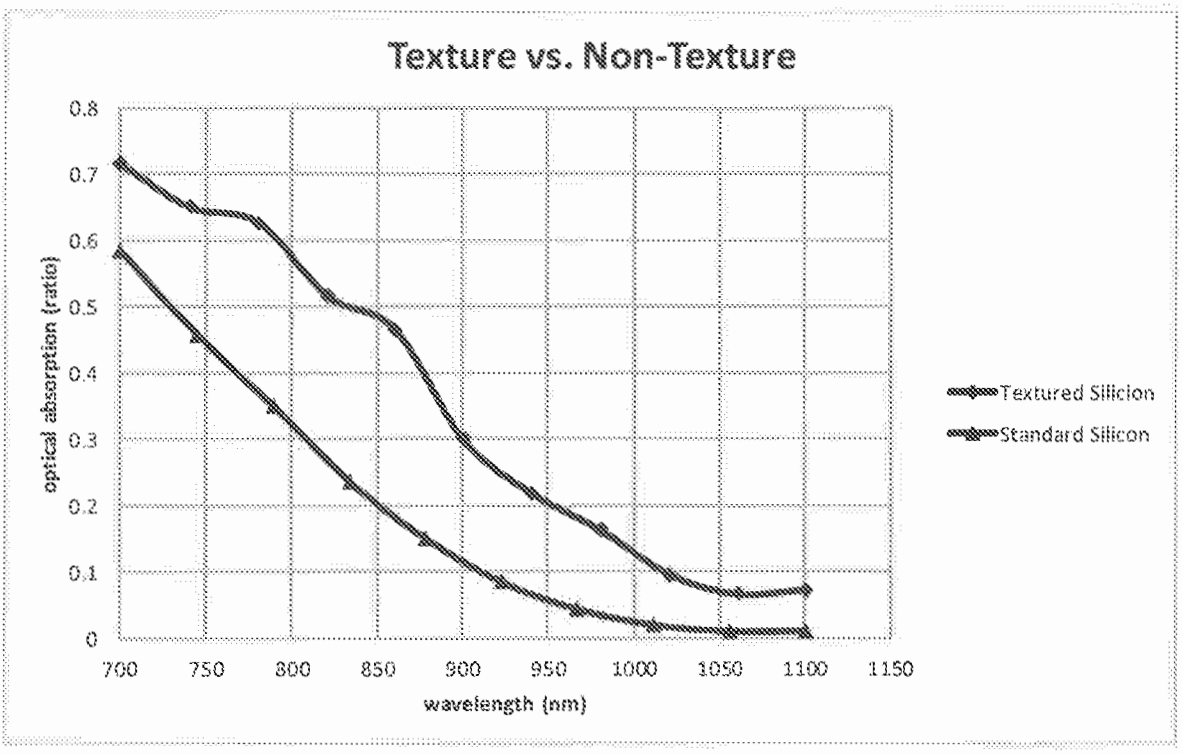

Texture vs. Non-Texture
optical absorption (ratio)
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
700
750
800
850
900
950
1000
1050
1100
1150
wavelength (nm)
Textured Silicion
Standard Silicon

FIG. 1

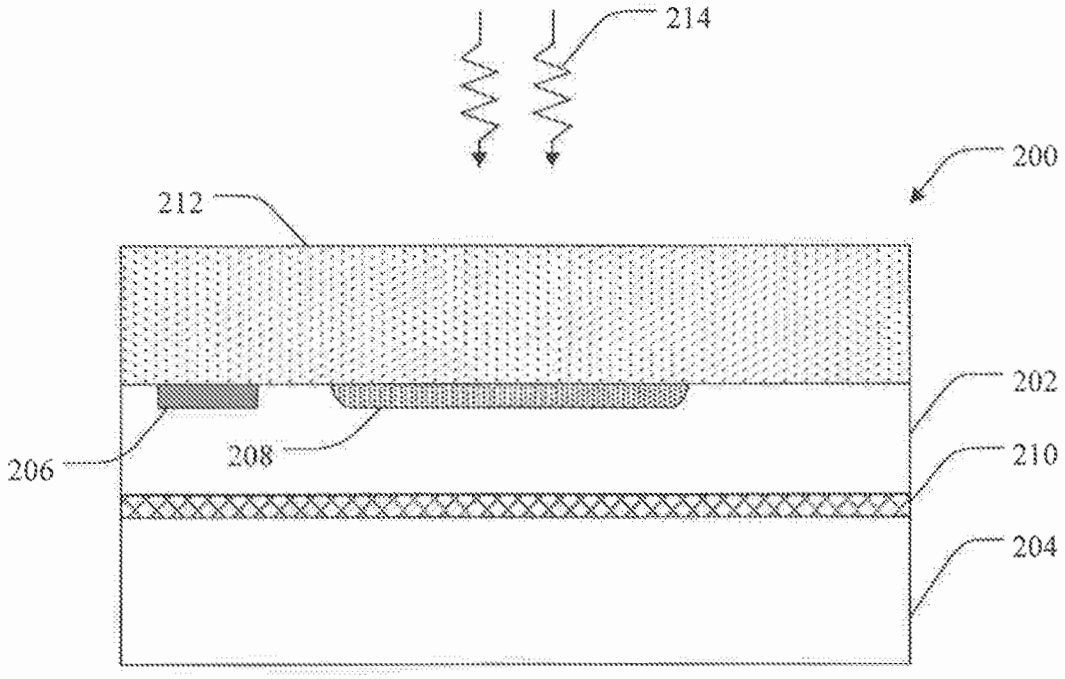

214
200
212
202
206
208
210
204

FIG. 2

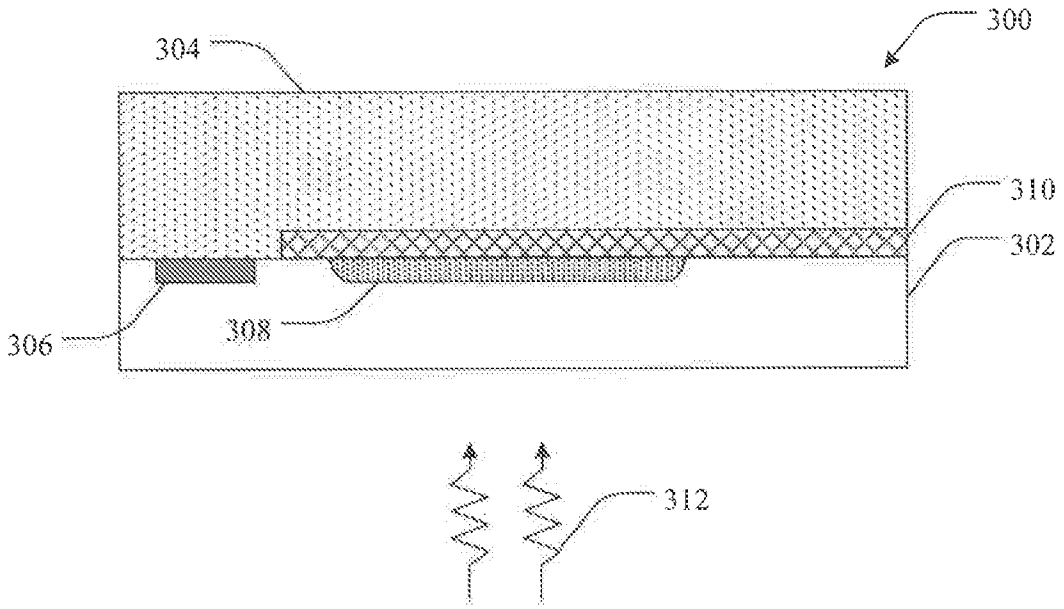


FIG. 3

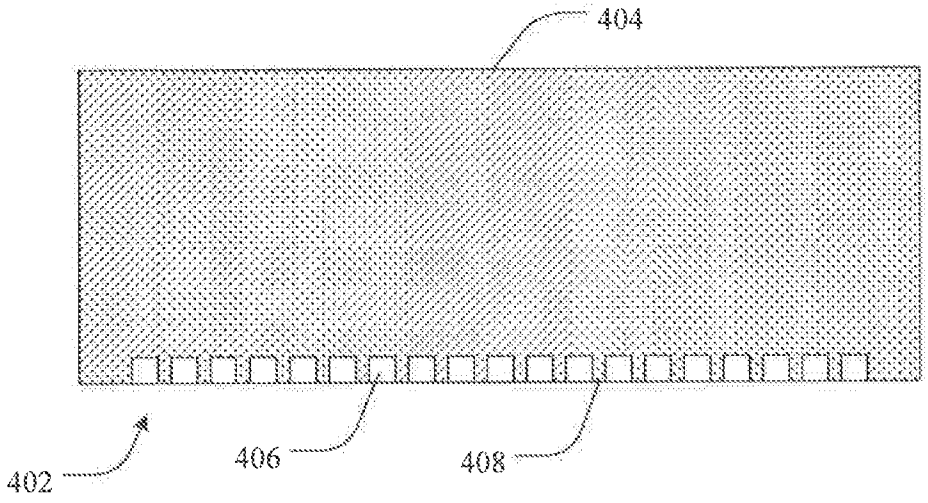


FIG. 4

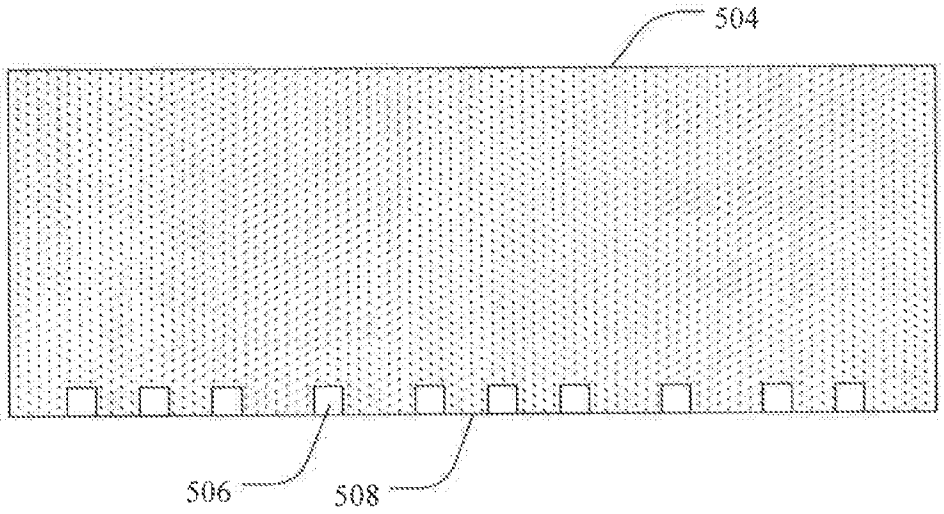


FIG. 5

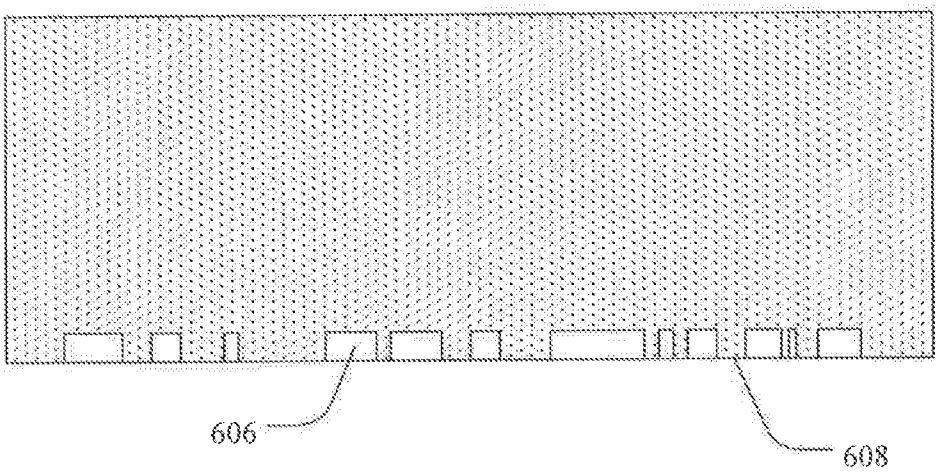


FIG. 6

Docket No.: 048-P2

Substitute Form PTO/AIA/01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	Shallow Trench Textured Regions and Associated Methods

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☑ United States application or PCT international application number 14/084,392 filed on 11/19/2013

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Homayoon Haddad Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

Docket Number: 3035-060.NP

Substitute Form PTO/AIA/01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	Shallow Trench Textured Regions and Associated Methods

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application or,

☑ United States application or PCT international application number 14/084,392

filed on 11/19/2013

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Jutao Jiang Date (Optional): 9/10/2015

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Filer:	Andrew W. Schultz/Jillian Stockel
Attorney Docket Number:	143705.06021

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1600

Electronic Acknowledgement Receipt

EFS ID:	29401015
Application Number:	15614256
International Application Number:	
Confirmation Number:	4345
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	136549
Filer:	Andrew W. Schultz/Jillian Stockel
Filer Authorized By:	Andrew W. Schultz
Attorney Docket Number:	143705.06021
Receipt Date:	05-JUN-2017
Filing Date:	
Time Stamp:	17:58:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1600
RAM confirmation Number	060617INTEFSW17592400
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	ADS.pdf	1823484 8f771c301be3f50fe970f064d2cf258d97fa201c	no	9
Warnings:					
Information:					
2		Application.pdf	178200 b09fcd4a3be4845de20ba6df7ffa7890d0f564d0	yes	22

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	18
Claims	19	21
Affidavit-Rule 130(a)-AIA (FITF) ONLY	22	22

Warnings:					
Information:					
3	Drawings-only black and white line drawings	Figures.pdf	804944 326383ec86d6f1570288bd7e49d90fa461f09754	no	3
Warnings:					
Information:					
4	Oath or Declaration filed	Declarations.pdf	145349 d62c0133fbcef012ae170346611b1f4f385b59f7	no	2
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	35252 9a63307dedeb413dafb1d640cf109a7659cae1b6	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	2987229

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	143705.06021
	Application Number	
Title of Invention	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Homayoon		Haddad	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Beaverton	OR	US

Mailing Address of Inventor:

Address 1	16640 SW Sanderling Ct.
Address 2	
City	Beaverton
State/Province	OR
Postal Code	97007
Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jutao		Jiang	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Tigard	OR	US

Mailing Address of Inventor:

Address 1	15121 SW Kenton Dr.
Address 2	
City	Tigard
State/Province	OR
Postal Code	97224
Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	143705.06021
	Application Number	
Title of Invention	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	136549		
Email Address	DocketingBN@pepperlaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS		
Attorney Docket Number	143705.06021	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	3	**Suggested Figure for Publication (if any)**	2

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	136549		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	143705.06021
	Application Number	
Title of Invention	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending			Remove
Application Number	Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of		14884181	2015-10-15
Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14884181	Continuation of	14084392	2013-11-19	9209345	2015-12-08
Prior Application Status	Expired			Remove
Application Number	Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14084392	Claims benefit of provisional		61841326	2013-06-29

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	143705.06021
	Application Number	
Title of Invention	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	143705.06021
	Application Number	
Title of Invention	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	143705.06021
	Application Number	
Title of Invention	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	SiOnyx, LLC		
Mailing Address Information For Applicant:			
Address 1	100 Cummings Ctr.		
Address 2	Suite 243-F		
City	Beverly	**State/Province**	MA
Country	US	Postal Code	01915
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	143705.06021
	Application Number	
Title of Invention	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Andrew W. Schultz/			Date (YYYY-MM-DD)	2017-06-05
First Name	Andrew	Last Name	Schultz	Registration Number	66869

Additional Signature may be generated within this form by selecting the Add button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	143705.06021
	Application Number	
Title of Invention	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS

PRIORITY DATA

This application is a continuation of U.S. patent application Ser. No. 14/884,181, filed on October 15, 2015, which is a continuation of U.S. patent application Ser. No. 14/084,392, filed Nov. 19, 2013, which claims the benefit of U.S. Provisional Patent Application Ser. No. 61/841,326, filed on Jun. 29, 2013, each of which are incorporated herein by reference in their entirety.

BACKGROUND

The interaction of light with semiconductor materials has been a significant innovation. Silicon imaging devices are used in various technologies, such as digital cameras, optical mice, video cameras, cell phones, and the like. Charge-coupled devices (CCDs) were widely used in digital imaging, and were later improved upon by complementary metal-oxide-semiconductor (CMOS) imagers having improved performance. Many traditional CMOS imagers utilize front side illumination (FSI). In such cases, electromagnetic radiation is incident upon the semiconductor surface containing the CMOS devices and circuits. Backside illumination (BSI) CMOS imagers have also been used, and in many designs electromagnetic radiation is incident on the semiconductor surface opposite the CMOS devices and circuits. CMOS sensors are typically manufactured from silicon and can covert visible incident light into a photocurrent and ultimately into a digital image. Silicon-based technologies for detecting infrared incident electromagnetic radiation have been problematic, however, because silicon is an indirect bandgap semiconductor having a bandgap of about 1.1eV. Thus the absorption of electromagnetic radiation having wavelengths of greater than about 1100 nm is, therefore, very low in silicon.

SUMMARY

The present disclosure provides optoelectronic devices having enhanced light absorption characteristics, including systems incorporating such devices and various associated methods. In one aspect, for example, an optoelectronic device having

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enhanced absorption of electromagnetic radiation is provided. Such a device can include a semiconductor layer coupled to a support substrate and an array of shallow trench isolation surface features positioned between the semiconductor layer and the support substrate, the surface features positioned to interact with electromagnetic radiation that passes through the semiconductor layer. In one aspect, the semiconductor layer is single crystal silicon. In another aspect, a device layer can be coupled to the semiconductor layer on a side opposite the surface features.

In one aspect, a first bonding layer can be coupled between the semiconductor layer and the support substrate. While various configurations are contemplated, in one specific aspect first bonding layer can be coupled between the support substrate and the surface features. In another aspect, a second bonding layer can be positioned between the first bonding layer and the support substrate. In yet another aspect, a reflector layer can be disposed between the first bonding layer and the second bonding layer.

The surface features can have a variety of configurations and can be formed in a variety of locations between the semiconductor layer and the semiconductor support. For example, in one aspect the surface features can be formed in the support substrate. In another aspect, the surface features can be formed in the semiconductor layer. Furthermore, in one aspect the surface features can be arranged according to a predetermined pattern. In one specific aspect, such a predetermined pattern can be an at least substantially uniform grid. In specific aspect, such a predetermined pattern can be a non-uniform arrangement. Additionally, in one aspect the surface features can have an at least substantially uniform height. In another aspect, the surface features are not uniform in height.

Additionally, a variety of architectural configurations are contemplated. For example, in one aspect the device can be architecturally configured as a front-side illuminated optoelectronic device. In another aspect, the device can be architecturally configured as a back-side illuminated optoelectronic device.

In another aspect, a method of making an optoelectronic device is provided. Such a method can include creating an array of surface features using shallow trench isolation etching and bonding the array of surface features between a support substrate and a semiconductor layer. In another aspect, creating the array of surface features can further

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include creating the array of surface features on at least a portion of a surface of the semiconductor layer. In yet another aspect, creating the array of surface features further includes creating the array of surface features on at least a portion of a surface of the support substrate. Furthermore, in one aspect bonding the array of surface features between the support substrate and the semiconductor layer can further include depositing a first bonding layer onto the semiconductor layer and bonding the first bonding layer to a second bonding layer disposed on the support substrate. In some aspects a reflector can be deposited on at least one of the first bonding layer or the second bonding layer prior to bonding the semiconductor layer to the support substrate. In a further aspect the method can include thinning the semiconductor layer at a surface opposite the support substrate to a thickness of from about 1 microns to about 10 microns to create a pristine thinned surface and forming a device layer on the thinned surface. The semiconductor can then be further processed as desired to form the optoelectronic device.

BRIEF DESCRIPTION OF THE DRAWINGS

For a further understanding of the nature and advantage of the present disclosure, reference is being made to the following detailed description of embodiments and in connection with the accompanying drawings, in which:

FIG. 1 provides data showing the optical absorption of textured silicon compared to standard silicon as a function of wavelength in accordance with an embodiment of the present disclosure;

FIG. 2 is a cross-sectional view of an image sensor in accordance with another embodiment of the present disclosure;

FIG. 3 is a cross-sectional view of an image sensor in accordance with another embodiment of the present disclosure;

FIG. 4 is a cross-sectional view of a textured layer associated with a substrate in accordance with another embodiment of the present disclosure;

FIG. 5 is a cross-sectional view of a textured layer associated with the substrate in accordance with another embodiment of the present disclosure; and

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FIG. 6 is a cross-sectional view of a textured region associated with the substrate in accordance with another embodiment of the present layer.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the terms "light" and "electromagnetic radiation" can be used interchangeably and can refer to electromagnetic radiation in the ultraviolet, visible, near infrared and infrared spectra. The terms can further more broadly include electromagnetic radiation such as radio waves, microwaves, x-rays, and gamma rays. Thus, the term "light" is not limited to electromagnetic radiation in the visible spectrum. Many examples of light described herein refer specifically to electromagnetic radiation in the visible and infrared (and/or near infrared) spectra. For purposes of this disclosure, visible range wavelengths are considered to be from approximately 350 nm to 800 nm and non-visible wavelengths are considered to be longer than about 800 nm or shorter than about 350 nm. Furthermore, the infrared spectrum is considered to include a near infrared portion of the spectrum including wavelengths of approximately 800 to 1100 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1100 nm to 3 micrometers, and a mid-to-long wavelength infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to

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about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

As used herein, the term "detection" refers to the sensing, absorption, and/or collection of electromagnetic radiation.

As used herein, the term "backside illumination" refers to a device architecture design whereby electromagnetic radiation is incident on a surface of a semiconductor material that is opposite a surface containing the device circuitry. In other words, electromagnetic radiation is incident upon and passes through a semiconductor material prior to contacting the device circuitry.

As used herein, the term "frontside illumination" refers to a device architecture design whereby electromagnetic radiation is incident on a surface of a semiconductor material that contains the device circuitry. In other words, electromagnetic radiation is incident upon and passes through the device circuitry region prior to contacting the semiconductor material.

As used herein, the term "absorptance" refers to the fraction of incident electromagnetic radiation absorbed by a material or device.

As used herein, the terms "textured layer" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Such a surface topology can be formed by a variety of known STI techniques. It is noted that laser ablation techniques, at least in one aspect, are specifically disclaimed. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can include micron-sized structures (e.g. about 1 μm to about 10 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 10 μm. In another aspect, surface structures can be from about 100 nm to about 1 micron. A variety of criteria can be utilized to measure the size of such structures. For example, for cone-like structures the above ranges are intended to be measured from the peak of a structure to the valley formed between that structure and an adjacent neighboring structure. For structures such as nanopores, the above ranges are intended to be approximate diameters. Additionally, the surface structures can be spaced at various average distances from one another. In one aspect, neighboring structures can be spaced

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at a distance of from about 50nm to about 2 μm. Such spacing is intended to be from a center point of one structure to the center point of a neighboring structure.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range

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of "about 1 to about 5" should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

Traditional silicon photodetecting imagers have limited light absorption/detection properties. For example, such silicon based detectors can be mostly transparent to infrared light, particularly with thin silicon layers. In some cases, other materials such as InGaAs can be used to detect infrared light having wavelengths greater than about 1000 nm, silicon is still commonly used to detect wavelengths in the visible spectrum (i.e. visible light, 350 nm – 800 nm). Traditional silicon materials require substantial optical path lengths to detect photons from electromagnetic radiation having wavelengths longer than approximately 700 nm. As a result, visible light can be absorbed at relatively shallow depths in silicon, and absorption of longer wavelengths (e.g. 900 nm) in silicon of a standard wafer depth (e.g. approximately 750 μm) is poor. Increasing the thicknesses of the silicon layer to allow longer wavelength absorption thus greatly increases the thicknesses of the photodetecting imager.

The optoelectronic devices according to aspects of the present disclosure exhibit increased light absorption due to an increase in the effective optical path length for longer wavelengths of light as compared to traditional devices. The absorption depth in conventional silicon detectors is the depth into silicon at which the radiation intensity is reduced to about 36% of the value at the surface of the semiconductor. The increased optical path length of photons with the present silicon materials results in an apparent reduction in the absorption depth, or a reduced apparent or effective absorption depth. For example, the effective absorption depth of silicon can be reduced such that these longer wavelengths can be absorbed in silicon layers that are less than 850 microns thick.

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In other words, by increasing the optical path length, these devices are able to absorb longer wavelengths (e.g. > 1000 nm for silicon) within a thinner silicon material. In addition to absorbing light having longer wavelengths in thin silicon materials (e.g. less than 30 microns thick as compared to 700 microns thick), the response rate or response speed can also be increased by using such thin materials.

The optoelectronic devices of the present disclosure can be front side illumination (FSI) or back side illumination (BSI) devices. In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, can scatter off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can thus be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus at least partially avoiding the circuitry. A variety of lenses and lens configurations are contemplated, however in one aspect the lens can be a micro-lens.

BSI imagers, one the other hand, are configured such that incident light enters the device via the light sensitive region opposite the circuitry and is mostly absorbed prior to reaching the circuitry, thus greatly reducing scattering and/or noise. BSI designs also allow for greater sensitivity, smaller pixel architecture, and a high fill factor for the imager. Additionally, it should also be understood that devices according to aspects of the present disclosure, whether they be FSI or BSI, can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures.

Generally, and without limitation, the present disclosure provides a variety of optoelectronic devices, such as, broadband photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation, including associated methods of making such devices. In one specific aspect, for example, an optoelectronic device is provided having enhanced absorption of electromagnetic radiation. Such a device can include a semiconductor layer coupled to a support substrate and an array of shallow trench isolation surface features positioned between the semiconductor layer and the support substrate, the surface features positioned to interact with electromagnetic radiation that passes through the semiconductor layer.

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It has thus been discovered that such an array of shallow trench isolation surface features positioned in an architecturally appropriate manner can greatly increase the optical absorption of silicon materials. As is shown in FIG. 1, for example, such a textured region can increase the optical absorption of silicon as compared to non-textured silicon over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.

As can be seen in FIG. 2, for example, a FSI device is shown 200 having a semiconductor layer 202 coupled to a support substrate 204, where the semiconductor layer can include one or more doped regions 206, 208, that form at least one junction. A textured layer 210 including an array or plurality of STI surface features is positioned between the semiconductor layer 202 and the support substrate 204. A circuitry layer 212 is coupled to the semiconductor layer 202 on a side opposite the support substrate 204. Light 214 is shown impinging on the device 200 and passing through the circuitry layer 212 prior to contacting the semiconductor layer 202. Light 214 that is not absorbed by and subsequently passes through the semiconductor layer 202 contacts the textured layer 210 and is redirected back into the semiconductor layer 202, thus allowing light to be absorbed in a subsequent pass. As such, the textured layer 210 increases the effective optical path length of the light 214 as it passes through the device. In one aspect, the semiconductor layer can be single crystal silicon.

Turning to FIG. 3, a BSI device is shown 300 having a semiconductor layer 302 coupled to a support substrate 304, where the semiconductor layer can include one or more doped regions 306, 308, that form at least one junction. In this case the support substrate 304 can be a circuitry layer or a bulk substrate including a circuitry layer. A textured layer 310 including an array or plurality of surface features is positioned between the semiconductor layer 302 and the support substrate 304. Light 312 is shown impinging on the device 300 and passing through the semiconductor layer 302 without contacting any circuit elements that may be positioned in or at the support substrate 304. Light 312 that is not absorbed by and subsequently passes through the semiconductor layer 302 contacts the textured layer 310 and is redirected back into the semiconductor layer 302. As with the FSI device shown in FIG. 2, the textured layer 310 increases the effective optical path length of the light 312 as it passed through the device. In one

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aspect, the semiconductor layer can be single crystal silicon.

The multiple doped regions for both the FSI and the BSI case can have the same doping profile or different doping profiles, depending on the device. Furthermore, any number or configuration of doped regions is considered to be within the present scope. In some aspects the semiconductor layer can be doped, and thus can be considered to be a doped region.

Additionally, the device can include deep trench isolation (DTI) to isolate the imager and to provide light trapping functionality. In some aspects such a device can include a silicon handle wafer in addition to the support substrate to facilitate manipulation of the device. In some aspects, the support substrate can be a silicon handle wafer. One technique for coupling a silicon handle wafer to the semiconductor layer includes oxide bonding. Further details regarding substrates, bonding, and various imager details can be found in US Patent Application Serial Number 13/069,135, which is incorporated herein by reference.

Optoelectronic devices according to aspects of the present disclosure can include photodiodes or pixels that are capable of absorbing electromagnetic radiation within a given wavelength range. Such imagers can be passive pixel sensors (PPS), active pixel sensors (APS), digital pixel sensor imagers (DPS), or the like. Such devices can also be architecturally configured as a three or four transistor active pixel sensor (3T APS or 4T APS). Additionally, devices having greater than 4 transistors are also within the present scope. Such devices can also include pinned photodiode architectures as used in CMOS imagers. Also, such optoelectronic devices can be used in time-of-flight (TOF) applications, as well as various structured light applications. It is also contemplated that such devices can also be configured as rolling shutter or global shutter readout devices.

In some aspects, a device can include a passivation layer positioned between the textured layer and the doped regions. In some aspects, the passivation layer can be doped to create a surface field, as is described more fully below. It is noted, that with or without the passivation region, the textured region can be located on the light incident side of the semiconductor material, on a side of the semiconductor material opposite the light incident side, or both on the light incident side and opposite the light incident side. Additionally, the device can also include an electrical transfer element coupled to the

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semiconductor layer and operable to transfer an electrical signal from the doped regions. Additionally, an electrical transfer element can include a variety of devices, including without limitation, transistors, sensing nodes, transfer gates, transfer electrodes, and the like.

As has been described, the textured layer is comprised of a plurality of surface features, where such surface features have been formed in an array or other grouping across an interface between the semiconductor layer and the support substrate. In some aspects, the textured region can cover the entire interface between the semiconductor layer and the support substrate, while in other aspects the textured region may cover only a portion of the interface between the semiconductor layer and the support substrate. For example, in one aspect the textured layer can cover the interface between the materials at least in regions where light passing through the semiconductor layer would contact the interface. In another aspect, the textured layer can cover the interface between the materials only in regions where light passing through the semiconductor layer would contact the interface. As such, it should be understood that the coverage area of the textured layer can be dependent on the design of the device, as well as the intended pattern of light trapping and/or light redirection that is desired. It is thus intended that the scope of the present disclosure not necessarily be limited by the degree to which the interface includes textured layer.

Furthermore, in some aspects one or more intervening layers can be present between the semiconductor layer and the support substrate. Such layers can be used to facilitate bonding, for reflecting light, for a variety of other purposes. In one aspect, for example, one or more bonding layers can be utilized to facilitate bonding the support substrate to the semiconductor layer. In such cases, it can be beneficial to apply a first bonding layer to the semiconductor layer and a second bonding layer to the support substrate as a bonding mechanism. The bonding layer can include a material capable of facilitating bonding between the support substrate and the semiconductor layer. Non-limiting examples can include silicon oxides, silicon nitrides, amorphous silicons, and the like. The thickness of a given bonding layer can additionally vary depending on the manufacturing techniques utilized and preferences of the designer. In one aspect, however, a bonding layer can be thick enough to facilitate bonding and thin enough to

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minimize waveguide effects within the device. In another aspect, a bonding layer can have a thickness of from about 30 nm to about 3 microns. In yet another aspect, a bonding layer can have a thickness of from about 40 nm to about 2 microns.

The position of the textured layer can thus be affected by the nature of the coupling of the support substrate and the semiconductor layer as well as the location where the textured layer is formed. In one aspect, the textured layer can be formed in or on the semiconductor layer. In another aspect, the textured layer can be formed in or on the support substrate. For the situation where the textured layer is formed in or on the semiconductor layer, one or more bonding layers can be coupled between the support substrate and the textured layer. If two or more bonding layers are utilized, a first bonding layer can be formed on the textured layer, a second bonding layer can be formed on the support substrate, and the first and second bonding layers can then be bonded together.

For the situation where the textured layer is formed in or on the support substrate, one or more bonding layers can be coupled between semiconductor layer and the textured layer. For example, in one aspect one or more bonding layer can be coupled between the support substrate and the surface features. If two or more bonding layers are utilized, a first bonding layer can be formed on the textured layer, a second bonding layer can be formed on the semiconductor layer, and the first and second bonding layers can then be bonded together.

As has been described, a light reflector layer can additionally be disposed between any two of the above referenced layers or materials. For example, in one aspect a reflector layer can be applied to one side of the textured layer. In another aspect, a reflector layer can be applied to either side of a bonding layer. In one specific aspect, a reflector layer can be positioned between a first and second bonding layer. The reflector layer can include any material capable of reflecting light back into the semiconductor layer. Non-limiting examples can include metals, ceramics, oxides, glass, distributed Bragg reflector stacks, and the like, including alloys and combinations thereof.

The surface features of the textured layer can be made by any process capable of etching in a repeatable and predictable manner. In one aspect, however, the surface features can be formed by any number of shallow trench isolation (STI) techniques.

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While such manufacturing techniques are known, they have previously been utilized for creating regions of electrical isolation between circuit elements. Thus, such implementations have been utilized around the peripheries of circuit elements. The present scope, however, is directed to creating arrays of surface features in locations to interact with light. Through this interaction, light can be redirected, diffused, focused, or otherwise manipulated by the surface feature array.

Additionally, STI techniques can be used to form such surface features having a variety of shapes, patterns, and the like. In one aspect, for example, the surface features can be arranged into an array according to a predetermined pattern. In one specific aspect, such a predetermined pattern can be a uniform or substantially uniform grid. Additionally, a predetermined pattern can be an organized, an ordered, or a periodic pattern. In another aspect, the predetermined pattern can be a non-uniform or a substantially non-uniform pattern. Surface feature array patterns can also be disordered, quasi-periodic, random, or the like.

As has been described, the textured layer can function to diffuse light, to redirect light, and to thus increase the quantum efficiency of the device. In some cases, a portion of the light passes through the semiconductor layer to contact the textured layer. The surface features of the textured layer thus facilitate an increase the effective optical path length of the semiconductor layer. Such surface features can be micron-sized and/or nano-sized, and can be any shape or configuration that can be formed via a STI technique. Non-limiting examples of such shapes and configurations include cones, pillars, pyramids, inverted features, trenches, gratings, protrusions, and the like, including combinations thereof. Additionally, factors such as manipulating the feature sizes, dimensions, material type, dopant profiles, texture location, etc. can allow tuning of the textured layer for a specific wavelength or range of wavelengths. In one aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be absorbed. In another aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be reduced or eliminated via filtering.

Textured layers according to aspects of the present disclosure can allow a semiconductor layer to experience multiple passes of light within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection can increases the effective

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optical path length, thus allowing a material such as silicon to absorb light at thicknesses that are less than standard silicon. As has been described, this increase in the effective optical path length of electromagnetic radiation in silicon increases the quantum efficiency of the device, thus leading to an improved signal to noise ratio.

The materials used for making the textured layer can vary depending on the design and the desired characteristics of the device. As such, any material that can be utilized in the construction of a textured region is considered to be within the present scope. In one aspect, the textured region can be formed directly on the semiconductor layer (e.g. a silicon epi-layer). In another aspect, an additional material can be deposited onto the semiconductor layer to support the formation of the textured layer. Non-limiting examples of such materials include semiconductor materials, dielectric materials, silicon, polysilicon, amorphous silicon, transparent conductive oxides, and the like, including composites and combinations thereof. In one specific aspect, the textured layer can be a textured polysilicon layer. Thus a polysilicon layer can be deposited onto the semiconductor layer, either directly or onto an intermediate passivation layer, and then textured to form the textured region. In another aspect, the textured layer can be a textured dielectric layer. In this case the textured layer can be a portion of a dielectric layer making up a passivation region disposed on the semiconductor layer. In yet another aspect the textured layer can be a transparent conductive oxide or another semiconductor material. In the case of dielectric layers, the textured layer can be a textured portion of a passivation layer or the textured layer can be formed from other dielectric material deposited over a passivation layer.

Various methods can be utilized to form STI features, and any such shallow trench formation technique is considered to be within the present scope. It is noted that, in one aspect, texturing techniques that involve laser ablation are specifically disclaimed from the present scope.

In some cases, the textured layer can be formed by using a patterned mask and photolithography, followed by etching to define a specific structure or pattern. In one aspect, STI techniques can be used to form the textured region. Various STI techniques are contemplated, and any such technique is considered to be within the present scope. In one non-limiting example, an oxide material is deposited on the material to be etched

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with shallow trenches. A uniform coating of a nitride material is deposited on the oxide material followed by a patterned coating of a resist material to be used as a mask. Thus the pattern of the mask will define the future pattern of the textured region. Any of a number of etch processes can then be applied across the layered material. As a result, regions of the layered material beneath the resist are protected from the etch, while regions of the layered material that are not located beneath the resist are etched by the process. This process is continued to produce a shallow trench (or a hole) etched in the unprotected regions between the resist material through the nitride material, the oxide material, and into the substrate. Following etching of the shallow trench, the resist material can be removed by any appropriate process. It is noted that, while the term "shallow trench" is used to describe the etching process, the resulting etch pattern is not limited to trenches, but also includes holes, pits, cones, and the like.

In some aspects, the etched regions can be left as open spaces. In other aspects, further processing can be performed to fill in the etched regions. For example, an oxide material can be deposited along the sides and bottom of the trenches similar to an oxide liner. Such can be deposited by a thermal oxide process, a direct oxide deposition, or any other useful process. Once the etched regions are sufficiently filled, the resulting surface can be further processed by techniques such as CMP processing, and then, once exposed, the nitride layer can be removed.

In another aspect, the etched regions can be highly doped along sidewalls and/or bottoms with a dopant profile to create a surface field. A back surface field can function to impede the movement of photo-generated carriers from the junction toward the textured layer, and as such the dopant profile should be designed accordingly. The use of the back surface field in the etched regions can thus be used to electrically passivate the regions around the textured layer.

The surface features can have a variety of configurations, structures, and sizes, depending on the desired characteristics of the resulting device. In one aspect, as is shown in FIG. 4 for example, surface features 402 are shown formed in a material layer 404, such as, for example, the semiconductor layer. The surface features in this case are arranged uniformly as a uniform grid pattern comprised of a series of spaces or holes 406 and lines 408 or pillars. Various uniform grid patterns are contemplated, and in one

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aspect the pattern can include a uniformly spaced series pillars surrounded by spaces, or vice versa depending on whether the pattern is viewed from the topside or the bottom side of the etched material. In another aspect, the uniform grid pattern can include a series of lines surrounding a uniformly spaced series of spaces or holes cut between the lines, or vice versa.

Additionally, as has been described, the etch pattern of surface features can be a predetermined nonuniform pattern. As is shown in FIG. 5, for example, the spaces 506 etched into the material layer 504 are of approximately the same size and shape and the lines or pillars 508 vary in width. FIG. 6 shows an etch pattern were both the spaces 606 and the lines or pillars 608 are varied. It should be noted that a variety of etch patterns are contemplated, and that the present scope should not be limited thereby. With respect to nonuniform patterns, in some aspects the patterns can be random, either for the line or pillar, the spaces, or both.

In addition to the pattern formed by the STI process, the depth of the etch can also have an impact on optical absorption. In one aspect, for example, the surface features can have a uniform or substantially uniform depth or height. While the depth or height can vary depending on the intended use and design of the device, in one aspect the height or depth can be from about 50 nm to about 2 microns. It is noted that, in standard STI processes, the processing depth is about 0.35 microns, which is also considered to be within the present scope. In another aspect, the surface features can have a non-uniform depth or height, and thus can vary across the surface of the textured layer. Such variation in depth can be random in some cases, and nonrandom in other cases depending on the desired design of the device. In one aspect, the depth or height can be from about 50 nm to about 2 microns. In some aspects discrete levels of depths can be utilized. For example, in one aspect one level may have a depth of 0.35 microns, while another level may have a depth of 0.7 microns. By using different masks, different depth levels can be achieved. Similarly, subsequent levels can be etched to create a third level, a fourth level, or more. It is noted that in some aspects each level can have a depth of from about 50 nm to about 2 microns.

As has been described, the various devices according to aspects of the present disclosure can exhibit increased absorption as compared to traditional photosensitive

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devices. For example, for an active semiconductor layer according to aspects of the present disclosure that has a thickness of from about 1 micron to about 10 microns, the absorption characteristics can be as follows: in one aspect the semiconductor layer can absorb from about 60% to about 80% of incident 700 nm light; in another aspect, the semiconductor layer can absorb from about 40% to about 60% of incident 850 nm light; in yet another aspect, the semiconductor layer can absorb from about 25% to about 40% of incident 940 nm light; in a further aspect, the semiconductor layer can absorb from about 15% to about 30% of incident 1000 nm light; and in yet a further aspect, the semiconductor layer can absorb from about 5% to about 10% of incident 1064 nm light. Furthermore, depending on the architecture, devices according to aspects of the present disclosure can exhibit external quantum efficiencies (EQE) that are from about 1% to about 5% less than the above described absorption values for a given wavelength of light. Additionally, it is further noted that the devices of the present disclosure have at least substantially the same dark current as a standard EPI device with no textured region.

While the present disclosure has focused on silicon materials, it should be understood that a variety of semiconductor materials are also contemplated for use and should be considered to be within the present scope. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof. In yet another aspect, the semiconductor materials can include any material that is useful for making imagers, including, Si, SiGe, InGaAs, and the like, including combinations thereof.

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A silicon semiconductor layer can be of any thickness that allows electromagnetic radiation detection and conversion functionality, and thus any such thickness of silicon material is considered to be within the present scope. In some aspects the textured layer increases the efficiency of the device such that the silicon material can be thinner than has previously been possible. Decreasing the thickness of the silicon material reduces the amount of silicon required to make such a device. In one aspect, for example, the silicon material has a thickness of from about 500 nm to about 50 μm. In another aspect, the silicon material has a thickness of less than or equal to about 100 μm. In yet another aspect, the silicon material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the silicon material can have a thickness of from about 5 μm to about 50 μm. In yet a further aspect, the silicon material can have a thickness of from about 5 μm to about 10 μm.

A variety of dopant materials are contemplated for both the formation of the multiple doped regions and to create a surface field at the shallow trench regions, and any such dopant that can be used in such processes is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material.

A dopant can be either charge donating or accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more positive or negative in polarity as compared to the semiconductor layer. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped. A highly doped region can also be formed on or near the doped region to create a pinned diode. In one non-limiting example, the semiconductor layer can be negative in polarity, and a doped region and a highly doped region can be doped with p+ and n dopants respectively. In some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type doping of the regions can be used. In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof.

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CLAIMS

What is claimed is:

1. An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:

a semiconductor layer coupled to a support substrate; and

an array of shallow trench isolation surface features positioned between the semiconductor layer and the support substrate, the surface features positioned to interact with electromagnetic radiation that passes through the semiconductor layer.

2. The device of claim 1, wherein the semiconductor layer is single crystal silicon.

3. The device of claim 1, further comprising a first bonding layer coupled between the semiconductor layer and the support substrate.

4. The device of claim 3, wherein the first bonding layer is coupled between the support substrate and the surface features.

5. The device of claim 3, further comprising a second bonding layer positioned between the first bonding layer and the support substrate.

6. The device of claim 5, further comprising a reflector layer disposed between the first bonding layer and the second bonding layer.

7. The device of claim 1, wherein the surface features are formed in the support substrate.

8. The device of claim 1, wherein the surface features are formed in the semiconductor layer.

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9. The device of claim 1, wherein the surface features are arranged according to a predetermined pattern.

10. The device of claim 9, wherein the predetermined pattern is an at least substantially uniform grid.

11. The device of claim 9, wherein the predetermined pattern is a non-uniform arrangement.

12. The device of claim 1, wherein the surface features have an at least substantially uniform height.

13. The device of claim 1, wherein the surface features are not uniform in height.

14. The device of claim 1, further comprising a device layer coupled to the semiconductor layer on a side opposite the surface features.

15. The device of claim 1, wherein the device is architecturally configured as a front-side illuminated optoelectronic device.

16. The device of claim 1, wherein the device is architecturally configured as a back-side illuminated optoelectronic device.

17. A method of making an optoelectronic device, comprising:

creating an array of surface features on a semiconductor layer using shallow trench isolation etching; and

bonding the array of surface features between a support substrate and a semiconductor layer.

18. The method of claim 17, wherein creating the array of surface features further comprises creating the array of surface features on at least a portion of a surface of the

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semiconductor layer.

19. The method of claim 17, wherein creating the array of surface features further comprises creating the array of surface features on at least a portion of a surface of the support substrate.

20. The method of claim 17, wherein bonding the array of surface features between the support substrate and the semiconductor layer further includes:

depositing a first bonding layer onto the semiconductor layer; and

bonding the first bonding layer to a second bonding layer disposed on the support substrate.

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Application Number: 15614256 Document Date: 06/05/2017

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/614,256	06/05/2017	2811	1600	143705.06021	20	2

CONFIRMATION NO. 4345

136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

FILING RECEIPT

OC000000092040302

Date Mailed: 06/15/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

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Jutao Jiang, Tigard, OR;

Applicant(s)

SiOnyx, LLC, Beverly, MA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 14/884,181 10/15/2015 PAT 9673250
which is a CON of 14/084,392 11/19/2013 PAT 9209345
which claims benefit of 61/841,326 06/29/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/614,256**

Projected Publication Date: 09/21/2017

Non-Publication Request: No

Early Publication Request: No
Title

SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/614,256

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE($)	FEE($)		RATE($)	FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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Assignee Name and Address: SiOnyx, LLC
100 Cummings Center, Suit 243F
Beverly, MA 01915

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Signature		Date	12/18/15
Name	Stephen Saylor	Telephone	508.561.4305
Title	CEO, SiOnyx LLC		

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Electronic Acknowledgement Receipt

EFS ID:	29590713
Application Number:	15614256
International Application Number:	
Confirmation Number:	4345
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	136549
Filer:	Reza Mollaaghababa/Jillian Stockel
Filer Authorized By:	Reza Mollaaghababa
Attorney Docket Number:	143705.06021
Receipt Date:	23-JUN-2017
Filing Date:	05-JUN-2017
Time Stamp:	13:21:21
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	SIOnyx_POA.pdf	135241 3e9144ffe18fe0c3a5f4a21cbd2f422b21d9b7ac	no	2

Warnings:

Information:	
Total Files Size (in bytes):	135241

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/614,256	06/05/2017	Homayoon Haddad	143705.06021

CONFIRMATION NO. 4345

POA ACCEPTANCE LETTER

136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

OC000000092381112

Date Mailed: 06/28/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/23/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rnegga/

SAMSUNG EX. 1002 - 51/1684

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/614,256	06/05/2017	Homayoon Haddad	143705.06021	4345

136549 7590 09/20/2017

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER
EVERHART, CARIDAD

ART UNIT	PAPER NUMBER
2895	

NOTIFICATION DATE	DELIVERY MODE
09/20/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketingbn@pepperlaw.com
davisdr@pepperlaw.com

Office Action Summary	Application No. 15/614,256	Applicant(s) HADDAD ET AL.	
	Examiner CARIDAD EVERHART	Art Unit 2895	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *6/5/2017* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the claims that are directed to the same invention so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 3, 4, 5, 6, 17, 18, 19, and 20 is/are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1, 3, 11, 12, 16, 18, and 20, respectively of prior U.S. Patent No. 9,209,345 B2. This is a statutory double patenting rejection.

Claim 6 is/are rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of prior U.S. Patent No. 9,673,250 B2. This is a statutory double patenting rejection.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

Claims 1-2, 7, 9-10, 12, and 14-15 are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Kawabata (US 5,100,478).

Kawabata discloses an optoelectronic device, as Kawabata discloses a solar cell and a method of forming a solar cell (col. 1, lines 5-10), which includes a semiconductor layer 3 shown in Fig. 1(a), and which is coupled to a support substrate 1 as shown in Fig. 1(a), an array of shallow trench isolation surface features positioned between the semiconductor layer and the support substrate, as shown in Fig. 1(a) (col. 4, lines 19-53). Kawabata further discloses that the surface features are positioned to interact with the electromagnetic radiation that passes through the semiconductor layer, as Kawabata discloses in Fig. 8 and in col. 8, lines 3-16 that the structure results in an increase of efficiency . Fig. 8 shows a detail of Fig. 6(e), which corresponds to Fig. 1(a),

in which 7 is the support substrate, 2 is the isolation structure, and 1' is semiconductor such as silicon (col. 7, lines 5-22).

Re claim 2: Kawabata discloses the semiconductor layer 3, also labeled 1' , may be monocrystalline (col. 9, lines 10-22).

Re claim 7: It is seem in Fig. 1(a) that surface features are formed in the support substrate, in the form of trenches with a pyramid shape .

Re claim 9: Kawabata discloses the features are arranged according to a pattern , as Kawabata discloses a mask is formed in order to pattern the recesses or trenches shown in Fig. 6(b) (col. 7, lines 25-45). This disclosure is a disclosure that the pattern of the features is predetermined, because the mask pattern is prepared prior to the forming of the pattern of the features in the substrate, so that the pattern is predetermined.

Re claim 10: Kawabata discloses in Fig. 3(a) a grid, which Kawabata discloses is a uniform grid , as Kawabata discloses the width of the pits to be about 1 micron (col. 4, lines 55-67).

Re claim 12: Kawabata discloses the pits to have a uniform depth of about .5 microns (col. 4, lines 55-67).

Re claim 14: Kawabata discloses a device layer 20 shown in Fig. 9(a) coupled to the semiconductor layer 3 (col. 8, lines 47-67).

Re claim 15: Kawabata discloses the device is a front-side illuminated device, as Fig. 1(a) shows light on the front side of the optoelectronic device disclosed by Kawabata.

Claims 8 and 16 are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Noguchi et al (US 5,370,747).

Noguchi et al disclose a photoelectronic conversion device in which a surface enhances conversion efficiency (col. 1, lines 7-23 and Fig. 5). Fig. 5 shows the arrangement includes the support substrate 51 is the surface through which the electromagnetic irradiation enters the device, which is an arrangement in which the backside is illuminated, which compared with the arrangement disclosed by Kawabata, as Kawabata discloses the irradiation entering the surface opposite the support substrate, as discussed in the rejection of claim 1 above. Noguchi et al further disclose electrodes 52 and 55, photoactive layer 53i, n-type layer 53n and photoelectric conversion layer 53 shown in Fig. 5 (col. 7, lines 12-24). Noguchi also discloses a textured layer which improves conversion efficiency (col. 7, lines 24-41). The photoelectric conversion layer and the photoactive layer and the n-type layer are included in the semiconductor layer (paragraph 1, lines 24-42). Fig. 5 shows that Noguchi discloses surface features are formed in the semiconductor layer, which includes the n type layer 53n (col. 7, lines 12-24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole

> would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103 are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 11 and 13 are rejected under 35 U.S.C. 103 as being unpatentable over Kawabata as applied to claim 1 above, and further in view of Weber et al (US 7,828,983 B2).

Kawabata discloses the limitations of claim 1 as discussed above in the rejection of claim 1. Kawabata is silent with respect to the pattern of the surface feature arrangement and the height of the surface features being nonuniform.

Weber et al discloses the forming of surface features to increase the capability of semiconductor to trap light (col. 1, lines 5-10). Weber et al disclose in Fig. 2D that some of the pits formed in the formation of a textured surface will be of different depths, or the features will be of different heights as shown in Fig. 2D (col. 7, lines 40-57).

Weber further discloses that the arrangement of the pattern of the textured surface can be ununiform, as Weber discloses the pattern may be random (col. 2, lines 27-39).

It would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have combined the device disclosed by Kawabata with the disclosure made by Weber et al with respect to the pattern of the textured surface being ununiform and the heights of the features being ununiform because Weber et al disclose that nonuniform height and pattern of the surface features increase capability of the surface of the device to trap light, so that one of ordinary skill in the art would have been motivated to have used the nonuniform arrangement and height of the features as being of art recognized suitability for an intended purpose (MPEP 2144.07) or of art recognized equivalence for the same purpose (MPEP 2144.06).

Claim(s) 1, 9, 11-12, and 14-15 is/are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Smirnov et al (US 2014/0352779 A1) in view of Iranmesh et al (US 5,236,863 A) (Multiple references 35USC102 rejections may be used to show a characteristic not disclosed in a reference is inherent(MPEP 2131.01)).

Smirnov et al discloses an optoelectronic device, as Smirnov et al disclose photovoltaic solar cells (para. 0047) which include nanostructured surfaces (para. 0047), and Smirnov et al also disclose the nanostructured surface results in enhanced absorption of electromagnetic radiation, as Smirnov et al disclose optimized light capture by the surface (para. 0055), which device includes a semiconductor layer 143b (para. 0058 and Fig. 14H) coupled to a support substrate 141g (Fig. 14H) and an array

of nanoridges 24 (para. 0050) which correspond to shallow trench isolation surface features (Fig. 14I), as Smirnov et al disclose the trench isolation surface features include intrinsic silicon layer143c between the silicon layer 143b and the support substrate (para. 0058 and Fig. 14H) positioned between the semiconductor layer and the support substrate (Fig. 14H) , to interact with electromagnetic radiation that passes through the semiconductor layer, as Smirnov et al disclose that optimized light capture by the surface features results (para. 0055).

Iranmesh et al disclose that intrinsic silicon provides trench isolation material (col. 1, lines 52-56 and col. 5, lines 32-49).

Iranmesh et al supports that the intrinsic silicon disclosed by Smirnov et al is inherently a trench isolation material.

Re claims 9, and 11-12: Smirnov et al disclose the surface features have a structure pattern (para. 0006) with a uniform arrangement and a uniform height, as Smirnov et al disclose a uniform height (para. 0057).

Re claim 14: Smirnov et al disclose a device layer opposite to the surface features, as Smirnov et al disclose diffusion regions 162 (Fig. 14H and para. 0002).

Re claim 15: Smirnov et al disclose a front-side illuminated device, as Smirnov et al disclose light capture from the front side which is the side on which the surface features are formed (para. 0055).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARIDAD EVERHART whose telephone number is

(571)272-1892. The examiner can normally be reached on Monday through Fridays 7:30-4:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on 571-272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CARIDAD EVERHART/
Primary Examiner, Art Unit 2895

Notice of References Cited	Application/Control No. 15/614,256	Applicant(s)/Patent Under Reexamination HADDAD ET AL.	
	Examiner CARIDAD EVERHART	Art Unit 2895	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-5,100,478 A	03-1992	Kawabata; Kiyoshi	H01L31/061	136/249
*	B	US-5,370,747 A	12-1994	Noguchi; Shigeru	H01L31/0236	136/256
*	C	US-7,828,983 B2	11-2010	Weber; Klaus Johannes	H01L31/02363	216/17
*	D	US-2014/0352779 A1	12-2014	Smirnov; Valery K.	H01L31/02363	136/256
*	E	US-5,236,863 A	08-1993	Iranmanesh; Ali	H01L21/76294	148/DIG.50
*	F	US-2015/0076468 A1	03-2015	Yamaguchi; Fujito	G02B1/118	257/40
*	G	US-9,673,250 B2	06-2017	Haddad; Homayoon	H01L27/14625	1/1
*	H	US-9,209,345 B2	12-2015	Haddad; Homayoon	H01L27/14625	1/1
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
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	Q					
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	S					
	T					

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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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BIB DATA SHEET

CONFIRMATION NO. 4345

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/614,256	06/05/2017	257	2895	143705.06021

APPLICANTS

SiOnyx, LLC, Beverly, MA;

INVENTORS

Homayoon Haddad, Beaverton, OR;
Jutao Jiang, Tigard, OR;

**** CONTINUING DATA ***************************

This application is a CON of 14/884,181 10/15/2015 PAT 9673250
which is a CON of 14/084,392 11/19/2013 PAT 9209345
which claims benefit of 61/841,326 06/29/2013

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

06/13/2017

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /CARIDAD EVERHART/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		OR	3	20	2

ADDRESS

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736
UNITED STATES

TITLE

SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS

FILING FEE RECEIVED		
1600	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

SAMSUNG EX. 1002 - 63/1684

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L10	96	(substrate or support or wafer) same ((oxide or "sio.sub.2" or sti or isolation) same (interface near12 nanostructure$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 09:28
L11	3	("9537024").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/09/14 09:40
L24	442	(light adj emitting) near1 (optoelectronic or (electro adj optical))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 09:53
L25	80	24 and solar	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 09:56
L47	411	((nanostructure$1 or concavities) same ((oxide or "sio.sub.2" or insulat$4 or dielectric))) same (optoelectronic or (viewing and angle))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 11:23
L48	16	(((nanostructure$1 or concavities or nanotrenches or isolation) near8 ((oxide or "sio.sub.2" or insulat$4 or dielectric)))) same ((viewing and angle))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 11:48
L54	176	52 and optoelectronic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 11:57
L55	105	(nanostructures same extraction) same (wafer or si or silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 12:06
L56	1	h01l31/028.ipc. and ((nanostructures same extraction) same (wafer or si or silicon))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 12:35
L57	4	h01l31/18.ipc. and ((nanostructures same extraction) same (wafer or si or silicon))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 12:35

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L58	105	((nanostructures same extraction) same (wafer or si or silicon))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 12:37
L59	11	58 AND ((H01L31/02363 OR H01L31/0236 OR H01L31/028 OR H01L31/02327).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/14 12:42

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L60	144	(((nanostructure$1 or concavities or nanotrenches) near8 (oxide or "sio.sub.2" or insulat$4 or dielectric)) same ((wafer or substrate) near6 (si or silicon or semiconductor))).clm.	US-PGPUB; USPAT	OR	ON	2017/09/14 13:01
L61	19	((((nanostructure$1 or concavities or nanotrenches) near8 (oxide or "sio.sub.2" or insulat$4 or dielectric)) same ((wafer or substrate) near6 (si or silicon or semiconductor))) and (solar or sensor or optoelectronic)).clm.	US-PGPUB; USPAT	OR	ON	2017/09/14 13:02
L62	51	((((nanostructure$1 or concavities or nanotrenches or (shallow adj trench$2) or sti) near8 (oxide or "sio.sub.2" or insulat$4 or dielectric)) same ((wafer or substrate) near6 (si or silicon or semiconductor))) and (solar or sensor or optoelectronic)).clm.	US-PGPUB; USPAT	OR	ON	2017/09/14 13:03

9/14/2017 1:06:49 PM
C:\Users\ceverhart\Documents\EAST\Workspaces\15618017.wsp

SAMSUNG EX. 1002 - 65/1684

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15614256	HADDAD ET AL.
	Examiner	**Art Unit**
	CARIDAD EVERHART	2895

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/14/2017								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
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	19	✓								
	20	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15614256	HADDAD ET AL.
	Examiner	Art Unit
	CARIDAD EVERHART	2895

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/02363, 0236, 02327, 028	9/14/2017	ce

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST attached	9/14/2017	ce
Reviewed parents	9/14/2017	ce

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
EAST	attached	9/14/2017	ce

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/614,256	06/05/2017	Homayoon Haddad	143705.06021

CONFIRMATION NO. 4345

136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

PUBLICATION NOTICE

OC000000094238490

Title:SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS

Publication No.US-2017-0271394-A1
Publication Date:09/21/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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SAMSUNG EX. 1002 - 68/1684

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Homayoon Haddad *et al.* Application No.: 15/614,256 Filed: June 5, 2017 For: SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	Confirmation No.: 4345 Art Unit: 2895 Examiner: Everhart, Caridad

Commissioner for Patents
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I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

March 20, 2018 (Dated) Electronic Signature: /Reza Mollaaghababa/ Reza Mollaaghababa , Reg. No. 43,810

AMENDMENT AND RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

This paper is filed in response to the non-final Office Action dated September 20, 2017.

Amendments to the Claims begin on page 2.

Remarks begin on page 6.

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LISTING OF CLAIMS

1. (Currently Amended) An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:

a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,

a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,

~~coupled to~~ a support substrate coupled to said semiconductor layer; ~~and~~

a first bonding layer disposed between the semiconductor layer and the support substrate

~~an array of shallow trench isolation surface features positioned between the semiconductor layer and the support substrate, the surface features positioned to interact with electromagnetic radiation that passes through the semiconductor layer~~.

2. (Original) The device of claim 1, wherein the semiconductor layer is single crystal silicon.

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The device of claim 1 ~~3~~, further comprising a second bonding layer positioned between the first bonding layer and the support substrate.

6. (Original) The device of claim 5, further comprising a reflector layer disposed between the first bonding layer and the second bonding layer.

7. (Canceled)

8. (Currently Amended) The device of claim 1, wherein the shallow trench isolation surface features are formed in the semiconductor layer.

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9. (Currently Amended) The device of claim 1, wherein the shallow trench isolation surface features are arranged according to a ~~predetermined~~ pattern.

10. (Original) The device of claim 9, wherein the ~~predetermined~~ pattern is an at least substantially uniform grid.

11. (Currently Amended) The device of claim 9, wherein the ~~predetermined~~ pattern is a non-uniform arrangement.

12. (Currently Amended) The device of claim 1, wherein the shallow trench isolation surface features have ~~an at least~~ a substantially uniform height.

13. (Currently Amended) The device of claim 1, wherein the shallow trench isolation surface features are not uniform in height.

14. (Currently Amended) The device of claim 1, further comprising a device layer coupled to the semiconductor layer on ~~a~~ said side opposed to the light incident side ~~opposite the surface features~~.

15. (Canceled)

16. (Canceled)

17. (Currently Amended) A method of making an optoelectronic device, comprising:

bonding a semiconductor layer to a support substrate; and

creating a plurality of shallow trench isolation surface features on a light incident side of said semiconductor layer ~~an array of surface features on a semiconductor layer using shallow trench isolation etching; and~~

~~bonding the array of surface features between a support substrate and a semiconductor layer~~.

18. (Currently Amended) The method of claim 17, wherein the step of creating the plurality of shallow trench isolation surface features comprises generating an array of surface features using shallow trench isolation etching ~~further comprises creating the array of surface features on at least a portion of a surface of the semiconductor layer~~.

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19. (Canceled)

20. (Currently Amended) The method of claim 17, wherein bonding the semiconductor layer to the support substrate ~~array of surface features between the support substrate and the semiconductor layer further~~ includes:

depositing a first bonding layer onto the semiconductor layer; and

bonding the first bonding layer to a second bonding layer disposed on the support substrate.

21. (New) The device of claim 1, further comprising deep trench isolation for isolating the device.

22. (New) The device of claim 21, wherein said deep trench isolation provides light trapping functionality.

23. (New) The device of claim 1, wherein said first bonding layer comprises any of silicon oxide, silicon nitride and amorphous silicon.

24. (New) The device of claim 1, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.

25. (New) The device of claim 1, wherein said bonding layer has a thickness in a range of about 30 nm to about 3 microns.

26. (New) The device of claim 1, wherein said bonding layer has a thickness in a range of about 40 nm to about 2 microns.

27. (New) The device of claim 1, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.

28. (New) The device of claim 1, wherein said shallow trench isolation surface features comprise pyramids.

29. (New) The device of claim 1, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.

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30. (New) The device of claim 1, wherein said plurality of shallow trench isolation surface features comprise multiple etched levels.

31. (New) The device of claim 1, wherein said optoelectronic device is a photosensitive imager device.

32. (New) The device of claim 31, wherein said photosensitive imager device is capable of detecting visible and infrared electromagnetic radiation.

33. (New) The device of claim 1, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.

34. (New) The device of claim 1, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to a about 1100 nm.

35. (New) The device of claim 1, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.

36. (New) The device of claim 1, wherein said textured region allows the semiconductor layer to experience multiple passes of light.

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REMARKS

Applicants amend claims 1, 5, 8, 9, 11, 12, 13, 14, 17, 18, 20, cancel claims 3, 4, 7, 15, 16, and 19 without prejudice and add new claims 21 – 36. Support for the amendments and the new claims can be found, e.g., at paragraphs [0034], [0035], [0038], [0043], [0049], [0053], and [0058] and the published patent application. No new matter is added.

Double Patenting Rejections

I. Claims 3, 4, 5, 6, 17, 18, 19 and 20 are rejected based on statutory double patenting relative to claims 1, 3, 11, 12, 16, 18 and 20, respectively, of U.S. Patent No. 9,209,345 ("the 345 Patent").

Applicants note that the limitation of claim 3 is now incorporated into independent claim 1. However, the language of claim 1, as amended, is distinct from that of claim 1 of the '345 Patent. Hence, Applicants respectfully request that the statutory double patenting rejection relative to claim 1 be withdrawn. Claim 4 is canceled without prejudice. And claims 5 and 6 depend, directly or indirectly, on claim 1 and hence their rejection should be similarly withdrawn. Further, the amendments presented to independent claim 17 obviate the statutory double patenting rejection raised relative to this claim. And claims 18 and 20 depend on claim 17 and hence their rejection should be similarly withdrawn (claim 19 is canceled without prejudice).

II. Claim 6 is rejected as claiming the same invention as that of claim 1 of U.S. Patent No. 9,673,250.

Claim 6 depends, via intervening claim 5, on claim 1. The amendments presented to claim 1 are believed to overcome the statutory double patenting rejection raised relative to this claim.

Rejections Pursuant to 35 U.S.C. 102

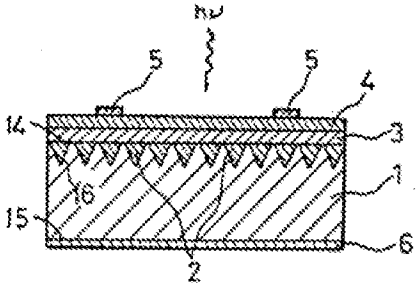
I. Claims 1-2, 7, 9-10, 12 and 14-15 are rejected as being anticipated by U.S. Patent No. 5,100,478 of Kawabata.

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Claim 1, as amended, recites an optoelectronic device having enhanced absorption of electromagnetic radiation, which comprises a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction, a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation, a support substrate coupled to said semiconductor layer; and a first bonding layer disposed between the semiconductor layer and the support substrate.

Kawabata is directed to "a solar cell including a member having a plurality of recesses filled with an electrically insulating material for forming a plurality of relatively small area, spaced apart rectifying junctions and/or for producing internal reflections of incident light for enhancing solar cell efficiency and to methods of manufacturing the solar cells." Col. 1, lines 5-12. FIG. 1(a) of Kawabata, reproduced below, depicts such a solar cell, which includes an n-type semiconductor substrate 1, such as silicon, that includes a first surface 14 and an opposed second surface 15. Col. 4, lines 19-25.

FIG. 1(a)



The substrate 1 includes a plurality of recesses 16 extending into the substrate from the first surface 14, where the recesses 16 are filled with an electrically insulating material 2, such as silicon dioxide, SiON, or silicon nitride. Col. 4, lines 25-29.

A p-type semiconductor film 3 is disposed on the first surface 14 and forms a rectifying junction with substrate 1 where it is in contact with that substrate. Col. 4, lines 33-35. In this manner, a plurality of spaced apart rectifying junctions are formed between film 3 and substrate 1, the junctions being separated by the electrically insulating material 2 in the respective recesses

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16. Col. 4, lines 35 – 39. A transparent, anti-reflection film 4, which is preferably an electrically conducting film, such as indium tin oxide, tin oxide, or tantalum pentoxide, is disposed on film 3. Col. 4, lines 39 – 42.

In Kawabata, the recesses 16 are not coupled to the light incident surface of the semiconductor film 3, but are rather in contact with the surface of the film 3 that is opposed to the light incident surface. In contrast, amended claim 1 recites that the "a plurality of shallow trench isolation surface features [are] located *on the light incident side* of the semiconductor layer." Moreover, while claim 1 recites that the optoelectronic device includes "a first bonding layer disposed between the semiconductor layer and the support substrate," Kawabata does not teach the use of a bonding layer between the substrate 1 and the semiconductor film 3. Rather, in Kawabata, the p-type semiconductor film 3 is deposited on the first surface 14 of the substrate 1, e.g., via chemical vapor deposition, after the recesses are formed in the substrate 1 and filled with an insulating material. See, e.g., col. 5, lines 5-37.

Thus, amended claim 1 and claim 2, 9-10, 12 and 14 are not anticipated by Kawabata.

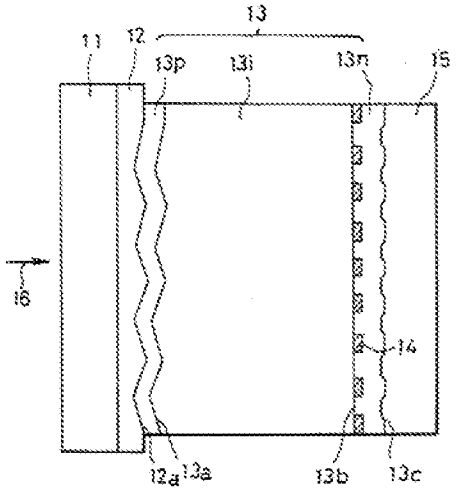
II. Claims 8 and 16 are rejected as being anticipated by U.S. Patent No. 5,370,747 of Noguchi.

Claim 8 depends on claim 1 and further recites that the plurality of shallow trench isolation surface features are formed in the semiconductor layer. Claim 16 is canceled without prejudice.

Noguchi discloses a photovoltaic device including a substrate, a first electrode layer provided on the substrate, a photoelectric conversion layer provided on the first electrode, and a second electrode layer provided on the photoelectric conversion layer. Abstract. With reference to FIG. 1 of Noguchi, reproduced below, the photovoltaic device 1 includes a transparent substrate 11 on which a front electrode 12 is provided. Col. 5, lines 17-20.

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FIG.1



A photoelectric conversion layer 13, which is mainly formed by an amorphous silicon film, is provided on the front electrode 12. Col. 5, lines 23-25. The photoelectric conversion layer 13 is formed by a p-type layer 13p which is provided on the front electrode 12, a photoactive layer 13i which is provided on the p-type conductive layer 13p, and an n-type conductive layer 13n which is provided on the photoactive layer 13i. Col. 5, lines 25-30. Each of the interface 12a between the front electrode 12 and the p-type layer 13p and the interface 13a between the p-type layer 13p and the photoactive layer 13i has a texture. Col. 5, lines 30-35. A discontinuous interfacial layer 14 is disposed at the interface 13b between the photoactive layer 13i and the n-type layer 13n. Col. 5, lines 40-42. Such interfacial layer 14 can be formed by a well-known method such as sputtering or atmospheric pressure CVD. Col. 5, lines 42-44. A back electrode 15 is provided on the n-type layer 13n. The back electrode 15 can be made of a metal such as aluminum or chromium. Col. 5, lines 46-47. The interface 13c defining the surface of the back electrode 15 is slightly textured such that the light 16 is reflected by its textured surface in various directions.

Noguchi does not anticipate claim 8 at least because it does not disclose a bonding layer disposed between a semiconductor layer and a support substrate as recited in claim 1.

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III. Claims 1, 9, 11-12, and 14-15 are rejected as being anticipated by US2014/0352779 of Smirnov in view of U.S. Patent No. 5,236,863 of Iranmanesh.

Smirnov is generally directed to a "nanostructured arrangement having a base and pyramidal features formed on the base." Abstract. FIG. 14H of Smirnov, to which the Examiner refers and which is reproduced below, is a solar cell having a silicon wafer 140h with a base region 141h of p-type conductivity, an ultra-shallow emitter layer 143b of n+-type or n-type having a nanostructured surface with nanoridges 24 covered by a thin TCO layer 171, a layer of intrinsic silicon 143c between the base region 141h and the emitter layer 143b, front metal contact 173 to the TCO layer, diffusion regions 162 of p+-type, a layer of silicon oxide 156 with openings to regions 162, and a metallization layer 157 as a rear contact. Col. 7, lines 20-29.

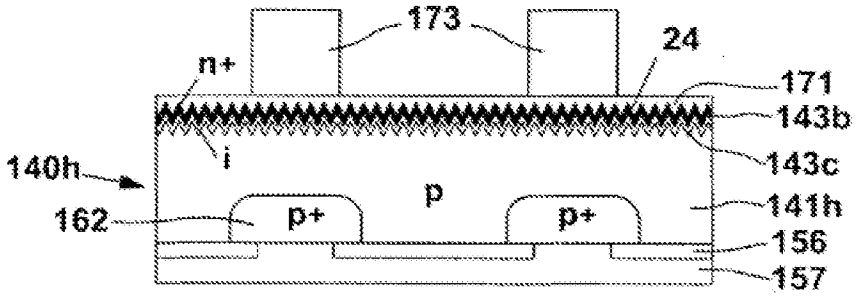


FIG. 14H

Smirnov does not, however, teach or suggest an optoelectronic device in which a bonding layer is disposed between a semiconductor layer and a support substrate as recited in claim 1.

Iranmanesh does not cure the shortcomings of Smirnov in this regard. Rather, Iranmanesh is generally directed to a process for forming an IC isolation trench pattern where the tranches have varying widths and are filled with near intrinsic single crystal silicon. Abstract.

Thus, claim 1 as well as claims 9, 11, 12 and 14, which depend on claim 1, are patentable over the cited art.

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Rejections Pursuant to 35 U.S.C. §103

I. Claims 11 and 13 are rejected as being unpatentable over Kawabata in view of U.S. Patent No. 7,828,983 to Weber.

Claim 11 depends, via intervening claim 9, on claim 1. Claim 9, as amended, recites that the shallow trench isolation surface features are arranged according to a pattern, and claim 11 recites that the pattern is a non-uniform arrangement. Claim 13 in turn depends on claim 1 and further recites that the shallow trench isolation surface features are not uniform in height.

As discussed in detail above, Kawabata fails to teach salient features of claim 1 and hence those of claims 11 and 13 that depend on claim 1. Weber does not teach these features either. Rather, Weber is simply directed to a process for texturing a surface of a semiconductor material. Abstract.

Thus, claims 11 and 13 are patentable over the cited art.

New Claims

New claims 21- 36 depend on claim 1 and hence are also patentable at least for the reasons provided in connection with claim 1.

CONCLUSION

The Examiner is invited to telephone the undersigned attorney for Applicant if such communication is deemed to expedite prosecution of this application.

The Director is authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 500436, under Docket No. 143705.01421.

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Respectfully submitted,

Dated: March 20, 2018

Electronic Signature: /Reza Mollaaghababa/

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SAMSUNG EX. 1002 - 80/1684

Electronic Patent Application Fee Transmittal

Application Number:	15614256
Filing Date:	05-Jun-2017
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Filer:	Reza Mollaaghababa/Irene Gommerstadt
Attorney Docket Number:	143705.06021

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

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Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1400	1400
Miscellaneous:				
			Total in USD ($)	**1400**

Electronic Acknowledgement Receipt

EFS ID:	32106301
Application Number:	15614256
International Application Number:	
Confirmation Number:	4345
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	136549
Filer:	Reza Mollaaghababa/Irene Gommerstadt
Filer Authorized By:	Reza Mollaaghababa
Attorney Docket Number:	143705.06021
Receipt Date:	20-MAR-2018
Filing Date:	05-JUN-2017
Time Stamp:	15:09:07
Application Type:	Utility under 35 USC 111(a)

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Multipart Description/PDF files in .zip description			
Document Description		**Start**	**End**
Amendment/Req. Reconsideration-After Non-Final Reject		1	1
Claims		2	5
Applicant Arguments/Remarks Made in an Amendment		6	12

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/614,256	Filing Date 06/05/2017	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	**280**
☒ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	**600**
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	**720**
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	**1600**

APPLICATION AS AMENDED – PART II

AMENDMENT **03/20/2018**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 30	Minus	** 20	= 10	X $100 =	1000
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $460 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**1000**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
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LIE
KATINA TOBIN

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/614,256	06/05/2017	Homayoon Haddad	143705.06021	4345

136549 7590 06/26/2018

Pepper Hamilton LLP/SiOnyx LLC
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Boston, MA 02110-2736

EXAMINER
EVERHART, CARIDAD

ART UNIT	PAPER NUMBER
2895	

NOTIFICATION DATE	DELIVERY MODE
06/26/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketingbn@pepperlaw.com
davisdr@pepperlaw.com

Office Action Summary	Application No. 15/614,256	Applicant(s) HADDAD ET AL.	
	Examiner CARIDAD EVERHART	Art Unit 2895	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/20/2018*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1,2,5,6,8-14,17,18 and 20-36* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,2,5,8-14,17,18 and 21-30, 33-36* is/are rejected.

8)☒ Claim(s) *6,20,31 and 32* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Response to Arguments

Applicant's arguments filed 3/20/2018 have been fully considered. Applicant's amendment has overcome the double patenting rejections, and therefore the double patenting rejections have been withdrawn. New grounds of rejection are applied to the claims.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-2, 5, 8-10, 12, 14, 17-18, 23, 28, and 33 is/are rejected under 35 U.S.C. 103 as being unpatentable over Dutta (US 2007/0204902 A1) in view of Kim et al (US 6,413,135 B1).

Dutta discloses a device including a semiconductor layer having a light incident side and an opposite side, as shown in Fig. 9C (para. 0063) the semiconductor layer having doped regions forming at least one junction, as Dutta discloses nanorods 1301 and electronic material 1302 form a pn junction (para. 0073 and Fig. 13E), the electronic material is disclosed to have p or n conduction (para. 0047), which satisfies the limitation the semiconductor layer having multpiple doped regions forming at least one junction

A textured region including a pluralitiy of trench isolation features on the light incident side configured to interact with incident electromagnetic radiation, as Dutta discloses nanorods 1301 which have trenches between them (Fig. 13D, which are the same as nanorods 1401 which are described in para. 0074) and isolation layer 1307 (Fig. 13E and para. 0073) in the trenches between the nanorods

A support substrate coupled to the semiconductor layer, as Dutta discloses the substrate may be for example, glass which is bonded to a silicon layer by anodic bonding (para. 0073), and Dutta also discloses an oxide bonding layer 940 between the glass substrate 930 and the silicon substrate 900 (para. 0061, 0062, and Fig. 9)

A first bonding layer between the semiconductor layer and the support substrate, as the anodic bonding forms an anodic bonding layer.

Dutta is silent with respect to a bonding layer, although Dutta discloses anodic bonding, which forms an anodic bonding layer.

Kim et al discloses that silicon forms an oxide as an anodic bonding layer (col. 4, lines 33-42).

Kim et al supports that an anodic bonding layer is formed by anodic bonding.

Re claim 2: Dutta discloses the semiconductor may be crystalline silicon, as Dutta discloses the substrate may be crystalline silicon (para. 0068) and that the nanorods may be formed of the same material by etching for example (para. 0061).

Re claim 5: Dutta discloses a second bonding layer between the first bonding layer and the substrate, as Dutta discloses a bonding layer from an anodic bonding step bonding the silicon layer 1300 and glass layer 1312 (Fig. 13B and 13C) and a second anodic bonding layer bonding the glass substrate 1330 and the silicon layer 1300(Fig. 13E).

Re claim 8: Dutta discloses shallow trench isolation features formed in the semiconductor layer, as Dutta discloses isolation trenches, as Dutta discloses textured region including a pluralitiy of trench isolation features on the light incident side configured to interact with incident electromagnetic radiation, as Dutta discloses nanorods 1301 which have trenches between them (Fig. 13D, which are the same as nanorods 1401 which are described in para. 0074) and isolation layer 1307 (Fig. 13E and para. 0073) in the trenches between the nanorods and that and that the nanorods may be formed of the same material by etching for example (para. 0061), which is a disclosure that the trenches are formed by etching.

Re claim 9: Dutta discloses the surface features arranged in a pattern (Fig. 4A and para. 0045).

Re claim 10: Dutta discloses the pattern in the form of a uniform grid (Fig. 3A).

Re claim 12: Dutta discloses the nanorods of uniform height (Fig. 4B).

Re claim 14: Dutta discloses a metal layer 1403b, which is a contact and corresponds to a device layer, on the side of the semiconductor layer opposed to the light (Fig. 14E and para. 0074).

Re claim 17: Dutta discloses a method of forming a device including A a step of bonding a support substrate to a semiconductor layer, as Dutta discloses the substrate may be for example, glass which is bonded to a silicon layer by anodic bonding (para. 0073) and forming a textured region including a pluralitiy of trench isolation features on the light incident side configured to interact with incident electromagnetic radiation, as Dutta discloses nanorods 1301 which have trenches between them (Fig. 13D, which are the same as nanorods 1401 which are described in para. 0074) and isolation layer 1307 (Fig. 13E and para. 0073) in the trenches between the nanorods.

Re claim 18: Dutta discloses isolation trenches, as Dutta discloses textured region including a pluralitiy of trench isolation features on the light incident side configured to interact with incident electromagnetic radiation, as Dutta discloses nanorods 1301 which have trenches between them (Fig. 13D, which are the same as nanorods 1401 which are described in para. 0074) and isolation layer 1307 (Fig. 13E and para. 0073) in the trenches between the nanorods and that and that the nanorods may be formed of

the same material by etching for example (para. 0061), which is a disclosure that the trenches are formed by etching.

Re claim 23: Dutta discloses oxide as the bonding layer, as stated above in the rejection of claim 1.

Re claim 28: Dutta discloses pyramids for the surface features (Fig. 2B).

Re claim 33: Dutta discloses the textured features amplify light incident to the device, which is a disclosure of enhancing absorption of electromagnetic radiation.

Claims 11 and 13 is/are rejected under 35 U.S.C. 103 as being unpatentable over Dutta in view of Kim et al as applied to claims 9 and 1 above, and further in view of Raymond et al (US 2010/0181014 A1).

Dutta in view of Kim et al discloses the limitations of claim 1 as stated above. Dutta in view of Kim et al is silent with respect to the shallow trench isolation features being in a non-uniform arrangement and non-uniform height.

Raymond et al disclose a photovoltaic (PV) device including absorption enhancement features (Abstract) which may be in the form of pyramids (Fig. 5) and which are disclosed in Fig. 5 (para. 0089 and 0089) to be in a non-uniform arrangement and a non-uniform height with respect to height and position of the pyramid structures.

It would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have combined in non-uniform arrangement of the enhancement features as disclosed by Raymond et al with the features disclosed by

Dutta in view of Kim et al in order to obtain optimization of the path length of the enhancement film as disclosed by Raymond et al (para. 0067).

Claims 21-22 is/are rejected under 35 U.S.C. 103 as being unpatentable over Dutta in view of Kim et al as applied to claim 1 above, and further in view of Pralle (US 2014/0138785 A1).

Dutta in view of Kim et al discloses the limitations of claim 1 as stated above. Dutta in view of Kim et al is silent with respect to deep trench isolation.

Pralle discloses light trapping in photovoltaic devices such as solar cells (para. 0003 and 0036). Pralle also discloses isolation in order to prevent cross-talk between elements (para. 0036, 0037, and 0041), and to provide light trapping (para. 0042).

It would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have combined the isolation disclosed by Pralle with the device disclosed by Dutta in view of Kim et al in order to obtain the benefits of preventing cross-talk and of providing light trapping disclosed by Pralle.

Re claim 22: The combination of Dutta in view of Kim et al and of Pralle discloses light trapping, as stated above in the rejection of claim 21.

Claims 24 and 27 is/are rejected under 35 U.S.C. 103 as being unpatentable over Dutta in view of Kim et al as applied to claim 1 above, and further in view of Dietrich et al (US 2002/0173119 A1) and of Fournel et al (US 2011/0201177 A1).

Dutta in view of Kim et al discloses the limitations of claim 1 as stated above. Dutta in view of Kim et al is silent with respect to the recited thickness range of the semiconductor layer.

Dietrich et al discloses that the smart cut method results in thickness of a silicon layer in the range of 1.0 microns (para. 0004), which is within the recited range, and therefore the recited range is obvious (MPEP 2144.05).

Fournel et al disclose that the smart cut method results in thickness of about 3 microns (para. 0007), which overlaps the recited range, and therefore the recited range is obvious (MPEP 2144.05).

It would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention that the semiconductor layer disclosed by Dutta et al in view of Kim et al would be in the range of a few microns in view of the disclosure made by Dietrich et al and by Fournel et al because Dutta discloses the semiconductor layer is formed by the smart cut method, as stated above in the rejection of claim 1.

Re claim 27: Dutta discloses in Fig. 15 that the shallow trenches 1570 which are between the features1501, 1502, are the about the same height as the features 1501, 1502, and therefore the shallow trenches are about 1.0 microns or about 3 microns, which are within the recited range, which renders the recited range obvious (MPEP 2144.05).

Claims 25-26 is/are rejected under 35 U.S.C. 103 as being unpatentable over Dutta in view of Kim et al as applied to claim 1 above, and further in view of Ben Mohamed et al (US 2012/0001293 A1).

Dutta in view of Kim et al discloses the limitations of claim 1 as stated above. Dutta discloses a bonding layer, as Dutta discloses anodic bonding, as stated above in the rejection of claim 1, however Dutta in view of Kim et al is silent with respect to the recited thickness range of the bonding layer.

Ben Mohamed et al discloses that in an anodic bonding of a semiconductor layer to a glass layer, the thickness of the SiO2 layer is in the range of 1 to 100 nm (para. 0020 and 0021), which overlaps the recited range, and therefore the recited range is obvious (MPEP 2144.05).

It would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have formed the bonding layer in the method disclosed by Dutta in view of Kim et al in the range disclosed by Ben Mohamed et al in order to obtain an anodic bond by the anodic bonding method as disclosed by Ben Mohamed (para. 0021).

Claim 29 is/are rejected under 35 U.S.C. 103 as being unpatentable over Dutta in view of Kim et al as applied to claim 1 above, and further in view of Kim et al (US 2009/0286347 A1)(Kim et al '347).

Dutta in view of Kim et al discloses the limitations of claim 1 as stated above. Dutta in view of Kim et al is silent with respect to a patterned mask, although Dutta discloses the trench features such as pyramids may be formed by patterning, photolithography and etching (para. 0052).

Kim et al '347 discloses forming pyramid structures in a solar cell in which a mask is patterned and photolithography and etching is used (para. 0063).

It would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have used a patterned mask as disclosed by Kim et al '347 in the method disclosed by Dutta in view of Kim et al because Kim et al '347 discloses that the method of using a patterned mask is conventional in the art (para. 0063).

Claim 34 is/are rejected under 35 U.S.C. 103 as being unpatentable over Dutta in view of Kim et al as applied to claim 1 above, and further in view of Niira et al (US 2012/0235268 A1)

Dutta in view of Kim et al discloses the limitations of claim 1 as stated above. Dutta in view of Kim et al is silent with respect to the recited wavelength increase in optical absorption range.

Niira et al disclose that silicon has sensitivity to light with wavelength 700 nm or more (para. 0011), which overlaps the recited range, therefore the recited range is obvious (MPEP 2144.05).

Niira supports that the range of wavelengths increase in optical absorption range by the textured surface disclosed by Dutta in view of Kim et al is obvious because Dutta discloses silicon nanostructures for the textured surface and Niira discloses a wavelength range which renders the recited range obvious.

Allowable Subject Matter

Claims 6, 20, 31, and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARIDAD EVERHART whose telephone number is (571)272-1892. The examiner can normally be reached on Monday through Fridays 7:30-4:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on 571-272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CARIDAD EVERHART/
Primary Examiner, Art Unit 2895

Notice of References Cited	Application/Control No. 15/614,256	Applicant(s)/Patent Under Reexamination HADDAD ET AL.	
	Examiner CARIDAD EVERHART	Art Unit 2895	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2009/0286347 A1	11-2009	Kim; Yun-Gi	H01L31/0236	438/72
*	B	US-2007/0204902 A1	09-2007	DUTTA; ACHYUT KUMAR	H01L31/0236	136/256
*	C	US-2012/0235268 A1	09-2012	Niira; Koichiro	H01L31/048	257/432
*	D	US-2012/0001293 A1	01-2012	Ben Mohamed; Nadia	H01L21/76254	257/506
*	E	US-2011/0201177 A1	08-2011	Fournel; Franck	H01L21/76254	438/458
*	F	US-6,413,135 B1	07-2002	Kim; Won-Joo	H01J9/185	156/273.7
*	G	US-2010/0181014 A1	07-2010	Raymond; Mark A.	G02B5/003	156/209
*	H	US-2014/0138785 A1	05-2014	Pralle; Martin U.	H01L27/14627	257/432
*	I	US-2002/0173119 A1	11-2002	Dietrich, Harry	H01L21/76256	438/455
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15614256	HADDAD ET AL.
	Examiner	Art Unit
	CARIDAD EVERHART	2895

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/02363, 0236, 02327, 028	9/14/2017	ce

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST attached	9/14/2017	ce
Reviewed parents	9/14/2017	ce
EAST attached	6/18/18; 6/19/18	ce

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
EAST	attached	9/14/2017	ce

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	65	(textured or nanostructure$1 or nanotexture$1 or (nano adj structure$1)) same (solar adj cell) same (adhesive or (bonding adj layer)) same substrate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 12:20
L2	669	(glass adj substrate) same ((si or silicon) adj (wafer or layer)) same adhesive	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 12:35
L4	31	2 and ((textured or nanostructure$1 or nanotexture$1 or (nano adj structure$1)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 12:36
L8	742	((textured or nanostructure$1 or nanotexture$1 or (nano adj structure$1)) same (solar adj cell)) and ((adhesive or (bonding adj layer)) same substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 12:53
L9	52	8 and (transparent adj adhesive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 12:54
L66	101	(light adj trap) near6 (isolation or insulation or dielectric or oxide or "sio.sub.2" or polymer$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 15:16

EAST Search History (Interference)

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15614256	HADDAD ET AL.
	Examiner	**Art Unit**
	CARIDAD EVERHART	2895

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/14/2017	06/20/2018							
	1	✓	✓							
	2	✓	✓							
	3	✓	-							
	4	✓	-							
	5	✓	✓							
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	8	✓	✓							
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	33		✓							
	34		✓							
	35		✓							
	36		✓							

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L25	9	(("20070204902") or ("20090127555") or ("6222117")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/18 09:40
L36	2	25 and incident	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 09:50
L37	2	36 and (bond or bonding or bonded)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 09:51
L38	27963	junction and (doped or implant$5) and bond$3 and (light same (detect$4 or sensing or sensed or sense or photodetector or (incident adj light)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 09:55
L40	1807	38 and ((insulation or isolation) same trench$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 09:55
L41	133	40 and (nanostructur$3 or concavities)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/18 09:56

EAST Search History (Interference)

<This search history is empty>

6/18/2018 10:05:25 AM

SAMSUNG EX. 1002 - 105/1684

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	15/614,256	Filing Date	2017-06-05	Docket Number (if applicable)	143705.06021	Art Unit	2895
First Named Inventor	Homayoon Haddad			Examiner Name	Caridad Everhart		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 500436

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

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Signature	/Andrew W. Schultz/	Date (YYYY-MM-DD)	2018-12-26
Name	Andrew W. Schultz	Registration Number	66869

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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SAMSUNG EX. 1002 - 108/1684

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Homayoon Haddad *et al.*	Confirmation No.: 4345
Application No.: 15/614,256	Art Unit: 2895
Filed: June 5, 2017	Examiner: Everhart, Caridad
For: SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Certificate of Mailing

I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

December 26, 2018 — Dated

Electronic Signature: /Andrew W. Schultz/
Andrew W. Schultz, Reg. No. 66,869

AMENDMENT AND RESPONSE TO FINAL OFFICE ACTION FILED WITH REQUEST FOR CONTINUED EXAMINATION

Dear Sir:

This paper is filed in response to the final Office Action dated June 26, 2018. A petition for a three-month extension of time and a Request for Continued Examination (RCE) is filed concurrently herewith.

Amendments to the Claims begin on page 2.

Remarks begin on page 8.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:

a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,

a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,

a support substrate coupled to said semiconductor layer[[;]], and

a first bonding layer disposed between the semiconductor layer and the support substrate, wherein said optoelectronic device is a photosensitive imager device capable of detecting visible and infrared electromagnetic radiation.

2. (Original) The device of claim 1, wherein the semiconductor layer is single crystal silicon.

3. (Canceled)

4. (Canceled)

5. (Previously Presented) The device of claim 1, further comprising a second bonding layer positioned between the first bonding layer and the support substrate.

6. (Original) The device of claim 5, further comprising a reflector layer disposed between the first bonding layer and the second bonding layer.

7. (Canceled)

8. (Previously Presented) The device of claim 1, wherein the shallow trench isolation surface features are formed in the semiconductor layer.

9. (Previously Presented) The device of claim 1, wherein the shallow trench isolation surface features are arranged according to a pattern.

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10. (Previously Presented) The device of claim 9, wherein the pattern is an at least substantially uniform grid.

11. (Previously Presented) The device of claim 9, wherein the pattern is a non-uniform arrangement.

12. (Previously Presented) The device of claim 1, wherein the shallow trench isolation surface features have a substantially uniform height.

13. (Previously Presented) The device of claim 1, wherein the shallow trench isolation surface features are not uniform in height.

14. (Previously Presented) The device of claim 1, further comprising a device layer coupled to the semiconductor layer on ~~a~~ said side opposed to the light incident side.

15. (Canceled)

16. (Canceled)

17. (Currently Amended) A method of making an optoelectronic device, comprising:

bonding a semiconductor layer to a support substrate, wherein bonding the semiconductor layer to the support substrate includes:

depositing a first bonding layer onto the semiconductor layer; and

bonding the first bonding layer to a second bonding layer disposed on the support substrate; and

creating a plurality of shallow trench isolation surface features on a light incident side of said semiconductor layer.

18. (Previously Presented) The method of claim 17, wherein the step of creating the plurality of shallow trench isolation surface features comprises generating an array of surface features using shallow trench isolation etching.

19. (Canceled)

20. (Canceled)

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21. (Previously Presented) The device of claim 1, further comprising deep trench isolation for isolating the device.

22. (Previously Presented) The device of claim 21, wherein said deep trench isolation provides light trapping functionality.

23. (Previously Presented) The device of claim 1, wherein said first bonding layer comprises any of silicon oxide, silicon nitride and amorphous silicon.

24. (Previously Presented) The device of claim 1, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.

25. (Previously Presented) The device of claim 1, wherein said bonding layer has a thickness in a range of about 30 nm to about 3 microns.

26. (Previously Presented) The device of claim 1, wherein said bonding layer has a thickness in a range of about 40 nm to about 2 microns.

27. (Previously Presented) The device of claim 1, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.

28. (Previously Presented) The device of claim 1, wherein said shallow trench isolation surface features comprise pyramids.

29. (Previously Presented) The device of claim 1, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.

30. (Previously Presented) The device of claim 1, wherein said plurality of shallow trench isolation surface features comprise multiple etched levels.

31. (Canceled)

32. (Canceled)

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33. (Previously Presented) The device of claim 1, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.

34. (Currently Amended) The device of claim 1, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to [[a]] about 1100 nm.

35. (Previously Presented) The device of claim 1, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.

36. (Previously Presented) The device of claim 1, wherein said textured region allows the semiconductor layer to experience multiple passes of light.

37. (New) An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:

a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,

a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,

a support substrate coupled to said semiconductor layer, and

a first bonding layer disposed between the semiconductor layer and the support substrate,

a second bonding layer positioned between the first bonding layer and the support substrate, and

a reflector layer disposed between the first bonding layer and the second bonding layer.

38. (New) The device of claim 37, wherein said shallow trench isolation surface features comprise pyramids.

39. (New) The device of claim 37, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.

40. (New) The device of claim 37, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.

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41. (New) The device of claim 37, further comprising deep trench isolation for isolating the device.

42. (New) The device of claim 41, wherein said deep trench isolation provides light trapping functionality.

43. (New) The device of claim 37, wherein the shallow trench isolation surface features are arranged according to a pattern.

44. (New) The device of claim 43, wherein the pattern is an at least substantially uniform grid.

45. (New) The device of claim 43, wherein the pattern is a non-uniform arrangement.

46. (New) The device of claim 37, wherein the shallow trench isolation surface features have a substantially uniform height.

47. (New) The device of claim 37, wherein the shallow trench isolation surface features are not uniform in height.

48. (New) The device of claim 37, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.

49. (New) The device of claim 37, wherein said photosensitive imager device is capable of detecting visible and infrared electromagnetic radiation.

50. (New) The device of claim 37, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.

51. (New) The device of claim 37, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.

52. (New) The device of claim 37, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.

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53. (New) The device of claim 37, wherein said textured region allows the semiconductor layer to experience multiple passes of light.

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REMARKS

The pending Office Action rejects claims 1, 2, 5, 8-14, 17, 18, 21-30 and 33-36 and objects to claims 6, 20, 31, and 32. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

Allowable Subject Matter

Applicant thanks Examiner Everhart for the indication that claims 6, 30, 31, and 32 would be allowable if rewritten in independent form. As discussed below, independent claims 1 and 17 are amended in accordance with the Examiner's indication of allowable subject matter.

Amendments to the Claims

Applicant presents the following claim amendments solely to expedite prosecution. These amendments should not be construed as Applicant's acceptance of the Examiner's rejection. Applicant reserves the right to prosecute any of the former claims in a continuing application.

As shown on the attached sheets, independent claim 1 is amended to incorporate the recitations of allowable claims 31 and 32, which are hereby canceled. Independent claim 17 is amended to incorporate the subject matter of allowable claim 20 (which is also canceled). In addition, claim 34 is amended to correct a typographical error. No new matter is added.

Rejections Pursuant to 35 U.S.C. § 103

The Office Action rejects claims 1, 2, 5, 8-10, 12, 14, 17, 18, 23, 28, and 33 as being obvious over U.S. Pub. No. 20070204902 of Dutta ("Dutta") in view of U.S. Pat. No. 6,413,135 of Kim *et al.* ("Kim"). Claims 11 and 13 are rejected as being obvious over Dutta and Kim and further in view of U.S. Pub. No. 20100181014 of Raymond *et al.* ("Raymond"). Claims 21 and 22 are rejected as being obvious over Dutta and Kim and further in view of U.S. Pub. No. 20140138785 of Pralle *et al.* ("Pralle"). Claims 24 and 27 are rejected as being obvious over Dutta and Kim and further in view of U.S. Pub. No. 20020173119 of Dietrich *et al.* ("Dietrich") and U.S. Pub. No. 20110201177 of Fournel *et al.* ("Fournel"). Claims 25 and 26 are rejected as being obvious over Dutta and Kim and further in view of U.S. Pub. No. 20120001293 of Ben Mohamed *et al.* ("Mohamed"). Claim 29 is rejected as being obvious over Dutta and Kim and further in view of U.S. Pub. No. 20090286347 of Kim *et al.* ("Kim '347"). Finally, claim 34 is

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rejected as being obvious over Dutta and Kim and further in view of U.S. Pub. No. 20120235268 of Niira *et al.* ("Niira").

As noted above, independent claim 1 is amended to incorporate the recitations of allowable claims 31 and 32, while claim 17 is amended to incorporate the recitations of allowable claim 20. In light of the Examiner's indication of allowable subject matter, Applicant respectfully submits that independent claim 1 (and its dependent claims 2, 5, 6, 8-14, 21-30, and 33-36) and independent claim 17 (and its dependent claim 18) are allowable.

New Claims

Claims 37-53 are newly presented. Applicant notes that new independent claim 37 represents the version of previous claim 1, amended to incorporate the recitations of allowable claim 6. Claims 38-53 represent the recitations of previous claims 28, 29, 24, 21, 22, 9-13, 27, 31, and 33-36. Support can be found throughout the application as filed and in the original claims. No new matter is added. Applicant respectfully submits that claims 37-53 are allowable in light of the Examiner's indication of allowable subject matter in previous claim 6.

Conclusion

Applicant believes that the claims are in proper condition for allowance and allowance thereof is respectfully requested. The Examiner is encouraged to telephone the undersigned attorney for Applicant if such communication is deemed to expedite prosecution of this application. The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0436, under Attorney Docket No. 143705.06021.

Dated: December 26, 2018

Respectfully submitted,
Electronic Signature: /Andrew W. Schultz/
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SAMSUNG EX. 1002 - 117/1684

Electronic Patent Application Fee Transmittal

Application Number:	15614256
Filing Date:	05-Jun-2017
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Filer:	Andrew W. Schultz
Attorney Docket Number:	143705.06021

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	14	100	1400
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Extension - 3 months with $0 paid	1253	1	1400	1400
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**4100**

Electronic Acknowledgement Receipt

EFS ID:	34692864
Application Number:	15614256
International Application Number:	
Confirmation Number:	4345
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	136549
Filer:	Andrew W. Schultz
Filer Authorized By:	
Attorney Docket Number:	143705.06021
Receipt Date:	26-DEC-2018
Filing Date:	05-JUN-2017
Time Stamp:	18:46:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$4100
RAM confirmation Number	122718INTEFSW18470900
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	RCE.pdf	1349940 07f0529b60622ac80a1676492bbbc07436c66b7c	no	3
Warnings:					
Information:					
2		Response20181226.pdf	123041 d60d4e12182002ed6b524a7e80176b8aadad2ff4	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment Submitted/Entered with Filing of CPA/RCE	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	9

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	33962 1b0a7bbbc106229c299e0be7bd039495459631e6	no	2
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New International Application Filed with the USPTO as a Receiving Office

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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/614,256	Filing Date 06/05/2017	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	12/26/2018	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 44	Minus	** 30	= 14	X $100 =	1400
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**1400**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
ANITA JOHNSON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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Espacenet

Bibliographic data: CN101053065 (A) — 2007-10-10

To processing laser doping with line focus laser beam to solid and to manufacture solar energy battery emitter electrode based on the said method

Inventor(s): AINHWA WERNER JURGEN H COLOR J [DE] ± (WERNER JURGEN H.,COLOR JURGEN,ESTURO-BRETTON AINHWA)

Applicant(s): WERNER JURGEN H [DE] ± (WERNER JURGEN H)

Classification: - international: ***H01L21/223; H01L21/225; H01L21/268; H01L31/18***

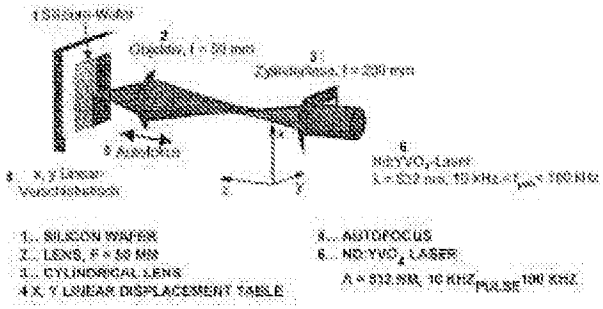
- cooperative: **B23K26/0738**; **H01L21/2254**; **H01L21/2255**; **H01L21/2256**; **H01L21/268**; **H01L31/1804**; Y02E10/547; Y02P70/521

Application number: CN2005828813 20050721

Priority number (s): DE20041036220 20040726

Also published as: AT408895 (T) DE102004036220 (A1) DE102004036220 (B4) EP1738402 (A1) EP1738402 (B1) more

Abstract not available for CN101053065 (A)
Abstract of corresponding document: WO2006012840 (A1)



The invention relates to a laser doping method, according to which a medium containing a doping substance is first brought into contact with a surface of the solid body. One region of the solid body lying below the surface that has been brought into contact with the medium is then melted for a short time by irradiation with laser pulses, allowing the doping substance to diffuse into the melted region and the latter to crystallise during the cooling process. The laser beam is focussed on the solid body in a linear manner, the width of said linear focus being preferably less than 10 µm.

SAMSUNG EX. 1002 - 124/1684

[19] 中华人民共和国国家知识产权局

[51] Int. Cl.
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H01L 31/18 (2006.01)

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[21] 申请号 200580028813.0

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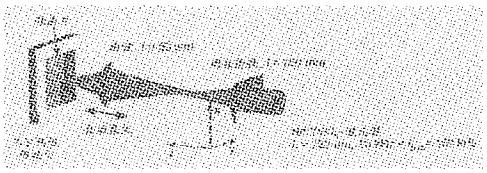
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权利要求书 3 页 说明书 7 页 附图 3 页

[54] 发明名称

用线性聚焦的激光束对固体进行激光掺杂以及基于所述方法制造太阳能电池发射极

[57] 摘要

在一种根据本发明的激光掺杂方法中，首先使包含掺杂物的介质与固体的表面形成接触。然后，通过激光脉冲的照射短时融化固体的在与介质接触的表面下的区域，使得掺杂物扩散进熔化的区域中并且在熔化区域冷却期间使熔融区域结晶。激光束以线性焦点聚焦在固体上，其中线性焦点的宽度优选小于 10μm。



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1. 一种在固体中产生掺杂的区域的方法，其中

将包含掺杂物的介质与所述固体的表面形成接触，

通过激光脉冲照射使所述固体的在与所述介质接触的表面下的区域融化，使得所述掺杂物扩散进所述熔化的区域中，并且在所述熔化的区域冷却期间再结晶，

其特征在于，所述激光束以线性焦点聚焦到所述固体上。

2. 根据权利要求 1 所述的方法，其特征在于，所述线性焦点的宽度小于 10μm。

3. 根据权利要求 1 所述的方法，其特征在于，所述线性焦点的长度在 100μm 至 10mm 的范围内。

4. 根据上述权利要求中任一项所述的方法，其特征在于，所述激光的波长这样选择，使得所述激光辐射在所述固体中的吸收长度与预定的长度、特别是 1μm 相应。

5. 根据权利要求 4 所述的方法，其特征在于，所述固体为硅并且所述激光辐射的波长小于 600nm。

6. 根据上述权利要求中任一项所述的方法，其特征在于，所述脉冲宽度这样地选择，使得所述掺杂物原子在所述熔化的固体中的热扩散长度与预定的长度、特别是 1μm 相应。

7. 根据权利要求 6 所述的方法，其特征在于，所述固体为硅并且所述脉冲宽度小于 100ns，特别是小于 50ns。

8. 根据上述权利要求中任一项所述的方法，其特征在于，辐射束扫过所述表面，其方式是在所述固体与所述辐射束之间产生相对运动。

9. 根据上述权利要求中任一项所述的方法，其特征在于，所述液体或固体涂层形式的介质通过旋涂方法或者丝网印刷或者薄膜印刷方法施加到所述表面上。

10. 根据上述权利要求中任一项或者根据权利要求 1 的前序部分所述的方法，其特征在于，所述介质以固体涂层（6）形式通过溅射方法来施加。

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11. 根据权利要求 10 所述的方法，其特征在于，

首先将所述介质施加到起始衬底（1）上，

在第一溅射步骤中被从所述起始衬底（1）进行溅射，并且沉积到中间目标（3）上，以及

在第二溅射步骤中从所述中间目标（3）被溅射并且沉积到所述待掺杂的固体（5）上。

12. 根据权利要求 11 所述的方法，其特征在于，所述中间目标（3）为硅衬底。

13. 根据权利要求 11 或者 12 所述的方法，其特征在于，所述介质由所述掺杂物构成并且粉末状地被施加到所述起始衬底（1）上。

14. 根据上述权利要求中任一项或者权利要求 1 的前序部分所述的方法，其特征在于，所述固体包含主体（10）和施加在所述主体（10）的表面上的中间层（11），并且所述介质被施加在所述中间层（11）上。

15. 根据权利要求 14 所述的方法，其特征在于，所述中间层（11）为钝化层。

16. 根据权利要求 14 或者 15 所述的方法，其特征在于，所述中间层（11）作为对所述激光辐射的抗反射层。

17. 根据上述权利要求 14 至 16 中任一项所述的方法，其特征在于，所述中间层（11）包含氮化硅、二氧化硅或者无定形硅或者由这些材料中的其中一种构造。

18. 一种通过根据上述权利要求中任一项所述的用于在半导体中产生掺杂的区域的方法来制造太阳能电池的发射极区域的方法。

19. 一种在半导体和金属之间产生欧姆接触的方法，在该方法中按照权利要求 1 至 17 中任一项所述地在半导体中产生掺杂的区域并且随后将金属层施加到所述掺杂的区域上。

20. 一种用于实施根据上述权利要求中任一项所述的方法的装置，所述装置包括

脉冲激光束源，

用于产生线性焦点的圆柱透镜，

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用于使所述线性焦点缩小地成像到所述固体的表面上的物镜。

21. 根据权利要求 20 所述的装置，其特征在于自动聚焦装置，其测量所述固体表面距参考点的间距并且这样地调整物镜与固体表面之间的间距，使得在所述固态表面上维持焦点位置在焦深内。

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用线性聚焦的激光束对固体进行激光掺杂以及基于所述方法制造太阳能电池发射极

本发明涉及一种根据权利要求 1 的前序部分所述的用于在固体中产生掺杂区域的方法，本发明也涉及一种用于实施该方法的装置。此外，本发明还涉及一种基于根据本发明的方法的、用于制造太阳能电池的发射极区域的方法。另外，本发明还涉及一种基于根据本发明的方法的、在半导体和金属之间产生欧姆接触的方法。

在由单晶硅或者多晶硅构成的太阳能电池的商业制造中，通过制造中的高温步骤来产生太阳能电池发射极，接着在温度为大约 1000K 的扩散炉中扩散掺杂物、一般为磷。为此所需的时间大约为 30 分钟。因此，传统的通过在扩散炉中扩散来制造太阳能电池发射极是耗能且耗时的。

此外，由于在传统的扩散工艺中发射极扩散的工艺时间冗长，所以在制造系统中仅能分批地实施制造。然而，低成本制造太阳能电池要求工艺中简单且快速的各个步骤，这些步骤可以集成为一个连续的、即在线（inline）制造工艺。通过在扩散炉中扩散来制造太阳能电池反射器不能满足这些要求。

在 US 5,918,140 中公开了一种用于激光掺杂半导体的方法，其中首先将包含掺杂物的材料的薄层施加到半导体表面上，接着将半导体表面暴露于脉冲激光辐射，其中在半导体表面和施加的掺杂物层之间的接触面的区域中，激光脉冲的能量被吸收并且转换成热能。这导致半导体的上部区域融化并且因此导致在融化期间掺杂物原子扩散到半导体的熔化区域中。在激光脉冲的下降时间中和在此之后，半导体的熔融区域再结晶，因此掺杂物原子混进晶格中。通过这种方式原理上可能在固体中产生高掺杂浓度的靠近表面的掺杂区域。然而，至今还不能对半导体例如硅实施激光掺杂，使得在融化的表面层中能够使硅再结晶大约 1μm 或者更小的厚度而没有缺陷。在测试中，使用市面上可得到的激光处理系统在硅中产生掺杂区域，这些区域随后作为太阳能电池发射极使用。结果是，太阳能电池发射极的质量非常差，特别是太阳能电池的空载电压和效率是非常低的。此外，TEM 分析显示太阳能电池发射极特别受到高位错密度而损坏。

因此，本发明的目的是，说明借助激光掺杂在固体中产生掺杂区域的

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方法，通过这些方法可以在掺杂的区域中得到固体的高度无缺陷性，或者借助这些方法，传统的方法可以以其它方式在提供掺杂物层、实现高掺杂浓度或者激光束功率的耦合输入的效率方面得以改善。

通过权利要求 1 和其它独立权利要求所述的特征来实现该目的。另一些有利的实施例和方面是从属权利要求的主题。同样说明了一种借助根据本发明的方法产生太阳能电池的发射极区域的方法。也说明了一种借助根据本发明的方法在半导体和金属之间产生欧姆接触的方法。此外，还说明了一种用于实施根据本发明的方法的装置。

在根据本发明的用于在固体中产生掺杂区域的方法中，首先将包含掺杂物的介质与固体的表面形成接触。然后，借助激光脉冲照射，使固体的与介质所接触的表面下的区域融化，使得掺杂物扩散进熔融的区域中并且在熔融区域冷却期间再结晶。

根据本发明的方法的重要方面是，激光束线性地聚焦在固体上，优选的是，选择线性焦点的宽度小于 10μm。例如，焦点宽度可以在 5μm 到 10μm 范围内。然而，焦点宽度甚至也可为大约 5μm 或者更小。

同时测试证实，通过为激光掺杂方法提供线性焦点可以产生再结晶的具有高无缺陷性的掺杂区域。这通过根据本发明的方法来实现，而不需要高温过程和冗长的工艺时间。相反，根据本发明的方法是一种产生高结晶度和无缺陷的掺杂区域的掺杂固体的低温方法。

因此，根据本发明的方法使得能够替代半导体晶片在高温炉中的成批处理（batch=Betrieb），而用后勤上更有效的在线过程来替换，并且直接集成到电子部件（例如太阳能电池）的生产线中。

在所实施的测试中，激光束形成 5μm 宽且数百微米长的线，线性焦点的长度一般优选在 100μm 至 10mm 的范围内。

在根据本发明的方法中，待掺杂的区域的深度的范围可通过合适地选择激光波长来确定。这通过选择这样的波长来完成，使得激光辐射在固体中的吸收长度或者穿透深度与待掺杂区域中所希望的深度范围相应。对于太阳能电池发射极，通常选择该深度为 1μm 或者更小。当固体是半导体硅时，激光辐射的波长应为 600nm 或者更小。

此外，当希望待掺杂区域为确定的深度时，脉冲宽度应这样选择，使得掺杂物原子在熔融固体中的热扩散长度为所希望的深度范围的量级。当

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固体为半导体硅并且所希望的深度范围为1μm时，脉冲宽度应低于100ns，特别是低于50ns。

通常，应掺杂其横向伸展至少在一个方向上大于激光焦点的区域，使得辐射束必须被扫描经过固体。在固体与辐射束之间产生垂直于线性焦点的线而对准的相对运动。优选地，固体安装在X-Y线性移动台上并且激光束保持不动。然而，也可以设置固体保持不动而配置激光束的光学系统，使激光束在固体上扫描。

包含掺杂物的介质可以以液体或者固体涂层的形式通过旋涂或者通过丝网印刷或者薄膜印刷方法被施加到界面上。然而，还可能的是，介质是气态的，并且与固体的表面直接接触。

另一种根据本发明的方法的重要方面是，通过溅射方法将固体涂层形式的、包含掺杂物的介质施加到固体上，其中在稍后的融化中不必将激光束成形为线性焦点。在此可以设置，首先将该介质施加到起始衬底上，接着在第一溅射方法步骤中被从起始衬底溅射并沉积到中间目标上，最后在第二溅射方法步骤中从中间目标被溅射并且沉积到待掺杂的固体上。

在该设置中，类似中间目标，起始衬底可以总是包括硅衬底，如硅晶片。该介质可以基本上或者完全由掺杂物本身构成，并且例如粉末状沉积在起始衬底上。因此，特别是通常提供的掺杂物元素，例如磷、砷、锑、硼、铝、镓、铟、钽或者钛，首先可以粉末状地沉积在硅晶片上，接着这些元素可以从硅晶片溅射到中间目标上。最后，从中间目标沉积到待掺杂的固体的层因此可以超过90%由掺杂物构成，因为在第一溅射步骤中在溅射时仅仅少量衬底硅被一同溅射。因此，在这种方法中，在待掺杂的固体上仅仅需要很薄的、例如仅仅几纳米厚度的掺杂物层，以在固体中产生很高的掺杂物浓度，例如达到$10^{22}/cm^3$。

应理解的是，本申请上下文中的待掺杂的固体可以为待掺杂的半导体本身，但是也应理解的是，固体包含主体，该主体是实际待掺杂的半导体本体，还包含沉积到主体的表面上的中间层，其中按照根据本发明的另一种方法，介质沉积在中间层上。在该设置中，并非强制地要求在后来激光束掺杂中激光束被线性聚焦。当作为对激光辐射的抗反射层起作用的中间层被施加到半导体本体上时，例如则给出这种实施形式。抗反射层使得激光辐射的全部光功率都被利用，并且用于融化位于中间层下的半导体材料的表面区域。然后，掺杂物可以在融化期间通过中间层扩散进半导体本体

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中。尽管有中间层，在半导体本体中仍能以这样的方式产生高掺杂物浓度，因为特别是通过前述的溅射方法事先在中间层上产生很高的掺杂物浓度。由于高掺杂物梯度，掺杂物也以高速扩散通过中间层。

中间层可以替代地或附加地构造成用于使半导体本体的表面钝化的钝化层。

特别是，中间层也可以包含氮化硅，二氧化硅或者无定形硅或者由这些材料其中之一构造。

中间层可以通过溅射方法来产生。特别是当掺杂物层通过溅射方法来产生时，可以在同一个的溅射装置中产生掺杂物层和中间层。

根据本发明的方法可以特别是用于制造太阳能电池的发射极区域，其中通过根据本发明的方法掺杂半导体表面的、用作太阳能电池发射极的区域。

此外，根据本发明的方法也可以用于在半导体和金属之间制造欧姆接触，其中在半导体中，根据本发明的方法生成被掺杂的区域，接着金属层被施加到该掺杂的区域上。通过这种方式，在 p 型晶片和 n 型晶片上都能够产生很低的接触电阻的欧姆接触。在该申请中所描述的方法此外也允许产生点接触或者带接触。

本发明也涉及一种用于实施根据本发明的方法的装置，该装置包括脉冲激光束源、用于产生线性焦点的圆柱透镜和用于将线性焦点缩小地成像到固体的表面上的物镜。

该装置优选具有自动聚焦装置，该自动聚焦装置测量固体表面距参考点的间距并且调整物镜与固体表面之间的间距，使得焦点位置维持在固体表面上的焦深之内。通过这种方式，即使表面弯曲或者粗糙也可以使焦点位置保持在晶片表面上的焦深之内。

参照附图将详述根据本发明的方法的实施例和用于实施根据本发明的方法的装置。其中：

图 1 是用于实施根据本发明的方法的装置的实施例的图示；

图 2a，b 是通过使用两步的溅射方法实施根据本发明的方法的实施例的图示；

图 3 是具有在半导体本体上的附加的抗反射层的、用于实施根据本发

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明的方法的实施例的图示。

在图 1 所示的装置中，作为激光束源在这种情况下使用了调 Q Nd:YVO_4 激光器，其通过使频率加倍而发射具有波长为 $\lambda = 532nm$ 的激光辐射。脉冲频率典型地在 10kHz 至 100kHz 范围内。当激光掺杂硅时，最佳脉冲能量密度在 2 至 6J/cm^{-2} 的范围内。

然后，（必要时在扩宽之后）通过圆柱透镜引导激光束以产生线性焦点。在该情况中，圆柱透镜具有 f = 200mm 的焦距。

最后，通过物镜将激光束成像在硅晶片上，在该实施例中该物镜具有 f = 50mm 的焦距。物镜将线性焦点缩小地成像在硅晶片上。在此，必需保证，甚至在表面弯曲或者粗糙的情况下，在晶片表面上焦点位置也总是维持在成像光学系统的焦深内。这可以通过自动聚焦装置来实现，该聚焦装置在工艺期间不断地测量晶片表面距参考点的间距并且修正物镜与硅晶片之间的间距。在所示的实施例中，物镜的位置通过使它在激光束的中心线上移动来修正，同样也可设置硅晶片的位置在激光束的中心线上移动来修正。

硅晶片安装在 X-Y 线性移动台上，X-Y 平面垂直于激光束。通过使硅晶片相对于碰撞的辐射束移动，可以在硅晶片上扫描更大的区域。

在制造太阳能电池发射极的测试中，借助旋涂器通过旋涂方法将市面上可得到的含磷的掺杂物液体施加到硅晶片上。通过一个或者多个激光脉冲来实施掺杂，其中晶片表面直到 1μm 或者更小的深度被迅速熔化并且磷原子从掺杂物液体进入液态硅中。在熔融物冷却和固化之后完成高掺杂的 n 型发射极区域。

n 型 Si 晶片上的硼掺杂的 p+型发射极也已通过根据本发明的方法处理过。

在确定对表面的每个区域需要多少个激光脉冲以达到令人满意的掺杂程度之后，优选连续地以预定的速度引导辐射束经过晶片表面。从该数量和脉冲频率可以确定扫描速度。优选地，扫描速度在 0.1 至 0.5m/s 的范围内。然而，作为上面的替换方案，也可以设置，以基本上与焦点宽度相应的离散步来移动移动台。在每个到达的点，硅晶片被固定地施加以预先给定数量的激光脉冲，并且随后线性焦点没有施加以激光脉冲地垂直于线的取向而移向下一个点。

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当使用 30W 激光系统时可以达到大约 10cm²/s 的产量。

现在参照图 2a、b，图示了根据本发明的方法的一种变形方案，其中以固体涂层的形式通过两步的溅射方法将介质施加到待掺杂的固体上。首先，掺杂物 2（例如纯磷）以粉末形式施加到作为起始衬底的硅晶片 1 上。然后，在图 2a 中在第一溅射步骤中，溅射粉末状的掺杂物 2 并且施加到同样通过硅晶片形成的中间目标 3 上并且作为掺杂物层 4 沉积在该中间目标 3 上。由此首先实现了，提供了相连接的掺杂物层 4，其例如可以具有超过 90％的掺杂物浓度。除掺杂物（例如磷）本身外，掺杂物层也可以含有硅，硅是在第一溅射步骤中从硅晶片 1 中被附加地去除的。

在如图 2b 中所示的第二溅射步骤中，掺杂物层 4 随后被溅射并且例如以第二掺杂物层 6 的形式沉积在实际要掺杂的固体 5 上。与掺杂物层 4 比较，该掺杂物层 6 的特征是其材料成分的更好的均匀性，使得在随后的激光束掺杂中在固体 5 中可以实现非常均匀的掺杂物分布。掺杂物层 6 可以为仅仅数 nm、例如 1-10nm 的厚度。

之后，激光束聚焦在具有沉积的掺杂物层的固体材料 5 上并且例如在表面区域短暂地熔化，只是不必一定使用线性焦点。然后，掺杂层 6 的掺杂物扩散进固体 5 的熔融的接近表面的区域并且在再结晶时合并进固体的晶格结构中。

现在，参照图 3 示出了根据本发明的方法的另一变形方案，其中在半导体本体 10 的待掺杂的区域上方，抗反射层 11 施加在半导体本体、例如硅晶片 10 上。抗反射层 11 这样构造，使得对于后来用于熔化的激光辐射具有尽可能低的反射系数，以致于其光功率几乎完全耦合输入到半导体本体 10 中。

然后，含有掺杂物的介质 12 施加到抗反射层 11 上。该介质本身可以例如由掺杂物构成，并且通过溅射方法施加到抗反射层 11 上。如上所述，特别是使用两步的溅射方法，掺杂物元素例如磷等可以以高浓度施加到抗反射层 11 上。同样可以通过溅射方法、优选地是在同一溅射室中产生抗反射层 11。

然后，激光束聚焦到半导体本体 10 上并且在表面区域短暂地用于融化，对此并非必须使用线性焦点。接着，掺杂物通过抗反射层 11 扩散进半导体本体 10 的熔融的靠近表面的区域并且在再结晶时混进半导体本体的晶格结构中。

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对于特别有效的太阳能电池，还公开了多级发射极，根据迄今公知的方法，多级发射极此外需要进一步的高温处理以及光刻结构化方法。通过根据本发明的方法利用具有比较高的脉冲频率的激光，可以额外地并且同时地实现掺杂物浓度的横向结构化，以产生多级发射极。

借助根据本发明的方法也可以附加地（或者例如单独地）产生所谓的“背面场（back surface field）”，其减小了背面少数载流子的复合。该工艺如上所述，其中含硼的掺杂物糊剂被施加到 p 型晶片的背面并且接着用激光处理表面。

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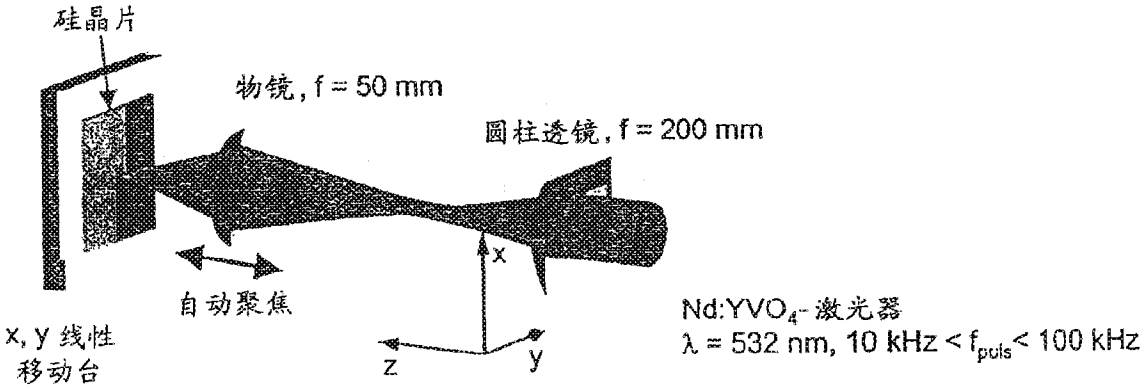


图1

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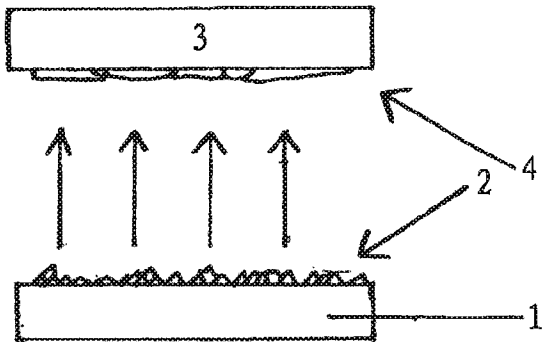


图2a

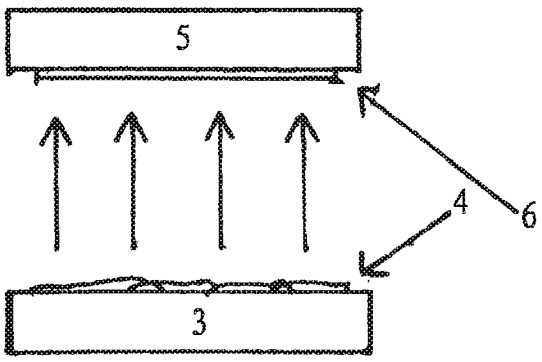


图2b

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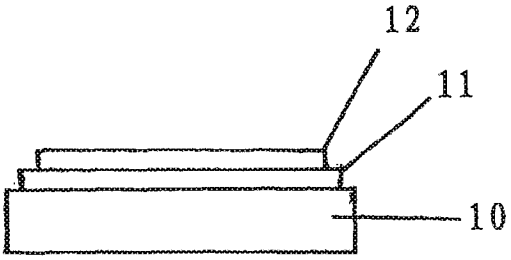


图3

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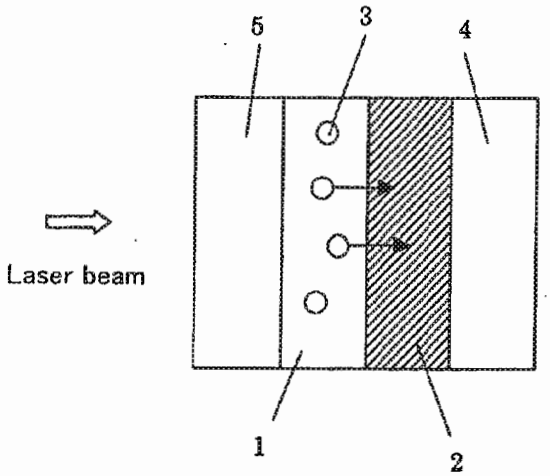
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(54) MATERIAL FOR ORGANIC ELECTROLUMINESCENCE DEVICE AND ITS MANUFACTURING METHOD

(57) A process for producing for a material for an organic electroluminescent device having an emission center comprises irradiating a laser beam to implant an emission center-forming compound 3 constituting a source 1 into a target 2 having at least one function selected from an electron-transporting function and a hole-transporting function. According to the process, the laser beam and at least the target are relatively moved with irradiating the beam to form the emission center with a predetermined pattern. Moreover, the source and the target being in contact with each other may be moved relative to the laser beam for forming the emission center with a predetermined pattern. Further, the emission center at an area, corresponding to an interference pattern of an interference light, of the target may be formed by irradiating the interference light of the laser beam.

Fig. 1



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Description

TECHNICAL FIELD

[0001] The present invention relates to a process for producing a material for an organic electroluminescent device by implanting or injecting an emission center-forming compound by molecular implantation with laser, a material for an organic electroluminescent device obtained by this process, and to an organic electroluminescent device (elements) produced with this organic electroluminescent device material.

BACKGROUND ART

[0002] Electroluminescent devices (hereinafter, occasionally referred to simply as EL devices) have generally been classified as inorganic EL devices or organic EL devices according to the materials they are made from. Some inorganic EL devices utilizing inorganic fluorescent molecules are in practical use partly, and have been brought into application to the backlight of clocks or the like. Meanwhile, organic EL devices have been desired to be brought into practical use because of their being more excellent in high brightness or luminance, high efficiency, and high-speed response than inorganic ones.

[0003] Electroluminescent devices are constituted of a compound or compounds having an electron-transporting function, a hole-transporting function, and an emission center-forming function. As for their structures, there have been reported devices of the single-layer mode having a single layer provided with all the functions mentioned above, and those of the multilayer-mode composed of layers each having different functions. The principle of light emission is considered to be based on the phenomenon that electrons or holes injected from a pair of electrodes recombine within a light-emitting layer to form excitons, exciting the molecules of a light emissive material for the light-emitting layer.

[0004] As a compound constituting each layer, a low-molecular weight compound of high light-emission efficiency, a macromolecular compound having a high physical strength, or the like is employed. When a low-molecular weight compound is used, a film is formed by means of a vapor deposition technique, while a macromolecular compound is formed into a film by coating or applying a solution in many cases.

[0005] Japanese Patent Application Laid-Open No. 96959/1996 (JP-A-8-96959) and Japanese Patent Application Laid-Open No. 63770/1997 (JP-A-9-63770) disclose organic EL devices comprising a single light-emitting layer made of a polymer binder having both electron-transporting function and hole-transporting function, within which varieties of fluorescent dyes (or colorants, pigments) are dispersed. These organic EL devises are reported to present, as a whole, white light due to the light emission of each light-emitting compound independent of one another. Moreover, as compared with organic EL devices of the multilayer-mode, those of the single-layer mode are hardly deteriorated in light-emission intensity.

[0006] Fine patterning, particularly multicolor patterning (full-coloration) of these organic EL devices is difficult because, in their fabrication, a film is formed by means of a solution coating technique in which a solution of a polymer binder and a fluorescent dye(s) dispersed in a specific solvent is applied onto a substrate.

[0007] As multicolor patterning methods, a color filter method, a color-converting method, the ink-jet method by T. R.Hebner (Appl. Phys. Lett. 72, 5 (1998), p.519), the photobleaching method by Kido, et al, and others have been reported.

[0008] The color filter method or color-converting method has the advantage of not requiring the patterning of a light-emitting layer, but suffers deterioration in conversion efficiency caused by the use of a filter. In the ink-jet method, since a pattern formed by ink-jet printing shows a center-raised, i.e., conical profile and is inferior in smoothness of its surface, it is difficult to provide electrodes thereon uniformly. Moreover, the cross section of the pattern is desired to be rectangular, but that of a pattern by ink-jet printing is circular. Further, the dimensions of a pattern largely depend on conditions under which the pattern is dried and the concentration of the solution. In the photobleaching method, only a special emission center-forming compound which loses its fluorescence upon UV oxidation is employable and therefore colors expressible by EL devices are limited.

[0009] As was described above, in conventional film-forming methods by solution coating, although it is possible to use a macromolecular compound with a high physical strength, it is difficult to provide fine patterns. In addition to that, also in the above-described patterning methods, compounds that can be used are limited, and films having surface smoothness suitable for organic EL devices cannot be obtained.

[0010] As the molecular implantation technique, Japanese Patent Application Laid-Open No. 297457/1994 (JP-A-6-297457) discloses a method comprising a step of, with a functional material or a solid material containing a functional material (A) and a solid material into which a functional component is to be implanted (B) placed such as to face each other, irradiating a laser pulse thereby to implant the functional component into the solid material (B). The literature describes that a position to be implanted of the functional component can be controlled by adjusting an irradiation position of the laser.

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[0011] Japanese Patent Application Laid-Open No. 106006/1996 (JP-A-8-106006) discloses a method comprising the steps of bringing a source film of an organic macromolecular compound within which dyes absorptive of a pulse laser are dispersed into tight contact with a target film of an organic macromolecular compound transmittable of a pulse laser, and irradiating a pulse laser from the target film side with an intensity of or below the ablation threshold value of the source film thereby to implant the dyes into the target film. This literature says that the molecular implantation technique can be utilized in the fabrication of color filters for use in displays or the like. Moreover, the literature describes that an image can be formed by moving a spot position of the laser, or the source film and the target film. In Examples of the literature, moving a sample in parallel forms a linear image.

[0012] Japanese Patent Application Laid-Open No. 150158/2000 (JP-A-2000-150158) discloses a process of producing a material for use in an organic electroluminescent device, in which a source containing an emission center-forming compound absorptive of a laser beam is brought into contact with a target having an electron-transporting function and/or a hole-transporting function and the source is irradiated with a pulsed laser beam with an intensity not higher than the ablation threshold of the source thereby to inject the emission center-forming compound into the target. This specification describes that irradiation of a laser beam through a photomask realizes unrestricted setting of a pattern form.

[0013] Accordingly, an object of the present invention is to provide a material for organic EL device (particularly, an organic EL device-use film) capable of minute and fine patterning even when a macromolecular compound is used as an EL device-use material and capable of implanting or injecting the emission center-forming compound simply and efficiently, a process for producing the same, and a material for an organic EL device, which is obtained by the process.

[0014] Another object of the present invention is to provide a material for an organic EL device, which is excellent in surface smoothness and has good contactness with electrodes, and an organic EL device using the same.

DISCLOSURE OF INVENTION

[0015] The inventors of the present invention made intensive and extensive studies to achieve the above objects, and finally found that, in a molecular implantation technique using a source constituted of an emission center-forming compound, fine patterning is realized simply and effectively by a process comprising (1) implanting or injecting an emission center-forming compound into a target by relatively moving a laser beam relative to the target, or (2) implanting or injecting an emission center-forming compound into a target with the use of an interference light of a laser. The present invention was accomplished based on the above findings.

[0016] That is, a process for producing a material for an organic electroluminescent device of the present invention comprises implanting an emission center-forming compound constituting a source into a target having at least one function selected from the group consisting of an electron-transporting function and a hole-transporting function by irradiating a laser beam, and wherein (1) the laser beam and at least the target are relatively moved with irradiating the beam to form the emission center with a predetermined pattern, or (2) the emission center at an area, corresponding to an interference pattern of an interference light, of the target is formed by irradiating the interference light of the laser beam.

[0017] In the method (1), the source and the target being in contact with each other may be moved relative to the laser beam for forming the emission center with a predetermined pattern. Moreover, the irradiation of the laser beam may be conducted through a waveguide, or the irradiation of the laser beam may be conducted with the use of an optical fiber. Further, the laser beam and the target may be relatively moved with irradiating the beam and with moving the source relative to the beam for forming the emission center. The laser beam may comprise a pulse laser beam. The laser beam and the target may be relatively moved with synchronizing the beam with a cycle of the pulse.

[0018] In the method (2), a laser beam from a single light source may be split into a plurality of light paths to cause the interference by an optical path difference. For example, the interference may be caused by introducing the laser beam into a hole or a slit, or the interference may be caused by reflecting the laser beam through a plurality of reflection paths.

[0019] The methods (1) and (2) may comprise irradiating the laser beam with an intensity of or below the ablation threshold value of the source. The laser beam may comprise a pulse laser beam. The target may comprise an organic polymer. The target may comprise a compound having at least one function selected from the group consisting of the electron-transporting function and the hole-transporting function, and a film-formable organic polymer. The compound may comprise an oxadiazole derivative having the electron-transporting function, and/or an aromatic tertiary amine having the hole-transporting function.

[0020] The present invention also includes a material for an organic electroluminescent device, which is obtainable by the above-mentioned process, and an organic electroluminescent device using the material for an organic electroluminescent device.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0021]

Figure 1 is a schematic view explaining the method (1), which is one embodiment of a technique of implanting or injecting an emission center-forming compound.
Figure 2 is a schematic view explaining the method (2), which is another embodiment of a technique of implanting or injecting an emission center-forming compound.
Figure 3 is a schematic sectional view showing one embodiment (single-layer structure) of the organic electroluminescent device of the present invention.
Figure 4 is a schematic sectional view showing another embodiment (multilayered structure) of the organic electroluminescent device of the present invention.
Figure 5 is a schematic sectional view showing further another embodiment (multilayered structure) of the organic electroluminescent device of the present invention.
Figure 6 is a schematic sectional view showing still another embodiment (multilayered structure) of the organic electroluminescent device of the present invention.
Figure 7 is a schematic view explaining another production process according to the method (1) of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

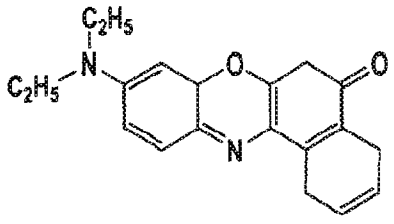
[Source (A)]

[0022] The source need only contain at least an emission center-forming compound, and may be comprised of the emission center-forming compound singly, or of the emission center-forming compound and a binder.

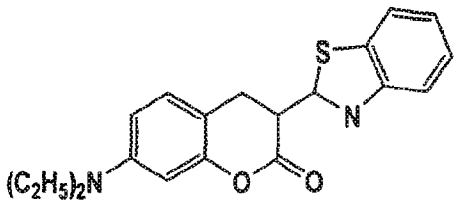
(Emission center-forming compound)

[0023] As the emission center-forming compound, a compound having function as an emission center-forming compound for organic EL device and being absorptive of laser beams, in particular a compound emitting a light by being excited by an electron and/or a hole (positive hole), can be utilized. The emission center-forming compound includes a heterocyclic compound containing at least one hetero atom selected from oxygen, nitrogen and sulfur atoms [e.g., a bis(C_{1-6}alkyl-benzoxazoyl)thiophene such as 2,5-bis(5-tert-butyl-2-benzoxazoyl)-thiophene, nile red, a coumarin such as coumarin 6 and coumarin 7, a 4-(dicyanoC_{1-4}alkylene)-2-C_{1-4}alkyl-6-(p-diC_{1-4}alkylaminostyryl)-4H-pyran such as 4-(dicyanomethylene)-2-methyl-6-(p-dimethylaminostyryl)-4H-pyran, and quinacridone]; a condensed polycyclic hydrocarbon such as rubrene and perylene; a tetraC_{6-12}aryl-1,3-butadiene such as 1,1,4,4-tetraphenyl-1,3-butadiene (TPB); a bis(2-(4-C_{1-4}alkylphenyl)C_{2-4}alkynyl)benzene such as 1,4-bis(2-(4-ethylphenyl)ethynyl)benzene; and a bis(2,2'-diC_{6-12}arylvinyl)biphenyl such as 4.4'-bis(2.2'-diphenylvinyl)biphenyl. Among them, nile red and coumarin 6 are particularly preferable.

[0024] The structures of nile red and coumarin 6 are shown below:



nile red



coumarin 6

[0025] The wavelength of light emitted by nile red is 580 nm (emission of red light) and that of coumarin 6 is 490 nm (emission of green light).

[0026] These emission center-forming compounds may be used either singly or in combination.

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(Binder)

[0027] As the binder, usually, a resin having film-forming properties (e.g., a thermoplastic resin, a thermosetting resin) can be used.

[0028] Examples of the thermoplastic resin are a olefinic resin such as a polyethylene, a polypropylene, an ethylene-propylene copolymer and a polybutene; a styrenic resin such as a polystyrene, a rubber-modified (or rubber-containing, rubber-reinforced) polystyrene (HIPS), an acrylonitrile-styrene copolymer and an acrylonitrile-butadiene-styrene copolymer; an acrylic resin [for example, a homo- or copolymer of a (meth)acrylic monomer (e.g., a C_{1-6}alkyl (meth) acrylate such as methyl (meth)acrylate, ethyl (meth)acrylate and butyl (meth)acrylate, a hydroxyC_{2-4}alkyl (meth)acrylate such as hydroxyethyl (meth)acrylate and hydroxypropyl (meth)acrylate, glycidyl (meth)acrylate, (meth)acrylic acid, and (meth)acrylonitrile), a copolymer of the (meth) acrylic monomer and a copolymerizable monomer (e.g., an aromatic vinyl monomer such as styrene) (for example, a methyl methacrylate-styrene copolymer)]; a vinyl alcohol-series polymer such as a polyvinyl alcohol and an ethylene-vinyl alcohol copolymer, a vinyl-series resin such as a polyvinyl chloride, a vinyl chloride-vinyl acetate copolymer, a polyvinylidene chloride, a polyvinyl acetate, an ethylene-vinyl acetate copolymer and a polyvinyl acetyl; a polyamide-series resin such as a 6-nylon, a 6,6-nylon, a 6,10-nylon and a 6,12-nylon; a polyester resin [for example, an alkylene arylate-series resin such as a polyalkylene terephthalate (e.g., a polyethylene terephthalate and a polybutylene terephthalate) and a polyalkylene naphthalate, or alkylene arylate copolyester resin]; a fluorine-containing resin; a polycarbonate; a polyacetal; a polyphenylene ether; a polyphenylene sulfide; a polyether sulfone; a polyether ketone; a thermoplastic polyimide; a thermoplastic polyurethane; and a norbornene-series polymer.

[0029] Exemplified as the thermosetting resin are a phenolic resin, an amino resin (e.g., a urea resin and a melamine resin), a thermosetting acrylic resin, an unsaturated polyester resin, an alkyd resin, a diallyl phthalate resin, an epoxy resin, and a silicone resin.

[0030] The binder may be used singly or in combination.

[0031] The content of the emission center-forming compound in the source is not particularly limited to a specific content, and is about 0.1 to 100% by weight, preferably about 1 to 90% by weight, and more preferably about 5 to 80% by weight. Moreover, in the case where the source comprises an emission center-forming compound and a binder, the content of the emission center-forming compound is not particularly limited to a specific content, and for example is about 0.1 to 60 parts by weight, preferably about 1 to 30 parts by weight, and more preferably about 3 to 20 parts by weight relative to 100 parts by weight of the binder.

[0032] The source is usually used in the form of a film. Moreover, the source may be a film or coat of the above emission center-forming compound singly formed on the substrate or the target, or that of the above emission center-forming compound and the binder. In the case of irradiating a laser beam from the source side, the substrate need only be sufficiently transparent to transmit laser beams, examples of which are a glass plate such as a soda glass, a no-alkali glass, and a quartz glass; and a polymer sheet or film of a polyester, a polystyrene, an acrylic resin, a vinyl-series resin (e.g., a polyvinyl acetal), a polysulfone, and of a polyethersulfone.

[0033] There is no particular restriction as to a process of forming a source film, and a conventional process [e.g., dry processes such as vapor deposition (vacuum deposition), wet coating processes that use a solvent, such as spin coating, dip coating and die coating] may be employed. Incidentally, the film may be formed in accordance with a conventional film-forming process (e.g., casting method and extrusion method).

[0034] If necessary, into the coating agent (coating liquid) for forming a coat (coating film) of the source, i.e., the source may be incorporated a solvent (e.g., water; alcohols such as methanol and ethanol; esters such as ethyl acetate and isobutyl acetate; ketones such as acetone and methyl ethyl ketone; aromatic hydrocarbons such as toluene; alicyclic hydrocarbons such as cyclohexane; halogenated hydrocarbons such as chloroform and chlorobenzene; ethers; cellosolves; carbitols). The thickness of the film (coat) may be about 0.01 to 50 μm, preferably about 0.1 to 30 μm, and more preferably about 0.5 to 20 μm.

[0035] Moreover, the source may not be defined in a pattern, or the source itself may be defined in a given pattern. A film (layer, deposit) defined in a pattern, if necessary, on a substrate (base material) or a target may be used as a source. For example, a film or sheet comprising an emission center-forming compound may be patterned by punching or other means to give a source. Moreover, the substrate need only be sufficiently transparent to transmit laser beams, examples of which are a glass plate such as a soda glass, a no-alkali glass, and a quartz glass; and a polymer sheet or film of a polyester, a polystyrene, an acrylic resin, a vinyl-series resin (e.g., a polyvinyl acetal), a polysulfone, and of a polyethersulfone.

[0036] In the case of defining into a pattern of a source, the pattern is selected according to the intended application, and for example may be any of a one dimensional pattern [a dotted pattern, a lined pattern (e.g., parallel, random, grid)] and a two-dimensional pattern [a plane pattern (e.g., circular, oval, polygonal such as triangle and rectangle, star-shaped)]. The predetermined pattern is provided on the substrate or the target by, for example, printing such as screen printing, ink jet system, melt or thermal transfer, or vapor deposition (sublimation printing) involving masking.

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[Target (B)]

[0037] Insofar as the target has at least one function selected from the electron-transporting function and the hole-transporting function, there is no particular restriction, and the target may be (I) a resin having at least one function selected from the electron-transporting function and the hole-transporting function, or (II) a resin composition comprising a resin which inherently has neither the electron-transporting function nor the hole-transporting function but given with at least one function selected from these. As the resins for the use of (I) and (II), resins (binder) having film- or coat-forming properties are preferred. Moreover, when the laser beam is incident from the side of the target, the target is transmittable of the laser beam.

[0038] Exemplified as the resin (I) having at least one function selected from the electron-transporting and hole-transporting functions is a polyphenylenevinylene [for example, a homo- or copolymer of a C_{6-12}arylenevinylene, which may have a substituent (e.g., a C_{1-10}alkoxy group), such as a polyphenylenevinylene, a poly(2,5-dimethoxyphenylenevinylene) and a polynaphthalenevinylene]; a polyphenylene (in particular, a polyparaphenylene) [for example, a homo- or copolymer of a phenylene, which may have a substituent (e.g., a C_{1-10}alkoxy group), such as a polyparaphenylene and a poly-2,5-dimethoxyparaphenylene]; a polythiophene [a homo- or copolymer of a polyC_{1-20}alkylthiophene such as a poly(3-alkylthiophene), a polyC_{3-20}cycloalkylthiophene such as a poly(3-cyclohexylthiophene), and a C_{6-20}arylthiophene, which may have a substituent (e.g., a C_{1-10}alkyl group), such as a poly(3-(4-n-hexylphenyl)thiophene)]; a polyfluorene such as a polyC_{1-20}alkylfluorene; a vinyl-series polymers having at least one functional group selected from a hole-transporting functional group and an electron-transporting functional group in the main or side chain, such as a poly-N-vinylcarbazole (PVK), a poly-4-N,N-diphenylaminostyrene, a poly(N-p-diphenylamino)phenylmethacrylamide), a poly(N,N'-diphenyl-N,N'-bis(3-methylphenyl)-1,1'-biphenyl-4,4'-diaminomethacrylamide) (PTPDMA) and a poly-4-(5-naphthyl-1,3,4-oxadiazole)styrene; a polyC_{1-4}alkylphenylsilane such as a polymethylphenylsilane; a polymer having an aromatic amine derivative in a side or main chain thereof; and a copolymer thereof. The resin can be used either singly or in combination. The preferred target includes a copolymer comprising a poly-N-vinylcarbazole or N-vinylcarbazole as a main component (not less than 50% by weight, and preferably about 60 to 98% by weight), and a polymer having an aromatic amine derivative in a side chain or main chain thereof.

[0039] PVK is amorphous and excellent in heat resistance (glass transition temperature Tg: 224°C). The degree of polymerization of PVK is not particularly restricted, and is, for example, about 200 to 5,000 (e.g., 300 to 3,000), and preferably about 500 to 2,000 (e.g., 500 to 1,500).

[0040] Further, if needed, the electron- or hole-transporting function may be given to the resin (I).

[0041] Examples of the compound having an electron-transporting function are an oxadiazole derivative [for example, an oxadiazole derivative having a C_{6-20}aryl group which may have a substituent, such as 2-(4-biphenyl)-5-(4-tert-butylphenyl)-1,3,4-oxadiazole (PBD), 2,5-bis(1-naphtyl)-1,3,4-oxadiazole (BND), 1,3-bis[5-(4-tert-butylphenyl]-1,3,4-oxadiazole)]benzene (BPOB), 1,3,5-tris[5-(4-tert-butylphenyl)-1,3,4-oxadiazole]benzene (TPOB) and 1,3,5-tris[5-(1-naphtyl)-1,3,4-oxadiazole]benzene (TNOB)]; a diphenoquinone [for example, a diphenoquinone which may have a substituent (e.g., a C_{1-10}alkyl group), such as 3,5,3',5'-tetrakis-tert-butyldiphenoquione]; 1,2,3,4,5-pentaphenyl-1,3-cyclopentadiene (PPCP); and a quinolinic acid complex such as a tris(8-quinolinorato)aluminium (III) complex, a bis(benzoquinolinolato)beryllium complex and a tris(10-hydroxybenzo[h]quinolilate)beryllium complex. Particularly PBD is preferred.

[0042] As the compound having a hole-transporting function, there may be exemplified an aromatic tertiary amine such as N,N'-diphenyl-N,N'-bis(3-methylphenyl)-1,1'-biphenyl-4,4'-diamine (TPD), N,N'-diphenyl-N,N'-bis(1-naphthyl)-1,1'-biphenyl-4,4'-diamine (NPD), 1,1-bis[(di-4-tolylamino)phenyl]cyclohexane, N,N,N'N'-tetra(3-methylphenyl)-1,3-diaminobenzene (PDA), 4,4',4", tris (3-methylphenylphenylamino) triphenylamine (m-MTDATA), 4,4',4"-tris(1-naphthylphenylamino)triphenylamine(1-TNATA), 4,4',4"-tris(2-naphthylphenylamino)triphenylamine (2-TNATA), 4,4',4"-tri(N-carbazolyl)triphenylamine (TCTA), 1,3,5-tris(4-(3-methylphenylphenylamino)phenyl]benzene (m-MTDAPB) and triphenylamine; and a phthalocyanine.

[0043] The above compound can be used either singly or in combination. Incidentally, among these compounds, a compound emitting a light by being excited by an electron and/or a hole may be used as an emission center-forming compound.

[0044] The proportion of the above-mentioned component contained in the resin (I) (e.g., PVK) can be selected within the range not adversely affecting the functions qualifying the resin as an organic EL device material, and is, for example, about 10 to 300 parts by weight, and preferably about 20 to 200 parts by weight relative to 100 parts by weight of the resin (I).

[0045] When the target is constituted of the resin (I) and the compound described above, the organic EL device which will later be described can be made so as to have a single-layered structure, and the organic EL device so fabricated not only has improved luminous efficiency but also is economically advantageous.

[0046] There is no specific restriction as to a resin to be used in the resin composition (II), and such a variety of above-mentioned binders having the film-forming properties (e.g., thermoplastic resins, thermosetting resins) are avail-

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able. At least one function selected from the electron-transporting function and the hole-transporting function may be given to these resins. Exemplified as the compound(s) to be used to provide the electron- or hole-transporting function are compounds similar to those listed above.

[0047] The amount of the compound having an electron-transporting or hole-transporting function to be added is about 10 to 300 parts by weight (e.g., about 10 to 200 parts by weight) and preferably about 20 to 100 parts by weight (e.g., about 20 to 80 parts by weight) relative to 100 parts by weight of the binder resin.

[0048] The resin (I) and the resin composition (II) may be used in combination, and such combined material may further be given at least one function selected from the electron-transporting function and the hole-transporting function.

[0049] Incidentally, a form (shape or configuration) of the target is not particularly limited to a specific form, and usually, is used in the form of a film. Moreover, the target is formed in the same manner as in the source, and usually is formed on the above-mentioned substrate.

[Production process of material for organic EL device (molecular implantation)]

[0050] The process for producing materials for organic EL devices of the present invention comprises implanting an emission center-forming compound in a source into the target by irradiating (or exposing) a laser beam, and wherein (1) the laser beam and at least the target are relatively moved with irradiating the beam to form the emission center with a predetermined pattern, or (2) the emission center at an area, corresponding to an interference pattern of an interference light, of the target is formed by irradiating the interference light of the laser beam. The laser beam may be irradiated from the source (A) side or the target (B) side. As the target, a film is usually employed to produce a film for an organic EL device. Moreover, the target may be brought into contact with the source.

[0051] Exemplified as the laser beam to be used in the present invention are, though it differs with the species of the emission center-forming compound to be used, those having an oscillation wavelength within the range of 190 to 1,100 nm. When using a pulse laser beam (pulsed laser beam), the frequency is about 0.5 to 50 Hz and preferably about 0.5 to 30 Hz. Moreover, although the pulse width varies with the wavelength of the laser beam, it is about 10 ps to 10 μs (e.g., about 10 ps to 1 μs), preferably about 50 ps to 100 ns (e.g., about 100 ps to 50 ns). The shorter the pulse width (duration) is, the less the decomposition of the emission center-forming compound occurs, and therefore, the emission center-forming compound is hardly damaged.

[0052] Exemplified as the source of the laser beam are gas laser [ArF excimer laser (193 nm), KrF excimer laser (248 nm), XeCl excimer laser (308 nm), XeF excimer laser (351 nm), nitrogen laser (337 nm)], dye laser [nitrogen laser, excimer laser, or YAG laser excitation, 300 to 1,000 nm], solid-state laser [(Nd:YAG excitation, semiconductor laser excitation, etc.), ruby laser (694 nm), semiconductor laser (650 to 980 nm), tunable diode laser (630 to 1,550 nm), titanium-sapphire laser (Nd:YAG excitation, 345 to 500 nm, 690 to 1,000 nm), and Nd:YAG laser (FHG: 266 nm, THG: 354 nm, SHG: 532 nm, fundamental wave: 1,064 nm)].

[0053] In the production process of the present invention, irradiation of a laser beam with an intensity of or below the ablation threshold of the source (that is, the emission center-forming compound or binder) makes it possible to effectively implant the emission center-forming compound into the target. The amount of the emission center-forming compound to be implanted can be controlled by regulating, e.g., the intensity and wavelength of the laser beam, and the number of times the laser beam is shot.

[0054] The ablation threshold of the source (A) varies with the species of the emission center-forming compound constituting the source. Moreover, the ablation threshold also depends on the wavelength and pulse width of the laser beam. Therefore, in the present invention, the ablation threshold is defined as follows.

[0055] The term "ablation threshold value" used in the present invention is defined as a term referring to, assuming that a source is irradiated with one shot of a laser beam and observed by a contact-type (mode) surface morphology measuring apparatus (e.g., DEKTAK3030ST, manufactured by SLOAN), the lowest laser intensity (mJ/cm^2) measured on the surface irradiated with the laser beam at which the surface might suffer changes in surface conditions by a depth of 50 nm or more. The source and the laser beam are the same as those employed in the present invention.

[0056] Hereinafter, the process of the present invention for producing a material for use in an organic EL device (particularly, films for use in organic EL devices) will be described with reference to Figures. Figure 1 shows a schematic view showing a production process in the method (1) of the present invention. Figure 2 shows a schematic view showing a production process in the method (2) of the present invention. A source 1, a target 2, an emission center-forming compound 3, a substrate resided in the target side 4, a substrate resided in the source side 5, and a hole 6 are illustrated in Figures.

[0057] According to Figure 1, firstly, the source 1 formed on the substrate 5 is brought into contact with or closely contact with the target 2 formed on the substrate 4, and irradiated with a laser beam with an intensity of or below the ablation threshold of the source from the source 1 side with relatively moving the beam relative to the target. The emission center-forming compound, which absorbed the laser beam, obtains high translational energy and is injected or implanted into the target 2 without being decomposed, and a material for an organic EL device (particularly, a film)

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is obtained.

[0058] According to Figure 2, firstly, the source 1 formed on the substrate 5 is brought into contact with or closely contact with the target 2 formed on the substrate 4, and irradiated with a laser beam with an intensity of or below the ablation threshold of the source from the source 1 side with causing an interference by introducing the beam into a hole 6. The emission center-forming compound, which absorbed the laser beam, obtains high translational energy and is injected or implanted into an area, corresponding to an interference pattern of the interference light, of the target 2 without being decomposed, and a material for an organic EL device (particularly, a film) is obtained.

[0059] In the methods (1) and (2), the laser beam is shot about 1 to 200 times, preferably about 1 to 150 times, and more preferably about 1 to 100 times (e.g., about 5 to 50 times). Moreover, the laser beam may be shot from the target side. Incidentally, the source may be formed on the target directly as a surface layer. The source formed on the target can be removed from the target easily after implanting the emission-center compound. Moreover, the source may be formed by a surface layer removable or separable from the target.

[0060] The substrate to be used need only have sufficient transparency to transmit a laser beam, examples of which are the above-mentioned substrates (e.g., a glass plate such as a quartz glass, a polymer sheet or film). As the substrate, a substrate used on forming of a source or a target film may be employed without modification, or a substrate produced freshly may be employed.

[0061] In the process for producing the material for the organic EL device of the present invention, there is no particular restriction as to the shape that the cross-section of the laser beam takes, and it may be circular, oval, or polygonal (e.g., triangle, rectangle). The average beam area of the laser beam is not particularly limited to a specific area, and can be selected from a wide range for any purpose. For example, the area is about 0.01 to 5,000 μm^2, preferably about 0.1 to 4,000 μm^2, and more preferably about 1 to 3,000 μm^2. Incidentally, in the method (1), a pattern may be defined or formed by narrowing an area of a laser beam down a desired size and scanning a predetermined pattern, or an emission center-forming compound may be implanted into a target in a predetermined area by enlarging the area of the laser beam to use a source having a predetermined pattern or relatively scanning a laser beam through a photomask.

[0062] Moreover, a plurality of sources having emission center-forming compounds different from one another may be employed. For example, the use of a compound capable of emitting a light in visible light region (a compound capable of emitting a light such as yellow, red, green or blue) realizes a desired emission color. Moreover, in the method (2), the use of a plurality of sources realizes that an emission light such as red, green and blue can be arranged or arrayed as corresponding to an interference fringe or pattern (e.g., vertical stripe, delta arrangement and tetragonal arrangement). Therefore, the present invention makes it possible to obtain materials for organic EL devices capable of emitting various colors and having various patterns.

[0063] The method (1) has a characteristic that the laser beam and at least the target are relatively moved for implanting an emission center-forming compound of a source into the target with a predetermined pattern. In the method (1), the source and the target are contacted with each other and positioned, and the source may be moved with the target, or the source may be movable relative to the target relatively. In the case where the source and the target are contacted with each other, an irradiation of a laser beam may, for example, be conducted either by (1-1) moving a light path of the laser beam relative to the source and the target, or by (1-2) moving the source and the target relative to a light path of the laser beam. Furthermore, in these methods, the light path of the laser beam is movable not only by moving a laser light source relatively but also (1-3) by using means for controlling the light path.

[0064] The means for controlling the light path includes a process of utilizing physical means or physico-optical means [for example, an optical device (or optical member) such as an optical fiber, a reflection mirror (e.g., a total reflection mirror, a half reflection mirror), a lens (e.g., condenser) and a deflecting prism, or means in combination with them], a process of utilizing electro-optical means [(e g., applying a voltage to an electro-optical crystal (a birefringent crystal)] to move a light path of a light beam of a waveguide, and a process of utilizing supersonic waves. Incidentally, in a process of utilizing supersonic waves, the waveguide can be moved by using a crystalline material (such as water, a chalcogenide-series vitreous material, PbMoO4, TeO_2, Ge, $LiNbO_3$ and GaP) as a medium, and applying a voltage to the medium through a piezoelectric thin film transducer (e.g., a piezoelectric device such as $LiNbO_3$ and ZnO) to generate supersonic waves to the medium.

[0065] In the physical means or physico-optical means, when the light path of the laser beam is moved by utilizing an optical fiber, a diffusion loss of the laser beam can be reduced, and efficient and fine patterning can be conducted simply.

[0066] Incidentally, according to the method (1), the laser beam is capable of moving relatively and two-dimensionally relative to at least a target. Therefore, an emission center-forming compound of a source can be implanted into a target with a predetermined pattern efficiently, and the emission center can be formed in the form of a two-dimensional pattern.

[0067] For example, precise positioning is realized easily and two-dimensional fine patterning is realized, by bringing a source into contact with a target, fixing them on a table movable for X-Y axial direction with turning up a target surface or source surface, setting up a sensor for detecting a displacement from a reference position of the target (or source)

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to X-axial and Y-axial directions, and moving the table to X-axial and Y-axial directions in response to a detection signal obtained from the sensor. Incidentally, if necessary, by setting up a memory memorized a data of the pattern, and a controller for moving the laser and/or the table in response to the pattern signal, patterning can be conducted simply.

[0068] In the case where a pulse laser is used as a laser beam, a target and a laser beam are relatively shifted by relatively moving the laser beam relative to at least the target according to the above-mentioned manner by synchronizing with a pulse cycle, and an emission center-forming compound can be implanted into a target efficiently. In the process, the target may be moved relative to the laser beam, and usually synchronizing with pulse cycle controls the laser beam or a light path of the laser beam.

[0069] Further, according to the present invention, a laser beam may be relatively moved relative to at least a target, and a source may be moved relative to the laser beam. Incidentally, by repeated irradiation of a laser beam to the same site of the source is consumed an emission center-forming compound, and is unable to form an emission center efficiently. In such a case, relative movement of the laser beam and the target with irradiating the laser beam and with relatively moving the source relative to the laser beam realizes that an emission center-forming compound is implanted into the target effectively and efficiently.

[0070] For example, a plurality of emission centers different from each other in emission color (e . g., emission centers having full-color) can be also formed efficiently. According to the method (1), a plurality of areas comprising each of emission center-forming compounds (e.g., an area comprising a yellow emission center-forming compound, an area comprising a red emission center-forming compound, and an area comprising a blue emission center-forming compound) may be formed into a source. The use of such a source ensures that a plurality of emission centers different from each other in emission color can be formed with use of a single source by relatively moving the source relative to the laser beam and/or the target toward X-axial and/or Y-axial direction(s).

[0071] Figure 7 shows a schematic view explaining another production process according to the method (1). In the embodiment, a production process of a red emission center comprises moving a light path of a laser beam (light source or waveguide) relative to a target toward a longitudinal direction and/or a lateral direction, irradiating (or exposing) the laser beam to an area comprising a green emission center-forming compound of a source to form a green emission center into the target, moving the source relative to the laser beam, then irradiating the laser beam to an area comprising a red emission center-forming compound to form a red emission center into the target. Further, a blue emission center is produced in the same manner as described above, and a material for an organic EL device capable of emitting a full-colored light can be produced. Moreover, according to the method, a pulse laser is irradiated (or emitted) to the target through the source with scanning toward a longitudinal direction and/or a lateral direction, and the source 1 and the target 2 is capable of contacting with each other at an irradiation site of the laser beam. Incidentally, the source 1 is movable to X-axial and/or Y-axial direction(s) by means of a feed apparatus.

[0072] In this way, when the source is moved relative to the laser beam, the use of a single source realizes that a plurality of emission centers different from each other in emission color are produced. An emission center-forming compound is used without wasting, the emission center-forming compound is implanted efficiently, and the process is advantageous in terms of cost. Moreover, the source may be formed with an undefined length film or the like. The use of such a film realizes a continuous or successive production of an emission center-forming compound.

[0073] The method (2) has a characteristic that the utilization of high coherence (coherency) of a laser beam realizes a production of an emission center into an area corresponding to an interference pattern of an interference light in the target by the interference light of the laser beam. Incidentally, "interference" also includes diffraction (considered as an interference of small wave (secondary wave) by the Principle of Huygens) ("Basis and Experiment of Laser", Koreiwa Matsudaira, issued by Kyoritsu Shuppan, Co., Ltd., the 11th edition, page 54).

[0074] In the method (2), an interference of a laser beam may be obtained from optical path difference caused by splitting a laser beam from the single light source into a plurality of light paths. A process for interfering with a laser beam is not limited to one using a hole as shown in Figure 2, and for example, may be conducted either by (2-1) introducing a laser beam into a hole or a slit to cause an interference, or by (2-2) reflecting a laser beam through a plurality of reflection paths capable of reflecting to cause an interference.

[0075] In the hole or the slit, a slit width (in case of the hole, the average hole diameter) is not particularly limited, and is about 0.01 to 100 mm, preferably about 0.1 to 10 mm, and more preferably about 0.5 to 5 mm (e.g., about 0.5 to 3 mm). Incidentally, there is no particular restriction as to a shape of the hole, and may be mentioned circular, oval, or polygonal (e.g., triangle, rectangle). In the case where the shape of the hole is noncircular, the average diameter means an average diameter of circumscribed circle of the hole.

[0076] Incidentally, the hole and the slit may be a single hole or slit, or each of them may be used plurally or in combination (e.g., double slit). Moreover, the hole and the slit may be used in combination. A laser beam guided by the hole or the slit is interfered by the optical path difference (in case of using a single hole or slit, diffracted), and interference fringe (or diffraction fringe) occurs.

[0077] In the method (2-2), a mirror (e.g., a semitransparent mirror, a reflecting mirror) is usually employed in order to reflect a laser beam. In particular, the use of a semitransparent mirror ensures that an optical path difference between

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a transmitted light and a reflected light generates simply. For example, the process comprises being incident a laser beam on a semitransparent mirror, which is disposed with gradient of a predetermined angle from an incident direction of the laser beam, transmitting part of the laser beam and reflecting the residual laser beam in an orthogonal direction to the incident direction of the laser beam. The transmitted light is incident on a first reflection mirror apart from the semitransparent mirror at a predetermined distance. On the other hand, the reflected light is incident on a second reflection mirror apart from the semitransparent mirror at a distance different from the above distance. A laser beam, which is obtained by reflecting with use of the first and the second reflection mirror, going through a different reflection path and being incident on the semitransparent mirror again, is incident on the target, and as a result, an interference occurs by an optical path difference. Moreover, by adjusting a distance between the transparent mirror and the reflection mirror, a desired interference pattern can be obtained.

[0078] Incidentally, each of the semitransparent mirror(s) and the reflection mirror(s) may be used singly or in combination. In order to be incident the laser beam on the semitransparent mirror efficiently, the laser beam may be made parallel pencil through a lens (such as a telemeter lens) and may be incident on the semitransparent mirror.

[0079] In such a method (2-1) or (2-2), a distance between interference fringes, or a shape (or form) of interference fringe can be adjusted by selecting parameters such as a hole diameter or a slit width and a mirror position suitably, and by varying an optical path distance. A desired interference pattern (interference fringe) can be obtained without through a mask and the like. In particular, when the hole diameter or the slit width is turned down to a wavelength of the laser beam, interference fringe having a fine distance can be obtained, and fine patterning of an emission center-forming compound can be conducted easily. Further, since the interference fringe is usually a concentric pattern (symmetric figure) in which a center energy is most highest, the amount to be implanted of the emission center-forming compound can be adjusted.

[0080] Moreover, the production process of the present invention realizes that an emission center-forming compound is implanted into a target not in a dispersed or diffused form but in a step form (that is, an oblong form, in which the depth of the compound implanted into the target is uniform). The depth is varied depending on a kind or species of the emission center-forming compound or the target, or intensity of a laser beam, and for example, is about 10 to 300 nm, preferably about 15 to 200 nm, and more preferably about 20 to 100 nm. Moreover, irradiation of the laser beam with an intensity of or below the ablation threshold value ensures that an emission center-forming compound is implanted efficiently without deterioration in surface smoothness of a material for an organic EL device.

[Organic electroluminescent device]

[0081] The organic electroluminescent device of the present invention comprises a material for an organic EL device obtained by the process described above (particularly, a light-emitting layer constituted of a target film into which an emission center-forming compound has been implanted) and a pair of electrodes.

[0082] As the anode, a transparent electrode formed by vacuum deposition or other methods (e.g., indium-tin-oxide (ITO) electrode) or the like is employed, and a highly conductive metal having a small work function (e.g., magnesium, lithium, aluminum, or silver) is used as the cathode. In the case where magnesium is employed as the cathode, the magnesium may be coevaporated with a small amount of silver (e.g., 1 to 10% by weight) for improving the adhesion with an organic EL device-use film.

[0083] When the light-emitting layer has both the electron-transporting function and the hole-transporting function, the organic EL device of the present invention can be made so as to have a single-layered structure. When the light-emitting layer is lacking in either the electron-transporting function or the hole-transporting function or when attempting to improve each function, a layer having the desired function may be laminated on the light-emitting layer by a conventional vapor deposition technique or a solution coating technique. These layers may be of low-molecular weight compounds or macromolecular compounds, and either will do. The organic EL device can take, for example, a single-layer structure or a multilayer-structure as shown in Figures 3 to 6.

[0084] That is, as illustrated in Figure 3, the organic EL device may be one composed of a substrate 10, an anode 11 formed thereon, a light-emitting layer 12, and a cathode 13 laminated on the anode in this order, or, as shown in Figure 4, it may be one composed of a substrate 20, an anode 21 formed thereon, a hole-transporting layer 24, a light-emitting layer 22, and a cathode 23 laminated on the anode in this order. Further, as shown in Figure 5, the organic EL device may be one composed of a substrate 30, an anode 31 formed thereon, a light-emitting layer 32, an electron-transporting layer 35, and a cathode 33 laminated on the anode in this order, or, as shown in Figure 6, it may be one composed of a substrate 40, an anode 41 formed thereon, a hole-transporting layer 44, a light-emitting layer 42, an electron-transporting layer 45, and a cathode 43 laminated on the anode in this order.

[0085] The thickness of each of the layers constituting the organic EL device is not particularly limited, and is about 10 nm to 1 μm(e.g., about 10 to 500 nm), preferably about 30 to 300 nm, more preferably about 30 to 200 nm, particularly about 5 to 20 nm. When films are employed, the thickness of each film can be selected within the ranges mentioned above.

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[0086] Exemplified as the substrate are those mentioned above, such as substrates having sufficient transparency to transmit laser beams (e.g., a glass plate, such as a soda glass, a no-alkali glass, and a quartz glass, a polymer sheet or film of a polyester, a polysulfone, and a polyethersulfone). For the fabrication of flexible organic EL devices, the use of polymer films are preferred. As the substrate, a substrate used on the molecular implantation may be employed without modification, or a substrate produced freshly may be employed.

[0087] According to the present invention, fine and multicolor patterning of an organic EL device made with macromolecular compounds which had long been difficult to realize was made possible. Further, since the material for the organic EL device (particularly, film for organic EL device) of the present invention is excellent in surface smoothness, it makes closely contact with the electrodes, and the organic EL device of the present invention is free from the irregularity in voltage caused upon application of voltage because of the emission center-forming compound implanted therein step-like.

INDUSTRIAL APPLICABILITY

[0088] The present invention ensure that high positioning is conducted by relatively moving a laser beam relative to at least a target, fine patterning is conducted simply, and the use of an optical fiber realizes high-precision fine patterning. Moreover, an efficient implantation of emission center-forming compound is realized by relatively moving a laser beam and at least a target with moving a source relative to the laser beam.

[0089] Moreover, according to the present invention, the utilization of high coherence (coherency) of a laser beam realizes a production of an emission center into an area corresponding to an interference pattern by an interference light of the laser beam. Since the interference pattern can be adjusted to a desired shape (form) and distance by selecting a parameter such as a hole diameter and a slit width suitably, fine patterning can be conducted simply.

EXAMPLES

[0090] The following examples are intended to describe this invention in further detail and should by no means be interpreted as defining the scope of the invention.

Example 1

(Preparation of source film)

[0091] A polybutylmethacrylate (manufactured by Aldrich Chemical Company, Inc., molecular weight: 3.4×10^5) containing 5% by weight of coumarin 6 (manufactured by Nippon Kankoh Shikiso, K.K.) was dissolved in chlorobenzene, and a layer having 1 μm thick was produced on a quartz substrate by a spin coating method.

(Preparation of target film)

[0092] 500 mg of a poly-N-vinylcarbazol having a hole-transporting function (PVK: manufactured by Kanto Kagaku, K.K.) and 500 mg of 2-(4-biphenyl)-5-(4-tert-butylphenyl)-1,3,4-oxadiazole having an electron-transporting function (PBD: manufactured by Aldrich Chemical Company, Inc.) were dissolved in 10 ml of 1,2-dichloroethane. A coat layer of indium-tin-oxide (ITO) was formed on a glass substrate. Using the above-mentioned 1,2-dichloroethane solution, on the ITO coat layer thus obtained was formed a 100 nm thick target film having the electron and hole-transporting functions by dip coating.

(Molecular implantation)

[0093] An emission center-forming compound was implanted into a pattern having an area of 20 mm^2 by bringing thus obtained source film into contact with thus obtained target film, fixing them on a table movable for X-axial and Y-axial directions with a target film surface turning up, using a laser processing apparatus capable of oscillating XeF excimer laser (wavelength: 351 nm) having 10 ns of a pulse width at 20 mm^2 of a beam area, and moving the table relative to the laser beam toward X-Y-axial direction.

(Organic EL device)

[0094] A 200 nm thick Al/Li electrode (manufactured by Kohjundo Kagaku, K.K.; Li content: 0.78% by weight) was formed on the molecular-implanted target film (test piece 1) by vacuum deposition to provide an organic EL device 1.

[0095] With the ITO electrode of the above organic EL device as the anode and the Al/Li electrode layer as the

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cathode, a direct electric field was applied between the electrodes in the atmospheric air to cause the organic EL device to emit light. At a voltage of 18 V or so, emission of light was observed for the organic EL device 1. Emission of green light due to coumarin 6 was observed at the area into which coumarin 6 had been injected, and that of blue light due to PVK at the area other than the area of green light emission.

Example 2

(Preparation of source film)

[0096] A polybutylmethacrylate (manufactured by Aldrich Chemical Company, Inc., molecular weight: 3.4×10^5) containing 5% by weight of coumarin 6 (manufactured by Nippon Kankoh Shikiso, K.K.) was dissolved in chlorobenzene, and a layer having 2 μm thick was produced on a quartz substrate by a spin coating method. (Preparation of target film)

[0097] A target film was produced in the same manner as in Example 1.

(Molecular implantation)

[0098] A test piece, constituted of two films obtained above being in contact with each other, was fabricated, and, from the direction of the target substrate, the test piece was irradiated with third harmonic of YAG laser (wavelength: 355 nm, pulse width: 3 ns, irradiation energy per unit area: 20 mJ/cm^2, beam diameter: 1.8 mm) 10 times through a pinhole having a diameter of 1 mm.

(Organic EL device)

[0099] A 200 nm thick Al/Li electrode layer (manufactured by Kohjundo Kagaku, K.K.; Li content: 0.78% by weight) was formed on the molecular-implanted target film by vacuum deposition to provide an organic EL device. With the ITO electrode of the above organic EL device as the anode and the Al/Li electrode layer as the cathode, a direct electric field was applied between the electrodes in the atmospheric air to cause the organic EL device to emit light. At a voltage of 18 V or so, emission of light was observed. An emission form (shape) reflected that of light interference generated on the occasion when YAG laser beam passed through the pinhole, and emission ring pattern being green concentrically was observed. In an area without molecular implantation, emission of blue due to PVK was observed, and in an area with molecular implantation, emission of green light due to coumarin 6 was observed.

Claims

1. A process for producing a material, for an organic electroluminescent device, having an emission center, which comprises implanting an emission center-forming compound constituting a source into a target having at least one function selected from the group consisting of an electron-transporting function and a hole-transporting function by irradiating a laser beam, and wherein

   (1) the laser beam and at least the target are relatively moved with irradiating the beam to form the emission center with a predetermined pattern, or
   (2) the emission center at an area, corresponding to an interference pattern of an interference light, of the target is formed by irradiating the interference light of the laser beam.

2. A process according to claim 1, wherein, in the method (1), the source and the target being in contact with each other are moved relative to the laser beam for forming the emission center with a predetermined pattern.

3. A process according to claim 1, wherein, in the method (1), the irradiation is conducted through a waveguide.

4. A process according to claim 1, wherein, in the method (1), the irradiation is conducted with the use of an optical fiber.

5. A process according to claim 1, wherein, in the method (1), the laser beam and the target are relatively moved with irradiating the beam and with moving the source relative to the beam for forming the emission center.

6. A process according to claim 1, wherein, in the method (2), a laser beam from a single light source is split into a plurality of light paths to cause the interference by an optical path difference.

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7. A process according to claim 6, wherein the interference is caused by introducing the laser beam into a hole or a slit.

8. A process according to claim 6, wherein the interference is caused by reflecting the laser beam through a plurality of reflection paths.

9. A process according to claim 1, which comprises irradiating the laser beam with an intensity of or below the ablation threshold value of the source.

10. A process according to claim 1, wherein the laser beam comprises a pulse laser beam.

11. A process according to claim 10, wherein, in the method (1), the laser beam and the target are relatively moved with synchronizing the beam with a cycle of the pulse.

12. A process according to claim 1, wherein the target comprises an organic polymer.

13. A process according to claim 1, wherein the target comprises a compound having at least one function selected from the group consisting of the electron-transporting function and the hole-transporting function, and a film-formable organic polymer.

14. A process according to claim 13, wherein the compound comprises at least one compound selected from the group consisting of an oxadiazole derivative having the electron-transporting function, and an aromatic tertiary amine having the hole-transporting function.

15. A material for an organic electroluminescent device, which is obtainable by a process recited in claim 1.

16. An organic electroluminescent device which comprises a pair of electrodes, and a material recited in claim 15 which is interposed between the electrodes.

17. An organic electroluminescent device according to claim 16, wherein a single layer formed with a material in claim 12 is interposed between the pair of electrodes.

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Fig. 1

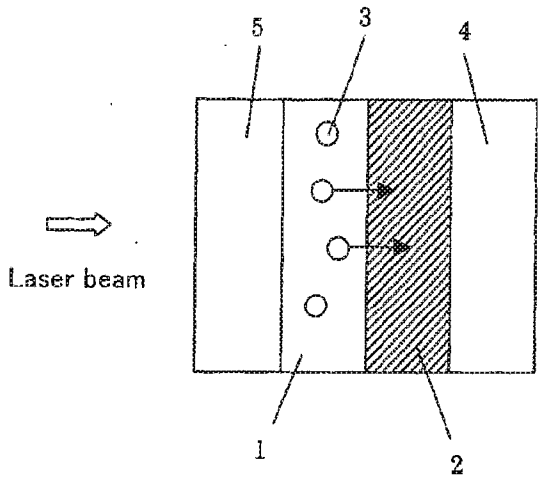


Fig. 2

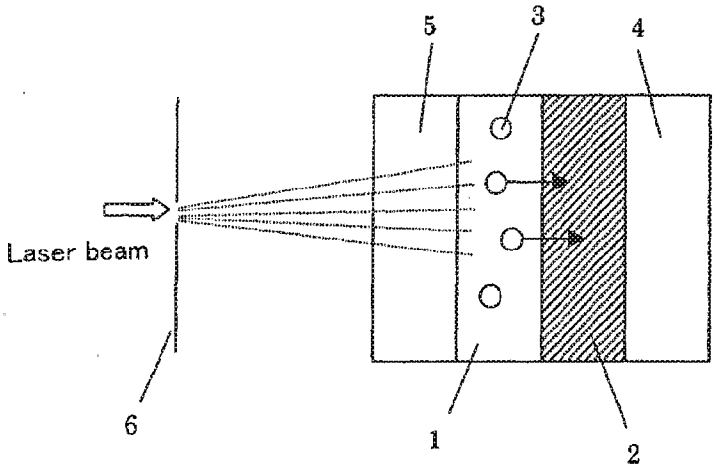
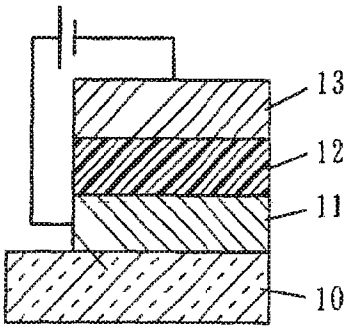


Fig. 3



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Fig. 4

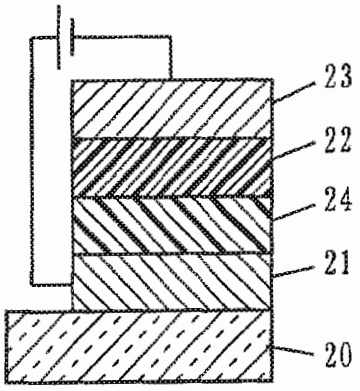


Fig. 5

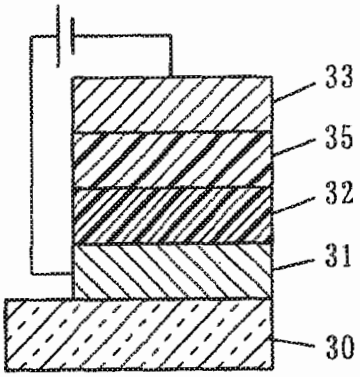
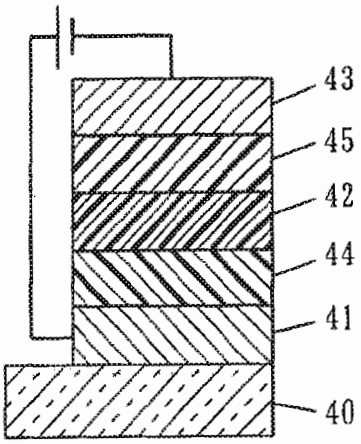
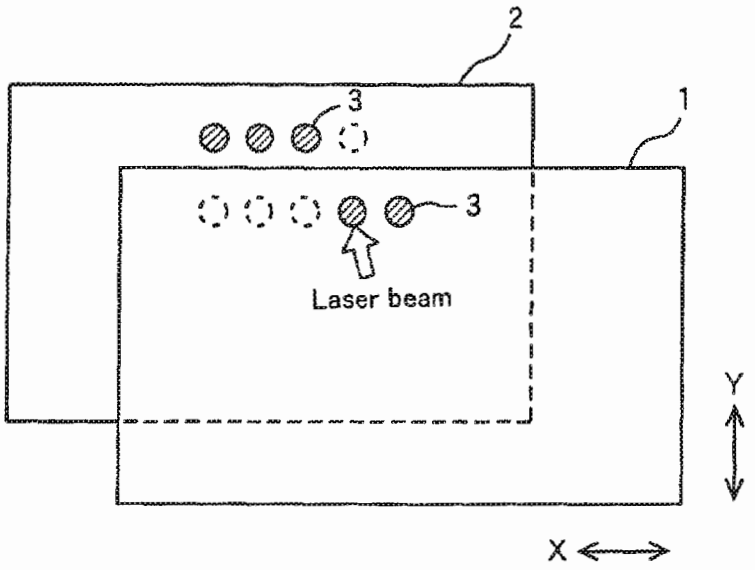


Fig. 6



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Fig. 7



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/10966

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H05B33/10, H05B33/14, C09K11/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H05B33/10, H05B33/14, C09K11/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1996-2002
Kokai Jitsuyo Shinan Koho 1971-2002 Jitsuyo Shinan Toroku Koho 1994-2002

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP 2000-150158 A (Daicel Chemical Industries, Ltd.), 30 May, 2000 (30.05.2000), Full text; Fig. 1 & WO 00/13470 A1 & EP 1043915 A	1-5,9-17 6-8
Y	JP 6-297457 A (Kanegafuchi Chem. Ind. Co., Ltd.), 25 October, 1994 (25.10.1994), Claims; column 2, lines 35 to 43; Fig. 2 (Family: none)	1-5,9-17
Y	JP 11-260549 A (Seiko Epson Corporation), 24 September, 1999 (24.09.1999), Claims; column 5, lines 26 to 29; Fig. 5 & WO 99/46961 A1	1-5,9-17
Y	JP 2000-256487 A (Japan Atomic Energy Research Institute), 19 September, 2000 (19.09.2000), Full text; Fig. 1 (Family: none)	1,3-5

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
06 February, 2002 (06.02.02)	19 February, 2002 (19.02.02)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No	Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/10966

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 11-302393 A (Japan Atomic Energy Research Institute), 02 November, 1999 (02.11.1999) (Family: none)	1
A	JP 59-123193 A (Nippon Seiki Co., Ltd.), 16 July, 1984 (16.07.1984) (Family: none)	1
A	JP 2000-33263 A (Japan Science and Technology Corp.), 02 February, 2000 (02.02.2000) (Family: none)	1
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Date: May 31, 2016

This attached set of pages comprises a CERTIFIED JAPANESE translation of the original ENGLISH language document. It has been independently translated according to translation industry practice. It is a true and accurate translation performed to the best of our ability.

Stan Lichtman, Director

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HAMAMATSU
EXHIBIT 1005

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Kokai Hei 06 (1994)-244444

(43) Date of Publication: September 2, 1994

(51) Int. Cl.[5]	Identification Symbols	JPO File Numbers	FI		Technical Indication Field
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G 02 B 5/00	Z	9224-2K			
H 01 L 31/10					
		7376-4M	H 01 L 31/04	F	
		8422-4M	31/10	Z	

Request for Examination: Not yet submitted Number of Claims: 10 OL (Total of 7 pages [in original])

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Continued on last page

(54) [Title of the Invention] LIGHT-CONFINING STRUCTURE AND LIGHT-RECEIVING ELEMENT USING THE SAME

(57) [Summary]

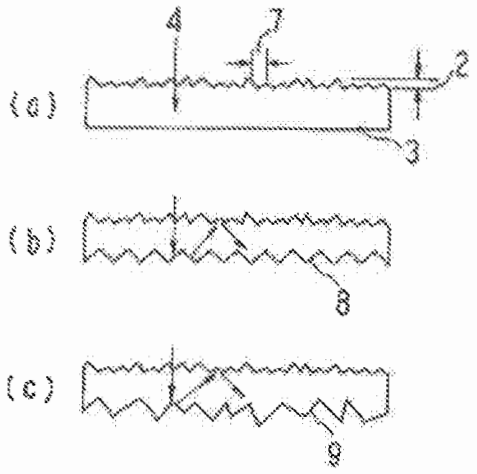
[Problem] To provide a light-confining structure which can reduce surface reflection and effectively confine light.

[Constitution] A transition layer 2 having depressions and projections is provided to the surface of a substrate 3. The repeating width 7 of these depressions and projections is set equal to or less than the wavelength of the main light 4 to be confined. It is preferable to provide the depressions and projections 8 and 9 on the rear surface of the substrate 3. The refractive index of the

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transition layer 2 is changed so as to approach the refractive index of the substrate from a side opposite the substrate toward the substrate.

Figure 7



2: transition layer
4: light
7: repeating width
8, 9: depressions and projections

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[Claim(s)]

[Claim 1]

A light-confining structure characterized by comprising a substrate and a transition layer having depressions and projections and is provided to the front surface of said substrate, the repeating width of said depressions and projections being equal to or less than the wavelength of a main light to be confined.

[Claim 2]

The light-confining structure cited in claim 1; said light-confining structure characterized by the refractive index of the above-mentioned transition layer being changed so as to approach the refractive index of the substrate from a side opposite the substrate toward the substrate.

[Claim 3]

The light-confining structure cited in claim 1; said light-confining structure characterized by the above-mentioned transition layer comprising a first substance part having depressions and projections disposed on the substrate side and a second substance part having depressions and projections in a reverse direction corresponding thereto and disposed on the side opposite to the substrate, the refractive index of the first substance being the same as the refractive index of the substrate or being closer to the refractive index of the substrate than to the refractive index of said second substance.

[Claim 4]

The light-confining structure cited in claim 3; said light-confining structure characterized by the shape of the above-mentioned depressions and projections being constituted so that the surface area of the above-mentioned second substance part occupied on a plane decreases from the front surface of the above-mentioned transition layer in the direction of the substrate.

[Claim 5]

The light-confining structure cited in claim 4; said light-confining structure characterized by the shape of the depressions and projections being constituted so that proportion of the decrease in the surface area of the above-mentioned second substance part occupied on a plane from the front surface of the above-mentioned transition layer in the direction of the substrate is larger close to the front surface than close to the rear surface of the transition layer.

[Claim 6]

The light-confining structure cited in claim 1; said light-confining structure characterized by the cross-sectional shape of the above-mentioned depressions and projections being substantially triangular.

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[Claim 7]

The light-confining structure cited in any one of claims 1 through 6; said light-confining structure characterized by the above-mentioned main light to be confined being visible light, and the repeating width of the above-mentioned depressions and projections being 1 μm or less.

[Claim 8]

The light-confining structure cited in any one of claims 1 through 7; said light-confining structure characterized by the above-mentioned substrate having second depressions and projections on the rear surface thereof, the depressions and projections having a larger repeating width than the wavelength of the main light to be confined.

[Claim 9]

The light-confining structure cited in any one of claims 1 through 8; said light-confining structure characterized by the above-mentioned substrate having a light-reflecting layer on the rear surface thereof.

[Claim 10]

A light-receiving element that uses the light-confining structure of any one of claims 1 through 7; said light-receiving element characterized by the above-mentioned substrate being a first electroconductive type, and having a second electroconductive region provided to the above-mentioned substrate and electrode that are connected thereto.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Application]

The present invention relates to a light-confining structure that is used in light-receiving devices, such as light sensors and photoelectric transducers; photo-optical transducers, such as photoexcitation lasers; or other devices, and to a light-receiving element using the same.

[0002]

[Prior Art]

When light is incident on a substrate and photo-optical conversion, photoelectrical conversion, or the like is performed, the light is effectively is captured within the substrate and this light is confined inside the substrate without escaping outside the substrate, whereby the efficiency of each above-mentioned conversion is increased. In order to perform this, a reduction in the reflectance of the light by the substrate surface and confining of the light incident inside the substrate are important.

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[0003]

The reflectance of the incident light reflected by the front surface of the substrate was conventionally reduced using depressions and projections on the front surface having a largeness of several tens of μm, an antireflection film, etc. In addition, as described in SID '89 Digest, pg. 270 (1989) and Japanese Patent Application No. Hei 3-54371, antireflection films making use of fine depressions and projections on the front surfaces that use fine SiO_2 or MgF_2 particles were used.

[0004]

[Problems to be Solved by the Invention]

The above-mentioned conventional method for using antireflection films had a problem in that the reflectance could not decrease substantially when the wavelength of the incident light extended over a wide range or the incident angle of the light changed. In addition, the method for using the depressions and projections on the front surface having a largeness of several tens of μm had a problem because when it was incident on the substrate, the light path was bent substantially by refraction. Hence, it was difficult to confine the light using the depressions and projections formed on the rear surface. In addition, because the refractive index of the substrate and the shape of the fine depressions and projections on the front surface were not considered when the antireflection film using fine depressions and projections on the front surface that used fine SiO_2 particles or the like, it was difficult for the reflectance to be made very low.

[0005]

An object of the present invention is to provide a light-confining structure that can reduce surface reflection and effectively confine light, and a light-receiving element using the same.

[0006]

[Means for Solving the Problems] In order to achieve the above object, the light-confining structure of the present invention is constituted so as to comprise a substrate and a transition layer having depressions and projections and provided to the front surface of the substrate, the repeating width of these depressions and projections are equal to or less than the wavelength of a main light to be confined.

[0007]

It is preferable that the refractive index of this transition layer change so as to approach the refractive index of the substrate from the reverse side of the substrate side toward the substrate. In this way, the refractive index changes continually in the substrate direction from outside the substrate, whereby a lower reflectance can be obtained over a wide wavelength range, as compared to an antireflection film using an interference thin-film formed from several layers.

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[0008]

In addition, it is preferable that this transition layer be composed of a first substance part having depressions and projections disposed on the substrate side and a second substance part having depressions and projections in a reverse direction corresponding thereto and disposed on the side opposite to the substrate, the refractive index of the first substance is the same as the refractive index of the substrate or is closer to the refractive index of the substrate than to the refractive index of the second substance. The first substance part may be formed using the substrate itself. For example, depressions and projections may be formed on the front surface of the substrate, or a part made of another substance may be attached to the front surface of the substrate. The second substance part may be air, or it may have a structure in which another substance is buried between the depressions and projections on the front surface of the substrate.

[0009]

It is preferable that the shape of these depressions and projections be constituted so that the surface area of the second substance part occupied on a plane decreases from the front surface of the above-mentioned transition layer in the direction of the substrate. The repeating width of the depressions and projections is 1 μm or less when the main light to be confined is visible light.

[0010]

In addition, the confining structure of the present invention can have second depressions and projections provided to the rear surface of the substrate, the second depressions and projections having a repeating width that is larger than the wavelength of the main light to be confined. Furthermore, a light reflection layer can be provided to the rear surface of the substrate.

[0011]

Furthermore, when the above-mentioned light-confining structure is used and the substrate is made a first electroconductive type, the light-receiving element of the present invention is constituted by providing a second electroconductive region that is an electroconductive type, which is reverse to the first electroconductive type to the substrate, and preferably, providing the first electroconductive region having an even higher density to the substrate and providing electrodes that are connected thereto.

[0012]

[Operation]

An operation of the present invention is described with reference to Figures 1 through 6. Figure 1(a) and (b) are a partial perspective view in the proximity of the front surface of the substrate, and a cross section thereof. When a repeating width 7 of the depressions and projections on the front surface of the substrate is smaller than the wavelength of the light when a light 4 is incident onto a substrate 3 from an external medium 1, this acts in the same optical manner as when the refractive index of the transition layer 2 changes continually from the front surface toward the

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substrate. That is to say, when the proportion of a second medium 5 and a first medium 6 changes gradually toward the substrate, as illustrated, the transition layer 2 is formed that is equivalent to a film having a refractive index that changes linearly, from the refractive index of the second medium 5 to the refractive index of the first medium 6.

[0013]

An aspect of the change in the refractive index within the transition layer is determined by how the first medium and the second medium are mixed. With a film composed of two kinds of media, the effective refractive indexes thereof are represented by an average of each medium. As illustrated in Figure 2(a), (b), (c), (d), (e), and (f), when the first medium 6 has a shape, such as a rectangle, triangular groove, pyramid, hemisphere, sphere, or an inverted pyramid, respectively, assuming the refractive index of the second medium 5 is set to 1.0 and the refractive index of the first medium 6 is set to 3.5, effective refractive indexes are provided, as shown in Figure 3.

[0014]

In addition, the calculated values of the reflectances for the pyramidal and spherical shapes are shown in Figure 4 when the refractive index of the external medium 1 is 1.0, the refractive index of the second medium 5 is 1.0, the refractive index of the first medium 6 is 3.5, and the refractive index of the substrate 3 is 3.5. Figure 4(a) and (b) illustrate the reflectances in the case of the pyramidal shape and Figure 4(c) and (d) show the reflectances in the case of a spherical shape using a linear scale and a logarithmic scale. The pyramidal shape exhibits a somewhat high reflectance when the thickness of the transition layer film is 40 nm, but it exhibits an extremely low reflectance when the film thickness is greater than this. At any thickness, the reflectance exceeds 10% on average when the shape is spherical, exhibiting a slightly higher reflectance than that of the pyramidal shape.

[0015]

In Figure 5 is shown a relationship between the amount of light absorption and the transition layer film thickness with the pyramidal shape. The calculated results are shown when the refractive index of the external medium 1 is set to 1.0, the refractive index of the first medium 6 is set to 3.5, the refractive index of the substrate 3 is set to 3.5, and the refractive indexes of the second medium 5 are set to 1.0 and 1.5. In any case, the amount of light absorption is high when the film thickness of the transition layer is about several hundred nm. When the film is thinner than this, nearly 100% of the light is absorbed.

[0016] In Figure 6 is shown a relationship between the amount of light absorption and the transition film thickness for each shape. Calculated results are shown when the refractive index of the external medium 1 is set to 1.0, the refractive index of the second medium 5 is set to 1.0, the refractive index of the first medium 6 is set to 3.5, and the refractive index of the substrate 3 is set to 3.5. The pyramidal shape provides the highest amount of light absorption at each film thickness, with respectively increasing absorption amounts being indicated up to the inverted pyramid. However, with the rectangle and the sphere, even when the transition layer film thickness is increased, the amount of light absorption does not increase that much. These results

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indicate that the amount of light absorption is high when the shape of the first medium is one where the curve inclines upward to the right in Figure 3. In addition, the pyramidal shape in particular had a downward projected curve as it inclined upward to the right in Figure 3 indicated good results. Hence, it was seen that the shape of the first medium 6 of this transition layer was preferably a shape having a larger proportion of a reduction in surface area of the second medium 5 in the substrate direction near the front surface of the transition layer 2 than the proportion of the reduction thereof near the rear surface of the transition layer 2, such as the pyramidal shape, a polyhedral pyramid, a cone, or a shape obtained by rotating the downward-projected line segment.

[0017]

A basic substrate shape is described with reference to Figure 7. As shown in Figure 7(a), the transition layer 2 comprising depressions and projections having a small repeating width 7 is provided to the top of the substrate. Accordingly the refractive index of the transition layer 2 changes continually, from the refractive index of the outside air to the refractive index of the substrate 3, from top to bottom. The light 4 that incidents on the substrate 3 from this transition layer is not reflected at all by the front surface of the substrate; it is incidented into the substrate. In addition, because the repeating width 7 is smaller than the wavelength of the incident light, the incidented light is not obliquely incidented by each slanted surface formed by the depressions and projections of the front surface of the substrate, but goes straight ahead to the rear surface of the substrate at the angle it was incidented.

[0018]

Depressions and projections 8 having a repeating width that is larger than the wavelength of the incident light and are periodic are formed, as in Figure 7(b), whereby the light reflected by the rear surface advances obliquely into the substrate and reaches the front surface of the substrate. At this time, when the angle of incidence is large than the critical angle, the light is totally reflected and proceeds into the substrate again. Thus, the light that incidented once is confined efficiently in the substrate 3. In addition, irregular depressions and projections 9 having a larger repeating width than the wavelength of the incident light are formed on the rear surface, as in Figure 7(c), whereby the light undergoes a scattered reflection by the rear surface. When the majority of the light reaches the front surface of the substrate, the light has a larger incident angle than the critical angle; hence, it is reflected again inside the substrate, and the incident light is efficiently confined by the substrate 3. In these configurations, light may be reflected more reliably by the rear surface by forming a reflector on the rear surface.

[0019]

[Working Examples]

<Working Example 1> A working example of the present invention is described with reference to Figure 8. In this working example, pyramids 11 having a regular width and largeness constituting the transition layer were formed on a silicon substrate 3 having a front surface with a (100) plane. These pyramids can be easily formed by masking the rear surface and etching only

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the front surface with an alkaline etchant. Microscopic pyramids 11 of 1 μm or less can be easily formed by etching using a heated aqueous solution composed mainly of ammonia and hydrazine as the etchant.'

[0020] The average size of the pyramids 11 on the front surface of the silicon substrate 3 obtained by the above process was approximately 0.3 μm according to a measurement using a scanning electron microscope (SEM). When the reflectance of the front surface of this silicon substrate was measured, the front surface reflectance substantially decreased in the wavelength range of 0.4 to 1.1 μm. In addition, when a film coating made of a thin oxide film was provided to the front surface of the silicon substrate 3, the change in the refractive index inside the transition layer 2 was steep, and further, the front surface reflectance decreased.

[0021]

<Working Example 2>

Another working example of the present invention is described with reference to Figure 9. In this working example, microscopic depressions and projections 11' having irregular largenesses and a cross section that mainly had a triangular shape were formed on the silicon substrate 3. The microscopic depressions and projections 11' were formed from a deposited film using chemical vapor phase formation (CVD). A material having a relative high refractive index and was transparent, such as ITO or ZnO_2, was used for the material of the film. The size of the microscopic depressions and projections 11' could be set to approximately 0.5 μm on average depending on the deposition rate, temperature, gas pressure, etc. In addition, a filler (not shown) was buried between the microscopic depressions and projections 11', to also serve as protection for the front surface. A material having a relatively small refractive index, such as SiO_2, was formed as this filler by a spin coating method, CVD method, or other method. The reflectance of the front surface of this silicon substrate substantially decreased in a wavelength range of 0.4 to 1.1 μm.

[0022]

<Working Example 3>

Yet another working example of the present invention is described with reference to Figure 10. In this working example, V-grooves 13 having a repeating width of 2 μm were formed on the rear surface of the silicon substrate 3 described according to Working Example 2. Accordingly, the light incident from the front surface was reflected by the rear surface, totally reflected when it reached the front surface again, and was confined inside the silicon substrate. The V-grooves 13 were easily formed by using an etching mask that used an ordinary photoresist. In this case, the mask is not required to be a photoresist mask; it may be a printed resist mask. A shape of the rear surface may be not only the V-shaped groove but also the inverse pyramid, a semicircle, or the like so long as the repeating width thereof may be a size larger than the wavelength of the incident light. In addition, a rear surface reflector 14 was formed thereon in order to increase the reflectance by the rear surface.

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[0023]

<Working Example 4>

Still another working example of the present invention is described with reference to Figure 11. In this working example, pyramid-shaped depressions and projections 15 were formed on the rear surface of the silicon substrate 3. Transparent glass was used for the material of the depressions and projections 15, which were adhered to the silicon substrate 3. Accordingly, a light-trapping structure could be easily formed without working the silicon substrate 3. And in the same manner as in Working Example 3, a rear surface reflector (not shown) was formed thereon.

[0024]

<Working Example 5>

A working example of the light-receiving element of the present invention is described with reference to Figure 12. As in Working Example 3, the microscopic depressions and projections 11' having an irregular size, wherein the cross section mainly had a triangular shape, were formed on a p-type silicon substrate 21 and V-grooves having a repeating width of 2 μm were formed on the rear surface. (The rear surface reflector shown in Working Example 3 was not formed thereon.) Next, a high-density p-type layer 19 and a high-density n-type layer 20 were formed thereon by a thermal diffusion method, a passivation oxide film 18 (an oxide film for the front surface is not shown) was provided to the front surface and rear surface of the p-type silicon substrate 21, holes were drilled in each of the oxide films 18 at prescribed positions, electrodes 16 and 17 were formed by vacuum vapor phase deposition, and the light-receiving element was formed. The photoelectric conversion efficiency of this light-receiving element was improved over that of a conventional light-receiving element which was not provided with a transition layer comprising the microscopic depressions and projections 11'.

[0025]

Moreover, although light-receiving element were formed in the same manner using the p-type silicon substrate having the transition layer with microscopic depressions and projections having shapes other than those stated above, i.e., a triangular groove, sphere, inverse pyramid, and rectangle, the photoelectric conversion efficiencies of all these elements were improved over that of a conventional light-receiving element.

[0026]

Although silicon was used as the substrate in the above working examples, needless to say the substrate may be any kind of substance besides silicon, such as monocrystal, polycrystal and porous monatomic and multicomponent semiconductors of gallium arsenide, indium phosphide, CuInS, CdS, and the like, and insulative materials, such as glass and plastic. In addition, the structure of the front surface depressions and projections and rear surface depressions and projections may be a combination of any of the structures described above. And needless to say,

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the cross-sectional shape of the depressions and projections may be the shape described according to Figure 2, and any regular or irregular shape similar thereto.

[0027]

[Effect of the Invention]

By using the structure of the present invention, light may be effectively confined when it is necessary to effectively confine light in light-receiving devices, such as light sensors and power reception conversion devices [TN: may be typo for photoelectric transducers]; photo-optical transducers, such as photoexcitation lasers; or other devices. In addition, the photoelectric conversion efficiency could be improved by the light-receiving element of the present invention that uses this light-confining structure.

[Brief Description of the Drawings]

[Figure 1] is a conceptual drawing explaining the principles of the present invention.

[Figure 2] is a conceptual drawing explaining the principles of the present invention.

[Figure 3] is a drawing showing an example of the calculated results for explaining the effect of the present invention.

[Figure 4] is a drawing showing an example of the calculated result for explaining the effect of the present invention.

[Figure 5] is a drawing showing an example of the calculated result for explaining the effect of the present invention.

[Figure 6] is a drawing showing an example of the calculated result for explaining the effect of the present invention.

[Figure 7] is a conceptual drawing explaining the principles of the present invention.

[Figure 8] is a cross-sectional schematic diagram of a working example of the light-confining structure of the present invention.

[Figure 9] is a cross-sectional schematic diagram of another working example of the light-confining structure of the present invention.

[Figure 10] is a perspective view of a working example of the light-confining structure of the present invention.

[Figure 11] is a perspective view of a working example of the light-confining structure of the present invention.

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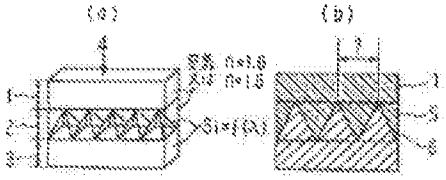
[Figure 12] is a perspective view of a working example of the light-receiving element of the present invention.

[Explanation of the Codes]

1: external medium; 2: transition layer; 3: substrate; 4: light; 5: second medium; 6: first medium; 7: repeating width; 8, 9, 15: depressions and projections; 11: pyramid; 11': microscopic depressions and projections; 13: V-groove; 14: rear surface reflector; 16, 17: electrodes; 18: oxide film; 19: high-density p-type layer; 20: high-density n-type layer; 21: p-type silicon substrate

[Figure 1]

Figure 1

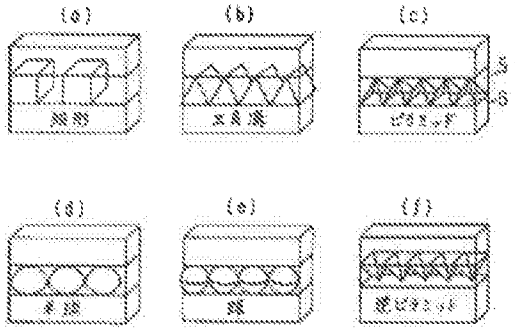


1: external medium; 2: transition layer; 3: substrate; 4: light; 5: second medium; 6: first medium

[Key]
a: air; n=1.0 or n=1.5

[Figure 2]

Figure 2

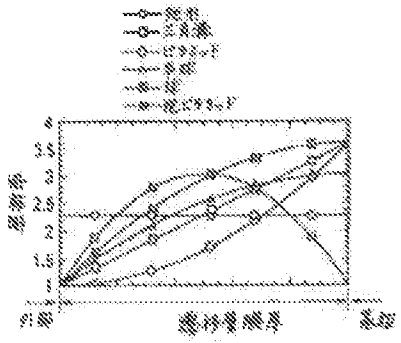


[Key] (a) rectangles; (b) triangular grooves; (c) pyramids; (d) hemispheres; (e) spheres; (f) inverted pyramids

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[Figure 3]

Figure 3

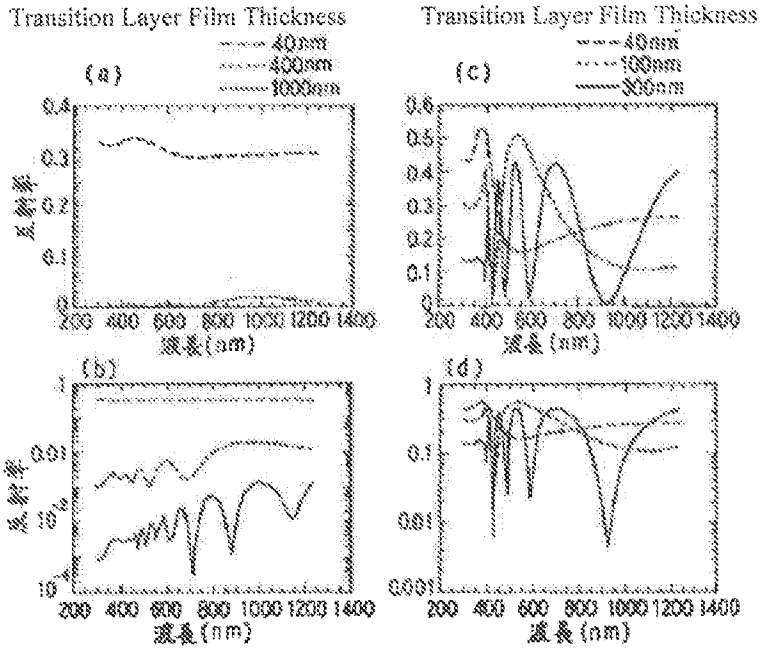


[Key]

—◇—: rectangle; —○—: triangular groove; —◇—: pyramid; —◡—: hemisphere; —●—: sphere; —▣—: inverted pyramid; Y-axis: Refractive Index; X-axis:: Outside / Transition Layer Film Thickness / Substrate

[Figure 4]

Figure 4



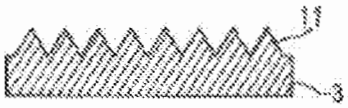
[Key]

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Y-axes: Reflectance; X-axes: Wavelength (nm)

[Figure 8]

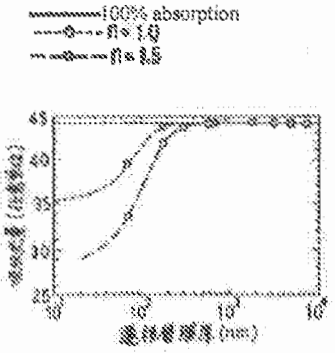
Figure 8



3: substrate; 11: pyramid

[Figure 5]

Figure 5



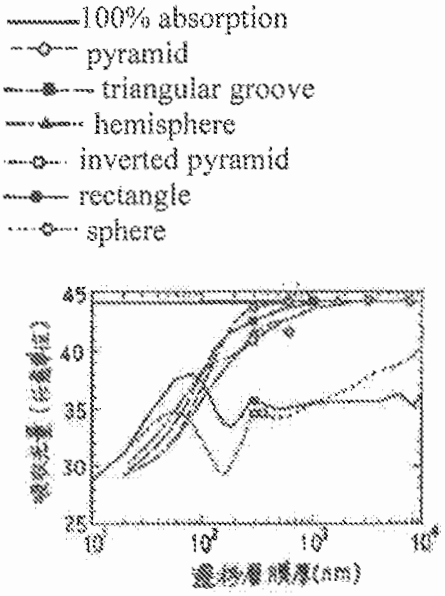
[Key]

Y-axis: Amount of Light Absorption (Arbitrary Unit); X-axis: Transition Layer Film Thickness (nm)

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[Figure 6]

Figure 6

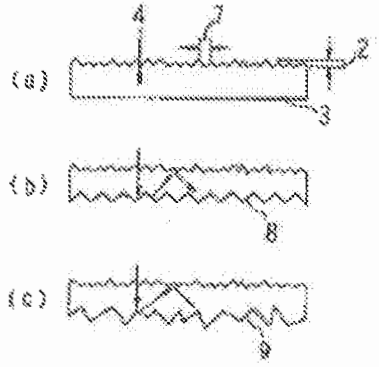


[Key]

Y-axis: Amount of Light Absorption (Arbitrary Unit); X-axis: Transition Layer Film Thickness (nm)

[Figure 7]

Figure 7

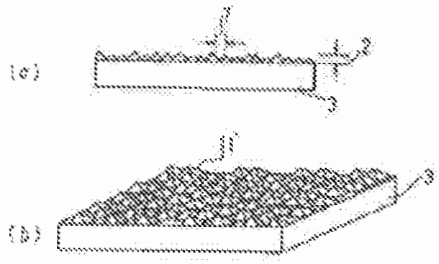


2: transition layer; 4: light; 7: repeating width; 8, 9: depressions and projections

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[Figure 9]

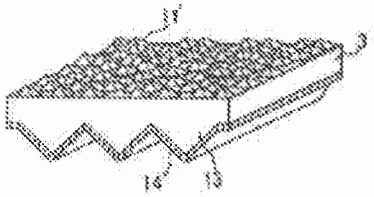
Figure 9



11': microscopic depressions and projections

[Figure 10]

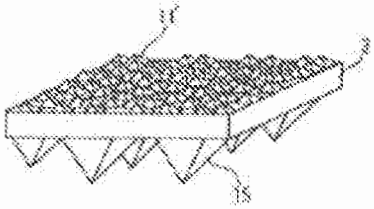
Figure 10



11': microscopic depressions and projections; 13: V-groove; 14: rear surface reflector

[Figure 11]

Figure 11

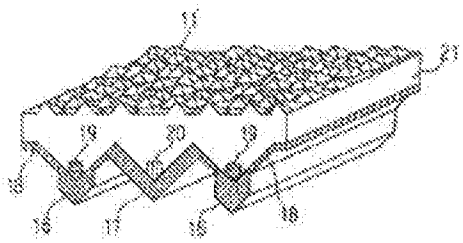


11': microscopic depressions and projections; 15: depressions and projections

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[Figure 12]

Figure 12



11': microscopic depressions and projection; 16, 17: electrodes; 18: oxide film; 19: high-density p-type layer; 20: high-density n-type layer; 21: p-type silicon substrate

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Continued from front page

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Espacenet

Bibliographic data: JP2002190386 (A) — 2002-07-05

MATERIAL FOR ORGANIC ELECTROLUMINESCENT ELEMENT, AND MANUFACTURING METHOD THEREOF

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Classification: - **international:** ***B01J19/12; H01L51/30; H01L51/50; H05B33/10; H01L51/00;*** (IPC1-7): B01J19/12; H05B33/10; H05B33/14
- **cooperative:** **H01L51/0013**; **H01L51/5012**; H01L2251/308; H01L51/0042; H01L51/005; H01L51/0071; H01L51/0073; H01L51/5036; H01L51/5048

Application number: JP20000387823 20001220

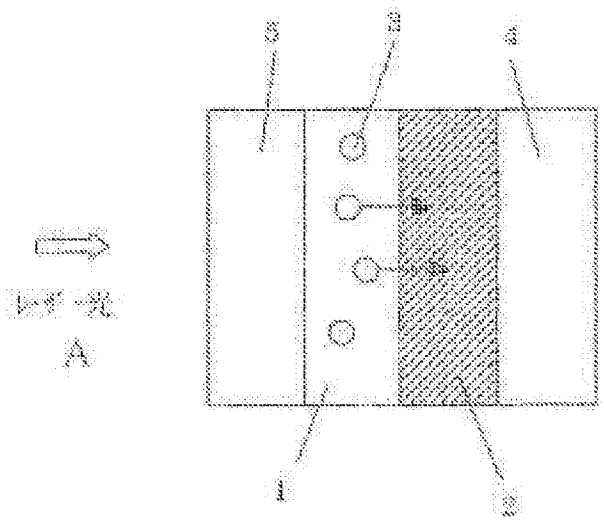
Priority number (s): JP20000387823 20001220

Also published as: WO0251212 (A1)

Abstract of JP2002190386 (A)

PROBLEM TO BE SOLVED: To provide a material for an organic EL element, together with its manufacturing method, wherein fine patterning is allowed, as well as an organic EL element using them. SOLUTION: With a laser beam being irradiated, an emission center forming compound 3 constituting a source 1 is injected into a target 2, having at least one function selected out of an electron transport function and a hole transport function, to manufacture the material for the organic electroluminescent element comprising an emission center. In this method, the laser beam is shifted at least relative to the target for irradiation, to form the emission center at a prescribed pattern. The source and the target which is brought into with each other may be shifted relative to the laser beam, to form the emission center at the prescribed pattern.

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A...LASER BEAM

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Ｈ０５Ｂ　33/14		Ｈ０５Ｂ　33/14	Ｂ	

審査請求　未請求　請求項の数14　ＯＬ　（全 10 頁）

(21)出願番号　特願2000－387823(P2000－387823)

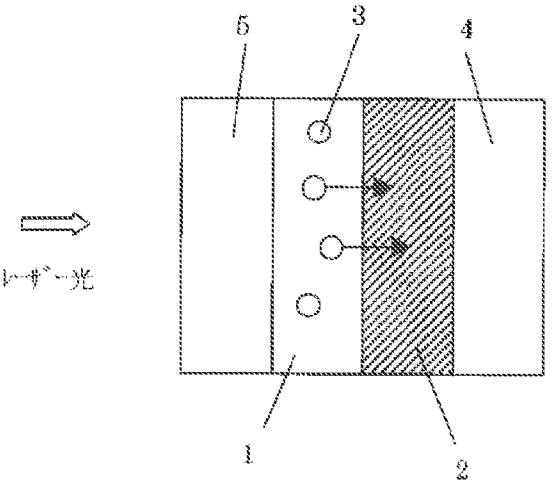
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4G075 AA30 AA62 BB03 BB05 BD14 CA36

(54)【発明の名称】　有機エレクトロルミネッセンス素子用材料およびその製造方法

(57)【要約】
【課題】　微細なパターニングが可能な有機ＥＬ素子用材料およびその製造方法、ならびにそれらを用いた有機ＥＬ素子を提供する。
【解決手段】　レーザー光を照射して、電子輸送機能およびホール輸送機能から選択された少なくとも１つの機能を有するターゲット２に、ソース１を構成する発光中心形成化合物３を注入して、発光中心を有する有機エレクトロルミネッセンス素子用材料を製造する。この方法は、レーザー光を少なくともターゲットに対して相対的に移動させて照射し、所定のパターンに発光中心を形成する。また、互いに接触したソースとターゲットとをレーザー光に対して移動させて、所定のパターンに発光中心を形成してもよい。



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【特許請求の範囲】

【請求項１】　レーザー光を照射して、電子輸送機能およびホール輸送機能から選択された少なくとも１つの機能を有するターゲットに、ソースを構成する発光中心形成化合物を注入して、発光中心を有する有機エレクトロルミネッセンス素子用材料を製造する方法であって、レーザー光を少なくともターゲットに対して相対的に移動させて照射し、所定のパターンに発光中心を形成する製造方法。

【請求項２】　互いに接触したソースとターゲットとをレーザー光に対して移動させて、所定のパターンに発光中心を形成する請求項１記載の製造方法。

【請求項３】　導波路を介して、レーザー光を照射する請求項１記載の製造方法。

【請求項４】　光ファイバを用いて、レーザー光を照射する請求項１記載の製造方法。

【請求項５】　レーザー光をターゲットに対して相対的に移動させて照射するとともに、レーザー光に対してソースを移動させて、発光中心を形成する請求項１記載の製造方法。

【請求項６】　ソースのアブレーション閾値以下の強度でレーザー光を照射する請求項１記載の製造方法。

【請求項７】　レーザー光がパルスレーザー光である請求項１記載の製造方法。

【請求項８】　パルス周期に同期させて、レーザー光をターゲットに対して相対的に移動させる請求項７記載の製造方法。

【請求項９】　ターゲットが、有機高分子である請求項１記載の製造方法。

【請求項１０】　ターゲットが、電子輸送機能およびホール輸送機能から選択された少なくとも１つの機能を有する化合物と、被膜形成能を有する有機高分子とで構成されている請求項１記載の製造方法。

【請求項１１】　化合物が、電子輸送機能を有するオキサジアゾール誘導体及びホール輸送機能を有する芳香族第３級アミン類から選択された少なくとも１種の化合物である請求項１０記載の製造方法。

【請求項１２】　請求項１記載の方法により得られた有機エレクトロルミネッセンス素子用材料。

【請求項１３】　一対の電極と、この一対の電極間に介在する請求項１２記載の有機エレクトロルミネッセンス素子用材料とで構成された有機エレクトロルミネッセンス素子。

【請求項１４】　一対の電極間に、請求項１２記載の有機エレクトロルミネッセンス素子用材料で構成された単層が介在している請求項１３記載の有機エレクトロルミネッセンス素子。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、レーザーを用いた

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分子注入により、発光中心形成化合物を注入して有機エレクトロルミネッセンス素子用材料を製造する方法、およびその方法により得られた有機エレクトロルミネッセンス素子用材料、ならびにその有機エレクトロルミネッセンス素子用材料を用いた有機エレクトロルミネッセンス素子に関する。

【０００２】

【従来の技術】従来、エレクトロルミネッセンス素子（以下、ＥＬ素子という場合がある）は、使用する材料により無機ＥＬ素子と有機ＥＬ素子とに分類されている。無機蛍光体分子を使用する無機ＥＬ素子は、一部実用化されており、時計のバックライトなどに使用されている。一方、有機ＥＬ素子は、無機ＥＬ素子に比べ、高輝度、高効率、ならびに高速応答性などの点で優れているため、その実用化が期待されている。

【０００３】エレクトロルミネッセンス素子は、電子輸送機能、ホール輸送機能、そして発光中心形成機能を有する化合物によって構成されている。その構造としては、１つの層が上記機能を全て備えた単層タイプ、異なる層が各機能を備えている多層タイプなどが報告されている。その発光原理は、一対の電極から注入された電子またはホールが発光層内で再結合して励起子を生成し、それが発光層を構成する発光材料分子を励起することに基づくと考えられている。

【０００４】各層を構成する化合物としては、発光効率の高い低分子量化合物や物理的強度が高い高分子化合物などが使用されている。低分子量化合物を使用した場合、蒸着法により膜形成を行うのに対し、高分子化合物の場合には、溶液塗布により膜形成を行う場合が多い。

【０００５】特開平８－９６９５９号公報および特開平９－６３７７０号公報には、電子輸送機能とホール輸送機能とを有する高分子バインダー中に、複数種の蛍光色素を分散させてなる単層発光層を備えた有機ＥＬ素子が開示されている。これらの有機ＥＬ素子は、各発光化合物が単独で発光し、全体として白色光を呈することが報告されている。また、多層構造の有機ＥＬ素子に比べ、その発光強度が低下し難い。

【０００６】これらの有機ＥＬ素子は、特定の溶媒に、高分子バインダーと蛍光色素とを分散させて基板に塗布する溶液塗布法により膜形成を行うため、微細なパターニング、特に、多色パターニング（フルカラー化）が困難である。

【０００７】多色パターニング方法としては、カラーフィルター法や色変換法、T.R.Hebnerらのインクジェット法(Appl.Phys.Lett.72,5(1998)p.519)、城戸らによるフォトブリーチング法などが報告されている。

【０００８】しかし、カラーフィルター法や色変換法では、発光層のパターニングを必要としないという利点があるものの、フィルターを通すため変換効率が低下する。インクジェット法においては、インクジェットによ

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り形成されたパターンは、中心が高くなる円錐型であり、表面の平滑性に劣るため、均一に電極を形成するのが困難である。また、断面パターンは四角形が理想とされるが、インクジェット法では円形となる。さらに、パターンの大きさが、乾燥条件や溶液の濃度に大きく依存する。フォトブリーチング法では、ＵＶ酸化により蛍光を失う特殊な発光中心化合物のみが使用可能であり、表現できる色が制限される。

【０００９】このように、従来の溶液塗布による製膜法では、物理的強度の高い高分子化合物の使用が可能であるが、微細なパターニングが困難である。また、上記のパターニング方法においても、使用できる化合物が制限されるばかりか、有機ＥＬ素子に適した表面平滑性を備えたフィルムを得ることができない。

【００１０】なお、分子注入法として、特開平６－２９７４５７号公報には、機能性材料又は機能性材料を含む固体材料（Ａ）と機能性成分が注入される固体材料（Ｂ）とを対置させ、これらにパルスレーザーを照射することにより、機能性成分を固体材料（Ｂ）に注入する方法が開示されている。この文献には、レーザーの照射位置を調整することによって、機能性成分の注入位置をコントロールできることが記載されている。

【００１１】また、特開平８－１０６００６号公報には、有機高分子化合物中にパルスレーザー光を吸収し得る色素が分散されたソースフィルムと、パルスレーザーが透過し得る有機高分子化合物からなるターゲットフィルムとを密着させて、ソースフィルムのアブレーション閾値以下の強度でパルスレーザー光をターゲットフィルム側から照射して色素をターゲットフィルム内に注入する方法が開示されている。この文献には、分子注入法が表示用カラーフィルター作成などに利用できることが記載されている。また、この文献には、レーザーのスポット位置やソースフィルムとターゲットフィルムを移動させて画像を形成できることが記載されており、実施例では試料を平行移動させて直線状の像を形成させている。

【００１２】ＷＯ００／１３４７０号には、レーザー光を吸収可能な発光中心形成化合物を含むソースと、電子輸送機能及び／又はホール輸送機能を有するターゲットとを接触させて、ソースのアブレーション閾値以下の強度でパルスレーザー光を照射して発光中心形成化合物をターゲット内に注入し、有機エレクトロルミネッセンス素子用材料を製造する方法が開示されている。

【００１３】

【発明が解決しようとする課題】従って、本発明の目的は、ＥＬ素子用材料として高分子化合物を使用する場合であっても微細パターニングが可能で、かつ簡便に効率よく発光中心形成化合物を注入できる有機ＥＬ素子用材料（特に有機ＥＬ素子用フィルム）およびその製造方法を提供することにある。

【００１４】本発明の他の目的は、表面平滑性に優れ、電極との接触性が良好な有機ＥＬ素子用材料およびそれを用いた有機ＥＬ素子を提供することにある。

【００１５】

【課題を解決するための手段】本発明者らは、前記課題を達成するため鋭意検討の結果、発光中心形成化合物で構成されたソースを用いる分子注入法において、レーザー光をターゲットに対して相対的に移動させることによって、微細なパターニングが簡単に効率よく行えることを見いだし、本発明を完成した。

【００１６】すなわち、本発明の有機ＥＬ素子用材料の製造方法は、レーザー光を照射して、電子輸送機能およびホール輸送機能から選択された少なくとも１つの機能を有するターゲットに、ソースを構成する発光中心形成化合物を注入して、発光中心を有する有機エレクトロルミネッセンス素子用材料を製造する方法であって、レーザー光を少なくともターゲットに対して相対的に移動させて照射し、所定のパターンに発光中心を形成する。また、互いに接触したソースとターゲットとをレーザー光に対して移動させて、所定のパターンに発光中心を形成してもよい。導波路を介して、レーザー光を照射してもよい。光ファイバを用いて、レーザー光を照射してもよい。レーザー光をターゲットに対して相対的に移動させて照射するとともに、レーザー光に対してソースを移動させて、発光中心を形成してもよい。ソースのアブレーション閾値以下の強度でレーザー光を照射してもよい。レーザー光はパルスレーザー光であってもよく、パルス周期に同期させて、レーザー光をターゲットに対して相対的に移動させてもよい。ターゲットは、有機高分子であってもよい。ターゲットは、電子輸送機能およびホール輸送機能から選択された少なくとも１つの機能を有する化合物と、被膜形成能を有する有機高分子とで構成されていてもよい。前記化合物が、電子輸送機能を有するオキサジアゾール誘導体及び／又はホール輸送機能を有する芳香族第３級アミン類であってもよい。

【００１７】本発明には、上記製造方法により得られた有機ＥＬ素子用材料、およびその有機ＥＬ素子用材料を用いた有機ＥＬ素子も含まれる。

【００１８】

【発明の実施の形態】[ソース(A)]ソースは、少なくとも発光中心形成化合物を含んでいればよく、発光中心形成化合物単独又は発光中心形成化合物とバインダーとで構成されていてもよい。

【００１９】[発光中心形成化合物]発光中心形成化合物としては、有機ＥＬ素子用の発光中心化合物としての機能を有し、レーザー光を吸収し得る化合物、特に電子及び／又はホール（正孔）によって励起されて発光する化合物が使用できる。発光中心形成化合物としては、例えば、２，５－ビス（５－tert－ブチル－２－ベンゾオキサゾイル）－チオフェンなどのビス（C_{1-6} アルキル－ベンゾオキサゾイル）チオフェン、ナイルレッド、クマ

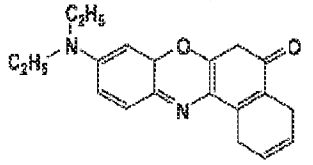
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リン６、クマリン７などのクマリン類、４－（ジシアノメチレン）－２－メチル－６－（ｐ－ジメチルアミノスチリル）－４Ｈ－ピランなどの４－（ジシアノC_{1-4}アルキレン）－２－C_{1-4}アルキル－６－（ｐ－ジC_{1-4}アルキルアミノスチリル）－４Ｈ－ピラン、キナクリドンなどの酸素原子、窒素原子及び硫黄原子から選択された少なくとも１種のヘテロ原子を含む複素環化合物；ルブレン、ペリレンなどの縮合多環式炭化水素；１，１，４，４－テトラフェニル－１，３－ブタジエン（ＴＰＢ）などのテトラC_{6-12}アリール－１，３－ブタジエン；１，４－ビス（２－（４－エチルフェニル）エチニル）ベンゼン＊などのビス（２－（４－C_{1-4}アルキルフェニル）C_{2-4}アルキニル）ベンゼン；４，４’－ビス（２，２’－ジフェニルビニル）ビフェニルなどのビス（２，２’－ジC_{6-12}アリールビニル）ビフェニルなどが挙げられる。特に、これらの中でナイルレッド、クマリン６が好ましい。

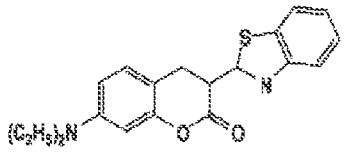
【００２０】ナイルレッドとクマリン６の構造を以下に示す。

【００２１】

【化１】



ナイルレッド



クマリン６

【００２２】ナイルレッドの発光波長は、５８０nm（赤色発光）、クマリン６の発光波長は４９０nm（緑色発光）である。

【００２３】これらの発光中心形成化合物は、単独で又は２種以上組み合わせて使用してもよい。

【００２４】［バインダー］バインダーとしては、通常、皮膜形成能を有する樹脂（熱可塑性樹脂、熱硬化性樹脂）が使用できる。

【００２５】熱可塑性樹脂としては、例えば、ポリエチレン、ポリプロピレン、エチレン－プロピレン共重合体、ポリブテンなどのオレフィン系樹脂；ポリスチレン、ゴム変性ポリスチレン（ＨＩＰＳ）、アクリロニトリル－スチレン共重合体、アクリロニトリル－ブタジエン－スチレン共重合体などのスチレン系樹脂；アクリル系樹脂［（メタ）アクリル系単量体（例えば、メチル（メタ）アクリレート、エチル（メタ）アクリレート、ブチル（メタ）アクリレートなどのC_{1-6}アルキル（メタ）アクリレート、ヒドロキシエチル（メタ）アクリレート、ヒドロキシプロピル（メタ）アクリレートなどのヒドロキシC_{2-4}アルキル（メタ）アクリレート、グリシジル（メタ）アクリレート、（メタ）アクリル酸、（メタ）アクリロニトリルなど）の単独または共重合体、前記（メタ）アクリレート系単量体と共重合性単量体（例えば、スチレンなどの芳香族ビニル単量体など）との共重合体（メチルメタクリレート－スチレン共重合体など）］；ポリビニルアルコール、エチレン－ビニルアルコール共重合体などのビニルアルコール系重合体、ポリ塩化ビニル、塩化ビニル－酢酸ビニル共重合体、ポリ塩化ビニリデン、ポリ酢酸ビニル、エチレン－酢酸ビニル共重合体、ポリビニルアセチルなどのビニル系樹脂；６－ナイロン、６，６－ナイロン、６，１０－ナイロン、６，１２－ナイロンなどのポリアミド系樹脂；ポリエステル樹脂［例えば、ポリアルキレンテレフタレート（ポリエチレンテレフタレート、ポリブチレンテレフタレートなど）、ポリアルキレンナフタレートなどのアルキレンアリレート系樹脂又はアルキレンアリレートコポリエステル樹脂］；フッ素系樹脂；ポリカーボネート；ポリアセタール；ポリフェニレンエーテル；ポリフェニレンスルフィド；ポリエーテルスルホン；ポリエーテルケトン；熱可塑性ポリイミド；熱可塑性ポリウレタン；ノルボルネン系ポリマーなどが挙げられる。

【００２６】熱硬化性樹脂としては、フェノール樹脂、アミノ樹脂（尿素樹脂、メラミン樹脂など）、熱硬化性アクリル樹脂、不飽和ポリエステル樹脂、アルキド樹脂、ジアリルフタレート樹脂、エポキシ樹脂、シリコーン樹脂などが挙げられる。

【００２７】これらのバインダーは、単独でまたは二種以上組合わせて使用してもよい。

【００２８】ソース中の発光中心形成化合物の含有量は、特に制限されず、０．１～１００重量％、好ましくは１～９０重量％、さらに好ましくは５～８０重量％程度である。また、ソースを発光中心形成化合物とバインダーとで構成する場合、発光中心形成化合物の含有量は、特に制限されないが、例えば、バインダー１００重量部に対して、０．１～６０重量部、好ましくは１～３０重量部、さらに好ましくは３～２０重量部程度である。

【００２９】ソースは、通常、フィルムの形態で使用される。また、ソースは、基板又はターゲット上に形成された前記発光中心形成化合物単独又は発光中心形成化合物とバインダーとの被膜であってもよい。基板としては、ソース側からレーザー光を照射する場合、レーザー光を透過可能な程度に透明であればよく、例えば、ソーダガラス、無アルカリガラス、石英ガラスなどのガラス板、あるいはポリエステル、ポリスチレン、アクリル系樹脂、ビニル系樹脂（ポリビニルアセタールなど）、ポ

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リスルホン、ポリエーテルスルホンなどの高分子シートまたはフィルムなどが挙げられる。

【００３０】ソースフィルムの製造方法は、特に制限されず、慣用の方法（例えば、蒸着法（真空蒸着法など）などの乾式法、スピンコーティング、ディップコーティング、ダイコーティングなどの溶媒を使用する湿式コーティング法など）などが挙げられる。なお、慣用のフィルム製造方法（例えば、流延法、押出法など）によりフィルムを形成してもよい。

【００３１】ソース被膜（塗膜）を形成するためのコーティング剤（塗布液）には、必要により、溶媒（例えば、水；メタノール、エタノールなどのアルコール類；酢酸エチル、酢酸イソブチルなどのエステル類；アセトン、メチルエチルケトンなどのケトン類；トルエンなどの芳香族炭化水素類；シクロヘキサンなどの脂環式炭化水素類；クロロホルム、クロロベンゼンなどのハロゲン化炭化水素類；エーテル類；セロソルブ類；カルビトール類など）などを使用してもよい。フィルム（又は被膜）の厚みは、特に制限されないが、０．０１～５０μｍ、好ましくは０．１～３０μｍ、さらに好ましくは０．５～２０μｍ程度であってもよい。

【００３２】また、ソースは、パターンに形成されていなくてもよいが、それ自身が所定のパターンに形成されていてもよく、基板（基材）又はターゲット上に、必要によりパターンを形成した被膜をソースとして用いてもよい。例えば、発光中心形成化合物を含むフィルム又はシートを打ち抜きなどの方法によりパターン形成し、ソースを得てもよい。また、基板としては、レーザー光を透過可能な程度に透明であればよく、例えば、ソーダガラス、無アルカリガラス、石英ガラスなどのガラス板、あるいはポリエステル、ポリスチレン、アクリル系樹脂、ビニル系樹脂（ポリビニルアセタールなど）、ポリスルホン、ポリエーテルスルホンなどの高分子シートまたはフィルムなどが挙げられる。

【００３３】ソースのパターンに形成する場合、パターンとしては、所望の用途に応じて選択され、例えば、一次元パターン［ドット状（点状）、線状（例えば、平行線、ランダム、格子状など）］、二次元パターン［平面形状（例えば、円状、楕円状、三角形、四角形などの多角形状、星型など）］のいずれであってもよい。基板上に所定のパターンを形成する方法としては、例えば、スクリーン印刷などの印刷、インクジェット法、溶融転写又は熱転写法、マスキングと組み合わせて行われる蒸着法（昇華印刷）により基板又はターゲット上に所定のパターンを形成できる。

【００３４】［ターゲット(B)］ターゲットは、電子輸送機能およびホール輸送機能から選択された少なくとも１つの機能を有していれば、特に制限されず、(I)電子輸送機能およびホール輸送機能から選択された少なくとも１つの機能を有する樹脂、又は（II)電子輸送機能およびホール輸送機能を備えていない樹脂に、電子輸送機能およびホール輸送機能から選択された少なくとも１つの機能を付与した樹脂組成物であってもよい。(I)及び(II)に使用される樹脂としては、被膜形成能を有する樹脂（バインダー）が好ましい。また、ターゲット側からレーザー光を入射する場合、ターゲットはレーザー光を透過可能である。

【００３５】前記電子輸送機能及びホール輸送機能から選択された少なくとも１つの機能を有する樹脂(I)としては、例えば、ポリフェニレンビニレン類［例えば、ポリフェニレンビニレン、ポリ（２，５－ジメトキシフェニレンビニレン）、ポリナフタレンビニレンなどの置換基（C_{1-10} アルコキシ基など）を有していてもよいC_{6-12} アリーレンビニレンの単独又は共重合体］；ポリフェニレン類（特に、ポリパラフェニレン類）［例えば、ポリパラフェニレン、ポリ２，５－ジメトキシパラフェニレンなどの置換基（C_{1-10} アルコキシ基など）を有していてもよいフェニレンの単独又は共重合体］；ポリチオフェン類［ポリ（３－アルキルチオフェン）などのポリC_{1-20} アルキルチオフェン類、ポリ（３－シクロヘキシルチオフェン）などのポリC_{5-20} シクロアルキルチオフェン類、ポリ（３－（４－ｎ－ヘキシルフェニル）チオフェン）などの置換基（C_{1-10} アルキル基）を有していてもよいC_{6-20} アリールチオフェン類の単独又は共重合体］；ポリC_{1-20} アルキルフルオレンなどのポリフルオレン類；ポリ－Ｎ－ビニルカルバゾール（ＰＶＫ）、ポリ－４－Ｎ，Ｎ－ジフェニルアミノスチレン、ポリ（Ｎ－（ｐ－ジフェニルアミノ）フェニルメタクリルアミド）、ポリ（Ｎ，Ｎ’－ジフェニル－Ｎ，Ｎ’－ビス（３－メチルフェニル）－１，１’－ビフェニル－４，４’－ジアミノメタクリルアミド）（ＰＴＰＤＭＡ）、ポリ－４－（５－ナフチル－１，３，４－オキサジアゾール）スチレンなどの主鎖又は側鎖にホール輸送機能基及び電子輸送機能基から選択された少なくとも１種の機能基を有するビニル系重合体；ポリメチルフェニルシランなどのポリC_{1-4} アルキルフェニルシラン；芳香族アミン誘導体を側鎖または主鎖に有する重合体；またはこれらの共重合体などが挙げられる。これらの樹脂は、単独で又は二種以上組み合わせて使用してもよい。好ましいターゲットとしては、ポリ－Ｎ－ビニルカルバゾール又はＮ－ビニルカルバゾールを主成分（５０重量％以上、好ましくは６０～９８重量％程度）として含む共重合体、芳香族アミン誘導体を側鎖または主鎖に有する重合体などが挙げられる。

【００３６】ＰＶＫは，非晶質で、耐熱性に優れている（ガラス転移温度Ｔｇ：２２４℃）。上記ＰＶＫの重合度は、特に制限されないが，例えば、２００～５０００（例えば、３００～３０００）、好ましくは５００～２０００（例えば、５００～１５００）程度である。

【００３７】さらに、必要に応じて、上記樹脂（I)に電

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子輸送機能又はホール輸送機能を付与してもよい。

【００３８】電子輸送機能を有する化合物としては、例えば、オキサジアゾール誘導体［例えば、２－（４－ビフェニル）－５－（４－tert－ブチルフェニル）－１，３，４－オキサジアゾール（ＰＢＤ）、２，５－ビス（１－ナフチル）－１，３，４－オキサジアゾール（ＢＮＤ）、１，３－ビス［５－（４－tert－ブチルフェニル）－１，３，４－オキサジアゾール］ベンゼン（ＢＰＯＢ）、１，３，５－トリス［５－（４－tert－ブチルフェニル）－１，３，４－オキサジアオール］ベンゼン（ＴＰＯＢ）、１，３，５－トリス［５－（１－ナフチル）－１，３，４－オキサジアゾール］ベンゼン（ＴＮＯＢ）などの置換基を有していてもよいC_{6-20}　アリール基を有するオキサジアゾール誘導体］；ジフェノキノン類［例えば、３，５，３’，５’－テトラキス－tert－ブチルジフェノキノンなどの置換基（C_{1-10}　アルキル基など）を有していてもよいジフェノキノン類；１，２，３，４，５－ペンタフェニル－１，３－シクロペンタジエン（ＰＰＣＰ）；トリス(８－キノリノラト)アルミニウム(III)錯体、ビス（ベンゾキノリノラト）ベリリウム錯体、トリス（１０－ヒドロキシベンゾ[h]キノリラート）ベリリウム錯体などのキノリン酸錯体が挙げられる。特に、ＰＢＤが好ましい。

【００３９】ホール輸送機能を有する化合物としては、例えば、Ｎ，Ｎ’－ジフェニル－Ｎ，Ｎ’－ビス（３－メチルフェニル）－１，１’－ビフェニル－４，４’－ジアミン（ＴＰＤ）、Ｎ，Ｎ’－ジフェニル－Ｎ，Ｎ’－ビス（１－ナフチル）－１，１’－ビフェニル－４，４’－ジアミン（ＮＰＤ）、１，１－ビス[(ジ－４－トリルアミノ)フェニル]シクロヘキサン、Ｎ，Ｎ，Ｎ’，Ｎ’－テトラ（３－メチルフェニル）－１，３－ジアミノベンゼン（ＰＤＡ）、４，４’，４”－トリス（３－メチルフェニルフェニルアミノ）トリフェニルアミン（ｍ－ＭＴＤＡＴＡ）、４，４’，４”－トリス（１－ナフチルフェニルアミノ）トリフェニルアミン（１－ＴＮＡＴＡ）、４，４’，４”－トリス（２－ナフチルフェニルアミノ）トリフェニルアミン（２－ＴＮＡＴＡ）、４，４’，４”－トリ（Ｎ－カルバゾリル）トリフェニルアミン（ＴＣＴＡ）、１，３，５－トリス［４－（３－メチルフェニルフェニルアミノ）フェニル］ベンゼン（ｍ－ＭＴＤＡＰＢ）、トリフェニルアミンなどの芳香族第３級アミン類；フタロシアニン類などが挙げられる。

【００４０】前記化合物は、単独で又は二種以上組み合わせて使用してもよい。なお、これらの化合物のうち、電子及び／又はホールにより励起され発光する化合物は、発光中心形成化合物として使用してもよい。

【００４１】樹脂(I)（例えば、ＰＶＫ)中に含まれる上記成分の割合は、有機ＥＬ素子用材料としての機能を損なわない範囲で選択でき、例えば、樹脂(I)１００重量部に対して、１０～３００重量部、好ましくは２０～２００重量部程度である。

【００４２】ターゲットが、樹脂(I)と前記化合物とで構成されている場合、後述する有機ＥＬ素子において、単層構造が可能となり、発光効率が向上するばかりか、経済的にも有利である。

【００４３】樹脂組成物（II)で使用される樹脂としては、特に制限されないが、例えば、前記例示の被膜形成能を有する種々のバインダー（熱可塑性樹脂や熱硬化性樹脂など）が使用できる。これらの樹脂に、電子輸送機能およびホール輸送機能のうち少なくとも１つの機能を付与してもよい。電子輸送機能及び／又はホール輸送機能を付与するために使用される化合物としては、上記と同様の化合物が挙げられる。

【００４４】電子輸送機能またはホール輸送機能を有する化合物の添加量は、バインダー樹脂１００重量部に対して、１０～３００重量部（例えば、１０～２００重量部）、好ましくは２０～１００重量部（例えば、２０～８０重量部）程度である。

【００４５】また、上記樹脂(I)および樹脂組成物(II)を組み合わせて使用してもよく、さらに、電子輸送機能およびホール輸送機能のうち少なくとも１つの機能を付与してもよい。

【００４６】なお、ターゲットの形態は、特に制限されないが、通常、フィルムの形態で使用される。また、ターゲットは、前記ソースと同様の方法で形成され、通常、前記例示の基板上に形成される。

【００４７】［有機ＥＬ素子用材料の製造方法（分子注入法）］本発明の有機ＥＬ素子用材料の製造方法は、レーザー光を照射して、前記ターゲットに、ソース中の発光中心形成化合物を注入する方法であり、レーザー光を少なくともターゲットに対して相対的に移動させることによって、所定のパターンに発光中心を形成する。レーザー光は、ソース(A)側又はターゲット(B)側から照射してもよい。ターゲットとしては、通常、フィルムを用い、有機ＥＬ素子用フィルムを製造する。また、ターゲットとソースは接触していてもよい。

【００４８】本発明に使用されるレーザー光としては、使用する発光中心形成化合物の種類によって異なるが、例えば、波長として１９０～１１００ｎｍの範囲の発振波長を有するレーザー光が挙げられる。パルスレーザー光を使用した場合、周波数は、例えば、０．５～５０Ｈｚ、好ましくは０．５～３０Ｈｚ程度である。また、パルス幅は、レーザー光の波長などによって異なるが、１０ｐｓ～１０μｓ（例えば、１０ｐｓ～１μｓ）、好ましくは５０ｐｓ～１００ｎｓ（例えば、１００ｐｓ～５０ｎｓ）程度である。パルス幅が短いほど、発光中心形成化合物の分解などを抑制でき、損傷を受け難い。

【００４９】レーザー光源としては、例えば、気体レーザー［ＡｒＦエキシマーレーザー（１９３ｎｍ）、Ｋｒ

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Ｆエキシマーレーザー（２４８ｎｍ）、ＸｅＣｌエキシマーレーザー（３０８ｎｍ）、ＸｅＦエキシマーレーザー（３５１ｎｍ）、窒素レーザー（３３７ｎｍ）］、色素レーザー（窒素レーザー、エキシマーレーザー、あるいはＹＡＧレーザー励起、３００～１０００ｎｍ）、固体レーザー［（Ｎｄ：ＹＡＧ励起、半導体レーザー励起など）；ルビーレーザー（６９４ｎｍ）、半導体レーザー（６５０～９８０ｎｍ）、チューナブルダイオードレーザー（６３０～１５５０ｎｍ）、チタンサファイアレーザー（Ｎｄ：ＹＡＧ励起、３４５～５００ｎｍ、６９０～１０００ｎｍ）、Ｎｄ：ＹＡＧレーザー（ＦＨＧ：２６６ｎｍ、ＴＨＧ：３５４ｎｍ、ＳＨＧ：５３２ｎｍ、基本波：１０６４ｎｍ）］などが挙げられる。

【００５０】本発明の製造方法では、ソース（すなわち、発光中心形成化合物又はバインダー）のアブレーション閾値以下の強度で、レーザー光を照射することにより、発光中心形成化合物を効率よく、ターゲットに注入できる。なお、レーザーの強度、波長、照射回数などを調整することにより、注入量をコントロールできる。

【００５１】ソース(A)のアブレーション閾値は、ソースを構成する発光中心形成化合物の種類によって異なる。また、レーザー光の波長、パルス幅にも依存する。従って、本発明においては、アブレーション閾値を以下のように定義する。

【００５２】本発明で使用するソースおよびレーザーと同一のものを使用して、ソースにレーザー光を１ショット照射し、そのソースを接触型の表面形状測定装置（例えば、SLOAN社製、DEKTAK3030ST）で観察したとき、レーザー光照射表面に、５０ｎｍ以上の形状変化が起こり得る照射表面での最小のレーザー光強度（mJ/cm^2）を、本発明におけるアブレーション閾値と定義する。

【００５３】以下、図面を用いて本発明の有機ＥＬ素子用材料（特に、有機ＥＬ素子用フィルム）の製造方法を説明する。図１は、本発明の製造方法を示す概略図である。ソース（１）、ターゲット（２）、発光中心形成化合物（３）、ターゲット側の基板（４）、ソース側の基板（５）を示す。

【００５４】まず、基板（５）上に形成されたソース（１）と、基板（４）上に形成されたターゲット（２）とを接触又は密着させ、ソース（１）側から、ソースのアブレーション閾値以下の強度のレーザー光をターゲットに対して相対的に移動させて照射する。そして、レーザー光を吸収した発光中心形成化合物が、高い並進エネルギーを有し、ターゲット（２）へ未分解のまま注入され、有機ＥＬ素子用材料（特にフィルム）が得られる。

【００５５】照射回数は、通常、１～２００回、好ましくは１～１５０回、さらに好ましくは１～１００回（例えば、５～１００回）程度である。また、レーザー光を、ターゲット側から照射してもよい。なお、ソースは、ターゲット上に表面層として直接形成させてもよい。ターゲット上に形成されたソースは、発光中心形成化合物を注入後、ターゲットから取り除くことができる。また、ソースは、除去又は剥離可能な表面層で形成されていてもよい。

【００５６】使用する基板としては、レーザー光を透過可能な程度に透明であればよく、例えば、前記例示の基板（石英ガラスなどのガラス板、高分子シートまたはフィルムなど）が使用できる。基板は、ソース又はターゲットフィルムを形成する際に使用した基板をそのまま使用してもよく、新たに作製してもよい。

【００５７】本発明の有機ＥＬ素子用材料を製造する方法において、レーザービームの断面形状は、特に制限されず、円状、楕円状、多角形状（三角形、四角形など）などであってもよい。レーザーの平均ビーム面積は、特に制限されず、目的に応じて広い範囲から選択できる。例えば、０．０１～５０００μm^2、好ましくは０．１～４０００μm^2、さらに好ましくは１～３０００μm^2程度である。なお、レーザー光のビーム面積を所望の大きさに絞り、所定のパターンを走査することによってパターンを形成してもよく、レーザー光のビーム面積を大きくし、予めパターンに形成されたソースを用いたり、又はフォトマスクを介在させてレーザー光を相対的に走査することにより、所定の領域に発光中心形成化合物をターゲット内に注入してもよい。

【００５８】また、異なる発光中心形成化合物を有する複数のソースを使用してもよい。例えば、可視光域で発光可能な化合物（黄、赤、緑又は青などの発光が可能な化合物）を使用すれば、所望の発光色を得ることができる。従って、本発明によれば、多色で多彩な形状のパターンを有する有機ＥＬ素子用材料を得ることができる。

【００５９】本発明の特色は、少なくともターゲットに対してレーザー光を相対的に移動させて、ソースの発光中心形成化合物をターゲットに所定のパターンで注入する点にある。この方法において、ソースおよびターゲットは互いに接触して位置決めされ、ソースおよびターゲットは同伴して移動してもよく、ターゲットに対してソースが相対的に移動可能であってもよい。ソースおよびターゲットが互いに接触している場合、レーザー光の照射は、例えば、（１）ソース及びターゲットに対してレーザー光の光路を移動させる方法、（２）レーザー光の光路に対してソース及びターゲットを移動させる方法のいずれであってもよい。さらに、これらの方法において、レーザー光の光路は、レーザー光源の相対的な移動のみならず、（３）光路を制御するための手段により移動可能である。

【００６０】（３）光路を制御するための手段としては、物理的又は物理光学的手段（例えば、光ファイバ、反射鏡（全反射ミラー、ハーフミラーなど）、レンズ（集光レンズなど）、偏向プリズムなどの光学素子（又は光学部材）又はこれらの組合せた手段）を利用する方

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法、電気光学的手段（例えば、電気光学結晶（複屈折結晶）への電圧印加など）を利用して導波路の光線の光路を移動させる方法、超音波を利用する方法などが挙げられる。なお、超音波を利用する方法としては、例えば、水、カルコゲナイド系ガラス質、$PbMoO_4$，TeO_2，Ｇｅ，$LiNbO_3$，ＧａＰなどの結晶材料を媒質とし、この媒質に圧電薄膜トランスジューサ（例えば、$LiNbO_3$やZnOなどの圧電素子）などを介して電圧を印加することによって媒質に超音波を発生させて導波路を移動させることができる。

【００６１】前記物理的又は物理光学的手段において、光ファイバを利用してレーザー光の光路を移動させると、レーザー光の伝搬損失を低減でき、効率よく、しかも微細なパターニングを簡便に行うことができる。

【００６２】なお、本発明の方法では、直線的だけでなく、少なくともターゲットに対してレーザー光を相対的に二次元的に移動可能である。そのため、ソースの発光中心形成化合物をターゲットに所望のパターンで効率よく注入し、二次元パターンで発光中心を形成できる。

【００６３】例えば、ソース及びターゲットを接触させて、ターゲット面又はソース面を上にして、Ｘ－Ｙ軸方向に移動可能なテーブルに固定し、前記ターゲット（又はソース）の基準位置からのＸ軸及びＹ軸方向への変位を検出するセンサを設け、前記センサの検出信号に応答して、前記テーブルをＸ軸及びＹ軸方向に移動させることにより、高度な位置決めが容易に行えるとともに、二次元の微細パターニングが可能である。なお、必要により、前記パターンのデータを記憶したメモリと、前記パターン信号に応答してレーザー及び／又はテーブルを移動させるコントローラとを設けることにより、簡便にパターニングを行うことができる。

【００６４】レーザー光としてパルスレーザーを使用する場合には、パルス周期に同期させて、前記方法により少なくともターゲットに対してレーザー光を相対的に移動させると、ターゲットとレーザ光とを相対的にシフトさせて発光中心形成化合物をターゲット内に効率よく注入できる。この方法において、レーザー光に対してターゲットを移動させてもよいが、通常、パルス周期に同期させてレーザー光又はレーザー光の光路を制御する場合が多い。

【００６５】さらに、本発明では、少なくともターゲットに対してレーザー光を相対的に移動させればよく、ソースはレーザー光に対して移動させてもよい。なお、ソースの同一部位にレーザー光を繰り返し照射すると、発光中心形成化合物が消費され、発光中心を有効に形成できなくなる。このような場合、レーザー光をターゲットに対して相対的に移動させて照射するとともに、レーザー光に対して相対的にソースを移動させると、発光中心形成化合物を有効かつ効率よくターゲットに注入できる。

【００６６】例えば、発光色の異なる複数の発光中心（例えば、フルカラーの発光中心）を効率よく形成することもできる。本発明によれば、ソースに、各発光中心形成化合物で構成された複数の領域、例えば、黄色発光中心形成化合物で構成された領域、赤色発光中心形成化合物で構成された領域、青色発光中心形成化合物で構成された領域を形成してもよい。このようなソースを用いると、レーザー光及び／又はターゲットに対してソースを相対的にＸ軸方向及び／又はＹ軸方向に移動させることにより、単一のソースを用いて、発光色の異なる複数の発光中心を形成できる。

【００６７】図６は、本発明の他の製造方法を示す概略図である。この例では、レーザー光の光路（光源又は導波）をターゲットに対して縦方向及び／又は横方向に移動させて、レーザー光をソースの緑色の発光中心形成化合物で構成された領域に照射して、緑色の発光中心をターゲットに形成した後、ソースをレーザー光に対して移動させ、次いでレーザー光を赤色発光中心形成化合物で構成された領域に照射し、赤色の発光中心をターゲットに形成する。さらに、同様にして青色の発光中心をターゲットに形成することによって、フルカラーで発光可能な有機ＥＬ素子材料を製造できる。また、この方法では、ソースを介して、ターゲットに対してパルスレーザーを縦方向及び／又は横方向に走査しながら照射しており、ソース１とターゲット２とはレーザー光の照射部位で互いに接触可能である。なお、ソース１は送り機構によりＸ軸及び／又はＹ軸方向に移動可能である。

【００６８】このように、ソースをレーザー光に対して移動させると、単一のソースを用いて、発光色の異なる複数の発光中心を形成できるとともに、発光中心形成化合物を無駄なく使用でき、効率よく発光中心形成化合物を注入できるのでコスト的にも有利である。また、ソースは不定長のフィルムなどで形成されていてもよく、このようなフィルムを使用すると、連続的に発光中心形成化合物を製造できる。

【００６９】また、本発明の製造方法によれば、注入された発光中心形成化合物は、ターゲット中に、分散又は拡散した形態ではなく、ステップ型（すなわち、ターゲット内に注入された深さが均一な矩形の形態）で注入できる。その深さは、発光中心形成化合物やターゲットの種類、またはレーザー強度などにより異なるが、例えば、１０～３００ｎｍ、好ましくは１５～２００ｎｍ、さらに好ましくは２０～１００ｎｍ程度である。また、アブレーション閾値以下の照射であれば、有機ＥＬ素子用材料表面の平滑性を低下させることなく、発光中心形成化合物を効率よく注入できる。

【００７０】[有機エレクトロルミネッセンス素子]本発明の有機エレクトロルミネッセンス素子は、上記方法により得られた有機ＥＬ素子用材料（特に、発光中心形成化合物が注入されたターゲットフィルムで構成された発

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光層）と、一対の電極から構成されている。

【００７１】陽極としては、真空蒸着法などにより形成された透明電極（例えば、インジウムースずー酸化物（ＩＴＯ）電極）などが使用され、陰極としては、仕事関数の小さい高導電性金属（例えば、マグネシウム、リチウム、アルミニウム又は銀など）が使用される。陰極としてマグネシウムを使用する場合には、有機ＥＬ素子用フィルムとの接着性を向上させるために、少量（例えば、１～１０重量％）の銀と共蒸着させてもよい。

【００７２】発光層が、電子輸送機能およびホール輸送機能を有する場合、本発明の有機ＥＬ素子は、単層構造が可能である。また、電子輸送機能およびホール輸送機能のうち、いずれかの機能を具備していない場合や、各機能を向上させる場合には、その機能を有する層を、従来の蒸着法や溶液塗布法などにより積層させてもよい。これらの層は、低分子化合物であっても、高分子化合物であってもよい。有機ＥＬ素子の構造は、例えば、図２～５に示される単層または多層構造が可能である。

【００７３】すなわち、図２に示すように、基板(10)上に陽極(11)が形成され、その上に発光層(12)、陰極(13)が順に積層した有機ＥＬ素子、図３に示すように、基板(20)上に陽極(21)が形成され、その上にホール輸送層(24)、発光層(22)、陰極(23)が順に積層した有機ＥＬ素子であってもよい。さらに、図４に示すように、基板(30)上に陽極(31)が形成され、その上に発光層(32)、電子輸送層(35)、陰極(33)が順に積層した有機ＥＬ素子、図５に示すように、基板(40)上に陽極(41)が形成され、その上にホール輸送層(44)、発光層(42)、電子輸送層(45)、陰極(43)が順に積層した有機ＥＬ素子であってもよい。

【００７４】有機ＥＬ素子を構成する各層の膜厚は、特に制限されないが、１０ｎｍ～１μｍ（例えば、１０～５００ｎｍ）、好ましくは３０～３００ｎｍ、さらに好ましくは３０～２００ｎｍ、特に５０～２００ｎｍ程度である。フィルムを用いた場合、フィルムの膜厚は、上記と同様の範囲から選択できる。

【００７５】なお、基板としては、前記例示の基板、例えば、レーザー光を透過可能な程度に透明な基板（例えば、ソーダガラス、無アルカリガラス、石英ガラスなどのガラス板など、あるいはポリエステル、ポリスルホン、ポリエーテルスルホンなどの高分子シートまたはフィルムなど）が使用できる。フレキシブルな有機ＥＬ素子を作製する場合には、高分子フィルムが好ましい。基板は、分子注入の際に使用した基板をそのまま使用してもよく、新たに作製してもよい。

【００７６】本発明の方法によれば、有機ＥＬ素子において、従来、高分子化合物を使用した有機ＥＬ素子で困難であった微細な多色パターニングが可能である。さらに、本発明の有機ＥＬ素子用材料（特に、有機ＥＬ素子用フィルム）は、表面平滑性に優れているため、電極との接着性が良く、さらに、発光中心形成化合物がステップ型に注入されているため、電圧を印加したときに電圧ムラなどが生じないばかりか、精度よく、所望のパターンを形成できる。

【００７７】

【発明の効果】本発明では、レーザー光を少なくともターゲットに対して相対的に移動させることによって、高度な位置決めが可能であり、微細なパターニングが簡便に行えるとともに、光ファイバなどを利用すれば、高精度で微細なパターニングが可能である。また、レーザー光を少なくともターゲットに対して相対的に移動させるとともに、レーザー光に対してソースを移動させることにより、効率よく発光中心形成化合物を注入できる。

【００７８】

【実施例】以下に、実施例に基づいて本発明をより詳細に説明するが、本発明はこれらの実施例によって限定されるものではない。

【００７９】実施例１

（ソースフィルムの調製）５重量％のクマリン６（日本感光色素（株）製）を含むポリブチルメタクリレート（アルドリッチ社製、分子量３．４×10^5）をクロロベンゼンに溶解し、スピンコーティング法により、石英基板上に厚さ１μｍの膜を作製した。（ターゲットフィルムの調製）ホール輸送機能を有するポリ－Ｎ－ビニルカルバゾール（ＰＶＫ：関東化学社製）５００ｍｇと、電子輸送機能を有する２－（４－ビフェニル）－５－（４－tert-ブチルフェニル）－１，３，４－オキサジアゾール（ＰＢＤ：アルドリッチ社製）５００ｍｇを、１，２－ジクロロエタン１０ｍＬに溶解した。一方、ガラス基板上にインジウムーすずー酸化物（ＩＴＯ）被膜を形成させた。上記の１，２－ジクロロエタン溶液を用いてディップコーティング法により、ＩＴＯ被膜上に膜厚１００ｎｍの電子・ホール輸送機能を有するターゲットフィルムを作製した。

（分子注入）上記のようにして得られたソースフィルムとターゲットフィルムとを接触させ、Ｘ軸及びＹ軸方向に移動可能なテーブルに、ターゲットフィルム面を上にして固定し、ビーム面積２０mm^2で、パルス幅１０ｎｓのＸｅＦエキシマーレーザー（波長３５１ｎｍ）を発振可能なレーザー加工装置を用い、前記テーブルをレーザー光に対してＸ－Ｙ軸方向に移動させて、２０mm^2のパターンに発光中心形成化合物を注入した。

（有機ＥＬ素子）分子注入したターゲットフィルム（試料１）に、厚み２００ｎｍのＡｌ／Ｌｉ電極（高純度化学（株）製、Ｌｉ含有量０．７８重量％）を真空蒸着法により作製し、有機ＥＬ素子１を得た。

【００８０】上記有機ＥＬ素子のＩＴＯ電極を陽極、Ａｌ／Ｌｉ電極層を陰極として、大気中で両電極間に直流電場を印加して発光させた。有機ＥＬ素子１は、電圧約１８Ｖより発光が確認できた。クマリン６を注入した領域では、クマリン６の緑色発光が確認された。前記領域

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以外の部分ではＰＶＫの青色発光が確認できた。

【図面の簡単な説明】

【図１】図１は、発光中心形成化合物を注入する方法を説明するための概略図である。

【図２】図２は、本発明の有機エレクトロルミネッセンス素子の１例（単層構造）を示す概略断面図である。

【図３】図３は、本発明の有機エレクトロルミネッセンス素子の他の例（多層構造）を示す概略断面図である。

【図４】図４は、本発明の有機エレクトロルミネッセンス素子のさらに他の例（多層構造）を示す概略断面図である。

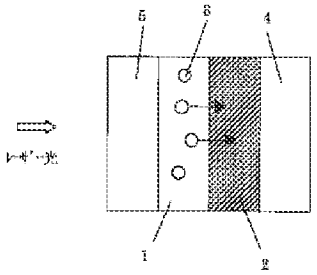
【図５】図５は、本発明の有機エレクトロルミネッセンス素子の別の例（多層構造）を示す概略断面図である。＊

＊【図６】図６は、本発明の他の製造方法を説明するための概略図である。

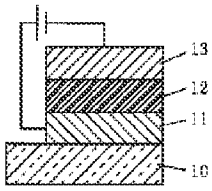
【符号の説明】

１…ソース
２…ターゲットフィルム
３…発光中心形成化合物
４，５…基板
１０，２０，３０，４０…基板
１１，２１，３１，４１…陽極
１２，２２，３２，４２…発光層
１３，２３，３３，４３…陰極
２４，４４…ホール輸送層
３５，４５…電子輸送層

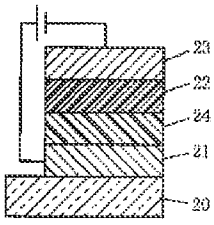
【図１】



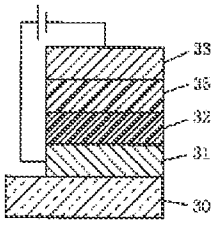
【図２】



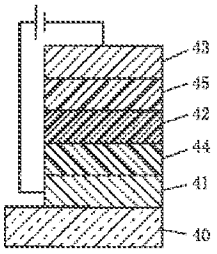
【図３】



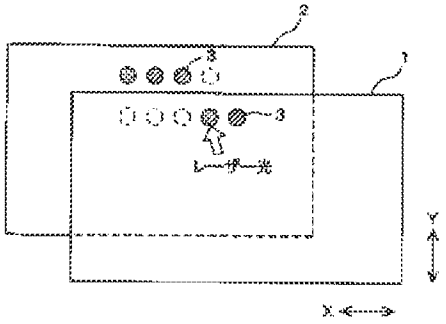
【図４】



【図５】



【図６】



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Espacenet

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FORMATION OF SILICON OXIDE SEMICONDUCTOR FILM

Inventor(s): POOPON SHITSUCHIYANURITSUTSU ± (POOPON SHITSUCHIYANURITSUTSU)

Applicant(s): FUJI ELECTRIC CO LTD ± (FUJI ELECTRIC CO LTD)

Classification: - international:***H01L21/205; H01L31/0376; H01L31/04; H01L31/075; H01L31/20;*** (IPC1-7): H01L21/205; H01L31/04
- cooperative: **H01L31/0376**; **H01L31/075**; **H01L31/20**; Y02E10/548

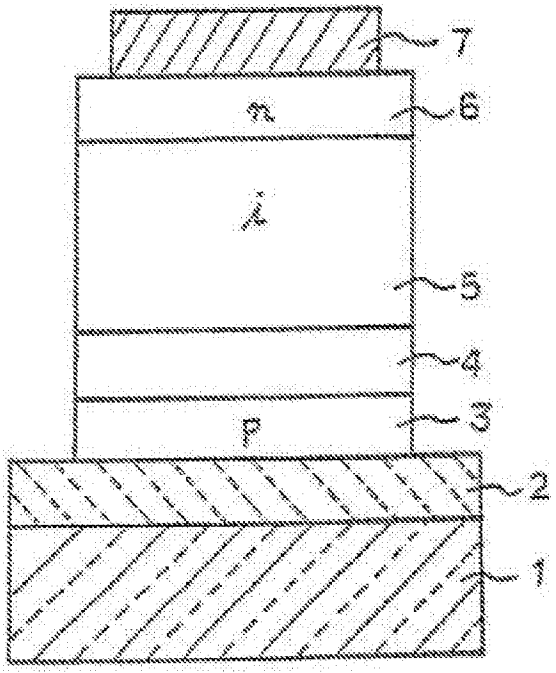
Application number: JP19930054433 19930316

Priority number (s): JP19930054433 19930316

Also published as: DE4408791 (A1) DE4408791 (B4) JP3047666 (B2)

Abstract of JPH06267868 (A)

PURPOSE:To industrially form a silicon oxide semiconductor film having a low light absorption coefficient and high photoconductivity by resolving a gaseous raw material which contains at least SiH4, CO2, and H2 in a state where CO2/(SiH4+CO2) becomes a specific value. CONSTITUTION:In the method which is used for forming an SiO semiconductor film composed of a-SiO2 containing a microcrystalline layer of Si, the SiO semiconductor film is formed by resolving a gaseous raw material which contains at least SiH4, CO2, and H2 in a state where CO2/(SiH4+CO2) becomes <=0.6. At the time of decomposing the mixed gas, it is effective to generate glow discharge in the gas at a high-frequency power density of >=40mW/cm<2>. The formed SiO semiconductor film has a absorption coefficient <=10<6>cm<-1> against light having a wavelength of >=340nm and photoconductivity of >=10<-6>S/cm.; In addition, it is effective, to use a p-type a-SiO layer 3 or n-type a-Si layer 6 obtained by mixing a doping gas with the gaseous raw material as the window layer of a solar battery.



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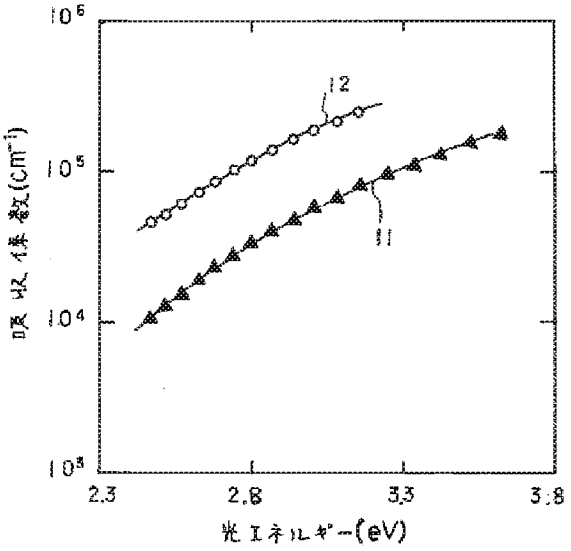
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(54)【発明の名称】　シリコンオキサイド半導体膜の成膜方法

(57)【要約】
【目的】太陽電池の窓層として用いるために他の元素を添加してワイドギャップ化するときに低下するａ－Ｓｉ系膜の光導電率を向上させるために微結晶化する。
【構成】CO_2 の（SiH_4 ＋CO_2 ）に対する流量比を0.6以下とした（CO_2 ＋SiH_4 ＋H_2 ）混合ガスを高周波パワー密度を高めてグロー放電分解すると、Ｓｉの微結晶相とａ－ＳｉＯ相とが混在している半導体膜を得ることができる。この膜は、10^{-6} Ｓ／cm以上の高光導電率で、吸収係数が10^5 cm^{-1}以下の低い値を示す。



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【特許請求の範囲】
【請求項１】少なくともSiH$_4$ 、CO$_2$ およびH$_2$ を含み、CO$_2$ ／（SiH$_4$ ＋CO$_2$ ）の値が0.６以下である原料ガスの分解によることを特徴とするシリコンの微結晶相を含む非晶質シリコンオキサイドよりなるシリコンオキサイド半導体膜の成膜方法。
【請求項２】混合ガスの分解のために40ｍW／cm以上の高周波パワー密度で原料ガス中にグロー放電を発生させる請求項１記載のシリコンオキサイド半導体膜の成膜方法。
【請求項３】得られた膜の340nm 以上の波長の光に対する吸収係数が10^5 cm^{-1}以下である請求項１あるいは２記載のシリコンオキサイド半導体膜の成膜方法。
【請求項４】得られた膜の光導電率が10^{-6}Ｓ／cm以上である請求項１、２あるいは３記載のシリコンオキサイド半導体膜の成膜方法。
【請求項５】原料ガスにドーピングガスを混合して得られたｐ形あるいはｎ形の膜を太陽電池の窓層として用いる請求項１、２、３あるいは４記載のシリコンオキサイド半導体膜の成膜方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、非晶質シリコン（以下ａ－Siと記す）系太陽電池の窓層として適しているシリコンオキサイド半導体膜の成膜方法に関する。
【０００２】
【従来の技術】原料ガスのグロー放電分解や光ＣＶＤ法により形成されるａ－Siを主材料とした太陽電池は薄膜、大面積化が容易という特長をもち、低コスト太陽電池として期待されている。この種の太陽電池の構造としてはｐｉｎ接合を有するｐｉｎ型ａ－Si太陽電池が一般的である。図２はこのような太陽電池の構造を示し、ガラス基板１の上に、透明電極２、ｐ形ａ－Si層３、ｐ／ｉ界面層４、ｉ質ａ－Si層５、ｎ形ａ－Si層６、金属電極７を順次積層することにより作製される。この太陽電池は、ガラス基板１を通して入射する光により発電が起こる。
【０００３】ここで、発電に寄与するフォトキャリアは主にｉ層で発生し、ｐおよびｎ層はデッドレイヤーになっている。従って、図２のようにｐ層３から光が入射する太陽電池では、窓層にあたるｐ層の光吸収係数を低くし、できるだけ多くの光がｉ層５まで到達できるようにすることが出力を増加させる上で重要である。そのためには、ｐ層の光学ギャップEg を増加させて光学吸収ロスを減少させることが有効である。このような目的からｐ形ａ－Si層に、例えば特開昭56－64476 号公報などで公知のように炭素原子を添加したり、特開昭57－181176号公報で公知のように窒素原子を添加したり、特開昭56－142680号公報で公知のように酸素原子を添加したり、または特開昭58－196064号公報あるいは特開昭61－242085号公報で公知のように酸素原子と炭素原子を添加したりすることが試みられている。
【０００４】また、最近では、特開昭64－51618 号公報に示すようにＥＣＲ－ＣＶＤ法により、あるいはTechnical Digest of the International PVSEC-3 (1987)p.49に記載されているようにプラズマＣＶＤ法により、炭素原子を添加した非晶質シリコンカーバイド（以下ａ－SiＣと記す）膜に微結晶相を含ませることに成功している。このような膜は、ａ－SiＣ相にSiの微結晶相を含むことにより、光導電率が高くなり、電気的特性が良好である。
【０００５】
【発明が解決しようとする課題】上記のようにａ－Si系膜にSiの微結晶相を含ませることは、ワイドギャップ化のために他元素原子を添加した場合に低下する光導電率を高めるので、太陽電池窓層としての特性を向上させるのに有望であるが、公知のａ－SiＣ膜の微結晶化する方法は、微結晶化のための成膜条件の範囲が狭く、付着率を高めるのが困難であるなど工業化には難点がある。
【０００６】本発明は、ａ－Si系膜のうち、酸素を含む非晶質シリコンオキサイド（以下ａ－SiＯと記す）膜を微結晶化した、低光吸収係数で高光導電率のシリコンオキサイド（以下SiＯと記す）半導体膜の工業化に適した成膜方法を提供することにある。
【０００７】
【課題を解決するための手段】上記の目的を達成するために、本発明のSiの微結晶層を含むａ－SiＯよりなるSiＯ半導体膜の成膜方法は、少なくともSiH$_4$ 、CO$_2$ およびH$_2$ を含み、CO$_2$ ／（SiH$_4$ ＋CO$_2$ ）の値が0.６以下である原料ガスの分解によるものとする。その場合、混合ガスの分解のために40mW／cm^2 以上の高周波パワー密度でグロー放電を原料ガス中に発生させることが有効である。また、得られたSiＯ半導体膜の340nm 以上の波長の光の吸収係数が10^5 cm^{-1}以下であり、光導電率が10^{-6}Ｓ／cm以上である。また、原料ガスにドーピングガスを混合して得られたｐ形あるいはｎ形の膜を太陽電池の窓層として用いることが有効である。
【０００８】
【作用】SiH$_4$ 、CO$_2$ 、H$_2$ を含む原料ガスを用いて太陽電池の窓層を形成することは、前掲の特開昭61－242085号公報で公知であるが、その場合のガス流量比CO$_2$ ／（SiH$_4$ ＋CO$_2$ ）の値は0.83であり、得られたａ－Si膜は、酸素原子および炭素原子を含む。これに対し、CO$_2$ ／（SiH$_4$ ＋CO$_2$ ）を0.６以下とした場合、特に高周波パワー密度40mW／cm^2 以上でのグロー放電分解により得られる膜では、炭素量は検出限界以下であり、微結晶化したSi層とａ－SiＯ相とが混在しているSiＯ膜となって、10^{-6}Ｓ／cm以上の高い光導電率で高い光吸収係数を示す。
【０００９】

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【実施例】SiH_4 、CO_2 、H_2 を混合し、ドーピングガスとしてB_2H_6 あるいはPH_3 を添加し、各ガスの流量比を変化させて、次の成膜条件でｐ形およびｎ形のＳｉＯ膜を形成した。

CO_2 ／（SiH_4 ＋CO_2 ）　0～0.6
H_2 ／SiH_4　160～320
B_2H_6 ／SiH_4 またはPH_3 ／SiH_4　0.08
基板温度　150 ℃
圧　力　0.5Torr
高周波パワー密度　50 mW／cm²

図３は、ドーピングガスとしてB_2H_6 を添加して成膜したｐ形の膜における340nm ～500nm の波長の光に対する吸収係数のガス流量比CO_2 ／（SiH_4 ＋CO_2 ）依存性を表している。吸収係数は、短い波長の光に対しても10^6 cm^{-1}以下であり、波長が長くなると減少し、またCO_2 流量比が多くなるにつれて減少してくることがわかった。図４は、ドーピングガスとしてPH_3 を添加して成膜したｎ形の膜における吸収係数のガス流量比依存性を表しており、ｐ形膜と同様の傾向を示す。形成されたＰ形およびｎ形膜をＥＳＣＡで分析したところ、混合するCO_2 の流量比の増加に伴って酸素量が増えてくることが確認された。そして、酸素量は25～40原子％であるのに対し、炭素量は１％以下の検出限界外になっていた。

【００１０】図５は、光導電率のガス流量比依存性を示し、CO_2 流量の増加と共に光導電率σ_{ph}が低くなり、線51で示すｎ形の方が線52で示すｐ形より光導電率が高いということがわかった。そして、光導電率を10^{-6} Ｓ／cm以上に抑えるには流量比CO_2 ／（SiH_4 ＋CO_2 ）を0.６以下とすることが必要である。このようにして得られたＳｉＯ膜についてラマン散乱を測定したところ、ラマンスペクトルにSi結晶の存在を示す530 cm^{-1}付近のピークが存在し、微結晶化したSi相とａ－ＳｉＯ相が混在していることが確認された。また、CO_2 流量比の増加と共に、530 cm^{-1}付近のピークの強度が減少してくることが確認された。

【００１１】図１は、光導電率σ_{ph}が太陽電池の窓層として用いることのできる最低限である10^{-6} Ｓ／cm付近にある本発明の実施例によるＳｉＯ膜の吸収係数を従来のｐ形ａ－ＳｉＯ膜と比較したもので、線11に示す微結晶相を含むａ－ＳｉＯ膜の吸収係数は、広い波長域にわたって線12に示す微結晶相を含まないａ－ＳｉＯ膜の吸収係数の１／３になっており、同様な特性をもつｎ形膜と共に太陽電池の窓層の材料として有望であることがわかった。

【００１２】また、CO_2 の代わりにC_2H_2 を用い、原料ガス以外は上記の実施例と同一の条件で成膜したところ、得られた膜の炭素の量は20原子％と少ないにもかかわらず、ラマンスペクトルはSi結晶相の存在を示す530 cm^{-1}付近のピークが見られず、微結晶化していないことが確認された。このことから、酸素原子と比較して炭素原子の方がシリコンの微結晶化を妨げると考えられ、ワイドギャップ化で吸収係数の減少が見られても導電率の低下により、太陽電池の窓層の材料として不適当であることがわかった。

【００１３】

【発明の効果】本発明によれば、混合比を低くしたCO_2 を酸素源として用い、SiH_4 、H_2との混合ガスによりａ－ＳｉＯを成膜することにより、炭素を含まず、Si微結晶相を含んだａ－ＳｉＯ相からなるＳｉＯ膜を成膜することができた。この結果、酸素原子によりワイドギャップ化されて低吸収係数であり、かつ微結晶相の存在により導電率の高いａ－Si系膜を得ることができ、ｐ形あるいはｎ形の窓層としてａ－Si系太陽電池に極めて有効に用いることができる。

【図面の簡単な説明】

【図１】本発明の一実施例により成膜されたｐ形ＳｉＯ膜と従来のｐ形ａ－ＳｉＯ膜との吸収係数と光エネルギーとの関係線図

【図２】本発明により成膜されるｐ形ＳｉＯ膜を用いることのできる太陽電池の断面図

【図３】本発明の一実施例により成膜されたｐ形ＳｉＯ膜の成膜時のCO_2 ガス流量比をパラメータとした吸収係数と光エネルギーとの関係線図

【図４】本発明の別の実施例により成膜されたｎ形ＳｉＯ膜の成膜時のCO_2 ガス流量比をパラメータとした吸収係数と光エネルギーとの関係線図

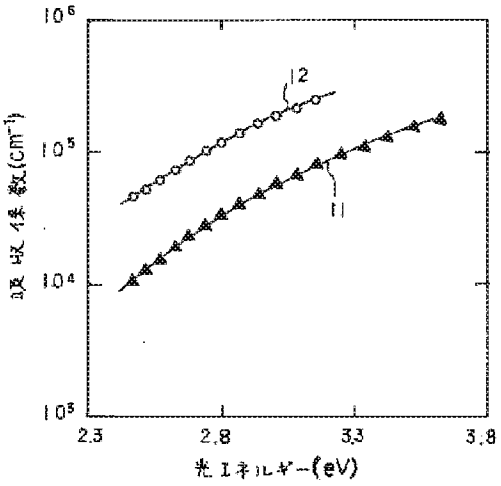
【図５】本発明の実施例により成膜されたｐ形およびｎ形ＳｉＯ膜の光導電率とCO_2 ガス流量比との関係線図

【符号の説明】

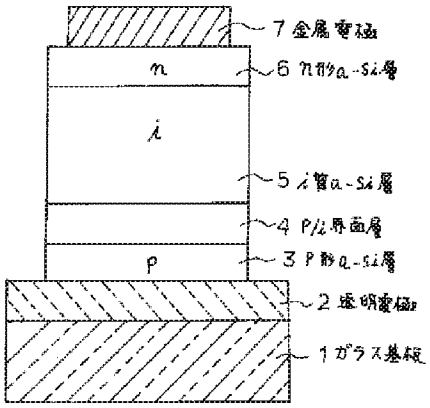
1　ガラス基板
2　透明電極
3　ｐ形ａ－Si層
4　ｐ／ｉ界面層
5　ｉ質ａ－Si層
6　ｎ形ａ－Si層
7　金属電極

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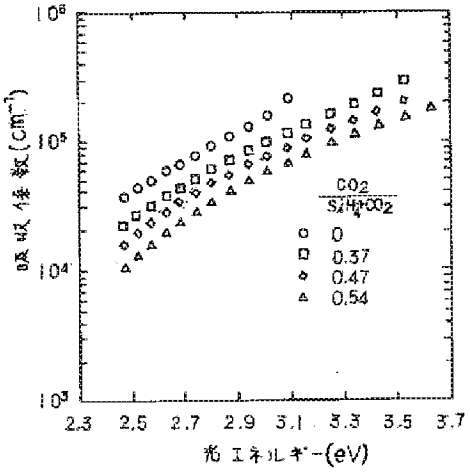
【図1】



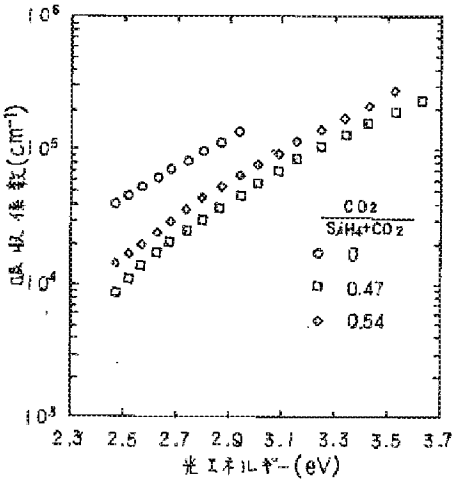
【図2】



【図3】

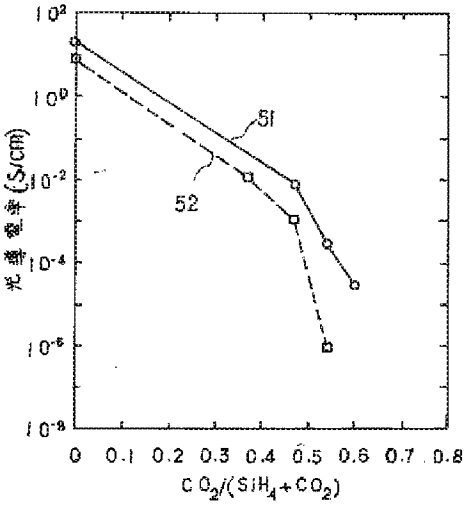


【図4】



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【図5】


光導電率 (S/cm)
10^{2}
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
51
52
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8
$CO_2/(SiH_4+CO_2)$

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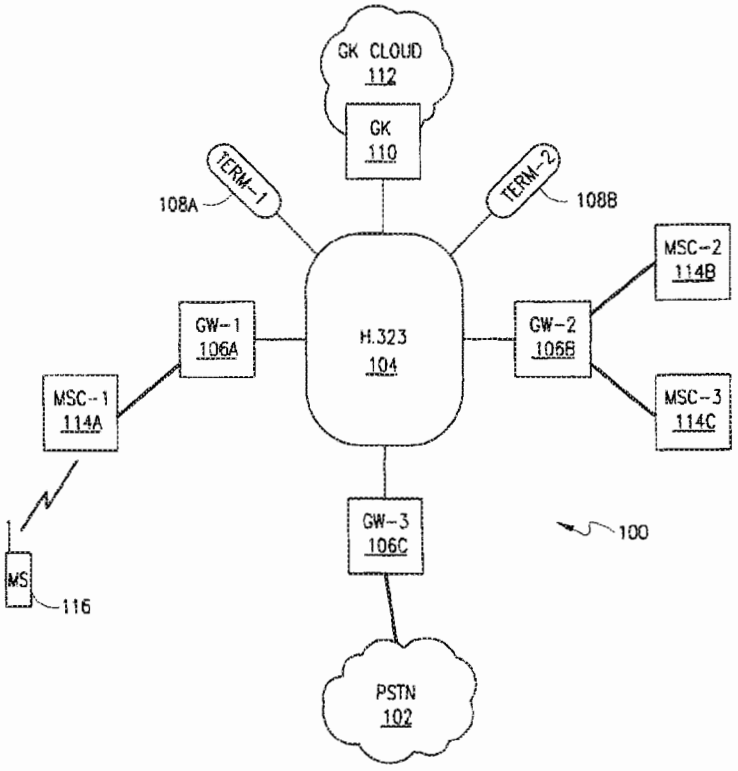
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[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR IMPROVED RESOURCE MANAGEMENT IN AN INTEGRATED TELECOMMUNICATIONS NETWORK HAVING A PACKET-SWITCHED NETWORK PORTION AND A CIRCUIT-SWITCHED NETWORK PORTION



(57) Abstract: A system and method for providing improved resource management, e.g., bandwidth re-allocation, in an integrated telecommunications network (100) having a packet-switched network portion (e.g., a Voice-over-Internet Protocol (VoIP) network portion) (104) and a cellular network portion (114). When a parametric variable associated with the number of registrations of mobile stations in a Mobile Switching Center (MSC) (114A) passes a threshold test (206), the MSC sends a message (306) to its gateway (106A), the message including a level change parameter. Responsive thereto, the gateway re-registers in a gatekeeper (110) that is provided for managing a zone in the VoIP network. The gateway includes in its registration request (308) the level change parameter received from the MSC. The gatekeeper uses the level change parameter as an input to its resource management function and re-allocates the resources available for the gateway.

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 99 52237 A (VERTICLE NETWORKS INC) 14 October 1999 (1999-10-14) page 17, line 11 - line 25 page 21, line 4 - line 9; claim 13	1-22
Y	EP 0 545 164 A (ALCATEL NV) 9 June 1993 (1993-06-09) abstract; claims	1-22
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 May 2001	29. 06. 2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Kristoffer Ogebjer

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Form PCT/ISA/210 (second sheet) (July 1992)

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

'ernational application No.
PCT/SE 00/02045

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☒ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

see extra sheet

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

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FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-22

   The invention re-allocates resources, by a gatekeeper, to the gateway when resources needed.

2. Claims: 23-26

   The invention routes an in-coming call by a gatekeeper to a mobile station using a gateway's network address. The gateway sends a register request to the gatekeeper including MDN and a network address associated with the gateway.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/SE 00/02045

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/SE 00/02045

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Filed on 10 November 1999 (10.11.1999)

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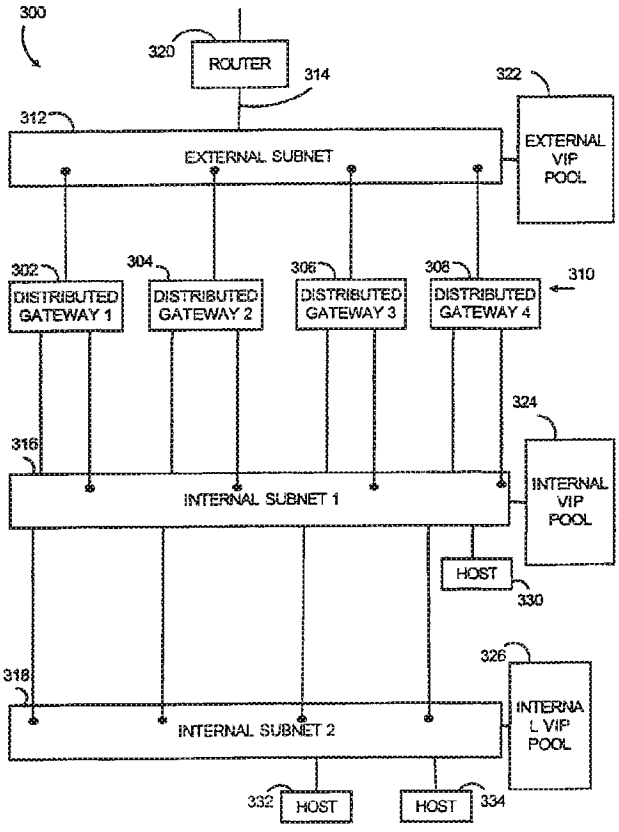
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[Continued on next page]

(54) Title: DISTRIBUTED TRAFFIC CONTROLLING SYSTEM AND METHOD FOR NETWORK DATA



(57) Abstract: A distributed gateway (310) represented in the figure for controlling computer network data traffic dynamically reconfigures traffic assignments among multiple gateway machines (302, 304, 306, 308) for increased network availability. If one of the distributed gateway machines becomes unavailable, traffic assignments are moved among the multiple machines such that network availability is substantially unchanged. The machines of the distributed gateway form a cluster (310) and communicate with each other using a Group Membership protocol word such that automatic, dynamic traffic assignment reconfiguration occurs in response to machines being added and deleted from the cluster, with no loss in functionality for the gateway overall, in a process that is transparent to network users, thereby providing a distributed gateway functionality that is scalable. Operation of the distributed gateway remains consistent as machines are added and deleted from the cluster. A scalable, distributed, highly available, load balancing network gateway is thereby provided, having multiple machines that function as a front server layer (310) between the network (314) and a back-end server layer (316,318) having multiple machines functioning as Web file servers, FTP servers, or other application servers. The front layer machines (302,304,306,308) comprise a server cluster that performs fail-over and dynamic load balancing for both server layers.

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Published:
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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DISTRIBUTED TRAFFIC CONTROLLING SYSTEM AND METHOD FOR NETWORK DATA

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Patent Application Serial No. 09/437,637 entitled "Distributed Traffic Controller for Network Data", filed November 10, 1999, which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to computer network data traffic and, more particularly, to controllers that manage the flow of data in a computer network.

2. Description of the Related Art

To enable sharing of data among computer users, most computer systems in use today are connected to a computer network. Computers in an office, for example, may be connected over a local area network (LAN) to gain access to a server computer, which manages common data storage. The Internet is a computer network in which literally millions of user computers communicate with server computers over a widely distributed

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network. The server computers may be file servers that provide data files in response to user requests, or they may perform other functions, such as e-mail processing.

Data traffic over the Internet generally follows a transportation protocol called the Transport Control Protocol/Internet Protocol (TCP/IP). Some of the data traffic involves user data messages that are sent from users over the network through routers and switches to destination computers. The destination computer may be a server computer, such as where an Internet user requests a page from a web site. In that case, a user sends a request message to a web server computer in accordance with a hypertext transfer protocol (HTTP). The request is received at the web server computer, which returns the web site data over the Internet network to the requesting user computer. Instead of a server computer, the destination computer may be another user, such as where an Internet user sends an e-mail message over the Internet to another user. In that case, a user sends an e-mail message to an outgoing mail server computer, which sends the message out over the Internet to an appropriate destination e-mail server, which then routes the message to the appropriate user computer.

Because the Internet is a public data network, there is no way to reliably ensure the integrity of data traffic being routed over the Internet. That is, so-called "hackers" may be sending computer viruses to randomly targeted destinations, or hackers may attempt to gain access to a web server computer to alter or destroy the data stored there. To protect against such malicious acts, firewall systems have been developed to screen out unwanted traffic and to protect against unauthorized intrusions.

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Figure 1 shows a conventional firewall system 100 in which a single firewall machine 102 acts as a secure gateway between the Internet 104 or other public network and two local user networks 106, 108. All traffic to and from the outside world (the Internet) must pass through the firewall machine 102. In accordance with TCP/IP addressing, Internet traffic views the address of the system 100 through an external subnet address, which in the Figure 1 system is illustrated as the external subnet of (200.199.198.0). In this document, network addresses will be enclosed within parentheses, whether for subnets or individual host machines. Those skilled in the art will understand that the firewall machine 102 will have a machine address that is an address under the external subnet. In particular, the address of (200.199.198.1) is shown in Figure 1 as the address, or Uniform Resource Locator (URL) of the firewall machine 102. Similarly, the two local networks 106, 108 are shown connected to the firewall machine 102, the first subnet 106 shown as the (192.168.1.0) subnet and the second subnet 108 shown as the (192.168.2.0) subnet.

To implement the firewall processing, the gateway computer 102 is loaded with firewall software programming, as well as being configured with network interfaces to each internal and external subnet 106, 108. Such firewall software is readily available and may comprise, for example, the "FireWall-1" product from Check Point Software Technologies Ltd. of Redwood City, California, USA.

The firewall machine 102 will have multiple Internet protocol (IP) addresses, one for each subnet. Because there is a single firewall machine, all client machines and routers of the local networks 106, 108 can simply specify the IP address of the firewall machine 102 as their default gateway for all outgoing data traffic destined for the Internet. This firewall

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implementation provides a simple and relatively inexpensive solution to ensuring integrity of the local networks on the "downstream" side of the gateway 102. Unfortunately, the single gateway is a single point of failure and can become a potential bottleneck for data traffic. This likely will be become more and more critical as firewall machines are asked to perform more and more tasks, such as encryption and authentication. That is, whenever the firewall machine 102 is not functioning, all of the internal, local network machines are isolated from the outside world via the Internet. The single bottleneck can be a serious problem, because even simple maintenance and upgrades on the firewall machine will be necessary from time to time, and when they occur, they will result in network downtime that will isolate the client side machines from the Internet. For many web sites, such as e-commerce sites, no amount of downtime is acceptable.

Conventionally, increased availability and reduced network downtime is provided by multiple gateway machines. In the system 200 shown in Figure 2, a multiple gateway system is provided to the Internet 202 that is comprised of multiple firewall machines 204, 206, 208, 210. Rather than a single IP address, the gateway is identified by a single external subnet (200.199.198.0) and with an associated set of IP addresses, comprising an address pool, off that subnet and corresponding to each of the firewall machines 204, 206, 208, 210, respectively. For example, the addresses may comprise the set of (200.199.198.1), (200.199.198.2), (200.199.198.3), and (200.199.198.4).

In Figure 2, each firewall machine 204, 206, 208, 210 is connected to two internal subnets, a first subnet 212 and a second subnet 214. Each of these internal subnets, which are local networks, can be connected to multiple local computers 216, 218, 220, such as web

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server or e-mail server computers. Each computer connected to either one of the internal subnets 212, 214 must select one IP address from a corresponding pool of subnet IP addresses as their default gateway address.

For example, the first subnet 212 is indicated as the (192.168.1.0) subnet, and may be associated with a pool of IP addresses comprising (192.168.1.1), (192.168.1.2), (192.168.1.3), and (192.168.1.4) addresses. Therefore, a web server 216 connected to the first subnet 212 can select either one of these four IP pool addresses as its default gateway computer for handling upstream data traffic. The second subnet 214 is indicated as the (192.168.2.0) subnet, and is shown as having an IP address pool comprising (192.168.2.1), (192.168.2.2), (192.168.2.3), and (192.168.2.4) addresses. Therefore, a web server 220 connected to the second subnet 214 can select either one of these second subnet IP addresses as its default gateway computer for handling upstream data traffic.

In the Figure 2 system 200, if there is a failure of any gateway machine 204, 206, 208, 210 or of any network interface or software at a firewall machine, then all local network machines and routers configured to use that machine as their default gateway will lose their connection to the outside world. For example, if the web server computer 216 is configured to use the first subnet firewall machine 204 as its default gateway, and if there is a failure with that machine, then the web server 216 will lose communication with the outside world, even though there are still three remaining firewall machines 204, 206, 208 that might be able to handle data traffic from that web server. Thus, whenever a failure occurs, some local network users will be out of communication. The multiple firewall machine implementation shown in Figure 2 therefore relieves the operational bottleneck problem described above by

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providing additional resources for handling data traffic, but cannot provide high availability in the case of machine failures.

From the discussion above, it should be apparent that there is a need for controlling data traffic over a network so as to provide firewall protection, relieve operational bottlenecks, and increase network availability. The present invention solves this need.

SUMMARY OF THE INVENTION

In accordance with the invention, a distributed gateway for computer network data traffic dynamically reconfigures traffic assignments among multiple machines for increased network availability. If one of the distributed gateway machines becomes unavailable, traffic assignments are moved among the multiple machines such that network availability is substantially unchanged. The machines of the distributed gateway form a cluster and communicate with each other such that automatic, dynamic traffic assignment reconfiguration occurs in response to machines being added and deleted from the cluster, with no loss in functionality for the gateway overall, in a process that is transparent to network users, thereby providing a distributed gateway functionality that is scalable. Thus, operation of the distributed gateway remains consistent as machines are added and deleted from the cluster. Each machine of the distributed gateway can continue with any applications it may be running, such as firewall software, while participating in the distributed gateway and dynamic reconfiguration processing of the present invention. In this way, the invention

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substantially maintains network availability regardless of machine failures, so that there is no single point of failure and no lapse in gateway functionality.

In one aspect of the invention, the machines of the distributed gateway cluster communicate with each other by passing a Group Membership protocol word among the cluster machines over the subnet network with which they are connected. The protocol word is used to inform the distributed gateway machines of the cluster status, including the status of individual machines, in a token ring arrangement. Thus, each machine of the cluster becomes aware of any problem with any of the other machines in the cluster and is aware of the operational status of each machine. With such knowledge, the machines will individually determine the traffic load being borne by the other machines. If any one machine observes that another machine is handling an excessive amount of network traffic, the observing machine will take on some of the traffic from the overloaded machine, thereby performing a load balancing operation.

In another aspect of the invention, a user can configure and monitor a machine of the distributed gateway cluster from any other machine of the cluster, and also can perform such configuration and monitoring from a remote location. Such operations can be conducted through a command line interface or through a graphical user interface (GUI) that permits real time changes in network IP address assignments.

In another aspect of the invention, a scalable, distributed, highly available, load balancing network server system is provided, having multiple machines that function as a front server layer between the network and a back-end server layer having multiple machines functioning as Web file servers, FTP servers, or other application servers. The front layer

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machines comprise a server cluster that performs fail-over and dynamic load balancing for both server layers. The operation of the servers on both layers is monitored, and when a server failure at either layer is detected, the system automatically shifts network traffic from the failed machine to one or more of the remaining operational machines, reconfiguring front-layer servers as needed without interrupting operation of the servers. The server system automatically accommodates additional machines in the server cluster, without service interruption. A system constructed in accordance with the invention provides a front layer server cluster that manages multiple network addresses and ensures availability of all network addresses assigned to the front layer at all times. The system operates with a dynamic reconfiguration protocol that permits reassignment of network addresses to the front layer machines. The server cluster may manage network address assignments and route network traffic, operating as a gateway, providing management of virtual network addresses such that network address assignments can be moved from gateway to gateway without requiring rebooting. Finally, the system provides symmetric routing of network traffic, guaranteeing that the incoming and outgoing traffic of the same network connection goes through the same front-layer server.

Other features and advantages of the present invention should be apparent from the following description of the preferred embodiment, which illustrates, by way of example, the principles of the invention.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a prior art computer system in which a single firewall computer controls the flow of data traffic from a network to local network computers.

Figure 2 is a schematic diagram of a prior art computer system in which multiple firewall computers control the flow of data traffic from a network to local network computers.

Figure 3 is a schematic diagram of a computer system constructed in accordance with the present invention.

Figure 4 is a representation of a gateway computer in Figure 3, illustrating the OSI networking model components of the gateway constructed in accordance with the present invention.

Figure 5 is a representation of the system architecture for the Application Wrapper illustrated in Figure 4.

Figure 6 is a block diagram of a gateway computer in the system of Figure 3, illustrating the hardware components of the computer.

Figure 7 is a representation of the Group Membership protocol word used by the distributed gateway computer of Figure 4 in communicating status information in the computer system of the invention.

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Figure 8 is a flow diagram of the operating steps executed by a distributed gateway computer of Figure 3 in starting up and processing group membership messages on a subnet of the system.

Figure 9 is a flow diagram that shows details of the group membership message processing performed by each of the distributed gateway computers of Figure 3.

Figure 10 is a representation of a GUI setup screen as shown on the display device of the Figure 6 computer, in accordance with the present invention, for setting up primary IP addresses.

Figure 11 is a representation of a GUI setup screen as shown on the display device of the Figure 6 computer, in accordance with the present invention, for setting up virtual IP addresses.

Figure 12 is a representation of a GUI screen as shown on the display device of the Figure 6 computer, in accordance with the present invention, for a Remote Management Console screen for running the distributed gateway cluster from a remote computer.

Figure 13 is a representation of the Remote Management Console screen of Figure 12, showing the Edit menu for entry of cluster configuration data.

Figure 14 is a representation of a token message train, sent by the distributed gateway servers illustrated in Figure 3.

Figure 15 is a flow diagram that shows the operating process of a distributed gateway in the system of Figure 3 to provide IP address reassignment without server OS rebooting.

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Figure 16 is a flow diagram that shows the operation of a distributed gateway in the system of Figure 3 to provide symmetric routing of traffic through the gateway server cluster.

Figure 17 is a schematic block diagram that illustrates the data traffic in the server cluster operation according to Figure 16.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 3 is a representation of a computer system 300 constructed in accordance with the present invention. A system constructed in accordance with the present invention is set up to include at least two computers acting as a distributed traffic control center, or gateway, between two networks. The Figure 3 system 300 includes four machines 302, 304, 306, 308 that act as a distributed gateway 310 between an external subnet 312 interface to the Internet 314 and two internal subnets 316, 318. The four machines control network traffic to and from the internal subnets. The four machines can dynamically reconfigure traffic assignments among themselves and provide increased network availability. For example, if one of the machines 302, 304, 306, 308 becomes unavailable, traffic assignments are moved among the remaining machines such that network availability to host machines on the internal subnets 316, 318 is substantially unchanged. In the illustrated embodiment of Figure 3, the external network is the Internet, and therefore the data traffic being handled by the gateway 310 follow the TCP/IP protocol model, but it should be understood that other network protocols may be accommodated by a distributed gateway constructed in accordance with the invention, without departing from the teachings of the invention.

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As described further below, the machines 302, 304, 306, 308 of the distributed gateway 318 communicate with each other such that dynamic traffic assignment reconfiguration occurs automatically in response to any machine being added or deleted from the gateway 310, with no loss in functionality for the gateway. The reconfiguration process is transparent to local network users, thereby providing a distributed gateway functionality that is scalable. Each machine of the gateway may implement an operational function, such as web server, e-mail server, or encryption services, and can continue with its operational functions while it participates in the distributed gateway and dynamic reconfiguration processing. In this way, the invention substantially maintains network availability regardless of machine failures, so that there is no single point of failure and no lapse in gateway functionality.

Each machine 302, 304, 306, 308 of Figure 3 is associated with an Internet protocol (IP) address that uniquely identifies the machine and provides an address that is associated with a network interface card (NIC) of the respective machine. This IP address, which is associated with a physical resource such as the NIC, will be referred to as a primary (or physical) IP address, and is an address off of the respective subnet 316, 318. Those skilled in the art will understand that each of the machines includes a NIC interface for each network (internal and external) to which the machine is connected.

In accordance with the invention, the machines 302, 304, 306, 308 provide a distributed gateway by maintaining a set of dynamically assignable IP addresses for each subnet 312, 316, 318. The set of assignable IP addresses for each subnet is called a virtual IP pool. Each subnet 312, 316, 318 in Figure 3 is identified with a respective virtual IP pool

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322, 324, 326. Software that provides the distributed gateway functionality is installed in each of the machines 302, 304, 306, 308. Thus, in Figure 3, each one of the gateway machines includes three NIC interfaces, for connection of the respective machine to the external subnet 312 and the two internal subnets 316, 318, and each of the machines is associated with a primary IP address and with a virtual IP address for each subnet.

Because of the distributed gateway software installed at each machine, users or host machines on both sides of the gateway 310 will know of and will direct data packets to an address in one of the virtual IP pools, rather than the primary IP address associated with each gateway machine. Thus, a router 320 that directs data traffic to the computers behind the gateway 310 will be aware of only the IP addresses in the virtual IP pool 322 on the external subnet and will not be aware of the primary IP addresses assigned to the NIC cards of each respective gateway machine 302, 304, 306, 308. Similarly, the internal host machines 330, 332, 334 behind the gateway 310 will be aware of only the IP addresses in the virtual IP pools 324, 326 on the respective internal subnets 316, 318 and will not be aware of the primary IP addresses assigned to the NIC cards in the gateway machines for each connection to an internal subnet.

As described more fully below, the dynamic assignment of virtual IP addresses to primary IP addresses permits reconfiguration in response to machine problems and in response to variations in network traffic loading among the machines. If a gateway machine becomes unavailable, then the virtual IP address (or addresses) for which it was responsible are simply assigned to one or more different gateway machines. This capability is referred to as a fail-over capability. A related feature is the scalability of the system, such that the

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system automatically reconfigures itself dynamically as machines are added or deleted. This also permits more efficient workload distribution among the gateway machines. If a gateway machine becomes heavily burdened with data traffic, one or more of the virtual IP addresses assigned to it will instead be assigned to one or more different gateway machines.

System Software Components

Figure 4 is a representation of a gateway computer in Figure 3, illustrating the system architecture 400 of the gateway constructed in accordance with the present invention. Those skilled in the art will understand that Figure 4 is a system architecture representation in terms of the Open Systems Interconnection (OSI) networking model published by the International Standards Organization.

The lowest level of the system architecture is the Physical layer, Layer 1, where data packets are received at a cable connection 402 from the distributed gateway machine to a subnet, which in the preferred embodiment typically comprises an Ethernet peer-to-peer network. The next OSI level is the Data Link layer, which packages data bits received from the physical layer into data frames that are processed by the higher layers. The Data Link layer is responsible for providing an error-free transmission of data frames between computers through the Physical layer. For example, data packets in the gateway machine are physically received at a network interface card (NIC) of the gateway from a network cable connection. Figure 4 shows the data link layer function being performed by a NIC Driver 404, which may be a conventional driver program for processing data traffic received in

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accordance with the Ethernet protocol, or whatever protocol is used for the associated subnet with which the NIC communicates.

The Network layer of the OSI system model is responsible for addressing messages and translating logical addresses into physical addresses. This layer determines which path data will take from a source computer to a destination computer. In Figure 4, the Network layer is occupied by the Application Wrapper Driver 406 and the Application Driver 408. The Application Wrapper Driver refers to the driver for the application wrapper software that provides the distributed gateway functionality of the present invention. The Application Driver refers to the driver for the application software with which the gateway machine operates. For example, the distributed gateway may be operated in conjunction with firewall software, to provide a distributed firewall gateway. Alternatively, the application software may comprise an e-mail server, in which case the invention provides a distributed mail server with extremely high availability. Other application software may work with the distributed gateway software of the invention to provide the desired gateway functionality.

The next layer in the OSI model is the Transport layer, which in Figure 4 is represented by the TCP/IP stack 410. The Transport layer repackages messages so as to avoid errors and ensure data is in the proper sequence. The details of this OSI layer in general, and the TCP/IP functioning in particular, will be well understood by those skilled in the art. In the Application/Presentation layer, the distributed gateway of the invention includes the Application Wrapper 412 and the Application 414 software. The Application module 414 refers to software that performs conventional functions, in concert with the distributed functionality of the present invention. For example, the Application module may

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provide firewall processing, e-mail services, or web page server functionality. As noted above, the Application Wrapper 412 is the software that provides the distributed gateway functionality in accordance with the invention, while the Application is the operational software whose functionality is enhanced, so as to be scalable and distributed, by the Application Wrapper software.

Figure 5 shows details of the Application Wrapper 410 to better illustrate the architecture of the distributed gateway. One component function of the Application Wrapper is the Virtual IP Address module 502, which maintains the virtual-to-primary IP address mapping between the primary addresses and the virtual IP address pool. Consistent State Sharing 504 is a module that permits the gateway machines to know which machines are functioning and which virtual IP addresses have been assigned to each of the machines. The Reliable Communication 506 component tracks acknowledgment messages communicated around the gateway, and also helps implement Group Membership Management 508, which keeps track of the available machines. Network operations are monitored by the Global Fault Monitor 510, which is complemented by a Local Fault Monitor 512 for the particular machine on which the Application Wrapper is running. A Local Load Monitor 514 determines the data flow rate through the NIC interface in bytes to keep track of machine loading. The Dynamic Load Balancing 516 ensures that no single gateway machine becomes overloaded. It does this by moving virtual IP address assignments, if necessary, in view of the monitored local loads. The Transparent Fail-Over 518 ensures that a failed machine is quickly replaced with an alternative machine, thereby providing high availability in a manner

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that is transparent to users. These functions operate in conjunction with overall Network Management tasks 520 performed by the gateway software.

Computer Construction

Figure 6 is a block diagram of a gateway computer in the system of Figure 3, illustrating the hardware components for one of the computers. Those skilled in the art will appreciate that the gateway computers 302, 304, 306, 308 and the internal host computers can all have a similar computer construction.

Figure 6 is a block diagram of an exemplary computer 600 such as might comprise any of the computers 302, 304, 306, 308. Each computer 600 operates under control of a central processor unit (CPU) 502, such as a "Pentium" microprocessor and associated integrated circuit chips, available from Intel Corporation of Santa Clara, California, USA. A computer user can input commands and data from a keyboard 504 and can view inputs and computer output at a display 606. The display is typically a video monitor or flat panel display. The computer 600 also includes a direct access storage device (DASD) 607, such as a hard disk drive. The memory 408 typically comprises volatile semiconductor random access memory (RAM). Each computer preferably includes a program product reader 610 that accepts a program product storage device 612, from which the program product reader can read data (and to which it can optionally write data). The program product reader can comprise, for example, a disk drive, and the program product storage device can comprise removable storage media such as a magnetic floppy disk, a CD-R disc, a CD-RW disc, or

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DVD disc. Each computer 600 can communicate with the others over the network through a network interface 614 that enables communication over a connection 616 between the network and the computer. The network interface typically comprises, for example, a Network Interface Card (NIC) that permits communications over a variety of networks. In the gateway 310 (Figure 3), the network can comprise an Ethernet network or can comprise a connection to the Internet.

The CPU 602 operates under control of programming steps that are temporarily stored in the memory 608 of the computer 600. When the programming steps are executed, the Distributed Gateway machine performs its functions. Thus, the programming steps implement the functionality of the distributed system architecture modules 100 illustrated in Figure 5. The programming steps can be received from the DASD 607, through the program product storage device 612, or through the network connection 616. The storage drive 610 can receive a program product 612, read programming steps recorded thereon, and transfer the programming steps into the memory 608 for execution by the CPU 602. As noted above, the program product storage device can comprise any one of multiple removable media having recorded computer-readable instructions, including magnetic floppy disks and CD-ROM storage discs. Other suitable program product storage devices can include magnetic tape and semiconductor memory chips. In this way, the processing steps necessary for operation in accordance with the invention can be embodied on a program product.

Alternatively, the program steps can be received into the operating memory 608 over the network 314. In the network method, the computer receives data including program steps into the memory 608 through the network interface 614 after network communication has

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been established over the network connection 616 by well-known methods that will be understood by those skilled in the art without further explanation. The program steps are then executed by the CPU to implement the processing of the Distributed Gateway system.

It should be understood that all of the computers 302, 304, 306, 308 of the computer system illustrated in Figure 3 have a construction similar to that shown in Figure 6, so that details described with respect to the Figure 6 computer 600 will be understood to apply to all computers of the system 300. Alternatively, any of the computers 302, 304, 306, 308 can have an alternative construction, so long as they can communicate with the other computers and support the functionality described herein.

Group Membership Protocol Word

The fail-over operation, scalability of the system, assignments of virtual IP (VIP) addresses to machines, and the ability to dynamically reconfigure such assignments, are achieved with the distributed gateway software through a Group Membership protocol word that provides state sharing information among all the machines in a cluster. The state-sharing protocol word is passed around the cluster machines who are members of the same subnet in a token ring arrangement that will be familiar to those skilled in the art.

Figure 7 is a representation of the Group Membership state protocol word 700 that is used by the cluster computers of Figure 6 in communicating the state information among the machines of the distributed gateway. The state protocol word 700 includes a Signal Type (SIG) field 702 that indicates whether the word is a token message for normal operating

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conditions or is a notification message (also called a "911" message). The next field is a Sequence (SEQ.) field 704 that is incremented by each node as the message makes its way around the nodes of the cluster. The next field is a Membership field 706 that indicates the group composition of the cluster, followed by a VIP list and assignments field 708 (Group Composition) to reflect cluster configuration data, and finally there is an Operational Data field containing load and byte count data 710 that indicates the data flow rate through a node. In particular, the data flow rate is indicated by information retrieved from the NIC of the node. Each received Group Membership message, whether it is a normal token message or a "911" message, is parsed by the distributed gateway software of each particular cluster machine to extract the necessary data.

The Sequence number field 704 is incremented by each node when it receives a message (a token message or 911 message). An initial random sequence number is selected as a default start value, and when the sequence numbering reaches a predetermined limit value, the sequence numbering wraps around and begins at the start value. When a node puts a message on the subnet, the node increments the sequence number that was contained in the received token, places the incremented token back out on the subnet, and stores the incremented number in memory. Thus, any message produced by a node will have a unique sequence number. A node should not receive a token message with a sequence number lower than the sequence number stored in its memory.

The Membership field 706 in a token message is a collection of sub-fields to indicate group composition. In particular, the Membership field of the preferred embodiment contains data that provides the number of nodes in the cluster, a list of the nodes, the current

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node sending the token message, and the destination node (the next node in the cluster, the node to whom the message is being sent). Each node changes the appropriate membership field values when the node receives the token, and in this way ensures that the token is passed along the machines in the cluster, from node to node in proper sequence.

For example, the "number of nodes" field in a token message might indicate a cluster having four nodes, such as illustrated in Figure 3. The token message might indicate subnet addresses of (1.1.1.1), (1.1.1.2), (1.1.1.3), and (1.1.1.4) in the "list of nodes" data of the Membership field 706. If the nodes are numbered, from first to last, as -1, -2, -3, and -4, and if, at a particular point in time, the token is being sent from the second node (node -2) and is received at the third node (-3), then the "current node" value is "2" (the second node in the cluster) and the "destination node" value is "3" (the third node). After the third node (-3) receives the token, the third node changes the "current node" to "3", changes the destination node to "4", and sends the token back out on the subnet to the next node. In this way, each node always knows whether it is the intended recipient of a token message.

The Membership field 706 in a "911" message includes two sub-fields comprising an originating node address and a permission flag. A "911" message is sent by a node (the "originating node") when that node determines that the token message might have been lost somewhere in the cluster, and therefore might need to be regenerated. This may occur, for example, if another node fails when it has possession of the token message for processing. In that case, the originating node needs to determine if it has the latest copy of the token to regenerate the token. This determination is made with the help of the "911" message.

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As a "911" message is sent around the machines of a distributed gateway cluster, the permission flag value in the message is set to TRUE by each node when it receives the "911" message, unless a receiving node has a higher sequence number stored in its memory for the last token message it sent out. If the receiving node has a higher sequence number, then it sets the permission flag to FALSE before putting the "911" message back out on the subnet. When the originating node receives back the "911" message, it will examine the message to determine if the permission flag sub-field contains TRUE or FALSE. If the permission flag is FALSE, then the originating node will not regenerate the token message it has in memory. That is, when the "911" message received by the originating node says FALSE, that means another node has already sent out a more recent token, with a higher sequence number. Therefore, the originating node will wait for the next token message (having a higher sequence number), and will adopt the system values (VIP list, membership, etc.) that are indicated in that token. If the originating node receives a "911" message back with TRUE, then the originating node knows it has the most recent token, so it will re-send the last token message it has, with all its system values (VIP list, membership, etc.). The unique sequence number ensures that only one node, the one with the most recent token message, will change the permission flag to TRUE.

The Group Composition field 708 of the Group Membership protocol word 700 contains a list of virtual IP addresses (VIP list) and of corresponding node assignments for those addresses. The Group Composition field contains sub-fields of data that specify the VIP address, the primary IP address to which that VIP address is currently assigned, an indication for each VIP address whether there is a preference for assignment to that address,

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and a persistence or "sticky" flag to indicate whether the preference is sticky. A sticky VIP address assignment means that the VIP address will be forced to an assignment to that particular node, so that all traffic for that VIP address must be directed to that node, unless the machine is unavailable. Thus, a sticky assignment in the Membership field means that all data traffic for that node will be directed to that node, if the node is available. If the node fails, traffic will be re-routed. If the node comes back up, then the data traffic intended for the node will again be directed to that node. A persistence flag set to a non-zero value indicates that a user has indicated a preference for assigning that VIP address to the node involved.

For example, if there are four addresses in the VIP list, then the information in the Group Composition field 708 might be summarized in Table 1 below:

Table 1.

VIP Address	Current Host	Preferred Host	Persistence Flag
1.1.1.1	1.1.1.5	1.1.1.6	0
1.1.1.2	1.1.1.5	1.1.1.5	1
1.1.1.3	1.1.1.6	0.0.0.0	0
1.1.1.4	1.1.1.6	1.1.1.6	3

As Table 1 shows, the Group Composition field 708 contains four sub-fields: VIP address, Current Host, Preferred Host, and Persistence Flag. Each of the first three fields

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holds the value of an IP address. The last field is an integer. In the preferred embodiment, data in the Group Composition field 708 will be placed in sequence, so that data for the first row of Table 1 is listed in the Group Composition field, followed by data for the second row, and so forth. Other schemes for packing the Group Composition field may be used.

In the Group Composition data, there is one VIP address sub-field, providing a VIP list for the entire cluster. The first sub-field, VIP address, lists the VIP addresses for the entire distributed gateway cluster. The second sub-field, Current Host, specifies which node currently owns this particular VIP address. The primary IP address of that node is used in the Current Host value. For example, according to Table 1, node (1.1.1.5) owns, or is assigned, VIP addresses (1.1.1.1) and (1.1.1.2). The third sub-field, Preferred Host, indicates the node at which this VIP prefers to be hosted. For example, to move VIP address (1.1.1.1) from Node (1.1.1.5) to Node (1.1.1.6), it would be necessary to specify Current Host as (1.1.1.5), and Preferred Host as (1.1.1.6). The VIP address assignments indicated by the Current Host and Preferred Host data sub-fields can be changed by a user during real-time operation of the distributed gateway application through a user interface, which is described in greater detail below.

The last sub-field of the Group Composition data is the Persistence Flag. It indicates whether the associated VIP address is "sticky" to the Preferred Host. When a VIP address is "sticky" to an assigned node (the one it is associated with in the same row of Table 1), it is no longer handled by the load balancing process of the distributed gateway application wrapper. The Persistence Flag field can take three possible integer values: "0", "1" and "3". When it is "0", it means that the associated VIP address is not sticky to any node. This VIP address

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can be moved, if so required by the load balancing process. When the Persistence Flag is "1", it means this VIP address is sticky to the Current Host specified in the same row of Table 1, and therefore it is not handled by the load balancing process. If the Current Host fails, this VIP address assignment will move to another node of the subnet, and will become sticky to that node. It will stay on that node even if the original Host recovers. When the Persistence Flag is "3", it means this VIP address is sticky to the Preferred Host.

Whenever the Preferred Host is functioning (alive), the VIP address will move to the Preferred Host node and stay with it (becomes "sticky" to it). When the Preferred Host fails, it fails over to another node of the subnet. The VIP address will move back to the Preferred Host when the Preferred Host recovers. It should be noted that regardless of which value the Persistence Flag takes, when the Current Host fails, the associated VIP address will always fail over to a healthy (alive) node. As described further below, the "sticky" feature of a VIP address assignment can be changed by a user in real time through a system interface.

Returning to Figure 7, the last data field of the protocol word 700 is the load and byte count data field 710. This data field indicates the traffic flow of message packets through each of the distributed gateway machines of the cluster subnet. In the preferred embodiment, the data comprises a byte count of data through the network interface card that connects each distributed gateway machine to the subnet. As with the group composition field 708, the byte count field 710 is organized in the protocol word such that the data for the first node occurs first, then the second node, then the byte count data for the third node, and so forth for each of the machines in the cluster who are connected to the pertinent subnet.

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In accordance with the invention, the protocol word 700 is circulated around the subnet from machine to machine, in sequence. Each machine receives a protocol word as part of the group membership message that is passed from machine to machine approximately at a rate of once every 100 milliseconds. Other message passing rates may be used, depending on the network configuration and machine operation.

Machine Operation

Figure 8 is a flow diagram of the operating steps executed by a distributed gateway computer of Figure 3 in starting up and processing group membership messages on a subnet of the system. This processing is executed by the computer from its program memory once the appropriate distributed gateway application software is loaded onto the computer and the setup operation (described below) has been completed.

In the first processing step performed by the starting computer, represented by the flow diagram box numbered 802, the configuration data of the machine is read from the direct access storage device, such as the hard disk of the computer. The configuration data includes a number of stored configuration files, including a node map, the virtual IP addresses of the cluster, cluster configuration options, local fault monitoring specifications for the machine, and a license key or password. The node map contains the primary IP addresses of all the nodes in the cluster, in an arbitrary ordering around the subnet that is determined by the user during the setup process. The configuration files specify the "initial" cluster setup. Users can change these settings at runtime with the user interface described

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below. Such runtime changes will not affect the configuration files, though a user may manually edit them with a text editor.

From the node map of the configuration data, the computer that is starting up knows whether it has companion machines in the subnet cluster, and it knows how many additional machines to expect in the cluster. Therefore, the starting computer next will attempt to contact all of the other machines on the subnet and determine if it is the first executing machine in the cluster. This process is represented by the decision box numbered 804.

The process of a starting computer to determine if it is the first operational node involves first sending a unicast UDP (User Datagram Protocol) packet message. The UDP message implements a conventional connectionless protocol message that provides a means of sending and receiving datagrams over a network. Those skilled in the art will be familiar with the use of UDP packet messages. The UDP message sent by a starting computer includes a Group Membership protocol word, as described above in conjunction with the description of Figure 7.

If the starting computer is actually attempting to recover or regenerate a token, and is not involved in an initial start sequence, then it could use the UDP message to send a "911" or notification message, as described above. When the computer rejoins the cluster, it will use the current cluster setup information in a token message for the cluster properties. If the starting computer is actually starting up from a cold start, then the UDP message will comprise a token message, such as that described above, that includes all the node data and configuration information that the starting computer retrieved from its configuration files. In either case, the computer that sends out the message waits for a reply.

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If the starting computer receives no replies to the message for all other nodes in the configuration, then it knows it must be the first node in the cluster. This corresponds to an affirmative (YES) outcome at the decision box numbered 804. If the starting computer is the first cluster computer, then it assumes responsibility for all the VIP addresses in the cluster. Thus, it will set the data fields in the Group Membership protocol word accordingly, and continue data traffic handling operation while it waits for the other machines of the cluster to join. In accordance with operation of the cluster machines of the invention, the starting computer will send out a gratuitous ARP (Address Resolution Protocol) message for each VIP address that it takes. This mode of operation is referred to as "alone mode", and is indicated by the Figure 8 flow diagram box numbered 806.

Those skilled in the art will be familiar with the conventional ARP scheme for translating logical IP addresses into physical network interface addresses in conjunction with stored address resolution information. More particularly, the network interface addresses are also known as Media Access Control (MAC) addresses for network cards. The ARP message is a conventional means of storing logical to physical address data in the machines connected to a network, such as each of the subnets connected to the starting computer. Thus, for each subnet to which it is connected, the starting computer will determine if it is the first node and, if it is, the starting computer will send out a gratuitous ARP message for the VIP addresses that it is taking.

If the starting computer receives a reply to the UDP message, then it knows other machines are active in the cluster, and it will attempt to join the cluster. This corresponds to the "join cluster" processing of box 808, following the negative outcome (NO) of the

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decision box 804. Any node that is already active and has received the UDP message from the starting computer will accept the starting computer into the operating cluster, in the following manner.

As noted above, a starting computer will send a 911 message with a Group Membership protocol word over the subnet with the data it has retrieved from its configuration files. When the operating node receives the 911 message from the starting computer, the operating node processes the node list in the message and adds the starting node into the list, as appropriate. Thus, permanent connections specified by initial data may indicate a particular VIP address assignment, or predetermined default assignments may be used. In either case, the operating node adds the new node into the node list data and then puts the processed Group Membership token back out onto the subnet. When the starting computer receives back the Group Membership token, it will process the node assignment data to reflect the presence of the operating node, and it thereby becomes part of the cluster. The starting computer will then pass the Group Membership token along, back out onto the subnet, in its normal operation.

Figure 9 is a flow diagram that illustrates the Group Membership message processing performed by each of the distributed gateway computers of Figure 3 during normal operation, as a node in a cluster. In general, for the distributed gateway application software, a token acts as a failure detector. Therefore, if a token does not reach the specified destination node from a current node, the current node will assume the destination node is down. As a result of not receiving an acknowledgment, the current node will modify the group membership information on the token accordingly, and will send the token to the next node in the subnet

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cluster, past the previous destination node. In contrast to the token processing described above, a "911" message will not modify the membership on the token when the destination cannot be reached. It will simply increment the destination node, and send to the next node in the subnet ring. This processing is illustrated in Figure 9, as explained further below.

First of all, if a node has not received a Group Membership message from another node for greater than a time-out interval, then the node will send out a "911" notification Group Membership message, as was described above in conjunction with Figure 7. This processing is represented by the flow diagram box numbered 901. In the next step of normal message processing, represented by the Figure 9 flow diagram box numbered 902, the node receives a Group Membership message. The node next determines whether the message is a token message or a "911" notification message, by examining the signal type message field described above in conjunction with Figure 7. If the message is not a token message, then it is a "911" message, a negative outcome at the decision box numbered 904. As indicated by the flow diagram box numbered 906, the node will process the "911" message to examine the sequence number, determine if the sequence number it has is greater than the received sequence number, and process the permission flag. The node may determine that the "911" message is one that it sent, in which case it may need to regenerate the last token message it sent (if permission = "TRUE"). In that case, it will regenerate the token, and put the message token back out onto the subnet. If it did not send the "911" message, then the node will determine if it has a sequence number greater than that in the message. If it has a higher sequence number, it will set the permission flag (FALSE) accordingly, and send the message back out onto the subnet. If the node does not have a higher sequence number, it does not

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change the permission flag setting, and the sends the message onto the subnet to the next node.

Whether or not the originating node changes the permission flag, it waits for an acknowledgment from the next node (the destination node) after sending the "911" message back out onto the subnet. This is represented by the decision box numbered 907. If the originating node receives a response, an affirmative outcome at the decision box numbered 907, it continues with normal processing. If the originating node does not receive an acknowledgment response within the timeout interval, a negative outcome at the decision box 907, then the originating node increments the destination node in the "911" message to skip the non-responsive node on the subnet, and sends out that modified "911" message. This processing is represented by the flow diagram box numbered 908. The originating node then waits for that new destination node to respond, in accordance with the decision box 907.

Token failure detection generally assumes that failure to receive an acknowledgment within a predetermined time interval indicates that a message never reached the destination node, and therefore assumes that the destination node is down. Such failure detection is not totally reliable, however, as a failure to respond within the time interval may simply indicate a slow node. Thus, in an asynchronous network environment, a reliable failure detector is virtually impossible to build, since one cannot tell a "dead" or down node from a "very slow" node. Under operations of the distributed gateway application software, however, if a "slow node" is mistaken for a "dead node" and is deleted from the list of active nodes, then the slow node will rejoin the cluster automatically. This is accomplished because of the following sequence of events: When a slow node is waiting for the token to arrive, its timeout interval

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will expire. That node will then send out a "911" message, thinking that the prior node is down. The "911" message will be regarded by the other nodes as an add request to join the cluster, and that slow node will effectively be added back into the distributed gateway cluster.

If the received Group Membership message is a token message, an affirmative outcome at the decision box 904, then the node processes the information contained in the message. This processing is represented by the flow diagram box numbered 909. Thus, changes in VIP address assignments may be received, or changes in such assignments may need to be implemented, in response to load information in the operational data. At the decision box numbered 910, the node may determine that a change in VIP address assignment is needed. The node may make this determination, for example, if the load level it is experiencing, or if the load level it sees another node experiencing, exceeds a predetermined byte rate load level limit.

Thus, individual nodes in a cluster may observe the configuration and operational data in a token message and recognize that another node in the cluster is receiving a sufficiently great amount of data traffic, due to its VIP address assignments, that the performance of the cluster as a group could be improved if the load of the other node is reduced. If that is the case, then the message processing node that has received the token message and has observed the need for reassignment will proceed with a VIP address reassignment in which the processing node will reassign one or more VIP addresses from the overloaded node to itself, or even reassign VIP addresses from itself to another node. For example, each processing node that recognizes an overloaded condition may take one additional VIP address assignment. If the next node that receives the token message sees that

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the overloaded condition still exists, it will take another VIP address assignment for itself. In this way, dynamic load balancing will occur during real time operation of the cluster.

If the processing node determines that a reassignment of VIP addresses is needed, an affirmative outcome at the decision box 910, then the node will implement whatever reassignment its processing dictates by changing the VIP address data in the Group Composition field 708 (Figure 7) of the token message. Whenever there is a new or changed VIP address assignment, the node making the change sends out the ARP message mentioned above in connection with startup processing. Unlike the startup processing, however, this ARP message occurs during normal processing, and is prompted not by startup processing but by the desire to change assignments and inform the other nodes. The message is therefore referred to as a "gratuitous" ARP message. This processing is represented by the flow diagram box numbered 912. Those skilled in the art will understand that each machine connected to a subnet includes an ARP cache that contains data to translate logical IP addresses into physical MAC addresses, and will further understand that an ARP message is a message that is sent out over a network and is automatically processed by any computer communicating with that network to store the ARP message information into the ARP cache of the computer. The clients and routers on the subnet will receive the ARP message and will then automatically refresh their respective ARP caches with the new assignment information. All such processing is incorporated into the processing of the flow diagram box numbered 912.

After the token message is processed, with or without VIP address changes, the node increments the sequence number and changes the current node and destination node data

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fields of the message, as described above with respect to Figure 7. The node then sends the token message back out on the subnet to the next node. This processing is represented by the flow diagram box numbered 916.

After the originating node sends the token message onto the subnet, it waits for an acknowledgment from the destination node. If the originating node receives a response, an affirmative outcome at the decision box numbered 918, it continues with normal processing. If the originating node does not receive an acknowledgment response within the timeout interval, a negative outcome at the decision box, then the originating node modifies the active membership list for the cluster to delete the non-responsive node, then increments the destination node number on the subnet to skip the non-responsive node, and sends out that modified token message onto the subnet. This processing is represented by the flow diagram box numbered 920. The originating node then waits for that new destination node to respond, in accordance with the decision box 918.

Graphical User Interface

The software to implement the distributed gateway processing described above (the Application Wrapper module of Figure 4) is installed into program memory of a computer that is to become part of a distributed gateway cluster in accordance with the invention. In the preferred embodiment, the software provides a graphical user interface (GUI) in both the program setup mode and in the program operational mode. Thus, a user will be shown GUI display screens to guide the user through setup and operation. Those skilled in the art will be

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familiar with GUI display screens and the manner in which they are created, displayed, and manipulated by users.

Figure 10 is a representation of a GUI setup screen 1000 as shown on the display device of the Figure 6 computer, in accordance with the present invention, for setting up primary IP addresses of the distributed gateway cluster. The setup screen of Figure 10 appears on the user computer display as a window when the setup program of the Application Wrapper (Figure 4) is launched. As Figure 10 indicates, the setup program of the distributed gateway first asks the user to set up the internal IP addresses (the primary IP pool) for each computer that will be a part of the distributed gateway cluster. In the exemplary data of Figure 10, the cluster has four IP addresses, represented by (1.1.1.1), (1.1.1.2), (1.1.1.3), and (1.1.1.4). These IP addresses are entered into an IP address list box 1002 one by one after the user enters them into a text box 1004. The IP addresses can be added and deleted by using the Add 1006 and Remove 1008 buttons of the setup window. When the numbers in the primary IP address pool have been entered, the user is ready for the next setup window, to which the user proceeds by selecting the Next button 1010.

Figure 11 is a representation of a GUI setup screen 1100 as shown on the display device of the Figure 6 computer, in accordance with the present invention, for setting up virtual IP addresses. After the addresses of the primary IP address pool have been set, the setup program must next process the virtual IP address pool. When the user selects the Next button 1010 from Figure 10, the distributed gateway program initiates a system check for network interface (NIC) cards. In the example of Figure 11, the program has displayed a message in the virtual IP (VIP) address setup window 1100 that indicates finding a NIC with

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an IP address of (1.1.1.2). It should be understood that the system check will find each NIC that is installed into the node computer, and that Figure 11 simply illustrates one of the display windows that will be shown during the entire setup process.

The Figure 11 display window 1100 indicates that the user should now enter the virtual IP address pool of addresses that will be associated with the NIC that has a primary IP address of (1.1.1.2). As indicated in the virtual IP address list box 1102, the subnet virtual IP addresses for this NIC will be (1.1.1.91), (1.1.1.92), (1.1.1.93), and (1.1.1.94). These addresses will be entered by the user with the virtual IP address text box 1104 and the Add button 1106 and Remove button 1108. The user must enter the virtual IP addresses for each machine being configured. It should be apparent that the list of virtual IP addresses should be the same for each machine on the subnet. It also should be clear that each subnet will have a set of virtual IP addresses entered for it, for both the external subnet(s) and the internal subnet(s).

After the setup procedure has been completed, the user must input the configuration parameters for the cluster. Configuring the distributed gateway cluster in accordance with the invention involves modifying the configuration files first described above. In a conventional window programming environment, for example, these files include a node map configuration called "nodemap.cfg" that will list the primary IP addresses for the gateway machines. Another configuration file is "vip.cfg", which determines the virtual IP addresses in the VIP address pool for each subnet connected to the cluster. These configuration files contain configuration data in a text format, in which the IP addresses are simply listed, for example. The distributed gateway application will know the nature of the data contained in

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each configuration file because the file names are predetermined. For example, a standard windowing operating system (such as "Windows NT" by Microsoft Corporation of Redmond, Washington, USA) will process a file name with a ".cfg" suffix as a text file, containing characters of a standard ASCII alphanumeric set. The configuration file contents may be easily edited by the user, using a command line editor utility of the distributed gateway or other suitable utility.

For example, the "vip.cfg" file may contain the text data shown below in Table 2:

Table 2.

virtual IP Pool
VIRTUAL_IP 131.143.36.0 {
131.143.36.91
131.143.36.91
131.143.36.91
131.143.36.91
}

In addition to the node map and the VIP address list, optional configuration files include the local monitor configuration file "localmonitor.cfg", which is used for specifying fault detection behavior of the machine. As described more fully below, the monitor

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functions that can be specified includes parameters for triggering monitoring of local NIC's, monitoring of the application (firewall), and monitoring of the remote hosts/router combination via the "Ping" protocol.

The NIC monitoring function tests the network interface cards in the local machine to determine if the cards are still functioning properly. The system can set this parameter to a default value. Details of the testing for NIC functionality will depend on the NIC being used, and will be understood by those skilled in the art.

Monitoring of the remote hosts/router involves testing the application (in the preferred embodiment, a firewall) for proper operation. In the case of a firewall application, the testing would involve generating "dummy" packets and checking to see if the firewall rejects or accepts such packets, based on the rules required by the firewall application. That is, the distributed gateway software (the Application Wrapper of Figure 4) would interface with the Application (Figure 4) to periodically generate predetermined dummy packets of a type that should be accepted by the firewall Application, and that should be rejected by the firewall. The distributed gateway software would then report the results as part of the GUI, as described further below.

Details of interfacing the distributed gateway software with the firewall software will depend on the firewall software being used. Those skilled in the art will understand how to implement such an interface, in accordance with the description herein. To properly interface the two applications, the default gateway of hosts or routers external to the distributed gateway should be set to one of the IP addresses from the external virtual IP address pool for the subnet of that host or router, and the default gateway of hosts or routers internal to the

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distributed gateway should be set to one of the IP addresses from the internal virtual IP address pool for the subnet of that host or router.

The use of the "Ping" function to monitor the remote host/router will be apparent to those skilled in the art, where the distributed gateway software will assume that a remote host/router is not functioning properly if it does not respond to a conventional "Ping" message within a predetermined time interval. In accordance with the invention, the Ping function may be activated and deactivated by setting a parameter in the "localmonitor.cfg" file, such as by inserting an "enableMonitor()" entry into the text file and inserting an IP address to be pinged by using an entry of the form "addMachine(IP address)". The function may be deactivated by including a "disableMonitor() entry into the text file.

By editing the configuration file, a user may directly set and modify operating parameters of the distributed gateway. Alternatively, the distributed gateway software may permit changing one or more of the parameters through the GUI display screens, as described further below.

Figure 12 is a representation of a GUI screen 1200 as shown on the display device of the Figure 6 computer, in accordance with the present invention, for a Remote Management Console screen for running the distributed gateway cluster from a remote computer. The Remote Management Console is generated by the distributed gateway application software and permits setting operating parameters of the distributed gateway, as well as monitoring the functioning of the gateway. The screen 1200 shows the status of a single machine in the distributed gateway, selected in accordance with a secure procedure described further below.

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The Remote Management Console screen 1200 is shown on the display device of the computer (Figure 6) and, in accordance with a window operating system for a GUI, includes conventional program window artifacts. Thus, the display screen includes a window title bar 1202 across the top of the screen with window sizing icons 1204. A menu bar 1206 provides a means for selecting user actions, such as opening files, editing file contents and system parameters, changing the display details, and requesting help information. The lower part of the display screen 1200 includes a graphical representation of the gateway machines 1208.

Each respective gateway machine is represented in the Remote Management Console screen 1200 with a separate area. For example, in the illustrated embodiment, there are four virtual IP addresses for the machine being monitored, comprising (1.1.1.91), (1.1.1.92), (1.1.1.93), and (1.1.1.94). Thus, these four VIP addresses are represented by four separate screen areas 1210, 1212, 1214, 1216 containing various icons. In the preferred embodiment, the exact shape and theme of the icons can be selected by the user. A general boxed shape is used in the drawing figures, for simplicity of presentation. Where details of one screen area 1210, 1212, 1214, 1216 are provided, it should be understood that the explanation of such details also applies to the other display areas of the Remote Management Console display screen, as all of them are capable of showing the same information.

A Gateway icon 1220 shows the overall status of the particular distributed gateway machine, indicating whether the machine is operational for the virtual IP address and indicating which global options are enabled. In one standard representation form of the icon 1220, the icon indicates that the distributed gateway is fully functional. If an automatic rejoin feature is enabled, the Gateway icon includes an "AUTO" or "A" indication 1222.

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When automatic rejoin is enabled, the distributed gateway machine will attempt to rejoin a cluster after recovery from an error condition that has resulted in a failed machine. The error condition may comprise a failed NIC, a failed firewall application, and the like. In the preferred embodiment, the automatic rejoin feature is enabled as a default condition. In another option, a load balancing feature may be selected. Load balancing is indicated with a suitable Gateway icon display feature, such as "L.BAL" or "L" 1224. If load balancing is selected, the distributed gateway application will move virtual IP addresses from machines with higher traffic loads to machines with lower traffic loads, automatically during normal operation. Load balancing is enabled as a default condition. Finally, the Gateway icon indicates a failed or closed gateway virtual IP address with a suitable "CLOSED" or "X" icon 1226. A user may edit the condition of a gateway and force the gateway condition to be closed, in which condition it will remain until the user opens the gateway again.

In each gateway VIP address screen area 1210, 1212, 1214, 1216, a load bar 1230 shows the current byte traffic load being handled by the machine. The load bar is colored in a vertical "thermometer scale" reading to indicate traffic load, preferably on a logarithmic scale. If a user places the display cursor stationary over the load bar, the GUI will display the numerical value of the traffic load, after a predetermined time interval. On either side of the load bar 1230, columns of IP icons represent the virtual IP numbers managed by a particular machine. Each icon indicates a particular IP address of the internal or external VIP address pool. In the first screen area 1210, for example, the IP icons 1232 to the left of the load bar 1230 represent the internal VIP addresses, and the IP icons 1234, 1236 to the right of the load bar represent the external VIP addresses. A number or character in an IP icon 1232, 1234,

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1236 indicates an IP address that is being managed or handled by the respective machine 1210, 1212, 1214, 1216. A blank icon indicates no assignment.

In accordance with the GUI and system operation, any VIP address can be set to stay on a particular distributed gateway machine by dragging and dropping the IP icons 1232, 1234, 1236 from a machine in one of the screen areas 1210, 1212, 1214, 1216 to a machine in a different one of the screen areas. It should be understood that the GUI will not permit dragging and dropping an IP icon from an external VIP area to an internal VIP area. When an IP icon is moved from one machine area to another, the IP address associated with the IP icon is moved to the new machine. If a user affirmatively moves an IP icon, the distributed gateway application will automatically set the "Preference" flag (described above with regard to the setup procedure) and will change the IP icon to indicate the setting of the "Preference" flag, such as by adding a red dot 1238 to the IP icon. As noted above, an IP address for which the user has indicated a preference assignment (either in setup or by dragging and dropping) will be moved by the distributed gateway application only if the preferred machine fails, or if the preference is removed by the user.

In the preferred embodiment, the GUI permits a user to set and change the VIP address options for a machine by using a conventional display mouse and right-clicking the display mouse when the display cursor is placed over an IP icon. The action of right-clicking causes the GUI to display a preferences menu that permits setting and removing an IP address preference. Setting the IP preference in this way means that the current machine assignment is the preferred assignment for the VIP address, so that the red dot 1238 will show.

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Below the load bar 1230 and IP icons 1232, 1234, 1236 in each display screen area 1210, 1212, 1214, 1216 are placed local monitor icons and condition icons that indicate the status associated with the local monitor components. The local monitor icons include a NIC Load icon 1240, an Application Condition (firewall) icon 1242, and a Ping icon 1244. Each local monitor icon is an identifier that is associated with a condition icon placed directly below it. The condition icons illustrate three different condition levels for their respective associated components and are represented in the preferred embodiment as a traffic signal display.

For example, the NIC Load icon 1240 indicates that the traffic signal 1250 with which it is associated shows the status of the network interface card to the indicated subnet, or the status of the link for that card to the subnet. A red traffic signal (or top-most icon display indication) indicates that the distributed gateway software has detected that the NIC is not functioning properly. A yellow traffic signal (or mid-level icon display indication) indicates that the NIC is not being monitored by the distributed gateway software. That is, the NIC load monitoring feature is either disabled or not supported by the installed software for this component. A green traffic signal (or lower-most icon display indication) indicates that the NIC is functioning properly.

Similarly, the Application Condition icon 1242 indicates that the traffic signal icon 1252 with which it is associated shows the status of the application (firewall) on the local machine. A red traffic signal indicates that the distributed gateway software has detected that the firewall is not functioning properly, a yellow signal indicates that the firewall is not being monitored by the software, and a green signal indicates that the firewall is functioning

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properly. The Ping icon 1244 indicates the status of the ping remote monitor. Thus, a red signal indicates that no timely ping response was received, a yellow signal indicates that the Ping feature is not being monitored, and a green signal indicates that the last ping response was timely received.

The operation of any one of the particular local monitor components 1240, 1242, 1244 can be enabled and disabled by right-clicking on the traffic signal icon for the desired component. Enabling the monitor means that the given component (NIC, application, or ping) will be monitored. If the component is functioning properly, the associated traffic signal icon will be set to green when the component is enabled in this way. If the component has failed, the traffic signal will be set to red. If the component cannot be monitored, such as where a NIC is incompatible with the monitor software, the traffic signal will be set to yellow when the component is enabled in this way.

Remote Monitoring

As described above, the Remote Management Console display 1200 permits changing and monitoring the distributed gateway through the GUI. In accordance with the Remote Management Console and the operation of the distributed gateway software, the cluster can be changed and monitored as described above from any one of the cluster machines, and from a suitably configured remote machine external to the cluster. More particularly, a remote machine can be used if it can communicate with a machine of the cluster and if it has access to the appropriate GUI graphical components. Access to the GUI components can be

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achieved either by installation of the distributed gateway software on the remote machine, or if the appropriate GUI components can be delivered to the remote machine during the cluster monitoring. Such remote monitoring will first be enabled from a machine of the cluster using the Edit menu of the Remote Management Console screen.

Figure 13 is a representation of the Remote Management Console screen 1200 of Figure 12, showing the drop-down Edit menu selections. Figure 13 shows the screen after a user has selected the Edit menu from the menu bar 1206 and caused the Edit menu 1302 to drop down from the menu bar. The menu selections include Add Gateway Monitor 1304, Set Number of Adapters 1306, Set Size of IP Pool 1308, Set Client Authentication Port 1310, and Set Password 1312. It should be noted that the first time the Remote Management Console is displayed after the distributed gateway software is installed, the details of the machines in the cluster will not be observed. Thus, neither a machine of the cluster or a remote machine may obtain the monitoring information from the display. The Edit menu 1302 must be selected and parameters set to enable monitoring of the cluster machines, as described below.

The Add Gateway Monitor function permits a user to enter a primary IP address for each gateway machine to be monitored. One IP address will be entered for each machine in the cluster. Ordinarily, the IP address of each machine in the cluster will be entered, so that each machine can be monitored. The Number of Adapters function is for entering the number of NICs to show for each machine. The default number of NICs is two, for a minimal cluster configuration, as this indicates connection of the machine to one external

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subnet and one internal subnet. The user entry in the Number of Adapters should match the number entered for the setup value, in the setup procedure described above.

The Set Size of IP Pool function permits a user to enter the size of the IP address pools, with a default number of four. This value defines the number of IP addresses managed by the distributed gateway on each subnet. The Set Client Authentication Port function involves connecting via a telnet operation to a port on the Application (firewall) machine. This ensures communication between the distributed gateway software and the application software (such as the firewall) with which it works.

The Set Password function provides a means of authenticating a user who wishes to gain access to the cluster monitoring information. The password entered here will be used to permit a remote user to communicate with a machine in the cluster. It should be noted that this authentication password does not guarantee access to the distributed gateway software and to information from the Remote Monitoring Console. Rather, a separate cluster password is necessary, in addition to the authentication password. The cluster password is preferably set only by a user at a cluster machine, using a local administrative utility program of the distributed gateway software. In the preferred embodiment, the distributed gateway software provides a "Change Service Password" option from the software "Start" menu that, when selected from a cluster machine, permits an authorized user to set the cluster password. In this way, a setup user specifies a password that must be provided when connecting to the cluster.

Finally, the distributed gateway software includes a command line interface utility program that provides an alternative to the GUI. The command line interface permits the

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same control as the Remote Monitoring Console of the GUI. That is, just as an authorized user may remotely connect to a cluster machine and view the GUI display to determine the status of the cluster, an authorized user may remotely connect to a cluster machine and receive cluster status information from a text-based, command line interface. The command line interface will appear in a text window, in a conventional manner that will be familiar to those skilled in the art.

In the preferred embodiment, the command line interface will report the local status of the machine to which a remote user connects or of the local machine at which a user has invoked the command line interface, and will also report on the global status of the cluster. The global status information may be retrieved by connecting to any machine of the cluster. In addition, a remote user may move VIP address assignments from one machine to another by connecting to any machine of the cluster. It should be noted, however, that the command line interface will return a success indication (that is, a no error condition) if the command from the remote machine is successfully communicated to the cluster machine, but the command line interface does not determine if the remote machine actually carries out the requested action. Such information is available when communicating with the GUI.

Thus, the distributed gateway constructed in accordance with the invention dynamically reconfigures traffic assignments among multiple machines for increased network availability. The distributed gateway moves traffic assignments among the multiple machines if one of the gateway machines becomes unavailable, such that network availability is substantially unchanged. The machines of the distributed gateway communicate with each other such that automatic, dynamic traffic assignment reconfiguration occurs in response to

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machines being added and deleted, with and no loss in functionality for the gateway cluster overall, in a process that is transparent to local network users, thereby providing a distributed gateway functionality that is scalable. Each machine of the gateway can advantageously continue with its operational functions, such as operating firewall software, while participating in the distributed gateway and dynamic reconfiguration processing. In this way, the invention substantially maintains network availability regardless of machine failures, so that there is no single point of failure and no lapse in gateway functionality.

Improved State Sharing Protocol

A network gateway server cluster constructed in accordance with the present invention includes multiple gateway server computers, also called traffic control computers, that function as a front layer gateway of a first subnet between the network and a back-end layer that includes multiple machines of a second subnet. The front-layer servers provide a scalable, distributed, highly available, load balancing server system that performs fail-over and dynamic load balancing for both server layers. The front-layer servers achieve their unique functionality with a dynamic reconfiguration protocol that permits reassignment of network addresses to the front layer machines and supports state information sharing and CPU load information sharing among the front-layer servers. To provide such functionality, the front-layer servers utilize a token scheme in an expanded format compared to that described above.

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The server cluster configuration and address assignment are achieved through the operation and protocol word scheme previously described. As noted above, a variety of unique functional features are provided by a gateway server cluster constructed and operated in accordance with the invention. The unique functional features will be described next.

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Consistent State Sharing

Consistent state sharing among the servers in the cluster is important for the distributed server application in accordance with the invention. In this embodiment, the 10 Group Membership Protocol Word described above in Section A is expanded and generalized to create a general Consistent State Sharing scheme. This Consistent State Sharing mechanism is reliable, has low-overhead, and serves as the core to enable other features of the front-layer distributed server system.

The foundation of the Consistent State Sharing mechanism is a Reliable Message 15 layer that is implemented with the distributed gateway server application software. In this embodiment, the Reliable Message layer sits on top of UDP (that is, it uses UDP to send data) and comprises a module of the application software. It has an acknowledgement and automatic resend mechanism that enables reliable delivery of data. Its main differentiation with TCP is that, first, it is a connectionless protocol; secondly, it supports multiple subnet 20 transport; furthermore, in the case of delivery failure, it calls a call-back function from the layer above it.

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Upper layer software, comprising modules of the distributed server application, can send a message of any size using the Reliable Message layer. The sender-side operation of the Reliable Message layer partitions the message being sent into a number of packets. It sends all packets using UDP, creating a record for each packet as well as for the message. When the timeout of any packet expires, it resends that packet, and doubles the timeout value. After a predetermined number of resends using all possible paths, if the Reliable Message layer still fails to receive acknowledgement, the Reliable Message layer will call the callback function to notify the upper layer software, passing it the record of the original message. On the other hand, after all packets have been acknowledged by the receiver, the Reliable Message layer cleans the records for the packets and for the message by deletion. The upper layer software comprises any software calling the Reliable Message layer for messaging.

On the receiver side of the Reliable Message layer processing, for every packet received, the Reliable Message layer sends out an acknowledgement. The Reliable Message layer of a front layer server maintains a buffer in which it places the packets, until all packets for a message are received. When all packets are received, the Reliable Message layer asks the upper layer software to process the message.

With the creation of the Reliable Message layer, this embodiment provides consistent state sharing with a reliable message passing interface. In this consistent state sharing scheme, the token described in the Group Membership Protocol Word serves as the "locomotive" of a state-sharing "train". This is illustrated in Figure 14. The "locomotive" 1402 can have an arbitrary number of data modules 1404 attached to it, like carriages of a

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train. This is achieved with a data field in the token header that specifies the number of data modules (carriages) associated with the token (locomotive). The token 1402, together with the data modules 1404, becomes a message. Thus, the Reliable Message layer is a means of transporting this message. This message travels in a token ring fashion around all the members of the gateway server cluster, as described above. Each member of the cluster can load and unload information onto or from the message train, changing the token header to specify the number of data modules, as needed.

Currently, the data that travels on the consistent state sharing mechanism described above include Virtual IP information, cluster configuration information, node fault and load monitoring information, connection information, server monitoring information. Other types of information may be added, as needed.

Dynamic Address Assignment without Reboot

Some server operating systems will not permit changing the IP address of a server without rebooting the server. Rebooting a server machine involves shutting down the server and reapplying power. It should be apparent that the server is unavailable while the reboot is performed, and therefore rebooting a server can cause a critical lapse of server availability and should be avoided. A gateway server constructed in accordance with the present invention provides a distributed gateway server that advantageously permits network address assignments to be moved from one distributed server to another of a gateway cluster without requiring rebooting. This is achieved by "hiding" the IP address reassignment from the server operating system (OS) software of the cluster machines. The OS may comprise, for

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example, the "Windows NT Server" operating system produced by Microsoft Corporation of Redmond, Washington, USA installed on the server machine.

Figure 15 shows the operating process of a distributed server in accordance with the invention. In the first operation, represented by the flow diagram box numbered 1502, the server OS is configured so that all IP addresses are assigned to all distributed server machines of the server cluster. That is, the OS of each distributed server in the cluster configured upon installation such that all IP addresses to be shared are, in the view of the OS, assigned to all of the cluster servers. This permits flexibility in assigning the IP addresses to any one of the cluster servers without rebooting, because any IP address reassignment is transparent to the server OS. Thus, to the server OS, it appears that no IP address reassignment ever occurs, and therefore no rebooting is ever needed.

In the next operation, represented by the flow diagram box numbered 1504, a distributed server (DS) that is reassigned by the server application (Figure 4) to a new IP address will generate a gratuitous ARP message, as described above. The other distributed servers of the server cluster respond to the gratuitous ARP message with their particular IP address assignment, per the description above (Figure 9). This operation is represented by the flow diagram box numbered 1506. Lastly, to prevent OS rebooting, the distributed server application software of each distributed server will block the ARP reply messages of the cluster servers from being detected by their respective server OS, by discarding the reply messages. This operation is indicated by the flow diagram box numbered 1508. In this way, it is guaranteed that there is no IP address conflict, because each server OS is unaware of the machines having duplicate IP numbers. For each virtual IP, at any time, only one server is

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answering the ARP request, and therefore the mutual exclusivity of the virtual IP addresses is maintained.

Symmetric Traffic Routing

Another feature provided by the server system constructed in accordance with the invention is that of symmetric routing of network traffic among the cluster machines. This is advantageous because a cluster of front layer servers may assign a distributed gateway server to handle incoming traffic to be forwarded to a machine on another subnet, but that distributed server may be different from the default server that will be used by the subnet machine. Thus, the distributed server handling incoming traffic destined for a subnet machine will not be the same distributed server that receives return responses from the subnet machine. This results in asymmetric traffic loading among the distributed servers, and is undesirable in some cases where symmetric routing is required. In accordance with the invention, the distributed servers of a gateway server cluster will forward data traffic among the machines in the cluster to ensure that data traffic enters and leaves the cluster from the same distributed server, thereby providing symmetric routing.

Figure 16 is a flow diagram that illustrates the operation of the server cluster to implement symmetric traffic handling in accordance with the invention. For a server cluster having distributed servers as described above, one of the distributed servers is assigned to be an "authoritative" server, or authoritative node, for the server cluster. This assignment is carried out by the front-layer server constructed in accordance with the present invention.

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In the first step of operation illustrated in Figure 16, as represented by the flow diagram box numbered 1602, a server, or node, of the server cluster receives a data request from a client machine and hashes the data request to determine which server node will be the authoritative node for the request. It should be understood that different nodes of the server cluster may be assigned "authoritative nodes" for different data requests, depending on the IP addresses (of destination Web server) involved. Once the authoritative node is identified, the data request is forwarded from the receiving node to the authoritative node. This operation comprises the operation identified by the box 1602.

When the authoritative node receives the data request, the authoritative node determines which distributed server in the server cluster will handle the data traffic associated with this request from this client to the designated Web server. When the authoritative node identifies the handling node, it forwards the data request to the identified node for handling. This operation is represented by the flow diagram box numbered 1604. Next, as represented by the flow diagram box numbered 1606, the handling node receives the data request and sends it along to the appropriate Web server for response. The Web server (WS) response is sent to a default node of the server cluster. Those skilled in the art will know that a Web server typically has a default upstream router (toward the Internet) to which it sends replies to data requests. Sending the Web server reply to the default reply node is represented by the flow diagram box numbered 1608.

Next, as represented by the flow diagram box numbered 1610, the default reply node hashes the received data request reply to the authoritative node for replies, and sends the reply message to that authoritative reply node. The authoritative reply node receives the

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reply message and forwards it to the server node that will ensure symmetric communication. That is, the authoritative reply node will determine the node of the server cluster that first received the data request from the client, and will forward the reply message to that node. In this way, the data request passes to and from the server cluster through the same distributed server, thereby providing symmetric communication. This operation is represented by the flow diagram box numbered 1612.

Finally, in an optimization step, the authoritative node sends forwarding information to the default reply node. The default reply node stores this information, which indicates the node to which the authoritative node forwarded the reply for symmetric communication. On subsequent reply messages received at the default reply node, the distributed server of the default reply node will know which server should receive the reply message, and will directly forward the reply message to that node. Thus, the default reply node can skip the step of sending the reply message to the authoritative node. This operation is represented by the flow diagram box numbered 1614.

Figure 17 diagrammatically illustrates the operation described in connection with Figure 16. A server cluster 1702 receives data requests from a router 1704 that interfaces to the Internet 1706. The data request is received at Server 1 of the server cluster, in accordance with IP address assignments and operation of the cluster, as indicated by the data path 1708. The receiving node Server 1 hashes the request to the authoritative node, which in this example is Server 2, as indicated by the arrow 1710. The authoritative node determines the Web server that will handle the data request, and the data request is then forwarded to Web Server 1, which is the destination Web server. In the preferred embodiment, the authoritative

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server informs the receiving node Server 1, which forwards the data request. This processing is represented by the data path 1712.

The sequence 1710 corresponds to the box 1602 of the Figure 16 flow diagram, and the sequence 1712 corresponds to box 1604 and box 1606 of Figure 16.

The reply message is sent from Web Server 1 to the default reply node for Web Server 1, which in this example is Server 3 of the server cluster. The default reply data path is represented by the arrow 1714 (corresponding to box 1608 of Figure 16). At the default reply node (Server 3), the reply node hashes the reply message to determine that the authoritative reply node for this message is Server 2, and then forwards the reply to Server 2. The forwarding operation is indicated by the arrow 1716. Finally, Server 2 forwards the reply to Server 1, which is the node needed to ensure symmetric operation of the cluster, in the operation represented by the arrow 1718. Server 1 then sends the reply back to the requesting client, through the router 1704, per the path 1720.

The operation of 1716 corresponds to the operation of the Figure 16 box 1610, and the operation of 1718 corresponds to the Figure 16 flow diagram box numbered 1612.

In the optimization step, Server 2, the authorization reply node, informs Server 3, the default reply node, that the server ultimately returning the reply message is Server 1. Therefore, Server 3 will store this information and send reply messages from Web Server 1 directly to Server 1, bypassing an intermediate step. This processing is indicated by the arrow 1722 (and corresponds to the Figure 16 box 1614).

The authoritative servers can, if desired, perform load balancing operations in accordance with well-known techniques for adjusting load among the servers. Both the

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receiving node and the handling node will cache the assignment data that are provided by the authoritative nodes. The technique described above for the symmetric routing can be applied to a variety of gateway server functions. Such symmetric load balancing capability is advantageous because some server functions, such as firewalls, may change certain IP address and port settings, which may result in changed hashing values. The operation as described above can be used to detect connection changes (detecting as changes to client or server IP address and port, or changes to protocol type) and then to restore symmetry.

The present invention has been described above in terms of presently preferred embodiments so that an understanding of the present invention can be conveyed. There are, however, many configurations for network data traffic controllers not specifically described herein but with which the present invention is applicable. The present invention should therefore not be seen as limited to the particular embodiments described herein, but rather, it should be understood that the present invention has wide applicability with respect to network data traffic controllers generally. All modifications, variations, or equivalent arrangements and implementations that are within the scope of the attached claims should therefore be considered within the scope of the invention.

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CLAIMS

WE CLAIM:

1. A data traffic controller for a computer network, the controller comprising:

a network interface that permits communication between the traffic controller and a subnet over which network data is sent and received; and

a distributed gateway application that dynamically determines network data traffic address assignments from multiple primary network addresses to multiple virtual network addresses to send network data to an intended host on the subnet, wherein network data intended for a host on the subnet is addressed to one of the virtual network addresses.

2. A method of controlling data traffic for a computer network through a traffic controller computer, wherein the data traffic is received through a network interface that permits communication between the traffic controller and a subnet over which network data is sent and received, the method comprising:

receiving network data intended for a host on the subnet at a data traffic controller, wherein the network data is addressed to one of a plurality of virtual network addresses that are on the subnet and are associated with one or more primary network addresses; and

dynamically determining network data traffic address assignments from multiple primary network addresses to multiple virtual network addresses to send network data to an intended host on the subnet.

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3. A method of controlling data traffic as defined in claim 2, further comprising:

communicating with a plurality of front layer server computers that are all members of a front layer subnet of network addresses over which network data is sent and received, wherein the communication includes state sharing information with a dynamic reconfiguration protocol that permits reassignment of network addresses among the front layer servers and specifies state information sharing and load information sharing among the front layer servers; and

communicating with a plurality of network computers that are members of the host subnet of network addresses, comprising a back layer of servers, to send and receive network data traffic.

4. A method as defined in claim 3, wherein communicating with a plurality of server computers comprises sending data using a Reliable Message layer scheme that comprises a token data packet and one or more data carriage packets, wherein the token data packet specifies the number of data carriage packets that together comprise a Reliable Message packet and wherein the data carriage packets include data relating to state information and data traffic load information about each of the front layer servers.

5. A method as defined in claim 3, further including:

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configuring an operating system of the server computer such that all network addresses in a pool of addresses assigned to the server computers of the first subnet are assigned to the server computer;

generating a gratuitous address resolution protocol (ARP) message in response to an address reassignment of the server computer and communicating the ARP message to the other server computers of the first subnet;

blocking the sending of an ARP acknowledgment message to the other server computers of the first subnet for any received gratuitous ARP message, thereby inhibiting reboot operation of the respective server computers and ensuring that each server computer is unaware of any duplicate assignment of network address numbers.

6. A method as defined in claim 3, further including operating as an authoritative node of the first subnet to ensure symmetric routing of network data traffic to and from the first subnet.

7. A method as defined in claim 6, wherein operating to ensure symmetric traffic routing comprises:

receiving a data request from a responding server computer of the first subnet, wherein the data request was initially received at the responding server computer, which determined the authoritative node for responding to the data request;

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identifying a server computer in the first subnet that will handle the data traffic associated with the data request and forwarding the data request to the identified server computer for handling;

receiving a reply message from a server computer of the first subnet that is operating as a default reply node to a second subnet computer that is responding to the data request; and

forwarding the reply message to a server computer of the first subnet that will ensure symmetric routing of the data request and reply message with respect to the server computers of the first subnet.

8. A method as defined in claim 7, further comprising forwarding assignment information to the server computer of the first subnet that was operating as the default reply node for the data request, wherein the assignment information includes forwarding information that the default reply node can use to directly forward response messages from the second subnet computer to the first subnet computer that will ensure symmetric routing.

9. A method of operating a server computer for controlling data traffic of a computer network, the method comprising:

receiving network data traffic through a network interface that permits communication between the server computer and other computers;

communicating with a plurality of server computers that are all members of a first subnet of network addresses over which network data is sent and received, comprising a front

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layer of servers, wherein the communication includes state sharing information with a dynamic reconfiguration protocol that permits reassignment of network addresses among the front layer servers and specifies state information sharing and load information sharing among the front layer servers; and

communicating with a plurality of network computers that are members of a second subnet of network addresses to send and receive network data traffic.

10. A method as defined in claim 9, wherein communicating with a plurality of server computers comprises sending data using a Reliable Message layer scheme that comprises a token data packet and one or more data carriage packets, wherein the token data packet specifies the number of data carriage packets that together comprise a Reliable Message packet and wherein the data carriage packets include data relating to state information and data traffic load information about each of the front layer servers.

11. A method as defined in claim 9, further including:

configuring an operating system of the server computer such that all network addresses in a pool of addresses assigned to the server computers of the first subnet are assigned to the server computer;

generating a gratuitous address resolution protocol (ARP) message in response to an address reassignment of the server computer and communicating the ARP message to the other server computers of the first subnet;

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blocking the sending of an ARP acknowledgment message to the other server computers of the first subnet for any received gratuitous ARP message, thereby inhibiting reboot operation of the respective server computers and ensuring that each server computer is unaware of any duplicate assignment of network address numbers.

5

12. A method as defined in claim 9, further including operating as an authoritative node of the first subnet to ensure symmetric routing of network data traffic to and from the first subnet.

10 13. A method as defined in claim 12, wherein operating to ensure symmetric traffic routing comprises:

receiving a data request from a responding server computer of the first subnet, wherein the data request was initially received at the responding server computer, which determined the authoritative node for responding to the data request;

15 identifying a server computer in the first subnet that will handle the data traffic associated with the data request and forwarding the data request to the identified server computer for handling;

receiving a reply message from a server computer of the first subnet that is operating as a default reply node to a second subnet computer that is responding to the data request;

20 and

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forwarding the reply message to a server computer of the first subnet that will ensure symmetric routing of the data request and reply message with respect to the server computers of the first subnet.

14. A method as defined in claim 13, further comprising forwarding assignment information to the server computer of the first subnet that was operating as the default reply node for the data request, wherein the assignment information includes forwarding information that the default reply node can use to directly forward response messages from the second subnet computer to the first subnet computer that will ensure symmetric routing.

15. A program product for use in a computer that executes program steps recorded in a computer-readable media to perform a method of operating the computer for controlling data traffic of a computer network, the program product comprising:

a recordable media;

a plurality of computer-readable instructions executable by the computer to perform a method comprising:

receiving network data traffic through a network interface that permits communication between the server computer and other computers;

communicating with a plurality of server computers that are all members of a first subnet of network addresses over which network data is sent and received, comprising a front layer of servers, wherein the communication includes state sharing information with a dynamic reconfiguration protocol that permits reassignment of network addresses among the

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front layer servers and specifies state information sharing and load information sharing among the front layer servers; and

communicating with a plurality of network computers that are members of a second subnet of network addresses to send and receive network data traffic.

16. A program product as defined in claim 15, wherein communicating with a plurality of server computers comprises sending data using a Reliable Message layer scheme that comprises a token data packet and one or more data carriage packets, wherein the token data packet specifies the number of data carriage packets that together comprise a Reliable Message packet and wherein the data carriage packets include data relating to state information and data traffic load information about each of the front layer servers.

17. A program product as defined in claim 15, further including:

configuring an operating system of the server computer such that all network addresses in a pool of addresses assigned to the server computers of the first subnet are assigned to the server computer;

generating a gratuitous address resolution protocol (ARP) message in response to an address reassignment of the server computer and communicating the ARP message to the other server computers of the first subnet;

blocking the sending of an ARP acknowledgment message to the other server computers of the first subnet for any received gratuitous ARP message, thereby inhibiting

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reboot operation of the respective server computers and ensuring that each server computer is unaware of any duplicate assignment of network address numbers.

18. A program product as defined in claim 15, further including operating as an authoritative node of the first subnet to ensure symmetric routing of network data traffic to and from the first subnet.

19. A program product as defined in claim 18, wherein operating to ensure symmetric traffic routing comprises:

receiving a data request from a responding server computer of the first subnet, wherein the data request was initially received at the responding server computer, which determined the authoritative node for responding to the data request;

identifying a server computer in the first subnet that will handle the data traffic associated with the data request and forwarding the data request to the identified server computer for handling;

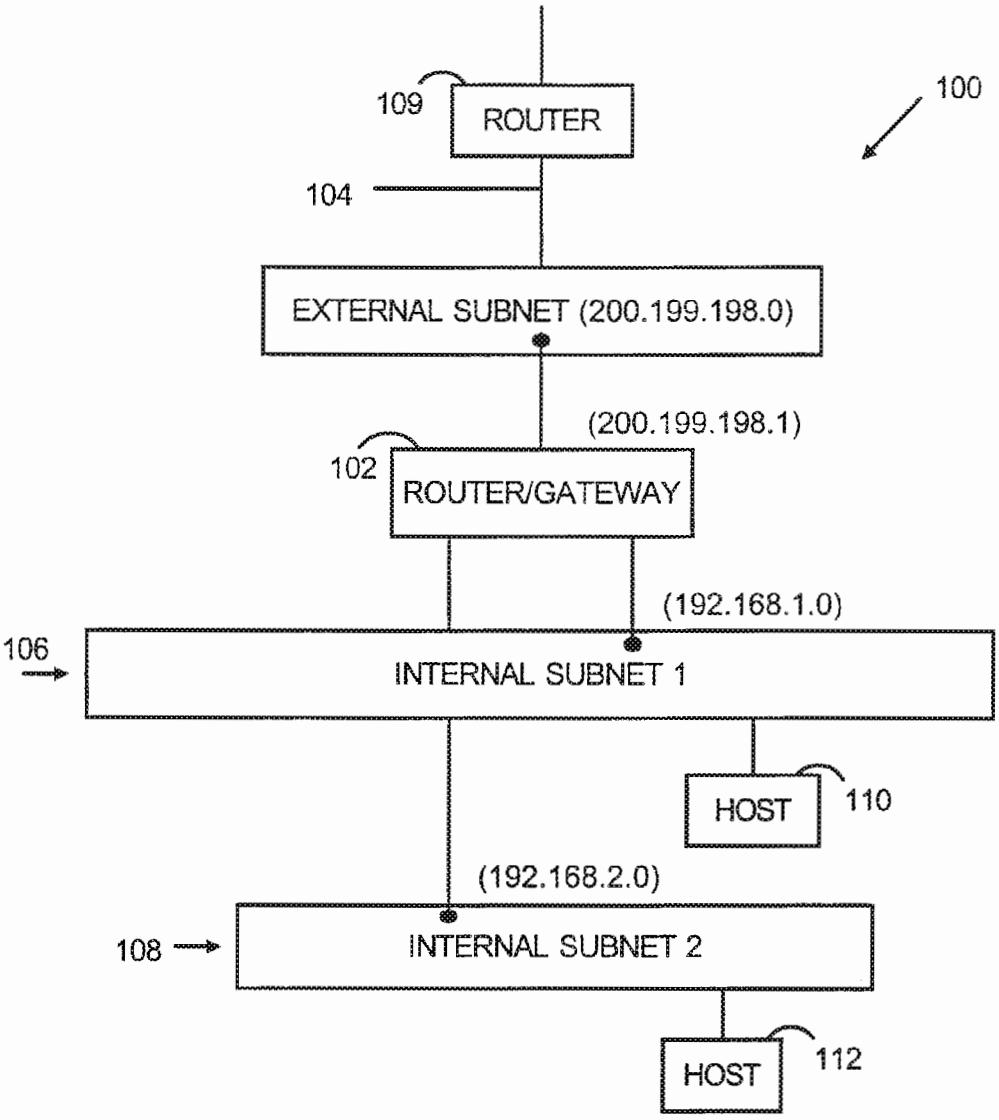
receiving a reply message from a server computer of the first subnet that is operating as a default reply node to a second subnet computer that is responding to the data request; and

forwarding the reply message to a server computer of the first subnet that will ensure symmetric routing of the data request and reply message with respect to the server computers of the first subnet.

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20. A program product as defined in claim 19, further comprising forwarding assignment information to the server computer of the first subnet that was operating as the default reply node for the data request, wherein the assignment information includes forwarding information that the default reply node can use to directly forward response messages from the second subnet computer to the first subnet computer that will ensure symmetric routing.

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PRIOR ART

FIG. 1

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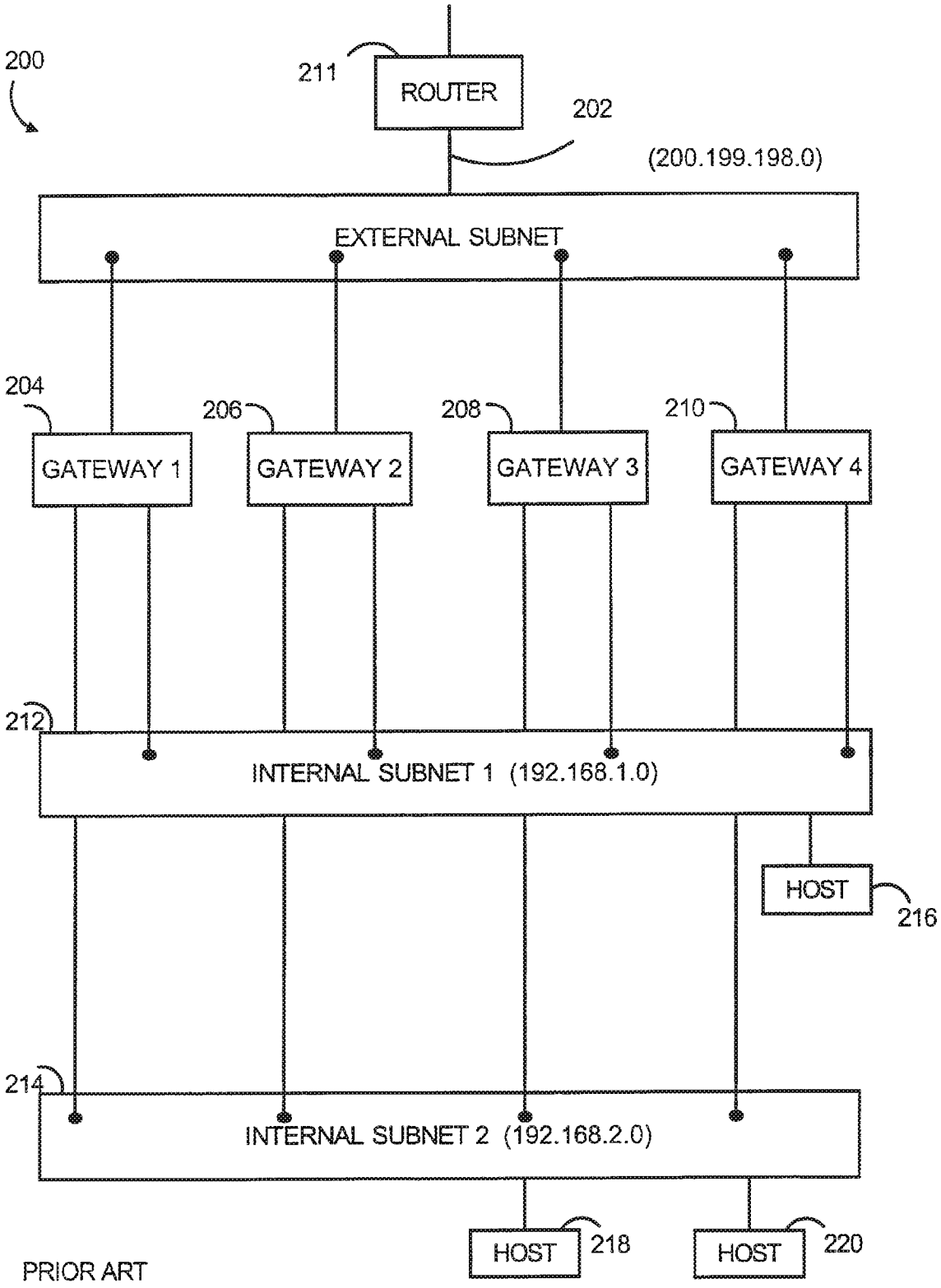


FIG. 2

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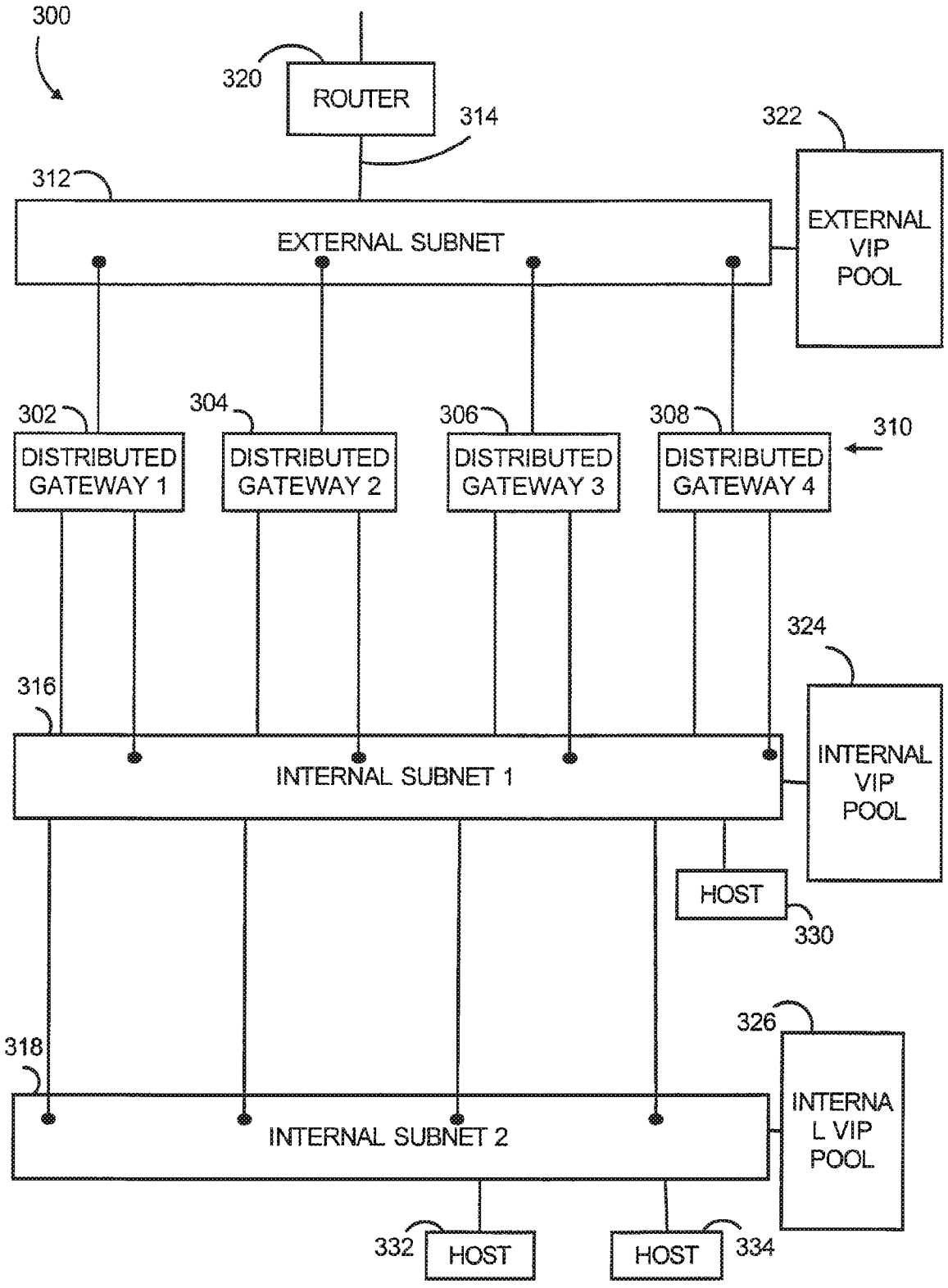


FIG. 3

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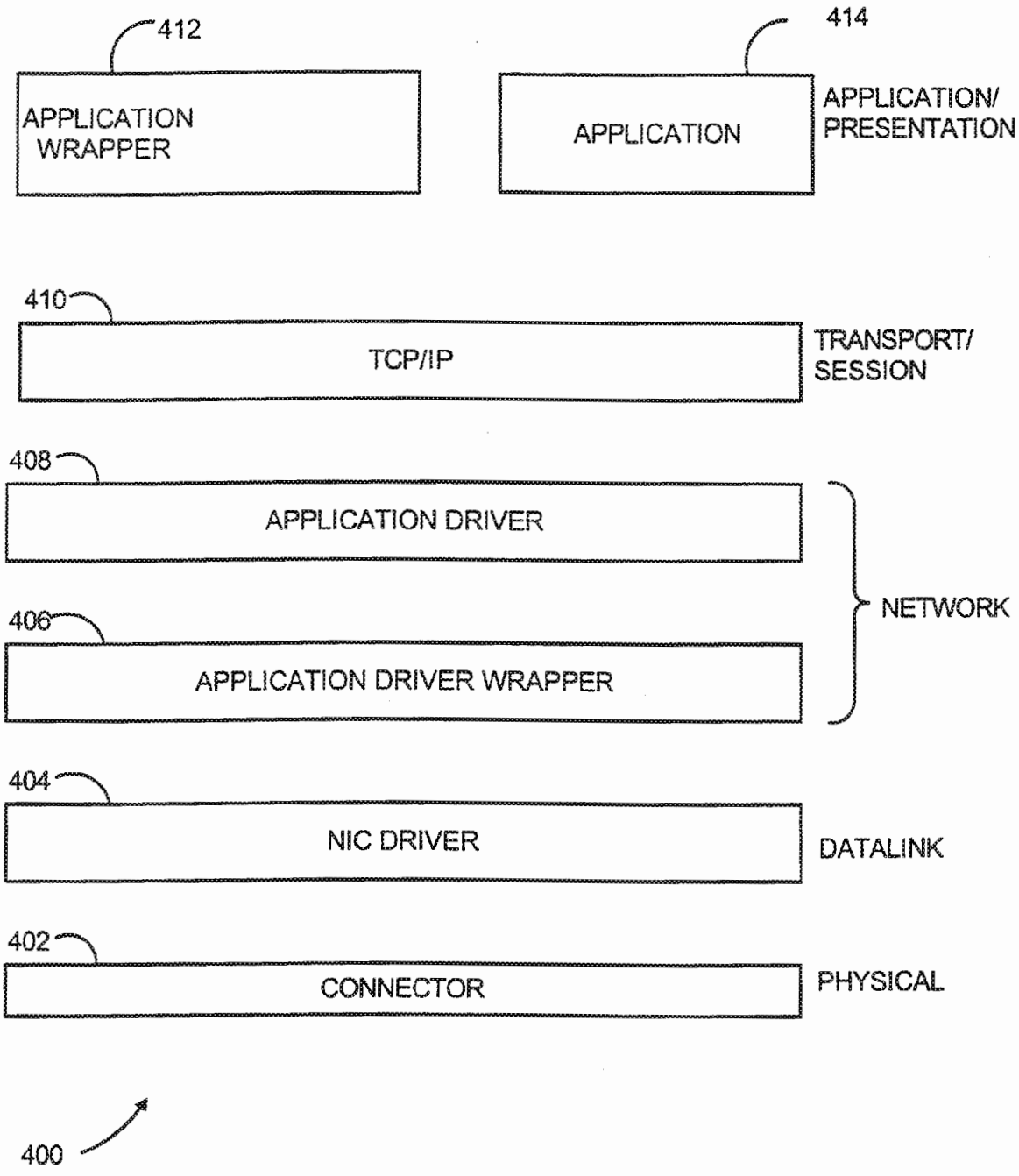


FIG. 4

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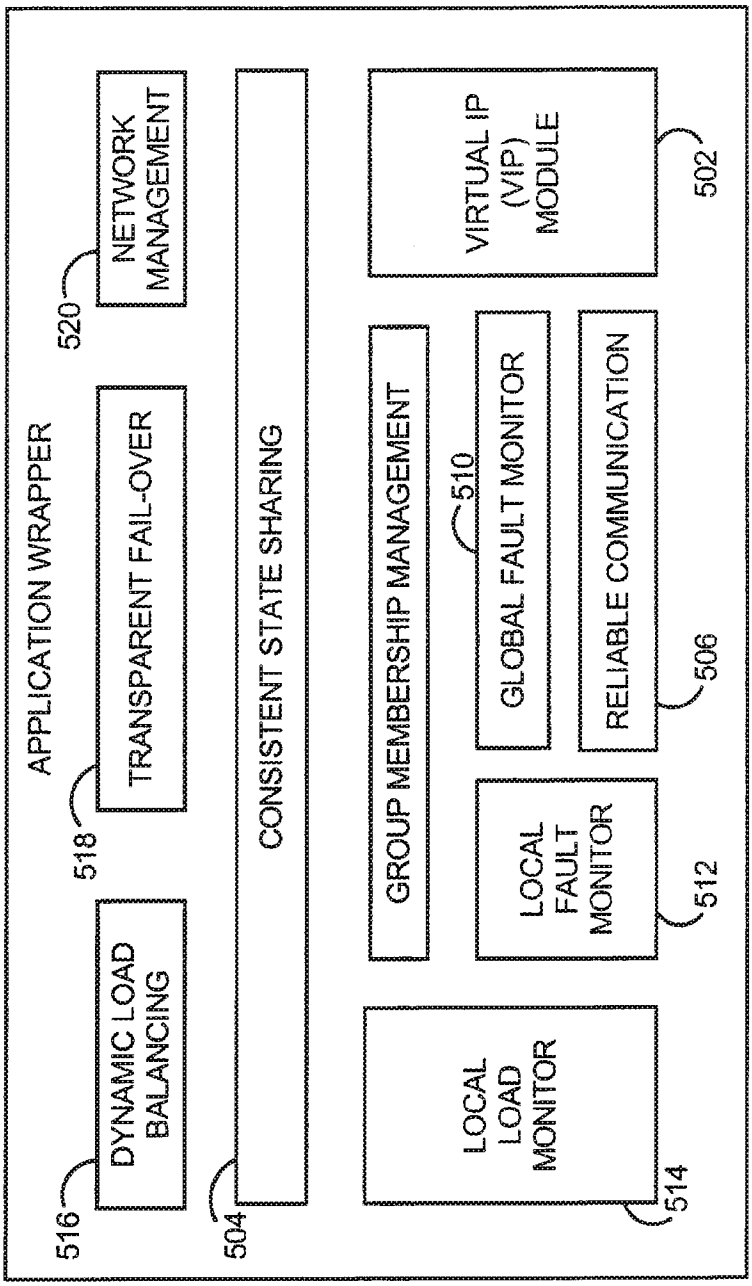


FIG. 5

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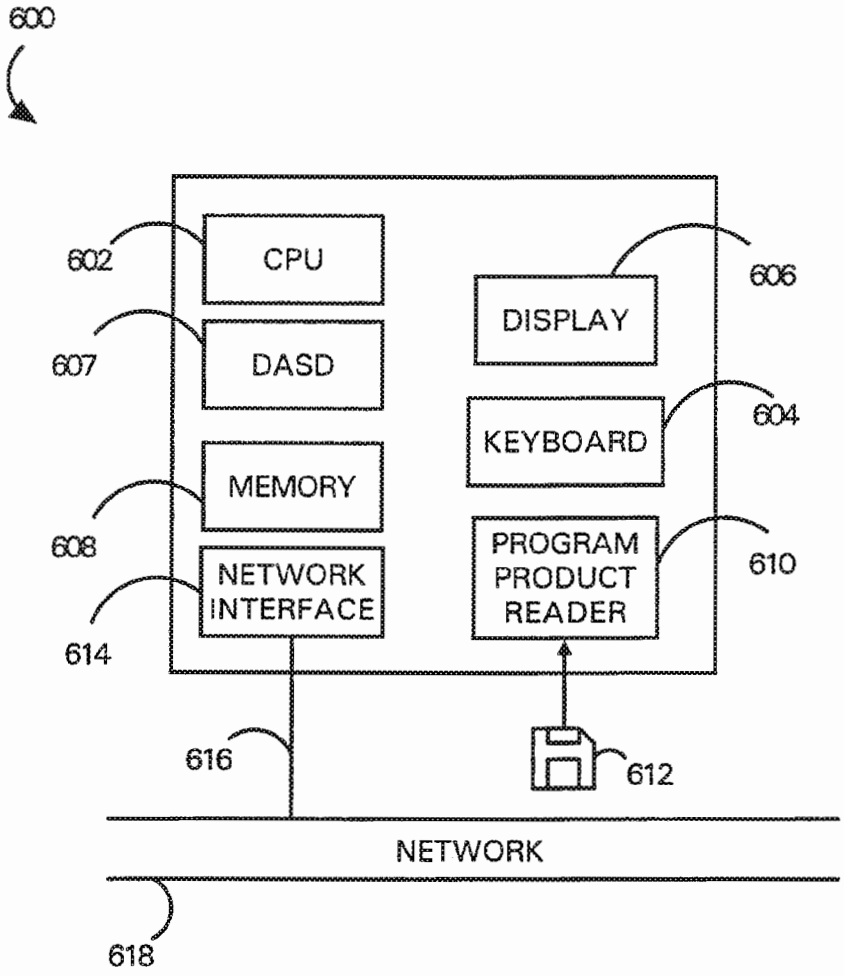


FIG. 6

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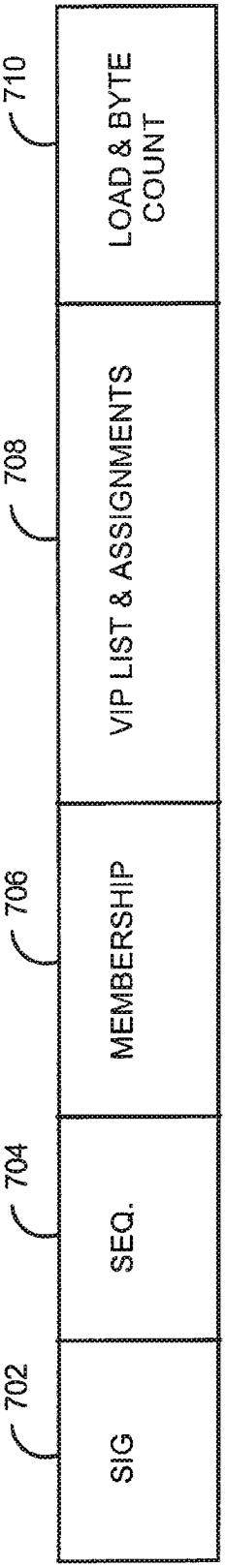


FIG. 7

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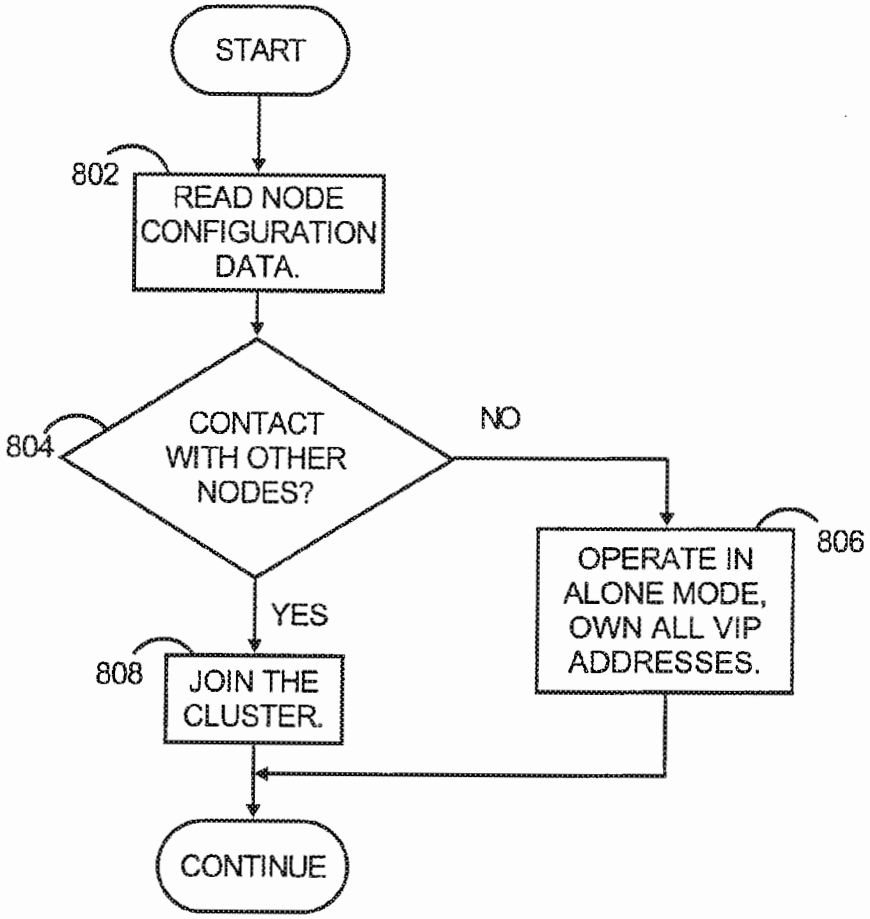


FIG. 8

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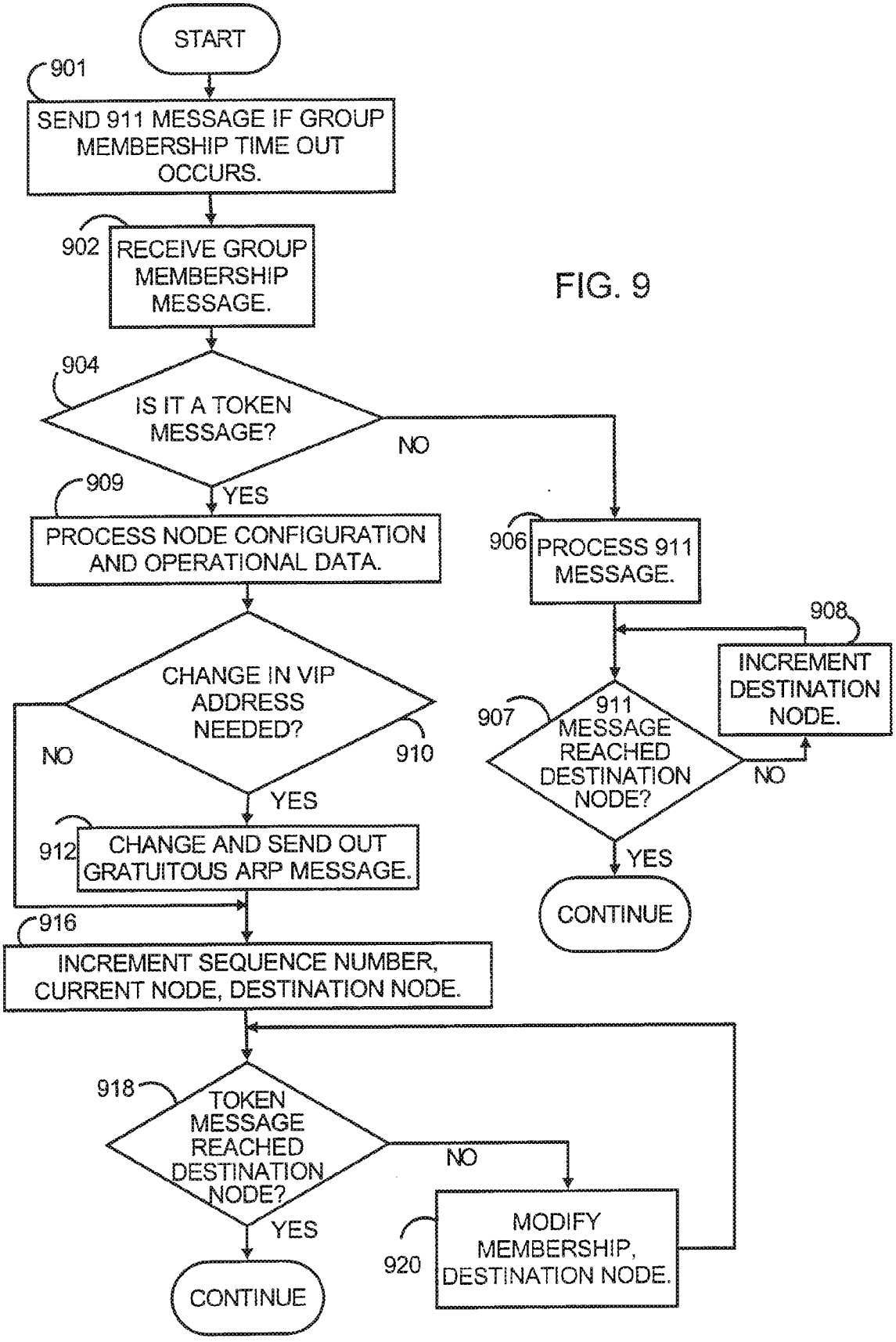


FIG. 9

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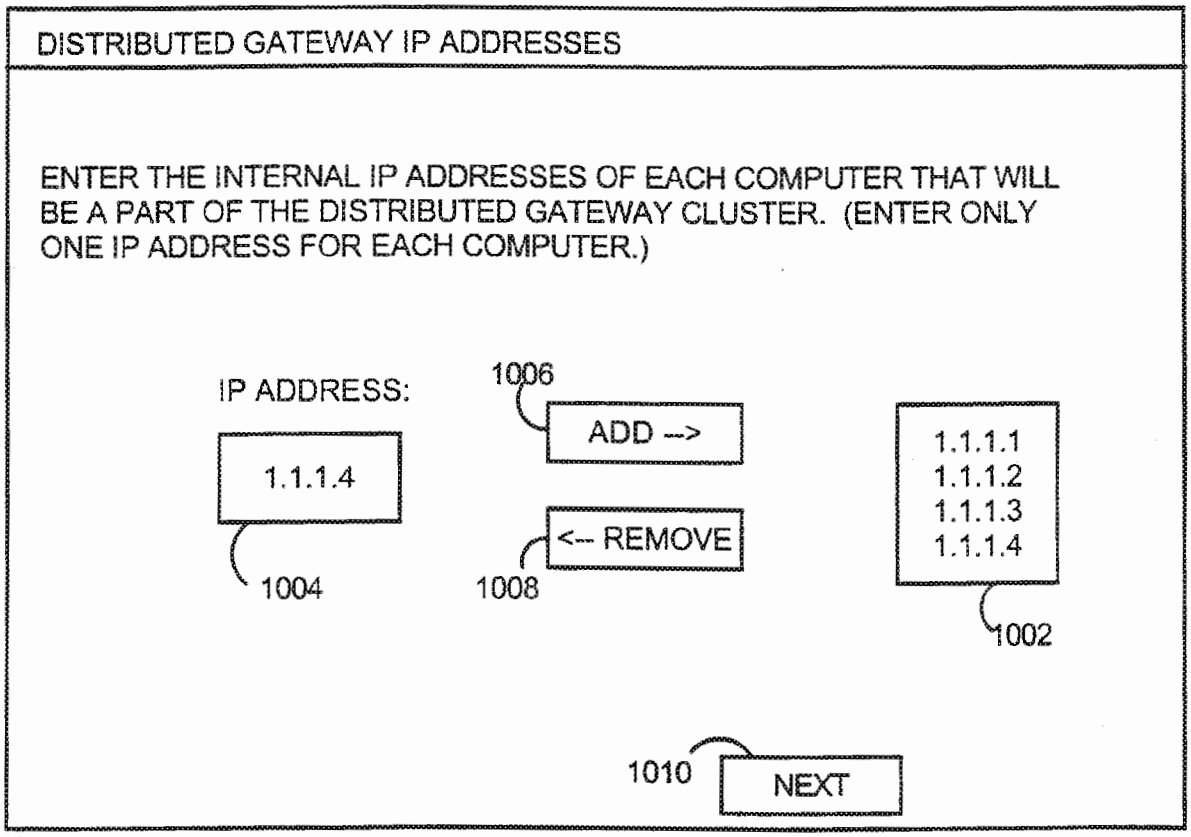


FIG. 10

1000

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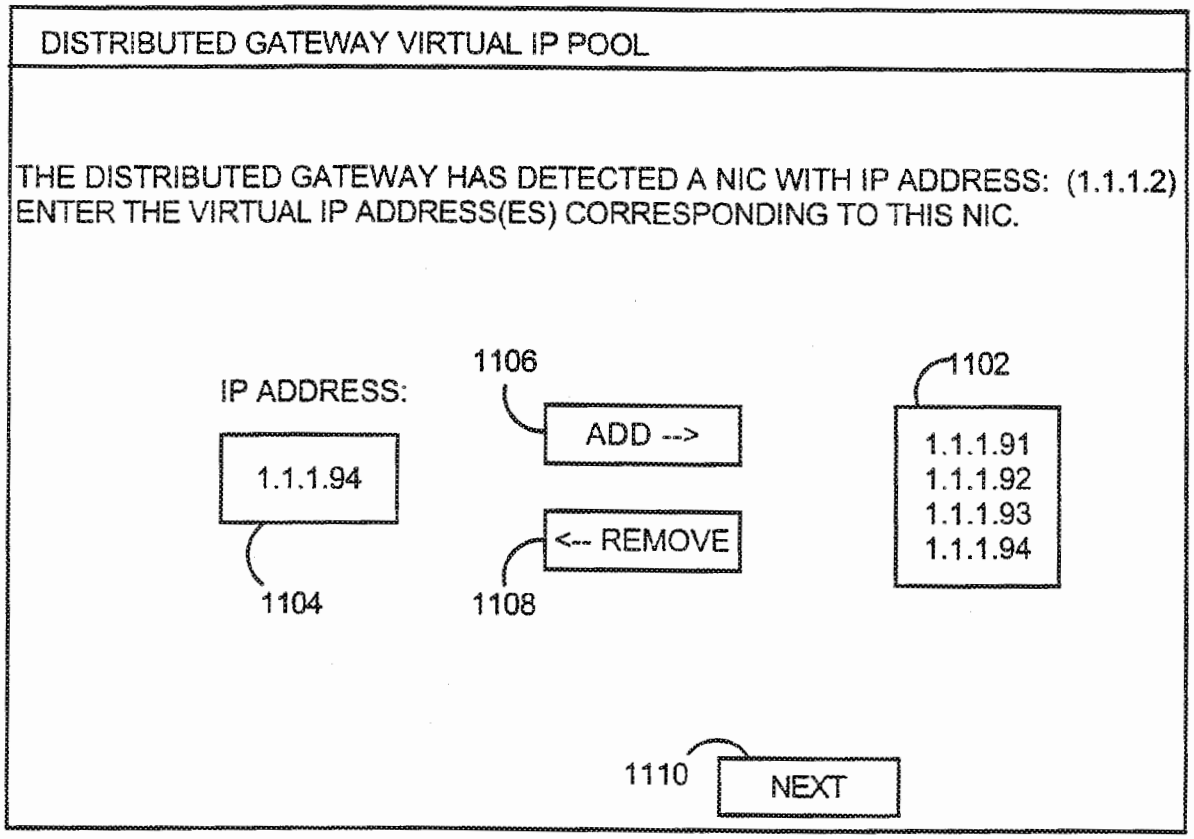

DISTRIBUTED GATEWAY VIRTUAL IP POOL
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ENTER THE VIRTUAL IP ADDRESS(ES) CORRESPONDING TO THIS NIC.
IP ADDRESS:
1.1.1.94
1104
1106
ADD -->
<-- REMOVE
1108
1102
1.1.1.91
1.1.1.92
1.1.1.93
1.1.1.94
1110
NEXT

FIG. 11

1100

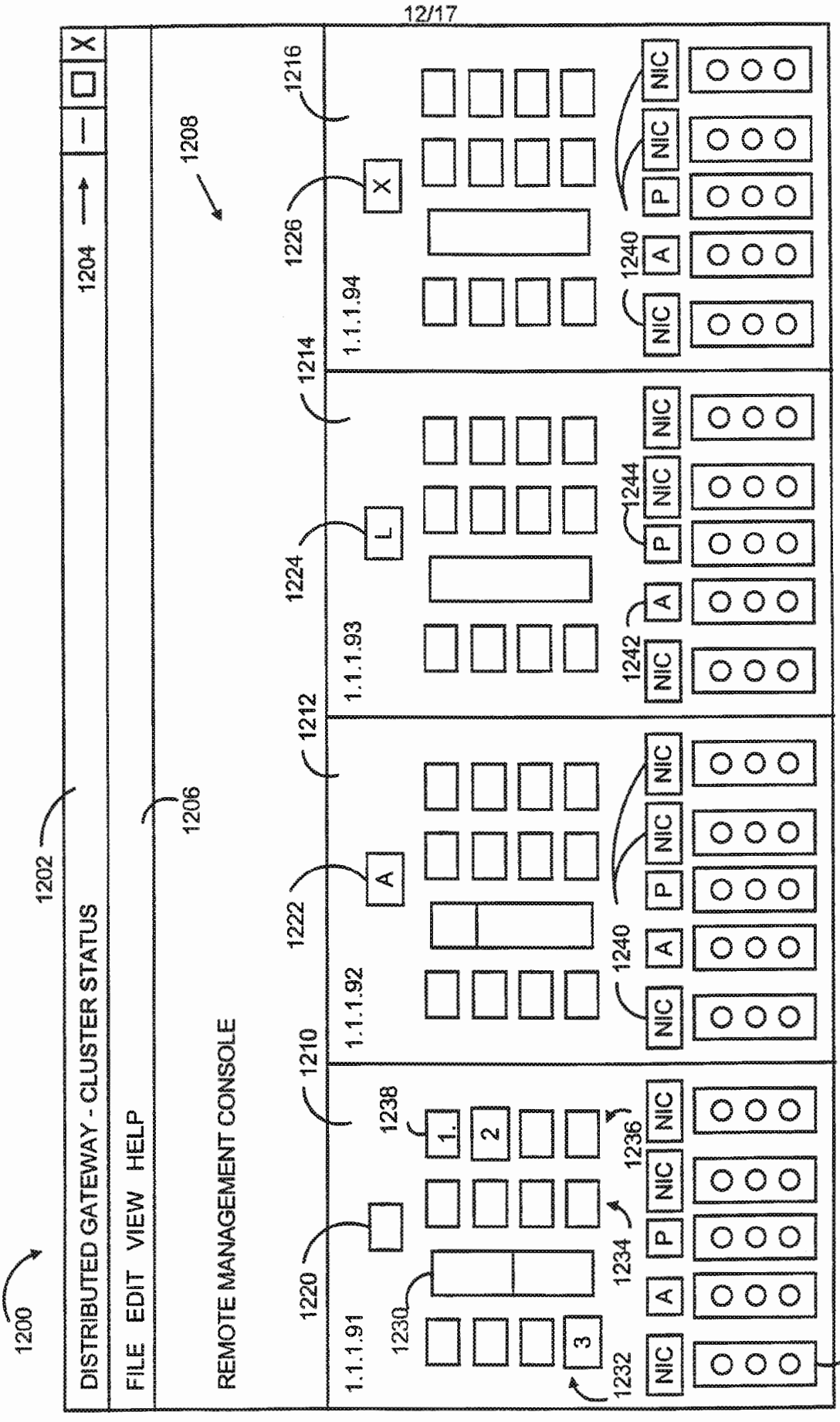


FIG. 12

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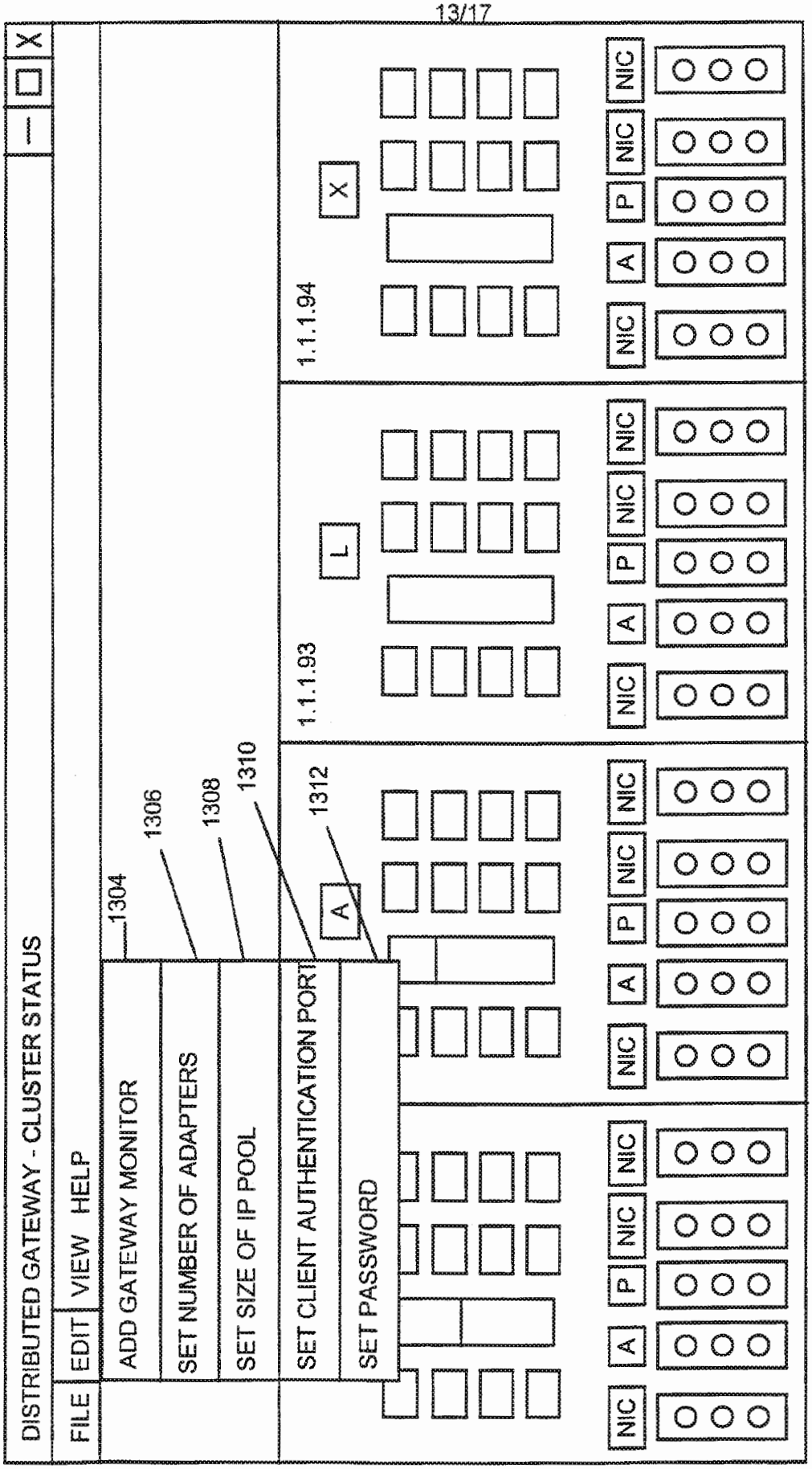


FIG. 13

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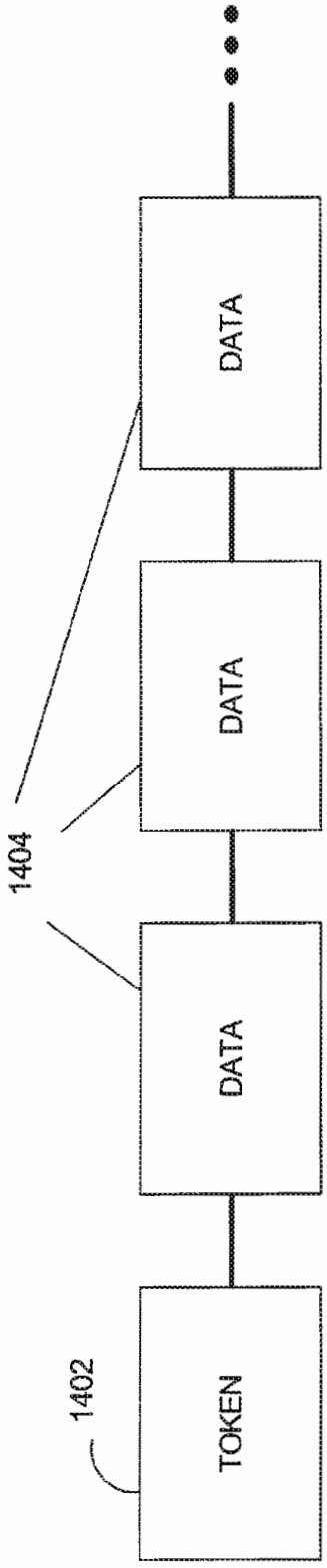


FIG. 14

SAMSUNG EX. 1002 - 284/1684

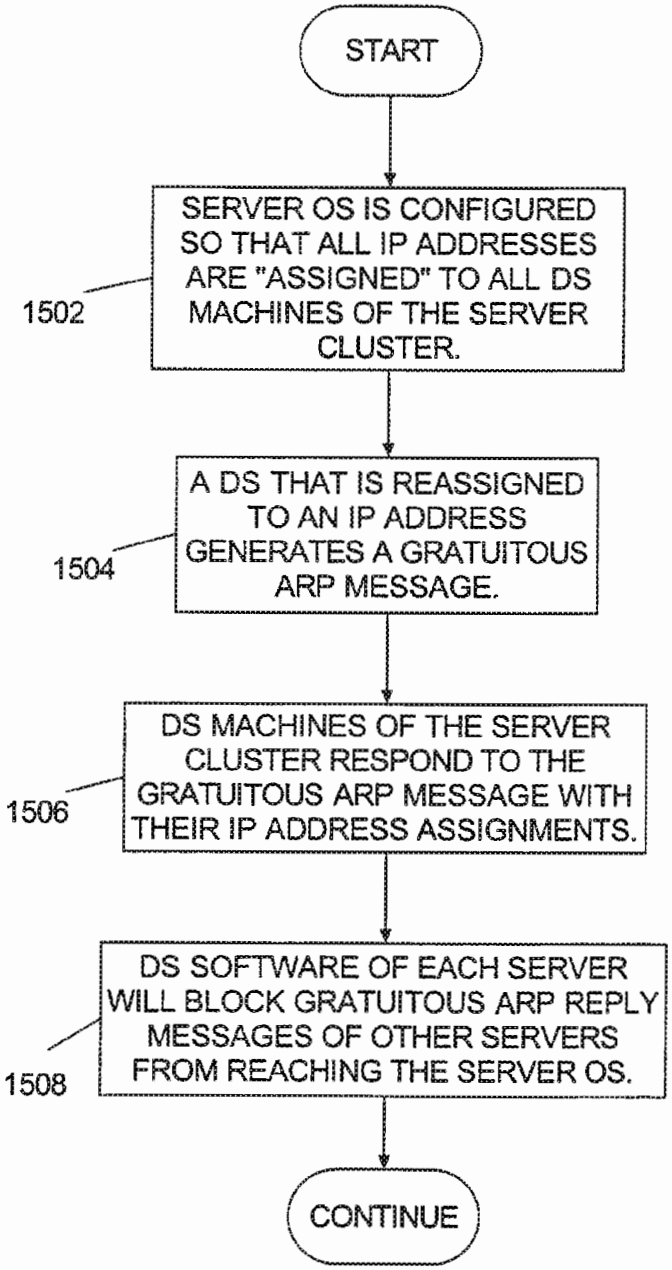


FIG. 15

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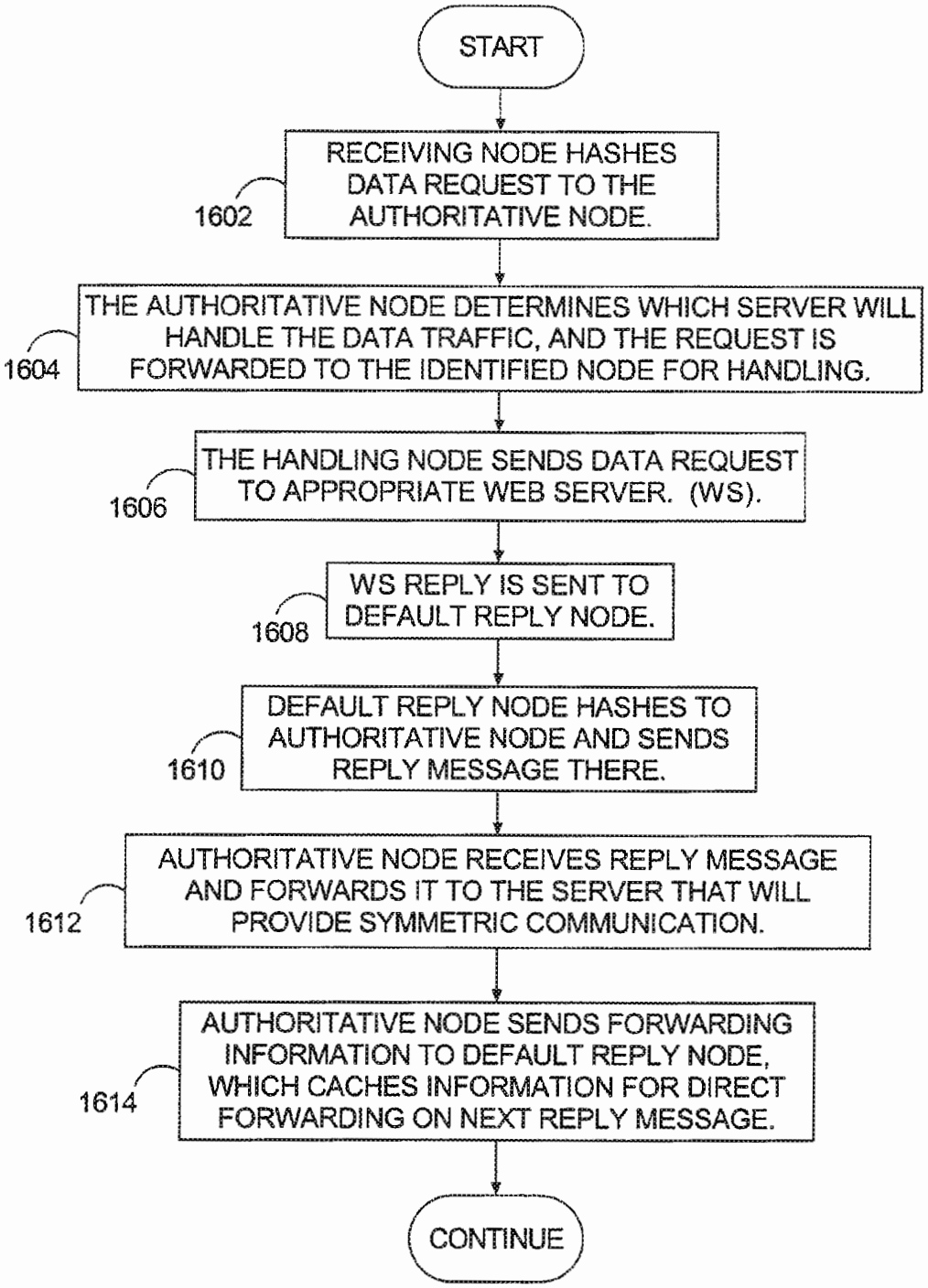


FIG. 16

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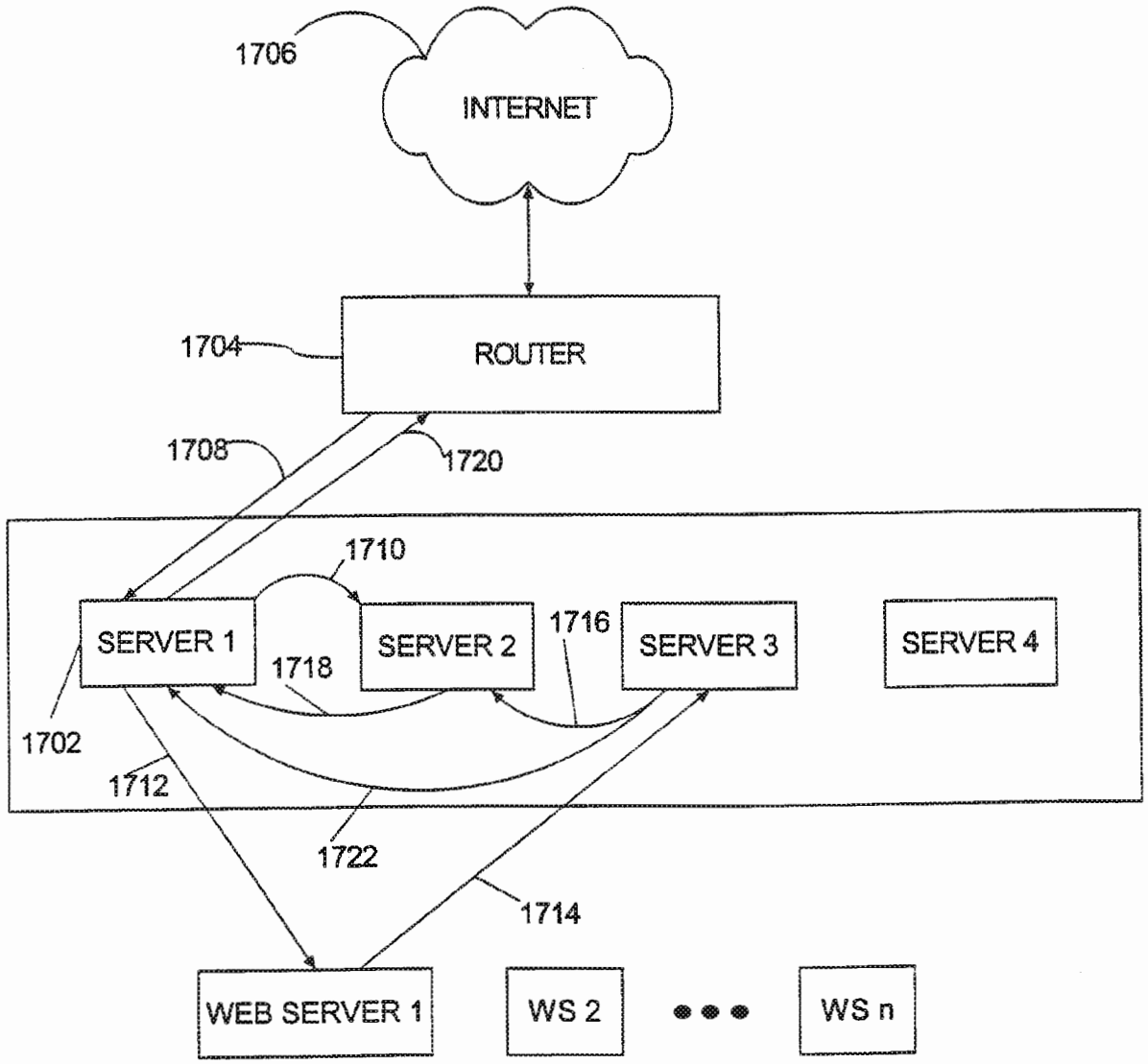


FIG. 17

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/09966

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L29/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, IBM-TDB, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 98 26559 A (GTE INTERNETWORKING INC) 18 June 1998 (1998-06-18) page 13, line 29 -page 21, line 23 figures 2B,3C,4C	1,2
A		3,9,15
X	US 5 898 830 A (COLEY CHRISTOPHER D ET AL) 27 April 1999 (1999-04-27) figures 4,9 column 8, line 25 -column 9, line 51 column 12, line 29 -column 13, line 53	1,2
X	WO 99 33227 A (HOLONTECH CORP) 1 July 1999 (1999-07-01) page 11, paragraph 2 -page 12, paragraph 3 page 16, paragraph 2 -page 18, paragraph 2 figure 2	1

-/---

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 September 2000	06/10/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Eraso Helguera, J

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/09966

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 341 477 A (MORENCY JOHN P ET AL) 23 August 1994 (1994-08-23) figures 2,2A,7 column 4, line 38 - line 68 column 11, line 15 - line 50	1-3,9,15
A	US 5 774 668 A (CHOQUIER PHILIPPE ET AL) 30 June 1998 (1998-06-30) figures 1,5A,5B column 4, line 54 -column 8, line 63 column 12, line 5 -column 13, line 38	1-3,9,15
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A	GOLDSZMIDT G S: "LOAD MANAGEMENT FOR SCALING UP INTERNET SERVICES" IEEE NETWORK OPERATIONS AND MANAGEMENT SYMPOSIUM,US,NEW YORK, NY: IEEE, vol. CONF. 10, 15 February 1998 (1998-02-15), pages 828-835, XP000793430 ISBN: 0-7803-4352-2 the whole document	1-20

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INTERNATIONAL SEARCH REPORT

Information on patent family members

rnational Application No
PCT/US 00/09966

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(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **TANAKA, Kenichiro** [JP/JP]; c/o Matsushita Electric Works, Ltd., 1048, Oaza-Kadoma, Kadoma-shi, Osaka 5718686 (JP). **KUBO, Masao** [JP/JP]; c/o Matsushita Electric Works, Ltd., 1048, Oaza-Kadoma, Kadoma-shi, Osaka 5718686 (JP).

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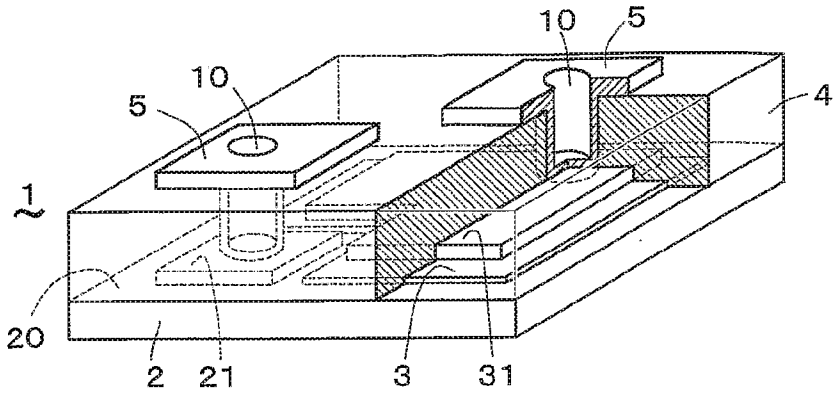
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(54) Title: LIGHT-EMITTING DEVICE AND ITS MANUFACTURING METHOD



(57) Abstract: In a light-emitting device and its manufacturing method, mounting by batch process with surface-mount technology, high light extraction efficiency, and low manufacturing cost are realized. The light-emitting device 1 comprises semiconductor layers (2, 3) of p-type and n-type nitride semiconductor, semiconductor-surface-electrodes (21, 31) to apply currents into each of the semiconductor layers (2, 3), an insulating layer 4 which holds the semiconductor layers (2, 3), and mount-surface-electrodes (5). The semiconductor layers (2) has a non-deposited area 20 where the other semiconductor layer (3) is not deposited. The insulating layer (4) has VIA 10 which electrically connect the mount-surface-electrodes 5 and the semiconductor-surface-electrodes (21, 31). In the manufacturing process, firstly, semiconductor layers (2, 3) and semiconductor-surface-electrodes (21, 31) are deposited on the transparent crystal substrate, and by using build-up process, insulating layer (4) and the mount-surface-electrodes (5) are formed, and secondly, VIA 10 are formed, and finally, the transparent crystal substrate is separated to get light-emitting device (1). Light can be extracted directly and efficiently from the semiconductor layers (2, 3). With the mount-surface-electrodes (21, 31), light-emitting device (1) can be mounted by using surface mount technology.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

DESCRIPTION

LIGHT-EMITTING DEVICE AND ITS MANUFACTURING METHOD

Technical Field

The present invention relates to a light-emitting device and its manufacturing method.

Background Art

Conventionally, there have been technologies for mounting semiconductor light-emitting devices made of light-emitting diode onto a substrate by using wire bonding or flip-chip mounting. Because those technologies require high precision placement, such a light-emitting device is expected that it can be mounted in batch process using surface-mount technology.

Recently, a light-emitting device using nitride semiconductors is largely applied as a semiconductor light-emitting device. Such a light-emitting device is manufactured by depositing semiconductors on a sapphire substrate, so lights from such a device are extracted through the transparent sapphire substrate. However, there exist differences of index of refraction between semiconductor thin film and sapphire substrate, and also between sapphire substrate and the atmosphere, and thus a part of lights is confined in a chip of the device and radiated as heat. In the case that the lights are extracted from the semiconductor surface opposite to the sapphire substrate and lights do not go through the sapphire substrate, therefore the device can

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be mounted at the sapphire substrate side, however heat release efficiency is not good because of the interposition of sapphire substrate. Thus such a technology is proposed that the sapphire substrate is removed and a heat sink is attached on the place where the substrate is removed(e.g., Japanese Laid-Open Patent Publication No. 2000-196197).

Subsequently, above-mentioned technology, removing the sapphire substrate, is described. This technology is used in the production of laser diode array which is a collective of multiple laser diodes. FIG. 19A-19F show a series of laser diode array manufacturing process. As shown in FIG. 19A, a laser diode array is made on the sapphire substrate with thin film layers of semiconductor 102 and electrodes 121. Next, as shown in FIG. 19B, the surface provided with electrodes 121 and is opposite to the sapphire substrate is glued with the wax 103 to the support substrate 104 to support the array including the sapphire substrate.

In this situation, by applying laser beams 105 to the semiconductor 102 through the sapphire substrate, thin GaN layer pre-formed on the surface of the semiconductor 102 is decomposed to metal Ga and N_2, and as shown in FIG. 19C, the sapphire substrate is separated and is removed.

In the next step, as shown in FIG. 19D, a metal layer 106 is formed on the surface of the semiconductor 102, where the sapphire substrate was removed, and thermal conductive substrate 108 is prepared which has a metal layer 107(if metal substrate is used, metal layer 107 is not necessary). Next, as shown in FIG. 19E, semiconductor 102 and thermal conductive substrate(heat sink) 108 are bonded at each metal layer by solder layer 109. As shown in FIG. 19F, wax 103 is melted to complete laser diode array

which is composed of semiconductor 102 and electrodes 121 supported on the thermal conductive substrate 108.

As described above, by removing a sapphire substrate, and attaching a thermal conductive substrate on a place where the sapphire substrate existed, flip side contacts on common surface can be made for all laser diodes in the array. Besides, heat sink is effectively used. The technology to remove a sapphire substrate can be applied not only to a laser diode but also to a semiconductor light-emitting device such as a light-emitting diode(LED).

However, as to above-mentioned method to remove a sapphire substrate, to form electrodes, or to bond a heat sink as shown in FIG.19A-19F or patent document, many process steps are necessary, and the cost for preparing the support substrate is high. Moreover, since light beams are extracted from the surface where electrodes are provided, there is a problem that the light extraction efficiency of the light-emitting device becomes low.

Disclosure of Invention

The present invention is carried out to solve the above-mentioned problems and aimed to provide a light-emitting device and its manufacturing method, which can be mounted in batch process by using surface-mount technology, and which has high light extraction efficiency, and which can be manufactured at low cost.

For accomplishing the above-mentioned purpose, according to the present invention, a light-emitting device formed by depositing p-type and n-type nitride semiconductor layers, comprising:

semiconductor-surface-electrodes to apply currents into each of the semiconductor layers;

an insulating layer which holds the semiconductor layers; and

mount-surface-electrodes provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made;

wherein one of the semiconductor layers has a non-deposited area where the other semiconductor layer is not deposited;

one of the semiconductor-surface-electrodes is built up on the surface of the non-deposited area;

VIA's are made in the insulating layer which connect electrically the semiconductor-surface-electrodes and the mount-surface-electrodes; and

the semiconductor-surface-electrodes, the insulating layer, and the mount-surface-electrodes are built up in this order on one side of the deposited semiconductor layers.

By such a configuration, since mount-surface-electrodes electrically connected to the semiconductor-surface-electrodes with VIA are provided on the surface of the insulating layer, unlike the semiconductor mounting technology which is using wire-bonding, flip-chip-bonding or the like, it is possible to mount the light-emitting device by using the mount-surface-electrodes, and by using the surface-mount technology which is widely-applied in the print-circuit board process. Furthermore, since there are no obstacles on one of the surfaces of semiconductor layers such a sapphire substrate or electrodes and from which light beams are extracted, unlike the conventional devices, it is possible to extract light beams directly and

efficiently from the semiconductor layers to outside.

Preferably, in the light-emitting device, wherein the insulating layer is made of one of resin, ceramics, or silicon.

By such a configuration, it is possible to get such light-emitting devices having reasonably selected material for the insulating layer in respect of the manufacturing cost or product performance.

Preferably, in the light-emitting device , wherein the VIA is filled with electric conductor.

By such a configuration, since electric conductor is generally good thermal conductor, the heat generated at semiconductor layers, which constitute light-emitting portion, can be efficiently radiated through the electric conductor filled in the VIA's to the board on which the device is mounted, and it is possible to lower the thermal load to the light-emitting device, and is possible to realize stable light extraction and long life-time of the light-emitting device.

Preferably, in the light-emitting device, wherein phosphor is provided on the surface or in the interior portion of the semiconductor layer.

By such a configuration, it is possible to convert the color tone of the light emitted by the semiconductor layers into another color tone with high efficiency by using the phosphor. Furthermore, in the case that the light-emitting device is sealed with resin or the like, it is possible to suppress the deterioration of the sealing resin, because phosphor is not dispersed in the sealing resin.

For accomplishing the above-mentioned purpose, according to the present invention, a manufacturing method of light-emitting device,

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comprising:

a substrate forming process in which a semiconductor-substrate is formed by depositing p-type and n-type semiconductor layers on a transparent crystal substrate with a partly non-deposited portion, and by providing semiconductor-surface-electrodes on the semiconductor layers to apply currents into each of the semiconductor layers, wherein each of the electrode surfaces is exposed in one direction;

VIA forming process in which an insulating layer is formed on the surface of the semiconductor-substrate where the semiconductor-surface-electrodes are provided, also holes for VIA are made by partly removing the insulating layer over the semiconductor-surface-electrodes, also electric conductors are provided to form VIA's on the exposed surfaces of the semiconductor-surface-electrodes exposed by the insulator removals and on the inner walls of the holes for VIA, and also mount-surface-electrodes electrically connected to the semiconductor-surface-electrodes through the VIA are made on the surface of the insulating layer; and

substrate separation process in which the transparent crystal substrate is separated off from the semiconductor layers after the VIA forming process.

By such a configuration, it is possible to manufacture low cost and of high efficiency light-emitting device by applying the conventional print-circuit board manufacturing process. That is, in the VIA forming process, it is possible to form the insulating layer for supporting the semiconductor layers and the mount-surface-electrodes for mounting the device on the semiconductor layers by using build-up or substrate depositing process of

the conventional print-circuit board process. Since the light-emitting device completed by the removal of transparent crystal substrate has the mount-surface-electrodes on the surface of the insulating layer, it is possible to do surface mounting without using the semiconductor mount technology such the wire-bonding, flip-chip-bonding or the like. Furthermore, since the transparent crystal substrate is separated and removed, it is possible directly to extract light beams from the light emitting portion constituted by semiconductor layers. Thus this light-emitting device is excellent in both of mountability and light-emitting efficiency, and can be manufactured at low cost.

Preferably, in the manufacturing method of light-emitting device, wherein the insulating layer is made of one of resin, ceramics, or silicon.

By such a configuration, it is possible to get such light-emitting devices having reasonably selected material for the insulating layer in respect of the manufacturing cost or products performance.

Preferably, in the manufacturing method of light-emitting device, wherein the insulating layer formed in the VIA forming process is made of a insulating material of resin coated copper.

By such a configuration, it is possible to use the resin coated copper of the conventional print-circuit board process, and also it is possible to do the substrate forming process and the VIA forming process by using the conventional print-circuit board process.

Preferably, in the manufacturing method of light-emitting device, wherein the partial removal of the resin over the semiconductor-surface-electrodes in the VIA forming process is done firstly by removing copper

foils located on predefined resin of the resin coated copper, and secondly using the remained foil as a mask for resin removal process.

By such a configuration, in the case that laser beams are used to remove resin, it is possible to process the resin with high precision without any precise positioning of laser beams. And also, in the case that plasma is used to remove resin, it is no need to prepare a mask material.

Preferably, in the manufacturing method of light-emitting device, wherein the partial removal of the insulating layer over the semiconductor-surface-electrodes in the VIA forming process is done by exposing the insulating layer to laser beams or plasma.

By such a configuration, in the case that laser beams are used, it is possible to selectively remove only insulating layer by adjusting the process condition, and also high-precision processing can be done. Furthermore, no vacuum system is necessary, and then it is possible to process in the atmosphere conveniently and in high speed. In the case that plasma is used, it is possible to process many number of VIA, and also many substrates can be processed in batch to form VIA efficiently.

Preferably, in the manufacturing method of light-emitting device, wherein the separation of the transparent crystal substrate in the substrate separation process is done by using laser beams.

By such a configuration, it is possible to remove the transparent crystal substrate with the least damage to the semiconductor by concentrating energy in space and time, and this is done conveniently in the atmosphere and in high speed.

Preferably, in the manufacturing method of light-emitting device,

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wherein a roughness structure is formed on a separation-induced surface of the semiconductor layers simultaneously with the separation of the transparent crystal substrate from the semiconductor layers by using laser beams.

By such a configuration, it is possible to cut down the operation for set-up or arrangement. Furthermore, since the light reflection at the surface of the semiconductor layers for outgoing light is suppressed by the roughness structure on the surface of the semiconductor layers, with the completed light-emitting device it is possible to extract light from the semiconductor layers to outer region efficiently.

Preferably, in the manufacturing method of light-emitting device, wherein the roughness structure on the surface of the semiconductor layers is formed by irradiating the surface of the semiconductor layers with laser beams dedicated to forming the roughness structure along with the irradiation with the laser beams dedicated to separating the transparent crystal substrate.

By such a configuration, it is possible to easily control the shape of the fine structure on the surface by adjusting the irradiation interference conditions of plural laser beams.

For accomplishing the above-mentioned purpose, according to the present invention, a manufacturing method of light-emitting device, comprising:

a substrate forming process in which a semiconductor-substrate is formed by depositing p-type and n-type semiconductor layers on a transparent crystal substrate with a partly non-deposited portion, and by

providing semiconductor-surface-electrodes on the semiconductor layers to apply currents into each of the semiconductor layers, wherein each of the electrode surfaces is exposed in one direction;

VIA forming process in which an insulating layer having pre-formed holes for VIA corresponding to the semiconductor-surface-electrodes is laminated on the surface of the semiconductor-substrate where the semiconductor-surface-electrodes are provided, also electric conductors are provided to form VIA's on the surfaces of the semiconductor-surface-electrodes and on the inner walls of the holes for VIA, and also mount-surface-electrodes electrically connected to the semiconductor-surface-electrodes through the VIA are made on the surface of the insulating layer; and

substrate separation process in which the transparent crystal substrate is separated off from the semiconductor layers after the VIA forming process.

By such a configuration, it is possible to manufacture low cost and high efficiency light-emitting device by applying the conventional print-circuit board manufacturing process. That is, in the VIA forming process, it is possible to prepare the insulating layer having pre-formed holes by applying the conventional print-circuit board process, and by attaching such a insulating layer on the semiconductor-substrate the insulating layer to support the semiconductor layers and the mount-surface-electrodes to mount the device are easily formed. The light-emitting devices completed by the removal of transparent crystal substrate are, in the same way as describe above, capable of surface mounting and capable of direct extraction of the

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light from the semiconductor layers, and thus this light-emitting device is excellent in both of mountability and light-emitting efficiency, and can be manufactured at low cost.

Preferably, in the manufacturing method of light-emitting device, wherein the insulating layer is made of one of resin, ceramics, or silicon.

By such a configuration, in the same way as describe above, the availability of the insulating layer material is enlarged, and then it is possible to get such light-emitting devices having reasonably selected material for the insulating layer in respect of the manufacturing cost or products performance.

Preferably, in the manufacturing method of light-emitting device, wherein the holes in the insulating layer are formed by exposing the insulating layer to laser beams or plasma.

By such a configuration, in the case that laser beams are used, as describe above, it is possible to selectively remove only insulating layer, and also high-precision processing can be done. Furthermore, no vacuum system is necessary, and then it is possible to process in the atmosphere conveniently and in high speed. In the case that plasma is used, as describe above, it is possible to process many number of VIA, and also many substrates can be processed in batch to form VIA efficiently.

Preferably, in the manufacturing method of light-emitting device, wherein the separation of the transparent crystal substrate in the substrate separation process is done by using laser beams.

By such a configuration, as describe above, it is possible to remove the transparent crystal substrate with the least damage to the semiconductor

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by concentrating energy in space and time, and this is done conveniently in the atmosphere and in high speed.

Preferably, in the manufacturing method of light-emitting device, wherein a roughness structure is formed on a separation-induced surface of the semiconductor layers simultaneously with the separation of the transparent crystal substrate from the semiconductor layers by using laser beams.

By such a configuration, as describe above, it is possible to cut down the operation for set-up or arrangement. Furthermore, since the light reflection at the surface of the semiconductor layers for outgoing light is suppressed by the roughness structure on the surface of the semiconductor layers, with the completed light-emitting device it is possible to extract light from the semiconductor layers to outer region efficiently.

Preferably, in the manufacturing method of light-emitting device, wherein the roughness structure on the surface of the semiconductor layers is formed by irradiating the surface of the semiconductor layers with laser beams dedicated to forming the roughness structure along with the irradiation with the laser beams dedicated to separating the transparent crystal substrate.

By such a configuration, as describe above, it is possible to easily control the shape of the fine structure on the surface by adjusting the irradiation conditions of both laser beams.

Brief Description of Drawings

FIG. 1 is a perspective view partly containing a sectional view

showing a light-emitting device in accordance with an embodiment of the present invention.

FIG. 2 is a sectional view showing the above-mentioned light-emitting device.

FIG. 3A, FIG. 3B, and FIG. 3C are flow charts showing processes for manufacturing methods of a light-emitting device in accordance with embodiments of the present invention.

FIG. 4A-4E are sectional views of a light-emitting device showing processes in time-series for the above-mentioned manufacturing methods.

FIG. 5A-5E are perspective views corresponding to the above-mentioned FIG. 4A-4E.

FIG. 6 is a sectional view showing a VIA forming process of the above-mentioned manufacturing methods.

FIG. 7 is a sectional view showing another example for a VIA forming process of the above-mentioned manufacturing methods.

FIG. 8 is a sectional view showing a further example for a VIA forming process of the above-mentioned manufacturing methods.

FIG. 9 is a sectional view showing another example of a light-emitting device of the present invention.

FIG. 10A and FIG. 10B are sectional views showing a mounting process of a light-emitting device of the present invention.

FIG. 11A and FIG. 11B are sectional views showing a substrate separation process of the above-mentioned manufacturing methods.

FIG. 12A and FIG. 12B are sectional views showing other examples for a substrate separation process of the above-mentioned manufacturing

methods.

FIG. 13 is a sectional view showing a further example for a substrate separation process of the above-mentioned manufacturing methods.

FIG. 14 is a sectional view showing a light-emitting device of the present invention having a roughness structure on a surface of the semiconductor layers.

FIG. 15 is a sectional view showing a light-emitting device of the present invention having phosphor on the surface of the semiconductor layers.

FIG. 16 is a sectional view showing other examples for a manufacturing method of a light-emitting device of the present invention.

FIG. 17A-17D are sectional views showing other examples for a manufacturing method of a light-emitting device of the present invention.

FIG. 18A, FIG. 18B, and FIG.18C are sectional views showing still further examples for a manufacturing method of a light-emitting device of the present invention.

FIG. 19A-19F are sectional views showing manufacturing processes of a conventional laser diode array.

Best Mode for Carrying Out the Invention

A light-emitting device and its manufacturing method in accordance with embodiments of the present invention is described with reference to the drawings. FIG. 1 and FIG. 2 show a light-emitting device 1 of present invention. The light-emitting device 1 comprises semiconductor layers 2, 3 made up of p-type and n-type nitride semiconductor layers, semiconductor-

surface-electrodes 21, 31 to apply currents into each of the semiconductor layers 2, 3, an insulating layer 4 which holds the semiconductor layers 2, 3, and mount-surface-electrodes 5 provided on one surface (top side in the figure) of the insulating layer 4 which is opposite to the other surface of the insulating layer with which the semiconductor-surface-electrodes 21, 31 are in contact. One semiconductor layer 2 has a non-deposited area 20 where the other semiconductor layer 3 is not deposited, and one semiconductor-surface-electrode 21 is built up on the surface of the non-deposited area 20. The mount-surface-electrodes 5 and the semiconductor-surface-electrodes 21, 31 are electrically connected by electrical conductor 51 provided on the inner wall of the VIA holes 41 formed in the insulating layer 4. The semiconductor-surface-electrodes 21, 31, the insulating layer 4, and the mount-surface-electrodes 5 are built up in this order on one side of the deposited semiconductor layers 2, 3.

In the above-mentioned light-emitting device 1, the semiconductor layer 2 is, for example, n-type semiconductor, and the semiconductor layer 3 is p-type. Reverse order is also possible, that is, the semiconductor layer 3 is n-type semiconductor and the semiconductor layer 2 is p-type semiconductor. Those semiconductor layers 2, 3 have an active layer in the two layers interface forming the light-emitting diode (LED). One surface (bottom side in the figure) of the deposited semiconductor layers 2, 3 of the light-emitting device 1 is a light extraction surface. The other surface (top side in the figure) is a mount-surface and the mount-surface-electrodes 5 are formed there.

With such a configuration, the light-emitting device 1 comprises

mount-surface-electrodes 5 on the surface opposite the light-emitting surface, and because of this fact, the light-emitting device 1 can be treated as a surface-mount device which is mounted on a print-circuit board, and the mounting method used for the print-circuit board can be applied for the mounting of the light-emitting device. This means that the semiconductor mount technologies such as wire-bonding, flip-chip-bonding, or the like are not required, and the surface mount technologies such as solder re-flow, or the like can be utilized. Furthermore, since the light extraction surface of the light-emitting device 1 is not covered by transparent crystal substrate such as sapphire, light beams can be extracted directly and efficiently to outside from the semiconductor layers 2, 3.

The light-emitting device shown in FIG.1 and FIG. 2 is of a single device type having one pair of semiconductor-surface-electrodes 21, 31 and one pair of mount-surface-electrodes 5, 5 associated with the former. Such a light-emitting device 1 is firstly manufactured in batch process in a combined state of many light-emitting devices as a planar array, and secondly they are diced into each chips. The planar array of the light-emitting devices can be used without dicing or with dicing into a lump containing given number of light-emitting devices.

(Process flow)

The process flow of the light-emitting device 1 is described. FIG. 3A shows a brief summary of the manufacturing process. Hereinafter FIG. 2 is referred too whenever occasion requires. In the first step of the manufacturing of the light-emitting device 1, that is, in substrate forming process (S1), a semiconductor-substrate is formed by depositing p-type and

n-type semiconductor layers 2, 3 on a transparent crystal substrate with a partly non-deposited area 20, and by providing semiconductor-surface-electrodes 21, 31on the semiconductor layers 2, 3 to apply currents into each of the semiconductor layers 2, 3, wherein each of the electrode surfaces is exposed in the same direction.

Next, in VIA forming process (S2), an insulating layer 4 is formed on the surface of the semiconductor-substrate where the semiconductor-surface-electrodes 21, 31 are provided, and mount-surface-electrodes 5 which are electrically connected to the semiconductor-surface-electrodes 21, 31 are formed on the surface of insulating layer 4. In VIA forming process (S2), two types of method are utilized as shown in later.

Last, in substrate separation process (S3), the transparent crystal substrate is separated and removed off from the semiconductor layer 2, and the light-emitting device is completed.

Two methods applicable to above-mentioned VIA forming process (S2) are shown in FIG.3B and FIG. 3C. In VIA forming process (A), as shown in FIG. 3B, firstly, insulating layer is formed on the surface of the semiconductor-substrate (S11), secondly, holes for VIA are formed in the insulating layer (S12), lastly, the semiconductor-surface-electrodes and mount-surface-electrodes are electrically connected (S13). Processes shown later in FIG.4A-4E, FIG.5A-5E, FIG.6, FIG.7, FIG.8, FIG.16 are related to the VIA forming process (A).

In VIA forming process (B), as shown in FIG. 3C, firstly, insulating layer is formed which has pre-formed holes for VIA corresponding to the semiconductor-surface-electrodes (S21), secondly, the insulating layer is

laminated on the surface of the semiconductor-substrate where the semiconductor-surface-electrodes are provided (S22), lastly, the semiconductor-surface-electrodes and mount-surface-electrodes are electrically connected (S23). Processes shown later in FIG.17A-17D, FIG.18A, FIG. 18B, and FIG. 18C are related to the VIA forming process (B).

(Example 1 of light-emitting device manufacturing)

The manufacturing method of the light-emitting device 1 is described with concrete example. FIG. 4A-4E show sectional views at typical stage of manufacturing processes in time-series, and FIG. 5A-5E show the perspective views corresponding to those figures. Firstly, as shown in FIG. 4A and FIG. 5A, n-type nitride semiconductor layer 2 is deposited on the surface of the transparent crystal substrate 6, and p-type nitride semiconductor layer 3 is deposited on it in a manner that some part of the semiconductor layer 2 is exposed without lamination. Subsequently, semiconductor-surface-electrodes 21 for semiconductor layer 2 are formed on the non-deposited area 20 where the semiconductor layer 2 is largely exposed, and also semiconductor-surface-electrodes 31 are formed on semiconductor layer 3. Thus above-mentioned semiconductor-substrate is completed.

Subsequently, as shown in FIG. 4B and FIG. 5B, a insulating layer 4 and electrical conductor layer 7 are formed on the semiconductor layer 2, 3 and semiconductor-surface-electrodes 21, 31. Those insulating layer 4 and electrical conductor layer 7 are individually formed by resin application, and by metal vapor deposition for example. As alternative method for the

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individual forming, a resin coated copper which is a print-circuit board material for build-up process, can be laminated on the semiconductor-surface-electrodes 21, 31 as one process. In this case, the insulating layer 4 is made of resin, and the electrical conductor layer 7 is made of copper film. The resin in a resin coated copper can be pure resin or filler containing resin such as glass fiber or the like.

The case that resin coated copper is used, as an insulating layer 4 to be laminated on the semiconductor-surface-electrodes 21, 31, is described. By using the resin coated copper, it is possible to easily laminate an insulating layer for manufacturing light-emitting devices. For example, resin coated copper of epoxy resin type R-0880 manufactured by Matushita Electric Works, Ltd. can be used as follows. The resin coated copper is placed on the semiconductor-substrate, and pressed by a pressing machine at 3.1Mpa, and under this situation, the resin coated copper temperature is kept at 165 degrees centigrade for 60 minutes or over, and then by cooling, lamination is completed. In the process, it is preferable to process in the vacuum state 13.3kPa. During the pressing for lamination, it is possible to make wraparound resin at the end faces where semiconductor layers appear, and thus made wraparound resin can protect the semiconductor layers at the end faces. Therefore, damage to the semiconductor layers in the post process is suppressed by the wraparound resin.

Subsequently, VIA hole patterns are made in the electrical conductor layer 7, and as shown in FIG. 4C and FIG. 5C, the resin on the semiconductor-surface-electrodes 21, 31 is partly removed by the method described later. By this process, VIA holes 41 are formed. After the

formation of VIA holes 41, chemical etching may be done in order to remove the resin residual on the surface of the semiconductor-surface-electrodes 21, 31.

Subsequently, as shown in FIG. 4D and FIG. 5D, patterned mount-surface-electrodes 5, and VIA 10 are formed by making plating layer on the surface of inner walls of the VIA holes 41, of mount-surface-electrodes of the insulating layer, and on semiconductor-surface-electrodes. With VIA 10, the semiconductor-surface-electrodes 21, 31 and the mount-surface-electrodes 5 are electrically connected. Electric conductive paste may be used to fill the VIA holes 41 and to get electrical connection between both of the electrodes. After the processes mentioned above, the light-emitting device 1 on the transparent crystal substrate 6 is completed. Above-mentioned processes for semiconductor-surface-electrodes 21, 31, VIA 10, and mount-surface-electrodes 5 are conventional in the print-circuit board manufacturing process.

Subsequently, as shown in FIG. 4E and FIG. 5E, in substrate separation process, the transparent crystal substrate 6 and light-emitting devices 1 are separated to get the light-emitting devices 1. Thus obtained light-emitting devices 1 are lump of a single light-emitting device 1, and therefore, if necessary, a single light-emitting device 1 is available by dicing. The substrate separation process is also described later.

(Formation of the VIA holes)

A series of methods to make the VIA holes by removing insulating layer 4 is described. FIG. 6 shows a situation that the VIA holes 41 are made by laser beams L1. The case that the insulating layer 4 is made by

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resin coated copper is described. Laser beams L1 can be used to form VIA holes 41 by removing regionally the insulating layer, that is, the region laminated on the semiconductor-surface-electrode 21, 31. Usable laser in the process is CO_2 laser, harmonic YAG laser, excimer laser, or the like. If the hole diameter is ϕ50μm over, CO_2 laser is well-adopted, and if less than ϕ50μm, harmonic YAG laser is well-adopted.

In the case that CO_2 laser is used, and if electric conductive layer (copper film) 7 exists on the surface of the insulating layer, as shown in FIG. 6, it is necessary firstly to make openings 71 by removing copper films at the place VIA is to be formed. Such copper films can be removed by resist patterning and copper etching. Alternatively, it is also realistic to form only insulating layer 4 without using the resin coated copper, and to make VIA holes in the insulating layer with laser beams L1, and then to make mount-surface-electrodes on the insulating layer.

If harmonic YAG laser is used, copper films can be removed by laser. Therefore, in this case, above-mentioned etching to make openings 71 is not necessary. The damage to the inner layers, that is, to the semiconductor-surface-electrodes 21, 31, can be avoided to select different processing energy between copper film processing and resin processing. Excimer laser can be used in the case that large area is processed and quality of processing is important too.

When thickness of 60μm epoxy resin is processed with CO_2 laser, the processing energy is from 1mJ to 10mJ per ϕ100μm. In such a process, it is important to prevent the occurrence of the damage in the inner semiconductor-surface-electrodes . If CO_2 laser is used for processing,

some resin remains on the surface of the inner semiconductor-surface-electrodes 21, 31. Therefore, after the VIA hole processing to the insulating layer 4 with CO_2 laser, the semiconductor-substrate is dipped into the permanganic acid solution or chromic acid solution to oxidize and resolve the resin, and the remained resin can be removed. The permanganic acid potassium solution can be used in place of the permanganic acid solution, and chromic acid potassium solution can be used in place of chromic acid solution.

The process using the permanganic acid solution is described with concrete example. The semiconductor-substrate having the insulator layer which is processed by above-mentioned VIA hole processing is dipped 5 minutes in the 80 degree centigrade MLB211 solution, which is manufactured by Shipley Company L.L.C, and after this swelling process, in order to oxidize and resolve the resin the semiconductor-substrate is dipped 5 minutes in the 80 degree centigrade MLB213 solution, which is a solution containing permanganic acid and also is manufactured by Shipley Company L.L.C. Next, after water washing, the semiconductor-substrate is dipped 5 minutes in the 10% sulfuric acid solution to neutralize the residuals, and furthermore water washing is done. By those processes, the residual resin on the semiconductor-surface-electrodes 21, 31 is removed by the permanganic acid solution.

As mentioned above, by removing the residual resin on the semiconductor-surface-electrodes 21, 31, which are the bottoms of VIA holes 41, the electrical contact between semiconductor-surface-electrodes 21, 31and plating layer is not inhibited by residual resin, and the reliability

can be maintained for the electrical connection between semiconductor-surface-electrodes 21, 31 and mount-surface-electrodes 5 through the plating layer in the VIA holes 41. Furthermore, if the process for the residual resin is done as mentioned above by using permanganic acid solution or chromic acid solution, the process can be done easily only by dipping the semiconductor-substrate into the solution, and since many semiconductor-substrates can be processed at one time, the process can be done at low cost and high speed.

FIG. 7 shows a method to form VIA holes 41 with laser. The case that the insulating layer is formed by resin coated copper is described. In order to make the VIA holes 41 in the insulating layer 4 which have a electrical conductor made of copper film on the surface, firstly, as described above, openings 71 are made by removing the copper films at the place where VIA's to be formed by using resist patterning and copper etching. The copper film around the openings 71 can be used as a mask (copper film mask) for laser processing, and thus precise positioning between laser beams L2 and semiconductor-substrate becomes unnecessary.

As the results, VIA holes 41 can be made with good position accuracy by irradiating the resin through the mask with laser beams L2 of larger diameter spot size than the VIA holes 41 size. As an example, if the diameter of the openings 71 is ϕ200μm and the accuracy is $\pm$50μm, laser beams of diameter ϕ300μm spot can be used. In the case of ultra-violet laser, like harmonic YAG laser or excimer laser, a copper mask also can be used. For this, the difference of the processing energy threshold between copper film and resin (the threshold value is higher for copper film than

resin) is used, that is, the energy of the laser beams L2 is lowered so as not to damage the mask, and only resin is selectively processed.

FIG. 8 shows another method to form VIA holes 41 with laser. The method described here, unlike above-mentioned two methods, is applied to the insulating layer 4 having no copper films. A mask 42 which has enlarged pattern of VIA holes 41 and their layout (processing pattern) is used to irradiate the spots where VIA holes 41 are to be made with laser beams L3 . The image of the mask 42 is focused onto the processing point on the insulating layer 4 by focussing lens 43. For example, if the laser processing optical system of image transfer ratio is 1/10, a mask of ϕ1000μm opening is used for circular VIA holes of ϕ100μm, and a mask of 5000μm square opening is used for square VIA holes of 500μm. A mask of 2000μm opening center distance is used, for the VIA holes center distance of 200μm. By using such a mask 42 having enlarged processing shape pattern, it is possible to do two dimensional processing in batch, and manufacturing efficiency can be improved.

(Heat radiation by VIA and surface mounting)

The improvement of the heat radiation performance by VIA is described. FIG. 9 shows filled VIA's. When the electrical conductor 51 in the VIA holes 41 is formed, by filling up the VIA holes with electrical conductor 51, which is also good thermal, a filled up VIA structure can be made, and with this structure it is possible to improve the heat radiation of the semiconductor layers 2, 3, that is, light-emitting portion. The filling with the electric conductor can be done by thick plating to the inner surface of the VIA holes 41. Alternatively, the VIA holes 41 may be filled with

electric conductive paste. Material of high thermal conductivity is preferable as the filling material. For example, copper (403W/m/K), silver (428W/m/K), aluminum (236W/m/K) are such material. Furthermore, the larger the planar dimension of VIA hole is the better for improvement of heat radiation. The improvement of heat radiation results suppression of thermal load for light-emitting device, and stable light extraction can be achieved.

As another filling method for VIA holes 41, as shown FIG. 10A and FIG. 10B, a method using solder is available, where the solder is used for mounting the device onto mounting substrate 54. The thermal conductivity of the solder is, for example, 50W/m/K, and solder can efficiently dissipate the heat. For the mounting of the light-emitting device, the device mounting process in the print-circuit board technologies can be used, and therefore no special mounting process is necessary, and the mounting process can be made simple too.

(Substrate separation process)

The method to separate the transparent crystal substrate 6 from the light-emitting device 1 is descried. FIG. 11A and FIG.11B show the substrate separation process done by irradiation with laser beams. When the laser beams are irradiated to the surface of the semiconductor layer 2 through the transparent crystal substrate 6, as described in the background art, the nitride semiconductor on the surface of the semiconductor layer 2, for example, GaN layer is decomposed to metal Ga and N_2, and as shown in FIG. 11B, the transparent crystal substrate 6 is separated and removed from the light-emitting device 1. The lasers available for substrate separation are

excimer laser (XeCl, KrF, ArF, F_2, etc.), THG-YAG laser (the third harmonic laser), FHG-YAG laser (the fourth harmonic laser), ultraviolet laser, and extra short pulse laser of less than 1ps pulse width (Ti:Sapphire laser and its harmonic laser, excimer laser, etc.) or the like.

If sapphire is used as the transparent crystal substrate 6, since sapphire is transparent for the light from infra-red to about 140nm wavelength light, those range of laser beams can be used to separate sapphire substrate. In the case that sapphire is used on gallium-nitride layer, the process condition for the temperature of light-emitting device 1 is from 30 to 100 degree centigrade. Here, this temperature is of the light-emitting device 1 under the process, and not of the laser irradiated spot under the laser irradiation. It is not necessary that the temperature of the light-emitting device 1 is set at the time laser processing, but is enough to set temperature up after laser processing. The laser energy density at processing surface is, for example, from 2 to 10mJ/mm^2. The laser irradiation can be done by a method to scan the processing surface with concentrated beams, or by a method to irradiate full surface at once with uniform strength large spot laser beams.

It may happen to occur that metal Ga, which is one of the components of GaN after decomposition to metal Ga and N_2, stay on the GaN surface after removal of sapphire substrate. Those Ga can be removed by acid washing, for example, by using HCl solution.

(Process for light-emitting surface)

In the following, several processing for the surface of light-emitting device (light-emitting surface) are described. FIG. 12A and FIG. 12B

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show the formation of a roughness structure by using laser. During the separation process in which the transparent crystal substrate 6 is removed by using laser beams L5, a roughness structure 22 is formed simultaneously on the surface of the nitride semiconductor layer 2, that is, onto surface facing the transparent crystal substrate 6. The roughness structure 22 can be formed by using the interference between incident laser beams and diffused/reflected laser beams, or between multiple number of light beams. The roughness structure 22 can improve the light extraction efficiency.

By giving the periodicity to the roughness structure 22, the light extraction efficiency can be more improved. The reason for improving is that the light beams, which are confined in the light-emitting device because of the difference of index of refraction, can be extracted by the action of diffraction phenomena caused by roughness structure . For example, with a roughness structure 22 of 1000nm period and 1000nm depth on the surface of nitride semiconductor layer 2, the light extraction efficiency is doubled. There is the same effect with a roughness structure 22 of 1500nm period and 750nm depth. As mentioned above, it is possible to efficiently extract light beams from the light-emitting device 1 to outward by utilizing the roughness structure 22, and since the roughness structure 22 can be formed simultaneously with the separation process, such a effect can be get by few process step.

FIG. 13 shows another example of the formation of a roughness structure by using laser. When the separation of the transparent crystal substrate 6 is done by laser beams L6, other laser beams L7, L8 which are dedicated to forming the roughness structure 22 are used along with the laser

beams L6 in order to form the roughness structure 22 on the surface of the nitride semiconductor layer 2, that is, on the surface which faces the transparent crystal substrate 6. The laser beams L6 go from vertical direction to the front face of the light-emitting device 1, and the laser beams L7, L8 dedicated to forming the roughness structure 22 go from oblique direction. If multiple number of laser beams are used as the laser beams and if their interference is used for forming the roughness structure 22, the control of the shape of the surface micro structure is easily done, and also it is possible to give periodicity to the structure. As described above, by giving the periodicity to the roughness structure 22, the light extraction efficiency from the light-emitting device 1 can be more improved.

FIG. 14 shows another method of the formation of the roughness structure for the purpose of improving the light extraction efficiency. In this method, a transparent optical part 8, which has a surface of micro roughness structure, is put on the surface of the nitride semiconductor layer 2, where the transparent crystal substrate 6 was removed. The index of refraction of the nitride semiconductor (GaN) is 2.5, and this is very high. On the other hand, the index of refraction of the atmosphere, where light beams are extracted in, is 1.0, and therefore the ratio of the two indices is 2.5. Therefore, in this condition, the critical angle is small for the light goes from the semiconductor layer 2 to the atmosphere, and then the light tend to be trapped by total reflection, so the light extraction loss is large. Thus, the transparent optical part 8 which has a surface of micro roughness structure, is formed with such transparent material that the index of refraction is over the value, X/3+Y, where X is the difference between the

indices of refraction of nitride semiconductor and atmosphere, and Y is the index of refraction of atmosphere. Preferably, the roughness structure has surface-roughness of from 0.1 to 100μm, and has periodicity too. For example, if quartz glass is used as the material of the transparent optical part 8, its index of refraction is about 1.5, index of refraction of GaN is 2.5, and index of refraction of atmosphere is 1.0, and therefore above-mentioned condition is satisfied, and it is possible to improve the light extraction efficiency. The index of refraction of the transparent optical part 8 is the higher, the better, and sapphire (index of refraction: 1.77) may be used.

FIG. 15 shows the processing for the semiconductor surface, which relates to the color tone conversion (wave-length conversion). By providing phosphor 9 on the surface or in the interior portion of the semiconductor layer 2, it is possible to convert the color tone of the light emitted by the light-emitting device 1 into another color tone with high efficiency by using the phosphor 9. Furthermore, in the case that the light-emitting device 1 is sealed with resin or the like, by this configuration it is possible to suppress the deterioration of the sealing resin than the sealing resin in which phosphor is dispersed. The phosphor 9 is provided for the semiconductor layer 2 after the removal of the transparent crystal substrate which is removed, as described above, by laser beams in the separation process. The phosphor 9 is provided on the surface of the nitride semiconductor layer 2, or is doped in the interior of the semiconductor layer 2. As to kind of the phosphor 9, for example, a material which converts blue color to yellow color, or emits green and red colors is used for the blue light-emitting nitride semiconductor, and a material which emits blue, green,

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and red colors is used for the ultra violet light-emitting nitride semiconductor. By providing phosphor on the surface or in the interior portion of the nitride semiconductor, it is possible to efficiently inject the emitted light into phosphor, and it is possible to suppress the deterioration of the sealing resin which is used to seal the light-emitting device.

The doping of the phosphor into the surface (or inner region) of the nitride semiconductor layer can be done firstly, by irradiating the surface, for example, with laser beams to make softened surface, and secondly by irradiating the softened surface with accelerated phosphor particles. The laser condition to soften the surface is, for example, (1) for femto-second laser: wavelength 800nm, pulse width 120fs, pulse repeat frequency 1kHz, and processing energy density 0.001 - 0.05J/mm^2, (2) for excimer femto-second laser: wavelength 248nm, pulse width 270fs, pulse repeat frequency 350Hz, and processing energy density 0.01 - 1.0J/mm^2. If nanometer size of accelerated phosphor particles is used, color tone can be converted with higher efficiency.

(Another example of the insulating layer forming)

Another example of manufacturing method of the light-emitting device 1 is described with reference to FIG. 16. In this manufacturing method, VIA forming process (A) is used in the same method as described above, and after forming the insulating layer 4 on the surface semiconductor layers, VIA holes are formed in the insulating layer. Here, unlike above-mentioned resin or resin coated copper, the case that ceramics or silicon is used as the material for insulating layer 4, is described. Ceramics or silicon wafer is bonded to semiconductor layers 2, 3 and also semiconductor-

surface-electrodes 21, 31 of the semiconductor-substrate. Alumina may be used as the ceramics wafer. Those can be bonded together between surfaces by pressing them under clean and activated surface condition.

As to above-mentioned bonding, there are several type of bonding methods for metal-metal bonding (diffusion bonding, pressure welding, and ultrasonic bonding, or the like), and in the case of insulator-semiconductor bonding, bonding can be done by cleaning process in which bonding surfaces are cleaned, for example, by using Ar ion bombardment, and by pressing process in which two wafers are stacked up facing each cleaned surface and pressed to be bonded under room temperature. It is also realistic to apply low melting temperature glass on the bonding surfaces of insulating layer 4 and semiconductor-substrate, and to bond by using the glass. Thus made insulating layer 4 which is bonded on the semiconductor-substrate can be processed as mentioned above, that is, VIA holes can be made by using laser in the insulating layer 4 made of ceramics or silicon, and VIA's and mount-surface-electrodes are formed by using plating.

If the insulating layer 4 is made of silicon, VIA holes can be made by plasma etching.

(Example 2 of light-emitting device manufacturing)

Another manufacturing method of the light-emitting device 1 is described with reference to FIG. 17A-17D. This manufacturing method uses the VIA forming process (B) shown in FIG. 3C. As shown in FIG. 17A, the insulating layer 4, in which VIA holes 41 corresponding to the semiconductor-surface-electrodes 21, 31 are pre-formed, is laminated and bonded to semiconductor layers 2, 3 and also semiconductor-surface-

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electrodes 21, 31 of the semiconductor-substrate.

As the material of insulating layer 4 for bonding use, resin, resin coated copper, ceramics for example alumina, and silicon can be used. The method to make VIA holes 41 in the insulating layer made of those material is practically the same as mentioned above, and the method using laser beams can be applied. In the case of silicon, VIA holes 41 can be made by plasma etching. In the case of ceramics, the ceramic insulating layer 4 may be prepared by firing of the green sheet in which holes are made corresponding to the VIA holes. In the case of resin or resin coated copper, VIA holes 41 can be opened easily by punching or drilling, since those holes are through holes.

FIG. 17B shows the situation that insulating layer 4 is bonded on the semiconductor substrate. If the insulating layer 4 is of resin, the bonding can be done with above-mentioned epoxy type R-0880, and in the same method mentioned above. If the insulating layer 4 is of ceramics or silicon, the bonding can be done by the method described with reference to FIG. 16. The formation of the mount-surface-electrodes 5, and electrical connection between electrodes through the electrical conductor 51 in the VIA holes 41 shown in FIG. 17C, and separation of the semiconductor-substrate shown in FIG. 17D can be done by using one of the above-mentioned methods.

(Example 3 of light-emitting device manufacturing)

Other manufacturing method of the light-emitting device 1 is described with reference to FIG. 18A, FIG. 18B, and FIG. 18C. In this manufacturing method, in the same manner mentioned above with reference to FIG. 7A, VIA holes 41 are pre-formed in the insulating layer 4, and

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moreover, the mount -surface-electrodes 5 and the electrical conductor 51 in the VIA holes 41 are also pre-formed in the insulating layer 4. Furthermore, VIA electrodes 52 which are corresponding to the semiconductor-surface-electrodes 21, 31 are also formed around VIA holes 41 on the surface of the insulating layer 4. Such VIA electrodes 52 are formed electrically and reliably to connect electrical conductor 51 and semiconductor-surface-electrodes 21, 31. In this method, the insulating layer 4 before bonding already has VIA's 10 and mount-surface-electrodes 5, in their final states.

By using such a insulating layer 4 having VIA's 10 and mount-surface-electrodes 5, as shown in FIG. 18B, light-emitting device 1 can be formed by bonding the insulating layer 4 and semiconductor-substrate together. The bonding can be done by using one of the above-mentioned methods. Furthermore, as shown in FIG. 18C, light-emitting device 1 from which the transparent crystal substrate is removed, can be obtained by using one of the above-mentioned methods. Although the present invention has been fully described by way of example with reference to the accompanying drawings, it is to be understood that various changes and modifications will be apparent to those skilled in the art.

The present application claims the priority based upon the patent application filed on September 24, in 2003. The entire contents of the application are incorporated into the present application by reference thereto.

CLAIMS

1. A light-emitting device formed by depositing p-type and n-type nitride semiconductor layers, comprising:

semiconductor-surface-electrodes to apply currents into each of the semiconductor layers;

an insulating layer which holds the semiconductor layers; and

mount-surface-electrodes provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made;

wherein one of the semiconductor layers has a non-deposited area where the other semiconductor layer is not deposited;

one of the semiconductor-surface-electrodes is built up on the surface of the non-deposited area;

VIA's are made in the insulating layer which connect electrically the semiconductor-surface-electrodes and the mount-surface-electrodes; and

the semiconductor-surface-electrodes, the insulating layer, and the mount-surface-electrodes are built up in this order on one side of the deposited semiconductor layers.

2. The light-emitting device of claim 1, wherein the insulating layer is made of one of resin, ceramics, or silicon.

3. The light-emitting device of claim 1, wherein the VIA is filled with electric conductor.

4. The light-emitting device of claim 1, wherein phosphor is provided on the surface or in the interior portion of the semiconductor layer.

5. A manufacturing method of light-emitting device, comprising:

a substrate forming process in which a semiconductor-substrate is formed by depositing p-type and n-type semiconductor layers on a transparent crystal substrate with a partly non-deposited portion, and by providing semiconductor-surface-electrodes on the semiconductor layers to apply currents into each of the semiconductor layers, wherein each of the electrode surfaces is exposed in one direction;

VIA forming process in which an insulating layer is formed on the surface of the semiconductor-substrate where the semiconductor-surface-electrodes are provided, also holes for VIA are made by partly removing the insulating layer over the semiconductor-surface-electrodes, also electric conductors are provided to form VIA's on the exposed surfaces of the semiconductor-surface-electrodes exposed by the insulator removals and on the inner walls of the holes for VIA, and also mount-surface-electrodes electrically connected to the semiconductor-surface-electrodes through the VIA are made on the surface of the insulating layer; and

substrate separation process in which the transparent crystal substrate is separated off from the semiconductor layers after the VIA forming process.

6. The manufacturing method of light-emitting device of claim 5, wherein the insulating layer is made of one of resin, ceramics, or silicon.

7. A manufacturing method of light-emitting device of claim 5, wherein the insulating layer formed in the VIA forming process is made of a insulating material of resin coated copper.

8. The manufacturing method of light-emitting device of claim 7, wherein the partial removal of the resin over the semiconductor-surface-

electrodes in the VIA forming process is done firstly by removing copper foils located on predefined resin of the resin coated copper, and secondly using the remained foil as a mask for resin removal process.

9. The manufacturing method of light-emitting device of claim 5, wherein the partial removal of the insulating layer over the semiconductor-surface-electrodes in the VIA forming process is done by exposing the insulating layer to laser beams or plasma.

10. The manufacturing method of light-emitting device of claim 5, wherein the separation of the transparent crystal substrate in the substrate separation process is done by using laser beams.

11. The manufacturing method of light-emitting device of claim 10, wherein a roughness structure is formed on a separation-induced surface of the semiconductor layers simultaneously with the separation of the transparent crystal substrate from the semiconductor layers by using laser beams.

12. The manufacturing method of light-emitting device of claim 11, wherein the roughness structure on the surface of the semiconductor layers is formed by irradiating the surface of the semiconductor layers with laser beams dedicated to forming the roughness structure along with the irradiation with the laser beams dedicated to separating the transparent crystal substrate.

13. A manufacturing method of light-emitting device, comprising:

a substrate forming process in which a semiconductor-substrate is formed by depositing p-type and n-type semiconductor layers on a transparent crystal substrate with a partly non-deposited portion, and by

providing semiconductor-surface-electrodes on the semiconductor layers to apply currents into each of the semiconductor layers, wherein each of the electrode surfaces is exposed in one direction;

VIA forming process in which an insulating layer having pre-formed holes for VIA corresponding to the semiconductor-surface-electrodes is laminated on the surface of the semiconductor-substrate where the semiconductor-surface-electrodes are provided, also electric conductors are provided to form VIA's on the surfaces of the semiconductor-surface-electrodes and on the inner walls of the holes for VIA, and also mount-surface-electrodes electrically connected to the semiconductor-surface-electrodes through the VIA are made on the surface of the insulating layer; and

substrate separation process in which the transparent crystal substrate is separated off from the semiconductor layers after the VIA forming process.

14. The manufacturing method of light-emitting device of claim 13, wherein the insulating layer is made of one of resin, ceramics, or silicon.

15. The manufacturing method of light-emitting device of claim 13, wherein the holes in the insulating layer are formed by exposing the insulating layer to laser beams or plasma.

16. The manufacturing method of light-emitting device of claim 13, wherein the separation of the transparent crystal substrate in the substrate separation process is done by using laser beams.

17. The manufacturing method of light-emitting device of claim 16, wherein a roughness structure is formed on a separation-induced surface of

the semiconductor layers simultaneously with the separation of the transparent crystal substrate from the semiconductor layers by using laser beams.

18. The manufacturing method of light-emitting device of claim 17, wherein the roughness structure on the surface of the semiconductor layers is formed by irradiating the surface of the semiconductor layers with laser beams dedicated to forming the roughness structure along with the irradiation with the laser beams dedicated to separating the transparent crystal substrate.

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FIG. 1

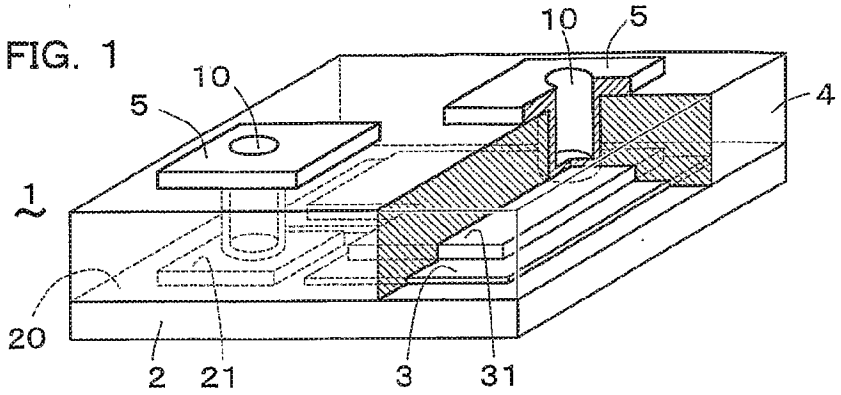


FIG. 2

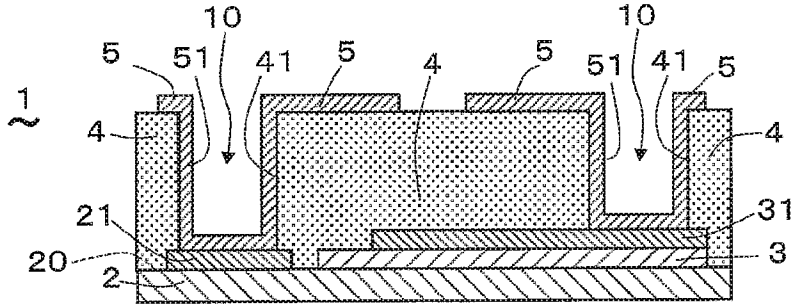


FIG. 3A

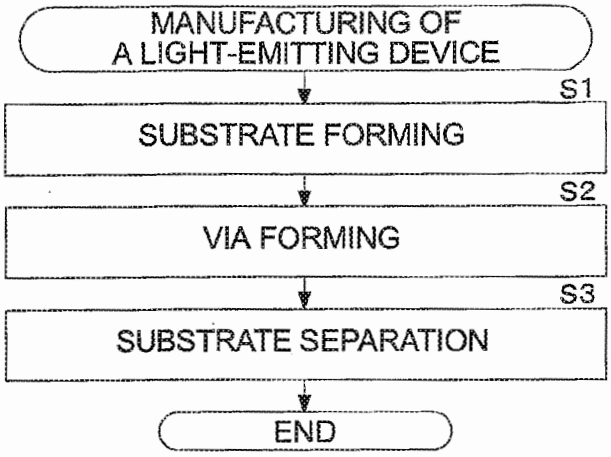


FIG. 3B

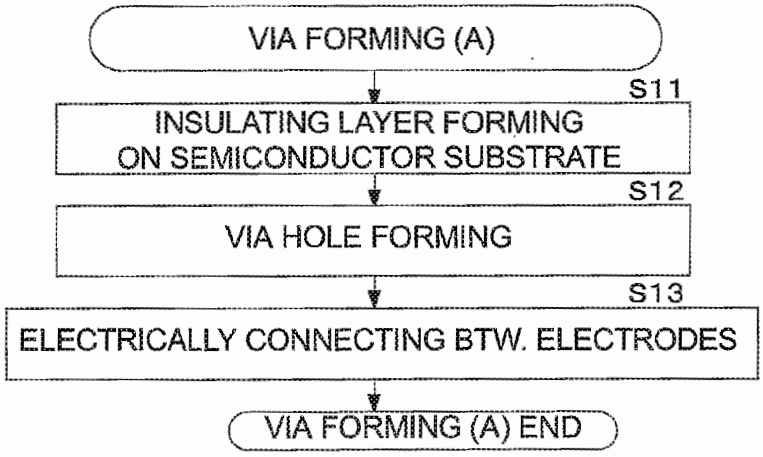


FIG. 3C

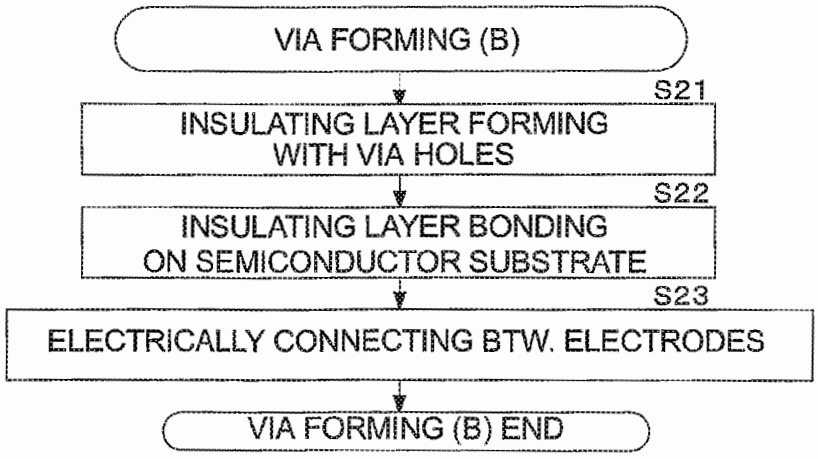


FIG. 4A

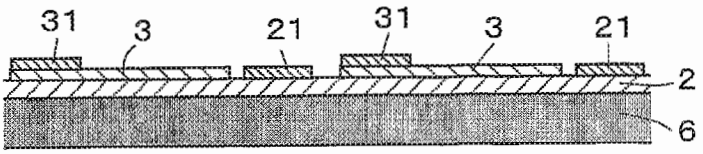


FIG. 4B

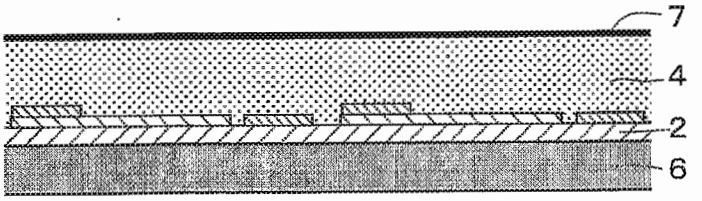


FIG. 4C

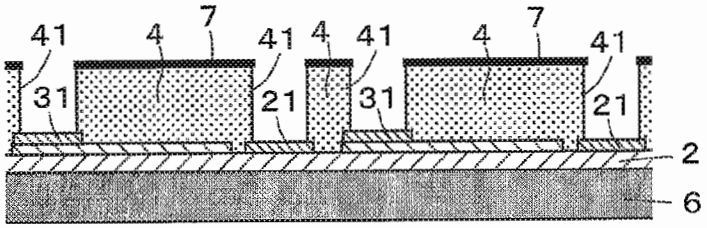


FIG. 4D

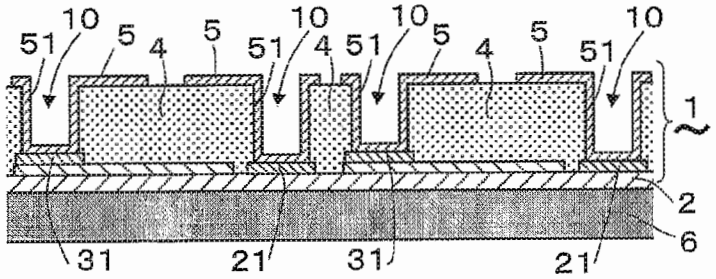


FIG. 4E

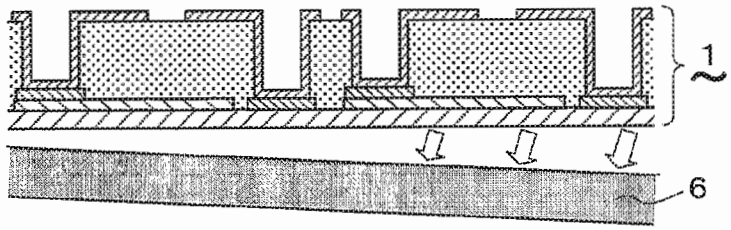


FIG. 5A

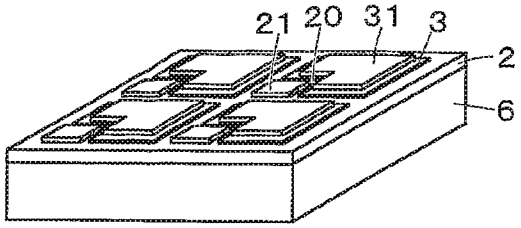


FIG. 5B

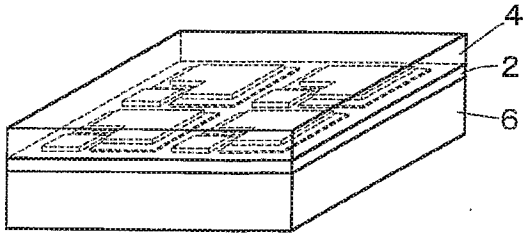


FIG. 5C

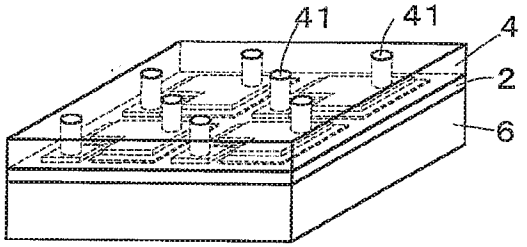


FIG. 5D

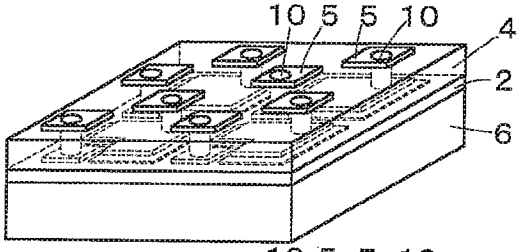


FIG. 5E

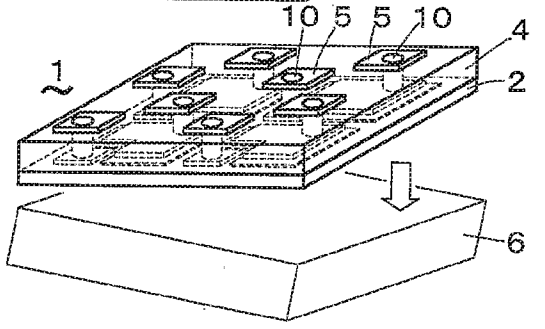


FIG. 6

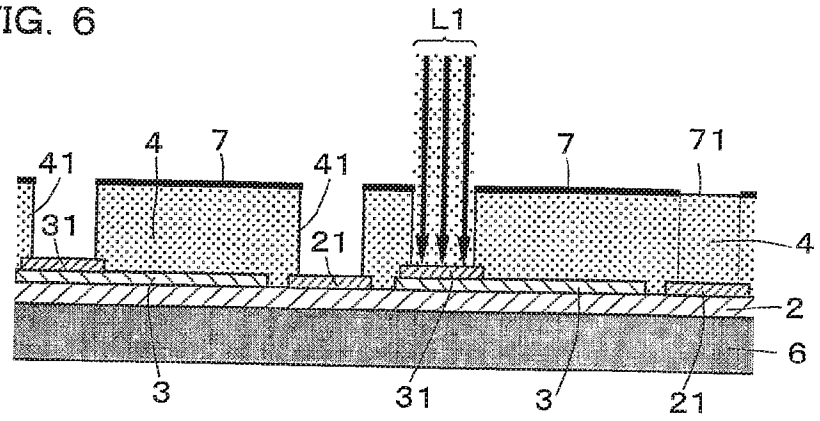


FIG. 7

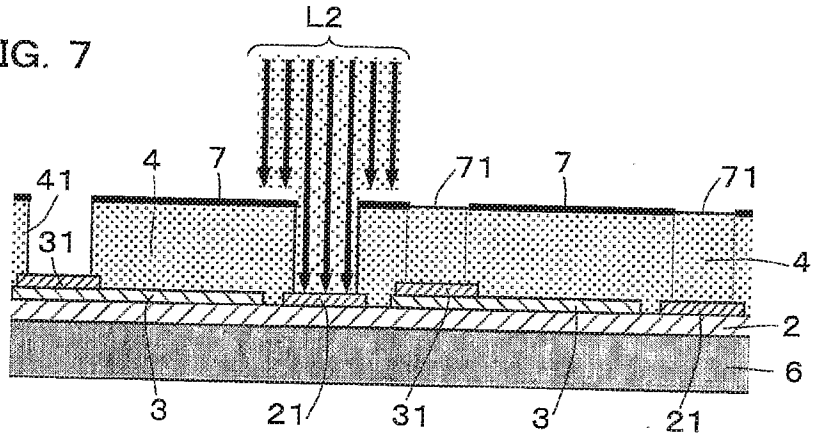


FIG. 8

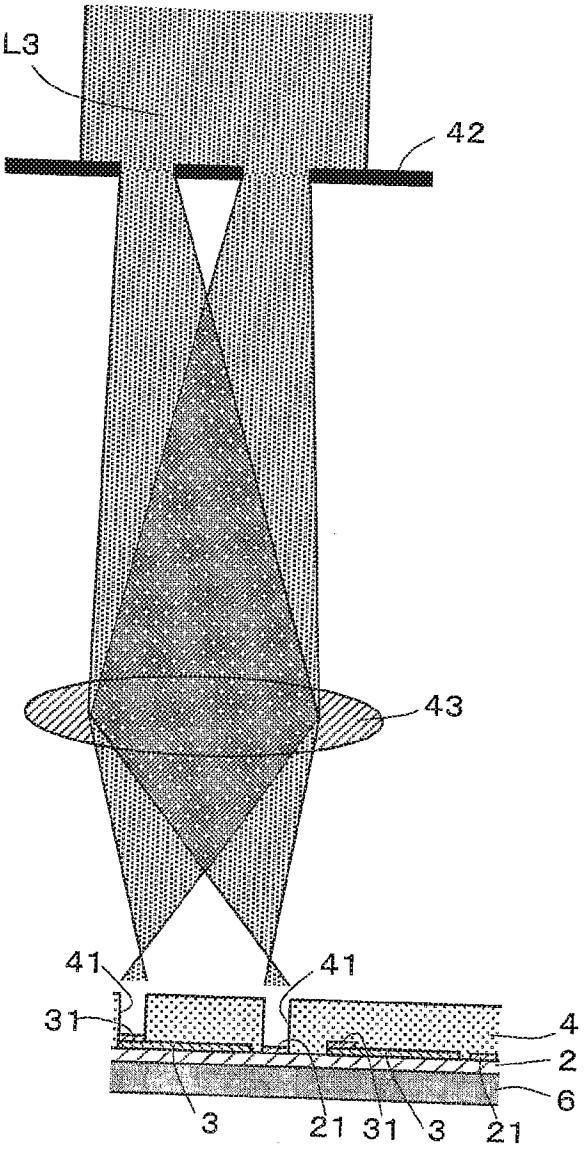


FIG. 9

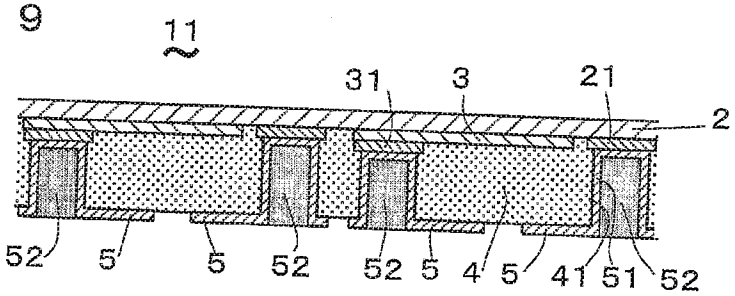


FIG. 10A

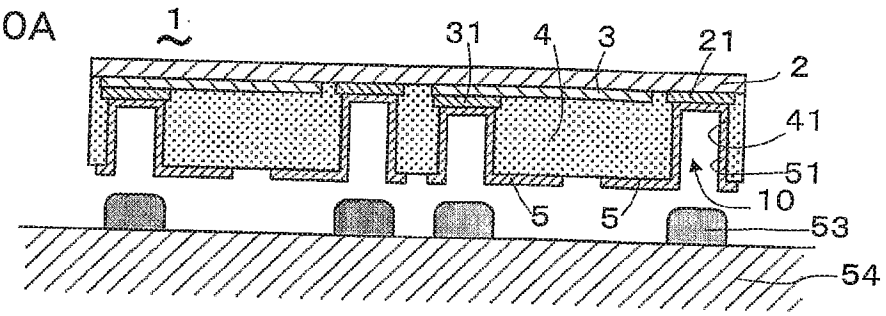


FIG. 10B

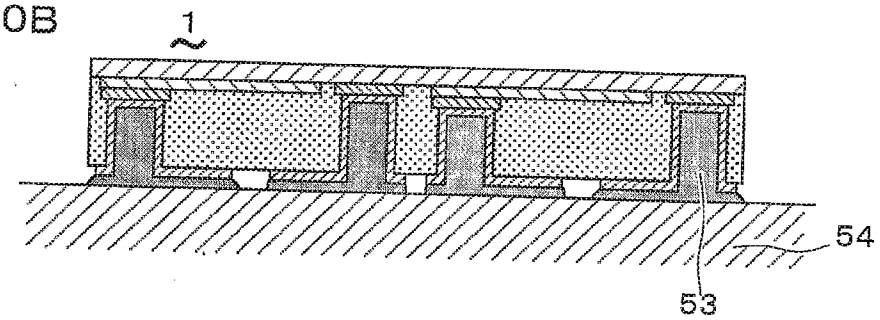


FIG. 11A

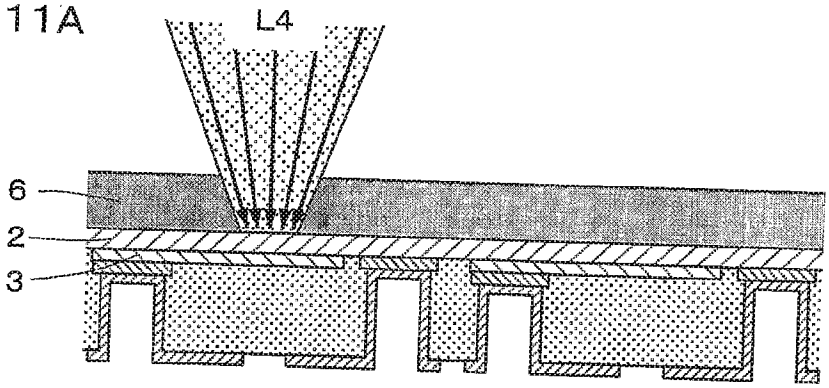


FIG. 11B

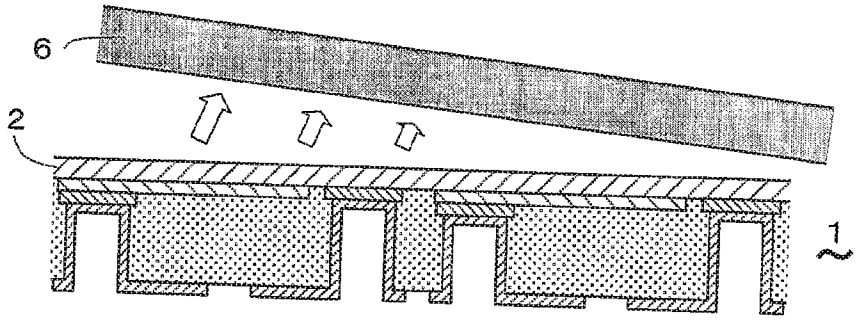


FIG. 12A

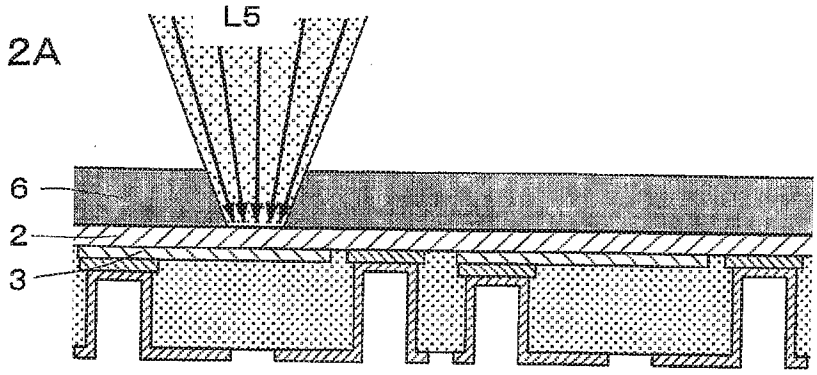


FIG. 12B

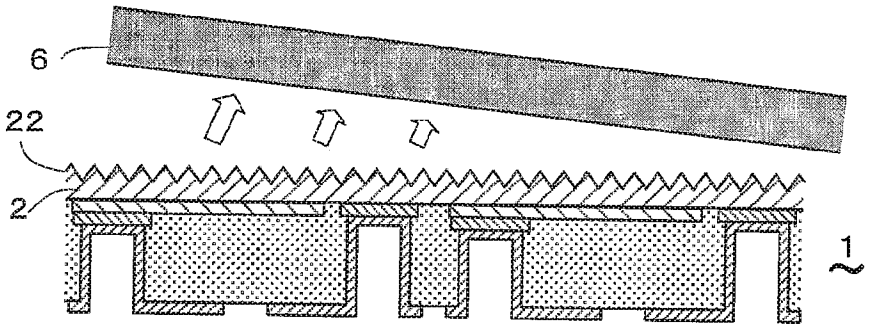


FIG. 13

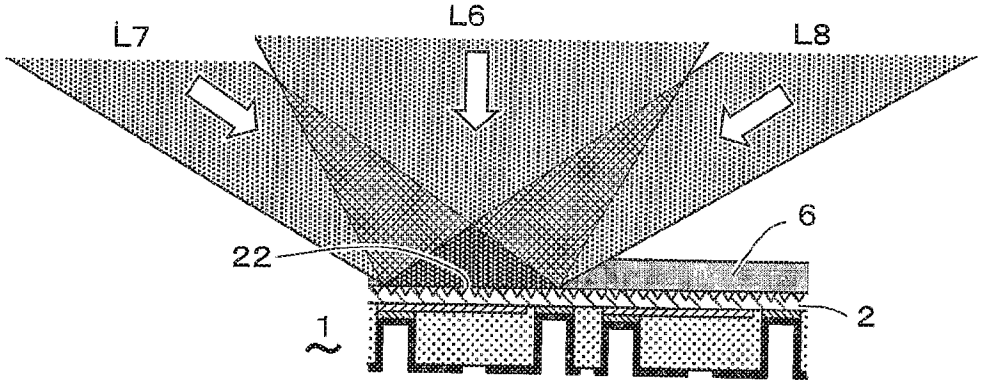


FIG. 14

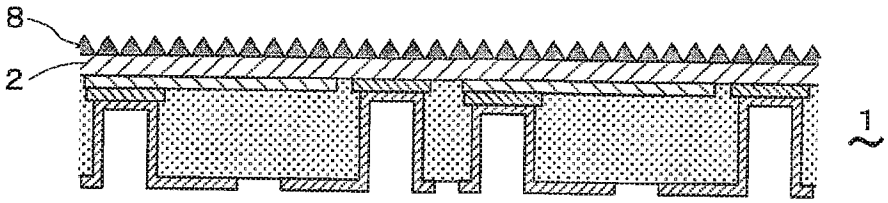


FIG. 15

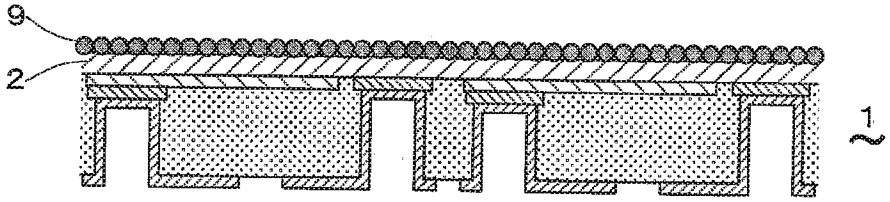


FIG. 16

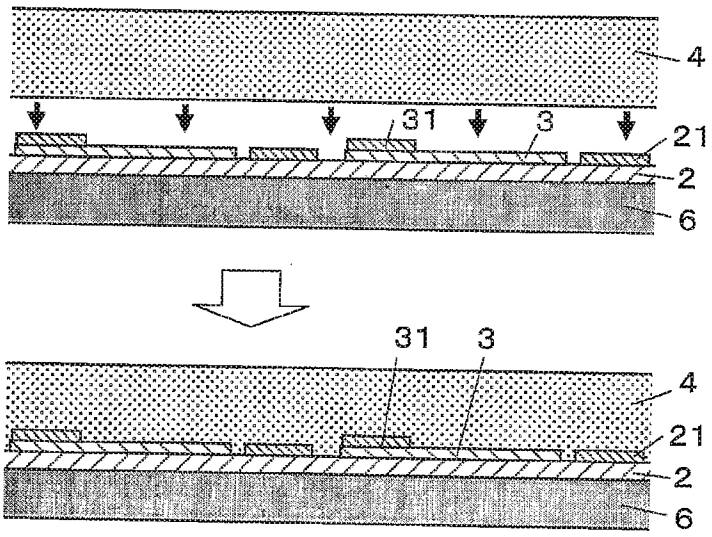


FIG. 17A

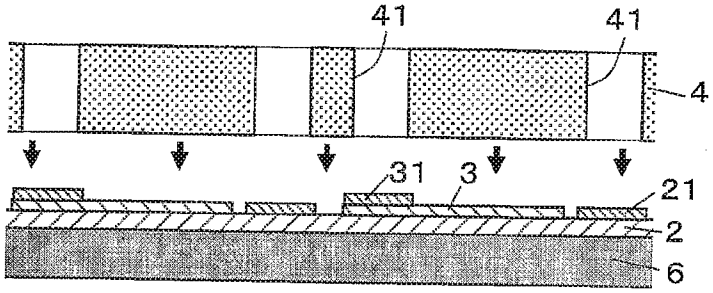


FIG. 17B

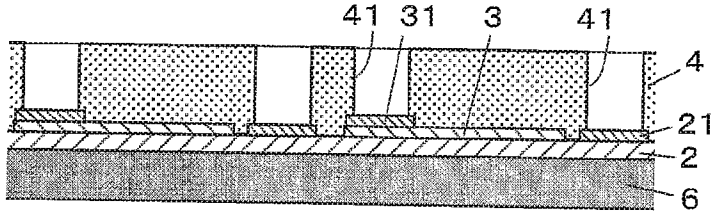


FIG. 17C

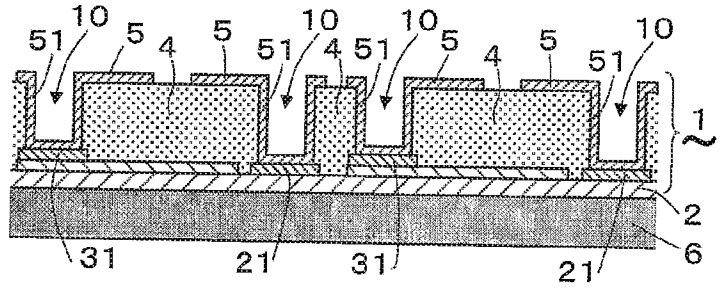


FIG. 17D

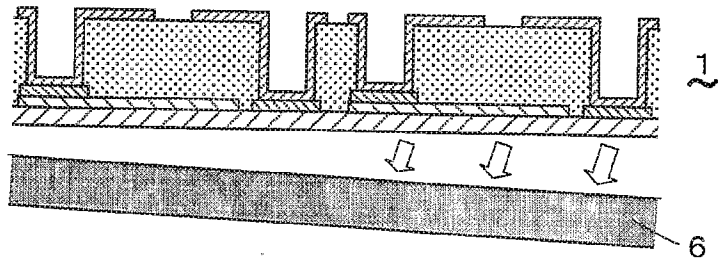


FIG. 18A

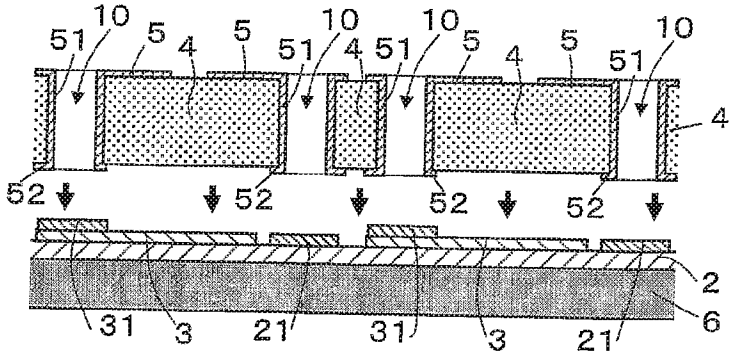


FIG. 18B

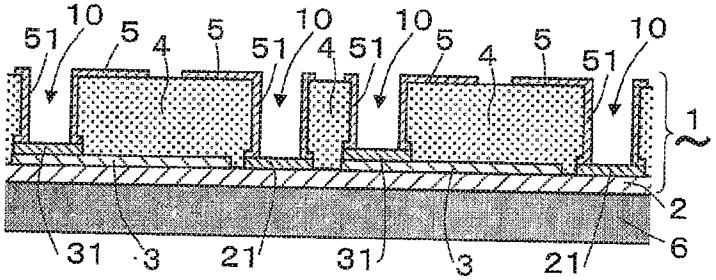


FIG. 18C

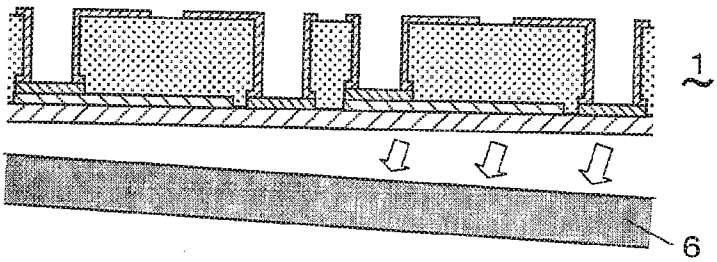


FIG. 19A

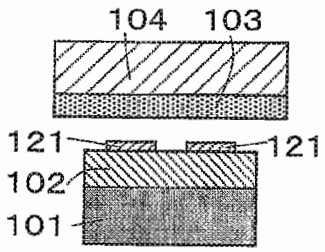


FIG. 19B

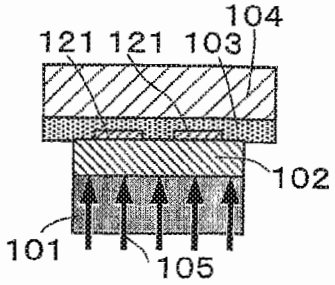


FIG. 19C

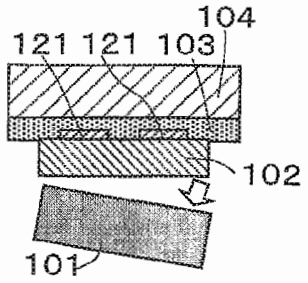


FIG. 19D

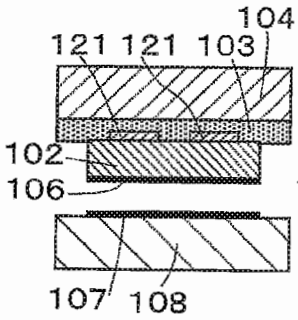


FIG. 19E

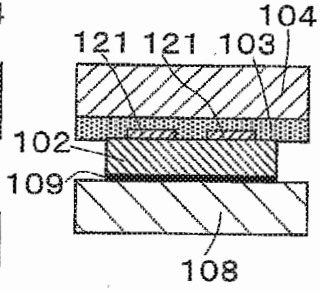
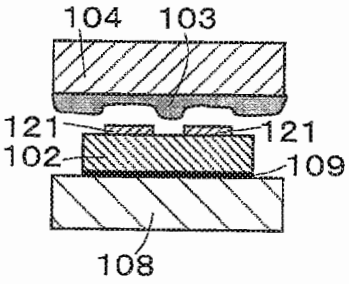


FIG. 19F



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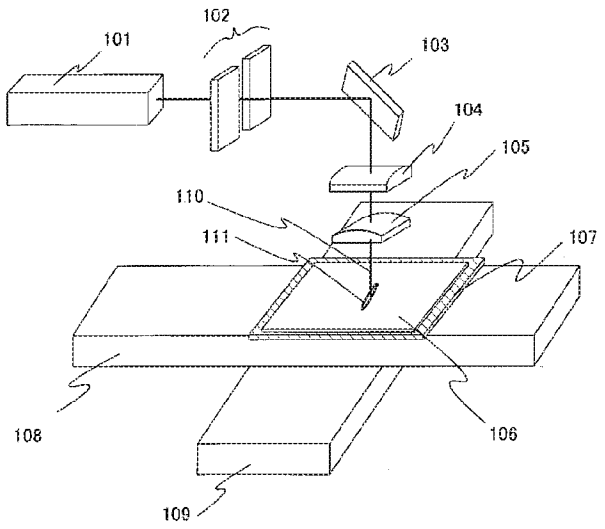
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** LASER IRRADIATION METHOD, LASER IRRADIATION APPARATUS AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE



(57) **Abstract:** In conducting laser annealing using a CW laser or a quasi-CW laser, productivity is not high as compared with an excimer laser and thus, it is necessary to further enhance productivity. According to the present invention, a fundamental wave is used without putting laser light into a non linear optical element, and laser annealing is conducted by irradiating a semiconductor thin film with pulsed laser light having a high repetition rate. A laser oscillator having a high output power can be used for laser annealing, since a non linear optical element is not used and thus light is not converted to a harmonic. Therefore, the width of a region having large grain crystals that is formed by scanning once can be increased, and thus the productivity can be enhanced dramatically.

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DESCRIPTION

LASER IRRADIATION METHOD, LASER IRRADIATION APPARATUS AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

TECHNICAL FIELD

The present invention relates to a laser irradiation apparatus for irradiating an object with laser light, a method for forming a crystalline semiconductor film using the apparatus, and a manufacturing method of a semiconductor device. In addition, the present invention relates to a semiconductor device having a circuit including a thin film transistor (also referred to as a TFT) or a photovoltaic device (such as an optical sensor or a solar battery). Further, the present invention relates to an electronic device incorporating, as a part thereof, e.g., an electro-optic device typified by a liquid crystal display panel, a light-emitting display device having an organic light-emitting element, a sensor device such as a line sensor, or a memory device such as SRAM.

Note that a semiconductor device in this specification means a generic device which can operate with use of semi-conductive characteristics and includes all types of devices such as an electro-optic device, a semiconductor circuit and an electronic device.

BACKGROUND ART

In recent years, a technology for forming a thin film transistor (TFT) using a semiconductor thin film (a thickness of around several nanometers to several hundred nanometers) formed over a substrate having an insulating surface has been attracting attention. Thin film transistors are broadly applied to electronic devices such as an IC or an electro-optic device, and are particularly developed as switching elements for image display devices at a rapid rate.

A semiconductor thin film that can be used for higher speed operation has been required since a image display device or an image sensor is made larger and higher density of pixels (high definition) is advanced recently. In addition, in order to achieve

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light-weight or cost reduction, a thin film transistor is applied also to a driver element in the periphery of a display region, as well as a switching element of an image display device.

A method for enhancing electric characteristics such as mobility by forming a semiconductor thin film having a crystal structure, for example, a solid phase epitaxy method or a laser annealing method has been studied.

The solid phase epitaxy method is a method by which an amorphous silicon thin film is formed over a substrate and is heated to become a polycrystal thin film. The heating is conducted at a temperature of about 600 to 1000 °C for a long time, and an expensive quartz substrate that can endure high temperature is required.

Glass substrates are of great promise in terms of costs as compared with quartz substrates or single crystal semiconductor substrates. However, glass substrates have poor heat resistance and are easy to be deformed by heat. Thus, in the case of forming a TFT using a polycrystal semiconductor film over a glass substrate, a laser annealing method is suitable for crystallization of a semiconductor film to prevent a thermal deformation of the glass substrate.

The laser annealing has advantages that the processing time can be shortened to a large degree as compared with another annealing method using radiation heat or conduction heat, and that a semiconductor substrate or a semiconductor film can be heated selectively, so that the substrate is hardly damaged thermally.

Laser oscillators are classified broadly into two kinds, which are a pulsed laser oscillator and a continuous wave laser oscillator, in a standpoint of the oscillation method. Laser light (also, referred to as a laser beam) oscillated from a pulsed excimer laser is used for laser annealing in many cases. The excimer laser has advantages that it has a high output power and repetition irradiation is possible at a high frequency.

Laser light oscillated from an excimer laser has an advantage such as high absorption efficiency to a silicon thin film that is used as a semiconductor film in many cases.

For example, in laser irradiation, laser light is shaped into linear laser light on the irradiation surface by an optical system (such as a beam homogenizer) and

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irradiation position of laser light is moved relatively to the irradiation surface. This method is superior industrially because an amorphous silicon film having a large area can be crystallized at one time and thus, high productivity is obtained by this method. Hereinafter, laser light having a linear shape on an irradiation surface is referred to as a linear beam.

DISCLOSURE OF INVENTION

A conventional laser annealing method using laser light oscillated from a pulsed excimer laser has some problems to be solved, for example, a problem that crystal diameter or crystallinity is not uniform, a problem that electric characteristics of a TFT are not stable, and the like.

As one of methods for solving the problems, there is a method in which a continuous wave laser (hereinafter, CW laser) such as an Ar laser or a YVO_4 laser or a pulsed laser having an extremely high repetition rate of 10 MHz or higher (hereinafter, a quasi-CW laser) is employed.

It is found that a grain diameter of a crystal formed in a semiconductor film is enlarged by using laser light oscillated from a CW laser or a quasi-CW laser. Electric characteristics such as mobility become higher, as the grain diameters of crystals in polycrystal silicon thin film is larger in general. When the grain diameters of crystals in the semiconductor film becomes large, the number of crystal boundaries located in a channel forming region of a TFT formed with the semiconductor film is reduced. Thus, the mobility becomes higher and the semiconductor film can be used for a development of a higher performance device. Hereinafter, a crystal having a large grain diameter is referred to as a large grain crystal.

However, in the case of using a CW laser and a quasi-CW laser using a solid state laser medium, the wavelength band of the fundamental wave is from red ray to near-infrared ray, and absorption efficiency of the semiconductor film is extremely low. Laser light having high absorption efficiency of the semiconductor film is laser light having a wavelength of visible light to ultraviolet light.

Therefore, in the case of using a CW laser and a quasi-CW laser for a laser

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annealing method, a wavelength is converted to a harmonic of visible light or shorter with a non linear optical element. For example, the highest conversion efficiency can be obtained in the method of converting a fundamental wave of near-infrared ray that easily provides a high output to green laser light of the second harmonic.

Harmonics can be obtained by putting a fundamental wave oscillated from a laser medium into a non linear optical element. However, there is a problem that, when the output of laser becomes high, a non linear optical element is damaged by a non linear optical effect such as multiphoton absorption, and thus, is broke down. Therefore, a CW laser of visible range that is produced at present has an output power of at most about 15 W due to a problem of a non linear optical element.

Further, in conducting laser annealing using a CW laser or a quasi-CW laser, productivity is not high as compared with an excimer laser and thus, it is necessary to further enhance productivity. For example, CW laser light of 532 nm with 10W is formed into a linear beam of about 300 μm in a long-side direction and about 10 μm in a short-side direction to conduct laser annealing. At this time, the width of a region having large grain crystals which is formed by scanning once is about 200 μm. Accordingly, scanning of a beam spot is required to be conducted several thousand times in order to crystallize the whole surface of a semiconductor film in rectangle with several hundreds mm or more on one side that is used in a mass production process.

According to the present invention, a fundamental wave is used without putting laser light into a non linear optical element, and laser annealing is conducted by irradiating a semiconductor thin film with pulsed laser light having a high repetition rate. One feature of the present invention is that the repetition rate of a laser used in the present invention is 10 MHz or more.

High intensity means a high peak output power per unit of time and per area, and the peak output power of laser light according to the present invention ranges from $1GW/cm^2$ to $1TW/cm^2$.

A fundamental wave with a wavelength of about 1 μm is not absorbed so much by a semiconductor thin film in irradiating the semiconductor thin film with the fundamental wave. Thus, the fundamental wave has a low absorption efficiency. The

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present inventors have found that a fundamental wave emitted from a pulsed laser having a pulse width in the range of picosecond, or in the range of femtosecond (10^{-15} seconds) can provide high intensity laser light. Thus, a non linear optical effect (multiphoton absorption) is generated and the fundamental wave is absorbed by the semiconductor film.

According to the present invention, a laser oscillator having a higher output power than 15 W, e.g., 40 W output power can be used for laser annealing, since a non linear optical element is not used and thus light is not converted to a harmonic. Therefore, the width of a region having large grain crystals that is formed by scanning once can be increased, and thus the productivity can be enhanced dramatically.

In addition, according to the present invention, multiphoton absorption is generated to melt a semiconductor thin film, and thus, the thickness of the semiconductor thin film is small and for example, even a semiconductor thin film having a thickness of 100 nm or less can absorb high intensity laser light. Therefore, a formation time of a semiconductor thin film can be shortened by making the thickness of the semiconductor thin film smaller.

A structure of the present invention relating to a laser irradiation method disclosed in this specification is a laser irradiation method comprising the steps of: emitting a first laser beam which is a fundamental wave from a laser oscillator having a repetition rate of 10 MHz or higher; forming the first laser beam into a second laser beam with a condenser lens; delivering the second laser beam onto an irradiation surface; and moving the second laser beam relatively to the irradiation surface.

Another structure of the present invention relating to a laser irradiation method is a laser irradiation method comprising the steps of: emitting a first laser beam which is a fundamental wave from a laser oscillator having a repetition rate of 10 MHz or higher; forming the first laser beam into a second laser beam with a condenser lens; delivering the second laser beam onto an object to generate multiphoton absorption for melting the object; and moving the second laser beam relatively to the object.

In the above structure, the first laser beam is emitted with a pulse width of 1 femtosecond or more and 10 picoseconds or less. The pulsed width of 1 femtosecond

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or more and 10 picoseconds or less is employed to obtain a sufficiently high intensity for generating multiphoton absorption. A laser beam with a pulsed width of several ten picoseconds longer than ten picoseconds does not generate multiphoton absorption. In addition, when an experimental test for heating a semiconductor film by a laser beam with a pulse width of 150 femtoseconds was conducted, it could be observed that the semiconductor film was heated. Therefore, it is thought that multiphoton absorption is generated.

In addition, a laser irradiation apparatus including a laser oscillator in which a non linear optical element is not incorporated and an optical member is also one feature of the present invention. A structure thereof is a laser irradiation apparatus comprising: a laser oscillator for emitting a fundamental wave; an optical member for processing a laser beam emitted from the laser oscillator into a long laser beam on an irradiation surface; and means for moving the irradiation surface relatively to the laser beam.

Further, another structure is a laser irradiation apparatus comprising: a laser oscillator for emitting a fundamental wave; a condenser lens for forming a laser beam emitted from the laser oscillator; a mechanism for projecting and delivering the laser beam using the condenser lens onto an irradiation surface; and means for moving the irradiation surface relatively to the laser beam.

The above-described laser irradiation apparatus of the present invention does not incorporate a non linear optical element and thus, the cost for the non linear optical element can be reduced from the cost for manufacturing the irradiation apparatus.

In general, when an energy gap of one photon is smaller than an energy gap of a semiconductor film, the photon is not absorbed by the semiconductor film. Thus, in a conventional manner, energy of one photon is increased by converting a fundamental wave to a harmonic with a non linear optical element as described above. In the case of using an n-th harmonic with a wavelength λ, the energy E of one photon is represented by the next equation using Planck's constant $\hbar$ and light velocity c.

$$E = \frac{\hbar c}{\lambda / n} \qquad \text{EQUATION 1}$$

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For example, light with a wavelength of 1064 nm corresponds to energy of 1.17 eV. Thus, in the case of using an amorphous silicon film with an energy band gap of 1.6 to 1.8 eV as a semiconductor film, absorption is not made. Light with a wavelength of 532 nm corresponds to energy of 2.34 eV, and thus, absorption is made to an amorphous silicon film.

However, when laser light with high intensity is used, high electromagnetic field is generated in a material irradiated with laser light, thereby generating a nonlinear optical effect (multiphoton absorption). By the multiphoton absorption, photons can be absorbed at the same time multistep without letting light passing through the semiconductor film, in the case where the energy of one photon smaller than the energy band gap of the semiconductor film .

For example, when an amorphous silicon film is irradiated with laser light having a wavelength of 1064 nm, the energy of one photon is 1.17 eV and thus, absorption by the amorphous silicon film is not made. However, two photons are simultaneously absorbed by multiphoton absorption and thus, 2.34 eV similarly to the second harmonic is obtained to generate light absorption.

As a laser that can provide high enough intensity to cause multiphoton absorption, there is a short pulsed laser with a pulse width of pico second or femto second in its unit. As the pulsed laser, lasers in which Nd, Yb, Cr, Ti, Ho, Er, and the like are added as a dopant into crystals of Sapphire, YAG, ceramics YAG, ceramics Y_2O_3, KGW, KYW, Mg_2SiO_4, YLF, YVO_4, $GdVO_4$ and the like are given.

In the above described structure, the condenser lens includes two pieces of convex cylindrical lenses. In addition, an optical member may be arranged appropriately in a path from a laser oscillator to an irradiation surface without being limited to a dioptric member typified by a condenser lens. As other optical members that can be applied to the present invention, there is given catoptrical optical member such as a mirror or a diffractive optical member such as diffraction grating.

In the present invention, a pulsed laser having a repetition rate of 10 MHz or higher is used. This is because it takes about 100 nano seconds for an amorphous silicon film that has been melted by absorbing laser light to be recrystallized by cooling

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due to thermal diffusion, in the case of using the amorphous silicon film as a semiconductor film. By irradiating the same portion in the amorphous silicon film with laser light again within 100 nanoseconds, a melted state of the film can be maintained. Therefore, when a pulsed laser having a repetition rate of 10 MHz or more is adopted, it can be considered as a CW laser in a quasi manner and thus, such a laser is referred to as a quasi-CW laser.

Another aspect of the present invention is to manufacture a semiconductor device by a laser annealing method in which a fundamental wave is emitted. A structure of the manufacturing method is a laser irradiation method comprising the steps of: processing a laser beam which is a fundamental wave on a surface of a semiconductor into a long laser beam; and moving the surface of the semiconductor relatively to the long laser beam to be irradiated with the long laser beam so as to crystallize the semiconductor.

An impurity element added to a semiconductor can be activated by a laser annealing method in which a fundamental wave is emitted. And another structure of manufacturing method of a semiconductor device is a laser irradiation method comprising the steps of: forming an impurity region in a semiconductor; processing a laser beam which is a fundamental wave on a surface of a semiconductor into a long laser beam; and moving the surface of the semiconductor relatively to the long laser beam so as to activate the impurity region formed in the semiconductor.

A laser annealing method in which a fundamental wave is emitted can be employed to a semiconductor layer over a conductive layer with an insulating film therebetween. A laser irradiation method comprising the steps of: forming a conductive layer over a glass substrate; forming an insulating layer to cover the conductive film; forming a semiconductor layer over the insulating layer; processing a laser beam which is a fundamental wave into a long laser beam on a surface of the semiconductor layer; and moving the surface of the semiconductor relatively to the long beam to be irradiated with the long beam.

Note that a laser annealing method in this specification indicates a technique by which a damaged layer or an amorphous layer formed in a semiconductor substrate or a

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semiconductor film is recrystallized or a technique by which an amorphous semiconductor film formed over a substrate is crystallized. In addition, the laser annealing method includes a technique for planarizing or surface modification of a semiconductor substrate or a semiconductor film.

In addition, multiphoton absorption in this specification means simultaneous absorption of two or more photons, and that reactive electronic excitation state, which cannot be reached by energy of one photon with the same energy as the two photons, can be reached by the absorption energy of two or more photons. It should be noted that the term "simultaneous" means that two phenomena occur within 10^{-14} seconds. In addition, the described above electronic excitation state is an electronic state of molecules at higher energy than an electronic ground state of molecules, which is achieved by absorbing electromagnetic radiated emission and in which a life time is longer than 10^{-13} seconds.

By the present invention, a non linear optical element for converting a wavelength is not needed, and a laser beam with an extremely large output power, for example, a laser beam having an output power twice or more times as large as a harmonic can be obtained. Therefore, the grain diameter of a crystal in a semiconductor film can be enlarged and the number of grain boundaries in a channel forming region of a TFT formed using the semiconductor film is reduced to increase the mobility. Thus, the semiconductor film is suitable for developing a high performance device.

Further, a non linear optical element has a defect that a maintenance-free state, which is an advantage of a solid state laser, cannot be kept long since the non linear optical element is easily changed in its quality. However, the present invention can overcome the defect, since the present invention does not need a non linear optical element. In other words, stability and reliability of a laser irradiation apparatus itself can be enhanced, according to the present invention.

BRIEF DESCRIPTION OF DRAWINGS

In the accompanying drawings:

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FIG. 1 is a perspective view showing one example of a laser irradiation apparatus according to an aspect of the present invention;

FIGS. 2-(1) and 2-(2) each show an optical system according to an aspect of the present invention;

FIG. 3 is an optical microscope photograph;

FIG. 4 is a SEM photograph;

FIGS. 5A to 5E are cross-sectional views showing a manufacturing process of a top gate TFT;

FIGS. 6A and 6B are cross-sectional views showing one example of GOLD structure TFT.

FIG. 7 is a cross-sectional view showing one example of a dual gate structure TFT;

FIG. 8 shows one example of a cross-sectional view of a display device;

FIGS. 9A and 9B each show a top view of a display device;

FIGS. 10A to 10C are cross-sectional views showing a manufacturing steps of a CPU;

FIGS. 11A to 11C are cross-sectional views showing manufacturing steps of a CPU;

FIGS. 12A to 12C are cross-sectional views showing manufacturing steps of a a CPU;

FIGS. 13A and 13B are cross-sectional views showing manufacturing steps of a CPU;

FIG. 14 is a block diagram of a CPU;

FIGS. 15A to 15E are cross-sectional views showing manufacturing steps of an IC tag;

FIGS. 16A to 16E are cross-sectional views showing manufacturing steps of an IC tag.

FIGS. 17A to 17C are cross-sectional views showing manufacturing steps of an IC tag.

FIGS. 18A and 18B are cross-sectional views showing manufacturing steps of

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an IC tag; and

FIGS. 19A to 19E each show one example of electronic devices.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiment Modes of the present invention are described below. The present invention can be carried out in many different modes, and it is easily understood by those skilled in the art that modes and details herein disclosed can be modified in various ways without departing from the spirit and the scope of the present invention.

Embodiment Mode 1

FIG. 1 shows one example of a laser irradiation apparatus according to the present invention.

As a laser oscillator 101 shown in FIG. 1, a laser oscillator that oscillates with a pulse width in the range of femtosecond (10^{-15}second) is used (also referred to as a femtosecond laser). As the laser oscillator, lasers in which Nd, Yb, Cr, Ti, Ho, Er, and the like are added as a dopant into crystals of Sapphire, YAG, ceramics YAG, ceramics Y_2O_3, KGW, KYW, Mg_2SiO_4, YLF, YVO_4, $GdVO_4$ and the like are given. Note that a non linear optical element is not included in the laser oscillator 101 and thus a fundamental wave of a laser beam is emitted. A non linear optical element for converting light oscillated from a laser medium to a harmonic is not included in the pulsed laser oscillator 101; however, the pulsed laser oscillator 101 has high enough light intensity to generate a non linear optical effect (multiphoton absorption) in a semiconductor film.

A laser beam emitted from the laser oscillator 101 passes through a slit 102. By the slit 102, a weak portion in energy of a laser beam can be blocked and the length in the long-side direction of the laser beam on an irradiation surface can be adjusted. The slit 102 used in the present invention is not especially limited, and a slit having a structure or a shape that can block a weak portion of intensity when light passes through a slit.

Thereafter, a laser beam that has passed through the slit 102 is changed in its direction by a mirror 103 and is deflected toward a semiconductor film 106 formed on a

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surface of a glass substrate. It should be noted that the direction of the laser beam that has been changed may be perpendicular or diagonal to the substrate.

Then, the laser beam whose direction has been changed by the mirror 103 projects an image of the slit 102 onto the semiconductor film 106 that is an irradiation surface by a cylindrical lens 104 that operates only in one direction. Further, the laser beam is converged in one direction by a second cylindrical lens 105 which is rotated by 90° from the first cylindrical lens 104 and which operates only in one direction. Then, the laser beam is delivered to the semiconductor film 106. A beam irradiation region 111 having a linear, elliptical or rectangle shape on the irradiation surface is obtained by the first and second cylindrical lenses 104 and 105. By the first cylindrical lens 104, a laser beam is formed in a long-side direction of the beam irradiation region 111, and by the second cylindrical lens 105, the laser beam is formed in a short-side direction of the beam irradiation region 111. The cylindrical lens used in the present invention may be planoconvex on the side which the laser beam is incident into or emitted from or biconvex. In the case of the planoconvex cylindrical lens, it is preferable that the cylindrical lens has a convex surface on the side where the laser beam is incident in point of low aberration and high accuracy.

An optical system of the present invention is described in detail with reference to FIGS. 2-(1) and 2-(2). The reference numerals used in FIGS. 2-(1) and 2-(2) are the same as those in FIG.1. FIG. 2-(1) shows a long-side direction of a laser irradiation region and FIG. 2-(2) shows a short-side direction of the laser irradiation region. A laser beam emitted from the laser oscillator 101 is blocked partially by the slit 102 and only a portion of the laser beam having high intensity passes through the slit. The laser beam that has passed through the slit projects an image formed by the slit 102 onto the semiconductor film 106 by the first cylindrical lens 104. The laser beam 110 shown by the solid line in FIG. 1 shows a laser beam that passes through a center of the beam irradiation region 111.

The positional relations among the first cylindrical lens 104, the slit 102, and the semiconductor film 106 as an irradiation surface are described in detail. The slit 102 is used so as to prevent a portion of the laser beam having weak energy from being

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delivered onto the semiconductor film. If such a laser beam having the portion with weak energy is delivered onto the semiconductor film, a polycrystal region having relatively small crystal grains whose surface is uneven (here, referred to as a poorly crystalline region) is formed, which is not preferable. In view of the problem, the slit 102 is used so as not to form such a region in a semiconductor film. In general, when a laser beam is partially blocked by a slit, a phenomenon called diffraction due to coherence of laser light is caused and thus, diffraction fringes are generated in the laser beam. A method for preventing diffraction fringes on the irradiation surface is described below.

In the two equations shown below, f is the focal length of the first cylindrical lens 104, s is the width of the opening of the slit 102, M1 is the distance between the slit 102 and the cylindrical lens 104, M2 is the distance between the first cylindrical lens 104 and the semiconductor film 106, and L is the length of the linear beam in the long-side direction on the semiconductor film 106, which is the irradiation surface. The positional relations are given by the following two equations:

$$\frac{s}{L} = \frac{M1}{M2} \qquad \text{[Equation 2]}$$

$$\frac{1}{f} = \frac{1}{M1} + \frac{1}{M2} \qquad \text{[Equation 3]}$$

Based on these equations shown above, other two equations shown below can be given by:

$$M1 = \frac{f(s+L)}{L} \qquad \text{[Equation 4]}$$

$$M2 = \frac{f(s+L)}{s} \qquad \text{[Equation 5]}$$

Therefore, the fringes due to the diffraction are not translated to the semiconductor film by arranging the slit, the first cylindrical lens, and the irradiation surface, based on the above equations. Accordingly, the laser irradiation which hardly forms the poorly crystalline region can be achieved.

If a diameter, an output power or a shape of an emitted laser beam can be used

as they are, two cylindrical lenses are not necessarily used. In addition, when the ratio between a long-side and a short-side of the emitted laser beam is kept to converge light, a spherical lens may be used instead of a cylindrical lens.

The glass substrate provided with the semiconductor film 106 is moved at an appropriate speed to irradiate the whole surface of the substrate with laser light. The substrate provided with the semiconductor film 106 is made of a glass. In irradiating the substrate with laser light, the substrate is fixed on a substrate fixing stage 107 by sucking means or mechanically-fixing means so as not to drop. In addition, the substrate fixing stage 107 can be moved in X direction or in Y direction on a face parallel to a surface of the semiconductor film using an X stage 108 and a Y stage 109. By the X stage 108 and the Y stage 109, the glass substrate fixed on the substrate fixing stage 107 can be moved at a speed of 100 to 1000 mm/sec. Here, a stage on which a substrate is set is moved in X direction (or Y direction) with respect to the fixed irradiation region of a laser beam so as to scan laser light. It should be noted that an optimum scanning speed which is anticipated based on the experience of the present inventors is around 400 mm/sec.

The scanning method is not limited to the method in which X stage 108 and Y stage 109 are moved, and laser light may be scanned by a galvanometer mirror or a polygon mirror. A laser beam that is formed into a band-like shape along the vertical side direction (Y direction) of the substrate is delivered and the irradiation region is moved relatively to the substrate so as to scan laser light in the horizontal direction (X direction).

Actually, an amorphous silicon film formed on a glass substrate was irradiated with a laser beam by a laser annealing method of the present invention (laser medium: Ti:sapphire, output power of 1.3 W, wavelength of 800 nm, pulse width of 150 femtosecond, and repetition rate of 90 MHz), and at this time, crystallization could be conducted. The beam spot was 8 μm × 40 μm and the scanning speed of the stage was 100 mm/sec. An optical microscope photograph (magnification 1,000 times) of the surface of a semiconductor film obtained at this time is shown in FIG. 3. In addition, a SEM photograph of the surface of the semiconductor film obtained at this time is shown

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in FIG. 4. By the experiment, it can be confirmed that large grain crystals by crystallization according to the present invention can be formed.

The photograph shown in FIG. 3 is a photograph of a surface of a semiconductor film in which only a region irradiated with laser light by scanning in one direction is crystallized so as to distinguish the irradiation region from a non-irradiation region. In FIG. 3, scanning is partially conducted; however, it is natural that scanning is conducted at an appropriate speed to obtain large grain crystals on the whole surface of the substrate.

By the present invention, a semiconductor element such as a TFT is formed appropriately using a semiconductor film in which such large grain crystals are formed, and thus, it can be applied for a development of a high performance device.

Embodiment Mode 1 represents the example where the laser beam is delivered to the amorphous semiconductor film (amorphous silicon film) to be crystallized so as to obtain a semiconductor film having a crystalline structure (hereinafter, also referred to as a crystalline semiconductor film). However, the embodiment is not especially limited to the crystallization purpose but can be applied to a variety of laser annealing treatments typified by an activation treatment or a treatment for forming a silicide.

The present invention may be applied to laser irradiation for enhancing crystallinity and repairing defects remaining in crystal grains, for a crystalline semiconductor film that is crystallized by a solid phase epitaxy method or a method of adding a metal element for promoting crystallization such as Ni and heating it (Japanese Patent Laid-Open No. H7-130652 or Japanese Patent Laid-Open No. H8-78329).

Embodiment Mode 2

A manufacturing process of a top gate TFT according to the present invention is shown briefly with reference to FIGS. 5A to 5E. Laser light that has a repetition rate of 10 MHz or more and that is a fundamental wave is delivered to a semiconductor film having an amorphous structure (hereinafter, also referred to as an amorphous semiconductor film) and a non linear optical effect (multiphoton absorption) is caused to conduct crystallization.

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As shown in FIG. 5A, a base insulating film 11 serving as a blocking layer and an amorphous semiconductor film 12 are formed over a substrate 10 having an insulating surface.

A glass substrate such as a barium borosilicate glass or an alumino borosilicate glass is used for the substrate 10 having an insulating surface. In addition, a plastic substrate that can endure a processing temperature in this process, for example, a plastic substrate obtained by processing, into a sheet-like form, a material in which inorganic particles with a diameter of several nm are dispersed in an organic polymer matrix may be used.

As the base insulating film 11 formed over the substrate 10 having an insulating surface, an insulating film such as a silicon oxide film, a silicon nitride film or a silicon oxynitride film (SiO_xN_y) is used. As a typical example of the base insulating film 11, a two-layer structure in which a silicon nitride oxide film of 50 to 100 nm thick that is formed using SiH_4, NH_3 and N_2O as a reactive gas and a silicon oxynitride film of 100 to 150 nm thick that is formed using SiH_4 and N_2O as a reactive gas are stacked, can be employed. In addition, a silicon nitride film (SiN film) or a silicon oxynitride film (SiN_xO_y film, x>y) that is 10 nm or less thick is preferably used as one layer of the base insulating film 11. Alternatively, a three-layer structure in which a silicon nitride oxide film, a silicon oxynitride film and a silicon nitride film are continuously stacked may be employed.

A semiconductor material mainly containing silicon is used as the amorphous semiconductor film 12. Typically, an amorphous silicon film or an amorphous silicon germanium film is formed by a known method (such as sputtering, LPCVD or plasma CVD).

Instead of the amorphous semiconductor film 12, a crystalline semiconductor film that is formed without being subjected to crystallization separately (such as a polycrystal silicon film, a microcrystal semiconductor film or a semiamorphous semiconductor film) may be used.

Thereafter, the laser irradiation apparatus shown in FIG. 1 is used to irradiate the amorphous semiconductor film 12 with laser light that has a repetition rate of 10

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MHz or more and that is a fundamental wave. A non linear optical element is not incorporated in a laser oscillator of the laser irradiation apparatus shown in FIG. 1 and the laser oscillator can emit laser light of a fundamental wave with a high output power. FIG. 5B is a cross sectional view of a process in which the amorphous semiconductor film 12 is irradiated with laser light. In FIG. 5B, laser light 16 is converged by optical systems 30a and 30b to form an irradiation region 13, and at the same time, a stage on which a substrate is fixed is moved in a direction shown by the arrow 15 to crystallize the whole substrate.

By the laser irradiation method shown in Embodiment Mode 1, even when laser light that is a fundamental wave with high intensity is emitted to generate multiphoton absorption, the laser light is absorbed by the amorphous semiconductor film 12, thereby forming a crystalline semiconductor film 14. By the laser irradiation method described in Embodiment Mode 1, laser irradiation that hardly generates a poorly crystalline region can be conducted. Therefore, a region that cannot be used as a channel forming region of a TFT can be reduced drastically; therefore, yield can be increased and cost reduction can be easily achieved.

When a crystalline semiconductor film that is formed without being subjected to crystallization separately is used instead of the amorphous semiconductor film 12, a crystal having a grain diameter larger than a crystal after film formation can be obtained by irradiation of laser light with a fundamental wave.

In any case, when laser irradiation is conducted, a thin oxide film is formed on a surface of the crystalline semiconductor film 14. The thin oxide film on the surface is preferably removed because the thickness or the evenness thereof is uncertain. A watermark is easily generated due to drying on a water repellent surface. After removing the oxide film, it is preferable to prevent watermark by forming an oxide film with a water solution containing ozone. In addition, in order to reduce the number of processes, an oxide film formed on a surface by laser irradiation is not necessarily removed.

Then, selective etching is conducted by a photolithography technique to obtain a semiconductor layer 17 (FIG. 5C). Before forming a resist mask, an oxide film is

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formed with a water solution containing ozone or ozone generated by UV irradiation in an oxygen atmosphere so as to protect the semiconductor layer. The oxide film here also has an effect of improving wettability of resist.

If necessary, before selective etching using resist is conducted, doping of a slight amount of an impurity element (such as boron or phosphorus) is conducted through the oxide film to control a threshold voltage of a TFT. In the case of doping through the oxide film, the oxide film is removed and another oxide film is formed with a water solution containing ozone.

Then, after cleaning for removing unnecessary materials (such as residue of resist or resist peeling solution) made in the selective etching using resist is conducted, an insulating film containing silicon oxide as a main component is formed to cover the surface of the semiconductor layer 17 as a gate insulating film 18 (FIG. 5D).

Thereafter, a gate electrode 19 is formed after washing the surface of the gate insulating film 18. A material including a high melting point metal in which few hillocks are generated is preferably used as a material of the gate electrode 19. One kind selected from W, Mo, Ti, Ta, Co, and the like or an alloy thereof is used as the high melting point metal in which fewer hillocks are generated. Two or more layers of nitrides of the high melting point metal (such as WN, MoN, TiN, and TaN) may be stacked.

Then, the semiconductor film is doped appropriately with an impurity element (for example, P or As) that gives n-type conductivity to a semiconductor, phosphorus here, to form a source region 20 and a drain region 21. After the doping, a heat treatment, intense light irradiation, or laser irradiation is performed in order to activate the impurity element. In addition, as well as activation, plasma damage to the gate insulating film and plasma damage to the interface between the gate insulating film and the semiconductor layer can be recovered.

The laser irradiation apparatus shown in FIG. 1 may be used to conduct laser irradiation by the laser irradiation method described in Embodiment Mode 1 so as to activate the impurity element. When the laser irradiation apparatus shown in FIG. 1 is used, activation of the impurity element that is added to the semiconductor film can be

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conducted uniformly.

By subsequent steps of forming an interlayer insulating film 23, performing hydrogenation, forming contact holes reaching the source region 20 and the drain region 21, forming a conductive film, and forming a source electrode 24 and a drain electrode 25 by selectively etching the conductive film with a resist, a TFT (n-channel TFT) is completed (FIG. 5E). The source electrode 24 and the drain electrode 25 are formed by using a single layer including an element selected from the group consisting of Mo, Ta, W, Ti, Al, and Cu, or an alloy material or a compound material containing the element as its main component, or by using a stacked layer of these. For example, a three layer structure of a Ti film, a pure-Al film, and a Ti film, or a three layer structure of a Ti film, an Al alloy film containing Ni and C, and a Ti film is used. Further, in consideration of forming an interlayer insulating film and the like in subsequent steps, it is preferable that the cross section of the electrode has a tapered shape.

Here, a top gate TFT is described as an example; however, the present invention can be applied regardless of a TFT structure. For example, the present invention can be applied to a bottom gate (inversely staggered type) TFT or a staggered type TFT.

Further, the present invention is not limited to the TFT structure in FIG. 5E. If necessary, a lightly doped drain (LDD) structure that has an LDD region between a channel forming region and a drain region (or a source region) may be employed. In this structure, a region doped with an impurity element at a lower concentration is provided between a channel forming region and a source region or a drain region formed by doping with an impurity element at a higher concentration, and this region is referred to as an LDD region. Further, a so-called GOLD (Gate-drain Overlapped LDD) structure, in which an LDD region is overlapped with a gate electrode with a gate insulating film interposed therebetween, may be employed.

In addition, a TFT having a GOLD structure is described as an example with reference to FIGS. 6A and 6B. A part of a gate electrode structure or the like in the TFT having a GOLD structure shown in FIG. 6A is different from that in FIG. 5E, and thus, the same reference numerals are used for the same portions as those in FIG. 5E.

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The TFT having a GOLD structure shown in FIG. 6A includes a first LDD region 26 formed between a channel forming region 22 and a source region 20, and a second LDD region 27 formed between the channel forming region 22 and a drain region 21. The first and second LDD regions 26 and 27 are arranged to be overlapped with a lower layer 29b of the gate electrode with a gate insulating film 18 therebetween. The gate electrode is formed to have an upper layer 29a and the lower layer 29b that has a width wider than that of the upper layer 29a. In the TFT having a GOLD structure shown in FIG. 6A, a protective film 28 formed with a silicon nitride film is formed. As the protective film 28, a dense inorganic insulating film (such as a SiN film or a SiNO film) formed by PCVD, a dense inorganic insulating film (such as a SiN film or a SiNO film) formed by sputtering, a thin film mainly containing carbon (such as a DLC film, a CN film or an amorphous carbon film), a metal oxide film (such as WO_2, CaF_2, Al_2O_3 or AlN_xO_y), and the like are preferably used.

The TFT having a GOLD structure shown in FIG. 6B includes a first LDD region 36 formed between a channel forming region 32 and a source region 31a, and a second LDD region 37 formed between the channel forming region 32 and a drain region 31b. The first and second LDD regions 36 and 37 are partially overlapped with the gate electrode in FIG. 6B, while the first and second LDD regions are fully overlapped with the gate electrode in FIG. 6A. In the TFT shown in FIG. 6B, the gate insulating layer has a two-layer structure in which a first gate insulating film 38a made with a silicon oxide film and a second gate insulating layer 38b made with a silicon nitride film are stacked. The gate insulating film can be made thinner by using the second gate insulating film 38b made of a silicon nitride film.

In addition, in the TFT shown in FIG. 6B, a first interlayer insulating film 33a is formed with a silicon nitride film, and the second gate insulating film 38b and the first interlayer insulating film 33a of silicon nitride are provided to surround a single layer of the gate electrode 39. When the gate electrode 39 is formed with a conductive material such as Mo, which is easily oxidized, it is effective to surround the gate electrode with a silicon nitride film so as not to be in contact with the oxide film. By adopting a silicon nitride film for the first interlayer insulating film 33a, it can function

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as a protective film and can enhance adhesiveness with the second gate insulating film 38b made of the same material.

In the TFT shown in FIG. 6B, the second interlayer insulating film 33b is formed with a silicon oxide film and a source electrode 24 and a drain electrode 25 are formed over the second interlayer insulating film 33b. In addition, the TFT in FIG. 6B has a partially different structure from that in FIG. 5E, and thus, the same reference numerals are used for the same portions as those in FIG. 5E.

An n-channel TFT is shown in FIGS. 5A to 5E and FIGS. 6A and 6B. However, it is natural that a p-channel TFT can be formed using a p-type impurity element instead of an n-type impurity element.

The present invention is not limited to a single gate TFT, and may be applied to a multigate TFT having plural channel forming regions, for example, a double gate TFT, so as to reduce variations in OFF current value of a TFT.

An n-channel TFT and a p-channel TFT can be formed over the same substrate, and a CMOS circuit can be formed by combining an n-channel TFT and a p-channel TFT. The CMOS circuit is a circuit including at least one n-channel TFT and at least one p-channel TFT, for example, an inverter circuit, a NAND circuit, an AND circuit, a NOR circuit, an OR circuit, a shift register circuit, a sampling circuit, a D/A converter circuit, an A/D converter circuit, a latch circuit, a buffer circuit and the like. In addition, a memory element such as SRAM or DRAM and other elements can be provided over the substrate by combining such CMOS circuits. Further, a CPU can be formed over a substrate by integrating various elements or circuits.

This embodiment mode can be freely combined with Embodiment Mode 1.

Embodiment Mode 3

A dual gate TFT to which the present invention is applied is described below as an example with reference to FIG. 7.

In a TFT shown in FIG. 7, a base insulating film 711 is formed over a substrate 710 having an insulating surface and a lower electrode 712 is formed over the base insulating film 711.

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The lower electrode 712 can be formed with a metal or a polycrystal semiconductor doped with one conductivity type impurity element. If a metal is used, tungsten (W), molybdenum (Mo), titanium (Ti), tantalum (Ta), aluminum (Al) and the like can be used. Here, tungsten is used for the lower electrode 712 and the tungsten layer is formed with a thickness of 50 nm. It should be noted that the thickness of the lower electrode 712 may be 20 to 50 nm.

After that, the lower electrode 712 is formed by etching the tungsten layer with the use of a mask (for example, a resist mask). For example, at this time, the resist mask can be narrowed by applying oxygen plasma. When the etching is conducted after such a process, the side of the lower electrode 712 to become the gate electrode can be tapered.

The lower electrode 712 can be directly formed by a printing method or a droplet-discharge method typified by an ink-jet method, which can each discharge a material to the predetermined location. With this method, the lower electrode 712 can be formed without using the mask.

In addition, the lower electrode 712 is covered with a first insulating film 713 and a second insulating film 714 that are to be a first gate insulating film. The first insulating film 713 contains at least oxygen or nitrogen. In this embodiment mode, a silicon nitride oxide film (SiN_xO_y) (x>y) is formed with a thickness of 50 nm as the first insulating film 713 and a silicon oxynitride film (SiO_xN_y) (x>y) is formed with a thickness of 100 nm as the second insulating film 714. However, the present invention is not limited to these.

A semiconductor layer overlapped with the lower electrode 712 is formed over the second insulating film 714 with the first insulating film therebetween. The semiconductor layer is obtained by forming a semiconductor film by a method such as a low pressure thermal CVD method, a plasma CVD method or a sputtering method, and then crystallizing it by the laser irradiation method shown in Embodiment Mode 1. After that, etching is selectively conducted using a mask. The laser irradiation method using multiphoton absorption effect described in Embodiment Mode 1 can realize laser irradiation that hardly generates a poorly crystalline region. Therefore, a region that

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cannot be used as a channel forming region of a TFT is reduced drastically; therefore, yield can be increased and cost reduction can be easily achieved.

The semiconductor layer is covered with a second gate insulating film 718 that is an insulating film containing at least oxygen or nitrogen. The second gate insulating film 718 is formed without conducting laser irradiation for crystallization and the semiconductor layer is pressed physically with the second gate insulating film 718 and laser irradiation may be conducted using the laser irradiation apparatus shown in FIG. 1. In that case, peeling of the semiconductor film due to laser irradiation can be prevented by the second gate insulating film 718.

A lower layer 720b of an upper electrode and an upper layer 720a of the upper electrode are formed over the second gate insulating film 718. The lower layer 720b of the upper electrode has a width wider than that of the upper layer 720a of the upper electrode. The lower layer 720b and upper layer 720a of the upper electrode may both be formed with a conductive material.

In addition, the semiconductor layer includes at least a source region 716 doped with an impurity element at a high concentration, a channel forming region 715, and a drain region 717 doped with an impurity element at a high concentration. Here, in a state that the upper layer 720a and the lower layer 720b of the upper electrode are provided, an impurity element is added through the lower layer 720b of the upper electrode. Thus, a first low concentration impurity region (a first LDD region) 719a that is overlapped with the lower layer 720b of the upper electrode is formed between the source region 716 and the channel forming region 715. In addition, a second low concentration impurity region (a second LDD region) 719b that is overlapped with the lower layer 720b of the upper electrode is formed between the drain region 717 and the channel forming region 715.

An insulating film 721 covering the lower layer 720b and the upper layer 720a of the upper electrode is formed and an insulating film 722 for enhancing planarity is formed over the insulating film 721. As the insulating film 722 for enhancing planarity, an organic material or an inorganic material can be used. As the organic material, resist, polyimide, acryl, polyamide, polyimide amide, benzocyclobutene,

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siloxane, or polysilazane can be used. Siloxane is an insulating material, for example, an inorganic siloxane insulating material which has a Si-O-Si bond among compounds formed from silicon, oxygen and hydrogen, or an organic siloxane insulating material in which hydrogen bonded with silicon is substituted by an organic group such as methyl or phenyl. In addition, polysilazane is a substance formed from a liquid material containing a polymer material having a bond of silicon (Si) and nitrogen (N) i.e., polysilazane. As an inorganic material, an insulating film having at least oxygen or nitrogen, such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y, x> y), or silicon nitride oxide (SiN_xO_y, x> y) can be used. In addition, as the insulating film 722 for enhancing planarity, a stacked layer of these insulating films may be used. Specifically, when the insulating film for enhancing planarity is formed with an organic material, water or oxygen is absorbed by the organic material, although the planarity is increased. In order to prevent this, an insulating film including an inorganic material may be formed over the organic material. When an insulating film including nitrogen is used as the inorganic material, intrusion of alkali ions such as Na can be prevented.

Over the insulating film 722 for enhancing planarity, a source wiring 723 is formed through a contact hole that reaches the source region 716. Similarly, over the insulating film 722 for enhancing planarity, a drain wiring 724 is formed through a contact hole that reaches the drain region 717.

A TFT having a structure shown in FIG. 7 is a dual gate TFT in which channels are formed in upper and lower parts of one semiconductor layer. The lower electrode 712 of the dual gate TFT has a characteristic of controlling a TFT in a different way from the upper electrode. The lower electrode 712 can suppress variation of a threshold value and reduce an OFF current. In addition, in the dual gate TFT, a capacitor can be formed with the lower electrode and the semiconductor layer with an insulating film therebetween.

This embodiment mode can be freely combined with Embodiment Mode 1 or Embodiment Mode 2.

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Embodiment Mode 4

The present invention can be applied to a manufacturing method of a liquid crystal display device or a light-emitting display device. Here, a display device in which a pixel portion, a driver circuit and a terminal portion are formed on the same substrate is shown as one example. By the present invention, a semiconductor thin film that can respond to high speed driving can be obtained and a driver circuit can be formed using a higher-performance TFT. FIG. 8 shows an example of a light emitting device having an organic light emitting element as a display device.

After a base insulating film is formed over a substrate 610, each semiconductor layer is formed. Crystallization of the semiconductor layer is conducted following Embodiment Mode 1 or Embodiment Mode 2. By conducting crystallization in accordance with Embodiment Mode 1, laser irradiation that hardly generates a poorly crystalline region can be conducted and a semiconductor layer of a TFT that constitutes a part of a driver circuit can be formed with a semiconductor film having large grain crystals can be formed. Therefore, a driver circuit that can operate at high speed can be realized.

Then, after a gate insulating film covering the semiconductor layer is formed, a gate electrode and a terminal electrode are each formed. Subsequently, a source region and a drain region, and an LDD region if necessary, are appropriately formed by doping the semiconductor with an impurity element which imparts n-type conductivity (typically, phosphorus or arsenic) to form an n-channel TFT 636 and by doping the semiconductor with an impurity element which imparts p-type conductivity (typically, boron) to form a p-channel TFT 637. Subsequently, the impurity element added to the semiconductor layer is activated and hydrogenated after forming a silicon nitride oxide film (SiNO film) which contains hydrogen and which is obtained by PCVD.

Subsequently, a planarizing insulating film 616 which serves as an interlayer insulating film is formed. As the planarizing insulating film 616, an insulating film in which a skeletal including a bond of silicon (Si) and oxygen (O) obtained by a coating method is used.

Next, the planarizing insulating film in a peripheral portion is removed at the

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same time as forming a contact hole in the planarizing insulating film using a mask.

Next, etching is conducted using the planarizing insulating film 616 as a mask to remove selectively an exposed part of the SiNO film containing hydrogen or the gate insulating film.

After forming a conductive film, etching is conducted using the mask, thereby forming a drain wiring and a source wiring.

Next, a first electrode 623, that is, an anode (or a cathode) of the organic light-emitting element is formed. The first electrode 623 is preferably formed of a conductive film having a high work function, for example, a film including a transparent conductive material such as ITO containing Si (ITSO) and indium zinc oxide (IZO) which is the mixture of indium oxide and zinc oxide (ZnO) of 2 to 20 %, in addition to indium tin oxide (ITO), or a compound film which combines such materials, in addition to indium tin oxide (ITO). Above all, ITSO remains in an amorphous state without being crystallized even when subjected to baking, unlike ITO which would be crystallized. Thus, ITSO is superior in planarity to ITO, and does not easily cause a short circuit with the cathode even when the organic compound-containing layer is thin, which is thus suitable for the anode of the light-emitting element.

Next, an SOG film (for example, a SiO_x film containing an alkyl group) obtained by a coating method is selectively etched, thereby forming an insulator 629 (referred to as a bank, a partition wall, a barrier, an embankment, or the like) covering an end portion of the first electrode 623. The insulator 629 is formed using a material including silicon, an organic material and compound material. In addition, a porous film may be used. When the insulator is formed using a photosensitive or a non photosensitive material such as acrylic or polyimide, the side thereof has a shape in which the curvature radius is changed continuously, and a thin film in the upper layer can be formed without disconnection, which is preferable. As the material of the insulator 629, a photosensitive or a non photosensitive organic material dispersed with black pigment or carbon black may be used, and it may function as a black matrix (BM).

An organic compound-containing layer 624 is formed by an evaporation

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method, a thermal transfer printing method, a droplet-discharge method or a screen printing method. The organic compound-containing layer 624 has a multilayer structure, for example, a structure in which an electron transporting layer (an electron injecting layer), a light emitting layer, a hole transporting layer, and a hole injecting layer are sequentially stacked.

Here, molybdenum oxide (MoO_x), 4,4'-bis[N- (1-naphthyl)-N-phenyl-amino]-biphenyl (α-NPD) and rubrene are co-evaporated by an evaporation method to form a first organic compound containing layer (first layer) over the first electrode 623. Then, α-NPD is selectively deposited with an evaporation mask to form a hole transporting layer (second layer) over the first organic compound containing layer. In addition, instead of molybdenum oxide (MoO_x), one or plural kinds selected from MoN_x, VO_x, RuO_x, CoO_x, CuO_x, ZnN_x, WN_x, InO_x, InN_x, SnO_x, SnN_x, SbO_x, and SbN_x can be used.

A light-emitting layer (third layer) is selectively formed. The light-emitting layer is formed with a charge injecting-transporting material including an organic compound or inorganic compound and a luminescent material. The light-emitting layer includes one layer or more layers selected from layers including a low molecular weight organic compound, an intermediate molecular weight organic compound (referring to an organic compound which has no sublimation property and has 20 molecules or less or a chained molecule of 10 μm or less in length), or a high molecular weight organic compound which are classified based on the number of molecules, and may be combined with an electron injecting-transporting or hole injecting-transporting inorganic compound. Further, for the light-emitting layer, a triplet-excitation luminescent material such as metal complexes may be used in addition to a singlet-excitation luminescent material. For example, among a red light-emitting pixel, a green light-emitting pixel, and a blue light-emitting pixel, the red light-emitting pixel, of which luminance is decreased by half in a relatively short time, is formed with the use of a triplet-excitation luminescent material while the others are formed with the use of singlet-excitation luminescent materials. Since triplet-excitation luminescent materials are excellent in luminous efficiency, it is a feature that less power is consumed to obtain the same luminance. In other words, when a triplet-excitation luminescent

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material is applied to the red pixel, the amount of the current flowing in a light-emitting element is small so that the reliability can be improved. In order to lower power consumption, the red light-emitting pixel and the green light-emitting pixel may be formed with the use of triplet-excitation luminescent materials while the blue light-emitting pixel may be formed with the use of a singlet-excitation luminescent material. Also, as to a green light-emitting element for green emission that people can see at high visibility acuity, the power consumption can be lowered by forming the green light-emitting element with the use of a triplet-excitation luminescent material.

As an example of the triplet excitation luminescent material, there is a material using a metal complex as a dopant, and for example, a metal complex having platinum that is a third transition series element as a central metal and a metal complex having iridium as a central metal, and the like are known. The triplet-excitation luminescent material is not limited to these compounds, and a compound that has the structure described above and that has an element belonging to Groups 8 to 10 of the periodic table as a central metal can also be used.

In order to obtain a full color display device, evaporation masks for each emission color (R, G, B) are aligned to deposit light-emitting layers of each color. Typically, a light-emitting layer corresponding to each emission color R (red), G (green) and B (blue) is formed in each pixel.

Tris(8-quinolinato) aluminum (Alq_3) is selectively deposited with a use of an evaporation mask to form an electron transporting layer (fourth layer) over the light-emitting layer. Then, 4,4-bis (5-methylbenzoxazol-2-yl)stilbene (BzOs) and Li are co-evaporated to form an electron injecting layer (fifth layer) over the whole surface to cover the electron transporting layer and the insulator. Materials of the first to fifth layers in the organic compound containing layer 624 are each appropriately selected and the thicknesses thereof are adjusted.

The aforementioned substances for forming the organic compound containing layer 624 are only examples, and a light-emitting element can be formed by appropriately stacking each functional layer such as a hole injecting-transporting layer, a hole-transporting layer, an electron injecting-transporting layer, an

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electron-transporting layer, a light-emitting layer, an electron-blocking layer, and a hole-blocking layer. In addition, a mixed-layer or mixed-junction structure combining such layers may be employed. The layer structure of the light-emitting layer can be changed. A modification is possible without departing the spirit of the present invention, such that no specific electron-injecting region or light-emitting region is provided but an electrode layer for this purpose is provided or a light-emitting material is dispersed.

A second electrode 625 formed with a transparent conductive film, that is, a cathode (or anode) of an organic light emitting element, is formed over the organic compound containing layer 624. Then, a transparent protective layer 626 is formed by an evaporation method or a sputtering method. The transparent protective layer 626 protects the second electrode 625. The transparent protective layer 626 is preferably formed of a dense inorganic insulating film (e.g., SiN film or SiNO film) obtained by PCVD, a dense inorganic insulating film (e.g., SiN film or SiNO film) obtained by sputtering, a thin film containing carbon as a main component (e.g., DLC film, CN film or amorphous carbon film), a metal oxide film (e.g., WO_2, CaF_2, Al_2O_3 or AlN_xO_y) or the like. Note that "transparent" means that the transmissivity of visible light is 80 to 100%.

A transparent sealing substrate 633 is attached by a sealing agent 628 to encapsulate a light-emitting element. In a light emitting display device, a circumference of a display portion is surrounded by the sealing agent and sealed with a pair of substrates. However, the interlayer insulating film of the TFT is provided over the entire surface of the substrate. Therefore, when a pattern of the sealing agent is drawn inside a circumference edge of the interlayer insulating film, there is a possibility that moisture or an impurity may enter from a part of the interlayer insulating film which is located outside the pattern of the sealing agent. Consequently, as for the circumference of the planarizing insulating film used as the interlayer insulating film of the TFT, the sealing agent covers the inside of the pattern of the sealing agent, preferably, the edge portion of the planarizing insulating film to overlap the pattern of the sealing agent. Note that a region surrounded by the sealing agent 628 is filled with

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a transparent filler 627. As the transparent filler 627, ultraviolet curable resin, a thermosetting resin, a silicone resin, an epoxy resin, an acrylic resin, a polyimide resin, a phenol resin, PVC (polyvinyl chloride), PVB (polyvinyl butyral), EVA (ethylene vinyl acetate) or the like can be used.

Instead of filling the region surrounded by the sealing agent 628 with transparent filler, a dry inert gas may be used. At this time, a drying agent that absorbs moisture by chemical absorption, such as calcium oxide or barium oxide is arranged in a location such that does not hinder displaying.

Lastly, an FPC 632 is attached to the terminal electrode with an anisotropic conductive film 631 by a known method. The terminal electrode is preferably formed by stacking a transparent conductive film over a terminal electrode formed simultaneously with a gate wiring (FIG. 8).

According to the above steps, a pixel portion, a driver circuit, and a terminal portion can be formed over one substrate.

Light generated in the light-emitting element can be extracted to opposite sides, in other words, through the substrate 610 and the sealing substrate 633. The structure in FIG. 8 is a light-emitting device having a structure in which light is extracted through the substrate and the sealing substrate.

Thus, according to the present invention, a polarizing plate, a circularly polarizing plate, or a combination thereof can be provided depending on a structure of a light-emitting device in which light can be extracted through the substrate and the sealing substrate. Therefore, clear black display can be performed and a contrast is improved. Further, the circularly polarizing plate can prevent reflective light.

If a reflective metal material is used for the second electrode 625 instead of a transparent conductive film, a bottom emission type light-emitting element can be manufactured. On the contrary, a top emission type light-emitting device can be manufactured by using a transparent conductive film as the second electrode 625.

In addition, if necessary, other optical films (such as a retardation film, a color filter, or a color conversion filter) or a micro lens array, may be arranged as well as a polarizing plate or a circularly polarizing plate. For example, a color filter is provided

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on the side of a light-emitting element of the sealing substrate overlapping the display region, or an observer side so as to enhance color purity of each emission from the light-emitting elements of RGB provided in the display portion. In addition, a light-emitting element for white may be provided in the display portion and a color filter or a color filter and color conversion layer may be provided separately to display full color.

In the light emitting device, a method of driving screen display is not especially limited. For example, a dot sequential driving method, a line sequential driving method, a frame sequential driving method, and the like may be used. A line sequential driving method is typically used, and a time division gray scale driving method or a frame area gray scale driving method may also be appropriately employed. Further, video signals input to a source line of the light emitting device may be either analog signals or digital signals. A driver circuit and the like may be properly designed according to the video signals.

Further, light-emitting devices using digital video signals are classified into one in which video signals are inputted into a pixel at a constant voltage (CV), and one in which video signals are inputted into a pixel at a constant current (CC). The light-emitting devices in which video signals are inputted into a pixel at a constant voltage (CV) are further classified into one in which a constant voltage is applied to a light-emitting element (CVCV), and one in which a constant current is applied to a light-emitting element (CVCC). The light-emitting devices in which video signals are inputted into a pixel at a constant current (CC) is classified into one in which a constant voltage is applied to a light-emitting element (CCCV), and one in which a constant current is applied to a light-emitting element (CCCC).

In the light emitting device, a protection circuit (such as a protection diode) may be provided for the purpose of inhibiting electrostatic discharge damage.

An example of mounting an FPC or a driver IC for driving to a light-emitting display panel manufactured according to the above described method is described.

FIG. 9A is a top view of a light-emitting device in which FPCs 1209 are attached to four terminal portions 1208 as an example. A pixel portion 1202 including

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a light-emitting element and a TFT, a gate-side driver circuit 1203 including a TFT, and a source-side driver circuit 1201 including a TFT are formed over a substrate 1210. These circuits can be formed over one substrate when active layers of TFTs each are formed from a crystalline semiconductor film. Therefore, an EL display panel in which the system-on-panel is realized can be manufactured.

Note that the substrate 1210 is covered with a protective film except a contact portion, and a base layer containing a photocatalytic substance is provided over the protective film.

Two connecting regions 1207 provided so as to sandwich the pixel portion are provided for contacting a second electrode of the light-emitting element to a lower wiring. Note that a first electrode of the light-emitting element is electrically connected to a TFT provided in the pixel portion.

A sealing substrate 1204 is fixed to the substrate 1210 by a sealing agent 1205 surrounding the pixel portion and the driver circuits and by a filler surrounded by the sealing agent. In addition, a filler including a transparent drying agent may be used to fill a space. The drying agent may be disposed in a region which is not overlapped with the pixel portion.

The structure shown in FIG. 9A is a preferred example of a light-emitting device of a relatively large size of XGA class (for example, the opposite angle: 4.3 inches). FIG. 9B is an example of employing a COG mode which is suitable for a small size light-emitting device whose frame is narrowed (for example, the opposite angle: 1.5 inches).

In FIG. 9B, a driver IC 1301 is mounted on a substrate 1310 and an FPC 1309 is mounted on a terminal portion 1308 disposed at the end of the driver IC. A plurality of the driver ICs 1301 to be mounted are preferably formed over a rectangular substrate that is 300 to 1000 mm or more on one side, from a view point of improving the productivity. In other words, a plurality of circuit patterns having a driver circuit portion and an input-output terminal as a unit are preferably formed over a substrate and separated so that driver ICs can be obtained individually. As a semiconductor layer of TFTs used for the driver ICs, a semiconductor layer which is crystallized with the laser

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irradiation apparatus shown in FIG. 1 is used. Thus, a high-performance driver IC can be obtained. The driver IC may be formed to become a rectangular having a longer side of 15 to 80 mm and a shorter side of 1 to 6 mm in consideration of a length of one side of a pixel portion or a pixel pitch. In addition, the driver IC may be have a longer side corresponding to one side of a pixel portion or a length in which one side of a driving circuit is added to one side of the pixel portion.

The driver IC is superior to an IC chip in terms of an external size, since it has a longer side. When a driver IC formed to be 15 to 80 mm in a longer side is used, the number of driver ICs to be required for being mounted corresponding to the pixel portion is small, as compared with the case of using IC chips, thereby improving the yield in manufacturing. When a driver IC is formed over a glass substrate, the productivity is not lost because there is no limitation on the shape of a mother substrate. This is a great advantage, as compared with the case of forming IC chips using a circular silicon wafer.

In addition, a TAB mode may be employed, and in that case, a plurality of tapes are attached and a driver IC may be mounted on the tapes. As in the case of the COG mode, a single driver IC may be mounted on a single tape. In this case, a metal piece or the like for fixing a driver IC is preferably attached together for enhancing the intensity.

The substrate 1310 is covered with a protective film except a contact portion, and a base layer containing a photocatalytic substance is provided over the protective film.

A connecting region 1307 provided between a pixel portion 1302 and the driving IC 1301 is provided for contacting a second electrode of a light-emitting element to a lower wiring. Note that the first electrode of the light-emitting element is electrically connected to the TFT provided in the pixel portion.

A sealing substrate 1304 is fixed on the substrate 1310 by a sealing agent 1305 surrounding the pixel portion 1302 and by a filler surrounded with the sealing agent.

In the case of using an amorphous semiconductor film as an active layer of a TFT, it is difficult to form a driver circuit over the same substrate, and thus, the structure

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shown in FIG. 9B is employed even when it has a large size.

The active matrix light emitting display device is shown as an example of a display device here, and it is natural that the present invention can be applied to an active matrix liquid crystal display device. In the active matrix liquid crystal display device, pixel electrodes arranged in matrix are driven to display an image pattern on the screen. Specifically, a voltage is applied to a selected pixel electrode and an opposite electrode corresponding to the pixel electrode, and thus, a liquid crystal between the pixel electrode provided in the element substrate and the opposite electrode provided in the opposite substrate is modulated optically. The optical modulation can be recognized as an image pattern by an observer. The opposite substrate and the element substrate are arranged at an even interval and the space therebetween is filled with a liquid crystal. The substrates may be pasted to each other by dropping the liquid crystal material under reduced pressure so that a bubble does not enter by the sealing agent having a closed pattern. Alternatively, a dip method (pumping method) may be employed in which the liquid crystal is injected using capillary phenomenon after providing a seal pattern having an opening portion and pasting the TFT substrate.

The present invention can be applied to a liquid crystal display device which employs a structure in which an optical shutter is constituted by a polarizing plate and a liquid crystal panel without a color filter, and a driving method of a field sequential system of blinking a backlight light source for three colors of RGB at high speed.

This embodiment mode can be freely combined with Embodiment Mode 1, 2, or 3.

Embodiment Mode 5

Embodiment Mode 5 describes an example of manufacturing a CPU (Central Processing Unit) according to the present invention with reference to FIGS. 10A to 10C, FIGS. 11A to 11C, FIGS. 12A to 12C, FIGS. 13A to 13B, and FIG. 14.

As shown in FIG. 10A, a base insulating film 1401 is formed over a substrate 1400 having an insulating surface. As the substrate 1400, a glass substrate such as barium borosilicate glass or alumino borosilicate glass can be used. Further, a

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substrate made of synthetic resin having flexibility such as plastic or acrylic typified by PET, PES, or PEN tends to have lower heat resistance than another substrate. Such a substrate can be used, as long as the substrate can resist the treatment temperature in the manufacturing steps.

The base insulating film 1401 is provided to prevent an alkali metal or an alkali-earth metal such as Na included in the substrate 1400 from diffusing into a semiconductor film to adversely affect the characteristic of a semiconductor element. Therefore, the base insulating film 1401 is formed with an insulating film such as silicon oxide, silicon nitride, or silicon oxide containing nitrogen which can suppress the diffusion of an alkali metal or an alkali-earth metal into the semiconductor film.

An amorphous semiconductor film 1402 is formed over the base insulating film 1401. The thickness of the amorphous semiconductor film 1402 is set to 25 to 100 nm (preferably 30 to 60 nm). As the amorphous semiconductor, not only silicon but also silicon germanium can be used. In the case of using silicon germanium, the concentration of germanium is preferably approximately 0.01 to 4.5 atomic%. In this embodiment mode, a 66-nm-thick semiconductor film containing silicon as its main component (also referred to as an amorphous silicon film or amorphous silicon) is used.

After that, the amorphous semiconductor film 1402 is irradiated with a laser light (laser beam) 1405 which is fundamental wave (refer to FIG. 10 B) to produce multiphoton absorption as described in Embodiment Mode 1. Note that the pulse width of laser light is set to picosecond or femtosecond so as to produce multiphoton absorption. By this laser irradiation, the amorphous semiconductor film 1402 is crystallized, and a crystalline semiconductor film is formed (Here, poly silicon film).

As shown in FIG. 10C, the crystalline semiconductor film is selectively etched into a predetermined shape, thereby obtaining island-shaped semiconductor layers 1406a to 1406e.

After that, a small amount of an impurity element (for example, boron) is added into the crystalline semiconductor film as necessary to make a threshold value, which is the electric characteristic of the thin film transistor, closer to zero.

After that, an insulating film to cover the island-shaped semiconductor layers

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1406a to 1406e, which is a so-called gate insulating film 1408, is formed. Before forming the gate insulating film 1408, the surface of the island-shaped semiconductor film is washed with hydrofluoric acid or the like. The gate insulating film 1408 is formed with an insulating film containing silicon with a thickness of 10 to 150 nm, preferably 20 to 40 nm, by a plasma CVD method or a sputtering method. Of course, the gate insulating film is not limited to the silicon oxide film, and another insulating film containing silicon (such as silicon nitride film or silicon oxynitride film) may be formed as a single layer or multilayer structure.

After that, conductive films 1409a and 1409b to serve as a gate electrode are formed over the gate insulating film 1408. Here, the gate electrode is a two layer structure. It is natural that the gate electrode may have a single layer structure or a multilayer structure including three layers or more. The conductive films 1409a and 1409b may be formed with an element selected from Ta, W, Ti, Mo, Al, and Cu, or an alloy material or a compound material containing the above element as its main component.

As shown in FIG. 11A, a resist mask 1410 is formed to etch the first conductive film 1409a and the second conductive film 1409b. Note that an end portion of the resist mask 1410 may have a tapered shape, and the shape of the resist mask may be sector or trapezoidal.

Next, the second conductive film 1409b is selectively etched using the resist mask 1410 as shown in FIG. 11B. Note that the first conductive film 1409a serves as an etching stopper so that the gate insulating film and the semiconductor film are not etched. The etched second conductive film 1409b has a gate length 1413 which ranges from 0.2 to 1.0 μm.

As shown in FIG. 11C, the first conductive film 1409a is etched with the resist mask 1410 provided. At this time, the first conductive film 1409a is etched under a condition where the selective ratio between the gate insulating film 1408 and the first conductive film 1409a is high. With this step, the resist mask 1410 and the second conductive film 1409b may be somewhat etched and be narrower. In this way, the gate electrode, which is extremely small, having a gate length of 1.0 μm or less is formed.

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After that, the resist mask 1410 is removed by O_2 ashing or resist stripping solution, and a resist mask 1415 for adding an impurity element is appropriately formed. In this manner, the resist mask 1415 is formed to cover a region to become a p-channel TFT.

Next, phosphorus (P), which is an impurity element, is added in a self-alignment manner into a region to become an n-channel TFT by using the gate electrode as a mask as shown in FIG. 12A. Here, doping of phosphine (PH_3) is conducted at 60 to 80 keV. Then, impurity regions 1416a to 1416c are formed in the region to become an n-channel TFT.

Next, the resist mask 1415 is removed and then, a resist mask 1417 is formed to cover the region to become an n-channel TFT. After that, boron B, which is an impurity element, is added in a self-alignment manner using the gate electrode as a mask as shown in FIG.12 B. With this step, impurity regions 1418a and 1418b are formed in the region to become a p-channel TFT.

After removing the resist mask 1417, an insulating film covering the side of the gate electrode, so-called sidewalls 1419a to 1419c, is formed as shown in FIG. 12C. The sidewalls can be formed by etching appropriately after an insulating film containing silicon is formed by a plasma CVD method or a low-pressure CVD (LPCVD) method.

Next, a resist mask 1421 is formed over the p-channel TFT. Here, phosphine (PH_3) is added at 15 to 25 keV to form high-concentration impurity regions, so-called source and drain regions, are formed. With this step, high-concentration impurity regions 1420a to 1420c are formed in a self-alignment manner using the sidewalls 1419a to 1419c as masks as shown in FIG. 12C.

After that, the resist mask 1421 is removed by O_2 ashing or resist stripping solution.

Next, a heat treatment to activate each impurity region is conducted. Here, the impurity regions are activated by the laser irradiation method shown in Embodiment Mode 1. Note that the impurity regions may be activated by heating the substrate at a temperature of 550°C in a nitrogen atmosphere.

Next, a first interlayer insulating film 1422 covering the gate insulating film

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1408 and the gate electrode is formed. For the first interlayer insulating film 1422, an inorganic insulating film containing hydrogen such as a silicon nitride film is used.

After that, a heat treatment is conducted for hydrogenation. Dangling bonds in the silicon oxide film or the silicon film are terminated with hydrogen released from silicon nitride film, which is the first interlayer insulating film 1422.

Then, a second interlayer insulating film 1423 is formed so as to cover the first interlayer insulating film 1422 as shown in FIG. 13 A. The second interlayer insulating film 1423 can be formed with an inorganic material (such as silicon oxide, silicon nitride, or silicon nitride containing oxygen), a photosensitive or non-photosensitive organic material (polyimide, acrylic, polyamide, polyimide amide, resist, or benzocyclobutene), a material which includes a skeleton having a bond of silicon (Si) and oxygen (O) and includes at least hydrogen in a substituent or includes at least one of fluorine, alkyl group, and aromatic carbon hydrogen in a substituent , that is to say siloxane, and a multilayer structure of these.

Next, an opening portion, a so-called contact hole is formed in the gate insulating film 1408, the first interlayer insulating film 1422, and the second interlayer insulating film 1423. Wirings 1425a to 1425e connected to each impurity region are formed as shown in FIG. 13B. Simultaneously, a wiring connected to the gate electrode is formed, if necessary. Note that those wirings are formed with a film formed with an element selected from aluminum (Al), titanium (Ti), molybdenum (Mo), tungsten (W), and silicon (Si), or an alloy film using these elements may be used. Further, those wirings may be formed with an aluminum alloy film containing carbon and at least one element selected from nickel, cobalt and iron.

In this way, an n-channel thin film transistor having a gate length of 1.0 μm or less and an LDD structure formed so as to have a low-concentration impurity region can be formed. Moreover, a p-channel thin film transistor having a gate length of 1.0 μm or less and a single-drain structure formed so as not to have a low-concentration impurity region is completed. A TFT having a gate length of 1.0 μm or less can be referred to also as a submicron TFT. Since the deterioration due to the hot carrier and the short-channel effect are difficult to occur in the p-channel thin film transistor, the

single-drain structure can be employed.

In the present invention, the p-channel thin film transistor may have the LDD structure. Further, both of the n-channel thin film transistor and the p-channel thin film transistor may have, instead of the LDD structure, a GOLD structure in which the low-concentration impurity region is overlapped with the gate electrode.

A semiconductor device having the thusly formed thin film transistor, which is a CPU in this embodiment mode, can be manufactured and high-speed operation at a drive voltage of 5 V and an operating frequency of 30 MHz becomes possible.

Next, an example of constituting various circuits with the above-mentioned thin film transistors is described with reference to FIG. 14. FIG. 14 shows a block diagram of a CPU formed over a glass substrate 1600.

The CPU shown in FIG. 14 mainly includes an arithmetic logic unit (ALU) 1601, an arithmetic logic unit controller (ALU controller) 1602, an instruction decoder 1603, an interrupt controller 1604, a timing controller 1605, a register 1606, a register controller 1607, a bus interface (Bus I/F) 1608, a rewritable ROM 1609, and a ROM interface (ROM I/F) 1620 over the glass substrate 1600. The ROM 1609 and the ROM I/F 1620 may be provided in another chip.

Of course, the CPU shown in FIG. 14 is just an example in which the structure is simplified, and actual CPUs have various structures according to their intended purposes.

An instruction inputted into the CPU through the bus interface 1608 is inputted into the instruction decoder 1603 and decoded, and then inputted into the arithmetic logic unit controller 1602, the interrupt controller 1604, the register controller 1607, and the timing controller 1605.

The arithmetic logic unit controller 1602, the interrupt controller 1604, the register controller 1607, and the timing controller 1605 conduct various controls based on the decoded instructions. Specifically, the arithmetic logic unit controller 1602 generates signals for controlling the operation of the arithmetic logic unit 1601. Further, the interrupt controller 1604 processes an interrupt request from a peripheral circuit or an external input/output device during the execution of a program of the CPU

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by judging based on the priority or the mask condition. The register controller 1607 generates an address of the register 1606 and reads out or writes in the register 1606 in accordance with the state of the CPU.

The timing controller 1605 generates signals for controlling the timing of the operation of the arithmetic logic unit 1601, the arithmetic logic unit controller 1602, the instruction decoder 1603, the interrupt controller 1604, and the register controller 1607. For example, the timing controller 1605 includes an internal clock generator that generates an internal clock signal CLK2 (1622) based on a standard clock signal CLK1 (1621), and supplies the clock signal CLK2 to the above-described various circuits.

Since laser irradiation can be conducted to a large area by one time scanning of a laser beam according to the present invention, a CPU can be manufactured at low cost.

In addition, this embodiment mode can be freely combined with Embodiment Modes 1 to 4.

Embodiment Mode 6

Here, an example of manufacturing an IC tag according to the present invention is shown with reference to FIG. 15A to 15E, FIG. 16A to 16E, FIG. 17 A to 17C, FIG. 18 A and FIG. 18B.

Although this embodiment mode shows an example of an isolated and insulated TFT as a semiconductor element used for an integrated circuit of an IC tag, the semiconductor element used for an integrated circuit of an IC tag is not limited to the TFT, and any elements can be used. For example, besides the TFT, a storage element, a diode, a photoelectric conversion element, a resistance element, a coil, a capacitor element, an inductor, and the like are typically given.

First, as shown in FIG. 15A, a peeling layer 1501 is formed over a glass substrate (a first substrate) 1500 by a sputtering method. The peeling layer 1501 can be formed by a sputtering method, a low pressure CVD method, a plasma CVD method or the like. In this embodiment mode, amorphous silicon with a thickness of about 50 nm is formed by a low pressure CVD method, and used as the peeling layer 1501. The material for the peeling layer 1501 is not limited to silicon, other materials that can be

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removed selectively by etching (for example, W, Mo, or the like) can be used for forming the peeling layer 1501. The thickness of the peeling layer 1501 is preferably 50 to 60 nm.

Next, a base insulating film 1502 is formed over the peeling layer 1501. The base insulating film 1502 is formed to prevent an alkali-earth metal or an alkali metal such as Na contained in the first substrate from diffusing into the semiconductor film to adversely affect the characteristic of a semiconductor element such as a TFT. The base insulating film 1502 also has a function of protecting the semiconductor element in a later step of peeling the semiconductor element. The base insulating film 1502 may be a single layer or may have plural insulating films which have been stacked. Therefore, an insulating film, such as silicon oxide, silicon nitride, silicon oxide containing nitrogen (SiON), or silicon nitride containing oxygen (SiNO), which can prevent the diffusion of an alkali metal or an alkali-earth metal into a semiconductor film is used.

Next, a semiconductor film is formed over the base insulating film 1502. A semiconductor film 1503 is desirably formed without being exposed to the air after forming the base insulating film 1502. The thickness of the semiconductor film is set to 20 to 200 nm (desirably 40 to 170 nm, preferably 50 to 150 nm).

In addition, the semiconductor film 1503 is irradiated with a laser light, which is a fundamental wave, so that multiphoton absorption is produced for crystallization, in accordance with Embodiment Mode 1. Thus, crystallization is completed. A crystalline semiconductor film 1504 is formed by irradiating the semiconductor film 1503 with laser light. Note that FIG. 15A is a cross sectional view showing a state in which laser light is scanned.

Then, a gate insulating film 1509 is formed after island-shaped semiconductor films 1506 to 1508 are formed by etching selectively the semiconductor film 1504 having a crystalline structure as shown in FIG. 15 B. The gate insulating film 1509 can be formed with a single layer or a multilayer of a film containing silicon nitride, silicon oxide, silicon oxide containing nitrogen, or silicon nitride containing oxygen by a plasma CVD method, a sputtering method, or the like.

After forming the gate insulating film 1509, a heat treatment may be performed

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in an atmosphere including hydrogen for 3 % or more at a temperature of 300 to 450°C for 1 to 12 hours (this treatment is also referred to as hydrogenation) in order to hydrogenate the island-shaped semiconductor films 1506 to 1508. As another means for the hydrogenation, plasma hydrogenation (using hydrogen excited by plasma) may be performed.

Next, as shown in FIG. 15C, gate electrodes 1510 to 1512 are formed. Here, the gate electrodes 1510 to 1512 are formed by stacking Si and W by a sputtering method and then, etching them with the use of a resist 1513 as a mask. It is natural that the conductive materials, the structures, and the manufacturing method of these gate electrodes 1510 to 1512 are not limited to these, and they can be selected appropriately. For example, the gate electrodes may have a multilayer structure of NiSi (nickel silicide) and Si doped with an impurity imparting n-type conductivity or a multilayer structure of TaN (tantalum nitride) and W (tungsten). Moreover, the gate electrodes may be a single layer formed with various kinds of conductive materials. In addition, in the case where the gate electrode and an antenna are formed simultaneously, materials may be selected in consideration of the functions of those.

A mask of SiO_x or the like may be used instead of the resist mask. In this case, a step of forming a mask of SiO_x, SiON or the like (also, referred to as a hard mask) by selectively etching is added. However, since the decrease in a film thickness of the mask at the etching is less than the resist, the gate electrodes 1510 to 1512 having the desired widths can be formed. Alternatively, the gate electrodes 1510 to 1512 may be formed selectively by a droplet-discharge method without using the resist 1513.

Next, as shown in FIG. 15D, the island-shaped semiconductor film 1507 to become a p-channel TFT is covered with a resist 1515, and then the island-shaped semiconductor films 1506 and 1508 are doped at a low-concentration with an impurity element imparting n-type conductivity (typically, P (phosphorus) or As (arsenic)) by using the gate electrodes 1510 and 1512 as masks. In this doping step, the doping is performed through the gate insulating film 1509, and a pair of low-concentration impurity regions 1516 and 1517 is formed in the island-shaped semiconductor films 1506 and 1508. It is to be noted that the doping step may be performed without

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covering the island-shaped semiconductor film 1507 to become a p-channel TFT with a resist.

Next, as shown in FIG. 15E, after removing the resist 1515 by ashing or the like, a resist 1518 is formed anew so as to cover the island-shaped semiconductor films 1506 and 1508 to become n-channel TFTs. Then, the island-shaped semiconductor film 1507 is doped with an impurity element imparting p-type conductivity (typically B (boron)) at high-concentration by using the gate electrode 1511 as a mask. In the doping step, the doping is performed through the gate insulating film 1509, and a pair of p-type high-concentration impurity regions 1520 is formed in the island-shaped semiconductor film 1507.

Next, an insulating film 1521 is formed so as to cover the gate insulating film 1509 and the gate electrodes 1510 to 1512 after removing the resist 1518 by ashing or the like as shown in FIG. 16A.

Next, the insulating film 1521 and the gate insulating film 1509 are etched partially by an etch-back method to form sidewalls 1522 to 1524 which are in contact with the side of the gate electrodes 1510 to 1512 in a self-alignment manner as shown in FIG. 16 B. As an etching gas, a mixed gas of CHF_3 and He is used. Note that the step of forming a sidewall is not limited to this.

After that, a resist 1526 is formed anew to cover the island-shaped semiconductor film 1507 to become a p-channel TFT, and an impurity element imparting n-type conductivity (typically P or As) is added at high-concentration using the gate electrodes 1510 and 1512, and side walls 1522 and 1524 as masks as shown in FIG.16 C. By this doping step, island-shaped semiconductor films 1506 and 1508 are doped through the gate insulating film 1509, and a pair of n-type high-concentration impurity regions 1527 and 1528 is formed.

After removing the resist 1526 by ashing or the like, thermal activation of the impurity region may be performed. For example, after forming a SiON film having a thickness of 50 nm, a heat treatment may be performed for four hours under a nitrogen atmosphere at 550°C. When a SiN_x film containing hydrogen is formed with 100 nm thick and then, a heat treatment is performed thereto for one hour under a nitrogen

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atmosphere at 410°C, a defect in the polycrystal semiconductor film can be improved. This is for the purpose of terminating the dangling bonds existing in, for example, the polycrystal semiconductor film and is called a hydrogenation treatment or the like.

According to a series of the above-mentioned steps, an n-channel TFT 1530, a p-channel TFT 1531, and an n-channel TFT 1532 are formed. When the size of the sidewall is adjusted by changing the condition of an etch-back method appropriately in these manufacturing steps, a TFT having a channel length of 0.2 to 2 μm can be formed.

After that, a passivation film may be formed to protect the TFTs 1530 to 1532.

Next, a first interlayer insulating film 1533 is formed so as to cover the TFTs 1530 to 1532 as shown in FIG. 16 D.

Further, a second interlayer insulating film 1534 is formed over the first interlayer insulating film 1533. A filler may be mixed into the first interlayer insulating film 1533 or the second interlayer insulating film 1534 in order to prevent the first interlayer insulating film 1533 or the second interlayer insulating film 1534 from peeling and being damaged due to the stress caused by a difference in the coefficient of thermal expansion between a conductive material or the like for constituting a wiring to be formed afterward and the first interlayer insulating film 1533 or the second interlayer insulating film 1534.

Next, as shown in FIG. 16 (D), contact holes are formed in the first interlayer insulating film 1533, the second interlayer insulating film 1534, and the gate insulating film 1509, and wirings 1535 to 1539 to connect with the TFTs 1530 to 1532 are formed. Note that wiring 1535 and 1536 are connected to a high-concentration impurity region 1527 of a n-channel TFT 1530, wirings 1536 and 1537 are connected to a high-concentration impurity region 1520 of a p-channel TFT 1531, and wirings 1538 and 1539 are connected to a high-concentration impurity region 1528 of a n-channel TFT 1532. Moreover, the wiring 1539 is connected to a gate electrode 1512 of the n-channel TFT 1532. Note that the n-channel TFT 1532 can be used as a memory element of a random ROM.

Next, as shown in FIG. 16 E, a third interlayer insulating film 1541 is formed over the second interlayer insulating film 1534 so as to cover the wirings 1535 to 1539.

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The third interlayer insulating film 1541 is formed so as to have an opening portion at a location for partially exposing the wiring 1535. The third interlayer insulating film 1541 can be formed with the same material as the first interlayer insulating film 1533.

Next, an antenna 1542 is formed over the third interlayer insulating film 1541. The antenna 1542 can be formed with a conductive material having one or a plurality of metal such as Ag, Au, Cu, Pd, Cr, Mo, Ti, Ta, W, Al, Fe, Co, Zn, Sn, and Ni or metal compounds. The antenna 1542 is connected to the wiring 1535. Although the antenna 1542 is directly connected to the wiring 1535 in FIG. 16 E, the IC tag of the present invention is not limited to this structure. For example, the antenna 1542 may be electrically connected with the wiring 1535 by using a wiring separately formed.

The antenna 1542 can be formed by a printing method, a photolithography method, an evaporation method, a droplet-discharge method, or the like. In FIG. 16 E, the antenna 1542 is formed with a single layer of a conductive film. However, the antenna 1542 can be formed by stacking a plurality of conductive films. For example, the antenna 1542 may be formed with a wiring which has been made of Ni or the like and which is coated with Cu by electroless plating.

The droplet-discharge method is a method for forming a predetermined pattern by discharging a droplet including a predetermined composition from a small nozzle hole. An ink-jet method and the like are included in the category. On the other hand, the printing method includes a screen printing method, an offset printing method, and the like. When the printing method or the droplet-discharge method is employed, the antenna 1542 can be formed without using the mask for the light exposure. Moreover, when the printing method or the droplet-discharge method is employed, unlike the photolithography method, the material that will be etched away can be saved. Moreover, since the expensive mask for the light exposure is not necessary, the cost for manufacturing an IC tag can be reduced.

In the case of employing the droplet-discharge method or various kinds of printing methods, for example, a conductive particle of Cu coated with Ag can also be used. When the antenna 1542 is formed by a droplet-discharge method, it is desirable to perform a process for improving the adhesiveness of the antenna 1542 to a surface of

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the third interlayer insulating film 1541.

As methods for improving the adhesiveness, specifically, a method in which metal or a metal compound that can improve the adhesiveness of the conductive film or the insulating film due to the catalyst action is attached to the surface of the third interlayer insulting film 1541, a method in which an organic insulating film, a metal, or a metal compound having high adhesiveness to a conductive film or an insulating film to be formed is attached to the surface of the third interlayer insulating film 1541, a method in which a plasma process is performed to the surface of the third interlayer insulating film 1541 under atmospheric pressure or reduced pressure so that the surface thereof is modified, and the like are given.

When the metal or the metal compound attached to the third interlayer insulating film 1541 is conductive, the sheet resistance is controlled so that the normal operation of the antenna is not interrupted. Specifically, the average thickness of the conductive metal or metal compound may be controlled so as to range from 1 to 10 nm, for example. Moreover, the metal or the metal compound may be insulated partially or totally by oxidization. Alternatively, the attached metal or metal compound may be etched selectively except in the region where the adhesiveness needs to be improved. The metal or the metal compound may be attached selectively only to a particular region by a droplet-discharge method, a printing method, or a sol-gel method instead of attaching the metal or the metal compound to the whole surface of the substrate. The metal or the metal compound is not necessarily a totally continuous film on the surface of the third interlayer insulating film 1541 but may be dispersed to some extent.

Then, as shown in FIG. 17 A, after forming the antenna 1542, a protective layer 1545 is formed over the third interlayer insulating film 1541 so as to cover the antenna 1542. The protective layer 1545 is formed with a material capable of protecting the antenna 1542 when the peeling layer 1501 is etched afterward. For example, the protective layer 1545 can be formed by applying epoxy based resin, acrylate based resin, or silicon based resin which can dissolve in water or alcohols to the whole surface.

Next, as shown in FIG. 17B, a groove 1546 is formed in order to divide IC tags from each other. The groove 1546 may have such a depth that the peeling layer 1501

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is exposed. The groove 1546 can be formed by dicing or scribing. It is to be noted that the groove 1546 is not necessarily formed when it is not required to divide the IC tags formed over the first substrate 1500.

Next, as shown in FIG. 17C, the peeling layer 1501 is removed by etching. Here, halogen fluoride as an etching gas is introduced from the groove 1546. For example, ClF_3 (chlorine trifluoride) is used under a condition where the temperature is 350°C, the flow rate is 300 sccm, the air-pressure is 798 pascal (798Pa), and the time is 3 hours. Moreover, a gas in which nitrogen is mixed into ClF_3 gas may be used. The peeling layer 1501 can be selectively etched by using the halogen fluoride such as ClF_3, so that the TFTs 1530 to 1532 can be peeled from the first substrate 1500. The halogen fluoride may be either gas or liquid.

A method for peeling an integrated circuit including a TFT from an insulating substrate is not limited to the method of etching an amorphous silicon film as shown in this embodiment mode, and other various methods can be employed. For example, a metal oxide film is provided between a substrate having high heat resistance and an integrated circuit and then, the metal oxide film is weakened. Thereafter, peeling is conducted so that the integrated circuit including a TFT provided over the metal oxide film can be peeled. Moreover, at least a portion of the peeling layers is destroyed by laser irradiation so that an integrated circuit including a TFT can be peeled from a substrate. In addition, an integrated circuit including a TFT can be peeled from a substrate by eliminating mechanically a substrate in which an integrated circuit including a TFT is formed, or removing a substrate by etching with solution or gas.

Next, as shown in FIG. 18A, the peeled TFTs 1530 to 1532 and the antenna 1542 are pasted to a second substrate 1551 by using an adhesive agent 1550. As the adhesive agent 1550, a material which can paste the second substrate 1551 and the base insulating film 1502 is used. As the adhesive agent 1550, various kinds of curable adhesive agents can be employed: for example, a reactive-curable type adhesive agent, a thermosetting type adhesive agent, a photo-curable type adhesive agent such as a UV-curable type adhesive agent, or an anaerobic type adhesive agent.

The second substrate 1551 can be formed with a flexible organic material such

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as paper or plastic.

As shown in FIG. 18 B, after removing the protective layer 1545, an adhesive agent 1552 is applied onto the third interlayer insulating film 1541 so as to cover the antenna 1542, and then a cover material 1553 is pasted. As the cover material 1553, a flexible organic material such as paper or plastic can be used like the second substrate 1551. The thickness of the adhesive agent 1552 may be set, for example, in the range of 10 to 200 μm.

As the adhesive agent 1552, a material which can paste the cover material 1553 with the third interlayer insulating film 1541 and the antenna 1542, is used. As the adhesive agent 1552, various kinds of curable adhesive agents can be used: for example, a reactive-curable type adhesive agent, a thermosetting type adhesive agent, a photo-curable type adhesive agent such as a UV-curable type adhesive agent, or an anaerobic type adhesive agent.

Through the above-mentioned steps, an IC tag is completed. Through the above manufacturing method, an extremely thin integrated circuit having the total thickness in the range of 0.3 to 3 μm, typically about 2 μm, can be formed between the second substrate 1551 and the cover material 1553.

The thickness of the integrated circuit includes not only the thickness of the semiconductor element itself but also the thickness of various insulating films and interlayer insulating films formed between the adhesive agent 1550 and the adhesive agent 1552. The area in the IC tag which is occupied by an integrated circuit can be set to a 5-mm-square or less (25 mm^2 or less), more preferably in the range of approximately 0.3-mm-square (0.09 mm^2) to 4-mm-square (16 mm^2) on a side.

Although this embodiment mode has described a method of peeling the substrate from the integrated circuit by providing a peeling layer between the first substrate 1500 having high heat resistance and an integrated circuit, and etching the peeling layer, the method for manufacturing an IC tag of the present invention is not limited to this method. For example, a metal oxide film may be provided between the integrated circuit and the substrate having high heat resistance, and the metal oxide film may be weakened by crystallization so that the integrated circuit is peeled.

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Alternatively, the peeling layer formed with an amorphous semiconductor film containing hydrogen may be provided between the integrated circuit and the substrate having high heat resistance, and the peeling layer may be removed by laser irradiation so as to peel the substrate from the integrated circuit. Alternatively, the integrated circuit may be separated from the substrate by mechanically removing the substrate having high heat resistance over which the integrated circuit is formed or by etching the substrate using a solution or a gas.

Although this embodiment mode has described the example for forming the antenna over the same substrate as the integrated circuit, the present invention is not limited to this structure. The antenna and the integrated circuit each of which is formed over a different substrate may be pasted to each other afterward so that they are connected electrically.

The frequency of the electric wave usually used in RFIC is 13.56 MHz or 2.45 GHz, and it is extremely important to form the IC tag so that these frequencies of the electric wave can be detected in order to enhance the versatility.

The IC tag of this embodiment mode has advantages that the IC tag blocks almost no electric waves, as compared to the RFIC formed using a semiconductor substrate and that attenuation of signals due to blocking of electric waves can be prevented. Since the semiconductor substrate is not necessary, the cost for manufacturing the IC tag can be reduced drastically.

Although this embodiment mode has described the example in which the peeled integrated circuit is pasted to the flexible substrate, the present invention is not limited to this structure. For example, when a substrate having allowable temperature limit which can resist a heat treatment in the manufacturing steps of the integrated circuit, such as a glass substrate, is used, the integrated circuit is not necessarily peeled.

This embodiment can be freely combined with Embodiment Modes 1 to 5.

Embodiment Mode 7

A TFT manufactured using the laser irradiation apparatus of the present invention can be used for various electronic devices. As the electronic device, cameras

such as video cameras or digital cameras, goggle-type displays, navigation systems, sound reproduction devices (car audio compositions, audio compositions, and the like), personal computers, game machines, mobile information terminals (mobile computers, mobile phones, mobile game machines, electronic books, and the like), image reproduction devices equipped with a recording medium (specifically, devices which can reproduce a recording medium such as Digital Versatile Disk (DVD) and have a display for displaying the image), and the like are given.

Since the present invention can conduct a laser irradiation process favorably to a semiconductor film, it is possible to increase the freedom degree of layout or size of a semiconductor element and improve the integration degree. Moreover, it is possible to eliminate a variation since the quality of the manufactured semiconductor element is in preferable state. The specific example is showed with reference to FIGS. 19A to 19C.

FIG. 19 A shows a display device including a casing 1901, a support 1902, a display portion 1903, speaker portions 1904, a video input terminal 1905 and the like. The display device is manufactured using a thin film transistor formed by the manufacturing method shown in other embodiment modes to its display portion 1903 and its driving circuit. The display device indicates a liquid crystal display device, a light emitting device and the like, and it includes all display devices for information display, for example, ones for a computer, a TV receiving, and an advertising display.

FIG. 19 B shows a personal computer including a casing 1911, a display portion 1912, a keyboard 1913, an external connection port 1914, a pointing mouse1915, and the like. By using the manufacturing method shown in the above mentioned embodiment mode, it can be applied to the display portion 1912, other circuit portions, and the like. Further, the present invention can be applied to a CPU inside the main body, a semiconductor device such as a memory, and the like.

FIG. 19C shows a mobile phone, and a typical example of mobile information terminal. The mobile phone includes a casing 1921, a display portion1922, a sensor portion 1924, operation keys 1923, and the like. The sensor portion 1924 has an optical sensor element, and the amount of consumption current of the mobile phone can be suppressed by controlling the brightness of the display portion 1922 based on the

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illumination intensity obtained by the sensor portion 1924, conducting the lighting control of the operation keys 1923 corresponding to the illumination intensity obtained by the sensor portion 1924. In addition, in the case of a mobile phone having an imaging function such as a CCD or the like, whether a person who takes a picture looks in an optical finder or not is detected as the amount of light received by a sensor of the sensor portion 1924 provided in the vicinity of the optical finder changes. In the case where a person who takes a picture looks in the optical finder, the amount of electric power consumption can be suppressed by making off the display portion 1922.

The display screen of electronic devices such as the above mentioned mobile phone, a PDA (Personal Digital Assistants), a digital camera, a compact game machine or the like, is small, since these electronic devices are each a mobile information terminal. Therefore, by forming functional circuits such a CPU, a memory, a sensor with using a minute transistor shown in the above mentioned embodiment mode, electronic devices can be smaller and lighter.

The TFT manufactured by using the laser irradiation device of the present invention can be used as a thin film integrated circuit or a non-contact thin film integrated circuit device (also, referred to as Radio Frequency IC tag, RFID (Radio Frequency Identification)). Moreover, such as a distribution route of the electronic devices can be revealed by attaching an IC tag to various electronic devices. The specific example is showed with reference to FIGS. 19D and 19E.

FIG. 19D shows a state in which a radio frequency IC tag 1942 is attached to a passport 1941. The passport 1941 may be embedded in the radio frequency IC tag. In the same manner, the radio frequency IC tag can be attached to or embedded in a driver's license, a credit card, cash, coin, securities, a gift certificate, a ticket, a traveler's check (T/C), insurance, a residence certificate, a family register, and the like. In this case, only the information showing the real one is inputted into the radio frequency IC tag and an access right is set to prevent illegal reading or writing of information. This can be realized by using a memory shown in another embodiment mode. By using it as a tag, in this manner, it is possible to distinguish a counterfeit

from the real one.

In addition to the above, the radio frequency IC tag can also be used as a memory. FIG. 19E shows an example in which the radio frequency IC tag 1951 is attached to a label attached to a vegetable wrapping. Also, the radio frequency IC tag may be attached to or embedded in the wrapping itself. The radio frequency IC tag 1951 can record process of commodity circulation, price, numerical quantity, use application, shape, weight, expire date, various identification information, etc, and stages of a production process such as place of production, producer, date of manufacture, processing method, etc. The information from the radio frequency IC tag 1951 is read by receiving it with an antenna portion 1953 of a wireless reader 1952, and displaying on a display portion 1954 of the reader 1952. Thus, the information can be easily known by a dealer, a retail seller, and a consumer. In addition, by providing the access right to each producer, trader, and consumer, it is set so that a person who does not have an access right cannot read, write, change or erase information.

Further, the radio frequency IC tag can be used as below. In stores, the information that payment has been made is written in the radio frequency IC tag, and whether payment has been made or not is checked at a provided checking device at an entrance. If people leave the stores without payment, an alarm rings. By this method, forgetting payment or shoplifting can be prevented.

In considering the privacy protection of customers, the following methods are possible. Either of the methods is employed when the payment is made: (1) the data inputted in the radio frequency IC tag is locked with a code number; (2) the data itself inputted in the radio frequency IC tag is encrypted; (3) the data inputted in the radio frequency IC tag is erased; or (4) the data inputted in the radio frequency IC tag is destroyed. These methods can be realized by using a memory shown in the above described embodiment modes. A checking device is provided at an entrance, and whether or not either of the processes (1) to (4) is conducted, or whether nothing is written in the data in the radio frequency IC tag is checked, in order to check whether payment has been made. In this manner, it is possible to check whether payment has been made in stores, and it can prevent the information in the radio frequency IC tag to

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be read without the holder's intention outside of stores.

The manufacturing cost of the above mentioned radio frequency IC tag is higher than that of a barcode used conventionally. Thus, it is necessary to reduce the cost. By the present invention, the width of a region of large grain crystals formed by one time scanning can be increased. In addition, the rate of border portion of adjacent crystalline regions (in other words, micro crystalline region) dramatically decrease more than ever before. Thus, the semiconductor element can be formed without waste, so that it is effective for cost reduction. Further, it is possible to manufacture all radio frequency IC tags with high quality and without variations of its function.

As mentioned above, the applicable range of a semiconductor device manufactured by the present invention is extremely large, and a semiconductor device manufactured by the present invention can be used for various electronic devices.

In addition, this embodiment mode can be freely combined with Embodiment Modes 1 to 6.

INDUSTRIAL APPLICABILITY

According to the present invention, a laser beam with an extremely high output power can be obtained without using a nonlinear optical element for converting a wavelength. Therefore, the width of a region of large grain crystals formed by one time scanning can be increased so that the productivity can be increased dramatically.

This application is based on Japanese Patent Application serial No. 2004-306140 filed in Japan Patent Office on October 20, 2004, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A method of manufacturing a semiconductor device comprising the steps of:

emitting a laser beam which is a fundamental wave from a laser oscillator;

delivering the laser beam onto a semiconductor; and

crystallizing the semiconductor by irradiating with the laser beam which generates multiphoton absorption while moving the surface of the semiconductor relatively to the laser beam.

2. A method of manufacturing a semiconductor device comprising the steps of:

forming an impurity region in a semiconductor;

emitting a laser beam which is a fundamental wave from a laser oscillator;

delivering the laser beam onto the semiconductor; and

activating the impurity region by irradiating with the laser beam which generates multiphoton absorption while moving the surface of the semiconductor relatively to the laser beam.

3. A method of manufacturing a semiconductor device comprising the steps of:

emitting a laser beam which is a fundamental wave from a laser oscillator;

delivering the laser beam onto a semiconductor; and

crystallizing the semiconductor by irradiating with the laser beam which generates multiphoton absorption while moving the surface of the semiconductor relatively to the laser beam,

wherein the laser beam has a peak out power ranging from 1 GW/cm^2 to 1 TW/cm^2.

4. A method of manufacturing a semiconductor device comprising the steps of:

forming an impurity region in a semiconductor;

emitting a laser beam which is a fundamental wave from a laser oscillator;

delivering the laser beam onto the semiconductor; and

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activating the impurity region by irradiating with the laser beam which generates multiphoton absorption while moving the surface of the semiconductor relatively to the laser beam,

wherein the laser beam has a peak out power ranging from 1 GW/cm^2 to 1 TW/cm^2.

5. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate;

forming an insulating layer adjacent to the semiconductor layer;

forming a conductive layer adjacent to the insulating layer;

emitting a laser beam which is a fundamental wave from a laser oscillator;

delivering the laser beam onto the semiconductor layer; and

crystallizing the semiconductor layer by irradiating with the laser beam which generates multiphoton absorption while moving the surface of the semiconductor layer relatively to the laser beam.

6. The method of manufacturing the semiconductor device according to any one of claims 1 to 5,

wherein the laser beam which is a fundamental wave is oscillated with a pulse width of a 1 femtosecond or more and 10 picoseconds or less.

7. The method of manufacturing the semiconductor device according to any one of claims 1 to 5,

wherein the laser beam has a repetition rate of 10MHz or more.

8. The method of manufacturing the semiconductor device according to any one of claims 1 to 5,

wherein the laser beam which is a fundamental wave is emitted from a laser oscillator which includes a crystal selected from the group consisting of Sapphire, YAG, ceramics YAG, ceramicsY_2O_3, KGW, KYW, Mg_2SiO_4, YLF, YVO_4, and $GdVO_4$,

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wherein the crystal is added at least one of Nd, Yb, Cr, Ti, Ho, and Er as a dopant.

9. The method of manufacturing the semiconductor device according to any one of claims 1 to 5,

wherein the laser beam has one of a linear shape and an elliptical shape on the irradiation surface.

10. A laser irradiation method comprising the steps of:

emitting a first laser beam which is a fundamental wave from a laser oscillator;

processing the first laser beam into a second laser beam which has one of a linear shape and a rectangular shape on an irradiation surface;

irradiating an object with the second laser beam which generates a multiphoton absorption.

11. The laser irradiation method according to claim 10, wherein the first laser beam has a repetition rate of 10 MHz or higher.

12. The laser irradiation method according to claim 10, wherein the first laser beam which is a fundamental wave is oscillated with a pulse width of a 1 femtosecond or more and 10 picoseconds or less.

13. The laser irradiation method according to claim 10,

wherein the first laser beam is a laser beam emitted from a laser oscillator which includes a crystal selected from the group consisting of Sapphire, YAG, ceramics YAG, ceramics Y_2O_3, KGW, KYW, Mg_2SiO_4, YLF, YVO_4, and $GdVO_4$,

wherein the crystal is added at least one of Nd, Yb, Cr, Ti, Ho, and Er as a dopant.

14. A laser irradiation apparatus comprising:

a solid state laser oscillator for emitting a laser beam which is a fundamental

wave;

a mechanism for projecting and delivering the laser beam which is the fundamental wave onto an irradiation surface, said mechanism including a condenser lens; and

means for moving the irradiation surface relatively to the laser beam which is the fundamental wave,

wherein the condenser lens forms the laser beam which is the fundamental wave into one of a linear shape and an elliptical shape .

15. The laser irradiation apparatus according to claim 15, wherein the condenser lens includes two pieces of convex cylindrical lenses.

16. The laser irradiation method according to claim 15, wherein the laser beam has a repetition rate of 10 MHz or higher.

17. The laser irradiation apparatus according to claim 15, wherein the laser beam emitted from the laser oscillator is oscillated with a pulse width of 1 femtosecond or more and 10 picoseconds or less.

18. The laser irradiation apparatus according to claim 15, wherein the laser beam oscillated from the laser oscillator is emitted from a laser oscillator which includes a crystal selected from the group consisting of Sapphire, YAG, ceramics YAG, ceramicsY_2O_3, KGW, KYW, Mg_2SiO_4, YLF, YVO_4, and $GdVO_4$ added at least one of Nd, Yb, Cr, Ti, Ho, and Er as a dopant.

19. The laser irradiation apparatus according to claim 15, wherein the laser beam has a peak out power ranging from 1 GW/cm^2 to 1 TW/cm^2.

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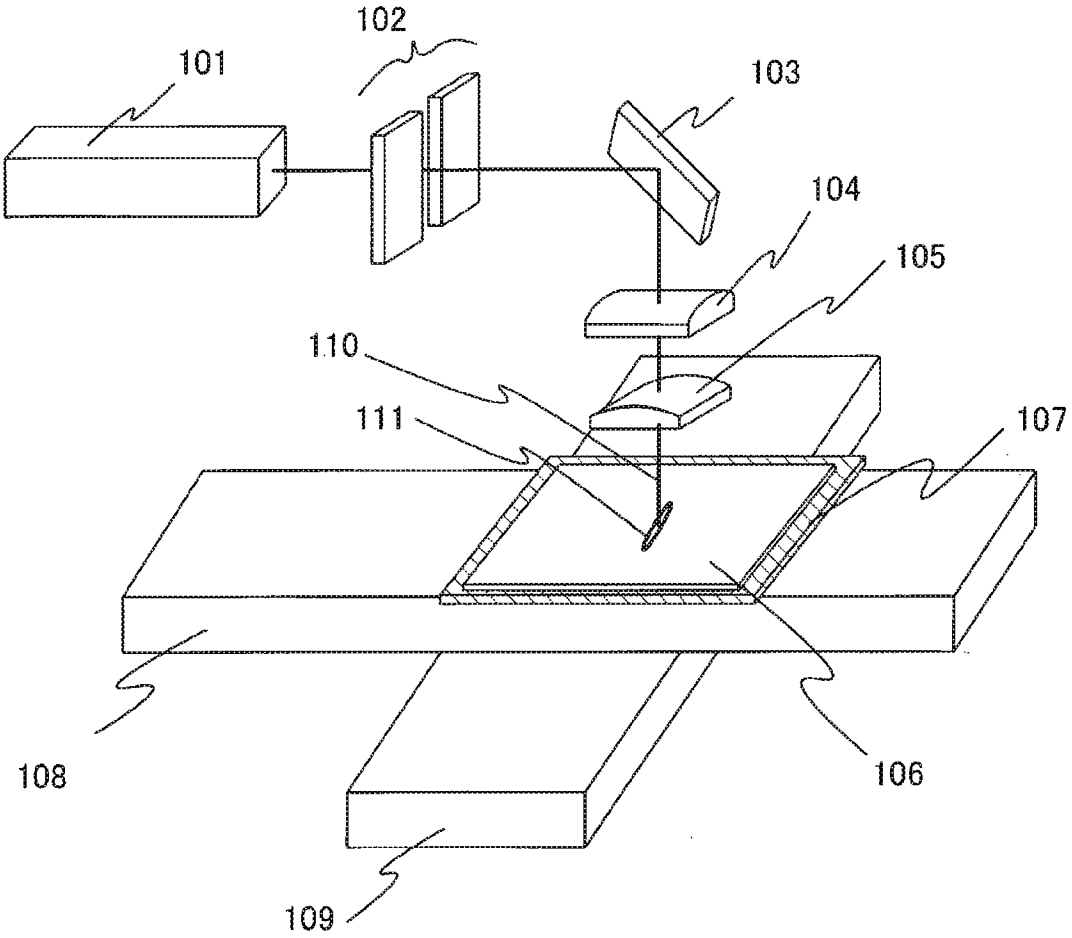


FIG. 1

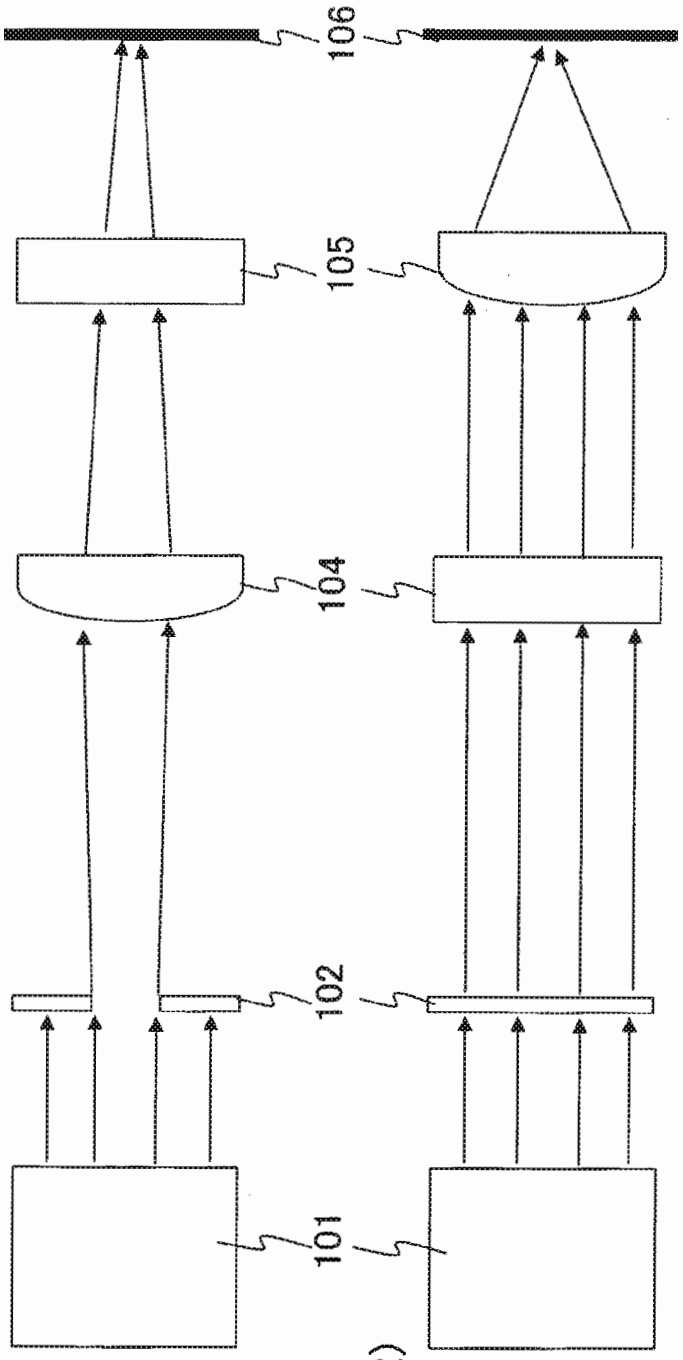


FIG. 2-(1)

FIG. 2-(2)

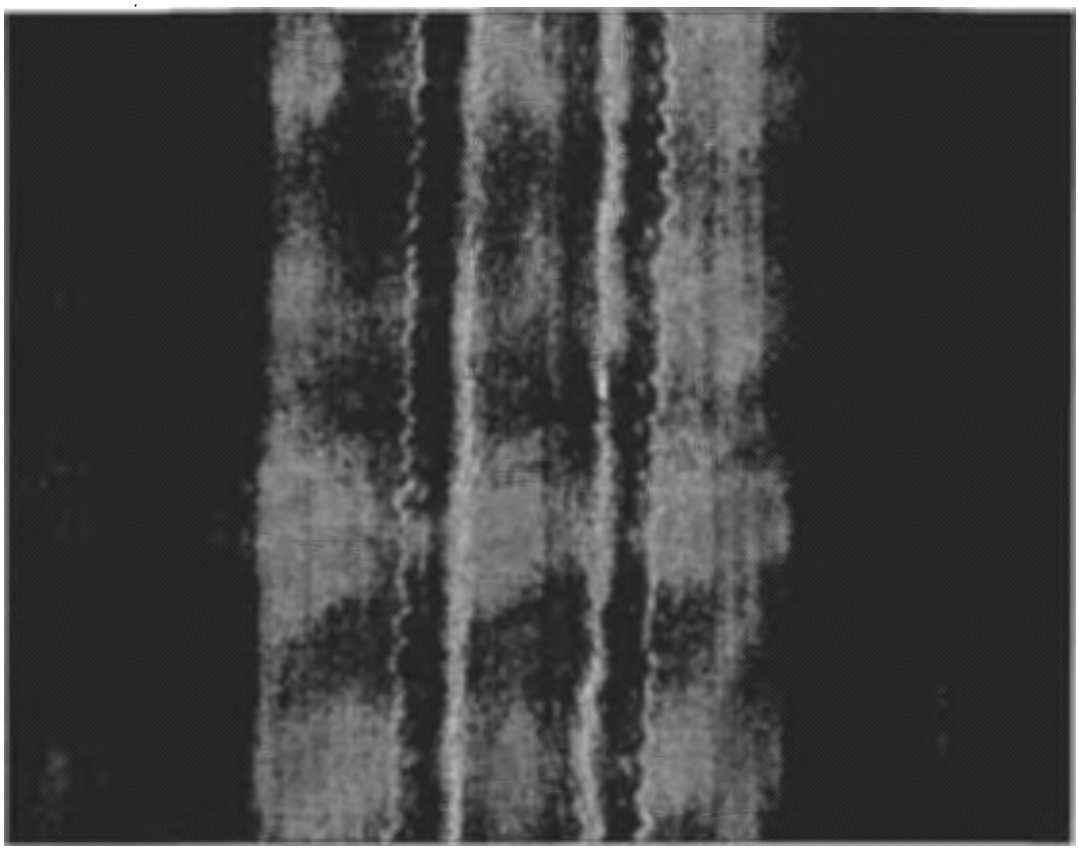


FIG. 3

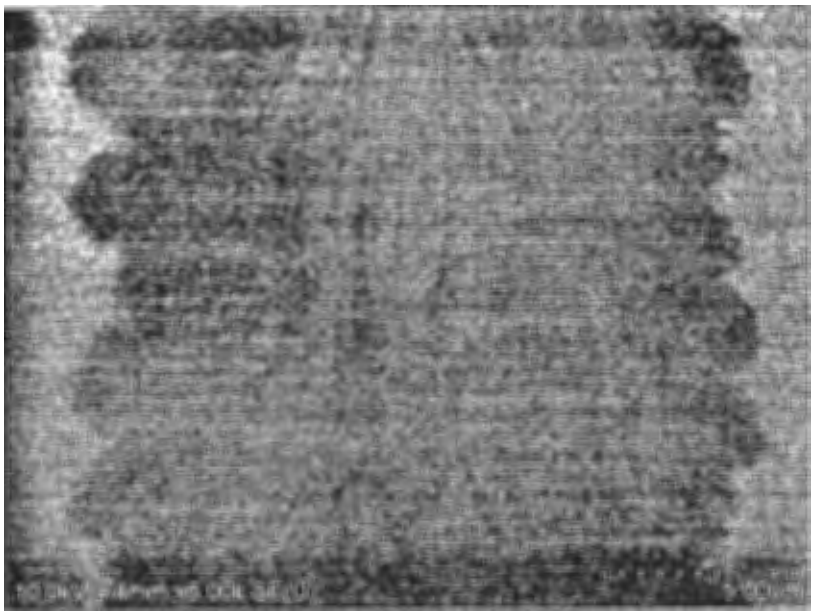


FIG. 4

FIG. 5A

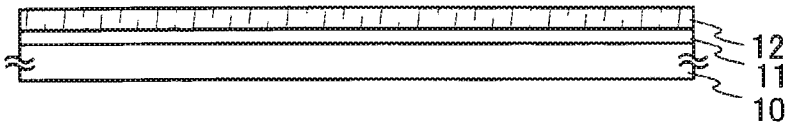


FIG. 5B

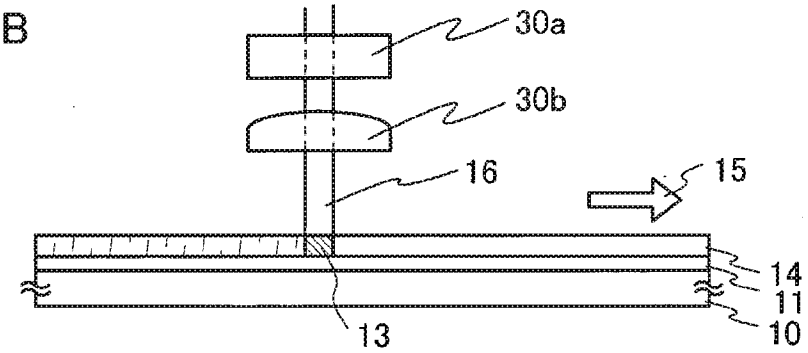


FIG. 5C

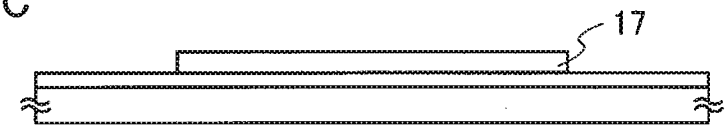


FIG. 5D

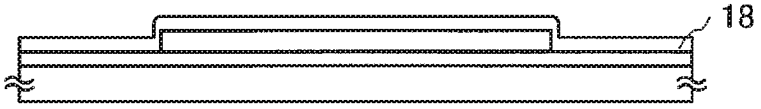


FIG. 5E

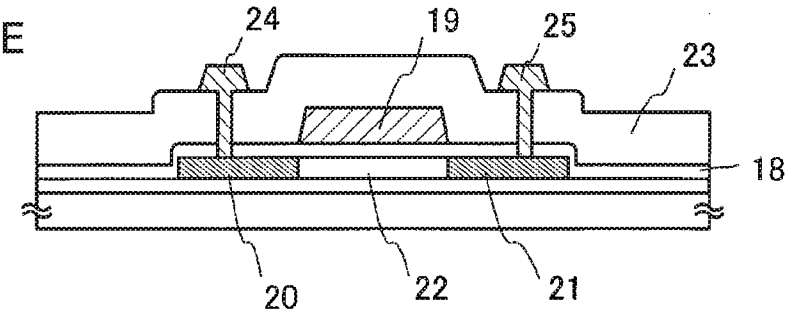


FIG. 6A

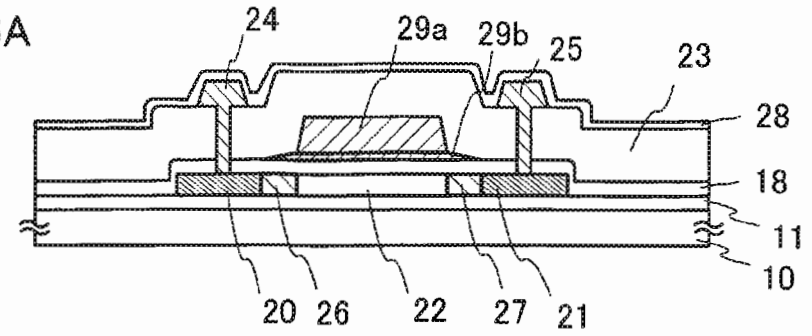
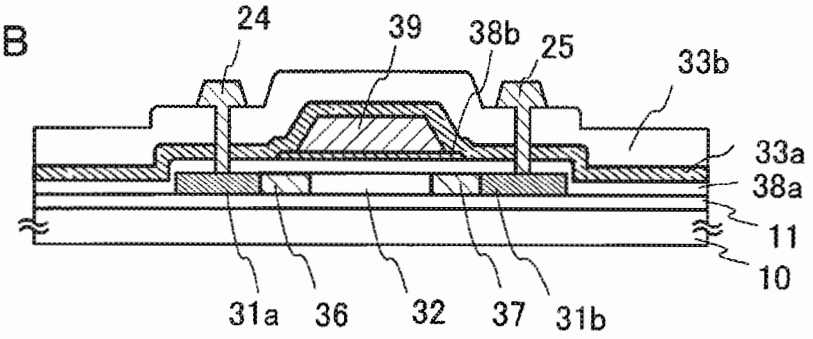

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FIG. 6B


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33b
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38a
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31a
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32
37
31b

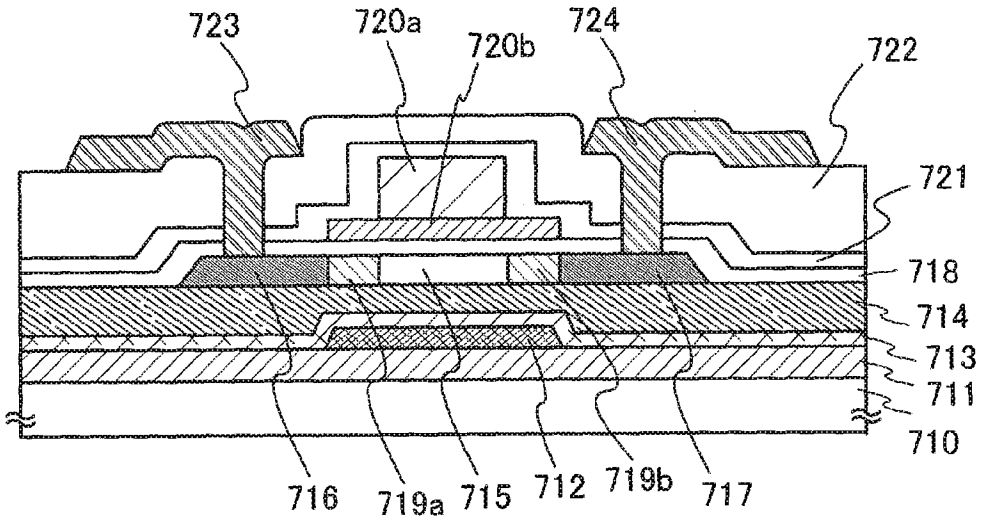

723
720a
720b
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719a
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719b
717

FIG. 7

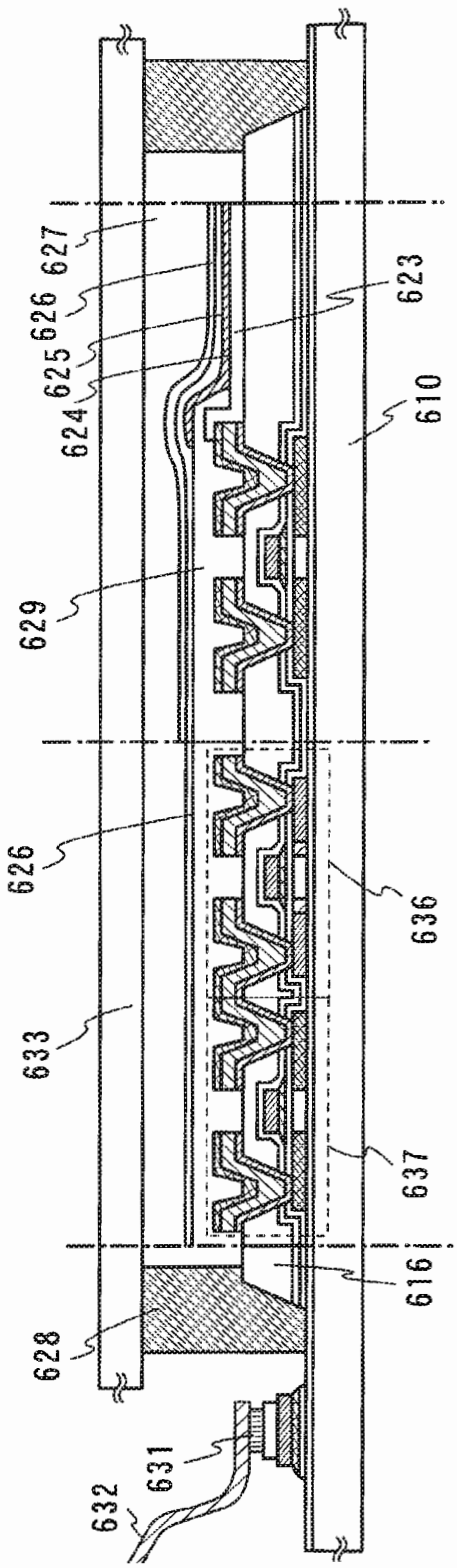


FIG. 8

FIG. 9A

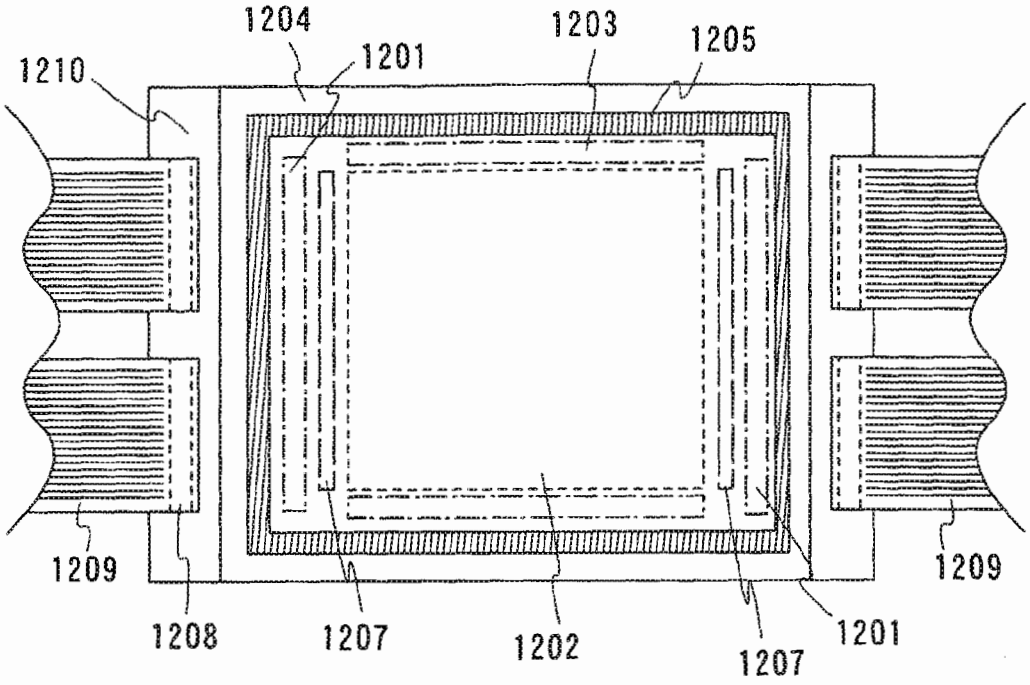
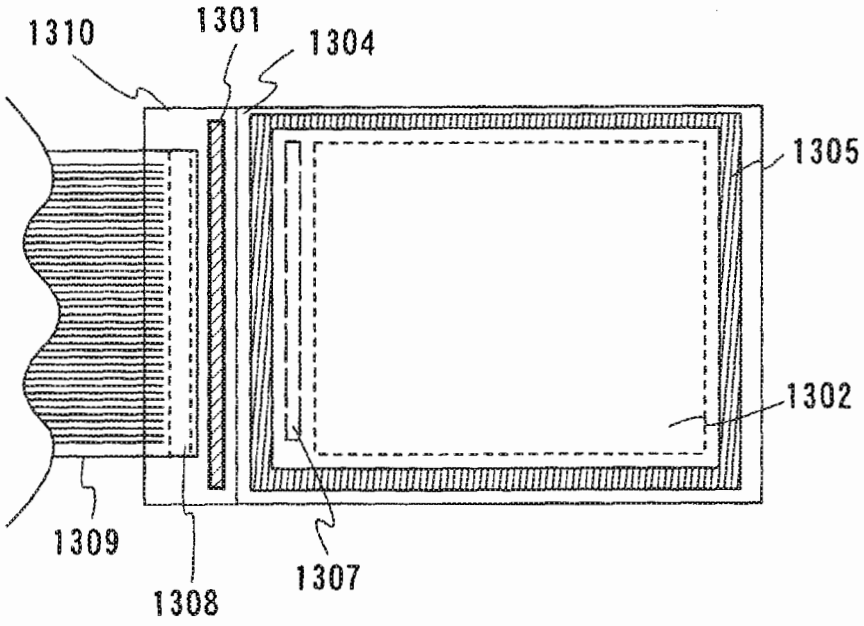

1204
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FIG. 9B


1310
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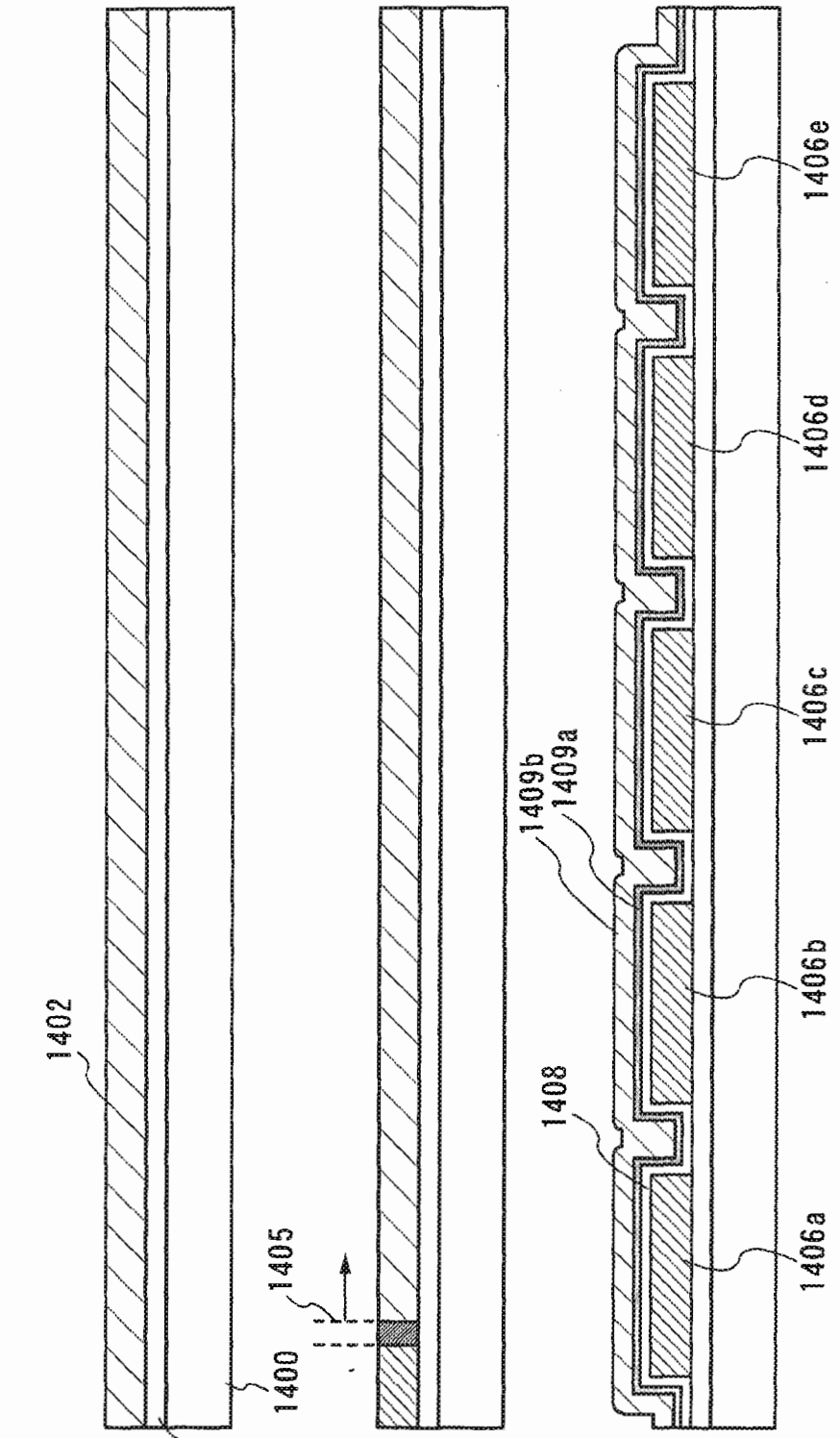


FIG. 10A FIG. 10B FIG. 10C

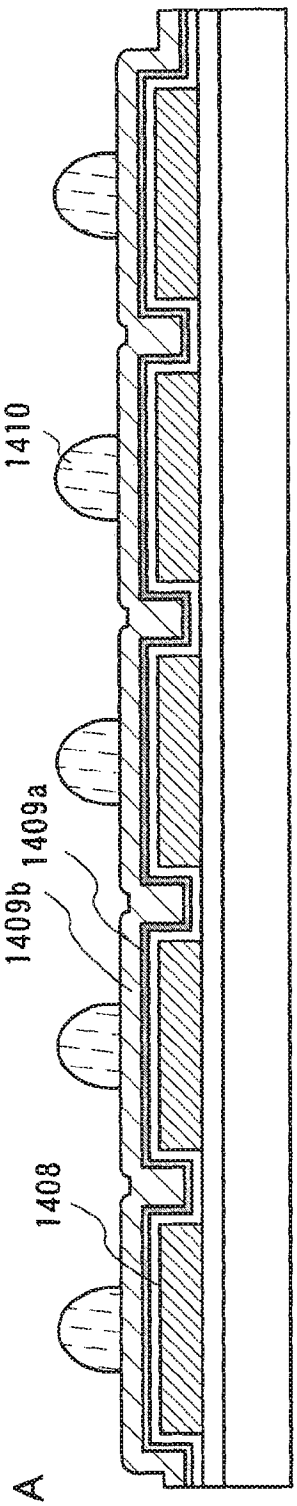


FIG. 11A

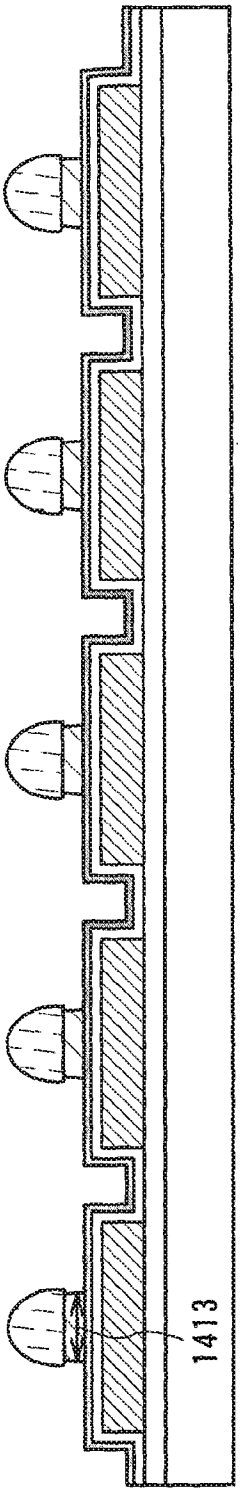


FIG. 11B

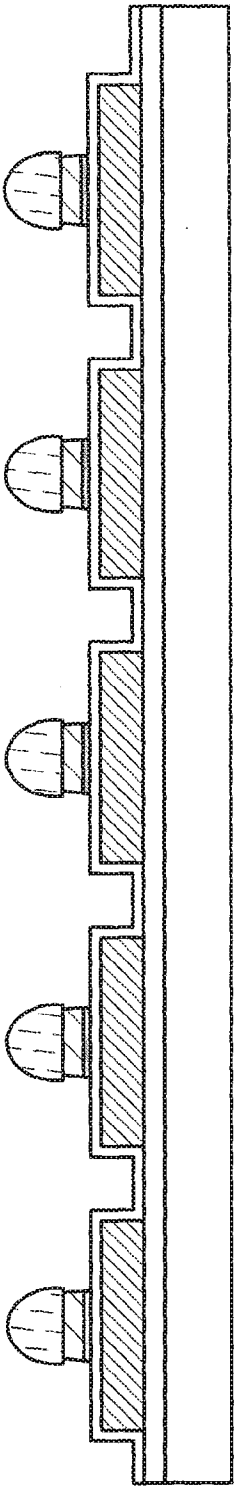


FIG. 11C

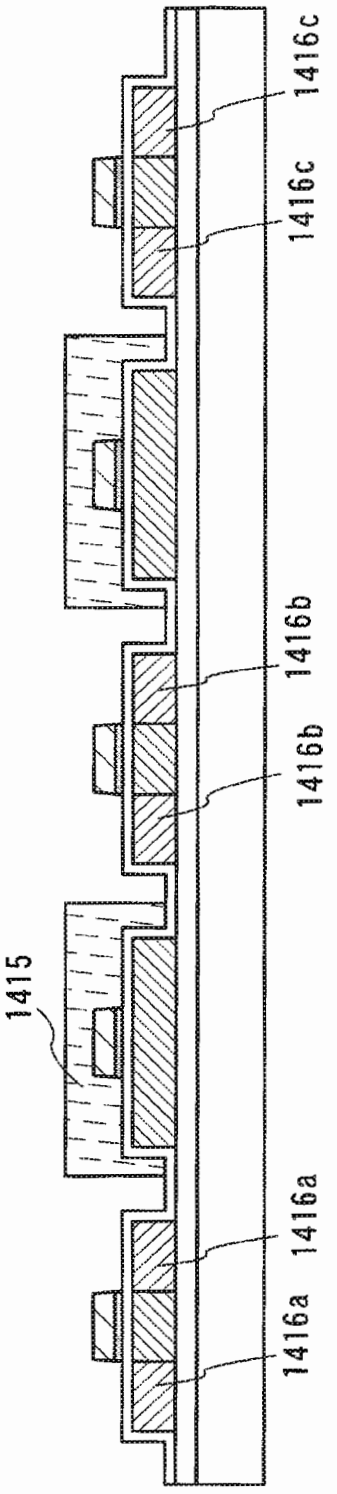


FIG. 12A

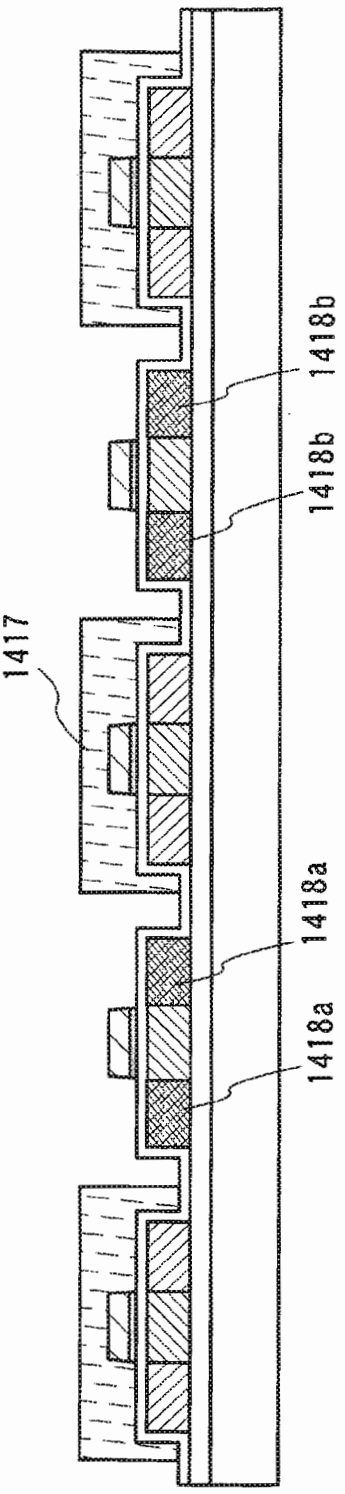


FIG. 12B

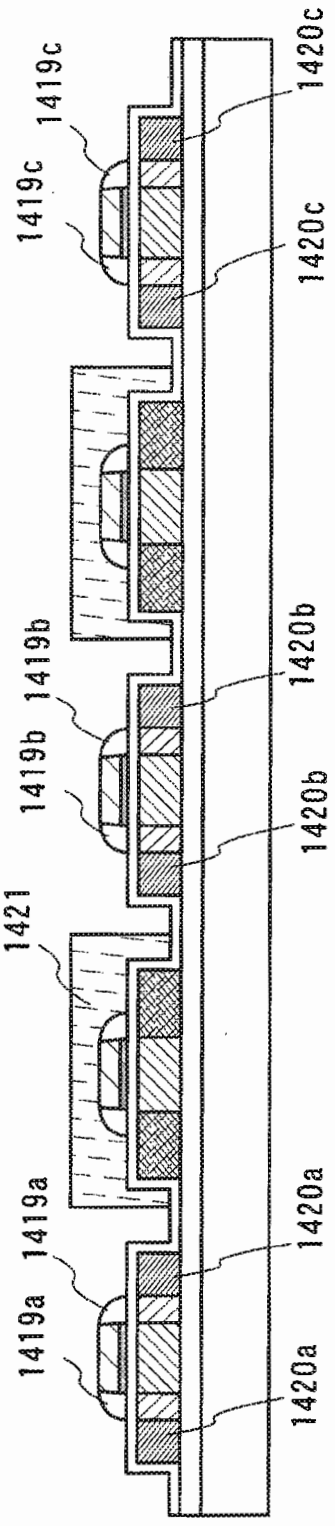


FIG. 12C

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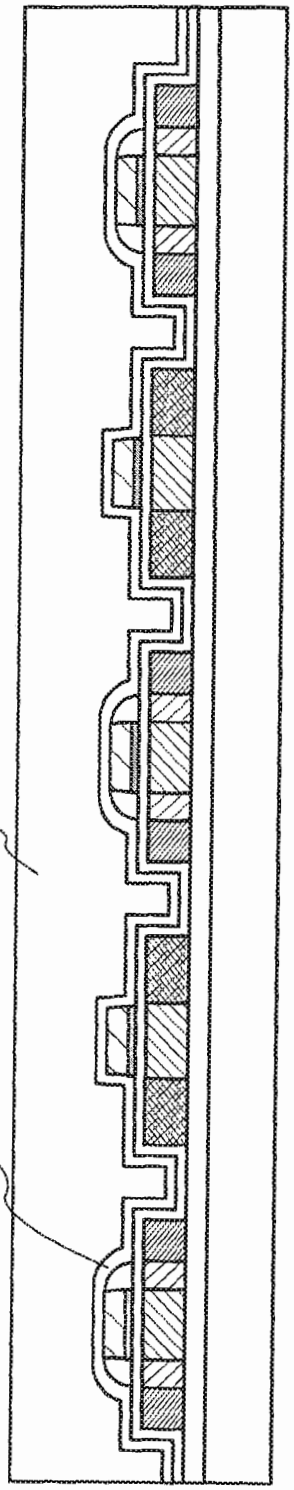


FIG. 13A

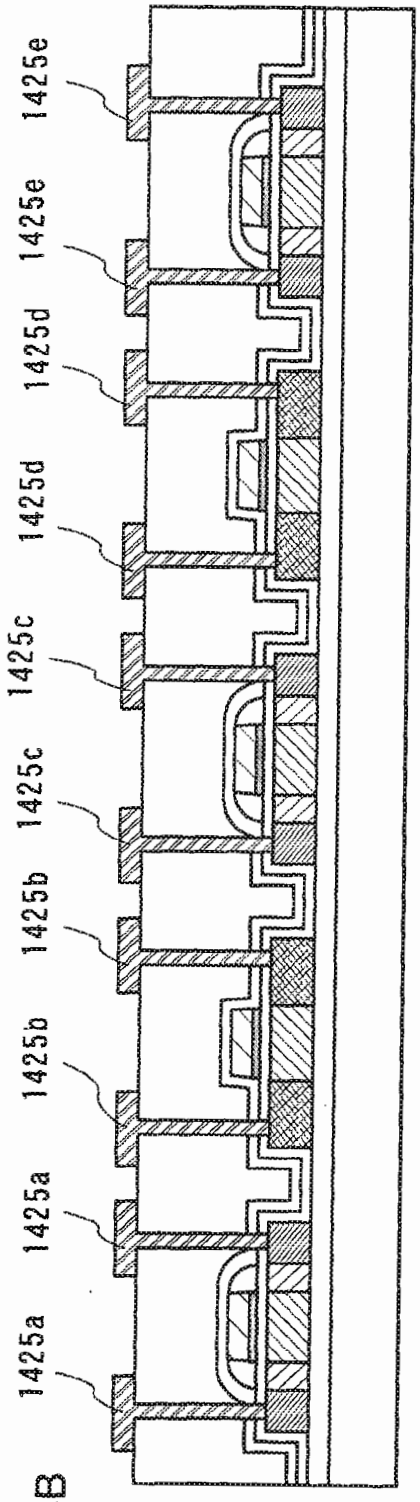


FIG. 13B

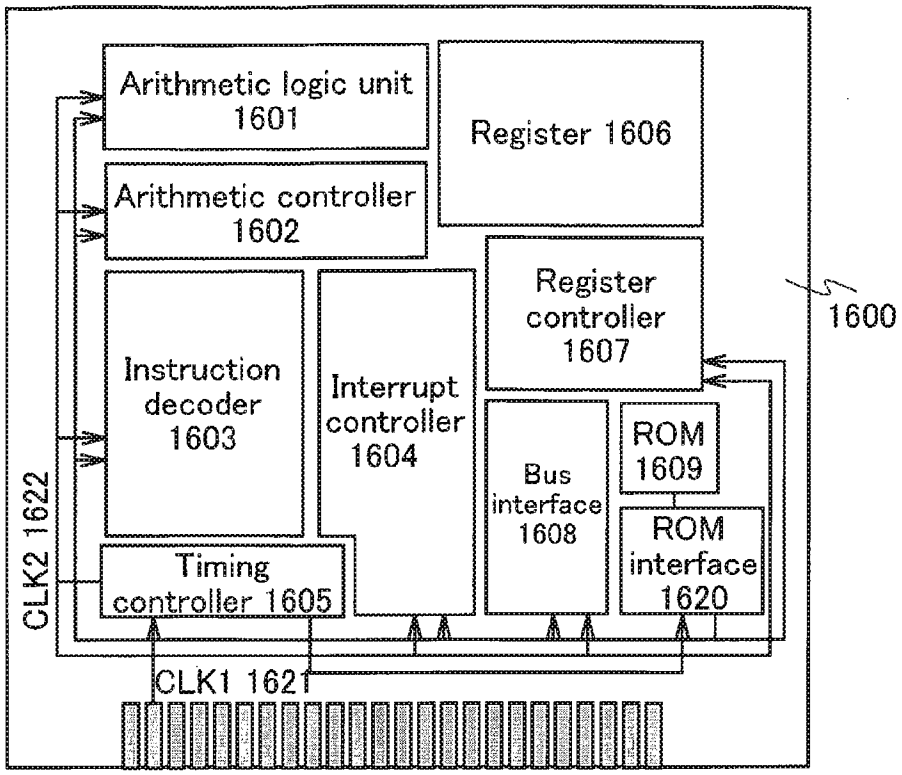

Arithmetic logic unit 1601
Register 1606
Arithmetic controller 1602
Register controller 1607
1600
Instruction decoder 1603
Interrupt controller 1604
Bus interface 1608
ROM 1609
ROM interface 1620
CLK2 1622
Timing controller 1605
CLK1 1621

FIG. 14

FIG. 15A

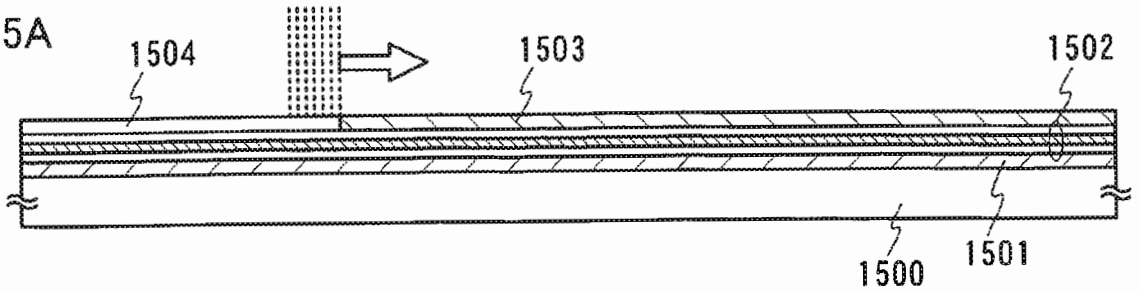


FIG. 15B

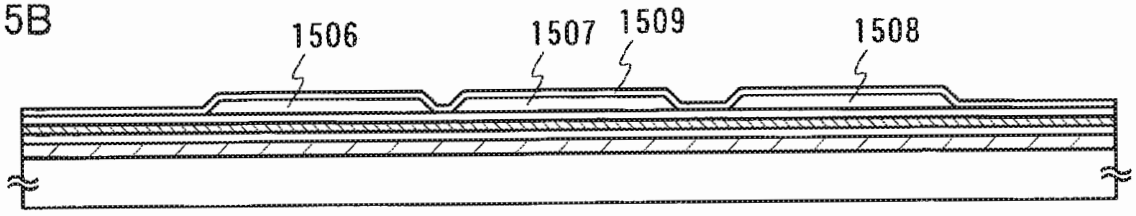


FIG. 15C

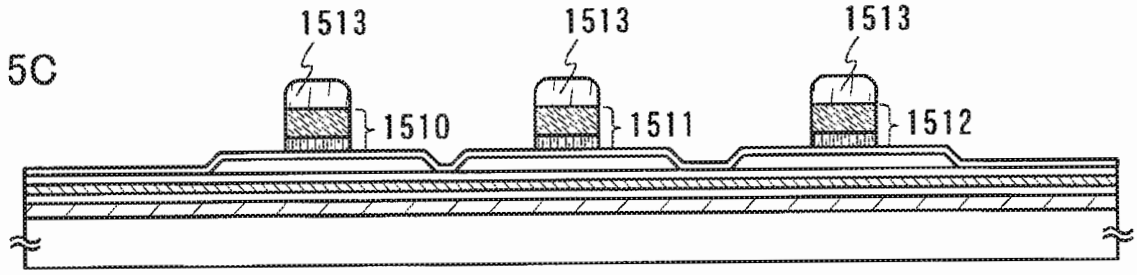


FIG. 15D

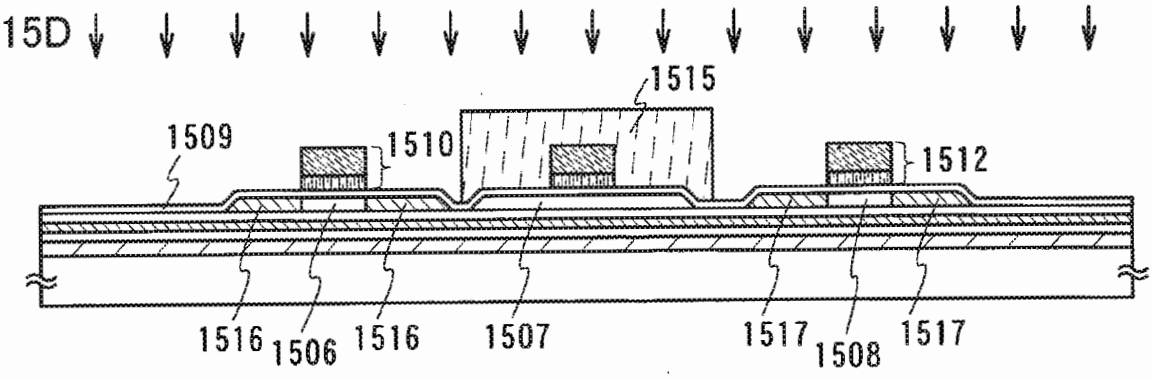


FIG. 15E

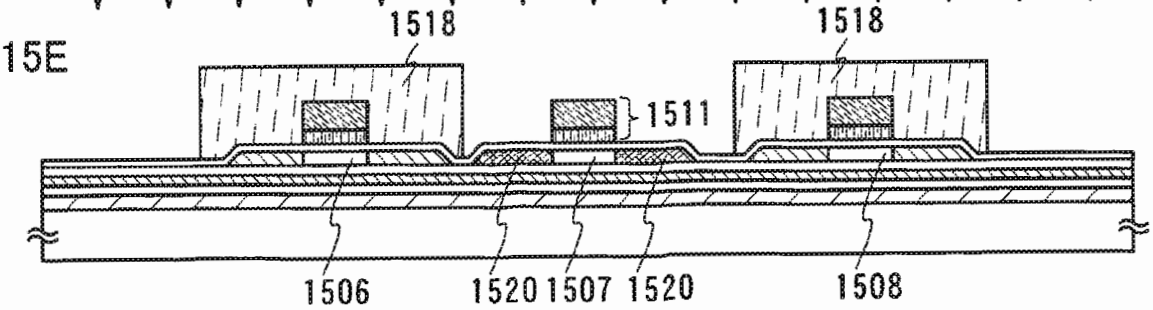


FIG. 16A

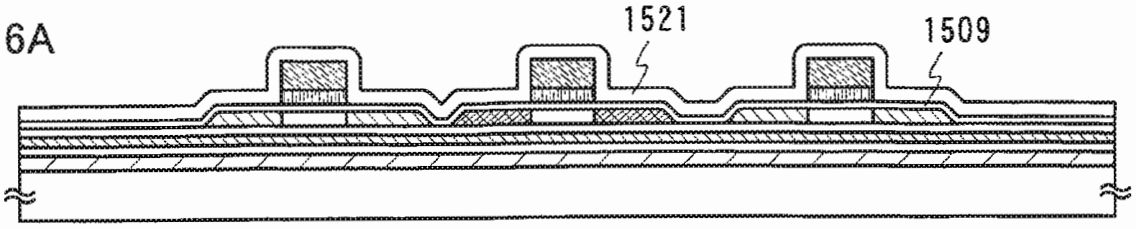


FIG. 16B

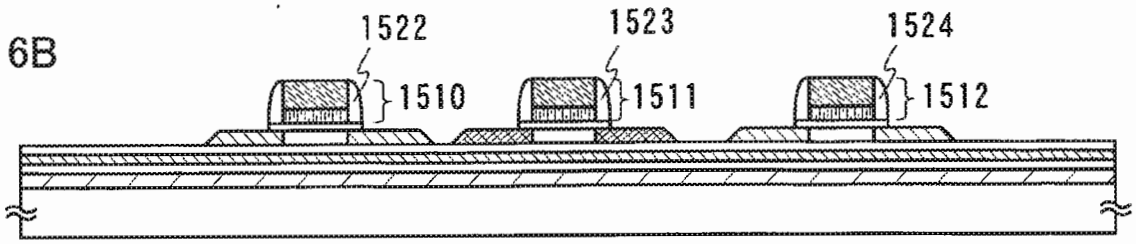


FIG. 16C

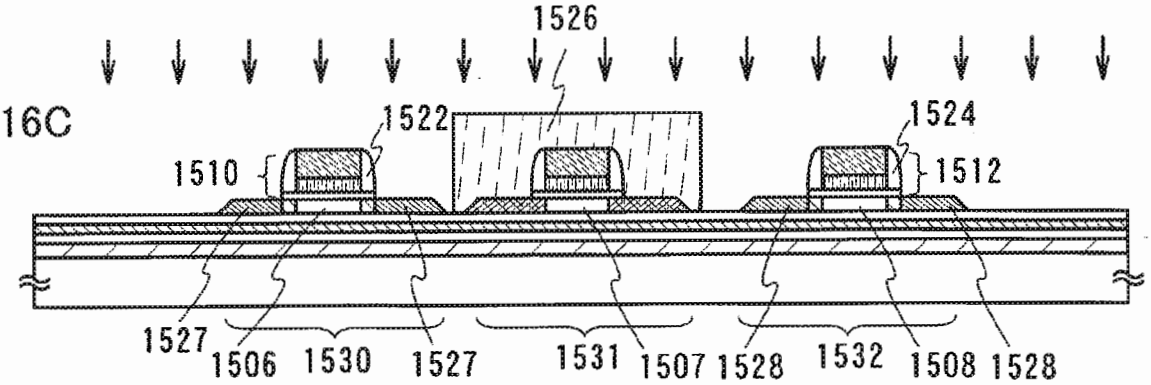


FIG. 16D

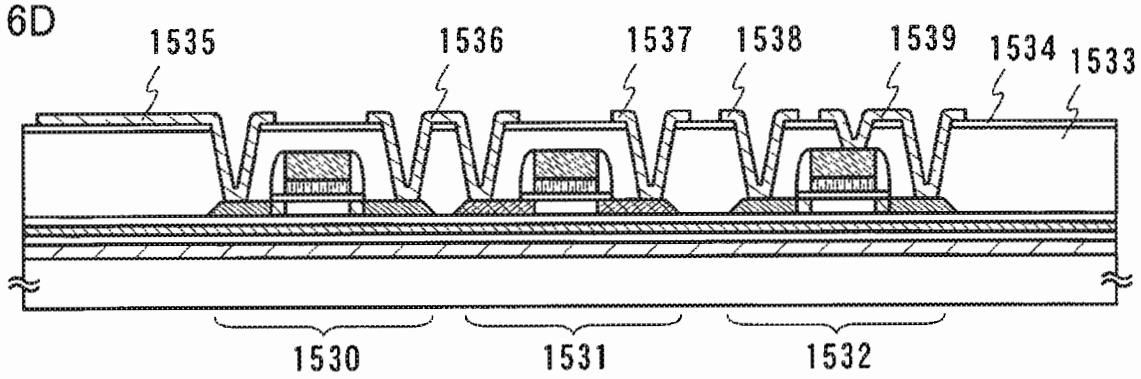


FIG. 16E

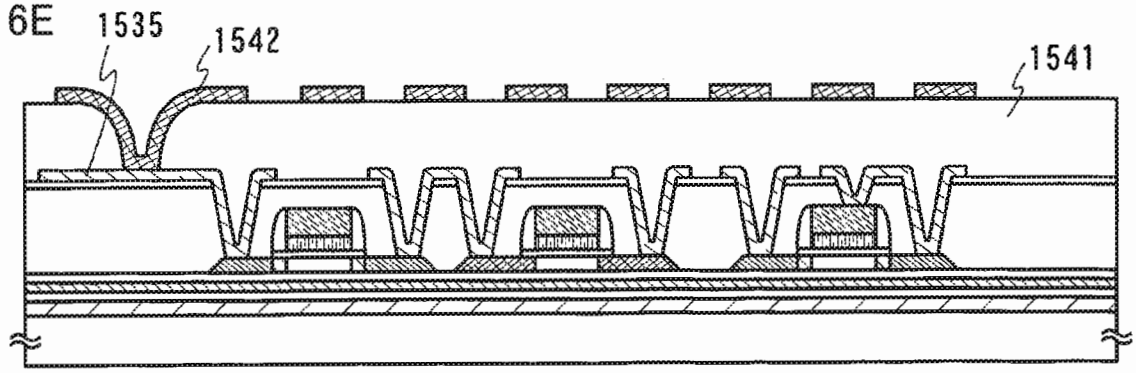


FIG. 17A

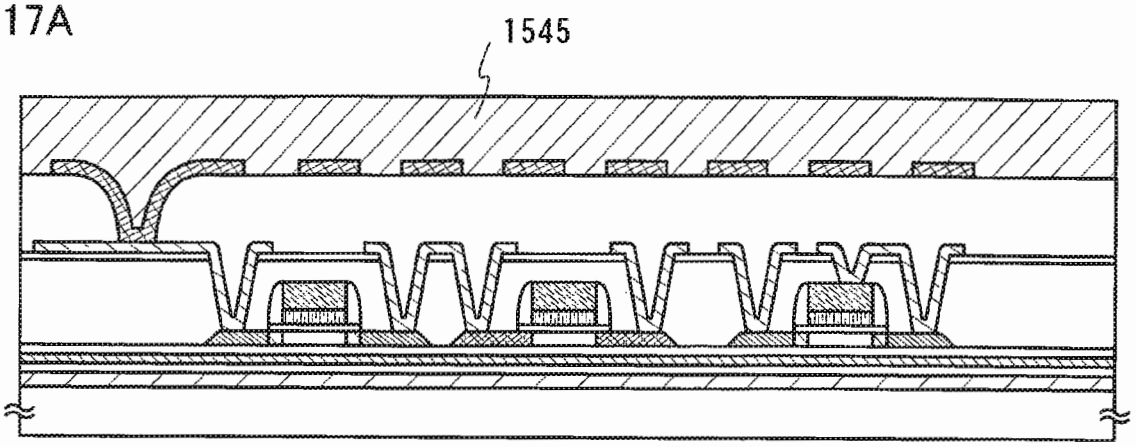


FIG. 17B

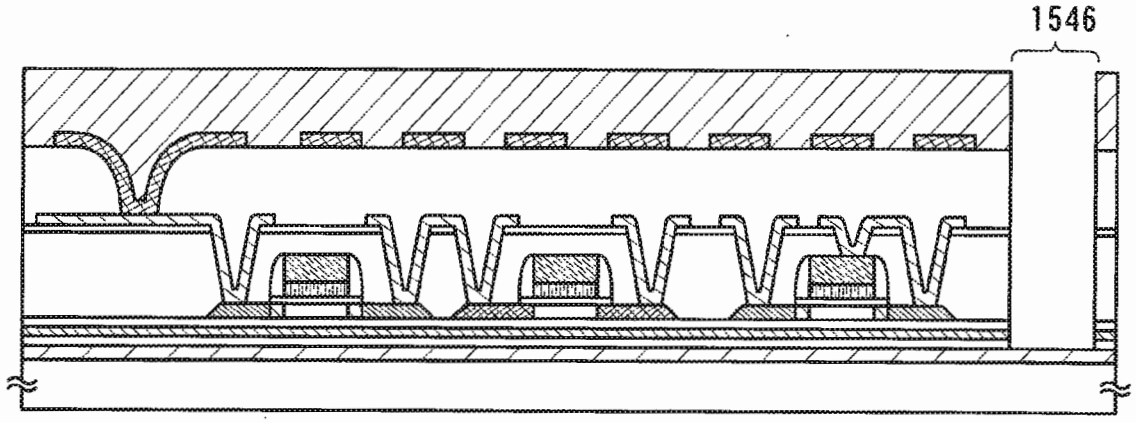


FIG. 17C

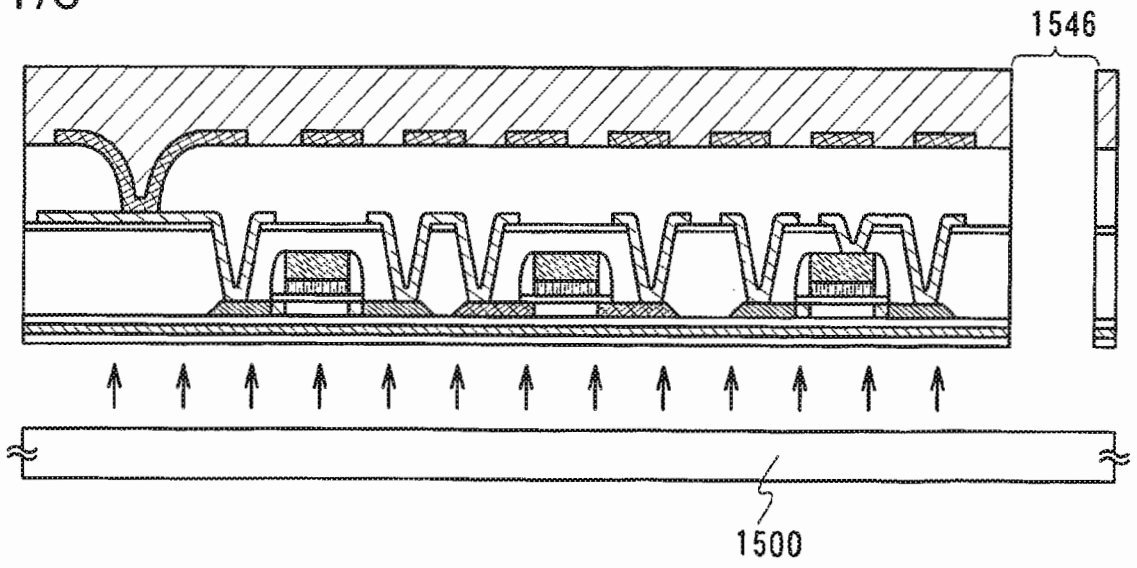


FIG. 18A

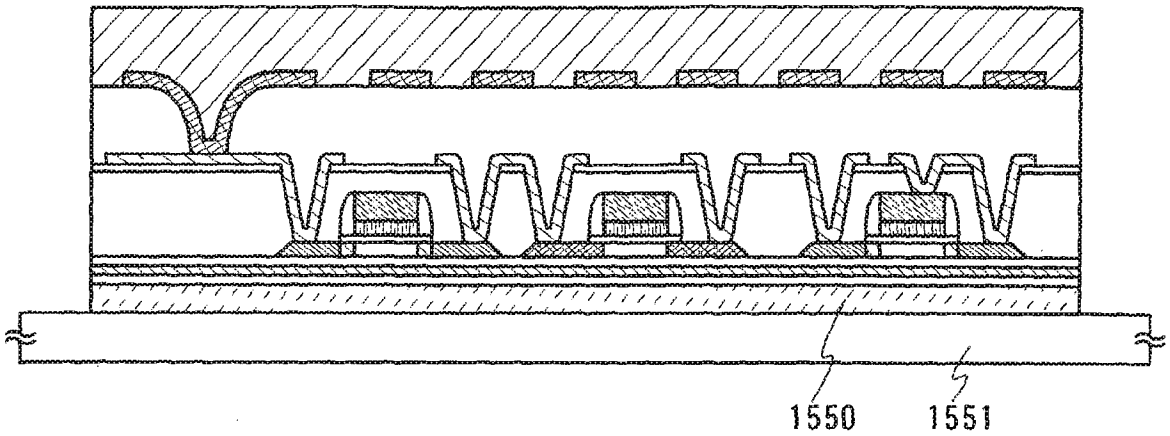


FIG. 18B

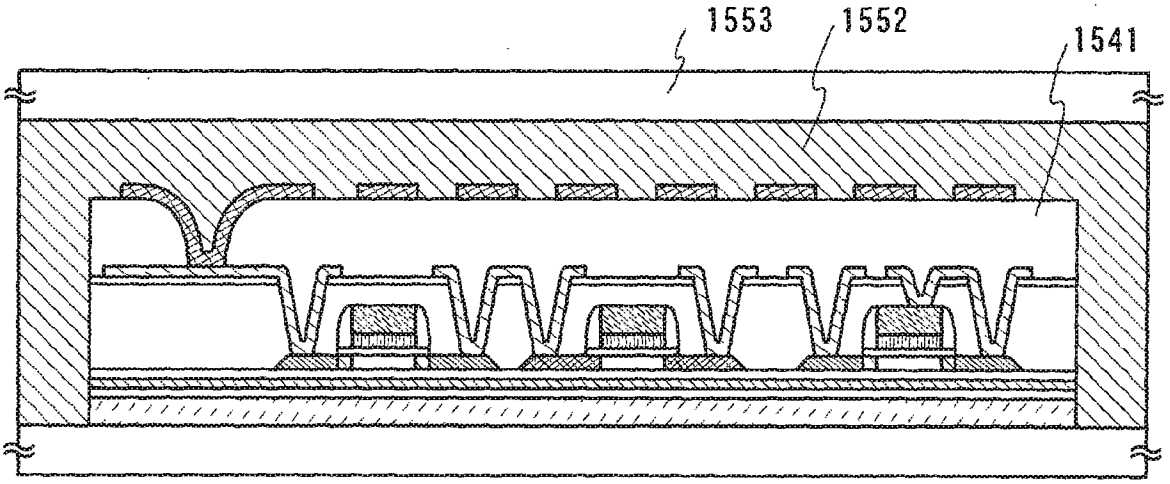


FIG. 19A

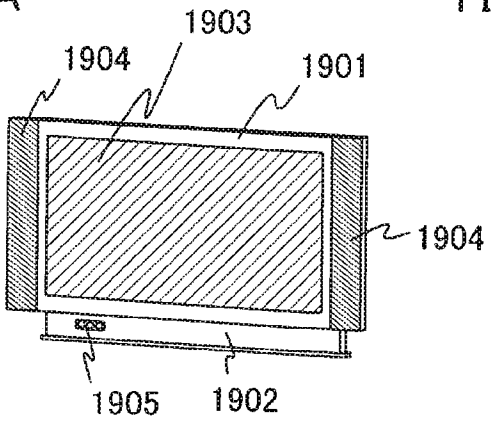


FIG. 19B

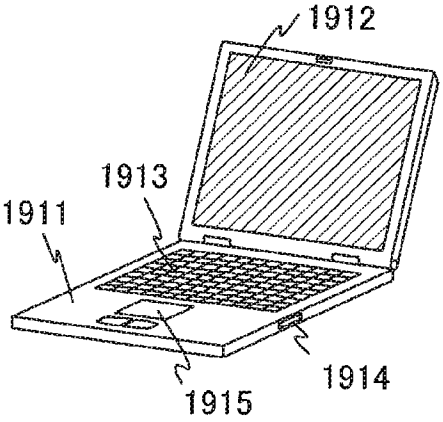


FIG. 19C

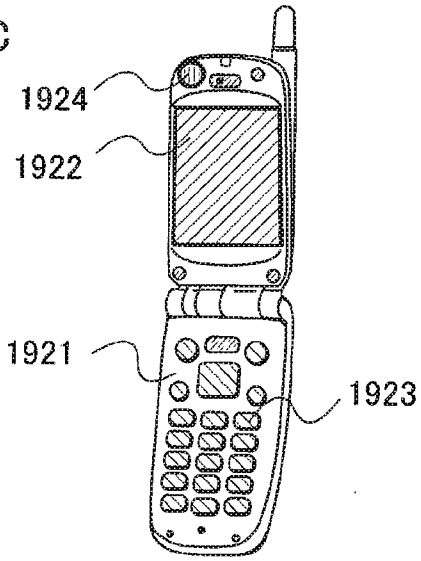


FIG. 19D

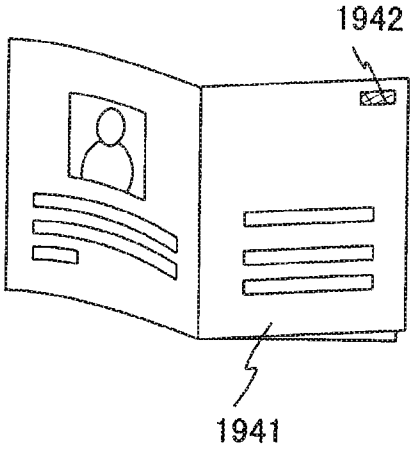
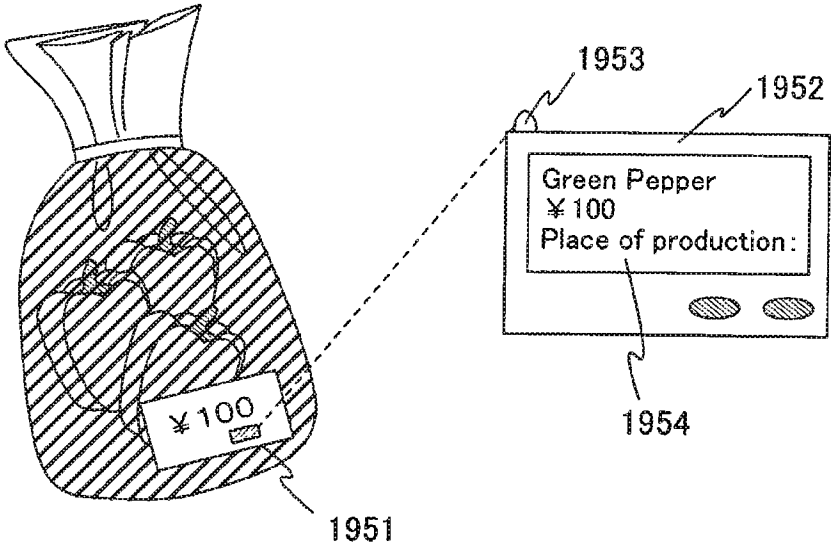


FIG. 19E



EXPLANATION OF REFERENCE

10: substrate, 11: base insulating film, 12: amorphous semiconductor film (semiconductor film having amorphous structure), 13: irradiation region, 14: crystalline semiconductor film (semiconductor film having crystalline structure), 15: arrow, 16: laser light, 17: semiconductor layer, 18: gate insulating film, 19: gate electrode, 20: source region, 21: drain region, 22: channel forming region, 23: interlayer insulating film, 24: source electrode, 25: drain electrode, 26: first LDD region, 27: second LDD region, 28: protective film, 29a: upper layer, 29b: lower layer, 30a: optical system, 30b: optical system, 31a: source region, 31b: drain region, 32: channel forming region, 33a: first interlayer insulating film, 33b: second interlayer insulating film, 36: first LDD region, 37: second LDD region, 38a: first gate insulating film, 38b: second gate insulating film, 39: gate electrode, 101: laser oscillator, 102: slit, 103: mirror, 104: first cylindrical lens, 105: second cylindrical lens, 106: semiconductor film, 107: substrate fixing stage, 108: X stage, 109: Y stage, 110: laser beam, 111: beam irradiation region, 610: substrate, 616: planarizing insulating film, 623: first electrode, 624: layer containing organic compound, 625: second electrode, 626: transparent protective layer, 627: transparent filler, 628: sealing agent 629: insulator, 631: anisotropic conductive film, 632: FPC, 633: sealing substrate, 636: n-channel TFT, 637: p-channel TFT, 710: substrate having insulating surface, 711: base insulating film, 712: lower electrode, 713: first insulating film, 714: second insulating film, 715: channel forming region, 716: source region, 717: drain region, 718: second gate insulating film, 719a: first low-concentration impurity region, 719b: second low-concentration impurity region, 720a: upper layer of upper electrode, 720b: lower layer of upper electrode, 721: insulating film, 722: insulating film, 723: source wiring, 724: drain wiring, 1201: source-side driving circuit, 1202: pixel portion, 1203: gate-side driving circuit, 1204: sealing substrate, 1205: sealing agent, 1207: connecting region, 1208: terminal portion, 1209: FPC, 1210: substrate, 1301: driving IC, 1302: pixel portion, 1304: sealing substrate, 1305: sealing agent, 1307: connecting region, 1308: terminal portion, 1309: FPC, 1310: substrate, 1400: substrate, 1401: base insulating film, 1402: amorphous semiconductor film, 1405: laser light, 1406a: island-shaped semiconductor layer, 1406b: island-shaped semiconductor layer,

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1406c: island-shaped semiconductor layer, 1406d: island-shaped semiconductor layer, 1406e: island-shaped semiconductor layer, 1408: gate insulating film, 1409a: conductive film, 1409b: conductive film, 1410: resist mask , 1413: gate length, 1415: resist mask, 1416a: impurity region, 1416b: impurity region, 1416c: impurity region, 1417: resist mask, 1418a: impurity region, 1418b: impurity region, 1419a: side wall, 1419b: sidewall, 1419c: sidewall, 1420a: high concentration impurity region, 1420b: high concentration impurity region, 1420c: high concentration impurity region, 1421: resist mask, 1422: first interlayer insulating film, 1423: second interlayer insulating film, 1425a: wiring, 1425b: wiring, 1425c: wiring, 1425d: wiring, 1425e: wiring, 1500: first substrate, 1501: peeling layer, 1502: base insulating film, 1503: semiconductor film, 1504: semiconductor film having crystalline structure, 1506: island-shaped semiconductor layer, 1507: island-shaped semiconductor layer, 1508: island-shaped semiconductor layer, 1509: gate insulating film, 1510: gate electrode, 1511: gate electrode, 1512: gate electrode, 1513: resist, 1515: resist, 1516: low-concentration impurity region, 1517: low-concentration impurity region, 1518: resist, 1520: high-concentration impurity region, 1521: insulating film, 1522: sidewall, 1523: sidewall, 1524: sidewall, 1526: resist, 1527: high concentration impurity region, 1528: high concentration impurity region, 1530: n-channel TFT, 1531: p-channel TFT, 1532: n-channel TFT, 1533: first interlayer insulating film, 1534: second interlayer insulating film, 1535: wiring, 1536: wiring, 1537: wiring, 1538: wiring, 1539: wiring, 1541: third interlayer insulating film, 1542: antenna, 1545: protective layer, 1546: groove, 1550: adhesive agent, 1551: second substrate, 1552: adhesive agent, 1553: cover material, 1600: glass substrate, 1601: arithmetic logic unit, 1602: arithmetic logic unit controller, 1603: instruction decoder, 1604: interrupt controller, 1605: timing controller, 1606: resister, 1607: register controller, 1608: bus interface, 1609: ROM, 1620: ROM interface, 1621: CLK 1, 1622: CLK 2, 1901: casing, 1902: support, 1903: display portion, 1904: speaker portion, 1905: video input terminal, 1911: casing, 1912: display portion, 1913: keyboard, 1914: external connection port, 1915: pointing mouse, 1921: casing, 1922: display portion, 1923: operation keys, 1924: sensor portion, 1941: passport, 1942: radio frequency IC tag, 1951: radio frequency IC tag, 1952: reader, 1953: antenna

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portion, 1954: display portion

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2005/019456

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. *H01L21/268 (2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. *H01L21/268 (2006.01)*

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2006
Registered utility model specifications of Japan 1996-2006
Published registered utility model applications of Japan 1994-2006

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0087118 A1 (RENESAS TECHNOLOGY CORP) 2004.05.06, the whole document & JP 2004-158627 A Claim 1,Claim 9,Claim 14, 【0006】, 【0019】, 【0039】, 【0045】-【0046】 & KR 2004040326 A	1,3,2,4,5-9,10-13,14-19
X	JP 2001-338894 A (MATSUSHITA DENKI SANGYO KK) 2001.12.07, Claim 1-Claim 6, 【0007】, 【0012】, 【0026】, 【0030】, 【0032】 (Family None)	1,3,2,4,5-9,10-13,14-19
X	WO 2004/050291 A1 (HAMAMATSU PHOTONICS KK) 2004.06.17, the whole document & JP 3683580 B2 Claim 1, 【0038】-【0039】, 【0043】 & AU 2003289188 A1	1,3,2,4,5-9,10-13,14-19
X	WO 2002/022301 A1 (HAMAMATSU PHOTONICS KK) 2002.03.31, the whole document & AU 200186227 A1 & KR 2003029990 A & EP	1,3,2,4,5-9,10-13,14-19

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04.01.2006	17.01.2006

Name and mailing address of the ISA/JP	Authorized officer
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	1338371 A & US 2004/0002199 A1 & CN 1473087 A	
X	JP 2004-165436 A (ROHM CO LTD) 2004.06.10, the whole document (Family None)	1,3,2,4,5-9,10-13, 14-19

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2005/019456

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
see extra sheet

1. ☑ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☑ No protest accompanied the payment of additional search fees.

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The separate inventions are not so linked as to form a single general inventive concept for the following reasons:

The same or corresponding matters between the inventions of claims Nos. 1-19 are "irradiating an object with the laser beam which generates a multiphoton absorption"

However, after taking the prior art into consideration, it became apparent that the matters were mentioned in a document US 2004/0087118 A1 (RENESAS TECHNOLOGY CORP) 2004.05.06, the whole document , JP 2001-338894 A (MATSUSHITA DENKI SANGYO KK) 2001.12.07, Claim 1,Claim 4,【0012】,【0026】,【0030】,【0032】 , WO 2004/050291 A1(HAMAMATSU PHOTONICS KK) 2004.06.17, the whole document , WO 2002/022301 A1 (HAMAMATSU PHOTONICS KK) 2002.03.31, the whole document , JP 2004-165436 A (ROHM CO LTD) 2004.06.10, the whole document. Therefore, the matters makes no contribution over the prior art.

Consequently, there is no same or corresponding "special technical features" which is the expression in the PCT Rule 13.2. Therefore, there is no technical relationship between the inventions of claims Nos. [1,3] ,[2,4] ,[5-9] ,[10-13] ,and [14-19] .

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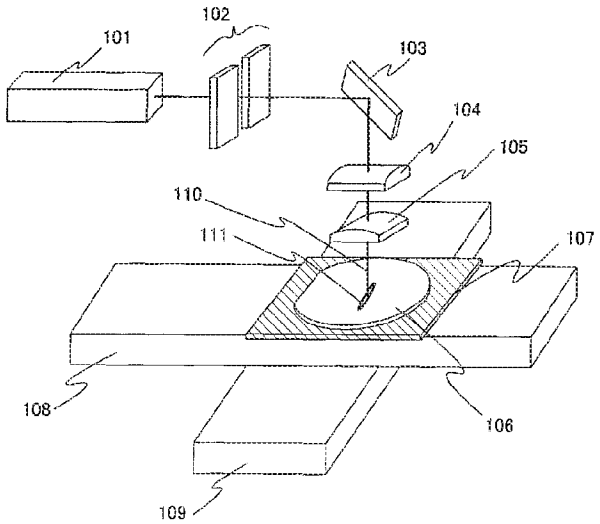
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME



(57) **Abstract:** An RTA method has a limitation on miniaturization. The RTA method needs a heating time of several seconds, and has a risk that impurities are diffused into a deep portion, since a semiconductor substrate is heated at a high temperature. Thus, the RTA method has a difficulty in responding miniaturization which is expected in the future. According to the present invention, a fundamental wave is used without putting laser light into a non-linear optical device, and laser annealing is conducted by irradiating an impurity diffusion layer with pulsed laser light having high intensity and a high repetition rate, so as to electrically activate the impurities. By the present invention, a thin layer on the surface of a silicon substrate can be partially melted to conduct activation. Further, the width of the region activated by laser-scanning once can be increased, and thus the productivity can be enhanced dramatically.

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DESCRIPTION

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME

TECHNICAL FIELD

The present invention relates to a manufacturing method of a semiconductor device, using a laser irradiation apparatus for irradiating an object with laser light. Specifically, the present invention relates to a semiconductor device having a circuit including a field effect transistor (hereinafter, referred to as an FET). Further, the present invention relates to electronic devices incorporating, as a part thereof, e.g., large scale integrated circuits (LSI), electro-optic devices typified by liquid crystal display panels, light-emitting display devices having an organic light-emitting element, sensor devices such as line sensors, or memory devices such as SRAM or DRAM.

Note that semiconductor devices in this specification mean generic devices which can operate with use of semi-conductive characteristics, and the category includes all types of devices such as electro-optic devices, semiconductor circuits and electronic devices.

In recent years, miniaturization and high-integration of LSI have advanced, for instance, the gate length of a MOS transistor formed over a semiconductor substrate is reduced to a submicron level. When a MOS transistor is simply miniaturized, the effective channel-length is shortened, thereby causing a short channel effect between a source and a drain and reducing a threshold voltage of the MOS transistor. In addition, frequent occurrence of a punchthrough, the increase in leakage current, and the like due to the short-channel effect becomes remarkable.

In order to prevent short channel effects, there is employed an LDD structure or a structure in which the junction depth of a diffusion layer formed in a transistor is shallow. The structure in which the junction depth of a diffusion layer is referred to as an ultra shallow junction. The ultra shallow junction is also referred to as extension.

As well as a doping technique in which impurities are added into a desired region or at a desired depth, an annealing technique for activating added impurities has

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been considered.

As one of conventional annealing techniques, a RTA (rapid thermal annealing) method in which a whole semiconductor substrate doped with impurities is heated at about 1000 °C with an infrared lamp or the like is known and frequently used. However, the RTA method has a limitation on miniaturization. The RTA method needs a heating time of several seconds, and has a risk that impurities are diffused into a deep portion, since a semiconductor substrate is heated at a high temperature. Thus, the RTA method has a difficulty in responding miniaturization which is expected in the future.

In view of the above problem, a laser annealing method has attracted attentions as a technique for responding miniaturization which is expected in the future. As a conventional technique using a laser, a technique is known in which the surface of a silicon substrate is melted by a 308-nm XeCl excimer laser and then, silicon atoms are recrystallized.

The laser annealing has advantages that the processing time can be shortened to a large degree as compared with another annealing method using radiation heat or conduction heat, and that a semiconductor substrate can be heated selectively, so that the substrate is hardly damaged thermally.

Laser oscillators used for laser annealing are classified broadly into two kinds, which are a pulsed laser oscillator and a continuous wave laser oscillator, in a standpoint of the oscillation method. Laser light (also, referred to as a laser beam) oscillated from a pulsed excimer laser is used for laser annealing in many cases. The excimer laser has advantages that it has a high output power and repetition irradiation is possible at a high repetition rate.

Laser light emitted from an excimer laser has a high absorption efficiency to silicon which is used as a semiconductor in many cases.

For example, laser irradiation is conducted in the manner that laser light is shaped into linear laser light on an irradiation surface by an optical system (such as a beam homogenizer) and an irradiation position of laser light is moved relatively to the irradiation surface. This method is superior industrially because a semiconductor

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having a large area can be crystallized at one time and thus, high productivity is obtained by this method. Hereinafter, laser light having a linear shape on an irradiation surface is referred to as a linear beam.

DISCLOSURE OF INVENTION

The main purpose of silicon recrystallization with a laser annealing method is to make an impurity region which is damaged by implantation of impurity ions to have a single-crystal state as much as possible, and to electrically activate the impurity region.

[0013]

A conventional laser annealing method using laser light oscillated from a pulsed excimer laser has some problems to be solved. For example, there is a problem that crystal defects are generated in melting and recrystallizing by laser annealing.

As one of methods for solving the problems, there is a method in which a continuous wave laser oscillator (hereinafter, CW laser) such as an Ar laser or a YVO_4 laser or a pulsed laser oscillator having an extremely high repetition rate of 10 MHz or higher (hereinafter, a quasi-CW laser) is employed.

However, in the case of using a CW laser and a quasi-CW laser using a solid state laser medium, the wavelength band of a fundamental wave is from red ray to near-infrared ray, and laser light absorption efficiency in the semiconductor is extremely low. Laser light having high absorption efficiency in the semiconductor is laser light having a wavelength of visible light to ultraviolet light.

Therefore, in the case of using a CW laser or a quasi-CW laser for a laser annealing method, a wavelength is converted to a harmonic of visible light or shorter with a non-linear optical device. For example, the highest conversion efficiency can be obtained in the method of converting a fundamental wave of near-infrared ray which easily provides a high output, to green laser light of the second harmonic.

Harmonics can be obtained by putting a fundamental wave oscillated from a laser medium into a non-linear optical device. However, there is a problem that, when the output of a laser becomes high, a non-linear optical device is damaged by a non

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linear optical effect such as multiphoton absorption, and thus, is broke down. Therefore, a CW laser of visible range which is produced at present has an output power of at most about 15 W due to such a problem of a non-linear optical device.

Further, in conducting laser annealing using a CW laser or a quasi-CW laser, productivity is low as compared with an excimer laser and thus, it is necessary to further enhance the productivity. For example, CW laser light of 532 nm with 10W is formed into a linear beam of about 300 μm in a major axis direction and about 10 μm in a minor axis direction to conduct laser annealing. At this time, the width of a region which can be annealed by scanning once is about 200 μm. Accordingly, scanning of a beam spot is required to be conducted an infinite number of times in order to irradiate the whole surface of a semiconductor wafer having a diameter of 100 to 300 mm which is used in a mass production process. Note that, in this specification, the major axis refers to the long side of a laser beam, and the minor axis refers to the short side of the laser beam, regardless of the shape of the laser beam on an irradiation surface, such as a linear shape, an elliptical shape or a rectangular shape.

According to the present invention, a fundamental wave is used without putting laser light into a non-linear optical device, and laser annealing is conducted by irradiating a semiconductor wafer with pulsed laser light having high intensity and a high repetition rate.

High intensity means a high peak output power per unit of time and per area, and the peak output power of laser light in the present invention ranges from $1GW/cm^2$ to $1TW/cm^2$.

A fundamental wave with a wavelength of about 1 μm is not absorbed so much by a semiconductor wafer in irradiating the semiconductor wafer with the fundamental wave. Thus, the fundamental wave has a low absorption efficiency. The present inventors have found that a fundamental wave emitted from a pulsed laser having a pulse width on the order of picoseconds, or on the order of femtoseconds (10^{-15} seconds) can provide high intensity laser light. Thus, a non linear optical effect (multiphoton absorption) is generated and the fundamental wave can be absorbed by the semiconductor wafer.

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In general, when an energy of one photon is smaller than an energy gap of a semiconductor, the photon is not absorbed by the semiconductor. Thus, in a conventional manner, energy of one photon is increased by converting a fundamental wave to a harmonic with a non-linear optical device as described above. In the case of using an n-th (n is a natural number) harmonic with a wavelength λ, the energy E of one photon is represented by the next equation using Planck's constant $\hbar$ and light velocity c.

$$E = \frac{\hbar c}{\lambda / n} \quad \text{----------[EQUATION 1]}$$

When laser light with high intensity is used, high electromagnetic field is generated in a material irradiated with laser light, thereby generating a nonlinear optical effect (multiphoton absorption). By the multiphoton absorption, photons can be absorbed at the same time in multiple steps without letting light passing through the semiconductor, in the case where the energy of one photon smaller than the energy band gap of the semiconductor.

According to the present invention, a laser oscillator having a higher output power than 15 W, e.g., 40 W output power can be used for laser annealing, since a non-linear optical device is not used and thus light is not converted to a harmonic. Therefore, the width of an impurity region activated by one time laser-scanning can be increased, and thus the productivity can be enhanced dramatically.

A structure of the present invention disclosed in this specification is a manufacturing method of a semiconductor device, which comprises the steps of: selectively injecting impurities into a semiconductor substrate to form an impurity region; processing a laser beam having a fundamental wave into a long beam on a surface of the impurity region; and moving the surface of the impurity region relatively to the long beam to scan the laser beam to activate the impurity region.

In the above structure, the semiconductor substrate is a single-crystal silicon substrate or a compound semiconductor substrate, typically, an n-type or p-type single-crystal silicon substrate, a GaAs substrate, an InP substrate, a GaN substrate, a SiC substrate, a sapphire substrate, or a ZnSe substrate. As a semiconductor element

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including an integrated circuit formed using a semiconductor substrate, typically, a power supply circuit, a reception-transmission circuit, a memory and an amplifier of an audio processing circuit are given.

Further, an SOI substrate may be used. Another structure of the present invention is a manufacturing method of a semiconductor device, which comprises the steps of: forming a gate insulating film over a semiconductor layer of an SOI substrate; forming a gate electrode over the gate insulating film; selectively injecting impurities into the semiconductor layer of the SOI substrate to form an impurity region; processing a laser beam having a fundamental wave into a long beam on a surface of the impurity region; and moving the surface of the impurity region relatively to the long beam to scan the laser beam to activate the impurity region.

In each of the above structures, the impurity regions are source and drain regions of a field effect transistor. An impurity element imparting an n-type conductivity to a semiconductor (such as As or P) or an impurity element imparting a p-type conductivity to a semiconductor (such as B) is added into the source and drain regions to reduce resistance. By selective laser irradiation, a desired region is only activated to reduce resistance.

In the above structure, the impurity region is an extension region of a field effect transistor. The junction depth of the extension region is shallower than the junction depth of the source and drain regions. An impurity element imparting an n-type conductivity to a semiconductor or an impurity element imparting a p-type conductivity to a semiconductor is included in the extension region. In addition, both an impurity element imparting an n-type conductivity to a semiconductor and an impurity element imparting a p-type conductivity to a semiconductor may be included.

In the above structure, the laser beam is oscillated with a pulse width of 1 femtosecond or more and 10 picoseconds or less. The pulse width of 1 femtosecond or more and 10 picoseconds or less is employed to obtain a sufficiently high intensity for generating multiphoton absorption. A laser beam with a pulse width of several ten picoseconds longer than ten picoseconds does not generate multiphoton absorption. In addition, when an experimental test for heating a semiconductor by a laser beam with a

pulse width of 150 femtoseconds was conducted, it could be observed that the semiconductor was heated. Therefore, it is thought that multiphoton absorption is generated.

As a laser that can provide high enough intensity to cause multiphoton absorption, there is a pulsed laser with a pulse width of pico second or femto second. As the pulsed laser, lasers in which Nd, Yb, Cr, Ti, Ho, Er, or the like is added as a dopant into a crystal of Sapphire, YAG, ceramics YAG, ceramics Y_2O_3, KGW, KYW, Mg_2SiO_4, YLF, YVO_4, $GdVO_4$ or the like are given.

Also, one feature of the present invention is that the repetition rate of a laser used in the present invention is 10 MHz or more. This repetition rate is extremely higher than that of the conventional pulsed laser, which is from several tens to several hundreds Hz. It is said that it takes several tens to several hundreds nanoseconds to solidify the semiconductor completely after the semiconductor is irradiated with the pulsed laser light. When the pulsed laser light has a repetition rate of 10 MHz or more, it is possible to irradiate the semiconductor with pulsed laser light before the semiconductor is solidified after it has been melted by the previous laser light.

By irradiating the same portion with laser light again within several tens to several hundreds nanoseconds, a melting state can be maintained. Therefore, when a pulsed laser having a repetition rate of 10 MHz or more is adopted, it can be considered as a CW laser in a quasi manner and thus, such a laser is referred to as a quasi-CW laser.

Note that the category of a laser annealing method in this specification includes a technique by which a damaged layer or an amorphous layer formed in a semiconductor substrate or a semiconductor film is recrystallized, a technique by which an amorphous semiconductor film formed over a substrate is crystallized, and a technique for activating a dopant added into a semiconductor layer. In addition, the laser annealing method includes a technique for planarization or surface modification of a semiconductor substrate or a semiconductor film.

In addition, multiphoton absorption in this specification means simultaneous absorption of two or more photons, and that reactive electronic excitation state, which cannot be reached by absorption energy of only one photon having the same energy as

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each of the two or more photons, can be reached by the absorption energy of two or more photons. It should be noted that the term "simultaneous" means that two phenomena occur within 10^{-14} seconds. In addition, the described above electronic excitation state is an electronic state of molecules at higher energy than an electronic ground state of molecules, which is achieved by absorbing electromagnetic radiated emission and in which a life time is longer than 10^{-13} seconds.

A device obtained by the above manufacturing method is also one of the present invention. A structure of the device is a semiconductor device having an integrated circuit including a field effect transistor, which comprises a gate insulating film formed over a semiconductor layer; a gate electrode provided over the gate insulating film; a channel forming region formed in the semiconductor layer under the gate electrode through the gate insulating film; an extension region into which an n-type or p-type impurity element is added, and which is located on opposite sides of the channel forming region; and a source region and a drain region which are in contact with the extension region, wherein the extension region has a junction depth shallower than the source region and the drain region; and wherein a length of the channel forming region is 5 nm or more and 80 nm or less.

According to the present invention, selective laser irradiation can be carried out much precisely to conduct activation. Therefore, the length of a channel forming region of a field effect transistor can be set arbitrarily in the range of 5 nm to 80 nm.

In the above structure, the length of the channel forming region is equal to the width of the gate electrode. A channel forming region which is overlapped with the gate electrode is not irradiated with laser light, and diffusion does not occur there. Thus, the length of the channel forming region is equal to the width of the gate electrode.

In the above structure, the integrated circuit includes at least one of a controller, a CPU, and a memory.

By the present invention, a non-linear optical device for converting a wavelength is not needed, and a laser beam with an extremely high output power, for example, a laser beam having an energy of twice or more times as high as a harmonic

can be obtained. Further, by the present invention, it is possible to prevent activated impurities from unnecessarily diffusing into a deep portion in a substrate. Therefore, impurities in an irradiated region can be activated efficiently in a state in which a semiconductor substrate is kept at a sufficient low temperature in recrystallization, and the element thus obtained is suitable for developing a higher performance device.

According to the present invention, an ultra shallow junction having a shallow junction depth can be formed. By forming an ultra shallow junction, leak current can be reduced, and low power consumption can be achieved. Further, miniaturization and high integration of a semiconductor integrated circuit become possible.

Further, a non-linear optical device has a defect that a maintenance-free state, which is an advantage of a solid state laser, cannot be kept long, since the non-linear optical device is easily changed in its quality. However, the present invention can overcome the defect, since the present invention does not need a non-linear optical device. In other words, stability and reliability of a laser irradiation apparatus itself can be enhanced, according to the present invention.

BRIEF DESCRIPTION OF DRAWINGS

In the accompanying drawings:

FIG. 1 is a perspective view showing one example of a laser irradiation apparatus;

FIGS. 2A and 2B show an optical system of a laser irradiation apparatus;

FIGS. 3A and 3B are cross-sectional views of manufacturing steps of an FET according to one aspect of the present invention;

FIGS. 4A to 4D each show manufacturing steps of a SIMOX substrate;

FIGS. 5A to 5F each show manufacturing steps of an FET using SIMOX substrate;

FIG. 6 is a cross-sectional view of a DRAM using a SIMOX substrate;

FIG. 7 is a perspective view showing a cross-sectional structure of a packaged device;

FIGS. 8A and 8B are each a top view of an example of mounting an IC chip of

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the present invention on a panel module;

FIG. 9 is a top view of an example of mounting an IC chip of the present invention on a card; and

FIGS. 10A to 10E each shows an example of electronic devices.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiment Modes of the present invention are described below. The present invention can be carried out in many different modes, and modes and details herein disclosed can be modified in various ways without departing from the spirit and the scope of the present invention.

Embodiment Mode 1

FIG. 1 is a perspective view showing one example of a laser irradiation apparatus according to the present invention.

As a laser oscillator 101 shown in FIG. 1, a laser oscillator which oscillates with a pulse width on the order of femtoseconds (10^{-15}second) is used (also referred to as a femtosecond laser). As the laser oscillator, lasers in which Nd, Yb, Cr, Ti, Ho, Er, or the like is added as a dopant into a crystal of Sapphire, YAG, ceramics YAG, ceramics Y_2O_3, KGW, KYW, Mg_2SiO_4, YLF, YVO_4, $GdVO_4$ or the like can be given. Note that a non-linear optical device is not included in the laser oscillator 101 and thus the fundamental wave of a laser beam is emitted. A non-linear optical device for converting light oscillated from a laser medium to a harmonic is not included in the laser oscillator 101; however, the laser oscillator 101 has high enough light intensity to generate a non linear optical effect (multiphoton absorption) in a semiconductor.

First, a laser beam emitted from the laser oscillator 101 passes through a slit 102. By the slit 102, a weak portion in energy of a laser beam can be blocked and the length of the major axis of the laser beam on an irradiation surface can be controlled. The slit 102 used in the present invention is not especially limited, and a slit having a structure or a shape that can block a weak portion of intensity when light passes through a slit, can be used.

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Thereafter, the direction of a laser beam that has passed through the slit 102 is changed by a mirror 103 and is deflected toward a semiconductor substrate 106. It should be noted that the direction of the laser beam that has been changed may be perpendicular or diagonal to the substrate.

Then, the laser beam whose direction has been changed by the mirror 103 projects an image of the slit 102 onto the semiconductor substrate 106 which is an irradiation surface, by a first cylindrical lens 104 that operates only in one direction. Further, the laser beam is condensed by a second cylindrical lens 105 that operates only in one direction, which is rotated by 90° from the first cylindrical lens 104. Then, the laser beam is delivered to the semiconductor substrate 106. A beam irradiation region 111 having a linear, elliptical or rectangular shape on the irradiation surface is obtained by the first cylindrical lens 104 and the second cylindrical lens 105. The first cylindrical lens 104 shapes a laser beam in a major axis direction of the beam irradiation region 111, while the second cylindrical lens 105 shapes the laser beam in a minor axis direction of the beam irradiation region 111. The cylindrical lens used in the present invention may be planoconvex, in which either the side the beam is incident into or emitted from is convex, or biconvex. In the case of using a planoconvex cylindrical lens, it is preferable that the cylindrical lens has a convex surface on the side which the laser beam is incident into, for the sake of low aberration and high accuracy.

An optical system of the present invention is described in detail with reference to FIGS. 2A and 2B. The reference numerals used in FIGS. 2A and 2B are the same as those in FIG.1. FIG. 2A shows a laser beam in the major axis direction of a laser irradiation region and FIG. 2B shows a laser beam in the minor axis direction of the laser irradiation region. A laser beam emitted from the laser oscillator 101 is blocked partially by the slit 102 and only a portion of the laser beam having high intensity passes through the slit. The laser beam which has passed through the slit 102 projects an image formed by the slit 102 onto the semiconductor substrate 106, by the first cylindrical lens 104. The laser beam 110 shown by the solid line in FIG. 1 shows a laser beam which passes through a center of the beam irradiation region 111.

The positional relationship between the first cylindrical lens 104, the slit 102,

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and the semiconductor substrate 106 as an irradiation surface, which is one feature of the present invention, are described in detail. The reason for using slit 102 is to prevent a portion of the laser beam having weak energy from being delivered onto the semiconductor substrate. If such a laser beam having the portion with weak energy is delivered onto the semiconductor substrate, a polycrystal region having relatively small crystal grains and having an uneven surface (here, referred to as a poorly crystalline region) is formed, which is not preferable. In view of this problem, the slit 102 is used so as not to form such a region in the semiconductor substrate. In general, when a laser beam is partially blocked by a slit, a phenomenon called diffraction due to coherence of laser light is caused, and thus diffraction fringes are generated in the laser beam. A method for preventing diffraction fringes on the irradiation surface is described below.

In the two equations shown below, f is the focal length of the first cylindrical lens 104, s is the width of the opening of the slit 102, $M1$ is the distance between the slit 102 and the cylindrical lens 104, $M2$ is the distance between the first cylindrical lens 104 and the semiconductor substrate 106, and L is the length of the linear beam in the major axis direction on the semiconductor substrate 106 which is the irradiation surface. The positional relationships are given by the following two equations:

$$\frac{s}{L} = \frac{M1}{M2} \quad \text{---------- [Equation 2]}$$

$$\frac{1}{f} = \frac{1}{M1} + \frac{1}{M2} \quad \text{---------- [Equation 3]}$$

Based on the equations shown above, two other equations can be given:

$$\mathrm{M1} = \frac{f(s+L)}{L} \quad \text{---------- [Equation 4]}$$

$$\mathrm{M2} = \frac{f(s+L)}{s} \quad \text{---------- [Equation 5]}$$

By arranging the slit, the first cylindrical lens, and the irradiation surface, in accordance with the above equations, the fringes due to diffraction are not translated to the semiconductor substrate. Accordingly, a laser irradiation which rarely forms a

poorly crystalline region can be realized.

In the case that the diameter, the output power or the shape of an emitted laser beam can be used as they are, two cylindrical lenses are not necessarily used. In addition, in the case that the ratio between the major axis and the minor axis of an emitted laser beam is kept during condensing light, a spherical lens may be used instead of a cylindrical lens.

The semiconductor substrate 106 is moved at an appropriate speed to irradiate the whole surface of the substrate with the laser light. In irradiating the substrate with the laser light, the semiconductor substrate 106 is fixed on a substrate fixing stage 107 by a suction means or a mechanical-fixing means so as not to drop. In addition, the substrate fixing stage 107 can be moved using an X stage 108 and a Y stage 109, in an X or Y direction in the surface of the substrate fixing stage, which is parallel to the surface of the semiconductor substrate. By the X stage 108 and the Y stage 109, the semiconductor substrate fixed on the substrate fixing stage 107 can be moved at a speed of 100 to 1000 mm/sec. Here, the stage which the semiconductor substrate is set on is moved in an X direction (or a Y direction) with respect to the fixed irradiation region of a laser beam so as to scan laser light. It should be noted that the optimum scanning speed that is anticipated based on the experience of the present inventors is around 400 mm/sec.

The scanning method is not limited to the method in which X stage 108 and Y stage 109 are moved, and laser light may be scanned by a galvanometer mirror or a polygon mirror. A laser beam that is formed into a belt-like shape is delivered along the lengthwise direction (Y direction) of the substrate and the irradiation region is moved relatively to the substrate so as to scan laser light in the crosswise direction (X direction).

By forming a semiconductor element such as an FET appropriately and by using laser irradiation of the present invention as an activation treatment, such an FET can be applied in the development of a higher performance device.

The diffusion distance of impurities with respect to the pulse width of a laser can be obtained by the following equation.

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$$L_D \fallingdotseq (D_F \tau_L)^{1/2} \text{ ----------[Equation 6]}$$

In the equation 6, τ_L represents time, i.e., a pulse width of a laser. In addition, D_F represents a thermal diffusion coefficient of a material, and $D_F=K_T/\rho C_P$, wherein K_T represents thermal conductivity, ρ represents density and C_P represents specific heat capacity. The thermal conductivity K_T of crystalline silicon is 148W/m·k, and the density ρ of crystalline silicon is 2330kg/cm^3, the specific heat capacity C_P of crystalline silicon is 700J/(kg·k). Accordingly, the thermal diffusion coefficient D_F of crystalline silicon is 9.074×10^{-5}m^2/s.

For example, when the pulse width is set at 1ps, the distance of the thermal diffusion of crystalline silicon is calculated as 9.525853 nm. In the case where a laser beam emitted from a pulse laser having a pulse width on the order of picoseconds, or on the order of femtoseconds (10^{-15} seconds), the distance of the thermal diffusion of crystalline silicon is extremely small, and only a portion irradiated with the laser beam becomes a state of high temperature and high density energy. Thus, almost no thermally affected layer due to thermal diffusion is generated. In other words, in the case where a laser beam emitted from a pulse laser having a pulse width on the order of picoseconds, or on the order of femtoseconds (10^{-15} seconds) is used to activate impurities added into the semiconductor, an ultra shallow junction having a shallow junction depth can be formed.

In the present invention, a junction depth can be freely set by appropriately setting an irradiation condition such as a pulse width of a laser.

Here, an example of laser annealing applied for activation has been described. However, the present invention is not especially limited, and can be applied to various kinds of laser annealing processes typified by such a process as a silicide formation process.

Embodiment Mode 2

A procedure for manufacturing an FET using the present invention will be hereinafter described briefly with reference to FIGS. 3A and 3B. Here, an example of activation is shown, in which a non linear optical effect (multiphoton absorption) is

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produced in an irradiation region by irradiating an impurity region doped with impurities by laser light having a fundamental wave with a wavelength of a near-infrared region, and a pulse width of about 10 ps or less.

A silicon substrate 301 formed of single-crystal silicon is prepared. An n-well 302 is selectively formed in a first element formation region over a main surface (an element formation region or a circuit formation region) of the silicon substrate, and a p-well 303 is selectively formed in a second element formation region over the same surface.

Next, a field oxide film 306 to be an element isolation region for partitioning the first element formation region and the second element formation region is formed. The field oxide film 306 is a thick thermal oxide film and may be formed by a known LOCOS method. Note that the method for partitioning the element formation regions is not limited to the LOCOS. For example, the element isolation region may have a trench structure by using a trench isolation method, or the LOCOS structure and the trench structure may be combined.

Subsequently, a gate insulating film is formed by, for example, thermally oxidizing the surface of the silicon substrate. The gate insulating film may also be formed by CVD. A silicon oxynitride film, a silicon oxide film, a silicon nitride film, or a stack thereof may be used. For example, a stack film of a silicon oxide film with a thickness of 5 nm which is obtained by thermal oxidation and a silicon oxynitride film with a thickness of 10 to 15 nm which is obtained by CVD, is formed.

A stack film of polysilicon layers 311a and 317a and silicide layers 311b and 317b are formed over the entire surface, and the stack film is patterned by lithography and dry etching so as to form gate electrodes 311 and 317 having a polycide structure over the gate insulating film. The polysilicon layers 311a and 317a may be doped with phosphorus (P) at a concentration of about $10^{21}/cm^3$ in order to reduce the resistance. Alternatively, high concentration n-type impurities may be diffused after forming the polysilicon layers 311a and 317a. Further, the silicide layers 311b and 317b can be formed of a material such as molybdenum silicide (MoSix), tungsten silicide (WSix), tantalum siliside (TaSix), or titanium silicide (TiSix) using a known method.

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Subsequently, ion implantation is conducted on the silicon semiconductor substrate through the gate insulating film to form an extension region. In this embodiment mode, an impurity region formed between each channel forming region and each source and drain region is referred to as an extension region. The impurity concentration in the extension regions 307 and 313 may be lower or higher than, or the same as the impurity concentration in the source region and the drain region. Accordingly, the impurity region of the extension region may be determined depending on the characteristics required for a semiconductor device.

Since this embodiment mode describes a case of manufacturing a CMOS, the first element formation region for forming a p-channel FET is coated with a resist material, and arsenic (As) or phosphorus (P) which is an n-type impurity is injected into the silicon substrate. Further, the second element formation region for forming an n-channel FET is coated with a resist material, and boron (B) which is a p-type impurity is injected into the silicon substrate.

Subsequently, a first activation treatment is conducted in order to activate the implanted impurities and to repair crystal defects in the silicon substrate, which is generated by ion-implantation. In this embodiment mode, as shown in Embodiment Mode 1, irradiation of laser light having a fundamental wave and a pulse width of 10 ps or less is conducted to generate a non linear optical effect (multiphoton absorption) to carry out an activation. In order to efficiently conduct this process, the repetition rate of the laser may be 10 MHz or more. The semiconductor substrate is heated up to a temperature around the melting point of Si, and a thin layer on the surface is locally heated to be activated. At this time, since impurities inside Si are heated in an extremely short time, the distance in which the impurities can move is extremely short. However, since the distance is sufficient for the impurities to move to the lattice point of Si, the implanted impurities can be activated sufficiently by this process. In addition, as mentioned above, since the distance in which the impurities can move is extremely short, i.e., about 1 nm or less, diffusion of impurities can be suppressed to the utmost extent.

Thereafter, sidewalls 312 and 318 are formed on the sides of gate electrodes.

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For example, an insulating material layer formed of silicon oxide may be deposited over the entire surface by CVD, and the insulating material layer may be etched back to form the sidewalls. In the etch back, the gate insulating film may be selectively removed in a self-alignment manner. Alternatively, the gate insulating film may be etched after the etch back. Thus, the gate insulating films 310 and 316 having the total width of the gate electrodes and the sidewalls provided on the opposite sides of the gate electrodes are formed.

Next, ion implantation is conducted to the exposed silicon substrate to form a source region and a drain region. Since this is a case of manufacturing a CMOS, the first element formation region for forming a p-channel FET is coated with a resist material, and arsenic (As) or phosphorus (P) which is an n-type impurity is injected into the silicon substrate to form a source region 314 and a drain region 315. Further, the second element formation region for forming an n-channel FET is coated with a resist material, and boron (B) which is an p-type impurity is injected into the silicon substrate to form a source region 308 and a drain region 309.

A second activation treatment is thereafter conducted in order to activate the implanted impurities and to repair crystal defects in the silicon substrate, which is generated by ion-implantation. The second activation treatment is conducted by irradiation of laser light having a fundamental wave and a pulse width of 10 ps or less, and a non linear optical effect (multiphoton absorption) is generated. At this time, the state shown in FIG. 3A is obtained.

After the activation, an interlayer insulating film, a plug electrode, a metal wiring, and the like are formed. The first interlayer insulating film 331 is formed to have a thickness of 100 to 2000 nm with a silicon oxide film, a silicon oxynitride film, or the like by plasma CVD or low pressure CVD. Further, a second interlayer insulating film 332 formed of phosphosilicate glass (PSG), borosilicate glass (BSG), or pborophosphosilicate glass (BPSG) is formed thereover. The second interlayer insulating film 332 is manufactured by spin coating or normal pressure CVD to increase planarity.

Source electrodes 333 and 335, and drain electrodes 334 and 336 are formed

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after forming contact holes reaching the source regions and the drain regions of the respective FETs in the first interlayer insulating film 331 and the second interlayer insulating film 332, and aluminum (Al) which is commonly used as a low resistance material may preferably used. Further, the electrodes may have a stacked structure of aluminum (Al) and titanium (Ti).

[0082]

Although not shown here, a contact hole reaching a gate electrode is provided in the first interlayer insulating film 331 and the second interlayer insulating film 332, and an electrode electrically connecting to a wiring provided over the second interlayer insulating film is formed over the part of the first interlayer insulating film exposed in the opening.

Lastly, a passivation film 341 and a third interlayer insulating film 342 are formed. At this time, the state shown in FIG. 3B is obtained. In FIG. 3B, a transistor shown on the left side is a p-channel FET 201 and a transistor shown on the right side is an n-channel FET 202.

Further, the passivation film 341 is formed of a silicon nitride film, a silicon oxide film, or a silicon nitride oxide film by plasma CVD. The third interlayer insulating film 342 is formed using an organic resin material to have a thickness 1 to 2 μm. As the organic resin material, polyimide, polyamide, acrylic, benzocyclobutene (BCB), or the like can be used. It is advantageous to use an organic resin film since a method for forming an organic resin film is simple, the parasitic capacitance can be reduced because of low dielectric constant, it is suitable for planarization, and the like. Naturally, an organic resin film other than the one mentioned above may also be used.

According to the present invention, short-channel effects such as a punchthrough and a gate leakage current can be suppressed. Thus, miniaturization of a semiconductor device can be promoted. Further, by the present invention, the distance between a source region and a drain region of an FET, and the width of an extension region can be designed freely. Therefore, by the present invention, the channel length of an FET can be set freely within the range of 5 to 80 nm.

This embodiment mode can be freely combined with Embodiment Mode 1.

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Embodiment Mode 3

A manufacturing method of a semiconductor device of the present invention is described with reference to FIGS. 4A to 7. Embodiment Mode 3 describes an example of employing an SOI (silicon on insulator) substrate in which an insulating layer and a single-crystal semiconductor layer are stacked.

As SOI substrates, for example, a SIMOX (separation by implanted oxygen) substrate can be given. A SIMOX substrate 510 is a substrate which is manufactured by embedding oxygen molecules into a portion slightly deeper than the surface of the single-crystal semiconductor layer, and oxidizing it at a high temperature, thereby forming an insulating layer and a single-crystal semiconductor layer on the insulating layer. The substrate is a stack of a first single-crystal semiconductor layer 511, an insulating layer 512, and a second single-crystal semiconductor layer 513 (FIG. 4A).

A manufacturing method of a semiconductor device of the present invention using a SIMOX substrate 510 is described. A plurality of first elements such as a field effect transistor using, as an active layer, a first single-crystal semiconductor layer 511 which is one surface of the SIMOX substrate 510, are formed. Then, a layer 514 including a second element is formed over the first single-crystal semiconductor layer 511 (FIG. 4B). The second single-crystal semiconductor layer 513, which is an opposite surface to the one surface of the SIMOX substrate 510, is removed by etching (FIG. 4C). Then, a semiconductor device 516 in which the insulating layer 512, the first single-crystal semiconductor layer 511 and the layer 514 including second elements are sequentially stacked, is completed (FIG. 4D).

It is to be noted that the second single-crystal semiconductor layer 513 may be removed by using a grinding and polishing apparatus 515 such as a grind stone, by using an etching agent, or by using both the grinding and polishing apparatus 515 and an etching agent in combination. It is preferable that the second single-crystal semiconductor layer 513 be ground and polished until the second single-crystal semiconductor layer 513 is thinned to a certain degree and then removed by an etching agent until the insulating layer 512 is exposed. If wet etching is employed, the etching

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agent may be, for example, a mixed solution in which fluorinated acid is diluted with water or ammonium fluoride; a mixed solution of fluorinated acid and nitric acid; a mixed solution of fluorinated acid, nitric acid, and acetic acid; a mixed solution of hydrogen peroxide and sulfuric acid; a mixed solution of hydrogen peroxide, ammonia water and water; or a mixed solution of hydrogen peroxide, hydrochloric acid and water. If dry etching is employed, the etching agent may be, for example, a gas containing a halogen atom or molecule such as fluorine, or a gas containing oxygen. It is preferable to use a gas or a liquid containing halogen fluoride or an interhalogen compound. For example, chlorine trifluoride (ClF_3) is preferably used as the gas including halogen fluoride.

The thickness of the second single-crystal semiconductor layer 513 included in the SIMOX substrate 510 ranges from several tens to several hundred μm while that of the first single-crystal semiconductor layer 511 is as small as 0.3 μm or less. Therefore, when the second single-crystal semiconductor layer 513 is removed after forming a plurality of field-effect transistors using the first single-crystal semiconductor layer 511, a small, thin, and lightweight semiconductor device, e.g., an ultra large scale integrated circuit (ULSI), memory devices such as SRAMs, DRAMs, can be provided.

For further explanation, a manufacturing method for forming a field effect transistor as the first element, and a DRAM, which is a memory element, as the second element, is described with reference to FIGS. 5A to 5F and 6.

As shown in FIG. 5A, an inorganic insulating film 614 is formed over the SIMOX substrate in which the first single-crystal semiconductor layer 511, the insulating layer 512 and the second single-crystal semiconductor layer 513 are stacked.

Thereafter, a gate electrode 616 made of a conductive material is formed, and an inorganic insulating film is etched in a self-alignment manner using the gate electrode 616 as a mask to form a gate insulating film 615. At this time, the state shown in FIG. 5B is obtained.

Then, impurities are introduced by a plasma doping method to form a first impurity region 617a, so as to form an extension region. By the plasma doping method, the impurities can be introduced at an extremely shallow level. At this time,

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the state shown in FIG. 5C is obtained.

Thereafter, irradiation of laser light having a fundamental wave and a pulse width of 10 ps or less is carried out to activate the introduced impurities at the extremely shallow level and a high concentration profile (distribution). By the laser irradiation, laser annealing for generating a non linear optical effect (multiphoton absorption) in the irradiated region is conducted. In this way, a first impurity region 617b which is electrically activated is formed. At this time, the state shown in FIG. 5D is obtained.

A silicon nitride film is formed to cover the gate electrode 616, and is anisotropically dry-etched in the film thickness. In this way, as shown in FIG. 5E, the silicon nitride film remaining partially on the side portions of the gate electrode 616 becomes a sidewall 618. The reliability of the field effect transistor is enhanced, because the concentration gradient of the impurities is formed at the end portions of the gate electrode 616 by forming the sidewall 618.

Then, impurities are introduced by an ion doping method to form a second impurity region 619, to form source and drain regions. By the ion doping method, the impurities are injected more deeply than the first impurity region. At this time, the state shown in FIG. 5F is obtained.

Subsequently, the second impurity region 619 is activated. For this activation, laser annealing is conducted with an energy density of about 0.1 to 1 J/cm^2 using a YAG laser or a XeCl laser. Instead of this laser annealing, laser annealing using laser light having a fundamental wave and a pulse width of 10 ps or less can also be conducted.

After a first silicon oxide film 620 is formed by a CVD method, it is planarized by CMP and a contact hole is formed by a photolithography process. The contact hole formed by etching the first silicon oxide film 620 is filled with polysilicon, and a leading terminal (also referred to as a plug) 621 to be in contact with the second impurity region 619 is formed. Plugs 624 and 625 for capacitors are formed at the same time. Then, after a second silicon oxide film 622 is formed over the entire surface, a portion for forming a bit line, is opened. A TiN film and a W film are stacked by a sputtering method and patterned to form a bit line 623. The bit line 623 is

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shared by two memory cells.

In order to form a capacitor over the bit line 623, after a third silicon oxide film 626 and a silicon nitride film 627 are formed by a CVD method, they are planarized by CMP, and a contact hole is formed by a photolithography process. The contact hole formed by etching the third silicon oxide film 626 and the silicon nitride film 627 is filled with polysilicon, and second plugs 628 and 629 for the capacitors, which are to be in contact with the first plugs 624 and 625, are formed.

Thereafter, in order to form a cylindrical capacitor, a fourth silicon oxide film is formed by a CVD method with a film thickness corresponding to the height of the capacitor to be formed. Hole patterns of the capacitors are formed by etching with a photolithography method. The capacitors are designed as largely as possible, but so as not to be in contact with the adjacent capacitors.

A thin polysilicon film is formed by a CVD method over the entire surface including holes of the fourth silicon oxide film. Thereafter, the polysilicon film is selectively removed by an etch-back method to leave the polysilicon film only in the holes, thereby forming a cylindrical electrode (a lower electrode of the capacitor) 630.

In addition, the present invention is not limited to the structure of a memory cell shown in FIG. 6 and a planar type, a stacked type, a trench type may be adopted, for example.

A Ta_2O_5 film and a TiN film are formed by a CVD method, and patterned to form an upper electrode (also referred to as a plate) 631 made of a TiN film. Through the above steps, a memory cell is completed. Further, $BaSrTiO_3$, Si_3N_4, or SiO_2 can be used as a substitute derivative for the Ta_2O_5 film.

A first interlayer insulating film 632 and a second interlayer insulating film 633 is formed, and a CMOS circuit (not shown) formed in the periphery is connected by first and second wirings. The upper and lower wirings are electrically connected to each other by forming the contact hole and the plug.

The CMOS circuit is connected by the first and second wirings. As shown in FIG. 6, only the first and second wirings cross over the memory array. A wiring structure of three wirings, i.e., the bit line, the first wiring, and the second wiring is

formed for a field effect transistor that is in the periphery.

The first wiring is formed with a structure in which a TiN film 634a, and a film 634b mainly containing Al are stacked. In addition, the second wiring is also formed with a structure in which a TiN film 635a, and a film 635b mainly containing Al are stacked.

Annealing is conducted in a hydrogen atmosphere to recover damages caused during the various steps. And a final protective film 636 including a silicon oxide film or a silicon nitride film is formed, and opening is conducted to expose the second wiring in only a bonding pad (a terminal portion connected to a package).

Lastly, the second single-crystal semiconductor layer 513 is ground to become thin. In this way, a DRAM, which a part of its structure is shown in FIG. 6, is formed.

Dicing is conducted to individually isolate chips having a DRAM from a wafer. Then, the chip is picked up from the wafer one by one, and mounted on a lead frame. An electrode terminal of the chip is electrically connected to an inner lead of the lead frame by a gold wire having a diameter of about 20 to 30 μm. Sealing is conducted using a mold resin layer for easy handling. The lead is plated with a solder to prevent the element from rusting. Thereafter, the chips are separated every individual package from the lead frame to form a lead. In this way, packaging is done.

FIG. 7 is a perspective view showing a cross sectional structure of a packaged device. In the structure shown in FIG. 7, a chip 702 is connected to a lead frame 701 by a wire bonding method. In addition, the chip 702 is sealed with the mold resin layer 703. The chip 702 is mounted on the lead frame 701 by an adhesive agent 704 for mounting.

The lead frame 701 is a ball grid array type in which a solder ball 705 is provided. The solder ball 705 is formed on the opposite surface of the lead frame 701, to the surface provided with the chip 702. A wiring 706 provided in the lead frame 701 is electrically connected to the solder ball 705 via a contact hole provided in the lead frame.

In this embodiment mode, the wiring 706 for electrically connecting the chip 702 and the solder ball 705 is provided on the surface of the lead frame 701 provided

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with the chip; however, the lead frame is not limited to this structure. For example, a multilayer wiring may be formed inside the lead frame.

In FIG. 7, the chip 702 and the wiring 706 are electrically connected to each other by a gold wire 707. A semiconductor element is provided for the chip 702, and a pad is provided on the opposite surface of the chip 702, to the surface provided with the lead frame 701. The pad is electrically connected to the semiconductor element. The pad is electrically connected to the wiring 706 provided for the lead frame 701, by the gold wire 707.

This Embodiment Mode can be freely combined with Embodiment Mode 1 or Embodiment Mode 2.

Embodiment Mode 4

Various types of electronic devices can be completed by mounting an IC chip including an FET formed by a laser annealing method of the present invention. Further, an FET is formed as a switching element by a laser annealing method of the present invention, and a reflective electrode connected to the switching element is provided to form a reflective active matrix substrate. A display portion of an electronic device is formed using the reflective active matrix substrate. In this manner, various types of electronic devices can be manufactured.

As such electronic devices, personal computers, game machines, portable information terminals (such as mobile computers, cellular phones, portable game machines, or electronic books), cameras such as video cameras or digital cameras, reflective projectors, navigation systems, audio reproduction devices (such as car audio systems, car audio components), image reproduction devices provided with a memory medium (specifically, a device equipped with an IC chip, and a display by which the content of a memory medium such as a digital versatile disc (DVD) can be reproduced and the image can be displayed), and the like can be completed.

A cellular phone which is one of electronic devices in the present invention is taken as an example. FIG. 8A shows how the electronic device is practically equipped with a package.

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[0120]

A module of the cellular phone shown in FIG. 8A includes a printed wiring board 816 mounted with a CPU 811 stacked over a memory 802, a power supply circuit 803, a controller 829 provided over an audio processing circuit 801, a transmitter-receiver circuit 804, and other elements such as a resistor, a buffer, and a capacitor. Moreover, a panel 800 is mounted on the printed wiring board 816 using an FPC 808. The panel 800 is provided with a pixel portion 805, a scan line driver circuit 806 for selecting a pixel included in the pixel portion 805, a signal line driver circuit 807 for supplying a video signal to the selected pixel.

Supply voltage to the printed wiring board 816 and various signals inputted with a key board are supplied through an interface portion 809 of the printed wiring board in which plural input terminals are disposed. Further, an antenna port 810 which transmits and receives signals between the printed wiring board and an antenna is provided for the printed wiring board 816.

In FIG. 8A, the printed wiring board 816 is mounted on the panel 800 by using an FPC. The present invention is not limited to this structure. A controller 829, a sound processing circuit 801, a memory 802, a CPU 811, or a power supply circuit 803 may be directly mounted on the panel 800 with a COG (Chip on Glass) method.

Further, in the printed wiring board 816, there is a case that capacitance formed between leading wirings and resistance of a wiring itself etc., cause noise to a supply voltage or a signal, or make a rise of a signal dull. Correspondingly, various kinds of elements such as a capacitor element and a buffer are provided over the printed wiring board 816, thereby preventing the noise to the supply voltage or the signal and the dull rise of the signal.

Further, FIG. 8B shows an example of a module equipped with an integrated circuit provided over an FPC.

As shown in FIG. 8B, integrated circuits (a controller 901, a CPU (central processing unit) 902, and a memory 903) are mounted over an FPC 908. A panel 900 is provided with a pixel portion 905 and driver circuits (such as a signal line driver circuit 907 and a scan line driver circuit 906), and an FPC 908 for connecting them to

an external power or the like (not shown) which is provided outside is attached to the panel 900 with an adhesive agent 909. The integrated circuits (the controller 901, CPU 902, and memory 903) using a semiconductor substrate is mounted on the FPC 908; thus, the noise in the supply voltage or the signal and the dull rise of the signal are prevented.

Further, this embodiment can be freely combined with Embodiment Modes 1 to 3.

Embodiment Mode 5

An IC chip in which an FET formed by a laser annealing method of the present invention is integrated, can be used as a thin film integrated circuit or a noncontact thin film integrated circuit device (also referred to as a wireless IC tag or RFID (radio frequency identification)).

FIG. 9 shows an example of an ID card in which an IC chip 1516 of the present invention is attached to a card-like substrate 1518 provided with a conductive layer 1517 which serves as an antenna. Thus, the IC chip 1516 of the present invention is small, thin, and lightweight, so that diverse uses can be realized and it does not spoil the design of an article even when it is attached to the article.

An IC chip 1516 of the present invention is not limited to the case of being attached to the card-like substrate 1518, and it can be attached to an article having a curved surface, or various shapes. For example, the IC chips can be used in bill, money, coin, securities, bearer bonds, certificates (such as a driver's license, or a resident's card, packing cases (such as a wrapper or a bottle), memory media (such as a DVD, a video tape), vehicles (such as a bicycle), belongings (such as a bag, or glasses), food, clothing, commodities, and the like.

This embodiment mode can be freely combined with Embodiment Mode 1 to 4.

Embodiment Mode 6

Various types of electronic devices can be formed by mounting an IC chip using an FET formed by a laser annealing method of the present invention. Specific

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examples thereof are described with reference to FIGS. 10A to 10E.

FIG. 10A shows a display device including a casing 1901, a support 1902, a display portion 1903, speaker portions 1904, a video input terminal 1905 and the like. The display device is manufactured using an FET formed by the manufacturing method described in the above mentioned embodiment mode for a driver IC. As the display devices, liquid crystal display devices, light emitting devices and the like are given, and the category of such display devices includes all types of display devices for information display, for example, display devices for a computer, a TV receiving, and an advertising display.

FIG. 10B shows a computer including a casing 1911, a display portion 1912, a keyboard 1913, an external connection port 1914, a pointing mouse 1915, and the like. By forming a FET with the manufacturing method shown in the above mentioned embodiment mode, the thus formed FET can be applied to a CPU or a memory inside the main body, and the like.

FIG. 10C shows a cellular phone, which is a typical example of mobile information terminal. The cellular phone includes a casing 1921, a display portion 1922, a sensor portion 1924, operation keys 1923, and the like. The sensor portion 1924 has an optical sensor element, and the amount of consumption current of the cellular phone can be suppressed by controlling the brightness of the display portion 1922 based on the illumination intensity obtained by the sensor portion 1924, or by conducting the lighting control of the operation keys 1923 corresponding to the illumination intensity obtained by the sensor portion 1924. In addition, in the case of a cellular phone having an imaging function such as a CCD or the like, whether a person who takes a picture looks in an optical finder or not is detected, as the amount of light changes, which is received by a sensor of the sensor portion 1924 provided in the vicinity of the optical finder. In the case where a person who takes a picture looks in the optical finder, the amount of electric power consumption can be suppressed by making off the display portion 1922.

The display screen of an electronic device such as the above mentioned cellular phone, a PDA (Personal Digital Assistants), a digital camera, or a compact game

machine, is small, since these electronic devices are each a mobile information terminal. Therefore, by forming functional circuits such a CPU, a memory, a sensor with using an FET shown in the above mentioned embodiment mode, electronic devices can be smaller and lighter.

Moreover, distribution route of electronic devices can be made clear by attaching IC tags to various types of electronic devices. FIG. 10D shows a state in which a wireless IC tag 1942 is attached to a passport 1941. The wireless IC tag may be embedded in the passport 1941. In the same manner, the wireless IC tag can be attached to or embedded in driver's licenses, credit cards, bills, coins, securities, gift certificates, tickets, traveler's checks (T/C), insurances, residence certificates, family registers, and the like. In this case, only the information showing the real one is inputted into the wireless IC tag and an access right is set to prevent illegal reading or writing of information. This can be realized by using a memory shown in another embodiment mode. By using such a tag in this manner, it is possible to distinguish a counterfeit from the real one.

In addition to the above, the wireless IC tag can also be used as a memory. FIG. 10E shows an example in which the wireless IC tag 1951 is attached to a label attached to a vegetable wrapping. Also, the wireless IC tag may be attached to or embedded in the wrapping itself. The wireless IC tag 1951 can record process of commodity circulation, price, numerical quantity, use application, shape, weight, expire date, various identification information, etc, and stages of a production process such as place of production, producer, date of manufacture, processing method, etc. The information from the wireless IC tag 1951 is read by receiving it with an antenna portion 1953 of a reader 1952, and displaying the information on a display portion 1954 of the reader 1952. Thus, the information can be easily known by a dealer, a retail seller, and a consumer. In addition, by providing the access right to each producer, trader, and consumer, it is set so that a person who does not have an access right cannot read, write, change or erase information.

Further, the wireless IC tag can be used as follows. In stores, the information that payment has been made is written in the wireless IC tag, and whether payment has

been made or not is checked at a provided checking device at an entrance. If people leave the stores without payment, an alarm rings. By this method, forgetting payment or shoplifting can be prevented.

In considering the privacy protection of customers, the following methods are possible. Either of the methods is employed when the payment is made: (1) the data inputted in the wireless IC tag is locked with a code number etc.; (2) the data itself inputted in the wireless IC tag is encrypted; (3) the data inputted in the wireless IC tag is erased; or (4) the data inputted in the wireless IC tag is destroyed. These methods can be realized by using a memory described in the above described embodiment modes. A checking device is provided at an entrance, and whether or not either of the processes (1) to (4) is conducted, or whether nothing is done in the data in the wireless IC tag is checked, in order to check whether payment has been made. In this manner, it is possible to check whether payment has been made in stores, and it can prevent the information in the wireless IC tag from being read without the holder's intention outside of stores.

According to the present invention, a short channel effect can be suppressed and further miniaturization can be done; therefore, an IC chip provided for a wireless IC tag can be miniaturized. As IC chips become smaller, the strength against impacts is more increased. Thus, the reliability of IC chips is enhanced. By a laser annealing method of the present invention, all types of wireless IC tags can be formed with high quality and without variations in performance.

As described above, the application range of a semiconductor device manufactured according to the present invention is extremely wide, and a semiconductor device formed according to the preset invention can be applied to electronic devices in various fields.

The present invention can be freely combined with Embodiment Modes 1 to 5.

INDUSTRIAL APPLICABILITY

According to the present invention, a non-linear optical device for converting a wavelength is not needed, and a laser beam having an extremely high output power can

be used for activation. Accordingly, the width of a region which can be activated by one-time laser scanning can be made larger, and thus the productivity can be increased dramatically.

According to the present invention, a semiconductor integrated circuit can be more miniaturized and thus, high integration of an IC can be developed. In addition, according to the present invention, the number of chips which are obtained from one wafer can be increased.

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CLAIMS

1. A manufacturing method of a semiconductor device, comprising the steps of:

selectively injecting impurities into a semiconductor substrate to form an impurity region;

processing a laser beam having a fundamental wave into a long beam on a surface of the impurity region; and

moving the surface of the impurity region relatively to the long beam to scan the laser beam to activate the impurity region.

2. A manufacturing method of a semiconductor device, comprising the steps of:

forming a gate insulating film over a semiconductor layer of an SOI substrate;

forming a gate electrode over the gate insulating film;

selectively injecting impurities into the semiconductor layer of the SOI substrate to form an impurity region;

processing a laser beam having a fundamental wave into a long beam on a surface of the impurity region; and

moving the surface of the impurity region relatively to the long beam to scan the laser beam to activate the impurity region.

3. The manufacturing method of a semiconductor device according to claim 1 or 2, wherein the impurity region is source and drain regions of a field effect transistor.

4. The manufacturing method of a semiconductor device according to claim 1 or 2, wherein the impurity region is an extension region of a field effect transistor.

5. The manufacturing method of a semiconductor device according to any one of claims 1 to 4, wherein the laser beam having a fundamental wave is oscillated with a pulse width of 1 femtosecond or more and 10 picoseconds or less.

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6. The manufacturing method of a semiconductor device according to any one of claims 1 to 5, wherein the laser beam having a fundamental wave is emitted from one kind of lasers in which one or more of Nd, Yb, Cr, Ti, Ho and Er, is/are added as a dopant into a crystal of Sapphire, YAG, ceramics YAG, ceramicsY_2O_3, KGW, KYW, Mg_2SiO_4, YLF, YVO_4, or $GdVO_4$.

7. The manufacturing method of a semiconductor device according to any one of claims 1 to 6, wherein the laser beam is pulsed laser light with a repetition rate of 10MHz or more.

8. A semiconductor device having an integrated circuit including a field effect transistor, comprising:

a gate insulating film formed over a semiconductor layer;

a gate electrode provided over the gate insulating film;

a channel forming region formed in the semiconductor layer under the gate electrode through the gate insulating film;

an extension region into which an n-type or p-type impurity element is added, and which is located on opposite sides of the channel forming region; and

a source region and a drain region which are in contact with the extension region,

wherein the extension region is has a junction depth shallower than the source region and the drain region; and

wherein a length of the channel forming region is 5 nm or more and 80 nm or less.

9. The semiconductor device according to claim 8, the length of the channel forming region is equal to a width of the gate electrode.

10. The semiconductor device according to claim 8 or 9, wherein the integrated circuit includes at least one of a controller, a CPU and a memory.

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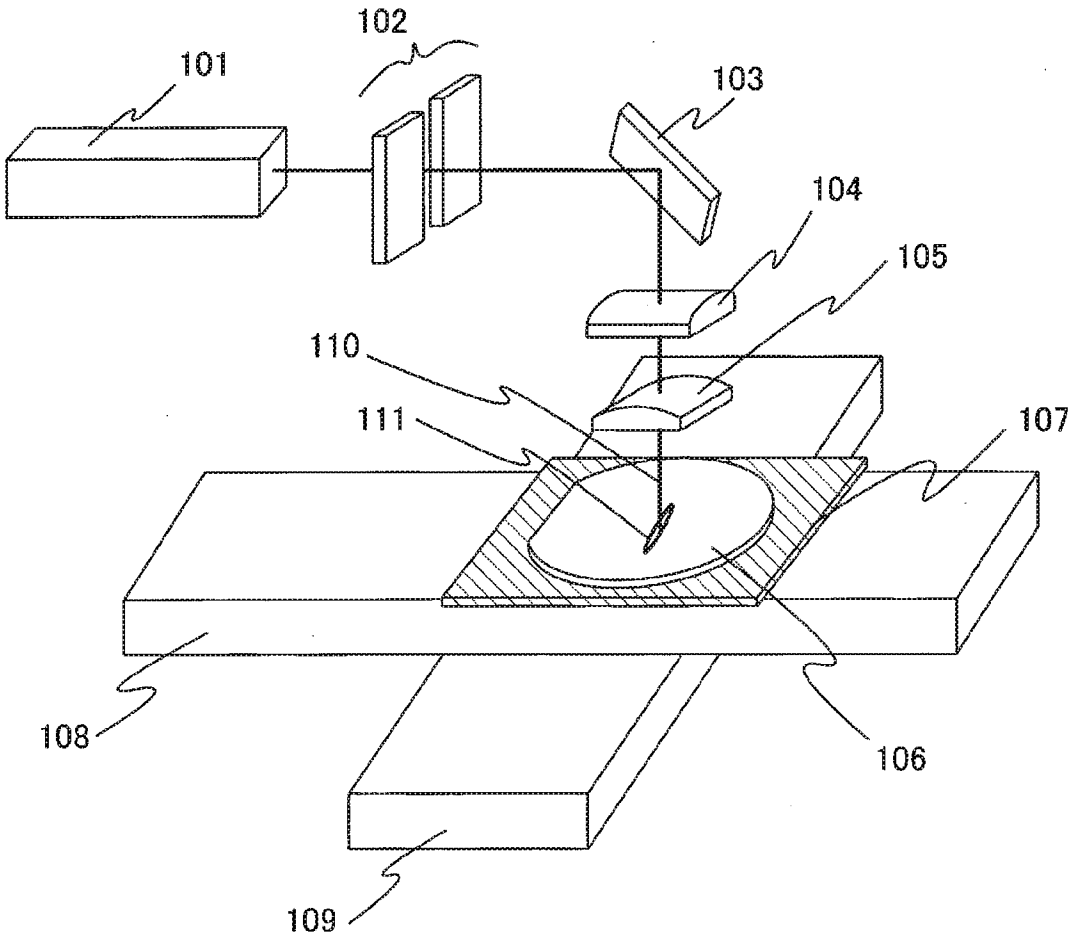


FIG. 1

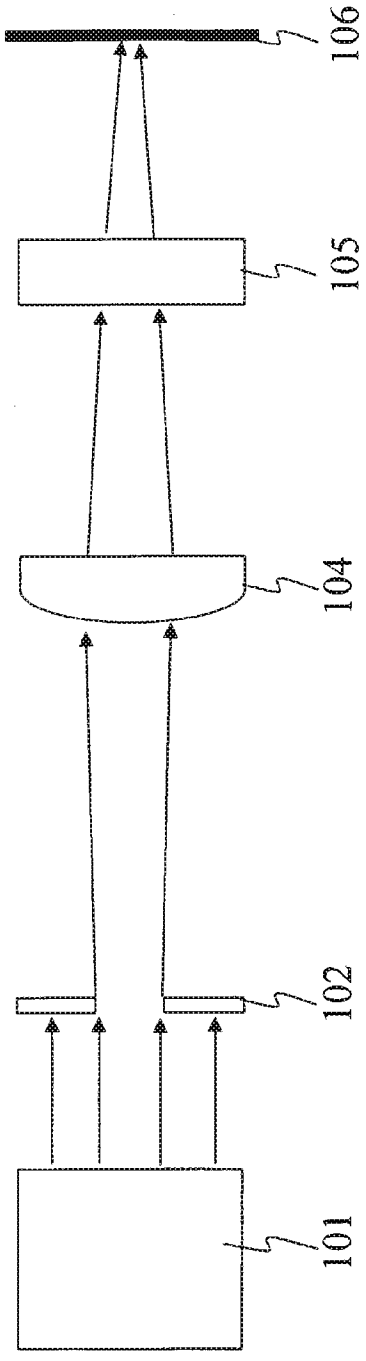


FIG. 2A

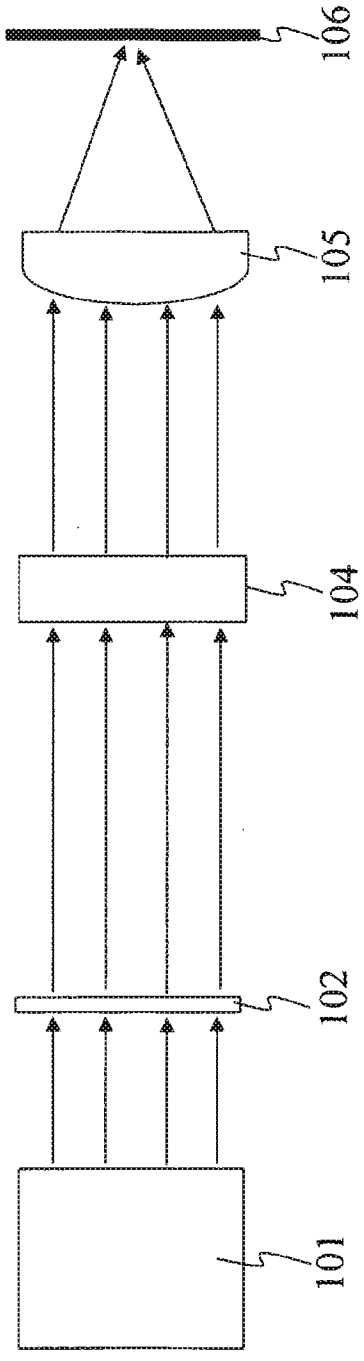


FIG. 2B

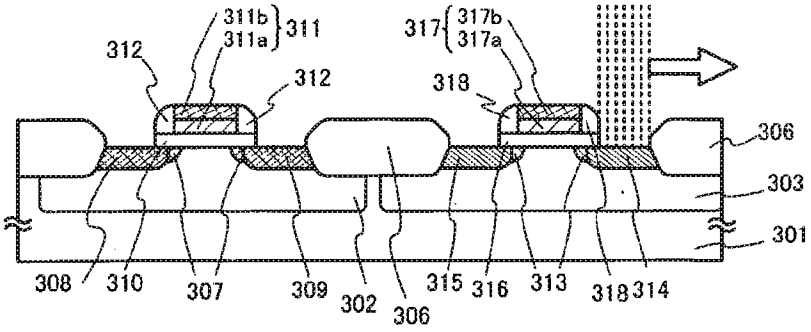

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FIG. 3A

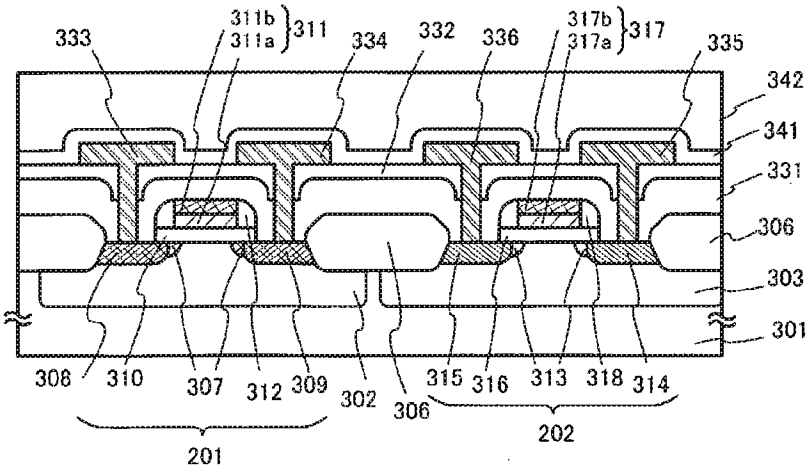

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FIG. 3B

FIG. 4A

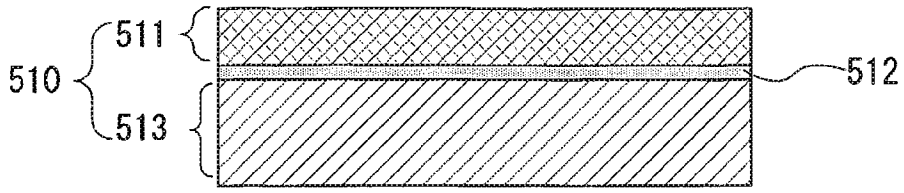


FIG. 4B

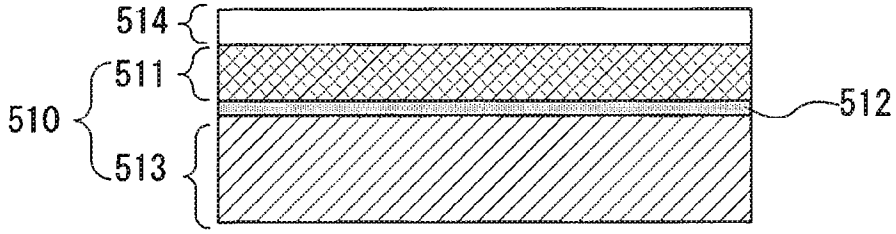


FIG. 4C

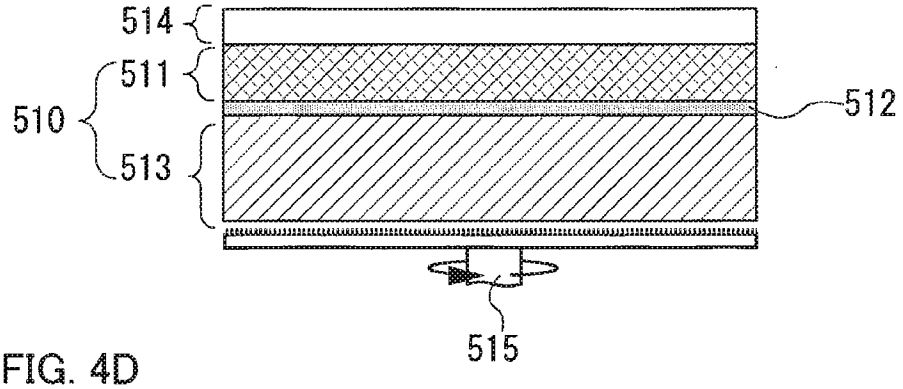


FIG. 4D

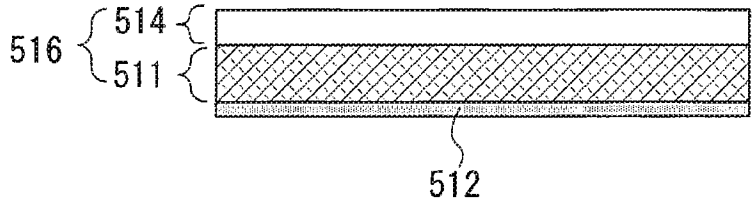


FIG. 5A

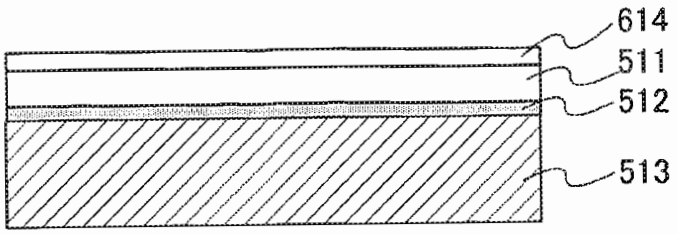


FIG. 5B

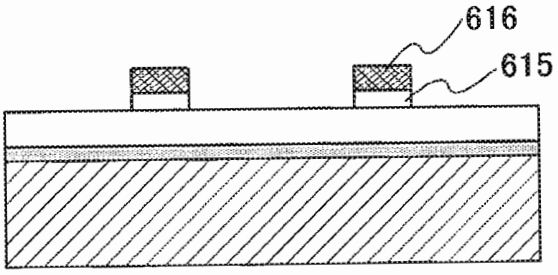


FIG. 5C

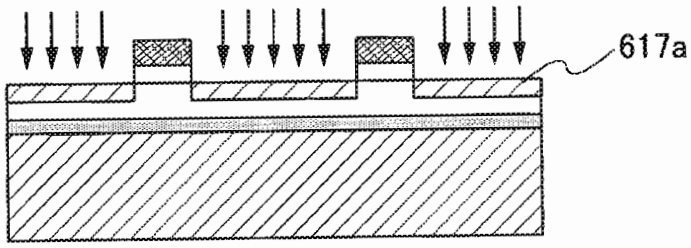


FIG. 5D

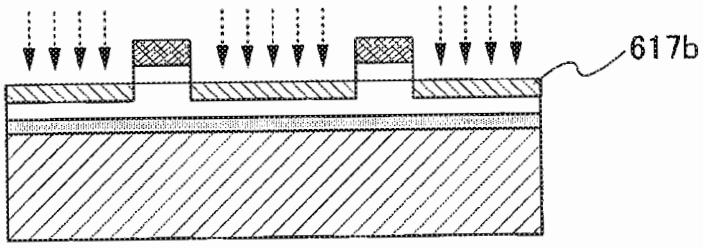


FIG. 5E

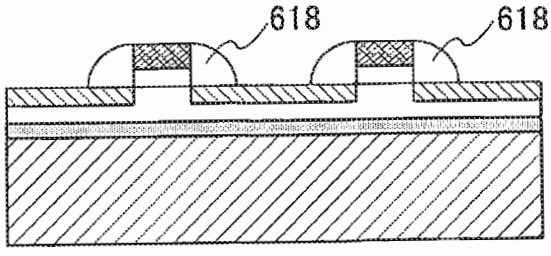
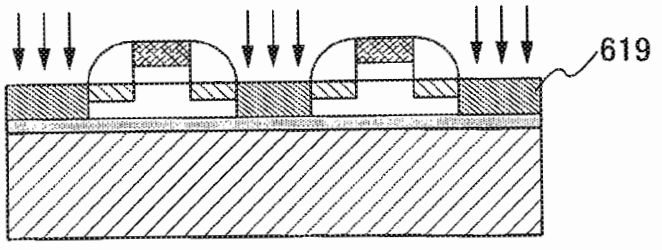


FIG. 5F



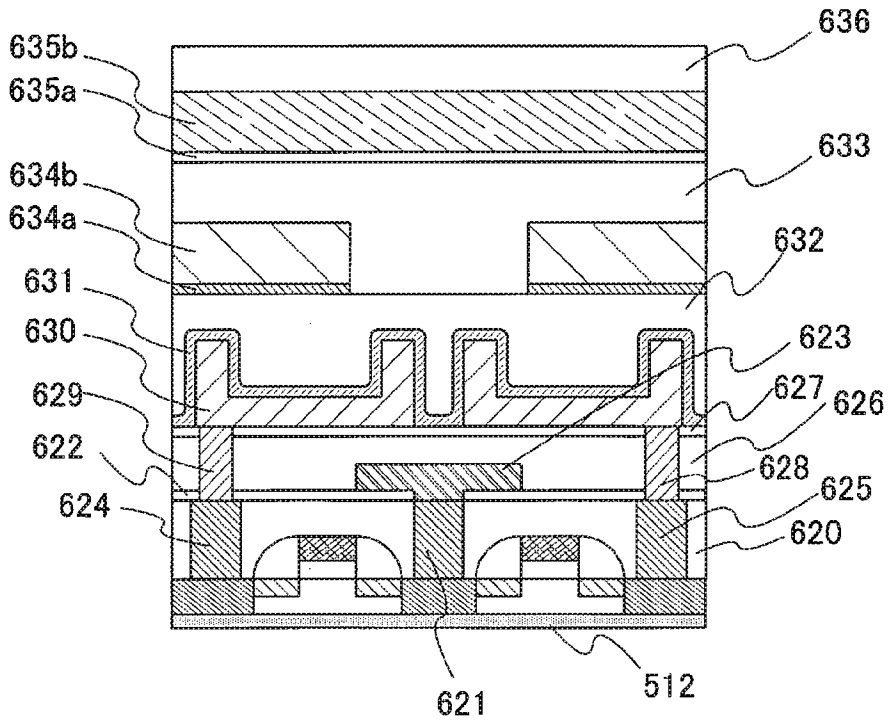

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FIG. 6

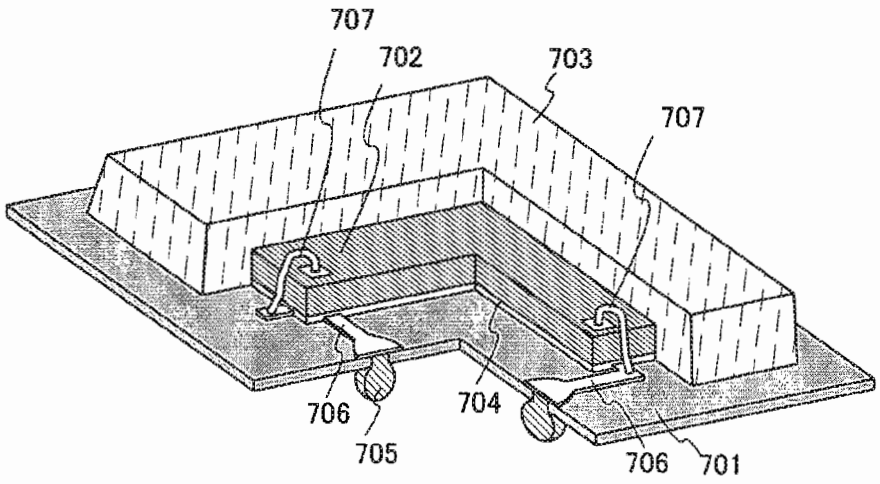


FIG. 7

FIG. 8A

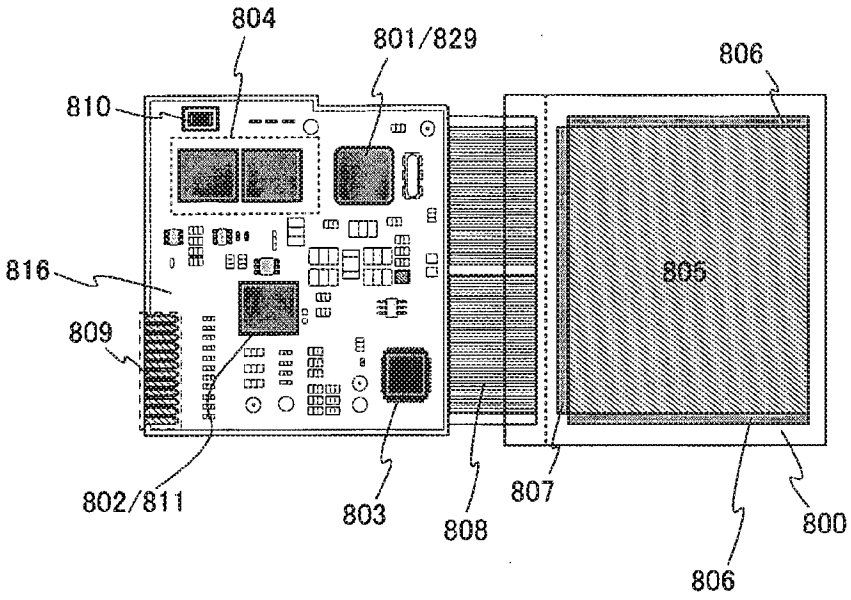
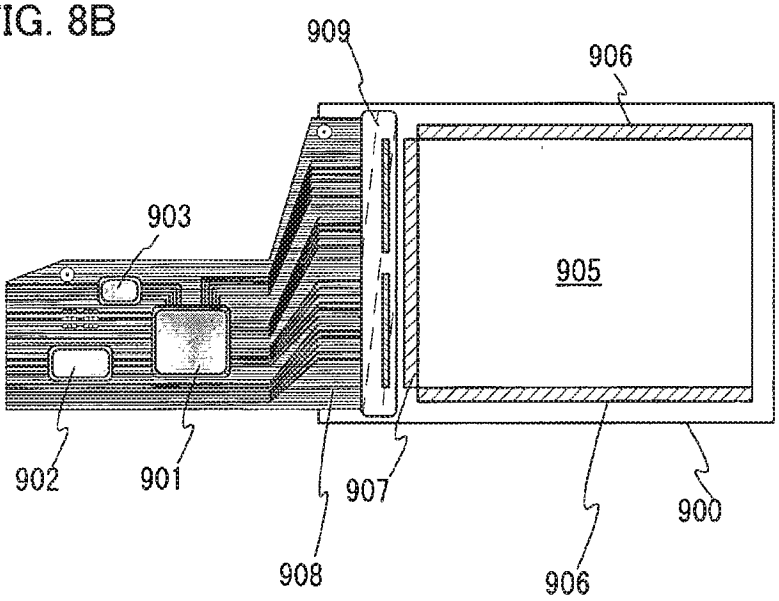

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FIG. 8B


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906

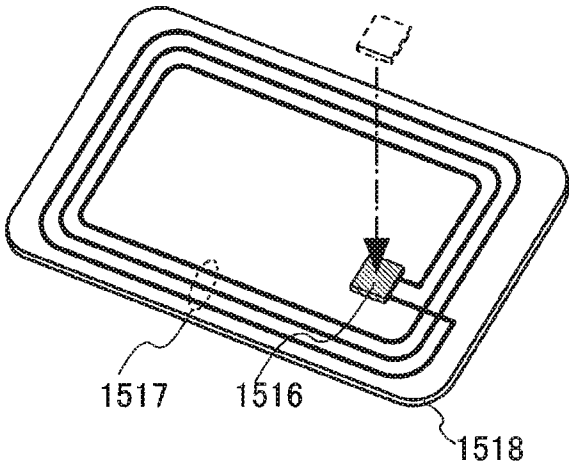


FIG. 9

FIG. 10A

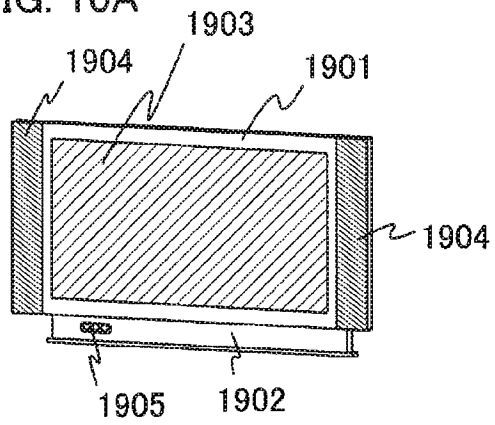


FIG. 10B

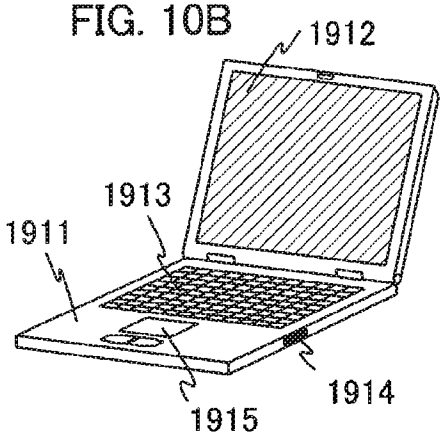


FIG. 10C

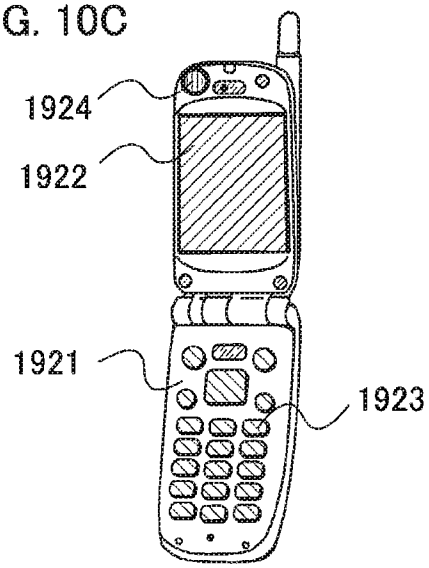


FIG. 10D

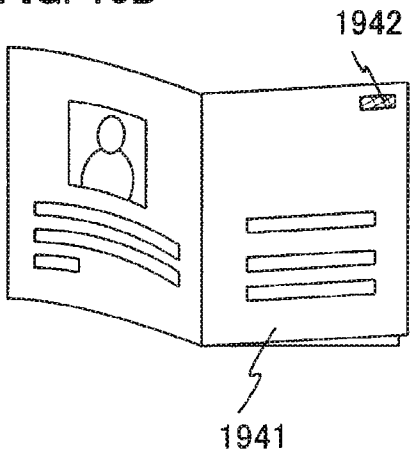
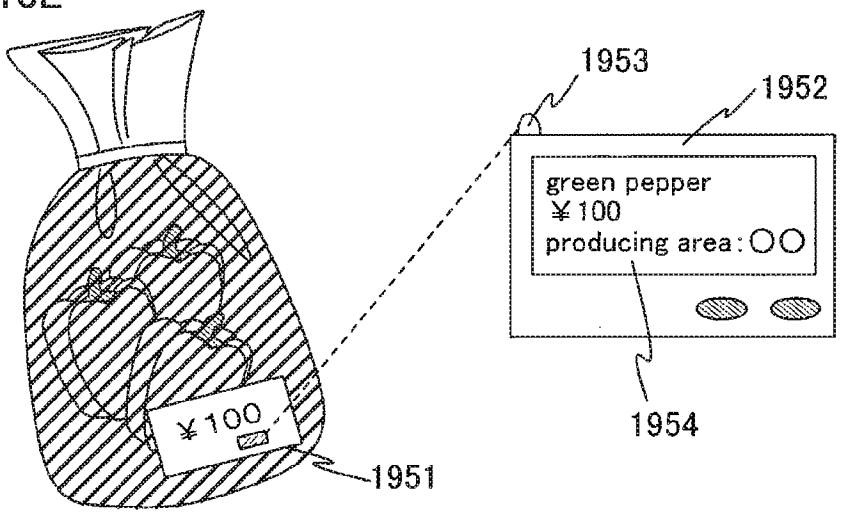


FIG. 10E



EXPLANATION OF REFERENCE

101: laser oscillator, 102: slit, 103: mirror, 104: first cylindrical lens, 105: second cylindrical lens, 106: semiconductor substrate, 107: substrate fixing stage, 108: X stage, 109: Y stage, 110: laser beam, 111: beam irradiation region, 201: p-channel FET, 202: n-channel FET, 301: substrate, 302: n-well, 303: p-well, 306: field oxide film, 307: extension region, 308: source region, 309: drain region, 310: gate insulating film, 311: gate electrode, 311a: polysilicon layer, 311b: silicide layer, 312 :sidewall, 313: extension region, 314 :source region, 315: drain region, 316: gate insulating film, 317: gate electrode, 317a: polysilicon layer, 317b: silicide layer, 318: sidewall, 331: first interlayer insulating film, 332: second interlayer insulating film, 333: source electrode, 334: drain electrode, 335: source electrode, 336: drain electrode, 341: passivation film, 342: third interlayer insulating film, 510: SIMOX substrate, 511: first single-crystal semiconductor layer, 512: insulating layer, 513: second single-crystal semiconductor layer, 514: layer including second element, 515: grinding and polishing apparatus, 516: semiconductor device, 614: inorganic insulating film, 615: gate insulating film, 616: gate electrode, 617a: first impurity region, 617b: first impurity region, 618: sidewall, 619: second impurity region, 620: first silicon oxide film, 621: leading terminal, 622: second silicon oxide film, 623: bit line,, 624: plug, 625: plug, 626: third silicon oxide film 627: silicon nitride film, 628: plug, 629: plug, 630: electrode, 631: upper electrode, 632: first interlayer insulating film, 633: second interlayer insulating film, 634a: TiN film, 634b: film mainly containing Al, 635a: TiN film, 635b: film mainly containing Al, 636: final protective film, 701: lead frame, 702: chip, 703: mold resin layer, 704: adhesive agent, 705: solder ball, 706: wiring, 707: gold wire, 800: panel, 801: sound processing circuit, 802: memory, 803: power supply circuit, 804: transmitter-receiver circuit, 805: pixel portion, 806: scan line driver circuit, 807: signal line driver circuit, 808: FPC, 809: interface portion, 810: antenna port, 811: CPU, 816: printed wiring board, 829: controller , 900: panel, 901: controller, 902: CPU, 903: memory, 905: pixel portion, 906: scan line driver circuit, 907: signal line driver circuit, 908: FPC, 909:

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adhesive agent, 1516: IC chip, 1517: conductive layer, 1518: card-like substrate, 1901: casing, 1902: support, 1903: display portion, 1904: speaker portion, 1905: video input terminal, 1911: casing, 1912: display portion, 1913: keyboard, 1914: external connection port, 1915: pointing mouse, 1921: casing, 1922: display portion, 1923: operation key, 1924: sensor portion, 1941: passport, 1942: wireless IC tag, 1951: wireless IC tag, 1952: reader, 1953: antenna portion, 1954: display portion

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2005/021397

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. ***H01L21/265*** (2006.01), ***H01L21/336*** (2006.01), ***H01L29/786*** (2006.01), ***H01L29/78*** (2006.01),

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L 21/265

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2006
Registered utility model specifications of Japan 1996-2006
Published registered utility model applications of Japan 1994-2006

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2001-308344 A (SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.) 2001.11.02,whole document,Fig 1-5 (Family:none)	1-10
X	JP 2004-158627 A (KABUSIKIGAISYA RUNESASUTEKUNOROJI) 2004.06.03,whole document,Fig 1-39 & US 2004/87118 A1	1-10
X	JP 2001-338894 A (MATSUSITA DENKISANGYOU KABUSIKIGAISYA) 2001.12.07,whole document,Fig 1-5 (Family:none)	1-10

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20.01.2006	07.02.2006

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	4L 9277 SONOKO MIYAZAKI Telephone No. +81-3-3581-1101 Ext. 3498

Form PCT/ISA/210 (second sheet) (April 2005)

SAMSUNG EX. 1002 - 472/1684

INTERNATIONALSEARCHREPORT

International application No.
PCT/JP2005/021397

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	JP 2002-246601 A (SEIKOEPUSON KABUSIKIGAISYA) 2002.08.30 ,whole document,Fig 1-6 & US 2002/175372 A1	1-10

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International application No.
PCT/JP2005/021397

Continuation of International Patent Classification(IPC) or both national classification and IPC

H01L21/8234 (2006.01), ***H01L27/088*** (2006.01), ***H01L21/8242*** (2006.01), ***H01L27/108*** (2006.01)

SAMSUNG EX. 1002 - 474/1684

Electronic Acknowledgement Receipt

EFS ID:	34705805
Application Number:	15614256
International Application Number:	
Confirmation Number:	4345
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	136549
Filer:	Andrew W. Schultz
Filer Authorized By:	
Attorney Docket Number:	143705.06021
Receipt Date:	28-DEC-2018
Filing Date:	05-JUN-2017
Time Stamp:	14:30:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	CN101053065A.pdf	2401415 366bad80ae187b5f62e375d2860f396ca162fd5f	no	15

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2	Foreign Reference	EP1347670A1.pdf	2696909 8938299052b46d52a1b6e35c33c0b33124f225d8	no	18
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3	Foreign Reference	JP1994-244444.pdf	1558265 a14f144025f9bc06615db876844af30a8469f7bf	no	18
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4	Foreign Reference	JP2002-190386A.pdf	2464456 d9cfbe878f2b93e2926d1d26f0620ecea61a4ca8	no	12
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5	Foreign Reference	JPH06267868A.pdf	540319 8cd88915f9c2c2f7466ed4ca50b16d7de701be1d	no	7
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6	Foreign Reference	WO0131842A3.pdf	847765 16da6f73344fad38193d6f5a734842ae488fd2e9	no	8
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7	Foreign Reference	WO0135601A1.pdf	9506152 30146e0f7eadf272e37fd95ed72a22f14b1d09df	no	89
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8	Foreign Reference	WO2005029599A2.pdf	6827765 e9d3ec9025e1e8f46437d9933d620505bbe683dc	no	52
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9	Foreign Reference	WO2006043690A1.pdf	10570883 a6ea3203a998761e22cf8082468097a67364561f	no	84
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Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	15/614,256
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	06-05-2017
				First Named Inventor:	Homayoon Haddad
				Group Art Unit:	2895
(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
Sheet	1	of	6	Attorney Docket No.:	143705.06021(H)

(a) U. S. PATENT DOCUMENTS						
Examiner's Initials	**Cite No.**	**U.S. Patent Document** Number Kind Code (if known)	**Name of Patentee or Applicant of Cited Document**	**Date of Publication of Cited Document MM-DD-YYYY**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	
	A1	4105955	Hayashi	8/8/1978		
	A2	4181538	Narayan et al.	1/1/1980		
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Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	15/614,256
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	06-05-2017
				First Named Inventor:	Homayoon Haddad
				Group Art Unit:	2895
(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
Sheet	2	of	6	Attorney Docket No.:	143705.06021(H)

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	A77	20170141258	McFarland	5/18/2017		

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	15/614,256
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	06-05-2017
				First Named Inventor:	Homayoon Haddad
				Group Art Unit:	2895
(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
Sheet	3	of	6	Attorney Docket No.:	143705.06021(H)

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Examiner's Initials	Cite No.	Foreign Patent Document Number Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear			T
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Examiner Signature		Date Considered	

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Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	15/614,256
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	06-05-2017
				First Named Inventor:	Homayoon Haddad
				Group Art Unit:	2895
(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	06-05-2017
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(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
Sheet	6	of	6	Attorney Docket No.:	143705.06021(H)

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Electronic Acknowledgement Receipt

EFS ID:	34706170
Application Number:	15614256
International Application Number:	
Confirmation Number:	4345
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	136549
Filer:	Andrew W. Schultz
Filer Authorized By:	
Attorney Docket Number:	143705.06021
Receipt Date:	28-DEC-2018
Filing Date:	05-JUN-2017
Time Stamp:	14:31:58
Application Type:	Utility under 35 USC 111(a)

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File Listing:

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Homayoon Haddad *et al.*	Confirmation No.: 4345
Application No.: 15/614,256	Art Unit: 2895
Filed: June 5, 2017	Examiner: Everhart, Caridad
For: SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

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I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

December 28, 2018 — Dated

Electronic Signature: /Andrew W. Schultz/
Andrew W. Schultz, Reg. No. 66,869

INFORMATION DISCLOSURE STATEMENT (IDS) TRANSMITTAL LETTER

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached substitute for PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing of a first office Action after the filing of a request for continued examination (37 CFR 1.97(b)(4)). A certification statement pursuant to 37 C.F.R. 1.97(e) is not submitted herewith.

In accordance with 37 CFR 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications. Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 CFR 1.98(a)(2). In accordance with 37 CFR 1.98(d), copies of foreign patents and non-patent literature that were previously cited in U.S. Patent

Application Nos. 14/084,392 and 14/884,181, to which the instant application claims priority, have not been submitted herewith. In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in § 1.56(b).

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) t our Deposit Account No. 50-0436, under Order No. 143705.06021.

Dated: December 28, 2018

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SAMSUNG EX. 1002 - 498/1684

Espacenet

Bibliographic data: CN101241923 (A) — 2008-08-13

Image sensor semiconductor device

Inventor(s): SHINE CHUNG [CN] ± (CHUNG SHINE, ; WANG WEN-DE, ; YAUNG DUN-NIAN, ; HSU TZU-HSUAN)

Applicant(s): TAIWAN SEMICONDUCTOR MFG [CN] ± (TAIWAN SEMICONDUCTOR MFG, ; TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD)

Classification: - international: ***H01L27/146***
- cooperative: **H01L27/14625**; **H01L27/14632**; **H01L27/14687**

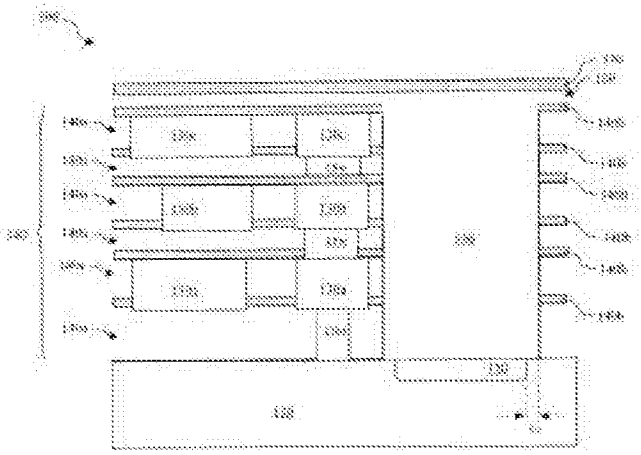
Application number: CN20071127069 20070628

Priority number(s): US20070672681 20070208

Also published as: CN101241923 (B) JP2008198971 (A) US2008191296 (A1) US7803647 (B2)

Abstract of CN101241923 (B)

The present disclosure provides an image sensor semiconductor device. The semiconductor device includes a sensor element disposed in a semiconductor substrate; an inter-level dielectric (ILD) disposed on the semiconductor substrate; and a trench disposed in the ILD, overlying and enclosing the sensor element, and filled with a first dielectric material.



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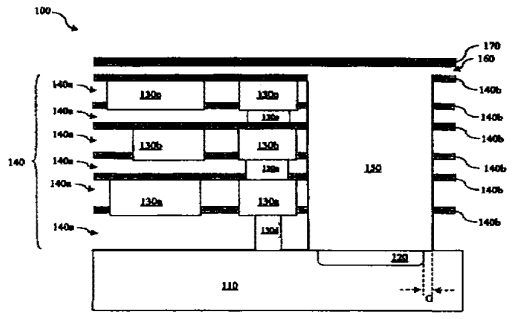
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[54] 发明名称

图像传感器半导体器件

[57] 摘要

本发明公开了一种图像传感器半导体器件。此半导体器件包括传感组件，置于半导体基板内；层间介电材料(ILD)，置于半导体基板上；以及沟槽，置于 ILD 内，覆盖并包围传感组件，且填充有第一介电材料。



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1. 一种图像传感器半导体器件，包括:

传感组件，置于半导体基板内;

层间介电材料，置于该半导体基板上；以及

沟槽，置于该层间介电材料内，该沟槽覆盖并包围该传感组件且填充有第一介电材料。

2. 如权利要求 1 所述的器件，其特征在于，该沟槽更内衬第二介电材料。

3. 如权利要求 2 所述的器件，其特征在于，该第一介电材料包括折射率高于该第二介电材料的介电材料。

4. 如权利要求 2 所述的器件，其特征在于，该第二介电材料包括一含氮材料。

5. 如权利要求 2 所述的器件，其特征在于，该第二材料的厚度范围约在 50～500 埃之间。

6. 如权利要求 1 所述的器件，其特征在于，该第一介电材料包括介电材料可被从待成像物体朝向该传感组件的可见光所穿透，其中该可见光的波长范围在约 300～800 nm 之间。

7. 如权利要求 1 所述的器件，其特征在于，该第一介电材料包括折射率高于该层间介电材料的介电材料。

8. 如权利要求 1 所述的器件，其特征在于，该第一介电材料包括氧化硅。

9. 如权利要求 1 所述的器件，其特征在于，该第一介电材料包括多膜结构。

10. 如权利要求 1 所述的器件，其特征在于，该层间介电材料包括掺杂氟化物的硅化玻璃或掺杂碳的氧化硅。

11. 如权利要求 1 所述的器件，其特征在于，该传感组件包括互补式金属氧化物半导体图像传感器、电荷耦合器件传感器或有源图象素传感器。

12. 如权利要求 1 所述的器件，其特征在于，通过俯视，该传感组件位于该沟槽内，具有至少 0.1 微米的偏距。

13. 如权利要求 1 所述的器件，其特征在于，还包括置于该层间介电材料内的多个金属特征，每一金属特征的临界尺寸实质地小于约 0.25 微米。

14. 如权利要求 1 所述的器件，其特征在于，该传感组件的尺寸范围在约 0.5～5 微米之间。

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图像传感器半导体器件

技术领域

本发明涉及一种图像传感器半导体器件，具体地涉及改进高等互补式金属氧化物半导体（CMOS）成像器中多介电层结构的光传播。

背景技术

图像传感器是含若干形成在半导体基板上的传感组件或图象素的集成电路器件。传感组件用来感应投向半导体基板的大量暴露光。由于集成电路类型的多，随着半导体技术的发展而有改进图像传感器的需要。半导体技术的常规发展是在一或多导电层中采用铜。例如，高等半导体技术中互连金属使用铜，它可于金属层间介电层（inter-metal dielectric layers）之间增加各种蚀刻终止层与阻挡层，以防止铜迁移到附近的氧化硅介电材料中。氮化硅已广泛用作阻挡层和终止层。然而，氮化硅与氧化硅之间的折射率差异将引起光干涉，从而导致改变或降低图像传感器的性能。

发明内容

因此，本本发明提供一种图像传感器半导体器件。该器件包含置于半导体基板内的传感组件；置于半导体基板上的层间介电材料（ILD）以及置于ILD内的沟槽，该沟槽覆盖并包围住传感组件并填充有第一介电材料。

在一些实施例中，沟槽进一步与内衬第二介电材料。第一介电材料可包含折射率高于第二介电材料的介电材料。第二介电材料可包含含氮材料。第二材料的厚度范围可在约50~500埃之间。

在一些实施例中，第一介电材料包含可使从成像物体朝传感组件方向的可见光透射的介电材料。可见光的波长范围在约 300~800nm 之间。第一介电材料可包含折射率高于ILD的介电材料。

在一些实施例中，第一介电材料包含氧化硅。第一介电材料可包含多膜结构。第一介电材料可与传感组件接触。ILD可包含掺杂氟化物的硅酸盐玻璃（FSG）。ILD可包含掺杂碳的氧化硅。

在一些实施例中，传感组件包含互补式金属氧化物半导体（CMOS）图像传感器。传感组件可包含电荷耦合器件传感器。传感组件可包含有源图象

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素传感器。传感组件可包含无源图象素传感器。通过俯视，传感器组件可在沟槽内，并具有至少约 0.1 微米的偏距（offset）。该器件可进一步地包含置于 ILD 内的若干金属特征，每一金属特征的临界尺寸实质地小于约 0.25 微米。传感组件的尺寸范围可在约 0.5 微米至 5 微米之间。

本本发明还提供制造半导体器件的方法。该方法包含在半导体基板内形成传感组件；在半导体基板上形成层间介电材料（ILD），及多层互连（MLI）置于该 ILD；在 ILD 内形成开口，其中，该开口包围该传感组件；用介电材料填充该开口；以及对该开口内的介电材料实施抛光工艺。

在一些实施例中，本方法进一步包含在开口填充之前，在开口内形成衬垫。填充开口可包括使用折射率高于该衬垫的介电材料。在另一实施例中，填充开口包括使用折射率高于该 ILD 的介电材料。

在另一实施例中，图像传感器半导体器件包含：置于半导体基板内的传感组件；置于该半导体基板上的层间介电材料（ILD）；以及置于 ILD 内的沟槽，覆盖并接触传感组件，且用第一介电材料填充。

在一些实施例中，第一介电材料包含一种材料，其可为成像光所透射并作为成像光的波导。第一介电材料可包含具有高折射率的材料，被具有低折射率的材料所包围，用来对成像光全反射。第一介电材料可包含玻璃。

附图说明

本发明所揭示的各种态样可通过以下详细描述并结合附图而获得最佳的理解。值得强调的是，附图的尺寸及比例未必按照此技艺中的标准实务来绘制。事实上，为清楚讨论，不同特征的尺寸可任意地增加或减小。

图 1 是依照本发明所揭示的态样，例示一实施例的半导体器件的剖面图；

图 2 是依照本发明所揭示的态样，例示制造图 1 所示半导体器件的实施例的方法流程图；

图 3 是依照本发明所揭示的态样，例示图 1 所示的实施例的半导体器件的俯视图；

图 4 是依照本发明所揭示的态样，例示所构建的另一实施例的半导体器件剖面图。

具体实施方式

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将要理解的是，本揭示提供许多不同的实现方式或实例，它们将获利自本发明。下列将描述各组件及装配的具体实例，以简化本揭示。当然，它们仅为实例性而不意图是限制性。此外，本发明所揭示可在不同实例中重复使用各标号和/或字母。这种重复使用仅是为了简洁或清楚的目的，其本身不代表被讨论的实例和/或构造之间的关系。而且本说明中，第一特征形成于随后的第二特征上或之上，可包含第一与第二特征以直接接触方式而形成的实例，也可包含附加特征介入第一及第二特征而形成的实例，这样一来，第一与第二特征可不直接接触。

参考图 1 与图 2，以下将分别叙述具有图像传感组件的半导体器件 100 及其制造方法 200。图 1 是半导体器件 100 的实施例的剖面图，图 2 是一实施例的方法 200 的流程图。

方法 200 开始于步骤 210，提供半导体基板 110，在其内形成图像传感器 120。基板 110 包含晶体结构的硅。基板 110 可替代地或额外地包含其它基本的半导体如锗或金刚石。基板 110 也可包含化合半导体如碳化硅、砷化镓、砷化铟或磷化铟。基板 110 可包含各种 p 型掺杂区和/或 n 型掺杂区，经构建及耦合形成各种器件及功能特征。在各种步骤及工艺中，所有掺杂特征可通过使用如离子注入或扩散的工艺来实现。基板 110 可包含其它特征如浅沟槽隔离（STI）、外延层、绝缘层上半导体（SOI）结构或其各种组合。

图像传感组件 120 设置于半导体基板 110 内。传感组件 120 包含光感区，光感区可以是具有 N 型和/或 P 型掺杂的掺杂区域，其系通过如扩散或离子注入的方法，形成于半导体基板 110 内。光感区的掺杂浓度范围可在约 1014~1021 原子/cm3 之间。光感区可有一表面面积，其范围为相关联的传感组件的面积的约 10%～80%之间，其可加以运作以接收光（或来自待成像物体的其它形式的辐射能）。传感组件 120 的实例包含光电二极管、互补式金属氧化物半导体（CMOS）图像传感器、电荷耦合器件（CCD）传感器、有源传感器、无源传感器和/或散布于或形成于基板 110 内的其它类型器件。同样地，传感组件 120 可包含传统和/或未来开发的图像传感器件。

在此仅为示范目的提供传感组件 120。半导体器件 100 可包含设置于数组或其它合适结构内的若干传感组件。若干传感组件可设计成不同的传感类型。例如，一组传感组件可以是 CMOS 图像传感器，而其它组传感组件可以是无源传感器。而且，传感组件 120 可包含彩色图像传感器和/或单色图像

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传感器。

接着进行方法200的步骤220，在半导体基板110上形成多层互连（MLI）130和层间介电材料（ILD）140。MLI 130耦合于传感组件120及形成于半导体基板110内的其它电单元。图1例示具有三金属层的MLI结构。MLI 130包含不同金属特征如金属一130a、金属二130b、及金属三130c。MLI 130还包含接触特征130d，接触特征130d构建在金属一130a与半导体基板之间，并与两者耦合。MLI 130还包含通孔130e，每个通孔130e构建在相邻金属层间，并相互耦合。例如，通孔130e可设置在金属一130a与金属二130b之间，以及设置在金属二130b与金属三130c之间。金属特征130a、130b、130c、130d及130e中每一金属特征的临界尺寸实质地小于0.25微米。MLI 130包含铜。MLI 130可替代地或共同地包含其它导电材料如铜合金、钛、氮化钛、钽、氮化钽、钨、多晶硅、硅化金属或它们的各种组合。硅化金属可包含硅化镍、硅化钴、硅化钨、硅化钽、硅化钛、硅化铂、硅化铒、硅化钯或其各种组合。

多层互连可通过技术如CVD、溅射、电镀、其它合适工艺或其各种组合而形成。例如，PVD可用来形成铜种子层，然而电镀工艺用来沉积更多的铜以作为互连。图1所示的三金属层仅为简要示范起见。在不同的实施例中，MLI 130可包含少于或多于三金属层。MLI 130设计布置成没有阻挡传感组件120与成像光。

ILD 140设置在半导体基板110上，与MLI 130电绝缘。ILD 140可包含前金属介电层（PMD）和多种金属间介电层140a及多种蚀刻终止/阻挡层140b（或简化起见称为阻挡层）介入于邻接的IMD 140a之间。PMD与IMD层140a中每一层的厚度范围在约0.1微米~1微米之间。在一实例中，PMD的厚度范围在约3500～7000埃之间。通孔一与通孔二之间的IMD层的厚度范围在约1000～4000埃之间。金属一与金属二之间的IMD层的厚度范围在约1000~5000埃之间。位在较高金属层的IMD 140a可更厚。IMD与PMD 140a可包含二氧化硅如：未掺杂的硅玻璃（USG）、氮化硅、氮氧化硅、聚酰亚胺、旋涂式玻璃（SOG）、掺杂氟化物的硅酸玻璃（FSG）、掺杂碳的氧化硅如SiCOH、黑钻石（Black Diamond®）（美国加州Santa Clara的Applied Materials (应用材料)，）、干凝胶（Xerogel）、气凝胶（Aerogel）、无定形氟化碳、聚对二甲苯基（Parylene）、BCB（二苯并环丁烯）、SiLK（陶氏化学，

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中部，密歇根州）和/或其它合适材料。阻挡层 140b 在镶嵌工艺中可提供蚀刻终止功能、及阻挡功能以消除湿气扩散至 MLI130 以及铜迁移至 ILD140。阻挡层 140b 可包含氮化硅、氮氧化硅、碳化硅或其它适当的材料。ILD140（包含 140a 和 140b）可通过如旋涂、CVD、溅射、或其它合适工艺等技术来形成。例如，等离子体增强（PE）CVD 可用来将硅烷（SiH4）或四乙氧基硅烷（TEOS）形成氧化硅。在另一实施例中，可使用高密度等离子体（HDP）CVD。

MLI 130 与 ILD 140 可以称作镶嵌工艺如双镶嵌工艺或单镶嵌制成的集成工艺来形成。在一实例中，每一金属层、通孔及接触孔可通过下列描述的工艺流程而形成。蚀刻终止和/或阻挡层首先形成在半导体器件 100 上。蚀刻阻挡层可包含氮化硅或氮氧化硅。介电材料沉积在蚀刻终止层上形成介电层，并可进一步利用如化学机械平坦化（CMP）工艺或回蚀刻工艺而平坦化。CMP 终止层可形成在介电层上。然后根据预设计电路图案利用光光刻工艺蚀刻介电层形成沟槽（如贯通 130a 的 130e）。利用如溅射方法，在沟槽内沉积用于阻挡和/或粘结的衬垫层。接着在衬垫化后的沟槽内利用溅射工艺填充铜形成铜种子层，及利用电镀工艺形成铜填充。然后可除去介电层上形成的铜，并用 CMP 或回蚀刻工艺平坦化半导体器件 100。可替代的是，可利用现有技术的各种实施例中已知的双镶嵌工艺来形成 MLI 130 与 ILD 140。在一些实施例中，在步骤 220，可与 MLI 130 一起形成虚拟金属特征(dummy metal features)。例如，虚拟金属特征可形成在传感单元 120 之上的区域内，用于调节图案密度以及提高 CMP 性能。在下一步骤中，在沟槽形成期间，可除去虚拟金属特征。

方法 200 进行到步骤 230，在 ILD 140 内形成沟槽（开口）150。定义并布置出沟槽 150，从而暴露出传感单元 120。沟槽 150 具有延伸至传感组件 120 表面的深度。在另一实施例中，沟槽 150 不延伸至传感组件 120 表面，并且一部分 ILD 140 仍介于沟槽 150 与传感组件 120 之间（图未示）。通过俯视，沟槽 150 的水平尺寸实质地包围传感组件 120。例如，另外地如图 3 所示的传感组件 120 和沟槽 150 的俯视图，沟槽 150 之外围线将传感组件 120 包围在内。传感组件 120 与沟槽 150 的每一尺寸用 A 和 B 标出。传感组件 120 的尺寸范围在约 0.5 微米~5 微米之间。沟槽 150 的尺寸 B 可具有相似的范围，但具有一偏距，从而实质地包围传感组件。沟槽 150 设置成沟槽之外

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围线与传感组件 120 的各边具有一间隙，用 'G' 表示。间隙 G 可约 0.1 微米或更大。可用工艺流包含光刻图案化以及蚀刻来形成沟槽 150。例如，在 ILD 140 上施加光刻胶层，并利用光刻工艺将其图案化以形成开口。接着，蚀刻 ILD 130 并贯穿图案化光刻胶的开口，暴露出传感组件 120，生成沟槽 150。蚀刻工艺可利用干蚀刻技术，并使用碳氟基蚀刻剂以及氧气。在各种实施例中，碳氟基蚀刻剂可包含 CF_4、CHF_3、C_2F_6、C_3F_8、C_4F_8 或其各种组合。干蚀刻工艺的工艺温度可在约 100~150 度之间。可替代的是，蚀刻工艺可利用以氢氟酸（HF）为主的蚀刻剂的湿蚀刻技术。监控蚀刻工艺，以免过度蚀刻至半导体基板 110 与形成于内的传感组件 120。在另一实施例中，在形成 MLI 130 与 ILD 140 之前，在半导体基板 110 上可形成蚀刻终止层。因此，蚀刻工艺将停止在蚀刻终止层上。沟槽内的蚀刻终止层可用其它的蚀刻工艺除去，以便暴露出下面的传感组件 120。在另一实施例中，在 ILD 140 内形成沟槽 150 中，使用掩模层。例如施加一掩模层至 ILD 140。在掩模层上施加光刻胶层，并利用光刻工艺将其图案化形成开口。接着，蚀刻掩模层，将开口从光刻胶层转移到掩模层。用湿剥除或其后的等离子体灰化以除去光刻胶层。然后，蚀刻 ILD 140 贯过掩模层开口，从而在半导体基板 110 上形成沟槽 150 并暴露出传感组件 120。

方法 200 进行到步骤 240，填充沟槽 150。沟槽 150 实质地用可一种从成像物体朝传感组件方向的光可穿透的介电材料来填充。该光可以是可见光，波长范围在约 300～800nm 之间。

此外，在一实施例中，沟槽 150 内填充的介电材料的折射率高于周围的材料。填充的介电材料在显微透镜与传感组件之间形成波导，以达到对来自待成像物体的成像光的全反射。其它要求，例如显微透镜的焦距或显微透镜与传感组件间的距离可得到缓和，而不牺牲成像效率和品质。在一实施例中，沟槽 150 内填充的介电材料的折射率高于 ILD 140。

沟槽 150 内的填充材料包含以各种技术沉积的氧化硅，如未掺杂的硅石玻璃（USG）、用等离子体增强 CVD 从硅烷（SiH_4）所形成的氧化硅、用等离子体增强 CVD 从四乙氧基硅烷（TEOS）形成的氧化硅、高密度等离子体（HDP）CVD、旋涂式玻璃或其各种组合。沟槽 150 内的填充材料可替代地包含掺杂氧化物如氟化硅玻璃、掺杂碳的硅酸盐（SiCOH）或其它合适的材料如其它透明玻璃。沟槽 150 内的填充材料可以是一多膜结构。

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方法 200 进行至步骤 250，对沟槽 150 内以及 ILD 140 之上的填充材料实施平坦化工艺，从而平坦化半导体器件 100 并除去多余的填充材料。平坦化工艺可包含回蚀刻、CMP 或其各种组合。

方法 200 进行到步骤 260，在 ILD 140 及 MLI 130 上形成一钝化层，以实质地覆盖半导体器件并密封器件以避免受潮及其它污染。在一实例中，钝化层可包含置于 ILD 140 和填充的沟槽 150 上的氧化硅层 160、及氧化硅层 160 上的氮化硅层 170，用于增强钝化和粘结。

半导体器件 100 及其制造方法 200 可具有不同的变化形式。图 4 显示另一实施例的半导体器件 100 的剖面图。沟槽 150 进一步包含衬垫层 150a。衬垫层 150a 实质地形成在沟槽 150 的侧壁上，并可另外地形成在沟槽 150 的底部上。衬垫层 150a 可包含含氮材料，如氮化硅、氮氧化硅或其它合适的材料。在步骤 230 形成沟槽 150 之后并在步骤 240 填充沟槽 150 之前，衬垫层 150a 可用 CVD 工艺或其它适当的方法形成。衬垫层 150a 的厚度范围在约 50~500 埃之间，可具有多膜结构。衬垫层 150a 提供密封效果，以消除来自 MLI 130 的湿气和污染，及/或提供折射功能，以控制朝向传感组件的成像光，从而具有更高的成像效率并降低与其它功能单元如半导体器件中的其它传感组件间的干扰。在另一实施例中，衬垫化后的沟槽内的填充的介电材料的折射率高于衬垫层 150a。在另一实施例中，衬垫层 150a 的折射率高于 ILD 层 140。在另一实施例中，衬垫层 150a 的折射率高于 IMD 层 140a。利用填充的介电材料和衬垫层可实现全折射。为此目的，填充的介电材料和衬垫层可使用各种材料，该各种材料可包含不同材料、或者具有制造技术、不同工艺参数、不同类型掺杂和/或不同掺杂浓度的同一材料。例如，上面提及的 CVD 方法可通过动态控制工艺温度以形成衬垫层和填充的介电材料，而达成从衬垫层到填充的介电层的折射率变化。在另一实例中。填充的介电材料可包含用 CVD 方法形成的硼掺杂的硅酸盐。在另一实施例中，衬垫层或 ILD 可使用低 k 材料。

前面已概述了几个实施例的特征，从而本领域技术人员可更好地理解其后的详细描述。本领域技术人员应当理解，他们可容易地利用本揭示作为基础，来设计或修正其它工艺和结构，以实现在此介绍的实施例的目的和/或优点。本领域的技术人员也意识到，这种等同构建并没有脱离本发明的精神和范围，而且他们可作各种变化、替代、改变而不脱离本发明的精神和范围。

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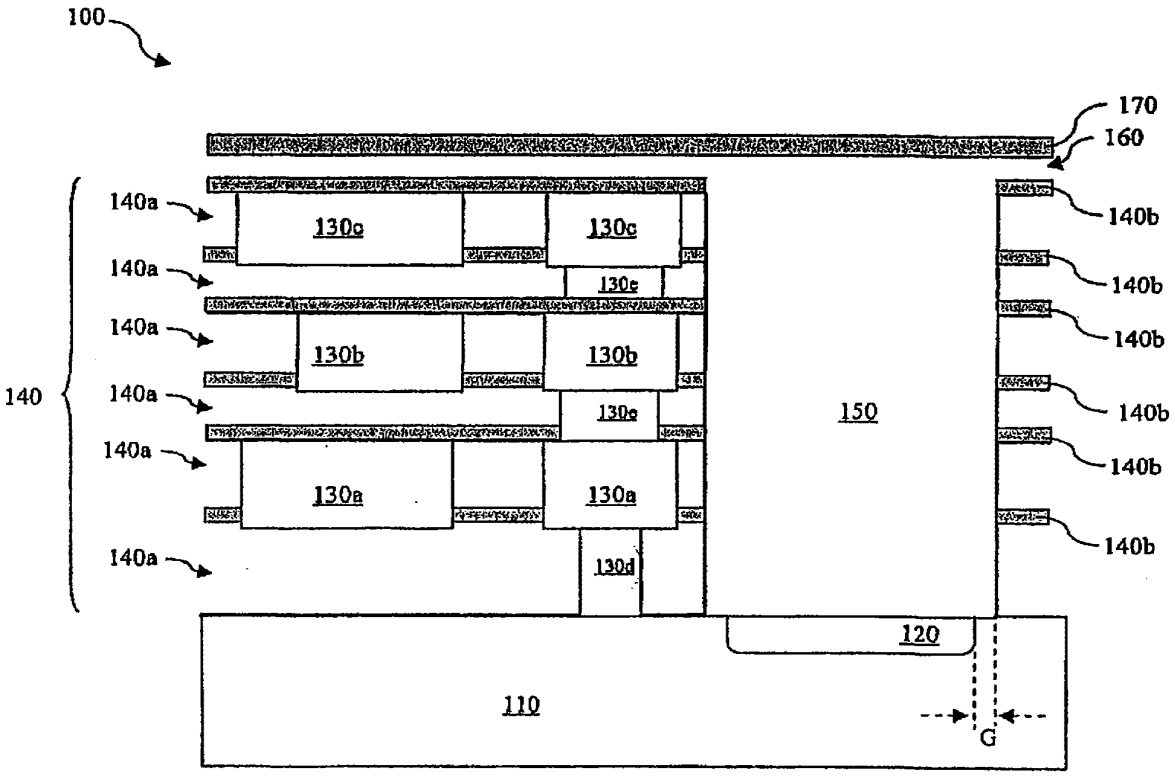


图 1

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Espacenet

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Production method for polycrystalline silicon solar cell texture surface

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Abstract of CN101404307 (A)

The invention discloses a method for manufacturing a matte surface of a polysilicon solar cell. A laser beam is adopted to intensively scan the surface of a polysilicon wafer, thus causing silicon materials in the scanned region to generate fusion, gasification and spill reaction to form a micro-sized concave-convex structure on the surface of the polysilicon wafer, and the surface is etched and then is subject to surface cleaning by a chemical method to remove the damaged layer. The polysilicon wafer structure produced by the method can lead incident light to produce multiple reflection therein, increase the absorption of the incident light, achieve good surface anti-reflection effect and can cause little damage to the polysilicon wafer. The method solves the problem of manufacturing the matte surface of the polysilicon cell and can obtain the polysilicon wafer with surface reflectivity far less than the surface reflectivity of the silicon wafer manufactured by a pure chemical method. The method plays an important role of improving the light absorption and photoelectric conversion efficiency of the polysilicon solar cell.

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权利要求书 1 页 说明书 4 页 附图 2 页

[54] 发明名称

一种多晶硅太阳电池绒面制作方法

[57] 摘要

本发明公开了一种多晶硅太阳电池绒面制作方法，该方法利用激光束在多晶硅片表面密集扫描，使扫描区域内的硅材料发生熔融、气化和溅出反应，在多晶硅片表面形成微米级的凹凸结构，刻蚀后采用化学方法做表面清洗和去除损伤层。采用本发明方法制成的多晶硅片结构可以使入射光在其中多次反射，增加对入射光的吸收，获得良好的表面减反射效果，并且对硅片的损伤影响较小。本发明解决了困扰多晶硅电池的制绒问题，可以获得远小于纯化学制绒的硅片表面反射率，对提高多晶硅太阳电池的光吸收以及光电转换效率有着重要作用。

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1、一种多晶硅太阳电池绒面制作方法，其特征在于，利用激光束在多晶硅片表面密集扫描，使扫描区域内的硅材料发生熔融、气化和溅出反应，在多晶硅片表面形成微米级的凹凸结构，刻蚀后采用化学方法做表面清洗和去除损伤层。

2. 根据权利要求 1 所述的多晶硅太阳电池绒面制作方法，其特征在于，采用功率 1~1000W、波长 1100~200nm 的脉冲或连续激光束，在经过聚焦后达到微米量级直径的光斑照射到硅片表面进行扫描。

3. 根据权利要求 1 或 2 所述的多晶硅太阳电池绒面制作方法，其特征在于，根据多晶硅片和激光束的性能，选择合适扫描刻蚀图样，在硅片表面密集刻蚀，形成均匀绒面。

4. 根据权利要求 1 或 2 所述的多晶硅太阳电池绒面制作方法，其特征在于，在多晶硅片表面所形成的微米级的凹凸结构的高宽比值达 0.1~2。

5. 根据权利要求 1 或 2 所述的多晶硅太阳电池绒面制作方法，其特征在于，刻蚀后采用碱液、酸液或两者配合，清洗硅片表面的残渣，并腐蚀刻蚀区域表面的损伤层。

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一种多晶硅太阳电池绒面制作方法

技术领域

本发明涉及一种多晶硅表面制绒的方法，具体地说是一种在多晶硅太阳电池表面制绒的方法。

技术背景

硅太阳电池利用 p-n 结的光生伏特效应实现光电转换，已经成为新能源发展主流之一。2007 年多晶硅太阳电池占世界太阳电池总产量的 45.2%，处在稳步上升阶段，困扰多晶硅电池的技术原因主要是晶界的存在和缺乏合适的表面制绒方法。表面减反射决定了太阳电池吸收入射光的比例，关系到电池最终光电转换效率，对于目前占主流的晶体硅太阳电池，未经表面处理的反射率一般超过 30%，经过碱液各向异性化学腐蚀形成表面微米级随机金字塔结构绒面后单晶硅电池表面反射率可以降到 10%，多晶硅电池由于表面晶粒的晶向差异，目前普遍采用的各向同性化学腐蚀只能将反射率降低到 20%左右。

由于绒面对电池效率具有直接、明显的作用，开发新的多晶硅表面制绒技术具有重要意义。这些技术首先要求能在多晶硅表面形成微米级且具有合适高宽比的凹凸结构，同时要求处理过程对硅片的电学性能没有明显的损害。最后应对生产要求，制绒技术还要做到在时间和成本上有较好控制，适合产业化。

发明内容

本发明的目的是提供一种多晶硅太阳电池绒面制作方法，采用该方法可以制作高性能多晶硅太阳电池绒面，并且具有产业化前景，使多晶硅电池在绒面的反射率达到甚至低于单晶硅的水平。

本发明的目的通过采取以下技术方案予以实现：

一种多晶硅太阳电池绒面制作方法，其特征在于，利用激光束在多晶硅片表面密集扫描，使扫描区域内的硅材料发生熔融、气化和溅出反应，在多晶硅片表面形成微米级的凹凸结构，刻蚀后采用化学方法做表面清洗和去除损伤层。

作为本发明的进一步完善，采用功率 1~1000W、波长 1100~200nm 的脉冲或连续激光束，在经过聚焦后达到微米量级直径的光斑照射到硅片表面进行扫描。

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作为本发明的进一步完善，根据多晶硅片和激光束的性能，选择合适扫描刻蚀图样，在硅片表面密集刻蚀，形成均匀绒面。

作为本发明的一种实施方式，在多晶硅片表面所形成的微米级的凹凸结构的高宽比值达 0.1~2。

作为本发明的一种实施方式，刻蚀后采用碱液、酸液或两者配合，清洗硅片表面的残渣，并腐蚀刻蚀区域表面的损伤层，以恢复正常的电学性能。

本发明制作绒面的主要手段是采用激光束刻蚀硅片表面，采用较大功率的脉冲或连续激光束，在经过聚焦（如激光束本身足够细则不用聚焦）后达到微米量级直径的光斑照射到硅片表面进行扫描，使照射区域的表面材料熔融，溅射甚至气化，从而形成沟槽坑洞等密集的凹凸结构，即绒面。最后用化学方法去除激光刻蚀区域表面形成的杂质层（氧化物、氮化物等）和损伤层。入射光照射到太阳电池表面会发生反射，只有一定比例的光能进入电池内部被吸收转化为电能，如果电池表面平整没有绒面结构，入射光只存在一次反射，如图 1 所示。而本发明方法制成的太阳电池表面可以具有高宽比达到 1 甚至更高的凹凸结构表面，光线入射到这样的结构，会在结构表面多次反射，如图 2 所示，每一次有一定比例的光进入到电池内部被吸收，从而提高了太阳电池吸收的光占入射光的比例，降低了电池表面光反射率，提高了太阳电池的光电转换效率。

本发明方法的具体处理步骤是：

（1）清洗硅片表面杂质，避免杂质在激光刻蚀过程扩散；

（2）选择合适的激光刻蚀图样，激光刻蚀的图样最简单的是平行线或交叉线阵列，也可设计点阵，或其他图样，图样的尺寸要配合激光束的刻蚀宽度和深度，阵列周期在几十到几百微米；

（3）选择合适的激光波长、光束模式、光斑大小、光束功率、脉冲频率和扫描速度等激光参数方案，做好设置；

（4）将硅片固定在工作台上，按预定的参数和图样利用激光束扫描做刻蚀；

（5）刻蚀后采用碱液、酸液或两者配合，清洗硅片表面的残渣，并腐蚀刻蚀区域表面的损伤层，之后便可进行太阳电池制作的其他工序。

与现有技术相比，本发明具有的有益效果是：

本发明利用激光刻蚀，可以在多晶硅表面形成高宽比大于 1 的微米结构，激

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光刻蚀区域的表面反射率可降低到 6%，经过化学处理后的表面反射率可以达到 10% ，在减反射效果上已经达到了单晶硅的水平。同时通过对样品少子寿命的检测，少子寿命的衰减可以控制到 30%，符合电池制作的要求。与各向异性化学腐蚀方法相比，本发明方法对晶向无要求，同样适用于单晶硅电池。

附图说明

图 1 为光线在没有绒面结构的电池表面发生反射的示意图；

图 2 为光线在制有绒面结构的电池表面发生反射的示意图；

图 2 为本发明实施例 1 制得样品的形貌图（扫描电镜拍摄图）；

图 3 为本发明实施例 2 制得样品的形貌图（扫描电镜拍摄图）。

具体实施方式

以下列举具体实施例对本发明进行说明。需要指出的是，实施例只用于对本发明作进一步说明，不代表本发明的保护范围，其他人根据本发明的提示做出的非本质的修改和调整，仍属于本发明的保护范围。

实施例 1

采用一台波长 1064nm 的 Nd：YAG 激光器：激光脉冲频率 1K~30KHz，振镜扫描，光速横模为低阶模式。设置激光脉冲频率为 1~7KHz，扫描速度为 20~100mm/s，激励电流为 18~25A。样品硅片为厚度 260 微米的多晶硅片，先对原始硅片做适当化学清洗去除表面附着杂质。刻蚀图样选用平行线阵列，线长 30mm，间距 1.6mm，激光刻蚀后用 20%NaOH 溶液清洗腐蚀 15 分钟，然后去离子水清洗，氮气烘干，即完成制绒过程，制得样品的形貌为密排槽形状，如图 3 所示。

实施例 2

采用一台波长 1064nm 的 Nd：YAG 激光器：激光脉冲频率 1K~30KHz，振镜扫描，光速横模为低阶模式。设置激光脉冲频率为 7~15KHz，扫描速度为 20~100mm/s，激励电流为 22~30A。样品硅片为厚度 260 微米的多晶硅片，先对原始硅片做适当化学清洗去除表面附着杂质。刻蚀图样选用平行线阵列，线长 30mm，间距 0.1~0.2mm，激光刻蚀后用 20%NaOH 溶液清洗腐蚀 2~6 分钟，再用 $HF:HNO_3$ 混合溶液腐蚀 2~10 分钟，然后去离子水清洗，氮气烘干，即完成制绒过程，制得样品的形貌为密排类锥形凹坑形状，如图 4 所示，最佳表面反射率

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可达 10%。

实施例 3

采用一台波长 1064nm 的 Nd：YAG 激光器：激光脉冲频率 1K~30KHz，振镜扫描，光速横模为低阶模式。设置激光脉冲频率为 1~10KHz，扫描速度为 20~200mm/s，激励电流为 18~25A。样品硅片为厚度 330 微米的单晶硅片，先对原始硅片做适当化学清洗去除表面附着杂质。刻蚀图样选用平行线阵列，线长 30mm，间距 0.06~0.15mm，激光刻蚀后用 20%NaOH 溶液清洗 10~20 分钟，再用 HF:HNO_3 混合溶液腐蚀 2~10 分钟，然后去离子水清洗，氮气烘干，即完成制绒过程，制得样品的形貌为密排槽形状。

实施例 4

采用一台波长 532nm 的 Nd：YAG 激光器：激光脉冲频率 1K~50KHz，振镜扫描，光速横模为低阶模式。设置激光脉冲频率为 1~10KHz，扫描速度为 20~200mm/s，激励电流为 18~25A。样品硅片为厚度 260 微米的多晶硅片，先对原始硅片做适当化学清洗去除表面附着杂质。刻蚀图样选用垂直交叉平行线阵列，线长 30mm，间距 0.1~0.3mm，激光刻蚀后用 20%NaOH 溶液清洗 5~15 分钟，再用 HF:HNO_3 混合溶液腐蚀 2~15 分钟，然后去离子水清洗，氮气烘干，即完成制绒过程，制得样品的形貌为密排台状或类金字塔突起形状。

实施例 5

采用一台波长 532nm 的 Nd：YAG 激光器：激光脉冲频率 1K~50KHz，振镜扫描，光速横模为低阶模式。设置激光脉冲频率为 1~5KHz，扫描速度为 100~600mm/s，激励电流为 20~30A。样品硅片为厚度 260 微米的多晶硅片，先对原始硅片做适当化学清洗去除表面附着杂质。刻蚀图样选用平行线阵列，线长 30mm，间距 0.05~0.3mm，使用单个高能量激光脉冲打点，形成点状凹坑，激光刻蚀后用 HF:HNO_3 混合溶液腐蚀 2~15 分钟，然后去离子水清洗，氮气烘干，即完成制绒过程，制得样品的形貌为密排凹坑形状。

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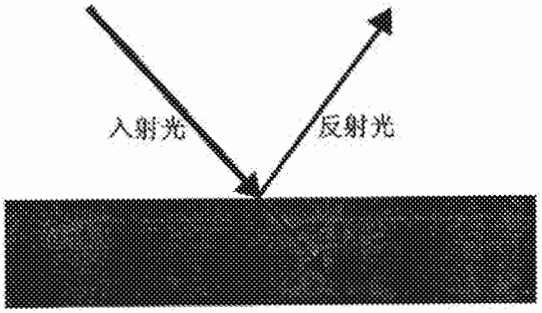


图 1

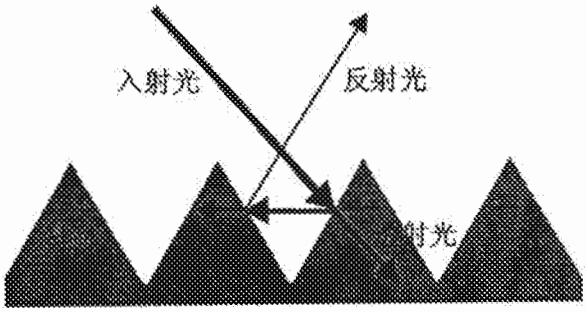


图 2

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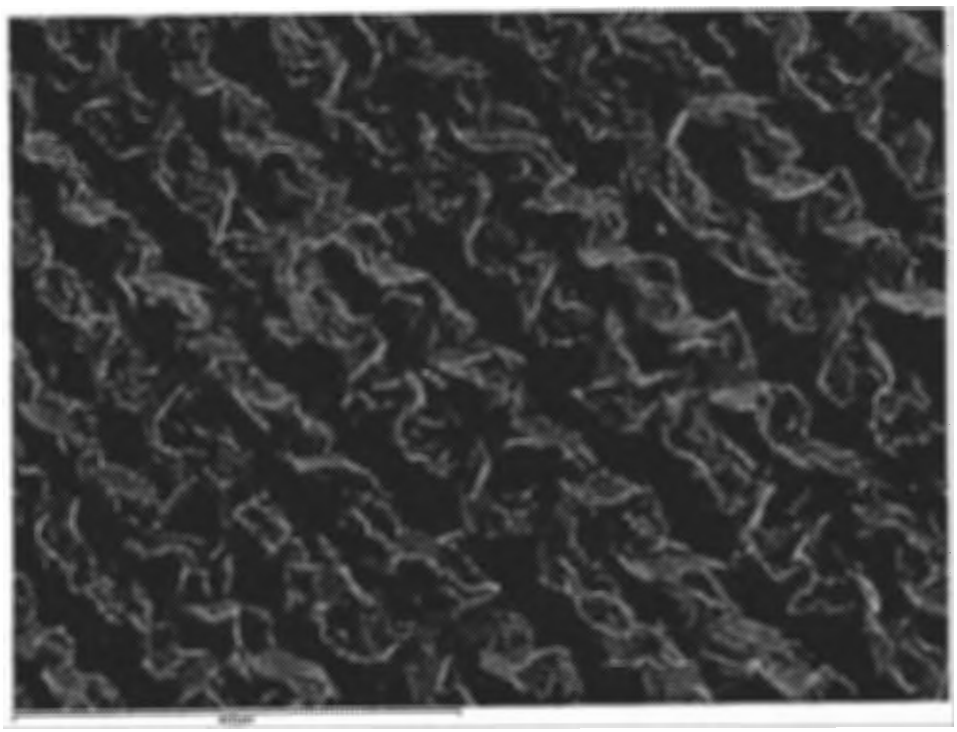


图 3

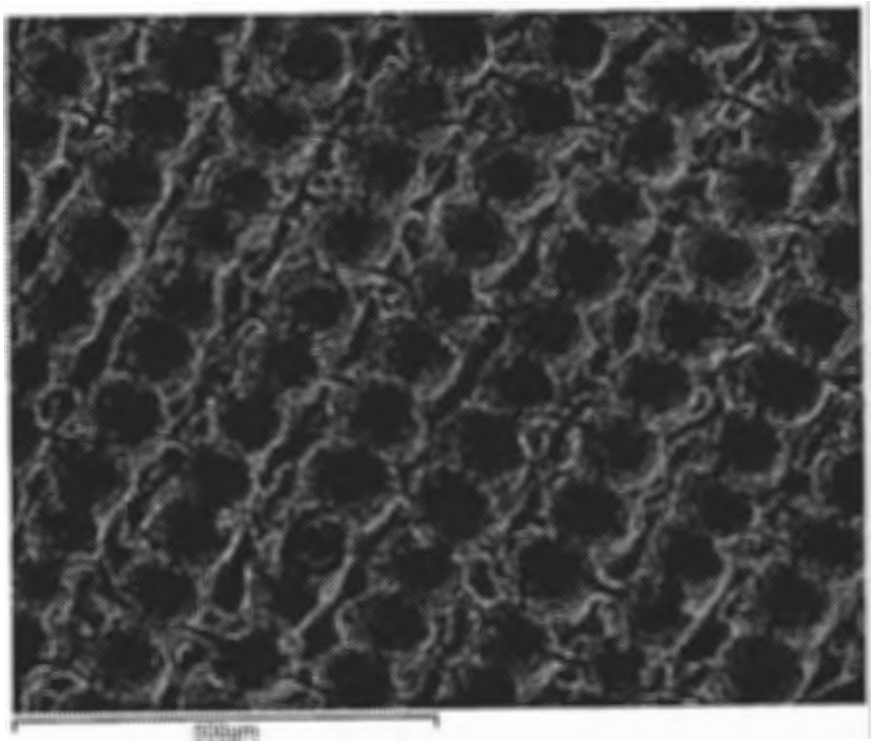


图 4

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Espacenet

Bibliographic data: CN101423942 (A) — 2009-05-06

Alkali etch solution and method for preparing monocrystalline silicon pile fabrics

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Classification: **- international:** ***C23F1/40***
- cooperative: Y02E10/50; Y02P70/521

Application number: CN20081122243 20081113

Priority number (s): CN20081122243 20081113

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Abstract of CN101423942 (A)

The invention belongs to the field of monocrystalline silicon solar battery production and discloses an alkaline corrosion solution and a method for preparing monocrystalline silicon texture. The solution is a mixed liquor of an alkaline solution, isopropanol and Na2SiO3, and is structurally characterized in containing 0.002 to 0.01 weight percent of Pb(NO3)2 or Pb. The weigh percentage of the alkaline solution is 1 to 3.5 percent, the weight percentage of the isopropanol is 5 to 7 percent, and the weight percentage of Na2SiO3 is 0.2 to 2 percent. The method is to soak a monocrystalline silicon piece in the alkaline solution to perform a corrosion reaction for 20 to 30 minutes under a condition that the alkaline corrosion solution is at a temperature of between 75 and 80 DEG C.; The alkaline corrosion solution and the method have the advantages of reducing surface reflectivity of the monocrystalline silicon piece, preparing a fine texturing 'pyramid', along with low cost, simple operation and stable and effective preparation of the monocrystalline silicon texture.

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C23F 1/40 (2006.01)

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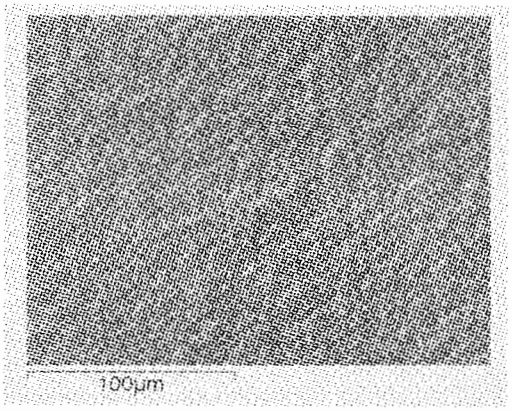
权利要求书 1 页 说明书 4 页 附图 2 页

[54] 发明名称

一种制备单晶硅绒面的碱腐蚀溶液及方法

[57] 摘要

本发明属于制造单晶硅太阳能电池领域，公开了一种制备单晶硅绒面的碱腐蚀溶液及方法。该溶液为碱溶液、异丙醇和 Na_2SiO_3 的混合液，其结构特点是还含有重量百分比为 0.02‰～0.1‰的 $Pb(NO_3)_2$ 或 Pb；碱溶液的重量百分比为 1%～3.5%，异丙醇的重量百分比为5%～7%，Na_2SiO_3 的重量百分比为 0.2%～2%。该方法为将单晶硅片浸泡在该碱腐蚀溶液中进行腐蚀反应，反应时间为 20～30 分钟，碱腐蚀溶液的温度为 75～85℃。本发明具有使单晶硅片表面反射率降低、制备的绒面金字塔细密、成本低、操作简单、稳定有效制备单晶硅绒面的优点。



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1、一种制备单晶硅片绒面的碱腐蚀溶液，该溶液为碱溶液、异丙醇和 Na_2SiO_3 的混合液，其特征是：还含有重量百分比为 0.02‰～0.1‰的 $Pb(NO_3)_2$ 或 Pb。

2、根据权利要求 1 所述的制备单晶硅片绒面的碱腐蚀溶液，其特征是：所述碱溶液的重量百分比为 1%～3.5%，异丙醇的重量百分比为 5%～7%，Na_2SiO_3 的重量百分比为 0.2%～2%。

3、根据权利要求 1 或 2 所述的制备单晶硅片绒面的碱腐蚀溶液，其特征是：所述的碱溶液为 NaOH 或 KOH 溶液。

4、一种使用权利要求 1 所述碱腐蚀溶液的制备单晶硅片绒面的方法，其特征是：将单晶硅片浸泡在该碱腐蚀溶液中进行腐蚀反应，反应时间为 20～30 分钟，碱腐蚀溶液的温度为 75～85℃。

5、根据权利要求 4 所述的制备单晶硅片绒面的方法，其特征是：所述的单晶硅片经过碱腐蚀溶液腐蚀后，表面形成大小为 0.5～1.5 微米的绒面。

6、根据权利要求 4 所述的制备单晶硅片绒面的方法，其特征是：被腐蚀的单晶硅片厚度为 5～20 微米。

7、根据权利要求 4 所述的制备单晶硅片绒面的方法，其特征是：该单晶硅片绒面是在对损伤层的清洗过程中完成的。

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一种制备单晶硅绒面的碱腐蚀溶液及方法

技术领域

本发明属于制造单晶硅太阳能电池领域，涉及一种制备单晶硅绒面的碱腐蚀溶液及方法。

背景技术

自从太阳能电池问世以来，至目前为止整个市场仍以单晶硅太阳能电池为主导，提高单晶硅片绒面制备稳定性和将单晶硅片绒面金字塔制备成纳米级一直是该领域技术人员努力追求的目标之一。提高单晶硅片绒面制备稳定性可以减少溶液配制频率，大大提供生产效率；缩小单晶硅绒面金字塔的体积可以杜绝太阳能电池生产过程中的许多隐患。因此，在单晶硅太阳能电池领域中，怎样稳定、有效地制备绒面是一个非常热门的课题。

所谓的绒面就是指存在于物体表面上的一系列有规则或无规则的高低不同和大小不同的表面形状。由于绒面的存在，物体表面的反射率就会大大降低。换句话说，物体表面的绒面可增加光的吸收。因此，绒面技术被广泛应用在太阳能电池领域。

单晶硅片绒面制备技术虽然开发得较早，传统工艺可以投入批量生产，但在传统工艺中，碱腐蚀制备单晶硅片绒面时，对碱溶液浓度、温度、腐蚀时间、异丙醇添加量、Na_2SiO_3添加量等一系列相关工艺参数要求控制的非常精确，否则会造成制绒过程的极不稳定，以及更换溶液频率和绒面制备返工率的上升，浪费不必要的财物和时间；并且制备的绒面不均匀就会加大光的反射，最终影响太阳能电池片的转化效率。

随着工艺的不断改进，硅片减薄工艺已被绒面过程所取代，传统工艺要保证绒面制备过程中损伤层去除彻底，又相对减小绒面金字塔的体积是几乎不可能的；而金字塔体积相对较大，会提高电池片生产过程的碎片发生率，同时不同角度的光反射也会上升，最终影响太阳能电池片的转化效率。

此外，现有采用线切割的方法由硅棒切割而成的单晶硅片厚度一般在 200 微米以下，这种单晶硅片应该是干净的，没有任何有机物质污染。在切割硅棒过程中，单晶硅片表面与碳化硅微粒和钢丝剧烈摩擦，在单晶硅片的表面生成了一层厚度不均匀的损伤层，这层损伤层是半导体电子和空穴的复合源。所以在太阳

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能电池生产过程中，首先要把这层损伤层清除干净，清除这层损伤层的传统工艺是采用碱溶液腐蚀单晶硅片。

发明内容

本发明所要解决的技术问题是提供一种使单晶硅片表面反射率降低、制备的绒面金字塔细密、成本低、操作简单、稳定有效制备单晶硅绒面的碱腐蚀溶液及方法。

本发明解决上述问题所采用的技术方案是：该溶液为碱溶液、异丙醇和Na_2SiO_3的混合液，其结构特点是还含有重量百分比为0.02‰～0.1‰的$Pb(NO_3)_2$或Pb。

所述碱溶液的重量百分比为1%～3.5%，异丙醇的重量百分比为5%～7%，Na_2SiO_3的重量百分比为0.2%～2%。

所述的碱溶液为NaOH或KOH溶液。

该方法为将单晶硅片浸泡在该碱腐蚀溶液中进行腐蚀反应，反应时间为20～30分钟，碱腐蚀溶液的温度为75～85℃。

所述的单晶硅片经过碱腐蚀溶液腐蚀后，表面形成大小为0.5～1.5微米的绒面。

被腐蚀的单晶硅片厚度为5～20微米。

该单晶硅片绒面是在对损伤层的清洗过程中完成的。

本发明与现有技术相比，具有以下有益效果：1、该碱腐蚀溶液中添加适量的化学添加剂$Pb(NO_3)_2$或单质Pb，单晶硅片浸泡在该溶液中， 不仅可以形成均匀的绒面，降低制绒后反射率和提高太阳能电池转化效率，且制备的绒面金字塔大小比传统工艺制备的绒面金字塔大小要小10倍以上，同时一槽溶液制备单晶硅片绒面的数量比传统工艺制备的数量可以提高3倍以上，制绒过程非常稳定；2、该碱腐蚀溶液所添加的$Pb(NO_3)_2$或单质Pb用量少，市场上普遍供应、价格便宜、制造成本上升极小，几乎可以忽略；3、该碱腐蚀溶液配制的工艺参数控制范围很广，不需控制地非常精确，这样制备绒面时就非常稳定；4、该制备方法不需要特殊的制绒过程，也不需要添加额外的生产设备，损伤层的清洗过程就是制绒过程，具有操作简单和成本低的优点。

附图说明

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图 1 为传统工艺制备的单晶硅片绒面的扫描图。

图 2 为本发明制备的单晶硅片绒面的扫描图。

图 3 为本发明制备的单晶硅片绒面与传统工艺制备的单晶硅片绒面的反射率比较图。

图 4 为采用本发明制备的单晶硅片太阳能电池的量子效应及反射率图。

具体实施方式

该溶液由碱溶液、异丙醇、Na_2SiO_3 以及 $Pb(NO_3)_2$ 或 Pb 组成，其中碱溶液的重量百分比为 1%～3.5%，异丙醇的重量百分比为 5%～7%，Na_2SiO_3 的重量百分比为 0.2%～2%，$Pb(NO_3)_2$ 或 Pb 的重量百分比为 0.02‰～0.1‰。碱溶液为 NaOH 或 KOH 溶液，且碱溶液的浓度与配制传统碱腐蚀溶液时所用的碱溶液相同。

该制备方法为将单晶硅片浸泡在上述碱腐蚀溶液中进行腐蚀反应，反应时间为 20～30 分钟，碱腐蚀溶液的温度为 75～85℃。单晶硅片经过碱腐蚀溶液腐蚀后，被腐蚀的厚度为 5～20 微米，表面形成大小为 0.5～1.5 微米的绒面。单晶硅片绒面是在对损伤层的清洗过程中完成的。

本发明所用的单晶硅片一般是 P 型单晶硅片，还适用于 N 型单晶硅片或者其它半导体材料。

参见图 1～图 4，与传统工艺相比，本发明所制备出来的单晶硅片绒面明显更为细密，反射率有所降低。

实施例 1：

本实施例中 NaOH 溶液的重量百分比为 2%，异丙醇的重量百分比为 6%，Na_2SiO_3 的重量百分比为 0.5%，$Pb(NO_3)_2$ 的重量百分比为 0.05‰。该碱腐蚀溶液温度为 80℃，单晶硅片的碱腐蚀时间为 20 分钟，制备的绒面金字塔大小测量结果为 0.9μm。

实施例 2：

本实施例中 NaOH 溶液的重量百分比为 3%，异丙醇的重量百分比为 5%，Na_2SiO_3 的重量百分比为 1%，$Pb(NO_3)_2$ 的重量百分比为 0.02‰。该碱腐蚀溶液温度为 85℃，单晶硅片的碱腐蚀时间为 28 分钟，制备的绒面金字塔大小测量结果为 1.5μm。

实施例 3：

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本实施例中NaOH溶液的重量百分比为1.5%，异丙醇的重量百分比为7%，Na_2SiO_3的重量百分比为0.2%，$Pb(NO_3)_2$的重量百分比为0.1‰。该碱腐蚀溶液温度为82℃，单晶硅片的碱腐蚀时间为25分钟，制备的绒面金字塔大小测量结果为0.7μm。

以上实施例中NaOH溶液可以用同量的KOH溶液代替，$Pb(NO_3)_2$可以用同量的Pb代替。

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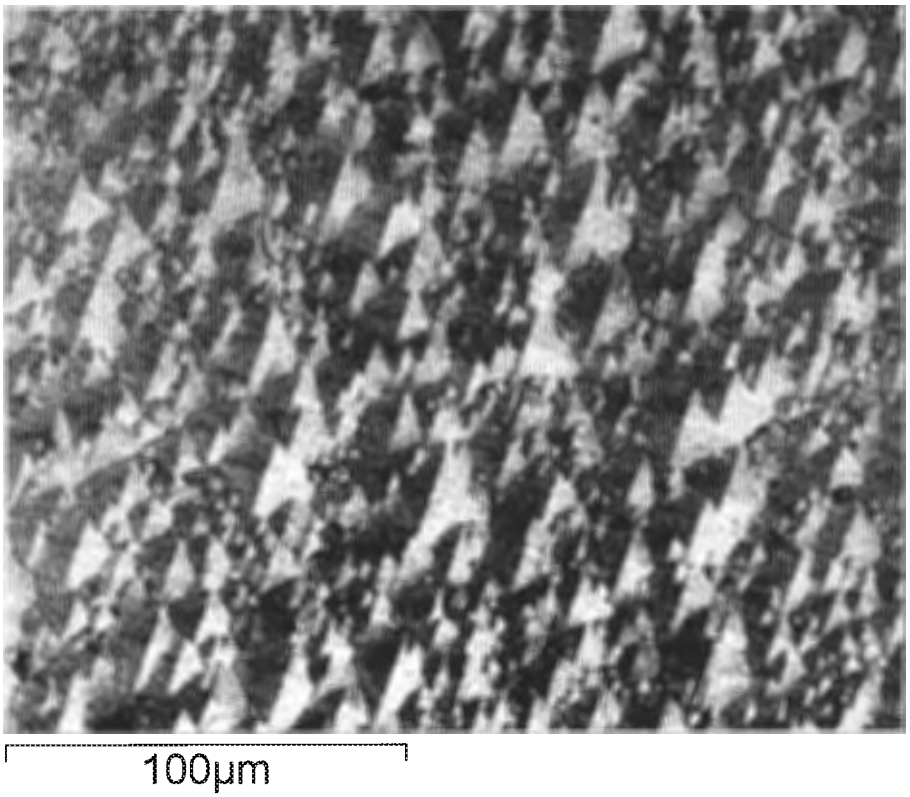
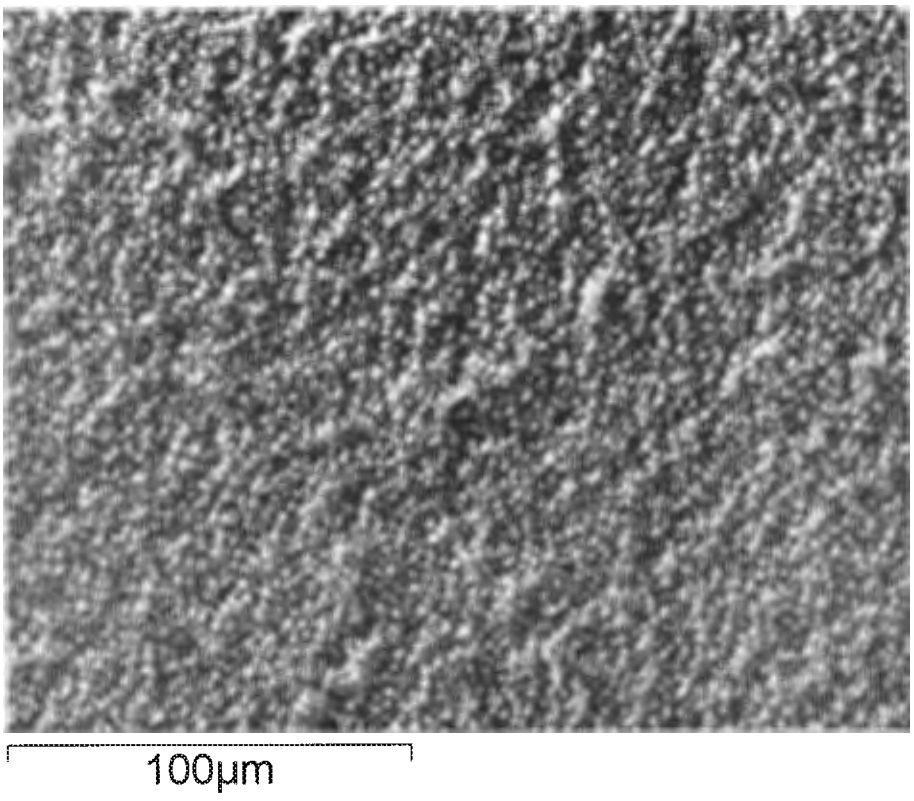


图 1



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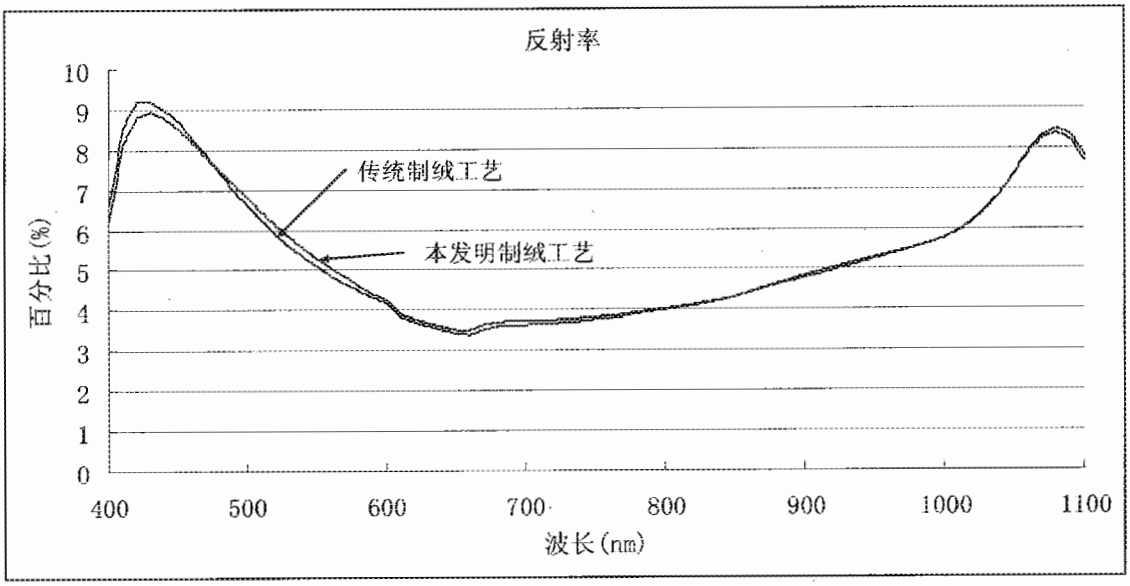


图 3

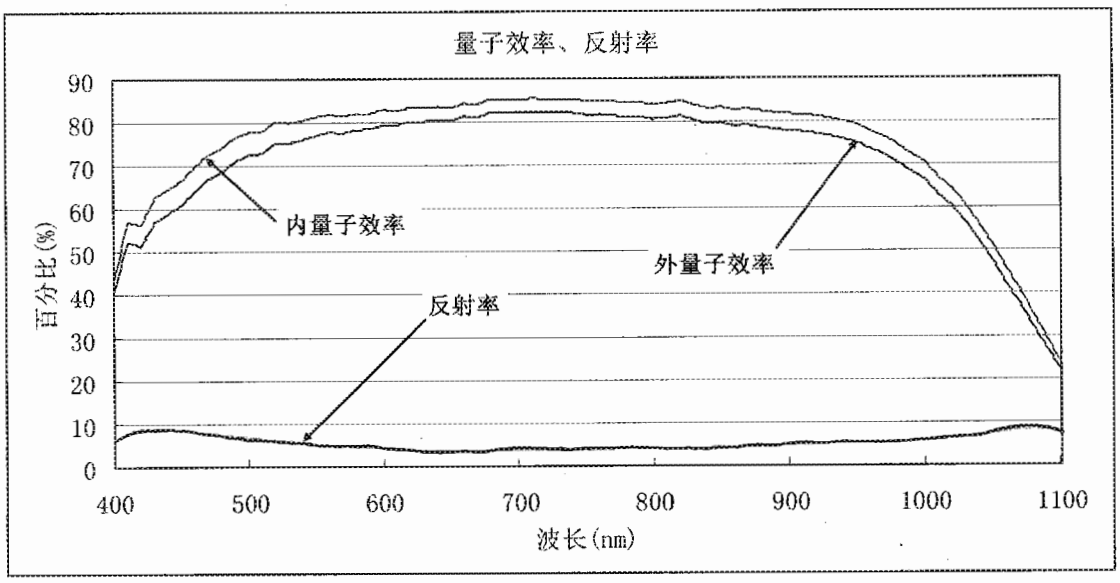


图 4

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Espacenet

Bibliographic data: CN101465361 (A) — 2009-06-24

Isolation structure of image sensor element

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Classification: **- international:** ***H01L27/146***
- cooperative:

Application number: CN20071302306 20071218

Priority number(s): CN20071302306 20071218

Abstract of CN101465361 (A)

The invention provides an image sensor element, which comprises a substrate with a pixel region and a peripheral region. A first isolation structure is formed in the pixel region of the substrate. The first isolation structure comprises a ditch with a first depth. A second isolation structure is formed in the peripheral region of the substrate. The second isolation structure comprises a ditch with a second depth. The first depth is greater than the second depth.

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DESCRIPTION CN101465361

The present invention provides an image sensor element that includes a substrate having a pixel area and a peripheral area. The first isolation structure is formed in a pixel area of the substrate. The first isolation structure includes a trench having a first depth. The second isolation structure is formed in a peripheral region of the substrate. The second isolation structure includes a trench having a second depth. The first depth is greater than the second depth.

Image sensor element isolation structure

Technical field

The present disclosure relates generally to image sensors and, more specifically, to image sensors including integrated circuits such as complementary metal-oxide semiconductor (CMOS) image sensors and charge coupled devices (CCDs). Image Sensor.

Background technique

In semiconductor technology, an image sensor is used to sense the amount of exposure projected onto the semiconductor substrate. CMOS sensors and CCD sensors are widely used in many applications such as digital cameras. These image sensors use a matrix of pixels containing light sensing elements to collect light energy and convert the image to digital data. However, when the pixel size is reduced, the sensitivity of the pixel will be reduced. In addition, the crosstalk between pixels will increase. Mutual interference can detract from spatial resolution, reduce overall sensitivity, provide poor color isolation, and can introduce additional noise into the

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image, especially after the color correction process. Processes and thin color filters containing these thin layers of material (e.g., thin dielectric and metal layers) can be used to improve optical interference. However, these conventional methods of improving electrical mutual interference (e.g., providing a sensor with a thin epitaxial layer) are provided for other problems such as Electrostatic discharge (ESD) failure. Problems with other conventional image sensors include long-wavelength light sensitivity and image defects, such as from a Blooming effect (a particular area of the output image is displayed brighter than the original image).

Therefore, there is a need for improved image sensors.

Summary of the Invention

The present disclosure provides disclosures related to semiconductor devices, and more particularly to an isolation structure of an image sensor. The proposed novel structure can reduce electrical mutual interference and other optical defects between pixels.

The present invention provides an image sensor having a substrate including a pixel area and a peripheral area, a first isolation structure formed in a pixel area of the substrate, and a second isolation formed in a peripheral area of the substrate structure. The first isolation structure includes a first trench having a first depth, the second isolation structure includes a second trench having a second depth, and wherein the first depth is greater than the second depth.

In other words, the present invention provides an image sensor element including a substrate having a pixel area and a peripheral area. The isolation structure is formed in the pixel area of the substrate. The isolation structure includes a trench. Another isolation structure is formed in the peripheral region of the substrate. The isolation structure also includes trenches. The trench formed in the pixel area has a greater depth than the trench formed in the peripheral area.

In another aspect, the present invention provides another image sensor element including a substrate having a pixel area and a peripheral area. A plurality of pixels are formed in the substrate of the pixel region. Ditches are formed between two pixels. The trench has a first depth. The second trench is formed in the peripheral region of the substrate. The depth of the second trench is less than the first depth.

In yet another aspect, the present invention provides a method of forming an image sensor. A substrate including a pixel area and a peripheral area is provided. A first isolation trench is formed in a pixel region of the substrate,

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and forming the first isolation trench includes etching the substrate to a first depth. A second isolation trench is formed in the peripheral region of the substrate. Forming the second isolation trench includes etching the substrate to a second depth, the second depth being less than the first depth.

Description of the drawings

The various aspects disclosed herein are best understood from the foregoing detailed description and by reading the accompanying drawings. It should be emphasized that many features are not drawn to scale according to industry standard practice. In fact, the size of each feature may be arbitrarily increased or decreased for clarity of discussion.

FIG. 1 is a top view of an image sensor including a pixel area and a peripheral area; FIG.

FIG. 2 is a sectional view of a conventional image sensor including a matrix of pixels and a peripheral area; FIG.

3 is a cross-sectional view of an image sensor including a pixel matrix and a peripheral area of an embodiment;

FIG. 4 is a flowchart showing an embodiment of a method of manufacturing the image sensor of FIG. 3; FIG.

Figures 5a to 5g are sectional views of the embodiment of the method of Figure 4;

6 is a flow chart of another alternative embodiment of the method of manufacturing an image sensor of FIG. 3;

Figures 7a to 7e are cross-sectional views of the method embodiment of Figure 5; and

FIG. 8 is a cross-sectional view of an alternate embodiment of an image sensor including a matrix of pixels and a peripheral region.

detailed description

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The present disclosure relates generally to semiconductor elements, particularly image sensors. It should be understood, however, that specific embodiments are provided as examples to teach broader concepts of the invention and that those skilled in the art can readily apply the teachings of this disclosure to other methods or elements. In addition, it should be understood that the methods and apparatus discussed in this disclosure encompass some conventional structures and/or processes. Since these structures and processes are well known in the field, they will only be discussed in general detail. Moreover, for convenience and example, reference numerals are repeated throughout the drawings, and the repetitions do not indicate any desirable features or combination of steps throughout the drawings. Also, forming the first feature past the second feature, over the second feature, or coupled to the second feature may include in the subsequent description such embodiments in which the first and second features are formed in direct contact; or may be included in Between the first and second features are inserted embodiments that form additional features, such that the first and second features may not be in direct contact. Furthermore, forming features on the surface of the substrate or substrate may include forming features (eg, implant regions, trenches) over the substrate surface, adjacent to the substrate surface, directly on the substrate surface, and/or extending below the substrate surface. Examples.

Referring to FIG. 1, the image sensing element 100 provides a pixel area 110 and a peripheral area 120. The pixel area 110 includes a matrix of pixels 110a. In an embodiment, the image sensing element 100 may be a complementary metal oxide semiconductor (CMOS) image sensor (CIS) or an active pixel sensor. In alternative embodiments, the image sensor 100 may be a charge coupled device (CCD) sensor. The image sensing element 100 may be a front-side light sensor or a back-side light sensor. In the structure of the back side light emitting sensor, the sensed light is incident on the back side of the substrate and the pixels are formed on the front side of the substrate. Pixel 110a includes at least one optical detector (e.g., photodiode) to record light intensity or intensity. In an embodiment, pixel 110a includes a pin photodiode. Each pixel 110a also includes at least one transistor. The pixel 110a includes a reset transistor, a source follower transistor, a selector transistor, and/or a transfer transistor. The reset transistor may perform reset of the pixel 110a. The source follower transistor may allow the voltage to be combined with the observed pixel 110a without removing the accumulated charge. The selector transistor may be a row selector transistor and allow reading of a single row of pixels 110a when the selector transistor is on. The transfer transistor can move the accumulated charge in the photodetector of the pixel 110a to another element, thus outputting data from the pixel. Transfer transistors may allow associated subsampling. In an embodiment, the pass transistor may be combined (assigned) to a single photodiode, and the source follower, reset and selector transistors may be combined (shared) with multiple photodiodes. In the second embodiment, the transfer transistor may be coupled to a photodiode, and the source follower and reset transistor may be coupled to a plurality of photodiodes. In one embodiment, each pixel 110 includes four transistors. The image sensor element is a 4T CMOS image sensor commonly used in the field. The 4T CMOS image sensor may include a pass transistor, a reset transistor, a source follower transistor, and a selector transistor. In one embodiment, the transistors included in pixel region 110 include a metal oxide semiconductor field effect transistor (MOSFET) having a gate that includes a silicide layer. The silicide layer may include silicides such as nickel silicides, cobalt silicides, tungsten silicides, germanium silicides, titanium silicides, platinum silicides, germanium silicides, palladium silicides, and/or combinations thereof.

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In the peripheral region 120, additional circuitry and inputs/outputs are provided adjacent to the pixel region 110 to provide an operating environment for the pixel 110a and/or to support external communication with the pixel 110a. The peripheral area 120 may also be a logic area as it may include logic circuitry coupled to the pixel 110a. The peripheral area 120 may include low power logic circuitry. The low power logic circuit may include low power, high speed, high performance logic circuits. The peripheral circuit 120 may include, for example, a pixel driving circuit, a circuit for obtaining a signal charge, an A/D converter, a processing circuit for forming an image output signal, an electrical connector to which other elements may be connected, and/or commonly used in the field. Other components. In an embodiment, the peripheral region 120 includes MOSFET elements having source, drain, and gate electrodes, each of which includes a silicide layer. The silicide layer may include silicides such as nickel silicide, cobalt silicide, tungsten silicide, germanium silicide, titanium silicide, platinum silicide, germanium silicide, palladium silicide, and/or combinations thereof.

Referring now to FIG. 2, a cross-sectional view of a conventional image sensor 200 is shown. The image sensor 200 includes a pixel area 210 and a peripheral area 220. The color filter 230 is disposed above the pixel area 210 . The color filter 230 has a plurality of filters including a blue filter 230a, a green filter 230b, a red filter 230c, and a blue filter 230d. The sensor 200 includes a substrate 250 having a sub-layer 250a and an epitaxial layer 250b. A plurality of trenches including trenches 260a, 260b, 260c, and 270 are formed on the substrate 250. The trenches 260a, 260b, and 260c are formed in the pixel area 210. The trench 270 is formed in the peripheral area 220 . The trench 270 is substantially similar to the trenches 260a, 260b, and 260c. For example, the trench 270 and the trenches 260a, 260b, and 260c have substantially the same depth D1. In general, D1 is between 0.3 and 0.6 μ m.

Ditches in the pixel area (including 260a, 260b, and 260c) are used to separate pixels from the second pixel. For example, the trench 260b is used to separate a pixel formed in the substrate 250 (region P2) under the red filter 230c and a substrate 250 formed under the green filter 230b (region P1) pixels. The trench 270 can be used to separate one or more components in the peripheral area. The element 200 has the disadvantage that the trenches 260a, 260b, and/or 260c may not properly separate one pixel region from another. Depths of the trenches 260a, 260b, and/or 260c may not be sufficient to prevent light-generating carriers from the first pixel region (e.g., the region P1) from moving to the second pixel region (e.g., the region P2). This will cause electrical interference with each other and degrade the performance of the sensor 200. Therefore, there is a need for an improved isolation structure.

Referring to FIG. 3, an image sensor element 300 of an embodiment of the present invention is shown. The image sensor 300 includes a substrate 310 having a sub-layer 310a and an epitaxial layer 310b, and a color filter 320 above the substrate 310. The image sensor element 300 may be substantially the same as the image sensor element 100 of FIG. 1 described above. The image sensor element 300 includes a pixel area 302 and a peripheral area 304. A plurality of pixels (not shown) may be formed in the pixel area 302 of the substrate 310. For example, a first

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pixel may be formed in region P3, and a second pixel may be formed in region P4. The pixel includes a photodetector and one or more transistors. One or more pixels of the image sensor element 300 may be substantially similar to the pixels 110a of Figure 1 previously described. The peripheral region 304 may be substantially similar to the peripheral region 120 shown in Figure 1 previously described.

The color filter 320 includes blue filters 320a and 320d, a green filter 320b, and a red filter 320c, although color filters of other embodiments are also possible. In an alternate embodiment, the image sensing element 300 is a backside light emitting sensor. In an embodiment, the color filter 320 is disposed adjacent to the back surface of the substrate 310, and filters light incident on the back side of the substrate 310. One or more micro-lenses (not shown) may be formed adjacent to the color filter 320 with respect to the substrate 310 .

The substrate 310 may be a crystalline silicon. In alternative embodiments, the substrate 310 may include other base semiconductors (e.g., germanium), or may include compound semiconductors (e.g., silicon carbide, gallium arsenide, indium arsenide, and indium phosphide). In one embodiment, the substrate 310 is a P-type substrate (P conductive) (eg, a substrate doped with a P-type dopant (eg, boron or aluminum) with conventional diffusion or ion implantation). In other embodiments, the substrate 310 may include a P+ substrate, an N+ substrate, and/or other conductive types known in the art. The substrate 310 may include a silicon-on-insulator (SOI) substrate. The epitaxial layer 310b allows different doping profiles than other portions of the substrate 310 (including the sub-layer 310a). The epitaxial layer 310b can be grown on the substrate 310 using conventional methods. In one embodiment, the epitaxial layer 310b is a p-epitaxial layer. In one embodiment, the sub-layer 310a is a p+ layer. Possible embodiments include the epitaxial layer 310b is an N-epitaxial layer and the sub-layer 310a is an N+ sub-layer, the epitaxial layer 310b is an N-epitaxial layer and the sub-layer 310a is a P+ sub-layer, and/or Other commonly used conductive types in the field. The thickness T of the epitaxial layer 310b may be between about 2 μ m and 10 μ m. In another embodiment, the thickness T of the epitaxial layer may be approximately 4 μ m.

In one embodiment, the epitaxial layer 310b is a p-type conductivity type, and a photodiode included in a pixel (not shown) formed in the substrate 310 includes an N-type photogeneration region (eg, formed in a P-type region). An epitaxial N-type well photodetector. The N-type light generating region may be formed by doping the substrate with N-type dopants (e.g., phosphorous, arsenic, and/or other N-type dopants commonly used in the described art). The doping may be accomplished using conventional processes known in the art (e.g., lithographic patterning followed by ion implantation or diffusion). In other embodiments, the photodiode includes a pin photodiode. The pin layer may be doped with a p-type dopant. The p-type dopant may include boron, aluminum, and/or other P-type conductivity type dopants commonly used in the art.

An isolation structure including isolation trenches 340 is formed in the peripheral region 304 of the image sensor 300 . The isolation trench 340 may include a shallow trench isolation (STI) structure. The isolation trench 340

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can assist in isolating one or more components formed on the peripheral region 304. The depth D2 of the isolation trench 340 is less than about 0.6 μm. In an embodiment, the depth D2 of the isolation trench 340 is about 0.3 μm to 0.6 μm. A deeper depth D2 (eg, greater than 0.6 μm) may provide a high sheet resistance (Rs) of the N-type well junction located in the peripheral region 304 . A higher Rs detracts from the pick-up function. The isolation trench 340 may include silicon oxide. In one embodiment, the isolation trench 340 may contain air in addition to or in place of silicon oxide. Other embodiments in which the trenches 340 contain other insulating materials are also possible. The isolation trench 340 may be formed by conventional methods commonly used in the art. For example, hole etching is performed in the peripheral region 304 of the substrate 310 using conventional processes such as reactive ion etching (RIE) of a pattern formed according to a conventional photolithography process. The hole can then be filled. For example, in one embodiment, the trenches are filled with silicon oxide. In one embodiment, the process includes high-density plasma chemical vapor deposition (HDPCVD) of silicon oxide to fill holes and then a chemical mechanical polish (CMP) process The oxide is planarized. In alternative embodiments, the process includes Sub-Atmospheric Chemical Vapor Deposition (SACVD) of silicon oxide followed by a chemical mechanical polishing process to planarize the oxide. The method of forming the isolation trench 340 will be discussed later in more detail.

A plurality of isolation structures including isolation trenches 330a, 330b, and 330c are formed in the pixel area 302 of the substrate 310. The isolation trenches 330a, 330b, and 330c may include shallow trench isolation (STI) structures. The isolation trenches 330a, 330b, and/or 330c at least partially isolate the pixels from the second pixels of the pixel area 302. For example, the isolation trench 330b provides blocking barriers from the pixel area P3 to the pixel area P4. The depth D3 of the isolation trenches 330a, 330b and/or 330c is greater than about 0.6 μm. In an embodiment, the isolation trenches 330a, 330b, and/or 330c may have a depth D3 of between about 0.6 μm and 2 μm. In an embodiment, the isolation trenches 330a, 330b and/or 330c may have a depth D3 of between about 0.6 μm and 1 μm. In an embodiment, the isolation trenches 330a, 330b, and/or 330c may have a depth D3 of about 1 μm to 2 μm.

The isolation trenches 330a, 330b, and/or 330c may include (eg, completely fill in or partially fill in) the insulation material. The insulating material (such as silicon oxide) can isolate minority carriers from the pixels to the second pixel. In alternative embodiments, the isolation trenches 330a, 330b, and/or 330c may be filled with an oxide, a substantially optically opaque material, and/or a low-refractive index material, which will be described in detail later with reference to FIG. The isolation trenches 330a, 330b, and/or 330c may be formed using conventional techniques commonly used in the field. For example, hole etching is performed in the pixel region 302 of the substrate 310 using conventional processes such as reactive ion etching (RIE) performed after the pattern formed by a conventional photolithography process. The hole can then be filled. For example, in one embodiment, the trenches are filled with silicon oxide. In one embodiment, the process includes high density plasma chemical vapor deposition of silicon oxide to fill holes, followed by a chemical mechanical polishing process to flatten the oxide. In an alternate embodiment, the process includes sub-atmospheric chemical vapor deposition of silicon oxide followed by a chemical mechanical polishing process to planarize the oxide. The method of forming the isolation trenches 330a, 330b, and 330c will be discussed in more detail later.

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FIG. 4 shows a method 400 of forming an image sensor including an isolation structure. FIGS. 5 a, 5 b, 5 c, 5 d, 5 e, and 5 f show continuous changes of the substrate 500, which correspond to the steps of FIG. 4. The method 400 may be used to fabricate an image sensor element substantially similar to the image sensor 300 described in FIG.

Method 400 begins at step 402 by providing a substrate including a pixel area and a peripheral area. The substrate also includes an epitaxial layer. The substrate provided may be substantially similar to substrate 310 of FIG. 3 previously described. In the example of Fig. 5a, a substrate 500 is provided. Substrate 500 includes a sub-layer 502 and an epitaxial layer 504 . In one embodiment, the sub-layer 502 is a P+ layer and the epi-layer 504 is a P-layer. The substrate 500 further includes a pixel area 500a and a peripheral area 500b. The pixel area 500a may be substantially similar to the pixel area 110 and/or the pixel area 302 shown in FIGS. 1 and 3, respectively. The peripheral region 500b may be substantially similar to the peripheral region 120 and/or the peripheral region 304 shown in FIGS. 1 and 3, respectively.

The method 400 then proceeds to step 404 where a plurality of isolation structures are formed in the pixel area of the substrate. The isolation structure includes isolation trenches. The trenches are formed to a depth greater than about 0.6 μ m. The trenches may be formed using processes commonly used in the art (e.g., lithographic patterning with RIE etching) to form holes (ditches) in the patterned regions. In the example of FIG. 5b, the trench 510 is etched in the substrate 500, and more precisely in the epitaxial layer 504 of the substrate 500. The trench 510 is etched to a depth D4. D4 may be between about 0.6 μ m and 2 μ m.

The method 400 proceeds to step 406 where a layer of insulating material is formed on the substrate. The layer may be made of a deposition material using chemical vapor deposition, Plasma Enhanced Chemical Vapor Deposition (PECVD), Atmospheric Pressure Chemical Vapor Deposition (APCVD), Low Pressure Chemical Vapor Deposition, High Density Plasma Chemical Vapor Deposition, Atomic Layer Chemical Vapor Deposition, Sub-atmospheric Chemical Vapor Deposition (SACVD), and/or other processes commonly used in such fields. In an embodiment, the isolating material is silicon oxide. In an embodiment, the oxide is deposited by HDP CVD or SACVD. The layer may be partially or completely filled with the trenches of the pixel area as previously described with respect to step 404. In the example of FIG. 5c, a conformal insulating layer 520 is deposited on the substrate 500. The insulating layer 520 fills the trench 510, which is now designated isolation trench 510a. The method then proceeds to step 408 where the insulating layer is planarized. In an embodiment, the layer is planarized using a chemical mechanical polishing process. The example of FIG. 5d shows a flattened layer of insulating material 520, so that the insulating material fills completely in the isolation trench 510a and provides a substantial plane of the substrate 500.

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The method 400 proceeds to step 410 where at least one isolation structure is formed in a peripheral region of the substrate. The isolation structure includes isolation trenches. The depth of the trench etch is less than the depth of the trench formed in the pixel region as described in step 404. The etch depth of the trenches may be less than about 0.6 μm. The trenches may be etched using processes commonly used in the art, such as photolithographic patterning followed by RIE etching to form holes (ditches) in accordance with patterned regions. In the example of FIG. 5e, the trench 530 is etched in the peripheral region 500b of the substrate 500, and more precisely in the epitaxial layer 504 of the substrate 500. The trench 530 is etched to a depth D5. D5 is smaller than D4 shown in FIG. 5b. In one embodiment, D5 is less than about 0.6 μm. The method 400 proceeds to step 412 where a conformable layer of insulating material is deposited on the substrate. The layer can be completely or partially filled into the trench of the peripheral area as described in step 410 . The insulating material layer may be Physical Vapor Deposition (PVD) (sputtering), chemical vapor deposition, plasma enhanced chemical vapor deposition, atmospheric pressure chemical vapor deposition, low pressure chemical vapor deposition, high density plasma chemistry Deposition is performed by vapor deposition (HDPCVD), atomic layer chemical vapor deposition, sub-atmospheric pressure chemical vapor deposition (SACVD), and/or other processes commonly used in the art. In an embodiment, the insulating material is silicon oxide. In another embodiment, the oxide is deposited by HDP CVD or SACVD. In the example of FIG. 5f, a conformal topography layer 540 of insulating material is deposited on the substrate 500 and includes filling the trenches 530. The method 400 proceeds to step 414 where the insulating layer is planarized. In one embodiment, the insulating layer is planarized using an electrochemical mechanical polishing process. The example of FIG. 5g shows a planarized layer of insulating material 540, so the insulating material fills in the trench 530 and provides a substantially planar surface of the substrate 500. In an embodiment, the insulating layer 540 includes silicon oxide.

Referring to FIG. 6, a method 600 of manufacturing an image sensor element is shown; FIGS. 7a, 7b, 7c, 7d, and 7e show continuous changes of the substrate 700, which correspond to the steps of FIG. The method 600 may be used to fabricate image sensor elements substantially similar to the image sensor 300 described in FIG.

Method 600 begins in step 602 with providing a substrate including a pixel area and a peripheral area. The substrate also includes an epitaxial layer. The substrate provided may be substantially similar to substrate 310 of FIG. 3 previously described. In the example of FIG. 7a, a substrate 700 is provided. Substrate 700 includes a sub-layer 702 and an epitaxial layer 704 . In an embodiment, the sub-layer 702 is a P+ layer, and the epitaxial layer 704 may be a P-layer. The substrate 700 further includes a pixel area 700a and a peripheral area 700b. The pixel area 700a may be substantially similar to the pixel area 110 and/or the pixel area 302 shown in FIGS. 1 and 3, respectively. The peripheral area 700b may be substantially similar to the peripheral area 120 and/or the peripheral area 304 shown in FIGS. 1 and 3, respectively.

Method 600 then proceeds to step 604 where a plurality of isolation structures are formed in the pixel area of the substrate. The isolation structure includes isolation trenches. The trench may be formed at a depth of the substrate greater than 0.6 μm. The trenches may be formed using processes commonly used in the art, such as

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etching in accordance with the patterned RIE after photolithographic patterning to form holes (ditches). In the example of FIG. 7b, the trench 710 is etched in the substrate 700, and more precisely in the epitaxial layer 704 of the substrate 700. The trench 710 is etched to a depth D6. D6 is greater than 0.6 μm. In one embodiment, D6 is between about 0.6 μm and 2 μm.

The method 600 proceeds to step 606 where at least one isolation structure is formed in a peripheral region of the substrate. The isolation structure includes isolation trenches. The formation depth of the trench may be less than 0.6 μm. The depth of the trench etch is less than the depth of the trench formed in the pixel region in step 604 . The trenches can be formed by processes commonly used in the field, such as photolithographic patterning and RIE etching according to the patterned regions to form holes (ditches). In the example of FIG. 7c, the trench 720 is etched in the peripheral region 700b of the substrate 700. The depth of the trench 720 is D7. D7 is smaller than D6 shown in Fig. 7b. In an embodiment, D7 may be less than 0.6 μm.

The method 600 proceeds to step 608 where a layer of insulating material is formed on the substrate. The layers may be formed by conventional deposition processes such as chemical vapor deposition, plasma enhanced chemical vapor deposition, atmospheric pressure chemical vapor deposition, low pressure chemical vapor deposition, high density plasma chemical vapor deposition (HDPCVD), atomic layer chemical vapor deposition, Pressure Vapor Chemical Vapor Deposition (SACVD) and/or other processes commonly used in the field. In an embodiment, a silicon oxide layer may be formed on the substrate using, for example, HDPCVD or SACVD deposition. The insulating material layer completely or partially fills the trenches formed in steps 606 and 604, respectively, in the peripheral area and the pixel area. In the example of FIG. 7d, a conformal topography layer 730 comprising an insulating material is deposited over the substrate 700 and includes filling the trenches 710 and 720, which are currently designated as isolation trenches 710a and 720a. In an embodiment, the layer 730 includes silicon oxide. The method 600 proceeds to step 610 where the insulating layer is planarized. In an embodiment, the insulating layer is planarized using a chemical mechanical polishing process. The example of FIG. 7e shows a planarized layer of insulating material 730, so the trenches 710a and 720b are filled in and provide a substantially planar surface of the substrate 700.

Referring to FIG. 8, an image sensor 800 is shown. The image sensor 800 includes a substrate 802 having a sub-layer 804 and an epitaxial layer 806, and a color filter 808 above the substrate 802. The image sensor 800 has a pixel area 802a and a peripheral area 802b. The image sensor element 800 may be substantially similar to the image sensor element 300 and/or image sensor 100 shown previously in FIGS. 3 and 1 respectively. Moreover, for example, the substrate 802 may be substantially similar to the substrate 310 shown in FIG. 3; the peripheral region 802b may be substantially similar to the peripheral region 102 shown in FIGS. 1 and 3 respectively. And/or peripheral area 304. The color filter 808 may be substantially similar to the color filter 320 shown in Figure 3 previously described. A plurality of pixels (not shown) may be formed in the pixel area 802a of the substrate 800. The one or more pixels formed on the substrate 802 may be substantially similar to the pixels 110a of Figure 1 previously described.

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An isolation structure including isolation trenches 816 is formed in the peripheral area 802b of the image sensor 800. The isolation trenches 816 may be substantially similar to the isolation trenches 340 shown in Figure 3 previously described. A plurality of isolation structures including isolation trenches 810, 812, and 814 may be formed in the pixel area 802a of the image sensor 800. The isolation trenches 810, 812, and/or 814 may include STI structures. The isolation trenches 810, 812, and/or 814 provide enhanced isolation between the pixels of the pixel area 802a and the second pixels. The depth of the isolation trenches 810, 812 and/or 814 is greater than the isolation trench 816. In one embodiment, the isolation trenches 810, 812, and/or 814 include a depth greater than 0.6 μ m, and the isolation trenches 816 include a depth less than 0.6 μ m.

The isolation trenches 810, 812 and/or 814 may be filled with one or more materials. The isolation trench 810 includes a first layer 810a and a second layer 810b. The isolation trench 812 includes a first layer 812a and a second layer 812b, and the isolation trench includes a first layer 814a and a second layer 814b. The first layers 810a, 812a, and/or 814a of the isolation trench may include a layer of insulating material. The insulating material (e.g. silicon oxide) can assist in isolating the minority carriers from the pixel to the second pixel. In an embodiment, the second layer 810b, 812b and/or 814b of the isolation trenches comprise a substantially optically opaque material. In an embodiment, the opacity of the substantially optically opaque material is greater than about 50%. In the example of the substantially optically opaque material, tungsten and/or other opaque materials including other metal films may be included. The use of a substantially optically opaque material may increase the sensitivity of the image sensor 800 to long wavelength light. In alternative embodiments, the second layers 810b, 812b, and/or 814b comprise a low refractive index material (RI), such as air. In an embodiment, the low RI material includes an RI value of less than about 5 . In an embodiment, the second layers 810b, 812b, and/or 814b may include air gaps in the first layers 810a, 812a, and 814a that have an insulating material. Adding a low RI material allows for increased incident light reflection. The above embodiments are only for illustration and not limitation. Other structures and material combinations are possible.

Therefore, an image sensor element is provided. The element includes a substrate having a pixel area and a peripheral area. Isolation structures are formed in the pixel area of the substrate. The isolation structure includes a trench. Another isolation structure is formed in the peripheral region of the substrate. The isolation structure also includes a trench. The trenches formed in the pixel area have a greater depth than the trenches formed in the peripheral area.

In addition, another image sensor element is provided that includes a substrate having a pixel area and a peripheral area. A plurality of pixels are formed in the substrate of the pixel region. Ditches are formed between two pixels. The trench has a first depth. The second trench is formed in the peripheral region of the substrate. The depth of the second trench is less than the first depth.

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A method of forming an image sensor is also provided. A substrate including a pixel area and a peripheral area is provided. A first isolation trench is formed in a pixel region of the substrate, and forming the first isolation trench includes etching the substrate to a first depth. A second isolation trench is formed in the peripheral region of the substrate. Forming the second isolation trench includes etching the substrate to a second depth, the second depth being less than the first depth.

Although the present invention has been described in detail with respect to some embodiments thereof, it will be apparent to those skilled in the art that various modifications may be made without departing from the novel teachings and advantages of the present disclosure based on the teachings and disclosure of the present invention.

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CLAIMS CN101465361

1.
An image sensor element characterized by comprising:

a substrate including a pixel area and a peripheral area;

a first isolation structure formed in a pixel region of the substrate, wherein the first isolation structure includes a first trench having a first depth; and

A second isolation structure formed in a peripheral region of the substrate, wherein the second isolation structure includes a second trench having a second depth, and wherein the first depth is greater than the second depth.

2.
The element of claim 1 wherein the first isolation structure comprises silicon oxide.

3.
The element of claim 1 wherein the first isolation structure comprises a material selected from the group consisting of insulating materials, substantially optically opaque materials, low refractive index materials, and combinations thereof.

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4.
The element of claim 1 wherein the first depth is greater than about 0.6 μ m.

5.
The element according to claim 1, wherein the substrate comprises an epitaxial layer having a first conductivity type and a substrate layer having a second conductivity type.

6.
The element according to claim 5, wherein said substrate is selected from the group consisting of a substrate of a first conductivity type including p-type and a second conductivity type of p+ type, a first conductivity type including n-type, and n+. The substrate of the second conductivity type includes a group consisting of an n-type first conductivity type and a p+ type second conductivity type substrate.

7.
An image sensor element characterized by comprising:

a substrate including a pixel area and a peripheral area;

a first pixel and a second pixel formed in a pixel region of the substrate;

a first trench isolation structure formed in a pixel region of the substrate and between the first pixel and the second pixel, wherein the first trench isolation structure has a first depth; and

A second trench isolation structure is formed in the peripheral region, the second trench isolation structure has a second depth, and the second depth is less than the first depth.

8.
The element of claim 7, wherein the substrate comprises an epitaxial layer having a first conductivity type, and wherein the first pixel comprises a photodiode having a second conductivity type.

9.
The element of claim 7 wherein the first depth is between about 0.6 μ m and 1 μ m.

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10.

The element of claim 7 wherein the second depth is about 0.6 μ m or less.

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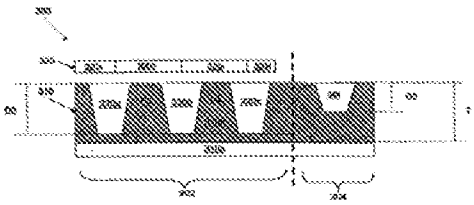
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权利要求书 1 页 说明书 10 页 附图 13 页

[54] 发明名称

图像传感器元件的隔离结构

[57] 摘要

本发明提供一种图像传感器元件，其包含具有像素区域和外围区域的衬底。 第一隔离结构形成于所述衬底的像素区域中。 所述第一隔离结构包含具有第一深度的沟渠。 第二隔离结构形成于所述衬底的外围区域中。 所述第二隔离结构包含具有第二深度的沟渠。 所述第一深度大于所述第二深度。



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1. 一种图像传感器元件，其特征在于包含：

包含像素区域和外围区域的衬底；

形成于所述衬底的像素区域中的第一隔离结构，其中所述第一隔离结构包含具有第一深度的第一沟渠；以及

形成于所述衬底的外围区域中的第二隔离结构，其中所述第二隔离结构包含具有第二深度的第二沟渠，且其中所述第一深度大于所述第二深度。

2. 根据权利要求 1 所述的元件，其特征在于所述第一隔离结构包含氧化硅。

3. 根据权利要求 1 所述的元件，其特征在于所述第一隔离结构包含的材料选自由绝缘材料、实质光学不透明材料、低折射率材料和其组合组成的群组。

4. 根据权利要求 1 所述的元件，其特征在于所述第一深度大于约 0.6 μm。

5. 根据权利要求 1 所述的元件，其特征在于所述衬底包含具第一导电型的外延层和具第二导电型的衬底层。

6. 根据权利要求 5 所述的元件，其特征在于所述衬底选自由包含 p-型的第一导电型和 p+型的第二导电型的衬底、包含 n-型的第一导电型和 n+型的第二导电型的衬底以及包含 n-型的第一导电型和 p+型的第二导电型的衬底组成的群组。

7. 一种图像传感器元件，其特征在于包含：

包含像素区域和外围区域的衬底；

形成于所述衬底的像素区域中的第一像素和第二像素；

第一沟渠隔离结构，其形成于所述衬底的像素区域中，且位于所述第一像素和第二像素之间，其中所述第一沟渠隔离结构具有第一深度；以及

第二沟渠隔离结构，其形成于所述外围区域中，所述第二沟渠隔离结构具有第二深度，所述第二深度小于所述第一深度。

8. 根据权利要求 7 所述的元件，其特征在于所述衬底包含具有第一导电型的外延层，且其中所述第一像素包含具有第二导电型的光电二极管。

9. 根据权利要求 7 所述的元件，其特征在于所述第一深度介于约 0.6 μm 与 1 μm 之间。

10. 根据权利要求 7 所述的元件，其特征在于所述第二深度为约 0.6 μm 或更小。

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图像传感器元件的隔离结构

技术领域

本揭示内容大体上涉及图像传感器，且明确地说，涉及包含集成电路的图像传感器，例如互补金属氧化物半导体（Complementary metal-oxide semiconductor；CMOS）图像传感器和电荷耦合元件（Charge coupled device；CCD）图像传感器。

背景技术

在半导体技术中，图像传感器用来感测投射于所述半导体衬底的曝光量。CMOS 传感器和 CCD 传感器均广泛使用于许多应用，如数码相机。这些图像传感器使用包含光线感测元件的像素矩阵以收集光能量并将图像转换成数字数据。然而，当像素尺寸缩小后，像素的敏感度将减低。另外，像素间的相互干扰（Crosstalk）将增加。相互干扰可减损空间分辨率、减低整体敏感度、提供不良颜色隔离，且可在图像中引入额外的噪声，特别是在色彩校正程序之后。包含这些需要较薄材料层（例如薄介电和金属层）的工艺和薄彩色滤光片可用来改善光学相互干扰。然而，这些传统改善电气相互干扰的方法（例如提供具有薄外延层的传感器）被提供用于例如静电放电（Electrostatic discharge；ESD）失败的其它问题。其它传统图像传感器的问题包含长波长光敏感度和图像缺陷，例如从兴盛效应（Blooming effect）（输出图像的特定区域显示较原始图像为亮）。

因此，需要经改进的图像传感器。

发明内容

本发明提供涉及半导体元件的揭示内容，特别是涉及图像传感器的隔离结构。所提出的新颖结构可以减低像素间的电气相互干扰和其它光学缺陷。

本发明提供一种图像传感器，其具有包含像素区域和外围区域的衬底、形成于所述衬底的像素区域中的第一隔离结构、形成于所述衬底的外围区域中的第二隔离结构。其中所述第一隔离结构包含具有第一深度的第一沟渠，所述第二隔离结构包含具有第二深度的第二沟渠，且其中所述第一深度大于所述第二深度。

换句话说，本发明提供一种图像传感器元件，所述元件包含具有像素区域和外围区域的衬底。隔离结构形成于衬底的像素区域中。所述隔离结构包含沟渠。另一隔离结构形成于所述衬底的外围区域中。所述隔离结构也包含沟渠。形成于像素区域中的沟渠与

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形成于外围区域中的沟渠相比具有较大深度。

另一方面，本发明提供另一种图像传感器元件，所述元件包含具有像素区域和外围区域的衬底。多个像素形成于所述像素区域的衬底中。在两个像素之间形成沟渠。所述沟渠具有第一深度。第二沟渠形成于所述衬底的外围区域中。所述第二沟渠的深度小于第一深度。

又一方面，本发明提供一种形成图像传感器的方法。提供包含像素区域和外围区域的衬底。第一隔离沟渠形成于所述衬底的像素区域中，形成所述第一隔离沟渠包含将所述衬底蚀刻到第一深度。第二隔离沟渠形成于所述衬底的外围区域中。形成所述第二隔离沟渠包含将所述衬底蚀刻到第二深度，所述第二深度小于所述第一深度。

附图说明

本发明所揭示的各方面最佳地由上述详细说明且通过读取附图加以了解。需强调的是，根据工业的标准实践，许多特征并未依照比例绘制。事实上，为了论述的明确，可任意增加或减少各项特征的尺寸。

图 1 是包含像素区域和外围区域的图像传感器的俯视图；

图 2 是包含像素矩阵和外围区域的常规图像传感器的剖视图；

图 3 是实施例的包含像素矩阵和外围区域的图像传感器的剖视图；

图 4 是展示制造图 3 的图像传感器的方法的实施例的流程图；

图 5a 到 5g 是图 4 方法实施例的剖视图；

图 6 是图 3 制造图像传感器方法的另一替代实施例的流程图；

图 7a 到 7e 是图 5 方法实施例的剖视图；以及

图 8 是包含像素矩阵和外围区域的图像传感器的替代实施例的剖视图。

具体实施方式

本揭示内容大体上涉及半导体元件，特别是图像传感器。然而，应了解，提供特定实施例作为范例以教示较广的发明观念，而所属领域的一般技术人员可轻易将本揭示内容的教示应用于其它方法或元件。另外，应了解，本揭示内容中所论述的方法和装置包含一些传统的结构和/或工艺。既然这些结构和工艺在所述领域中是众所周知的，那么将仅以一般详细程度对其进行论述。再者，为了方便和举例，在整个图式中重复参考标号，且所述重复在整个图式中并非指示任何需要的特征或步骤组合。而且，越过第二特征、在第二特征上方或耦合于第二特征形成第一特征在后续叙述中可包含这样的实施例，其中所述第一和第二特征直接接触形成；或可包含在第一与第二特征之间插入形成额外特

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征的实施例，如此所述第一和第二特征或许并非直接接触。再者，在衬底或衬底表面形成特征可包含在衬底表面上方、邻近于衬底表面、直接于衬底表面及/或延伸于衬底表面下方形成特征（例如植入区、沟渠）的实施例。

参看图 1，图像感测元件 100 提供像素区域 110 和外围区域 120。所述像素区域 110 包含像素 110a 的矩阵。在一实施例中，所述图像感测元件 100 可为互补金属氧化物半导体（CMOS）图像传感器（CIS）或主动像素传感器。在替代实施例中，所述图像传感器 100 可为电荷耦合元件（CCD）传感器。所述图像感测元件 100 可为前侧发光传感器或背侧发光传感器。在背侧发光传感器的结构中，被感测的光线入射到衬底背侧，而在衬底前侧形成像素。像素 110a 包含至少一光学检测器（例如光电二极管）以记录光线亮度或强度。在一实施例中，像素 110a 包含接脚光电二极管。各个像素 110a 还包含至少一个晶体管。所述像素 110a 包含复位（reset）晶体管、源极跟随器（source follower）晶体管、选择器（selector）晶体管和/或传输（transfer）晶体管。所述复位晶体管可执行对所述像素 110a 的复位。所述源极跟随器晶体管可允许电压与被观测像素 110a 结合而不移除累积电荷。所述选择器晶体管可以是行选择器晶体管，且当选择器晶体管开启时允许读取单行像素 110a。传输晶体管可将像素 110a 的光检测器中的累积电荷移动到另一元件，因此从像素输出数据。传输晶体管可允许关联的二次采样。在一实施例中，传输晶体管可结合（分派）于单一光电二极管，而源极跟随器、复位和选择器晶体管可结合于（共用于）多个光电二极管。在第二实施例中，传输晶体管可结合于光电二极管，而源极跟随器和复位晶体管可结合于多个光电二极管。在一实施例中，各像素 110 包含 4 个晶体管。所述图像传感器元件是所述领域中常用的 4T CMOS 图像传感器。所述 4T CMOS 图像传感器可包含传输晶体管、复位晶体管、源极跟随器晶体管和选择器晶体管。在一实施例中，包含于像素区域 110 中的晶体管包含金属氧化物半导体场效晶体管（MOSFET），其具有包含硅化物层的栅极。所述硅化物层可包含硅化物，例如镍硅化物、钴硅化物、钨硅化物、钽硅化物、钛硅化物、铂硅化物、铒硅化物、钯硅化物和/或其组合。

在外围区域 120 中，在邻近所述像素区域 110 处提供增加的电路和输入/输出，以提供像素 110a 的操作环境且/或支持与像素 110a 的外在沟通。所述外围区域 120 也可为逻辑区域，如同其可包含结合于像素 110a 的逻辑电路。所述外围区域 120 可包含低功率逻辑电路。所述低功率逻辑电路可包含低功率、高速、高效能逻辑电路。所述外围电路 120 可包含例如依序驱动像素、得到信号电荷的电路、A/D 转换器、形成图像输出信号的处理电路、可连接其它元件的电连接器和/或所述领域中常用的其它构件。在一实施例中，

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所述外围区域 120 包含具有源极、漏极和栅极电极的 MOSFET 元件，其均包含硅化物层。所述硅化物层可包含硅化物，例如镍硅化物、钴硅化物、钨硅化物、钽硅化物、钛硅化物、铂硅化物、铒硅化物、钯硅化物和/或其组合。

现参看图 2，其展示传统的图像传感器 200 的剖视图。所述图像传感器 200 包含像素区域 210 和外围区域 220。彩色滤光片 230 置于所述像素区域 210 上方。所述彩色滤光片 230 具有多个滤光片，包含蓝色滤光片 230a、绿色滤光片 230b、红色滤光片 230c 和蓝色滤光片 230d。所述传感器 200 包含具有次层 250a 和外延层 250b 的衬底 250。包含沟渠 260a、260b、260c 和 270 的多个沟渠形成于衬底 250 上。所述沟渠 260a、260b 和 260c 形成于像素区域 210 中。所述沟渠 270 形成于所述外围区域 220 中。所述沟渠 270 实质上类似于所述沟渠 260a、260b 和 260c。例如，所述沟渠 270 与沟渠 260a、260b 和 260c 具有实质上相同的深度 D1。一般来说，D1 介于 0.3 到 0.6 μm。

像素区域中的沟渠（包含 260a、260b 和 260c）用于分隔像素与第二像素。举例来说，沟渠 260b 用于分隔形成于所述红光滤光片 230c 下方的衬底 250 中（区域 P2）的像素与形成于所述绿光滤光片 230b 下方的衬底 250 中（区域 P1）的像素。所述沟渠 270 可用于分隔外围区域中的一个或一个以上构件。所述元件 200 具有沟渠 260a、260b 和/或 260c 可能无法适当分隔一个像素区域与另一个像素区域的缺点。所述沟渠 260a、260b 和/或 260c 的深度可能不足以防止来自第一像素区域（例如区域 P1）的光产生载子移动到第二像素区域（例如区域 P2）。这将导致电气相互干扰且减损所述传感器 200 的效能。因此，需要一种经改善的隔离结构。

参看图 3，其展示本发明实施例的图像传感器元件 300。所述图像传感器 300 包含具有次层 310a 和外延层 310b 的衬底 310，以及位于所述衬底 310 上方的彩色滤光片 320。所述图像传感器元件 300 可实质上与前述图 1 的图像传感器元件 100 相同。所述图像传感器元件 300 包含像素区域 302 和外围区域 304。多个像素（未图示）可形成于所述衬底 310 的像素区域 302 中。举例来说，第一像素可形成于区域 P3 中，且第二像素可形成于区域 P4 中。所述像素包含光检测器和一个或一个以上晶体管。所述图像传感器元件 300 的一个或一个以上像素可实质上类似于前述图 1 的像素 110a。所述外围区域 304 可实质上类似于前述图 1 所示的外围区域 120。

所述彩色滤光片 320 包含蓝光滤光片 320a 和 320d、绿光滤光片 320b 和红光滤光片 320c，虽然其它实施例的彩色滤光片也是可能的。在替代实施例中，所述图像感测元件 300 是背侧发光传感器。在一实施例中，所述彩色滤光片 320 设于邻近所述衬底 310 的

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背面处，且过滤入射于所述衬底 310 背侧的光线。可形成邻近所述彩色滤光片 320、相对于所述衬底 310 的一个或一个以上微透镜（未图示）。

所述衬底 310 可以是具结晶结构的硅。在替代实施例中，所述衬底 310 可包含其它基础半导体（如锗（germanium）），或可包含化合物半导体（如硅碳化物、镓砷化物、铟砷化物和铟磷化物）。在一实施例中，所述衬底 310 是 P 型衬底（P 导电型）（例如以传统的扩散或离子植入掺杂 P 型掺杂物（如硼或铝）的衬底）。在其它实施例中，所述衬底 310 可包含 P+衬底、N+衬底和/或其它所述领域已知的导电型。所述衬底 310 可包含绝缘层上硅（SOI）衬底。所述外延层 310b 与衬底 310 的其它部分（包含次层 310a）相比允许不同的掺杂形貌。所述外延层 310b 可使用传统方法来成长于所述衬底 310 上。在一实施例中，所述外延层 310b 为 p-外延层。在一实施例中，所述次层 310a 为 p+层。可能的实施例包含所述外延层 310b 为 N-外延层且所述次层 310a 为 N+次层，所述外延层 310b 为 N-外延层且所述次层 310a 为 P+次层，和/或其它所述领域中常用的导电型。外延层 310b 的厚度 T 可介于大约 2 μm 与 10 μm 之间。在另一实施例中，外延层的厚度 T 可大约为 4 μm。

在一实施例中，所述外延层 310b 为 p 型导电型，且形成在衬底 310 中的像素（未图示）中所包含的光电二极管包含具有 N 型光产生区域（例如形成于 P 型外延层的 N 型阱）的光检测器。所述 N 型光产生区域可利用将 N 型掺杂物（如磷、砷和/或其它所述领域常用的 N 型掺杂物）掺杂于所述衬底来形成。所述掺杂可利用所述领域已知的传统工艺（如光刻图案化接着离子植入或扩散）来实现。在其它实施例中，所述光电二极管包含接脚光电二极管。所述接脚层可掺杂 p 型掺杂物。所述 p 型掺杂物可包含硼、铝和/或其它所述领域常用的 P 型导电型掺杂物。

包含隔离沟渠 340 的隔离结构形成于所述图像传感器 300 的外围区域 304 中。所述隔离沟渠 340 可包含浅沟渠隔离（STI）结构。所述隔离沟渠 340 可协助隔离一个或一个以上形成于所述外围区域 304 上的构件。所述隔离沟渠 340 的深度 D2 小于大约 0.6 μm。在一实施例中，所述隔离沟渠 340 的深度 D2 介于大约 0.3 μm 到 0.6 μm。较深的深度 D2（例如大于 0.6μm）可提供位于所述外围区域 304 的 N 型阱接合的高片电阻（Rs）。较高的 Rs 可减损拾取（Pick-up）功能。所述隔离沟渠 340 可包含氧化硅。在一实施例中，除氧化硅以外或替代氧化硅，隔离沟渠 340 可包含空气。所述沟渠 340 包含其它隔离材料的其它实施例也是可行的。所述隔离沟渠 340 可由所述领域中常用的传统方法形成。例如，利用传统的工艺（如根据传统光刻工艺形成的图案的反应式离子蚀刻（RIE））在衬

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底 310 的外围区域 304 中进行孔洞蚀刻。所述孔洞可接着被填满。例如在一实施例中，所述沟渠被填入氧化硅。在一实施例中，所述工艺包含氧化硅的高密度等离子体化学气相沉积（High Density Plasma Chemical Vapor Deposition；HDPCVD）以填入孔洞，并接着进行化学机械抛光（Chemical Mechanical Polish；CMP）工艺以平坦化所述氧化物。在替代实施例中，所述工艺包含氧化硅的次大气化学气相沉积（Sub-Atmospheric Chemical Vapor Deposition；SACVD），并接着进行化学机械抛光工艺以平坦化所述氧化物。形成所述隔离沟渠 340 的方法将随后进行更详细论述。

包含隔离沟渠 330a、330b 和 330c 的多个隔离结构形成于衬底 310 的像素区域 302 中。所述隔离沟渠 330a、330b 和 330c 可包含浅沟渠隔离（STI）结构。所述隔离沟渠 330a、330b 和/或 330c 至少部分将像素与所述像素区域 302 的第二像素隔离。例如，所述隔离沟渠 330b 提供阻隔少数载子从像素区域 P3 到达像素区域 P4。所述隔离沟渠 330a、330b 和/或 330c 的深度 D3 大于大约 0.6μm。在一实施例中，所述隔离沟渠 330a、330b 和/或 330c 可具有介于大约 0.6μm 到 2μm 的深度 D3。在一实施例中，所述隔离沟渠 330a、330b 和/或 330c 可具有介于大约 0.6 μm 到 1 μm 的深度 D3。在一实施例中，所述隔离沟渠 330a、330b 和/或 330c 可具有介于大约 1 μm 到 2μm 的深度 D3。

所述隔离沟渠 330a、330b 和/或 330c 可包含（例如完全填满或部分填入）绝缘材料。所述绝缘材料（如氧化硅）可隔离少数载子从像素到达第二像素。在替代实施例中，所述隔离沟渠 330a、330b 和/或 330c 可填入氧化物、实质光学不透明材料和/或低折射率材料，其将参看图 7 在随后详细叙述。所述隔离沟渠 330a、330b 和/或 330c 可利用所述领域常用的传统技术形成。例如，利用传统的工艺（如执行于传统光刻工艺形成的图案后的反应式离子蚀刻（RIE））在衬底 310 的像素区域 302 中进行孔洞蚀刻。所述孔洞可接着被填满。例如在一实施例中，所述沟渠被填入氧化硅。在一实施例中，所述工艺包含氧化硅的高密度等离子体化学气相沉积以填入孔洞，并接着进行化学机械抛光工艺以平坦化所述氧化物。在替代实施例中，所述工艺包含氧化硅的次大气化学气相沉积，并接着进行化学机械抛光工艺以平坦化所述氧化物。形成所述隔离沟渠 330a、330b 和 330c 的方法将随后进行更详细论述。

图 4 展示形成包含隔离结构的图像传感器的方法 400。图 5a、5b、5c、5d、5e 和 5f 展示衬底 500 的持续改变，其对应于图 4 的步骤。所述方法 400 可用于制造实质上类似于图 3 所述的图像传感器 300 的图像传感器元件。

方法 400 起始于步骤 402，提供包含像素区域和外围区域的衬底。所述衬底还包含

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外延层。所提供的衬底可实质上类似于前述图 3 的衬底 310。在图 5a 的例子中，提供衬底 500。衬底 500 包含次层 502 和外延层 504。在一实施例中，所述次层 502 为 P+层，而外延层 504 可为 P-层。所述衬底 500 进一步包含像素区域 500a 和外围区域 500b。所述像素区域 500a 可实质上类似于图 1 和 3 分别所示的像素区域 110 和/或像素区域 302。所述外围区域 500b 可实质上类似于图 1 和图 3 分别所示的外围区域 120 和/或外围区域 304。

方法 400 接着进行步骤 404，其中在衬底的像素区域中形成多个隔离结构。所述隔离结构包含隔离沟渠。所述沟渠形成的深度大于大约 0.6 μm。所述沟渠可利用所述领域常用的工艺形成（如光刻图案化伴随 RIE 蚀刻）以在图案化区域中形成孔洞（沟渠）。在图 5b 的例子中，沟渠 510 蚀刻于衬底 500 中，而更精确地说是在衬底 500 的外延层 504 中。所述沟渠 510 被蚀刻到深度 D4。D4 可介于大约 0.6 μm 到 2 μm。

方法 400 进行步骤 406，其中在所述衬底上形成绝缘材料层。所述层可由沉积材料制成，其使用化学气相沉积、等离子体增强化学气相沉积（Plasma Enhanced Chemical Vapor Deposition；PECVD）、大气压化学气相沉积（Atmospheric Pressure Chemical Vapor Deposition；APCVD）、低压（Low Pressure）化学气相沉积、高密度等离子体化学气相沉积、原子层（Atomic Layer）化学气相沉积、次气压化学气相沉积（Sub-atmospheric Chemical Vapor Deposition；SACVD）和/或其它所述领域常用的工艺。在一实施例中，所述隔离材料是氧化硅。在一实施例中，所述氧化物由 HDPCVD 或 SACVD 沉积。所述层可部分或完全填入如先前关于步骤 404 所述的像素区域的沟渠。在图 5c 的例子中，顺应形貌的绝缘层 520 沉积于所述衬底 500 上。所述绝缘层 520 填入所述沟渠 510，其现在被指定为隔离沟渠 510a。所述方法接着进行步骤 408，其中将所述绝缘层进行平坦化。在一实施例中，所述层利用化学机械抛光工艺进行平坦化。图 5d 的例子展示平坦化后的绝缘材料层 520，因此所述绝缘材料完全填入所述隔离沟渠 510a 中，且提供衬底 500 的实质平面。

方法 400 进行步骤 410，其中在所述衬底的外围区域中形成至少一隔离结构。所述隔离结构包含隔离沟渠。沟渠蚀刻的深度小于步骤 404 所述形成于像素区域的沟渠的深度。所述沟渠的蚀刻深度可小于大约 0.6 μm。所述沟渠可利用所述领域常用的工艺来蚀刻形成，如光刻图案化后伴随 RIE 蚀刻以根据图案化区域形成孔洞（沟渠）。在图 5e 的例子中，沟渠 530 蚀刻于衬底 500 的外围区域 500b 中，而更精确地说是在衬底 500 的外延层 504 中。所述沟渠 530 被蚀刻到深度 D5。D5 小于图 5b 所示的 D4。在一实施例中，

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D5 小于大约 0.6 μm。所述方法 400 进行到步骤 412，其中在所述衬底上沉积顺应形貌的绝缘材料层。所述层如步骤 410 所述可完全或部分填入所述外围区域的沟渠。所述绝缘材料层可由物理气相沉积（Physical Vapor Deposition：PVD）（溅镀（Sputtering））、化学气相沉积、等离子体增强化学气相沉积、大气压化学气相沉积、低压化学气相沉积、高密度等离子体化学气相沉积（HDPCVD）、原子层化学气相沉积、次气压化学气相沉积（SACVD）和/或其它所述领域常用的工艺进行沉积。在一实施例中，所述绝缘材料是氧化硅。在另一实施例中，所述氧化物由 HDPCVD 或 SACVD 沉积。在图 5f 的例子中，绝缘材料的顺应形貌层 540 沉积在所述衬底 500 上，并包含填入所述沟渠 530。所述方法 400 进行到步骤 414，其中将所述绝缘层进行平坦化。在一实施例中，所述绝缘层利用化学机械抛光工艺进行平坦化。图 5g 的例子展示平坦化后的绝缘材料层 540，因此所述绝缘材料填入所述沟渠 530 中，且提供衬底 500 的实质平面。在一实施例中，所述绝缘层 540 包含氧化硅。

参看图 6，其展示制造图像传感器元件的方法 600；图 7a、7b、7c、7d 和 7e 展示衬底 700 的持续改变，其对应于图 6 的步骤。所述方法 600 可用于制造实质上类似于图 3 所述的图像传感器 300 的图像传感器元件。

方法 600 起始于步骤 602，提供包含像素区域和外围区域的衬底。所述衬底还包含外延层。所提供的衬底可实质上类似于前述图 3 的衬底 310。在图 7a 的例子中，提供衬底 700。衬底 700 包含次层 702 和外延层 704。在一实施例中，所述次层 702 为 P+层，而外延层 704 可为 P-层。所述衬底 700 进一步包含像素区域 700a 和外围区域 700b。所述像素区域 700a 可实质上类似于图 1 和 3 分别所示的像素区域 110 和/或像素区域 302。所述外围区域 700b 可实质上类似于图 1 和图 3 分别所示的外围区域 120 和/或外围区域 304。

方法 600 接着进行步骤 604，其中在衬底的像素区域中形成多个隔离结构。所述隔离结构包含隔离沟渠。所述沟渠可形成于所述衬底的深度大于 0.6 μm。所述沟渠可利用所述领域常用的工艺形成，如在光刻图案化后根据所述图案化 RIE 进行蚀刻，以形成孔洞（沟渠）。在图 7b 的例子中，沟渠 710 蚀刻于衬底 700 中，而更精确地说是在衬底 700 的外延层 704 中。所述沟渠 710 被蚀刻到深度 D6。D6 大于 0.6 μm。在一实施例中，D6 介于大约 0.6 μm 到 2 μm。

方法 600 进行步骤 606，其中在所述衬底的外围区域中形成至少一隔离结构。所述隔离结构包含隔离沟渠。所述沟渠的形成深度可小于 0.6 μm。所述沟渠蚀刻的深度小于

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Method for producing solar cell silicon wafer suede by reactive ion etching and solar cell produced thereby

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Abstract of CN101478013 (A)

The invention relates to a method for fabricating silicon texture of a solar battery by reactive ion etching and a solar battery fabricated by the method. Concretely, the invention relates to a method for carrying out reactive ion etching in a reactive ion etching cavity by using a reactive ion etching gas containing at least two kinds of gas containing halogens and an oxidative gas, and the solar battery fabricated by the method. The silicon texture fabricated by the method has the advantages of uniform structure and low reflectivity.

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[54] 发明名称

一种反应离子刻蚀制备太阳电池硅片绒面的方法以及用该方法制造的太阳电池

[57] 摘要

本发明涉及一种反应离子刻蚀制备太阳电池硅片绒面的方法以及用该法制造的太阳电池。具体而言，涉及通过包含至少两种含卤素的气体和氧化性气体的反应离子刻蚀气体在反应离子刻蚀腔中进行反应离子刻蚀的方法以及用该法制造的太阳电池。用该法制备的硅片绒面均一、反射率低。

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1、一种反应离子刻蚀制备太阳电池硅片绒面的方法，该方法是将硅片放入反应离子刻蚀腔，然后通入反应离子刻蚀气体进行硅片表面刻蚀，其特征在于，所述反应离子刻蚀气体中包含至少两种含卤素的气体和氧化性气体。

2、根据权利要求 1 所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，所述含卤素的气体的总量和氧化性气体的体积比为 3~18 : 5~25。

3、根据权利要求 2 所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，所述含卤素的气体的总量和氧化性气体的体积比为 5~17 : 9~23。

4、根据权利要求 3 所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，所述含卤素的气体的总量和氧化性气体的体积比为 6~15 : 10~19。

5、根据权利要求 1~4 中任意一项所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，所述至少两种含卤素的气体为 Cl_2、CF_4、HBr、C_2F_6、SF_6、F_2、CHF_3 和 NF_3 中的至少两种的任意组合；所述氧化性气体为 O_2 或 O_3。

6、根据权利要求 5 所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，所述至少两种含卤素的气体中至少一种为 Cl_2；所述氧化性气体为 O_2。

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7、根据权利要求 6 所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，所述反应离子刻蚀气体中包含两种含卤素的气体，其中 Cl_2 与另一种含卤素的气体的体积比为 1~6 : 2~12。

8、根据权利要求 7 所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，其中 Cl_2 与另一种含卤素的气体的体积比为 1~5 : 5~11。

9、根据权利要求 8 所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，其中 Cl_2 与另一种含卤素的气体的体积比为 2~5 : 6~10。

10、根据权利要求 1~4 中任意一项所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，所述硅片包括单晶硅片和多晶硅片。

11、根据权利要求 1~4 中任意一项所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，所述反应离子刻蚀气体被激发形成等离子体，并由电场控制其方向。

12、根据权利要求 1~4 中任意一项所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，具体为：把硅片放入反应离子刻蚀腔中，抽真空至 $1.5 \times 10^{-8} \sim 1.5 \times 10^{-1}$ 帕，然后以 300 ~ 1800 毫升/分钟的流量通入含卤素的气体以及以 500~2500 毫升/分钟的流量通入氧化性气体，待腔体内压力稳定后，加射频功率 200 ~ 1500 瓦，刻蚀 0.2 ~ 1.5 分钟，停止供气，抽真空至 $1.5 \times 10^{-8} \sim 1.5 \times 10^{-1}$ 帕，然后以 600 ~ 1500 毫升/分钟的流量通入氮气至 1 个大气压，之后打开工艺腔，将硅片取出。

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13、根据权利要求 1~4 中任意一项所述的反应离子刻蚀制备太阳电池硅片绒面的方法，其特征在于，通过该法制备的硅片的绒面反射率为 7.90%～9.30%。

14、一种太阳电池，其特征在于，该太阳电池中使用的硅片的绒面通过权利要求 1~13 中的任意一项所述的方法制造。

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一种反应离子刻蚀制备太阳电池硅片绒面的方法以及用该方法制造的太阳电池

技术领域

本发明涉及光伏电池制造领域，特别涉及利用反应离子刻蚀进行单晶硅或多晶硅表面制绒的方法以及用该方法制造的太阳电池。

背景技术

在晶体硅太阳电池的制造过程中，由于单晶硅片和多晶硅片与溶液反应不易控制，溶液腐蚀工艺不能在单晶硅和多晶硅表面上产生足够均匀一致和足够低反射率的绒面。利用掩膜腐蚀法制备硅片绒面需要相当复杂的工艺。首先要在硅片上氧化出一层二氧化硅掩膜，然后在掩膜上开一系列大约 4 微米的小孔，再进行酸腐蚀。尽管掩膜腐蚀法可以制备出反射率很低的绒面，由于工艺复杂性，掩膜腐蚀法还不能在工业生产中得到应用。传统方法制造单晶硅绒面一般需要使用与多晶硅制绒不同的设备或工艺，给产品的切换带来困难。另外，溶液腐蚀法需要使用大量的化学品溶液，给减少废液排放或实现零排放带来较大压力。虽然已有反应离子刻蚀技术方面的报道，但是已有的反应离子刻蚀技术采用含一种卤素气体与其他气体的组合制造单晶或多晶绒面，这种方法仍不能得到足够低反射率的绒面，已有技术制备的绒面的反射率在 10%~20%。并且已有的反应离子刻蚀技术制造速度较慢，无法实现每小时 1200 片以上连续制造。

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发明内容

本发明人在研究中，通过大量实验发现：当使用包含至少两种含卤素的气体和氧化性气体的反应离子刻蚀气体进行晶体硅绒面制备时，制备的硅片的绒面，与已有的反应离子刻蚀技术所制备的硅片的绒面相比，绒面的反射率显著地降低，且能够实现大批量连续生产。基于此实验成果，完成了本发明。

因此，本发明的一个目的是提供一种反应离子刻蚀制备太阳电池硅片绒面的方法。

本发明的另一目的是提供一种太阳电池，该电池的基质材料如多晶硅或单晶硅片采用上述方法来制备绒面。

本发明提供的一种反应离子刻蚀制备太阳电池硅片绒面的方法，该方法是将硅片放入反应离子刻蚀腔，然后通入反应离子刻蚀气体进行硅片表面刻蚀，其中，所述反应离子刻蚀气体中包含至少两种含卤素的气体和氧化性气体。

上述方法中，所述含卤素的气体的总量和氧化性气体的体积比为3~18 : 5~25，优选为 5~17 : 9~23，最优选为 6~15 : 10~19。

上述方法中，所述至少两种含卤素的气体为 Cl_2、CF_4、HBr、C_2F_6、SF_6、F_2、CHF_3 和 NF_3 中的至少两种的任意组合；所述氧化性气体为 O_2 或 O_3。

优选地，上述方法中，所述至少两种含卤素的气体中至少一种为 Cl_2；所述氧化性气体为 O_2。

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进一步优选地，所述反应离子刻蚀气体中包含两种含卤素的气体，且 Cl_2 与另一种含卤素的气体的体积比为 1~6 : 2~12，优选为 1~5 : 5~11，最优选为 2~5 : 6~10。

上述方法中，所述硅片包括单晶硅片和多晶硅片。

在上述方法中，所述反应离子刻蚀气体被激发形成等离子体，并由电场控制其方向。

具体地，所述方法为：把硅片放入反应离子刻蚀腔中，抽真空至 1.5×10^{-8} ~ 1.5×10^{-1} 帕，然后，以 300 ~ 1800 毫升/分钟的流量通入含卤素的气体以及以 500~2500 毫升/分钟的流量通入氧化性气体，待腔体内压力稳定后，加射频功率 200 ~ 1500 瓦，刻蚀 0.2 ~ 1.5 分钟，停止供气，抽真空至 1.5×10^{-8} ~ 1.5×10^{-1} 帕，然后以 600 ~ 1500 毫升/分钟的流量通入氮气至 1 个大气压，之后打开工艺腔，将硅片取出。

通过上述方法制备的硅片的绒面反射率在 7.90% ~ 9.30%。

本发明提供的一种太阳电池，其中使用的硅片的绒面通过上述的方法制造。

具体实施方式

本发明提供了一种反应离子刻蚀硅片（包括单晶硅片和多晶硅片）的方法。该反应离子刻蚀方法的特征是：采用包含至少两种含卤素气体与氧化性气体的反应离子刻蚀气体，产生由电场控制方向的等离子体撞击，形成各向异性微观侧壁图形和粗糙表面，撞击出来的微颗粒对部分表面的撞击产生阻挡作用，进一步强化表面粗糙，反应离子刻蚀气体中的氧化和化学活性基团同时与单晶硅片或多晶硅片表面产生

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氧化和腐蚀化学反应，使硅原子受物理撞击脱离硅片表面更容易，加速粗糙表面的形成。这样，在硅片表面形成非常均匀一致的绒面。这种绒面表面反射率比已有技术制造的绒面反射率更低，本发明制造的绒面反射率在 7.90%～9.30%。并且本发明的制造速度快，可以实现每小时 2500 片以上的连续制造。

本发明的制绒过程是一个反应离子刻蚀过程。本发明的反应离子刻蚀过程是把硅片放入一种等离子体气氛中刻蚀。本发明所使用的等离子体是由至少两种含卤素的气体和氧化性气体经过激发所形成。所述含卤素的气体选自 Cl_2、CF_4、HBr、C_2F_6、SF_6、F_2、CHF_3 和 NF_3 中；所述氧化性气体包括 O_2 或 O_3。优选地，所述含卤素的气体中至少一种为 Cl_2；所述氧化性气体为 O_2。例如，本发明所使用的含卤素气体以及氧化性气体可以是 Cl_2 和 SF_6 以及 O_2。但本发明的含卤素气体以及氧化性气体并不局限于 Cl_2 和 SF_6 以及 O_2。本发明例如，还可以使用 CF_4、C_2F_6 以及 O_2 或者 NF_3、HBr 以及 O_3 的混合物。

当把硅片放入反应离子刻蚀腔中，抽真空至 1.5×10^{-8} ～ 1.5×10^{-1} 帕，以 300～1800 毫升/分钟的流量通入含卤素的气体（其中，以 100～600 毫升/分钟的流量通入 Cl_2 和以 200 ～ 1200 毫升/分钟的流量通入另一种含卤素化合物气体）以及以 500~2500 毫升/分钟的流速通入氧化性气体，待腔体内压力稳定后，加射频功率 200～1500 瓦，刻蚀 0.2～1.5 分钟，停止供气，抽真空至 1.5×10^{-8} 到 ～ 1.5×10^{-1} 帕，以 600~1500 毫升/分钟的流速通入氮气至 1 个大气压，打开工艺腔，将硅片取出。硅片表面被受控的等离子体撞击并发生反应。由于等离子体方向受控，部分微观表面的受撞击程度和反应生成气化产物的速度快于相邻微观

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表面。所以形成受控形貌均匀一致的绒面。绒面的大小可以通过气体种类，加工功率和反应离子刻蚀时间来调节。

所述方法中，所述的激发是通过射频方法或装置达到的。

所述方法中，所述的射频是通过通电形成高频交流变化的电磁波方法或装置达到的。

所述方法中，所述的等离子体方向可控是通过阳极和阴极极化方法或装置达到的。

硅片在经过本发明的反应离子刻蚀后，表面形成了大小为 0.1～15 微米的尺寸可控的绒面。这种绒面能非常有效的降低硅片表面的反射率。使包括利用该法制造硅片绒面的太阳电池的转换效率大大提高。

另外，由于本发明的反应离子刻蚀处理过程有效地去除损伤层的缺陷和杂质，因而可以提高晶体硅太阳电池的转换效率。再有，本发明的反应离子刻蚀形成尺寸可控的均匀一致绒面，并且实现了硅片的单面制绒，背面制成平整光滑的表面。因此本发明的反应离子刻蚀绒面有效地避免了表面高低不平的现象。所以本发明所制得的绒面对后续工艺，特别对正面电极印刷和形成高质量的背场，有很好的帮助。从而进一步提高了硅片太阳电池的转换效率。由于在制绒过程中反应物和生成物均为气态，因而不存在液态腐蚀制绒对硅片的机械冲击损伤。这不仅提高了硅太阳电池的机械强度，大大降低碎片率，也有助于提高电流密度，即提高了硅片太阳电池的转换效率。由于在制绒过程中反应物和生成物均为气态，排放物用洗气装置即可很容易实现符合环保要求的排放。

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实施例 1

将 156 × 156 平方毫米的 P 型多晶硅片放入反应离子刻蚀腔，抽真空至 1.1×10^{-2} 帕，以 160 毫升/分钟的流量通入 Cl_2 和以 370 毫升/分钟的流量通入 CF_4 以及以 930 毫升/分钟的流量通入 O_2，待腔体内压力稳定后，加射频功率 675 瓦，刻蚀 0.3 分钟，停止供气，抽真空至 1.1×10^{-2} 帕，然后以 870 毫升/分钟的流量通入氮气至 1 个大气压，打开工艺腔，将硅片取出。制得硅片的绒面反射率 7.99%。然后把该多晶硅片进行扩散、去边、沉积钝化膜、印刷、烧结，制成太阳电池。该太阳电池的转换效率、填充因子、开路电压和短路电流分别为 16.33%、0.79、624 毫伏和 8.09 安培。而用现有技术的反应离子刻蚀法制备的硅片绒面得到的太阳电池的各项参数为 15.50%、0.73、602 毫伏和 7.01 安培。

实施例 2

将 156 × 156 平方毫米的 P 型多晶硅片放入反应离子刻蚀腔，抽真空至 1.6×10^{-3} 帕，以 230 毫升/分钟的流量通入 Cl_2 和以 350 毫升/分钟的流量通入 HBr 以及以 520 毫升/分钟的流量通入 O_3，待腔体内压力稳定后，加射频功率 330 瓦，刻蚀 0.2 分钟，停止供气，抽真空至 1.6×10^{-3} 帕，然后以 920 毫升/分钟的流量通入氮气至 1 个大气压，打开工艺腔，将硅片取出。制得硅片的绒面反射率 7.90%。然后把该多晶硅片制成太阳电池。该太阳电池的转换效率、填充因子、开路电压和短路电流分别为 16.47%、0.79、623 毫伏和 8.12 安培。

实施例 3

将 156 × 156 平方毫米的 P 型多晶硅片放入反应离子刻蚀腔，抽真空至 1.7×10^{-2} 帕，以 310 毫升/分钟的流量通入 Cl_2 和以 570 毫升/分钟

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的流量通入 C_2F_6 以及以 620 毫升/分钟的流量通入 O_2，待腔体内压力稳定后，加射频功率 730 瓦，刻蚀 0.6 分钟，停止供气，抽真空至 1.7×10^{-2} 帕，然后以 920 毫升/分钟的流量通入氮气至 1 个大气压，打开工艺腔，将硅片取出。制得硅片的绒面反射率 7.93%。然后把该多晶硅片制成太阳电池。该太阳电池的转换效率、填充因子、开路电压和短路电流分别为 16.27%、0.79、623 毫伏和 8.01 安培。

实施例 4

将 156 × 156 平方毫米的 P 型多晶硅片放入反应离子刻蚀腔，抽真空至 1.2×10^{-3} 帕，以 150 毫升/分钟的流量通入 Cl_2 和以 690 毫升/分钟的流量通入 SF_6 以及以 870 毫升/分钟的流量通入 O_2，待腔体内压力稳定后，加射频功率 573 瓦，刻蚀 0.5 分钟，停止供气，抽真空至 1.2×10^{-3} 帕，然后以 790 毫升/分钟的流量通入氮气至 1 个大气压，打开工艺腔，将硅片取出。制得硅片的绒面反射率 9.30%。然后把该多晶硅片制成太阳电池。该太阳电池的转换效率、填充因子、开路电压和短路电流分别为 15.70%、0.77、609 毫伏和 7.95 安培。

实施例 5

将 156 × 156 平方毫米的 P 型多晶硅片放入反应离子刻蚀腔，抽真空至 1.0×10^{-3} 帕，以 155 毫升/分钟的流量通入 F_2 和以 670 毫升/分钟的流量通入 CHF_3 以及以 860 毫升/分钟的流量通入 O_2，待腔体内压力稳定后，加射频功率 570 瓦，刻蚀 0.6 分钟，停止供气，抽真空至 1.1×10^{-3} 帕，然后以 760 毫升/分钟的流量通入氮气至 1 个大气压，打开工艺腔，将硅片取出。绒面反射率 8.20%。然后把该多晶硅片制成太阳

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电池。该太阳电池的转换效率、填充因子、开路电压和短路电流分别为 16.43%、0.79、623 毫伏和 8.02 安培。

实施例 6

将 125 × 125 平方毫米的 P 型单晶硅片放入反应离子刻蚀腔，抽真空至 1.5×10^{-2} 帕，以 170 毫升/分钟的流量通入 Cl_2 和以 550 毫升/分钟的流量通入 SF_6 以及以 730 毫升/分钟的流量通入 O_2，待腔体内压力稳定后，加射频功率 590 瓦，刻蚀 0.2 分钟，停止供气，抽真空至 1.5×10^{-2} 帕，然后以 750 毫升/分钟的流量通入氮气至 1 个大气压，打开工艺腔，将硅片取出。制得硅片的绒面反射率 9.23%。然后把该单晶硅片制成太阳电池。该太阳电池的转换效率、填充因子、开路电压和短路电流分别为 17.0%、0.77、608 毫伏和 5.6 安培。

SAMSUNG EX. 1002 - 566/1684

Espacenet

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Corrosive liquid for preparing monocrystal silicon textured surface and method thereof

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Classification: **- international:** ***C23F1/32***
- cooperative:

Application number: CN2009191826 20090826

Priority number (s): CN2009191826 20090826

Abstract of CN101634026 (A)

The invention relates to a corrosive liquid for preparing monocrystal silicon textured surfaces and a method thereof. The corrosive liquid comprises an alkali solution, sodium silicate and isopropanol, and is characterized by also comprising a perfluoro octoate aqueous solution, wherein the perfluoro octoate aqueous solution has the volume percent of 0.2-1 percent and the concentration within a range of 5*10<-5>-5*10<-3>mol/L; the alkali solution has the mass percent of 1-2.5 percent, the sodium silicate has the mass percent of 0.1-2 percent, and the isopropanol has the volume percent of 0.3-2 percent; and the alkali solution is sodium hydroxide or potassium hydroxide or sodium carbonate. The corrosive liquid has low cost, pyramids formed on the prepared monocrystal silicon textured surfaces have small and uniform sizes, and the corrosive liquid is favorable for solar energy absorption and can be widely applied to the field of solar batteries.

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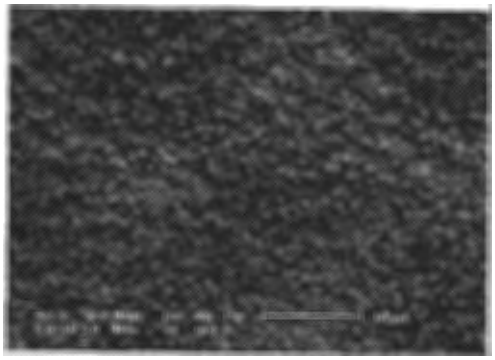
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权利要求书 1 页 说明书 3 页 附图 2 页

[54] 发明名称

一种制备单晶硅绒面的腐蚀液及方法

[57] 摘要

本发明涉及一种制备单晶硅绒面的腐蚀液及方法，它包括碱溶液、硅酸钠和异丙醇，其特征在于：它还包括体积百分比为 0.2% ~ 1%浓度范围为 $5*10^{-5}$ ~ $5*10^{-3}$ mol/L 的全氟辛酸盐水溶液；所述碱溶液的质量百分比为 1% ~ 2.5%，所述硅酸钠的质量百分比为 0.1% ~ 2%，所述异丙醇的体积百分比为 0.3% ~ 2%；所述碱溶液为氢氧化钠或氢氧化钾或碳酸钠。本发明成本低，制备出的单晶硅绒面上形成的金字塔尺寸小，且均匀，利于太阳能吸收，可以广泛应用在太阳能电池领域中。



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1、一种制备单晶硅绒面的腐蚀液，它包括碱溶液、硅酸钠和异丙醇，其特征在于：它还包括体积百分比为 0.2%～1%浓度范围为 $5*10^{-5}$～$5*10^{-3}$mol/L 的全氟辛酸盐水溶液。

2、如权利要求 1 所述的一种制备单晶硅绒面的腐蚀液，其特征在于：所述碱溶液的质量百分比为 1%～2.5%，所述硅酸钠的质量百分比为 0.1%～2%，所述异丙醇的体积百分比为 0.3%～2%。

3、如权利要求 1 所述的一种制备单晶硅绒面的腐蚀液，其特征在于：所述碱溶液为氢氧化钠或氢氧化钾或碳酸钠。

4、一种使用如权利要求 1～3 中任一项所述的腐蚀液制备单晶硅绒面的方法，其特征在于：将未清洗的或粗抛的 P 型或 N 型单晶硅放入所述腐蚀液中进行腐蚀反应，反应温度范围为 75～85℃，腐蚀时间范围为 5～18min。

5、如权利要求 4 所述的一种制备单晶硅绒面的方法，其特征在于：经腐蚀反应后的所述单晶硅表面形成金字塔边长为 0.5～8μm 均匀的绒面。

6、如权利要求 4 或 5 所述的一种制备单晶硅绒面的方法，其特征在于：被腐蚀掉的单晶硅厚度为 5～15μm。

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一种制备单晶硅绒面的腐蚀液及方法

技术领域

本发明涉及一种太阳能电池技术领域，特别是关于一种制备单晶硅绒面的腐蚀液及方法。

背景技术

低成本、高效率的太阳能电池一直是人们追逐的焦点，目前单晶硅太阳能电池表面织构化是提高太阳能电池转换效率的有效手段之一。通常，织构化的方法主要是碱腐蚀法，碱腐蚀法是在碱腐蚀液中加入各种缓冲液，比如异丙醇、乙醇、硅酸钠等来控制反应速度，以得到具有微米量级金字塔形貌的绒面，金字塔形貌的尺寸越小，越均匀，单晶硅的吸光能力越强，太阳能电池的转换效率也就越高。目前，大规模太阳能电池生产上主要使用异丙醇作为缓冲液，浓度通常采用 5%～10%。但是，由于异丙醇成本较高，挥发性大，用量大，而且在生产过程中需要不断的补充溶液，从而导致成本升高。而且上述腐蚀液使得单晶硅腐蚀掉的厚度偏大，厚度越来越薄脆，易断裂也会使生产成本进一步提高。

发明内容

针对上述问题，本发明的目的是提供一种成本低、优质的制备单晶硅太阳能电池绒面的腐蚀液及方法。

为实现上述目的，本发明采取以下技术方案：一种制备单晶硅绒面的腐蚀液，它包括碱溶液、硅酸钠和异丙醇，其特征在于：它还包括体积百分比为 0.2%～1%浓度范围为 $5*10^{-5}$～$5*10^{-3}$mol/L 的全氟辛酸盐水溶液。

所述碱溶液的质量百分比为 1%～2.5%，所述硅酸钠的质量百分比为 0.1%～2%，所述异丙醇的体积百分比为 0.3%～2%。

所述碱溶液为氢氧化钠或氢氧化钾或碳酸钠。

一种使用上述腐蚀液制备单晶硅绒面的方法，其特征在于：将未清洗的或粗抛的 P 型或 N 型单晶硅放入所述腐蚀液中进行腐蚀反应，反应温度范围为 75～85℃，腐蚀时间范围为 5～18min。

经腐蚀反应后的所述单晶硅表面形成金字塔边长为 0.5～8μm 均匀的绒面。

被腐蚀掉的单晶硅厚度为 5～15μm。

本发明由于采取以上技术方案，其具有以下优点：1、本发明由于将全氟辛酸盐溶液加入了由碱溶液、硅酸钠和异丙醇混合的溶液内，全氟辛酸盐作为一种

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阴离子中性表面活性剂，具有非常高的热力学稳定性、化学稳定性以及很好的相容性，而且能够在极低的溶液浓度下将水溶液的表面张力降到很低，增强浸润效果，因此在各种 PH 值范围、各类水性、溶剂型体系中性质稳定，无需短时间补液，因此节约了成本。2、由于本发明采用的全氟辛酸盐浓度极低，其用量与其它缓冲液相比，用量很少，因此进一步节省了成本。3、本发明的腐蚀液中由于采用了全氟辛酸盐溶液作为缓冲液，因此仅花费了 5～18min 的反应时间，得到了金字塔边长为 0.5～8μm 均匀的绒面，比较常规织构化时间 25～35min 有很大的降低，大大地提高了生产效率。4、本发明方法制备出的单晶硅腐蚀掉的厚度为 5～15μm，得到的单晶硅表面为金字塔边长为 0.5～8μm 均匀的绒面，因此有利于太阳光的吸收，得到了优质的单晶硅绒面。本发明降低了生产成本，制备出的单晶硅太阳能电池绒面大大提高了太阳能电池的转换效率，并能广泛应用在太阳能电池生产领域中。

附图说明

图 1 是在金相显微镜下经放大 400 倍的单晶硅绒面形貌图

图 2 是在扫描电镜下经放大 488 倍的单晶硅绒面形貌图

图 3 是在扫描电镜下经放大 977 倍的单晶硅绒面形貌图

具体实施方式

下面结合附图和实施例对本发明进行详细的描述。

本发明的腐蚀液包括质量百分比为 1%～2.5%的碱溶液，质量百分比为 0.1%～2%的硅酸钠，体积百分比为 0.3%～2%的异丙醇和体积百分比为 0.2%～1%浓度范围为 $5*10^{-5}$～$5*10^{-3}$mol/L 的全氟辛酸盐水溶液。上述碱溶液可以采用氢氧化钠或氧氢化钾或碳酸钠等。

使用本发明腐蚀液制备单晶硅绒面的方法如下：

首先，在 75～85℃恒温槽内配制腐蚀液，在体积百分比为 1%～2.5%的碱溶液和质量百分比为 0.1%～2%的硅酸钠混合溶液内加入浓度为 $5*10^{-5}$～$5*10^{-3}$mol/L 全氟辛酸盐溶液，使全氟辛酸盐溶液的体积百分比为 0.2%～1%。等恒温后，加入 0.3%～2%的异丙醇，把未清洗的或粗抛的 P 型或 N 型单晶硅片置入花篮内，一并放入溶液中，5～18min 后取出，直接用去离子水冲洗干净。如图 1～3 所示，在显微镜和扫描电镜下观察到单晶硅片上形成的金字塔边长为 0.5～8μm 均匀的绒面，单晶硅腐蚀掉的厚度为 5～15μm。本实施例中，单晶硅片采用的是市售 P 型或 N 型，<100>晶向单晶硅衬底，电阻率 0.5～7Ω cm，厚度 180～500μm。

以下通过几个具体实施例对本发明进行进一步验证。

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实施例 1：

如图 1～3 所示，图 1～3 为恒温槽的温度为 75℃，碱溶液为 1.5（%质量百分比）氢氧化钠，0.12（%质量百分比）硅酸钠，0.5（%体积百分比）异丙醇，0.5（%体积百分比）浓度为 $5*10^{-5}$～$5*10^{-3}$mol/L 的全氟辛酸盐水溶液，且腐蚀时间为 18min 时，得到的具有金字塔绒面的单晶硅，在显微镜下观察到单晶硅的表面上形成了均匀的金字塔绒面（如图 1 所示），且金字塔的边长为 0.5～8μm（如图 2、图 3 所示），单晶硅上被腐蚀掉的厚度为 10μm。

实施例 2：

当恒温槽的温度为 85℃，碱溶液为 1.5（%质量）氢氧化钠，0.12（%质量）硅酸钠，0.5（%体积）异丙醇，0.5（%体积）浓度为 $5*10^{-5}$～$5*10^{-3}$mol/L 的全氟辛酸盐水溶液，且腐蚀时间为 7min 时，得到的单晶硅绒面上金字塔的边长为 0.5～8μm，单晶硅上被腐蚀掉的厚度为 10μm。

本发明中采用的全氟辛酸盐为一种阴离子中性表面活性剂，其具有非常高的热力学和化学稳定性，可在强酸、强碱、强氧化介质等特殊应用体系中稳定有效地发挥其表面活性剂作用，不会与体系发生反应或分解；全氟辛酸盐还具有很好的相容性，可以广泛用于各种 PH 值范围、各类水性、溶剂型体系，并能与体系中其它表面活性剂和组份很好地相容，即使在极低的溶液浓度下，全氟辛酸盐也可以将水溶液的表面张力降到很低，增强浸润性。

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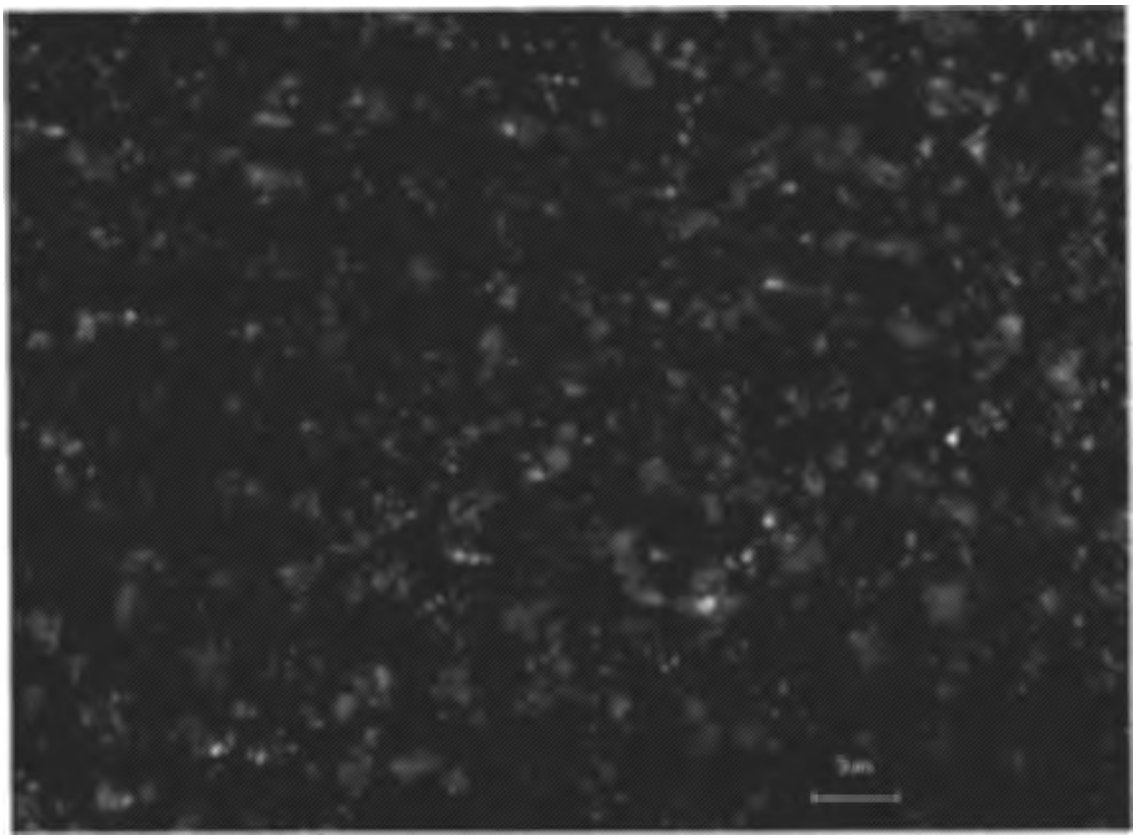


图 1

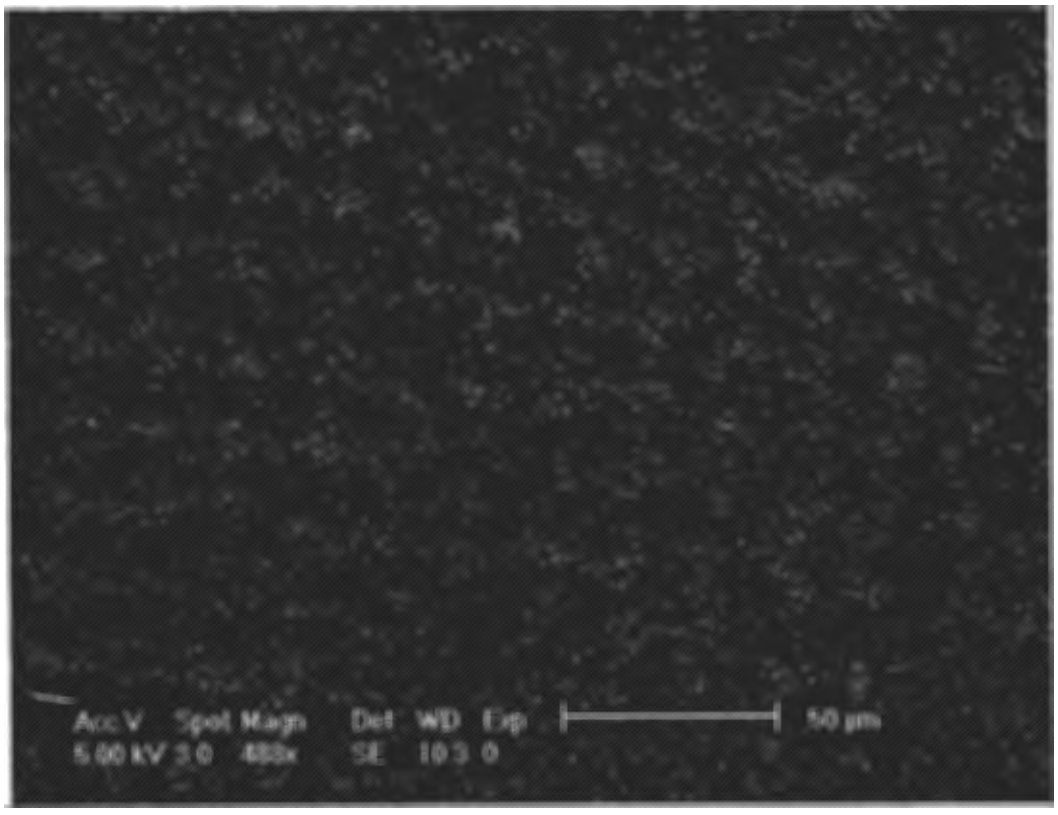


图 2

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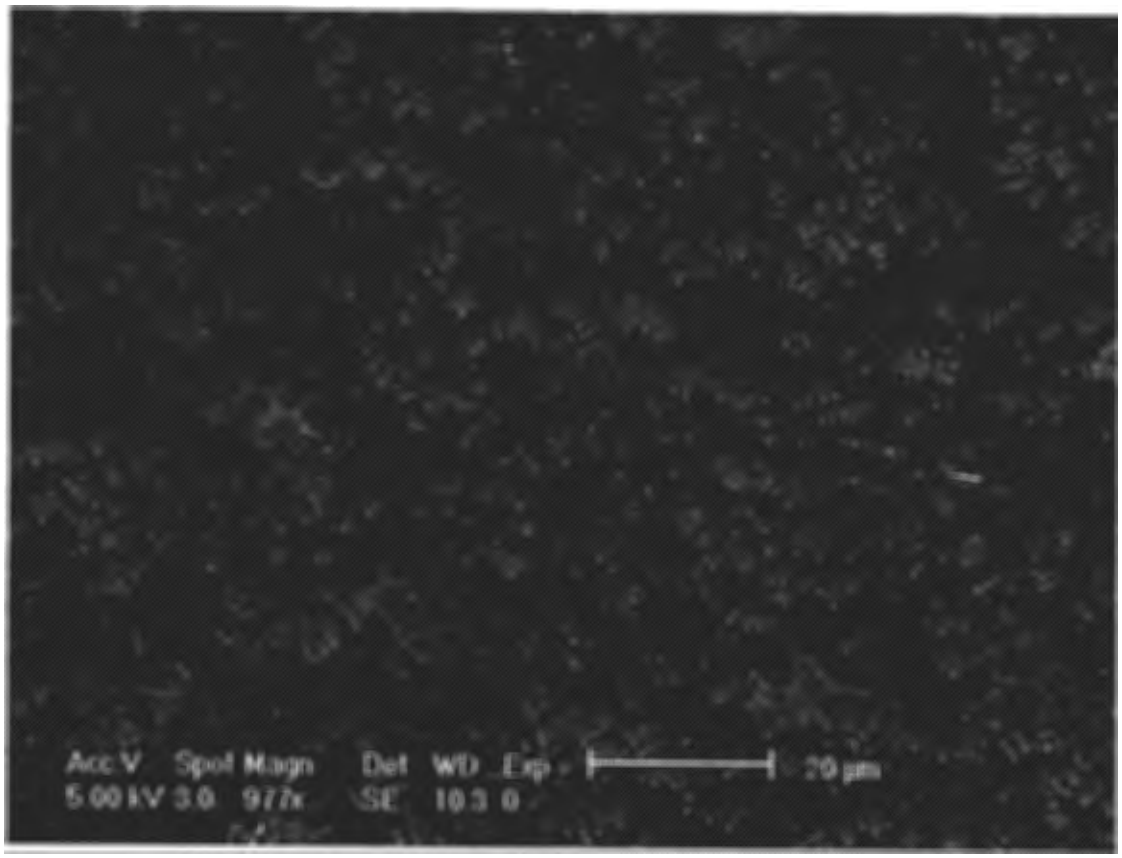


图 3

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Bibliographic data: CN101634027 (A) — 2010-01-27

Method for preparing monocrystal silicon textured surface

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Applicant(s): BEIJING SOLAR ENERGY RES INST ± (BEIJING SOLAR ENERGY RESEARCH INSTITUTE CO., LTD)

Classification: **- international:** ***C23F1/32***
- cooperative:

Application number: CN2009191827 20090826

Priority number (s): CN2009191827 20090826

Abstract of CN101634027 (A)

The invention relates to a method for preparing monocrystal silicon textured surfaces, which comprises the following steps: (1). preparing alkali corrosive liquid comprising an alkali solution, sodium silicate and isopropanol in a thermostatic bath at the temperature of 75-85DEG C, wherein the alkali solution has the volume percent of 1-2.5 percent, the sodium silicate has the mass percent of 0.1-2 percent, and the isopropanol has the mass percent of 0.5-3 percent; (2). adding a perfluorooctyl sulfonate solution with the concentration of 5*10<-5>-5*10<-3>mol/L into the thermostatic bath filled with the alkali corrosive liquid in step 1 such that the volume percent of perfluorooctyl sulfonate solution is 0.2-1 percent, simultaneously putting monocrystal silicon into the thermostatic bath for corrosion reaction, taking out the monocrystal silicon after 10-20 minutes, flushing with deionized water and drying. Pyramids formed on the prepared monocrystal silicon textured surfaces have small and uniform sizes, and the method is favorable for improving the efficiency of solar batteries and can be used for the large-scale production of the solar batteries.

[19] 中华人民共和国国家知识产权局

[51] Int. Cl.
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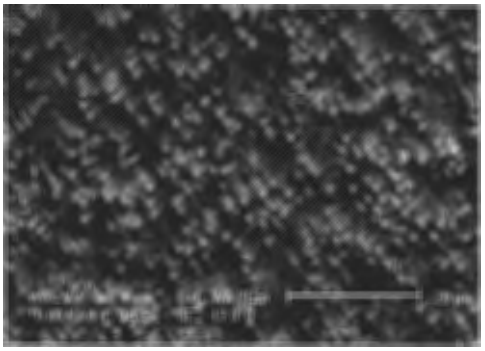
[22] 申请日 2009.8.26
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权利要求书 1 页 说明书 3 页 附图 1 页

[54] 发明名称

一种制备单晶硅绒面的方法

[57] 摘要

本发明涉及一种制备单晶硅绒面的方法，它包括以下步骤：1)在 75℃～85℃恒温槽内配制包括碱溶液、硅酸钠和异丙醇的碱腐蚀溶液，其中，碱溶液的体积百分比为 1%～2.5%，硅酸钠的质量百分比为 0.1%～2%，异丙醇的质量百分比为 0.5%～3%；2)将浓度为 $5*10^{-5}$～$5*10^{-3}$mol/L 的全氟辛基磺酸盐溶液加入步骤 1)中配制有碱腐蚀溶液的恒温槽中，使全氟辛基磺酸盐溶液的体积百分比为 0.2～1%，同时将单晶硅放入恒温槽中进行腐蚀反应，10～20min 后，将单晶硅取出，用去离子水冲洗干净并烘干。本发明制备出的单晶硅绒面上的金字塔尺寸小且均匀，有利于提高太阳能电池的效率，用于大规模的太阳能电池生产中。



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1、一种制备单晶硅绒面的方法，它包括以下步骤：

1）在75℃～85℃恒温槽内配制包括碱溶液、硅酸钠和异丙醇的碱腐蚀溶液，其中，碱溶液的体积百分比为1%～2.5%，硅酸钠的质量百分比为0.1%～2%，异丙醇的质量百分比为0.5%～3%；

2）将浓度为$5*10^{-5}$～$5*10^{-3}$mol/L的全氟辛基磺酸盐溶液加入步骤1）中配制有碱腐蚀溶液的恒温槽中，使全氟辛基磺酸盐溶液的体积百分比为0.2～1%，同时将单晶硅放入恒温槽中进行腐蚀反应，10～20min后，将单晶硅取出，用去离子水冲洗干净并烘干。

2、如权利要求1所述的一种制备单晶硅绒面的方法，其特征在于：所述步骤1）中的碱溶液为氢氧化钠或氢氧化钾或碳酸钠溶液。

3、如权利要求1所述的一种制备单晶硅绒面的方法，其特征在于：恒温槽的温度为80℃且碱溶液为氢氧化钠时，所述单晶硅经碱腐蚀溶液腐蚀后的表面上形成了均匀的金字塔绒面，且金字塔的边长为1～8μm。

4、如权利要求2所述的一种制备单晶硅绒面的方法，其特征在于：恒温槽的温度为80℃且碱溶液为氢氧化钠时，所述单晶硅经碱腐蚀溶液腐蚀后的表面上形成了均匀的金字塔绒面，且金字塔的边长为1～8μm。

5、如权利要求1或2或3或4所述的一种制备单晶硅绒面的方法，其特征在于：恒温槽的温度为80℃且碱溶液为氢氧化钠时，所述单晶硅上被腐蚀掉的厚度为5～15μm。

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一种制备单晶硅绒面的方法

技术领域

本发明涉及一种太阳能电池技术领域，特别是关于一种制备单晶硅绒面的方法。

背景技术

近年来，由于能源与环境日趋紧张的问题，促使了太阳能电池光伏组件行业的飞速发展。降低生产成本、提高太阳能电池的效率是目前研究的重中之重，提高太阳能电池效率的有效方法之一是提高太阳能电池的吸光能力，而吸光能力主要取决于单晶硅表面形成的绒面上金字塔的尺寸大小和均匀性。绒面上的金字塔尺寸越小、越均匀，则单晶硅绒面的吸光能力越强，转换效率则越高。现有制备单晶硅绒面的方法主要包括机械刻槽法、离子刻蚀法和化学腐蚀法等。其中，机械刻槽法和离子刻蚀法存在种种弊端，很少应用于工业生产。目前常用的方法是化学腐蚀法，该方法是利用单晶硅的各向异性特性，对单晶硅进行腐蚀，得到具有微米量级金字塔形貌的单晶硅绒面。在利用化学腐蚀法进行生产的过程中，通常需要加入各种缓冲液，比如：异丙醇、乙醇、硅酸钠等，来控制反应速度，以得到更为优质的单晶硅绒面。由于异丙醇可以使制备出的单晶硅更为美观，因此异丙醇在大规模太阳能电池生产中常被使用，但是异丙醇挥发性大，在生产过程中需要不断地补液，耗费大，成本较高。

发明内容

针对上述问题，本发明的目的是提供一种低成本的制备单晶硅绒面的方法，该方法制备出的单晶硅绒面上的金字塔尺寸小且均匀，有利于提高太阳能电池的效率。

为实现上述目的，本发明采取以下技术方案：一种制备单晶硅绒面的方法，它包括以下步骤：1）在75℃～85℃恒温槽内配制包括碱溶液、硅酸钠和异丙醇的碱腐蚀溶液，其中，碱溶液的体积百分比为 1%～2.5%，硅酸钠的质量百分比为0.1%～2%，异丙醇的质量百分比为 0.5%～3%；2）将浓度为 $5*10^{-5}$～$5*10^{-3}$mol/L的全氟辛基磺酸盐溶液加入步骤1）中配制有碱腐蚀溶液的恒温槽中，使全氟辛基磺酸盐溶液的体积百分比为0.2～1%，同时将单晶硅放入恒温槽中进行腐蚀反应，10～20min后，将单晶硅取出，用去离子水冲洗干净并烘干。

所述步骤1）中的碱溶液为氢氧化钠或氢氧化钾或碳酸钠溶液。

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恒温槽的温度为 80℃且碱溶液为氢氧化钠时，所述单晶硅经碱腐蚀溶液腐蚀后的表面上形成了均匀的金字塔绒面，且金字塔的边长为 1～8μm。

恒温槽的温度为 80℃且碱溶液为氢氧化钠时，所述单晶硅上被腐蚀掉的厚度为 5～15μm。

本发明由于采取以上技术方案，其具有以下优点：1、由于本发明在由碱溶液、硅酸钠和异丙醇构成的腐蚀液中加入了极少量的全氟辛基磺酸盐溶液，使得反应时间仅为 10～20min，就得到了金字塔边长为 1～8μm 且均匀的绒面，而且腐蚀掉的单晶硅的厚度为 5～15μm，与利用传统方法得到的单晶硅相比，本发明得到的单晶硅腐蚀厚度小，不易断裂，节约了成本。2、由于本发明采用的全氟辛基磺酸盐是一种阴离子中性表面活性剂，具有非常高的热力学稳定性和化学稳定性，因此不需要在生产过程中补液，进一步降低了成本。3、由于本发明使用的全氟辛基磺酸盐具有很好的相容性，能够在极低的溶液浓度下把水溶液的表面张力降到很低，增强浸润性，利于化学腐蚀的顺利进行，减少了反应时间。4、由于本发明采用的全氟辛基磺酸盐浓度极低，其用量与其它缓冲液相比，用量很少，因此大大节省了成本。

附图说明

图 1 是在金相显微镜下经放大 400 倍的单晶硅绒面形貌图

图 2 是在扫描电镜下经放大 1472 倍的单晶硅绒面形貌图

图 3 是在扫描电镜下经放大 5888 倍的单晶硅绒面形貌图

具体实施方式

下面结合附图和实施例对本发明进行详细的描述。

本发明包括以下步骤：

1）在 75℃～85℃恒温槽内配制包括碱溶液、硅酸钠和异丙醇的碱腐蚀溶液。碱腐蚀溶液中，碱溶液的质量百分比为 1%～2.5%，碱溶液为氢氧化钠或氢氧化钾或碳酸钠溶液；硅酸钠的质量百分比为 0.1%～2%，异丙醇的体积百分比为 0.5%～3%。

2）将浓度为 $5*10^{-5}$～$5*10^{-3}$mol/L 的全氟辛基磺酸盐溶液加入步骤 1）中配制有碱腐蚀溶液的恒温槽中，使全氟辛基磺酸盐溶液的体积百分比为 0.2%～1%，同时将未清洗的或粗抛的市售 P 型或 N 型、电阻率 0.3～8Ω·cm、厚度 180～500μm、<100>晶向单晶硅衬底置入花篮内，再一起放入步骤 1）中配制有碱腐蚀溶液的恒温槽中进行腐蚀反应，10～20min 后，将单晶硅取出，用去离子水冲洗干净并烘干。

以下通过几个具体实施例对本发明进行进一步验证。

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实施例 1：

如图 1～3 所示，图 1～3 为恒温槽的温度为 80℃，碱溶液为 1.6（%质量百分比）氢氧化钠，0.1（%质量百分比）硅酸钠，0.6（%体积百分比）异丙醇，0.3（%体积百分比）浓度为 $5*10^{-5}$～$5*10^{-3}$mol/L 的全氟辛基磺酸盐溶液，且腐蚀时间为 15min 时，得到的具有金字塔绒面的单晶硅，在显微镜下观察到单晶硅的表面上形成了均匀的金字塔绒面（如图 1 所示），且金字塔的边长为 1～8μm（如图 2、图 3 所示），单晶硅上被腐蚀掉的厚度为 12μm。

实施例 2：

当恒温槽的温度为 75℃，碱溶液为 1.6（%质量）氢氧化钠，0.1（%质量）硅酸钠，0.6(%体积）异丙醇，0.3（%体积）浓度为 $5*10^{-5}$～$5*10^{-3}$mol/L 的全氟辛基磺酸盐溶液，且腐蚀时间为 20min 时，得到的单晶硅绒面上金字塔的边长为 1～8μm（此处请核实!），单晶硅上被腐蚀掉的厚度为 13μm（此处请核实!）。

实施例 3：

当恒温槽的温度为 85℃，碱溶液为 1.6（%质量）氢氧化钠，0.1（%质量）硅酸钠，0.6（%体积）异丙醇，0.3（%体积）浓度为 $5*10^{-5}$～$5*10^{-3}$mol/L 的全氟辛基磺酸盐溶液，且腐蚀时间为 10min 时，得到的单晶硅绒面上金字塔的边长为 1～8μm，单晶硅上被腐蚀掉的厚度为 10μm。

上述各实施例中，全氟辛基磺酸盐为一种阴离子中性表面活性剂，具有非常高的热力学和化学稳定性，在 350～400℃不发生分解，在强酸、强碱、强氧化介质等特殊应用体系中稳定有效地发挥其表面活性剂作用；全氟辛基磺酸盐还具有很好的相容性，其能与体系中其它表面活性剂和组份很好地相容，并能够在极低的溶液浓度下把水溶液的表面张力降到很低，增强浸润性，可广泛用于各种 PH 值范围、各类水性、溶剂型体系中。

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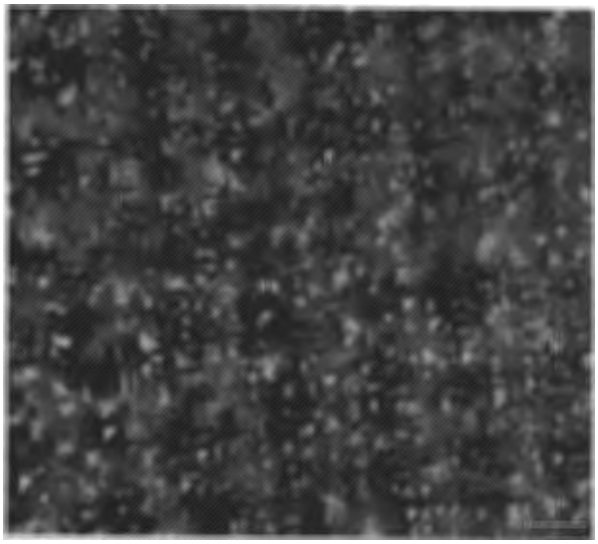


图 1

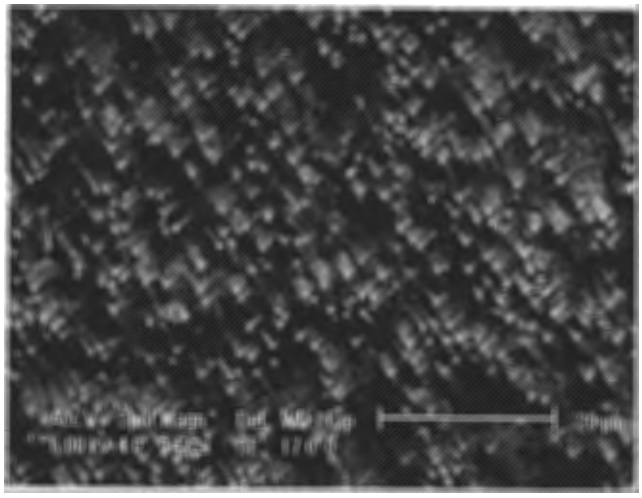


图 2

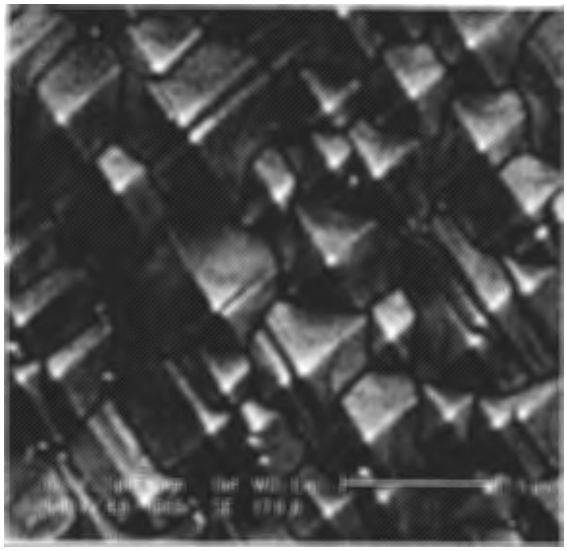


图 3

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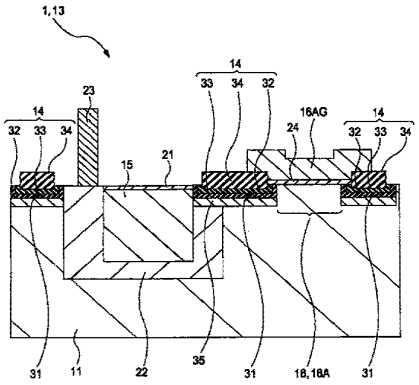
权利要求书 2 页 说明书 21 页 附图 15 页

(54)发明名称

固态成像装置、固态成像装置的制造方法和成像设备

(57)摘要

本发明涉及固态成像装置、固态成像装置的制造方法和成像设备。该固态成像装置在半导体基板上包括具有多个像素的像素部分，所述像素部分设置有：光电转换部分，对入射光进行光电转换以获得信号电荷；和像素晶体管部分，将从光电转换部分读取的信号电荷转换成电压，其中布置在像素部分中的元件隔离区域包括埋入布置在半导体基板中的沟槽中的绝缘膜，并且该绝缘膜包括具有负电荷的绝缘膜。



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1. 一种固态成像装置，其在半导体基板上包括具有多个像素的像素部分，所述像素部分设置有：

光电转换部分，对入射光进行光电转换以获得信号电荷；和

像素晶体管部分，将从光电转换部分读取的信号电荷转换成电压，

其中，布置在所述像素部分中的元件隔离区域包括埋入布置在所述半导体基板中的沟槽中的绝缘膜，并且

所述绝缘膜包括具有负电荷的绝缘膜。

2. 根据权利要求 1 的固态成像装置，

其中，所述元件隔离区域至少将所述像素彼此隔离。

3. 根据权利要求 1 的固态成像装置，

其中，所述具有负电荷的绝缘膜是包含从包括以下元素的组中选择的至少一种元素的绝缘膜：铪、锆、铝、钽、钛、钇和镧系元素。

4. 根据权利要求 1 的固态成像装置，

其中，P 型杂质区域布置在所述元件隔离区域下方的半导体基板中。

5. 根据权利要求 4 的固态成像装置，

其中，所述 P 型杂质区域的电势是固定的。

6. 一种固态成像装置的制造方法，该方法按顺序包括如下步骤：

在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；

在第一沟槽和第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；

去除布置在周边电路区域中并具有负电荷的绝缘膜；

使得第二沟槽深于第一沟槽；以及

将埋入式绝缘膜埋入第一沟槽和第二沟槽中，以在第一沟槽中形成第一元件隔离区域并且在第二沟槽中形成第二元件隔离区域。

7. 根据权利要求 6 的固态成像装置的制造方法，

其中，在去除具有负电荷的绝缘膜之后并且在将埋入式绝缘膜埋入第一沟槽和第二沟槽中之前，在第一沟槽底部的半导体基板中形成 P 型杂质区域。

8. 一种固态成像装置的制造方法，该方法按顺序包括如下步骤：

在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；

在对第一沟槽加掩模的同时使得第二沟槽深于第一沟槽；

在第一沟槽和第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；

去除布置在周边电路区域中并具有负电荷的绝缘膜；以及

将埋入式绝缘膜埋入第一沟槽和第二沟槽中，以在第一沟槽中形成第一元件隔离区域并且在第二沟槽中形成第二元件隔离区域。

9. 根据权利要求 8 的固态成像装置的制造方法，

其中，在去除具有负电荷的绝缘膜之后并在将埋入式绝缘膜埋入第一沟槽和第二沟槽

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中之前，在第一沟槽底部的半导体基板中形成 P 型杂质区域。

10. 一种固态成像装置的制造方法，该方法按顺序包括如下步骤：

在包括半导体基板的基板的周边电路区域中形成用于进行元件隔离的第一沟槽；

将第一埋入式绝缘膜埋入到第一沟槽中以形成第一元件隔离区域；

在基板上形成覆盖第一元件隔离区域的绝缘膜；

在设置有所述绝缘膜的半导体基板的像素区域中形成用于进行元件隔离的第二沟槽；

在第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第二沟槽的内表面与具有负电荷的绝缘膜之间；以及

将第二埋入式绝缘膜埋入第二沟槽中以形成第二元件隔离区域。

11. 根据权利要求 10 的固态成像装置的制造方法，

其中，在形成第二沟槽之后并且在将第二埋入式绝缘膜埋入第二沟槽中之前，在第二沟槽底部的半导体基板中形成 P 型杂质区域。

12. 一种固态成像装置的制造方法，该方法按顺序包括如下步骤：

在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；

在对第一沟槽加掩模的同时使得第二沟槽深于第一沟槽；

在第一沟槽和第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；以及

将埋入式绝缘膜埋入第一沟槽和第二沟槽中，以在第一沟槽中形成第一元件隔离区域并在第二沟槽中形成第二元件隔离区域。

13. 根据权利要求 12 的固态成像装置的制造方法，

其中，在去除具有负电荷的绝缘膜之后并且在埋入埋入式绝缘膜之前，在第一沟槽底部的半导体基板中形成 P 型杂质区域。

14. 一种成像设备，包括：

图像聚焦光学部分，对入射光进行会聚；

成像部分，包括固态成像装置，用于接收由图像聚焦光学部分会聚的光并对其进行光电转换；以及

信号处理部分，对进行了光电转换的信号进行处理，

其中，所述固态成像装置在半导体基板上包括像素部分，所述像素部分设置有：

光电转换部分，对入射光进行光电转换以获得信号电荷；和

像素晶体管部分，将从光电转换部分读取的信号电荷转换成电压，

布置在所述像素部分中的元件隔离区域包括埋入布置在所述半导体基板中的沟槽中的绝缘膜，并且

所述绝缘膜包括具有负电荷的绝缘膜。

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固态成像装置、固态成像装置的制造方法和成像设备

技术领域

[0001] 本发明涉及固态成像装置、该固态成像装置的制造方法以及成像设备。

背景技术

[0002] 近年来，通常，在细小半导体集成电路中使用浅沟槽隔离 (STI) 进行元件隔离。然而，由于通过在半导体基板中深挖沟槽来提供 STI，所以在埋入沟槽中的用于进行元件隔离的绝缘膜与半导体基板之间的界面处出现晶体缺陷或界面态 (interface state)，从而变成噪声源。因此，关于 CMOS 图像传感器，在采用 STI 作为并行于周边电路的像素部分的元件隔离方法的情况下，以如下方式出现特性劣化：在被挖掘的半导体基板与埋入式绝缘膜之间的界面处产生噪声。因此，提出下面这种方法作为减小由于噪声导致的固态成像元件的劣化的技术，在该方法中减小像素区域的元件隔离区域中的半导体基板的挖掘量，从而抑制从元件隔离端产生噪声（例如，参照日本未审专利申请公报 No. 2006-24786 和日本未审专利申请公报 No. 2006-93319）。

[0003] 然而，即使在应用上述的减小像素部分的元件隔离的挖掘量的元件隔离方法的情况下，如图 13 和图 14 所示，也需要通过引入 P 型杂质在像素部分 111 的元件隔离区域 112 下形成空穴累积层 113。上述的图 13 示出了像素部分的平面布局，图 14 是示出沿图 13 所示的线 XIV-XIV 剖开的、像素部分的截面的截面图。

[0004] 结果，由于像素变得更加细小，空穴累积层 113 的杂质的扩散的影响变得明显，并且由于 P 型杂质的扩散影响，减小了复位晶体管 114R、放大晶体管 114A、选择晶体管 114S 的有效沟道宽度。如果如上所述减小了有效沟道宽度，则尤其放大晶体管 114A 的 1/f 噪声的劣化是成问题的。

[0005] 另外，由于使像素变得更加细小，所以难以增加沟道宽度。

[0006] 因此，难以确保降噪与细小像素之间的兼容性。

[0007] 此外，提出了一种方法，其中为了抑制在 STI 结构的元件隔离区域中产生噪声，在 STI 中埋入用于施加电压的导体以使得用于进行元件隔离的绝缘膜与半导体基板之间的界面进入空穴累积状态（例如，参照日本未审专利申请公报 No. 2006-120804）。

[0008] 在将用于施加电压的导体埋入上述 STI 中的方法中，需要在元件隔离区域中埋入用于施加负电压的导体。此时，需要将该导体埋入元件隔离区域中，尤其是像素区域的选择晶体管和放大晶体管附近的元件隔离区域中，以避免与用作晶体管的栅电极的多晶硅电导通。然而，难以在避开栅电极的多晶硅的同时在细小像素的像素区域的整个元件隔离区域埋入该导体。因此，对于抑制 1/f 噪声的劣化以及减小像素的晶体管的沟道的效果的目的，难以通过埋入导体来获得劣化抑制效果。

发明内容

[0009] 本发明的发明人认识到，由于像素变得更加细小而难以增大沟道宽度，并且如果减小了有效沟通宽度，则像素晶体管部分尤其是放大晶体管的 1/f 噪声劣化，因此很难获

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得降噪与细小像素之间的兼容性。

[0010] 期望噪声减小与细小像素可以互相兼容。

[0011] 提供了一种根据本发明的实施例的固态成像装置，其在半导体基板上包括具有多个像素的像素部分，所述像素部分包括：光电转换部分，对入射光进行光电转换以获得信号电荷；以及像素晶体管部分，将从上述光电转换部分读取的信号电荷转换成电压，其中，布置在上述像素部分中的元件隔离区域包括埋入布置在上述半导体基板中的沟槽中的绝缘膜，并且上述绝缘膜包括具有负电荷的绝缘膜。

[0012] 在根据本发明的实施例的固态成像装置中，布置在像素部分中的元件隔离区域包括具有负电荷的绝缘膜。因此，在紧邻元件隔离区域位于下方的半导体基板中产生由具有负电荷的绝缘膜中的负电荷生成的空穴累积层。通过该空穴累积层抑制了由元件隔离区域与半导体基板之间的界面处的缺陷导致的噪声产生。另外，由于通过负电荷形成空穴累积层，所以可以省去现有技术中的在紧邻元件隔离区域位于下方的半导体基板中形成的 P 型杂质区域。作为另一选择，在形成 P 型杂质区域的情况下，可以减小它的浓度。因此，抑制了由于 P 型杂质区域的 P 型杂质的扩散导致的像素晶体管部分中的晶体管的有效沟道宽度的减小，由此可以确保足够的有效沟道宽度。因此，减小了像素晶体管部分中的晶体管的 1/f 噪声。换言之，抑制了由于 P 型杂质区域导致的 P 型杂质的扩散并且相应减小了像素尺寸，同时确保了有效沟道宽度并且减小了 1/f 噪声。

[0013] 本发明提供了一种根据本发明的实施例的固态成像装置的制造方法（第一制造方法），该方法按顺序包括如下步骤：在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；在上述第一沟槽和上述第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；去除布置在上述周边电路区域中并具有负电荷的上述绝缘膜；使得上述第二沟槽深于第一沟槽；以及将埋入式绝缘膜埋入上述第一沟槽和上述第二沟槽中，以在上述第一沟槽中形成第一元件隔离区域并且在上述第二沟槽中形成第二元件隔离区域。

[0014] 本发明提供了一种根据本发明的实施例的固态成像装置的制造方法（第二制造方法），该方法按顺序包括如下步骤：在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；使得上述第二沟槽深于上述第一沟槽，同时对上述第一沟槽加掩模；在上述第一沟槽和上述第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；去除布置在上述周边电路区域中并具有负电荷的上述绝缘膜；以及将埋入式绝缘膜埋入上述第一沟槽和上述第二沟槽中，以在上述第一沟槽中形成第一元件隔离区域并且在上述第二沟槽中形成第二元件隔离区域。

[0015] 本发明提供了一种根据本发明的实施例的固态成像装置的制造方法（第三制造方法），该方法按顺序包括如下步骤：在包括半导体基板的基板的周边电路区域中形成用于进行元件隔离的第一沟槽；将第一埋入式绝缘膜埋入到上述第一沟槽中以形成第一元件隔离区域；在上述基板上形成覆盖上述第一元件隔离区域的绝缘膜；在设置有上述绝缘膜的上述半导体基板的像素区域中形成用于进行元件隔离的第二沟槽；在上述第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第二沟槽的内表面与具有负电荷的绝

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缘膜之间；以及将第二埋入式绝缘膜埋入上述第二沟槽中以形成第二元件隔离区域。

[0016] 本发明提供了一种根据本发明的实施例的固态成像装置的制造方法（第四制造方法），该方法按顺序包括如下步骤：在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；使得上述第二沟槽深于上述第一沟槽，同时对山数第一沟槽加掩模；在上述第一沟槽和上述第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；以及将埋入式绝缘膜埋入上述第一沟槽和上述第二沟槽中，以在上述第一沟槽中形成第一元件隔离区域并在上述第二沟槽中形成第二元件隔离区域。

[0017] 在根据本发明的实施例的固态成像装置的各制造方法中，在布置在像素部分中的元件隔离区域中形成具有负电荷的绝缘膜。因此，在紧邻元件隔离区域位于下方的半导体基板中产生由具有负电荷的绝缘膜中的负电荷生成的空穴累积层。通过该空穴累积层抑制了由元件隔离区域与半导体基板之间的界面处的缺陷导致的噪声产生。另外，由于通过负电荷形成空穴累积层，所以可以省去现有技术中的在紧邻元件隔离区域位于下方的半导体基板中形成的 P 型杂质区域。作为另一选择，在形成 P 型杂质区域的情况下，可以减小它的浓度。因此，抑制了由于 P 型杂质区域的 P 型杂质的扩散导致的像素晶体管部分中的晶体管的有效沟道宽度的减小，由此可以确保足够的有效沟道宽度。因此，减小了像素晶体管部分中的晶体管的 1/f 噪声。换言之，抑制了由于 P 型杂质区域导致的 P 型杂质的扩散并且相应减小了像素尺寸，同时确保了有效沟道宽度并且减小了 1/f 噪声。

[0018] 本发明提供了一种根据本发明的实施例的成像设备，包括：图像聚焦光学部分，对入射光进行会聚；成像部分，包括固态成像装置，用于接收由上述图像聚焦光学部分会聚的光并对其进行光电转换；以及信号处理部分，对进行了光电转换的信号进行处理，其中，上述固态成像装置在半导体基板上包括像素部分。所述像素部分设置有：光电转换部分，对入射光进行光电转换以获得信号电荷；和像素晶体管部分，将从上述光电转换部分读取的信号电荷转换成电压。布置在上述像素部分中的元件隔离区域包括埋入布置在上述半导体基板中的沟槽中的绝缘膜，并且上述绝缘膜包括具有负电荷的绝缘膜。

[0019] 在根据本发明的实施例的成像设备中，采用根据本发明的实施例的固态成像装置。因此，抑制了固态成像装置的像素晶体管部分中的晶体管的有效沟道宽度的减小，由此减小了像素晶体管部分中的晶体管的 1/f 噪声。

[0020] 关于根据本发明的实施例的固态成像装置，抑制了由于 P 型杂质区域导致的 P 型杂质的扩散并且可以相应减小了像素尺寸，同时确保有效沟道宽度并且减小了 1/f 噪声。因此，噪声抑制与细小像素可以相互兼容。因此，存在提高成像的图像质量的优点。

[0021] 关于根据本发明的实施例的固态成像装置的各制造方法，抑制了由于 P 型杂质区域导致的 P 型杂质的扩散并且可以相应减小了像素尺寸，同时确保有效沟道宽度并且减小了 1/f 噪声。因此，噪声抑制与细小像素可以相互兼容。因此，存在提高成像的图像质量的优点。

[0022] 关于根据本发明的实施例的成像设备，由于采用了根据本发明的实施例的降噪与细小像素可以兼得的固态成像装置，所以存在由于更高图像质量和更高灵敏度而提高了成像的图像质量的优点。

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附图说明

[0023] 图 1 是示出根据本发明的第一实施例的固态成像装置的示例的示意性结构截面图；

[0024] 图 2A 和图 2B 分别是示出根据本发明的第一实施例的固态成像装置的示例的平面布局图和电路图；

[0025] 图 3A 到图 3E 是示出根据本发明的第二实施例的固态成像装置的制造方法的第一示例的生产步骤的截面图；

[0026] 图 4A 到图 4E 是示出根据本发明的第二实施例的固态成像装置的制造方法的第一示例的生产步骤的截面图；

[0027] 图 5A 到图 5E 是示出根据本发明的第三实施例的固态成像装置的制造方法的第二示例的生产步骤的截面图；

[0028] 图 6A 到图 6F 是示出根据本发明的第三实施例的固态成像装置的制造方法的第二示例的生产步骤的截面图；

[0029] 图 7A 到图 7E 是示出根据本发明的第四实施例的固态成像装置的制造方法的第三示例的生产步骤的截面图；

[0030] 图 8A 到图 8D 是示出根据本发明的第四实施例的固态成像装置的制造方法的第三示例的生产步骤的截面图；

[0031] 图 9A 到图 9C 是示出根据本发明的第四实施例的固态成像装置的制造方法的第三示例的生产步骤的截面图；

[0032] 图 10A 到图 10E 是示出根据本发明的第五实施例的固态成像装置的制造方法的第四示例的生产步骤的截面图；

[0033] 图 11A 到图 11D 是示出根据本发明的第五实施例的固态成像装置的制造方法的第四示例的生产步骤的截面图；

[0034] 图 12 是示出根据本发明的第六实施例的成像设备的示例的框图；

[0035] 图 13 是现有技术中的固态成像装置的示例的示意性结构截面图；以及

[0036] 图 14 是示出现有技术中的固态成像装置的示例的平面布局图。

具体实施方式

[0037] 将在下面描述执行本发明的优选实施例（下文中称作实施例）。

[0038] 第一实施例

[0039] 固态成像装置的结构的一个示例

[0040] 将参照图 1 所示的示意性结构截面图、图 2A 所示的平面布局图以及图 2B 所示的电路图来描述根据本发明的第一实施例的固态成像装置的结构的一个示例。图 1 是示意性示出了沿图 2A 所示的线 I-I 剖开的截面的图。

[0041] 如图 2A 和 2B 所示，根据本发明的实施例的固态成像装置 1 包括像素部分 12 以及位于像素部分 12 的周边的周边电路部分（附图中没有示出），在像素部分 12 中在半导体基板 11 上布置有多个像素 13（在附图中示出了一个典型像素）。另外，上述的像素部分 12 包括用于隔离各个像素 13 的元件隔离区域 14。此外，上述的像素部分 12 和周边电路部分被除上述的元件隔离区域 14 以外的元件隔离区域（附图中没有示出）隔离。

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[0042] 上述像素 13 包括光电转换部分 15 和像素晶体管部分 16。

[0043] 上述光电转换部分 15 对入射光进行光电转换以获得信号电荷，并且例如由光电二极管形成光电转换部分 15。

[0044] 上述像素晶体管部分 16 将从上述光电转换部分 15 读取的信号电荷转换成电压。例如，从上述光电转换部分 15 一侧依次布置有转移晶体管（可以称作读取晶体管）16T、复位晶体管 16R、放大晶体管 16A 和选择晶体管 16S。在这点上，上述转移晶体管 16T 和上述复位晶体管 16R 共有的扩散层构成了浮动扩散区 FD。浮动扩散区 FD 连接到放大晶体管 16A 的栅电极 16AG（图 2A 中没有示出）。

[0045] 此外，上述周边电路部分包括像素垂直扫描电路、水平扫描电路、驱动电路、定时产生电路等。

[0046] 将在下文中参照图 1 详细描述上述像素 13。在图 1 中，放大晶体管 16A 被显示为像素晶体管部分 16 的代表。

[0047] 如图 1 所示，被元件隔离区域 14 隔离的光电转换部分 15 和像素晶体管部分 16（放大晶体管 16A 以及附图中没有示出的复位晶体管、选择晶体管等）布置在半导体基板 11 上。

[0048] P 型扩散层 21 布置在上述光电转换部分 15 的表面上以抑制噪声。

[0049] 另外，P 型扩散层 22 布置在上述光电转换部分 15 的周围以将光电转换部分 15 与周围隔离。电极部分 23 布置在 P 型扩散层 22 上以将 P 型扩散层 22 的电势固定在恒定值。

[0050] 关于上述的放大晶体管 16A，栅电极 16AG 布置在半导体基板 11 上，栅极绝缘膜 24 位于半导体基板 11 与栅电极 16AG 之间，并且源极 - 漏极区域（附图中没有示出）布置在该栅电极 16AG 的两侧（沟道长度方向：与图垂直的方向）。尽管附图中没有示出，但是复位晶体管、选择晶体管和转移晶体管具有相似的结构。然而，关于转移晶体管，源极 - 漏极区域之一还用作光电转换部分的 N 型区域，而另一个区域用作浮动扩散区 FD（参照图 2A）。

[0051] 上述的元件隔离区域 14 布置在沟槽 31 上，用以对布置在半导体基板 11 中的沟槽 31 进行填充。也就是说，氧化硅膜 32 布置在上述沟槽 31 的内表面上，具有负电荷的绝缘膜 33 布置在氧化硅膜 32 的表面上。另外，埋入式绝缘膜 34 布置在沟槽 31 中，其中上述的氧化硅膜 32 和具有负电荷的绝缘膜 33 布置在绝缘膜 34 与沟槽 31 之间，从而使得绝缘膜 34 具有高于半导体基板 11 的表面的高度。

[0052] 例如由氧化铪（HfO_2）膜、氧化锆（ZrO_2）膜、氧化铝（Al_2O_3）膜、氧化钽（Ta_2O_5）膜、氧化钛（TiO_2）膜或者氧化钇（Y_2O_3）膜形成上述的具有负电荷的绝缘膜 33。

[0053] 对于上述的具有负电荷的绝缘膜 33，可以使用通过化学气相沉积法、喷溅法、原子层沉积（ALD）法等形成的膜。然而，具有与基板的良好界面并且通过原子层沉积方法形成的膜是有利的。

[0054] 另外，由于在形成膜的同时可以形成用于减小界面态的大约 1nm 的氧化硅（SiO_2）层，所以利用原子层沉积法是有利的。在这种情况下，可以省去上述的氧化硅膜 32 的形成。

[0055] 除了上述的材料以外的材料的示例包括：镧系元素氧化物，例如氧化镧（La_2O_3）、氧化铈（CeO_2）、氧化镨（Pr_2O_3）、氧化钕（Nd_2O_3）、氧化钷（Pm_2O_3）、氧化钐（Sm_2O_3）、氧化铕（Eu_2O_3）、氧化钆（Gd_2O_3）、氧化铽（Tb_2O_3）、氧化镝（Dy_2O_3）、氧化钬（Ho_2O_3）、氧化铒（Er_2O_3）、氧化铥（Tm_2O_3）、氧化镱（Yb_2O_3）和氧化镥（Lu_2O_3）。此外，还可以由氮化铪膜、氮化铝膜、氮氧化

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铪膜或氮氧化铝膜形成上述的具有负电荷的绝缘膜 33。

[0056] 关于上述的具有负电荷的绝缘膜 33，在损害绝缘性的范围内，可以对该绝缘膜 33 加入硅 (Si) 或氮 (N)。在不损害膜的绝缘性的范围内，适当地确定硅或氮的浓度。在如上所述加入硅 (Si) 或氮 (N) 的情况下，可以增强膜的耐热性并且提高在处理期间防止离子注入的能力。

[0057] 在上述沟槽 31 的底部，P 型杂质区域 35 布置在上述半导体基板 11 中。通过对半导体基板 11 掺入 P 型杂质（例如，硼或二氟化硼）形成该 P 型杂质区域 35。该 P 型杂质区域 35 的杂质浓度可以低于现有技术的布置在元件隔离区域下的半导体基板中的 P 型杂质区域的杂质浓度。

[0058] 在这点上，在通过上述的具有负电荷的绝缘膜 33 的负电荷向上述元件隔离区域 14 下的半导体基板 11 充分引入空穴的情况下，不需要形成上述的 P 型杂质区域 35。

[0059] 此外，上述的 P 型杂质区域 35 连接到上述的 P 型杂质区域 22。因此，通过上述的 P 型杂质区域 22 固定了上述的 P 型杂质区域 35 的电势。

[0060] 在上述的固态成像装置 1 中，像素部分 12 的元件隔离区域 14 包括具有负电荷的绝缘膜 33。因此，在紧邻元件隔离区域 14 位于下方的半导体基板 11 中产生由于具有负电荷的绝缘膜 33 中的负电荷而生成的空穴累积层。通过空穴累积层抑制由于元件隔离区域 14 与半导体基板 11 之间的界面处的缺陷而导致的噪声生成。

[0061] 另外，由于通过负电荷形成空穴累积层，所以可以省去现有技术中在紧邻元件隔离区域位于下方的半导体基板中形成的 P 型杂质区域。

[0062] 作为另一选择，在形成 P 型杂质区域 35 的情况下，可以减小它的浓度。也就是说，在形成上述的 P 型杂质区域 35 的情况下，除了由于上述的具有负电荷的绝缘膜 33 的负电荷而生成的空穴累积层以外，还增强了空穴累积效果。

[0063] 因此，即使当 P 型杂质区域 35 的浓度减小时，仍通过上述的具有负电荷的绝缘膜 33 的负电荷引发与之对应的空穴，由此获得了与现有技术中的固态成像装置的空穴浓度基本相等的空穴浓度，在现有技术中布置 P 型杂质区域而没有上述的具有负电荷的绝缘膜 33。结果，与现有技术中的布置在固态成像装置的元件隔离区域下的 P 型杂质区域相比，可以减小上述的 P 型杂质区域 35 的浓度。

[0064] 如上所述，与以前相比可以减小 P 型杂质区域 35 的杂质浓度，或者可以省去 P 型杂质区域 35。因此，减小了 P 型杂质向晶体管的沟道区域的扩散。因此，可以使晶体管的有效沟道宽度大于现有技术中的固态成像装置的有效沟道宽度。

[0065] 也就是说，尽管随着晶体管变得更加细小由于 P 型杂质的扩散导致沟道减小的效果变得明显，但是仍能够抑制该效果。具体地讲，由于抑制了放大晶体管 16A 的有效沟道宽度的减小，所以减小了 1/f 噪声。另外，由于抑制了沟道减小的效果，所以实现了如下效果：抑制了晶体管的阈值电压的增加以及减小了阈值电压的变化。

[0066] 换言之，抑制了由于 P 型杂质区域 35 导致的 P 型杂质的扩散并且相应地减小了像素尺寸，同时确保了像素晶体管部分 16 的晶体管的有效沟道宽度并且减小了 1/f 噪声。

[0067] 因此，噪声抑制和细小像素可以变得相互兼容。

[0068] 此外，由于降噪而提高了成像的图像质量。此外，细小像素可以增加像素的数目。成像的图像质量由此变成更高水平的清晰度。存在如上所述的优点。

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[0069] 如果上述的 P 型杂质区域 35 的 P 型杂质扩散到光电转换部分 15 侧，则可能会出现不利影响，例如，饱和电荷量下降或者残像劣化）。然而，在上述的固态成像装置 1 中，由于可以省去上述的 P 型杂质区域 35 或者可以减小上述的 P 型杂质区域 35 的浓度，所以可以抑制饱和电荷量下降以及残像劣化。

[0070] 在固态成像装置的某结构中，通过元件隔离区域完全隔离形成有光电转换部分和转移晶体管的区域与形成有复位晶体管、放大晶体管和选择晶体管的像素晶体管部分。具有这种结构的固态成像装置可以具有与根据本发明的实施例的固态成像装置 1 的结构相同的结构，在根据本发明的实施例的固态成像装置 1 中具有负电荷的绝缘膜被应用于元件隔离区域。

[0071] 第二实施例

[0072] 固态成像装置的制造方法的第一示例

[0073] 将参照图 3A 到图 4E 所示的生产步骤的截面图，描述根据本发明的第二实施例的固态成像装置的制造方法的第一示例。

[0074] 如图 3A 所示，在半导体基板 11 上依次形成氧化硅膜 71 和氮化硅膜 72。例如，将硅基板用于上述的半导体基板 11。

[0075] 然后，如图 3B 所示，在上述的氮化硅膜 72 上形成用于形成元件隔离沟槽的抗蚀剂掩模（附图中没有示出）。将获得的掩模用作蚀刻掩模，并且对上述的氮化硅膜 72、上述的氧化硅膜 71 和上述的半导体基板 11 进行蚀刻。也就是说，在半导体基板 11 的像素区域 17 中形成用于进行元件隔离的第一沟槽 51，在周边电路区域 18 中形成用于进行元件隔离的第二沟槽 52。

[0076] 基于在像素部分中形成的元件隔离区域的绝缘膜的膜厚度，确定对于上述的第一沟槽 51 和第二沟槽 52 的、半导体基板 11 的挖掘深度。上述的挖掘深度被指定为例如 150nm 以下，并且优选是大约 50nm。

[0077] 然后，去除上述的抗蚀剂掩模。

[0078] 接下来，如图 3C 所示，在上述的第一沟槽 51 的内表面上形成氧化硅膜 53，在上述的第二沟槽 52 的内表面上形成氧化硅膜 54。例如通过热氧化方法对暴露在上述的第一沟槽 51 和第二沟槽 52 的内部的上述的半导体基板 11 进行氧化，形成上述的氧化硅膜 53 和 54。

[0079] 因此，通过氧化硅膜 53 和 54，减小了上述的第一沟槽 51 和第二沟槽 52 与上述的半导体基板 11 的界面处存在的缺陷。

[0080] 然而，由于上述的氧化硅膜 53 和 54 的膜厚度增加，减小了之后埋入并且具有负电荷的膜向半导体基板 11 引入空穴的效果。

[0081] 因此，上述的氧化硅膜 53 和 54 的膜厚度优选为 5nm 以下。

[0082] 然后，如图 3D 所示，在上述的第一沟槽 51 和上述的第二沟槽 52 的内表面上形成具有负电荷的绝缘膜 55，其中上述的氧化硅膜 53 和 54 位于在它们之间。在上述的氮化硅膜 72 上也形成该具有负电荷的绝缘膜 55。

[0083] 例如，通过氧化铪（HfO_2）膜、氧化锆（ZrO_2）膜、氧化铝（Al_2O_3）膜、氧化钽（Ta_2O_5）膜、氧化钛（TiO_2）膜或者氧化钇（Y_2O_3）膜形成上述的具有负电荷的绝缘膜 55。

[0084] 膜形成方法的示例包括化学气相沉积法、喷溅法和原子层沉积（ALD）法。为了提

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Method for preparing texture of monocrystalline-silicon solar cell by one-step process

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Abstract of CN101818348 (A)

The invention discloses a method for preparing texture of a monocrystalline-silicon solar cell by an one-step process. A monocrystalline silicon wafer is immersed in a mixed solution to be etched at 80-85 DEG C for 10-30 minutes, so that texture is formed on the surface of the monocrystalline silicon wafer; and the mixed solution comprises the following components in percentage by volume: 15-20% of NaClO, 10-15% of C2H5OH and the balance water. The method can reduce the process steps, reduce the manufacturing cost and enhance the commercial efficiency. The invention has the advantages of simple operation, and good compatibility of equipment and conventional texture making process, and is suitable for large-scale industrial production.

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(54)发明名称

一步法制备单晶硅太阳能电池绒面的方法

(57)摘要

本发明公开了一步法制备单晶硅太阳能电池绒面的方法，将单晶硅片置入混合液中，在80～85℃条件下浸泡腐蚀10～30分钟，在单晶硅片表面形成绒面，所述的混合液的体积百分比组成为：15%～20%的NaClO、10%～15%的C_2H_5OH和余量的水。本发明方法制备单晶硅片绒面可以减少工艺步骤，降低制作成本，提高经济效率。本发明操作简单，设备与常规的制绒工艺兼容，适宜于大规模工业生产。

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1. 一步法制备单晶硅太阳能电池绒面的方法，其特征在于，将单晶硅片置入混合液中，在 80 ～ 85℃条件下浸泡腐蚀 10 ～ 30 分钟，在单晶硅片表面形成绒面，所述的混合液的体积百分比组成为：15％～ 20％的 NaClO、10％～ 15％的 C_2H_5OH 和余量的水。

2. 如权利要求 1 所述的方法，其特征在于，所述的绒面的厚度为 1 微米到 5 微米。

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一步法制备单晶硅太阳能电池绒面的方法

技术领域

[0001] 本发明涉及半导体材料技术领域，尤其涉及一种单晶硅太阳能电池绒面的制备方法。

背景技术

[0002] 自从太阳能电池问世以来，提高太阳能电池的转换效率和降低太阳能电池的制作成本一直是太阳能电池产业追求的目标。改进太阳能电池的结构设计、工艺技术、制作流程以及提高太阳能电池对阳光的吸收能力是达到上述两个目标的努力方向。绒面和减反膜是减少太阳能电池的反射率，提高太阳能电池吸收率的主要手段，也是硅基太阳能电池生产中必不可少的步骤，因此，在硅基太阳能电池领域，怎样制备高效的绒面是一个热门的课题。

[0003] 所谓绒面就是指存在于物体表面上的一系列有规则或无规则的高低不同、大小不同的表面形貌。由于绒面的存在，物体表面的反射率可以大大降低，吸收率就可以显著提高。

[0004] 单晶硅太阳能电池表面的绒面制备一般是通过碱溶液腐蚀而成，利用单晶硅在低浓度碱溶液中各向异性的腐蚀特性，在硅片表面形成金字塔结构。当太阳光照射在硅片表面时，由于金字塔的存在，光线在金字塔之间来回反射，形成多次吸收，从而提高了硅片吸收太阳光的能力。

[0005] 常规的单晶硅绒面制备技术，是先使用清洗液除去硅片表面的污染物。然后在85℃下把硅片放在高浓度的NaOH或者KOH溶液（～15%左右）中腐蚀10分钟，使硅片两面各被腐蚀掉约10微米，以除去硅片表面的机械损伤层（如果不去除硅片的损伤层，会使得后继的杂质扩散不均匀，增加电池的漏电流）。然后将去除损伤层的硅片放在85℃的低浓度NaOH或者KOH（～2%左右）和IPA（异丙醇）的混合溶液中反应20分钟，就能在硅片表面制备出一层金字塔状的绒面，这就是通常所说的二步法制备单晶硅太阳能电池绒面的技术。

[0006] 但采用二步法，制备过程复杂，也增加了生产成本。

发明内容

[0007] 本发明提供一种制备单晶硅太阳能电池绒面的方法，能通过同一种腐蚀液，在去除单晶硅表面损伤层的同时获得优良的金字塔绒面。在现有技术的基础上不需要增加另外的生产设备。

[0008] 一步法制备单晶硅太阳能电池绒面的方法，将单晶硅片置入混合液中，在80～85℃条件下浸泡腐蚀10～30分钟，在单晶硅片表面形成绒面，所述的混合液的体积百分比组成为15%～20%的NaClO、10%～15%的C_2H_5OH和余量的水。

[0009] 本发明首先把单晶硅片浸泡在该制绒液（即所述的混合液）中，硅片经过制绒液腐蚀后，表面形成了大小为1微米到5微米的绒面，被腐蚀掉的单晶硅片的（总）厚度为

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10 ～ 25 微米。

[0010] 本发明的一个重要特征就是其不需要特殊的去损伤层的过程。在传统的制绒过程中，单晶硅片先要去除损伤层，然后再制备绒面。在本发明中，损伤层的去除过程就是制绒过程，通过将硅片浸泡在制绒液中，腐蚀其表面的损伤层，同时达到制绒的目的。

[0011] NaClO 经水解生成 OH⁻，使制绒液呈碱，利用碱溶液对硅片的各向异性腐蚀，硅片表面在去除损伤层的同时也形成了绒面。为了在一定时间内既能完全去除损伤层又能生成效果良好的绒面，控制制绒液的腐蚀速率非常重要。如果腐蚀速率过慢，那么在一定的时间内无法完全去除损伤层；如果腐蚀速率过快，容易造成绒面的金字塔颗粒过大，就不利于减少硅片表面的反射率。所以在本发明中，控制合适的反应速率是关键。

[0012] 选择合适的 NaClO 浓度是控制腐蚀速率的一个重要手段，本发明所使用的混合液中，NaClO 浓度为 15％到 20％。现在工业上普遍使用的 2％ NaOH 和 10％ C_2H_5OH 混合溶液在 85℃，20 分钟内硅片表面只能腐蚀掉 16 微米，而使用本发明腐蚀硅片，在相同条件下，可以将硅片腐蚀掉 20 微米以上。本发明对硅片的腐蚀速率大于现在普遍使用的 NaOH 制绒液，因此可以应用于一步法绒面制备。本发明发现，随着 NaClO 浓度的增加，硅片被腐蚀的厚度增加，制得的金字塔颗粒增大，使得硅片表面的反射率也随之增加。所以选择合适的 NaClO 浓度，既可以在一定的时间内完全腐蚀掉损伤层，又可以得到比较理想的反射率。在本发明中，15％～ 20％的 NaClO 溶液混合一定量的 C_2H_5OH 均可以达到理想的一步制绒效果

[0013] 控制反应速率的第二个重要手段是控制 C_2H_5OH 的浓度。本发明发现，当浓度为 17％的 NaClO 溶液中无 C_2H_5OH 时，在 85℃下经 20 分钟反应之后，硅片表面没有任何金字塔颗粒形成，并且硅片表面比反应之前更加光亮，起到了抛光的作用，硅片单面厚度可以腐蚀掉 15 微米。在此溶液中加入 C_2H_5OH 后，硅片表面可以形成均匀的金字塔结构，并且单面腐蚀掉的硅片厚度明显小于 15 微米，减缓了反应速率。本发明还发现，当 C_2H_5OH 浓度控制在 10％到 15％时，能得到最佳的绒面效果，且能完全去除损伤层。

[0014] 控制反应速率的第三个重要手段是控制反应的温度。本发明制绒液的反应温度控制在 80℃到 85℃，在此温度范围内能够将硅片损伤层完全去除，并且得到较低的表面反射率。

[0015] 这就是说，本发明的制绒过程，既是一个去除损伤层的过程，也是一个制备绒面的过程。因此采用本发明的技术，可以大大简化生产步骤，降低生产成本。

[0016] 单晶硅片在经过本发明的制绒液腐蚀后，表面形成了 1 微米到 5 微米的金字塔结构。这种绒面能有效降低单晶硅片表面的反射率，增加太阳光的吸收，提高太阳能电池的转换效率。

[0017] 本发明制备单晶硅片绒面可以减少工艺步骤，降低制作成本，提高经济效率。本发明操作简单，设备与常规的制绒工艺兼容，适宜于大规模工业生产。

附图说明

[0018] 图 1 为实施例 1 制备的硅片表面形貌；

[0019] 图 2 为实施例 2 制备的硅片表面形貌；

[0020] 图 3 为实施例 3 制备的硅片表面形貌；

[0021] 图 4 为 85℃下硅片在含有 NaClO 和 C_2H_5OH 的制绒液中反应 20 分钟后表面反射率，

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其中 NaClO 的体积百分比浓度分别为 15%、17%和 20%，C_2H_5OH 的浓度为 10%。

具体实施方式

[0022] 实施例 1

[0023] 配制混合液（制绒液），混合液的体积百分比组成为：

[0024] NaClO 15%

[0025] C_2H_5OH 10%

[0026] 余量为水。

[0027] 制绒液搅拌均匀后温度控制在 85℃，将经过清洗的单晶硅片放入该制绒液中，反应 20 分钟，取出后用去离子水清洗，烘干。测得硅片单面腐蚀掉 10 微米，反射率为 11.1%。

[0028] 实施例 2

[0029] 配制混合液（制绒液），混合液的体积百分比组成为：

[0030] NaClO 17%

[0031] C_2H_5OH 10%

[0032] 余量为水。

[0033] 制绒液搅拌均匀后温度控制在 85℃，将经过清洗的单晶硅片放入该制绒液中，反应 20 分钟，取出后用去离子水清洗，烘干。测得硅片单面厚度腐蚀掉 11 微米，反射率为 12%。

[0034] 实施例 3

[0035] 配制混合液（制绒液），混合液的体积百分比组成为：

[0036] NaClO 20%

[0037] C_2H_5OH 10%

[0038] 余量为水。

[0039] 制绒液搅拌均匀后温度控制在 85℃，将经过清洗的单晶硅片放入该制绒液中，反应 20 分钟，取出后用去离子水清洗，烘干。测得硅片单面厚度腐蚀掉 12.5 微米，反射率为 12.1%。

[0040] 实施例 4

[0041] 配制混合液（制绒液），混合液的体积百分比组成为：

[0042] NaClO 17%

[0043] C_2H_5OH 15%

[0044] 余量为水。

[0045] 制绒液搅拌均匀后温度控制在 85℃，将经过清洗的单晶硅片放入该制绒液中，反应 20 分钟，取出后用去离子水清洗，烘干。测得硅片单面厚度腐蚀掉 8.5 微米，反射率为 14.1%。

[0046] 实施例 5

[0047] 配制混合液（制绒液），混合液的体积百分比组成为：

[0048] NaClO 17%

[0049] C_2H_5OH 10%

[0050] 余量为水。

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[0051] 制绒液搅拌均匀后温度控制在80℃，将经过清洗的单晶硅片放入该制绒液中，反应20分钟，取出后用去离子水清洗，烘干。测得硅片单面厚度腐蚀掉9.5微米，反射率为11.4%。

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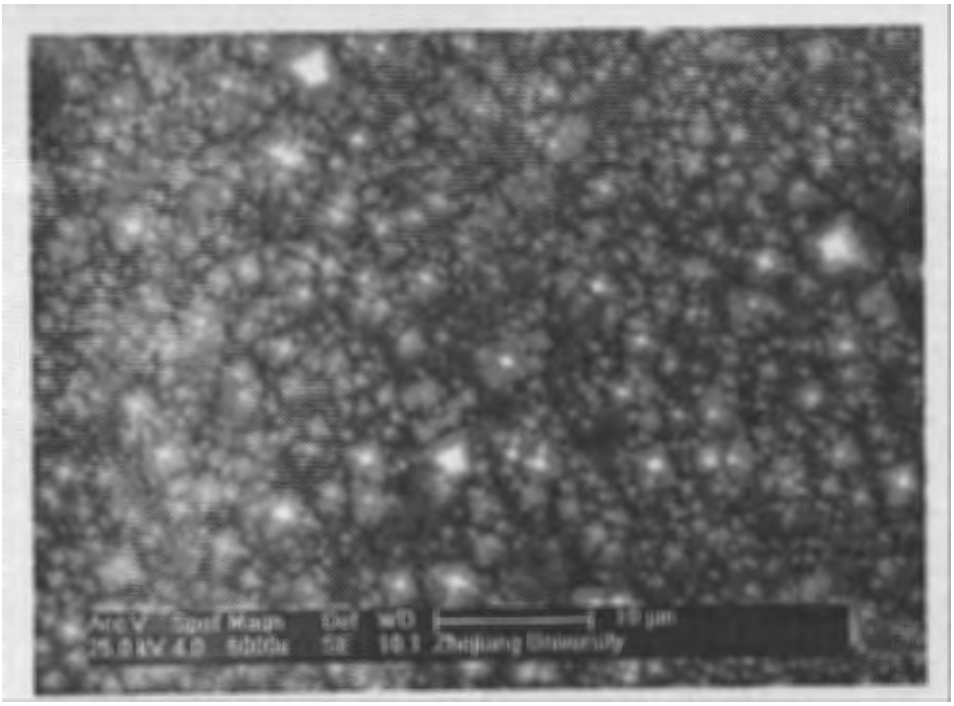


图 1

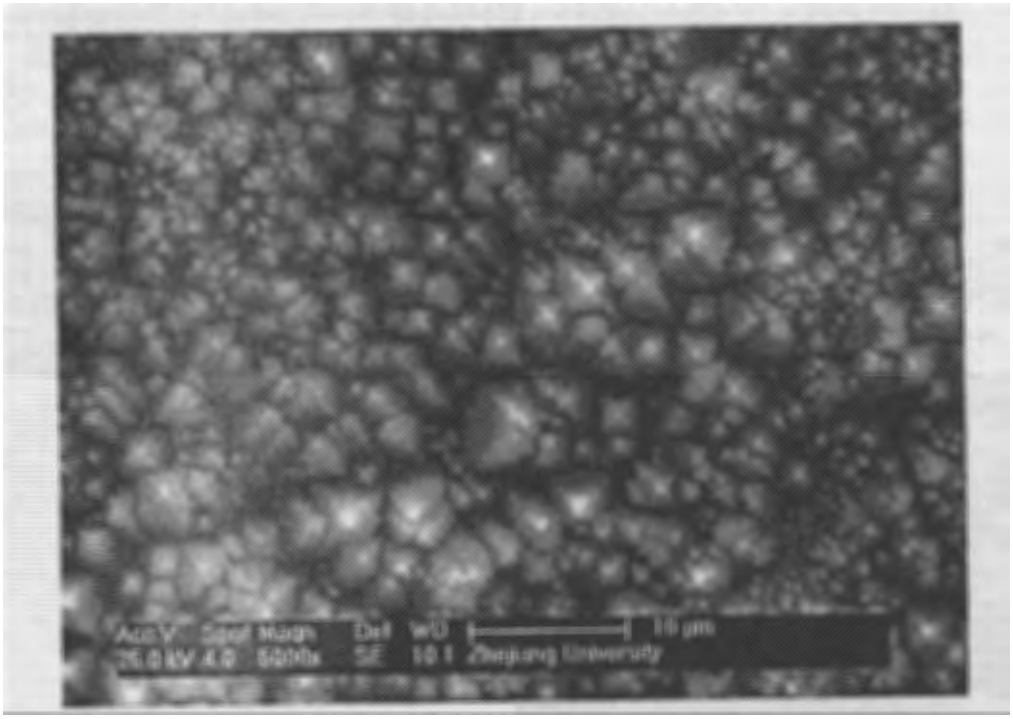


图 2

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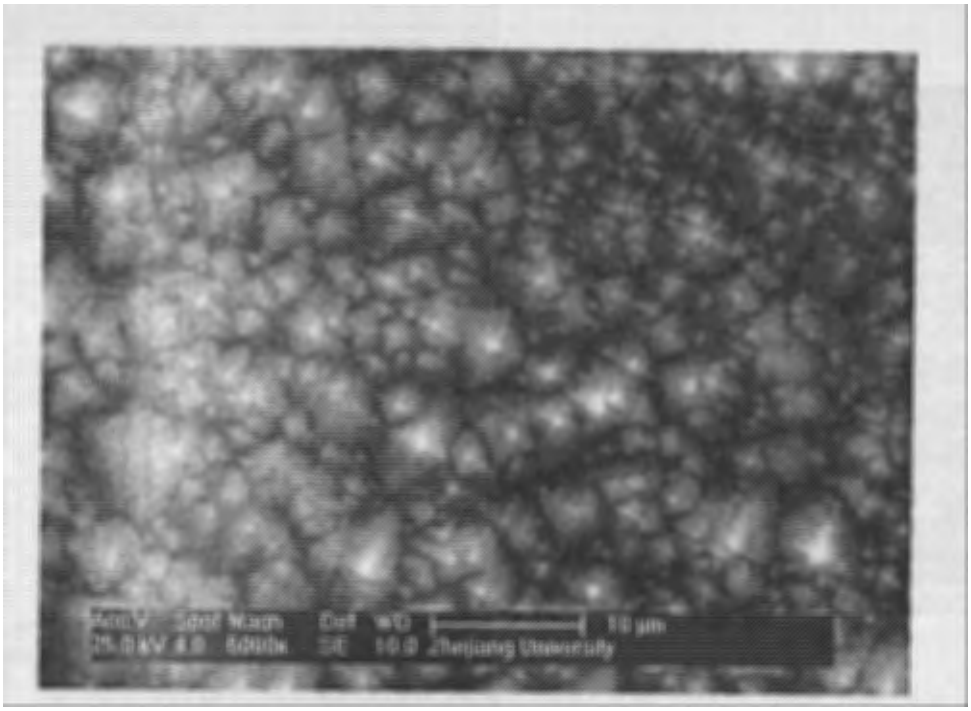


图 3

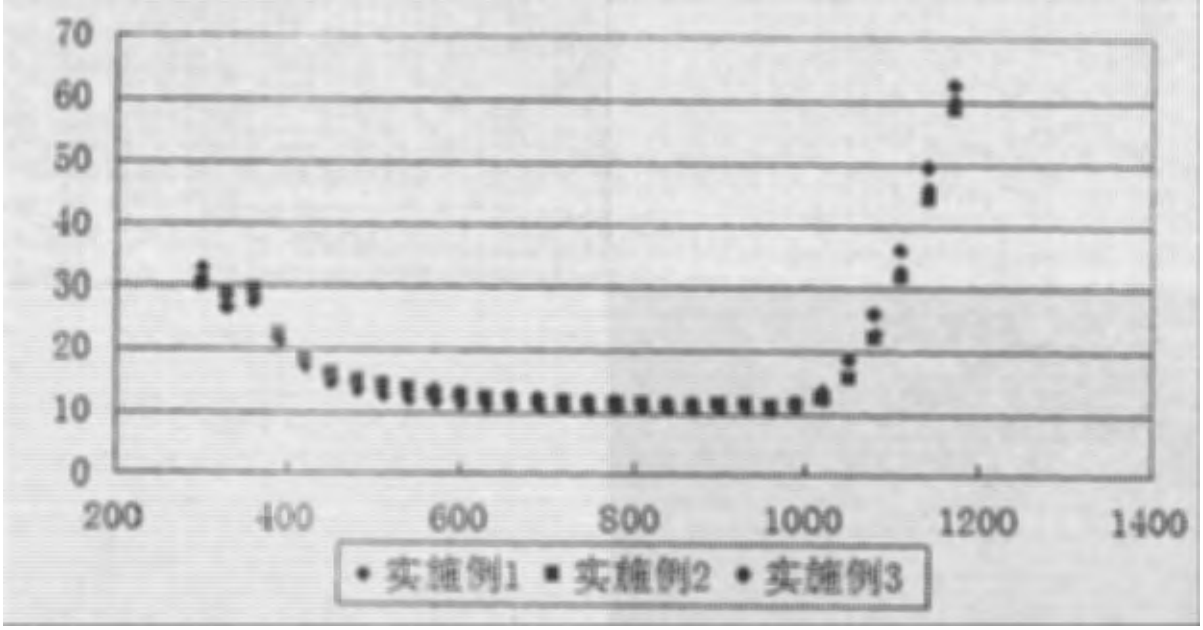


图 4

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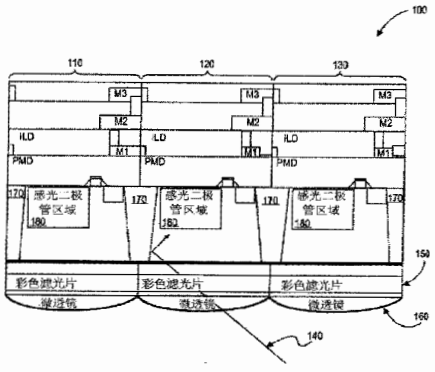
权利要求书 2 页 说明书 5 页 附图 7 页

(54)发明名称

具有深光反射沟槽的背照式图像传感器

(57)摘要

本发明提供一种像素阵列，其是使用基板形成的，该基板具有前侧及用于接收入射光的背侧。各个像素通常包含金属化层、感光区域及沟槽，这种金属化层被包含在该基板的前侧中，该感光区域是形成于该基板的后侧中，该沟槽围绕该基板的后侧中的感光区域而形成。该沟槽造成入射光被导引远离该沟槽并朝向该感光区域。



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1. 一种图像传感器，包括：

利用具有前侧及背侧的基板形成的像素阵列，其中该背侧是用于接收入射光，每个像素包含：

该基板的前侧中所包括的金属化层；及

形成至所述金属化层的背侧的感光区域；及

围绕该基板的背侧中的感光区域形成的沟槽，该沟槽造成该入射光被导引远离该沟槽并朝向该感光区域。

2. 如权利要求 1 所述的装置，其中该沟槽是由气体填充的或被排空以产生真空或部分真空。

3. 如权利要求 1 所述的装置，其中该沟槽的一部分位于一区域中，该区域至少部分地处于相邻像素的周边。

4. 如权利要求 1 所述的装置，其中该沟槽是在使该基板的背侧薄化之后形成的。

5. 如权利要求 4 所述的装置，其中利用化学或机械平坦化 (CMP) 处理使该基板薄化。

6. 如权利要求 4 所述的装置，其中在使用浅沟槽隔离 (STI) 区域作为蚀刻终止层的情况下利用化学蚀刻处理使该基板薄化。

7. 如权利要求 1 所述的装置，其中该基板的背侧所接收的入射光响应于在该沟槽与该基板之间的介面处的全内反射而从该沟槽反射。

8. 如权利要求 1 所述的装置，其中填充该沟槽的材料具有比该基板的折射率小的折射率。

9. 如权利要求 1 所述的装置，其中该沟槽具有在该沟槽与该感光区域的介面处的反射性金属。

10. 如权利要求 1 所述的装置，其中该沟槽是使用非保形沉积介电膜加以密封的。

11. 如权利要求 1 所述的装置，其中该沟槽是通过在围绕着该感光区域的周边区域的一部分中的浅沟槽隔离 (STI) 区域的背侧蚀刻而形成的。

12. 如权利要求 1 所述的装置，其中该基板的背侧被图案化并被蚀刻以露出浅沟槽隔离 (STI) 区域。

13. 如权利要求 1 的装置，其中该沟槽是通过蚀刻该浅沟槽隔离 (STI) 区域并通过用二氧化硅来填充被蚀刻的 STI 区域而形成的。

14. 如权利要求 1 所述的装置，其中该沟槽是通过蚀刻该浅沟槽隔离 (STI) 区域使得一硅层残留于该 STI 区域中而形成的。

15. 一种方法，包括：

形成与沟槽相邻的感光区域，该感光区域形成为至少通过在其中形成有该沟槽的水平；

移除基板的背侧的一部分使得该沟槽的表面被暴露；

移除被暴露的沟槽的一部分；及

用具有与该基板不同的折射率的材料来填充由基板背侧被移除的部分及被暴露的沟槽的被移除的部分先前所占据的区域。

16. 如权利要求 15 所述的方法，其进一步包括施加非保形层以涂布该基板的背侧。

17. 如权利要求 15 所述的方法，其进一步包括将反射层施加至通过移除被暴露的沟槽

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的一部分而露出的表面。

18. 一种方法，包括：

形成与沟槽相邻的感光区域，其中该感光区域及该沟槽是使用基板的顶侧形成的；

蚀刻该基板的背侧的一部分，使得该沟槽的表面被暴露；及

用具有不同折射率的材料来填充由基板背侧被移除的部分先前所占据的区域。

19. 如权利要求 15 所述的方法，其中该沟槽被蚀刻以留下一硅层。

20. 如权利要求 19 所述的方法，其进一步包括离子注入背侧硅。

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具有深光反射沟槽的背照式图像传感器

[0001] 本发明主张 2008 年 2 月 8 号申请的美国专利临时申请案第 61/027,393 号题为「具有深光反射沟槽的背照式图像传感器」的权利，其以引用方式并入本文中。

技术领域

[0002] 本发明一般涉及成像电路，尤其涉及但不限于图像传感器。

背景技术

[0003] 集成电路已被研发以减小用于实施电路系统的元件的尺寸。举例来说，集成电路利用越来越小的设计特征，其能减少用于实施该电路系统的面积，使得现在多种设计特征正好在可见光的波长以下。随着图像传感器及作为感测阵列的一部分的单独的像素的尺寸不断缩小，重要的是更有效地捕获照射该感测阵列的入射光。因此，更有效地捕获入射光有助于维持或改善由尺寸不断缩小的感测阵列所捕获的电子图像的品质。

发明内容

[0004] 本文描述一种图像感测深光反射沟槽的实施例。在如下描述中提到多个具体细节以提供这种实施例的一透彻的理解。然而，本领域技术人员将了解此处描述的技术可被实践而不具有一个或更多个这种具体细节，或具有其他方法、元件、材料等。在其他情况下，熟知的结构、材料或操作未被详细显示或描述以避免混淆某些方面。

[0005] 贯穿此说明书，对「一个实施例」或「一实施例」的引用意为一种结合该实施例而描述的特定特征、结构、或特性被包含于本发明的至少一个实施例中。因此，在此说明的多个地方，用语「在一个实施例中」或「在一实施例中」的出现不必都涉及该相同的实施例。此外，在一个或更多个实施例中，这种特定的特征、结构或特性可以任何适当的方式组合。使用于此的术语「或」通常意为包含一种包含功能的意思，例如「及 / 或」。

[0006] 总体而言，集成电路包括用于多种应用的电路。这种应用使用多种装置，例如逻辑装置、成像器（包含 CMOS 及 CCD 成像器）及存储器（例如 DRAM 以及基于 NOR 及 NAND 的闪存存储器装置）。这些装置通常利用晶体管以发挥多种功能，包含信号的切换及放大。

[0007] 晶体管通常是通过执行于一硅基板上的光刻处理而形成于集成电路中。这种处理包含诸如将一光刻胶层施加至该基板、使用光（包含深紫外波长）将该光刻胶层曝光成一图案、通过蚀刻移除该光刻胶的曝光部分（或非曝光部分，仰赖于所使用的正光刻胶或负光刻胶）及例如通过沉积或注入附加材料而修改曝光结构的步骤以形成多种用于电子元件（包含晶体管）的结构。

[0008] 术语「基板」包含使用基于硅、锗化硅、锗、砷化镓及类似物的半导体形成的基板。术语基板亦可涉及已被执行于该基板上以在该基板中形成区域及 / 或结的先前处理步骤。术语基板亦可包含多种技术，例如掺杂及未掺杂半导体、硅的外延层及形成于该基板上的其他半导体结构。

[0009] 化学机械平坦化 (CMP) 可经执行以提供适于形成附加结构的被修改基板的表面。

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这种附加结构可通过执行诸如上述列出的处理步骤而被添加至该基板。

[0010] 由于作为一感测阵列的一部分的单独的像素中的这种图像传感器的尺寸日益变小，多种设计尝试更有效地捕获照射该感测阵列的入射光。举例来说，像素的光感测元件（例如光电二极管）的面积通常是通过在各个像素上（或之下）配置一微透镜而被最大化，使得该入射光被更好地聚焦于该光感测元件上。光通过该微透镜的聚焦尝试捕获通常入射于该像素被该感光元件占据的区域之外的光（并因此消失及 / 或「泄露」至其他非目的像素）。

[0011] 另一种可使用的方法是自该 CMOS 图像传感器（例如之下）的「背侧」收集光。使用该图像传感器的背侧允许光子被收集于一区域中，该区域相对而言未被许多通常用于形成典型的图像传感器的介电及金属层阻挡。一种背照式 (BSI) 图像传感器可通过使该图像传感器的硅基板变薄而制成，其可降低入射光在遇到该图像传感器的感测区域之前所穿越的硅的量。

[0012] 然而，在使该图像传感器的基板变薄时，将遭遇在该像素的灵敏度及（与相邻像素的）串扰之间做出权衡。举例来说，当较少地薄化时（其导致较厚的剩余硅基板），用于将光转换为电子 - 空穴对的光电二极管的较大的（体积）区域可被提供。当这种电子 - 空穴对被形成（在被提供的该较大区域中）相对远离该光电二极管空乏区时，被形成的这种电子 - 空穴对更易于被相邻的光电二极管捕获。由相邻光电二极管对形成的这种电子 - 空穴对的捕获是一种被称为电串扰的效应（其可导致彩色图像传感器中的彩色噪声）。因此，电串扰的机率随着该硅基板的厚度而增加，而灵敏度随着较薄的硅基板的使用而减小。

[0013] 光学串扰亦影响捕获入射光的效率。前照式 (FSI) 装置通常包含金属化层，入射光横穿穿过这种金属化层。FSI 装置可利用适当放置在这种金属化层中的金属结构以将光引导至该光电二极管，进而阻挡杂光进入错误的光电二极管而产生光学串扰。与之相反的是，背照式 (BSI) 装置通常不将入射光穿过这种金属化层，且因此不朝感光区域引导光。因此光学串扰是 BSI 装置中的一个更大的问题（与例如 FSI 装置相比）。

[0014] 根据本发明，BSI 像素阵列是利用一基板形成，该基板具有一前侧及一用于接收入射光的背侧。各个像素通常包含被包含于该基板的该前侧上的金属化层、一形成于该基板的该背侧（或该前侧）中的感光区域。一沟槽促使该入射光被导引远离该沟槽并朝向该感光区域。

[0015] 各个 BSI 像素具有深沟槽，其由一种在相邻的像素之间的低折射率的材料（例如 SiO_2，或其中该材料可为「空的」，如由一种常压气体填充或被抽空以产生一真空或部分真空）填充。这种深沟槽提高像素的灵敏度同时减少像素之间的串扰。像素之间的电子串扰被减少是因为相对而言在像素收集区域的较低处形成的电子 - 空穴对通常不会（或不能）迁移至相邻的像素。大体减少（或消除）的电子 - 空穴对的迁移允许一更厚的硅收集区域被使用，其导致灵敏度被提高。光学串扰被减少是因为该基板（例如硅）及这种深沟槽之间的折射率差异导致具有例如大于例如 16.6 度的入射角的光的全内反射（其中空气填充的深沟槽被提供于相邻的像素之间）。

附图说明

[0016] 图 1 为在 CMOS 图像传感器中背照式 (BSI) 像素的范例传感器阵列的一截面图；

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[0017] 图 2 为根据本发明的一实施例该 CMOS 图像传感器的一范例背照式 (BSI) 像素的一截面图；

[0018] 图 3 包含图 3A 到图 3E，显示一种形成一深光反射沟槽的范例方法；

[0019] 图 4 包含图 4A 到图 4E，显示另一种形成一深光反射沟槽的方法；

[0020] 图 5 显示一种具有一薄衬里氧化物的深光反射沟槽；

[0021] 图 6 显示一种具有一氧化物填充剂的深光反射沟槽；及

[0022] 图 7 显示一种不自前表面延伸至后表面的深光反射沟槽。

具体实施方式

[0023] 为达说明的目的，图 1 显示根据本发明的一实施例在 CMOS 图像传感器中的背照式 (BSI) 像素的范例传感器阵列的截面。阵列 100 包含像素 110、120 及 130。结构 100 通常含有至少数千个像素且通常含有不止一百万个像素。为了显示的清晰性，三个像素被显示。

[0024] 该像素阵列 100 通常是以二维阵列被配置使得可响应于被各个像素捕获的入射光 (140) 而形成一电子图像。各个像素可具有滤光片 150（包含彩色滤光片）使得该电子图像可被用以捕获彩色图像或提高该像素对例如某个波长的光的敏感性。各个像素亦可具有与各个像素关联的微透镜 160，使得该入射光被更直接地引导至该像素中。

[0025] 举例来说，入射光 140 横穿像素 120 的微透镜 160。该入射光是由该微透镜 160 更直接地折射至该像素 120 的基板中。然而，该入射光通过该微透镜 160 的方向改变（在此实例中）不足以防止该入射光 140 遇到位于像素 110 及 120 之间的沟槽 170。根据本发明，该沟槽 170 的一先前的氧化物被移除及 / 或替换，使得在该沟槽 170 与该像素 120 的基板之间的介面的相对折射率被增大而使得入射光 140 朝该像素 120 的一感光部位 180 反射。因此图 1 被用于例如显示该光可由该深沟槽弯曲至该像素或光电二极管中。

[0026] 图 2 显示根据本发明的一实施例一 CMOS 图像传感器的一范例背照式 (BSI) 像素的一截面图。结构 200 包含一基板 202，其上形成有一感光的感光二极管区域 204。一浮动漏极 206 通常形成为具有一种导电类型（例如 N 型，与感光二极管区域 204 的导电类型相比，N 型具有更高的 N 型材料浓度）。

[0027] 绝缘结构 208 形成于该基板 202 内以促进将这些像素彼此绝缘。绝缘结构 208 通常可利用诸如深沟槽隔离 (DTI) 或硅局部氧化 (LOCOS) 的方法而形成。一绝缘结构 208 可利用一 DTI 方法通过在该基板 202 内蚀刻一沟槽及在该沟槽内沉积一介电材料（例如二氧化硅）而形成。这种沟槽可自该基板 202 的前侧或背侧蚀刻。经沉积的介电材料可利用 CMP 而平坦化。一栅极结构 210 被形成于该基板 202 之上以控制自该感光二极管区域 204 流向该浮动漏极 206 的电流。

[0028] 在一图像传感器中一种典型的单独像素 200 可包含多个层的堆迭体，这些层包含金属层、平坦化层及类似物。如图所示，该像素 200 包含一前金属介电材料 212。该介电材料 212 可为任何绝缘体，例如氧化物。对于一些实施例来说，该介电材料可为氧化硅。通孔 214 可通过蚀刻及沉积一合适的金属或导电材料而形成于该介电材料 212 内。

[0029] 具有若干 M1 导体的第一金属层可形成于该介电材料 212 中（或上）。对于一些实施例来说，该第一金属层可被蚀刻为这种 M1 金属导体的形状。该介电材料 216 可被沉积及 / 或成长以填充这种 M1 导体之间的空隙。该介电材料 212 可使这种 M1 导体与下方结构绝

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缘。这种 M1 导体可为铜、铝、铜铝混合物或其他适于传输一信号的材料（例如钨）。

[0030] 如图所示，该像素 200 包含第二金属层，该第二金属层具有配置于一中间层介电材料 216 中（或上）的若干 M2 导体。对于一些实施例来说，该第二金属层可被蚀刻成这种 M2 导体的形状。该介电材料 218 可被沉积及 / 或成长以填充这种 M2 导体之间的空隙。该介电材料 216 可使这种 M1 金属导体与这种 M2 金属导体绝缘。通孔 214 可被使用以电连接在该阵列的不同层上的结构。

[0031] 该像素 200 进一步包含第三金属层，该第三金属层具有配置于一中间层介电材料 218 中（或上）的若干 M3 导体。对于一些实施例来说，该第二金属层可经蚀刻为这种 M3 导体的形状。一介电材料 220 可被沉积及 / 或成长以填充这种 M3 导体之间的空隙。该介电材料 218 可使这种 M2 金属导体与这种 M3 金属导体绝缘。该介电材料 220 可被成长及 / 或沉积以使 M3 金属导体绝缘及 / 或使该阵列的顶面平坦化。

[0032] 图 3 显示一种形成一深光反射沟槽的范例方法。深光反射沟槽可形成于一用于浅沟槽隔离的区域中。浅沟槽隔离是经形成以电隔离相邻的像素及周边电路装置。该浅沟槽隔离通常为一种在硅基板内蚀刻且之后由二氧化硅填充的沟槽。典型的沟槽深度为大约 300 纳米到 400 纳米（依据用于形成该沟槽的技术），或可小于 400 纳米。

[0033] 图 3A 显示一包含大约一到三微米深的深沟槽光反射结构 310（深沟槽结构 310）的范例截面。这种深沟槽结构 310 通常亦由氧化物填充。在这种深沟槽结构 310 形成后，可应用一前侧制造方法。在图 3B 中在该前侧制造处理完成后，背侧薄化处理被完成，以开始一背照式 (BSI) 制造处理。在一常规 BSI 处理中，基板 320 的背侧通常通过 CMP 及 / 或不涉及蚀刻终止层的使用的化学蚀刻而被薄化。根据本发明，深沟槽结构 310 可被用作一 CMP 蚀刻终止层，其可改善对背侧薄化的厚度控制。

[0034] 在该基板 320 已被薄化后，这种深沟槽结构 310 的下表面被暴露，如图 3B 所显示。在图 3C 中，在这种深沟槽中被暴露的二氧化硅是利用一种对硅具选择性的蚀刻方法移除（例如湿式或干式蚀刻方法）。此时，深光反射沟槽形成于空的沟槽 330 中，产生一较大的折射率差异（例如硅到空气）。或者，这种空沟槽 330 可用一种金属涂布（及 / 或填充）以制成一更加完美的反射器。图 3D 显示一种在该阵列的下表面上沉积非保形涂层 340。一非保形介电膜被沉积，其密封住这种沟槽（其可为空的、被涂布或被填充的）。SiO_2 亦可被留于这种沟槽中。

[0035] 图 3E 显示了额外的背侧处理，诸如硅背侧保护（例如注入）或溢料式浇口（未显示）或防反射涂层 350。此外，滤光片 360 被配置于由该非保形涂层 340 所界定的层之上。这种滤光片可与感光元件对齐使得一滤光片 360 与该像素的该基板及该二极管感测区域对齐。一微透镜 370 可被配置于该彩色滤光片 360 之上以促进将光线折射至该像素中。

[0036] 图 4 显示形成一深光反射沟槽的一种替代性方法。图 4A 显示一种相似于图 3A 的像素结构的像素结构（其中隔离由 STI 实现，而非深沟槽）。在被薄化至一理想厚度后，利用光刻胶 440 使基板 420 的背侧光刻图案化。基板 420 的背侧可利用图 4B 所显示的标准方法而图案化。在图 4C 中，（基板 420 的）硅及 (STI 结构 410 的）氧化物被蚀刻，如图 4C 所示。因此，该蚀刻形成深光反射沟槽 430。在图 4D 中，该光刻胶被移除。在图 4E 中一反射涂层 450 被保形施加至这种深光反射沟槽 430 的表面，并填充沟槽 430，如图 4E 所示。可继续附加处理以添加诸如一防反射层、一彩色滤光片及一微透镜的结构。在多种实施例中

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该沟槽可自不同的边侧蚀刻。举例来说，该深沟槽可自背侧蚀刻并与该前侧 STI 对齐。该背侧蚀刻亦可在该深沟槽不与该前侧 STI 对齐且连接至该前侧 STI 的情况下被完成。在另一替代实施例中，该前侧 STI 可被消除，及所有隔离自背侧执行。

[0037] 图 5 显示一种具有一薄衬里氧化物的深光反射沟槽。该标准浅沟槽隔离可形成于像素阵列及周边电路中。在浅沟槽蚀刻之后，该周边电路可由光刻胶掩盖，且该像素阵列沟槽经更深地蚀刻至一微米到三微米（以形成一如图 5 所显示的深光反射沟槽 510）。一薄衬里氧化物 520 利用一高温在深光反射沟槽 510 内成长以使该深光反射沟槽 510 的硅侧壁钝化。周边的浅沟槽可用一种典型的沟槽填充技术（使用，例如，氧化物 540）填充。由于该沟槽的相对较高的长宽比，该深沟槽在该 STI 被填充时并不必被完全填充。因此气隙 530 可被自然地形成于该沟槽的内部。因此，在硅薄化之后不需要氧化物蚀刻。不执行该氧化物蚀刻的优点在于保持该衬里氧化物以更好地使表面钝化及降低处理复杂度。在硅薄化之后可通过等离子体浸入离子注入而完成进一步钝化。

[0038] 图 6 显示一种具有一氧化物填充剂的深光反射沟槽。该像素 600 的背侧可经图案化，深沟槽结构 610 可被蚀刻。一种沟槽填充技术（适于填充具有高长宽比的沟槽，例如「高且薄的」沟槽）可被用以用氧化物填充这种沟槽以形成一具有一氧化物填充剂的深光反射沟槽。在多种范例方法中，原始氧化物 620 可能是存在的。由于硅及二氧化硅之间的折射率差异相对较大，用于全内反射的最终临界角仍足以应付多种传感器应用。

[0039] 图 7 显示一种不自前表面延伸至后表面的深光反射沟槽。在硅 730 被薄化至一理想厚度后，该后表面可注入 P 型注入物 740 以进行钝化。一形成于像素阵列及周边电路中的深沟槽隔离可经蚀刻使得一相对较薄的硅层 720（例如几分的一微米）残留于该深沟槽 710 的底部及该后表面之间。残留于该沟槽之下的薄硅层 720 亦可被使用以电连接像素基板及阵列晶体管。

[0040] 本发明的例示的实施例的以上描述，包含描述于摘要中的内容，并非意图其详尽或将本发明限制为所揭示的任何精确形式。虽然本发明的这种具体实施例及实例以说明的目的描述于此，但本领域技术人员将发现多种修改可在本发明的范围内。

[0041] 鉴于如上的详细描述，可对被本发明做出这些修改。使用于如下权利要求中的术语不应被理解为将本发明限制为在本说明书中揭示的特定实施例。本发明的范围将完全由如下的这种权利要求确定，其应根据已确立的权利要求解读原理而被理解。

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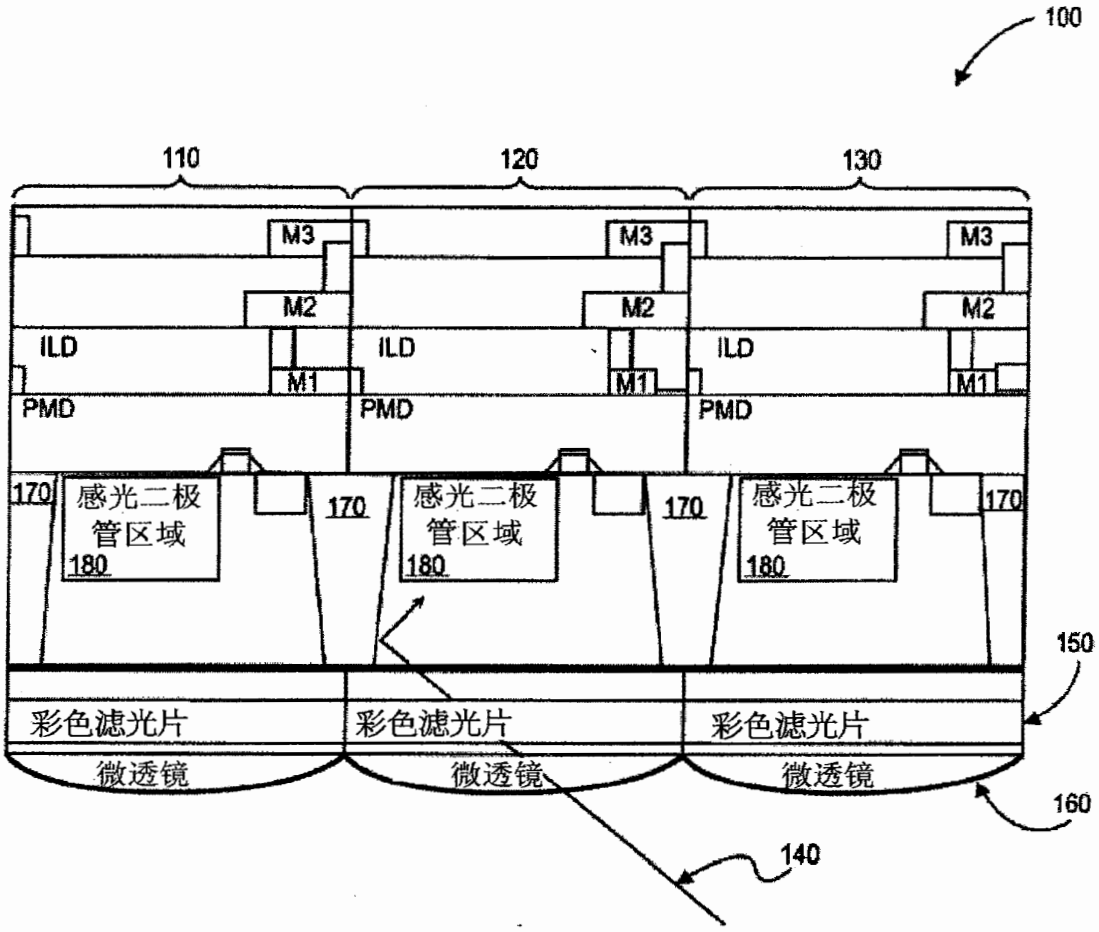


图 1

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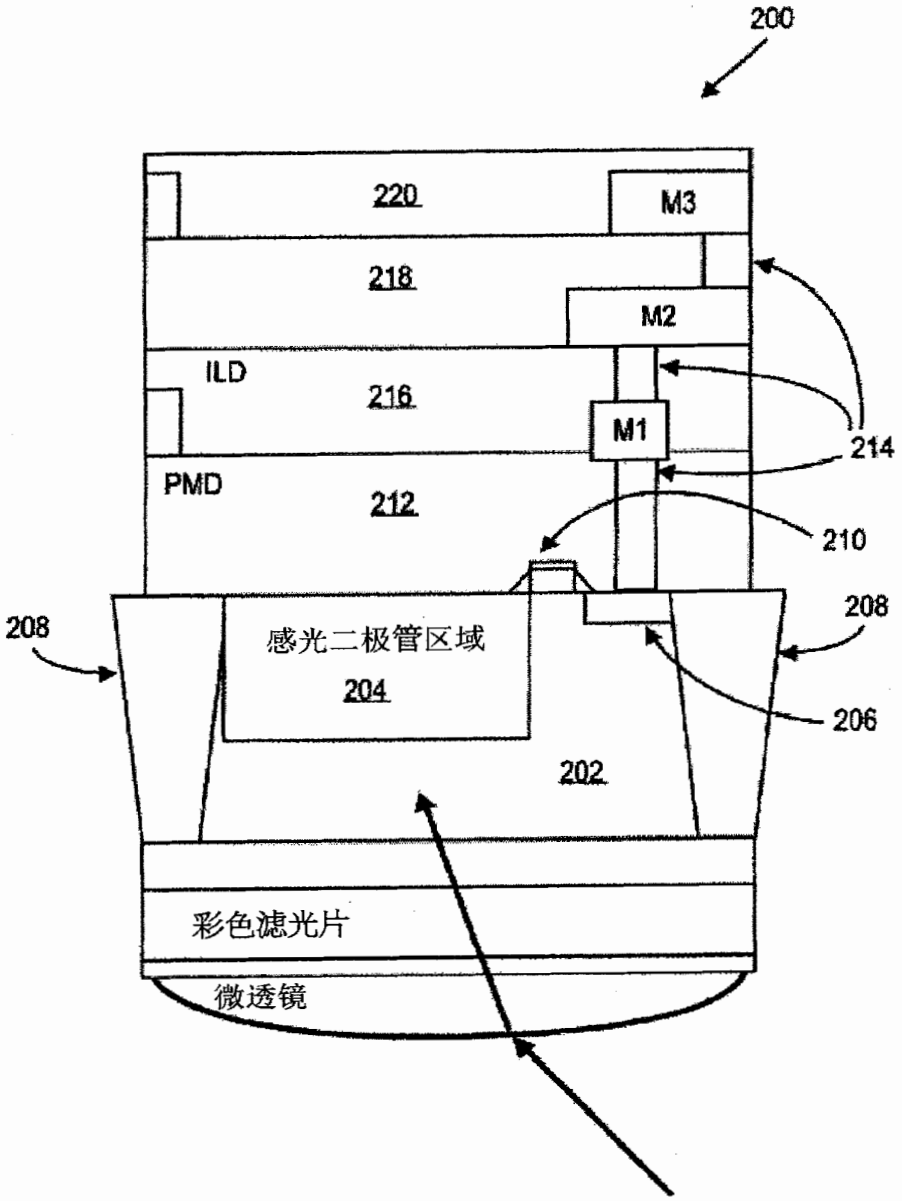


图 2

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Espacenet

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DESCRIPTION CN102270646

The invention provides a back-illuminated CMOS image sensor comprising: a semiconductor substrate having a first surface and a second surface opposite thereto; the semiconductor substrate including at least one pixel cell region; an isolation structure located Between adjacent pixel cell regions; wherein the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate. The present invention reduces crosstalk of electrical signals between adjacent pixel cell regions, improves display fade of CMOS image sensors, and improves imaging quality.

Backlighting CMOS image sensor

Technical field

The present invention relates to an image sensor, and more particularly to a backlit CMOS image sensor.

Background technique

The image sensor is an important part of the digital camera. According to the different components, the image sensor is divided into a Charge Coupled Device (CCD) image sensor and a Complementary Metal-Oxide Semiconductor (CMOS) image sensor. Among them, CMOS image sensors are highly integrated, easily compatible with standard CMOS fabrication processes, and have low power consumption. With the improvement of CMOS fabrication processes, CMOS image sensors have become the mainstream of current image sensors.

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An existing CMOS image sensor is disclosed in Chinese Patent Application No. 200710148796.5. Existing CMOS image sensors include a semiconductor substrate, which typically includes a plurality of pixel cell regions arranged in a matrix with shallow trench isolation structures (STIs) between adjacent pixel cell regions. Please refer to FIG. 1. FIG. 1 is a schematic structural diagram of a conventional CMOS image sensor. The CMOS image sensor includes a semiconductor substrate 100. The semiconductor substrate 100 includes a plurality of pixel unit regions 103. In the figure, there are 2 pixel unit regions. 103 is described as an example; there is a shallow trench isolation structure 106 between adjacent pixel cell regions 103 . The pixel unit area 103 is used to form a pixel. The pixel unit area 103 generally includes a photodiode area 104 and a transistor area 105. The photodiode area 104 is used to form a photodiode, and the photodiode is used for photoelectric conversion. The transistor region 105 is used to form a transistor for amplifying and outputting an electrical signal converted by a photodiode. The shallow trench isolation structure 106 is used for isolation of adjacent pixels. The semiconductor substrate 100 includes a first surface 101 and a second surface 102 opposite thereto. Light enters the pixel unit area 103 from the second surface 102. Those skilled in the art refer to the CMOS image sensor as a Backside illuminated CMOS image sensor.

In practice, it has been found that the above-mentioned back-illuminated CMOS image sensor has a problem of display fading, which affects the imaging quality.

Therefore, there is a need for a back-illuminated CMOS image sensor that can improve the display fading problem and improve the image quality of the CMOS image sensor.

Summary of the Invention

The problem solved by the present invention is to provide a back-illuminated CMOS image sensor capable of improving the display fading problem and improving the image quality of the CMOS image sensor.

To solve the above problem, the present invention provides a backlit CMOS image sensor including:

a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto;

The semiconductor substrate includes at least one pixel unit area;

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The isolation structure is located between adjacent pixel unit regions;

Wherein, the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate.

Optionally, the width of the deep trench isolation structure is less than or equal to 0.25 micrometers.

Optionally, the depth of the deep trench isolation structure ranges from 1.5 to 4 microns.

Optionally, the filler in the deep trench isolation structure is a dielectric.

Optionally, the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate.

Optionally, the semiconductor substrate is sequentially formed with a filter and a microlens, and the filter and the microlens are located on the second surface of the semiconductor substrate.

The invention also provides a method for manufacturing a backlit CMOS image sensor, comprising:

A semiconductor substrate is provided, the semiconductor substrate having a first surface and a third surface opposite thereto, the semiconductor substrate including at least one pixel cell region;

A deep trench isolation structure is formed in the semiconductor substrate along the first surface, the deep trench isolation structure has a bottom along a depth direction of the trench, the trench depth direction is perpendicular to the first surface and the third The surface, the deep trench isolation structure is located between adjacent pixel cell regions;

The bottom of the deep trench isolation structure is used as a stop layer, the semiconductor substrate is thinned along the third surface of the semiconductor substrate, stops at the second surface, and the second surface exposes the deep trench The bottom of the isolation structure.

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Optionally, the thinning method includes a chemical mechanical polishing method.

Optionally, forming the deep trench isolation structure in the semiconductor substrate along the first surface includes the following steps:

Forming a hard mask layer having a first opening between adjacent pixel cell regions of the first surface;

Etching the semiconductor substrate along the first opening to form a second opening in the semiconductor substrate;

Filling the second opening with a dielectric

The hard mask layer is removed to form a deep trench isolation structure.

Optionally, the depth of the deep trench isolation structure ranges from 1.5 to 4 microns.

Optionally, the width of the deep trench isolation structure is less than or equal to 0.25 micrometers.

Optionally, the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate.

Optionally, the method further includes: forming a filter and a micro lens sequentially along the second surface with the pixel unit area, and the method for manufacturing the filter and the micro lens comprises a photolithography step, and The deep trench isolation structure serves as a photolithographically aligned mark.

Compared with the prior art, the present invention has the following advantages:

By providing a deep trench isolation structure penetrating the first surface and the second surface of the

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semiconductor substrate between adjacent pixel cell regions, isolation between adjacent pixels is performed, thereby preventing the photocarriers in the pixel cell region from diffusing to The adjacent pixel unit area reduces the crosstalk caused by electrical signals to the adjacent pixel unit area, improves the display fade of the CMOS image sensor, and improves the imaging quality.

Further, the filler in the deep trench isolation structure is a dielectric, and the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate, and the light totally reflects at the interface between the deep trench isolation structure and the semiconductor substrate. The light is prevented from entering the adjacent pixel unit area through the deep trench isolation structure, the crosstalk to the optical signal of the adjacent pixel unit area is reduced, the display fading of the CMOS image sensor is further improved, and the imaging quality is improved; The dielectric material of the trench isolation structure is silicon oxide and has a different color from the silicon of the semiconductor substrate. In the process of forming a filter and a microlens by a photolithography process, the deep trench isolation structure can be used as an alignment mark for lithography. No special alignment layer is required, saving process steps and reducing production costs.

Description of the drawings

FIG. 1 is a schematic structural diagram of a prior art CMOS image sensor.

FIG. 2 is a schematic structural diagram of a CMOS image sensor according to an embodiment of the present invention.

FIG. 3 is a schematic diagram illustrating the principle of total reflection formed at the interface between the deep trench isolation structure and the semiconductor substrate.

FIG. 4 is a schematic flowchart of a method for manufacturing a CMOS image sensor according to an embodiment of the present invention.

FIG. 5 to FIG. 9 are schematic cross-sectional views of a method for fabricating a CMOS image sensor according to the present invention.

detailed description

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The existing Backside illuminated CMOS image sensor has a problem of display fading. The inventor's research found that the cause of fading is crosstalk of neighboring pixels. One of the reasons for the crosstalk is that the existing shallow trench isolation structure cannot effectively isolate the photocarrier diffusion between adjacent pixel units. Since the incident light of the CMOS image sensor using the backlight illuminates the pixel cell region of the semiconductor substrate through the microlens and the filter, in the prior art, in order to increase the effective photosensitive area of the photodiode in the pixel unit region, the depth of the photodiode is usually higher. Large, its depth can reach more than 10000 Angstroms, while the depth of the existing shallow trench isolation structure is usually 2000 to 5000 Angstroms. In the photoelectric conversion, the photo-generated carriers generated by photoelectric conversion of the photodiode may be diffused, and the existing shallow trench isolation structure cannot effectively isolate the photo-generated carriers so that the photo-generated carriers may go to adjacent pixels. Crosstalk of electrical signals is caused to adjacent pixels, causing the display of the CMOS image sensor to fade.

The back-illuminated CMOS image sensor provided by the present invention solves the crosstalk of electrical signals and improves the display fading problem of CMOS image sensors. The back-illuminated CMOS image sensors include:

a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto;

The semiconductor substrate includes at least one pixel unit area;

The isolation structure is located between adjacent pixel unit regions;

Wherein, the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate.

The technical solutions of the present invention will be described in detail below in conjunction with specific embodiments. Please refer to FIG. 2 . FIG. 2 is a schematic structural diagram of a CMOS image sensor according to an embodiment of the present invention.

The CMOS image sensor includes a semiconductor substrate 200, and the material of the semiconductor substrate 200 may be silicon, SOI, gallium nitride, or gallium arsenide. The semiconductor substrate 200 has a

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first surface 201 and a second surface 202 opposite thereto. In the present embodiment, the semiconductor substrate 200 is a silicon substrate having a P-type conductivity type.

As shown in FIG. 2, the semiconductor substrate 200 includes at least one pixel unit area 203. For convenience of description, the two pixel unit area 203 will be described as an example. There is a deep trench isolation structure 206 between adjacent pixel cell regions 203. The deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200 . The pixel unit region 203 of the semiconductor substrate 200 is formed with a filter 209 and a microlens 210. In this embodiment, the refractive index of the micro lens 210 ranges from 1.2 to 4, and its material may be silicon nitride SiNX, zirconium oxide ZrO2, hafnium oxide HfO2, titanium oxide TiO2, aluminum oxide Al3O2, zinc oxide ZnO2, etc. The range of the refractive index of the filter 209 is 1.4 to 2. The material of the filter 209 may be a photoresist material. The filter 209 and the microlenses 210 are formed by a photolithography process, and the deep trench isolation structure 206 can be used as an alignment mark for photolithography during a photolithography process that forms the filter.

Still referring to FIG. 2, the pixel cell area 203 is used to form a pixel. The pixel cell region 203 includes a photodiode region 204 and a transistor region 205. The photodiode region 204 is used to form a photodiode, which is used for photoelectric conversion, and converts light signals incident from the second surface 202 into corresponding electrical signals to generate photogenerated carriers. The transistor region 205 is used to form a transistor for amplifying and outputting the electrical signal converted by the photodiode. According to actual conditions, the transistor region 205 includes three or more transistors. The transistors have a shallow trench isolation structure and are used to isolate the transistors in the pixels. The depth of the shallow trench isolation structure ranges from 2000 to 5000 Angstroms.

In this embodiment, the deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200 . As an embodiment, the thickness of the semiconductor substrate 200 is in the range of 1.5 to 4 microns. The thickness of the deep trench isolation structure 206 should be the same as the depth of the semiconductor substrate 200, that is, 1.5 to 4 microns. As a preferred embodiment, the thickness of the semiconductor substrate 200 is 2 33 μ m, so that the photodiodes in the pixel unit region 203 can better absorb incident light, and accordingly, the deep trench isolation structure 206 is The depth is preferably in the range of 2 to 3 microns. Since the deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200, the deep trench isolation structure 206 can effectively prevent the photo-generated light generated by the photodiode of the pixel during photoelectric conversion. The flow diffuses to adjacent pixels, reduces the crosstalk of electrical signals to adjacent pixels, improves the pixel fading of the CMOS image sensor, and improves the imaging quality of the CMOS image sensor.

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The width of the deep trench isolation structure 206 is less than or equal to the width of the prior art shallow trench isolation structure to save chip area. As an embodiment, the width of the deep trench isolation structure 206 is 0.25 μm or less.

The filler in the deep trench isolation structure 206 is a dielectric whose refractive index is less than 0.8 times the refractive index of the semiconductor substrate. In this way, when the incident light enters the pixel unit area 203, total reflection is formed at the interface between the deep trench isolation structure 203 and the semiconductor substrate 200, so that incident light is prevented from entering the adjacent pixel unit area 203 through the deep trench isolation structure 206, and adjacent pixel units are The area 203 causes crosstalk of the optical signal, further improving the display fading problem of the CMOS image sensor. In order to facilitate the description of the principle that the light forms a total reflection at the interface between the deep trench isolation structure and the semiconductor substrate, the partial region 300 of the CMOS image sensor in Fig. 2 is enlarged and illustrated. The partial region 300 includes a pixel unit region 203, a corresponding filter 209, a microlens 210, and a deep trench isolation structure 206 on both sides of the pixel unit region 203. Please refer to FIG. 3. FIG. 3 is a schematic diagram illustrating the principle of total reflection formed at the interface between the deep trench isolation structure and the semiconductor substrate.

As shown in FIG. 3, the light A enters the pixel unit area 203 from the air through the micro lens 210, the filter 209, and the second surface 202 of the semiconductor substrate 200. Ideally, the light A is the photodiode of the pixel unit area 203. Absorption, however, may allow light to enter the interface of the deep trench isolation structure 206 and the semiconductor substrate 200 because the light A may have a certain tilt angle. Due to the difference in refractive index between the materials of the air, the microlens 210, the filter 209, and the semiconductor substrate 200, the light A reaches the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 to refract light a plurality of times. Specifically, the normal line between the micro lens 210 and the air interface is O1, the angle between the light line A in the air and the normal line O1 is a1, and after the refraction, the angle between the light line A and the normal line O1 in the micro lens 210 is refracted. A2; The light A is transmitted to the interface between the microlens 210 and the filter 209 in the micro lens 210, the normal of the interface between the micro lens 210 and the filter 209 is O2, and the light A is in the micro lens 210. The included angle of the normal line O2 is a3. After refraction, the angle between the light A in the filter 209 and the normal line O2 is aa4; the light A is transmitted to the filter 209 and the semiconductor liner in the filter 209. The interface of the bottom 200, the normal of the interface between the filter 209 and the semiconductor substrate 200 is O3, and the angle between the light A and the normal O3 in the filter 209 is a5, and after being refracted, The angle a6 between the light A and the normal O3 in the semiconductor substrate 200; within the semiconductor substrate 200, the light A is transmitted to the interface between the semiconductor substrate 200 and the deep trench isolation structure 206. The normal to the interface between the 200 and the deep trench isolation structure 206 is O4, and the angle between the light A and the normal O4 in the semiconductor substrate 200 is β . In this embodiment, the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 is perpendicular to the interface between the filter 209 and the semiconductor substrate 200. Therefore, the normal line O4 is perpendicular to the normal line O3, and thus, the

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angle β and the angle a6. Mutual corner.

Since in practice, the thickness of the micro lens 210 and the thickness of the filter 209 are optimally set by those skilled in the art, it is possible to make the angle a6 the same as the angle a1. The maximum value of the angle a1 is called the chief ray angle (CRA), and the angle of the principal ray tilt angle is in the range of 0 to 35° . Therefore, the angle a6 has an inclination angle ranging from 0 to 35° , and the angle β of the angle β of the angle a6 ranges from 55 to 90° , that is, the incident angle of the light ray and the normal O4 ranges from 55 to 90° . Therefore, assuming that the total reflection critical angle is α , if the light is to be totally reflected at the interface between the semiconductor substrate 200 and the deep trench isolation structure 206, α should be smaller than 55° to ensure the incident angle range between the light and the normal O4. At 55 to 90° , any incident angle is larger than α , and total reflection can be formed when the incident angle of the light and the normal O4 is 55 to 90° . Assuming that the total reflection critical angle is 55° , the refractive index of the semiconductor substrate 200 is x, and the refractive index of the dielectric filled in the deep trench isolation structure 206 is y, then according to the total reflection calculation formula: sin55° /sin90° =y/ x

y=sin55° *x=0.8*x

According to the above analysis, when the total reflection critical angle is 55° , the refractive index of the dielectric filled in the corresponding deep trench isolation structure 206 is 0.8 times the refractive index of the semiconductor substrate 200 .

Since the critical angle α of total reflection depends on the refractive index of the semiconductor substrate 200 and the refractive index of the filled dielectric in the deep trench isolation structure 206. Specifically, in the case where the refractive index of the semiconductor substrate 200 is constant, the smaller the refractive index of the dielectric filled in the deep trench isolation structure 206 is, the smaller the total angle a of the total reflection is. From the foregoing analysis, it can be seen that when the critical angle of total reflection is 55° , the refractive index of the dielectric in the corresponding deep trench isolation result 206 is 0.8 times the refractive index of the semiconductor substrate 200 . To make the total reflection critical angle less than 55° , the refractive index of the dielectric filled in the deep trench isolation structure 206 should be less than 0.8 times the refractive index of the semiconductor substrate 200 to ensure the light A in the deep trench isolation structure 206 and the semiconductor liner The total reflection occurs at the interface of the bottom 200. Therefore, the light A is left in the pixel unit area 203, so as to prevent crosstalk caused by the light A through the deep trench isolation structure 206 to the adjacent pixel unit area, and further improve the display fading phenomenon of the existing CMOS image sensor.

As an embodiment, when the material of the semiconductor substrate 200 is silicon, the filler of the deep trench

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isolation structure 206 may be silicon oxide, and the silicon oxide may have a refractive index less than or equal to 0.8 of the refractive index of silicon. Times. In this embodiment, the refractive index of silicon is 3.46, and the refractive index of silicon oxide is 1.46. In this way, the incident light can form a full reflection at the interface between the deep trench isolation structure 206 and the semiconductor substrate 200. Alternatively, the dielectric filled in the deep trench isolation structure 206 may be of other materials, provided that the refractive index of the dielectric filled in the deep trench isolation structure 206 is less than or equal to 0.8 times the refractive index of the silicon substrate. When the material of the semiconductor substrate 200 is other semiconductor material, the material of the dielectric filled in the deep trench isolation structure 206 may also be other materials, but the dielectric filled in the deep trench isolation structure 206 should have a lower refractive index than the semiconductor substrate. 200 is 0.8 times the refractive index to ensure that total reflection is formed at the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 .

It should be noted that the above analysis is consistent with the width of the deep trench isolation structure 206 along the perpendicular to the first surface 201 and the second surface 202, so that the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 is perpendicular to the first surface 201. The second surface 202 is described as an example. In practice, the width of the deep trench isolation structure 206 in the direction perpendicular to the first surface 201 to the second surface 202 may not be uniform due to the limitation of the manufacturing process, resulting in the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 The first surface 201 and the second surface 202 have a certain inclination angle, but the inclination angle has little influence on the total reflection of the incident light rays at the interface and can be ignored. Therefore, in the case where the refractive index of the filling dielectric in the deep trench isolation structure 206 is less than 0.8 times the refractive index of the semiconductor substrate 200, incident light can be totally reflected at the interface.

The invention also provides a method for manufacturing a CMOS image sensor. Please refer to FIG. 4. FIG. 4 is a schematic flowchart of a method for manufacturing a CMOS image sensor according to an embodiment of the present invention. The method includes:

Step S1, providing a semiconductor substrate, the semiconductor substrate having a first surface and a third surface opposite thereto, the semiconductor substrate including at least one pixel unit area;

In step S2, a deep trench isolation structure is formed along the first surface in the semiconductor substrate, the deep trench isolation structure has a bottom along the trench depth direction, and the trench depth direction is perpendicular to the first surface. And the third surface, the deep trench isolation structure is located between adjacent pixel cell regions;

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Step S3, using the bottom of the deep trench isolation structure as a stop layer, thinning the semiconductor substrate along the third surface of the semiconductor substrate, stopping at the second surface, and exposing the second surface to the second surface. The bottom of the deep trench isolation structure. The technical scheme of the present invention will be described in detail with reference to the following embodiments. Please refer to FIG. 5 to FIG. 9. FIG. 5 to FIG. 9 are schematic cross-sectional views of a method for fabricating a CMOS image sensor according to the present invention.

First, referring to FIG. 5, a semiconductor substrate 200 is provided. The semiconductor substrate 200 has a first surface 201 and a third surface 211 opposite thereto. The semiconductor substrate 200 includes at least one pixel unit area 203. For convenience of description, the two pixel unit areas 203 of this embodiment are taken as an example for illustration. The pixel unit area 203 is for subsequent formation of pixels.

Then, a hard mask layer 207 having a first opening is formed between the adjacent pixel unit regions 203 of the first surface 201, and a material of the hard mask layer 207 may be oxide, silicon nitride, or the like. Then, the semiconductor substrate 200 is etched along the first opening, and a second opening 208 is formed in the semiconductor substrate 200. The second opening 208 is located between adjacent pixel unit regions 203. The second opening 208 has a 211 opening direction perpendicular to the first surface 201 and the third surface.

Next, referring to FIG. 6, a dielectric is filled in the second opening 208. The refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate 200. As an example, when the material of the semiconductor substrate 200 is silicon, the material of the dielectric is selected from silicon oxide. In this embodiment, the refractive index of silicon is 3.46, and the refractive index of silicon oxide is 1.46. Alternatively, when the material of the semiconductor substrate 200 is silicon, the material of the dielectric may be other dielectric (e.g., silicon nitride, silicon oxynitride, or the like) having a refractive index less than 0.8 times that of silicon. In other embodiments, the material of the semiconductor substrate 200 may be other semiconductor materials such as germanium, gallium arsenide, etc., and the material of the dielectric material has a refractive index less than 0.8 times the refractive index of the semiconductor substrate 200 . It can also be silicon nitride or silicon oxynitride. If the material of the dielectric is silicon oxide, the filling method may be high density plasma chemical vapor deposition (HDPCVD) and spin glass (SOG).

Then, referring to FIG. 7 , the dielectrics above the first surface 201 of the hard mask layer 207 and the second opening 208 are removed to form a deep trench isolation structure 206 with a deep trench isolation structure 206 along the trench depth direction. The bottom portion of the bottom portion of the deep trench isolation structure 206 is substantially perpendicular to the first surface 201 and the third surface 211. The deep trench isolation structure 206 has a depth ranging from 1.5 to 4 microns and a width of less than or equal to 0.25 microns. As one embodiment, the method of removing the dielectrics located above the first surface 201 of the hard mask layer 207 and the second opening 208 is a chemical mechanical polishing method.

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8, with the bottom of the deep trench isolation structure 206 as a stop layer, the semiconductor substrate 200 is thinned along the third surface 211 of the semiconductor substrate 200 to stop at the second surface 202. The second surface 202 exposes the bottom of the deep trench isolation structure 206 . The deep trench isolation structure 206 penetrates the first surface 201 of the semiconductor substrate 200 and the second surface 202 opposite thereto. As an embodiment, the thinning method includes a chemical mechanical polishing method. Since the material of the semiconductor substrate 200 is silicon, the dielectric filled in the deep trench isolation structure 206 is silicon oxide. The chemical mechanical polishing step has different polishing rates for silicon and silicon oxide. Therefore, the deep trench isolation structure 206 is The bottom can serve as a grinding stop.

9, a filter 209 and a micro lens 210 are sequentially formed in the pixel unit area 202, and a process of forming the filter 209 and the micro lens 210 includes a photolithography process. Deep trench isolation structure 206 is a photolithographically aligned mark. Since the deep trench isolation structure 206 is filled with an oxide and the material of the semiconductor substrate 200 is silicon, the color of the deep trench isolation structure 206 is different from the color of the semiconductor substrate 200 , and the deep trench isolation structure is exposed during exposure. The 206 can be used as a mark for photolithography alignment. Compared with the prior art special technology for making a photolithography alignment layer, a special photolithography alignment layer is not required, and the process steps are reduced. The material of the filter 209 is the same as the prior art. As an example, the material of the filter 209 is a photoresist material; the material of the micro lens 210 is the same as the prior art, and as an embodiment, the micro lens The material of 210 can be silicon nitride SiNX, zirconium oxide ZrO2, hafnium oxide HfO2, titanium oxide TiO2, aluminum oxide Al3O2, zinc oxide ZnO2, and the like.

In general, after the formation of the deep trench isolation structure 206 and the thinning process of the semiconductor substrate 200, pixels are generally formed in the pixel unit area 203. As a person skilled in the art, it will not be described here in detail.

In summary, the present invention provides a backlit CMOS image sensor having a deep trench isolation structure between pixel cell regions of the backlit CMOS image sensor. The deep trench isolation structure penetrates the semiconductor substrate. The first surface and the second surface are opposite to each other, so as to effectively isolate adjacent pixels, avoid the crosstalk of the electrical signals of adjacent pixels, improve the display fading problem of the CMOS image sensor, and improve the imaging quality. Further, the deep trench isolation structure is internally filled with a dielectric, the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate, and the light forms a total reflection at the interface between the deep trench isolation structure and the semiconductor substrate, avoiding Light enters adjacent pixels, causing crosstalk of optical signals to adjacent pixels, which further improves the display fading problem of CMOS image sensors and improves the imaging quality. At the same time, during the photolithography process of forming the filters and microlenses, the deep trench isolation structure can serve as a mark for photolithographic alignment,

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reducing the number of process steps.

Although the present invention has been disclosed as the preferred embodiments, it is not intended to limit the present invention. Any person skilled in the art can make possible changes and modifications without departing from the spirit and scope of the present invention. Therefore, the present invention The scope of protection shall be subject to the scope defined by the claims of the present invention.

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CLAIMS CN102270646

1.

A backlit CMOS image sensor includes:

一种背面照光的CMOS图像传感器，包括：

a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto;

半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

The semiconductor substrate includes at least one pixel unit area;

所述半导体衬底包括至少一个像素单元区域；

The isolation structure is located between adjacent pixel unit regions;

隔离结构，位于相邻像素单元区域之间；

The method is characterized in that the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates

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其特征在于，所述隔离结构为深沟槽隔离结构、所述深沟槽隔离结构贯穿

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The first surface and the second surface of the semiconductor substrate.

所述半导体衬底的第一表面和第二表面。

2.

The backlight-powered CMOS image sensor according to claim 1, wherein the width of the deep trench isolation structure is 0.25 μ m or less.

如权利要求1所述的背面照光的CMOS图像传感器，其特征在于，所述深沟槽隔离结构的宽度小于等于0.25微米。

3.

The backlight powered CMOS image sensor of claim 1, wherein the deep trench isolation structure has a depth in the range of 1.5 to 4 microns.

如权利要求1所述的背面照光的CMOS图像传感器，其特征在于，所述深沟槽隔离结构的深度范围为1.5～4微米。

4.

The backlight powered CMOS image sensor according to claim 1, wherein the filler in the deep trench isolation structure is a dielectric.

如权利要求1所述的背面照光的CMOS图像传感器，其特征在于，所述深沟槽隔离结构内填充物为电介质。

5.

The backlit CMOS image sensor according to claim 4, wherein the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate.

如权利要求4所述的背面照光的CMOS图像传感器，其特征在于，所述电介质的折射率小于所述半导体衬底的折射率的0.8倍。

6.

The backlight-source CMOS image sensor according to claim 1, wherein the semiconductor substrate is formed with a filter and a microlens in this order, and the filter and the microlens are located on the semiconductor

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substrate. Two surfaces.

如权利要求1所述的背面照光的CMOS图像传感器，其特征在于，所述半 导体衬底的依次形成有滤光片和微透镜，所述滤光片和微透镜位于所述半 导体衬底的第二表面。

7.

A method for fabricating a backside illuminated CMOS image sensor, comprising: providing a semiconductor substrate, the semiconductor substrate having a first surface and a third surface opposite thereto, the semiconductor substrate including at least one pixel Unit area

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一种背面照光的CMOS图像传感器的制作方法，其特征在于，包括：提供半导体衬底，所述半导体衬底具有第一表面和与之相对的第三表面，所述半导体衬底包括至少一个像素单元区域；

A deep trench isolation structure is formed in the semiconductor substrate along the first surface, the deep trench isolation structure has a bottom along a depth direction of the trench, the trench depth direction is perpendicular to the first surface and the third The surface, the deep trench isolation structure is located between adjacent pixel cell regions;

沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构，所述深沟槽隔 离结构具有沿槽深方向的底部，所述槽深方向垂直于所述第一表面和第三 表面，所述深沟槽隔离结构位于相邻的像素单元区域之间；

The bottom of the deep trench isolation structure is used as a stop layer, the semiconductor substrate is thinned along the third surface of the semiconductor substrate, stops at the second surface, and the second surface exposes the deep trench The bottom of the isolation structure.

以所述深沟槽隔离结构的底部为停止层，沿所述半导体衬底第三表面对所 述半导体衬底进行减薄，停止在第二表面，所述第二表面露出所述深沟槽 隔离结构的底部。

8.

The method of fabricating a backlit CMOS image sensor according to claim 7, wherein the thinning method includes a chemical mechanical polishing method.

如权利要求7所述的背面照光的CMOS图像传感器的制作方法，其特征在 于，所述减薄方法包括化学机械研磨的方法。

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9.

The method of fabricating a backlit CMOS image sensor according to claim 7, wherein forming the deep trench isolation structure in the semiconductor substrate along the first surface comprises the following steps:

如权利要求7所述的背面照光的CMOS图像传感器的制作方法，其特征在于，所述沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构包括步骤：

a hard mask layer having a first opening is formed between adjacent pixel cell regions of the first surface; the semiconductor substrate is etched along the first opening, and a second opening is formed in the semiconductor substrate;

在第一表面的相邻像素单元区域之间形成具有第一开口的硬掩膜层；沿所述第一开口对半导体衬底进行刻蚀，在所述半导体衬底内形成第二开口；

Filling the second opening with a dielectric

在所述第二开口内填充电介质，

The hard mask layer is removed to form a deep trench isolation structure.

去除所述硬掩膜层，形成深沟槽隔离结构。

10.

The method of fabricating a backlit CMOS image sensor according to claim 9, wherein the deep trench isolation structure has a depth in the range of 1.5 to 4 microns.

如权利要求9所述的背面照光的CMOS图像传感器的制作方法，其特征在于，所述深沟槽隔离结构的深度范围为1.5～4微米。

11.

The method of fabricating a backlit CMOS image sensor according to claim 9, wherein the width of the deep trench isolation structure is less than or equal to 0.25 micrometers.

如权利要求9所述的背面照光的CMOS图像传感器的制作方法，其特征在于，所述深沟槽隔离结构的宽度小于等于0.25微米。

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12.

The method of fabricating a back light CMOS image sensor according to claim 9, wherein the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate.

如权利要求9所述的背面照光的CMOS图像传感器的制作方法，其特征在于，所述电介质的折射率小于所述半导体衬底的折射率的0.8倍。

13.

The method for fabricating a backlit CMOS image sensor according to claim 7, further comprising: forming a filter and a microlens sequentially along the second surface with the pixel unit area, the filter and The fabrication method of the microlens includes a photolithography step in which the deep trench isolation structure is used as a mark for photolithography alignment.

如权利要求7所述的背面照光的CMOS图像传感器的制作方法，其特征在于，还包括：在与像素单元区域沿所述第二表面依次形成滤光片和微透镜，所述滤光片和微透镜的制作方法包括光刻步骤，所述光刻步骤中以所述深沟槽隔离结构作为光刻对准的标记。

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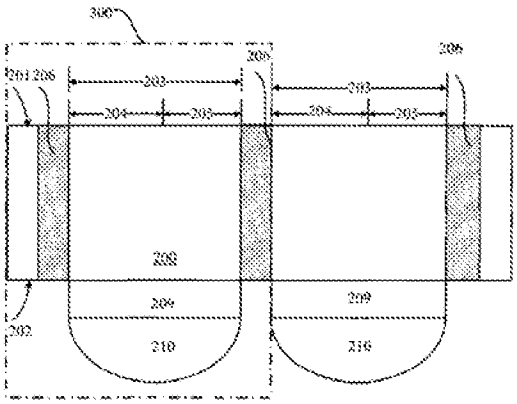
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(54)发明名称

背面照光的CMOS图像传感器

(57)摘要

本发明提供背面照光的CMOS图像传感器，包括：半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；所述半导体衬底包括至少一个像素单元区域；隔离结构，位于相邻像素单元区域之间；其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。本发明减少了相邻像素单元区域之间的电信号的串扰，改善了CMOS图像传感器的显示颜色，提高了成像质量。



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1. 一种背面照光的 CMOS 图像传感器，包括：

半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

所述半导体衬底包括至少一个像素单元区域；

隔离结构，位于相邻像素单元区域之间；

其特征在于，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿

所述半导体衬底的第一表面和第二表面。

2. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

3. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

4. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构内填充物为电介质。

5. 如权利要求 4 所述的背面照光的 CMOS 图像传感器，其特征在于，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

6. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述半导体衬底的依次形成有滤光片和微透镜，所述滤光片和微透镜位于所述半导体衬底的第二表面。

7. 一种背面照光的 CMOS 图像传感器的制作方法，其特征在于，包括：提供半导体衬底，所述半导体衬底具有第一表面和与之相对的第三表面，所述半导体衬底包括至少一个像素单元区域；

沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构，所述深沟槽隔离结构具有沿槽深方向的底部，所述槽深方向垂直于所述第一表面和第三表面，所述深沟槽隔离结构位于相邻的像素单元区域之间；

以所述深沟槽隔离结构的底部为停止层，沿所述半导体衬底第三表面对所述半导体衬底进行减薄，停止在第二表面，所述第二表面露出所述深沟槽隔离结构的底部。

8. 如权利要求 7 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，所述减薄方法包括化学机械研磨的方法。

9. 如权利要求 7 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，所述沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构包括步骤：

在第一表面的相邻像素单元区域之间形成具有第一开口的硬掩膜层；沿所述第一开口对半导体衬底进行刻蚀，在所述半导体衬底内形成第二开口；

在所述第二开口内填充电介质，

去除所述硬掩膜层，形成深沟槽隔离结构。

10. 如权利要求 9 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

11. 如权利要求 9 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

12. 如权利要求 9 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

13. 如权利要求 7 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，还包

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括：在与像素单元区域沿所述第二表面依次形成滤光片和微透镜，所述滤光片和微透镜的制作方法包括光刻步骤，所述光刻步骤中以所述深沟槽隔离结构作为光刻对准的标记。

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背面照光的 CMOS 图像传感器

技术领域

[0001] 本发明涉及图像传感器，特别涉及背面照光的 CMOS 图像传感器。

背景技术

[0002] 图像传感器是组成数字摄像头的重要组成部分，根据元件不同分为电荷耦合 (CCD, Charge Coupled Device) 图像传感器和金属氧化物半导体 (CMOS, Complementary Metal-Oxide Semiconductor) 图像传感器。其中，由于 CMOS 图像传感器集成度高，容易与标准的 CMOS 制作工艺兼容，并且功耗低，随着 CMOS 制作工艺的改进，CMOS 图像传感器成为目前图像传感器的主流技术。

[0003] 在申请号为 200710148796.5 的中国专利申请中公开了一种现有的 CMOS 图像传感器。现有的 CMOS 图像传感器包括半导体衬底，所述半导体衬底通常包括若干呈矩阵排布的像素单元区域，相邻的像素单元区域之间具有浅沟槽隔离结构 (STI)。请参考图 1，图 1 是现有的 CMOS 图像传感器结构示意图，所述 CMOS 图像传感器包括：半导体衬底 100，所述半导体衬底 100 包括若干像素单元区域 103，图中以 2 个像素单元区域 103 为例进行说明；相邻像素单元区域 103 之间具有浅沟槽隔离结构 106。其中所述像素单元区域 103 用于形成像素，通常所述像素单元区域 103 包括光电二极管区域 104 和晶体管区域 105，所述光电二极管区域 104 用于形成光电二极管，所述光电二极管用于光电转换；所述晶体管区域 105 用于形成晶体管，所述晶体管用于将光电二极管转换的电信号放大后输出。所述浅沟槽隔离结构 106 用于相邻像素的隔离。所述半导体衬底 100 包括第一表面 101 和与之相对的第二表面 102。光线从第二表面 102 进入像素单元区域 103 内。本领域技术人员将所述 CMOS 图像传感器称为背面照光的 (Backside illuminated)CMOS 图像传感器。

[0004] 在实际中发现，上述背面照光的 CMOS 图像传感器具有显示褪色的问题，影响了成像质量。

[0005] 因此，需要一种背面照光的 CMOS 图像传感器，能够改善显示褪色的问题，提高 CMOS 图像传感器的成像质量。

发明内容

[0006] 本发明解决的问题是提供了一种背面照光的 CMOS 图像传感器，能够改善显示褪色的问题，提高 CMOS 图像传感器的成像质量。

[0007] 为解决上述问题，本发明提供一种背面照光的 CMOS 图像传感器，包括：

[0008] 半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

[0009] 所述半导体衬底包括至少一个像素单元区域；

[0010] 隔离结构，位于相邻像素单元区域之间；

[0011] 其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。

[0012] 可选的，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

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[0013] 可选的，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

[0014] 可选的，所述深沟槽隔离结构内填充物为电介质。

[0015] 可选的，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

[0016] 可选的，所述半导体衬底的依次形成有滤光片和微透镜，所述滤光片和微透镜位于所述半导体衬底的第二表面。

[0017] 本发明还提供一种背面照光的 CMOS 图像传感器的制作方法，包括：

[0018] 提供半导体衬底，所述半导体衬底具有第一表面和与之相对的第三表面，所述半导体衬底包括至少一个像素单元区域；

[0019] 沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构，所述深沟槽隔离结构具有沿槽深方向的底部，所述槽深方向垂直于所述第一表面和第三表面，所述深沟槽隔离结构位于相邻的像素单元区域之间；

[0020] 以所述深沟槽隔离结构的底部为停止层，沿所述半导体衬底第三表面对所述半导体衬底进行减薄，停止在第二表面，所述第二表面露出所述深沟槽隔离结构的底部。

[0021] 可选的，所述减薄方法包括化学机械研磨的方法。

[0022] 可选的，所述沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构包括步骤：

[0023] 在第一表面的相邻像素单元区域之间形成具有第一开口的硬掩膜层；

[0024] 沿所述第一开口对半导体衬底进行刻蚀，在所述半导体衬底内形成第二开口；

[0025] 在所述第二开口内填充电介质，

[0026] 去除所述硬掩膜层，形成深沟槽隔离结构。

[0027] 可选的，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

[0028] 可选的，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

[0029] 可选的，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

[0030] 可选的，还包括：在与像素单元区域沿所述第二表面依次形成滤光片和微透镜，所述滤光片和微透镜的制作方法包括光刻步骤，所述光刻步骤中以所述深沟槽隔离结构作为光刻对准的标记。

[0031] 与现有技术相比，本发明具有以下优点：

[0032] 通过在相邻像素单元区域之间设置贯穿半导体衬底的第一表面和第二表面的深沟槽隔离结构，进行相邻像素间的隔离，避免了像素单元区域内的光生载流子扩散至相邻像素单元区域，减少对相邻像素单元区域造成电信号的串扰，改善了 CMOS 图像传感器的显示褪色，提高了成像质量。

[0033] 进一步地，所述深沟槽隔离结构内的填充物为电介质，所述电介质的折射率小于半导体衬底折射率的 0.8 倍，光线在深沟槽隔离结构和半导体衬底的界面形成全反射，避免光线经深沟槽隔离结构进入相邻的像素单元区域，减小了对相邻像素单元区域的光信号的串扰，进一步改善了 CMOS 图像传感器的显示褪色，提高了成像质量；所述深沟槽隔离结构填充电介质为氧化硅，与半导体衬底的硅具有不同的颜色，在进行光刻工艺形成滤光片和微透镜的过程中，深沟槽隔离结构可以作为光刻的对准标记，无需专门的对准层，节省了工艺步骤，降低了生产成本。

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附图说明

[0034] 图 1 是现有技术 CMOS 图像传感器结构示意图。

[0035] 图 2 是本发明的一个实施例的 CMOS 图像传感器结构示意图。

[0036] 图 3 是光线在深沟槽隔离结构与半导体衬底界面形成全反射原理示意图。

[0037] 图 4 是本发明的一个实施例的 CMOS 图像传感器的制作方法流程示意图。

[0038] 图 5 ～图 9 是本发明 CMOS 图像传感器制作方法剖面结构示意图。

具体实施方式

[0039] 现有的背面照光的 (Backside illuminated)CMOS 图像传感器存在显示褪色的问题。经发明人研究发现，褪色的原因是相邻像素的串扰 (crosstalk)。所述串扰的原因之一是现有的浅沟槽隔离结构无法有效隔离相邻的像素单元之间光生载流子扩散。由于采用背面照光的 CMOS 图像传感器的入射光线经过微透镜和滤光片进入半导体衬底的像素单元区域，现有技术为了提高像素单元区域内的光电二极管的有效感光面积，通常光电二极管的深度较大，其深度可达 10000 埃以上，而现有的浅沟槽隔离结构的深度范围通常为 2000 ～ 5000 埃。在进行光电转换时，所述光电二极管光电转换所产生的光生载流子可能扩散，而现有的浅沟槽隔离结构无法有效隔离光生载流子，从而光生载流子可能至相邻像素，对相邻像素造成电信号的串扰，从而导致 CMOS 图像传感器的显示褪色。

[0040] 本发明提供的背面照光的 CMOS 图像传感器解决了电信号的串扰，改善了 CMOS 图像传感器的显示褪色问题，所述背面照光的 CMOS 图像传感器包括 ：

[0041] 半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面 ；

[0042] 所述半导体衬底包括至少一个像素单元区域 ；

[0043] 隔离结构，位于相邻像素单元区域之间 ；

[0044] 其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。

[0045] 下面将结合具体的实施例对本发明的技术方案进行详细的说明。请参考图 2，图 2 是本发明一个实施例的 CMOS 图像传感器结构示意图。

[0046] 所述 CMOS 图像传感器包括半导体衬底 200，所述半导体衬底 200 的材料可以是硅、SOI、氮化镓或者砷化镓。所述半导体衬底 200 具有第一表面 201 和与之相对的第二表面 202。本实施例中，所述半导体衬底 200 为具有 P 型导电类型的硅衬底。

[0047] 如图 2，所述半导体衬底 200 包括至少一个像素单元区域 203，为了便于说明，以 2 个像素单元区域 203 为例进行说明。相邻的像素单元区域 203 之间具有深沟槽隔离结构 206。所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和第二表面 202。半导体衬底 200 的像素单元区域 203 形成有滤光片 209 和微透镜 210。本实施例中，所述微透镜 210 的折射率范围为 1.2 ～ 4，其材质可以为氮化硅 SiN_x、氧化锆 ZrO_2、氧化铪 HfO_2、氧化钛 TiO_2、氧化铝 Al_2O_3、氧化锌 ZnO_2 等，所述滤光片 209 的折射率范围为 1.4 ～ 2，其材质可以为光阻材料。所述滤光片 209 和微透镜 210 通过光刻工艺形成，在形成滤光片的光刻工艺过程中，深沟槽隔离结构 206 可以作为光刻的对准标记使用。

[0048] 仍参考图 2，所述像素单元区域 203 用于形成像素。所述像素单元区域 203 包括光电二极管区域 204 和晶体管区域 205。所述光电二极管区域 204 用于形成光电二极管，所述

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光电二极管用于进行光电转换，将从第二表面 202 入射的光信号转换为相应的电信号，产生光生载流子。所述晶体管区域 205 用于形成晶体管，所述晶体管用于将所述光电二极管转换的电信号放大、输出。根据实际情况，所述晶体管区域 205 内包括 3 个或 3 个以上晶体管，所述晶体管之间具有浅沟槽隔离结构，用于像素内的晶体管之间相互隔离。所述浅沟槽隔离结构的深度范围为 2000 ～ 5000 埃。

[0049] 本实施例中，所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和第二表面 202。作为一个实施例，所述半导体衬底 200 的厚度范围为 1.5 ～ 4 微米，所述深沟槽隔离结构 206 的厚度应与所述半导体衬底 200 的深度相同，即为 1.5 ～ 4 微米。作为优选的实施例，所述半导体衬底 200 的厚度为 2 ～ 3 微米，以使得像素单元区域 203 内的光电二极管能更好的吸收入射光线，相应地，所述深沟槽隔离结构 206 的深度范围优选为 2 ～ 3 微米。由于所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和第二表面 202，因此，深沟槽隔离结构 206 可以有效阻止像素的光电二极管在光电转换时产生的光生载流子扩散至相邻像素，减少对相邻像素的电信号的串扰，改善 CMOS 图像传感器的像素褪色，提高了 CMOS 图像传感器的成像质量。

[0050] 所述深沟槽隔离结构 206 的宽度小于或等于现有技术的浅沟槽隔离结构的宽度，以节约芯片面积。作为一个实施例，所述深沟槽隔离结构 206 的宽度范围为小于等于 0.25 微米。

[0051] 所述深沟槽隔离结构 206 内填充物为电介质，所述电介质的折射率小所述半导体衬底的折射率的 0.8 倍。这样入射光线进入像素单元区域 203 时在深沟槽隔离结构 203 与半导体衬底 200 的界面形成全反射，避免入射光线经过深沟槽隔离结构 206 进入相邻像素单元区域 203，对相邻像素单元区域 203 造成光信号的串扰，进一步改善 CMOS 图像传感器的显示褪色的问题。为了便于说明光线在深沟槽隔离结构和半导体衬底的界面形成全反射的原理，对图 2 中 CMOS 图像传感器的部分区域 300 进行放大说明。所述部分区域 300 包括像素单元区域 203、与之对应的滤光片 209、微透镜 210、以及像素单元区域 203 两侧的深沟槽隔离结构 206。请参考图 3，图 3 是光线在深沟槽隔离结构与半导体衬底界面形成全反射原理示意图。

[0052] 如图 3 所示，光线 A 自空气经过微透镜 210、滤光片 209、半导体衬底 200 的第二表面 202 进入像素单元区域 203，理想的状况是，光线 A 被像素单元区域 203 的光电二极管吸收，但是，由于光线 A 可能具有一定倾斜角因此光线可能会入射深沟槽隔离结构 206 与半导体衬底 200 的界面。由于通常空气、微透镜 210、滤光片 209、半导体衬底 200 的材质不同而折射率不同，光线 A 到达深沟槽隔离结构 206 与半导体衬底 200 的界面发生多次光的折射。具体地，在微透镜 210 和空气界面的法线为 01，在空气中光线 A 与所述法线 01 的夹角为 a1，经过折射，在微透镜 210 内光线 A 与法线 01 的夹角为 a2；光线 A 在微透镜 210 内传输至微透镜 210 和滤光片 209 的界面，所述微透镜 210 和滤光片 209 的界面的法线为 02，在微透镜 210 内光线 A 与所述法线 02 的夹角为 a3，经过折射，在滤光片 209 内光线 A 与所述法线 02 的夹角为 aa4；光线 A 在滤光片 209 内传输至滤光片 209 与半导体衬底 200 的界面，所述滤光片 209 与半导体衬底 200 的界面的法线为 03，在滤光片 209 内所述光线 A 与所述法线 03 的夹角为 a5，经过折射，在半导体衬底 200 内光线 A 与法线 03 的夹角 a6；在半导体衬底 200 内，所述光线 A 传输至半导体衬底 200 与所述深沟槽隔离结构 206 的界面，所述半导体

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衬底 200 与所述深沟槽隔离结构 206 的界面的法线为 O4，在半导体衬底 200 内光线 A 与法线 O4 的夹角为 β。本实施例中，深沟槽隔离结构 206 与半导体衬底 200 的界面垂直于滤光片 209 与半导体衬底 200 的界面，因此，法线 O4 与法线 O3 垂直，从而，角度 β 与角度 a6 互为余角。

[0053] 由于在实际中，本领域技术人员对微透镜 210 的厚度、滤光片 209 的厚度进行优化设置，可以使得使得角度 a6 与角度 a1 相同。角度 a1 的最大值称为主光线倾斜角 (chief ray angle，CRA)，而主光线倾斜角的角度范围为 0 ～ 35°。因此，角度 a6 倾斜角度范围为 0 ～ 35°，角度 a6 的余角 β 的角度范围为 55 ～ 90°，即光线与法线 O4 的入射角范围为 55 ～ 90°。因此，假设全反射临界角为 α，若要光线在半导体衬底 200 与深沟槽隔离结构 206 的界面形成全反射，α 应小于为 55°，以保证在光线与法线 O4 的入射角范围为 55 ～ 90° 时，任一入射角均大于 α，从而光线与法线 O4 的入射角为 55 ～ 90° 时可以形成全反射。假设全反射临界角为 55°，半导体衬底 200 的折射率为 x，深沟槽隔离结构 206 内填充的电介质的折射率为 y，则根据全反射计算公式：sin55° /sin90° = y/x

[0054] y = sin55° *x = 0.8*x

[0055] 由上述分析可知，当全反射临界角为 55° 时，对应的深沟槽隔离结构 206 内填充的电介质的折射率为半导体衬底 200 的折射率的 0.8 倍。

[0056] 由于全反射的临界角 α 取决于半导体衬底 200 的折射率和深沟槽隔离结构 206 内填充电介质的折射率关系。具体地，在半导体衬底 200 的折射率一定的情况下，深沟槽隔离结构 206 内填充的电介质的折射率越小，全反射的临界角 α 越小。由前面的分析可知，在全反射的临界角为 55° 时对应的深沟槽隔离结果 206 内的电介质的折射率为半导体衬底 200 折射率的 0.8 倍。若要使得全反射临界角小于 55°，深沟槽隔离结构 206 内填充的电介质的折射率应小于半导体衬底 200 折射率的 0.8 倍，以保证光线 A 在深沟槽隔离结构 206 和半导体衬底 200 的界面发生全反射。从而，光线 A 留在像素单元区域 203 内，避免光线 A 经过深沟槽隔离结构 206 对相邻像素单元区域造成串扰，进一步改善现有的 CMOS 图像传感器的显示褪色现象。

[0057] 作为一个实施例，所述半导体衬底 200 的材质为硅时，所述深沟槽隔离结构 206 的填充物可以为氧化硅，并且所述氧化硅的折射率可以小于等于硅的折射率的 0.8 倍。本实施例中，硅的折射率为 3.46，氧化硅的折射率为 1.46，这样入射光线在深沟槽隔离结构 206 和半导体衬底 200 的界面可以形成全反射。可替代地，在深沟槽隔离结构 206 内填充的电介质的折射率小于等于硅衬底的折射率的 0.8 倍前提下，深沟槽隔离结构 206 内填充的电介质可以为其他材质。当半导体衬底 200 的材质为其他半导体材料时，深沟槽隔离结构 206 内填充的电介质的材质还可以为其他材质，但是深沟槽隔离结构 206 内填充的电介质的折射率应小于半导体衬底 200 折射率的 0.8 倍，以保证在深沟槽隔离结构 206 和半导体衬底 200 的界面形成全反射。

[0058] 需要说明的是，上述分析以深沟槽隔离结构 206 沿垂直于第一表面 201 和第二表面 202 的宽度一致，从而深沟槽隔离结构 206 与半导体衬底 200 的界面为垂直于第一表面 201 和第二表面 202 为例进行说明。在实际中，由于制造工艺的限制，深沟槽隔离结构 206 沿垂直于第一表面 201 至第二表面 202 方向的宽度可能不均匀，导致深沟槽隔离结构 206 与半导体衬底 200 的界面与第一表面 201 和第二表面 202 之间具有一定的倾斜角度，但是

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所述倾斜角度对入射光线在所述界面形成全反射的影响较小，可以忽略不计。因此，在深沟槽隔离结构 206 内填充电介质的折射率小于半导体衬底 200 折射率的 0.8 倍的情况下，入射光线在所述界面可以形成全反射。

[0059] 本发明还提供一种 CMOS 图像传感器的制作方法。请参考图 4，图 4 是本发明一个实施例的 CMOS 图像传感器的制作方法流程示意图。所述方法包括：

[0060] 步骤 S1，提供半导体衬底，所述半导体衬底具有第一表面和与之相对的第三表面，所述半导体衬底包括至少一个像素单元区域；

[0061] 步骤 S2，沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构，所述深沟槽隔离结构具有沿槽深方向的底部，所述槽深方向垂直于所述第一表面和第三表面，所述深沟槽隔离结构位于相邻的像素单元区域之间；

[0062] 步骤 S3，以所述深沟槽隔离结构的底部为停止层，沿所述半导体衬底第三表面对所述半导体衬底进行减薄，停止在第二表面，所述第二表面露出所述深沟槽隔离结构的底部。下面结合实施例对本发明的技术方案进行详细说明。请参考图 5～图 9，图 5～图 9 是本发明的 CMOS 图像传感器制作方法剖面结构示意图。

[0063] 首先，请参考图 5，提供半导体衬底 200，所述半导体衬底 200 具有第一表面 201 和与之相对的第三表面 211。所述半导体衬底 200 包括至少一个像素单元区域 203，为了便于说明，本实施例 2 个像素单元区域 203 为例进行说明。所述像素单元区域 203 用于后续形成像素。

[0064] 然后，在第一表面 201 的相邻的像素单元区域 203 之间形成具有第一开口的硬掩膜层 207，所述硬掩膜层 207 的材质可以为氧化物、氮化硅等。然后，沿所述第一开口对半导体衬底 200 进行刻蚀，在所述半导体衬底 200 内形成第二开口 208，所述第二开口 208 位于相邻像素单元区域 203 之间。所述第二开口 208 具有垂直于第一表面 201 和第三表面的 211 开口方向。

[0065] 接着，参考图 6，在所述第二开口 208 内填充电介质。所述电介质的折射率小于半导体衬底 200 的折射率的 0.8 倍。作为一个实施例，当所述半导体衬底 200 的材质为硅时，所述电介质的材质选自氧化硅。本实施例中，硅的折射率为 3.46，氧化硅的折射率为 1.46。可替代的，当所述半导体衬底 200 的材质为硅时，所述电介质的材质可以为折射率小于硅的折射率的 0.8 倍的其他电介质（例如是氮化硅或氮氧化硅等）。在其他的实施例中，所述半导体衬底 200 的材质可以为锗、砷化镓等其他半导体材料，在折射率小于半导体衬底 200 的折射率的 0.8 倍的前提下，所述电介质的材质也可以为氮化硅或氮氧化硅。若所述电介质的材质为氧化硅，其填充方法可以为高密度等离子体化学气相沉积法 (HDPCVD) 和自旋玻璃法 (SOG)。

[0066] 然后，参考图 7，去除所述硬掩膜层 207 和第二开口 208 的位于第一表面 201 上方的电介质，形成深沟槽隔离结构 206，所述深沟槽隔离结构 206 具有沿槽深方向的底部，所述槽深方向与第二开口 208 的开口方向一致，即所述深沟槽隔离结构 206 的槽深方向垂直于所述第一表面 201 和第三表面 211。所述深沟槽隔离结构 206 的深度范围为 1.5～4 微米，其宽度小于等于 0.25 微米。作为一个实施例，所述去除所述硬掩膜层 207 和第二开口 208 的位于第一表面 201 上方的电介质的方法为化学机械研磨的方法。

[0067] 然后，参考图 8，以所述深沟槽隔离结构 206 的底部为停止层，沿所述半导体衬底

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200 第三表面 211 对半导体衬底 200 进行减薄，停止在第二表面 202，所述第二表面 202 露出所述深沟槽隔离结构 206 的底部。所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和与之相对的第二表面 202。作为一个实施例，所述减薄方法包括化学机械研磨方法。由于半导体衬底 200 的材质为硅，深沟槽隔离结构 206 内填充的电介质为氧化硅，所述化学机械研磨步骤对硅和氧化硅具有不同的研磨速率，因此，深沟槽隔离结构 206 的底部可以作为研磨的停止层。

[0068] 接着，参考图 9，在所述像素单元区域 202 依次形成滤光片 209 和微透镜 210，所述滤光片 209 和微透镜 210 的形成过程包括光刻工艺，所述光刻工艺以所述深沟槽隔离结构 206 为光刻对准的标记。由于深沟槽隔离结构 206 内填充氧化物，而半导体衬底 200 的材质为硅，所述深沟槽隔离结构 206 的颜色与半导体衬底 200 的颜色不同，在曝光时，深沟槽隔离结构 206 可以作为光刻对准的标记，与现有技术专门制作光刻对准层的技术相比，不需要专门的光刻对准层，减少工艺步骤。所述滤光片 209 的材质与现有技术相同，作为一个实施例，滤光片 209 的材质为光阻材料；所述微透镜 210 的材质与现有技术相同，作为一个实施例，微透镜 210 的材质为可以为氮化硅 SiN_x、氧化锆 ZrO_2、氧化铪 HfO_2、氧化钛 TiO_2、氧化铝 Al_2O_3、氧化锌 ZnO_2 等。

[0069] 通常，在深沟槽隔离结构 206 形成之后和对半导体衬底 200 进行减薄工艺之前，通常要在像素单元区域 203 内形成像素。作为本领域技术人员的公知技术，在此不做详细说明。

[0070] 综上，本发明提供了一种背面照光的 CMOS 图像传感器，所述背面照光的 CMOS 图像传感器的像素单元区域之间具有深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和与之相对的第二表面，从而有效隔离相邻像素，避免了相邻像素电信号的串扰，改善了 CMOS 图像传感器的显示褪色问题，提高了成像质量。进一步地，所述深沟槽隔离结构内部填充电介质，所述电介质的折射率小于半导体衬底的折射率的 0.8 倍，光线在深沟槽隔离结构和半导体衬底的界面上形成全反射，避免光线进入相邻像素，对相邻像素造成光信号的串扰，更加改善了 CMOS 图像传感器的显示褪色问题，提高了成像质量。同时，在形成滤光片和微透镜的光刻工艺时，所述深沟槽隔离结构可以作为光刻对准的标记，减少了工艺步骤。

[0071] 本发明虽然以较佳实施例公开如上，但其并不是用来限定本发明，任何本领域技术人员在不脱离本发明的精神和范围内，都可以做出可能的变动和修改，因此本发明的保护范围应当以本发明权利要求所界定的范围为准。

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Surface structure of monocrystalline silicon solar cell and its making process

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The surface structure of monocrystalline silicon solar cell features that the surface of the cell body has turned pyramids and normal pyramid areas comprising several pyramids arranged alternately. The making process of the surface structure includes the following steps: growing 1000-3000 A thick oxide layer on the surface of silicon chip; photoetching the surface of the silica to form required turned pyramid windows; etching the silicon chip to form turned pyramids; removing residual silica; etching the silicon chip to form randomly normal pyramids in the planes between the turned pyramids. The present invention can lower extremely the reflectivity of the surface of solar cell and raise the short-circuit current of the cell, and the present invention may be used widely in industrial production of monocrystalline silicon solar cell.

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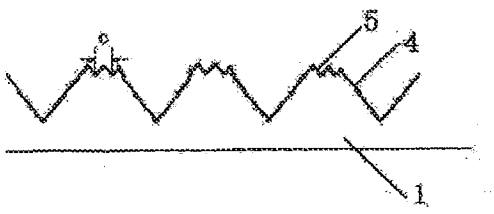
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权利要求书 1 页 说明书 4 页 附图 1 页

[54] 发明名称 单晶硅太阳能电池的表面结构及其制作方法

[57] 摘要

本发明涉及一种单晶硅太阳能电池的表面结构，它包括电池本体，其特征在于：在所述电池本体的表面间隔设置有倒金字塔，在所述倒金字塔之间的平面间隔上设置有由若干正金字塔组成的正金字塔区。这种电池表面的制作方法包括以下步骤：(1)在硅片表面生成厚度为 1000～3000 埃的氧化层；(2)在氧化硅的表面进行光刻，形成所需的倒金字塔窗口；(3)对硅片进行腐蚀，形成倒金字塔；(4)去除残余氧化硅；(5)对硅片进行腐蚀，在倒金字塔之间的平面上随机形成正金字塔。本发明由于采用表面正金字塔和倒金字塔结合的方式，可以最低限度地降低太阳能电池表面的反射率，提高电池的短路电流，同时采用本发明方法，使用普通的光刻机就可以加工，促进了倒金字塔的制作从实验室中走出，走向产业化。本发明可以广泛用于单晶硅太阳能电池的生产中。



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1、一种单晶硅太阳能电池的表面结构，它包括电池本体，其特征在于：在所述电池本体的表面间隔设置有倒金字塔，在所述倒金字塔之间的平面间隔上设置有由若干正金字塔组成的正金字塔区。

2、如权利要求 1 所述的单晶硅太阳能电池的表面结构，其特征在于：所述倒金字塔底边的大小为 8～20 微米，倒金字塔的深度为 5.6～14 微米，所述正金字塔区的宽度为 2～8 微米，正金字塔的大小为 2～8 微米。

3、如权力要求 2 所述的单晶硅太阳能电池的表面结构，其特征在于：所述倒金字塔底边的大小为 10～15 微米，倒金字塔的深度为 7～10 微米，所述正金字塔区的宽度为 2～4 微米，正金字塔的大小为 2～4 微米。

4、一种单晶硅太阳能电池表面的制作方法，其特征在于它包括以下步骤：

（1）在硅片表面生成厚度为 1000～3000 埃的氧化层；

（2）在氧化硅的表面进行光刻，形成所需的倒金字塔窗口；

（3）对硅片进行腐蚀，形成倒金字塔；

（4）去除残余氧化层；

（5）对硅片进行腐蚀，在倒金字塔之间的平面间隔上随机形成正金字塔。

5、如权利要求 4 所述的单晶硅太阳能电池表面的制作方法，其特征在于：其中步骤（1）中的所述硅片表面生成的氧化层厚度为 1000～2000 埃。

6、如权利要求 4 所述的单晶硅太阳能电池表面的制作方法，其特征在于：其中步骤(3)中腐蚀硅片的腐蚀液为氢氧化钾、异丙醇的水溶液，氢氧化钾浓度为 5～10%，异丙醇浓度为 10～20%，反应温度为 75～90℃，腐蚀时间为 10～20 分钟。

7、如权利要求 6 所述的单晶硅太阳能电池表面的制作方法，其特征在于：所述氢氧化钾浓度为 6～8%，所述异丙醇浓度为 14～18%，反应温度为 80～90℃，反应时间为 12～18 分钟。

8、如权利要求 4 所述的单晶硅太阳能电池表面的制作方法，其特征在于：其中步骤（5）中腐蚀硅片的腐蚀液为氢氧化钠、异丙醇的水溶液，氢氧化钠浓度为 0.5～5%，异丙醇浓度为 3～10%，反应温度为 75～90℃，腐蚀时间为 10～30 分钟。

9、如权利要求 8 所述的单晶硅太阳能电池表面的制作方法，其特征在于：所述氢氧化钠浓度为 0.5～2%，所述异丙醇浓度为 5～10%，反应温度为 80～90℃，腐蚀时间为 10～20 分钟。

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单晶硅太阳能电池的表面结构及其制作方法

技术领域

本发明涉及一种太阳能电池表面结构及其制作方法，特别是关于一种能够降低太阳能电池表面反射率的单晶硅太阳能电池的表面结构及其制作方法。

背景技术

在太阳能电池的制作中，降低电池表面的反射损失是十分重要的。在单晶硅太阳能电池中，一般采用表面金字塔结构，以对光进行多次反射，这种结构不仅可以降低光的反射损失，延长光程，增加光生载流子的产量，而且表面的金字塔结构可以增加 pn 结的面积，从而增加对光生载流子的收集率，提高电池的短路电流。

单晶硅表面的金字塔结构是利用硅的各向异性进行定向腐蚀制作而成的，一般来说，晶面间共价键的密度越高，该晶面越难被腐蚀。由于《100》晶面的共价键密度比《111》晶面低，所以《100》晶面比《111》晶面的腐蚀速度快。对于单晶硅而言，选择合适的腐蚀条件，《100》晶面的腐蚀速度可以比《111》晶面的腐蚀速度快数十倍以上。因此《100》晶面的硅片的各向异性腐蚀特性，可以导致在表面形成为《111》晶面的金字塔。

目前制作金字塔的方法主要有两种，一种是制作随机的正金字塔 5（如图 1 所示），另一种是制作倒金字塔 4（如图 2 所示）。

随机正金字塔的制作采用化学腐蚀的方式进行，控制反应液的浓度，温度及反应时间等因素，可以在单晶硅表面形成大小不等的正四方锥（正金字塔），即形成绒面状的硅表面（如图 1 所示）。这种制作方法广泛用于单晶硅太阳能电池的生产中，其工艺比较简单，成本低，但是由于正四方锥的大小不等，其均匀性受到限制。此外，当电池制作中采用表面钝化时，正四方锥顶部的表面钝化容易被破坏，影响钝化效果。

倒金字塔的制作采用光刻和化学腐蚀结合的方式进行。单晶硅片氧化后，进行光刻，即在氧化硅的表面刻出大小一致的窗口，然后进行腐蚀，形成大小一致的倒金字塔（如图 2 所示）。在倒金字塔的制作过程中，根据所设计的图形，可以控制倒金字塔底边及倒金字塔间距离的尺寸。表面倒金字塔结构对降低反射损失，保护表面钝化层的作用是显而易见的，但是由于需要进行光刻，工艺比较复杂，倒金字塔的制作一般仅用于实验室。此外，由于光刻工艺的限制，倒金字塔间一般有 2～4 微米的平面间隔，这种平面间隔的表面反射率损失是不可避免的。

发明内容

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针对上述问题，本发明的目的是提供一种既可以保持金字塔大小较为一致，并保护表面钝化层，又可以进一步降低反射率，避免倒金字塔间反射损失的单晶硅太阳能电池的表面结构及其制作方法。

为实现上述目的，本发明采用以下技术方案：一种单晶硅太阳能电池的表面结构，它包括电池本体，其特征在于：在所述电池本体的表面设置有倒金字塔，在所述倒金字塔之间的平面间隔上设置有若干正金字塔组成的正金字塔区。

所述倒金字塔的底边大小为 8～20 微米，倒金字塔的深度为 5.6～14 微米，所述正金字塔区的宽度为 2～8 微米，正金字塔的大小为 2～8 微米。

当所述倒金字塔底边的大小为 10～15 微米，倒金字塔的深度为 7～10 微米，所述正金字塔区的宽度为 2～4 微米，正金字塔的大小为 2～4 微米时更佳。

一种单晶硅太阳能电池表面的制作方法，其特征在于它包括以下步骤：

（1）在硅片表面生成厚度为 1000～3000 埃的氧化层；

（2）在氧化硅的表面进行光刻，形成所需的倒金字塔窗口；

（3）对硅片进行腐蚀，形成倒金字塔；

（4）去除残余氧化层；

（5）对硅片进行腐蚀，在倒金字塔之间的平面间隔上随机形成正金字塔。

其中步骤（1）中，所述硅片上生成氧化层厚度为 1000～2000 埃时更佳。

其中步骤（3）中，腐蚀硅片的腐蚀液为氢氧化钾、异丙醇的水溶液，氢氧化钾浓度为 5～10%，异丙醇浓度为 10～20%，反应温度为 75～90℃，腐蚀时间为 10～20 分钟。

所述氢氧化钾浓度为 6～8%，所述异丙醇浓度为 14～18%，反应温度为 80～90℃，反应时间 12～18 分钟更佳。

其中步骤（5）中，腐蚀硅片的腐蚀液为氢氧化钠、异丙醇的水溶液，氢氧化钠浓度为 0.5～5%，异丙醇浓度为 3～10%，反应温度为 75～90℃，腐蚀时间为 10～30 分钟。

所述氢氧化钠浓度为 0.5～2%，所述异丙醇浓度为 5～10%，反应温度为 80～90℃，腐蚀时间为 10～20 分钟更佳。

本发明由于采用以上设计，其具有以下优点：1、本发明由于在太阳能电池表面倒金字塔之间的平面间隔上设置了正金字塔区，因此既可以具有倒金字塔大小较为一致的优点，又可以有效地避免倒金字塔间平面间隔造成的反射损失，提高了电池的短路电流。2、本发明由于在倒金字塔之间很窄的区域内形成许多很小的正金字塔，因此其不但最大限度地减少了反射损失，而且使正金字塔对钝化层的影响降到最低，提高了电池的开路电压。3、本发明由于采用倒金字塔与正金字塔结合的

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方式，因此对倒金字塔之间的平面间隔可以适当地放宽而不怕反射损失，进而使倒金字塔的形成工艺要求降低，使用普通的光刻机就可以加工，促进了倒金字塔的制作从实验室中走出，走向产业化。4、本发明的制作方法是利用《100》晶面比《111》晶面的腐蚀速度快的原理，在电池通过光刻腐蚀形成大小一致的倒金字塔之后，去除氧化层，将硅片整个放入腐蚀液中，由于《100》晶面的腐蚀速度可以比《111》晶面快数十倍以上，因此可以在倒金字塔之间的平面间隔上很快地随机形成正金字塔区，但在已形成的倒金字塔表面上却不会形成正金字塔，这种对《111》晶面的轻微腐蚀作用，仅形成毛面，而这一毛面的形成又可以进一步减少反射损失。

下面结合附图和实施例对本发明作进一步说明。

附图说明

图 1 是现有技术中表面随机正金字塔（绒面）结构示意图

图 2 是现有技术中表面倒金字塔结构示意图

图 3 是本发明硅表面生成氧化硅示意图

图 4 是本发明光刻技术形成倒金字塔窗口示意图

图 5 是本发明腐蚀倒金字塔后示意图

图 6 是本发明去除氧化硅后示意图

图 7 是本发明腐蚀正金字塔后形成的正、倒金字塔结合结构示意图

具体实施方式

本发明的单晶硅太阳能电池是在电池本体表面设置正、倒金字塔相结合的结构形式，即在倒金字塔之间的平面间隔上设置有由若干正金字塔组成的正金字塔区。

本发明正金字塔和倒金字塔结合的表面结构，可以采用下面的制作方法而成：如图 3 所示，首先在单晶硅硅片 1 上生成厚度为 1000～3000 埃的氧化层 2，然后采用光刻技术在硅片 1 表面形成窗口 3（如图 4 所示），对窗口 3 进行腐蚀，在窗口 3 中形成倒金字塔 4（如图 5 所示），去除残存的氧化层 2 后，便可以在硅片 1 表面形成倒金字塔 4（如图 6 所示）。再对硅片进行第二次腐蚀后，利用硅片 1 上倒金字塔之间的平面间隔（即《100》晶面）比倒金字塔表面（即《111》晶面）的腐蚀速度快的原理，在倒金字塔 5 之间的平面间隔上形成由若干很小的正金字塔组成的正金字塔区(如图 7 所示)，从而形成了本发明倒金字塔 4 与正金字塔 5 结合的表面结构。

在上述制作过程中，腐蚀是十分关键的，腐蚀窗口采用氢氧化钾，异丙醇的水溶液。氢氧化钾浓度控制在 5～10%，，异丙醇浓度控制在 10～20%，反应温度控制在 75～90°C，腐蚀时间控制在 10～20 分钟。

上述氢氧化钾浓度控制在 6～8%，异丙醇浓度控制在 14～18%，反应温度控制在 80～90°C，腐蚀时间控制在 12～18 分钟更佳。

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腐蚀正金字塔的过程也十分关键，腐蚀采用氢氧化钠，异丙醇的水溶液。氢氧化钠浓度控制在 0.5～5%，异丙醇浓度控制在 3～10%，反应温度控制在 75～90°C，腐蚀时间控制在 10～30 分钟。

上述氢氧化钠浓度控制在 0.5～2%，异丙醇浓度控制在 5～10%，反应温度控制在 80～90°C，腐蚀时间控制在 10～20 分钟更佳。

下面举几个实施例，进一步说明本发明。

实施例一

如图 3～7 所示，在硅片 1 上生成厚度为 1100 埃的氧化层 2，通过光刻形成边长 a 为 10 微米，间隔 b 为 3 微米的窗口 3，然后用氢氧化钾浓度为 6.5%，异丙醇浓度为 15%的水溶液进行腐蚀，反应温度为 85°C，反应时间 16 分钟，然后去除氧化层 2 后形成底边 a 为 10 微米，间隔 b 为 3 微米的倒金字塔 4。再用氢氧化钠为 2%，异丙醇浓度为 10%的水溶液进行腐蚀，反应温度为 90°C，反应时间 12 分钟，即可得到随机形成的若干正金字塔 5。

实施例二

在硅片 1 上生成厚度为 1300 埃的氧化层 2，通过光刻形成的窗口，用氢氧化钾浓度为 7%，异丙醇浓度为 16%的水溶液进行腐蚀，反应温度为 85°C，反应时间 14 分钟，然后去除氧化层 2 后形成底边 a 为 12 微米，间隔 b 为 2 微米的倒金字塔 4。再用氢氧化钠浓度为 1.5%，异丙醇浓度为 6%的水溶液进行腐蚀，反应温度为 85°C 反应时间 15 分钟，即可得到随机形成的若干正金字塔 5。

实施例三

在硅片 1 上生成厚度为 1500 埃的氧化层 2，通过光刻形成边长 a 为 14 微米，间隔 b 为 3 微米的窗口 3，用氢氧化钾浓度为 7.5%，异丙醇浓度为 13%的水溶液进行腐蚀，反应温度为 88°C，反应时间 15 分钟，然后去除氧化层 2 后形成底边 a 为 14 微米，间隔 b 为 3 微米的倒金字塔 4。再用氢氧化钠浓度为 1%，异丙醇浓度为 5%的水溶液进行腐蚀，反应温度为 82°C，反应时间 20 分钟，即可得到随机形成的若干正金字塔 5。

上述各实施例中，倒金字塔 4 的底边 a 可以控制在 8～20 微米之间，倒金字塔 4 深度 h 可以控制在 5.6～14 微米之间。而正金字塔区的宽度 b（也就是倒金字塔 4 之间的平面间隔）控制 2～8 微米之间，正金字塔 5 的大小 c 控制在 2～8 微米之间。

上述对正、倒金字塔 5、4 尺寸的控制中，当倒金字塔底边 a 为 10～15 微米，倒金字塔深度 h 为 7～10 微米，正金字塔区的宽度 b 为 2～4 微米，正金字塔的大小 c 为 2～4 微米时更佳。

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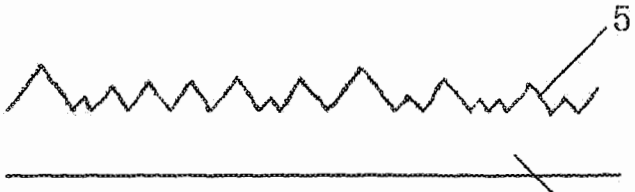


图 1

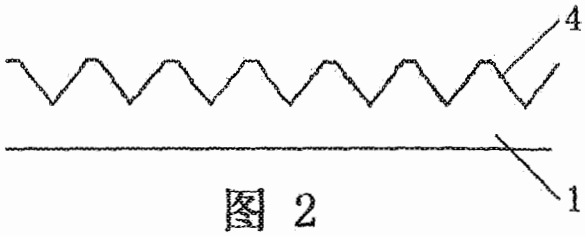


图 2

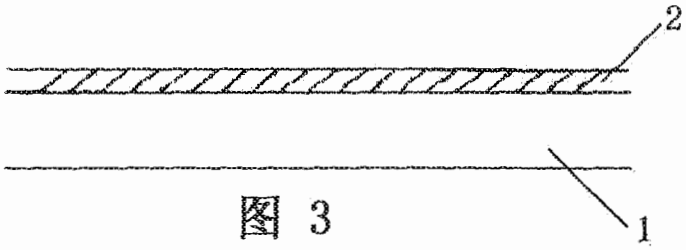


图 3

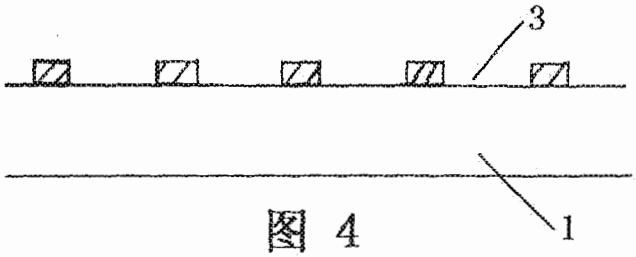


图 4

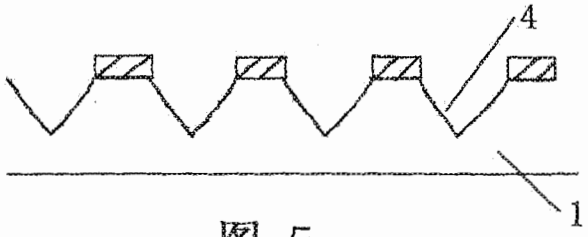


图 5

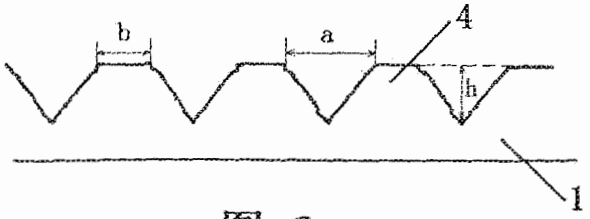


图 6

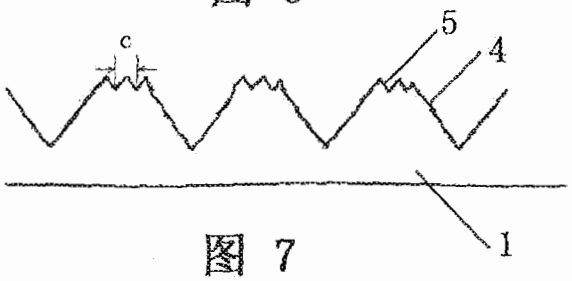


图 7

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Espacenet

Bibliographic data: CN1614789 (A) — 2005-05-11

Method for preparing polycrystalline silicon suede

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Abstract of CN1614789 (A)

The pile fabrics of polycrystalline silicon wafer are made by using acid corrosion solution. The acid corrosion solution is a mixed liquor of oxidant and hydrofluoric acid. The concentration range of oxidant is 0.01-0.5 mole/ liter. The concentration range of hydrofluoric solution is 1-15 mole/liter. The temperature range is 5-50deg.C. The range of acid corrosion time is 5-60 min.

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[43] 公开日 2005 年 5 月 11 日

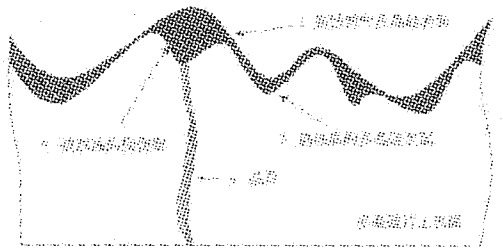
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权利要求书 1 页 说明书 5 页 附图 3 页

[54] 发明名称 一种制备多晶硅绒面的方法

[57] 摘要

本发明属于制造多晶硅太阳能电池领域，涉及制备多晶硅片绒面技术。按照本发明所提供的设计方案，该多晶硅片绒面用酸腐蚀溶液制成，该酸腐蚀溶液是一种氧化剂和氢氟酸混合液，其中，氧化剂的浓度范围为 0.01 到 0.5 摩尔/升，氢氟酸的浓度范围为 1 到 15 摩尔/升，温度范围为 5 摄氏度到 50 摄氏度，酸腐蚀时间范围为 5 分钟到 60 分钟。相比传统的采用碱溶液(NaOH 或 KOH)清除损伤层的方法，经本发明的酸腐蚀溶液腐蚀后的多晶硅片不仅可以形成均匀的绒面，而且可以提高太阳能电池转化效率 5%以上。若将本发明的绒面多晶硅太阳能电池层压成组件，可进一步提高转换效率 3%。本发明所提供的方法具有成本低，易操作和适宜大规模生产等特点。



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1、一种制备多晶硅绒面的方法，其特征在于，该多晶硅片绒面用酸腐蚀溶液制成，该酸腐蚀溶液是一种氧化剂和氢氟酸混合液，其中，氧化剂的浓度范围为 0.01 到 0.5 摩尔/升，氢氟酸的浓度范围为 1 到 15 摩尔/升，温度范围为 5 摄氏度到 50 摄氏度，酸腐蚀时间范围为 5 分钟到 60 分钟。

2、根据权利要求 1 所述的多晶硅绒面的制备方法，其特征在于，在酸腐蚀时，把多晶硅片浸泡在该酸腐蚀溶液中。

3、根据权利要求 1 所述的多晶硅绒面的制备方法，其特征在于，氧化剂是 CrO_3 或 $K_2Cr_2O_7$ 或它们的混合物。

4、根据权利要求 1 所述的多晶硅绒面的制备方法，其特征在于，多晶硅片经过酸腐蚀溶液腐蚀后，表面形成了大小为 1 到 15 微米的绒面。

5、根据权利要求 1 所述的多晶硅绒面的制备方法，其特征在于，被腐蚀的多晶硅片厚度为 5~20 微米。

6、根据权利要求 1 所述的多晶硅绒面的制备方法，其特征在于，该多晶硅片绒面是在对损伤层的清洗过程中完成的。

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一种制备多晶硅绒面的方法

技术领域

本发明是有关制备太阳能电池的技术，特别是涉及利用多晶硅片制备太阳能电池的技术。本发明提供了一个制备多晶硅片绒面的方法。使用本发明的方法制备多晶硅片绒面，能提高多晶硅太阳能电池的转换效率 5%以上。本发明所提供的方法具有成本低，易操作和适宜大规模生产等特点。

背景技术

自从太阳能电池问世以来，提高太阳能电池的转换效率一直是科学家和工程师们努力追求的目标。改善太阳能电池本征特性和提高太阳能电池吸收光的能力是提高太阳能电池转换效率的两个主要方向。减反膜和绒面是提高太阳能电池吸收光的主要手段。因此，在太阳能电池领域中，怎样制备一个有效的绒面是一个非常热门的课题。

所谓的绒面就是指存在于物体表面上的一系列有规则或无规则的高低不同和大小不同的表面形状。由于绒面的存在，物体表面的反射率就会大大降低。换句话说，物体表面的绒面可增加光的吸收。因此绒面技术被广泛地应用在太阳能电池领域。

单晶硅片绒面制备技术开发得较早，并且比较成熟。该技术是利用晶体硅的各种晶相在特定条件下被腐蚀速率有所不同的特性来制备绒面的。利用这个特性，很容易在单晶硅片上制备出金字塔型绒面。

但是，由于多晶硅存在各种晶相，单晶硅片制绒技术不能在多晶硅片表面产生有效的绒面。因此，必须开发特殊的工艺来制备多晶硅绒面。例如，掩膜腐蚀法就是一个非常成功的绒面制备技术。用这个方法制备的多晶硅绒面，再配合使用其他一些先进工艺，创造了至今保持着的多晶硅太阳能电池转换效率的世界记录。尽管掩膜腐蚀法可以大幅度地降低多晶硅片的反射率，但由于工艺复杂性，掩膜腐蚀法还不能在工业生产中得到应用。

在多晶硅片表面上形成一层多孔硅层也具有良好的减反效果。可是，制备一个有效的多孔硅，要求对各项操作进行非常严格地控制。另外，多孔硅层使多晶硅片变得非常的脆弱，为后续工艺的操作带来很多问题。因此用多孔硅层来降低反射率的技术基本上也没有多大的商业价值。相对说来，用等离子刻蚀

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的方法制备多晶硅绒面可能有些商业价值。但是，较大的设备成本和操作成本还是阻碍了该方法的大规模应用。

发明目的

本发明的目的之一是寻求一种制备多晶硅绒面的方法。该方法能使多晶硅片表面的反射率降低，从而提高多晶硅太阳能电池的转换效率。

本发明的另一目的是开发一个能在工业生产的多晶硅片上制备绒面的方法。该方法应该有大规模生产的商业价值，即该方法具有成本低，操作简单等特点。

本发明的最后一个目的是开发一个能很容易地应用于现有多晶硅太阳能电池生产线上的制备多晶硅片绒面的方法。该方法可以直接应用于传统的多晶硅片太阳能电池生产线，而不需要添加额外的生产设备。

按照本发明所提供的设计方案，该多晶硅片绒面用酸腐蚀溶液制成，该酸腐蚀溶液是一种氧化剂和氢氟酸混合液，其中，氧化剂的浓度范围为 0.01 到 0.5 摩尔/升，氢氟酸的浓度范围为 1 到 15 摩尔/升，温度范围为 5 摄氏度到 50 摄氏度，酸腐蚀时间范围为 5 分钟到 60 分钟。

在酸腐蚀时，把多晶硅片浸泡在该酸腐蚀溶液中。氧化剂是 CrO_3 或 $K_2Cr_2O_7$ 或它们的混合物。多晶硅片经过酸腐蚀溶液腐蚀后，表面形成了大小为 1 到 15 微米的绒面。被腐蚀的多晶硅片厚度为 5~20 微米。该多晶硅片绒面是在对损伤层的清洗过程中完成的。

用于本发明的多晶硅片一般是 P 型多晶硅片。但是本发明并不局限于 P 型多晶硅片，本发明还适用于 N 型多晶硅片，或者其它半导体材料。

本发明所使用的多晶硅片是采用线切割的方法把硅锭切割而成的。这种多晶硅片厚度一般在 200 到 400 微米范围内。这种多晶硅片应该是干净的，没有任何有机物质污染。在切割硅锭的过程中，多晶硅片表面与碳化硅微粒和钢丝剧烈摩擦，在多晶硅片的表面生成了一层厚度不均匀的损伤层。这层损伤层是半导体电子和空穴的复合源。所以在太阳能电池生产过程中，首先要把这层损伤层清除干净。清除这层损伤层的传统工艺是用 NaOH 或 KOH 溶液腐蚀多晶硅片。由于在多晶硅存在多种晶相，传统的 NaOH 和 KOH 腐蚀方法不仅不能在多晶硅表面生成有效的绒面，反而会使得多晶硅片的大部分表面变得非常光滑，导致反射率增高。

本发明提供了一种腐蚀多晶硅片的方法。该腐蚀方法的特征是损伤层在本发明的腐蚀溶液内被腐蚀的速率要比多晶硅被腐蚀的速率大。因此损伤层厚度

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不均匀的特性能在损伤层被完全腐蚀后被保留下来。这样，在损伤层被腐蚀后，多晶硅片表面形状就是一个非常有效的绒面。这种绒面能大大降低多晶硅片的表面反射率。

本发明的一个重要特征就是本发明不需要特殊的制绒过程。在传统的制绒过程中，多晶硅片先要在清洗过程中去除损伤层，然后再制备绒面。在本发明中，损伤层的清洗过程就是制绒过程。这样，本发明就有操作简单和成本低的特点。

本发明的清洗和制绒过程是一个酸腐蚀过程。本发明的酸腐蚀过程是把多晶硅片放入一种酸腐蚀溶液中浸泡。本发明所使用的酸腐蚀溶液是由氢氟酸和某种氧化剂所组成。本发明所使用的氧化剂是 CrO_3。但本发明的氧化剂并不局限于 CrO_3。例如，还可以使用 $K_2Cr_2O_7$ 或者 CrO_3 和 $K_2Cr_2O_7$ 的混合物。

当把多晶硅片浸泡在酸腐蚀溶液中，多晶硅片首先被氧化剂氧化，生成 SiO_2。然后，酸腐蚀溶液中的氢氟酸很容易地将 SiO_2 腐蚀生成硅酸盐。在整个酸腐蚀过成中，氧化反应的速率小于氢氟酸和 SiO_2 的反应速率。或者说，本发明的酸腐蚀多晶硅片的过程是一个氧化反应速率控制过程。

在本发明中，控制氧化反应速率是非常重要的。控制氧化反应速率的目的使腐蚀损伤层的速率大大超过腐蚀多晶硅的速率。控制氧化剂浓度是控制氧化反应速率的一个重要手段。本发明所使用的氧化剂浓度为 0.01 到 0.5 摩尔/升。

另一个控制氧化反应速率的重要因素是酸腐蚀溶液的温度。本发明的酸腐蚀溶液温度控制在 5 摄氏度到 50 摄氏度。本发明进一步发现当反应温度控制在 20 摄氏度到 30 摄氏度时，能得到最佳的绒面效果。也就是说，本发明的酸腐蚀溶液是控制在常温下操作。这样既降低了生产成本，又有容易操作的特点。

由于本发明的酸腐蚀是氧化反应控制过程，因此，氢氟酸的浓度在本发明中可有较大的变化范围。它的变化范围可从 1 到 15 摩尔/升。

在经过本发明的酸腐蚀溶液腐蚀后，用去离子水对多晶硅片表面进行适当的清洗。经过去离子水清洗的多晶硅片就可以直接用作多晶硅太阳能电池的制备。例如，可以直接去进行 N+型扩散。这就是说，本发明的酸腐蚀过程，既是一个去除损伤层的过程，也是一个制备了多晶硅片绒面的过程。因此采用本发明的技术，可以大大节约生产成本。

多晶硅片在经过本发明的酸腐蚀溶液腐蚀后，表面形成了大小为 1 到 15 微米的绒面。这种绒面能有效的降低多晶硅片表面的反射率。使多晶硅片太阳能电池的电流密度大大提高，即大大提高了多晶硅片太阳能电池的转换效率。

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由于本发明的酸腐蚀溶液能有效地腐蚀损伤层，而对晶体硅的腐蚀相对比较慢。因此本发明的酸腐蚀溶液能有效地避免了产生晶格之间高低不平的现象。所以本发明所制得的绒面对后续工艺，特别对电极印刷工艺，有很好的帮助。从而进一步提高了多晶硅片太阳能电池的转换效率。由于同样的原因，本发明的酸腐蚀溶液不需要腐蚀过多的多晶硅。被腐蚀的多晶硅片厚度一般在 10 微米左右。这不仅提高了多晶硅太阳能电池的机械强度，也有助于提高电流密度，即提高了多晶硅片太阳能电池的转换效率。

本发明的绒面制备技术不仅提高了多晶硅太阳能电池的转换效率，而且还能明显地提高多晶硅太阳能电池组件的转换效率。由于多晶硅表面的绒面，使得从多晶硅表面反射的光在玻璃的上表面有较大入射角，增加了全反射光。因此本发明的多晶硅绒面太阳能电池，在层压成组件之后，比一般多晶硅太阳能电池组件增加至少 3%的转换效率。

附图说明

图 1 为本发明制备多晶硅片绒面原理图。本发明的酸腐蚀溶液能较快地腐蚀损伤层。腐蚀后的多晶硅表面形状保留了损伤层的表面特性。其中，1 是由线切割所形成的表面特性。2 是被本发明的酸腐蚀溶液所腐蚀的损伤层部分。3 是腐蚀后所形成的绒面。4 是多晶硅的晶界。

图 2 为实例 1 的多晶硅片绒面的反射率和没有绒面的多晶硅片的反射率的比较。

图 3 为实例 2 的多晶硅片绒面在镀上减反膜后的反射率和没有绒面的多晶硅片在镀上减反膜后的反射率的比较

图 4 为实例 3 的多晶硅片绒面太阳能电池的量子效应反射率。

图 5 为多晶硅绒面在层压之后，进一步减少反射光的原理图。多晶硅表面的绒面增加了反射到玻璃上表面的入射角，也就是增加了全反射光，即捕获大部分从多晶硅表面反射的光。

具体实施方式

实例 1

将 0.01 摩尔/升的 $K_2Cr_2O_7$ 溶液与 10 摩尔/升的氢氟酸（氢氟酸）溶液混合。搅拌均匀后将该溶液的温度控制在 50 摄氏度。直接将不经过特殊清洗的线切割制得的 125*125 平方毫米的 P 型多晶硅片放入该混合液浸泡 5 分钟。测得多晶硅片减薄量为 15 微米。然后把该多晶硅片制成太阳能电池。该太阳能电池的转换效率，填充因子，开路电压和电流分别为 14.5%，0.774，595 毫伏和 4.97 安

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培。

实例 2。

将 0.15 摩尔/升的 CrO_3 溶液与 7 摩尔/升的氢氟酸溶液混合。搅拌均匀后将该溶液的温度控制在 30 摄氏度。直接将不经过特殊清洗的线切割制得的 125*125 平方毫米的 P 型多晶硅片放入该混合液浸泡 10 分钟。测得多晶硅片减薄量为 8 微米。然后把该多晶硅片制成太阳能电池。该太阳能电池的转换效率，填充因子，开路电压和电流分别为 14.95%，0.774，598 毫伏和 5.05 安培。

实例 3。

将 0.5 摩尔/升的 CrO_3 和 $K_2Cr_2O_7$ 的混合物溶液与 1 摩尔/升的氢氟酸溶液混合。搅拌均匀后将该溶液的温度控制在 5 摄氏度。直接将不经过特殊清洗的线切割制得的 125*125 平方毫米的 P 型多晶硅片放入该混合液浸泡 60 分钟。测得多晶硅片减薄量为 20 微米。然后把该多晶硅片制成太阳能电池。该太阳能电池的转换效率，填充因子，开路电压和电流分别为 15.1%，0.773，598 毫伏和 5.11 安培。

实例 4。

将 0.1 摩尔/升的 CrO_3 溶液与 15 摩尔/升的氢氟酸溶液混合。搅拌均匀后将该溶液的温度控制在 10 摄氏度。直接将不经过特殊清洗的线切割制得的 125*125 平方毫米的 P 型多晶硅片放入该混合液浸泡 40 分钟。测得多晶硅片减薄量为 5 微米。然后把该多晶硅片制成太阳能电池。该太阳能电池的转换效率，填充因子，开路电压和电流分别为 15.1%，0.773，597 毫伏和 5.05 安培。

实例 5。

将 3.75 公斤 NaOH 加入 15 升水中。搅拌均匀后将该溶液的温度控制在 70 摄氏度。直接将不经过特殊清洗的线切割制得的 125*125 平方毫米的 P 型多晶硅片放入该混合液浸泡 20 分钟。然后把该多晶硅片制成太阳能电池。该太阳能电池的转换效率，填充因子，开路电压和电流分别为 13.98%，0.756，591 毫伏，4.58 安培。

实例 6。

将 36 片平均电流为 4.98 安培绒面多晶硅太阳能电池层压成组件，测得该组件的在一个日光照下电流，电压和输出功率分别为 5.148 安培，22 伏和 86 瓦。

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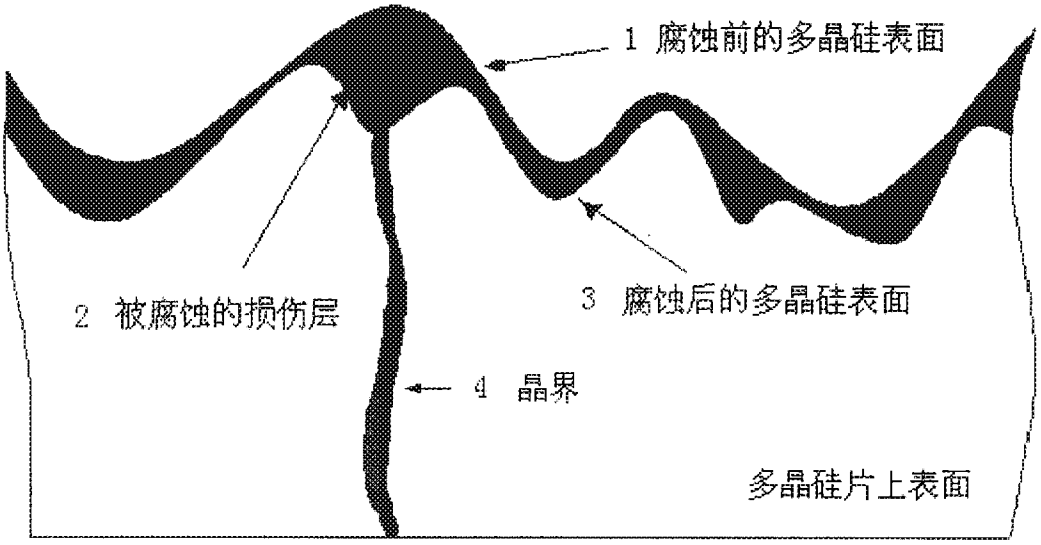


图 1

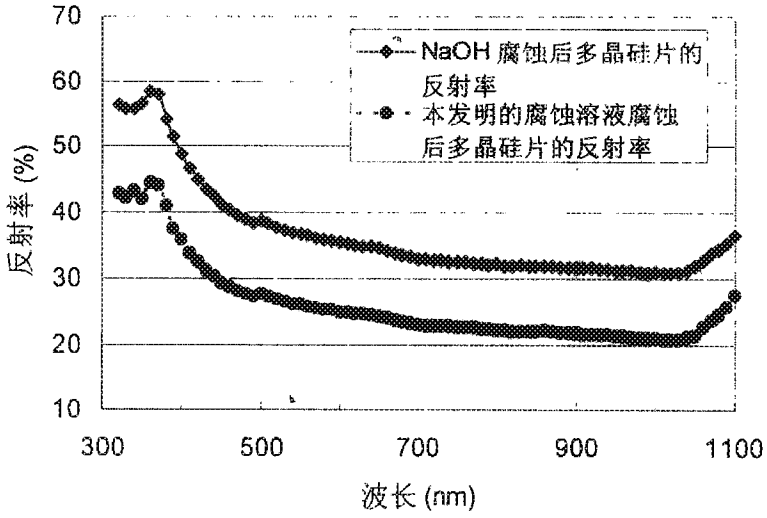


图 2

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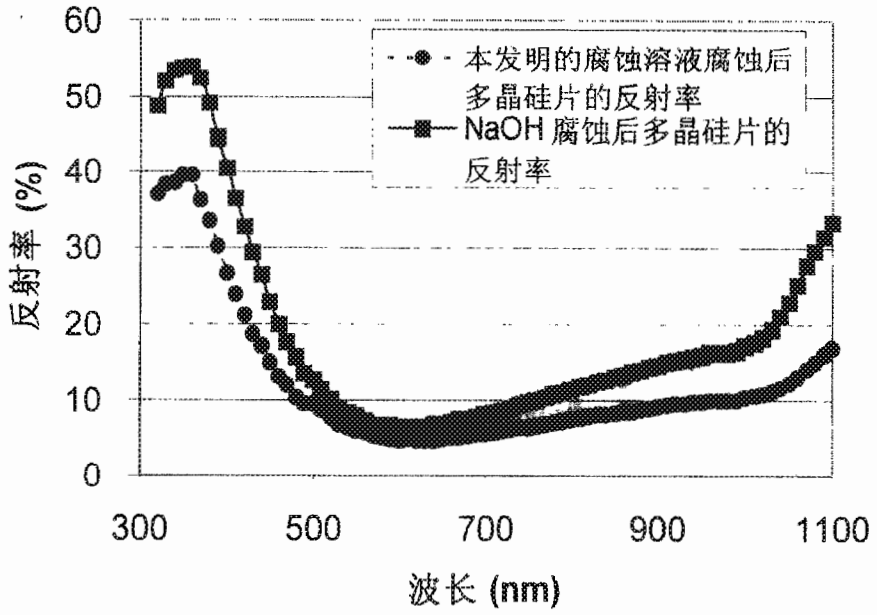


图 3

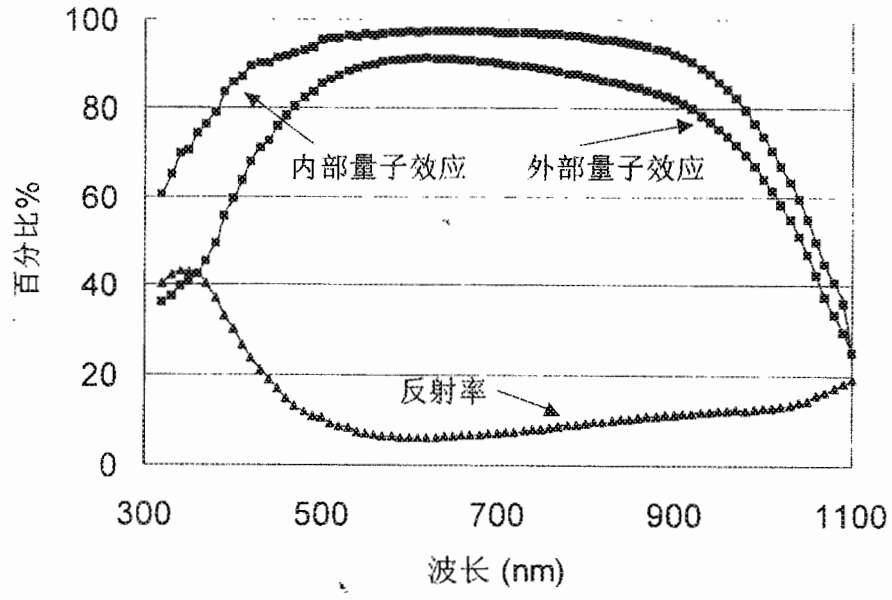


图 4

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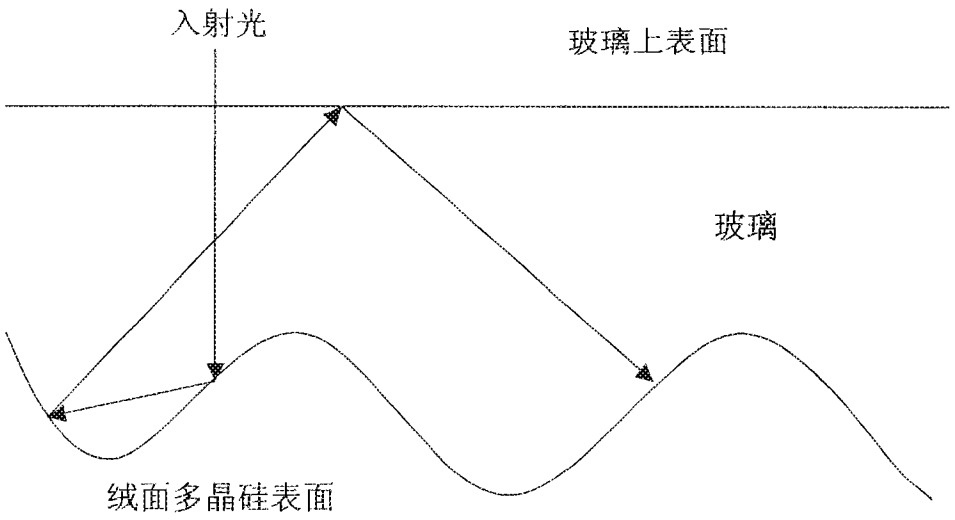


图 5

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Espacenet

Bibliographic data: CN201725796 (U) — 2011-01-26

CMOS image sensor with back illumination

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Applicant(s): GALAXYCORE INC ± (GALAXYCORE INC)

Classification: **- international:** ***H01L27/146***
- cooperative:

Application number: CN20102222129U 20100601

Priority number(s): CN20102222129U 20100601

Abstract of CN201725796 (U)

The utility model provides a CMOS image sensor with back illumination. The image sensor comprises: a semiconductor substrate that is provided with a first surface and a second surface opposite to the first surface and comprises at least one pixel unit area, and an isolation structure between adjacent pixel unit areas, wherein the isolation structure is deep trench isolation structure that penetrates through the first surface and the second surface of the semiconductor substrate. The CMOS image sensor reduces the crosstalk of electric signals between adjacent pixel unit areas, improves the display fading of CMOS image sensors and enhances imaging quality.

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DESCRIPTION CN201725796

The utility model provides a back-illuminated CMOS image sensor, comprising: a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto; the semiconductor substrate comprising at least one pixel unit area; an isolation structure, Located between adjacent pixel cell regions; wherein the isolation structure is a deep trench isolation structure that penetrates the first surface and the second surface of the semiconductor substrate. The utility model reduces the crosstalk of electrical signals between adjacent pixel unit regions, improves the display fading of the CMOS image sensor, and improves the imaging quality.

Backlighting CMOS image sensor

Technical field

The utility model relates to an image sensor, in particular to a CMOS image sensor with backlighting.

Background technique

The image sensor is an important part of the digital camera. According to the different components, the image sensor is divided into a Charge Coupled Device (CCD) image sensor and a Metal Oxide Semiconductor (CMOS) image sensor. Among them, due to the high integration of CMOS image sensors, it is easy to be compatible with standard CMOS fabrication processes, and the power consumption is low. With the improvement of CMOS fabrication processes, CMOS image sensors have become the mainstream technology of current image sensors.

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An existing CMOS image sensor is disclosed in Chinese Patent Application No. 200710148796.5. Existing CMOS image sensors include a semiconductor substrate, which typically includes a plurality of pixel cell regions arranged in a matrix with shallow trench isolation structures (STIs) between adjacent pixel cell regions. Please refer to FIG. 1. FIG. 1 is a schematic structural diagram of a conventional CMOS image sensor. The CMOS image sensor includes a semiconductor substrate 100. The semiconductor substrate 100 includes several pixel unit regions 103. In the figure, there are two pixel unit regions. 103 is described as an example; there is a shallow trench isolation structure 106 between adjacent pixel cell regions 103 . The pixel unit area 103 is used to form a pixel. The pixel unit area 103 generally includes a photodiode area 104 and a transistor area 105. The photodiode area 104 is used to form a photodiode, and the photodiode is used for photoelectric conversion. The transistor region 105 is used to form a transistor for amplifying and outputting an electrical signal converted by a photodiode. The shallow trench isolation structure 106 is used for isolation of adjacent pixels. The semiconductor substrate 100 includes a first surface 101 and a second surface 102 opposite thereto. Light enters the pixel unit area 103 from the second surface 102 . Those skilled in the art refer to the CMOS image sensor as a Backside illuminated CMOS image sensor.

In practice, it has been found that the above-mentioned back-illuminated CMOS image sensor has a problem of fading, which affects the image quality.

Therefore, there is a need for a back-illuminated CMOS image sensor that can improve the display fading problem and improve the image quality of the CMOS image sensor.

Utility model content

The utility model solves the problem that the invention provides a backlight CMOS image sensor, which can improve the display fading problem and improve the imaging quality of the CMOS image sensor.

To solve the above problems, the present invention provides a backlit CMOS image sensor including:

a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto;

The semiconductor substrate includes at least one pixel unit area;

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The isolation structure is located between adjacent pixel unit regions;

Wherein, the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate.

Optionally, the width of the deep trench isolation structure is less than or equal to 0.25 micrometers.

Optionally, the depth of the deep trench isolation structure ranges from 1.5 to 4 microns.

Optionally, the filler in the deep trench isolation structure is a dielectric.

Optionally, the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate.

Optionally, the semiconductor substrate is sequentially formed with a filter and a microlens, and the filter and the microlens are located on the second surface of the semiconductor substrate.

Compared with the prior art, the utility model has the following advantages:

By providing a deep trench isolation structure penetrating the first surface and the second surface of the semiconductor substrate between adjacent pixel cell regions, isolation between adjacent pixels is performed, thereby preventing the photocarriers in the pixel cell region from diffusing to The adjacent pixel unit area reduces the crosstalk caused by electrical signals to the adjacent pixel unit area, improves the display fade of the CMOS image sensor, and improves the imaging quality.

Further, the filler in the deep trench isolation structure is a dielectric, and the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate, and the light totally reflects at the interface between the deep trench isolation structure and the semiconductor substrate. The light is prevented from entering the adjacent pixel unit area through the deep trench isolation structure, the crosstalk to the optical signal of the adjacent pixel unit area is reduced, the display fading of the CMOS image sensor is further improved, and

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the imaging quality is improved; The dielectric material of the trench isolation structure is silicon oxide, which has a different color from the silicon of the semiconductor substrate. In the process of forming a filter and a microlens by a photolithography process, the deep trench isolation structure can be used as an alignment mark for lithography. No special alignment layer is required, saving process steps and reducing production costs.

Description of the drawings

FIG. 1 is a schematic structural diagram of a prior art CMOS image sensor.

FIG. 2 is a schematic structural diagram of a CMOS image sensor according to an embodiment of the present invention.

FIG. 3 is a schematic diagram illustrating the principle of total reflection formed at the interface between the deep trench isolation structure and the semiconductor substrate.

detailed description

Existing Backside illuminated CMOS image sensors have problems with display fading. The inventor's research found that the cause of fading is crosstalk of neighboring pixels. One of the reasons for the crosstalk is that the existing shallow trench isolation structure cannot effectively isolate the photocarrier diffusion between adjacent pixel units. Since the incident light of the CMOS image sensor using the backlight illuminates the pixel cell region of the semiconductor substrate through the microlens and the filter, in the prior art, in order to increase the effective photosensitive area of the photodiode in the pixel unit region, the depth of the photodiode is usually higher. Large, its depth can reach more than 10000 angstroms, while the depth of the existing shallow trench isolation structure is usually 2000-5000 angstroms. In the photoelectric conversion, the photo-generated carriers generated by photoelectric conversion of the photodiode may be diffused, and the existing shallow trench isolation structure cannot effectively isolate the photo-generated carriers so that the photo-generated carriers may go to adjacent pixels. Crosstalk of electrical signals is caused to adjacent pixels, causing the display of the CMOS image sensor to fade.

The back-illuminated CMOS image sensor provided by the present invention solves the crosstalk of electrical signals and improves the display fading problem of the CMOS image sensor. The back-illuminated CMOS image sensor includes:

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a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto;

The semiconductor substrate includes at least one pixel unit area;

The isolation structure is located between adjacent pixel unit regions;

Wherein, the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate.

The technical solutions of the present invention will be described in detail below in conjunction with specific embodiments. Please refer to FIG. 2 . FIG. 2 is a schematic structural diagram of a CMOS image sensor according to an embodiment of the present invention.

The CMOS image sensor includes a semiconductor substrate 200 whose material may be silicon, SOI, gallium nitride, or gallium arsenide. The semiconductor substrate 200 has a first surface 201 and a second surface 202 opposite thereto. In the present embodiment, the semiconductor substrate 200 is a silicon substrate having a P-type conductivity type.

As shown in FIG. 2, the semiconductor substrate 200 includes at least one pixel unit area 203. For convenience of description, the two pixel unit area 203 will be described as an example. There is a deep trench isolation structure 206 between adjacent pixel cell regions 203 . The deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200 . The pixel unit region 203 of the semiconductor substrate 200 is formed with a filter 209 and micro lenses 210 . In this embodiment, the refractive index of the micro lens 210 is in the range of 1.2 to 4, and its material may be silicon nitride SiNX, zirconium oxide ZrO2, hafnium oxide HfO2, titanium oxide TiO2, aluminum oxide Al3O2, zinc oxide ZnO2, etc. The range of the refractive index of the filter 209 is 1.4 to 2. The material of the filter 209 may be a photoresist material. The filter 209 and the micro lens 210 are formed through a photolithography process. During the photolithography process for forming the filter, the deep trench isolation structure 206 can be used as an alignment mark for photolithography.

Still referring to FIG. 2, the pixel cell area 203 is used to form a pixel. The pixel cell region 203 includes a photodiode region 204 and a transistor region 205 . The photodiode region 204 is used to form a photodiode,

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which is used for photoelectric conversion and converts an optical signal incident from the second surface 202 into a corresponding electrical signal to generate photogenerated carriers. The transistor region 205 is used to form a transistor for amplifying and outputting the electrical signal converted by the photodiode. According to actual conditions, the transistor region 205 includes three or more transistors, and the transistors have a shallow trench isolation structure therebetween, and the transistors in the pixel are isolated from each other. The depth of the shallow trench isolation structure ranges from 2000 to 5000 Angstroms.

In this embodiment, the deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200 . As an embodiment, the thickness of the semiconductor substrate 200 ranges from 1.5 to 4 microns. The thickness of the deep trench isolation structure 206 should be the same as the depth of the semiconductor substrate 200, that is, 1.5 to 4 microns. As a preferred embodiment, the thickness of the semiconductor substrate 200 is 2 33 μ m so that the photodiodes in the pixel unit region 203 can better absorb incident light, and accordingly, the deep trench isolation structure 206 is The depth is preferably in the range of 2 to 3 microns. Since the deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200, the deep trench isolation structure 206 can effectively prevent the photo-generated light generated by the photodiode of the pixel during photoelectric conversion. The flow diffuses to adjacent pixels, reduces the crosstalk of electrical signals to adjacent pixels, improves the pixel fading of the CMOS image sensor, and improves the imaging quality of the CMOS image sensor.

The width of the deep trench isolation structure 206 is less than or equal to the width of the prior art shallow trench isolation structure to save chip area. As an embodiment, the width of the deep trench isolation structure 206 is 0.25 micrometers or less.

The filler in the deep trench isolation structure 206 is a dielectric whose refractive index is less than 0.8 times the refractive index of the semiconductor substrate. In this way, when the incident light enters the pixel unit area 203, total reflection is formed at the interface between the deep trench isolation structure 203 and the semiconductor substrate 200, so that incident light is prevented from entering the adjacent pixel unit area 203 through the deep trench isolation structure 206, and adjacent pixel units are The area 203 causes crosstalk of the optical signal, further improving the display fading problem of the CMOS image sensor. In order to facilitate the description of the principle that the light forms a total reflection at the interface between the deep trench isolation structure and the semiconductor substrate, a partial region 300 of the CMOS image sensor in FIG. 2 is enlarged and illustrated. The partial region 300 includes a pixel unit region 203, a corresponding filter 209, a microlens 210, and a deep trench isolation structure 206 on both sides of the pixel unit region 203. Please refer to FIG. 3 , which is a schematic diagram illustrating the principle of total reflection of light at the interface between the deep trench isolation structure and the semiconductor substrate.

As shown in FIG. 3, the light A enters the pixel unit area 203 from the air through the micro lens 210, the filter

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209, and the second surface 202 of the semiconductor substrate 200. Ideally, the light A is the photodiode of the pixel unit area 203. Absorption, however, may allow light to enter the interface of the deep trench isolation structure 206 and the semiconductor substrate 200 because the light A may have a certain tilt angle. Due to the difference in refractive index between the air, the micro lens 210, the filter 209, and the semiconductor substrate 200, the light rays A reach the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 to refract light a plurality of times. Specifically, the normal line between the micro lens 210 and the air interface is O1, the angle between the light line A in the air and the normal line O1 is a1, and after the refraction, the angle between the light line A and the normal line O1 in the micro lens 210 is refracted. For a2, the light A is transmitted to the interface between the microlens 210 and the filter 209 in the micro lens 210. The normal of the interface between the micro lens 210 and the filter 209 is O2. The light A and the light in the micro lens 210 are The included angle of the normal line O2 is a3. After refraction, the angle between the light A in the filter 209 and the normal line O2 is aa4; the light A is transmitted to the filter 209 and the semiconductor liner in the filter 209. The interface of the bottom 200, the normal of the interface between the filter 209 and the semiconductor substrate 200 is O3, and the angle between the light A and the normal O3 in the filter 209 is a5, and after being refracted, The angle a6 between the light A and the normal O3 in the semiconductor substrate 200; within the semiconductor substrate 200, the light A is transmitted to the interface between the semiconductor substrate 200 and the deep trench isolation structure 206. The normal to the interface between the 200 and the deep trench isolation structure 206 is O4, and the angle between the light A and the normal O4 in the semiconductor substrate 200 is β. In this embodiment, the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 is perpendicular to the interface between the filter 209 and the semiconductor substrate 200. Therefore, the normal line O4 is perpendicular to the normal line O3, and thus, the angle β and the angle a6. Mutual corner.

Since in practice, the thickness of the micro lens 210 and the thickness of the filter 209 are optimally set by those skilled in the art, it is possible to make the angle a6 the same as the angle a1. The maximum value of the angle a1 is called the chief ray angle (CRA), and the angle of the chief ray inclination angle ranges from 0 to 35°. Therefore, the angle α 6 of the angle of inclination is in the range of 0-35°, and the angle β of the angle β of the angle a6 is in the range of 55-90°, that is, the range of the incident angle of the light ray and the normal O4 is 55-90°. Therefore, assuming that the total reflection critical angle is α, if the light is to be totally reflected at the interface between the semiconductor substrate 200 and the deep trench isolation structure 206, α should be smaller than 55° to ensure the incident angle range between the light and the normal O4. At 55 to 90°, any incident angle is larger than α, and total reflection can be formed when the incident angle of the light and the normal O4 is 55 to 90°. Assuming that the total reflection critical angle is 55°, the refractive index of the semiconductor substrate 200 is x, and the refractive index of the dielectric filled in the deep trench isolation structure 206 is y, then according to the total reflection calculation formula: sin55° /sin90° =y/ x

y=sin55° *x=0.8*x

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According to the above analysis, when the total reflection critical angle is 55° , the refractive index of the dielectric filled in the corresponding deep trench isolation structure 206 is 0.8 times the refractive index of the semiconductor substrate 200 .

Since the critical angle α of the total reflection depends on the refractive index of the semiconductor substrate 200 and the refractive index of the filled dielectric in the deep trench isolation structure 206 . Specifically, in the case where the refractive index of the semiconductor substrate 200 is constant, the smaller the refractive index of the dielectric filled in the deep trench isolation structure 206 is, the smaller the critical angle α of the total reflection is. From the foregoing analysis, it can be seen that when the critical angle of total reflection is 55° , the refractive index of the dielectric in the corresponding deep trench isolation result 206 is 0.8 times the refractive index of the semiconductor substrate 200 . To make the total reflection critical angle less than 55° , the refractive index of the dielectric filled in the deep trench isolation structure 206 should be less than 0.8 times the refractive index of the semiconductor substrate 200 to ensure the light A in the deep trench isolation structure 206 and the semiconductor liner The total reflection occurs at the interface of the bottom 200. Therefore, the light A stays in the pixel unit area 203 , so as to prevent crosstalk caused by the light A through the deep trench isolation structure 206 to the adjacent pixel unit area, and further improve the display fading phenomenon of the existing CMOS image sensor.

As an embodiment, when the material of the semiconductor substrate 200 is silicon, the filler of the deep trench isolation structure 206 may be silicon oxide, and the silicon oxide may have a refractive index less than or equal to 0.8 of the refractive index of silicon. Times. In this embodiment, the refractive index of silicon is 3.46, and the refractive index of silicon oxide is 1.46, so that the incident light can form total reflection at the interface between the deep trench isolation structure 206 and the semiconductor substrate 200. Alternatively, under the condition that the refractive index of the dielectric filled in the deep trench isolation structure 206 is less than or equal to 0.8 times the refractive index of the silicon substrate, the dielectric filled in the deep trench isolation structure 206 may be other materials. When the material of the semiconductor substrate 200 is other semiconductor material, the material of the dielectric filled in the deep trench isolation structure 206 may also be other materials, but the dielectric filled in the deep trench isolation structure 206 should have a smaller refractive index than the semiconductor substrate. 200 is 0.8 times the refractive index to ensure that total reflection is formed at the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 .

To sum up, the present invention provides a back-illuminated CMOS image sensor having a deep trench isolation structure between pixel cell regions of the back-illuminated CMOS image sensor. The deep trench isolation structure penetrates the semiconductor liner. The first surface of the bottom and the second surface opposite thereto effectively isolate the adjacent pixels, avoid crosstalk of electrical signals of adjacent pixels, improve the display fading problem of the CMOS image sensor, and improve the imaging quality. Further, the deep trench isolation structure is internally filled with a dielectric, the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate, and the light forms a total reflection at the interface

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between the deep trench isolation structure and the semiconductor substrate, avoiding Light enters adjacent pixels, causing crosstalk of optical signals to adjacent pixels, which further improves the display fading problem of CMOS image sensors and improves the imaging quality. At the same time, in the photolithography process for forming the filter and the microlens, the deep trench isolation structure can serve as a mark for photolithography alignment, reducing the number of process steps.

Although the utility model is disclosed as the preferred embodiment as above, it is not intended to limit the utility model. Any person skilled in the art can make possible changes and modifications without departing from the spirit and scope of the utility model. Therefore, the protection scope of the present invention should be based on the scope defined by the claims of the present invention.

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CLAIMS CN201725796

1.
A backside illuminated CMOS image sensor, comprising: a semiconductor substrate having a first surface and a second surface opposite thereto; the semiconductor substrate including at least one pixel cell region; an isolation structure at a phase The adjacent pixel unit region is characterized in that the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate.

2.
The backlight-powered CMOS image sensor according to claim 1, wherein the width of the deep trench isolation structure is less than or equal to 0.25 micrometers.

3.
The backlit CMOS image sensor according to claim 1, wherein the deep trench isolation structure has a depth in the range of 1.5 to 4 microns.

4.
The backlit CMOS image sensor according to claim 1, wherein the filler in the deep trench isolation structure is a dielectric.

5.
The backlit CMOS image sensor according to claim 4, wherein the refractive index of the dielectric is less than 0.8

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times the refractive index of the semiconductor substrate.

6.

The backlight-source CMOS image sensor according to claim 1, wherein the semiconductor substrate is formed with a filter and a microlens in this order, and the filter and the microlens are located on the semiconductor substrate. Two surfaces.

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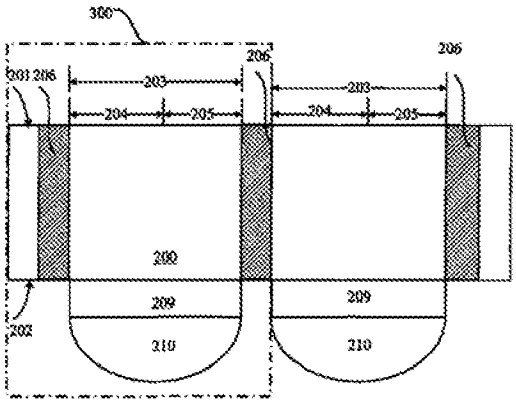
权利要求书 1 页 说明书 5 页 附图 2 页

(54)实用新型名称

背面照光的 CMOS 图像传感器

(57)摘要

本实用新型提供背面照光的 CMOS 图像传感器，包括：半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；所述半导体衬底包括至少一个像素单元区域；隔离结构，位于相邻像素单元区域之间；其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。本实用新型减少了相邻像素单元区域之间的电信号的串扰，改善了 CMOS 图像传感器的显示颜色，提高了成像质量。



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1. 一种背面照光的 CMOS 图像传感器，包括：

半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

所述半导体衬底包括至少一个像素单元区域；

隔离结构，位于相邻像素单元区域之间；

其特征在于，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。

2. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

3. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

4. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构内填充物为电介质。

5. 如权利要求 4 所述的背面照光的 CMOS 图像传感器，其特征在于，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

6. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述半导体衬底的依次形成有滤光片和微透镜，所述滤光片和微透镜位于所述半导体衬底的第二表面。

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背面照光的 CMOS 图像传感器

技术领域

[0001] 本实用新型涉及图像传感器，特别涉及背面照光的 CMOS 图像传感器。

背景技术

[0002] 图像传感器是组成数字摄像头的重要组成部分，根据元件不同分为电荷耦合 (CCD, Charge Coupled Device) 图像传感器和金属氧化物半导体 (CMOS, Complementary Metal-Oxide Semiconductor) 图像传感器。其中，由于 CMOS 图像传感器集成度高，容易与标准的 CMOS 制作工艺兼容，并且功耗低，随着 CMOS 制作工艺的改进，CMOS 图像传感器成为目前图像传感器的主流技术。

[0003] 在申请号为 200710148796.5 的中国专利申请中公开了一种现有的 CMOS 图像传感器。现有的 CMOS 图像传感器包括半导体衬底，所述半导体衬底通常包括若干呈矩阵排布的像素单元区域，相邻的像素单元区域之间具有浅沟槽隔离结构 (STI)。请参考图 1，图 1 是现有的 CMOS 图像传感器结构示意图，所述 CMOS 图像传感器包括：半导体衬底 100，所述半导体衬底 100 包括若干像素单元区域 103，图中以 2 个像素单元区域 103 为例进行说明；相邻像素单元区域 103 之间具有浅沟槽隔离结构 106。其中所述像素单元区域 103 用于形成像素，通常所述像素单元区域 103 包括光电二极管区域 104 和晶体管区域 105，所述光电二极管区域 104 用于形成光电二极管，所述光电二极管用于光电转换；所述晶体管区域 105 用于形成晶体管，所述晶体管用于将光电二极管转换的电信号放大后输出。所述浅沟槽隔离结构 106 用于相邻像素的隔离。所述半导体衬底 100 包括第一表面 101 和与之相对的第二表面 102。光线从第二表面 102 进入像素单元区域 103 内。本领域技术人员将所述 CMOS 图像传感器称为背面照光的 (Backside illuminated)CMOS 图像传感器。

[0004] 在实际中发现，上述背面照光的 CMOS 图像传感器具有显示褪色的问题，影响了成像质量。

[0005] 因此，需要一种背面照光的 CMOS 图像传感器，能够改善显示褪色的问题，提高 CMOS 图像传感器的成像质量。

实用新型内容

[0006] 本实用新型解决的问题是提供了一种背面照光的 CMOS 图像传感器，能够改善显示褪色的问题，提高 CMOS 图像传感器的成像质量。

[0007] 为解决上述问题，本实用新型提供一种背面照光的 CMOS 图像传感器，包括：

[0008] 半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

[0009] 所述半导体衬底包括至少一个像素单元区域；

[0010] 隔离结构，位于相邻像素单元区域之间；

[0011] 其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。

[0012] 可选的，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

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[0013] 可选的，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

[0014] 可选的，所述深沟槽隔离结构内填充物为电介质。

[0015] 可选的，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

[0016] 可选的，所述半导体衬底的依次形成有滤光片和微透镜，所述滤光片和微透镜位于所述半导体衬底的第二表面。

[0017] 与现有技术相比，本实用新型具有以下优点：

[0018] 通过在相邻像素单元区域之间设置贯穿半导体衬底的第一表面和第二表面的深沟槽隔离结构，进行相邻像素间的隔离，避免了像素单元区域内的光生载流子扩散至相邻像素单元区域，减少对相邻像素单元区域造成电信号的串扰，改善了 CMOS 图像传感器的显示褪色，提高了成像质量。

[0019] 进一步地，所述深沟槽隔离结构内的填充物为电介质，所述电介质的折射率小于半导体衬底折射率的 0.8 倍，光线在深沟槽隔离结构和半导体衬底的界面形成全反射，避免光线经深沟槽隔离结构进入相邻的像素单元区域，减小了对相邻像素单元区域的光信号的串扰，进一步改善了 CMOS 图像传感器的显示褪色，提高了成像质量；所述深沟槽隔离结构填充电介质为氧化硅，与半导体衬底的硅具有不同的颜色，在进行光刻工艺形成滤光片和微透镜的过程中，深沟槽隔离结构可以作为光刻的对准标记，无需专门的对准层，节省了工艺步骤，降低了生产成本。

附图说明

[0020] 图 1 是现有技术 CMOS 图像传感器结构示意图。

[0021] 图 2 是本实用新型的一个实施例的 CMOS 图像传感器结构示意图。

[0022] 图 3 是光线在深沟槽隔离结构与半导体衬底界面形成全反射原理示意图。

具体实施方式

[0023] 现有的背面照光的 (Backside illuminated)CMOS 图像传感器存在显示褪色的问题。经发明人研究发现，褪色的原因是相邻像素的串扰 (crosstalk)。所述串扰的原因之一是现有的浅沟槽隔离结构无法有效隔离相邻的像素单元之间光生载流子扩散。由于采用背面照光的 CMOS 图像传感器的入射光线经过微透镜和滤光片进入半导体衬底的像素单元区域，现有技术为了提高像素单元区域内的光电二极管的有效感光面积，通常光电二极管的深度较大，其深度可达 10000 埃以上，而现有的浅沟槽隔离结构的深度范围通常为 2000 ～ 5000 埃。在进行光电转换时，所述光电二极管光电转换所产生的光生载流子可能扩散，而现有的浅沟槽隔离结构无法有效隔离光生载流子，从而光生载流子可能至相邻像素，对相邻像素造成电信号的串扰，从而导致 CMOS 图像传感器的显示褪色。

[0024] 本实用新型提供的背面照光的 CMOS 图像传感器解决了电信号的串扰，改善了 CMOS 图像传感器的显示褪色问题，所述背面照光的 CMOS 图像传感器包括：

[0025] 半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

[0026] 所述半导体衬底包括至少一个像素单元区域；

[0027] 隔离结构，位于相邻像素单元区域之间；

[0028] 其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬

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底的第一表面和第二表面。

[0029] 下面将结合具体的实施例对本实用新型的技术方案进行详细的说明。请参考图2，图2是本实用新型一个实施例的CMOS图像传感器结构示意图。

[0030] 所述CMOS图像传感器包括半导体衬底200，所述半导体衬底200的材料可以是硅、SOI、氮化镓或者砷化镓。所述半导体衬底200具有第一表面201和与之相对的第二表面202。本实施例中，所述半导体衬底200为具有P型导电类型的硅衬底。

[0031] 如图2，所述半导体衬底200包括至少一个像素单元区域203，为了便于说明，以2个像素单元区域203为例进行说明。相邻的像素单元区域203之间具有深沟槽隔离结构206。所述深沟槽隔离结构206贯穿所述半导体衬底200的第一表面201和第二表面202。半导体衬底200的像素单元区域203形成有滤光片209和微透镜210。本实施例中，所述微透镜210的折射率范围为1.2～4，其材质可以为氮化硅SiN_x、氧化锆ZrO_2、氧化铪HfO_2、氧化钛TiO_2、氧化铝Al_2O_3、氧化锌ZnO_2等，所述滤光片209的折射率范围为1.4～2，其材质可以为光阻材料。所述滤光片209和微透镜210通过光刻工艺形成，在形成滤光片的光刻工艺过程中，深沟槽隔离结构206可以作为光刻的对准标记使用。

[0032] 仍参考图2，所述像素单元区域203用于形成像素。所述像素单元区域203包括光电二极管区域204和晶体管区域205。所述光电二极管区域204用于形成光电二极管，所述光电二极管用于进行光电转换，将从第二表面202入射的光信号转换为相应的电信号，产生光生载流子。所述晶体管区域205用于形成晶体管，所述晶体管用于将所述光电二极管转换的电信号放大、输出。根据实际情况，所述晶体管区域205内包括3个或3个以上晶体管，所述晶体管之间具有浅沟槽隔离结构，用于像素内的晶体管之间相互隔离。所述浅沟槽隔离结构的深度范围为2000～5000埃。

[0033] 本实施例中，所述深沟槽隔离结构206贯穿所述半导体衬底200的第一表面201和第二表面202。作为一个实施例，所述半导体衬底200的厚度范围为1.5～4微米，所述深沟槽隔离结构206的厚度应与所述半导体衬底200的深度相同，即为1.5～4微米。作为优选的实施例，所述半导体衬底200的厚度为2～3微米，以使得像素单元区域203内的光电二极管能更好的吸收入射光线，相应地，所述深沟槽隔离结构206的深度范围优选为2～3微米。由于所述深沟槽隔离结构206贯穿所述半导体衬底200的第一表面201和第二表面202，因此，深沟槽隔离结构206可以有效阻止像素的光电二极管在光电转换时产生的光生载流子扩散至相邻像素，减少对相邻像素的电信号的串扰，改善CMOS图像传感器的像素褪色，提高了CMOS图像传感器的成像质量。

[0034] 所述深沟槽隔离结构206的宽度小于或等于现有技术的浅沟槽隔离结构的宽度，以节约芯片面积。作为一个实施例，所述深沟槽隔离结构206的宽度范围为小于等于0.25微米。

[0035] 所述深沟槽隔离结构206内填充物为电介质，所述电介质的折射率小所述半导体衬底的折射率的0.8倍。这样入射光线进入像素单元区域203时在深沟槽隔离结构203与半导体衬底200的界面形成全反射，避免入射光线经过深沟槽隔离结构206进入相邻像素单元区域203，对相邻像素单元区域203造成光信号的串扰，进一步改善CMOS图像传感器的显示褪色的问题。为了便于说明光线在深沟槽隔离结构和半导体衬底的界面形成全反射的原理，对图2中CMOS图像传感器的部分区域300进行放大说明。所述部分区域300包括像

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素单元区域 203、与之对应的滤光片 209、微透镜 210、以及像素单元区域 203 两侧的深沟槽隔离结构 206。请参考图 3，图 3 是光线在深沟槽隔离结构与半导体衬底界面形成全反射原理示意图。

[0036] 如图 3 所示，光线 A 自空气经过微透镜 210、滤光片 209、半导体衬底 200 的第二表面 202 进入像素单元区域 203，理想的状况是，光线 A 被像素单元区域 203 的光电二极管吸收，但是，由于光线 A 可能具有一定倾斜角因此光线可能会入射深沟槽隔离结构 206 与半导体衬底 200 的界面。由于通常空气、微透镜 210、滤光片 209、半导体衬底 200 的材质不同而折射率不同，光线 A 到达深沟槽隔离结构 206 与半导体衬底 200 的界面发生多次光的折射。具体地，在微透镜 210 和空气界面的法线为 01，在空气中光线 A 与所述法线 01 的夹角为 a1，经过折射，在微透镜 210 内光线 A 与法线 01 的夹角为 a2；光线 A 在微透镜 210 内传输至微透镜 210 和滤光片 209 的界面，所述微透镜 210 和滤光片 209 的界面的法线为 02，在微透镜 210 内光线 A 与所述法线 02 的夹角为 a3，经过折射，在滤光片 209 内光线 A 与所述法线 02 的夹角为 aa4；光线 A 在滤光片 209 内传输至滤光片 209 与半导体衬底 200 的界面，所述滤光片 209 与半导体衬底 200 的界面的法线为 03，在滤光片 209 内所述光线 A 与所述法线 03 的夹角为 a5，经过折射，在半导体衬底 200 内光线 A 与法线 03 的夹角 a6；在半导体衬底 200 内，所述光线 A 传输至半导体衬底 200 与所述深沟槽隔离结构 206 的界面，所述半导体衬底 200 与所述深沟槽隔离结构 206 的界面的法线为 04，在半导体衬底 200 内光线 A 与法线 04 的夹角为 β。本实施例中，深沟槽隔离结构 206 与半导体衬底 200 的界面垂直于滤光片 209 与半导体衬底 200 的界面，因此，法线 04 与法线 03 垂直，从而，角度 β 与角度 a6 互为余角。

[0037] 由于在实际中，本领域技术人员对微透镜 210 的厚度、滤光片 209 的厚度进行优化设置，可以使得使得角度 a6 与角度 a1 相同。角度 a1 的最大值称为主光线倾斜角 (chief ray angle，CRA)，而主光线倾斜角的角度范围为 0 ～ 35°。因此，角度 a6 倾斜角度范围为 0 ～ 35°，角度 a6 的余角 β 的角度范围为 55 ～ 90°，即光线与法线 04 的入射角范围为 55 ～ 90°。因此，假设全反射临界角为 α，若要光线在半导体衬底 200 与深沟槽隔离结构 206 的界面形成全反射，α 应小于为 55°，以保证在光线与法线 04 的入射角范围为 55 ～ 90° 时，任一入射角均大于 α，从而光线与法线 04 的入射角为 55 ～ 90° 时可以形成全反射。假设全反射临界角为 55°，半导体衬底 200 的折射率为 x，深沟槽隔离结构 206 内填充的电介质的折射率为 y，则根据全反射计算公式：sin55° /sin90° = y/x

[0038] y = sin55° *x = 0.8*x

[0039] 由上述分析可知，当全反射临界角为 55° 时，对应的深沟槽隔离结构 206 内填充的电介质的折射率为半导体衬底 200 的折射率的 0.8 倍。

[0040] 由于全反射的临界角 α 取决于半导体衬底 200 的折射率和深沟槽隔离结构 206 内填充电介质的折射率关系。具体地，在半导体衬底 200 的折射率一定的情况下，深沟槽隔离结构 206 内填充的电介质的折射率越小，全反射的临界角 α 越小。由前面的分析可知，在全反射的临界角为 55° 时对应的深沟槽隔离结果 206 内的电介质的折射率为半导体衬底 200 折射率的 0.8 倍。若要使得全反射临界角小于 55°，深沟槽隔离结构 206 内填充的电介质的折射率应小于半导体衬底 200 折射率的 0.8 倍，以保证光线 A 在深沟槽隔离结构 206 和半导体衬底 200 的界面发生全反射。从而，光线 A 留在像素单元区域 203 内，避免光

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线 A 经过深沟槽隔离结构 206 对相邻像素单元区域造成串扰，进一步改善现有的 CMOS 图像传感器的显示褪色现象。

[0041] 作为一个实施例，所述半导体衬底 200 的材质为硅时，所述深沟槽隔离结构 206 的填充物可以为氧化硅，并且所述氧化硅的折射率可以小于等于硅的折射率的 0.8 倍。本实施例中，硅的折射率为 3.46，氧化硅的折射率为 1.46，这样入射光线在深沟槽隔离结构 206 和半导体衬底 200 的界面可以形成全反射。可替代地，在深沟槽隔离结构 206 内填充的电介质的折射率小于等于硅衬底的折射率的 0.8 倍前提下，深沟槽隔离结构 206 内填充的电介质可以为其他材质。当半导体衬底 200 的材质为其他半导体材料时，深沟槽隔离结构 206 内填充的电介质的材质还可以为其他材质，但是深沟槽隔离结构 206 内填充的电介质的折射率应小于半导体衬底 200 折射率的 0.8 倍，以保证在深沟槽隔离结构 206 和半导体衬底 200 的界面形成全反射。

[0042] 综上，本实用新型提供了一种背面照光的 CMOS 图像传感器，所述背面照光的 CMOS 图像传感器的像素单元区域之间具有深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和与之相对的第二表面，从而有效隔离相邻像素，避免了相邻像素电信号的串扰，改善了 CMOS 图像传感器的显示褪色问题，提高了成像质量。进一步地，所述深沟槽隔离结构内部填充电介质，所述电介质的折射率小于半导体衬底的折射率的 0.8 倍，光线在深沟槽隔离结构和半导体衬底的界面上形成全反射，避免光线进入相邻像素，对相邻像素造成光信号的串扰，更加改善了 CMOS 图像传感器的显示褪色问题，提高了成像质量。同时，在形成滤光片和微透镜的光刻工艺时，所述深沟槽隔离结构可以作为光刻对准的标记，减少了工艺步骤。

[0043] 本实用新型虽然以较佳实施例公开如上，但其并不是用来限定本实用新型，任何本领域技术人员在不脱离本实用新型的精神和范围内，都可以做出可能的变动和修改，因此本实用新型的保护范围应当以本实用新型权利要求所界定的范围为准。

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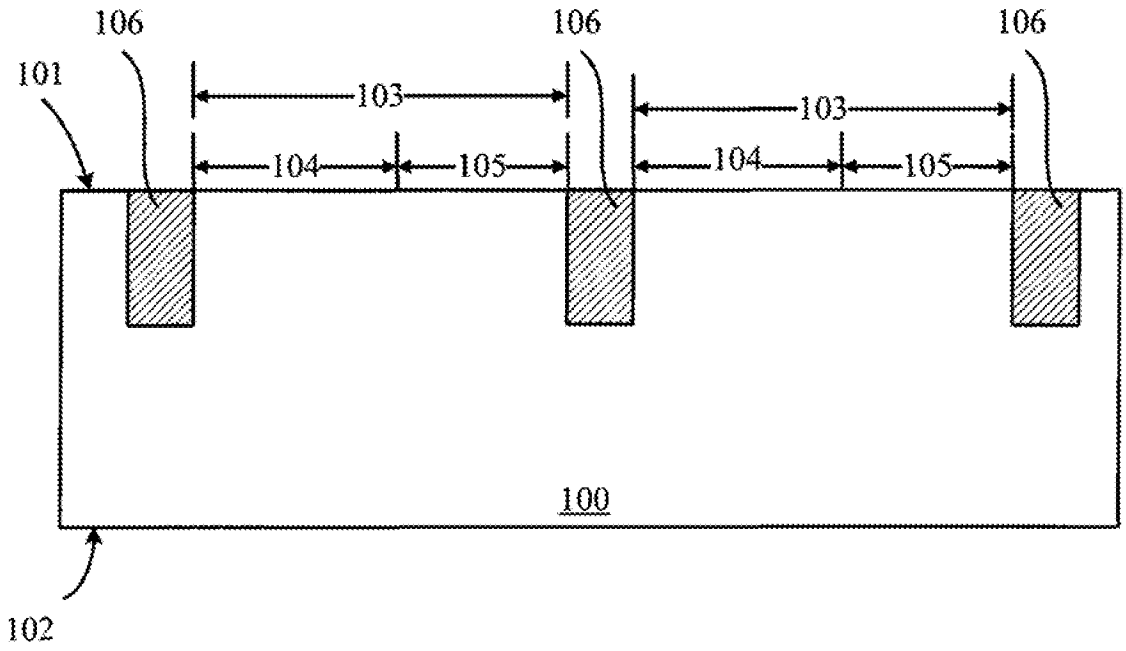


图 1

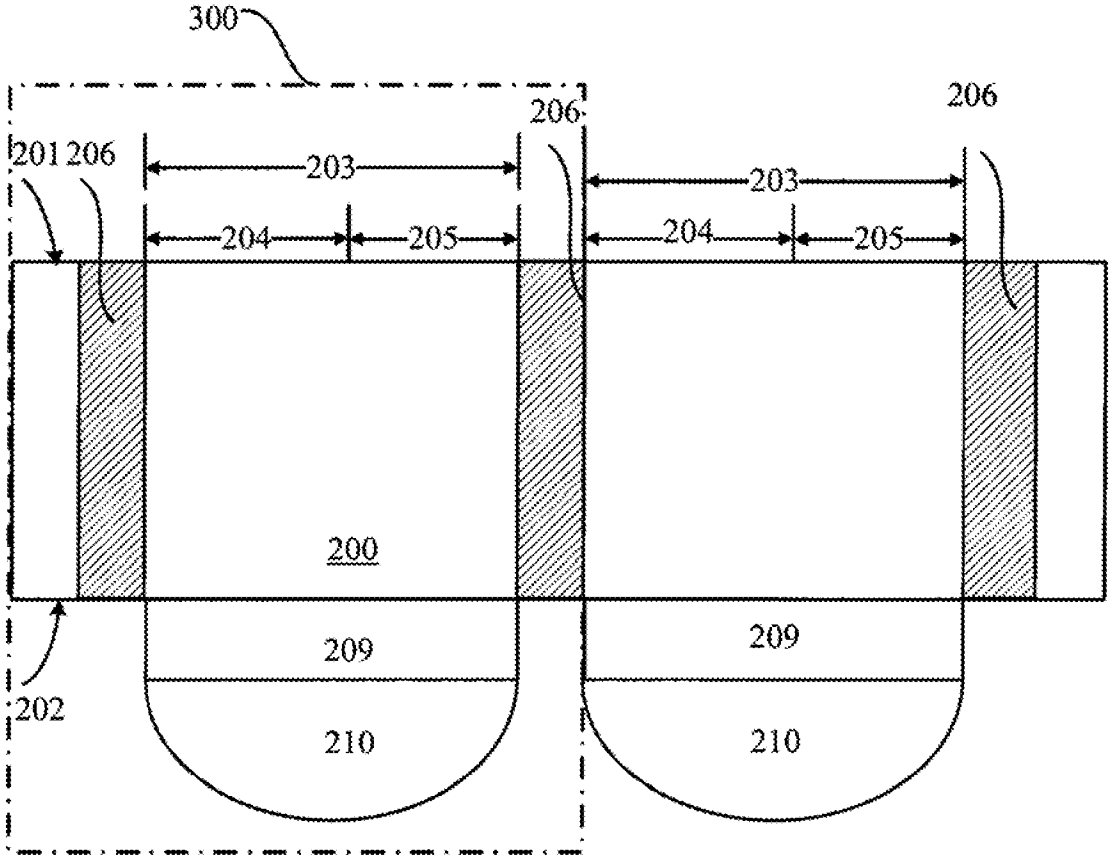


图 2

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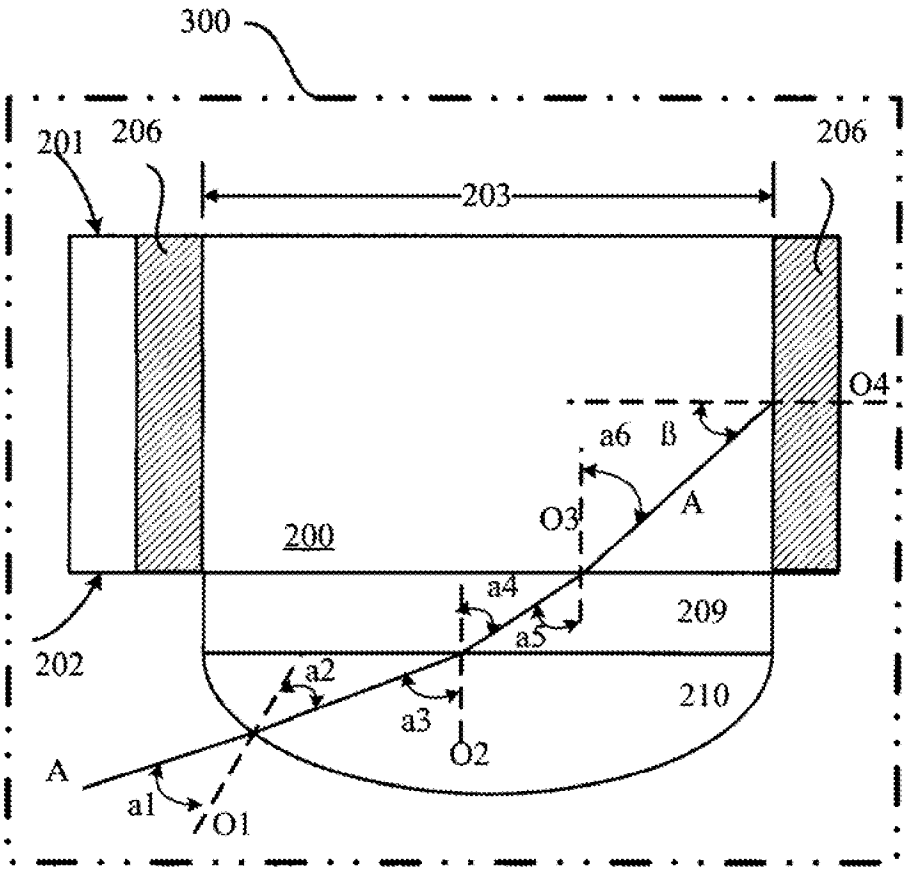


图 3

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