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SOLID STATE IMAGE SENSOR, MANUFACTURING METHOD THEREFOR, AND ELECTRONIC APPARATUS

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Abstract of JP2012169530 (A)

PROBLEM TO BE SOLVED: To enhance the image quality of a captured image.SOLUTION: A first light shielding part 313A is provided in a trench TR formed in a pixel separation part 301 of a semiconductor substrate 101. A second light shielding part 313B is provided on the upper surface of the first light shielding part 313A. The second light shielding part 313B is formed so that the center of the second light shielding part 313B is shifted more to the peripheral side of a pixel region PA than the center of the pixel separation part 301, on the periphery of the center of the pixel region PA. In other words, "pupil correction" is performed for at least the second light shielding part.

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DESCRIPTION JP2012169530

PROBLEM TO BE SOLVED: To improve image quality of captured images. A first light shielding portion 313 A is provided inside a trench TR formed in a pixel separation portion 301 of a semiconductor substrate 101. At the same time, the second light shielding portion 313B is provided on the upper surface side of the first light shielding portion 313A. Here, in order to shift the center of the second light shielding portion 313 </ b> B more toward the periphery of the pixel region PA than the center of the pixel separating portion 301 around the center of the pixel region PA, the second light shielding portion 313B are formed. That is, "pupil correction" is performed for at least the second light shielding portion. (FIG.

Solid-state imaging device, manufacturing method thereof, electronic device

[0001]
The present technology relates to a solid-state imaging device, a manufacturing method thereof, and an electronic apparatus.

[0002]

Electronic devices such as digital video cameras and digital still cameras include solid state imaging devices.

For example, a CMOS (Complementary Metal Oxide Semiconductor) type image sensor and a CCD (Charge Coupled Device) type image sensor are included as a solid-state imaging device.

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[0003]

In the solid-state imaging device, a plurality of pixels are arranged in a pixel region of a substrate. In each pixel, a photoelectric conversion unit is provided. The photoelectric conversion unit is, for example, a photodiode, and receives incident light on a light receiving surface and photoelectrically converts it to generate a signal charge.

[0004]

Among solid-state image pickup devices, a CCD image sensor has a vertical transfer portion provided between a plurality of pixel rows arranged in a vertical direction in a pixel region. In the vertical transfer section, a plurality of transfer electrodes are provided so as to face the vertical transfer channel region with a gate insulating film interposed therebetween, and the signal charges read from the photoelectric conversion section by the charge readout section are transferred in the vertical direction As shown in FIG.

[0005]

On the other hand, in the CMOS image sensor, in addition to the photoelectric conversion portion, pixels are formed so as to include pixel transistors. The pixel transistor is configured to read the signal charge generated by the photoelectric conversion unit and output it as an electric signal to the signal line.

[0006]

Generally, in a solid-state imaging device, a substrate is provided on the surface side where a multilayer wiring layer in which a plurality of wirings are laminated is provided, and light incident from the surface side of the substrate is received by the photoelectric conversion portion on the light receiving surface .

[0007]

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In the case of "surface illumination type", a multilayer wiring layer is interposed between the microlens and the light receiving surface, and the distance between the light collecting surface and the light receiving surface is long.

Therefore, when light is incident at an inclination with respect to the light receiving surface, the light included in the multilayer wiring layer may be blocked and may not reach the light receiving surface in some cases. Therefore, it may be difficult to improve the sensitivity.

[0008]
For this reason, a "backside illumination type" in which the photoelectric conversion unit receives light incident from the back side opposite to the surface on which the multilayer wiring layer is provided on the substrate has been proposed.

[0009]

In the solid-state imaging device, incident light incident on one pixel may not be incident on the photodiode of the one pixel but may be incident on the photodiode of another adjacent pixel.

Therefore, due to such an optical phenomenon, noise is included in the signal, and the image quality of the captured image may be deteriorated in some cases. For example, in the case of capturing a color image, when incident light is incident obliquely with respect to the light receiving surface, it is not incident on the light receiving surface right under the incident light but another light receiving originally receiving colored light of another color May enter the surface. For this reason, so-called "color mixing" occurs, which causes color misregistration in the captured color image, which may degrade image quality. In order to suppress the occurrence of such a problem, a light shielding film is provided between a plurality of pixels (see, for example, Patent Documents 1 and 2).

[0010]

Further, at the central portion of the pixel region in which a plurality of pixels are arranged, the angle of the principal ray incident through the external optical system is substantially perpendicular to the light receiving surface, whereas the pixel In the peripheral portion of the region, the angle of the incident principal ray is inclined. For this reason, the central portion of

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the captured image becomes a bright image and the peripheral portion becomes a dark image in some cases. In other words, a so-called shading phenomenon may occur, which may degrade image quality. In order to solve such a problem, it is called "pupil correction" to correct the arrangement of on-chip lenses and the like. Specifically, it has been practiced to provide an on-chip lens so that the position of the on-chip lens disposed around the pixel region shifts toward the center of the pixel region with respect to the light receiving surface. For example, each part is arranged so that the pitch of the on-chip lens becomes narrower than the pitch of the plurality of photoelectric conversion parts arranged in the pixel region (see, for example, Patent Document 3).

[0011]

Further, in the solid-state imaging device, in order to suppress the occurrence of dark current due to the interface state of the semiconductor substrate provided with the photoelectric conversion portion to improve the image quality, the photoelectric conversion portion is formed by HAD (Hole Accumulation Diode) structure has been proposed. In the HAD structure, the generation of dark current is suppressed by forming a positive charge accumulation (hole) accumulation region on the light receiving surface of the n-type charge accumulation region. In order to form the positive charge accumulation region at the interface portion of the photoelectric conversion portion, it has been proposed to provide "a film having a negative fixed charge" as a pinning layer to suppress the generation of dark current. For example, a high dielectric film such as a hafnium oxide film (HfO 2 film) is used as "a film having negative fixed charges" (see, for example, Patent Document 4).

[0012]

In order to suppress the generation of dark current, it has been proposed to provide a control gate on the front side of the "back side irradiation type" and apply a negative voltage to the control gate (for example, refer to Japanese Patent Application Laid-Open reference). In addition, in order to suppress the generation of dark current, it has been proposed to apply a negative voltage to a metal light-shielding film having a light-receiving surface portion for receiving light having an opening (see, for example, Patent Document 6)

[0013]

As described above, in the solid-state imaging device, various techniques have been proposed to improve the image quality of the captured image.

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[0014]
Japanese Unexamined Patent Publication No. 2010-109295 Patent Document 2: Japanese Patent Application Laid-Open No. 2010-186818 Patent Document 3: Japanese Patent No. 3551437 Patent Document 4: Japanese Unexamined Patent Application Publication No. 2008-306154 Patent Document 2: Japanese Unexamined Patent Application Publication No. 2007-258684 Patent Document 3: Japanese Unexamined Patent Publication No. Hei 5-275673

[0015]
In the solid-state imaging device, further improvement of the image quality etc. of the captured image is desired.

[0016]
Accordingly, the present technology provides a solid-state imaging device, a manufacturing method thereof, and an electronic device, which can improve the image quality of a captured image and the like.

[0017]
In the solid-state imaging device and the electronic device of the present technology, a plurality of the solid-state imaging device and the electronic device are provided inside the semiconductor substrate, corresponding to each of a plurality of pixels arranged in the pixel region of the semiconductor substrate with a space therebetween, And a pixel separating portion provided inside the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein the pixel separating portion is formed on the semiconductor substrate A first light shielding portion provided inside a trench formed on the incident surface side of the first light shielding portion on the incident surface side of the semiconductor substrate and provided on the incident surface side of the first light shielding portion And the second light shielding portion is formed so that the center of the second light shielding portion in the periphery from the center of the pixel region is larger than the center of the pixel separating portion in the pixel Shift a lot to the side of the area It is sea urchin formation.

[0018]
A manufacturing method of a solid-state image pickup device according to the present technology is a method of manufacturing a solid-state image pickup device including a photoelectric conversion portion that receives incident light on a light receiving surface, so as to correspond to each of a plurality of pixels arranged in a pixel region of a semiconductor

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substrate with a space therebetween A pixel separating portion forming step of providing a pixel separating portion inside the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein the pixel separation In the portion forming step, a first light shielding portion is provided in a trench formed in the pixel separation portion of the semiconductor substrate on the incident surface side, and a first light shielding portion is formed on the surface of the semiconductor substrate on the incident surface side, At least the second light shielding portion is provided on the incident surface side of the one light shielding portion, and in the step of forming the second light shielding portion, the center of the second light shielding portion is located closer to the periphery than the center of the pixel region, The center of Against it, to shift more toward the periphery of the pixel region, forming the second light-shielding portion.

[0019]

In the present technology, the first light shielding portion is provided inside the trench formed in the pixel separation portion of the semiconductor substrate, and the second light shielding portion is provided on the incident surface side of the first light shielding portion.

Here, the second light shielding portion is formed so that the center of the second light shielding portion shifts more toward the periphery of the pixel region than the center of the pixel separation portion in the periphery of the center of the pixel region.

That is, "pupil correction" is performed at least for the second light shielding portion.

[0020]

According to the present technology, it is possible to provide a solid-state imaging device, a manufacturing method thereof, and an electronic device capable of improving the image quality or the like of a captured image.

[0021]

FIG. 1 is a configuration diagram showing a configuration of a camera in the first embodiment.

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FIG. 2 is a diagram showing the overall configuration of the solid-state imaging device according to the first embodiment.

FIG. 3 is a diagram showing a main part of the solid-state imaging device according to the first embodiment.

FIG. 4 is a diagram showing a main part of the solid-state imaging device according to the first embodiment.

FIG. 5 is a diagram showing a main part of the solid-state imaging device according to the first embodiment.

FIG. 6 is a diagram showing a main part of the solid-state imaging device according to the first embodiment. FIG. 7 is a diagram showing a main part of the solid-state imaging device according to the first embodiment. FIG. 8 is a timing chart showing a control signal to be transmitted to the pixel transistor Tr of the pixel P when imaging is performed in the first embodiment. FIG. 9 is a diagram showing a method of manufacturing the solid-state imaging device according to the first embodiment. FIG. 10 is a diagram showing a method of manufacturing the solid-state imaging device in the first embodiment. FIG. 11 is a diagram showing a method for manufacturing the solid-state imaging device in the first embodiment. FIG. 12 is a view showing a manufacturing method of the solid-state imaging device in the first embodiment. FIG. 13 is a diagram showing a manufacturing method of the solid-state imaging device in the first embodiment. FIG. 14 is a cross-sectional view showing how the incident light enters the solid-state imaging device in the first embodiment. FIG. 15 is a diagram showing a main part of the solid-state imaging device according to the second embodiment. FIG. 16 is a cross-sectional view showing how incident light enters the solid-state imaging device in the second embodiment. FIG. 17 is a diagram showing a main part of the solid-state imaging device according to the third embodiment. FIG. 18 is a cross-sectional view showing how incident light enters the solid-state imaging device in the third embodiment. FIG. 19 is a diagram showing a main part of the solid-state imaging device according to the fourth embodiment. FIG. 20 is a diagram showing a main part of the solid-state imaging device according to the fourth embodiment. FIG. 21 is a diagram showing a main part of the solid-state imaging device in the fifth embodiment. FIG. 22 is a diagram showing a main part of the solid-state imaging device in the sixth embodiment. FIG. 23 is a diagram showing a main part of the solid-state imaging device according to the seventh embodiment. FIG. 24 is a diagram showing a main part of the solid-state imaging device according to the eighth embodiment. FIG. 25 is a diagram showing a main part of the solid-state imaging device according to the ninth embodiment.

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[0022]
Embodiments will be described with reference to the drawings.

[0023]

The description is given in the following order.

1. Embodiment 1 (Case of "pupil correction" on the upper part of the light shielding film of the pixel separating section) 2. Second Embodiment (Case of "Pupil Correction" on the Top of Light Shielding Film of Pixel Separation Unit) 3. Third Embodiment (Case of "Pupil Correction" on the Top of Light Shielding Film of Pixel Separation Unit) Embodiment 4 (a case where a diffusion layer is provided in a pixel separation portion) 5. Fifth Embodiment (Case of "Pupil Correction" on the Top and Bottom of Light Shielding Film of Pixel Separation Unit) Embodiment 6 (Case of "pupil correction" on the upper part and the lower part of the light shielding film of the pixel separation part) Embodiment 7 (Case of "pupil correction" on the upper part and the lower part of the light shielding film of the pixel separation part) 8. Eighth Embodiment (Penetration of Shading Film of Pixel Separation Unit) 9. Embodiment 9 (Case where the light shielding film of the pixel separating portion is penetrated) Other

[0024]

< 1. First Embodiment (A) Device Configuration (A-1) Configuration of Main Part of Camera FIG. 1 is a configuration diagram showing a configuration of a camera in a first embodiment.

[0025]
As shown in FIG. 1, the camera 40 includes a solid-state imaging device 1, an optical system 42, a control unit 43, and a signal processing unit 44.

[0026]

In the camera 40, the solid-state imaging device 1 receives incident light H incident as a subject

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image via the optical system 42 on the imaging plane PS and photoelectrically converts it to generate signal charges.

Here, the solid-state imaging device 1 is driven based on a control signal output from the control unit 43, reads the generated signal charge, and outputs an electric signal.

[0027]
The optical system 42 includes optical members such as an imaging lens and a diaphragm and is arranged so as to condense the incident light H onto the imaging surface PS of the solid-state imaging device 1.

[0028]
The control unit 43 outputs various control signals to the solid-state imaging device 1 and the signal processing unit 44, and controls and drives the solid-state imaging device 1 and the signal processing unit 44.

[0029]
The signal processing unit 44 is configured to generate a digital image of the subject image by performing signal processing with the electric signal output from the solid-state imaging device 1 as raw data.

[0030]

In the present embodiment, as shown in FIG. 1, a light beam H 1 emitted from the optical system 42 is incident as incident light H at an angle perpendicular to the imaging plane PS at the center portion of the imaging plane PS.

On the other hand, in the peripheral portion of the imaging plane PS, the principal ray H 2 is incident as incident light H at an angle tilted with respect to the direction perpendicular to the imaging plane PS.

Here, the principal ray H 2 of the incident light is inclined from the center of the imaging plane PS toward the periphery.

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This is because the exit pupil distance formed by the diaphragm forming the optical system 42, which will be described later, is finite.

[0031]

(A-2) Main Configuration of Solid-State Imaging Device The overall configuration of the solid-state imaging device 1 will be described.

[0032]

FIG. 2 is a diagram showing the overall configuration of the solid-state imaging device according to the first embodiment.

[0033]

The solid-state imaging device 1 of this embodiment is a CMOS type image sensor, and includes a semiconductor substrate 101, as shown in FIG. 2.

In the semiconductor substrate 101, for example, a single crystal silicon substrate is thinned, and a pixel region PA and a peripheral region SA are provided on the surface.

[0034]

As shown in FIG. 2, the pixel region PA has a rectangular shape, and a plurality of pixels P are arranged at equal intervals in the horizontal direction x and the vertical direction y, respectively.

That is, the pixels P are arranged in a matrix.

[0035]

In the pixel region PA, the pixel P is configured to receive incident light and generate signal

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charges. Then, the generated signal charge is read out by a pixel transistor (not shown) and outputted as an electric signal. The detailed configuration of the pixel P will be described later.

[0036]

As shown in FIG. 2, the peripheral area SA is located around the pixel area PA. In the peripheral area SA, a peripheral circuit is provided.

[0037]
Specifically, as shown in FIG. 2, the vertical drive circuit 13, the column circuit 14, the horizontal drive circuit 15, the external output circuit 17, the timing generator (TG) 18, and the shutter drive circuit 19, And is provided as a peripheral circuit.

[0038]
As shown in FIG. 2, the vertical drive circuit 13 is provided in the side portion of the pixel area PA in the peripheral area SA, and is configured to select and drive the pixels P of the pixel area PA in units of rows There.

[0039]

As shown in FIG. 2, the column circuit 14 is provided in the lower end portion of the pixel area PA in the peripheral area SA, and performs signal processing on a signal output from the pixel P on a column basis.

Here, the column circuit 14 includes a CDS (Correlated Double Sampling) circuit (not shown) and performs signal processing for removing fixed pattern noise.

[0040]

As shown in FIG. 2, the horizontal drive circuit 15 is electrically connected to the column circuit 14.

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The horizontal drive circuit 15 includes, for example, a shift register, and sequentially outputs signals held for each column of pixels P in the column circuit 14 to the external output circuit 17.

[0041]

As shown in FIG. 2, the external output circuit 17 is electrically connected to the column circuit 14, performs signal processing on the signal output from the column circuit 14, and outputs it to the outside. The external output circuit 17 includes an AGC (Automatic Gain Control) circuit 17 a and an ADC circuit 17 b. In the external output circuit 17, after the AGC circuit 17 a applies a gain to the signal, the ADC circuit 17 b converts the analog signal to the digital signal and outputs it to the outside.

[0042]

As shown in FIG. 2, the timing generator 18 is electrically connected to the vertical drive circuit 13, the column circuit 14, the horizontal drive circuit 15, the external output circuit 17, and the shutter drive circuit 19, respectively. The timing generator 18 generates various timing signals and outputs the timing signals to the vertical drive circuit 13, the column circuit 14, the horizontal drive circuit 15, the external output circuit 17, and the shutter drive circuit 19, thereby controlling the drive of each part.

[0043]
The shutter drive circuit 19 is configured to select the pixels P in units of rows and adjust the exposure time in the pixels P.

[0044]
(A-3) Detailed Configuration of Solid-State Imaging Device Detailed contents of the solid-state imaging device according to the present embodiment will be described.

[0045]
3 to 7 are diagrams showing the main parts of the solid-state imaging device in the first embodiment.

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[0046]

FIG. 3 is a cross-sectional view of the pixel P.

In FIG. 3, one pixel arranged in the central portion of the pixel area PA shown in FIG. 2 and showing the X 1 -X 2 portion.

[0047]

FIG. 4 is a top view of the pixel P, showing four pixels P arranged in the central portion of the pixel area PA shown in FIG. 2.

In FIG. 4, for the sake of convenience of explanation, there are portions showing each member by using a line other than a solid line such as a broken line.

[0048]

FIG. 5 is a cross-sectional view of the pixel separation unit 301.

FIG. 6 is a top view of the pixel separation unit 301. In FIGS. 5 and 6, (a) shows the pixel separation section 301 between the pixels P arranged in the central portion of the pixel area PA shown in FIG. 2, and shows the X 1 C - X 2 C section. On the other hand, (b) shows a pixel separation section 301 between pixels P arranged in the peripheral part of the pixel region PA shown in FIG. 2, and shows the X 1 S - X 2 S part. That is, in FIGS. 5 and 6, the pixel separation section 301 provided between a pair of pixels P aligned in the horizontal direction x is shown. Although not shown, the pixel separating unit 301 provided between the pair of pixels P arranged in the vertical direction y is also provided in a form similar to that of FIG. 5 and FIG. 6.

[0049]

Further, FIG. 7 shows the circuit configuration of the pixel P.

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[0050]

As shown in FIG. 3, in the solid-state imaging device 1, a photodiode 21 is provided inside a semiconductor substrate 101.

Here, it is provided on the semiconductor substrate 101 of thinned single crystal silicon.

[0051]
On the back surface (upper surface in FIG. 3) of the semiconductor substrate 101, members such as a color filter CF and a microlens ML are provided.

[0052]

On the other hand, the pixel transistor Tr shown in FIG. 7 is provided on the front surface (the lower surface in FIG. 3) of the semiconductor substrate 101 although not shown in FIG. 3.

As shown in FIG. 3, a wiring layer 111 is provided so as to cover the pixel transistor Tr, and on the surface of the wiring layer 111 opposite to the semiconductor substrate 101 side, a support substrate SS Are provided.

[0053]
That is, the solid-state imaging device 1 of the present embodiment is a "back-illuminated CMOS image sensor", in which the incident light H incident from the back side (upper surface) side is received by the photodiode 21 and a color image is generated by imaging As shown in FIG.

[0054]
Details of each part will be sequentially explained.

[0055]

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(A) Photodiode 21 In the solid-state imaging device 1, a plurality of photodiodes 21 are arranged in the pixel area PA so as to correspond to the plurality of pixels P shown in FIG. 2.

That is, on the imaging plane (xy plane), they are provided side by side in the horizontal direction x and the vertical direction y orthogonal to the horizontal direction x.

[0056]
A plurality of photodiodes 21 are provided in the semiconductor substrate 101 with a space therebetween so that the incident light H is received by the light receiving surface JS and photoelectrically converted so as to generate and accumulate signal charges.

[0057]

Here, as shown in FIG. 3, the photodiode 21 receives incident light H incident from the rear surface (upper surface in FIG. 3) of the semiconductor substrate 101.

As shown in FIG. 3, a flattening film HT, a color filter CF, and a microlens ML are provided above the photodiode 21. The incident light H that has entered through each part sequentially is received by the light receiving surface JS And photoelectric conversion is performed.

[0058]
As shown in FIG. 3, the photodiode 21 is provided in the semiconductor substrate 101.

[0059]

For example, in the photodiode 21, the n-type semiconductor region 101 n is formed as a charge accumulation region that accumulates charges (here, electrons).

In the photodiode 21, the n-type semiconductor region 101 n is provided inside the p-type semiconductor regions 101 pa, 101 pc of the semiconductor substrate 101.

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Here, a p-type semiconductor region 101 pc is provided on the back surface (upper surface) side of the semiconductor substrate 101 in the n-type semiconductor region 101 n. In the n-type semiconductor region 101 n, on the surface (lower surface) side of the semiconductor substrate 101, a p-type semiconductor region 101 pc having a higher impurity concentration than the back surface (upper surface) side is provided. That is, the photodiode 21 has the HAD structure, and the p-type semiconductor regions 101 pa and 101 pc are formed so as to suppress generation of dark current at each interface between the upper surface side and the lower surface side of the n-type semiconductor region 101 n Has been done.

[0060]

As shown in FIG. 3, a pixel separation section 301 for electrically separating a plurality of pixels P is provided, and the photodiode 21 is provided in the region of the pixel P partitioned by the pixel separation section 301 Has been done. For example, as shown in FIG. 4, the pixel separating unit 301 is formed in a grid pattern so as to be interposed between a plurality of pixels P, and the photodiode 21 is formed by arranging the pixels P And is formed in the region.

[0061]

As shown in FIG. 7, the anode of each photodiode 21 is grounded, the accumulated signal charge (here, electrons) is read out by the pixel transistor Tr and is transferred as an electric signal to the vertical signal line 27 And is configured to be outputted.

[0062]

(B) Color Filter CF In the solid-state imaging device 1, as shown in FIG. 3, the color filter CF is provided on the back side (upper surface in FIG. 3) side of the semiconductor substrate 101.

[0063]

Here, as shown in FIG. 3, the planarizing film HT is formed of a light transmitting material so as to cover the back surface (upper surface) of the semiconductor substrate 101, and the semiconductor substrate 101 A color filter CF is formed on the back surface (upper surface) of the color filter CF.

[0064]

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As shown in FIG. 4, the color filter CF includes a red filter layer CFR, a green filter layer CFG, and a blue filter layer CFB.

Each of the red filter layer CFR, the green filter layer CFG, and the blue filter layer CFB is disposed adjacent to each other, and one of them is provided corresponding to each of the plurality of pixels P.

[0065]

Here, as shown in FIG. 4, the red filter layer CFR, the green filter layer CFG, and the blue filter layer CFB are arranged so as to be aligned in a Bayer array.

That is, the plurality of green filter layers CFG are arranged side by side in the diagonal direction so as to form a checkered pattern.

The red filter layer CFR and the blue filter layer CFB are arranged in the diagonal direction in the plurality of green filter layers CFG.

[0066]

In the color filter CF, the red filter layer CFR has high light transmittance in a wavelength band corresponding to red (for example, 625 to 740 nm). In other words, the red filter layer CFR is formed so that the incident light H passes through the light receiving surface JS as red light.

[0067]

In the color filter CF, the green filter layer CFG has high light transmittance in a wavelength band corresponding to green (for example, 500 to 565 nm). In other words, the green filter layer CFG is formed so that the light transmittance of light in a wavelength range shorter than that of the red filter layer CFR is high, and the incident light H passes through the light receiving surface JS as green light.

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[0068]

In the color filter CF, the blue filter layer CFB has high light transmittance in a wavelength band corresponding to blue (for example, 450 to 485 nm). In other words, the blue filter layer CFB is formed so that the light transmittance of light having a wavelength range shorter than that of the green filter layer CFG is high, and the incident light passes through the light receiving surface JS as blue light.

[0069]

In this way, the color filter CF has a plurality of types of filter layers CFR, CFG, CFB with high transmittance for light in different wavelength ranges corresponding to each of the plurality of pixels P and are disposed adjacent to each other .

[0070]

(C) Microlens ML In the solid-state imaging device 1, as shown in FIG. 3, the microlens ML is provided on the upper surface of the color filter CF on the side of the back surface (upper surface in FIG. 3) of the semiconductor substrate 101 .

[0071]

A plurality of microlenses ML are arranged so as to correspond to each pixel P.

The microlens ML is a convex lens that protrudes in a convex shape on the back surface side of the semiconductor substrate 101 and is configured to collect incident light H to the photodiode 21 of each pixel P.

For example, the microlens ML is formed using an organic material such as a resin.

[0072]

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(D) Pixel Separation Unit 301 In the solid-state imaging device 1, the pixel separation unit 301 is formed so as to partition a plurality of pixels P as shown in FIGS. 3 and 4. The pixel separation unit 301 electrically separates the respective pixels P from each other. That is, inside the semiconductor substrate 301, the photodiodes 21 of each pixel P are electrically isolated.

[0073]
As shown in FIG. 3, in the pixel separating section 301, p type semiconductor regions 101 pa, 101 pc are provided between the n type semiconductor regions 101 n constituting the charge accumulation region of the photodiode 21.

[0074]
As shown in FIG. 3, in the pixel separating section 301, in the portion of the semiconductor substrate 101 on the rear surface (upper surface) where the incident light H is incident and located on the side of the photodiode 21, the trench TR Are provided.

[0075]
As shown in FIG. 3, the pixel separation portion 301 includes an insulating layer 311 and a light shielding layer 313, and these portions are provided inside the above-described trench TR.

[0076]

As shown in FIG. 4, the pixel separating unit 301 has a lattice shape in plan view, and is interposed between a plurality of pixels P.

A trench TR is formed in the pixel separating portion 301 so that the planar shape is a lattice shape.

A photodiode 21 is formed in the rectangular region partitioned by the grid-like pixel separation portion 301.

[0077]

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Specifically, as shown in FIG. 4, the pixel separating unit 301 divides the pixel P so that it extends in a straight line in a vertical direction y orthogonal to the horizontal direction x between a pair of pixels P arranged in the horizontal direction x For example.

Along with this, the pixel separation section 301 is provided so as to extend linearly in the horizontal direction x between a pair of pixels P aligned in the vertical direction y.

[0078]

As shown in FIG. 4, similarly to the pixel separation section 301, the trench TR extends in the vertical direction y between a pair of pixels P aligned in the horizontal direction x and a pair of Is provided so as to extend in the horizontal direction x between the pixels P. The insulating layer 311 and the light shielding layer 313 are provided so as to extend in the vertical direction y and the horizontal direction x between the respective pixels P like the pixel separation portion 301 and the trench TR.

[0079]

As shown in FIGS. 5 and 6, the pixel separating unit 301 separates a portion located in the center of the pixel area PA (see FIG. 2) (in the case of (a)) and a portion located in the periphery of the pixel area PA (In the case of b), some are formed in different modes.

[0080]

As shown in FIGS. 5 and 6, in the pixel separating section 301, the trench TR is formed such that the center portion (in the case of (a)) of the pixel area PA (see FIG. 2) and the peripheral portion ((b) of the pixel area PA) In the case of FIG.

[0081]

Specifically, as shown in FIG. 5, the trench TR has a tapered cross section of a plane (xz plane) along the horizontal direction x and the depth direction z, and the trench TR is formed on the back surface (upper surface) Side is formed to be wider than the width TH 1 on the surface (lower surface) side.

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In addition, as shown in FIG. 5, the trench TR is formed such that this cross section is symmetrical with respect to the axis along the depth direction z.

[0082]
As shown in FIG. 6, the trench TR is formed so that its side surface extends in the vertical direction y.

[0083]

In the present embodiment, as shown in FIGS. 5 and 6 (a), in the central portion of the pixel region PA (see FIG. 2), the trench TR is located between the pair of pixels P in the central axis in the horizontal direction x Coincides with the center axis 301CX in the horizontal direction x of the pixel separation section 301. [

2B), the central axis in the horizontal direction x between the pair of pixels P in the peripheral portion of the pixel area PA (see FIG. 2) is located in the horizontal direction x of the pixel separation unit 301 And is formed so as to coincide with the center axis 301CX in the center axis 301CX.

[0084]

As shown in FIGS. 5 and 6, the insulating layer 311 is provided so as to cover the inner surface of the trench TR formed on the back surface (upper surface) side of the semiconductor substrate 101.

The insulating layer 311 is similarly formed in the central portion (in the case of (a)) of the pixel region PA (see FIG. 2) and in the peripheral portion (in the case of (b)) of the pixel region PA.

[0085]

As shown in FIGS. 5 and 6, a light shielding layer 313 is provided so as to bury the inside of the trench TR covered with the insulating layer 311. A part of the light shielding layer 313 is formed

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in a different manner in the center part (in the case of (a)) of the pixel region PA (see FIG. 2) and in the peripheral part (in the case of (b)) of the pixel region PA There.

[0086]
5 and 6 show the pixel separation section 301 provided between a pair of pixels P aligned in the horizontal direction x, the pixel separation section 301 provided between a pair of pixels P arranged in the vertical direction y Are also formed in the same manner as above.

[0087]
The details of each part constituting the pixel separation section 301 will be described.

[0088]
(D-1) Insulating Layer 311 The insulating layer 311 is provided in the pixel separating portion 301, as shown in FIG. 3.

[0089]
Here, the insulating layer 311 is formed inside the trench TR so as to cover the side surface and the bottom surface.

[0090]
3, in addition to the pixel separating section 301, the insulating layer 311 is formed so as to cover the light receiving surface JS on which the incident light H is incident on the back surface (upper surface) of the semiconductor substrate 101 There.

[0091]
In the present embodiment, the insulating layer 311 includes a first insulating film 311 A and a second insulating film 311 B, as shown in FIG. 3.

[0092]

As shown in FIG. 3, the first insulating film 311 </ b> A is formed inside the trench TR and covers the side surface and the bottom surface in the pixel separation portion 301.

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As shown in FIG. 3, the first insulating film 311 </ b> A is formed so as to cover the light receiving surface JS on which the incident light H is incident on the back surface (upper surface) of the semiconductor substrate 101.

[0093]

As shown in FIG. 3, the second insulating film 311 B is formed so as to cover the side surface and the bottom surface of the trench TR inside the trench TR via the first insulating film 311 A in the pixel separation portion 301 as shown in FIG. 3 .

As shown in FIG. 3, the second insulating film 311 </ b> B is formed so as to cover the light receiving surface JS on the back surface (upper surface) of the semiconductor substrate 101 with the first insulating film 311 </ b> A interposed therebetween.

[0094]
As shown in FIGS. 5 and 6, the first insulating film 311 A and the second insulating film 311 B are formed so that the center portion (in the case of (a)) of the pixel region PA (see FIG. 2) and the peripheral portion (B)) are formed in the same manner.

[0095]
Each of the first insulating film 311 A and the second insulating film 311 B is formed using an insulating material such as SiO 2, SiN, a low-k material (SiOC, SiLK) or the like.

[0096]

Here, it is preferable that the refractive index of the first insulating film 311 </ b> A is formed using a material between the second insulating film 311 </ b> B and the semiconductor substrate 101.

That is, it is preferable that the first insulating film 311 </ b> A and the second insulating film 311 </ b> B are laminated so that the refractive index is sequentially lowered in the trench TR.

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By doing like this, it is possible to suitably prevent light traveling from the semiconductor substrate 101 side to the trench TR from being reflected at the interface.

[0097]

Although the case where the insulating layer 311 is formed of two films of the first insulating film 311 </ b> A and the second insulating film 311 </ b> B has been described, the insulating layer 311 is not limited thereto.

The insulating film 311 may be composed of three or more films.

In addition, the insulating layer 311 may be formed of a single material.

[0098]
(D-2) Light-shielding layer 313 As shown in FIGS. 3 and 4, the light-shielding layer 313 is provided in the pixel separation portion 301.

[0099]
In this embodiment, as shown in FIGS. 3 and 4, the light shielding layer 313 includes a first light shielding portion 313 A and a second light shielding portion 313 B, and the first light shielding portion 313 A and the second light shielding portion 313 B Are provided so as to be integrated with each other.

[0100]

As shown in FIG. 3, the first light shielding portion 313 A of the light shielding layer 313 is formed so as to bury the inside of the trench TR with the insulating layer 311 interposed therebetween.

The first light shielding portion 313 </ b> A is provided within the range of a portion where the trench TR is provided on the back surface (upper surface) of the semiconductor substrate 101.

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[0101]

Here, as shown in FIG. 3, the first light-shielding portion 313 A is formed so that a cross section of a plane (xz plane) along the horizontal direction x and the depth direction z is tapered.

That is, as shown in FIG. 5 (a), the first light shielding portion 313 A is formed so that the width HA 2 on the back surface (upper surface) side of the semiconductor substrate 101 is wider than the width HA 1 on the surface (lower surface) side There.

In addition, the first light shielding portion 313 </ b> A is formed so that this cross section is symmetrical with respect to the axis along the depth direction z.

[0102]

As shown in FIGS. 5 and 6, the first light shielding portion 313 A has a central portion (in the case of (a)) of the pixel region PA (see FIG. 2) and a peripheral portion (in the case of (b)) of the pixel region PA, In the same manner.

[0103]

Specifically, as shown in FIGS. 5 and 6 (a), in the center portion of the pixel area PA, the first light shielding portion 313 </ b> A is arranged in a horizontal direction x (x) between a pair of pixels P arranged in the horizontal direction x Is coincident with the central axis 301CX in the horizontal direction x of the pixel separating unit 301. In this case,

[0104]

As shown in FIGS. 5 and 6 (b), also in the peripheral portion of the pixel region PA, the first light shielding portion 313 </ b> A has the center axis in the horizontal direction x larger than the center in the horizontal direction x of the pixel separation portion 301 And is formed to coincide with the shaft 301CX.

[0105]

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As shown in FIG. 3, the second light shielding portion 313 </ b> B of the light shielding layer 313 is formed above the back surface (upper surface) of the semiconductor substrate 101 with the insulating layer 311 interposed therebetween.

The lower surface of the second light shielding portion 313 </ b> B is connected to the upper surface of the first light shielding portion 313 </ b> A.

In addition, the second light shielding portion 313 </ b> B is provided so as to protrude in a convex shape above the back surface (upper surface) of the semiconductor substrate 101 covered with the insulating layer 311.

The second light shielding portion 313 </ b> B is provided in the range of the portion where the trench TR is provided on the back surface (upper surface) of the semiconductor substrate 101.

[0106]

Here, as shown in FIG. 3, the second light-shielding portion 313 </ b> B is formed between the pair of pixels P arranged adjacent to each other in the horizontal direction x, the surface along the horizontal direction x and the depth direction z (the xz plane) Is formed so as to have a rectangular shape.

As shown in FIG. 5A, the second light shielding portion 313B is formed such that the width HB in the horizontal direction x is larger than the widths HB1, HB2 of the first light shielding portion 313A. In addition, the second light shielding portion 313 </ b> B is formed such that the cross section is symmetrical with respect to the axis along the depth direction z.

[0107]

As shown in FIG. 5 and FIG. 6, the second light shielding portion 313 B has a central portion (in the case of (a)) of the pixel region PA (see FIG. 2) and a peripheral portion (in the case of (b)) of the pixel region PA, And are formed at different positions from each other.

[0108]

Specifically, as shown in FIGS. 5 and 6 (a), at the central portion of the pixel region PA (see FIG.

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2), the second light shielding portion 313 </ b> B is formed such that the center of the cross section (xz plane) in the horizontal direction x The axis is formed so as to coincide with the central axis 301CX in the horizontal direction x of the pixel separating unit 301. As shown in FIG.

[0109]

On the other hand, as shown in FIGS. 5 and 6 (b), in the peripheral portion of the pixel region PA (see FIG. 2), the second light shielding portion 313 B is formed such that the center axis in the horizontal direction x of this cross section 313 BCX does not coincide with the center axis 301 CX in the horizontal direction x of the pixel separation unit 301.

Here, the center axis 313 BCX of the second light shielding portion 313 B is located closer to the periphery side (see FIG. 2) of the pixel region PA than the center axis 301 CX of the pixel separation portion 301.

And the second light shielding portion 313 </ b> B is formed so as to shift to the right side in FIG. 5). That is, the second light shielding portion 313 B is formed so that the center axis 313 BCX of the second light shielding portion 313 B and the center axis 301 CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x .

[0110]

As described above, the so-called "pupil correction" is not performed on the first light shielding portion 313 A of the light shielding layer 313, and "pupil correction" is performed on the second light shielding portion 313 B. That is, since the shift amount of the first light shielding portion 313A is zero, the second light shielding portion 313B is formed so that the shift amount Dx of the second light shielding portion 313B is larger than the shift amount of the first light shielding portion 313A ing.

[0111]

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In the present embodiment, the pixel region PA is divided into a central part and a peripheral part thereof, and the pixel region PA is provided with a second light shielding part 313 B as shown in FIGS. 5 and 6 (a) with respect to the central part , And the second light shielding portion 313 B is provided in the peripheral portion as shown in FIGS. 5 and 6 (b). Specifically, as shown in FIG. 5A, at the center of the pixel area PA, the pitch PBc of the second light shielding units 313 </ b> B arranged at equal intervals in the horizontal direction x is equal to the distance between the pixels arranged at equal intervals in the horizontal direction x Is formed to be the same as the pitch PG of the separation section 301. That is, as shown in FIG. 6 (a), the pitch PBc of the second light shielding portion 313 </ b> B extending in the vertical direction y in the horizontal direction x and the pitch PBc of the pixel separating portion 301 extending in the vertical direction y Are aligned in the horizontal direction x are the same as each other. On the other hand, in the peripheral area of the pixel area PA, as shown in FIG. 5 (b), the pitch PBs of the second light shielding units 313 </ b> B arranged at equal intervals in the horizontal direction x is equal to the number of pixels And is formed so as to be wider than the pitch PG of the separation portion 301. That is, as shown in FIG. 6B, the pitch PBc of the second light shielding portion 313 </ b> B extending in the vertical direction y in the horizontal direction x is extended in the vertical direction y of the pixel separation portion 301 Are wider than the pitch PG arranged in the horizontal direction x. Although not shown, the second light shielding portion 313 B is also provided in the vertical direction y as well.

[0112]

In addition to this, with respect to the second light shielding portion 313B, the shift amount Dx between the center axis 313BCX of the second light shielding portion 313B and the center axis 301CX of the pixel separation portion 301 May be increased. Specifically, with respect to each of the second light-shielding portions 313 </ b> B provided in each of the pixel separation portions 301 between the plurality of pixels P aligned in the horizontal direction x, the pitch in the horizontal direction x thereof is larger than the pitch of the pixel separation portion 301 As shown in FIG. The pitch in the vertical direction y of each of the second light shielding portions 313 B provided in each of the pixel separation portions 301 between a plurality of pixels P arranged in the vertical direction y is wider than the pitch of the pixel separation portion 301 As shown in FIG. That is, with respect to the pixel separating portion 301 and the second light shielding portion 313 provided between the pair of pixels P in the pixel region PA, the second light shielding portion 313 is arranged at a wider pitch than the pixel separating portion 301 at equal intervals As shown in FIG.

[0113]

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The light shielding layer 313 is formed using a light shielding material that shields light by reflecting light. For example, a light shielding layer 313 is formed using a metal material such as Ti, TiN, W, Al or the like.

[0114]

In the present embodiment, the first light-shielding portion 313 A and the second light-shielding portion 313 B are formed of the same material and formed so as to be integrated, but the present invention is not limited thereto. The first light shielding portion 313 A and the second light shielding portion 313 B may be formed of different materials. That is, the light shielding layer 313 may have a laminated structure.

[0115]
(E) Pixel Transistor Tr In the solid-state imaging device 1, a plurality of pixel transistors Tr are provided so as to correspond to the plurality of pixels P shown in FIG. 2.

[0116]
As shown in FIG. 7, the pixel transistor Tr includes a transfer transistor 22, an amplification transistor 23, a selection transistor 24, and a reset transistor 25, and is configured to read the signal charge from the photodiode 21 and output it as an electric signal There.

[0117]

Though not shown in FIG. 3, each of the transistors 22 to 25 constituting the pixel transistor Tr is provided on the surface on which the wiring layer 111 is provided in the semiconductor substrate 101.

For example, each of the transistors 22 to 25 is an N-channel MOS transistor, and each gate is formed using, for example, polysilicon.

Each of the transistors 22 to 25 is covered with a wiring layer 111.

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[0118]

In the pixel transistor Tr, as shown in FIG. 7, the transfer transistor 22 is configured to transfer the signal charge generated by the photodiode 21 to the floating diffusion FD. Specifically, as shown in FIG. 7, the transfer transistor 22 is provided between the cathode of the photodiode 21 and the floating diffusion FD. In the transfer transistor 22, the transfer line 26 is electrically connected to the gate. In the transfer transistor 22, based on the transfer signal TG transmitted from the transfer line 26 to the gate, the signal charge accumulated in the photodiode 21 is transferred to the floating diffusion FD.

[0119]

In the pixel transistor Tr, as shown in FIG. 7, the amplification transistor 23 is configured to amplify and output an electrical signal converted from charge to voltage in the floating diffusion FD. Specifically, as shown in FIG. 7, the gate of the amplifying transistor 23 is electrically connected to the floating diffusion FD. Further, the drain of the amplification transistor 23 is electrically connected to the power supply line Vdd, and the source thereof is electrically connected to the selection transistor 24. When the selection transistor 24 is selected to be in the ON state, the amplification transistor 23 is supplied with a constant current from the constant current source I and operates as a source follower. Therefore, in the amplification transistor 23, the selection signal is supplied to the selection transistor 24, whereby the electric signal converted from the charge to the voltage in the floating diffusion FD is amplified.

[0120]

In the pixel transistor Tr, as shown in FIG. 7, the selection transistor 24 is configured to output the electric signal output by the amplification transistor 23 to the vertical signal line 27 based on the selection signal. Specifically, as shown in FIG. 7, the selection transistor 24 has a gate connected to the address line 28 to which the selection signal is supplied. The selection transistor 24 is turned on when the selection signal is supplied, and outputs the output signal amplified by the amplification transistor 23 to the vertical signal line 27 as described above.

[0121]

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In the pixel transistor Tr, in the reset transistor 25, as shown in FIG. 7, the reset transistor 25 is configured to reset the gate potential of the amplification transistor 23. Specifically, as shown in FIG. 7, the gate of the reset transistor 25 is electrically connected to the reset line 29 to which the reset signal is supplied. In the reset transistor 25, the drain is electrically connected to the power supply line Vdd, and the source is electrically connected to the floating diffusion FD. The reset transistor 25 resets the gate potential of the amplification transistor 23 to the power supply voltage via the floating diffusion FD based on the reset signal transmitted from the reset line 29.

[0122]
FIG. 8 is a timing chart showing a control signal to be transmitted to the pixel transistor Tr of the pixel P when imaging is performed in the first embodiment.

[0123]

8A shows the selection signal SEL to be input to the gate of the selection transistor 24. In FIG.

(B) shows the reset signal RST input to the gate of the reset transistor 25. (C) shows the transfer signal TG input to the gate of the transfer transistor 22. (See FIG. 7).

[0124]

As shown in FIG. 8, when imaging is performed, the selection signal SEL is set to the high level at the first time point t 1, and the selection transistor 24 is turned on. Then, at the second time point t 2, the reset signal RST is set to the high level, and the reset transistor 25 is turned on. Thereby, the gate potential of the amplifying transistor 23 is reset (see FIG. 7).

[0125]

As shown in FIG. 8, at the third time point t 3, the reset signal RST is set to the low level, and the reset transistor 25 is turned off. Thereafter, a voltage corresponding to the reset level is read out to the column circuit 14 as an output signal (see FIGS. 2 and 7).

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[0126]

As shown in FIG. 8, at the fourth time point t 4, the transfer signal TG is set to the high level, and the transfer transistor 22 is turned on. As a result, the signal charge accumulated in the photodiode 21 is transferred to the floating diffusion FD (see FIG. 7).

[0127]

As shown in FIG. 8, at the fifth time point t 5, the transfer signal TG is set to the low level, and the transfer transistor 22 is turned off. Thereafter, a voltage of a signal level corresponding to the amount of the accumulated signal charge is read out to the column circuit 4 as an output signal (see FIGS. 2 and 7).

[0128]

In the column circuit 14, the signal of the reset level read out earlier and the signal of the signal level read out later are differentially processed to accumulate signals (see FIGS. 2 and 7).

[0129]

As a result, fixed pattern noise generated due to variations in Vth of each transistor provided for each pixel P is canceled.

[0130]

In the operation of driving the pixel P as described above, since the gates of the respective transistors 22, 24, and 25 are connected in units of rows composed of a plurality of pixels P arranged in the horizontal direction x, they are arranged in row units Are simultaneously performed on a plurality of pixels P.

[0131]

More specifically, it is sequentially selected in the vertical direction on a horizontal line (pixel row) basis by the selection signal supplied by the vertical drive circuit 13 described above.

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The transistors of each pixel P are controlled by various timing signals output from the timing generator 18.

As a result, the signal in each pixel is read out to the column circuit 14 for each column of pixels P through the vertical signal line 27 (see FIGS. 2 and 7).

[0132]
Then, the signals accumulated in the column circuit 14 are selected by the horizontal drive circuit 15 and sequentially output to the external output circuit 17 (see FIGS. 2 and 7).

[0133]
Then, the signal processing unit 44 carries out signal processing with the signal obtained by this imaging as raw data to generate a digital image (see FIG. 1).

[0134]
(F) About the Wiring Layer 111 In the solid-state imaging device 1, the wiring layer 111 includes, as shown in FIG. 3, a back surface (upper surface) on which the respective parts such as the color filter CF and the microlens ML are provided in the semiconductor substrate 101 Is provided on the opposite surface (lower surface).

[0135]

The wiring layer 111 includes a wiring 111 h and an insulating layer 111 z. In the insulating layer 111 z, a wiring 111 h is formed so as to be electrically connected to each element.

The wiring layer 111 is a so-called multilayer wiring layer, and is formed by alternately stacking an interlayer insulating film and a wiring 111 h constituting the insulating layer 111 z plural times.

Here, a plurality of wirings 111 h are stacked via an insulating layer 111 z so as to function as wirings such as the transfer line 26, the address line 28, the vertical signal line 27, the reset line

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29 and the like shown in FIG. 7 And is formed.

[0136]

In the wiring layer 111, a support substrate SS is provided on the surface opposite to the side on which the semiconductor substrate 101 is located.

For example, a substrate made of a silicon semiconductor having a thickness of several hundreds μm is provided as a support substrate SS.

[0137]
(B) Manufacturing Method A principal part of a manufacturing method for manufacturing the above-described solid-state imaging device 1 will be described.

[0138]
9 to 13 are diagrams showing a method for manufacturing a solid-state imaging device according to the first embodiment.

[0139]
Each figure shows a cross section similarly to FIG. 3.

[0140]
In the present embodiment, the steps (a) to (e) shown in each drawing are sequentially performed, and the solid-state imaging device 1 shown in FIG. 3 and the like is manufactured.

[0141]
Details of each process are sequentially shown.

[0142]
(A) Formation of Photodiodes 21 and the Like First, as shown in FIG. 9, photodiodes 21 and the like are formed.

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[0143]

Here, impurities are ion-implanted from the surface of the semiconductor substrate 101 made of a single crystal silicon semiconductor, so that each part such as the photodiode 21 is formed.

For example, after forming the p-type semiconductor region 101 pa over the entire surface of the semiconductor substrate 101, a p-type semiconductor region 101 pc having a higher impurity concentration than that is formed.

Then, an n-type semiconductor region 101 n is formed in a portion of the semiconductor substrate 101 where the photodiode 21 is to be formed.

[0144]

For example, each part is formed so as to have the following impurity concentration.

Impurity concentration of the p-type semiconductor region 101 pa: 5.0 × 10 <16> to 5.0 × 10 <17> cm <-3> Impurity concentration of the p-type semiconductor region 101 pc: 5.0 × 10 <17> to 5.0 × 10 < > cm <-3> Impurity concentration of n-type semiconductor region 101 n: 5.0 × 10 <15> to 5.0 × 10 <16> cm <-3>

[0145]

After forming the pixel transistor Tr (not shown in FIG. 7) on the surface of the semiconductor substrate 101, the wiring layer 111 is formed so as to cover the pixel transistor Tr.

Then, the supporting substrate SS is bonded to the surface of the wiring layer 111.

[0146]

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Thereafter, the semiconductor substrate 101 is thinned.

For example, it is preferable to perform thinning so as to satisfy the following conditions.

Thickness of semiconductor substrate 101 after thinning: 2 to 10 μ m Method: Chemical mechanical polishing (CMP) method (Otherwise, dry etching, wet etching is also acceptable.

Alternatively, a combination of CMP and dry etching or wet etching may be used.)

[0147]
Note that members such as the photodiode 21, the pixel transistor Tr, and the like are formed in the semiconductor layer of the SOI substrate (not shown), the wiring layer 111 and the supporting substrate SS are provided in the same manner as described above, and then thinning processing is performed Also good.

[0148]
(B) Formation of Trench TR Next, as shown in FIG. 10, a trench TR is formed.

[0149]
Here, in the semiconductor substrate 101, the trench TR is formed in the pixel separation portion 301 located between the plurality of pixels P.

[0150]

For example, after forming a mask (not shown) having a portion where a trench TR is to be formed on the back surface (upper surface) of the semiconductor substrate 101, the semiconductor substrate 101 is processed using the mask to form a trench TR .

For example, a dry etching process is performed on the semiconductor substrate 101 to form a trench TR.

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Then remove that mask.

[0151]

In the present embodiment, for example, it is preferable to form the trench TR so as to satisfy the following conditions.

- Width TH 1 on the lower surface side: 100 nm to 400 nm (When the width TH 1 is 100 nm or less, when burying the insulating film 311, probability of occurrence of defect may increase due to the self stress of the insulating film 311 itself. On the other hand, if the width TH 1 is too wide, the area of the formation region of the photodiode 21 decreases and the saturated electron amount decreases.) Width TH 2 on the upper surface side: 200 nm to 500 nm (The width TH 2 is determined by lithography resolution. The width YH 2 is a value in an exposure machine that uses, for example, KrF as a light source designation. Depth DT: 100 nm to 600 nm (Regions where color mixing tends to occur are distributed at positions where the depth DT from the light receiving surface JS is 100 nm to 500 nm, and this portion is divided by the trench TR to suppress color mixing it can.)

[0152]
(C) Formation of First Insulating Film 311 A Next, as shown in FIG. 11, the first insulating film 311 A is formed.

[0153]

Here, as shown in FIG. 11, the first insulating film 311 A is formed so as to cover the side surface and the bottom surface inside the trench TR in the pixel separation portion 301.

At the same time, the first insulating film 311 A is formed so as to cover the back surface (upper surface) of the semiconductor substrate 101.

[0154]

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For example, it is preferable to form the first insulating film 311 </ b> A under the following conditions. Material: HfO 2 (refractive index n = 2.1), TaO (refractive index n = 2.2), ZrO 2 (refractive index = 2.3), Al 2 O 3 (refractive index n = 2.1) Thickness: 40 nm To 60 nm Forming method: atomic layer deposition (ALD) method, sputtering method, metalorganic vapor phase CVD method (MOCVD method)

[0155]
(D) Formation of Second Insulating Film 311 B Next, as shown in FIG. 12, a second insulating film 311 B is formed.

[0156]

Here, as shown in FIG. 12, the second insulating film 311 B is formed so as to cover the side surface and the bottom surface of the trench TR via the first insulating film 311 A inside the trench TR.

At the same time, the second insulating film 311 B is formed so as to cover the back surface (upper surface) of the semiconductor substrate 101 with the first insulating film 311 A interposed therebetween.

[0157]

For the second insulating film 311 </ b> B, for example, it is preferable to form the second insulating film 311 </ b> B under the following conditions. Material: SiO 2 (refractive index n = 1.5), SiOC (refractive index n = 1.1) Thickness: 50 nm to 500 nm Method of formation: sputtering method, CVD method

[0158]
(E) Formation of light shielding layer 313 Next, as shown in FIG. 13, a light shielding layer 313 is formed.

[0159]

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Here, as shown in FIG. 13, the light shielding layer 313 is provided in the pixel separation portion 301.

[0160]
In the present embodiment, the light shielding layer 313 is provided so that the first light shielding portion 313 A and the second light shielding portion 313 B are integrated.

[0161]
Specifically, the first light shielding portion 313 A fills the inside of the trench TR with the insulating layer 311 interposed therebetween, and the second light shielding portion 313 B covers the back surface (upper surface) of the semiconductor substrate 101 via the insulating layer 311 , A light shielding layer 313 is formed.

[0162]

Regarding formation of the light shielding layer 313, first, a light shielding material that shields light is embedded in the trench TR with the insulating layer 311 interposed therebetween, thereby forming the first light shielding portion 313 A.

At the same time, a light shielding material for shielding light is formed so as to cover the back surface (upper surface) of the semiconductor substrate 101.

Then, the portion covering the back surface (upper surface) of the semiconductor substrate 101 is patterned to form the second light shielding portion 313B.

[0163]

For example, the light shielding layer 313 is formed under the following conditions.

Metal material such as Ti, Ti, W, Al and the like. The width HA 1 on the lower surface side of the first light-shielding portion 313 A: 0 nm to 50 nm (there is no limitation as to the width, depending on the shape of the trench TR and the film thickness of the insulating film 311 It is

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determined.

) Width HA 2 on the upper surface side of the first light shielding portion 313 A: 50 to 200 nm (there is no limitation on the width, and it is determined by the shape of the trench TR and the film thickness of the insulating film 311.) - Depth DA of the first light shielding portion 313 A: 100 nm to 300 nm (Improvement in optical characteristics is prominent because the first light shielding portion 313 A enters the wiring layer 111 side from the upper surface of the semiconductor substrate 101 by 50 nm or more . The width HB of the second light shielding portion 313B is 200 nm to 300 nm the thickness TB of the second light shielding portion 313B is 100 nm to 500 nm (optimized by the metal material used for the light shielding layer 313 and the film forming method). As an index, this thickness is set so that the light attenuation factor at 600 nm to 800 nm becomes -80 dB.)

[0164]
As shown in FIGS. 5 and 6, with respect to the second light shielding portion 313 B, the central portion (in the case of (a)) of the pixel region PA (see FIG. 2) and the peripheral portion ((b)) Are formed so as to be at different positions from each other.

[0165]

Here, in the peripheral portion of the pixel region PA, the center axis 313 BCX of the second light shielding portion 313 B is located closer to the peripheral side of the pixel region PA (see FIG. 2) than the central axis 301 CX of the pixel separation portion 301.

(Right side in FIG. 5 (b)), the second light shielding portion 313 B is formed. That is, the second light shielding portion 313 </ b> B is formed so that the center axis 313 </ b> BCX of the second light shielding portion 313 </ b> B and the central axis 301 </ b> CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x.

[0166]
As described above, the second light shielding portion 313B is formed by performing so-called "pupil correction".

[0167]

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For example, the shift amount Dx is determined by the size of the pixel P and the distance between the microlens ML and the light receiving surface JS.

Calculation of the shift amount Dx is performed, for example, using a ray tracing method or FDTD method.

[0168]
(F) Formation of Color Filter CF and Microlens ML Next, as shown in FIG. 3, the respective members of the color filter CF and microlens ML are formed.

[0169]
Here, the planarization film HT is formed on the back surface (upper surface) of the semiconductor substrate 101 provided with the light shielding layer 313.

[0170]
Thereafter, a color filter CF is formed.

[0171]

For example, a coating solution containing a dye such as a pigment or a dye and a photosensitive resin is coated by a coating method such as a spin coating method to form a coating film, and the coating film is patterned by lithography technique.

In this way, by forming the respective filter layers CFR, CFG, CFB, the color filter CF is provided.

[0172]
Thereafter, a microlens ML is provided on the upper surface of the color filter CF.

[0173]

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For example, after patterning the photosensitive resin film by photolithography technology, it is deformed into a lens shape by reflow processing, thereby forming the microlens ML.

In addition to this, after forming a lens-shaped resist pattern on the lens material film, the microlens ML may be formed by performing an etch back process using the resist pattern as a mask.

[0174]
By successively carrying out each step in this manner, a CMOS type image sensor of "back side irradiation type" is completed.

[0175]

(C) Summary As described above, in the present embodiment, the pixel separation unit 301 is provided inside the semiconductor substrate 101 so as to be interposed between the plurality of pixels P in the pixel area PA.

In the pixel separation portion 301, a first light shielding portion 313 A is provided inside a trench TR formed on the back surface (upper surface) side of the semiconductor substrate 101.

At the same time, a second light shielding portion 313 B is provided on the back surface (upper surface) of the semiconductor substrate 101.

Here, in the periphery of the center of the pixel region PA, the center of the second light shielding part 313 </ b> B of the second light shielding part 313 </ b> B shifts more toward the periphery of the pixel region PA than the center of the pixel separation part 301 As shown in FIG.

[0176]
That is, in the present embodiment, "pupil correction" is performed for the second light shielding portion 313B.

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[0177]
FIG. 14 is a cross-sectional view showing how the incident light enters the solid-state imaging device in the first embodiment.

[0178]

In FIG. 14, as with FIG. 5 (b), the peripheral portion of the pixel region PA (see FIGS. 1 and 2) is shown.

In FIG. 14, (a) shows a case where "pupil correction" is not performed on the second light shielding portion 313 B, unlike the present embodiment.

On the other hand, (b) is the case of the present embodiment, and shows the case where "pupil correction" is performed.

[0179]

As shown in FIG. 14, in the peripheral portion (see FIGS. 1 and 2) of the pixel area PA, no light beam is incident perpendicularly to the back surface of the semiconductor substrate 101, and the inclined light beam H 2 is incident. Here, the light ray H 2 is inclined so as to travel from the center of the pixel region PA to the periphery when heading toward the back surface of the semiconductor substrate 101.

[0180]

14 (a) and 14 (b), the light vector L1 of the light beam H2 incident on the inclined surface is reflected by the first light-shielding portion 313A of the light-shielding layer 313 after entering the insulating layer 311. As shown in FIG. Then, the reflected light vector L 1 is incident on the photodiode 21 and photoelectrically converted.

[0181]

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In addition, among the light beams H 2 incident at an inclination, the light vectors L 2 and L 3 are shielded by the second light shielding portion 313 B of the light shielding layer 313 as shown in FIGS. 14 (a) and 14 (b). Among them, the light vector L <b> 2 is reflected by the side surface of the second light shielding portion 313 </ b> B of the light shielding layer 313.

[0182]

At this time, as shown in FIG. 14 (a), when "pupil correction" is not performed for the second light shielding portion 313 B, the distance from the reflected portion to the back surface of the semiconductor substrate 101 is long , It attenuates before being photoelectrically converted.

[0183]

On the other hand, as shown in FIG. 14 (b), when "pupil correction" is performed on the second light shielding portion 313 B, the distance from the reflected portion to the back surface of the semiconductor substrate 101 is short Is not attenuated, enters the photodiode 21, and is photoelectrically converted.

In this manner, when "pupil correction" is performed, light can reach the photodiode 21 efficiently. Therefore, the image quality of the captured image can be improved.

[0184]

As shown in FIG. 14 (a), the light vector L 4 among the light beams H 2 incident on the inclined surface is such that when "pupil correction" is not performed on the second light shielding portion 313 B, the light shielding portion 313 B And is incident on the photodiode 21 of the adjacent pixel P. For this reason, "mixed color" or the like occurs, and the image quality of the captured image may be deteriorated in some cases.

[0185]

However, as shown in FIG. 14 (b), when "pupil correction" is performed on the second light

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shielding portion 313 B, the light vector L 4 is shielded by the second light shielding portion 313 B and the photodiode 21 . Therefore, in the present embodiment, it is possible to suppress the occurrence of "mixed color" and the like and to improve the image quality of the captured image.

[0186]
Therefore, in the present embodiment, the image quality of the captured image can be improved.

[0187]

In the present embodiment, the first insulating film 311 </ b> A constituting the insulating layer 311 is provided so as to cover the inner surface of the trench TR.

A second insulating film 311 </ b> B is provided so as to cover the inner surface of the trench TR with the first insulating film 311 </ b> A interposed therebetween. The first insulating film 311 </ b> A is formed using a material having a refractive index between the semiconductor substrate 101 and the second insulating film 311 </ b> B. Therefore, at the interface between the semiconductor substrate 101 and the trench TR, since the difference in refractive index is small, reflection of light at the interface can be suppressed. Therefore, in the ear embodiments, the effect of suppressing the surface reflectance can be more suitably exhibited.

[0188]

< 2 . Embodiment 2> (A) Device Configuration, etc. FIG. 15 is a diagram showing a main part of a solid-state imaging device in Embodiment 2. In FIG.

[0189]

FIG. 15 shows a pixel separation section 301 between pixels P arranged in the peripheral portion of the pixel area PA shown in FIG. 2 as in FIG. 5 and FIG. 6 (b), showing the X 1 S - X 2 S portion ing. FIG. 15A is a cross-sectional view of the pixel separation unit 301, and FIG. 15B is a top view of the pixel separation unit 301.

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[0190]

As shown in FIG. 15, in this embodiment, as can be seen from FIGS. 5 and 6 (b), the position of the second light shielding portion 313 B of the light shielding layer 313 in the peripheral portion of the pixel region PA is shifted Which is different from the first embodiment. Except for this point and related points, the present embodiment is similar to the first embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0191]

As shown in FIG. 15, the first light shielding portion 313 A of the light shielding layer 313 is formed so as to bury the inside of the trench TR via the insulating layer 311 as in the case of the first embodiment.

[0192]

As shown in FIG. 15, the second light shielding portion 313 </ b> B of the light shielding layer 313 is formed above the back surface (upper surface) of the semiconductor substrate 101 with the insulating layer 311 interposed therebetween.

[0193]

2), the center axis 313BCX of the second light shielding portion 313B is located closer to the periphery side of the pixel area PA (see FIG. 2) than the center axis 301CX of the pixel separation portion 301. In addition, in the peripheral portion of the pixel area PA (see FIG.

And the second light shielding portion 313 </ b> B is formed so as to shift to the right side in FIG. 5).

That is, so-called "pupil correction" is performed for the second light shielding portion 313B.

[0194]

However, in the present embodiment, as shown in FIG. 15, the shift amount Dx between the central axis 313 BCX of the second light shielding portion 313 B and the central axis 301 CX of the pixel separation portion 301 is larger than that in the first embodiment The second light

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shielding portion 313 </ b> B is formed.

[0195]
Specifically, in the case of the first embodiment, the second light shielding portion 313B is formed so as to be positioned within the range of the portion where the upper surface of the trench TR is located on the back surface (upper surface) of the semiconductor substrate 101 (See Fig. 5, Fig. 6 (b) etc).

[0196]

On the other hand, in the present embodiment, as shown in FIGS. 15A and 15B, the second light shielding portion 313 </ b> B is formed such that the range of the portion where the upper surface of the trench TR is located on the back surface (upper surface) of the semiconductor substrate 101 , It is formed so as to be located in a portion other than the range.

That is, the second light shielding portion 313 </ b> B is formed such that a predetermined shift amount Gx is shifted from the range of the portion where the upper surface of the trench TR is located on the back surface (upper surface) of the semiconductor substrate 101.

[0197]
Thus, in the present embodiment, the light shielding layer 313 is formed so that the upper surface of the first light shielding portion 313 </ b> A does not cover with the second light shielding portion 313 </ b> B but includes a portion where the light is incident upon being exposed.

[0198]
(B) Summary As described above, in the present embodiment, in the second light shielding portion 313B, the center of the second light shielding portion 313B is located closer to the center of the pixel separation portion 301 than the center of the pixel area PA , And is formed so as to be shifted to the peripheral side of the pixel area PA more.

[0199]
That is, in the present embodiment, "pupil correction" is performed for the second light shielding portion 313B.

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[0200]
Therefore, in the present embodiment, as in the first embodiment, the image quality of the captured image can be improved.

[0201]
In particular, in the present embodiment, in order to make the shift amount Dx between the center axis 313 BCX of the second light shielding portion 313 </ b> B and the central axis 301 </ b> CX of the pixel separation portion 301 larger than that in the first embodiment, A light shielding portion 313B is formed (see FIG. 15).

[0202]

Therefore, in the present embodiment, the light can reach the photodiode 21 more efficiently than in the case of the first embodiment.

Further, occurrence of "mixed color" and the like can be more effectively suppressed.

[0203]
FIG. 16 is a cross-sectional view showing how incident light enters the solid-state imaging device in the second embodiment.

[0204]
FIG. 16 shows a peripheral portion (see FIGS. 1 and 2) of the pixel area PA similarly to FIG. 15 (a).

[0205]

As shown in FIG. 16, in the peripheral portion (see FIGS. 1 and 2) of the pixel region PA, no light beam is incident perpendicularly to the back surface of the semiconductor substrate 101, and the inclined light beam H 2 is incident.

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Here, the light ray H 2 is inclined so as to travel from the center of the pixel region PA to the periphery when heading toward the back surface of the semiconductor substrate 101.

[0206]

As shown in FIG. 16, the light vector L 1 out of the inclined incident light H 2 is reflected by the first light shielding portion 313 A of the light shielding layer 313 after entering the insulating layer 311.

Then, the reflected light vector L 1 is incident on the photodiode 21 and photoelectrically converted.

[0207]

The light vectors L2 and L3 among the light beams H2 which are incident in an inclined state are blocked by the second light shielding portion 313B of the light shielding layer 313, as shown in FIG.

Among them, the light vector L 3 is reflected by the side surface of the second light shielding portion 313 B of the light shielding layer 313.

Then, it enters the photodiode 21 and is photoelectrically converted.

Therefore, in the present embodiment, light can reach the photodiode 21 efficiently.

Therefore, the image quality of the captured image can be improved.

[0208]

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The light vector L4 among the light beams H2 incident in an inclined state is shielded by the second light shielding portion 313B and does not enter the photodiode 21 of the adjacent pixel P as shown in FIG.

In the present embodiment, "pupil correction" is performed so that the second light shielding portion 313 </ b> B shifts to the peripheral side of the pixel region PA than in the first embodiment. Therefore, in the present embodiment, it is possible to more effectively suppress the occurrence of "mixed color" and the like and to improve the image quality of the captured image.

[0209]

＜3． Embodiment 3 (A) Device Configuration and the Like FIG. 17 is a diagram showing a main part of a solid-state imaging device in Embodiment 3.

[0210]

FIG. 17 shows a pixel separating portion 301 between pixels P arranged in the peripheral portion of the pixel area PA shown in FIG. 2, similarly to FIG. 15, and shows the X 1 S - X 2 S portion. FIG. 17A is a cross-sectional view of the pixel separation unit 301, and FIG. 17B is a top view of the pixel separation unit 301.

[0211]

As shown in FIG. 17, in the present embodiment, the width HBS of the second light shielding portion 313 B of the light shielding layer 313 is different from that in the second embodiment as can be seen from comparison with FIG. 15. Except for this point and related points, the present embodiment is similar to the second embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0212]

As shown in FIG. 17, the second light shielding portion 313 B of the light shielding layer 313 is formed above the back surface (upper surface) of the semiconductor substrate 101 via the

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insulating layer 311 as in the second embodiment There.

[0213]

2), the center axis 313BCX of the second light shielding portion 313B is located closer to the periphery side of the pixel area PA (see FIG. 2) than the center axis 301CX of the pixel separation portion 301. In addition, in the peripheral portion of the pixel area PA (see FIG.

And the second light shielding portion 313 </ b> B is formed so as to shift to the right side in FIG. 17). That is, so-called "pupil correction" is performed for the second light shielding portion 313B.

[0214]
Furthermore, in the present embodiment, the shift amount Dx between the center axis 313 BCX of the second light shielding portion 313 </ b> B and the central axis 301 </ b> CX of the pixel separation portion 301 is larger than that in the first embodiment The second light shielding portion 313 </ b> B is formed.

[0215]
However, in the present embodiment, unlike the second embodiment, the second light shielding portion 313 </ b> B is formed so as to be located within the range of the portion where the upper surface of the trench TR is located on the back surface (upper surface) of the semiconductor substrate 101 ing.

[0216]

Further, as shown in FIG. 17, the second light shielding portion 313B is formed such that the width HBS is narrower than the central portion in the peripheral portion of the pixel area PA.

The second light shielding portion 313 </ b> B is formed with a width HB similar to that in the first embodiment (see FIG. 5 (a)) in the center portion of the pixel region PA.

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[0217]
Thus, in the light-shielding layer 313 of the present embodiment, the upper surface of the first light-shielding portion 313 A is formed not to be covered with the second light-shielding portion 313 B but including the exposed portion as in the second embodiment .

[0218]
(B) Summary As described above, in the present embodiment, in the second light shielding portion 313B, the center of the second light shielding portion 313B is located closer to the center of the pixel separation portion 301 than the center of the pixel area PA , And is formed so as to be shifted to the peripheral side of the pixel area PA more.

[0219]
That is, in the present embodiment, "pupil correction" is performed for the second light shielding portion 313B.

[0220]
Therefore, in the present embodiment, as in the second embodiment, the image quality of the captured image can be improved.

[0221]

In the case of the second embodiment, as shown in FIG. 15A, in the peripheral portion of the pixel region PA, the second light shielding portion 313 B is located at a position other than the range of the portion where the upper surface of the trench TR is located are doing.

Therefore, in the second embodiment, the effective light-shielding width EH is a value obtained by adding the width HB of the second light-shielding portion 313 </ b> B and the width of the portion where the upper surface of the first light-shielding portion 313 </ b> A is exposed.

[0222]

On the other hand, in the present embodiment, as shown in FIG. 17, in the present embodiment, the second light shielding portion 313 </ b> B is formed such that a portion where the upper

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surface of the trench TR is located on the back surface (upper surface) of the semiconductor substrate 101 in the peripheral portion of the pixel region PA Of the outer circumference of the inner circumferential surface of the casing.

In the peripheral portion of the pixel region PA, the second light shielding portion 313B is formed so that the width HBS is narrower than the central portion.

Therefore, in the present embodiment, the effective light shielding width EH is a value obtained by adding the width HBS of the second light shielding portion 313 </ b> B and the width of the portion where the upper surface of the first light shielding portion 313 </ b> A is exposed.

[0223]

In this manner, in the peripheral portion of the pixel region PA, the width HBS of the second light shielding portion 313 </ b> B in the present embodiment is narrower than the width HB in the second embodiment.

Therefore, the effective light-shielding width EH is narrower in the case of this embodiment (see FIG. 17 (a)) than in the case of the second embodiment (see FIG. 15 (a)).

[0224]

In the case where the effective light shielding width EH is wide as in the case of the second embodiment, a decrease in sensitivity occurs.

Since this decrease in sensitivity occurs continuously in the pixel area PA, "shading" occurs in the captured image, which may cause deterioration in image quality. However, in the present embodiment, as described above, since the effective light-shielding width EH is narrower than that in the second embodiment, occurrence of "shading" can be suppressed and the image quality can be improved.

[0225]

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FIG. 18 is a cross-sectional view showing how incident light enters the solid-state imaging device in the third embodiment.

[0226]
FIG. 18 shows a peripheral portion (see FIGS. 1 and 2) of the pixel area PA similarly to FIG. 17 (a).

[0227]

As shown in FIG. 18, in the peripheral portion (see FIGS. 1 and 2) of the pixel region PA, when the width HBS of the second light shielding portion 313 B is narrow, the light L 5 due to the rounding advances to another pixel There are cases.

When the light reflected by the second light shielding portion 313 B enters into the second insulating film 311 B having a low refractive index, the wraparound occurs.

Then, since the first light-shielding portion 313 A and the second light-shielding portion 311 B surrounded by the first light-shielding portion 311 A function as an optical waveguide, there is a case where the light L 5 that has traveled around reaches other pixels P is there.

[0228]
For this reason, it is conceivable that the occurrence of "color mixture" increases due to this light L 5.

[0229]

However, in the present embodiment, since the first light shielding portion 313 </ b> A is provided in the trench TR, the first light shielding portion 313 </ b> A shields the light L <b> 5 and does not enter the other pixels P.

Therefore, in the present embodiment, the occurrence of "color mixing" can be effectively suppressed.

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[0230]

< 4 . Embodiment 4> (A) Apparatus Configuration, etc. FIG. 19 and FIG. 20 are diagrams showing essential parts of a solid-state imaging device in Embodiment 4. FIG.

[0231]

FIG. 19 is a cross-sectional view of the pixel separation section 301 similarly to FIG. 5. FIG. 20 is a top view of the pixel separating unit 301 similarly to FIG. 6. In FIGS. 19 and 20, (a) shows the pixel separation section 301 between the pixels P arranged in the central portion of the pixel area PA shown in FIG. 2, and shows the X 1 C - X 2 C section. On the other hand, (b) shows a pixel separation section 301 between pixels P arranged in the peripheral part of the pixel region PA shown in FIG. 2, and shows the X 1 S - X 2 S part.

[0232]

As shown in FIG. 19 and FIG. 20, in the present embodiment, as can be seen from comparison with FIGS. 5 and 6, a pixel separation diffusion layer 101 pb is further provided. Except for this point and related points, the present embodiment is similar to the first embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0233]

As shown in FIGS. 19 and 20, the pixel separation diffusion layer 101 pb is provided in the pixel separation section 301.

[0234]

The pixel separation diffusion layer 101 pb is formed by diffusing an impurity of a conductivity type different from that of the n type semiconductor region 101 n that accumulates the signal charge in the photodiode 21.

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Specifically, the pixel separation diffusion layer 101 pb is formed by ion-implanting a p-type impurity into the semiconductor substrate 101, and the pixel separation diffusion layer 101 pb of the photodiodes 21 (see FIG. 3) provided in each of the plurality of pixels P And electrically separates them.

[0235]

For example, the pixel separation diffusion layer 101 pb is formed under the following conditions. Impurity concentration: 5 × 10 <16> to 5 × 10 <18> cm <-3>

[0236]

As shown in FIGS. 19 and 20, in the center portion and the peripheral portion of the pixel area PA (see FIG. 2), the central axis in the horizontal direction x of the pixel separation diffusion layer 101 pb is located in the horizontal direction x of the pixel separation unit 301 And is formed to coincide with the center axis 301CX. Although not shown, in the vertical direction y, the pixel separation diffusion layer 101 pb is also formed so that the central axis in the vertical direction y coincides with the central axis in the vertical direction y of the pixel separation section 301.

[0237]
As in the first embodiment, a trench TR is provided in the semiconductor substrate 101 provided with the pixel separation diffusion layer 101 pb, and the insulating layer 311 and the light shielding layer 313 are provided inside the trench TR .

[0238]
That is, as shown in FIGS. 19 and 20, the second light-shielding portion 313 B is formed so that the center portion (in the case of (a)) of the pixel region PA (see FIG. 2) and the peripheral portion And in the case of FIG.

[0239]
(B) Summary As described above, in the present embodiment, in the second light shielding portion 313B, the center of the second light shielding portion 313B is located closer to the center of the pixel separation portion 301 than the center of the pixel area PA , And is formed so as to

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be shifted to the peripheral side of the pixel area PA more.

[0240]
That is, in the present embodiment, "pupil correction" is performed for the second light shielding portion 313B.

[0241]
In addition, since the pixel separation diffusion layer 101 pb is provided, separation between the plurality of pixels P can be suitably expressed.

[0242]
Therefore, in the present embodiment, as in the first embodiment, the image quality of the captured image can be improved.

[0243]

In the present embodiment, the case where the trench TR is provided in the semiconductor substrate 101 similarly to the first embodiment, and the insulating layer 311 and the light shielding layer 313 are provided inside the trench TR has been described, but the present invention is not limited to this.

As in the second and third embodiments, the light shielding layer 313 and the like may be formed.

[0244]

＜5.

FIFTH EMBODIMENT (A) Device Configuration, etc. FIG. 21 is a diagram showing a main part of a solid-state imaging device according to a fifth embodiment.

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[0245]

FIG. 21 shows a pixel separation unit 301 between pixels P arranged in the peripheral portion of the pixel area PA shown in FIG. 2, similar to FIG. 19 and FIG. 20 (b), showing the X 1 S - X 2 S portion ing.

FIG. 21A is a cross-sectional view of the pixel separation unit 301, and FIG. 21B is a top view of the pixel separation unit 301.

[0246]

As shown in FIG. 21, in the present embodiment, as can be seen from FIG. 19 and FIG. 20 (b), in the peripheral portion of the pixel region PA, the trench TR, the insulating layer 311, the light shielding layer 313 1 The position of the light shielding portion 313 A is different from that of the fourth embodiment.

Except for this point and related points, the present embodiment is similar to the fourth embodiment.

For this reason, descriptions of overlapping parts are omitted as appropriate.

[0247]
As shown in FIG. 21, the pixel separation section 301 is provided with a pixel separation diffusion layer 101 pb as in the fourth embodiment.

[0248]

In the pixel separation section 301, as shown in FIG. 21, a trench TR is provided on the back surface (upper surface) side of the semiconductor substrate 101.

In the pixel separation portion 301, the insulating layer 311 and the light shielding layer 313 are

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provided inside the trench TR.

[0249]
Specifically, as shown in FIG. 21, in the trench TR, unlike in the fourth embodiment, in the peripheral portion of the pixel region PA (see FIG. 2), the center axis 313 ACX in the horizontal direction x is divided by the pixel separation portion 301 Does not coincide with the center axis 301CX in the horizontal direction x of

[0250]

Here, as shown in FIG. 21, the center axis 313 ACX of the trench TR is located closer to the peripheral side of the pixel region PA (see FIG. 2) than the center axis 301 CX of the pixel separation portion 301.

The right side in FIG. 21), the trench TR is formed.

That is, the trench TR is formed so that the center axis 313 ACX of the trench TR and the center axis 301 CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x.

[0251]
In the present embodiment, the trench TR is formed in a portion where the pixel separation diffusion layer 101 pb is formed.

[0252]
As shown in FIG. 21, an insulating layer 311 is provided in the same manner as in the fourth embodiment so as to cover the inner surface of the trench TR.

[0253]

Here, as shown in FIG. 21, since the trench TR is shifted in the peripheral portion of the pixel region PA, the insulating layer 311 is also provided in a shifted position similarly to this.

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That is, the center axis 313 ACX of the insulating layer 311 in the trench TR is located closer to the periphery side (see FIG. 2) of the pixel region PA than the center axis 301 CX of the pixel separation portion 301.

An insulating layer 311 is formed so as to shift to the right side in FIG. 21).

[0254]
Then, as shown in FIG. 21, a light shielding layer 313 is provided so as to bury the inside of the trench TR covered with the insulating film 311.

[0255]
Here, the first light-shielding portion 313 A of the light-shielding layer 313 is different from the central portion (see FIG. 19A) of the pixel region PA (see FIG. 2) and the peripheral portion And in the case of FIG. 21 (a)) are formed at different positions.

[0256]

Specifically, as shown in FIG. 21, in the peripheral portion of the pixel region PA (see FIG. 2), the first light shielding portion 313 A is arranged such that the center axis 313 ACX in the horizontal direction x is shifted in the horizontal direction x of the pixel separation portion 301 And does not coincide with the center axis 301CX.

The central axis 313 ACX of the first light shielding portion 313 A is located closer to the peripheral side of the pixel region PA (see FIG. 2) than the central axis 301 CX of the pixel separation portion 301.

And the first light shielding portion 313 </ b> A is formed so as to shift to the right side in FIG. 21). That is, the first light shielding portion 313 A is formed so that the center axis 313 ACX of the first light shielding portion 313 A and the center axis 301 CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x .

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[0257]

The second light shielding portion 313 </ b> B of the light shielding layer 313 is formed such that the center portion (see FIG. 19A) of the pixel area PA (see FIG. 2) and the peripheral portion And in the case of FIG. 21 (a)) are formed at different positions. Here, the center axis 313 BCX of the second light shielding portion 313 B is located closer to the periphery side (see FIG. 2) of the pixel region PA than the center axis 301 CX of the pixel separation portion 301. And the first light shielding portion 313 </ b> A is formed so as to shift to the right side in FIG. 21). That is, the second light shielding portion 313 B is formed so that the center axis 313 BCX of the second light shielding portion 313 B and the center axis 301 CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x .

[0258]

As described above, in the present embodiment, so-called "pupil correction" is performed for both of the first light shielding portion 313 A and the second light shielding portion 313 B constituting the trench TR, the insulating layer 311, and the light shielding layer 313 . Here, in each pixel separating section 301, the light shielding layer 313 is formed so that the central axis 313 ACX of the first light shielding section 313 A and the central axis 313 BCX of the second light shielding section 313 B coincide with each other.

[0259]

In the present embodiment, the pixel region PA is divided into a central part and a peripheral part thereof, and in the central part of the pixel region PA, as shown in FIGS. 19 and 20 (a), each part such as the light shielding layer 313 is provided ing. On the other hand, in the peripheral portion of the pixel region PA, as shown in FIGS. 21A and 21B, various portions such as the light shielding layer 313 are provided.

[0260]

Besides this, with respect to each portion such as the light-shielding layer 313, the shift amount Dx between the center axes 313 ACX, 313 BCX of the respective portions and the central axis 301 CX of the pixel separation portion 301 along the direction from the center of the pixel area PA toward the periphery May be increased.

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[0261]

Specifically, with respect to the trench TR, the first light shielding portion 313 A, and the second light shielding portion 313 B provided in each of the pixel separation portions 301 between the plurality of pixels P arranged in the horizontal direction x, the pitch in the horizontal direction x thereof Is formed so as to be wider than the pitch of the pixel separation section 301.

Further, with respect to the trench TR, the first light-shielding portion 313 A, and the second light-shielding portion 313 B provided in each pixel separation portion 301 between the plurality of pixels P arranged in the vertical direction y, the pitch in the vertical direction y of the pixel separation portion 301 as shown in FIG.

[0262]

That is, with respect to the pixel separation portion 301 and the trench TR provided between the pair of pixels P in the pixel region PA, the trenches TR are formed so as to be aligned with the pixel region PA at a wider pitch than the pixel separation portion 301 . Further, with respect to the pixel separating portion 301 and the first light shielding portion 313 A provided between the pair of pixels P in the pixel region PA, the first light shielding portion 313 A has a wider pitch than the pixel separating portion 301 with the pixel area PA As shown in FIG. Further, with respect to the pixel separating portion 301 and the second light shielding portion 313 </ b> B provided between the pair of pixels P in the pixel area PA, the second light shielding portion 313 </ b> B has a wider pitch than the pixel separating portion 301, Formed to line up with PA. Further, the trench TR, the first light shielding portion 313 A, and the second light shielding portion 313 B are formed to be arranged at the same pitch in the pixel region PA.

[0263]

(B) Summary As described above, in the present embodiment, in the second light shielding portion 313B, the center of the second light shielding portion 313B is located closer to the center of the pixel separation portion 301 than the center of the pixel area PA , And is formed so as to be shifted to the peripheral side of the pixel area PA more.

[0264]

Therefore, in the present embodiment, as in the case of the fourth embodiment, the image quality

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of the captured image can be improved.

[0265]
In addition, in the present embodiment, so-called "pupil correction" is also performed for the trench TR, the insulating layer 311, and the first light shielding portion 313 A configuring the light shielding layer 313.

[0266]

In the case where the width of the second light shielding portion 313 B is narrowed in the peripheral portion of the pixel region PA as in the third embodiment (see FIG. 17), processing of the second light shielding portion 313 B may not be easy in some cases.

However, in the present embodiment, since the structure of the trench TR, the insulating layer 311, and the light shielding layer 313 is the same in the entire pixel region PA and the width of the second light shielding portion 313 B is not narrow, it is preferable to perform processing it can.

[0267]

In addition, in this embodiment, the trench TR is formed in the portion where the pixel separation diffusion layer 101 pb is formed.

For this reason, "pupil correction" can be performed without changing the sensitivity or the number of saturated electrons.

[0268]

＜6.

Sixth Embodiment (A) Device Configuration and the Like FIG. 22 is a diagram showing a main

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part of a solid-state imaging device according to a sixth embodiment.

[0269]

22, similarly to FIG. 21, the pixel separating unit 301 between the pixels P arranged in the peripheral portion of the pixel area PA shown in FIG. 2 and showing the X 1 S - X 2 S portion. FIG. 22A is a cross-sectional view of the pixel separation unit 301, and FIG. 22B is a top view of the pixel separation unit 301.

[0270]

As shown in FIG. 22, in this embodiment, as can be seen from comparison with FIG. 21, the position of the second light shielding portion 313 B of the light shielding layer 313 in the peripheral portion of the pixel region PA is different from that in the fifth embodiment. Except for this point and related points, the present embodiment is similar to the fifth embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0271]
As shown in FIG. 22, the first light shielding portion 313 A of the light shielding layer 313 is formed so as to fill the inside of the trench TR with the insulating layer 311 interposed therebetween in the same manner as in the case of Embodiment 5 (see FIG. 21) And is formed.

[0272]

Specifically, in the peripheral portion of the pixel region PA (see FIG. 2), the central axis 313 ACX of the first light shielding portion 313 A is located closer to the peripheral side of the pixel region PA (see FIG. 2 .

And the first light shielding portion 313 </ b> A is formed so as to shift to the right side in FIG. 21). That is, the first light shielding portion 313 A is formed so that the center axis 313 ACX of the first light shielding portion 313 A and the center axis 301 CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x .

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[0273]
Further, as shown in FIG. 22, the second light shielding portion 313 </ b> B is formed above the back surface (upper surface) of the semiconductor substrate 101 with the insulating layer 311 interposed therebetween.

[0274]

2), the center axis 313BCX of the second light shielding portion 313B is located closer to the periphery side of the pixel area PA (see FIG. 2) than the center axis 301CX of the pixel separation portion 301 .

And the second light shielding portion 313 </ b> B is formed so as to shift to the right side in FIG. 21). That is, the second light shielding portion 313B is formed so that the center axis 313BCX of the second light shielding portion 313B and the center axis 301CX of the pixel separation portion 301 are separated by a predetermined shift amount Dxb in the horizontal direction x .

[0275]

In the present embodiment, as shown in FIG. 22, a second light shielding portion 313 B is formed so that the shift amount Dxb is larger than in the case of the fifth embodiment (see FIG. 21). That is, as shown in FIG. 22, the second light shielding portion 313B is formed so that the shift amount Dxb of the second light shielding portion 313B is larger than the shift amount Dx of the first light shielding portion 313A.

[0276]
(B) Summary As described above, in the present embodiment, so-called "pupil correction" is performed on the first light shielding portion 313 A and the second light shielding portion 313 B configuring the trench TR, the insulating layer 311, and the light shielding layer 313 ing.

[0277]
Therefore, in the present embodiment, as in the case of the fifth embodiment, the image quality of the captured image can be improved.

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[0278]

In particular, in the present embodiment, in order to make the shift amount Dx between the center axis 313 BCX of the second light shielding portion 313 </ b> B and the central axis 301 </ b> CX of the pixel separation portion 301 larger than that in the fifth embodiment, A light shielding portion 313B is formed (see FIG. 22).

That is, the light-shielding layer 313 of the fifth embodiment is replaced by the light-shielding layer 313 of the second embodiment.

[0279]

Therefore, in this embodiment, as described in the second embodiment, the light can reach the photodiode 21 more efficiently than in the fifth embodiment.

Further, occurrence of "mixed color" and the like can be more effectively suppressed.

[0280]

In the present embodiment, the light-shielding layer 313 of Embodiment 5 is replaced with the light-shielding layer 313 of Embodiment 2, but the present invention is not limited to this. The light shielding layer 313 of the fifth embodiment may be replaced with the light shielding layer 313 of the third embodiment.

[0281]

＜7． Seventh Embodiment (A) Device Configuration and the Like FIG. 23 is a diagram showing a main part of a solid-state imaging device according to a seventh embodiment.

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[0282]

FIG. 23 shows the pixel separation section 301 between the pixels P arranged in the peripheral part of the pixel region PA shown in FIG. 2, similarly to FIG. 21, and shows the X 1 S - X 2 S part. FIG. 23 shows a cross section of the pixel separation section 301.

[0283]

As shown in FIG. 23, in the present embodiment, as can be seen from comparison with FIG. 21, in the peripheral portion of the pixel region PA, the positions of the trench TR, the insulating layer 311, and the light shielding layer 313 are the same as in Embodiment 5 and It is different. Except for this point and related points, the present embodiment is similar to the fifth embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0284]
As shown in FIG. 23, the pixel separation portion 301 is provided with a pixel separation diffusion layer 101 pb as in the fifth embodiment.

[0285]

23, in the pixel separating section 301, as shown in FIG. 23, the center axis 313 ACX of the trench TR and the center axis 301 CX of the pixel separating section 301 are separated from each other by a predetermined shift amount Dx in the horizontal direction x , A trench TR is formed.

Further, the center axis 313 ACX of the insulating layer 311 in the trench TR is located closer to the peripheral side of the pixel region PA (see FIG. 2) than the central axis 301 CX of the pixel separation portion 301. An insulating layer 311 is formed so as to shift to the right side in FIG. 21). The center axes 313 ACX and 313 BCX of the first light shielding portion 313 A and the second light shielding portion 313 B and the center axis 301 CX of the pixel separation portion 301 are formed so as to be separated by a predetermined shift amount Dx in the horizontal direction x There.

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[0286]
As described above, in the present embodiment, "pupil correction" is performed similarly for each of the first light-shielding portion 313 A and the second light-shielding portion 313 B constituting the trench TR, the insulating layer 311, and the light-shielding layer 313 There.

[0287]
However, in the present embodiment, as shown in FIG. 23, each part is formed so that the shift amount Dx is larger than in the case of the fifth embodiment.

[0288]
In this case, as shown in FIG. 23, the trench TR is formed so as to be positioned on a portion where the pixel separation diffusion layer 101 pb is formed and a portion other than that portion on the back surface (upper surface) of the semiconductor substrate 101 .

[0289]

Further, in this embodiment, the trench TR is formed so as to be located inside the p-type semiconductor region 101 pa provided on the back side of the n-type semiconductor region 101 n in the semiconductor substrate 101.

For example, the p-type semiconductor region 101 pa is formed so that the depth from the back surface of the semiconductor substrate 101 is 300 to 500 nm, and the trench TR is formed to a depth shallower than this depth.

[0290]
(8) Summary As described above, in the present embodiment, so-called "pupil correction" is performed on the first light shielding portion 313 A and the second light shielding portion 313 B configuring the trench TR, the insulating layer 311, and the light shielding layer 313 ing.

[0291]
Therefore, in the present embodiment, as in the case of the fifth embodiment, the image quality of the captured image can be improved.

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[0292]

The depletion layer of the photodiode 21 does not extend deep within the p-type semiconductor region 101 pa.

Therefore, in the range where the p-type semiconductor region 101 pa exists, the photoelectric conversion and the number of saturated electrons do not change.

Therefore, in the present embodiment, the trench TR is also formed in a portion other than the portion where the pixel separation diffusion layer 101 pb is formed, but the sensitivity and the number of saturated electrons do not change.

[0293]

＜8.

Embodiment 8> (A) Apparatus Configuration, etc. FIG. 24 is a diagram showing a main part of a solid-state imaging device in Embodiment 8. In FIG.

[0294]

FIG. 24 shows a pixel separation section 301 between pixels P arranged in the peripheral part of the pixel region PA shown in FIG. 2, similarly to FIG. 21, and shows the X 1 S - X 2 S part.

FIG. 24 shows a cross section of the pixel separation section 301.

[0295]

As shown in FIG. 24, in the present embodiment, as can be seen from comparison with FIG. 21, the trench TR in the peripheral portion of the pixel region PA is different from that in the fifth

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embodiment. Except for this point and related points, the present embodiment is similar to the fifth embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0296]
As shown in FIG. 24, the trench TR is formed so as to penetrate between the back surface (upper surface) and the front surface (lower surface) of the semiconductor substrate 101.

[0297]
As shown in FIG. 24, the insulating layer 311 is formed inside the trench TR so as to cover the side surface.

[0298]

As shown in FIG. 24, the first light shielding portion 313 A of the light shielding layer 313 is formed so as to bury the inside of the trench TR with the insulating layer 311 interposed therebetween.

Here, the first light shielding portion 313 </ b> A is formed so as to penetrate between the back surface (upper surface) and the front surface (lower surface) of the semiconductor substrate 101.

[0299]
The second light shielding portion 313 </ b> B is formed above the back surface (upper surface) of the semiconductor substrate 101 via the insulating layer 311.

[0300]
(B) Summary As described above, in the present embodiment, so-called "pupil correction" is performed on the first light shielding portion 313 A and the second light shielding portion 313 B configuring the trench TR, the insulating layer 311, and the light shielding layer 313 ing.

[0301]
Therefore, in the present embodiment, as in the case of the fifth embodiment, the image quality of the captured image can be improved.

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[0302]

In particular, in the present embodiment, the trench TR is formed so as to penetrate between the back surface (upper surface) and the front surface (lower surface) of the semiconductor substrate 101.

An insulating layer 311 and a light shielding layer 313 are formed inside the trench TR.

Like the trench TR, the first light shielding portion 313 A of the light shielding layer 313 is formed so as to penetrate between the back surface (upper surface) and the front surface (lower surface) of the semiconductor substrate 101.

[0303]

Therefore, in the present embodiment, it is possible to block light between the pixels P over the entire depth direction z of the semiconductor substrate 101.

Therefore, occurrence of "color mixing" or the like can be prevented more favorably.

[0304]

In the present embodiment, in the case of the fifth embodiment, the structure in which the trench TR penetrates is shown, but the configuration is not limited to this.

In another embodiment, the trench TR may be penetrated.

[0305]

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< 9 . Ninth Embodiment (A) Device Configuration and the Like FIG. 25 is a diagram showing a main part of a solid-state imaging device according to a ninth embodiment.

[0306]

FIG. 25 shows a pixel separation section 301 between pixels P arranged in the peripheral portion of the pixel area PA shown in FIG. 2, similarly to FIG. 24, showing the X 1 S - X 2 S portion. FIG. 25 shows a cross section of the pixel separation section 301.

[0307]

As shown in FIG. 25, in the present embodiment, as can be seen from comparison with FIG. 24, the first light shielding portion 313 A of the light shielding layer 313 is different from the case of the eighth embodiment in the peripheral portion of the pixel region PA. Except for this point and related points, the present embodiment is similar to the eighth embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0308]
As shown in FIG. 25, the first light shielding portion 313 A of the light shielding layer 313 penetrates between the back surface (upper surface) and the front surface (lower surface) of the semiconductor substrate 101.

[0309]

At the same time, the first light shielding portion 313 A of the light shielding layer 313 is provided so as to be connected to the wiring 111 h constituting the wiring layer 111.

Here, the first light shielding portion 313 </ b> A is connected to the wiring 111 h provided in the portion closest to the semiconductor substrate 101 among the plurality of wirings 111 h provided so as to be stacked in the wiring layer 111. As described above, the first light shielding portion 313 A is made of a metal material and has conductivity, so it is electrically connected to the wiring 111 h.

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[0310]

For the first light shielding portion 313 A of the light shielding layer 313, a voltage may be applied via the wiring 111 h. In the present embodiment, it is preferable to apply, for example, a negative voltage of -1.0 to 3.0 V to the first light shielding portion 313 </ b> A at the time of performing the imaging operation. As a result, holes are accumulated in the vicinity of the interface, so generation of dark current can be suitably prevented (see JP-A-2007-258684).

[0311]

(B) Summary As described above, in the present embodiment, so-called "pupil correction" is performed on the first light shielding portion 313 A and the second light shielding portion 313 B configuring the trench TR, the insulating layer 311, and the light shielding layer 313 ing.

[0312]

Therefore, in the present embodiment, as in the case of the fifth embodiment, the image quality of the captured image can be improved.

[0313]

In the present embodiment, the first light shielding portion 313 </ b> A penetrates between the surface on the back (upper surface) side and the surface (lower surface) side in the semiconductor substrate 101, and the insulating layer 111 z And is connected to the wiring 111 h provided therein.

Then, by applying a voltage to the first light shielding portion 313 A via the wiring 111 h, generation of dark current is suppressed.

Therefore, the image quality of the captured image can be further improved.

[0314]

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<10. Other> The implementation of the present technology is not limited to the above-described embodiment, and various modifications can be adopted.

[0315]

In the above embodiment, the case where the present technology is applied to a camera has been described, but the present invention is not limited thereto. The present technology may be applied to other electronic devices including a solid-state imaging device such as a scanner or a copier.

[0316]

In the above embodiment, the case where four types of transfer transistors, amplification transistors, selection transistors, and reset transistors are provided as pixel transistors has been described, but the present invention is not limited thereto. For example, the present invention may be applied to a case where three types of transfer transistors, amplification transistors, and reset transistors are provided as pixel transistors.

[0317]

In the above embodiment, a case where one transfer transistor, one amplification transistor, one selection transistor, and one reset transistor is provided for one photodiode has been described, but the present invention is not limited thereto. For example, the present invention may be applied to a case where one amplification transistor, one selection transistor, and one reset transistor are provided for each of a plurality of photodiodes.

[0318]
In addition to the CMOS type image sensor, the present technology may be applied to a CCD type image sensor.

[0319]

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Further, in the manufacture of the solid-state imaging device, when forming the trench TR in the portion formed by the pixel separation portion 301, the trench may be formed simultaneously with other portions.

For example, when the surface of a pad electrode (not shown) formed similarly to the wiring 111 h in the wiring layer 111 is exposed, a trench may be formed above the surface thereof in the same step as above. By doing so, it is possible to further improve the manufacturing efficiency.

[0320]

In addition, the insulating layer 311 of the above embodiment may be formed by a so-called LOCOS (Local Oxidation of Silicon) process. In other words, the insulating layer 311 may be formed by locally oxidizing the surface of the semiconductor substrate 101.

[0321]
In addition, each of the above embodiments may be appropriately combined.

[0322]
That is, the present technology can also take the following configuration.

[0323]
(1) A plurality of photoelectric conversion units are provided in the semiconductor substrate, corresponding to each of a plurality of pixels arranged in a pixel area of the semiconductor substrate with a space therebetween, and the photoelectric conversion unit receives incident light on a light receiving surface, And a pixel separation portion provided in the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein the pixel separation portion is formed on the incident surface side of the semiconductor substrate A first light shielding portion provided inside the trench, a second light shielding portion provided on the incident surface side surface of the semiconductor substrate, the second light shielding portion provided on the incident surface side of the first light shielding portion, , The second light shielding portion is formed such that the center of the second light shielding portion is shifted more toward the periphery of the pixel region than the center of the pixel separating portion around the center of the pixel region It is formed to be a solid Image apparatus.

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[0324]
(2) The pixel separating portion may further include an insulating layer covering the inner surface of the trench, and the first light shielding portion is formed so as to bury the inside of the trench with the insulating layer interposed therebetween. The solid-state imaging device according to (1) above.

[0325]

(3) The semiconductor device according to (1), wherein the insulating layer includes a first insulating film covering an inner surface of the trench and a second insulating film covering an inner surface of the trench with the first insulating film interposed therebetween, The solid-state imaging device according to (2), wherein a refractive index of the first insulating film is formed using a material between the semiconductor substrate and the second insulating film.

(4) The semiconductor device according to any one of (1) to (3), wherein the trench is formed such that the width of the incident surface side of the semiconductor substrate is larger than the width of the surface opposite to the incident surface, State image pickup device.

[0326]
(5) The semiconductor device according to any one of (1) to (4), wherein the second light shielding portion is formed so as to be located within a range of a portion where the trench is located on a surface of the semiconductor substrate on the incident surface side Wherein the solid-state imaging device is a solid-state imaging device.

[0327]
(6) The solid-state imaging device according to (5), wherein the second light shielding portion is formed so that a width of a peripheral portion of the pixel region is narrower than a width of a central portion of the pixel region.

[0328]
(7) The liquid crystal display device according to any one of (1) to (6) above, wherein the pixel separating unit includes a pixel separating / diffusing layer in which an impurity of a conductivity type different from that of a semiconductor region accumulating a signal charge in the photoelectric converting portion is diffused Of the solid-state imaging device.

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[0329]
(8) The trench is formed so that the center of the trench is more shifted toward the periphery of the pixel region than the center of the pixel isolation portion in the periphery of the center of the pixel region , The solid-state imaging device according to any one of the above (1) to (7).

[0330]
(9) In the first light-shielding portion, the center of the first light-shielding portion is more shifted toward the periphery of the pixel region than the center of the pixel separating portion around the center of the pixel region And the second electrode is formed so as to be in contact with the first electrode.

[0331]
(10) Each of the first light-shielding portion and the second light-shielding portion is formed such that the central axis of the first light-shielding portion and the central axis of the second light-shielding portion coincide with each other, 9).

[0332]
(11) The pixel separating unit may include a pixel separating / diffusing layer in which an impurity of a conductivity type different from that of a semiconductor region accumulating a signal charge in the photoelectric converting portion is diffused, and the trench is formed in the pixel The solid-state imaging device according to the above (8), wherein the solid-state imaging device is formed in a portion where a separation diffusion layer is formed.

[0333]
(12) The semiconductor device according to any one of (1) to (12), wherein the trench is formed so as to penetrate between the surface on the incident surface side and the surface on the opposite side from the incident surface in the semiconductor substrate).

[0334]
(13) The semiconductor device according to (12), wherein the first light shielding portion is formed so as to penetrate between the surface on the incident surface side and the surface on the opposite side to the incident surface, Of the solid-state imaging device.

[0335]

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(14) a pixel transistor which is provided on a surface of the semiconductor substrate opposite to the incident surface and outputs the signal charge generated by the photoelectric conversion portion as an electric signal; and And a wiring layer provided so as to cover the pixel transistor on a surface on the opposite side of the solid-state imaging device, the solid-state imaging device having the solid-state imaging device according to any one of (1) to (13).

(15) The semiconductor light-emitting device according to (15), wherein the first light-shielding portion penetrates between the surface on the incident surface side and the surface on the opposite side from the incident surface, in the semiconductor substrate, (14), wherein the solid-state imaging device is connected to the wiring.

[0336]
(16) The liquid crystal display device according to (16), further comprising a color filter through which the incident light is transmitted to the light receiving surface, wherein the color filter includes a plurality of filter layers having high transmittance for light in different wavelength ranges, (1) to (15), wherein the plurality of pixels are arranged adjacent to each other.

[0337]
(17) Forming a plurality of photoelectric conversion portions provided inside the semiconductor substrate so as to correspond to each of a plurality of pixels aligned in the pixel region of the semiconductor substrate with photoelectric conversion portions for receiving incident light on the light receiving surface And a pixel separation portion forming step of providing a pixel separation portion in the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein in the pixel separation portion forming step, A first light shielding portion is provided inside the trench formed on the incident surface side in the pixel separation portion of the first light shielding portion on the incident surface side of the semiconductor substrate, Wherein in the step of forming the second light shielding portion, at least in the periphery of the center of the pixel region, the center of the second light shielding portion is located closer to the center of the pixel separating portion than the second light shielding portion, region To shift more toward the periphery, forming the second light-shielding portion, the manufacturing method of the solid-state imaging device.

[0338]
(18) A photoelectric conversion device comprising: a plurality of photoelectric conversion units provided in the semiconductor substrate, each photoelectric conversion unit receiving incident

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light on a light receiving surface, corresponding to each of a plurality of pixels aligned in a pixel area of a semiconductor substrate with a spacing therebetween; And a pixel separation portion provided in the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein the pixel separation portion is formed on the incident surface side of the semiconductor substrate A first light shielding portion provided inside the trench, a second light shielding portion provided on the incident surface side surface of the semiconductor substrate, the second light shielding portion provided on the incident surface side of the first light shielding portion, , The second light shielding portion is formed such that the center of the second light shielding portion is shifted more toward the periphery of the pixel region than the center of the pixel separating portion around the center of the pixel region It is formed so that electricity Equipment.

[0339]

In the above embodiment, the photodiode 21 is an example of a photoelectric conversion unit.

Further, in the above embodiment, the camera 40 is an example of an electronic device.

[0340]

17: External output circuit 17a: AGC circuit 17b: ADC circuit 18: Timing generator 19: Shutter driving circuit 1: Solid state imaging device 13: Vertical driving circuit 14: Column circuit 15: Horizontal driving circuit 17: External output circuit 17: 21: photodiode, 22: transfer transistor, 23: amplification transistor, 24: selection transistor, 25: reset transistor, 26: transfer line, 27: vertical signal line, 28: address line, 29: reset line, 40: A p-type semiconductor region; 101 pc: a p-type semiconductor region; 111: a wiring layer; 111 h: a wiring , 111 z: an insulating layer, 301: a pixel separation portion, 311: an insulating layer, 311 A: a first insulating film, 311 B: a CF: color filter, CFB: green filter layer, CFR: green filter layer, CFR: red filter layer, FD: floating diffusions , H: incident light, HM: hard mask, HT: flattening film, I: constant current source, JS: light receiving surface, ML: microlens, P: pixel, PA: pixel region, PS: imaging surface, SA: peripheral Region, SS: support substrate, SZ, insulating film, TR: trench, Tr: pixel transistor

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CLAIMS JP2012169530

1.
A plurality of photoelectric conversion units provided inside the semiconductor substrate corresponding to each of a plurality of pixels aligned in a pixel region of the semiconductor substrate with a space therebetween and receiving incident light on a light receiving surface; And a pixel separating portion which is provided in the semiconductor substrate so as to be interposed between the plurality of pixels in the semiconductor substrate, wherein the pixel separating portion is formed in a portion of a trench formed on the incident surface side of the semiconductor substrate At least a first light shielding portion provided in the interior and a second light shielding portion provided on the incident surface side surface of the semiconductor substrate and provided on the incident surface side of the first light shielding portion , The second light shielding portion is formed such that the center of the second light shielding portion is shifted more toward the periphery of the pixel region from the center of the pixel separation portion in the periphery than the center of the pixel region Solid state imaging device formed .

2.
2. The semiconductor device according to claim 1, wherein the pixel separating portion further includes an insulating layer covering an inner surface of the trench, and the first light shielding portion is formed so as to bury the inside of the trench via the insulating layer. Of the solid-state imaging device.

3.
Wherein the insulating layer includes a first insulating film covering an inner surface of the trench and a second insulating film covering an inner surface of the trench with the first

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insulating film interposed therebetween, The solid-state imaging device according to claim 2, wherein the film is formed using a material having a refractive index between the semiconductor substrate and the second insulating film.

4.

The solid-state imaging device according to claim 1, wherein the trench is formed such that a width of the semiconductor substrate on the incident surface side is larger than a width on a surface side opposite to the incident surface.

5.

2. The solid-state imaging device according to claim 1, wherein the second light shielding portion is formed so as to be located within a range of a portion where the trench is located on a surface of the semiconductor substrate on the incident surface side.

6.

6. The solid-state imaging device according to claim 5, wherein the second light-shielding portion is formed so that a width in a peripheral portion of the pixel region is narrower than a width in a central portion of the pixel region.

7.

2. The solid-state imaging device according to claim 1, wherein the pixel separation unit includes a pixel separation diffusion layer in which an impurity having a conductivity type different from that of a semiconductor region in which the signal charge is accumulated in the photoelectric conversion unit is diffused.

8.

The trench is formed such that the center of the trench is shifted more toward the periphery of the pixel region than the center of the pixel isolation portion in the periphery of the center of the pixel region Wherein the solid-state imaging device is a solid-state imaging device.

9.

The first light-shielding portion is formed such that the center of the first light-shielding portion is shifted more toward the periphery of the pixel region with respect to the center of the pixel separation portion in the periphery than the center of the pixel region State image pickup device according to claim 8.

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10.
Each of the first light-shielding portion and the second light-shielding portion is formed such that a central axis of the first light-shielding portion and a central axis of the second light-shielding portion coincide with each other. .

11.
Wherein the pixel separating unit includes a pixel separation diffusion layer in which an impurity of a conductivity type different from that of a semiconductor region in which the signal charge is accumulated in the photoelectric conversion unit is diffused and the trench is formed in the pixel separation diffusion layer Is formed in a portion where the first electrode and the second electrode are formed.

12.
The solid-state imaging device according to claim 1, wherein the trench penetrates between a surface on the incident surface side and a surface on the opposite side to the incident surface in the semiconductor substrate.

13.
The solid state image pickup device according to claim 12, wherein the first light shielding portion is formed so as to penetrate between a surface on the incident surface side and a surface on the opposite side from the incident surface in the semiconductor substrate .

14.
A pixel transistor which is provided on a surface of the semiconductor substrate opposite to the incident surface and outputs a signal charge generated by the photoelectric conversion portion as an electric signal; a pixel transistor provided on a side of the semiconductor substrate opposite to the incident surface And a wiring layer provided so as to cover the pixel transistor in a plane of the solid-state imaging device.

15.
The first light-shielding portion penetrates between the surface on the incident surface side and the surface on the opposite side to the incident surface in the semiconductor substrate, and the first light-shielding portion penetrates through the wiring provided in the insulating layer in the wiring layer 15. The solid-state imaging device according to claim 14, being connected.

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16.

Wherein the plurality of types of filter layers having high transmittance for light in different wavelength ranges are adjacent to each other corresponding to each of the plurality of pixels, And the second light receiving element is arranged in the second direction.

17.

A photoelectric conversion portion forming step in which a plurality of photoelectric conversion portions for receiving incident light on a light receiving surface are provided inside the semiconductor substrate so as to correspond to each of a plurality of pixels aligned in a pixel region of the semiconductor substrate, And a pixel separation portion forming step of providing a pixel separation portion in the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein in the pixel separation portion forming step, A first light shielding portion is provided inside the trench formed on the incident surface side in the separation portion and a second light shielding portion is formed on the incident surface side surface of the semiconductor substrate and on the incident surface side of the first light shielding portion, Wherein in the step of forming the second light shielding portion, the center of the second light shielding portion is located closer to the center of the pixel separation portion than the center of the pixel region in the vicinity of the pixel region of To to shift more to form the second light-shielding portion, the manufacturing method of the solid-state imaging device.

18.

A plurality of photoelectric conversion units provided inside the semiconductor substrate corresponding to each of a plurality of pixels aligned in a pixel region of the semiconductor substrate with a space therebetween and receiving incident light on a light receiving surface; And a pixel separating portion which is provided in the semiconductor substrate so as to be interposed between the plurality of pixels in the semiconductor substrate, wherein the pixel separating portion is formed in a portion of a trench formed on the incident surface side of the semiconductor substrate At least a first light shielding portion provided in the interior and a second light shielding portion provided on the incident surface side surface of the semiconductor substrate and provided on the incident surface side of the first light shielding portion , The second light shielding portion is formed such that the center of the second light shielding portion is shifted more toward the periphery of the pixel region from the center of the pixel separation portion in the periphery than the center of the pixel region The electronic equipment being formed.

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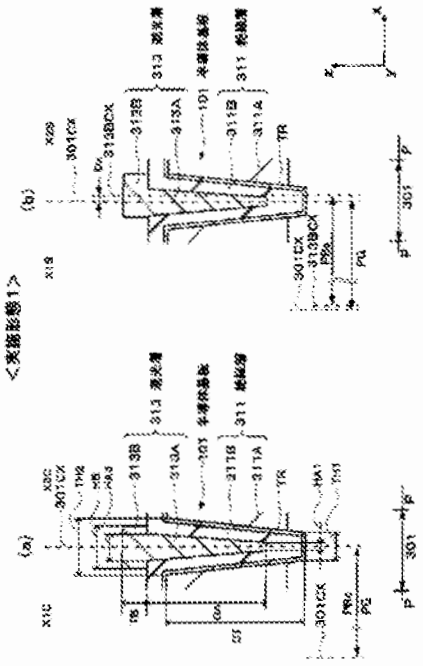
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(54)【発明の名称】固体撮像装置、および、その製造方法、電子機器

(57)【要約】
【課題】撮像画像の画像品質を向上させる。
【解決手段】半導体基板１０１の画素分離部３０１に形成されたトレンチＴＲの内部に第１遮光部３１３Ａを設ける。これと共に、その第１遮光部３１３Ａの上面側に第２遮光部３１３Ｂを設ける。ここでは、画素領域ＰＡの中心よりも周辺において、第２遮光部３１３Ｂの中心が、画素分離部３０１の中心に対して、画素領域ＰＡの周辺の側へ多くシフトするように、第２遮光部３１３Ｂを形成する。つまり、少なくとも第２遮光部について「瞳補正」を実施する。
【選択図】図５



【特許請求の範囲】
【請求項１】
半導体基板の画素領域に間を隔てて並ぶ複数の画素のそれぞれに対応して、複数が前記半導体基板の内部に設けられており、入射光を受光面で受光する光電変換部と、
前記画素領域において前記複数の画素の間に介在するように前記半導体基板の内部に設けられている画素分離部と
を有し、
前記画素分離部は、
前記半導体基板の前記入射面側に形成されたトレンチの内部に設けられている第１遮光部と、
前記半導体基板の前記入射面側の面上であって、前記第１遮光部の前記入射面側に設けられている第２遮光部と
を少なくとも含み、
前記第２遮光部は、前記画素領域の中心よりも周辺において、当該第２遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように形成されている、
固体撮像装置。
【請求項２】
前記画素分離部は、
前記トレンチの内部の面を被覆する絶縁層
を更に含み、
前記第１遮光部は、前記絶縁層を介して前記トレンチの内部を埋め込むように形成されている、
請求項１に記載の固体撮像装置。
【請求項３】
前記絶縁層は、
前記トレンチの内側の面を被覆する第１絶縁膜と、
前記第１絶縁膜を介在して前記トレンチの内側の面を被覆する第２絶縁膜と
を含み、
前記第１絶縁膜は、屈折率が前記半導体基板と前記第２絶縁膜との間の材料を用いて形成されている、
請求項２に記載の固体撮像装置。
【請求項４】
前記トレンチは、前記半導体基板において前記入射面側の幅が、前記入射面と反対側の面の側の幅よりも広くなるように形成されている、
請求項１に記載の固体撮像装置。
【請求項５】
前記第２遮光部は、前記半導体基板の前記入射面側の面において、前記トレンチが位置する部分の範囲内に位置するように形成されている、
請求項１に記載の固体撮像装置。
【請求項６】
前記第２遮光部は、前記画素領域の周辺部分における幅が、前記画素領域の中心部分における幅よりも狭くなるように形成されている、
請求項５に記載の固体撮像装置。
【請求項７】
前記画素分離部は、
前記光電変換部において信号電荷を蓄積する半導体領域とは異なる導電型の不純物が拡散された画素分離拡散層
を有する、
請求項１に記載の固体撮像装置。

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【請求項８】
前記トレンチは、前記画素領域の中心よりも周辺において、当該トレンチの中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように形成されている、
請求項１に記載の固体撮像装置。
【請求項９】
前記第１遮光部は、前記画素領域の中心よりも周辺において、当該第１遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように形成されている、
請求項８に記載の固体撮像装置。
【請求項１０】
前記第１遮光部と前記第２遮光部とのそれぞれは、当該第１遮光部の中心軸と当該第２遮光部の中心軸とが互いに一致するように形成されている、
請求項９に記載の固体撮像装置。
【請求項１１】
前記画素分離部は、
前記光電変換部において信号電荷を蓄積する半導体領域とは異なる導電型の不純物が拡散された画素分離拡散層
を有し、
前記トレンチは、前記半導体基板において前記画素分離拡散層が形成された部分に形成されている、
請求項８に記載の固体撮像装置。
【請求項１２】
前記トレンチは、前記半導体基板において、前記入射面の側の面と、前記入射面とは反対側の面との間を貫通するように形成されている、
請求項１に記載の固体撮像装置。
【請求項１３】
前記第１遮光部は、前記半導体基板において、前記入射面の側の面と、前記入射面とは反対側の面との間を貫通するように形成されている、
請求項１２に記載の固体撮像装置。
【請求項１４】
前記半導体基板において前記入射面とは反対側の面に設けられており、前記光電変換部で生成された信号電荷を電気信号として出力する画素トランジスタと、
前記半導体基板において前記入射面とは反対側の面にて、前記画素トランジスタを被覆するように設けられている配線層と
を有する、
請求項１に記載の固体撮像装置。
【請求項１５】
前記第１遮光部は、前記半導体基板において、前記入射面の側の面と、前記入射面とは反対側の面との間を貫通し、前記配線層において絶縁層中に設けられた配線に接続されている、
請求項１４に記載の固体撮像装置。
【請求項１６】
前記入射光が前記受光面へ透過するカラーフィルタ
を含み、
前記カラーフィルタは、
互いに異なる波長範囲の光について透過率が高い複数種のフィルタ層が、前記複数の画素のそれぞれに対応して互いに隣接して配置されている、
請求項１に記載の固体撮像装置。
【請求項１７】

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入射光を受光面で受光する光電変換部を、半導体基板の画素領域に間を隔てて並ぶ複数の画素のそれぞれに対応するように、前記半導体基板の内部に複数設ける光電変換部形成工程と、

前記画素領域において前記複数の画素の間に介在するように前記半導体基板の内部に画素分離部を設ける画素分離部形成工程と

を有し、

前記画素分離部形成工程では、

前記半導体基板の前記画素分離部において前記入射面側に形成されたトレンチの内部に第１遮光部を設けると共に、前記半導体基板の前記入射面側の面上であって前記第１遮光部の前記入射面側に第２遮光部を少なくとも設け、

前記第２遮光部の形成工程では、前記画素領域の中心よりも周辺において、前記第２遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように、前記第２遮光部を形成する、

固体撮像装置の製造方法。

【請求項１８】

半導体基板の画素領域に間を隔てて並ぶ複数の画素のそれぞれに対応して、複数が前記半導体基板の内部に設けられており、入射光を受光面で受光する光電変換部と、

前記画素領域において前記複数の画素の間に介在するように前記半導体基板の内部に設けられている画素分離部と

を有し、

前記画素分離部は、

前記半導体基板の前記入射面側に形成されたトレンチの内部に設けられている第１遮光部と、

前記半導体基板の前記入射面側の面上であって、前記第１遮光部の前記入射面側に設けられている第２遮光部と

を少なくとも含み、

前記第２遮光部は、前記画素領域の中心よりも周辺において、当該第２遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように形成されている、

電子機器。

【発明の詳細な説明】

【技術分野】

【０００１】

本技術は、固体撮像装置、および、その製造方法、電子機器に関する。

【背景技術】

【０００２】

デジタルビデオカメラ、デジタルスチルカメラなどの電子機器は、固体撮像装置を含む。たとえば、固体撮像装置として、ＣＭＯＳ（Ｃｏｍｐｌｅｍｅｎｔａｒｙ Ｍｅｔａｌ Ｏｘｉｄｅ Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）型イメージセンサ、ＣＣＤ（Ｃｈａｒｇｅ Ｃｏｕｐｌｅｄ Ｄｅｖｉｃｅ）型イメージセンサを含む。

【０００３】

固体撮像装置は、基板の画素領域に複数の画素が配列されている。各画素においては、光電変換部が設けられている。光電変換部は、たとえば、フォトダイオードであり、入射光を受光面で受光し光電変換することによって、信号電荷を生成する。

【０００４】

固体撮像装置のうち、ＣＣＤ型イメージセンサは、画素領域において、垂直方向に並ぶ複数の画素の列の間に、垂直転送部が設けられている。垂直転送部は、垂直転送チャネル領域にゲート絶縁膜を介して対面するように複数の転送電極が設けられており、電荷読出し部によって光電変換部から読み出された信号電荷を、垂直方向へ転送するように構成されている。

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【０００５】
これに対して、ＣＭＯＳ型イメージセンサは、光電変換部のほかに、画素トランジスタを含むように、画素が構成されている。画素トランジスタは、光電変換部で生成された信号電荷を読み出して，信号線へ電気信号として出力するように構成されている。
【０００６】
固体撮像装置では、一般に、基板において、複数の配線が積層された多層配線層が設けられた表面側に設けられており、その表面側から入射する光を、光電変換部が受光面で受光する。
【０００７】
「表面照射型」の場合には、マイクロレンズと受光面との間に、多層配線層が介在し集光面と受光面との間の距離が長い。このため、受光面に対して傾斜して光が入射したときには、その多層配線層に含まれる配線に、その光が遮られて、受光面に到達しない場合がある。よって、感度を向上させることが困難な場合がある。
【０００８】
このため、基板において多層配線層が設けられた表面とは反対側の裏面側から入射する光を、光電変換部が受光する「裏面照射型」が提案されている。
【０００９】
固体撮像装置においては、一の画素に入射した入射光が、その一の画素のフォトダイオードに入射せずに、隣接する他の画素のフォトダイオードに入射する場合がある。このため、このような光学的な現象に起因して信号にノイズが含まれることになり、撮像画像の画像品質が低下する場合がある。たとえば、カラー画像を撮像する場合において、入射光が受光面に対して傾斜して入射したときには、その直下の受光面に入射せずに、本来、他の色の着色光を受光する他の受光面へ入射する場合がある。このため、いわゆる「混色」が発生して、撮像したカラー画像において色調のズレが生じ、画像品質が低下する場合がある。このような不具合の発生を抑制するために、複数の画素の間に遮光膜を設けている（たとえば、特許文献１，２参照）。
【００１０】
また、複数の画素が配列された画素領域の中心部分においては、外付けの光学系を介して入射する主光線の角度が、受光面に対して、ほぼ垂直であるのに対して、その画素領域の周辺部分においては、入射する主光線の角度が傾斜している。このため，撮像画像の中心部分が明るい画像になり、周辺部分が暗い画像になる場合がある。つまり、いわゆるシェーディング現象が発生して、画像品質が低下する場合がある。このような不具合を改善するために、「瞳補正」と称して、オンチップレンズ等の配置を補正することが、実施されている。具体的には、画素領域の周辺において配置されるオンチップレンズの位置が、受光面に対して、画素領域の中心側へシフトするように、オンチップレンズを設けることが実施されている。たとえば、画素領域にて並ぶ複数の光電変換部のピッチよりも、オンチップレンズのピッチが狭くなるように、各部を配置している（たとえば、特許文献３などを参照）。
【００１１】
また，固体撮像装置では、光電変換部が設けられた半導体基板の界面準位に起因して暗電流が発生することを抑制して画像品質を向上させるために、光電変換部をＨＡＤ（Ｈｏｌｅ　Ａｃｃｕｍｕｌａｔｉｏｎ　Ｄｉｏｄｅ）構造にすることが提案されている。ＨＡＤ構造では、ｎ型の電荷蓄積領域の受光面上に正電荷蓄積（ホール）蓄積領域を形成することで、暗電流の発生を抑制している。そして、この正電荷蓄積領域を光電変換部の界面部分に形成するために、「負の固定電荷を有する膜」をピニング層として設けて、暗電流の発生を抑制することが提案されている。たとえば、酸化ハフニウム膜（HfO_2膜）のような高誘電体膜を、「負の固定電荷を有する膜」として用いている（たとえば，特許文献４などを参照）。
【００１２】
また、暗電流の発生を抑制するために、「裏面照射型」の表面側に、制御ゲートを設け

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、その制御ゲートに負電圧を印加することが提案されている（たとえば、特許文献５などを参照）。その他、暗電流の発生を抑制するために、光を受光する受光面部分が開口した金属遮光膜に負電圧を印加することが提案されている（たとえば、特許文献６などを参照）

【００１３】

このように、固体撮像装置においては、撮像画像の画像品質を向上させるために、種々の技術が提案されている。

【先行技術文献】

【特許文献】

【００１４】

【特許文献１】特開２０１０－１０９２９５号公報
【特許文献２】特開２０１０－１８６８１８号公報
【特許文献３】特許３５５１４３７号
【特許文献４】特開２００８－３０６１５４号公報
【特許文献５】特開２００７－２５８６８４号公報
【特許文献６】特開平５－２７５６７３号公報

【発明の概要】

【発明が解決しようとする課題】

【００１５】

固体撮像装置においては、さらに、撮像画像の画像品質などを向上させることが望まれている。

【００１６】

したがって、本技術は、撮像画像の画像品質などを向上可能な、固体撮像装置、および、その製造方法、電子機器を提供する。

【課題を解決するための手段】

【００１７】

本技術の固体撮像装置および電子機器は、半導体基板の画素領域に間を隔てて並ぶ複数の画素のそれぞれに対応して、複数が前記半導体基板の内部に設けられており、入射光を受光面で受光する光電変換部と、前記画素領域において前記複数の画素の間に介在するように前記半導体基板の内部に設けられている画素分離部とを有し、前記画素分離部は、前記半導体基板の前記入射面側に形成されたトレンチの内部に設けられている第１遮光部と、前記半導体基板の前記入射面側の面上であって、前記第１遮光部の前記入射面側に設けられている第２遮光部とを少なくとも含み、前記第２遮光部は、前記画素領域の中心よりも周辺において、当該第２遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように形成されている。

【００１８】

本技術の固体撮像装置の製造方法は、入射光を受光面で受光する光電変換部を、半導体基板の画素領域に間を隔てて並ぶ複数の画素のそれぞれに対応するように、前記半導体基板の内部に複数設ける光電変換部形成工程と、前記画素領域において前記複数の画素の間に介在するように前記半導体基板の内部に画素分離部を設ける画素分離部形成工程とを有し、前記画素分離部形成工程では、前記半導体基板の前記画素分離部において前記入射面側に形成されたトレンチの内部に第１遮光部を設けると共に、前記半導体基板の前記入射面側の面上であって前記第１遮光部の前記入射面側に第２遮光部を少なくとも設け、前記第２遮光部の形成工程では、前記画素領域の中心よりも周辺において、前記第２遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように、前記第２遮光部を形成する。

【００１９】

本技術においては、半導体基板の画素分離部に形成されたトレンチの内部に第１遮光部を設けると共に、その第１遮光部の入射面側に第２遮光部を設ける。ここでは、画素領域の中心よりも周辺において、第２遮光部の中心が、画素分離部の中心に対して、画素領域

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の周辺の側へ多くシフトするように、第２遮光部を形成する。つまり、すくなくとも第２遮光部について「瞳補正」を実施する。

【発明の効果】

【００２０】

本技術によれば、撮像画像の画像品質等を向上可能な、固体撮像装置、および、その製造方法、電子機器を提供することができる。

【図面の簡単な説明】

【００２１】

【図１】図１は、実施形態１において、カメラの構成を示す構成図である。

【図２】図２は、実施形態１において、固体撮像装置の全体構成を示す図である。

【図３】図３は、実施形態１において、固体撮像装置の要部を示す図である。

【図４】図４は、実施形態１において、固体撮像装置の要部を示す図である。

【図５】図５は、実施形態１において、固体撮像装置の要部を示す図である。

【図６】図６は、実施形態１において、固体撮像装置の要部を示す図である。

【図７】図７は、実施形態１において、固体撮像装置の要部を示す図である。

【図８】図８は、実施形態１において、撮像を実施する際に、画素Ｐの画素トランジスタＴｒへ送信する制御信号を示すタイミングチャートである。

【図９】図９は、実施形態１において、固体撮像装置の製造方法を示す図である。

【図１０】図１０は、実施形態１において、固体撮像装置の製造方法を示す図である。

【図１１】図１１は、実施形態１において、固体撮像装置の製造方法を示す図である。

【図１２】図１２は、実施形態１において、固体撮像装置の製造方法を示す図である。

【図１３】図１３は、実施形態１において、固体撮像装置の製造方法を示す図である。

【図１４】図１４は、実施形態１において、固体撮像装置に入射光が入射する様子を示す断面図である。

【図１５】図１５は、実施形態２において、固体撮像装置の要部を示す図である。

【図１６】図１６は、実施形態２において、固体撮像装置に入射光が入射する様子を示す断面図である。

【図１７】図１７は、実施形態３において、固体撮像装置の要部を示す図である。

【図１８】図１８は、実施形態３において、固体撮像装置に入射光が入射する様子を示す断面図である。

【図１９】図１９は、実施形態４において、固体撮像装置の要部を示す図である。

【図２０】図２０は、実施形態４において、固体撮像装置の要部を示す図である。

【図２１】図２１は、実施形態５において、固体撮像装置の要部を示す図である。

【図２２】図２２は、実施形態６において、固体撮像装置の要部を示す図である。

【図２３】図２３は、実施形態７において、固体撮像装置の要部を示す図である。

【図２４】図２４は、実施形態８において、固体撮像装置の要部を示す図である。

【図２５】図２５は、実施形態９において、固体撮像装置の要部を示す図である。

【発明を実施するための形態】

【００２２】

実施形態について、図面を参照して説明する。

【００２３】

なお、説明は、下記の順序で行う。

１．実施形態１（画素分離部の遮光膜の上部を「瞳補正」する場合）

２．実施形態２（画素分離部の遮光膜の上部を「瞳補正」する場合）

３．実施形態３（画素分離部の遮光膜の上部を「瞳補正」する場合）

４．実施形態４（画素分離部に拡散層を設ける場合）

５．実施形態５（画素分離部の遮光膜の上部および下部を「瞳補正」する場合）

６．実施形態６（画素分離部の遮光膜の上部および下部を「瞳補正」する場合）

７．実施形態７（画素分離部の遮光膜の上部および下部を「瞳補正」する場合）

８．実施形態８（画素分離部の遮光膜を貫通させる場合）

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９．実施形態９（画素分離部の遮光膜を貫通させる場合）
１０．その他
【００２４】
＜１．実施形態１＞
（Ａ）装置構成
（Ａ－１）カメラの要部構成
図１は、実施形態１において、カメラの構成を示す構成図である。
【００２５】
図１に示すように、カメラ４０は、固体撮像装置１と、光学系４２と、制御部４３と、信号処理部４４とを有する。
【００２６】
カメラ４０において、固体撮像装置１は、光学系４２を介して被写体像として入射する入射光Ｈを撮像面ＰＳで受光し光電変換して信号電荷を生成する。ここでは、固体撮像装置１は、制御部４３から出力される制御信号に基づいて駆動し、生成した信号電荷を読み出して、電気信号を出力する。
【００２７】
光学系４２は、結像レンズや絞りなどの光学部材を含み、入射光Ｈを、固体撮像装置１の撮像面ＰＳへ集光するように配置されている。
【００２８】
制御部４３は、各種の制御信号を固体撮像装置１と信号処理部４４とに出力し、固体撮像装置１と信号処理部４４とを制御して駆動させる。
【００２９】
信号処理部４４は、固体撮像装置１から出力された電気信号をローデータとして信号処理を実施することによって、被写体像についてデジタル画像を生成するように構成されている。
【００３０】
本実施形態では、図１に示すように、撮像面ＰＳの中心部分においては、光学系４２から出射される光線Ｈ１が、撮像面ＰＳに対して垂直な角度で、入射光Ｈとして入射する。一方で、撮像面ＰＳの周辺部分においては、主光線Ｈ２が、撮像面ＰＳに対して垂直な方向に対して傾斜した角度で、入射光Ｈとして入射する。ここでは、撮像面ＰＳの中心から周囲へ向かって入射光の主光線Ｈ２が傾斜する。これは、後述の光学系４２を構成する絞りによって形成される射出瞳距離が有限であることに起因する。
【００３１】
（Ａ－２）固体撮像装置の要部構成
固体撮像装置１の全体構成について説明する。
【００３２】
図２は、実施形態１において、固体撮像装置の全体構成を示す図である。
【００３３】
本実施形態の固体撮像装置１は、ＣＭＯＳ型イメージセンサであり、図２に示すように、半導体基板１０１を含む。半導体基板１０１においては、たとえば、単結晶シリコン基板が薄膜化されたものであり、画素領域ＰＡと、周辺領域ＳＡとが面に設けられている。
【００３４】
画素領域ＰＡは、図２に示すように、矩形形状であり、複数の画素Ｐが水平方向ｘと垂直方向ｙとのそれぞれに等間隔で配置されている。つまり、画素Ｐがマトリクス状に並んでいる。
【００３５】
画素領域ＰＡにおいて、画素Ｐは、入射光を受光して信号電荷を生成するように構成されている。そして、その生成した信号電荷が、画素トランジスタ（図示なし）によって読み出されて電気信号として出力される。画素Ｐの詳細な構成については、後述する。
【００３６】

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周辺領域ＳＡは、図２に示すように、画素領域ＰＡの周囲に位置している。そして、この周辺領域ＳＡにおいては、周辺回路が設けられている。

【００３７】

具体的には、図２に示すように、垂直駆動回路１３と、カラム回路１４と、水平駆動回路１５と、外部出力回路１７と、タイミングジェネレータ（ＴＧ）１８と、シャッター駆動回路１９とが、周辺回路として設けられている。

【００３８】

垂直駆動回路１３は、図２に示すように、周辺領域ＳＡにおいて、画素領域ＰＡの側部に設けられており、画素領域ＰＡの画素Ｐを行単位で選択して駆動させるように構成されている。

【００３９】

カラム回路１４は、図２に示すように、周辺領域ＳＡにおいて、画素領域ＰＡの下端部に設けられており、列単位で画素Ｐから出力される信号について信号処理を実施する。ここでは、カラム回路１４は、ＣＤＳ（Ｃｏｒｒｅｌａｔｅｄ Ｄｏｕｂｌｅ Ｓａｍｐｌｉｎｇ；相関二重サンプリング）回路（図示なし）を含み、固定パターンノイズを除去する信号処理を実施する。

【００４０】

水平駆動回路１５は、図２に示すように、カラム回路１４に電気的に接続されている。水平駆動回路１５は、たとえば、シフトレジスタを含み、カラム回路１４において画素Ｐの列ごとに保持されている信号を、順次、外部出力回路１７へ出力させる。

【００４１】

外部出力回路１７は、図２に示すように、カラム回路１４に電気的に接続されており、カラム回路１４から出力された信号について信号処理を実施後、外部へ出力する。外部出力回路１７は、ＡＧＣ（Ａｕｔｏｍａｔｉｃ Ｇａｉｎ Ｃｏｎｔｒｏｌ）回路１７ａとＡＤＣ回路１７ｂとを含む。外部出力回路１７においては、ＡＧＣ回路１７ａが信号にゲインをかけた後に、ＡＤＣ回路１７ｂがアナログ信号からデジタル信号へ変換して、外部へ出力する。

【００４２】

タイミングジェネレータ１８は、図２に示すように、垂直駆動回路１３、カラム回路１４、水平駆動回路１５，外部出力回路１７，シャッター駆動回路１９のそれぞれに電気的に接続されている。タイミングジェネレータ１８は、各種のタイミング信号を生成し、垂直駆動回路１３、カラム回路１４、水平駆動回路１５，外部出力回路１７，シャッター駆動回路１９に出力することで、各部について駆動制御を行う。

【００４３】

シャッター駆動回路１９は、画素Ｐを行単位で選択して、画素Ｐにおける露光時間を調整するように構成されている。

【００４４】

（Ａ－３）固体撮像装置の詳細構成

本実施形態にかかる固体撮像装置の詳細内容について説明する。

【００４５】

図３～図７は、実施形態１において、固体撮像装置の要部を示す図である。

【００４６】

図３は、画素Ｐの断面図である。図３では、図２に示す画素領域ＰＡの中心部分に配置された一の画素であって，Ｘ１－Ｘ２部分を示している。

【００４７】

図４は，画素Ｐの上面図であり，図２に示す画素領域ＰＡの中心部分に配置された４つの画素Ｐを示している。図４では、説明の都合で、破線などの実線以外の線を用いて、各部材を示している部分がある。

【００４８】

図５は、画素分離部３０１の断面図である。図６は、画素分離部３０１の上面図である

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。図５，図６において、（ａ）は、図２に示す画素領域ＰＡの中心部分に配置された画素Ｐの間の画素分離部３０１であって、ＸＩＣ－Ｘ２Ｃ部分を示している。これに対して、（ｂ）は、図２に示す画素領域ＰＡの周辺部分に配置された画素Ｐの間の画素分離部３０１であって、ＸＩＳ－Ｘ２Ｓ部分を示している。つまり、図５，図６では、水平方向ｘに並ぶ一対の画素Ｐの間に設けられた画素分離部３０１を示している。図示を省略しているが、垂直方向ｙに並ぶ一対の画素Ｐの間に設けられた画素分離部３０１についても、図５，図６と同様な形態で設けられている。

【００４９】

また、図７は、画素Ｐの回路構成を示している。

【００５０】

図３に示すように、固体撮像装置１は、半導体基板１０１の内部にフォトダイオード２１が設けられている。ここでは，薄膜化された単結晶シリコンの半導体基板１０１に設けられている。

【００５１】

半導体基板１０１の裏面（図３では上面）には，カラーフィルタＣＦ、マイクロレンズＭＬなどの部材が設けられている。

【００５２】

これに対して、半導体基板１０１の表面（図３では、下面）には、図３では図示していないが，図７に示す画素トランジスタＴｒが設けられている。そして、図３に示すように、その画素トランジスタＴｒを被覆するように配線層１１１が設けられており，配線層１１１において、半導体基板１０１の側に対して反対側の面には、支持基板ＳＳが設けられている。

【００５３】

つまり、本実施形態の固体撮像装置１は、「裏面照射型ＣＭＯＳイメージセンサ」であって、裏面（上面）側から入射する入射光Ｈを、フォトダイオード２１が受光し、カラー画像を撮像によって生成するように構成されている。

【００５４】

各部の詳細について順次説明する。

【００５５】

（ａ）フォトダイオード２１について

固体撮像装置１において、フォトダイオード２１は、図２に示した複数の画素Ｐに対応するように、複数が画素領域ＰＡに配置されている。つまり、撮像面（ｘｙ面）において、水平方向ｘと、この水平方向ｘに対して直交する垂直方向ｙとのそれぞれに並んで設けられている。

【００５６】

フォトダイオード２１は、入射光Ｈを受光面ＪＳで受光し光電変換することによって信号電荷を生成して蓄積するように、複数が半導体基板１０１の内部に間を隔てて設けられている。

【００５７】

ここでは、図３に示すように、半導体基板１０１の裏面（図３では上面）側から入射する入射光Ｈをフォトダイオード２１が受光する。フォトダイオード２１の上方には、図３に示すように、平坦化膜ＨＴ，カラーフィルタＣＦ，マイクロレンズＭＬが設けられており、各部を順次介して入射した入射光Ｈを、受光面ＪＳで受光して光電変換が行われる。

【００５８】

図３に示すように、フォトダイオード２１は、半導体基板１０１内に設けられている。

【００５９】

たとえば、フォトダイオード２１は、ｎ型半導体領域１０１ｎが，電荷（ここでは、電子）を蓄積する電荷蓄積領域として形成されている。フォトダイオード２１においては、ｎ型半導体領域１０１ｎは、半導体基板１０１のｐ型半導体領域１０１ｐａ，１０１ｐｃの内部に設けられている。ここでは、ｎ型半導体領域１０１ｎにおいて、半導体基板１０

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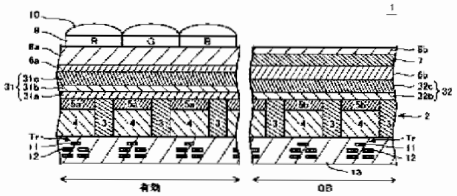
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(54)【発明の名称】固体撮像素子、固体撮像素子の製造方法および撮像装置

(57)【要約】
【課題】暗電流を抑制することができる固体撮像素子を提供する。
【解決手段】固体撮像素子は、光電変換が行われるフォトダイオードが形成された有効領域と、遮光膜により遮光された光学的黒領域とが形成された半導体基板と、前記有効領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第１の膜と、前記遮光領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第２の膜と、を備え、前記第１の膜が有する層の数が前記第２の膜が有する層の数と異なる。
【選択図】図１



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【特許請求の範囲】
【請求項１】
光電変換が行われるフォトダイオードが形成された有効領域、および遮光膜により遮光された光学的黒領域が形成された半導体基板と、
前記有効領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第１の膜と、
前記遮光領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第２の膜と、を備え、
前記第１の膜が有する層の数が前記第２の膜が有する層の数と異なる
固体撮像素子。
【請求項２】
前記第１の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、
前記第１層上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第２層と、
前記第２層上に、物理的気相成長を用いて形成された第３層と、を有し、
前記第２の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、
前記第１層上に、物理的気相成長を用いて形成された第２層と、を有する
請求項１に記載の固体撮像素子。
【請求項３】
前記第１の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、
前記第１層上に、物理的気相成長を用いて形成された第２層と、有し、
前記第２の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、
前記第１層上に、物理的気相成長を用いて形成された第２層と、
前記第２層上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第３層と、を有する
請求項１に記載の固体撮像素子。
【請求項４】
前記第１の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、
前記第１層上に、物理的気相成長を用いて形成された第２層と、
前記第２層上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第３層と、を有し、
前記第２の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層を有する
請求項１に記載の固体撮像素子。
【請求項５】
前記第１の膜および前記第２の膜を構成する層は、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜からなる
請求項１～４のいずれか１項に記載の固体撮像素子。

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【請求項６】
半導体基板に、光電変換が行われるフォトダイオードが形成された有効領域および遮光膜により遮光された光学的黒領域を形成する工程と、
前記有効領域上に負の固定電荷を有する層が少なくとも１層以上積層された第１の膜を形成する工程と、
前記遮光領域上に、負の固定電荷を有する層が少なくとも１層以上積層され、前記第１の膜が有する層の数とは異なる数の層を有する第２の膜を形成する工程と、を有する
固体撮像素子の製造方法。
【請求項７】
請求項１～５のいずれか１項に記載の固体撮像素子と、
前記固体撮像素子に被写体像を結像する光学系と、
前記固体撮像素子を駆動させる駆動パルスを生成する駆動部と、
前記固体撮像素子の出力画像信号を処理する信号処理回路と、を備える
撮像装置。
【発明の詳細な説明】
【技術分野】
【０００１】
本開示は、固体撮像素子、固体撮像素子の製造方法および撮像装置に関する。
【背景技術】
【０００２】
ＣＣＤ（Ｃｈａｒｇｅ Ｃｏｕｐｌｅｄ Ｄｅｖｉｃｅ）型やＣＭＯＳ（Ｃｏｍｐｌｅｍｅｎｔａｒｙ Ｍｅｔａｌ Ｏｘｉｄｅ Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）型の固体撮像素子では、フォトダイオードにおける結晶欠陥や、半導体基板に形成された受光部とその上の絶縁層との界面における界面準位が、暗電流の原因となることが知られている。
【０００３】
そこで、暗電流の発生を抑制する技術として、半導体基板の全面、例えば、受光画素領域(以下、「有効領域」という)および光学的黒領域（以下、「ＯＢ領域」という）上に、負の固定電荷を持つ膜を形成する技術が提案されている。この技術では、半導体基板上に負の固定電荷を持つ膜を形成し、受光部と絶縁層との界面付近に正電荷（ホール）を蓄積することで、界面準位に起因する暗電流の発生を抑制している。
【先行技術文献】
【特許文献】
【０００４】
【特許文献１】特開２０１０－２３９１１６号公報
【発明の概要】
【発明が解決しようとする課題】
【０００５】
しかしながら、界面準位に起因する暗電流は、有効領域とＯＢ領域とでは、その案電流量が異なる。従って、上述した負の固定電荷を有する膜を半導体基板の全面に形成する場合には、全体的な暗電流量は低減するものの、有効領域とＯＢ領域との暗電流差が発生し、いわゆるＯＢ段差が発生することが問題となっている。
【０００６】
かかる問題に鑑みて、本発明は、有効領域における暗電流と光学的黒領域における暗電流との差を小さくすることができ、いわゆるＯＢ段差を改善することができる固体撮像素子、固体撮像素子の製造方法および撮像装置を提供するものである。
【課題を解決するための手段】
【０００７】
そこで、本開示の固体撮像素子は、光電変換が行われるフォトダイオードが形成された有効領域と、遮光膜により遮光された光学的黒領域とが形成された半導体基板と、前記有効領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第１の膜と

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、前記遮光領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第２の膜と、を備え、前記第１の膜が有する層の数が前記第２の膜が有する層の数と異なるものである。

【０００８】

また、本開示の固体撮像素子においては、前記第１の膜は、前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、前記第１層上に、前記原子層蒸着法または前記有機金属化学的気相成長法を用いて形成された第２層と、前記第２層上に、物理的気相成長を用いて形成された第３層と、を有し、前記第２の膜は、前記半導体基板上に、前記原子層蒸着法または前記有機金属化学的気相成長法を用いて形成された第１層と、前記第１層上に、前記物理的気相成長を用いて形成された第２層と、を有するものである。

【０００９】

また、本開示の固体撮像素子においては、前記第１の膜は、前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、前記第１層上に、物理的気相成長を用いて形成された第２層と、有し、前記第２の膜は、前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、前記第１層上に、物理的気相成長を用いて形成された第２層と、前記第２層上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第３層と、を有するものである。

【００１０】

また、本開示の固体撮像素子においては、前記第１の膜は、前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、前記第１層上に、物理的気相成長を用いて形成された第２層と、前記第２層上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第３層と、を有し、前記第２の膜は、前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層を有するものである。

【００１１】

また、本開示の固体撮像素子においては、前記第１の膜および前記第２の膜を構成する層は、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜からなるものである。

【００１２】

また、本開示の固体撮像素子の製造方法は、半導体基板に、光電変換が行われるフォトダイオードが形成された有効領域および遮光膜により遮光された光学的黒領域を形成する工程と、前記有効領域上に負の固定電荷を有する層が少なくとも１層以上積層された第１の膜を形成する工程と、前記遮光領域上に、負の固定電荷を有する層が少なくとも１層以上積層され、前記第１の膜が有する層の数とは異なる数の層を有する第２の膜を形成する工程と、を有するものである。

【００１３】

また、本開示の撮像装置は、前記固体撮像素子と、前記固体撮像素子に被写体像を結像する光学系と、前記固体撮像素子を駆動させる駆動パルスを生成する駆動部と、前記固体撮像素子の出力画像信号を処理する信号処理回路と、を備えるものである。

【発明の効果】

【００１４】

本開示によれば、有効領域における暗電流と光学的黒領域における暗電流との差を小さくすることができ、いわゆるＯＢ段差を改善することができる。

【図面の簡単な説明】

【００１５】

【図１】本開示の実施形態に係る固体撮像素子の断面構造を示す図である。

【図２】負の固定電荷を有する膜の膜厚と暗電流量との関係図である。

【図３】本開示の実施形態に係る固体撮像素子の製造方法を示す図である。

【図４】本開示の実施形態に係る固体撮像素子を備えた撮像装置の構成を示す図である。

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【図５】変形例１係る固体撮像素子の断面構造を示す図である。
【図６】変形例１係る固体撮像素子の製造方法を示す図である。
【図７】負の固定電荷を有する膜の膜厚と暗電流量との関係図である。
【図８】変形例２係る固体撮像素子の断面構造を示す図である。
【図９】変形例２係る固体撮像素子の製造方法を示す図である。
【図１０】負の固定電荷を有する膜の膜厚と暗電流量との関係図である。
【発明を実施するための形態】
【００１６】
本開示に係る固体撮像素子では、固体撮像素子の半導体基板におけるフォトダイオードが形成された有効領域上に、負の固定電荷を有する第１の膜（以下、「第１の膜」という）を形成し、遮光膜により遮光された光学的黒領域上に、第１の膜とは積層される層の数が異なる負の固定電荷を有する第２の膜（以下、「第２の膜」という）を形成する。
【００１７】
第１の膜は、例えば、半導体基板上に形成された第１層と、この第１層上に形成された第２層と、この第２層上に形成された第３層とにより構成される。
【００１８】
第１の膜を構成する第１層および第２層は、ＡＬＤ（Atomic Layer Deposition；原子層蒸着）法またはＭＯＣＶＤ（Metal Organic Chemical Vapor Deposition；有機金属化学的気相成長）法を用いて形成する。また、第１の膜を構成する第３層は、ＰＶＤ（Physical Vapor Deposition；物理的気相成長）法により形成する。
【００１９】
また、第２の膜は、例えば、半導体基板上に形成された第１層と、この第１層上に形成された第２層とにより構成される。第２の膜を構成する第１層は、ＡＬＤ法またはＭＯＣＶＤ法を用いて形成する。また、第２の膜を構成する第２層は、ＰＶＤ法により形成する。
【００２０】
第１の膜および第２の膜を構成する層の材料としては、例えば、酸化ハフニウム（HfO_2）、酸化アルミニウム（Al_2O_3）、酸化ジルコン（ZrO_2）、酸化タンタル（Ta_2O_5）および酸化チタン（TiO_2）等の酸化物が挙げられる。これらの酸化物の層は、絶縁ゲート型電界効果トランジスタのゲート絶縁膜等に用いられている実績があるため、形成方法が確立されており、容易に形成することができる。
【００２１】
また、これらの材料のうち、特に、屈折率の比較的高い、酸化ハフニウム（屈折率２．０５）、酸化タンタル（屈折率２．１６）、酸化チタン（屈折率２．２０）等を形成した場合には、反射防止効果をも得ることも可能になる。
【００２２】
上記以外の材料としては、例えば、希土類元素の酸化物が挙げられる。即ち、ランタン、プラセオジム、セリウム、ネオジム、プロメチウム、サマリウム、ユウロピウム、ガドリニウム、テルビウム、ジスプロシウム、ホルミウム、エルビウム、ツリウム、イッテルビウム、ルテチウム、イットリウムの各酸化物が挙げられる。
さらにまた、窒化ハフニウム、窒化アルミニウム、酸窒化ハフニウム、酸窒化アルミニウムを使用することも可能である。
【００２３】
負の固定電荷を有する第１層、第２層、第３層に、絶縁性を損なわない範囲で、層中にシリコン（Ｓｉ）や窒素（Ｎ）が添加されていてもよい。その場合、シリコンや窒素の濃度は、層の絶縁性が損なわれない範囲で適宜決定される。このように、シリコンや窒素が添加されることによって、各層の耐熱性やプロセスの中でのイオン注入の阻止能力を上げることが可能になる。
【００２４】
第１の膜を構成する第１層および第２層、および第２の膜を構成する第１層は、上述の

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とおり、ＡＬＤ法またはＭＯＣＶＤ法を用いて形成する。ＡＬＤ法により第１の膜を形成する場合には、例えば、基板温度が２００～５００℃、プリカーサの流量が１０～５００ｓｃｃｍ、プリカーサの照射時間が１～１５秒、O_3の流量が５～５０ｓｃｃｍの条件とする。また、ＭＯＣＶＤ法により第１の膜を形成する場合には、例えば、基板温度が２００～６００℃の条件とする。

【００２５】

なお、半導体基板がシリコン層であり、その上に第１の膜を構成する第１層や第２の膜を構成する第１層をＡＬＤ法により形成した場合には、同時に、シリコン層の表面に界面準位を低減する酸化シリコン膜を厚さ１ｎｍ程度形成することが可能になる。

【００２６】

第１の膜を構成する第２層は、上述のとおり、ＡＬＤ法またはＭＯＣＶＤ法を用いて形成する。ＡＬＤ法により、第１の膜を構成する第２層を形成する場合には、例えば、基板温度が２００～５００℃、プリカーサの流量が１０～５００ｓｃｃｍ、プリカーサの照射時間が１～１５秒、O_3の流量が５～５０ｓｃｃｍの条件とする。また、ＭＯＣＶＤ法により、第１の膜を構成する第２層を形成する場合には、例えば、基板温度が２００～６００℃の条件とする。

【００２７】

また、第１の膜を構成する第３層および第２の膜を構成する第２層は、上述のとおり、ＰＶＤ法を用いて形成する。ＰＶＤ法により、第１の膜を構成する第３層、および第２の膜を構成する第２層を形成する際には、例えば、圧力が０．０１～５０Ｐａ、パワーが５００～２０００Ｗ、Ａｒの流量が５～５０ｓｃｃｍ、O_2の流量が５～５０ｓｃｃｍの条件とする。

【００２８】

ＰＶＤ法により、第１の膜を構成する第３層、および第２の膜を構成する第２層を形成するので、ＡＬＤ法やＭＯＣＶＤ法と比較して形成速度が速くなり、比較的短い時間で、ある程度厚い膜を形成することが可能になる。

【００２９】

第１の膜を構成する第２層の膜厚、および第２の膜を構成する第１層の膜厚は、特に限定されないが、第１の膜を構成する第３層、および第２の膜を構成する第２層をＰＶＤ法により形成する際に半導体基板にダメージを与えることがないように、第１の膜を構成する第２層、および第２の膜を構成する第１層にはある程度以上の厚さが必要である。好ましくは、第１の膜の膜厚を１ｎｍ以上とする。

また、第１の膜を構成する第２層、および第２の膜を構成する第１層は、ＡＬＤ法またはＭＯＣＶＤ法によって形成するため、厚く形成するには時間がかかる。そのため、第１の膜を構成する第２層および第２の膜を構成する第１層の厚さは、５ｎｍ程度以下とすることが好ましい。

【００３０】

本開示に係る固体撮像素子では、有効領域上にて第１層上に第２層を形成し、さらに、第２層上に第３層を形成する第１の膜を備えているため、３つの層を合わせて、充分な負バイアス効果が得られる。また、ＯＢ領域上にて第１層上に第２層を形成する第２の膜を備えているため、２つの層を合わせて、充分な負バイアス効果が得られる。

【００３１】

特に、有効領域における第１の膜と、ＯＢ領域における第２の膜との膜構造を異なるようにしたため、有効領域における暗電流とＯＢ領域における暗電流の差を小さくして、いわゆるＯＢ段差を改善することができる。また、暗電流量の負の固定電荷を有する膜厚依存性により、各固体撮像素子の暗電流量に合わせて膜厚を調整することでＯＢ段差を調整することもできる。

【００３２】

また、有効領域における第１の膜とＯＢ領域における第２の膜の膜厚を個別に変更することができるため、第１の膜側から受光する場合では、受光画素部は負の固定電荷を有す

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る膜を反射防止膜としての最適膜厚を選択できる。

【００３３】

また、ＯＢ領域においては、光の入射を考慮する必要がないため反射防止膜的な効果から離れ暗電流改善のみで第２の膜の膜厚を調整することができる。

【００３４】

また、第１の膜を構成する第２層および第２の膜を構成する第１層をＡＬＤ法またはＭＯＣＶＤ法を用いて形成するので、第１の膜を構成する第２層および第２の膜を構成する第１層を形成する際に半導体基板にダメージを与えないようにすることができる。

【００３５】

上述したように、本開示によれば、第１の膜の膜厚と、第２の膜の膜厚とを個別に調整することができる。これにより、第１の膜の膜厚を、反射防止膜としての機能を発揮する最適な膜厚にすることができる。

【００３６】

さらに、光学的黒領域には光が入射しないため、第２の膜が反射防止膜としての機能を有する必要がないため、暗電流を改善するための最適な膜厚にすることができる。

【００３７】

以下に、本開示の実施形態に係る固体撮像素子について、図面を参照して説明する。各図において、同一の構成要素には同一の符号を付してある。なお、説明は以下の順序で行う。

１．固体撮像素子の構成
２．固体撮像素子の製造方法
３．撮像装置の構成等
４．その他の固体撮像素子の構成及び製造方法

【００３８】

〔１．固体撮像素子の構成〕

まず、本実施形態に係る固体撮像素子１の構成について、図１を参照して説明する。図１は、本実施形態に係る固体撮像素子の断面構造を示す図である。なお、本実施形態では、本発明を、いわゆる裏面照射型のＣＭＯＳ固体撮像素子（ＣＭＯＳイメージセンサ）に適用した例について説明する。

【００３９】

固体撮像素子１は、半導体基板２における有効領域２１およびＯＢ領域２２に、入射光を光電変換する受光部として、フォトダイオードとなる電荷蓄積領域４が、Ｎ型の不純物領域によって形成されている。この電荷蓄積領域４の表面には、正電荷蓄積領域５が形成されており、これら電荷蓄積領域４および正電荷蓄積領域５によって、ＨＡＤ（Hole-Accumulation Diode sensor）構造が構成されている。なお、それぞれの電荷蓄積領域４および正電荷蓄積領域５は、素子分離領域３により分離されている。

【００４０】

半導体基板２の表面側においては、半導体基板２の電荷蓄積領域４の下方に、ＭＯＳトランジスタＴｒのゲート電極１１が形成され、さらに下方に金属配線による配線層１２が形成されている。

【００４１】

ゲート電極１１および各層の配線層１２の間は、層間の絶縁層１３によって絶縁されている。なお、絶縁層１３は、図示しないが、下方に設けられる支持基板等によって支持されている。

【００４２】

電荷蓄積領域４を有するフォトダイオードによって、それぞれの画素が構成される。各画素には、図示のＭＯＳトランジスタ（この場合は、電荷蓄積領域４に蓄積した電荷を読み出し・転送する転送トランジスタ）Ｔｒを含む、１個以上のトランジスタを有して構成される。

【００４３】

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各画素の電荷蓄積領域４の間は、Ｐ型の素子分離領域３により分離されている。なお、図示しないが、電荷蓄積領域４のＭＯＳトランジスタＴｒのゲート電極１１側の界面に、ｐ＋半導体領域を形成して、絶縁層１３との界面における暗電流の発生を抑制することが好ましい。

【００４４】

半導体基板２の裏面側において、有効領域２１の上層には、負の固定電荷を有する第１の膜（以下、「第１の膜」という）３１が形成されている。この第１の膜３１は、半導体基板２上に形成された第１層３１ａと、この第１層３１ａ上に形成された第２層３１ｂと、この第２層３１ｂ上に形成された第３層３１ｃとが積層された構成を有する。

【００４５】

第１層３１ａは、例えば、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜を有し、ＡＬＤ法またはＭＯＣＶＤ法により形成される。

【００４６】

また、第２層３１ｂは、例えば、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜を有し、ＡＬＤ法またはＭＯＣＶＤ法により形成される。

第１層３１ａ、第２層３１ｂは、いずれもＡＬＤ法又はＭＯＣＶＤ法で形成されるため、第１層３１ａ、第２層３１ｂをあわせてＡＬＤ層とも称する。

【００４７】

また、第３層３１ｃは、例えば、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜を有し、ＰＶＤ法により形成される。従って、第３層３１ｃをＰＶＤ層とも称する。

【００４８】

このように、有効領域２１の上層に負の固定電荷を有する第１層３１ａ、第２層３１ｂ、第３層３１ｃが積層された第１の膜３１を形成している。第１の膜３１の中の負の固定電荷によって、電荷蓄積領域４の表面に電界が加わり、電荷蓄積領域４の表面に正電荷蓄積領域５が形成される。これにより、電荷蓄積領域４の表面にイオン注入をしなくても、正電荷蓄積領域５を形成することが可能になる。

【００４９】

第１の膜３１上には、例えば酸化シリコン（SiO_2）膜からなる絶縁膜６ａが形成されており、この絶縁膜６ａの上には、平坦化膜８ａが形成されている。また、平坦化膜８ａの上には、画素毎に、対応する色（赤Ｒ、緑Ｇ、青Ｂ）のカラーフィルタ９が形成されており、各カラーフィルタ９の上には、それぞれ、集光のためのオンチップレンズ１０が設けられている。

【００５０】

ＯＢ領域２２の上層には、負の固定電荷を有する第２の膜（以下、「第２の膜」という）３２が形成されている。この第２の膜３２は、半導体基板２上に形成された第１層３２ｂと、この第１層３２ｂ上に形成された第２層３２ｃとが積層された構成を有する。

【００５１】

第１層３２ｂは、例えば、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜を有し、ＡＬＤ法またはＭＯＣＶＤ法により形成される。従って、第１層３２ｂをＡＬＤ層とも称する。

【００５２】

第２層３２ｃは、例えば、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜を有し、ＰＶＤ法により形成される。従って、第２層３２ｃをＰＶＤ層とも称する。

【００５３】

このように、ＯＢ領域２２の上層に、負の固定電荷を有する第１層３２ｂ及び第２層３２ｃが積層された第２の膜３２を形成しているため、この第２の膜３２の中の負の固定電

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荷によって、電荷蓄積領域４の表面に電界が加わり、電荷蓄積領域４の表面に正電荷蓄積領域５が形成される。これにより、電荷蓄積領域４の表面にイオン注入をしなくても、正電荷蓄積領域５を形成することが可能になる。

【００５４】

第２の膜３２上には、例えば酸化シリコン膜からなる絶縁膜６ｂが形成されており、この絶縁膜６ｂの上には、ＯＢ領域２２を覆うように、遮光膜７が形成されている。この遮光膜７によって、フォトダイオードに光が入らない領域（図示しないオプティカルブラック領域）を作り、そのフォトダイオードの出力によって画像での黒レベルを決定することができる。

【００５５】

上述したように、第１の膜３１は３層の積層構造であり、第２の膜３２は２層の積層構造である。このように、固体撮像素子１は、第１の膜３１が有する層の数が第２の膜３２が有する層の数と異なる。本実施形態では、第１の膜３１が有する層の数は、第２の膜３２が有する層の数より多く、第１の膜３１の膜厚が第２の膜３２の膜厚より厚くなっている。ただし、第１の膜３１の膜厚と第２の膜３２の膜厚の差（段差）は数ｎｍ程度である。この程度の段差は、後述するように第１の膜３１及び第２の膜３２上に絶縁膜６や平坦化膜８を形成することで吸収することができるため、固体撮像素子１のカラーフィルタ９などを平らな膜上に形成することができる。

【００５６】

絶縁膜６ｂおよび遮光膜７を覆って、平坦化膜８ｂが形成されている。

【００５７】

本実施の形態の固体撮像素子１は、図１の上方から光が入射されると、フォトダイオードの電荷蓄積領域４において光を信号電荷に変換する光電変換が生じるため、入射光を受光検出することができる。そして、固体撮像素子１は、フォトダイオードが形成された半導体基板２から見て、下層にある配線層１２の側（表面側）とは反対側（裏面側）の上層から光を入射させる、いわゆる裏面照射型構造となっている。

【００５８】

特に、固体撮像素子１では、有効領域２１上に第１の膜３１を形成し、ＯＢ領域２２上に第２の膜３２を形成しているため、有効領域２１における暗電流の低減と、ＯＢ領域２２における暗電流の低減を個別に行うことができる。これにより、図７に示すように、有効領域２１とＯＢ領域２２における暗電流量差を低減することができ、いわゆるＯＢ段差の発生を抑制することができる。

【００５９】

本実施の形態の固体撮像素子１においては、特に、有効領域２１における第１の膜３１が、第１層３１ａと、その上の第２層３１ｂと、その上の第３層３１ｃとの３層の積層構造となっている。また、ＯＢ領域２２における第２の膜３２が、第１層３２ｂと、その上の第２層３２ｃとの２層の積層構造となっている。

【００６０】

第１の膜３１では、第１層３１ａおよび第２層３１ｂはＡＬＤ法またはＭＯＣＶＤ法により形成し、第３層３１ｃはＰＶＤ法により形成する。また、第２の膜３２では、第１層３２ｂはＡＬＤ法またはＭＯＣＶＤ法により形成し、第２層３２ｃはＰＶＤ法により形成する。

【００６１】

これら第１の膜３１を構成する第１層３１ａ、第２層３１ｂおよび第３層３１ｃの材料としては、例えば、酸化ハフニウム、酸化アルミニウム、酸化ジルコン、酸化タンタルおよび酸化チタンのうちいずれか一つの酸化物を使用することが可能である。また、上述した、窒化物や酸窒化物、希土類元素の酸化物等も、使用することが可能である。

【００６２】

また、第２の膜３２を構成する第１層３２ｂおよび第２層３２ｃの材料としては、例えば、酸化ハフニウム、酸化アルミニウム、酸化ジルコン、酸化タンタルおよび酸化チタン

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のうちいずれか１つの酸化物を使用することが可能である。また、上述した、窒化物や酸窒化物、希土類元素の酸化物等も、使用することが可能である。

【００６３】

半導体基板２の上層に、第１の膜３１および第２の膜３２を設けたことにより、界面付近に正電荷（ホール）が蓄積されるようにすることができる。なお、特に、第１の膜３１として、屈折率の比較的高い、酸化ハフニウム膜、酸化タンタル膜および酸化チタン等の酸化膜を形成した場合には、反射防止効果を得ることも可能になる。

【００６４】

図２に上述した負の固定電荷を有する膜３１，３２の膜厚に対する暗電流量の関係を示す。図２（ａ）は、ＡＬＤ層の厚さと暗電流量の関係を示す図であり、図２（ｂ）、（ｃ）は、ＰＶＤ層の厚さと暗電流量の関係を示す図である。図２（ｂ）、（ｃ）に示すように暗電流量は、ＰＶＤ層の膜厚には大きく依存せず、図２（ａ）に示すように、暗電流量は、ＡＬＤ層の厚さに依存する。

【００６５】

図２（ａ）に示すように、有効領域における暗電流量は、ＯＢ領域における暗電流量よりも大きい。また、第１の膜３１および第２の膜３２ともにＡＬＤ層の厚さを薄くすることで、暗電流量は減少する。これまでの固体撮像素子は、有効領域及びＯＢ領域のＡＬＤ層の厚さが等しくなるように半導体基板２上に膜が形成されていた。従って、有効領域とＯＢ領域の暗電流量の差（ＯＢ段差）は一定以上発生し、膜厚が大きくなるほどその差が大きくなっていた。

一方、本実施形態の固体撮像素子１は、暗電流量が大きい有効領域のＡＬＤ層の厚さを、ＯＢ領域のＡＬＤ層より厚くしている。そのため、有効領域における暗電流量と、ＯＢ領域における暗電流量との暗電流量差が減少する。

【００６６】

〔２．固体撮像素子の製造方法〕

次に、本実施の形態の固体撮像素子１の製造方法について説明する。図３は固体撮像素子１の製造方法を示す図である。なお、以下の説明は、有効領域２１の半導体基板２内に電荷蓄積領域４が形成されており、ＭＯＳトランジスタＴｒのゲート電極１１および配線層１２が形成されている状態から始めることとする。

【００６７】

まず、図３（ａ）に示すように、ＡＬＤ法またはＭＯＣＶＤ法により、半導体基板２の有効領域２１およびＯＢ領域２２上に、負の固定電荷を有する膜３３として酸化ハフニウム膜を形成する。なお、負の固定電荷を有する膜３３ａの材料としては、上述した酸化ハフニウム以外にも、例えば、酸化アルミニウム、酸化ジルコン、酸化タンタルおよび酸化チタンのうちいずれか１つの酸化物を用いることができる。

【００６８】

ＡＬＤ法で形成する場合の形成条件は、例えば、形成基板温度２００～５００℃、プリカーサ流量が１０～５００ｓｃｃｍ、照射時間１～１５秒、O_3流量１０～５００ｓｃｃｍ、とする。また、負の固定電荷を有する膜３３ａの膜厚は、好ましくは１ｎｍ以上である。

【００６９】

次に、図３（ｂ）に示すように、有効領域２１における負の固定電荷を有する膜３３ａ上にレジスト４０を形成した後、ウェットエッチングによりレジスト４０および露出している負の固定電荷を有する膜３３ａを除去する。これにより、図３（ｃ）に示すように、半導体基板２の有効領域２１上に、第１の膜３１を構成する第１層３１ａを形成する。

【００７０】

次に、図３（ｄ）に示すように、ＡＬＤ法またはＭＯＣＶＤ法により、第１層３１ａおよびＯＢ領域２２上に、負の固定電荷を有する膜３４として酸化ハフニウム膜を形成する。これにより、第１層３１ａ上に第２層３１ｂを形成し、ＯＢ領域２２上に第２の膜３２の第１層３２ｂを形成する。なお、負の固定電荷を有する膜３４の材料としては、上述し

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Abstract of JP2012212349 (A)

PROBLEM TO BE SOLVED: To inhibit operation by a person other than a user himself/herself in the middle of the operation, by performing identity authentication over the whole period of access to confidential information or operation of a machine tool, using biometric authentication.SOLUTION: The biometric authentication device includes: photographing means for photographing biological information of a person who tries operating an operational object; determination means for collating the photographed biological information with biological information of a user himself/herself registered beforehand in a database and determining whether the person is the user himself/herself; and control means for controlling the photographing means and the determination means, periodically or always photographing the biological information, periodically or always determining whether the person is the user himself/herself based on the photographed photographic information, continuously authenticating that the person who tries operating the operational object is the user himself/herself, and permitting or inhibiting continuous operation of the operational object according to the result.

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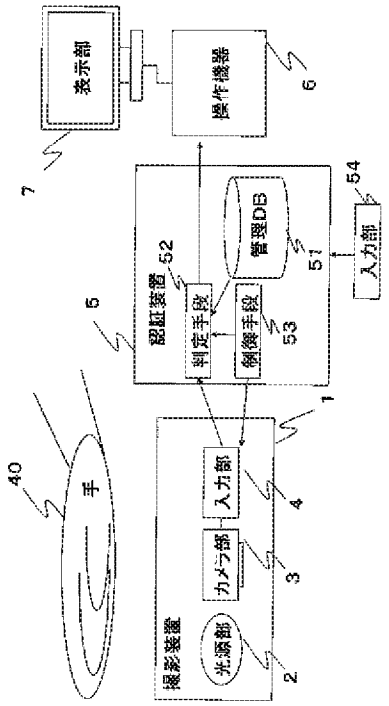
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(54)【発明の名称】生体認証装置

(57)【要約】
【課題】　生体認証を使用し、機密情報へのアクセスや工作機械の操作の全期間に渡って本人認証を行なうことにより、操作途中で本人以外の者の操作を抑止すること。
【解決手段】　操作対象を操作しようとする利用者の生体情報を撮影する撮影手段と、撮影された生体情報とデータベースに予め登録されている利用者本人の生体情報とを照合し、利用者本人であるかを判定する判定手段と、前記撮影手段および判定手段を制御し、生体情報を定期的または常時撮影し、その撮影した撮影情報に基づき利用者本人であるか否かを定期的または常時判定し、操作対象を操作しようとする利用者が利用者本人であることを継続的に認証し、その結果に応じて操作対象の継続操作を許可または抑止する制御手段とを有することを特徴とする。
【選択図】　図３



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【特許請求の範囲】
【請求項１】
操作対象を操作しようとする利用者の生体情報を撮影する撮影手段と、撮影された生体情報とデータベースに予め登録されている利用者本人の生体情報とを照合し、利用者本人であるかを判定する判定手段と、前記撮影手段および判定手段を制御し、生体情報を定期的または常時撮影し、その撮影した撮影情報に基づき利用者本人であるか否かを定期的または常時判定し、操作対象を操作しようとする利用者が利用者本人であることを継続的に認証し、その結果に応じて操作対象の継続操作を許可または抑止する制御手段とを有することを特徴とする生体認証装置。
【請求項２】
前記撮影手段は、操作対象を操作する操作子に取り付けられていること特徴とする請求項１に記載の生体認証装置。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、指静脈などの生体情報を読み取り、本人確認をリアルタイムに行なえるようにした生体認証装置に関するものである。
【背景技術】
【０００２】
近年、本人確認を行なう技術として生体認証装置が脚光を浴びている。この生体認証装置で本人確認を行なうことにより、利用者端末に格納されている機密情報の利用者による漏洩を防ぐものがある。
例えば、下記の特許文献１には、本人確認を行なうための携帯機器を小型化し、さらに多様な環境でも良好な精度が得られるよう、フード体を使用し、認証精度を向上させるようにした携帯型生体認証装置が開示されている。
【先行技術文献】
【特許文献】
【０００３】
【特許文献１】特開２００９－７０１１０号公報
【発明の概要】
【発明が解決しようとする課題】
【０００４】
現在、機密データへのアクセスや、工作機械や、建設機械など特定の人間しか操作が許可されていない装置を操作する際、パスワードやＩＣカード、あるいは生体認証による本人確認が行われている。
一方、これらの本人確認は操作開始時、例えば、個人情報や未発表情報などの機密データにアクセスに先立って一度だけ行なわれるものが多い。そのため、本人認証を行った環境においてはその後の操作は本人でなくても操作できてしまうという問題があった。例えば、パーソナルコンピュータの起動時に本人確認が必要な場合は、起動時に本人認証を行い、成功すると、本人以外でもそのパーソナルコンピュータが管理・共有している機密データを閲覧・変更することができるようになるという問題があった。
【０００５】
本発明の目的は、生体認証を使用し、機密情報へのアクセスや工作機械の操作の全期間に渡って本人認証を行なうことにより、操作途中で本人以外の者の操作を抑止すること、利用者が機密データを含むファイルの閲覧、編集作業を行なう際に本人確認を利用者が意識することなくリアルタイムに行なえるようにした生体認証搭装置を提供することにある。
【課題を解決するための手段】
【０００６】
上記目的を達成するために、本発明の生体認証装置は、操作対象を操作しようとする利

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用者の生体情報を撮影する撮影手段と、撮影された生体情報とデータベースに予め登録されている利用者本人の生体情報とを照合し、利用者本人であるかを判定する判定手段と、前記撮影手段および判定手段を制御し、生体情報を定期的または常時撮影し、その撮影した撮影情報に基づき利用者本人であるか否かを定期的または常時判定し、操作対象を操作しようとする利用者が利用者本人であることを継続的に認証し、その結果に応じて操作対象の継続操作を許可または抑止する制御手段とを有することを特徴とする。

そして、前記撮影手段は、操作対象を操作する操作子に取り付けられていること特徴とする。

【発明の効果】

【０００７】

本発明によれば、操作対象を操作しようとする利用者が本人であるか否かを継続的に認証するため、最初は利用者本人であることが認証されたとしても途中で操作する人が別人に変わった場合には、継続的な認証が否定されることになり、直ちに操作対象を操作することが不可能になる。

従って、本認証装置を自動車のハンドル操作者を認証するための装置として取り付けた場合、予め登録しておいた利用者以外の者が運転しようとしたときには、本人認証が否定され、継続的な運転できなくなり、盗難予防に役立てることが可能になる。

また、パーソナルコンピュータのマウスに適用した場合、予め登録しておいた利用者以外の者が機密情報などにアクセスしようとしても抑止され、機密情報の漏洩を防止することが可能になる。

また、工作機械の操作ハンドルの操作者を認証するための装置として取り付けた場合、予め登録しておいた操作者以外の者が操作しようとしたときには、本人認証が否定され、操作がすることが抑止され、事故の発生が未然に防止される。

【図面の簡単な説明】

【０００８】

【図１】本発明に係る生体認証装置の実施形態を示す上面図である。

【図２】本発明に係る生体認証装置の実施形態を示す側面図である。

【図３】本発明に係る生体認証装置の実施形態を示すブロック図である。

【図４】本発明に係る生体認証装置の実施形態において操作する手の置き方の例を示す図である。

【発明を実施するための形態】

【０００９】

以下、本発明を実施する場合の実施形態を、図面を用いて詳細に説明する。

図１は、本発明に係る生体認証置本体の外観上面図である。

認証装置１は、手のひらを置く手段を備えた本体筐体１００と、生体情報を撮影するための窓部１０２と、この窓部１０２を保持する手段を備えた保持部１０１で構成される。

本体筐体１００は、その内部に、少なくとも、窓部１０２に挿入された指に検知光を照射する光源部２（図３参照）と、窓部１０２に挿入された指から反射した検知光を検知するカメラ部３（図３参照）と、カメラ部３で撮影した生体情報の上下左右の動きを検知する動作入力部４（図３参照）を含んで構成される。

また、本体筐体１００の外観は、高さ寸法より横幅寸法が大きく、かつ横幅寸法より奥行寸法が大きい箱型の外観形状により形成されている。

【００１０】

窓部１０２に挿入された指は、本体筐体１００を縦長になるように手を乗せた際に奥側に当たる位置で広がるように置かれる。例えば窓部１０２の手前部分は本体筐体１００の奥部分の端から本体筐体１００に手の平を下にして乗せた場合に、人差し指や中指の第二間接から指の付け根辺りまでの範囲とする。本体筐体１００の窓部１０２部分の内部に光源部２（図３参照）と、カメラ部３（図３参照）と、動作入力部４（図３参照）が設けられ、この光源部２から発した光は指で反射したのち、窓部１０２を介してカメラ部３で撮影されることとなる。

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【００１１】
そして、この実施の形態に係る撮影装置１の大きな特徴の１つは、窓部１０２の範囲を広くすることにより、指を動かした際に指の先端の位置の変化を読み取り、その位置情報を操作対象を操作する指令情報として用いることができる点である。この特徴によれば、生体認証をリアルタイムで行なうとともに、マウス操作で行なっているようなクリックやスクロールなどの操作が使用可能である。これは、マウスなどの入力装置で頻繁に使用するボタンやホイール部分の劣化や故障を防ぐことができ、設置している指を自由に動かすことができる事から、これまでの生体情報取得時の利用者の不快感や窮屈さを取り除くことができる。

【００１２】
図２は、生体認証装置１の外観側面図である。
これは、指を保持する指保持手段を備えた本体筐体１００をなだらかな球面にすることで手にフィットし易く、生体情報の撮影や窓部１０２上で指などの入力操作を円滑にすることを可能にする。

【００１３】
図３は、生体認証装置の全体構成を示すブロック図である。
図３を参照しながら、生体認証装置の構成を簡単に説明する。
この実施の形態に係る生体認証装置は、撮影装置１と、撮影した生体情報により本人認証を行なう認証装置５とで構成され、認証結果は操作対象機器６に付属の表示部７に表示される。また、認証結果により、操作対象機器６への操作が抑止される。

【００１４】
認証装置５には、利用者の生体情報を予め登録した管理データベース５１が設けられると共に、管理データベース５１に登録した生体情報と撮影装置１で撮影した生体情報を照合し、予め登録した本人であるか否かを認証する判定手段５２と、撮影装置１の撮影動作および判定手段５２の判定動作を定期的または常時実施させるように制御する制御手段５３が内蔵されている。判定手段５２において判定結果が利用者本人ではないというものであった場合には、操作対象機器６に対して動作を停止させる制御信号が出力される。
ここで示す認証装置５は、撮影装置１とは別々に構成されているが、撮影装置１の中に含ませて構成することもできる。
撮影装置１は、操作対象を操作する操作子に取り付けて操作対象機器６を操作する利用者の生体情報を撮影し、認証装置５により認証を受けるように構成するのが望ましい。

【００１５】
図４は、生体認証装置本体の撮影装置１（図３参照）に利用者の手を置いた様子を表したものである。
利用者の手４０の人差し指と中指の第一関節と第二関節の間が窓部１０２に接するように撮影装置１（図３参照）を構成する。この場合、撮影装置１に利用者の手４０を置きやすいように、撮影装置１の形態を大きくしたり、小さくしたり、くびれさせたりしても良い。
ここで、窓部１０２の範囲を広くすることにより、指を動かした際に指の先端の位置の変化を読み取り、その位置情報を操作対象を操作する指令情報として用いることができる点である。このように構成すれば、生体認証をリアルタイムで行なうとともに、マウス操作で行なっているようなクリックやスクロールなどの操作が使用可能である。これは、マウスなどの入力装置で頻繁に使用するボタンやホイール部分の劣化や故障を防ぐことができ、設置している指を自由に動かすことができる事から、これまでの生体情報取得時の利用者の不快感や窮屈さを取り除くことができる。
なお、本発明は上記実施形態に限定されるものではなく、自動車や２輪車のハンドル操作を行う者を認証する装置、大型のクレーンを操作する者を認証する装置、高級カメラを使用する者を認証する装置などに適用することが可能である。

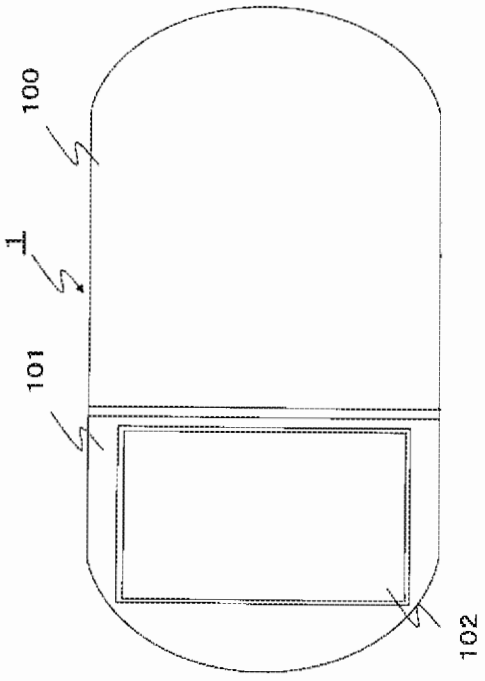
【符号の説明】

【００１６】

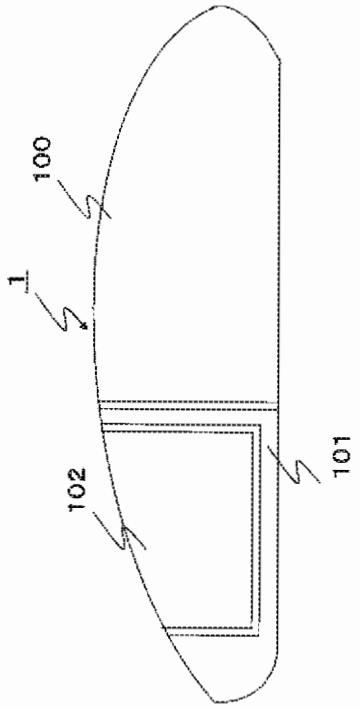
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１…撮影装置、２…光源部、３…カメラ部、４…動作入力部、５…認証装置、５１…管理ＤＢ、６…操作対象機器、５２…判定手段、５３…制御手段、５４…入力部、４０…利用者の手、１００…本体筐体、１０１…保持部、１０２…窓部。

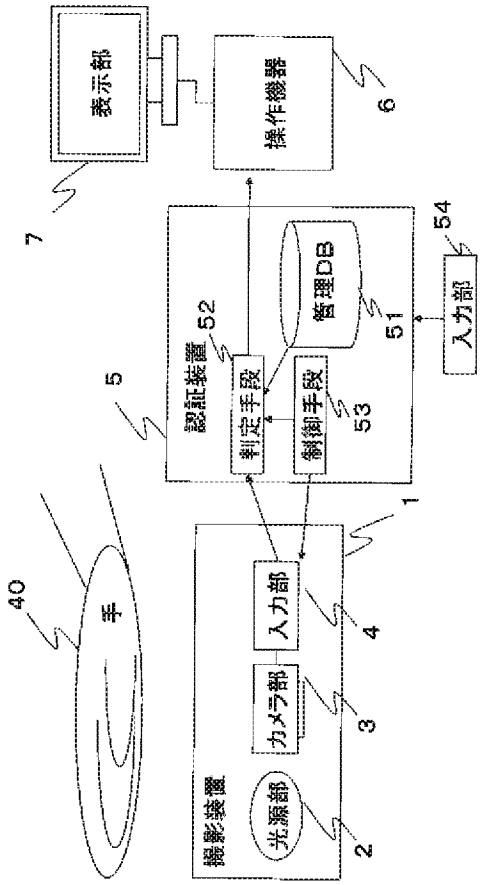
【図１】



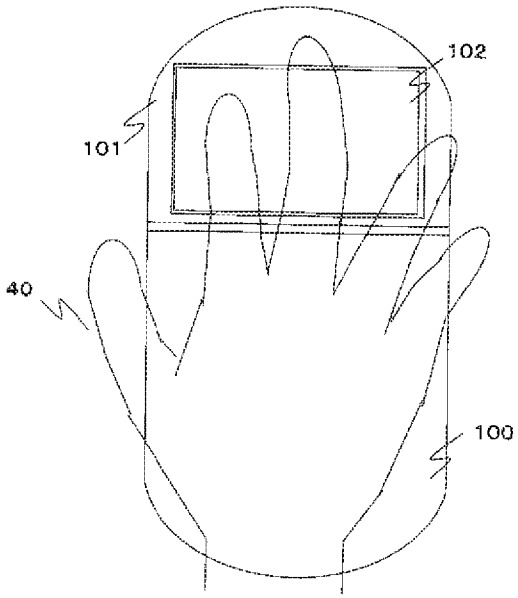
【図２】



【図３】


表示部
操作機器
6
7
54
入力部
管理DB
51
認証装置
52
判定手段
制御手段
53
5
1
40
手
入力部
4
カメラ部
3
撮影装置
光源部
2

【図４】

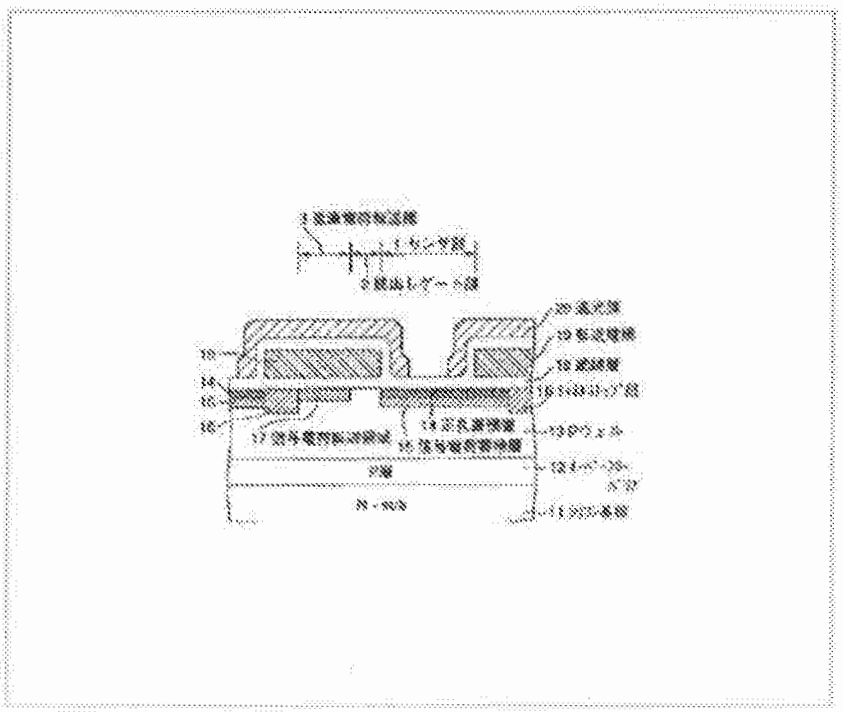

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(71)Applicant SONY CORP
(72)Inventor ABE HIDEJI

(54)SOLID-STATE IMAGE SENSOR AND FORMATION OF SENSOR STRUCTURE THEREOF

(57)Abstract
PURPOSE: To provide the structure of a solid-state image sensor, wherein the multiple reflections between the surface of a substrate and the lower edge of a light screening film or a transfer electrode in a charge transfer part is eliminated and smear can be decreased.
CONSTITUTION: In a CCD area sensor having a plurality of sensor parts 1 and vertical charge transfer parts 3 for transferring the signal charges read out of the sensor parts, the sensor structure is formed so that each incident surface of the sensor part 1 is formed in an irregular shape, and the light, which is obliquely cast into the sensor part 1, is not reflected into the protruding part forming the irregular shape and is not cast in a signal-charge transfer region 17.



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CLAIMS

[Claim(s)]

[Claim 1]A solid state imaging device which is provided with the following and characterized by a thing of each incident plane of two or more aforementioned sensor parts for which a peripheral edge part is making uneven form at least.
Two or more sensor parts which carry out photoelectric conversion of the incident light, and accumulate the signal charge and which were arranged by at least one row.
A charge transfer section which transmits a signal charge read from two or more aforementioned sensor parts.

[Claim 2]The solid state imaging device according to claim 1, wherein each whole incident plane surface of two or more aforementioned sensor parts is making uneven form.
[Claim 3]The solid state imaging device according to claim 1 or 2, wherein a pitch and height of a protruding part of said uneven form are set up 1 of wavelength of incident light / 10 to 10 times.
[Claim 4]Two or more sensor parts which carry out photoelectric conversion of the incident light, and accumulate the signal charge and which were arranged by at least one row.
A charge transfer section which transmits a signal charge read from two or more aforementioned sensor parts.
In a formation method of sensor structure in a solid state imaging device provided with the above,
A formation method of sensor structure which forms hemispherical grain polysilicon on it and is characterized by etching the aforementioned silicon oxide film from a gap between said hemispherical grain polysilicon while forming a silicon oxide film on a sensor surface.

[Claim 5]A formation method of the sensor structure according to claim 4 characterized by forming a trench in a sensor surface of the etching portion after etching the aforementioned silicon oxide film.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]The present invention relates to a solid state imaging device, and relates to structure of the sensor part especially in a solid state imaging device, and a formation method for the same.
[0002]
[Description of the Prior Art]As an example of a solid state imaging device, it is CCD (ChargeCoupled Device) of an interline transmission mode, for example. The schematic structure of an area sensor is shown in Fig.6. In the figure, level and two or more sensor parts 1 which two-dimensional array is perpendicularly carried out, carry out photoelectric conversion of the incident light, and accumulate the signal charge, The imaging part 4 is constituted by the vertical charge transfer section 3 which transmits perpendicularly the signal charge which was arranged for every vertical file of these sensor parts 1, and read at a part of vertical blanking period, and was read via the gate section 2.
[0003]In this imaging part 4, the sensor part 1 consists of photo-diodes, and the vertical charge transfer section 3 is constituted by CCD. The signal charge read from the sensor part 1 to the vertical charge transfer section 3 is transmitted to the horizontal transfer part 5 in order of partial [every] which is equivalent to one scanning line at a part of horizontal blanking period. The signal charge for this one scanning line is sequentially transmitted horizontally by the level charge transfer section 5.
[0004]The transmitted signal charge is detected, and it converts to a signal level, for example, the charge detector 6 which consists of FDA (Floating Diffusion Amplifier) is arranged at the output side of the level charge transfer section 5. The essential part of the section (A-A' arrowed cross-section of Fig.6) structure of the sensor part 1 and the vertical charge transfer section 3 is shown in Fig.7.
[0005]
[Problem to be solved by the invention]At the vertical charge transfer section 3 in the above-mentioned CCD area sensor, as shown in Fig.7, the structure which intercepts the incidence of an extraneous light to the signal-charge transfer region 73 is taken by forming the light-shielding film 72 which becomes the portion except the sensor part 1, i.e., the outside of the transfer electrode 71, from aluminum etc.
[0006]However, since the surface of the sensor part 1 is formed as a flat surface in the conventional sensor structure so that clearly from Fig.7, When light enters into the sensor part 1 aslant, the lower end surface 72a of the light-shielding film 72 has an incident component among the lights reflected in the sensor surface, This reflected light component repeated the multiple echo between the substrate surface, the lower end surface 72a of the light-shielding film 72, or the transfer electrode 71, it jumped into the signal-charge transfer region 73 eventually, the photoelectron was generated, and there was a problem of making a smear

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component increase.
[0007]In light of the above-mentioned problems, the present invention comes out.
the object loses a multiple echo between a substrate surface, a lower end surface of a light-shielding film, or a transfer electrode which can be boiled and set, and there is in providing sensor structure of a solid state imaging device which enabled reduction of a smear, and a formation method for the same.

[0008]
[Means for solving problem]Two or more sensor parts which the solid state imaging device according to claim 1 carries out photoelectric conversion of the incident light, and accumulate the signal charge and which were arranged by at least one row, The charge transfer section which transmits the signal charge read from two or more of these sensor parts is provided, and it has the composition of each incident plane of two or more sensor parts that the peripheral edge part made uneven form at least.
[0009]The solid state imaging device according to claim 2 has the composition that each whole incident plane surface of two or more sensor parts made uneven form, in the solid state imaging device according to claim 1. The solid state imaging device according to claim 3 has the composition that uneven-shaped the pitch and height of the protruding part were set up 1 of the wavelength of incident light / 10 to 10 times, in the solid state imaging device according to claim 1 or 2.
[0010]The formation method of the sensor structure according to claim 4 forms hemispherical grain polysilicon on it, and etches the silicon oxide film under it from the gap between this hemispherical grain polysilicon while it forms a silicon oxide film on a sensor surface. In the formation method of the sensor structure according to claim 4, the formation method of the sensor structure according to claim 5 forms a trench in the sensor surface of the etching portion, after etching a silicon oxide film.
[0011]
[Function]In the solid state imaging device according to claim 1, when light enters into a sensor part aslant, the incident light is reflecting on the side surface of the protruding part which forms the uneven form of an incident plane peripheral edge part, and it does not enter to the charge transfer section side. Therefore, the substrate surface in a charge transfer section, the lower end surface of a light-shielding film, or the multiple echo between transfer electrodes does not happen, and does not enter into the transfer region of a charge transfer section. On the side surface of a yet another protruding part, by repeating a reflection, eventually, the light reflected on the side surface of the protruding part transmits, and photoelectric conversion is carried out to the substrate side. As a result, the sensitivity of a sensor part improves.
[0012]In the solid state imaging device according to claim 2, when the light which entered into the sensor part from the upper part transmits the uneven surface of an incident plane, the part reflects it. This reflected light is repeating a reflection on the side surface of a protruding part, and it transmits it to the substrate side eventually. That is, although a reflection of a certain amount of light in an incident plane is not avoided, the reflected light is also eventually incorporated into a sensor part. As a result, the sensitivity of a sensor part improves. In the solid state imaging device according to claim 3, the above-mentioned operation is effectively exerted by setting up uneven-shaped the pitch and height of a protruding part 1 of the wavelength of incident light / 10 to 10 times.
[0013]In the formation method of the sensor structure according to claim 4, a silicon oxide film is formed on a sensor surface, and hemispherical grain polysilicon is formed on it.
Hemispherical grain polysilicon is formed as a thing of fine particle diameter. A silicon oxide film

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is etched from the gap between this hemispherical grain polysilicon. A sensor surface is locally exposed and a minute protruding part is formed by this etching. In the formation method of the sensor structure according to claim 5, a trench is formed in the sensor surface exposed by etching, and the height of a protruding part is set up by this.

[0014]

[Working example]Hereinafter, the working example of the present invention is described in detail based on Drawings. Fig.1 is a section structure figure of the sensor part in the CCD area sensor concerning the present invention, and a vertical charge transfer section, and shows the A-A' arrowed cross-section of Fig.6. In Fig.1, the P well 13 is laminated via the overflow barrier 12 which consists of P layer on the N type silicon substrate 11.

[0015]HAD (Holl Accumulation Diode) which consists of the electron hole accumulation layer 14 which consists of P^+ layer where the sensor part 1 was formed in the surface side of the P well 13, and the signal-charge accumulation layer 15 which consists of N layer under it It is taking structure and is aiming at improvement in sensitivity, and reduction of dark current. This electron hole accumulation layer 14 and the signal-charge accumulation layer 15 are adjoined, and the channel stop part 16 is formed. The vertical charge transfer section 3 is constituted by the signal-charge transfer region 17 formed in the surface side of the substrate 11, and the transfer electrode 19 consisting of the polysilicon formed via the insulating layer 18 which consists of silicon oxide films (SiO_2) on the substrate surface.

[0016]Between the sensor part 1 and the vertical charge transfer section 3, photoelectric conversion is carried out by the sensor part 1, and the read-out gate section 2 for reading the signal charge accumulated in the signal-charge accumulation layer 15 to the vertical charge transfer section 3 is provided. As a gate electrode of this read-out gate section 2, the transfer electrode 19 is made to serve a double purpose by this example. And it reads except for the sensor part 1, and it provides so that the light-shielding film 20 which consists of aluminum etc. via the insulating layer 18 may cover the outside of the transfer electrode 19 on the gate section 2, the vertical charge transfer section 3, and the channel stop part 16.

[0017]In the above-mentioned sensor structure, even if there are few incident planes of the sensor part 1, a peripheral edge part, preferably the whole incident plane surface are making uneven form. The enlarged section of an example of this uneven form is shown in Fig.2. In the figure, each protruding part 21 which forms uneven form is set up so that conical shape may be made and the pitch p and height h may be 1 of the wavelength of incident light / about 10 to 10 times. As an example, when the wavelength of incident light is 400 nm - 700 nm, moreover, the pitch p of the protruding part 21 and height h are set as about [of pixel size / less than 1/10] at 0.04 micrometer - about 7 micrometers.

[0018]Even if light enters into the sensor part 1 aslant as are mentioned above, and when [of the incident plane of the sensor part 1] the peripheral edge part is making uneven form at least shows to Fig.3, it reflects on the slope (side surface) of the protruding part 21 of conical shape. Then, the reflected light will be reflected towards the lower part [not the upper part of the sensor part 1 but] side. Therefore, since the reflected light in the surface of the sensor part 1 does not repeat a multiple echo between the substrate surface, the lower end surface of the light-shielding film 20, or the transfer electrode 19 in the vertical charge transfer section 3 and an incident thing therefore does not have the reflected light to the vertical charge transfer section 3 side, a smear can be reduced substantially.

[0019]And since it will transmit to the substrate side eventually and photoelectric conversion also of the reflected light component will be carried out by repeating a reflection between the slopes of other protruding parts several times, the reflected light in the slope of the protruding part 21 of conical shape can improve the sensitivity of the sensor part 1. By the way, when the surface of the sensor part 1 is flat, a part of light which entered is transmitted to the substrate

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side, and it serves as a signal charge after photoelectric conversion, is accumulated, and serves as an effective signal. However, since the refractive index of silicon is larger than the transparent membrane (a color filter is included) generally formed on the sensor part 1, the actual condition is being reflected several 10% on the surface of the sensor part 1, and having lost light.

[0020]However, as shown in Fig.3, while transmitting the slope of the protruding part 21 of conical shape, the part will reflect, but the light which entered into the sensor part 1 from the upper part in this example by having made not only the peripheral edge part of the incident plane of the sensor part 1 but the whole incident plane surface into uneven form. It transmits to the substrate side eventually because the reflected light repeats a reflection on the slope concerned several times. Since photoelectric conversion will be performed by this also about the reflected light component which had been lost conventionally, the sensitivity of the sensor part 1 can be improved.

[0021]By forming sufficiently the vertical angle of the conical shape of the protruding part 21 in an acute angle, it becomes possible to suppress an upward reflection of incident light very low, and can improve the sensitivity of the sensor part 1 more. The problem of the flare, such as a cell ghost, is also solvable by the ability of an upward reflection of the sensor part 1 to be reduced. A cell ghost means here the phenomenon which a minute pixel cell is expanded and projects, when the light reflected by the sensor part 1 causes multiple interference by the optical system of the lens etc. which were mounted on the CCD area sensor.

[0022]These operations and effects are effectively exerted by moreover setting the pitch p of the protruding part 21 of conical shape, and height h as about [of pixel size / less than 1/10] at 1 of the wavelength of incident light / about 10 to 10 times, as mentioned previously. incidentally, if the pitch p of the protruding part 21 of conical shape and height h are too small, a reflective effect will be lost to incident light, and if too conversely large, the adverse effect of an and also [sensor form gives compared with the size of an element] will become big.

[0023]Although the protruding part 21 which forms the uneven form of a sensor surface was made into the thing of conical shape in this example, It may be not the thing limited to this form but protruding part of shape of **** abbreviated hemisphere shown, for example in Fig.4 21', and in short, if a sensor surface is not a flat surface but unevenness, the desired end can be attained.

[0024]Next, based on process drawing of Fig.5 (a) - (d), it describes about the formation method of the sensor structure mentioned above. First, in the (a) process 1, on the sensor part 1, it is thinner than the transfer electrode 18 top, for example, grows up a silicon oxide film (5 nm - about 30 nm) (SiO_2). Next, HSG (Hemispherical Grained: hemispherical grain) polysilicon (Poly-Si) is grown up into the whole surface with the fine particle diameter of about 0.1 micrometer.

[0025]If formation of this HSG polysilicon is faced, karyogenesis is carried out at low temperature by performing core attachment using Si_2H_6 gas. And polysilicon is formed at low temperature focusing on this. The grain density and the particle diameter of HSG are decided by Si_2H_6 gas mass flow and substrate temperature. Si_2H_6 partial pressure under core attachment is set to 10^{-5} - 10^{-4}Torr, for example. As a formation method of HSG polysilicon, the thing of disclosure is known [1147 pages - 1151 pages / of the 11 No. (1992) with an academic journal "applied physics" of volume / 61st], for example.

[0026](b) the process 2 -- the silicon oxide film of the gap between HSG polysilicon to the bottom -- a hydrogen fluoride (HF) system -- expose a sensor surface locally by etching with a solution. (c) Form a minute trench in a sensor surface by RIE etching of silicon in the process 3. At this time, unnecessary polysilicon is removed simultaneously. (d) In the process 4, heat-treat the surface for interface-state-density stabilization, carry out NSG/PSG deposition, and

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form the light-shielding film 19 by a henceforth usual CCD process.

[0027]As mentioned above, when forming the uneven form of a sensor surface, a thin silicon oxide film (SiO_2) is grown up on the sensor part 1, HSG polysilicon can be formed on it and uneven form can be easily formed also in the sensor surface where pixel size is small by etching a lower silicon oxide film from the gap between HSG polysilicon, and exposing a sensor surface locally.

[0028]This is not indispensable requirements although it presupposed that a minute trench is formed in the sensor surface exposed locally in the process 3. However, a trench is formed and there is an advantage which can set up the height of a protruding part arbitrarily by adjusting the depth. As a formation method of the uneven form of a sensor surface, it is not restricted to the above-mentioned formation method, and, otherwise, many things are considered. For example, when pixel size is large, it is also possible to form uneven form using lithography and etching.

[0029]The present invention is not limited to application to a CCD area sensor, and a sensor part can apply it to the solid state imaging device at large which has charge transfer sections, such as a CCD line (linear) sensor by which only single-tier powder was arranged.

[0030]

[Effect of the Invention]As described above, according to the invention according to claim 1, by [of each incident plane of a sensor part] having made the peripheral edge part into uneven form at least, Since the light which entered aslant reflects in a sensor part on the side surface of the protruding part which forms uneven form and does not enter into it to a charge transfer section, a smear can be reduced substantially. Since the light reflected on the side surface of the protruding part transmits and photoelectric conversion is eventually carried out by repeating a reflection on the side surface of a yet another protruding part to the substrate side, it is also being able to improve the sensitivity of a sensor part.

[0031]According to the invention according to claim 2, by having made not only the peripheral edge part of each incident plane of a sensor part but the whole surface into uneven form, Since this reflected light transmits and photoelectric conversion is eventually carried out by repeating a reflection on the side surface of a protruding part to the substrate side even if that part reflects, when the light which entered into the sensor part from that upper part transmits the uneven surface of an incident plane, the sensitivity of a sensor part can be improved.

According to the invention according to claim 3, the above-mentioned operation and effect can be exerted to the utmost by setting up uneven-shaped the pitch and height of a protruding part 1 of the wavelength of incident light / 10 to 10 times.

[0032]While forming a silicon oxide film on a sensor surface according to the invention according to claim 4, Since a sensor surface is locally exposed and a minute protruding part is formed by forming hemispherical grain polysilicon on it and having etched the silicon oxide film from the gap between this hemispherical grain polysilicon, A sensor part with small pixel size can also form the sensor surface in uneven form easily.

[0033]By having formed the trench in the sensor surface exposed by etching, after etching a silicon oxide film according to the invention according to claim 5, Since the height of a protruding part can be arbitrarily set up by adjusting the depth of the trench, the height of a protruding part can be set up the optimal to the wavelength of incident light.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a section structure figure showing one working example of the present invention.

[Drawing 2]It is an expanded sectional view of a sensor surface.

[Drawing 3]It is the figure showing behavior of incident light.

[Drawing 4]It is a cross sectional view showing the modification of the form of a protruding part.

[Drawing 5]It is process drawing of the formation method of the sensor structure by the present invention.

[Drawing 6]It is a schematic configuration diagram of a CCD area sensor.

[Drawing 7]It is a cross sectional view of an essential part showing a conventional case.

[Explanations of letters or numerals]

1 Sensor part

3 Vertical charge transfer section

5 Level charge transfer section

11 N type silicon substrate

12 Overflow barrier

14 Electron hole accumulation layer

15 Signal-charge accumulation layer

17 Signal-charge transfer region

19 Transfer electrode

20 Light-shielding film

21 Protruding part

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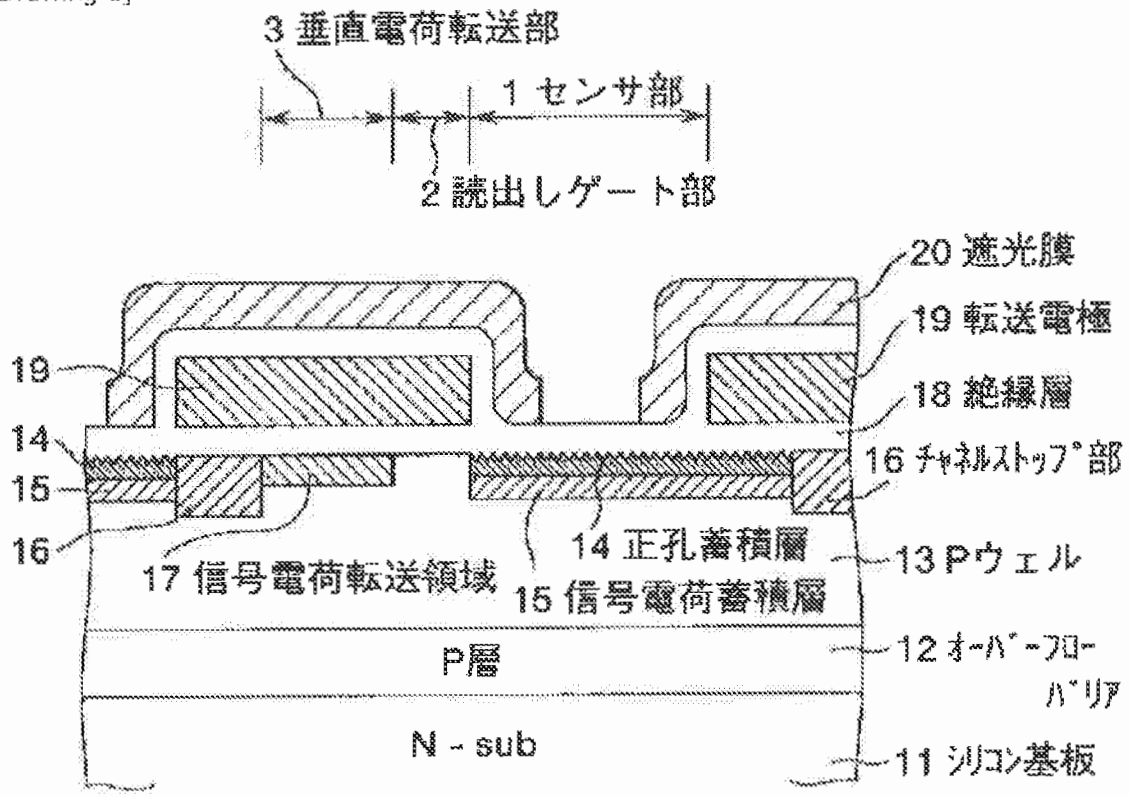
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DRAWINGS

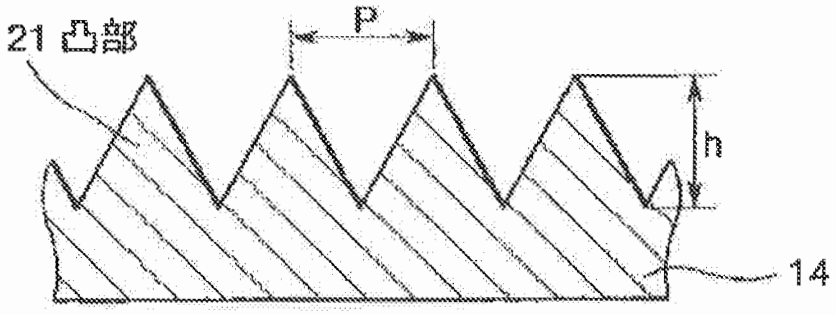
[Drawing 1]



本発明に係る断面構造図

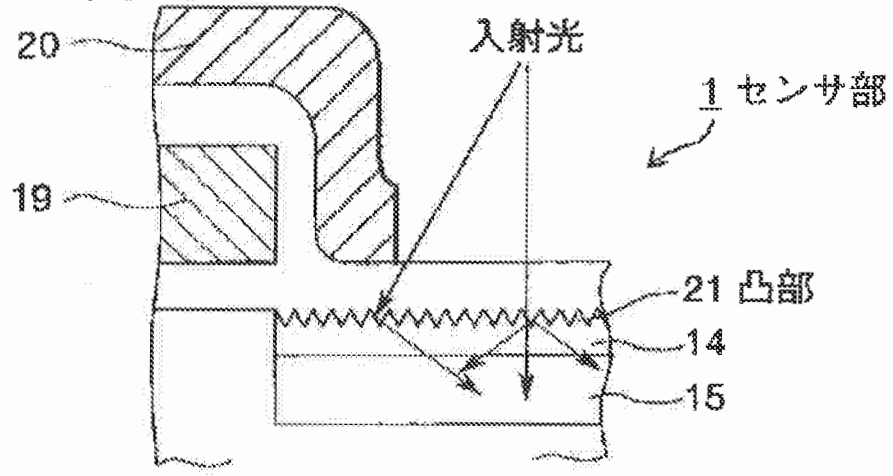
[Drawing 2]

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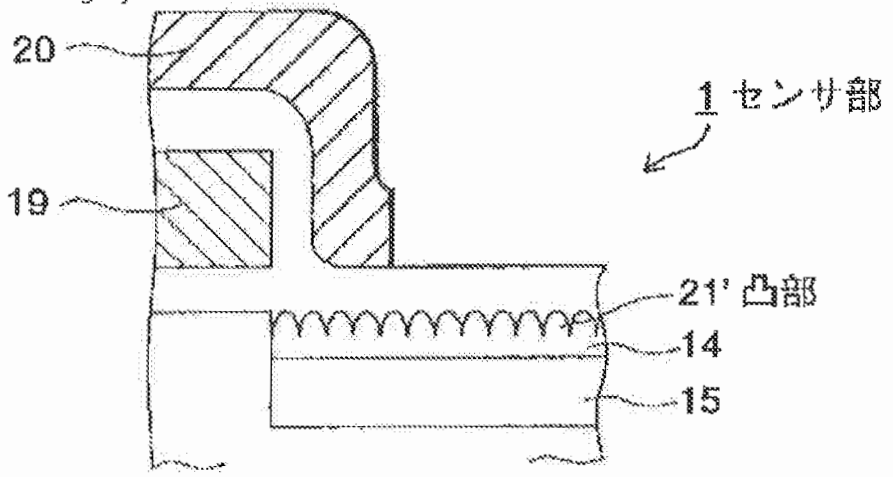
要部の拡大断面図

[Drawing 3]



入射光の振舞いを示す図

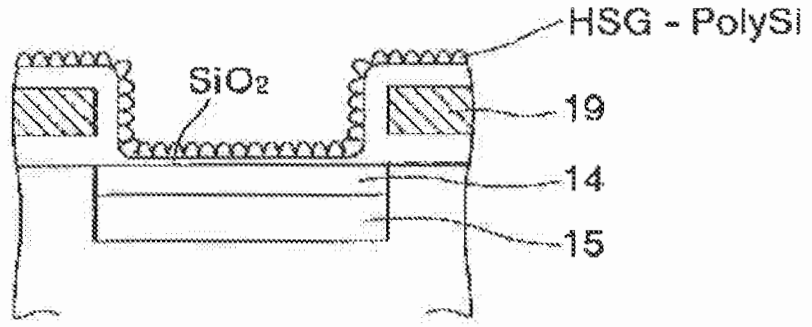
[Drawing 4]



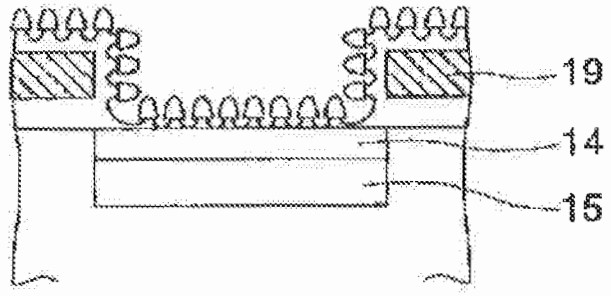
変形例を示す断面図

[Drawing 5]

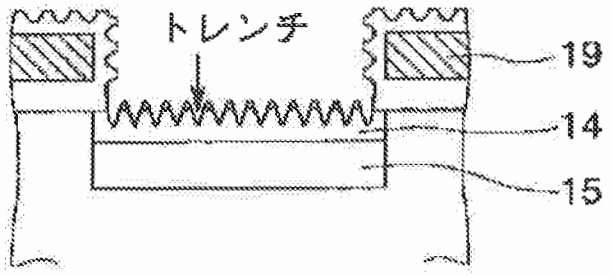
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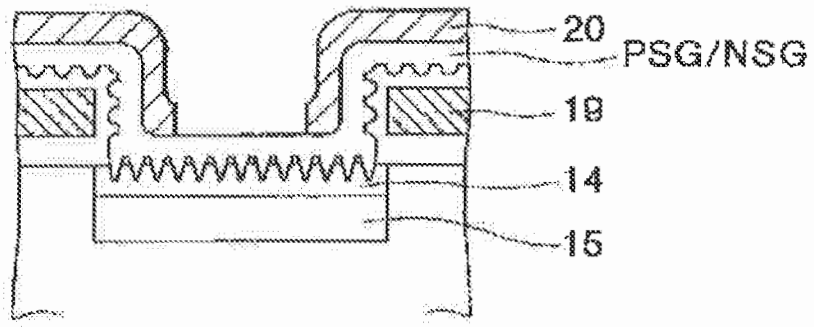
(a) 工程1



(b) 工程2



(c) 工程3

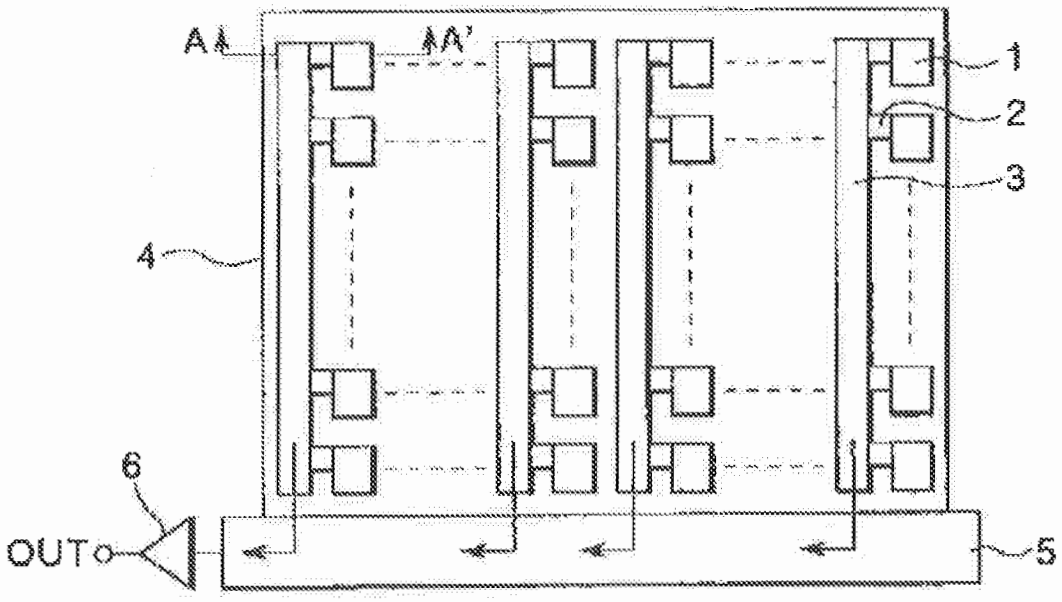


(d) 工程4

本発明に係る工程図

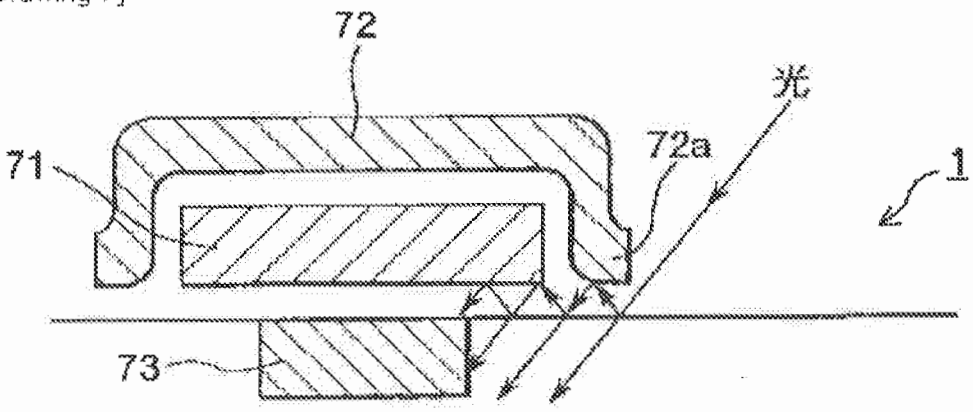
[Drawing 6]

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CCDエリアセンサの概略構成図

[Drawing 7]



従来例の要部断面図

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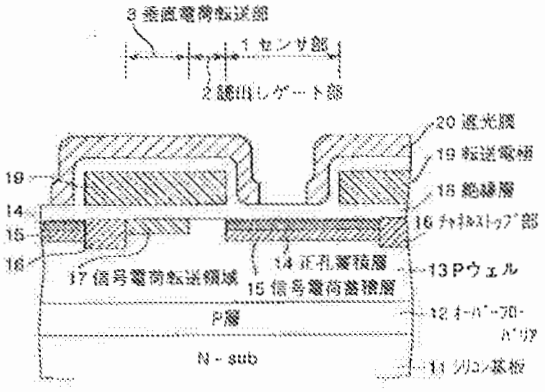
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(54)【発明の名称】　固体撮像装置及びそのセンサ構造の形成方法

(57)【要約】

【目的】　電荷転送部における基板表面と遮光膜の下端面又は転送電極との間での多重反射をなくし、スミアの低減を可能とした固体撮像装置のセンサ構造を提供する。

【構成】　複数個のセンサ部１とこのセンサ部から読み出された信号電荷を転送する垂直電荷転送部３とを具備するＣＣＤエリアセンサにおいて、センサ部１の各々の入射面を凸曲形状に形成し、センサ部１に斜めに入射した光が凸曲形状を形成する凸部で反射して信号電荷転送領域１７に入り込まないようにしたセンサ構造とする。



本発明に係る断面構造図

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【特許請求の範囲】
【請求項１】　入射光を光電変換してその信号電荷を蓄積する少なくとも１列分配列された複数個のセンサ部と、
前記複数個のセンサ部から読み出された信号電荷を転送する電荷転送部とを具備し、
前記複数個のセンサ部の各々の入射面の少なくとも周縁部が凸凹形状をなしていることを特徴とする固体撮像装置。
【請求項２】　前記複数個のセンサ部の各々の入射面全面が凸凹形状をなしていることを特徴とする請求項１記載の固体撮像装置。
【請求項３】　前記凸凹形状の凸部のピッチ及び高さは、入射光の波長の１／１０～１０倍に設定されていることを特徴とする請求項１又は２記載の固体撮像装置。
【請求項４】　入射光を光電変換してその信号電荷を蓄積する少なくとも１列分配列された複数個のセンサ部と、前記複数個のセンサ部から読み出された信号電荷を転送する電荷転送部とを具備した固体撮像装置におけるセンサ構造の形成方法であって、
センサ表面上にシリコン酸化膜を形成するとともに、その上に半球状グレインポリシリコンを形成し、
前記半球状グレインポリシリコンの隙間から前記シリコン酸化膜をエッチングすることを特徴とするセンサ構造の形成方法。
【請求項５】　前記シリコン酸化膜をエッチングした後、そのエッチング部分のセンサ表面にトレンチを形成することを特徴とする請求項４記載のセンサ構造の形成方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、固体撮像装置に関し、特に固体撮像装置におけるセンサ部の構造及びその形成方法に関する。
【０００２】
【従来の技術】固体撮像装置の一例として、例えばインターライン転送方式のＣＣＤ(Charge Coupled Device)エリアセンサの概略構成を図６に示す。同図において、水平及び垂直方向にて２次元配列されて入射光を光電変換し、その信号電荷を蓄積する複数個のセンサ部１と、これらセンサ部１の垂直列毎に配されかつ垂直ブランキング期間の一部にて読出しゲート部２を介して読み出された信号電荷を垂直方向に転送する垂直電荷転送部３とによって撮像部４が構成されている。
【０００３】この撮像部４において、センサ部１は例えばフォトダイオードからなり、垂直電荷転送部３はＣＣＤによって構成されている。センサ部１から垂直電荷転送部３に読み出された信号電荷は、水平ブランキング期間の一部にて１走査線に相当する部分ずつ順に水平転送部５へ転送される。この１走査線分の信号電荷は、水平

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電荷転送部５によって順次水平方向に転送される。
【０００４】水平電荷転送部５の出力側には、転送されてきた信号電荷を検出して信号電圧に変換する例えばＦＤＡ(Floating Diffusion Amplifier)からなる電荷検出部６が配されている。図７に、センサ部１及び垂直電荷転送部３の断面（図６のＡ・Ａ′矢視断面）構造の要部を示す。
【０００５】
【発明が解決しようとする課題】上記ＣＣＤエリアセンサにおける垂直電荷転送部３では、図７に示すように、センサ部１を除く部分、即ち転送電極７１の外側にアルミニウム等からなる遮光膜７２を形成することで、信号電荷転送領域７３への外部光の入射を遮断する構造を採っている。
【０００６】しかしながら、従来のセンサ構造では、図７から明らかなように、センサ部１の表面が平坦面として形成されているので、センサ部１に光が斜めに入射した場合、センサ表面で反射した光のうち遮光膜７２の下端面７２ａに入射する成分があり、この反射光成分が基板表面と遮光膜７２の下端面７２ａ又は転送電極７１との間で多重反射を繰り返し、最終的に信号電荷転送領域７３に飛び込んで光電子を発生し、スミア成分を増加させるという問題があった。
【０００７】本発明は、上記課題に鑑みてなされたものであり、その目的とするところは、電荷転送部における基板表面と遮光膜の下端面又は転送電極との間での多重反射をなくし、スミアの低減を可能とした固体撮像装置のセンサ構造及びその形成方法を提供することにある。
【０００８】
【課題を解決するための手段】請求項１記載の固体撮像装置は、入射光を光電変換してその信号電荷を蓄積する少なくとも１列分配列された複数個のセンサ部と、この複数個のセンサ部から読み出された信号電荷を転送する電荷転送部とを具備し、複数個のセンサ部の各々の入射面の少なくとも周縁部が凸凹形状をなした構成となっている。
【０００９】請求項２記載の固体撮像装置は、請求項１記載の固体撮像装置において、複数個のセンサ部の各々の入射面全面が凸凹形状をなした構成となっている。請求項３記載の固体撮像装置は、請求項１又は２記載の固体撮像装置において、凸凹形状の凸部のピッチ及び高さが、入射光の波長の１／１０～１０倍に設定された構成となっている。
【００１０】請求項４記載のセンサ構造の形成方法は、センサ表面上にシリコン酸化膜を形成するとともに、その上に半球状グレインポリシリコンを形成し、この半球状グレインポリシリコンの隙間からその下のシリコン酸化膜をエッチングする。請求項５記載のセンサ構造の形成方法は、請求項４記載のセンサ構造の形成方法において、シリコン酸化膜をエッチングした後、そのエッチン

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グ部分のセンサ表面にトレンチを形成する。

【００１１】

【作用】請求項１記載の固体撮像装置において、センサ部に光が斜めに入射したとき、その入射光は入射面周縁部の凸凹形状を形成する凸部の側面で反射することて、電荷転送部側へは入り込まない。したがって、電荷転送部における基板表面と遮光膜の下端面又は転送電極との間での多重反射は起こらず、よって電荷転送部の転送領域に入射しない。また、凸部の側面で反射した光がさらに他の凸部の側面で反射を繰り返すことで、最終的に基板側へ透過し、光電変換される。その結果、センサ部の感度が向上する。

【００１２】請求項２記載の固体撮像装置において、センサ部にその上方より入射した光は入射面の凸凹面を透過する際に、その一部が反射する。この反射した光は、凸部の側面で反射を繰り返すことで、最終的に基板側へ透過する。すなわち、入射面でのある程度の光の反射は避けられないが、その反射光も最終的にセンサ部へ取り込まれる。その結果、センサ部の感度が向上する。請求項３記載の固体撮像装置では、凸凹形状の凸部のピッチ及び高さを入射光の波長の１／１０～１０倍に設定することて、上記作用が有効に発揮される。

【００１３】請求項４記載のセンサ構造の形成方法において、センサ表面上にシリコン酸化膠を形成し、その上に半球状グレインポリシリコンを形成する。半球状グレインポリシリコンは微小粒径のものとして形成される。この半球状グレインポリンリコンの隙間からシリコン酸化膠をエッチングする。このエッチングにより、センサ表面が局所的に露出し、微小な凸部か形成される。請求項５記載のセンサ構造の形成方法において、エッチングによって露出したセンサ表面にトレンチを形成し、これによって凸部の高さを設定する。

【００１４】

【実施例】以下、本発明の実施例を図面に基づいて詳細に説明する。図１は、本発明に係るＣＣＤエリアセンサにおけるセンサ部及び垂直電荷転送部の断面構造図であり、図６のＡ－Ａ′矢視断面を示す。図１において、Ｎ型シリコン基板１１上にはＰ型からなるオーバーフローバリア１２を介してＰウェル１３が積層されている。

【００１５】センサ部１は、Ｐウェル１３の表面側に形成されたＰ＋層からなる正孔蓄積層１４と、その下のＮ層からなる信号電荷蓄積層１５とからなるＨＡＤ(Ｈｏｌｅ Accumulation Diode)構造を採ることで、感度の向上と暗電流の低減を図っている。この正孔蓄積層１４及び信号電荷蓄積層１５に隣接してチャネルストップ部１６が形成されている。垂直電荷転送部３は、基板１１の表面側に形成された信号電荷転送領域１７と、基板表面上にシリコン酸化膜(ＳｉＯ)よりなる絶縁層１８を介して形成されたポリンリコンよりなる転送電極１９とによって構成されている。

【００１６】また、センサ部１と垂直電荷転送部３の間には、センサ部１で光電変換され、信号電荷蓄積層１５に蓄積された信号電荷を垂直電荷転送部３へ読み出すための読出しゲート部２が設けられている。この読出しゲート部２のゲート電極として、本例では転送電極１９が兼用されている。そして、センサ部１を除いて読出しゲート部２、垂直電荷転送部３及びチャネルストップ部１６上には、絶縁層１８を介してアルミニウム等からなる遮光膜２０が転送電極１９の外側を覆うように設けられている。

【００１７】上記のセンサ構造において、センサ部１の入射面の少なくとも周縁部、好ましくは入射面全面が凸凹形状をなしている。この凸凹形状の一例の拡大断面を図２に示す。同図において、凸凹形状を形成する個々の凸部２１は円錐形状をなし、そのピッチｐ及び高さｈが入射光の波長の１／１０～１０倍程度になるように設定されている。一例として、入射光の波長を４００ｎｍ～７００ｎｍとしたとき、凸部２１のピッチｐ及び高さｈは、０．０４μｍ～７μｍ程度で、しかも画素サイズの１／１０程度以内に設定される。

【００１８】上述したように、センサ部１の入射面の少なくとも周縁部が凸凹形状をなしていることにより、図３に示すように、センサ部１に光が斜めに入射しても、円錐状の凸部２１の斜面（側面）で反射する。すると、その反射光はセンサ部１の上方側ではなく、その下方側に向けて反射することになる。したがって、センサ部１の表面での反射光が、垂直電荷転送部３における基板表面と遮光膜２０の下端面又は転送電極１９との間で多重反射を繰り返すことはなく、よってその反射光が垂直電荷転送部３側へ入射することはないので、スミアを大幅に低減できる。

【００１９】しかも、円錐状の凸部２１の斜面での反射光は、他の凸部の斜面との間で反射を何回か繰り返すことによって最終的に基板側へ透過し、反射光成分も光電変換されることになるため、センサ部１の感度を向上できる。ところで、センサ部１の表面が平坦な場合、入射した光の一部は基板側へ透過し、光電変換後信号電荷となって蓄積され、有効な信号となる。しかし、シリコンは屈折率が一般にセンサ部１上に形成される透明膠（カラーフィルタを含む）よりも大きいため、センサ部１の表面で数１０％は反射されてしまい、光を損失しているのが現状である。

【００２０】ところが、本実施例においては、センサ部１の入射面の周縁部のみならず、入射面全面を凸凹形状としたことにより、センサ部１に上方より入射した光は、図３に示すように、円錐状の凸部２１の斜面を透過するとともにその一部が反射することになるが、その反射光が当該斜面での反射を何回か繰り返すことで最終的に基板側へ透過する。これにより、従来損失となっていた反射光成分についても光電変換が行われることになる

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ため、センサ部１の感度を向上できる。

【００２１】なお、凸部２１の円錐状の頂角を十分に鋭角に形成することで、入射光の上方への反射を極めて低く抑えることが可能となり、センサ部１の感度をより向上できることになる。また、センサ部１の上方への反射を低減できることで、セルゴーストなどのフレアの問題も解消できる。ここに、セルゴーストとは、センサ部１で反射した光が、ＣＣＤエリアセンサ上にマウントされたレンズ等の光学系で多重干渉を起こすことにより、微小な画素セルが拡大されて映し出される現象を言う。

【００２２】これらの作用・効果は、円錐状の凸部２１のピッチｐ及び高さｈを、先述した如く入射光の波長の１／１０～１０倍程度に、しかも画素サイズの１／１０程度以内に設定することで有効に発揮される。ちなみに、円錐状の凸部２１のピッチｐ及び高さｈが小さすぎると、入射光に対して反射の効果はなくなり、逆に大きすぎると、素子のサイズに比べてセンサ形状が与える他への悪影響が大きなものとなる。

【００２３】なお、本実施例では、センサ表面の凸凹形状を形成する凸部２１を円錐状のものとしたが、この形状に限定されるものではなく、例えば図４に示す如き略半球状の凸部２１′であっても良く、要は、センサ表面が平坦面でなく、凸凹であれば、所期の目的を達成することができる。

【００２４】次に、上述したセンサ構造の形成方法について、図５（ａ）～（ｄ）の工程図に基づいて説明する。先ず、（ａ）工程１では、センサ部１上に転送電極１８上よりも薄い、例えば５ｎｍ～３０ｎｍ程度のシリコン酸化膜(SiO_2)を成長させる。次に、ＨＳＧ(Hemispherical Grained：半球状グレイン）ポリシリコン(Poly-Si)を全面に０．１μｍ程度の微小粒径で成長させる。

【００２５】このＨＳＧポリシリコンの形成に際しては、Si_2H_6ガスを用いて核付けを行うことによって低温で核発生させる。そして、これを中心に低温でポリシリコンの形成を行う。ＨＳＧの粒密度及び粒径は、Si_2H_6ガス流量及び基板温度によって決まる。また、核付け中のSi_2H_6分圧は、例えば10^{-3}～10^{-4}Ｔｏｒｒとする。ＨＳＧポリシリコンの形成方法としては、例えば学会誌「応用物理」第６１巻第１１号（１９９２）１１４７頁～１１５１頁に開示のものが知られている。

【００２６】（ｂ）工程２では、ＨＳＧポリシリコンの隙間から、下のシリコン酸化膜をフッ化水素（ＨＦ）系溶液でエッチングすることで、センサ表面を局所的に露出させる。（ｃ）工程３では、シリコンのＲＩＥエッチングにより、センサ表面に微小トレンチを形成する。このとき、不要なポリシリコンは同時に除去される。

（ｄ）工程４では、界面準位安定化のため表面を熱処理し、ＮＳＧ／ＰＳＧ堆積し、以降通常のＣＣＤプロセスによって遮光膜１９を形成する。

【００２７】上述したように、センサ表面の凸凹形状を形成するに際し、センサ部１上に薄いシリコン酸化膜(SiO_2)を成長させ、その上にＨＳＧポリシリコンを形成し、ＨＳＧポリシリコンの隙間から下のシリコン酸化膜をエッチングしてセンサ表面を局所的に露出させることで、画素サイズが小さいセンサ表面にも容易に凸凹形状を形成することができる。

【００２８】なお、工程３では、局所的に露出したセンサ表面に微小トレンチを形成するとしたが、これは必須の要件ではない。ただし、トレンチを形成し、その深さを調整することで凸部の高さを任意に設定できる利点がある。また、センサ表面の凸凹形状の形成方法としては、上記の形成方法に限られるものではなく、他にも種々考えられる。例えば、画素サイズが大きいときは、リソグラフィーとエッチングを使用して凸凹形状を形成することも可能である。

【００２９】また、本発明は、ＣＣＤエリアセンサへの適用に限定されるものではなく、センサ部が一列状だけ配列されたＣＣＤライン（リニア）センサ等、電荷転送部を有する固体撮像装置全般に適用し得るものである。

【００３０】

【発明の効果】以上説明したように、請求項１記載の発明によれば、センサ部の各々の入射面の少なくとも周縁部を凸凹形状としたことにより、センサ部に斜めに入射した光が凸凹形状を形成する凸部の側面で反射し、電荷転送部へは入り込まないため、スミアを大幅に低減できることになる。また、凸部の側面で反射した光がさらに他の凸部の側面で反射を繰り返すことで、最終的に基板側へ透過し、光電変換されるため、センサ部の感度を向上できることにもなる。

【００３１】請求項２記載の発明によれば、センサ部の各々の入射面の周縁部のみならず、全面を凸凹形状にしたことにより、センサ部にその上方より入射した光が入射面の凸凹面を透過する際にその一部が反射しても、この反射した光が凸部の側面で反射を繰り返すことで、最終的に基板側へ透過し、光電変換されるため、センサ部の感度を向上できることになる。なお、請求項３記載の発明によれば、凸凹形状の凸部のピッチ及び高さを入射光の波長の１／１０～１０倍に設定することにより、上記の作用・効果を最大限に発揮できることになる。

【００３２】請求項４記載の発明によれば、センサ表面上にシリコン酸化膜を形成するとともに、その上に半球状グレインポリシリコンを形成し、この半球状グレインポリシリコンの隙間からシリコン酸化膜をエッチングするようにしたことにより、センサ表面が局所的に露出し、微小な凸部が形成されるので、画素サイズの小さなセンサ部でも容易にそのセンサ表面を凸凹形状に形成することができる。

【００３３】請求項５記載の発明によれば、シリコン酸化膜をエッチングした後、エッチングによって露出したセンサ表面にトレンチを形成するようにしたことによ

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り、そのトレンチの深さを調整することによって凸部の高さを任意に設定することができるので、入射光の波長に対して凸部の高さを最適に設定できることになる。

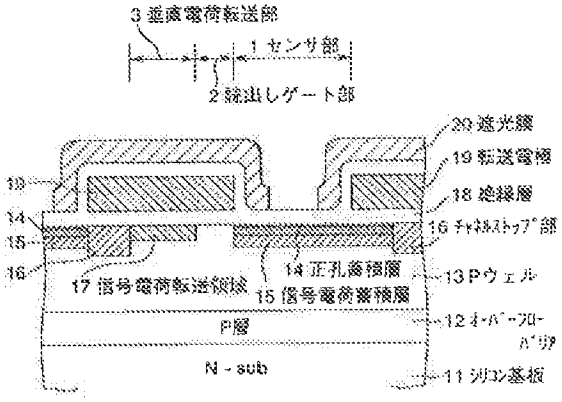
【図面の簡単な説明】

【図１】本発明の一実施例を示す断面構造図である。
【図２】センサ表面の拡大断面図である。
【図３】入射光の振舞いを示す図である。
【図４】凸部の形状の変形例を示す断面図である。
【図５】本発明によるセンサ構造の形成方法の工程図である。
【図６】ＣＣＤエリアセンサの概略構成図である。
【図７】従来例を示す要部の断面図である。

＊【符号の説明】

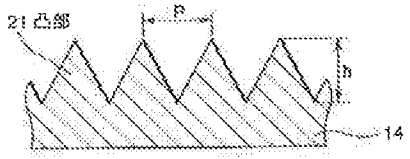
１　センサ部
３　垂直電荷転送部
５　水平電荷転送部
１１　Ｎ型シリコン基板
１２　オーバーフローバリア
１４　正孔蓄積層
１５　信号電荷蓄積層
１７　信号電荷転送領域
１９　転送電極
２０　遮光膜
２１　凸部

【図１】



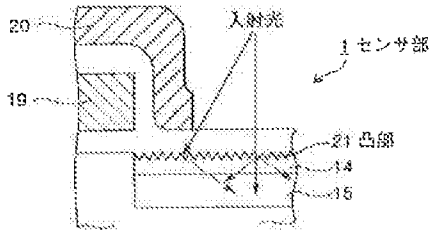
本発明に係る断面構造図

【図２】



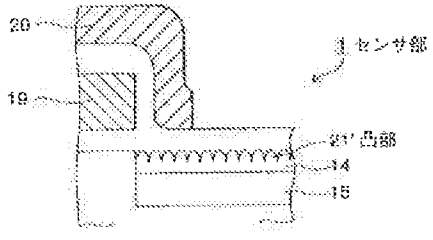
表部の拡大断面図

【図３】



入射光の振舞いを示す図

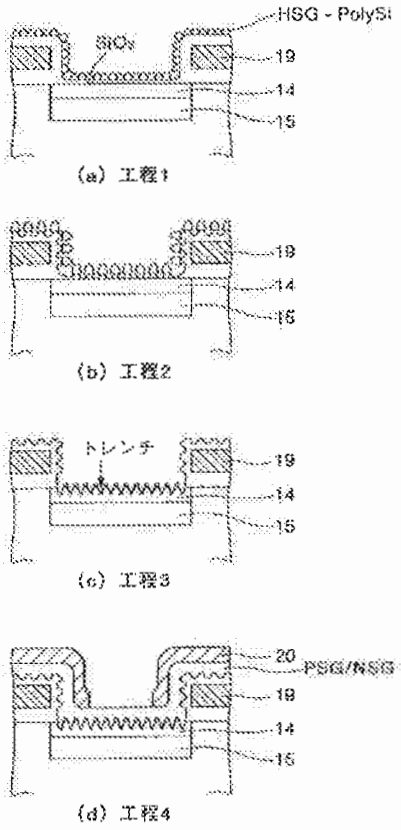
【図４】



変形例を示す断面図

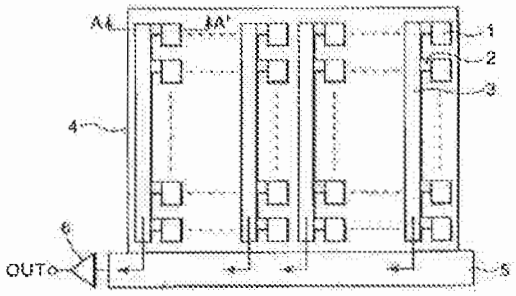
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【図5】



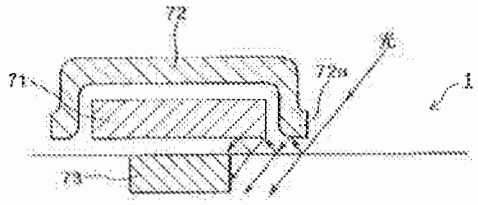
本発明に係る工程図

【図6】



CCDエリアセンサの概略構成図

【図7】



従来例の要部断面図

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Espacenet

Bibliographic data: JPH0774240 (A) — 1995-03-17

SEMICONDUCTOR DEVICE

Inventor(s): OOKA TSUKASA ± (OOKA TSUKASA, ; OOOKA TSUKASA)

Applicant(s): NEC CORP ± (NEC CORP, ; NIPPON ELECTRIC CO)

Classification: - international:***H01L21/76; H01L21/762; H01L27/12; H01L31/10;*** (IPC1-7): H01L21/762; H01L27/12; H01L31/10
- cooperative:

Application number: JP19930168606 19930615

Priority number (s): JP19930168606 19930615

Also published as: JP2590690 (B2)

Abstract of JPH0774240 (A)

PURPOSE:To enhance energy conversion efficiency by composing a dielectric isolation film of a combination materials having different refractive index thereby enhancing the reflection efficiency of incident light and reabsorbing the optical energy. CONSTITUTION:A silicon single crystal region 1 for forming a photodiode and a heavily doped impurity layer 2 are formed on a composite insulation film of oxide 6 and nitride 7 deposited on a single crystal substrate 5. Each photodiode element is isolated by an oxide 4 and polysilicon layer 3 and photodiodes, each having an anode 11 and a cathode 12, are formed on the silicon single crystal region 1 and connected in series through an Al electrode 13. A light impinging on the surface of the silicon single crystal region 1 passes through the silicon layer and reaches the composite insulation film with the energy thereof being absorbed in the vicinity of the P-N junction. The optical energy is reflected on the composite insulation film with high efficiency reaches again at the P-N junction where the optical energy is converted into an optoelectric current.

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(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平7－74240

(43)公開日　平成７年(1995)３月17日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｈ０１Ｌ　21/762					
27/12	Ｆ				
31/10					
		9169－4Ｍ	Ｈ０１Ｌ　21/ 76	Ｄ	
			31/ 10	Ａ	

審査請求　有　請求項の数２　ＦＤ　（全　３　頁）

(21)出願番号　特願平5－168606

(22)出願日　平成５年(1993)６月15日

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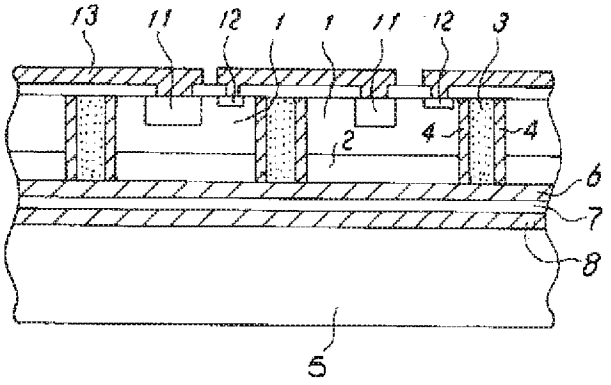
(74)代理人　弁理士　煤孫　耕郎

(54)【発明の名称】　半導体装置

(57)【要約】

【目的】　ＳＯＩ基板を用いたフォトダイオードを形成する場合、光電流を効率良く得るために、絶縁膜の光反射効率を向上させて、光エネルギーの吸収量を高める。

【構成】　ＳＯＩ基板を用いてフォトダイオードを形成し、光エネルギーの吸収効率を高めるために、入射した光を高効率で反射し、再吸収させる。そのために入射光を反射する半導体装置底面の絶縁分離膜を異なる屈折率を持った材質を組み合わせて複合化することで、反射率を高める。



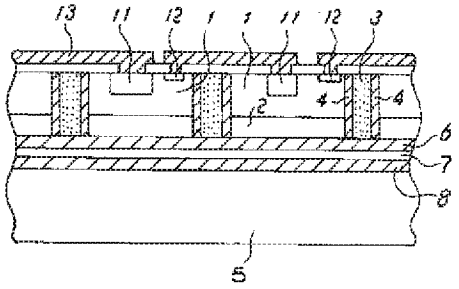
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【特許請求の範囲】
【請求項１】　単結晶シリコン基板と、前記単結晶シリコン基板の一表面上に設けられた複合絶縁膜と、前記複合絶縁膜上に設けられた単結晶シリコン層と、側面を接して設けられた絶縁膜と、前記絶縁膜間を充填する多結晶シリコン層とを有することを特徴とする半導体装置。
【請求項２】　複合絶縁膜が異なる材質の２種類以上の絶縁膜で構成されることを特徴とする請求項１に記載の半導体装置。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明はＳＯＩ基板を用いた半導体装置に関し、特にフォトダイオードに関する。
【０００２】
【従来の技術】従来のフォトダイオード半導体装置は、図２に示すように、多結晶シリコン２１を支持体として、ダイオード素子１つ１つを絶縁分離する酸化膜２２で単結晶シリコン層１を取り囲んだ誘電体分離構造を有している。これはダイオード素子を直列に直接し、高い起電力を得るため、ダイオード素子領域１つ１つを分離する必要があるためである。この従来の誘電体分離構造は、４００μｍ程度の厚い多結晶シリコンを有しているため、コストが高くなる、基板の反りが大きくなるなどの問題があった。
【０００３】これらの問題を解決するために、図３に示すような特開平３－１８００７０号や特開平３－１３６３４６号などによるＳＯＩ基板を用いたものが、提案されている。ここでフォトダイオード素子１つ１つの光電流を高めるために、光結合するキャリアの総量を多くする必要があり、各フォトダイオード素子領域のシリコン層厚さ１を厚くすることで対応している。図２に示す誘電体分離基板では、シリコン層１の厚さを厚くすることは容易であるが、図３に示すＳＯＩ基板はシリコン層１の厚さを厚くすると絶縁分離領域３及び４の形成が困難になるため、シリコン層１厚さを薄くしても、起電力を高めることができるように、特開昭６３－１３２４６０号に示されるように、シリコン層１と絶縁膜３１との界面に高不純物濃度層２を設けていた。
【０００４】
【発明が解決しようとする課題】この従来のＳＯＩ基板では、シリコン層が薄いため、絶縁膜を光が透過しやすく、起電効率を高めるために高不純物濃度層を形成しても、あまり起電効率が上らないという問題があった。
【０００５】
【課題を解決するための手段】本発明は、単結晶シリコン基板と、前記単結晶シリコン基板の一表面上に設けられた複合絶縁膜と、前記複合絶縁膜上に設けられた単結晶シリコン層と、側面を接して設けられた絶縁膜と、前記絶縁膜間を充填する多結晶シリコン層とを有する半導体装置である。
【０００６】
【作用】本発明においては、ＳＯＩ基板を用いた半導体装置は、フォトダイオードを形成するシリコン層と、各ダイオードを分離する絶縁領域と、光反射効率を高める複合絶縁膜と、シリコン層底部に設けられた高濃度不純物層と、支持基板となるシリコン基板とを備えており、シリコン層の表面上から光を受け、シリコン層（シリコン単結晶領域）を透過してＰ－Ｎ接合境界付近で吸収された光エネルギーは光電流となり、残りの光エネルギーは透過して複合絶縁膜に到達する。複合絶縁膜は、光エネルギーを高効率で反射し、再びＰ－Ｎ接合に達して、光電流に変換されるという作用をするものである。
【０００７】
【実施例】次に本発明の実施例について、図面を参照して説明する。図１は、本発明の一実施例の半導体装置の断面図である。支持体となる単結晶基板５上に絶縁酸化膜６及び８と窒化膜７で形成された複合絶縁膜上に、フォトダイオードを形成するシリコン単結晶領域１及び高濃度不純物層２が形成されており、各光フォトダイオード素子は、絶縁酸化膜４と、多結晶シリコン層３とで絶縁されている。シリコン単結晶領域１上には、アーノード１１、カソード１２を有するフォトダイオードが形成され、アルミ電極１３で各フォトダイオードは直列に接続されている。シリコン単結晶領域１の表面上から光を受け、シリコン層を透過してＰ－Ｎ接合境界付近で吸収された光エネルギーは、光電流となり、残りの光エネルギーは透過して複合絶縁膜に到達する。複合絶縁膜は、光エネルギーを高効率で反射し、再びＰ－Ｎ接合に達して、光電流に変換される。
【０００８】複合絶縁膜は、光エネルギーを効率的に反射するために、絶縁酸化膜６～８の材質、厚さを入射光の波長合わせ変更を行う。例えば、第１の実施例においては絶縁酸化膜６及び８の膜厚を１．０μｍ、絶縁膜７は、シリコン窒化膜０．１μｍを用い、第２の実施例では、絶縁酸化膜６及び８は２．０μｍを用い、絶縁膜７を多結晶シリコン膜０．１μｍを用いるなどである。第２の実施例は第１の実施例と構造は同じでものである。
【０００９】
【発明の効果】以上説明したように、本発明は、絶縁分離膜を異なった屈折率を持った材質のものを組み合わせて複合化し構成することにより、入射光の反射効率を高めて光エネルギーを再吸収させ、エネルギー変換効率を向上させることができる。
【図面の簡単な説明】
【図１】本発明の一実施例の断面図
【図２】従来の誘電体分離基板の半導体装置の断面図
【図３】従来のＳＯＩ基板の半導体装置の断面図
【符号の説明】
１　単結晶シリコン層
２　高濃度不純物層

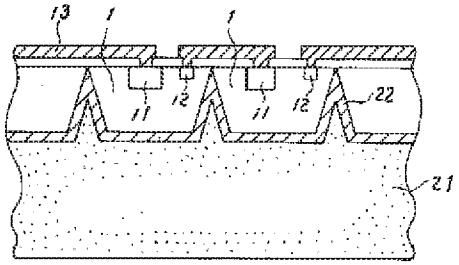
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３　多結晶シリコン層
４　絶縁酸化膜
５　単結晶シリコン基板
６　絶縁酸化膜
７　絶縁膜
８　絶縁酸化膜
１１　アノード
１２　カソード
１３　アルミ電極
２１　多結晶シリコン層
２２　絶縁酸化膜
３１　絶縁酸化膜

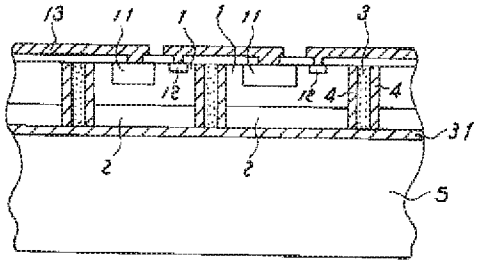
【図１】



【図２】



【図３】



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FABRICATING METHOD OF CMOS IMAGE SENSOR WITH REDUCED LOSS OF LIGHT

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DESCRIPTION KR20060020400

FIELD OF THE INVENTION [0001] The present invention relates to a CMOS image sensor,

FIG. 1A is a circuit diagram showing a unit pixel of a conventional CMOS image sensor,

1B shows a schematic structure of a conventional CMOS image sensor chip,

1C is a cross - sectional view illustrating a cross section of a pixel array portion and a logic region in a conventional CMOS image sensor,

FIGS. 2A to 2C are cross - sectional views illustrating a manufacturing process of a CMOS image sensor according to an exemplary embodiment of the present invention,

FIG. 2d is a plan view showing a state of a CMOS image sensor chip according to an embodiment of the present invention,

3 is a cross - sectional view showing a case where the technical idea of the present invention is applied to a unit pixel.

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Description of the Related Art [0002]

30 : Substrate 31: gate

32 : Spacer 33: Interlayer insulating film

34 : M1 contact 35: first metal wiring (M1)

36 : VIA 1 37, 39, 42: metal interlayer insulating film

38 : Second metal wiring (M2) 40: VIA 2

41 : Third metal wiring (M3) 43: VIA3

44 : Fourth metal wiring (M4) 45: mask

46 : Trench 47: oxide film

50 : Substrate 51: photodiode

52 : Gate 53: spacer

54 : Interlayer insulating film 55, 56: metal interlayer insulating film

57 : Oxide film

In particular, the present invention relates to a method of manufacturing a CMOS image sensor, in particular, an oxide film is buried in an edge region between a pixel array and

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a logic circuit to a depth of a second metal interconnection to receive light totally reflected by the oxide film back into the pixel array It is an invention that reduces the loss of light. Generally, an image sensor is a semiconductor device that converts an optical image into an electrical signal. Typical image sensor devices include a charge coupled device (CCD) and a CMOS image sensor. The charge - coupled device is a device in which individual MOS (Metal - Oxide - Silicon) capacitors are located in close proximity to each other and the charge carrier is stored and transferred to the capacitor. The Simos image sensor has a control circuit and a signal processing circuit (CMOS) technology that uses a signal processing circuit as a peripheral circuit to make MOS transistors as many as the number of pixels, and employs a switching system that sequentially detects the output using the MOS transistors. FIG. 1A is a circuit diagram showing a unit pixel composed of one photodiode PD and four MOS transistors in a conventional CMOS image sensor, which includes a photodiode 100 that receives light and generates photo charges, A transfer transistor 101 for transferring the photoelectrons collected in the photodiode 100 to the floating diffusion region 102; resetting the floating diffusion region 102 by setting the potential of the floating diffusion region to a desired value and discharging the charge; A drive transistor 104 having a gate to which a voltage of the floating diffusion region is applied to act as a source follower buffer amplifier and a switching transistor 104 serving as an addressing function And a select transistor 105 for performing the above operation. And a load transistor 106 is formed so that an output signal (Output Signal) can be read out of a unit pixel.

1B is a plan view showing an approximate view of a CMOS image sensor chip composed of a pixel array in which such a unit pixel is composed of several tens to millions of pixels, and a logic circuit portion and the like for processing image data. Referring to this, it can be seen that the logic circuit portion is arranged around the pixel array that receives the light. FIG. 1C is a cross - sectional view showing a cross section of a pixel array and a logic circuit portion together, and particularly, an interface between the pixel array and the logic circuit portion. FIG. First, in FIG. 1C, a pixel array region and a logic region are shown together. The pixel array region is a region where a light receiving portion composed of a photodiode or the like is formed. The logic region is a region where a general logic circuit for signal processing is mainly formed to be. That is, a gate electrode 12 having a spacer 13 is formed on a semiconductor substrate 11, and an interlayer insulating film 14 for insulation is formed on a substrate including a gate electrode. A metal contact 15 (M1 contact) for connecting the gate electrode 12 and the first metal interconnection 16 is formed on the gate electrode 12 through the interlayer insulating film 14. A first metal wiring 16 is patterned on the interlayer insulating film 14 and second to fourth metal wirings 18, 20 and 22 are stacked thereon. A metal wiring (Not shown) are provided for insulating the semiconductor substrate 1 from each other.

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Here, the metal interlayer insulating film typically has a structure in which an FSG film and a TEOS oxide film are stacked. 1C shows VIA 1 to VIA 3 for electrically connecting the respective metal wirings. Referring to FIG. 1C, it can be seen that in the conventional CMOS image sensor, the pixel array region is formed only up to the second metal interconnection (M2) 18, and the logic region is formed up to the fourth metal interconnection 22. In other words, in the pixel array region formed only up to the second metal wirings (M2) and (18), the oxide film series FGS film and the TEOS oxide film are formed in two layers to match the height of the fourth metal wiring in the logic region.

In the conventional image sensor having such a structure, the fourth metal wiring 22 of the logic region is formed of a shielding metal to surround the pixel array region, which is a boundary between the pixel array region and the logic region, And to reduce the loss of light incident on the edge of the region. However, according to the related art, the shielding metal using the fourth metal interconnection can not collect the incident light incident on the edge toward the pixel array, and has a disadvantage in that almost all of the incident light is lost due to the permittivity of the metal. SUMMARY OF THE INVENTION It is an object of the present invention to provide a method of manufacturing a CMOS image sensor in which light loss is reduced at an edge portion of a pixel array and a difference in light sensitivity between a center portion and an edge portion of the pixel array is reduced .

According to an aspect of the present invention, there is provided a method of manufacturing a CMOS image sensor having a pixel array region and a logic region, the method comprising: forming a second metal interconnection in the pixel array region and the logic region, Forming a fourth metal interconnection and forming an interlayer insulating film in the pixel array region; Etching the interlayer dielectric to form a trench of the second metal interconnection depth at an interface between the pixel array region and the logic region; And filling the trench with an oxide film having a refractive index lower than that of the interlayer insulating film. In the present invention, a film of an oxide film series is buried in the interface between the pixel array and the logic region to a depth of the second metal interconnection, and the incident light is totally reflected by the film of the oxide film series to be incident on the pixel array, The photosensitivity of the edge portion of the light emitting layer can be improved. DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings, so that those skilled in the art can easily carry out the technical idea of the present invention. FIGS. 2A to 2C are cross - sectional views illustrating a manufacturing process of a CMOS image sensor according to an

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embodiment of the present invention, and one embodiment of the present invention will be described with reference to FIG. First, the process up to the formation of the fourth metal interconnection 44 is the same as in the prior art. Referring to FIG. 1, an active layer and a field region defining a field region are formed on a semiconductor substrate having a pixel array region and a logic region. Such an element isolation film is not shown in FIG. 2A. Next, a photodiode is formed in the pixel array region. The photodiode is also not shown in FIG. 2A. Next, a gate electrode 31 having a spacer 32 is formed on a semiconductor substrate and a source / drain region (not shown) is formed. Next, an interlayer insulating film 33 is formed on the substrate 30 including the gate electrode 31, a certain portion of the interlayer insulating film 33 is removed, a conductive material is buried, and the gate electrode 31 and the first metal The metal contact 34 connecting the wiring 35 is formed.

Next, a first metal interlayer insulating film 37 is formed on the first metal interconnection 35, and then a first metal interconnection 37 is formed through the first metal interlayer insulating film 37 to connect the first metal interconnection and the second metal interconnection. Thereby forming a via (VIA 1) 36. Next, the second metal interconnection 38 is patterned on the first inter - metal - insulating film 37. Such a process proceeds in the same way in both the pixel array region and the logic region, but the subsequent process proceeds differently in the pixel array region and the logic region. That is, in the logic region, the process of sequentially stacking the third metal interconnection 41 and the fourth metal interconnection 44 proceeds. On the other hand, in the pixel array region, only the metal interlayer insulating films 39 and 42 are sequentially stacked, Wiring is not used. 2A, reference numerals 40 and 43 denote VIA 2 and VIA 3, respectively. After forming the fourth metal wirings 44 in this manner, the mask 45 is used to form the trench 46 at the interface between the pixel array region and the logic region. At this time, it is preferable that the depth of the trench is up to the second metal interconnection 38, and the depth of the trench is about 16000 in the 0.18 μ m class CMOS image sensor. Next, as shown in FIG. 2B, an oxide film 47 is deposited on the entire structure to fill the trench. Here, the oxide film 47 has a refractive index as low as about 1.41 and has a relatively lower refractive index than the metal interlayer insulating film on the pixel array side. Thus, in the embodiment of the present invention, the total light loss at the interface can be reduced through the total reflection using the oxide film 47. After the oxide film 47 is deposited, the etch - back process for the oxide film 47 is performed until the surface of the fourth metal interconnection 44 is exposed as shown in FIG. 2C. As a result, An oxide film remains in the form of a spacer, and the trench is buried with an oxide film. At this time, the thickness of the fourth metal interconnection is about 6500 ANGSTROM. Although not shown in FIG. 2C, conventional processes such as a passivation film, a color filter, and a microlens formation are performed to complete a CMOS image sensor.

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As a result, since an oxide film having a low refractive index is buried in the periphery of the pixel array, the light incident on the interface between the pixel array region and the logic region is totally reflected by the oxide film and re - enters the pixel array region. According to the present invention, it is possible to improve the photosensitivity at the edge portion of the pixel array and to reduce the difference in the photosensitivity between the center portion and the edge portion of the pixel array. FIG. 2D is a plan view showing a schematic view of a CMOS image sensor chip formed in accordance with an embodiment of the present invention. It can be seen that a low refractive index oxide film 47 is buried along the edge of the pixel array. 3 is a cross - sectional view showing a state in which the technical idea of the present invention is applied to a unit pixel. That is, FIG. 3 is a cross - sectional view showing one unit pixel as a center. Referring to FIG. First, formation of the second metal interconnection (M2) is the same as that of the first embodiment of the present invention. That is, the semiconductor substrate 50 is provided with a photodiode 51 for receiving light and converting it into an electric signal, and a gate electrode 52 having a spacer 53 is formed. An interlayer insulating film 54 is formed on the semiconductor substrate 50 including the gate electrode. On the interlayer insulating film, a first metal interconnection M 1 and a second metal interconnection M 2 laid out so as not to block the path of light incident on the photodiode, (M2) are formed. Reference numerals 54 and 55 denote metal interlayer insulating films. After the second metal interconnection line M2 is formed in this way, the upper part of the second metal interconnection line M2 is covered with the interlayer insulating film 56. Thereafter, the metal interlayer insulating film 56 is etched to form a trench, wherein the trench is formed at a position corresponding to the periphery of the photodiode. Next, when the trench is filled with the oxide film 57 having a low refractive index, the buried oxide film 57 functions to induce total reflection, thereby preventing loss of light incident on the photodiode. It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Will be apparent to those of ordinary skill in the art.

When the present invention is applied to a CMOS image sensor, it is possible not only to reduce the light loss occurring at the edge portion of the pixel array, but also to reduce the difference in sensitivity between the center portion and the edge portion of the pixel array.

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CLAIMS KR20060020400

1.
A method for manufacturing a CMOS image sensor having a pixel array region and a logic region, the method comprising the steps of forming a second metal interconnection in the pixel array region and the logic region, forming a fourth metal interconnection in the logic region, Forming an interlayer insulating film in the region; Etching the interlayer dielectric to form a trench of the second metal interconnection depth at an interface between the pixel array region and the logic region; And filling the trench with an oxide film having a refractive index lower than that of the interlayer insulating film.

2.
The method of claim 1, wherein the step of filling the trench with an oxide film having a refractive index lower than that of the interlayer insulating film includes: forming an interlayer insulating film including the trench and an oxide film having a refractive index lower than that of the interlayer insulating film ; And advancing the chivebeck process until the fourth metal interconnection is exposed. & Lt; Desc / Clms Page number 19 & gt;

3.
The method of claim 1, wherein the refractive index of the oxide film is 1.41 in the step of filling the trench with an oxide film having a refractive index lower than that of the interlayer insulating film.

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심사청구 : 없음

(54) 광 손실을 감소시킨 시모스 이미지센서의 제조방법

요약

본 발명은 시모스 이미지센서의 제조방법에 관한 것으로 특히, 픽셀어레이의 둘레부분에 상대적으로 저 굴절률을 갖는 산화막을 제 2 금속배선 깊이까지 매립함으로써 픽셀어레이의 엣지부분에서 발생하였던 광 손실을 절감한 발명이다. 이를 위한 본 발명은 픽셀 어레이 영역과 로직영역을 구비한 시모스 이미지센서의 제조방법에 있어서, 상기 픽셀 어레이 영역과 상기 로직 영역에 제 2 금속배선까지 형성한 후, 상기 로직 영역에는 제 4 금속배선까지 형성하며 상기 픽셀 어레이 영역에는 층간절연막을 형성하는 단계; 상기 층간절연막을 식각하여 상기 픽셀 어레이 영역과 상기 로직 영역 사이의 경계면에 상기 제 2 금속배선 깊이의 트렌치를 형성하는 단계; 및 상기 트렌치 내부를 상기 층간절연막 보다 굴절률이 낮은 산화막으로 매립하는 단계를 포함하여 이루어진다.

대표도

도 2c

색인어

시모스 이미지센서, 굴절률, 전반사, 픽셀 어레이, 광 손실

명세서

도면의 간단한 설명

도1a는 통상적인 시모스 이미지센서의 단위화소를 도시한 회로도,

도1b는 종래기술에 따른 시모스 이미지센서칩의 대략적인 구조를 도시한 도면,

도1c는 종래기술에 따른 시모스 이미지센서에서 픽셀 어레이 부분과 로직영역의 단면을 비교하여 도시한 단면도,

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도2a 내지 도2c는 본 발명의 일실시예에 따른 시모스 이미지센서의 제조공정을 도시한 공정단면도,

도2d는 본 발명의 일실시예에 따른 시모스 이미지센서 칩의 모습을 보인 평면도면,

도3은 본 발명의 기술적 사상을 단위화소에 적용한 경우를 도시한 단면도면.

도면의 주요부분에 대한 부호의 설명

30 : 기판 31 : 게이트

32 : 스페이서 33 : 층간절연막

34 : M1 콘택 35 : 제 1 금속배선(M1)

36 : VIA 1 37, 39, 42 : 금속층간절연막

38 : 제 2 금속배선(M2) 40 : VIA 2

41 : 제 3 금속배선(M3) 43 : VIA3

44 : 제 4 금속배선(M4) 45 : 마스크

46 : 트렌치 47 : 산화막

50 : 기판 51 : 포토다이오드

52 : 게이트 53 : 스페이서

54 : 층간절연막 55, 56 : 금속층간절연막

57 : 산화막

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 시모스 이미지센서의 제조방법에 관한 것으로 특히, 픽셀 어레이와 로직회로 사이의 엣지영역에 제 2 금속배선 깊이까지 산화막을 링 둘러 배리함으로써, 상기 산화막에 의해 전반사된 빛을 픽셀 어레이로 다시 받아들여 빛의 손실을 감소시킨 발명이다.

일반적으로, 이미지센서는 광학 영상(optical image)을 전기적 신호로 변환시키는 반도체 장치로서, 대표적인 이미지센서 소자로는 전하결합소자(Charge Coupled Device: CCD)와 시모스 이미지센서를 들 수 있다.

그 중에서 전하결합소자는 개개의 MOS(Metal-Oxide-Silicon) 캐패시터가 서로 매우 근접한 위치에 있으면서 전하 캐리어가 캐패시터에 저장되고 이송되는 소자이며, 시모스 이미지센서는 제어회로(control circuit) 및 신호처리회로(signal processing circuit)를 주변회로로 사용하는 CMOS 기술을 이용하여 화소(pixel)수 만큼 MOS 트랜지스터를 만들고 이것을 이용하여 순차적으로 출력을 검출하는 스위칭 방식을 채용하는 소자이다.

도1a는 통상의 시모스 이미지센서에서 1개의 포토다이오드(PD)와 4개의 MOS 트랜지스터로 구성된 단위화소(Unit Pixel)를 도시한 회로도로서, 빛을 받아 광전하를 생성하는 포토다이오드(100)와, 포토다이오드(100)에서 모아진 광전하를 플로팅확산영역(102)으로 운송하기 위한 트랜스퍼 트랜지스터(101)와, 원하는 값으로 플로팅 확산영역의 전위를 세팅

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하고 전하를 배출하여 플로팅 확산영역(102)를 리셋시키기 위한 리셋 트랜지스터(103)와, 플로팅 확산영역의 전압이 게이트로 입가되어 소스 팔로워 버퍼 증폭기(Source Follower Buffer Amplifier) 역할을 하는 드라이브 트랜지스터(104)와, 스위칭(Switching) 역할로 어드레싱(Addressing) 역할을 수행하는 셀렉트 트랜지스터(105)로 구성된다. 단위 화소 밖에는 출력신호(Output Signal)를 읽을 수 있도록 로드(load) 트랜지스터(106)가 형성된 모습을 도시하고 있다.

도1b는 이러한 단위화소가 수십 내지 수백만개 구비된 픽셀 어레이를 비롯하여 화상 데이터를 처리하는 로직회로부 등으로 구성된 시모스 이미지센서 칩의 대략적인 모습을 도시한 평면도이다. 이를 참조하면 빛을 수광하는 픽셀 어레이의 주변으로 로직회로부가 배치되어 있음을 알 수 있다.

도1c는 픽셀어레이와 로직회로부의 단면을 함께 도시한 단면도면으로 특히, 픽셀 어레이와 로직회로부의 경계면을 중점적으로 도시한 도면으로, 도1c를 참조하여 종래기술의 문제점을 설명하면 다음과 같다.

먼저, 도1c에는 픽셀 어레이 영역과 로직 영역이 함께 도시되어 있는 바, 픽셀어레이 영역은 포토다이오드 등으로 구성된 수광부가 형성되어 있는 영역이며, 로직영역은 신호처리를 위한 일반적인 논리회로가 중점적으로 형성된 부분이다.

즉, 반도체 기판(11) 상에는 스페이서(13)를 구비한 게이트 전극(12)이 형성되어 있으며, 게이트 전극을 포함한 기판 상에는 절연을 위한 층간절연막(14)이 형성되어 있다. 그리고 게이트 전극(12) 상에는 층간절연막(14)을 관통하여 게이트 전극(12)과 제 1 금속배선(16)을 연결하는 금속콘택(15)(M1 contact)이 형성되어 있다.

또한, 층간절연막(14) 상에는 제 1 금속배선(16)이 패터닝되어 있으며, 그 위로는 제 2 내지 제 4 금속배선(18, 20, 22)이 적층되어 형성되며, 각 금속배선 사이에는 금속배선들을 절연하기 위한 금속층간절연막(도면부호는 부여하지 않음)이 각각 구비되어 있다. 여기서 금속층간절연막은 통상적으로 FSG 막과 TEOS 산화막이 적층된 구조를 갖고 있음을 알 수 있다. 또한, 도1c에는 각각의 금속배선을 전기적으로 연결하기 위한 VIA 1 내지 VIA 3 가 도시되어 있다.

도1c를 참조하면 종래의 시모스 이미지센서에서, 픽셀 어레이 영역은 제 2 금속배선(M2)(18)까지만 형성되어 있으며, 로직영역은 제 4 금속배선(22)까지 형성되어 있음을 알 수 있다.

즉, 제 2 금속배선(M2)(18)까지만 형성된 픽셀어레이 영역에서는 산화막 계열의 FGS 막과 TEOS 산화막이 2 겹씩 형성되어, 로직 영역의 제 4 금속배선과 높이를 맞추고 있다.

이와같은 구조의 종래 이미지센서에서는, 로직 영역의 제 4 금속배선(22)을 실딩 메탈(shielding metal)로 형성하여 픽셀 어레이 영역을 둘러싸고 있는데, 이는 픽셀 어레이영역과 로직영역간의 경계임을 나타내는 동시에 픽셀 어레이 영역의 가장자리로 입사하는 빛의 손실을 감소시키기 위한 목적도 있었다.

하지만, 종래기술에 따라 제 4 금속배선을 이용한 실딩 메탈은 엣지로 입사하는 입사광을 픽셀 어레이 쪽으로 모아주지 못하고, 금속의 특성상 유전율에 의해 거의 대부분을 손실하는 단점이 있었다.

발명이 이루고자 하는 기술적 과제

본 발명은 상기한 종래의 문제점을 해결하기 위한 것으로, 픽셀 어레이의 엣지부분에서 광손실을 감소시키며 나아가 픽셀 어레이의 중심부분과 엣지부분의 광감도 차이를 줄인 시모스 이미지센서 제조방법을 제공함을 목적으로 한다.

발명의 구성 및 작용

상기한 목적을 달성하기 위한 본 발명은, 픽셀 어레이 영역과 로직영역을 구비한 시모스 이미지센서의 제조방법에 있어서, 상기 픽셀 어레이 영역과 상기 로직 영역에 제 2 금속배선까지 형성한 후, 상기 로직 영역에는 제 4 금속배선까지 형성하며 상기 픽셀 어레이 영역에는 층간절연막을 형성하는 단계; 상기 층간절연막을 식각하여 상기 픽셀 어레이 영역과 상기 로직 영역 사이의 경계면에 상기 제 2 금속배선 깊이의 트렌치를 형성하는 단계; 및 상기 트렌치 내부를 상기 층간절연막 보다 굴절률이 낮은 산화막으로 매립하는 단계를 포함하여 이루어진다.

본 발명에서는 픽셀 어레이와 로직 영역의 경계면에 제 2 금속배선 깊이까지 산화막 계열의 막을 매립시켜, 입사된 빛이 산화막 계열의 막에 의해 전반사되어 픽셀 어레이 쪽으로 입사하도록 유도함으로써 빛의 손실을 막고 픽셀 어레이의 엣지부분의 광감도를 향상시킬 수 있었다.

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이하, 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 본 발명의 기술적 사상을 용이하게 실시할 수 있을 정도로 상세히 설명하기 위하여, 본 발명의 가장 바람직한 실시예를 첨부된 도면을 참조하여 설명한다.

도2a 내지 도2c는 본 발명의 일실시예에 따른 시모스 이미지센서의 제조공정을 도시한 공정단면도로써 이를 이을 참조하여 본 발명의 일실시예를 설명한다.

우선, 제 4 금속배선(44)을 형성하기 까지의 공정은 종래기술과 동일하다.

이를 참조하면 먼저, 픽셀 어레이 영역과 로직영역을 갖는 반도체 기판 상에 활성영역과 필드영역을 정의하는 소자분리막을 형성한다. 이러한 소자분리막은 도2a에는 도시하지 않았다.

다음으로 픽셀 어레이 영역에 포토다이오드를 형성한다. 포토다이오드 역시 도2a에는 도시되어 있지 않다. 다음으로 반도체 기판 상부에 스페이서(32)를 구비한 게이트 전극(31)을 형성하고 소스/드레인 영역(미도시)을 형성한다.

다음으로, 게이트 전극(31)을 포함한 기판(30) 상부에 층간절연막(33)을 형성한 후, 층간절연막(33)을 일정부분 제거하고 전도물질을 매립하여 게이트 전극(31)과 제 1 금속배선(35)을 연결하는 금속콘택(34)을 형성한다.

이어서, 제 1 금속배선(35)의 상부에 제 1 금속층간절연막(37)을 형성한 후, 제 1 금속층간절연막(37)을 관통하여 제 1 금속배선과 제 2 금속배선을 연결하는 제 1 비아(VIA 1)(36)를 형성한다.

다음으로 제 1 금속층간절연막(37) 상에 제 2 금속배선(38)을 패터닝한다.

이와같은 공정은 픽셀어레이 영역과 로직영역에서 모두 동일하게 진행되나, 이후의 공정은 픽셀어레이 영역과 로직영역에서 달리 진행된다.

즉, 로직영역에서는 제 3 금속배선(41) 및 제 4 금속배선(44)이 차례로 적층되는 공정이 진행되는 반면에, 픽셀 어레이 영역에서는 금속층간절연막(39, 42)만이 차례로 적층되며 더이상의 금속배선은 사용되지 않는다.

도2a에서 미설명 부호 40, 43 은 각각 VIA 2 와 VIA 3 를 나타낸다.

이와같이 제 4 금속배선(44)까지 형성한 다음, 마스크(45)를 이용하여 픽셀어레이 영역과 로직영역 사이의 경계면에 트렌치(46)를 형성한다. 이때, 트렌치의 깊이는 제 2 금속배선(38)까지로 하며 0.18㎛ 급 시모스 이미지센서에서는 트렌치의 깊이가 16000Å 정도 되는 것이 바람직하다.

다음으로, 도2b에 도시된 바와같이 전체 구조상에 산화막(47)을 증착하여 트렌치를 매립한다.

여기서, 산화막(47)은 1.41 정도의 낮은 굴절률을 갖고 있으며, 픽셀 어레이쪽의 금속층간절연막 보다는 상대적으로 낮은 굴절률을 갖고 있다. 이와같이 본 발명의 일실시예에서는 상기의 산화막(47)을 이용한 전반사를 통해 경계면에서의 빛 손실을 줄일 수 있었다.

이와같이 산화막(47)을 증착한 다음에는 도2c에 도시된 바와같이 제 4 금속배선(44)의 표면이 드러날 때까지 산화막(47)에 대한 에치백 공정을 진행하게 되면, 제 4 금속배선의 측면에는 스페이서 형태로 산화막이 남게 되며, 트렌치는 산화막으로 매립된다. 이때, 제 4 금속배선의 두께는 6500Å 정도 된다.

이후에 도2c에는 도시되어 있지 않지만, 패시베이션막, 칼라필터, 마이크로렌즈 형성 등의 통상적인 공정을 진행하여 시모스 이미지센서를 완성한다.

결과적으로 픽셀어레이의 주변으로는 저 굴절률을 갖는 산화막이 매립되어 있으므로, 픽셀 어레이 영역과 로직영역사이의 경계면으로 입사하는 빛은 산화막에 의해 전반사되어 픽셀 어레이 영역으로 재입사하게 된다.

본 발명에서는 이러한 점을 이용하여 픽셀 어레이의 엣지부분에서의 광감도를 향상시켜 줄 수 있었으며 또한, 픽셀 어레이의 중앙부분과 엣지부분의 광감도 차이도 감소시킬 수 있었다.

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도2d는 본 발명의 일실시예에 따라 형성된 시모스 이미지센서 칩의 대략적인 모습을 도시한 평면도로써, 픽셀 어레이의 가장자리를 따라 저 굴절률의 산화막(47)이 매립되어 있음을 알 수 있다.

도3은 본 발명의 기술적 사상을 단위화소에 적용한 모습을 도시한 단면도이다. 즉, 도3은 하나의 단위화소를 중심으로 그 단면을 도시한 도면으로 이를 참조하여 설명한다.

먼저, 제 2 금속배선(M2)을 형성하기 까지는 본 발명의 제 1 실시예와 동일하다. 즉, 반도체 기판(50)에는 빛을 수광하여 전기신호로 변환하는 포토다이오드(51)가 형성되어 있으며, 또한 스페이서(53)을 구비한 게이트 전극(52)이 형성되어 있다.

또한, 게이트 전극을 포함한 반도체 기판(50) 상에는 층간절연막(54)이 형성되어 있으며, 층간절연막 상에는 포토다이오드로 입사하는 빛의 진로를 막지 않도록 레이아웃된 제 1 금속배선(M1) 및 제 2 금속배선(M2)이 형성되어 있다.

미설명 부호 54, 55 는 금속층간절연막이다.

이와같이 제 2 금속배선(M2)까지 형성한 후에는 그 상부를 금속층간절연막(56)으로 덮은 공정이 진행된다. 이후, 상기 금속층간절연막(56)을 식각하여 트렌치를 형성하되, 트렌치는 포토다이오드의 둘레에 대응하는 위치에 형성한다.

다음으로, 트렌치를 저 굴절률의 산화막(57)으로 매립하게 되면, 매립된 산화막(57)이 전반사를 유도하는 역할을 하여 포토다이오드로 입사하는 빛의 손실을 방지할 수 있게 된다.

이상에서 설명한 바와 같이 본 발명은 전술한 실시예 및 첨부된 도면에 의해 한정되는 것이 아니고, 본 발명의 기술적 사상을 벗어나지 않는 범위 내에서 여러 가지 치환, 변형 및 변경이 가능함이 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자에게 있어 명백할 것이다.

발명의 효과

본 발명을 시모스 이미지센서에 적용하게 되면, 픽셀 어레이의 엣지부분에서 발생하였던 광 손실을 절감할 수 있을 뿐 아니라 나아가 픽셀 어레이의 중앙부분과 엣지부분과의 광 감도 차이를 줄일 수 있는 장점이 있다.

(57) 청구의 범위

청구항 1.

픽셀 어레이 영역과 로직영역을 구비한 시모스 이미지센서의 제조방법에 있어서,

상기 픽셀 어레이 영역과 상기 로직 영역에 제 2 금속배선까지 형성한 후, 상기 로직 영역에는 제 4 금속배선까지 형성하며 상기 픽셀 어레이 영역에는 층간절연막을 형성하는 단계;

상기 층간절연막을 식각하여 상기 픽셀 어레이 영역과 상기 로직 영역 사이의 경계면에 상기 제 2 금속배선 깊이의 트렌치를 형성하는 단계; 및

상기 트렌치 내부를 상기 층간절연막 보다 굴절률이 낮은 산화막으로 매립하는 단계

를 포함하여 이루어지는 시모스 이미지센서의 제조방법.

청구항 2.

제 1 항에 있어서,

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상기 트렌치 내부를 상기 층간절연막 보다 굴절률이 낮은 산화막으로 매립하는 단계는,

상기 트렌치를 포함하는 층간절연막과 상기 제 4 금속배선 상부에 상기 층간절연막 보다 굴절률이 낮은 산화막을 적층형성하는 단계; 및

상기 제 4 금속배선의 노출될 때 까지 에치백 공정을 진행하는 단계

을 포함하여 이루어지는 것을 특징으로 하는 시모스 이미지센서의 제조방법.

청구항 3.

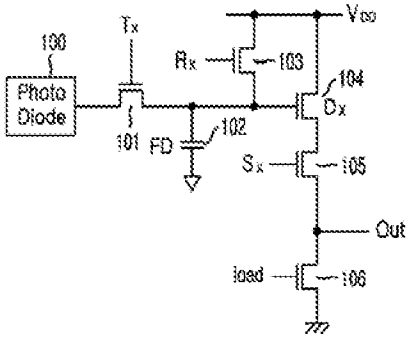
제 1 항에 있어서,

상기 트렌치 내부를 상기 층간절연막 보다 굴절률이 낮은 산화막으로 매립하는 단계에서,

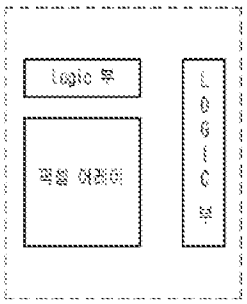
상기 산화막의 굴절률은 1.41 인 것을 특징으로 하는 시모스 이미지센서의 제조방법.

도면

도면1a

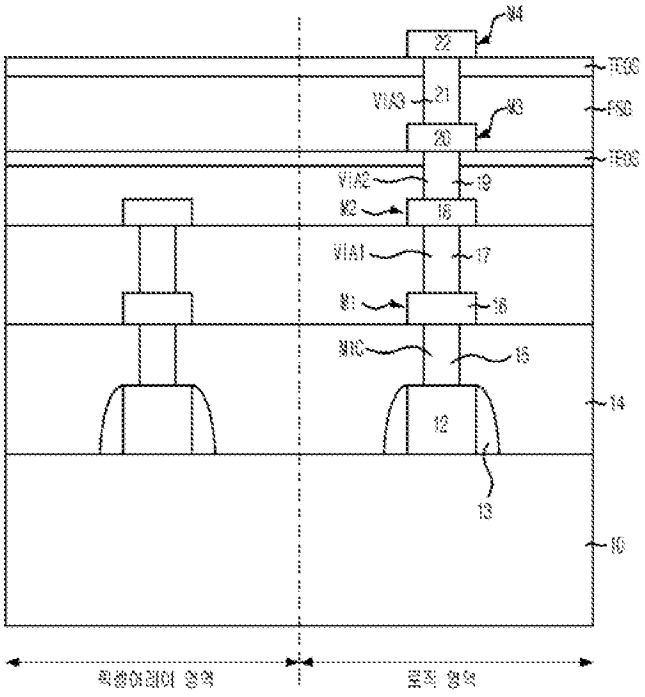


도면1b

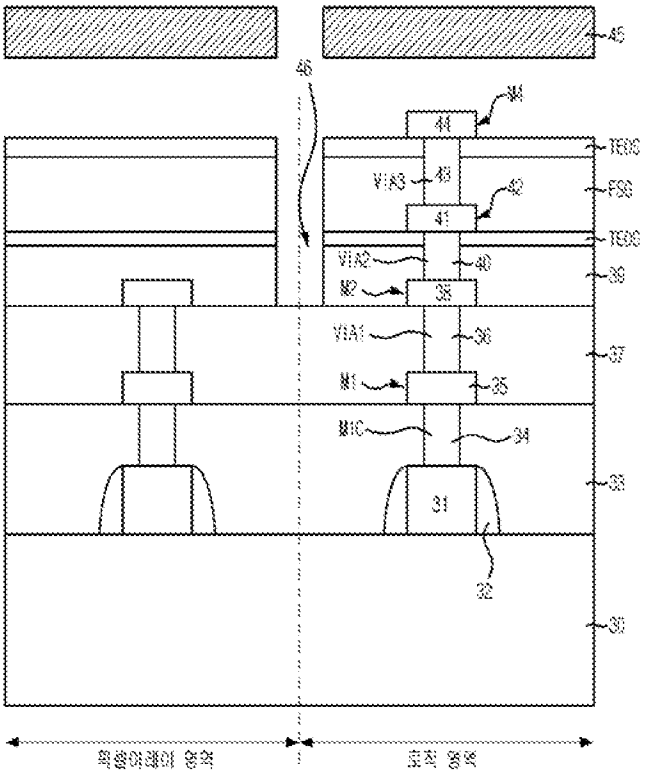


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도면1c

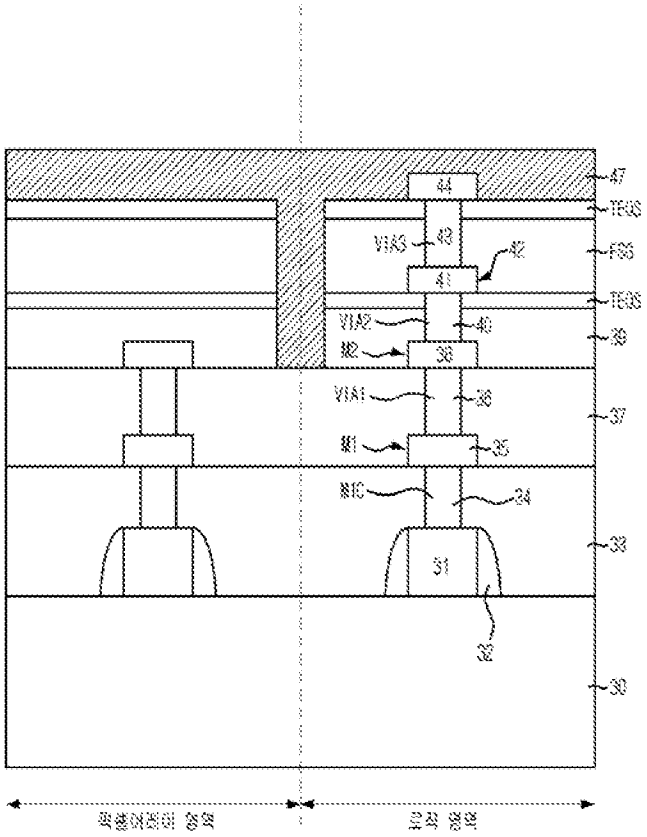


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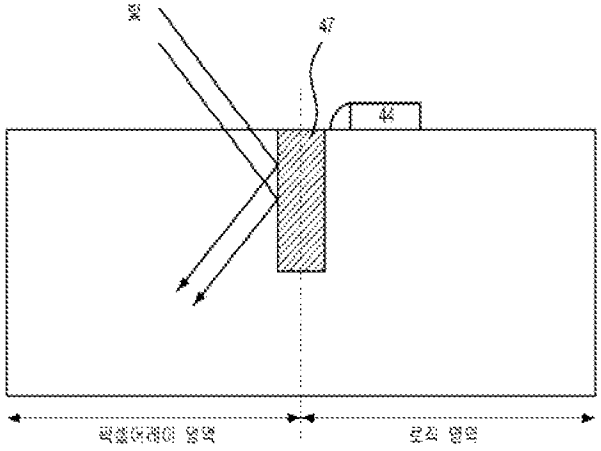


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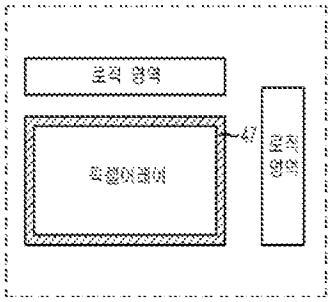


도면2c

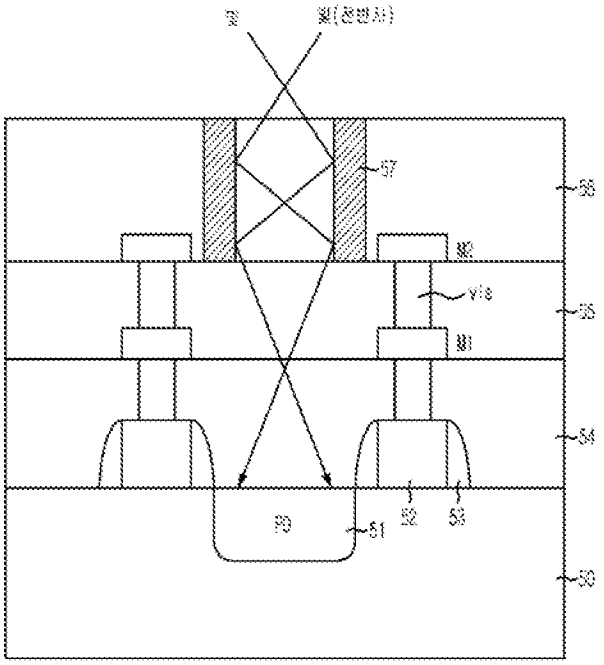


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도면2



도면3



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Espacenet

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BACK ILLUMINATED CMOS IMAGE SENSORS WITH DEEP TRENCH ISOLATION AND METHOD FOR PRODUCING THE SAME

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Abstract of KR20080014301 (A)

A back illuminated CMOS image sensor having a deep trench device isolating film and a method for producing the same are provided to prevent an electrical crosstalk and an optical crosstalk between pixels by isolating a photo diode of a pixel array using a device isolating film with a deep trench structure. A back illuminated CMOS image sensor comprises a device isolating film with a deep trench structure(13), a photo diode(11), a pixel circuit(20), and a lens(30). The device isolating film with the deep trench structure is formed by extending from a first side to a second side of a semiconductor substrate(10). The photo diode is defined by the device isolating film with the deep trench structure, and is formed by extending from a first side to a second side of the semiconductor substrate. The pixel circuit adjacent to the first side of the semiconductor substrate is formed. The lens adjacent to the second side of the semiconductor substrate is formed.

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DESCRIPTION KR20080014301

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a back - illuminated CMOS image sensor including a deep trench isolation film,

1 is a schematic cross - sectional view of a pixel array region of a conventional back - illuminated CMOS sensor.

2 is a schematic cross - sectional view of a pixel array region of a chip edge portion of a conventional back - illuminated CMOS sensor.

3 is a schematic cross - sectional view of a pixel array region of a back - illuminated CMOS image sensor according to an embodiment of the present invention.

FIG. 4 is a schematic flowchart for explaining a method of fabricating a back - illuminated CMOS image sensor according to the present invention in order.

Description of the Related Art

10: Semiconductor substrate 11: Photodiode

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13: Deep trench isolation film 20:

30: Lens part 31: Color filter

33: Micro lens 40: Support substrate

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a CMOS image device, and more particularly, to a back illuminated CMOS image sensor capable of preventing cross talk and a method of manufacturing the same. A typical image sensor is a semiconductor device that converts an optical image into an electrical signal. Such an image sensor can be classified into a CCD (charge coupled device) and a CMOS image sensor (CIS). Image sensors are based on a two - dimensional array of pixels. Each pixel includes a sensing element that can convert a portion of the optical image into an electrical signal. The electrical signals are used, for example, to reproduce the optical image on the display. A CMOS image sensor is a device having a photodiode for receiving an optical signal in a unit pixel and a MOS transistor for controlling the optical signal. The manufacturing process is very simple compared to a CCD, and a well - It has an advantage that it can be manufactured as one chip together with the signal processing element. As CMOS technology is developed in the direction of reduction of photolithography, the size of pixels and circuits of CMOS image sensors is also decreasing. As the size of a pixel decreases, a pixel array having a large number of pixels can be formed at a low cost. On the other hand, there is a problem in that the photosensitivity drops due to a small amount of incident light. In particular, in a front illuminated CMOS image sensor using an active pixel sensor (APS), a metal line associated with the active circuit reduces the fill factor of the pixel array. This is because, even if the line width of the metal line is reduced, the amount of light reaching the diffusion region is reduced due to the presence of the metal line, the photodiode diffusion region which is the light sensing unit is blocked, or the light reaches the photodiode diffusion region.

A back illuminated CMOS sensor is an image sensor in which a circuit is present on the front side of the substrate and a lens is present on the rear side of the substrate. Since the light does not pass through the circuit area but directly enters the impurity region of the photodiode through the lens, it is possible to solve the problem of reduction of the filling rate of the front - illuminated CMOS image sensor. 1 is a schematic cross - sectional view of a conventional back - illuminated CMOS sensor. The pixel circuit portion 1 of the CMOS sensor is formed in a laminated manner on one surface 7 of the

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substrate 2. | An impurity region 9 of a photodiode extending to the other surface 8 of the substrate 2 is formed on the pixel circuit portion 1 and a color filter 3 and a microlens 4 are formed thereon. The substrate 2 of the CMOS image sensor is very thin and is supported by the support substrate 6 contacting the pixel circuit portion 1. | A manufacturing method of such a conventional back - illuminated CMOS sensor is as follows. First, the impurity region 2 of the photodiode is formed at a depth of a certain depth from the front surface of the substrate by ion implantation, and the circuit pattern layers constituting the pixel circuit portion 1 are formed. A supporting substrate 6 is attached to the front surface of the substrate in contact with the pixel circuit portion 1 and the rear surface of the substrate is polished to expose the impurity region 2 of the photodiode from the rear surface of the substrate. A lens portion 5 including a color filter 3 and a microlens 4 is formed on the exposed photodiode 2. The region immediately below the color filter 3 in the region of the photodiode 2 corresponds to the farthest from the front surface of the substrate and the probability that the concentration of the ion implanted impurity is not uniform becomes high. In the back - illuminated CMOS sensor, the element isolation between the photodiodes 2 is performed by the doping profile. In the region under the color filter 3, the doping profile is not clear due to the irregularity of the impurity concentration, The electrical crosstalk may not be completely removed. 2, in the case of a pixel located at the edge of the chip, the microlens 3 and the color filter 4 are not aligned with the corresponding photodiode 2 and a photodiode (not shown) 2 by a predetermined amount.

Therefore, in the case of the pixels at the chip edge, the possibility of optical crosstalk is increased. An object of the present invention is to provide a back - illuminated CMOS image sensor capable of blocking electrical crosstalk between pixels and optical crosstalk. According to another aspect of the present invention, there is provided a method of fabricating a backside illumination type CMOS image sensor capable of blocking electrical crosstalk between pixels and optical crosstalk.

According to an aspect of the present invention, there is provided a back - illuminated CMOS image sensor including a semiconductor substrate having a first surface and a second surface, the device having a deep trench structure extending from the first surface toward the second surface, ; A photodiode defined by the deep trench isolation film and extended from the first surface to the second surface; A pixel circuit portion formed adjacent to the first surface of the semiconductor substrate; And a lens portion formed adjacent to the second surface of the semiconductor substrate. And a support substrate on the pixel circuit portion. It is preferable that the depth of the device isolation film of the deep trench structure is 3 to 10 mu m. The deep - trench structure may be formed of an insulating film having a refractive index lower than that of the

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semiconductor substrate such that light incident obliquely through the photodiode is totally reflected at the boundary of the isolation film, and may be a silicon oxide film. And a glass substrate between the second surface of the semiconductor substrate and the lens portion. The pixel circuit portion may include a transfer transistor, a reset transistor, a drive transistor, a selection transistor, and a wiring. The lens portion may include a color filter adjacent to the second surface of the semiconductor substrate and a microlens on the color filter. According to another aspect of the present invention, there is provided a method of manufacturing a back - illuminated CMOS image sensor, including: forming a deep - trench structure isolation layer from a first surface of a semiconductor substrate; Forming a photodiode region in the semiconductor substrate defined by the device isolation film by ion implantation from the first surface; Forming a pixel circuit portion on the first surface of the semiconductor substrate over the photodiode region; Polishing the second surface of the semiconductor substrate on which the pixel circuit portion is formed; And forming a lens portion on the second surface of the polished semiconductor substrate, the lens portion being aligned with the photodiode. Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings.

However, the present invention is not limited to the embodiments described herein but may be embodied in other forms. Rather, the embodiments disclosed herein are being provided so that this disclosure will be thorough and complete, and will fully convey the concept of the invention to those skilled in the art. In the drawings, the thicknesses of layers and regions are exaggerated for clarity. Like reference numerals designate like elements throughout the specification. 3 is a simplified cross - sectional view of a back - illuminated CMOS image sensor according to an embodiment of the present invention. 3 shows a pixel array portion including the photodiode 11, the pixel circuit portion 20, and the lens portion 30. In Fig. 3, the semiconductor substrate 10 on which the photodiode 11 is formed has a front side 13 directed downward and a back side 15 directed upward. In the back - illuminated CMOS image sensor, since the light is incident from the back surface 15 of the semiconductor substrate 10, the thickness of the substrate must be small enough to allow the incident light to reach the photodiode 11. The photodiode 11 in the semiconductor substrate 10 can be formed by the p - type impurity region in the n - type impurity or the n - type impurity region in the p - type impurity region. A pixel circuit portion 20 including transistors and wirings constituting a unit pixel together with a photodiode 11 is formed on the front surface 13 of the semiconductor substrate 10 under the photodiode 11. A passivation layer (not shown) and an adhesive layer (not shown) may be further formed between the pixel circuit portion 20 and the support substrate 40. The passivation layer A lens unit 30 including a color filter 31 and a microlens 33 is formed on the back surface of the semiconductor substrate 10 on the photodiode 11. A transparent substrate (not shown) such as glass may be further

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formed between the photodiode 11 and the lens unit 30. [In the present invention, adjacent photodiodes (11) are separated from each other by a deep trench isolation film (13).

The deep trench isolation film 13 may be formed by a depth of the photodiode 11 or may be formed to be slightly shallow. The deep trench isolation film 13 is formed just below the lens portion 30 so that the electrons or holes generated by the light in the photodiode 11 can not move vertically and move to the adjacent pixel region Electrical crosstalk can be prevented. Since the impurity region of the photodiode 11 is formed by deep ion implantation from the front surface of the semiconductor substrate 10 in the backside illumination type CMOS image sensor, the impurity region which is in contact with the back surface of the semiconductor substrate 10 under the lens portion 30 The doping profile is disturbed and electrical crosstalk can occur. The electrical crosstalk can be prevented by the deep trench isolation film 13 which is an insulating film. The incident light having a slope through the lens unit 30 is totally reflected at the boundary between the photodiode 11 and the isolation film 13 and can not pass through the photodiode 11 of the adjacent pixel. Therefore, optical crosstalk Can be prevented. In order to increase the light receiving efficiency of obliquely incident light, the pixels of the edge portion of the chip of the conventional CMOS image sensor are formed such that the lens portion 30 and the corresponding photodiode 11 in one pixel are overlapped obliquely There is a high possibility that optical crosstalk between adjacent pixels occurs. However, in the present invention, as shown in FIG. 4, the deep trench isolation film 13 between the photodiodes 11 is made of a material having a refractive index lower than that of the silicon of the photodiode 11 and is made obliquely incident on the deep trench isolation film 13 Optical crosstalk can be prevented by totally reflecting light. FIG. 5 is a schematic flowchart for explaining a method of manufacturing a back - illuminated CMOS image sensor according to the present invention in order. Referring to FIG. 5, a deep trench isolation layer is formed on a semiconductor substrate (S10). The deep trench isolation film is formed by etching a semiconductor substrate using a hard mask pattern such as a silicon nitride film as a mask to form a deep trench and then filling an insulating film such as a silicon oxide film.

The insulating film is formed by forming an insulating film to fill the deep trench, planarizing the insulating film, and removing the hard mask pattern. Next, a photodiode region is formed by ion implantation of impurities into the semiconductor substrate having the deep trench isolation film formed thereon (S20). The photodiode region can be formed by forming a p - type impurity region in the n - type impurity or an n - type impurity region in the p - type impurity region. After the photodiode region is formed on the semiconductor substrate, a pixel circuit portion including a transistor and a wiring

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that constitute a unit pixel such as a transfer transistor, a reset transistor, a driving transistor, and a selection transistor is formed on the substrate (S30). A supporting substrate is attached to the front surface of the semiconductor substrate on which the pixel circuit portion is formed (S40). A passivation layer for protecting the pixel circuit portion before attachment of the supporting substrate can be formed. After the supporting substrate is attached, the back surface of the semiconductor substrate is polished and chemically mechanically polished so that light can be incident from the back surface of the semiconductor substrate to the photodiode region, thereby reducing the thickness of the semiconductor substrate (S50). A lens portion including a color filter and a microlens is formed on the photodiode on the back surface of the semiconductor substrate (S60). At this time, a glass substrate may be further formed between the back surface of the semiconductor substrate and the lens portion. While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it is to be understood that the invention is not limited to the disclosed exemplary embodiments, It will be apparent to those skilled in the art that the present invention can be carried out without departing from the spirit and scope of the invention.

According to the present invention, the inter - pixel electrical crosstalk and the optical crosstalk can be blocked by isolating the photodiode of the pixel array into the deep - trench structure element isolation film in the back - illuminated CMOS image sensor.

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CLAIMS KR20080014301

1.
An element isolation layer of a deep trench structure formed in a semiconductor substrate having a first surface and a second surface and extended from the first surface to the second surface; A photodiode defined by the deep trench isolation film and extended from the first surface to the second surface; A pixel circuit portion formed adjacent to the first surface of the semiconductor substrate; And a lens portion formed adjacent to the second surface of the semiconductor substrate.

2.
The backside illumination type CMOS image sensor according to claim 1, further comprising a supporting substrate on the pixel circuit portion.

3.
The backside illumination type CMOS image sensor according to claim 1, wherein the depth of the device isolation film of the deep trench structure is 3 to 10 mu m.

4.
The backside illumination type CMOS image sensor according to claim 1, wherein the deep-trench structure element isolation film is formed of an insulating film having a refractive index lower than that of the semiconductor substrate so that light obliquely incident through the photodiode is totally reflected at a boundary of the isolation film.

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5.
The backside illumination type CMOS image sensor according to claim 4, wherein the device isolation film of the deep trench structure is a silicon oxide film.

6.
The back - illuminated CMOS image sensor according to claim 1, further comprising a glass substrate between the second surface of the semiconductor substrate and the lens portion.

7.
The backside illumination type CMOS image sensor according to claim 1, wherein the pixel circuit portion includes a transfer transistor, a reset transistor, a driving transistor, a selection transistor, and a wiring.

8.
The backside illumination type CMOS image sensor according to claim 1, wherein the lens portion includes a color filter adjacent to the second surface of the semiconductor substrate and a microlens on the color filter.

9.
Forming a device isolation film of a deep trench structure from the first surface of the semiconductor substrate; Forming a photodiode region in the semiconductor substrate defined by the device isolation film by ion implantation from the first surface; Forming a pixel circuit portion on the first surface of the semiconductor substrate over the photodiode region; Polishing the second surface of the semiconductor substrate on which the pixel circuit portion is formed; And forming a lens portion on the second surface of the polished semiconductor substrate in alignment with the photodiode.

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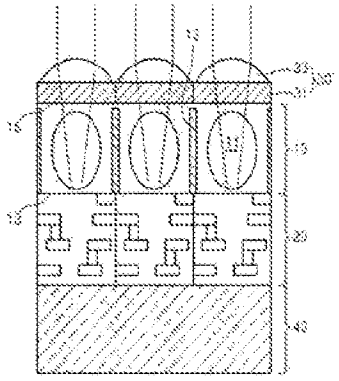
전체 청구항 수 : 총 9 항

(54) 딥트렌치 소자분리막을 포함하는 이면 조사형 CMOS이미지 센서 및 그 제조방법

(57) 요 약

딥트렌치 구조의 소자분리막을 구비한 이면 조사형 CMOS 이미지 센서 및 그 제조방법을 개시한다. 본 발명에 의한 CMOS 이미지 센서는 제1 면과 제2 면을 갖는 반도체 기판 내에서 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 딥트렌치 구조의 소자분리막; 상기 딥트렌치 소자분리막에 의하여 한정되며 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 포토다이오드; 상기 반도체 기판의 상기 제1 면에 인접하여 형성된 화소 회로부; 및 상기 반도체 기판의 상기 제2 면에 인접하여 형성된 랜즈부를 포함한다. 화소 어레이의 포토다이오드가 딥트렌치 구조의 소자분리막으로 격리됨으로써 화소간 전기적 크로스토크와 광학적 크로스토크를 방지할 수 있다.

대표도 - 도3



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특허청구의 범위

청구항 1

제1 면과 제2 면을 갖는 반도체 기판 내에서 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 딥트렌치 구조의 소자분리막;

상기 딥트렌치 소자분리막에 의하여 한정되며 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 포토다이오드;

상기 반도체 기판의 상기 제1 면에 인접하여 형성된 화소 회로부; 및

상기 반도체 기판의 상기 제2 면에 인접하여 형성된 렌즈부;를 포함하는 이면 조사형 CMOS 이미지 센서.

청구항 2

제1 항에 있어서, 상기 화소 회로부 위의 지지 기판을 더 포함하는 이면 조사형 CMOS 이미지 센서.

청구항 3

제1 항에 있어서, 상기 딥트렌치 구조의 소자분리막의 깊이는 3~10㎛인 이면 조사형 CMOS 이미지 센서.

청구항 4

제1 항에 있어서, 상기 딥트렌치 구조의 소자분리막은 상기 포토다이오드를 통과하여 경사입사된 빛이 상기 소자분리막의 경계에서 전반사되도록 상기 반도체 기판보다 굴절률이 낮은 절연막으로 형성된 이면 조사형 CMOS 이미지 센서.

청구항 5

제4 항에 있어서, 상기 딥트렌치 구조의 소자분리막은 실리콘 산화막인 이면 조사형 CMOS 이미지 센서.

청구항 6

제1 항에 있어서, 상기 반도체 기판의 상기 제2 면과 상기 렌즈부 사이에 글래스 기판을 더 포함하는 이면 조사형 CMOS 이미지 센서.

청구항 7

제1 항에 있어서, 상기 화소 회로부는 전달 트랜지스터, 리셋 트랜지스터, 구동 트랜지스터, 선택 트랜지스터 및 배선을 포함하는 이면 조사형 CMOS 이미지 센서.

청구항 8

제1 항에 있어서, 상기 렌즈부는 상기 반도체 기판의 상기 제2 면에 인접한 칼라필터와 상기 칼라필터 위의 마이크로 렌즈를 포함하는 이면 조사형 CMOS 이미지 센서.

청구항 9

반도체 기판의 제1 면으로부터 딥트렌치 구조의 소자분리막을 형성하는 단계;

상기 소자분리막에 의하여 한정되는 상기 반도체 기판 내에 상기 제1 면으로부터의 이온주입에 의하여 포토다이오드 영역을 형성하는 단계;

상기 포토다이오드 영역 위로 상기 반도체 기판의 상기 제1 면에 화소 회로부를 형성하는 단계;

상기 화소 회로부가 형성된 상기 반도체 기판의 상기 제2 면을 연마하는 단계;

연마된 상기 반도체 기판의 상기 제2 면에 상기 포토다이오드에 정렬하여 렌즈부를 형성하는 단계;를 포함하는 이면 조사형 CMOS 이미지 센서를 형성하는 방법.

명 세 서

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발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

<10> 본 발명은 CMOS 이미지소자에 관한 것으로 더욱 상세하게는 크로스토크(cross talk)을 방지할 수 있는 이면 조사형(back illuminated) CMOS 이미지 센서 및 그 제조방법에 관한 것이다.

<11> 일반적인 이미지 센서는 광학 영상(optical image)을 전기 신호로 변환시키는 반도체 소자를 의미한다. 이러한 이미지 센서는 CCD(Charge Coupled Device)와 CMOS 이미지 센서(CMOS Image Sensor; CIS)로 구분될 수 있다. 이미지 센서들은 화소(pixel)의 2차원적인 배열에 근거하고 있다. 각 화소는 광학 영상의 일부를 전기적인 신호로 변환할 수 있는 감지 요소(sensing element)를 포함한다. 전기적인 신호들은 예를 들면, 디스플레이에 광학적 영상을 다시 생성하는데 사용된다.

<12> CMOS 이미지 센서는 단위 화소 내에 광신호를 수신하는 포토다이오드와 상기 광신호를 제어할 수 있는 모스트랜지스터를 구비하는 소자로, CCD에 비해 제조공정이 매우 단순하며 잘 확립된 CMOS 기술을 이용하여 다른 여러 신호처리 소자와 더불어 하나의 칩으로 제조할 수 있는 장점이 있다.

<13> CMOS 기술이 포토리소그래피의 축소의 방향으로 전개됨에 따라 CMOS 이미지 센서의 화소 및 회로의 크기도 감소하고 있다. 화소의 크기가 감소함에 따라 적은 비용으로 많은 수의 화소로 이루어진 화소 어레이를 만들 수 있는 장점이 있으나, 한편으로 적은 양의 광입사로 인하여 광감도가 떨어지는 문제점이 있다. 특히, 능동 화소(active pixel sensor; APS)를 사용하는 전면 조사형(front illuminated) CMOS 이미지 센서에서는 능동회로와 관련된 금속 라인이 화소 어레이의 채움율(fill factor)을 감소시킨다. 이것은 금속 라인의 선폭이 축소되어도 금속 라인의 존재로 인하여 광감지부인 포토다이오드 확산영역이 가려지거나 빛이 포토다이오드 확산영역에 도달하는 거리가 멀어짐으로써 확산영역에 도달하는 빛의 양이 감소되어 일어난다.

<14> 이면 조사형(back illuminated) CMOS 센서는 회로가 기판의 전면에 존재하고 렌즈가 기판의 이면에 존재하는 이미지 센서이다. 빛이 회로영역을 통과하지 않고 렌즈를 통하여 바로 포토다이오드의 불순물 영역으로 들어오므로 전면 조사형 CMOS 이미지 센서의 채움율 감소의 문제를 해결할 수 있다.

<15> 도 1은 종래의 이면 조사형 CMOS 센서의 개략적인 단면도이다. 기판(2)의 일면(7)에 접하여 CMOS 센서의 화소 회로부(1)가 적층 형성되어 있다. 화소 회로부(1) 위로 기판(2)의 다른 일면(8)까지 확장되는 포토다이오드의 불순물 영역(9)이 형성되어 있으며 그 위로 칼라필터(3)와 마이크로 렌즈(4)가 형성되어 있다. CMOS 이미지 센서의 기판(2)은 그 두께가 매우 얇아 화소 회로부(1)에 접한 지지기판(6)에 의하여 지지된다.

<16> 이러한 종래의 이면 조사형 CMOS 센서의 제조 방법은 다음과 같다. 먼저, 이온주입에 의하여 기판의 전면으로부터 일정 깊이의 깊이에 포토다이오드의 불순물 영역(2)을 형성한 후 화소 회로부(1)를 구성하는 회로 패턴층들을 형성한다. 그리고 화소 회로부(1)에 접하여 기판의 전면에 지지기판(6)을 부착하고 기판의 후면을 연마하여 포토다이오드의 불순물 영역(2)을 기판의 일면으로부터 노출시킨다. 노출된 포토다이오드(2) 위로 칼라필터(3)와 마이크로 렌즈(4)를 포함하는 렌즈부(5)를 형성한다.

<17> 포토다이오드(2) 영역 중 칼라필터(3) 바로 아래 영역은 기판의 전면으로부터 가장 멀리 떨어진 곳에 해당되어 이온주입된 불순물의 농도가 균일하지 않을 확률이 높아진다. 이면 조사형 CMOS 센서에서는 포토다이오드(2) 간의 소자분리가 도핑 프로파일에 의하여 이루어지는데, 칼라필터(3) 아래 영역은 빛의 수광량이 많은 부분이면서도 불순물 농도의 불균일로 인하여 도핑 프로파일이 명확하지 않아 전기적인 크로스토크(electrical crosstalk)가 완벽하게 제거되지 못할 수 있다.

<18> 또한, 도 2에 도시한 바와 같이 칩의 에지에 있는 화소의 경우에는 마이크로 렌즈(3) 및 칼라필터(4)가 해당 포토다이오드(2)에 정렬되어 있지 않고 빛의 수광량을 높이기 위하여 포토다이오드(2)에 대하여 일정하게 이동(shift)하여 형성된다. 따라서 칩 에지의 화소의 경우에는 광학적 크로스토크(optical crosstalk)가 발생할 가능성이 높아진다.

발명이 이루고자 하는 기술적 과제

<19> 본 발명이 이루고자 하는 기술적 과제는 화소간 전기적 크로스토크와 광학적 크로스토크를 차단할 수 있는 이면

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조사형 CMOS 이미지 센서를 제공하는데 있다.

<20> 본 발명이 이루고자 하는 다른 기술적 과제는 화소간 전기적 크로스토크와 광학적 크로스토크를 차단할 수 있는 이면 조사형 CMOS 이미지 센서의 제조방법을 제공하는데 있다.

발명의 구성 및 작용

<21> 상기 목적을 달성하기 위한 본 발명에 따른 이면 조사형 CMOS 이미지 센서는 제1 면과 제2 면을 갖는 반도체 기판 내에서 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 딥트렌치 구조의 소자분리막; 상기 딥트렌치 소자분리막에 의하여 한정되며 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 포토다이오드; 상기 반도체 기판의 상기 제1 면에 인접하여 형성된 화소 회로부; 및 상기 반도체 기판의 상기 제2 면에 인접하여 형성된 랜즈부;를 포함한다.

<22> 상기 화소 회로부 위의 지지 기판을 더 포함할 수 있다.

<23> 상기 딥트렌치 구조의 소자분리막의 깊이는 3~10㎛인 것이 바람직하다.

<24> 상기 딥트렌치 구조의 소자분리막은 상기 포토다이오드를 통과하여 경사입사된 빛이 상기 소자분리막의 경계에서 전반사되도록 상기 반도체 기판보다 굴절율이 낮은 절연막으로 형성하는 것이 바람직하며, 실리콘 산화막일 수 있다.

<25> 상기 반도체 기판의 상기 제2 면과 상기 랜즈부 사이에 글래스 기판을 더 포함할 수 있다.

<26> 상기 화소 회로부는 전달 트랜지스터, 리셋 트랜지스터, 구동 트랜지스터, 선택 트랜지스터 및 배선을 포함할 수 있다.

<27> 상기 랜즈부는 상기 반도체 기판의 상기 제2 면에 인접한 칼라필터과 상기 칼라필터 위의 마이크로 랜즈를 포함할 수 있다.

<28> 상기 다른 목적을 달성하기 위한 본 발명에 따른 이면 조사형 CMOS 이미지 센서의 제조방법은 반도체 기판의 제1 면으로부터 딥트렌치 구조의 소자분리막을 형성하는 단계; 상기 소자분리막에 의하여 한정되는 상기 반도체 기판 내에 상기 제1 면으로부터의 이온주입에 의하여 포토다이오드 영역을 형성하는 단계; 상기 포토다이오드 영역 위로 상기 반도체 기판의 상기 제1 면에 화소 회로부를 형성하는 단계; 상기 화소 회로부가 형성된 상기 반도체 기판의 상기 제2 면을 연마하는 단계; 및 연마된 상기 반도체 기판의 상기 제2 면에 상기 포토다이오드에 정렬하여 랜즈부를 형성하는 단계;를 포함한다.

<29> 이하, 첨부된 도면을 참조하여 본 발명의 바람직한 실시예를 상세히 설명하기로 한다. 그러나, 본 발명은 여기서 설명되는 실시예들에 한정되지 않고 다른 형태로 구체화될 수도 있다. 오히려, 여기서 소개되는 실시예들은 개시된 내용이 철저하고 완전해질 수 있도록 그리고 당업자에게 본 발명의 사상이 충분히 전달될 수 있도록 하기 위해 제공되는 것이다. 도면들에 있어서, 층 및 영역들의 두께는 명확성을 기하여 위하여 과장된 것이다. 명세서 전체에 걸쳐서 동일한 참조번호들은 동일한 구성요소들을 나타낸다.

<30> 도 3은 본 발명의 일 실시예에 따른 이면 조사형 CMOS 이미지 센서의 일부를 단순화하여 보여주는 단면도이다. 도 3에는 포토다이오드(11), 화소 회로부(20) 및 랜즈부(30)를 포함하는 화소 어레이 부분이 도시되어 있다. 도 3에서 포토다이오드(11)가 형성되어 있는 반도체 기판(10)은 전면(front side, 13)이 아래를 향하고 있으며 이면(back side, 15)이 위를 향하고 있다. 이면 조사형 CMOS 이미지 센서에서는 빛이 반도체 기판(10)의 이면(15)으로부터 입사되므로 입사된 빛이 포토다이오드(11)에 도달할 수 있을 정도로 기판의 두께가 얇아야 한다.

<31> 반도체 기판(10) 내의 포토다이오드(11)는 n형 불순물 내의 p형 불순물 영역, 또는 p형 불순물 영역 내의 n형 불순물 영역에 의하여 형성될 수 있다. 포토다이오드(11) 아래의 반도체 기판(10)의 전면(13)에는 포토다이오드(11)와 함께 단위 화소를 구성하는 트랜지스터들과 배선들을 포함하는 화소 회로부(20)가 적층되어 형성되어 있다. 화소 회로부(20) 아래로 지지 기판(40)이 부착되어 있으며, 화소 회로부(20)와 지지 기판(40) 사이에는 패시베이션층(미도시)과 접착층(미도시)가 더 형성될 수 있다. 포토다이오드(11) 위의 반도체 기판(10)의 이면에는 칼라 필터(31) 및 마이크로 랜즈(33)를 포함하는 랜즈부(30)가 형성되어 있다. 포토다이오드(11)와 랜즈부(30) 사이에는 글래스와 같은 투명기판(미도시)이 더 형성될 수 있다.

<32> 본 발명에서는 인접하는 포토다이오드(11)가 딥트렌치 소자분리막(13)에 의하여 서로 분리된다. 딥트렌치 소자분리막(13)은 포토다이오드(11)의 깊이만큼 형성되거나 그보다 약간 얇게 형성될 수 있다. 딥트렌치 소자분리막(13)은 랜즈부(20)의 바로 아래까지 형성되어 있어서, 포토다이오드(11) 내에서 빛에 의해 생성된 전자 또는 전

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공이 수직으로 이동하기 못하고 인접 화소 영역으로 이동하여 발생하는 전기적 크로스토크(electrical crosstalk)를 방지할 수 있다. 이면 조사형 CMOS 이미지 센서에서는 포토다이오드(11)의 불순물 영역이 반도체 기판(10)의 전면으로부터 깊은 이온주입에 의하여 생성되므로 렌즈부(30) 아래의 반도체 기판(10)의 이면에 접하는 불순물 영역은 도핑 프로파일이 흐트러져서 전기적 크로스토크가 발생할 수 있는데, 절연막인 딥트렌치 소자분리막(13)에 의하여 전기적 크로스토크가 방지될 수 있는 것이다.

<33> 또한 렌즈부(30)를 통해 집사된 빛은 포토다이오드(11)와 소자분리막(13)의 경계에서 전반사되어 인접 화소의 포토다이오드(11)로 통과하지 못하므로 광학적 크로스토크(optical crosstalk)를 방지할 수 있다. 종래의 CMOS 이미지 센서의 칩의 에지부의 화소는 비스듬히 들어오는 빛의 수광효율을 높이기 위하여 하나의 화소에서 렌즈부(30)와 이에 대응하는 포토다이오드(11)가 서로 수직으로 접치지 않고 비스듬히 접치도록 형성되어 인접 화소간 광학적 크로스토크가 발생할 가능성이 컸다. 그러나 본 발명에서는 도 4에 나타낸 바와 같이 포토다이오드(11) 사이의 딥트렌치 소자분리막(13)이 포토다이오드(11)의 실리콘보다 굴절율이 낮은 물질을 사용하여 딥트렌치 소자분리막(13)으로 비스듬히 들어오는 빛을 전반사함으로써 광학적 크로스토크를 방지할 수 있다.

<34> 도 5는 본 발명에 따른 이면 조사형 CMOS 이미지 센서의 제조방법을 순서대로 설명하기 위한 개략적인 순서도이다.

<35> 도 5를 참조하면, 먼저 반도체 기판에 딥트렌치 소자분리막을 형성한다(S10). 딥트렌치 소자분리막은 실리콘 질화막과 같은 하드마스크 패턴을 마스크로 하여 반도체 기판을 식각하여 딥트렌치를 형성한 후, 실리콘 산화막과 같은 절연막을 충전하여 형성한다. 절연막 매립은 딥트렌치를 매립하도록 절연막의 형성하고 평탄화한 후 하드마스크 패턴을 제거하여 이루어진다.

<36> 이어서 딥트렌치 소자분리막이 형성된 반도체 기판 내에 불순물의 이온주입에 의하여 포토다이오드 영역을 형성한다(S20). 포토다이오드 영역은 n형 불순물 내에 p형 불순물 영역을 형성하거나 p형 불순물 영역 내의 n형 불순물 영역을 형성함으로써 만들 수 있다.

<37> 반도체 기판에 포토다이오드 영역을 만든 후에 기판 위로 전달 트랜지스터, 리셋 트랜지스터, 구동 트랜지스터, 선택 트랜지스터와 같은 단위 화소를 구성하는 트랜지스터와 배선을 포함하는 화소 회로부를 형성한다(S30).

<38> 화소 회로부가 형성된 반도체 기판의 전면에 지지 기판을 부착한다(S40). 지지기판의 부착 전 화소 회로부를 보호하기 위한 패시베이션층을 형성할 수 있다.

<39> 지지기판을 부착한 후 반도체 기판의 이면으로부터 포토다이오드 영역으로 빛이 입사될 수 있을 정도로 반도체 기판의 이면을 갈고 화학적 기계적 연마를 수행하여 반도체 기판의 두께를 얇게 만든다(S50).

<40> 반도체 기판의 이면의 포토다이오드 위로 칼라필터 및 마이크로 렌즈를 포함하는 렌즈부를 형성한다(S60). 이때 반도체 기판의 이면과 렌즈부 사이에 글래스 기판을 더 형성하여 있을 수도 있다.

<41> 이상에서 본 발명의 실시예에 대하여 상세히 설명하였지만, 설명한 본 발명은 전술한 실시예 및 첨부된 도면에 의해 한정되는 것이 아니고, 본 발명의 기술적 사상을 벗어나지 않는 범위 내에서 여러 가지 치환, 변형 및 변경이 가능하다는 것이 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자에게 있어 명백할 것이다.

발명의 효과

<42> 본 발명에 의하면 이면 조사형 CMOS 이미지 센서에서 화소 어레이의 포토다이오드를 딥트렌치 구조의 소자분리막으로 격리함으로써 화소간 전기적 크로스토크와 광학적 크로스토크를 차단할 수 있다.

도면의 간단한 설명

<1> 도 1은 종래의 이면 조사형 CMOS 센서의 화소 어레이 영역의 개략적인 단면도이다.

<2> 도 2은 종래의 이면 조사형 CMOS 센서의 칩 에지 부분의 화소 어레이 영역의 개략적인 단면도이다.

<3> 도 3은 본 발명의 일 실시예에 따른 이면 조사형 CMOS 이미지 센서의 화소 어레이 영역의 개략적인 단면도이다.

<4> 도 4는 본 발명에 따른 이면 조사형 CMOS 이미지 센서의 제조방법을 순서대로 설명하기 위한 개략적인 순서도이다.

<5> * 도면의 주요 부분에 대한 부호의 설명

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<6> 10: 반도체 기판 11: 포토다이오드

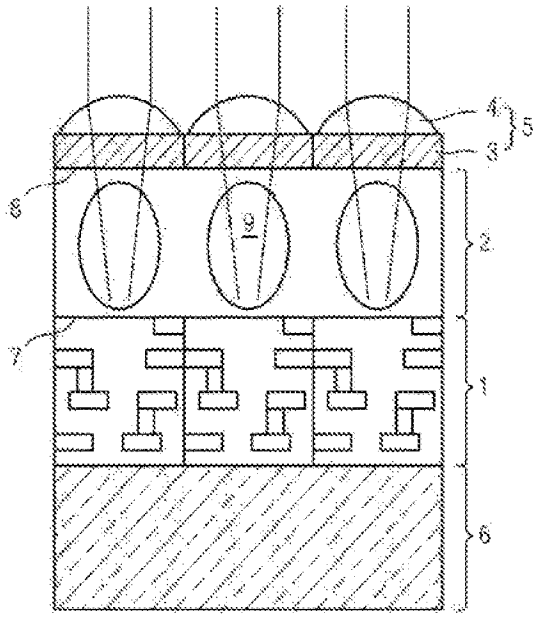
<7> 13: 빌트업층 소자분리막 20: 화소 회로부

<8> 30: 렌즈부 31: 렌티큘러

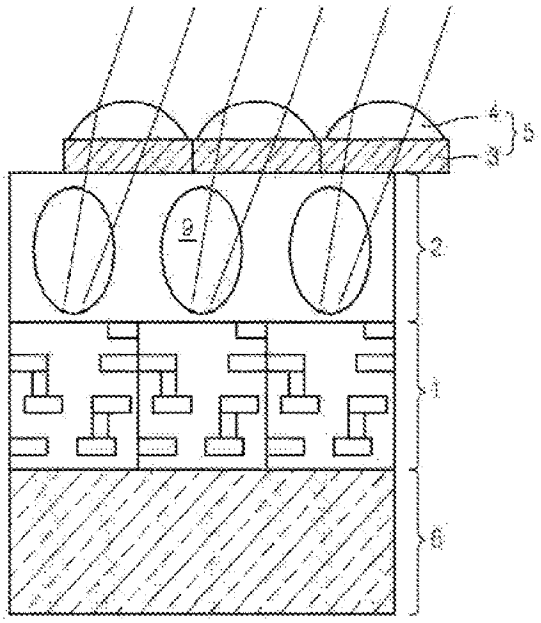
<9> 33: 마이크로 렌즈 40: 지지기판

도면

도면1

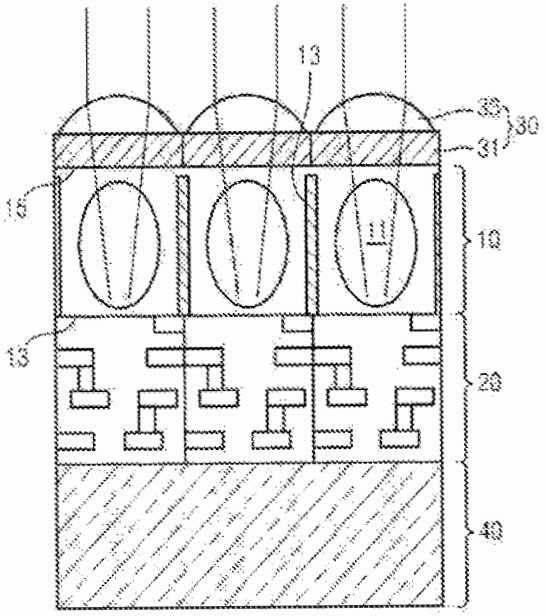


도면2

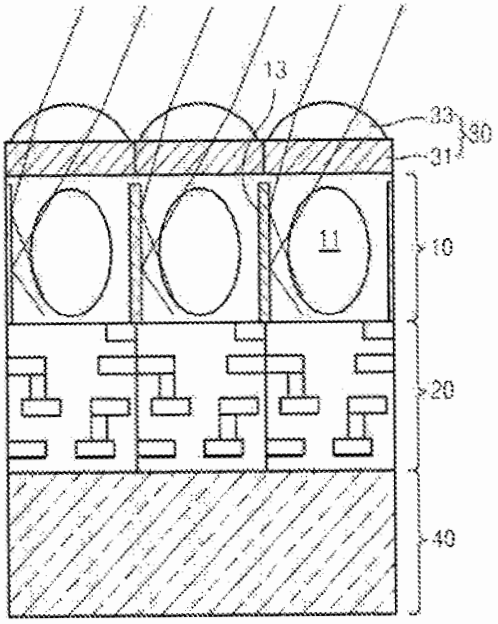


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도면3

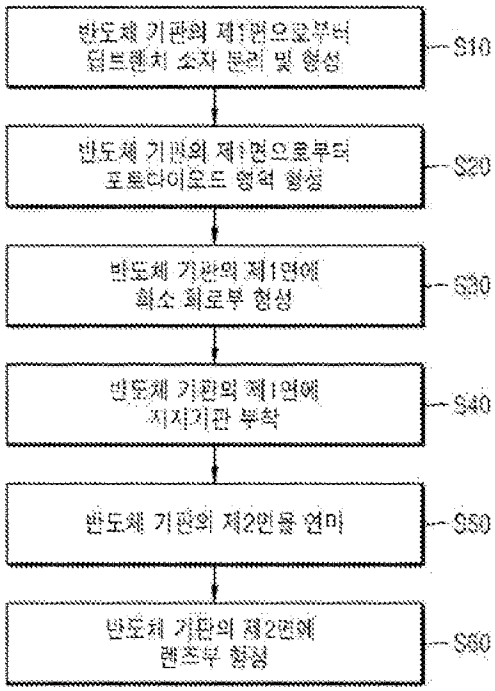


도면4



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도면5



SAMSUNG EX. 1002 - 1307/1684

Espacenet

Bibliographic data: KR20080097709 (A) — 2008-11-06

IMAGE SENSOR AND METHOD FOR FABRICATING OF THE SAME

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Abstract of KR20080097709 (A)

An image sensor and a method for fabricating the same are provided to improve the sensitivity of the image sensor by increasing the refractive index of the incident light. The image sensor includes the color filter array(30) formed on the array of pixel substrate(10); The first micro lens formed on the color filter array(50,51,52); the supplementary light-collecting portion(61) formed on the array of pixel of the substrate including first micro lens. The supplementary light-collecting portion is positioned in the gap region between the first micro lens. The trench having the form in which the floor side is pressed in the supplementary light-collecting portion is formed.

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DESCRIPTION KR20080097709

BACKGROUND OF THE INVENTION 1. Field of the Invention [0001] The present invention relates to an image sensor,

1 is a view showing a conventional image sensor.

2 to 6 are views showing a manufacturing process of the image sensor according to the first embodiment.

7 to 11 are views showing a manufacturing process of the image sensor according to the second embodiment.

In the present embodiment, an image sensor and a manufacturing method thereof are disclosed. An image sensor is a semiconductor device that converts an optical image into an electrical signal and is mainly composed of a charge coupled device (CCD) and a complementary metal oxide silicon (CMOS) image sensor Sensor (CIS). On the other hand, the CCD has a disadvantage in that the driving method is complicated, power consumption is high, and a multistage photo process is required, which complicates the manufacturing process. Recently, as a next generation image sensor for overcoming the disadvantages of the charge - Moss image sensors are attracting attention. The CMOS image sensor forms a photodiode and a MOS transistor in a unit pixel to sequentially detect an electrical signal of each unit pixel in a switching manner to realize an image. In manufacturing such various image sensors, focusing techniques for increasing the photo

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sensitivity of the image sensor have been developed, and a typical example of the focusing technique is forming a microlens. In the image sensor shown in FIG. 1, a micro lens is formed by patterning an organic photoresist for a microlens on a pixel array substrate 1 on which a unit pixel 2 including a photodiode (not shown) is formed and then performing a reflow process The convex microlenses 3 are formed to refract the path of the incident light to condense a larger amount of light into the photodiode region. The microlenses 3 are formed by a single patterning process and a gap D of about 0.1 to 0.2 μ m is generated between the microlenses 3 when the reflow process is performed. Particularly, the light entering between the gaps D of the microlenses 3 goes straight as they are, and is not condensed by the photodiodes, which causes a decrease in the photosensitivity of the image sensor. Also, there is a problem that light not condensed passes through the gap D of the microlenses 3 and is detected by unit pixels disposed on the pixel array substrate 1, thereby generating noise and crosstalk.

The present embodiment provides an image sensor capable of increasing light efficiency by primarily refracting light at an upper portion of a microlens and condensing light with a microlens, and a method of manufacturing the same. Embodiments of the present invention provide an image sensor capable of improving light sensitivity by reflecting light incident between gaps of microlenses, and a method of manufacturing the same.

The image sensor of the first embodiment comprises: a color filter array formed on a pixel array substrate; A first micro - lens formed on the color filter array; And an auxiliary light collecting portion formed on the color filter array including the first microlenses. The method of manufacturing an image sensor of the first embodiment further includes: forming a color filter array on a pixel array substrate; Forming a first microlens on the color filter array; And forming an auxiliary light collecting portion on the color filter array including the first microlenses. The image sensor of the second embodiment includes: a color filter array formed on a pixel array substrate; A planarization layer formed on the color filter array; And a microlens formed on the planarization layer, wherein a reflection film is formed on the planarization layer so as to be located in a gap region of the microlens. Forming a filter array; Forming a planarization layer including a reflective film on the color filter array; and forming a microlens on the planarization layer. Hereinafter, a method of manufacturing an image sensor according to an embodiment of the present invention will be described in detail with reference to the accompanying drawings. In the description of the embodiments, when it is described as being formed on & quot; on / over & quot; of each layer, the on / over may be directly and / indirectly formed. The thickness and size of each layer in the drawings are exaggerated, omitted, or schematically shown for convenience and clarity of explanation. Also, the size of each component does not entirely reflect the actual size.

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& Lt; First Embodiment & gt; Fig. 6 shows an image sensor according to the first embodiment. Referring to Fig. 6, the image sensor of the first embodiment includes a color filter array 30 formed on a pixel array substrate 10; First microlenses (50, 51, 52) formed on the color filter array (30); And an auxiliary condensing unit 61 formed on the pixel array substrate 10 including the first microlenses 50, 51, and 52.

The auxiliary condensing unit 61 includes a trench 62 having a concave bottom surface to be positioned between the first microlenses 50, that is, a gap region. And a second microlens 81 formed on the trench 62 of the auxiliary light collecting part 61. In particular, the second microlens 81 and the first microlenses 50, 51 and 52 may be formed of the same material. In addition, the auxiliary light - collecting portion 61 may be formed of an oxide film (SiO2). In addition, the upper surface of the first microlens 50 may be formed in a convex shape, and the lower surface of the second microlens 81 may be formed in a concave shape. As described above, since the auxiliary condensing portion formed of the oxide film is formed on the first microlens, the light incident from the object is refracted through the auxiliary condensing portion first and then incident on the first microlens. Therefore, The sensor performance of the image sensor can be improved. In addition, the bottom surface of the trench formed in the auxiliary light collecting portion is formed in a concave shape, and when the light incident from the object goes straight to the gap region of the first microlens, it passes through the trench region. Then, due to the concave shape of the bottom surface of the trench, the refractive index of the light is increased, thereby preventing the light from passing through the gap region of the first microlens, thereby improving the quality of the image sensor. In addition, by forming the second microlens in the trench of the auxiliary light collecting portion, when the light incident from the object goes straight to the gap region of the first microlens, the light passes through the second microlens. Then, the concave shape of the second microlens bottom surface causes the light to be bent outward and incident on the neighboring first microlens, so that the light collecting ratio of the image sensor is increased and the photosensitivity can be improved. Hereinafter, the manufacturing process of the image sensor according to the first embodiment will be described with reference to FIGS. 2 to 6. FIG. 2, a color filter array 30 is formed on a pixel array substrate 10 in a region corresponding to a unit pixel. The pixel array substrate 10 includes a unit pixel (not shown) formed of a photodiode (not shown) for sensing light incident through the color filter array 30 and transistors (not shown) for processing charges generated in the photodiode 11).

The pixel array substrate 10 may include a metal wiring layer 20 formed of a metal wiring (not shown) for transmitting a signal to the unit pixel 11 and an insulating film (not shown), and a passivation film (not shown) . Then, the color filter array 30 is

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formed on the pixel array substrate 10. The color filter array 30 forms a color filter layer (not shown) including a photosensitive material and a pigment or a photosensitive material and a dye on the pixel array substrate 10 through a spin coating process or the like. Then, the color filter layer is exposed by a pattern mask and developed to form a color filter array 30 on the pixel array substrate 10. The color filter array 30 has one color filter for each unit pixel to separate colors from incident light. For example, the first color filter of the color filter array 30 is red, the second color filter is green, and the third color filter is composed of three colors of blue , Adjacent color filters slightly overlap each other to form a step. A planarization layer 40 may be formed on the color filter array to compensate for the level difference of the color filter array 30. The first microlenses 50, 51, and 52 are formed on the color filter array 30 to condense light into the photodiode. The first micro lenses 50, 51, and 52 coat the photoresist for forming microlenses onto the color filter array 30 through a spin process or the like. After the photoresist film (not shown) is selectively exposed and developed, a photoresist pattern (not shown) is formed on each of the color filters. Thereafter, a reflow process is performed to form first dome - shaped first microlenses 50, 51, and 52 having a convex shape. At this time, a gap D1 may be generated between the adjacent first microlenses 51 and 52 in the first microlens 50. Referring to FIG. 3, in order to prevent light from being incident on the gap D1 between the first microlenses 50, 51, and 52, the first microlenses 50, 51, The auxiliary light collecting portion 61 is formed on the substrate 10.

The auxiliary light - collecting unit 61 is formed by depositing an oxide film (SiO 2) 60 on the pixel array substrate 10 including the first microlenses 50, 51, and 52. Since the refractive index of the first microlenses 50, 51 and 52 is about 1.7 and the refractive index of the oxide film 60 is about 1.4, the light incident through the air having the refractive index of about 1 passes through the oxide film 60 And the incident light is incident on the first microlenses 50, 51, and 52, so that the light collecting rate to the photodiode can be improved. Referring to FIG. 4, a photoresist film is coated on the oxide film 60 and patterned to form a mask pattern 71. The mask pattern 71 is formed on the oxide film 60 such that the upper surface of the auxiliary light collecting portion 61 at a portion corresponding to the gap D1 of the first microlenses 50, 51, . 5, when the auxiliary light - collecting portion 61 is etched using the mask pattern 71 as an etching mask, a trench having a width corresponding to the gap region of the first microlenses 50, 51, 62 are formed. For example, the trench 62 may be etched by a dry etching method, and the bottom surface of the trench 62 may be formed to have a concave shape by controlling the injection gas. When the bottom surface of the trench 62 of the auxiliary light collecting part 61 is formed in a concave shape and light is incident on the trench 62 of the auxiliary light collecting part 61 as described above, when the concave shape of the bottom surface of the trench 62 The incident light can be converged by the

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first microlenses 50, 51 and 52 without being incident on the region of the gap D1. 6, the mask pattern 71 is removed and a photoresist for microlens formation similar to that of the first microlens 50 is applied on the auxiliary light collecting portion 61 on which the trench 62 is formed, The surface of the light condensing portion 61 is exposed and planarized. A second microlens 81 is formed in the trench 62 of the auxiliary light collecting part 61. The bottom surface of the second microlens 81 is formed to have a concave shape with respect to the first microlens 50 according to the shape of the bottom surface of the trench 62.

Therefore, as shown in FIG. 6, since the second microlens 81 having a concave shape is formed on the upper side of the auxiliary light collecting part 61 at a position corresponding to the gap area, 1 light, the light is firstly refracted by the second microlens 81 to the outer region with respect to the straight - ahead direction, and the sub - The light is refracted by the light portion 61 and then incident on the adjacent first microlenses 51 and 52 of the first microlens 50 to increase the light efficiency of the photodiode. In addition, incident light is prevented from being incident on the gap region, so that crosstalk and noise can be prevented, and the photosensitivity can be improved. Further, an auxiliary light collecting part formed of an oxide film on the first microlens can prevent image defects that may occur from impact or particles in a subsequent package or bump process. & Lt; Second Embodiment & gt; Fig. 11 shows an image sensor according to the second embodiment. The image sensor of the second embodiment includes a color filter array 130 formed on a pixel array substrate 100; A planarization layer 141 formed on the color filter array 130; And a reflective layer 181 is formed on the planarization layer 140 so as to be positioned in a gap D2 between the microlenses 150, 151 and 152. The reflective layer 181 is formed on the planarization layer 140, In addition, the planarization layer 140 may be an oxide film (SiO 2), and the reflective layer 181 may be formed of a metal material. As described above, the reflection film is formed on the surface of the planarization layer exposed by the gap region of the microlens, and when the light entering from the object goes straight to the gap region of the microlens, it is reflected back to the outside by the reflection film. Therefore, it is possible to prevent the occurrence of crosstalk and noise by preventing light from entering the gap region of the microlens in advance, thereby improving the quality of the image sensor. Hereinafter, a manufacturing process of the image sensor according to the second embodiment will be described with reference to FIGS. 7 to 11. FIG.

Referring to FIG. 7, a color filter array 130 is formed on a pixel array substrate 100 in a region corresponding to the unit pixel 110. FIG. The pixel array substrate 100 includes a unit pixel (not shown) formed of a photodiode (not shown) for sensing light incident

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through the color filter array 130 and transistors (not shown) for processing charges generated in the photodiode 110). The pixel array substrate 100 may include a metal wiring layer 120 formed of a metal wiring (not shown) and a passivation film (not shown). The metal wiring layer 120 may transmit a signal to the unit pixel 110 . The color filter array 130 is formed on the pixel array substrate 100. The color filter array 130 forms a color filter layer (not shown) including a photosensitive material and a pigment or a photosensitive material and a dye on the pixel array substrate 100 through a spin coating process or the like. Then, the color filter layer is exposed by a pattern mask and developed to form a color filter on the pixel array substrate 100. The color filter array 130 has one color filter for each unit pixel 110 to separate colors from incident light. For example, the first color filter of the color filter array 130 is red, the second color filter is green, and the third color filter is composed of three colors of blue , Adjacent color filters slightly overlap each other to form a step. A planarization layer 140 is formed on the color filter array in order to compensate the step of the color filter array 30. For example, the planarization layer 140 may have an oxide film (SiO2) having a thickness of 6000 to 90000 angstroms. Referring to FIG. 8, a photoresist film is coated on the planarization layer 140 and patterned to form a mask pattern 170. The mask pattern 170 is formed to expose the upper surface of the planarization layer 61 corresponding to the gap D2 of the microlenses 150, 151 and 152 to be formed.

When the planarization layer 140 is etched using the mask pattern 170 as an etching mask, a trench 142 is formed. For example, the width of the trench 142 may be about 0.1 to 0.3 탆, and in order to protect the color filter array 130 formed under the planarization layer 141 when the trench 142 is formed, So that the planarization layer 141 is not completely etched. 9 and 10, a metal material is deposited on the planarization layer 141 on which the trench 142 is formed, and then a planarization process is performed to form a reflection film 181 in the trench 142. For example, the reflective layer 181 may be formed by depositing TiN, Al, W or the like by CVD or PVD to form a reflective layer 180, and then planarizing the surface of the planarized layer 140 by a CMP process A reflection film 181 may be formed in the trench 142. Referring to FIG. 11, microlenses 150, 151, and 152 are formed on the planarization layer 140 to condense light into a photodiode. The microlenses 150, 151, and 152 coat the photoresist for microlens formation on the planarization layer 140 through a spin process or the like. After the photoresist film (not shown) is selectively exposed and developed, a photoresist pattern (not shown) is formed on each of the color filters. Thereafter, a reflow process is performed to form dome - shaped microlenses 150, 151 and 152 having a convex shape. At this time, a gap D2 may be generated between the microlenses 150 and neighboring microlenses 151 and 152, and a gap D2 formed between the microlenses 150, 151, The reflective film 181 formed on the reflective film 140 is exposed. 11, a reflection film 181 is formed between the micro - lenses 150, 151

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and 152, so that light incident from an object is emitted from the micro - lens 150, The light that has not passed through the microlenses 150, 151, and 152 is reflected by the reflection layer 181, and is reflected by the reflection layer 181. Therefore, So that the photosensitivity of the photodiode can be improved.

The reflection film 181 can block the incidence of the light that is not condensed in the gap D2 of the microlens 150 so that noise and crosstalk of the photodiode disposed on the pixel array substrate 100 It is possible to improve the quality of the image sensor by preventing occurrence in advance. It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. It will be clear to those who have.

As described above, according to the image sensor and the manufacturing method thereof according to the first embodiment, the refractive index of the incident light is increased to improve the light collection efficiency of the microlens, thereby improving the sensor sensitivity of the image sensor. According to the first embodiment, the auxiliary light collecting portion formed on the upper portion of the microlens can prevent image defects that may be generated from impact or particles in a subsequent package or bump process. According to the image sensor and the method of manufacturing the same according to the second embodiment, a reflection film is formed in the gap region of the microlens to reflect light incident on the gap region, thereby preventing crosstalk between pixels and noise from occurring. The reliability can be improved.

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CLAIMS KR20080097709

1.
A color filter array formed on the pixel array substrate; A first micro-lens formed on the color filter array; And an auxiliary collecting portion formed on the pixel array substrate including the first microlens.

2.
The image sensor according to claim 1, wherein a trench having a concave bottom surface is formed in the auxiliary condensing unit so as to be located in a gap region between the first microlenses.

3.
The image sensor according to claim 1 or 2, further comprising a second microlens formed on the trench of the auxiliary light collecting portion.

4.
The image sensor according to any one of claims 1 to 3, wherein the auxiliary condenser is formed of an oxide film (SiO2).

5.
Forming a color filter array on the pixel array substrate; Forming a first microlens on

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the color filter array; And forming an auxiliary light collecting portion on the color filter array including the first microlenses.

6.
The method according to claim 5, wherein the forming of the auxiliary light collecting part comprises: forming an oxide film on the color filter array including the first microlenses, The method comprising the steps of:

7.
7. The method of claim 6, further comprising forming a second microlens by depositing the same material as the first microlens on the trench.

8.
A color filter array formed on the pixel array substrate; A planarization layer formed on the color filter array; And a microlens formed on the planarization layer, wherein the planarization layer includes a reflective film formed in a gap region of the microlens.

9.
Forming a color filter array on the pixel array substrate; Forming a planarization layer including a reflective film on the color filter array; and forming a microlens on the planarization layer.

10.
10. The image sensor of claim 9, wherein the planarization layer is an oxide film and the reflective film is formed of a metal material.

11.
10. The method of claim 9, wherein forming the planarization layer further comprises: forming an oxide film on the color filter array; Forming a mask on the oxide film; Etching the oxide film by the mask to form a trench in a region where a gap of the microlens is to be formed; And filling the trench with a metal material to form a reflective film.

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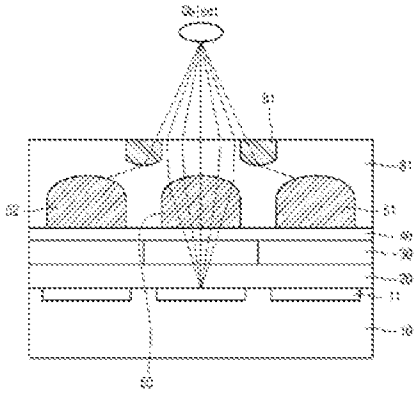
전체 청구항 수 : 총 11 항

(54) 이미지 센서 및 그의 제조방법

(57) 요 약

본 실시예의 이미지 센서는, 픽셀 어레이 기판 상에 형성된 컬러필터 어레이; 상기 컬러필터 어레이 상에 형성된 제1 마이크로렌즈; 및 상기 제1 마이크로렌즈를 포함하는 컬러필터 어레이 상에 형성된 보조 집광부를 포함한다.

대 표 도 - 도6



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특허청구의 범위

청구항 1

픽셀 어레이 기판 상에 형성된 컬러필터 어레이;

상기 컬러필터 어레이 상에 형성된 제1 마이크로렌즈; 및

상기 제1 마이크로렌즈를 포함하는 픽셀 어레이 기판 상에 형성된 보조 집광부를 포함하는 이미지 센서.

청구항 2

제1항에 있어서,

상기 제1 마이크로렌즈 사이의 갭 영역에 위치되도록 상기 보조 집광부에는 바닥면이 오목한 형태를 갖는 트렌치가 형성된 이미지 센서.

청구항 3

제1항 또는 제2항에 있어서,

상기 보조 집광부의 트렌치에 형성된 제2 마이크로렌즈를 포함하는 이미지 센서.

청구항 4

제1항 내지 제3항 중 어느 한 항에 있어서,

상기 보조 집광부는 산화막(SiO_2)으로 형성된 것을 특징으로 하는 이미지 센서.

청구항 5

픽셀 어레이 기판 상에 컬러필터 어레이를 형성하는 단계;

상기 컬러필터 어레이 상에 제1 마이크로렌즈를 형성하는 단계;

상기 제1 마이크로렌즈를 포함하는 상기 컬러필터 어레이 상부로 보조 집광부를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 6

제5항에 있어서,

상기 보조 집광부를 형성하는 단계는,

상기 제1 마이크로렌즈를 포함하는 상기 컬러필터 어레이 상부로 산화막을 형성하는 단계;

상기 제1 마이크로렌즈 사이에 바닥면이 오목한 형태의 트렌치를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 7

제6항에 있어서,

상기 트렌치에 제1 마이크로렌즈와 동일한 물질을 증착하여 제2 마이크로렌즈를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 8

픽셀 어레이 기판 상에 형성된 컬러필터 어레이;

상기 컬러필터 어레이 상에 형성된 평탄화층;

상기 평탄화층 상에 형성된 마이크로렌즈를 포함하며,

상기 평탄화층에는 상기 마이크로렌즈의 갭 영역에 위치되도록 반사막이 형성된 것을 포함하는 이미지 센서.

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청구항 9

픽셀 어레이 기판 상에 컬러필터 어레이을 형성하는 단계;

상기 컬러필터 어레이 상에 반사막을 포함하는 평탄화층을 형성하는 단계;및

상기 평탄화층 상에 마이크로렌즈를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 10

제9항에 있어서,

상기 평탄화층은 산화막이고 상기 반사막은 금속물질로 형성된 것을 포함하는 이미지 센서.

청구항 11

제9항에 있어서,

상기 평탄화층을 형성하는 단계는,

상기 컬러필터 어레이 상에 산화막을 형성하는 단계;

상기 산화막 상에 마스크를 형성하는 단계;

상기 마스크에 의해 산화막을 식각하여 마이크로렌즈의 갭이 형성될 영역에 트렌치를 형성하는 단계;

상기 트렌치에 금속물질을 매립하여 반사막을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

명 세 서

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

<4> 본 실시예에서는 이미지 센서 및 그의 제조방법을 개시한다.

<5> 이미지 센서(Image sensor)는 광학적 영상(optical image)을 전기적 신호로 변환시키는 반도체 소자로써, 크게 전하결합소자(charge coupled device; CCD)와 씨모스(CMOS; Complementary Metal Oxide Silicon) 이미지 센서(Image Sensor)(CIS)로 구분된다.

<6> 한편, CCD는 구동 방식이 복잡하고, 전력 소비가 클 뿐만 아니라, 다단계의 포토 공정이 요구되므로 제조 공정이 복잡한 단점을 갖고 있으므로, 최근에는 상기 전하 결합 소자의 단점을 극복하기 위한 차세대 이미지 센서로서 씨모스 이미지 센서가 주목을 받고 있다.

<7> 씨모스 이미지센서는 단위 화소 내에 포토 다이오드와 모스 트랜지스터를 형성시킴으로써 스위칭 방식으로 각 단위 화소의 전기적 신호를 순차적으로 검출하여 영상을 구현한다.

<8> 이러한 다양한 이미지 센서를 제조함에 있어서, 이미지 센서의 광감도(photo sensitivity)를 증가시키기 위한 집광기술들이 개발되고 있으며, 상기 집광 기술의 대표적인 예가 마이크로렌즈를 형성하는 것이다.

<9> 도 1에 도시된 이미지 센서에서 마이크로렌즈는 포토다이오드(미도시)를 포함하는 단위화소(2)가 형성된 픽셀 어레이 기판(1) 상부에 마이크로렌즈용 유기물 포토레지스트를 패터닝한 후 리플로우 공정을 진행하여 볼록형 마이크로 렌즈(3)를 형성함으로써 입사광의 경로를 굴절시켜 보다 많은 양의 빛을 포토다이오드 영역으로 집광한다.

<10> 상기와 같은 마이크로렌즈(3)는 한편의 패터닝 공정에 의해 형성되어 리플로우 공정을 거치면 각 마이크로 렌즈(3) 사이에 약 0.1 내지 0.2㎛의 갭(gap)(D)이 발생된다.

<11> 특히, 상기 마이크로렌즈(3)의 갭(D) 사이로 입사되는 빛은 그대로 직진하게 되어 포토다이오드로 집광되지 않게 되므로 이미지 센서의 광감도를 저하시키는 원인이 된다.

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<12> 또한, 상기 마이크로렌즈(3)의 갭(D) 사이로 집광되지 않은 빛이 통과하여 픽셀 어레이 기판(1)에 배치된 단위 픽셀에 감지됨으로써 노이즈 및 크로스 토크가 발생되는 문제점이 있다.

발명이 이루고자 하는 기술적 과제

<13> 본 실시예는 마이크로렌즈의 상부에서 광을 일차적으로 굴절시켜 마이크로렌즈로 광을 집광시켜 광 효율을 증대시킬 수 있는 이미지 센서 및 그의 제조방법을 제공한다.

<14> 본 발명의 실시예는 마이크로렌즈의 갭 사이로 입사되는 광을 반사시켜 광감도를 향상시킬 수 있는 이미지 센서 및 그의 제조방법을 제공한다.

발명의 구성 및 작용

<15> 제1 실시예의 이미지 센서는, 픽셀 어레이 기판 상에 형성된 컬러필터 어레이; 상기 컬러필터 어레이 상에 형성된 제1 마이크로렌즈; 및 상기 제1 마이크로렌즈를 포함하는 컬러필터 어레이 상에 형성된 보조 집광부를 포함한다.

<16> 또한 제1 실시예의 이미지 센서의 제조방법은, 픽셀 어레이 기판 상에 컬러필터 어레이를 형성하는 단계; 상기 컬러필터 어레이 상에 제1 마이크로렌즈를 형성하는 단계; 상기 제1 마이크로렌즈를 포함하는 상기 컬러필터 어레이 상부로 보조 집광부를 형성하는 단계를 포함한다.

<17> 제2 실시예의 이미지 센서는, 픽셀 어레이 기판 상에 형성된 컬러필터 어레이; 상기 컬러필터 어레이 상에 형성된 평탄화층; 상기 평탄화층 상에 형성된 마이크로렌즈를 포함하며, 상기 평탄화층에는 상기 마이크로렌즈의 갭 영역에 위치되도록 반사막이 형성된 것을 포함한다

<18> 또한, 제2 실시예의 이미지 센서의 제조방법은, 픽셀 어레이 기판 상에 컬러필터 어레이를 형성하는 단계; 상기 컬러필터 어레이 상에 반사막을 포함하는 평탄화층을 형성하는 단계;및 상기 평탄화층 상에 마이크로렌즈를 형성하는 단계를 포함한다.

<19> 이하, 본 발명의 실시예에 따른 이미지 센서의 제조방법을 첨부한 도면을 참조하여 상세히 설명한다.

<20> 실시예의 설명에 있어서, 각 층의 "상/위(on/over)"에 형성되는 것으로 기재되는 경우에 있어, 상/위(on/over)는 직접(directly)와 또는 다른 층을 개재하여(indirectly) 형성되는 것을 모두 포함한다.

<21> 도면에서 각층의 두께나 크기는 설명의 편의 및 명확성을 위하여 과장되거나 생략되거나 또는 개략적으로 도시되었다. 또한 각 구성요소의 크기는 실제크기를 전적으로 반영하는 것은 아니다.

<22> <제1 실시예>

<23> 도 6은 제1 실시예에 따른 이미지 센서를 도시하고 있다.

<24> 도 6을 참조하여, 제1 실시예의 이미지 센서는 픽셀 어레이 기판(10) 상에 형성된 컬러필터 어레이(30); 상기 컬러필터 어레이(30) 상에 형성된 제1 마이크로렌즈(50,51,52); 및 상기 제1 마이크로렌즈(50,51,52)를 포함하는 픽셀 어레이 기판(10) 상에 형성된 보조 집광부(61)를 포함한다.

<25> 또한, 상기 제1 마이크로렌즈(50) 사이 즉, 갭 영역에 위치되도록 상기 보조 집광부(61)에는 바닥면이 오목한 형태로 형성된 트렌치(62)를 포함한다.

<26> 또한, 상기 보조 집광부(61)의 트렌치(62)에 형성된 제2 마이크로렌즈(81)를 포함한다. 특히, 상기 제2 마이크로렌즈(81)와 상기 제1 마이크로렌즈(50,51,52)는 동일한 물질로 형성될 수 있다.

<27> 또한, 상기 보조 집광부(61)는 산화막(SiO_2)으로 형성될 수 있다.

<28> 또한, 상기 제1 마이크로렌즈(50)의 상면은 볼록한 형태로 형성되고, 제2 마이크로렌즈(81)의 하부면은 오목한 형태로 형성될 수 있다.

<29> 상기와 같이 제1 마이크로렌즈의 상부에 산화막으로 형성된 보조 집광부가 형성되어 물체로부터 입사되는 빛은 상기 보조 집광부를 통해 1차로 굴절된 후 제1 마이크로렌즈로 입사되기 때문에 제1 마이크로렌즈의 집광율을 향상시켜 이미지 센서의 센서티비티를 향상시킬 수 있다.

<30> 또한, 상기 보조 집광부에 형성된 트렌치의 바닥면이 오목한 형태로 형성되어 물체로부터 입사되는 빛이 상기

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제1 마이크로렌즈의 갭 영역으로 직진할 경우 트렌치 영역으로 통과하게 된다. 그러면 상기 트렌치 바닥면의 오목한 형태에 의하여 빛은 굴절률이 높아지게 되어 제1 마이크로렌즈의 갭 영역을 통과하는 것을 방지하므로써 이미지센서의 품질을 향상시킬 수 있다.

<31> 또한, 상기 보조 집광부의 트렌치에 제2 마이크로렌즈를 형성함으로써, 물체로부터 입사되는 빛이 상기 제1 마이크로렌즈의 갭 영역으로 직진할 경우 상기 제2 마이크로렌즈를 통과하게 된다. 그러면 상기 제2 마이크로렌즈 바닥면의 오목한 형태에 의하여 빛은 바깥 쪽으로 꺾이게 되어 이웃하는 제1 마이크로렌즈로 입사되므로 이미지 센서의 집광율이 높아져 광감도를 향상시킬 수 있다.

<32> 이하, 도 2 내지 도 6을 참조하여 제1 실시예에 따른 이미지 센서의 제조공정을 설명한다.

<33> 도 2를 참조하여, 픽셀 어레이 기판(10) 상으로 단위화소에 대응하는 영역에 컬러필터 어레이(30)를 형성한다.

<34> 상기 픽셀 어레이 기판(10)은 컬러필터 어레이(30)를 통해 입사된 빛을 감지하는 포토다이오드(미도시) 및 상기 포토다이오드에서 발생된 신호를 처리하는 트랜지스터들(미도시)로 구성된 단위화소(11)를 포함한다.

<35> 또한 상기 픽셀 어레이 기판(10)은 단위화소(11)로 신호를 전달하는 금속배선(미도시) 및 절연막(미도시)으로 이루어지는 금속배선층(20) 및 패시베이션막(미도시)을 포함할 수 있다.

<36> 그리고, 상기 픽셀 어레이 기판(10) 상에 상기 컬러필터 어레이(30)를 형성한다.

<37> 상기 컬러필터 어레이(30)는 감광물질 및 안료 또는 감광물질 및 염료를 포함하는 컬러필터층(미도시)을 스핀 코팅 공정등을 통해 픽셀 어레이 기판(10) 상에 형성한다. 이어서, 상기 컬러필터층을 패턴 마스크에 의하여 노광한 후 현상하여 상기 픽셀 어레이 기판(10) 상에 컬러필터 어레이(30)를 형성한다.

<38> 상기 컬러필터 어레이(30)는 각각의 단위화소 마다 하나의 컬러필터가 형성되어 입사하는 빛으로부터 색을 분리해 낸다. 예를 들어, 상기 컬러필터 어레이(30)의 제1 컬러필터는 레드(Red)이고, 제2 컬러필터는 그린(Green)이며, 제3 컬러필터는 블루(Blue)의 3가지 색으로 이루어지며, 인접한 컬러필터들은 서로 약간씩 오버랩되어 단차가 형성된다.

<39> 상기 컬러필터 어레이(30)의 단차를 보완하기 위하여, 상기 컬러필터 어레이 상부로 평탄화층(40)이 형성될 수도 있다.

<40> 그리고, 상기 컬러필터 어레이(30) 상부로 포토다이오드로의 집광을 위한 제1 마이크로렌즈(50,51,52)를 형성한다.

<41> 상기 제1 마이크로렌즈(50,51,52)는 상기 컬러필터 어레이(30) 상부로 마이크로 렌즈 형성용 포토레지스트를 스핀 공정등을 통해 도포한다. 그리고, 상기 포토레지스트막(미도시)을 선택적으로 노광 및 현상한 후 각각의 컬러필터 상부에 포토레지스트 패턴(미도시)을 형성한다. 이후, 리플로우 공정을 실시하여 볼록한 형상을 갖는 돔 형태의 제1 마이크로렌즈(50,51,52)를 형성한다.

<42> 이때, 상기 제1 마이크로렌즈(50)는 이웃하는 제1 마이크로렌즈(51,52) 사이에 갭(gap)(D1)이 발생될 수 있다.

<43> 도 3을 참조하여, 상기 제1 마이크로렌즈들(50,51,52) 사이의 갭(D1)으로 광이 입사되는 것을 방지하기 위하여 상기 제1 마이크로렌즈(50,51,52)가 형성된 픽셀 어레이 기판(10) 상으로 보조 집광부(61)를 형성한다.

<44> 상기 보조 집광부(61)는 상기 제1 마이크로렌즈(50,51,52)를 포함하는 상기 픽셀 어레이 기판(10) 상부로 산화막(SiO2)(60)을 증착하여 형성한다.

<45> 이는 상기 제1 마이크로렌즈(50,51,52)의 굴절률은 약 1.7 정도이고 상기 산화막(60)의 굴절률은 약 1.4 정도이기 때문에, 굴절률이 약 1인 공기를 통해 입사되는 광은 상기 산화막(60)를 통해 1차로 굴절되어 제1 마이크로렌즈(50,51,52)로 입사되기 때문에 포토다이오드로의 집광율을 향상시킬 수 있는 것이다.

<46> 도 4를 참조하여, 상기 산화막(60) 상부로 포토레지스트막을 도포하고 패터닝하여 마스크 패턴(71)을 형성한다. 상기 마스크 패턴(71)은 상기 제1 마이크로렌즈(50,51,52)의 갭(D1) 영역에 대응하는 부분의 상기 보조 집광부(61) 상면이 노출되도록 상기 산화막(60) 상에 형성된다.

<47> 도 5를 참조하여, 상기 마스크 패턴(71)을 식각마스크로 하여 상기 보조 집광부(61)를 식각하면 상기 제1 마이크로렌즈(50,51,52)의 갭 영역에 대응되는 너비를 갖는 트렌치(62)가 형성된다. 예를 들어, 상기 트렌치(62)는 건식식각방법에 의해 식각되고, 주입가스를 조절하여 상기 트렌치(62)의 바닥면이 오목한 형태를 가지도록 형성

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할 수 있다.

<48> 상기와 같이 보조 집광부(61)의 트렌치(62) 바닥면이 오목한 형태로 형성되어 상기 보조 집광부(61)의 트렌치(62)로 광이 입사되면 상기 트렌치(62)의 바닥면의 오목한 형태에 의해 입사광은 셀(D1) 영역으로 사입사 되지 않고 제1 마이크로렌즈(50,51,52)로 집광될 수 있게 된다.

<49> 도 6을 참조하여, 상기 마스크 패턴(71)을 제거하고 상기 트렌치(62)가 형성된 보조 집광부(61) 상부에 제1 마이크로렌즈(50)와 동일한 마이크로 렌즈 형성용 포토레지스트를 도포한 후 상기 보조 집광부(61)의 표면이 노출되도록 평탄화 시킨다.

<50> 그러면 상기 보조 집광부(61)의 트렌치(62) 내부에는 제2 마이크로렌즈(81)가 형성된다.

<51> 상기 제2 마이크로렌즈(81)의 바닥면은 상기 트렌치(62)의 바닥면 형태에 의하여 제1 마이크로렌즈(50)에 대하여 오목한 형태를 가지도록 형성된다.

<52> 따라서, 도 6에 도시된 바와 같이 상기 보조 집광부(61)의 상측에 상기 셀 영역에 대응되는 위치에 오목한 형태의 제2 마이크로 렌즈(81)가 형성되어 있으므로, 물체로부터 입사되는 광이 상기 제1 마이크로렌즈(50,51,52)의 셀(D1) 영역으로 입사될 경우 상기 광은 상기 제2 마이크로렌즈(81)에 의해 직진 방향에 대하여 바깥쪽 영역으로 1차 굴절되고 그 하부의 보조 집광부(61)에 의해 2차 굴절된 후 제1 마이크로렌즈(50)의 이웃하는 제1 마이크로렌즈(51,52)로 입사되어 포토다이오드로의 광 효율을 증가시킬 수 있다.

<53> 또한, 입사광이 셀 영역으로 입사되는 것이 방지되어 크로스 토크 및 노이즈 발생을 방지하여 광감도를 향상시킬 수 있다.

<54> 또한, 상기 제1 마이크로렌즈의 상부에 산화막으로 이루어진 보조 집광부에 의해 후속의 패키지 또는 범프 공정에서의 충격 또는 파티클 등으로부터 발생할 수 있는 이미지 결함을 방지할 수 있다.

<55> <제2 실시예>

<56> 도 11은 제2 실시예에 따른 이미지 센서를 도시하고 있다.

<57> 제2 실시예의 이미지 센서는 픽셀 어레이 기판(100) 상에 형성된 컬러필터 어레이(130); 상기 컬러필터 어레이(130) 상에 형성된 평탄화층(141); 상기 평탄화층(141) 상에 형성된 마이크로렌즈(150,151,152)를 포함하며, 상기 평탄화층(140)에는 상기 마이크로렌즈(150,151,152)의 셀(D2) 영역에 위치되도록 반사막(181)이 형성된 것을 포함한다.

<58> 또한, 상기 평탄화층(140)은 산화막(SiO_2)이고 상기 반사막(181)은 금속물질로 형성될 수 있다.

<59> 상기와 같이 마이크로렌즈의 셀 영역에 의해 노출되는 평탄화층의 표면에 반사막이 형성되어, 물체로부터 입사되는 빛이 상기 마이크로렌즈의 셀영역으로 직진할 경우 상기 반사막에 의해 외부로 다시 반사된다.

<60> 따라서, 상기 마이크로렌즈의 셀영역으로 빛이 입사되는 것을 사전에 차단하므로써 크로스토크 및 노이즈 발생을 방지하여 이미지 센서의 품질을 향상시킬 수 있다.

<61> 이하, 도 7 내지 도 11을 참조하여 제2 실시예에 따른 이미지 센서의 제조공정을 설명한다.

<62> 도 7을 참조하여, 픽셀 어레이 기판(100) 상으로 단위화소(110)에 대응하는 영역에 컬러필터 어레이(130)를 형성한다.

<63> 상기 픽셀 어레이 기판(100)은 컬러필터 어레이(130)를 통해 입사된 빛을 감지하는 포토다이오드(미도시) 및 상기 포토다이오드에서 발생된 전하를 처리하는 트랜지스터들(미도시)로 구성된 단위화소(110)를 포함한다.

<64> 또한 상기 픽셀 어레이 기판(100)은 단위화소(110)로 신호를 전달하는 금속배선(미도시) 및 절연막(미도시)으로 이루어지는 금속배선층(120) 및 패시베이션막(미도시)을 포함할 수 있다.

<65> 그리고, 상기 픽셀 어레이 기판(100) 상에 상기 컬러필터 어레이(130)를 형성한다.

<66> 상기 컬러필터 어레이(130)는 감광물질 및 안료 또는 염료를 포함하는 컬러필터층(미도시)을 스핀 코팅 공정등을 통해 픽셀 어레이 기판(100) 상에 형성한다. 이어서, 상기 컬러필터층을 패턴 마스크에 의하여 노광한 후 현상하여 상기 픽셀 어레이 기판(100) 상에 컬러필터를 형성한다.

<67> 상기 컬러필터 어레이(130)는 각각의 단위화소(110) 마다 하나의 컬러필터가 형성되어 입사하는 빛으로부터 색

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을 분리해 낸다. 예를 들어, 상기 컬러필터 어레이(130)의 제1 컬러필터는 레드(Red)이고, 제2 컬러필터는 그린(Green)이며, 제3 컬러필터는 블루(Blue)의 3가지 색으로 이루어지며, 인접한 컬러필터들은 서로 약간씩 오버랩되어 단차가 형성된다.

<68> 상기 컬러필터 어레이(30)의 단차를 보완하기 위하여, 상기 컬러필터 어레이 상부로 평탄화층(140)을 형성한다. 예를 들어, 상기 평탄화층(140)은 산화막(SiO_2)을 6000~60000Å의 두께로 형성할 수 있다.

<69> 도 8을 참조하여 상기 평탄화층(140) 상부에 포토레지스트막을 도포하고 패터닝하여 마스크 패턴(170)을 형성한다. 상기 마스크 패턴(170)은 이후 형성되는 마이크로렌즈(150,151,152)의 갭(G2) 영역에 대응하는 상기 평탄화층(61) 상면이 노출되도록 형성된다.

<70> 상기 마스크 패턴(170)을 식각 마스크로 하여 상기 평탄화층(140)을 식각하면 트렌치(142)가 형성된다. 예를 들어, 상기 트렌치(142)의 너비는 약 0.1~0.3㎛ 정도로 형성하고, 상기 트렌치(142) 형성시 상기 평탄화층(141)의 하부에 형성된 상기 컬러필터 어레이(130)를 보호하기 위하여 상기 평탄화층(141)이 완전히 식각되지 않도록 한다.

<71> 도 9 및 도 10을 참조하여, 상기 트렌치(142)가 형성된 평탄화층(141)의 상부로 광속물질을 증착한 다음 평탄화 공정을 진행하여 상기 트렌치(142) 내부에 반사막(181)을 형성한다. 예를 들어, 상기 반사막(181)은 CVD 또는 PVD 방법에 의해 TiN, Al, W 등을 증착하여 반사막층(180)을 형성한 후, CMP 공정에 의해 상기 평탄화층(140)의 표면을 평탄화시켜서 상기 트렌치(142)의 내부에 반사막(181)을 형성할 수 있다.

<72> 도 11 을 참조하여 상기 평탄화층(140) 상부로 포토다이오드로의 집광을 위한 마이크로렌즈(150,151,152)를 형성한다.

<73> 상기 마이크로렌즈(150,151,152)는 상기 평탄화층(140) 상부로 마이크로 렌즈 형성용 포토레지스트를 스핀 공정 등을 통해 도포한다. 그리고, 상기 포토레지스트막(미도시)을 선택적으로 노광 및 현상한 후 각각의 컬러필터 상부에 및 포토레지스트 패턴(미도시)을 형성한다. 이후, 리플로우 공정을 실시하여 볼록한 형상을 갖는 돔 형태의 마이크로렌즈(150,151,152)를 형성한다.

<74> 이때, 상기 마이크로렌즈(150)는 이웃하는 마이크로렌즈(151,152)와의 사이에 갭(gap)(G2)이 발생될 수 있으며, 상기 마이크로렌즈(150,151,152) 사이에 형성된 갭(G2)에 의하여 상기 평탄화층(140)에 형성된 반사막(181)이 노출된 상태가 된다.

<75> 따라서, 도 11에 도시된 바와 같이 상기 마이크로렌즈(150,151,152)들의 갭(G2) 사이에는 반사막(181)이 형성되어 있으므로, 만일 물체로부터 입사되는 광이 상기 마이크로렌즈(150)를 벗어나 상기 마이크로렌즈(150)의 갭(G2) 사이로 직진하게 되면 상기 반사막(181)으로 도달하게 되고 상기 광은 반사막(181)에 의해 다시 외부로 다시 반사되게 되므로, 마이크로렌즈(150,151,152)를 경유하지 않은 광은 포토다이오드로 입사되지 않게 되어 포토다이오드의 광감도를 향상시킬 수 있다.

<76> 또한, 상기 마이크로렌즈(150)의 갭(G2) 사이로 집광되지 않은 빛이 입사되는 것을 반사막(181)에 의하여 차단시킬 수 있으므로, 픽셀 어레이 기판(100)에 배치된 포토 다이오드의 노이즈 및 크로스 토크의 사전에 발생을 차단하여 이미지 센서의 품질을 향상시킬 수 있다.

<77> 이상에서 설명한 본 실시예는 전술한 실시예 및 도면에 의해 한정되는 것이 아니고, 본 실시예의 기술적 사상을 벗어나지 않는 범위 내에서 여러가지 치환, 변형 및 변경할 수 있다는 것은 본 발명이 속하는 기술 분야에서 통상의 지식을 가진 자에게 있어 명백할 것이다.

발명의 효과

<78> 이상에서 설명한 바와 같이 제1 실시예에 따른 이미지 센서 및 그의 제조방법에 의하면 입사광의 굴절율을 높여서 마이크로렌즈의 집광율을 향상시키므로써 이미지센서의 센서티비티를 향상시킬 수 있는 효과가 있다.

<79> 또한, 제1 실시예에 의하면 마이크로렌즈의 상부에 형성된 보조집광부에 의해 후속의 패키지 또는 범프 공정에서의 충격 또는 파티클 등으로부터 발생할 수 있는 이미지 결함을 방지할 수 있는 효과가 있다.

<80> 제2 실시예에 따른 이미지 센서 및 그의 제조방법에 의하면, 마이크로렌즈의 갭 영역에 반사막이 형성되어 갭 영역으로 입사되는 빛을 반사시키므로써 픽셀 간의 크로스토크 및 노이즈 발생을 사전에 차단하여 이미지 센서의 신뢰성을 향상시킬 수 있다.

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도면의 간단한 설명

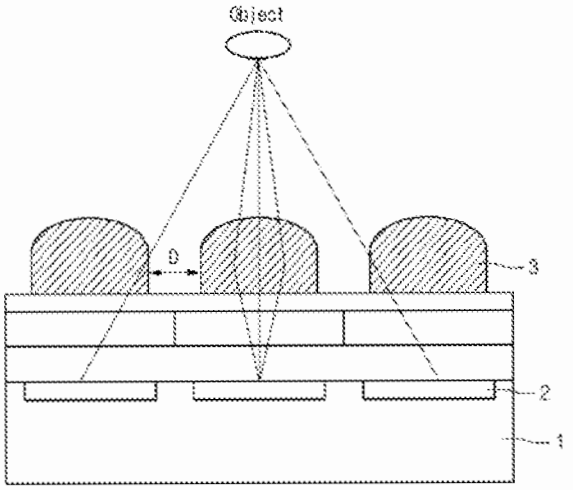
<1> 도 1 은 종래의 이미지 센서를 도시한 도면이다.

<2> 도 2 내지 도 6은 제1 실시예에 따른 이미지 센서의 제조 공정을 나타내는 도면이다.

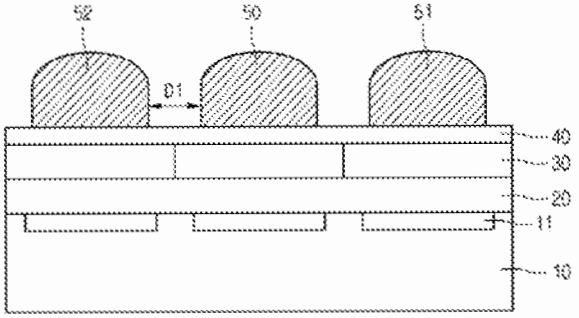
<3> 도 7 내지 도 11는 제2 실시예에 따른 이미지 센서의 제조 공정을 나타내는 도면이다.

도면

도면1

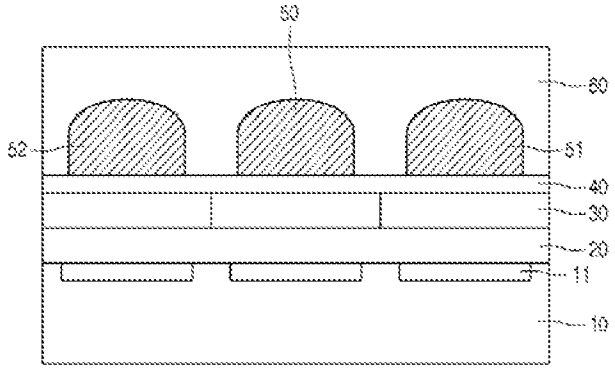


도면2

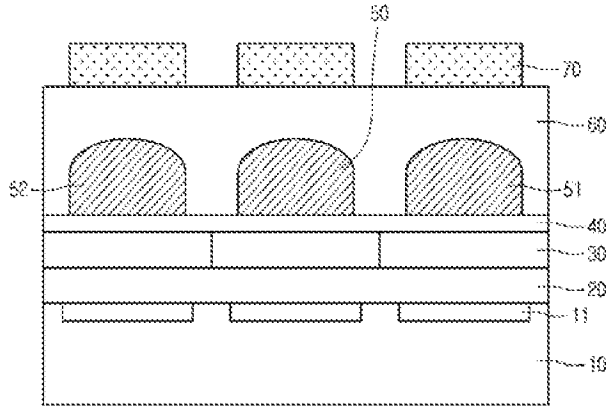


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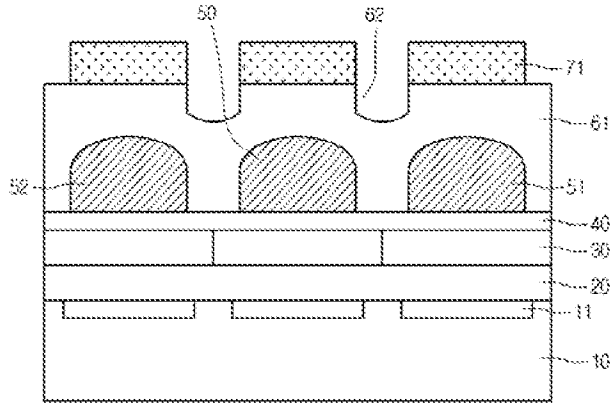
도면3



도면4

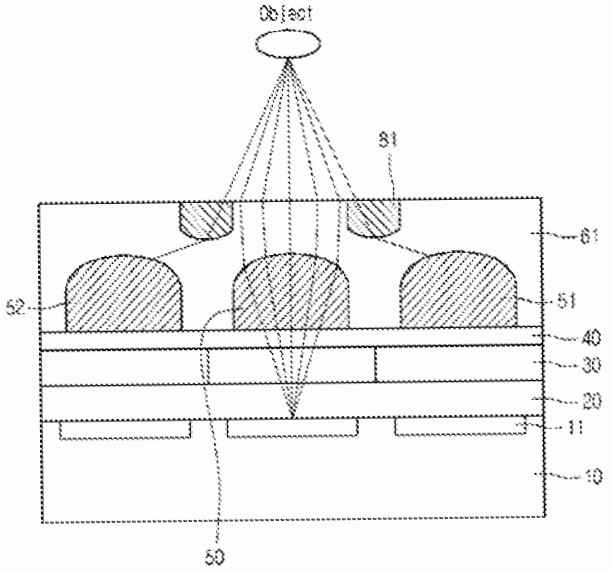


도면5

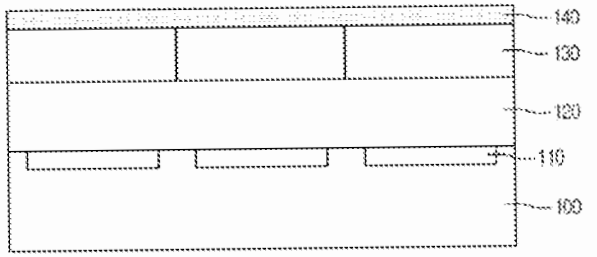


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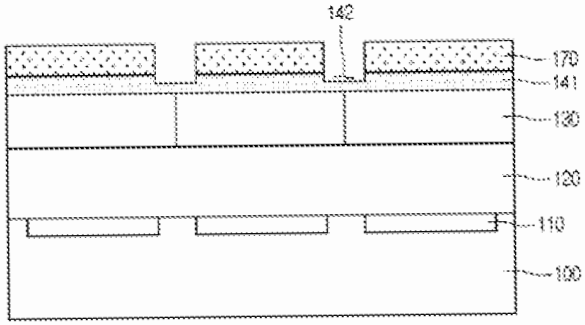
도면6



도면7



도면8



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Applicant	LG Electronics Inc.
Rightholder	LG Electronics Inc.

발명의 명칭

나노 텍스쳐링 구조를 갖는 반도체 웨이퍼 기판을 포함하는벌크형 태양전지의 제조방법

Title of Invention

The bulk type method for manufacturing solar cell including the semiconductor wafer substrate having the nano texturing structure.

요약

본 발명에 따르면, 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사 방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법이 제공된다. 본 발명에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

나노 텍스쳐링, 나노 금속, 촉매, 에칭, 태양전지

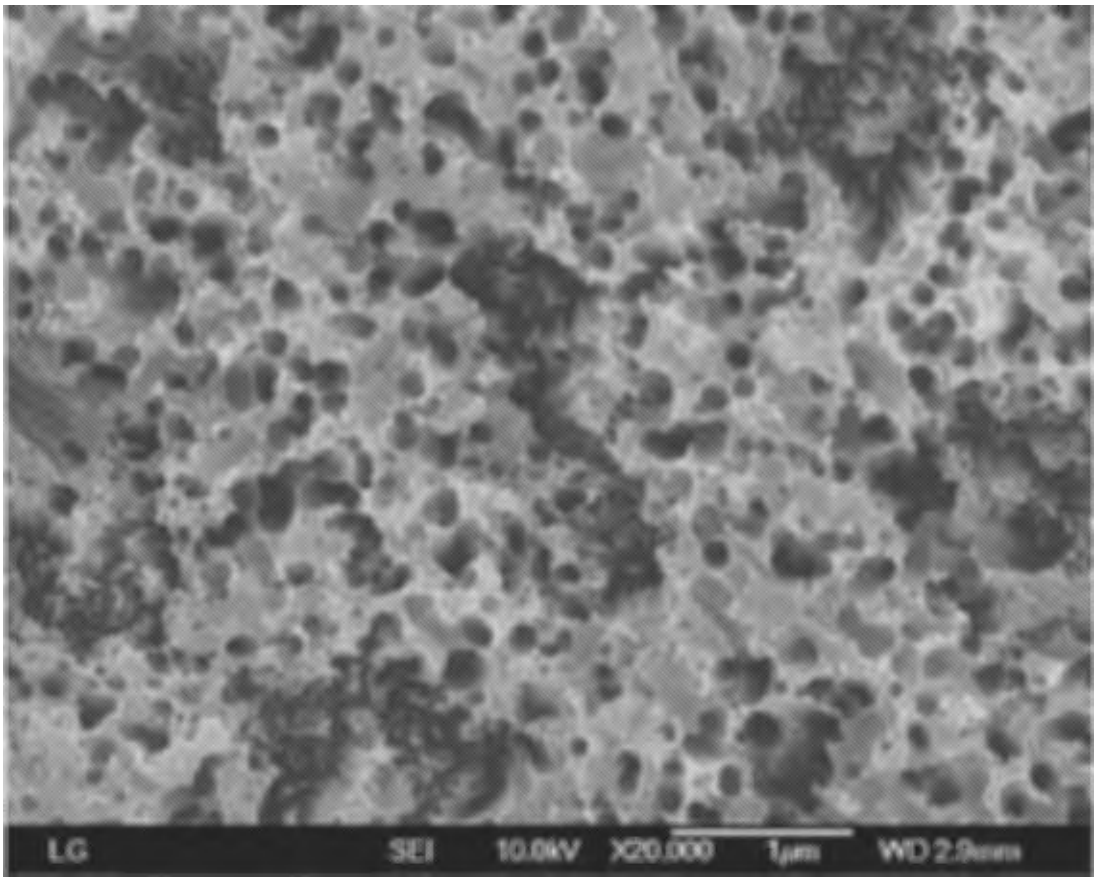
Abstract

According to the present invention, provided is the bulk type method for manufacturing solar cell which easily c an obtain the reflection barrier layer which has the exc ellent characteristic by forming the nano texturing stru cture as to the method for forming the nano texturing structure on the silicon wafer substrate included in the bulk type solar cell using the etching method the metal nanoparticle to the catalyst. According to the present i nvention, provided is the bulk type method for manufac turing solar cell which includes the step of forming the nano texturing structure of having the pattern of the n ano-size on the silicon wafer substrate surface as to t he bulk type method for manufacturing solar cell includi ng the silicon wafer substrate and in which the nano te xturing structure formation step is performed with the etching method the metal to the catalyst.

The nano texturing, the nano metal, the catalyst, the etching, the solar cell

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대표도면(Representative drawing)



청구의 범위

청구 **1**항:

실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되고, 상기 나노 텍스쳐링 구조 형성 단계는, 나노 금속 입자들이 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계;열처리에 의하여 상기 용액을 건조시켜 상기 나노 금속입자들이 사이로 상기 실리콘 웨이퍼 기판이 노출되도록 상기 나노 금속 입자들을 남기는 단계; 에칭액을 사용하여 상기 나노 금속 입자들 사이에 노출된 상기 실리콘 웨이퍼 기판을 에칭하는 단계; 및상기 나노 금속 입자들을 제거하는 단계를 포함하는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구 **2**항:

삭제

청구 **2**항:

Scope of Claims

Claim 1:

The bulk type method for manufacturing solar cell comprising the silicon wafer substrate, wherein the bulk type method for manufacturing solar cell is characterized by comprising the step: step: step: of etching the silicon wafer substrate exposed using the etchant between nano metal particles and the step of removing nano metal particles that nano metal particles leave nano metal particles the silicon wafer substrate is exposed by the interval it dries the solution with the thermal process that the nano texturing structure formation step disperses the solution in which nano metal particles are mixed on the silicon wafer substrate the nano texturing structure formation step is performed with the etching method the metal to the catalyst it includes the step of forming the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface.

Claim 2:

Deletion.

Claim 2:

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삭제

Deletion.

청구 **3**항:

Claim 3:

제1항에 있어서, 상기 나노 금속 입자들의 입경은 20nm 내지 200nm인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which the particle diameter of nano metal particles is 20nm to 200nm.

청구 **4**항:

Claim 4:

제1항에 있어서, 상기 나노 금속 입자들은 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which nano metal particles are at least one among the gold (Au), silver (Ag), copper (Cu), pailadium (Pd), tin (Sn).

청구 **5**항:

Claim 5:

제1항에 있어서, 상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합용액인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which the etchant is the mixture of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluoride (HF).

청구 **6**항:

Claim 6:

제5항에 있어서, 상기 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합비는 10:1인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 5, the bulk type method for manufacturing solar cell in which the mixing ratio of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluoride (HF) is 10:1.

청구 **7**항:

Claim 7:

제1항에 있어서, 상기 용액에서 상기 나노 금속 입자들의 농도는 1000ppm 내지 100000ppm 인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which the concentration of nano metal particles is 1000ppm to 100000ppm in the solution.

청구 **8**항:

Claim 8:

제1항에 있어서, 상기 나노 금속 입자들이 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 중 어느 하나에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell performed by any one of step, of dispersing the solution in which nano metal particles are mixed is the spraying, the spin coating method, and the dipping method.

청구 **9**항:

Claim 9:

제1항, 그리고 제3항 내지 제8항 중 어느 하나의 제조방법으로 제조된 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함하는 벌크형 태양전지.

The bulk type solar cell including the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface manufactured with one manufacturing method among the claims 1 and 3 through 8.

기술분야

Technical Field

본 발명은 벌크형 태양전지의 제조방법에 관한 것이다. 보다 상세하게는 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법에 관한 것이다.

The present invention relates to the bulk type method for manufacturing solar cell. More specifically, it is about the bulk type method for manufacturing solar cell which easily can obtain the reflection barrier layer which has the excellent characteristic by forming the nano texturing structure as to the method for forming the nano texturing structure on the silicon wafer substrate included in the bulk type solar cell using the etching method the metal nanoparticle to the catalyst.

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배경기술

태양전지는 포토다이오드의 일종으로 태양광을 직접 전력으로 전환시키는 목적에 이용되고 있어, 대체 에너지원으로서 지상에서는 물론이고 우주개발을 위해서도 그 이용이 점차 확대되어가고 있어 전력용 전자소자로서 매우 중요하다. 그 구조도 p-n 접합형, 쇼트키 배리어형 및 이종(異種)반도체의 접합으로 이루어지는 것 등이 있으며, 소재로서는 실리콘#183#갈륨비소 등의 결정체, 기타 각종 반도체가 광범위하게 이용되고 있다. 특히 근래에 와서는 다결정(多結晶) 실리콘이나 비정질(非晶質) 실리콘을 이용한 태양전지의 개발과 실용화가 크게 각광을 받고 있다.

그러나 높은 광전변환효율과 품질특성 때문에 단결정의 실리콘 웨이퍼를 기반으로하는 벌크형 태양전지가 상용화되고 있는 실정이다.

일반적으로 실리콘 결정계(crystalline) 태양전지는 실리콘 웨이퍼를 출발 원료로 한다. 실리콘 웨이퍼는 고순도로 정제된 실리콘을 고온으로 가열하여 결정으로 성장된 잉곳을 만들고 이를 절단 및 연마를 통해 대형의 결정판 형태의 웨이퍼 기판을 만든다. 결정은 원자가 규칙적으로 배열된 물질을 의미한다.

종래의 태양전지를 제조하기 위한 웨이퍼의 처리 방법 중 가장 중요한 처리는 기판 표면의 텍스처링(texturing), 즉 조직화이다. 이러한 텍스처링의 목적은 빛을 받는 태양전지의 전면부에서의 반사율을 감소시키고, 태양전지 내에서 빛의 통과 길이를 길게 함으로써 태양전지 내부로 빛이 흡수되도록 하여 효율을 향상시키고자 하는 것이다. 한편, 기판 상에 광학 박막을 형성시켜 반사방지막으로서의 기능을 하게 할 수도 있다.

텍스처링된 종래의 태양전지용 웨이퍼 기판의 표면을 확대한 단면도는 도 1a에 도시하였다. 텍스처링한 후의 표면은 피라미드 구조를 가지므로 옆면에서 관찰할 때 정삼각형의 형상을 가진다.

종래 기술에 의하면, 경면 연마처리(Polishing)된 웨이퍼 표면은 입사되는 태양 빛의 30% 내지 50% 정도를 반사시키고, 표면을 피라미드 형태로 조직화(texturing)시키면 입사되는 태양광의 10% 내지 20% 정도를 반사하게 되어 반사율이 현저하게 줄어든다. 또한, 조직화시킨 표면에 반사방지막(anti-reflection, AR)을 증착시키면 반사율을 약 5% 내지 10%까지 감소시킬 수 있는 것으로 알려져 있다.

그러나, 상기 반사율은 태양광의 주요 흡수 파장대역인 500nm 내지 1000nm 에서관찰된 평균값으로서, 태양광 파장범위의 낮은 파장영역인 300nm 내지 400nm에서는 비교적 높은 반사도를 가지며, 반사방지막의 증착 이후라야만 비로소 상대적으

Background Art

The solar cell is used to the purpose of converting the sunlight into the direct electricity as a kind of the photo diode and it is in ground and the usage is gradually expanded as the alternation energy source for the space development and the purpose is important as the electric power electric component. It has to be made of the structure is the p-n heterogeneous, and the junction of the inhomogeneous semiconductor and schottky barrier type and crystal, the other all kinds of semiconductor including silicone · the GaAs etc. are extensively used as the material. Particularly, recently, development and put to practical use of the solar cell coming and uses the poly-crystal silicon or the amorphous silicon are in the spotlight.

But the high photoelectric conversion efficiency and the bulk type solar cell which therefore has the silicon wafer of the monocrystal as the base with quality characteristic are commercialized.

Generally, the silicon crystal (crystalline) solar cell the silicon wafer to the starting raw material. The silicone refined to the high purity is heated with the high temperature and the silicon wafer makes the ingot grown up to the Decision and this the wafer substrate of the definitive edition form of the large size is made through the cut and grinding. The material in which the atom as to the Decision, is regularly arranged is meant.

Most, the important processing is the texturing of the substrate surface, in other words, the organizing among the processing method of the wafer for manufacturing the conventional solar cell. The reflectivity at the front surface of the solar cell in which the object of such texturing receives light is decreased and Light is absorbed in the solar cell into the solar cell inside by drawing the passing length of light and to improve the efficiency. In the meantime, the optical thin film is formed on the substrate and it functions as the reflection barrier layer.

The cross-sectional view enlarging the surface of the wafer substrate for the textured conventional solar cell showed in the drawing 1a. When observing in side since the surface of the texturing has the pyramid structure it has the shape of the regular triangle.

According to the prior art, 30% of the sunlight in which the wafer surface which becomes with the mirror-polishing processing (Polishing) is incoming to about 50% is reflected and 10% of the sunlight which is incoming if it orders the surface through the pyramid shape with the organizing (texturing) to about 20% is reflected and reflectivity remarkably decreases. Moreover, it is known that reflectivity can be reduced to about 5% to 10% if the reflection barrier layer (anti-reflection, AR) is evaporated in the surface structured.

But reflectivity includes the relatively high reflectivity in 300nm which is 500nm which is the major absorption wavelength band of the sunlight to the average value which becomes with 1000nm west observation and is t

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로 더 낮은 반사도를 갖게 되는 문제점을 가지고 있다. 따라서, 모든 태양광의 파장영역에서 균일하게 낮은 반사율을 갖는 기판 표면을 형성하고자 하는 연구가 진행되었고, 그 결과 나노 구조를 갖는 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지가 개발되었다.

he low wavelength area of the sunlight wavelength range. To 400nm, and the problem of having the reflectivity which is relatively lower as the deposition after of the reflection barrier layer at last. Therefore, in the wavelength area of all sunlights, the research to form the substrate surface having the low reflectivity proceeded and the bulk type solar cell including the silicon wafer substrate in which the nano texturing structure consequently of having the nanostructure was formed was developed.

이러한 나노 텍스쳐링 구조를 갖는 종래 태양전지용 실리콘 웨이퍼 기판의 표면을 확대한 이미지는 도 1과 같다. 도 1을 참조하면 조직화된 웨이퍼 기판 상에는 피라미드 형태의 나노 구조가 형성되어 있음을 알 수 있다.

The image enlarging the surface of the conventional solar battery use silicone wafer substrate having such nano texturing structure is same as those of fig. 1. Referring to Figure 1, it can know that the nanostructure of the pyramid shape is formed on the wafer substrate which becomes systemized.

이러한 나노 텍스쳐링 구조로 형성되는 반사방지막은 넓은 파장영역 및 넓은 입사각 범위에서 반사 방지막으로서의 기능을 수행한다. 종래에는 이러한 나노 텍스쳐링 구조를 형성하기 위해 진공 중에서 염소(Cl) 기체 또는 플루오르화 황(SF6)을 이용하여 반응성 이온 에칭(RIE; Reactive Ion Etching)을 수행하거나, 실리콘 웨이퍼 기판 표면에 금속을 매우 얇게 증착한 후 습식에칭을 수행하였다.

The function as the reflection barrier layer is performed in the wavelength area in which the reflection barrier layer formed into such nano texturing structure is broad and the wide incidence angular range. Conventionally, in order to form the nano texturing structure of being like that the reactive ion etch (RIE: Reactive Ion Etching) was performed among the vacuum using the chlorine (Cl) gas or the sulfonicfluoride (SF(SB)6(/SB)) or it was very thin the metal the wet etching was performed in the silicon wafer substrate surface after doing the deposition.

그러나, 상기 방법 중 반응성 이온 에칭법을 이용하는 방법은 복잡하고 값비싼 장비를 필요로 하는 진공 공정이 필수적이라는 문제가 있다. 한편, 습식 에칭을 이용하는 방법은 금속과 에칭액과의 촉매반응으로 실리콘을 에칭하여 나노 텍스쳐링 구조를 형성하는 방식으로 반응성 이온 에칭(RIE)을 이용하는 방식보다 공정상 간단하다는 장점이 있다. 그러나, 이 방법 또는 진공 장비를 사용하여야 하는 문제가 있다.

But it has the problem the vacuum process which need the expensive equipment in which the method for using the reactive ion etching method among the method is complicated and is essential. In the meantime, the wet etching is used. And a method has the advantage that is simple than the mode which uses with eutectic phase the metal, and the mode etching the silicone to the catalyst reaction with the etchant and forms the nano texturing structure the reactive ion etch (RIE). But there is a problem that it does using this method or the vacuum equipment.

따라서, 진공 장비 등을 사용하지 않기 위하여 실리콘에 전기도금 방식을 이용하여 금속을 얇게 도금한 후 이를 에칭하여 위와 같은 방법으로 나노 텍스쳐링 구조를 형성시키기도 한다.

Therefore, in order not to use the vacuum equipment etc., it thins this the metal is etched using the electro plating after doing plating and the nano texturing structure is formed into the method as in the above in the silicone.

한편, 실리콘 웨이퍼 기판 표면에 나노 텍스쳐링 구조를 형성시키는 또 다른 방법으로는 황 가스 분위기에서 실리콘 웨이퍼 기판 표면에 엑시머 레이저를 조사함으로써 나노 텍스쳐링 구조를 형성하는 방법이 있다.

In the meantime, in another method for forming the nano texturing structure in the silicon wafer substrate surface the sulfur gas atmosphere, it has the method for forming the nano texturing structure by irradiating the excimer laser in the silicon wafer substrate surface.

또한, 나노 텍스쳐링 구조가 아닌 복수 개의 홀로 이루어지는 다공성 구조를 실리콘 웨이퍼 기판에 형성시킴으로써 반사방지막을 형성하기도 한다. 그러나, 이 방법은 기판 표면에 다공성 구조를 형성시키기 위해 전기분해장치 등 복잡한 장치를 이용한 공정을 필요로 한다는 문제가 있다.

Moreover, by forming the porous structure of being alone made of being not nano texturing structure of multiple in the silicon wafer substrate the reflection barrier layer is formed. But this method has the problem that the process of using the apparatus complicated with the electrolysis device etc. in order to form the porous structure in the substrate surface, is required.

따라서, 간단한 공정만으로도 우수한 특성을 가지는 텍스쳐링 구조를 형성시킬 수 있는 기술에 대한 개발이 필요하다.

Therefore, the development about the technology forming the texturing structure of having the excellent

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characteristic into the simple process is.

발명의 내용

Summary of Invention

해결하고자 하는 과제

Problem to be solved

본 발명은 상술한 바와 같은 종래 기술의 문제점을 해결하기 위한 것으로, 진공공정 등의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있는 벌크형 태양전지의 제조방법을 제공하는 데에 그 목적이 있다.

It has the purpose to provides the bulk type method for manufacturing solar cell forming the nano texturing structure of having the excellent anti-reflection property on the silicon wafer substrate surface into the process of becoming streamlined without the need including the vacuum process etc. the invention solves the problem of the prior art as described above.

과제해결 수단

Means to solve the problem

상술한 목적을 달성하기 위한 본 발명의 일 실시형태에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

The step of forming the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface is included as to the bulk type method for manufacturing solar cell including the silicon wafer substrate for achieving the above-described purpose. The bulk type method for manufacturing solar cell performed by the etching method in which the nano texturing structure formation step the metal to the catalyst is provided.

상기 나노 텍스쳐링 구조 형성 단계는, 나노 금속 입자가 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계, 에칭액을 사용하여 상기 나노 금속 입자가 분산된 실리콘 웨이퍼 기판을 에칭하는 단계, 및 상기 나노 금속 입자를 제거하는 단계를 포함할 수 있다.

The nano texturing structure formation step comprises the step of dispersing the solution, and the step of etching the silicon wafer substrate and the step of removing the nano metal particle. As to the step of, the nano metal particle is mixed on the silicon wafer substrate. As to the step of, the nano metal particle is dispersed using the etchant.

상기 나노 금속 입자의 입경은 20nm 내지 200nm로 하는 것이 바람직하다.

It is the be desirable that the particle diameter of the nano metal particle is done by 20nm to 200nm.

상기 나노 금속 입자는 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나로 하는 것이 바람직하다.

It is the be desirable that the nano metal particle is done by at least one among the gold (Au), silver (Ag), copper (Cu), palladium (Pd), tin (Sn).

상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합용액인 것이 바람직하다.

The etchant is the be desirable the mixture of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluoride (HF).

상기 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합비는 10:1로 하는 것이 바람직하다.

It is the be desirable that the mixing ratio of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluoride (HF) is done by 10:1.

상기 용액에서 상기 나노 금속 입자의 농도는 1000ppm 내지 100000ppm 으로 하는 것이 바람직하다.

In the solution, it is the be desirable that the concentration of the nano metal particle is done by 1000ppm to 100000ppm.

상기 나노 금속 입자가 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 중 어느 하나에 의해 수행될 수 있다.

It can be performed by any one of step, of dispersing the solution in which the nano metal particle is mixed is the spraying, the spin coating method, and the dipping method.

상기 목적을 달성하기 위한 본 발명의 벌크형 태양전지는 상기의 제조방법으로 제조되고 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함할 수 있다.

The nano texturing structure of the bulk type solar cell of the invention for achieving the purpose being made of the manufacturing method described in the above and having the pattern of the nano-size on the silicon

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wafer substrate surface is include might.

발명의 효과

Effects of the Invention

본 발명에 따르면, 진공공정 등의 복잡한 공정의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있다.

According to the invention, the nano texturing structure of having the anti-reflection property of being excellent on the silicon wafer substrate surface can be formed into the process of becoming streamlined without the need of the process of being complicated including the vacuum process etc.

상세설명

Detailed Description

이하, 첨부되는 도면을 참조하여 본 발명의 실시형태들을 상세하게 설명하도록 한다.

Hereinafter, specifically the attached embodiments of the invention is illustrated.

도 2는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판의 표면을 전자현미경으로 관찰한 이미지이다.

Figure 2 is an image observing the surface of the solar battery use silicone wafer substrate to the electron microscope according to one embodiment of the invention.

도 2를 참조하면, 본 발명의 실리콘 웨이퍼 기판의 표면은 나노 패턴으로 이루어지는 나노 텍스쳐링 구조를 갖는다.

Referring to Figure 2, the surface of the silicon wafer substrate of the invention has the nano texturing structure of being made of the nano pattern.

상기 나노 텍스쳐링 구조는 나노크기의 패턴으로 이루어져 있다. 즉, 실리콘 웨이퍼 기판 상부에 나노 크기의 패턴들이 조직화되어 있는 구조이다. 나노 텍스쳐링 구조에 의하면 반사방지막(anti-reflection; AR)을 사용하는 것과 다른 특징을 얻을 수 있다. 즉, 반사방지막을 사용하면 특정 파장 대역에서만 반사방지의 효과를 얻을 수 있는 반면 나노 텍스쳐링 구조에 의하면 넓은 파장영역에서 균일하게 반사방지의 효과를 얻을 수 있다.

The nano texturing structure comprises the pattern of the nano-size. That is, the structure where the patterns of the nano-size become systematic in the silicon wafer substrate upside. According to the nano texturing structure, the other characteristic can be obtained the reflection barrier layer (anti-reflection: AR) is used. That is, if the reflection barrier layer is used the effect of the anti-reflection can be obtained from the certain wavelength band on the other hands the effect of the anti-reflection can be uniformly obtained according to the nano texturing structure from the wide wavelength area.

나노 패턴의 크기는 태양전지의 반사방지막으로서의 기능을 최대한 달성할 수 있는 범위 내에서 선택될 수 있다. 즉, 패턴의 크기가 너무 크면 반사율이 저하될 수 있고, 반대로 패턴의 크기가 너무 작으면 반사가 방지되어 태양전지로 흡수되는 광량이 미미해지기 때문에, 그 크기를 적절하게 선택하여야 한다.

The size of the nano pattern can be selected in the range that to the utmost can achieve the function as the anti-reflection layer for a solar cell. That is, reflectivity can be degraded if the size of the pattern is so big and the light quantity which the reflection is prevented if the size of the pattern is so small on the contrary and is absorbed into the solar cell is sight. Therefore the size has to be appropriately selected.

이하, 본 발명의 태양전지용 실리콘 웨이퍼 기판의 나노 텍스쳐링 구조를 형성하는 방법에 대해 설명하기로 한다. 도 3a 내지 도 3f는 본 발명의 일 실시형태에 따른 나노 텍스쳐링 구조를 갖는 실리콘 웨이퍼 기판을 포함하는 태양전지를 제조하는 과정을 설명하는 공정도이다.

Hereinafter, it decides to explain the method for forming the nano texturing structure of the solar battery use silicone wafer substrate of the invention. Figures 3a through 3f are the process map for illustrating the process of manufacturing the solar cell including the silicon wafer substrate having the nano texturing structure according to one embodiment of the invention.

먼저, 도 3a에 도시되는 바와 같은 실리콘 웨이퍼 기판(110) 표면에 잔류하는 네이티브 옥사이드(native oxide; 120)를 제거한다. 실리콘 웨이퍼 기판(110)의 표면에는 실리콘 웨이퍼 기판(110)의 제조 과정에서 형성되거나, 대기 중의 노출 등에 따라 형성되는 네이티브 옥사이드(120)가 잔류하게 되는데 나노 텍스쳐링 구조를 형성하기 전에 이러한 이물질을 제거해

In advance, the native oxide (native oxide: 120) remaining in the silicon wafer substrate (110) surface as illustrated in Figure 3a is removed. In the surface of the silicon wafer substrate (110), it is formed at the manufacturing process of the silicon wafer substrate (110) or before the native oxide (120) formed according to

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주어야 한다. 실리콘 웨이퍼 기판(110)을 플루오르화 수소(HF) 혼합용액에 담금으로써 일어나는 화학 반응에 의해 상기와 같은 네이티브 옥사이드(120)가 제거될 수 있다.

the exposure among the atmosphere etc. remaining behind but forming the nano texturing structure such foreign substance is removed. The above-mentioned native oxide (120) can be the silicon wafer substrate (110) removed in the hydrogen fluoride (HF) mixture as the dipping with the chemical reaction occurring.

그 후, 도 3b에 도시되는 바와 같이, 네이티브 옥사이드(120)가 제거된 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)가 분산되어 있는 수용액(130)을 도포하고 건조시킨다. 후에 나노 금속 입자(135)가 형성되어 있지 않은 부분의 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 텍스쳐링 구조가 형성된다. 상기 수용액(130)에는 나노 금속 입자(135)가 약 1000 ppm 내지 100000ppm 의 농도로 고르게 분산되어 있을 수 있다. 한편, 나노 금속 입자(135)의 입경은 형성하고자 하는 나노 텍스쳐링 구조의 패턴의 형태에 따라 적절하게 선택될 수 있다. 나노 금속 입자(135)의 입경이 너무 크면 나노 텍스쳐링 구조에 포함되는 패턴 간의 거리가 지나치게 멀어지게 되고, 입경이 너무 작으면 패턴이 너무 조밀하게 형성될 수 있으므로, 적절한 범위 내에서 선택될 수 있다. 일례로서 나노 금속 입자(135)의 입경을 20nm 내지 200nm 의 범위 내에서 선택할 수 있다. 한편, 나노 금속 입자의 구성 물질은 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 등으로 할 수 있다. 일례로서, 약 100nm의 입경을 갖는 은(Ag)을 나노 금속 입자(135)로 선택할 수 있다.

Thereafter, as shown in Figure 3b, the aqueous solution (130) in which the nano metal particle (135) is dispersed is coated with on the silicon wafer substrate (110) from which the native oxide (120) is removed and it dries. After, the nano texturing structure is formed since the silicon wafer substrate (110) of the part in which the nano metal particle (135) is not formed is etched. In the aqueous solution (130), the nano metal particle (135) is evenly dispersed into the concentration of about 1000ppm to 100000ppm. In the meantime, according to the form which the particle diameter of the nano metal particle (135) forms of the pattern of the nano texturing structure, it can be appropriately selected. If the particle diameter of the nano metal particle (135) is so large, the distance included in the nano texturing structure between the pattern becomes overly distant and the pattern can be so tightly formed if the grain size is so small. Therefore it can be selected in the proper range. As an example, the particle diameter of the nano metal particle (135) can be chosen in the range of 20nm to 200nm. In the meantime, the configuration element of the nano metal particle can be done by the gold (Au), the silver (Ag), the copper (Cu), the palladium (Pd), the tin (Sn) etc. As an example, the silver (Ag) having the particle diameter of about 100nm can be selected as the nano metal particle (135).

한편, 나노 금속 입자(135)가 혼합되어 있는 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 도포하는 데에는 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 등이 이용될 수 있다. 스프레이법은 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 고르게 분사하는 방식이고, 스핀코팅법은 실리콘 웨이퍼 기판(110) 상에 수용액(130)을 떨어뜨린 후 이를 회전시켜 수용액(130)이 원심력에 의해 실리콘 웨이퍼 기판(110) 상에 코팅될 수 있도록 하는 방식이며, 디핑법은 실리콘 웨이퍼 기판(110)을 수용액(130)에 담가 코팅을 하는 방식이다. 이러한 방식으로 나노 금속 입자(135)가 분산되어 있는 수용액(130)이 실리콘 웨이퍼 기판(110) 상에 도포되면, 열처리 등을 통하여 이를 건조시켜 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)만이 남을 수 있도록 한다.

In the meantime, the spraying, the spin coating method, the dipping method etc. can be used to coat with the aqueous solution (130) in which the nano metal particle (135) is mixed on the silicon wafer substrate (110). It is the mode in which the spraying evenly sprays the aqueous solution (130) on the silicon wafer substrate (110) and it is the mode in which it rotates this after the spin coating method drops down the aqueous solution (130) on the silicon wafer substrate (110) and the aqueous solution (130) is coated with the centrifugal force on the silicon wafer substrate (110) and it is the mode in which the dipping method dips the silicon wafer substrate (110) in the aqueous solution (130) and coated. In this way, if the aqueous solution (130) in which the nano metal particle (135) is dispersed is coated on the silicon wafer substrate (110) this is dried through the thermal process etc. and it remains on the silicon wafer substrate (110) only the nano metal particle (135).

다음으로, 실리콘 웨이퍼 기판(110)을 에칭액에 담궈 에칭(etching)한다. 상기 에칭액으로는 플루오르화 수소(HF)와 과산화수소수(H2O2)가 혼합되어 있는 용액을 사용할 수 있다. 본래는 플루오르화 수소(HF)와 과산화수소수(H2O2)가 혼합

Next, the silicon wafer substrate (110) is dipped in the etchant and it does with the etching (etching). The solution in which the hydrogen fluoride (HF) and hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) are mixed can

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되어 있는 용액만으로는 실리콘 웨이퍼 기판(110)을 에칭시킬 수 없으나, 기판(110) 상에 분산되어 있는 나노 금속 입자(135)가 촉매로 작용하여 나노 금속 입자(135)들 사이의 공간에 노출되어 있는 실리콘 웨이퍼 기판(110)이 에칭될 수 있는 것이다. 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합비는 10:1 정도로 하는 것이 바람직하다. 도 3c는 이러한 방법에 의해 에칭된 실리콘 웨이퍼 기판(110)의 단면 구조를 나타낸다. 나노 금속 입자(135)들 사이의 공간에 노출된 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 패턴으로 형성되는 나노 텍스쳐링 구조가 형성되게 되는 것이다.

be used as the etchant. The inherent cannot etch the silicon wafer substrate (110) to the solution in which t he hydrogen fluoride (HF) and hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) are mixed. But the nano met al particle (135) dispersed on the substrate (110) acts on the catalyst and the exposed silicon wafer substrat e (110) can be etched on space between nano metal p article (135). It is the be desirable that the mixing ratio of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/S B)) and hydrogen fluoride (HF) is done by about 10:1. Figure 3c shows the section structure of the silicon wa fer substrate (110) etched with such method. Since th e silicon wafer substrate (110) exposed to space betw een nano metal particle (135) is etched the nano textu ring structure of being formed with the nano pattern is formed.

에칭이 완료되면 순수(pure water)를 이용하여 실리콘 웨이퍼 기판(110)을 세척한 후에 금속 에칭을 수행하여 나노 금속 입자(135)를 제거한다. 도 3d는 에칭에 의해 나노 금속 입자(135)가 제거된 실리콘 웨이퍼 기판(110)의 모습을 나타낸다. 이렇게 함으로써 표면에 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판(110)이 얻어질 수 있다.

When the etching is completed, after the silicon wafer substrate (110) is washed using the pure water the me tal etching is performed and the nano metal particle (1 35) is removed. Figure 3d shows the display of the silic on wafer substrate (110) in which the nano metal parti cle (135) is removed using the etching. By doing this, t he silicon wafer substrate (110) in which the nano text uring structure is formed in the surface can be obtaine d.

그 후, 도 3e에 도시되는 바와 같이, 상기 나노 텍스쳐링 구조가 형성된 제1전도성(예를 들면, p형)을 갖는 실리콘 웨이퍼 기판(110)에 제2전도성(예를 들면, n형)을 갖는 물질을 확산시켜 p-n 접합을 형성하고, 표면에 패시베이션 층(passivation; 150)을 형성한다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)을 부동태화시켜 표면 결함을 최소화하기 위한 것이다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)의 표면을 산화시킴으로써 형성될 수 있다. 즉, 상기 산화 반응에 의해 안정한 물질인 실리콘 산화물(SiOx)이 실리콘 웨이퍼 기판(110) 표면에 형성됨으로써 패시베이션 층(150)이 형성될 수 있다. 한편, 실리콘 질화물(SiNx) 등의 물질을 상기 실리콘 웨이퍼 기판(110) 표면에 증착함으로써 패시베이션 층(150)을 형성시킬 수도 있다.

Thereafter, as shown in Figure 3e, material having the second conductivity (for example, the n-type) are diffu sed over the silicon wafer substrate (110) having the fi rst conductivity (for example, the p-type) in which the nano texturing structure is formed and the p-n junction is formed and the passivation layer (passivation: 150) i s formed on the surface. The passivation layer (150) m akes something passive the silicon wafer substrate (11 0) and the surface defect is to be minimized. The passi vation layer (150) can be formed by oxidizing the surfa ce of the silicon wafer substrate (110). That is, since t he silicon oxide (SiO(SB)x(/SB)) which is material which are stable with the oxidation reaction is formed in the s ilicon wafer substrate (110) surface the passivation lay er (150) can be formed. In the meantime, the passivati on layer (150) can be formed by depositing the materia l including the silicon nitride (SiN(SB)x(/SB)) etc. on th e silicon wafer substrate (110) surface.

다음으로, 도 3f에 도시되는 바와 같이, 상기 패시베이션 층(150)이 형성된 실리콘 웨이퍼 기판(110) 상에 전극(170)을 형성시킴으로써 태양전지가 완성된다. 전극(170)은 통상의 인쇄법(printing) 등에 의해 형성될 수 있다.

Next, as shown in Figure 3f, by forming the electrode (170) on the silicon wafer substrate (110) in which the passivation layer (150) is formed the solar cell is compl eted. The electrode (170) is formed by the normal print ing method etc.

이러한 방법에 의하면, 진공공정 또는 전기분해공정 등을 사용하지 않고도 실리콘 웨이퍼 기판에 나노 텍스쳐링 구조를 형성할 수 있으며, 이에 따라 나노 텍스쳐링 구조 형성에 필요한 작업 공수를 간소화할 수 있고, 제조 원가가 절감될 수 있다.

According to such method, the nano texturing structure can be formed on the silicon wafer substrate even though the vacuum process or the electrolysis pr ocess etc. are not used and accordingly the necessary man-hour can be streamlined in the nano texturing text uring and the manufacturing cost can be cut down.

또한, 값비싼 장비 또는 복잡한 공정 없이도 나노 텍스쳐링 구조와 같은 우수한 특성의 반사방지막을 얻을 수 있다.

Moreover, expensive the reflection barrier layer of the excellent characteristic like the nano texturing structur e can be obtained without the complex process.

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면책안내

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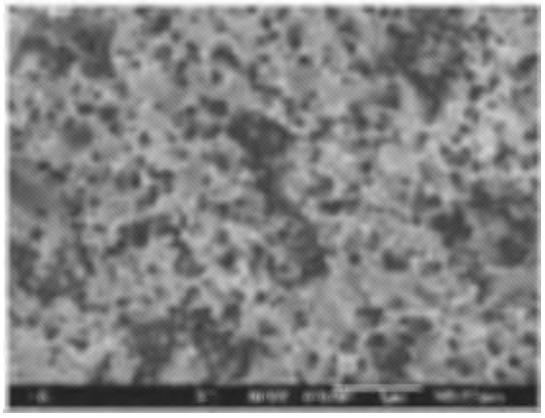
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(54) 발명의 명칭 **나노 텍스쳐링 구조를 갖는 반도체 웨이퍼 기판을 포함하는벌크형 태양전지의 제조방법**

(57) 요 약

본 발명에 따르면, 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법이 제공된다. 본 발명에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

대 표 도 - 도2



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특허청구의 범위

청구항 1

실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서,

상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되,

상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 2

제1항에 있어서,

상기 나노 텍스쳐링 구조 형성 단계는,

나노 금속 입자가 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계;

에칭액을 사용하여 상기 나노 금속 입자가 분산된 실리콘 웨이퍼 기판을 에칭하는 단계; 및

상기 나노 금속 입자를 제거하는 단계를 포함하는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 3

제2항에 있어서,

상기 나노 금속 입자의 입경은 20㎚ 내지 200㎚인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 4

제2항에 있어서,

상기 나노 금속 입자는 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 5

제2항에 있어서,

상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합용액인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 6

제5항에 있어서,

상기 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합비는 10:1인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 7

제2항에 있어서,

상기 용액에서 상기 나노 금속 입자의 농도는 1000ppm 내지 100000ppm 인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 8

제2항에 있어서,

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상기 나노 금속 입자가 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 중 어느 하나에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 9

제1항 내지 제8항 중 어느 하나의 제조방법으로 제조된 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함하는 벌크형 태양전지.

명 세 서

발명의 상세한 설명

기 술 분 야

[0001] 본 발명은 벌크형 태양전지의 제조방법에 관한 것이다. 보다 상세하게는 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법에 관한 것이다.

배 경 기 술

[0002] 태양전지는 포토다이오드의 일종으로 태양광을 직접 전력으로 전환시키는 목적에 이용되고 있어, 대체 에너지원으로서 지상에서는 물론이고 우주개발을 위해서도 그 이용이 점차 확대되어가고 있어 전력용 전자소자로서 매우 중요하다. 그 구조도 p-n 접합형, 쇼트키 배리어형 및 이종(異種)반도체의 접합으로 이루어지는 것 등이 있으며, 소재로서는 실리콘 갈륨비소 등의 결정체, 기타 각종 반도체가 광범위하게 이용되고 있다. 특히 근래에 와서는 다결정(多結晶) 실리콘이나 비정질(非晶質) 실리콘을 이용한 태양전지의 개발과 실용화가 크게 각광을 받고 있다.

[0003] 그러나 높은 광전변환효율과 품질특성 때문에 단결정의 실리콘 웨이퍼를 기반으로하는 벌크형 태양전지가 상용화되고 있는 실정이다.

[0004] 일반적으로 실리콘 결정계(crystalline) 태양전지는 실리콘 웨이퍼를 출발 원료로 한다. 실리콘 웨이퍼는 고순도로 정제된 실리콘을 고온으로 가열하여 결정으로 성장된 잉곳을 만들고 이를 절단 및 연마를 통해 대형의 결정판 형태의 웨이퍼 기판을 만든다. 결정은 원자가 규칙적으로 배열된 물질을 의미한다.

[0005] 종래의 태양전지를 제조하기 위한 웨이퍼의 처리 방법 중 가장 중요한 처리는 기판 표면의 텍스쳐링(texturing), 즉 조직화이다. 이러한 텍스쳐링의 목적은 빛을 받는 태양전지의 전면부에서의 반사율을 감소시키고, 태양전지 내에서 빛의 통과 길이를 길게 함으로써 태양전지 내부로 빛이 흡수되도록 하여 효율을 향상시키고자 하는 것이다. 한편, 기판 상에 광학 박막을 형성시켜 반사방지막으로서의 기능을 하게 할 수도 있다.

[0006] 텍스쳐링된 종래의 태양전지용 웨이퍼 기판의 표면을 확대한 단면도는 도 1a에 도시하였다. 텍스쳐링한 후의 표면은 피라미드 구조를 가지므로 옆면에서 관찰할 때 정삼각형의 형상을 가진다.

[0007] 종래 기술에 의하면, 경면 연마처리(Polishing)된 웨이퍼 표면은 입사되는 태양 빛의 30% 내지 50% 정도를 반사시키고, 표면을 피라미드 형태로 조직화(texturing)시키면 입사되는 태양광의 10% 내지 20% 정도를 반사하게 되어 반사율이 현저하게 줄어든다. 또한, 조직화시킨 표면에 반사방지막(anti-reflection, AR)을 증착시키면 반사율을 약 5% 내지 10%까지 감소시킬 수 있는 것으로 알려져 있다.

[0008] 그러나, 상기 반사율은 태양광의 주요 흡수 파장대역인 500㎚ 내지 1000㎚ 에서관찰된 평균값으로서, 태양광 파장범위의 낮은 파장영역인 300㎚ 내지 400㎚에서는 비교적 높은 반사도를 가지며, 반사방지막의 증착 이후라야만 비로소 상대적으로 더 낮은 반사도를 갖게 되는 문제점을 가지고 있다. 따라서, 모든 태양광의 파장영역에서 균일하게 낮은 반사율을 갖는 기판 표면을 형성하고자 하는 연구가 진행되었고, 그 결과 나노 구조를 갖는 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지가 개발되었다.

[0009] 이러한 나노 텍스쳐링 구조를 갖는 종래 태양전지용 실리콘 웨이퍼 기판의 표면을 확대한 이미지는 도 1과 같다. 도 1을 참조하면 조직화된 웨이퍼 기판 상에는 피라미드 형태의 나노 구조가 형성되어 있음을 알 수

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있다.

[0010] 이러한 나노 텍스쳐링 구조로 형성되는 반사방지막은 넓은 파장영역 및 넓은 입사각 범위에서 반사 방지막으로서의 기능을 수행한다. 종래에는 이러한 나노 텍스쳐링 구조를 형성하기 위해 진공 중에서 염소(Cl) 가스 또는 플루오르화 황(SF_6)을 이용하여 반응성 이온 에칭(RIE: Reactive Ion Etching)을 수행하거나, 실리콘 웨이퍼 기판 표면에 금속을 매우 얇게 증착 한 후 습식에칭을 수행하였다.

[0011] 그러나, 상기 방법 중 반응성 이온 에칭법을 이용하는 방법은 복잡하고 값비싼 장비를 필요로 하는 진공 공정이 필수적이라는 문제가 있다. 한편, 습식 에칭을 이용하는 방법은 금속과 에칭액과의 촉매반응으로 실리콘을 에칭하여 나노 텍스쳐링 구조를 형성하는 방식으로 반응성 이온 에칭(RIE)을 이용하는 방식보다 공정상 간단하다는 장점이 있다. 그러나, 이 방법 또는 진공 장비를 사용하여야 하는 문제가 있다.

[0012] 따라서, 진공 장비 등을 사용하지 않기 위하여 실리콘에 전기 도금 방식을 이용하여 금속을 얇게 도금한 후 이를 에칭하여 위와 같은 방법으로 나노 텍스쳐링 구조를 형성시키기도 한다.

[0013] 한편, 실리콘 웨이퍼 기판 표면에 나노 텍스쳐링 구조를 형성시키는 또 다른 방법으로는 할 가스 분위기에서 실리콘 웨이퍼 기판 표면에 엑시머 레이저를 조사함으로써 나노 텍스쳐링 구조를 형성하는 방법이 있다.

[0014] 또한, 나노 텍스쳐링 구조가 아닌 복수 개의 홈로 이루어지는 다공성 구조를 실리콘 웨이퍼 기판에 형성시킴으로써 반사방지막을 형성하기도 한다. 그러나, 이 방법은 기판 표면에 다공성 구조를 형성시키기 위해 전기분해 장치 등 복잡한 장치를 이용한 공정을 필요로 한다는 문제가 있다.

[0015] 따라서, 간단한 공정만으로도 우수한 특성을 가지는 텍스쳐링 구조를 형성시킬 수 있는 기술에 대한 개발이 필요하다.

발명의 내용

해결 하고자하는 과제

[0016] 본 발명은 상술한 바와 같은 종래 기술의 문제점을 해결하기 위한 것으로, 진공공정 등의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있는 벌크형 태양전지의 제조방법을 제공하는 데에 그 목적이 있다.

과제 해결수단

[0017] 상술한 목적을 달성하기 위한 본 발명의 일 실시형태에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

[0018] 상기 나노 텍스쳐링 구조 형성 단계는, 나노 금속 입자가 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계, 에칭액을 사용하여 상기 나노 금속 입자가 분산된 실리콘 웨이퍼 기판을 에칭하는 단계, 및 상기 나노 금속 입자를 제거하는 단계를 포함할 수 있다.

[0019] 상기 나노 금속 입자의 입경은 20nm 내지 200nm로 하는 것이 바람직하다.

[0020] 상기 나노 금속 입자는 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나로 하는 것이 바람직하다.

[0021] 상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합용액인 것이 바람직하다.

[0022] 상기 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합비는 10:1로 하는 것이 바람직하다.

[0023] 상기 용액에서 상기 나노 금속 입자의 농도는 1000ppm 내지 100000ppm 으로 하는 것이 바람직하다.

[0024] 상기 나노 금속 입자가 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin

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coating), 디핑법(dipping) 중 어느 하나에 의해 수행될 수 있다.

[0025] 상기 목적을 달성하기 위한 본 발명의 벌크형 태양전지는 상기의 제조방법으로 제조되고 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함할 수 있다.

효 과

[0026] 본 발명에 따르면, 진공공정 등의 복잡한 공정의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있다.

발명의 실시를 위한 구체적인 내용

[0027] 이하, 첨부되는 도면을 참조하여 본 발명의 실시형태들을 상세하게 설명하도록 한다.

[0028] 도 2는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판의 표면을 전자현미경으로 관찰한 이미지이다.

[0029] 도 2를 참조하면, 본 발명의 실리콘 웨이퍼 기판의 표면은 나노 패턴으로 이루어지는 나노 텍스쳐링 구조를 갖는다.

[0030] 상기 나노 텍스쳐링 구조는 나노크기의 패턴으로 이루어져 있다. 즉, 실리콘 웨이퍼 기판 상부에 나노 크기의 패턴들이 조직화되어 있는 구조이다. 나노 텍스쳐링 구조에 의하면 반사방지막(anti-reflection: AR)을 사용하는 것과 다른 특징을 얻을 수 있다. 즉, 반사방지막을 사용하면 특정 파장 대역에서만 반사방지의 효과를 얻을 수 있는 반면 나노 텍스쳐링 구조에 의하면 넓은 파장영역에서 균일하게 반사방지의 효과를 얻을 수 있다.

[0031] 나노 패턴의 크기는 태양전지의 반사방지막으로서의 기능을 최대한 달성할 수 있는 범위 내에서 선택될 수 있다. 즉, 패턴의 크기가 너무 크면 반사율이 저하될 수 있고, 반대로 패턴의 크기가 너무 작으면 반사가 방지되어 태양전지로 흡수되는 광량이 미미해지기 때문에, 그 크기를 적절하게 선택하여야 한다.

[0032] 이하, 본 발명의 태양전지용 실리콘 웨이퍼 기판의 나노 텍스쳐링 구조를 형성하는 방법에 대해 설명하기로 한다. 도 3a 내지 도 3f는 본 발명의 일 실시형태에 따른 나노 텍스쳐링 구조를 갖는 실리콘 웨이퍼 기판을 포함하는 태양전지를 제조하는 과정을 설명하는 공정도이다.

[0033] 먼저, 도 3a에 도시되는 바와 같은 실리콘 웨이퍼 기판(110) 표면에 잔류하는 네이티브 옥사이드(native oxide: 130)를 제거한다. 실리콘 웨이퍼 기판(110)의 표면에는 실리콘 웨이퍼 기판(110)의 제조 과정에서 형성되거나, 대기 중의 노출 등에 따라 형성되는 네이티브 옥사이드(120)가 잔류하게 되는데 나노 텍스쳐링 구조를 형성하기 전에 이러한 이물질을 제거해주어야 한다. 실리콘 웨이퍼 기판(110)을 플루오르화 수소(HF) 혼합용액에 담금으로써 일어나는 화학 반응에 의해 상기와 같은 네이티브 옥사이드(120)가 제거될 수 있다.

[0034] 그 후, 도 3b에 도시되는 바와 같이, 네이티브 옥사이드(120)가 제거된 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)가 분산되어 있는 수용액(130)을 도포하고 건조시킨다. 후에 나노 금속 입자(135)가 형성되어 있지 않은 부분의 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 텍스쳐링 구조가 형성된다. 상기 수용액(130)에는 나노 금속 입자(135)가 약 1000ppm 내지 100000ppm 의 농도로 고르게 분산되어 있을 수 있다. 한편, 나노 금속 입자(135)의 입경은 형성하고자 하는 나노 텍스쳐링 구조의 패턴의 형태에 따라 적절하게 선택될 수 있다. 나노 금속 입자(135)의 입경이 너무 크면 나노 텍스쳐링 구조에 포함되는 패턴 간의 거리가 지나치게 멀어지게 되고, 입경이 너무 작으면 패턴이 너무 조밀하게 형성될 수 있으므로, 적절한 범위 내에서 선택될 수 있다. 일례로서 나노 금속 입자(135)의 입경을 20nm 내지 200nm 의 범위 내에서 선택할 수 있다. 한편, 나노 금속 입자의 구성 물질은 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 등으로 할 수 있다. 일례로서, 약 100nm의 입경을 갖는 은(Ag)을 나노 금속 입자(135)로 선택할 수 있다.

[0035] 한편, 나노 금속 입자(135)가 혼합되어 있는 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 도포하는 데에는 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 등이 이용될 수 있다. 스프레이법은 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 고르게 분사하는 방식이고, 스핀코팅법은 실리콘 웨이퍼 기판(110) 상에 수용액(130)을 떨어뜨린 후 이를 회전시켜 수용액(130)이 원심력에 의해 실리콘 웨이퍼 기판(110) 상에 코팅될 수 있도록 하는 방식이며, 디핑법은 실리콘 웨이퍼 기판(110)을 수용액(130)에 담가 코팅을 하는 방식이다. 이

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러한 방식으로 나노 금속 입자(135)가 분산되어 있는 수용액(130)이 실리콘 웨이퍼 기판(110) 상에 도포되면, 열처리 등을 통하여 이를 건조시켜 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)만이 남을 수 있도록 한다.

[0036] 다음으로, 실리콘 웨이퍼 기판(110)을 에칭액에 담궈 에칭(etching)한다. 상기 에칭액으로는 플루오르화 수소(HF)와 과산화수소수(H_2O_2)가 혼합되어 있는 용액을 사용할 수 있다. 본래는 플루오르화 수소(HF)와 과산화수소수(H_2O_2)가 혼합되어 있는 용액만으로는 실리콘 웨이퍼 기판(110)을 에칭시킬 수 없으나, 기판(110) 상에 분산되어 있는 나노 금속 입자(135)가 촉매로 작용하여 나노 금속 입자(135)들 사이의 공간에 노출되어 있는 실리콘 웨이퍼 기판(110)이 에칭될 수 있는 것이다. 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합비는 10:1 정도로 하는 것이 바람직하다. 도 3c는 이러한 방법에 의해 에칭된 실리콘 웨이퍼 기판(110)의 단면 구조를 나타낸다. 나노 금속 입자(135)들 사이의 공간에 노출된 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 패턴으로 형성되는 나노 텍스쳐링 구조가 형성되게 되는 것이다.

[0037] 에칭이 완료되면 순수(pure water)를 이용하여 실리콘 웨이퍼 기판(110)을 세척한 후에 금속 에칭을 수행하여 나노 금속 입자(135)를 제거한다. 도 3d는 에칭에 의해 나노 금속 입자(135)가 제거된 실리콘 웨이퍼 기판(110)의 모습을 나타낸다. 이렇게 함으로써 표면에 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판(110)이 얻어질 수 있다.

[0038] 그 후, 도 3e에 도시되는 바와 같이, 상기 나노 텍스쳐링 구조가 형성된 제1전도성(예를 들면, p형)을 갖는 실리콘 웨이퍼 기판(110)에 제2전도성(예를 들면, n형)을 갖는 물질을 확산시켜 p-n 접합을 형성하고, 표면에 패시베이션 층(passivation; 150)을 형성한다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)을 부동태화시켜 표면 결함을 최소화하기 위한 것이다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)의 표면을 산화시킴으로써 형성될 수 있다. 즉, 상기 산화 반응에 의해 안정한 물질인 실리콘 산화물(SiO_2)이 실리콘 웨이퍼 기판(110) 표면에 형성됨으로써 패시베이션 층(150)이 형성될 수 있다. 한편, 실리콘 질화물(SiN_x) 등의 물질을 상기 실리콘 웨이퍼 기판(110) 표면에 증착함으로써 패시베이션 층(150)을 형성시킬 수도 있다.

[0039] 다음으로, 도 3f에 도시되는 바와 같이, 상기 패시베이션 층(150)이 형성된 실리콘 웨이퍼 기판(110) 상에 전극(170)을 형성시킴으로써 태양전지가 완성된다. 전극(170)은 통상의 인쇄법(printing) 등에 의해 형성될 수 있다.

[0040] 이러한 방법에 의하면, 진공공정 또는 전기분해공정 등을 사용하지 않고도 실리콘 웨이퍼 기판에 나노 텍스쳐링 구조를 형성할 수 있으며, 이에 따라 나노 텍스쳐링 구조 형성에 필요한 작업 공수를 간소화할 수 있고, 제조 원가가 절감될 수 있다.

[0041] 또한, 값비싼 장비 또는 복잡한 공정 없이도 나노 텍스쳐링 구조와 같은 우수한 특성의 반사방지막을 얻을 수 있다.

도면의 간단한 설명

[0042] 도 1은 종래 태양전지용 실리콘 웨이퍼 기판 표면에 형성된 나노 텍스쳐링 구조를 전자현미경으로 관찰한 이미지이다.

[0043] 도 2는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판의 표면을 전자현미경으로 관찰한 이미지이다.

[0044] 도 3a 내지 도 3f는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조과정을 설명하는 공정도이다.

[0045] <도면의 주요부분에 대한 부호의 설명>

[0046] 110: 기판 120: 네이티브 옥사이드

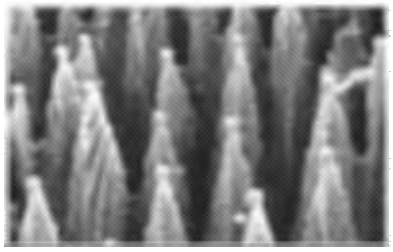
[0047] 130: 나노 금속 입자가 혼합된 수용액 135: 금속 나노 입자

[0048] 150: 패시베이션 층 170: 전극

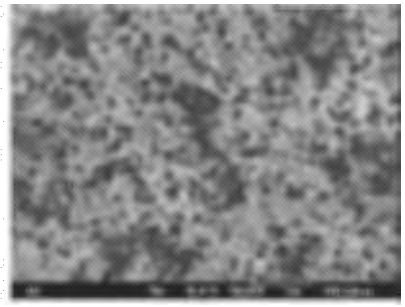
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도면

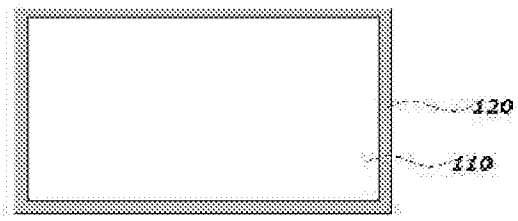
도면1



도면2

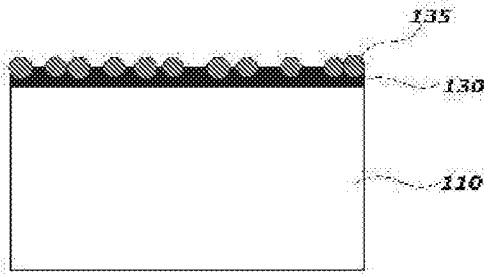


도면3a

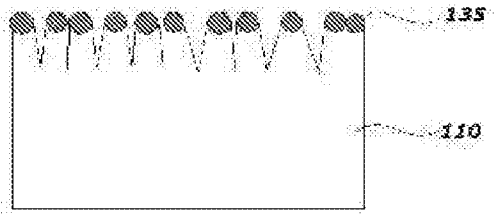


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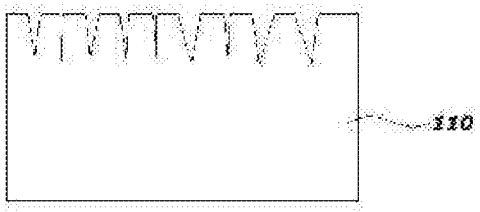
도면3b



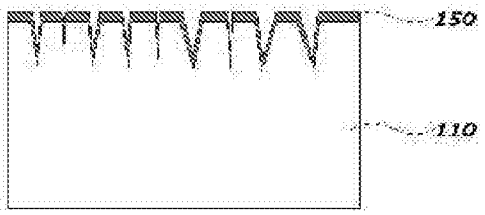
도면3c



도면3d

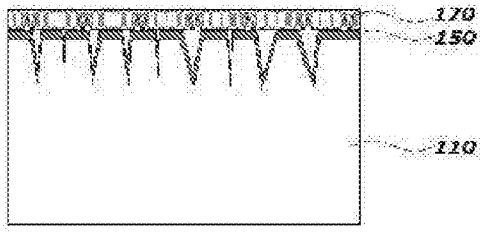


도면3e



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도면3



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Espacenet

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METHOD FOR MANUFACTURING SOLAR CELL

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Classification: - international:***H01L31/042***
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Application number: KR20080085480 20080829 Global Dossier

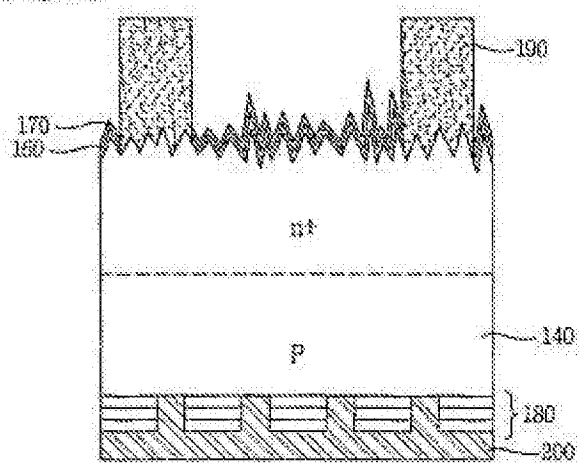
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Abstract of KR20100026463 (A)

PURPOSE: A method for manufacturing a solar cell is provided to improve the conversion efficiency of the solar cell by etching the surface of a textured-wafer in order to remove the defects of the wafer. CONSTITUTION: A convex part and a concave part are irregularly located on the surface of a wafer(140). Reflection barrier layers(160, 170) are placed on the one surface of the wafer. A reflective layer (180) including a plurality of reflective films is formed on the other surface of the wafer. A first electrode contacts to the first type semiconductor of the wafer. A

[Fig. 9]



second electrode contacts to the second type semiconductor of the wafer.

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전체 청구항 수 : 총 10 항

(54) 태양 전지의 제조 방법

(57) 요 약

본 발명의 태양 전지 제조 방법은 절단된 웨이퍼의 하나의 표면에 대한 조직화가 이루어지는 단계, 상기 조직화가 이루어진 웨이퍼의 표면에 대하여 습식 식각을 수행하는 단계, 상기 웨이퍼에 pn 접합을 형성하는 단계, 상기 조직화가 이루어진 상기 웨이퍼의 표면 상에 제1 전극을 형성하는 단계, 상기 조직화가 이루어진 상기 표면의 반대면에 제2 전극을 형성하는 단계를 포함하며, 상기 습식 식각에 사용되는 에칭액은 0.5 wt% 이상 10 wt% 이하의 HF, 30 wt% 이상 60 wt% 이하의 HNO_3, 및 0 wt% 보다 크고 30 wt% 이하인 Acetic acid을 포함한다.

대 표 도 - 도4

조건	Jsc (mA/cm2)	Voc (V)	FF (%)	EF (%)
습식 식각	34.34	0.629	79.35	17.13
표면 조직화	31.26	0.608	78.31	14.89
표면 조직화 + 습식 식각	35.02	0.628	79.61	17.50

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특허청구의 범위

청구항 1

표면에 랜덤하게 볼록부와 오목부가 위치하는 웨이퍼;

상기 웨이퍼의 표면 상에 위치하는 반사 방지막;

상기 웨이퍼의 제1 타입의 반도체와 접촉하는 제1 전극; 및

상기 웨이퍼의 제2 타입의 반도체와 접촉하는 제2 전극

을 포함하는 태양 전지.

청구항 2

제1항에 있어서,

상기 웨이퍼 상에 위치하는 제1 반사 방지막과, 상기 제1 반사 방지막 상에 위치하는 제2 반사 방지막을 포함하며,

상기 제1 반사 방지막의 굴절률은 상기 제2 반사 방지막의 굴절률보다 큰 것을 특징으로 하는 태양 전지.

청구항 3

제1항에 있어서,

상기 볼록부 또는 상기 오목부의 측면이 이루는 각도는 54.76° 보다 큰 것을 특징으로 하는 태양 전지.

청구항 4

절단된 웨이퍼의 하나의 표면에 랜덤하게 볼록부와 오목부를 형성하는 단계;

상기 웨이퍼에 불순물을 도핑하는 단계;

상기 웨이퍼의 제1 타입 반도체와 접촉하는 제1 전극을 형성하는 단계; 및

상기 웨이퍼의 제2 타입 반도체와 접촉하는 제2 전극을 형성하는 단계

를 포함하는 태양 전지의 제조 방법.

청구항 5

제4항에 있어서,

상기 볼록부와 상기 오목부가 형성된 후 상기 웨이퍼의 표면에 대하여 습식 식각을 수행하는 단계를 더 포함하는 것을 특징으로 하는 태양 전지의 제조 방법.

청구항 6

제5항에 있어서,

상기 습식 식각에 사용되는 예칭액은 0.5 wt% 이상 10 wt% 이하의 HF, 30 wt% 이상 60 wt% 이하의 HNO_3, 및 0 wt% 보다 크고 30 wt% 이하인 Acetic acid을 포함하는 것을 특징으로 하는 태양 전지의 제조 방법.

청구항 7

제4항에 있어서,

상기 볼록부와 상기 오목부는 플라즈마에 의하여 형성되는 것을 특징으로 하는 태양 전지의 제조 방법.

청구항 8

제5항에 있어서,

상기 습식 식각이 이루어진 후 상기 볼록부와 상기 오목부가 위치하는 웨이퍼의 표면 상에 복수의 반사 방지막

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이 형성되는 것을 특징으로 하는 태양 전지의 제조 방법.

청구항 9

제8항에 있어서,

상기 복수의 반사 방지막은 상기 표면 상에 형성되는 제1 반사 방지막과 상기 제1 반사 방지막 상에 형성되는 제2 반사 방지막을 포함하며,

상기 제1 반사 방지막의 굴절률은 상기 제2 반사 방지막의 굴절률보다 큰 것을 특징으로 하는 태양 전지의 제조 방법.

청구항 10

제4항에 있어서,

상기 볼록부와 상기 오목부가 형성되기 전에 상기 절단된 웨이퍼에 대한 습식 식각이 이루어지는 것을 특징으로 하는 태양 전지의 제조 방법.

명 세 서

발명의 상세한 설명

기 술 분 야

[0001] 본 발명은 태양 전지의 제조 방법에 관한 것이다.

배 경 기 술

[0002] 태양 전지는 광기전력 효과를 통하여 입사된 빛을 전기로 변환한다. 이에 따라 태양 전지의 변화 효율을 높이기 위해서는 광기전력 효과를 일으키는 빛의 양을 늘려야 하므로 입사된 빛 중 반사되는 빛의 양을 줄이고 태양 전지에 투과되는 빛의 양을 늘려야 한다.

[0003] 이와 같이 태양 전지의 변환 효율을 높이기 위하여 태양 전지의 제조 공정 중에 웨이퍼의 표면에 대한 조직화(texturing)가 이루어진다. 웨이퍼의 표면에 대한 조직화는 웨이퍼의 표면을 거칠게 함으로써 입사된 빛이 반사되는 것을 줄이고 빛의 산란면을 증가시켜 태양 전지의 변환 효율을 증가시킨다.

[0004] 그러나 웨이퍼의 표면에 대한 조직화 과정 중에 웨이퍼에 표면 손상(surface damage)이 일어날 수 있다. 이와 같은 웨이퍼의 표면 손상은 결함(defect)로 작용할 수 있으므로 캐리어가 많이 발생하더라도 웨이퍼의 결함에서 재결합되어 태양 전지의 전류가 감소하는 문제점이 있다.

발명의 내용

해결 하고자하는 과제

[0005] 본 발명은 태양 전지의 조직화 과정에서 발생하는 웨이퍼의 결함을 줄일 수 있는 태양 전지의 제조 방법을 제공하기 위한 것이다.

[0006] 본 발명이 이루고자 하는 기술적 과제들은 이상에서 언급한 기술적 과제들로 제한되지 않으며, 언급되지 않은 또 다른 기술적 과제들은 아래의 기재로부터 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자에게 명확하게 이해될 수 있을 것이다.

과제 해결수단

[0007] 본 발명의 태양 전지 제조 방법은 절단된 웨이퍼의 하나의 표면에 대한 조직화가 이루어지는 단계, 상기 조직화가 이루어진 웨이퍼의 표면에 대하여 습식 식각을 수행하는 단계, 상기 웨이퍼에 pn 접합을 형성하는 단계, 상기 조직화가 이루어진 상기 웨이퍼의 표면 상에 제1 전극을 형성하는 단계, 상기 조직화가 이루어진 상기 표면의 반대면에 제2 전극을 형성하는 단계를 포함하며, 상기 습식 식각에 사용되는 에칭액은 0.5 wt% 이상 10 wt% 이하의 HF, 30 wt% 이상 60 wt% 이하의 HNO_3, 및 0 wt% 보다 크고 30 wt% 이하인 Acetic acid을 포함한다.

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효 과

[0008] 본 발명의 태양 전지의 제조 방법은 웨이퍼 표면의 조직화 후 웨이퍼 표면에 대한 에칭으로 웨이퍼 표면의 결함을 없앰으로써 태양 전지의 변환 효율을 높인다.

발명의 실시를 위한 구체적인 내용

[0009] 기타 실시예들의 구체적인 사항들은 상세한 설명 및 도면들에 포함되어 있다. 본 발명의 이점 및 특징, 그리고 그것들을 달성하는 방법은 첨부되는 도면과 함께 상세하게 후술되어 있는 실시예들을 참조하면 명확해질 것이다.

[0010] 도 1a 내지 도 1i는 본 발명의 실시예에 따른 태양 전지의 제조 방법을 나타낸 것이다.

[0011] 실리콘 잉곳(silicon igot)(100)으로부터 얇은 웨이퍼를 형성하기 위한 절단 공정(sawing)이 이루어진다. 본 발명의 실시예에서는, 도 1a에 도시된 바와 같이, 와이어(wire)에 의한 절단 공정이 도시된다. 와이어에 의한 절단 공정은 와이어로부터 공급된 장력에 의하여 연마재가 실리콘 잉곳에 미세 균열을 만들어 실리콘 잉곳(silicon igot)을 마멸시킴으로써 웨이퍼를 형성한다. 연마제는 연마재 매니폴드(110)에 의하여 와이어(wire)에 공급되며 GC(Green Carborundum)가 사용될 수 있다.

[0012] 본 발명의 실시예에서는 절단 공정이 이루어질 수도 있고 이미 절단된 웨이퍼를 통하여 이후의 공정이 이루어질 수도 있다.

[0013] 절단 공정이 완료되면 습식 식각을 통하여 절단 공정에서 나타날 수 있는 웨이퍼의 표면 손상이 제거된다. 이 때 절단이 완료된 웨이퍼(140)는 직경 125mm인 단결정 실리콘일 수 있다.

[0014] 도 1b에 도시된 바와 같이, 입사된 태양빛의 반사율을 낮추기 위하여 웨이퍼 표면에 대하여 마스크 없이 플라즈마를 이용하여 조직화가 이루어진다. 즉, 외부 전원(120)에 의하여 챔버(130)의 양쪽에 위치하는 전극들(E1, E2)에 가스의 이온화를 위한 문턱 전압 이상의 전압이 공급되면, 전압에 의해 발생된 전계에 의하여 챔버(130) 내의 라디칼(radical)이나 이온들이 가속되어 웨이퍼(140)의 표면과 충돌함으로써 웨이퍼(140)의 표면에 볼록부(141a)와 오목부(141b)가 형성되어 웨이퍼(140)에 대한 조직화가 이루어진다.

[0015] 오목부(141b) 및 볼록부(141a)의 측면과 웨이퍼(140)의 밑면(140B)이 이루는 각도(Θ)는 54.76° 보다 클 수 있다. 54.76° 는 본 발명에서와 같이 플라즈마에 의한 조직화가 아니라 이방성 습식 식각을 통하여 형성된 오목부(141b) 및 볼록부(141a)의 측면과 웨이퍼(140)의 밑면(140B)이 이루는 각도이다. 플라즈마에 의한 조직화는 전계에 의하여 가속된 라디칼이나 이온의 충돌에 의하여 이루어지므로 이방성 습식 식각에 의하여 형성되는 각도보다 크다.

[0016] 이와 같은 플라즈마에 의한 조직화는 마스크 없이 이루어지므로 웨이퍼(140)의 표면에 형성된 볼록부(141a)와 오목부(141b)의 위치나 높이 또는 깊이는 랜덤(randum)하게 형성된다. 마스크없이 조직화가 이루어지면 태양 전지의 제조 공정이 감소하므로 제조 시간 및 제조 비용을 줄일 수 있다.

[0017] 웨이퍼(140) 표면에 대한 조직화 공정이 완료되면, 도 1c에 도시된 바와 같이, 웨이퍼(140) 표면에 흠(141)이 생기며, 흠(141)에 의하여 산란면이 증가하여 빛의 반사가 줄어든다. 한편, 웨이퍼(140)의 조직화에 의하여 웨이퍼(140) 표면에 손상이 발생한다. 도 2는 플라즈마에 의한 표면 조직화 후의 웨이퍼 표면에 대한 전자 현미경 사진이다.

[0018] 도 1d에 도시된 바와 같이, 웨이퍼(140)의 표면 손상을 제거하기 위하여 에칭 속도(etching rate)가 상당히 느린 산성 에칭액(150)에 표면 조직화가 이루어진 웨이퍼(140)가 노출된다. 이 때 산성 에칭액(150)은 웨이퍼(140)의 표면 손상만을 제거해야 하므로 에칭되는 양의 조절을 쉽게 하기 위하여 에칭 속도가 상당히 느려야 한다. 하지만, 에칭 속도가 너무 느릴 경우, 표면에 스테인(stain)이 발생할 수 있으므로 너무 느려서도 안된다. 스테인은 산성 에칭액으로 에칭할 때 발생하는 비정질 실리콘의 얇은 막이다. 이와 같은 에칭 속도의 조절을 위하여 산성 에칭액은 0.5 wt% 이상 10 wt% 이하의 HF, 30 wt% 이상 60 wt% 이하의 HNO_3, 및 0 wt% 보다 크고 30 wt% 이하인 Acetic acid을 포함한다.

[0019] HF가 0.5 wt% 보다 작을 때에는 에칭 속도가 너무 느리게 되고, 10 wt%보다 클 때에는 에칭 속도가 너무 빨라 웨이퍼의 표면 손상 이외에 표면 조직화의 흠들이 사라질 수 있다. HNO_3가 30 wt%보다 작으면 식각 균일성(etching uniformity)이 나빠질 수 있고, 60 wt% 보다 크면 에칭 속도가 너무 빨라진다. Acetic acid가 30 wt%

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보다 크면 에칭 속도가 너무 빨라진다.

[0020] 도 3에서 굵은 실선은 웨이퍼 표면의 조직화 없이 절단 공정 후에 습식 식각만을 했을 경우 빛의 파장에 대한 반사율을, 점선은 웨이퍼 표면의 조직화만을 했을 경우 빛의 파장에 대한 반사율을, 그리고 가는 실선은 웨이퍼 표면의 조직화와 함께 앞서 설명된 산성 에칭액을 통하여 습식 식각이 이루어진 경우 빛의 파장에 대한 반사율을 나타낸 것이다.

[0021] 특히, 산성 에칭액은 0.5 wt% 이상 10 wt% 이하의 HF, 30 wt% 이상 60 wt% 이하의 HNO_3, 및 0 wt% 보다 크고 30 wt% 이하인 Acetic acid을 포함할 수 있다.

[0022] 도 3의 그래프에서 상단에 표시된 퍼센트 값은 평균 가중 반사율(AWR : Average Weighted Reflectance)을 나타낸 것이다. 또한 반사율 측정은 Solid spec 3700이라는 반사율 측정 장치가 이용되었다.

[0023] 도 3에 도시된 바와 같이, 조직화 후에 산성 에칭액으로 표면 손상이제거되더라도 AWR 값은 15.58%로 조직화 없이 습식 식각이 진행된 것보다 약 8%(= 23.56 % - 15.58 %)의 AWR 이득이 획득된다.

[0024] 조직화 후에 산성 에칭액에 의한 습식 식각이 이루어지면 표면적이 넓어져서 표면 패시베이션(passivation) 문제가 발생할 수 있으므로 본 발명의 실시예에서는 도 1f에 도시된 바와 같이 복수의 반사 방지막(160, 170)이 형성되어 표면 패시베이션 효과가 극대화되었다.

[0025] 도 4는 본 발명의 실시예에 따른 태양 전지의 제조 방법에 따른 변환 효율을 나타낸 것이다. 도 4의 표에서 Jsc는 태양 전지의 단락 전류, Voc는 태양 전지의 개방 전류, FF는 필 팩터(Fill factor), EF는 변환 효율을 나타낸다. 본 발명의 실시예에서와 같이 표면 조직화 후 앞서 설명된 산성 에칭액을 통한 습식 식각이 이루어질 경우에서의 변환 효율이 태양 전지의 변화 효율이 절단 공정 후 표면 조직화 없이 습식 식각만이 이루어진 경우에서의 변환 효율이나, 표면 조직화 후 습식 식각이 없는 경우에서의 변환 효율에 비하여 큼을 알 수 있다.

[0026] 즉, 본 발명의 실시예에서와 같이 표면 조직화 후 앞서 설명된 산성 에칭액을 통한 습식 식각이 이루어질 경우 표면 조직화 과정에서 발생된 표면 손상이 제거됨으로써 캐리어의 재결합이 줄어들어 태양 전지의 변환 효율이 증가한다.

[0027] 도 1e에 도시된 바와 같이, pn 접합을 형성하기 위한 불순물 도핑이 이루어진다. 불순물의 도핑을 위하여 고온에서 p형 불순물인 3족 또는 n형 불순물인 5족에 속하는 불순물을 포함한 기체 또는 고체에 웨이퍼(140) 표면을 노출시켜 불순물을 웨이퍼(140) 내부로 도핑시킨다. 이 때 불순물 소스로는 PH_3, $POCl_3$, BN 등이 사용될 수 있다. 또한 이온 주입에 의하여 3족과 5족에 속하는 불순물을 웨이퍼(140) 내부로 도핑시킬 수도 있다. 즉, 웨이퍼(140)을 진공 챔버 안에 두고 불순물 이온을 가속하여 웨이퍼(140) 표면에 불순물을 주입시킬 수도 있다.

[0028] 도 1f에 도시된 바와 같이, 입사된 태양광의 반사를 방지하기 위한 복수의 반사 방지막이 형성된다. 제1 반사 방지막(160)은 조직화가 이루어진 웨이퍼(140)의 한쪽 표면 상에 형성되며, 제2 반사 방지막(170)은 제1 반사 방지막(160) 상에 형성된다. 제2 반사 방지막(170)으로부터 반사된 빛과 제1 반사 방지막(160)에서 반사된 빛은 서로 상쇄 간섭을 일으킴으로써 태양광의 반사를 줄이고 특정 파장 영역에서의 선택성을 증가시킨다. 이를 위하여 제1 반사 방지막(160)의 굴절률이 제2 반사 방지막(170)의 굴절률보다 크다. 제1 반사 방지막(160) 및 제2 반사 방지막(170)은 진공증착법, 화학기상증착법, 스핀 코팅(spin coating), 스크린 인쇄 또는 스프레이 코팅(spray coating)에 의하여 형성될 수 있다.

[0029] 도 1g에 도시된 바와 같이, 웨이퍼(140)의 다른 쪽 표면 상에 복수의 반사층(L1, L2, L3)으로 이루어진 반사막(180)을 형성하기 위하여 화학 기상 증착(Chemical Vapor Deposition)와 같은 증착 공정이 이루어진다. 이 때, 반사막(180)은 이후에 형성될 제2 전극이 충진되는 콘택 홀(contact hole)(CH)이 형성된다. 반사막(180)으로서 웨이퍼(140) 상에 SiOx 층(L1), SiOxNy 층(L2) 및 SiOx:H 층(L3)이 차례로 형성될 수 있다.

[0030] 도 1h에 도시된 바와 같이, 스크린 마스크(SM) 상에 제1 전극 페이스트(190)를 스퀴즈(squeeze)(미도시)로 문질러 제1 전극의 패턴을 제2 반사 방지막(170) 상에 형성한다. 제1 전극 페이스트(190)는 Ag와 함께 글라스 프릿(glass frit)을 포함할 수 있다. 또한 스크린 프린팅을 통하여 제2 전극 페이스트(200)가 반사막(180)의 콘택 홀을 통하여 밀려들어간다. 제2 전극 페이스트(200)는 알루미늄을 포함할 수 있다.

[0031] 이후 전극 패턴을 지닌 제1 전극 페이스트(190), 제1 반사 방지막(160), 제2 반사 방지막(170), 반사막(180) 및 제2 전극 페이스트(200)에 대한 소성 공정이 이루어진다. 즉, 1회 공정으로 제1 전극 페이스트(190), 제1 반사 방지막(160), 제2 반사 방지막(170), 반사막(180) 및 제2 전극 페이스트(200)에 대한 소성이 이루어진다. 1회의

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소성을 위하여 열처리가 이루어지면 제1 전극 페이스트(190)에 포함된 저융점 글라스 프릿이 제1 반사 방지막(160) 및 제2 반사 방지막(170)을 뚫고 웨이퍼(140)과 접촉하게 된다. 이에 따라 열처리가 완료되면 도 1i에 도시된 바와 같이 제1 전극 페이스트(190)가 복수의 반사 방지막들(160, 170)을 뚫고 웨이퍼(140)의 한쪽 표면과 접촉한다.

[0032] 이와 같은 소성 공정이 완료되면, 제1 전극은 제1 타입의 반도체와 접촉하고 제2 전극은 제1 타입과 다른 제2 타입의 반도체와 접촉한다. 본 발명의 실시예에서 제1 전극은 n형 반도체와 접촉하고, 제2 전극은 p형 반도체와 접촉한다.

[0033] 이상 첨부된 도면을 참조하여 본 발명의 실시예를 설명하였지만, 본 발명이 속하는 기술분야의 당업자는 본 발명이 그 기술적 사상이나 필수적 특징을 변경하지 않고 다른 구체적인 형태로 실시될 수 있다는 것을 이해할 수 있을 것이다. 그러므로 이상에서 기술한 실시예들은 모든 면에서 예시적인 것이며 한정적인 것이 아닌 것으로서 이해되어야 하고, 본 발명의 범위는 상기 상세한 설명보다는 후술하는 특허청구범위에 의하여 나타내어지며, 특허청구범위의 의미 및 범위 그리고 그 등가개념으로부터 도출되는 모든 변경 또는 변형된 형태가 본 발명의 범위에 포함되는 것으로 해석되어야 한다.

도면의 간단한 설명

[0034] 도 1a 내지 도 1i는 본 발명의 실시예에 따른 태양 전지의 제조 방법을 나타낸 것이다.

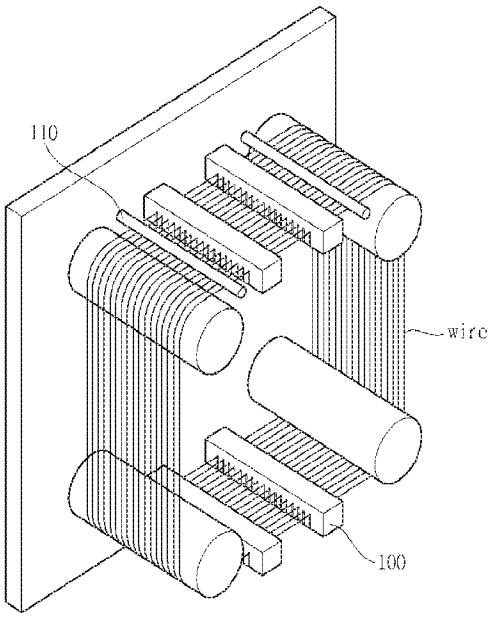
[0035] 도 2는 플라즈마에 의한 표면 조직화 후의 웨이퍼 표면에 대한 전자 현미경 사진이다.

[0036] 도 3은 산성 에칭액에 의한 반사율을 나타낸 그래프이다.

[0037] 도 4는 본 발명의 실시예에 따른 태양 전지의 제조 방법에 따른 변환 효율을 나타낸 것이다.

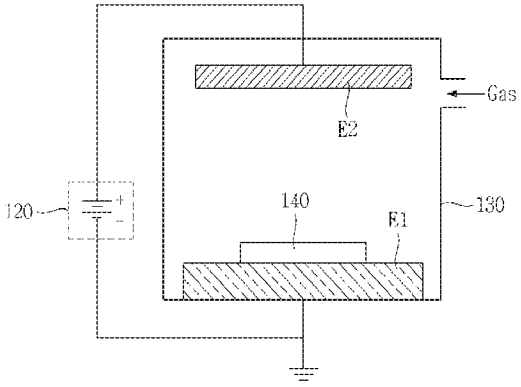
도면

도면1a

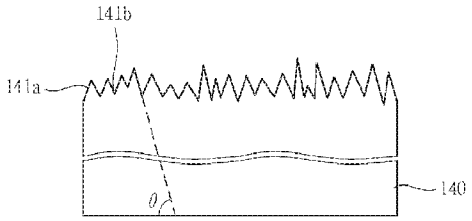


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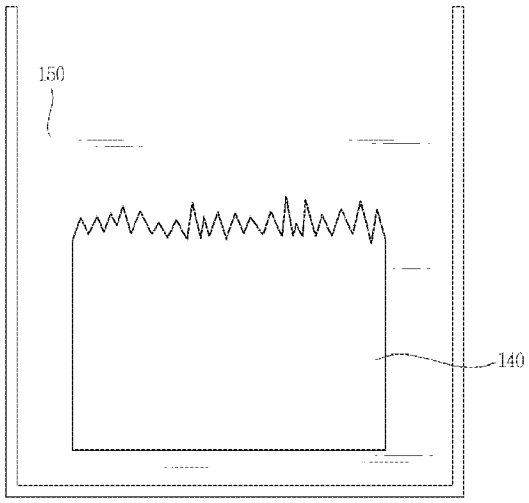
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도면1c

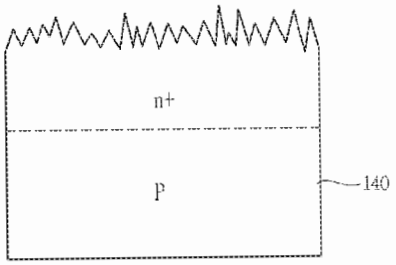


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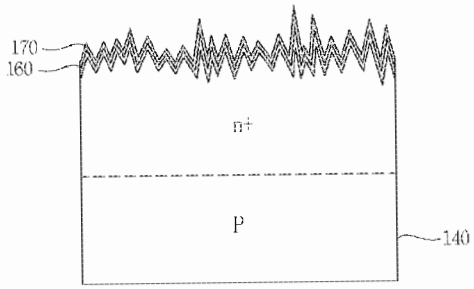


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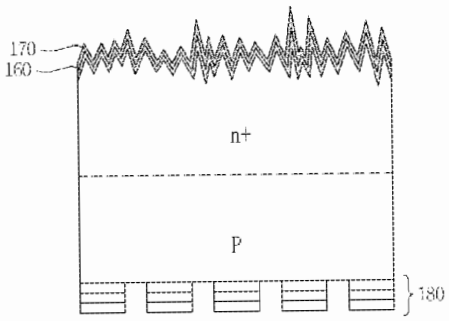
도면1e



도면1f

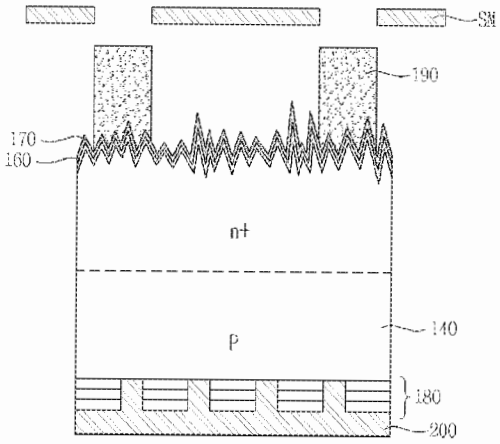


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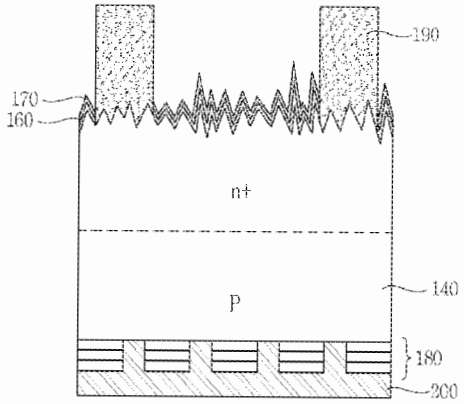


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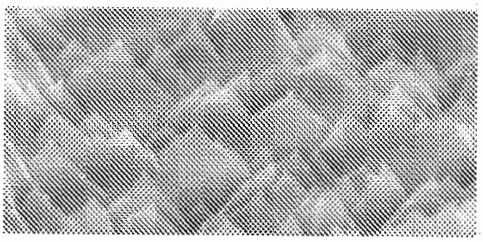
도면1b



도면1i

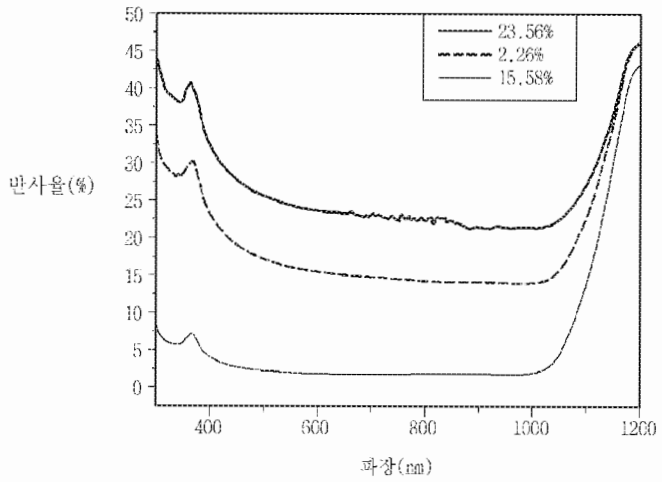


도면2



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도면3



도면4

조건	Jsc (mA/cm2)	Voc (V)	FF (%)	EF (%)
습식 식각	34.34	0.629	79.35	17.13
표면 조직화	31.26	0.608	78.31	14.89
표면 조직화 + 습식 식각	35.02	0.628	79.61	17.50

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Espacenet

Bibliographic data: KR20110079323 (A) — 2011-07-07

IMAGE SENSOR AND METHOD FOR MANUFACTURING THE SAME

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Classification: - **international:*H01L27/146***
- **cooperative:** **H01L27/14625**; **H01L27/1463**; **H01L27/14689**
more

Application number: KR20090136341 20091231 Global Dossier

Priority number(s): KR20090136341 20091231

Abstract of KR20110079323 (A)

PURPOSE: An image sensor and a manufacturing method thereof are provided to improve electric cross talk and an optical cross talk. CONSTITUTION: An image sensor includes the first element isolation film(120), a unit pixel, an interlayer insulating layer(150), a trench and the second element isolation film(170). The first element isolation film is formed in the front of a semiconductor substrate so that a pixel region is defined. The unit pixel includes a light sensing part and a readout circuit formed in a pixel region. The interlayer insulating layer includes a wiring formed on the front side of the semiconductor substrate. The trench is formed in a backside of the semiconductor substrate in correspondence to the element isolation film. The second element isolation film is formed in the trench.

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DESCRIPTION KR20110079323

[0001] IMAGE SENSOR AND METHOD FOR MANUFACTURING THE SAME [0002]

Embodiments relate to an image sensor and a method of manufacturing the same. An image sensor is a semiconductor device that converts an optical image into an electrical signal and is classified into a charge coupled device (CCD) image sensor and a CMOS image sensor (CIS) .

Generally, an image sensor forms a photodiode on a silicon substrate by ion implantation. As the size of the photodiode gradually decreases for the purpose of increasing the number of pixels without increasing the chip size, the image quality is reduced due to reduction of the area of the light receiving portion. In addition, since the stack height is not reduced as much as the area of the light receiving portion is reduced, the number of photons incident on the light receiving portion due to the diffraction phenomenon of light called an airy disk also tends to decrease. One of the alternatives to overcome this is to try to minimize the level difference of the light receiving part by receiving light through the wafer backside and to prevent the interference of light by metal routing Sensor) is performed. There is a problem in that the backside light receiving image sensor is not susceptible to optical crosstalk because there is no element isolation region on the back surface of the substrate.

Embodiments provide an image sensor capable of preventing crosstalk and a method of manufacturing the same. An image sensor according to an embodiment includes: a first isolation layer formed on a front surface side of a semiconductor substrate so that a

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pixel region is defined; A unit pixel including a light sensing part and a lead - out circuit formed in the pixel area; An interlayer insulating layer including a wiring formed on a front side of the semiconductor substrate; A trench formed on a back side of the semiconductor substrate opposite to a front surface of the semiconductor substrate and formed on a rear surface of the semiconductor substrate so as to correspond to the first element isolation film; And a second isolation layer formed in the trench. A method of manufacturing an image sensor according to an embodiment includes forming a first device isolation film on a front side of a semiconductor substrate so that a pixel region is defined; Forming a unit pixel including a light sensing part and a lead - out circuit in the pixel area; A step of forming an interlayer insulating layer including wiring on a front side of the semiconductor substrate; Forming a trench on the back side of the semiconductor substrate opposite to the front surface of the semiconductor substrate so as to correspond to the first device isolation film; And forming a second isolation film in the trench. The image sensor and the manufacturing method thereof according to the embodiment can simultaneously improve the electrical crosstalk and the optical crosstalk in the rear light receiving image sensor. That is, a first element isolation region may be formed on the front side of the semiconductor substrate, and a second element isolation region may be formed on the rear side of the semiconductor substrate. Particularly, since the electron generating region of the semiconductor substrate can be formed by the second element isolation region, the optical crosstalk can be fundamentally prevented. In addition, the second isolation regions are formed in a dual structure having different refractive indexes, and the light sensitivity of the unit pixel can be improved since the path of the incident light can be changed.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS Hereinafter, a rear light receiving image sensor according to an embodiment and a method of manufacturing the same will be described in detail with reference to the accompanying drawings. In the description of the embodiment, in the case of being described as being formed on & quot; on / under & quot; of each layer, it is to be understood that the top / bottom may be formed directly, All included. 7, 8 and 9 are sectional views of the image sensor according to the embodiment. An image sensor according to an embodiment includes: a first isolation layer 120 formed on a front side of a semiconductor substrate such that a pixel region is defined; A unit pixel including a light sensing unit 130 and a lead - out circuit 140 formed in the pixel region; An interlayer insulating layer 150 including wirings M1 and M2 formed on a front side of the semiconductor substrate 100; The semiconductor device according to the present invention includes a semiconductor substrate 100 and a semiconductor substrate 100. The semiconductor substrate 100 is formed on the back side of the semiconductor substrate 100 opposite to the front surface of the semiconductor substrate 100, (160); And a second isolation layer 170 formed on the trench 160. The color filter 200 or the microlens 210 may be disposed on

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the rear surface of the semiconductor substrate 100 corresponding to the unit pixel. The second isolation layer 170 may be formed of an insulating material or a metal material. The rear surface of the semiconductor substrate 100 can be separated by unit pixels by the second isolation layer 170. Thus, crosstalk can be prevented by adjusting the photocharge generating region in the semiconductor substrate 100. [8, the second isolation layer 170 includes a first insulation layer 180 formed on the surface of the trench 160 and a second insulation layer 180 formed on the first insulation layer 180 And a second insulating layer 190 formed on the second insulating layer 190. [For example, the first insulating layer 180 may have a first refractive index, and the second insulating layer 190 may have a second refractive index that is greater than the first refractive index.

For example, the refractive index of the first insulating layer 180 may be 1.0 to 1.46, and the refractive index of the second insulating layer 190 may be 1.68 to 3.0. Since the outer side and the inner side of the second isolation film 170 are formed to have different refractive indexes, light incident on a neighboring pixel with an inclination angle can be incident on the corresponding pixel by the second isolation film 170 have. Accordingly, it is possible to prevent the light sensing rate and the crosstalk of the light sensing unit corresponding to the unit pixel. Referring to FIG. 9, the second conductive type layer 300 may be formed on the rear surface of the semiconductor substrate 100. For example, a p + layer can be formed, but is not limited thereto. The second conductive type layer may neutralize the charge trap at the interface of the back side surface of the semiconductor substrate. At this time, the second isolation layer 170 may be formed on the second conductive type layer 300 and the rear surface of the semiconductor substrate 100. The second conductive type layer 300 and the second isolation layer 170 may be formed on the semiconductor substrate 100 to improve full well characteristics. The image sensor according to the embodiment can prevent electrical crosstalk by the first device isolation film formed on the front surface of the semiconductor substrate and effectively prevent optical crosstalk by the second device isolation film formed on the rear surface of the semiconductor substrate. Hereinafter, a method of manufacturing an image sensor according to an embodiment will be described with reference to FIGS. 1 to 9. FIG. First, as shown in FIG. 1, a first device isolation layer 120 is formed on a front side of a semiconductor substrate 100 to define a pixel region. The semiconductor substrate 100 may be a high concentration p - type substrate (p + +). The front side of the semiconductor substrate 100 may include a low concentration p - epi layer 110 by performing an epitaxial process. An ion implantation layer 105 may be formed on the entire surface of the semiconductor substrate 100.

That is, in the embodiment, the lower portion of the semiconductor substrate 100 can be

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easily removed by forming the ion - implanted layer 105 before the wiring process. The ion implantation layer 105 may be formed by implanting ions such as hydrogen (H) or helium (He), but is not limited thereto. The back surface of the semiconductor substrate 100 may be easily removed by using the ion implantation layer 105 instead of removing the back surface of the semiconductor substrate 100 by backgrinding, And can be stably removed. Thus, the production yield of the rear light receiving image sensor can be remarkably increased. The first isolation layer 120 may be formed on the front side of the epi layer 110 of the semiconductor substrate 100 by an STI process. Although not shown, an ion implantation region may be further formed to isolate the light sensing unit 130. This ion implantation region can be formed before or after the first isolation film 120 is formed. Next, a unit pixel including a light sensing part 130 and a lead - out circuit 140 is formed in a pixel region of the semiconductor substrate 100. The light sensing unit 130 may be a photodiode. The light sensing unit 130 may be formed on the semiconductor substrate 100 by a pn junction formed by an n - type ion implantation region and a p - type ion implantation region, but the present invention is not limited thereto. Surplus electrons and the like can be prevented by the p - type ion implantation region. In addition, embodiments can achieve a charge dumping effect by forming PNP junctions. A lead - out circuit 140 for signal processing is formed on the semiconductor substrate 100 on which the light sensing part 130 is formed. For example, the lead - out circuit 140 may include, but is not limited to, a transfer transistor, a reset transistor, a drive transistor, and a select transistor. Next, an interlayer insulating layer 150 and a wiring are formed on the front side of the semiconductor substrate 100. For example, the wiring may include a first metal M1 and a second metal M2.

On the other hand, a carrier wafer (not shown) can be bonded onto the interlayer insulating layer 150 including the wiring. The carrier wafer may be a means for handling the semiconductor substrate 100. Referring to FIG. 2, a part of the back side opposite to the front side of the semiconductor substrate 100 is removed. For example, the lower side of the ion implantation layer 105 of the semiconductor substrate 100 is removed. That is, the heat treatment is performed on the ion - implanted layer 105 to blob the hydrogen ions, and the hydrogen ions are cut with a blade or the like to remove the hydrogen ions, and the upper side of the semiconductor substrate 100 is left as a linar layer . Thereafter, the planarization process may be performed on the rear surface of the cut semiconductor substrate 100. Alternatively, the opposite side of the front side of the semiconductor substrate 100 may be removed by a back graining process. Accordingly, a p - layer (p ++) having a high concentration, which is the back side of the semiconductor substrate 100, can be exposed. Alternatively, the second conductive type layer (p +) 300 may be formed on the rear surface of the semiconductor substrate 100 as shown in FIG. The second conductive type layer 300 may neutralize the charge trap at the interface of the back surface of the semiconductor substrate 100. Next, a

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photoresist pattern 10 is formed on the rear surface of the semiconductor substrate 100. The photoresist pattern 10 may be patterned to correspond to the unit pixel. At this time, the opening 15 of the photoresist pattern 10 may selectively expose the rear surface of the semiconductor substrate 100 corresponding to the position of the first isolation layer 120. Referring to FIG. 3, a trench 160 is formed on the rear surface of the semiconductor substrate 100. The trench 160 may be formed on the backside of the semiconductor substrate 100 to correspond to the first isolation layer 120. The trench 160 may be formed through an etching process using the photoresist pattern as an etching mask.

The trench 160 may be formed by etching a p ++ region of a high concentration of the semiconductor substrate 100 and the p - type epitaxial layer 110 to a predetermined depth. Referring to FIG. 4, a second isolation layer 170 is formed in the trench 160. The rear surface of the semiconductor substrate 100 may be divided into unit pixels by the second isolation layer 170. The second isolation layer 170 may be formed by applying a metal or an insulating material to the trench 160. For example, the second isolation layer 170 may be formed of a metal such as tungsten, aluminum, or titanium. In particular, the second isolation layer 170 may be formed of a metal to prevent incident light from being incident on a photo - sensing portion of an adjacent pixel other than the corresponding pixel. For example, the second isolation layer 170 may be formed of the same oxide or nitride as the first trench 160. As shown in FIGS. 5 and 6, the second isolation layer 170 may have a different refractive index n in the trench 160. Referring to FIG. 5, a first insulating layer 180 is formed along the surface of the trench 160. The first insulating layer 180 may be formed of a material having a first refractive index. For example, the first refractive index may be 1.0 to 1.46. Referring to FIG. 6, a second insulating layer 190 is formed on the first insulating layer 180 so that the trench 160 is formed. The second insulating layer 190 may be formed of a material having a second refractive index greater than the first refractive index. For example, the second refractive index may be 1.68 to 3.0. For example, the first insulating layer 180 may be SiO 2 (n = 1.46) and the second insulating layer 190 may be SiN (n = 2.05), but the present invention is not limited thereto. The second isolation layer 170 may be formed by filling the outer surface of the trench 160 with a material having a small index of refraction and filling the inner portion of the trench with a material having a large index of refraction.

Since the second isolation layer 170 has a double layer structure having different refractive indexes, the incident light having a tilt angle is refracted by the second isolation layer 170 to the corresponding pixel, . That is, the second isolation film may be one in which the total reflection principle is applied. Accordingly, the incident light can be refracted by the second isolation layer 170 to the light sensing unit 130 of the

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corresponding pixel, and the light receiving rate of the unit pixel can be improved. Referring to FIG. 7, a color filter 200 is formed on the rear surface of the semiconductor substrate 100. The color filter 200 is formed for each unit pixel using a dyed photoresist, and can separate colors from incident light. For example, the color filter 200 may be a red, a green, and a blue color filter. Thereafter, a microlens 210 is formed on the color filter 200. The microlens 210 is formed in the shape of a convex lens, and can condense light into the photo - sensing unit of the corresponding unit pixel. A first isolation layer 120 is formed on a front side of the semiconductor substrate 100 and a second isolation layer 170 is formed on a back side of the semiconductor substrate 100, Crosstalk of the light incident on the rear surface of the substrate 100 can be prevented. Particularly, in the rear light receiving image sensor, since the incidence of light is made through the rear surface of the substrate and the red, green, and blue regions are formed from the substrate surface, the crosstalk against the blue signal located at the bottom of the light sensing portion is prevented Can be. Accordingly, the photosensitivity of the image sensor can be uniform. 8 is a cross - sectional view showing a color filter 200 and a microlens 210 formed on the rear surface of the semiconductor substrate 100 including the second isolation layer 170 having a double sidewall structure. 9 is a cross - sectional view illustrating a second device isolation layer 170 having a double sidewall structure selectively formed on the second conductive type layer 300 and the semiconductor substrate 100.

The light passing through the microlens 210 and the color filter 200 may be incident on the corresponding light sensing unit. At this time, light incident at an inclination angle is refracted by the second isolation layer 170 and may be incident on the light sensing unit 130 of the corresponding pixel. Thus, the light sensitivity of the image sensor can be improved. The present invention is not limited to the described embodiments and drawings, and various other embodiments are possible within the scope of the claims.

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CLAIMS KR20110079323

1.
A first device isolation layer formed on a front surface side of the semiconductor substrate so as to define a pixel region; A unit pixel including a light sensing part and a lead - out circuit formed in the pixel area; An interlayer insulating layer including a wiring formed on a front side of the semiconductor substrate; A trench formed on a back side of the semiconductor substrate opposite to a front surface of the semiconductor substrate and formed on a rear surface of the semiconductor substrate so as to correspond to the first element isolation film; And a second isolation layer formed in the trench.

2.
The image sensor according to claim 1, wherein the second isolation film is formed of an insulating material or a metal material.

3.
The semiconductor device according to claim 1, wherein the second isolation layer comprises: a first insulation layer formed on a surface of the trench and having a first refractive index; And a second insulating layer formed on the first layer so that the trench is taped, and having a second refractive index larger than the first refractive index.

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4.
The image sensor of claim 1, further comprising a second conductive type layer formed on a rear surface of the semiconductor substrate, wherein the second conductive type layer and the second conductive type layer are formed on a rear surface of the semiconductor substrate.

5.
The image sensor according to claim 1, comprising a color filter or a microlens formed on the rear surface of the semiconductor substrate corresponding to the unit pixel.

6.
Forming a first device isolation film on a front side of a semiconductor substrate so that a pixel region is defined; Forming a unit pixel including a light sensing part and a lead - out circuit in the pixel area; A step of forming an interlayer insulating layer including wiring on a front side of the semiconductor substrate; Forming a trench on the back side of the semiconductor substrate opposite to the front surface of the semiconductor substrate so as to correspond to the first device isolation film; And forming a second isolation film in the trench.

7.
7. The method of claim 6, wherein the second isolation layer is formed by applying an insulating material to the trench.

8.
7. The method of claim 6, wherein the second isolation layer is formed by applying a metal material to the trench.

9.
The method according to claim 6, wherein the forming of the second isolation layer comprises: forming a first insulation layer having a first refractive index on a surface of the trench; And forming a second insulating layer having a second refractive index larger than the first refractive index on the first insulating layer so that the trench is formed on the first insulating layer.

10.

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The method of claim 6, further comprising forming a second conductive type layer on a rear surface of the semiconductor substrate, and then forming the second element isolation film.

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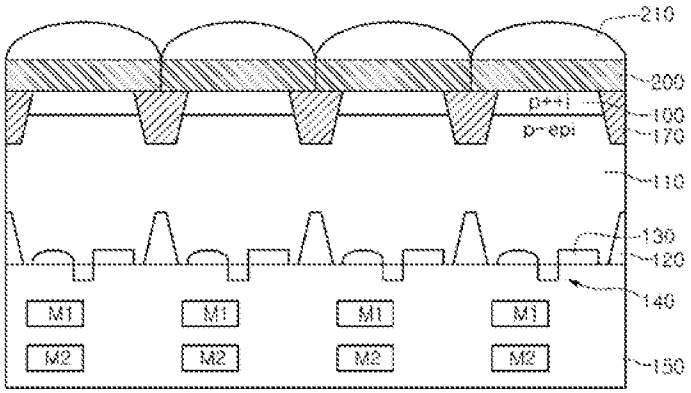
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(54) 이미지 센서 및 그 제조방법

(57) 요 약

실시예에 따른 이미지 센서는, 픽셀영역이 정의되도록 반도체 기판의 전면측에 형성된 제1 소자분리막; 상기 픽셀영역에 형성된 광감지부 및 리드아웃 서킷을 포함하는 단위픽셀; 상기 반도체 기판의 전면(front side) 상에 형성된 배선을 포함하는 층간절연층; 상기 반도체 기판의 전면과 반대되는 상기 반도체 기판의 후면(back side)에 형성되고, 상기 제1 소자분리막과 대응되도록 상기 반도체 기판의 후면에 형성된 트렌치; 및 상기 트렌치에 형성된 제2 소자분리막을 포함한다.

대 표 도 - 도7



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후의청구의 범위

청구항 1

픽셀영역이 정의되도록 반도체 기판의 전면측에 형성된 제1 소자분리막;

상기 픽셀영역에 형성된 광감지부 및 리드아웃 서킷을 포함하는 단위픽셀;

상기 반도체 기판의 전면(front side) 상에 배선을 포함하는 층간절연층;

상기 반도체 기판의 전면과 반대되는 상기 반도체 기판의 후면(back side)에 형성되고, 상기 제1 소자분리막과 대응되도록 상기 반도체 기판의 후면에 형성된 트렌치; 및

상기 트렌치에 형성된 제2 소자분리막을 포함하는 이미지 센서.

청구항 2

제1항에 있어서,

상기 제2 소자분리막은 절연물질 또는 금속 물질로 형성된 이미지 센서.

청구항 3

제1항에 있어서,

상기 제2 소자분리막은,

상기 트렌치의 표면에 형성되고 제1 굴절률을 가지는 제1 절연층; 및

상기 트렌치가 갭필되도록 상기 제1 층 상에 형성되고, 제1 굴절률보다 큰 제2 굴절률을 가지는 제2 절연층을 포함하는 이미지 센서.

청구항 4

제1항에 있어서,

상기 반도체 기판의 후면 상에 형성된 제2 도전형 층을 더 포함하고,

상기 제2 소자분리막은 상기 제2 도전형 층 및 상기 반도체 기판의 후면에 형성된 것을 포함하는 이미지 센서.

청구항 5

제1항에 있어서,

상기 단위픽셀에 대응하는 상기 반도체 기판의 후면 상에 형성된 컬러필터 또는 마이크로 렌즈를 포함하는 이미지 센서.

청구항 6

픽셀영역이 정의되도록 반도체 기판의 전면측에 제1 소자분리막을 형성하는 단계;

상기 픽셀영역에 광감지부 및 리드아웃 서킷을 포함하는 단위픽셀을 형성하는 단계;

상기 반도체 기판의 전면(front side) 상에 배선을 포함하는 층간절연층을 형성하는 단계;

상기 반도체 기판의 전면과 반대되는 상기 반도체 기판의 후면(back side)에 상기 제1 소자분리막과 대응되도록 트렌치을 형성하는 단계; 및

상기 트렌치에 제2 소자분리막을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 7

제6항에 있어서,

상기 제2 소자분리막은 상기 트렌치에 절연물질을 갭필하여 형성되는 이미지 센서의 제조방법.

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청구항 8

제6항에 있어서,

상기 제2 소자분리막은 상기 트렌치의 유전물질을 갭필하여 형성되는 이미지 센서의 제조방법.

청구항 9

제6항에 있어서,

상기 제2 소자분리막을 형성하는 단계는,

상기 트렌치의 표면에 제1 유전물을 가지는 제1 절연층을 형성하는 단계; 및

상기 트렌치가 갭필되도록 상기 제1 절연층 상에 제1 유전물보다 큰 제2 유전물을 가지는 제2 절연층을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 10

제6항에 있어서,

상기 반도체 기판의 후면 상에 제2 도전형 층을 형성한 다음, 상기 제2 소자분리막을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

명 세 서

발명의 상세한 설명

기 술 분 야

[0001] 실시예는 이미지 센서 및 그 제조방법에 관한 것이다.

[0002] 이미지센서(Image sensor)는 광학적 영상(optical image)을 전기적 신호로 변환시키는 반도체소자로서, 전하결합소자(Charge Coupled Device: CCD) 이미지센서와 씨모스 이미지센서(CMOS Image Sensor: CIS)로 구분된다.

배 경 기 술

[0003] 일반적으로 이미지 센서는 실리콘 기판에 포토다이오드(Photodiode)를 이온주입 방식으로 형성시킨다. 칩 사이즈(Chip size) 증가 없이 픽셀(Pixel) 수 증가를 위한 목적으로 포토다이오드의 사이즈가 점점 감소함에 따라 수광부 면적 축소로 이미지 특성(Image Zuality)이 감소하는 경향을 보이고 있다.

[0004] 또한, 수광부 면적 축소만큼의 적층높이(Stack height)의 감소가 이루어지지 못하여 에어리 디스크(Airy disk)라 불리는 빛의 회절 현상으로 수광부에 입사되는 포톤(photon)의 수 역시 감소하는 경향을 보이고 있다.

[0005] 이를 극복하기 위한 대안 중 하나로 웨이퍼 백사이드(Wafer Back Side)를 통해 빛을 받아들여 수광부의 단자를 최소화하고, 메탈 라우팅(Metal routing)에 의한 빛의 간섭을 현상을 방지할 수 있는 시도(후면수광 이미지 센서)가 이루어지고 있다.

[0006] 이러한 후면수광 이미지 센서에서 기판(substrate)의 후면 상에 소자분리 영역이 존재하지 않아 광학적 크로스 토크(Cross talk)에 매우 취약한 문제가 있다.

발명의 내용

해결 하고자하는 과제

[0007] 실시예는 크로스 토크를 방지할 수 있는 이미지센서 및 그 제조방법을 제공한다.

과제 해결수단

[0008] 실시예에 따른 이미지 센서는, 픽셀영역이 정의되도록 반도체 기판의 전면측에 형성된 제1 소자분리막; 상기 픽셀영역에 형성된 광감지부 및 리드아웃 회로를 포함하는 단위픽셀; 상기 반도체 기판의 전면(front side) 상에 형성된 배선을 포함하는 층간절연층; 상기 반도체 기판의 전면과 반대되는 상기 반도체 기판의 후면(back sid

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e)에 형성되고, 상기 제1 소자분리막과 대응되도록 상기 반도체 기판의 후면에 형성된 트렌치; 및 상기 트렌치에 형성된 제2 소자분리막을 포함한다.

[0009] 실시예에 따른 이미지 센서의 제조방법은, 픽셀영역이 정의되도록 반도체 기판의 전면측에 제1 소자분리막을 형성하는 단계; 상기 픽셀영역에 광감지부 및 리드아웃 서킷을 포함하는 단위픽셀을 형성하는 단계; 상기 반도체 기판의 전면(front side) 상에 배선을 포함하는 층간절연층을 형성하는 단계; 상기 반도체 기판의 전면과 반대되는 상기 반도체 기판의 후면(back side)에 상기 제1 소자분리막과 대응되도록 트렌치를 형성하는 단계; 및 상기 트렌치에 제2 소자분리막을 형성하는 단계를 포함한다.

효 과

[0010] 실시예에 따른 이미지 센서 및 그 제조방법은, 후면수광 이미지 센서에서 전기적 크로스 토크 및 광학적 크로스 토크를 동시에 개선할 수 있다.

[0011] 즉, 반도체 기판의 전면측에 제1 소자분리 영역을 형성하고, 상기 반도체 기판의 후면측에 제2 소자분리 영역을 형성할 수 있다.

[0012] 특히, 상기 제2 소자분리 영역에 의하여 반도체 기판의 전자 생성 영역을 설정할 수 있으므로, 근본적으로 광학적 크로스 토크를 방지할 수 있다.

[0013] 또한, 상기 제2 소자분리 영역은 서로 다른 굴절률을 가지는 이중구조로 형성되고, 입사광의 경로를 바꿀수 있으므로 단위픽셀의 광 감도를 향상시킬 수 있다.

발명의 실시를 위한 구체적인 내용

[0014] 이하, 실시예에 따른 후면수광 이미지센서 및 그 제조방법을 첨부된 도면을 참조하여 상세히 설명한다.

[0015] 실시예의 설명에 있어서, 각 층의 "상/아래(on/under)"에 형성되는 것으로 기재되는 경우에 있어, 상/아래는 직접(directly)과 또는 다른 층을 개재하여(indirectly) 형성되는 것을 모두 포함한다.

[0016] 도 7, 도 8 및 도 9는 실시예에 따른 이미지 센서의 단면도이다.

[0017] 실시예에 따른 이미지 센서는, 픽셀영역이 정의되도록 반도체 기판의 전면측에 형성된 제1 소자분리막(120); 상기 픽셀영역에 형성된 광감지부(130) 및 리드아웃 서킷(140)을 포함하는 단위픽셀; 상기 반도체 기판(100)의 전면(front side) 상에 형성된 배선(81,82)을 포함하는 층간 절연층(150); 상기 반도체 기판(100)의 전면과 반대되는 상기 반도체 기판(100)의 후면(back side)측에 형성되고, 상기 제1 소자분리막(120)과 대응되도록 상기 반도체 기판(100)의 후면에 형성된 트렌치(160); 및 상기 트렌치(160)에 형성된 제2 소자분리막(170)을 포함한다.

[0018] 상기 단위픽셀에 대응하는 상기 반도체 기판(100)의 후면 상에 컬러필터(200) 또는 마이크로 렌즈(210)가 배치될 수 있다.

[0019] 상기 제2 소자분리막(170)은 절연물질 또는 금속 물질로 형성될 수 있다.

[0020] 상기 제2 소자분리막(170)에 의하여 반도체 기판(100)의 후면을 단위픽셀 별로 분리할 수 있다. 이에 따라, 상기 반도체 기판(100) 내의 광 전하 생성영역을 조절함으로써 크로스 토크를 방지할 수 있다.

[0021] 도 8을 참조하여, 상기 제2 소자분리막(170)은, 상기 트렌치(160)의 표면에 형성된 제1 절연층(180) 및 상기 트렌치(160)가 갭필되도록 상기 제1 절연층(180) 상에 형성된 제2 절연층(190)을 포함한다. 예를 들어, 상기 제1 절연층(180)은 제1 굴절률을 가지고, 상기 제2 절연층(190)은 제1 굴절률보다 큰 제2 굴절률을 가질 수 있다.

[0022] 예를 들어, 상기 제1 절연층(180)의 굴절률은 1.0~1.46일 수 있고, 제2 절연층(190)의 굴절률은 1.68~3.0일 수 있다.

[0023] 상기 제2 소자분리막(170)의 외측 및 내측이 서로 다른 굴절률을 가지도록 형성됨으로써, 경사각을 가지고 이웃하는 픽셀로 입사하는 광이 상기 제2 소자분리막(170)에 의하여 해당하는 픽셀로 입사될 수 있다. 이에 따라, 단위픽셀에 해당하는 광감지부의 광감지율 및 크로스 토크를 방지할 수 있다.

[0024] 도 9를 참조하여, 상기 반도체 기판(100)의 후면 상에 제2 도전형 층(300)이 형성될 수 있다.

[0025] 예를 들어, p+층을 형성할 수 있으나, 이에 한정되는 것은 아니다. 상기 제2 도전형 층은 상기 반도체 기판의 후면(back side) 표면의 인터페이스(interface)에서 전하 트랩(trap)을 중성화시킬 수 있다.

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[0026] 이때, 상기 제2 소자분리막(170)은 상기 제2 도전형 층(300) 및 상기 반도체 기판(100)의 후면에 형성될 수 있다.

[0027] 상기 제2 도전형 층(300) 및 상기 반도체 기판(100)에 제2 소자분리막(170)이 형성되어, 풀웰특성(Full well) 특성을 향상시킬 수 있다.

[0028] 실시예에 따른 이미지 센서는, 반도체 기판의 전면에 형성된 제1 소자분리막에 의하여 전기적 크로스 토크를 방지하고, 상기 반도체 기판의 후면에 형성된 제2 소자분리막에 의하여 광학적 크로스 토크를 효과적으로 방지할 수 있다.

[0029] 이하, 도 1 내지 도 9를 참조하여 실시예에 따른 이미지 센서의 제조방법을 설명한다.

[0030] 우선, 도 1에 도시된 바와 같이 반도체 기판(100)의 전면(Front Side)에 제1 소자분리막(120)을 형성하여 픽셀 영역을 정의한다.

[0031] 상기 반도체 기판(100)은 고농도의 p형 기판(p++) 일 수 있다. 상기 반도체 기판(100)의 전면(Front Side)은 에피택셜(epitaxial) 공정을 실시하여 저농도의 p형 에피층(p-epi)(110)을 포함할 수 있다.

[0032] 상기 반도체 기판(100)의 전면에 이온주입층(105)를 형성할 수 있다. 즉, 실시예는 배선공정 전에 미리 이온주입층(105)을 형성함으로써 상기 반도체 기판(100)의 하부를 용이하게 제거할 수 있다. 이러한 이온주입층(105)은 수소(H) 또는 헬륨(He) 등의 이온을 주입하여 형성할 수 있으나, 이에 한정되지 않는다.

[0033] 상기 이온주입층(105)을 형성하는 경우, 백 그라인딩에 의해 상기 반도체 기판(100)의 후면을 제거하는 것이 아니라, 상기 이온주입층(105)을 이용하여 상기 반도체 기판(100)의 후면을 용이하고 안정적으로 제거할 수 있게 된다. 이에 따라, 후면수광 이미지 센서의 제조 수율을 현격히 상승시킬 수 있다.

[0034] 상기 제1 소자분리막(120)은 STI 공정에 의하여 상기 반도체 기판(100)의 에피층(110) 전면(front)측에 형성될 수 있다. 도시되지는 않았지만, 상기 광감지부(130)의 격리를 위해 이온주입영역을 더 형성할 수도 있다. 이러한 이온주입 영역은 제1 소자분리막(120)의 형성 전 또는 후에 형성할 수 있다.

[0035] 다음으로, 상기 반도체 기판(100)의 픽셀영역에 광감지부(130) 및 리드아웃 서킷(140)을 포함하는 단위픽셀을 형성한다.

[0036] 상기 광감지부(130)는 포토다이오드일 수 있다.

[0037] 상기 광감지부(130)는 상기 반도체 기판(100)에 n형 이온주입영역 및 p형 이온주입영역의 의한 pn정션에 의하여 형성될 수 있으나, 이에 한정되는 것은 아니다.

[0038] 상기 p형 이온주입 영역에 의해 잉여전자 등을 방지할 수 있다. 또한, 실시예는 PNP 정션을 형성하여 전하덤핑(charge dumping) 효과를 얻을 수 있다.

[0039] 상기 광감지부(130)가 형성된 반도체 기판(100) 상에 신호처리를 위한 리드아웃 서킷(140)을 형성한다.

[0040] 예를 들어, 상기 리드아웃 서킷(140)은 트랜스퍼 트랜지스터, 리셋 트랜지스터, 드라이브 트랜지스터 및 셀렉트 트랜지스터를 포함할 수 있으나 이에 한정되는 것은 아니다.

[0041] 다음으로, 상기 반도체 기판(100)의 전면(Front Side) 상에 층간 절연층(150)과 배선을 형성한다. 예를 들어, 상기 배선은 제1 메탈(M1) 및 제2 메탈(M2) 등을 포함할 수 있다.

[0042] 한편, 상기 배선을 포함하는 층간 절연층(150) 상에 캐리어 웨이퍼(미도시)를 본딩할 수 있다. 이러한 캐리어 웨이퍼는 상기 반도체 기판(100)을 핸들링하기 위한 수단일 수 있다.

[0043] 도 2를 참조하여, 상기 반도체 기판(100) 전면(Front Side)의 반대인 후면(Back Side)의 일부를 제거한다.

[0044] 예를 들어, 상기 반도체 기판(100)의 이온주입층(105)을 기준으로 그 하측을 제거한다.

[0045] 즉, 상기 이온주입층(105)에 대한 열처리를 진행하여 수소이온을 기공화(bubble) 시킨 후 블레이드 등으로 깃탕하여 제거하고, 상기 반도체 기판(100)의 상측이 라이너 레이어(liner layer)로 남아있게 된다. 이후, 깃탕된 상기 반도체 기판(100)의 후면에 대한 평탄화공정이 진행될 수도 있다.

[0046] 또는, 상기 반도체 기판(100)의 전면측(Front Side)의 반대측을 백그라인딩(back grinding) 공정으로 제거할 수도 있다.

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[0047] 이에 따라, 상기 반도체 기판(100)의 후면(Back Side)인 고농도의 p층(p++)이 노출될 수 있다.

[0048] 또는 도 9에 도시된 바와 같이 상기 반도체 기판(100)의 후면 상에 제2 도전형 층(p+)(300) 형성할 수도 있다.

[0049] 상기 제2 도전형 층(300)은 반도체 기판(100) 후면 표면의 인터페이스에서 전하 트랩을 중성화시킬 수 있다.

[0050] 다음으로, 상기 반도체 기판(100)의 후면 상에 포토레지스트 패턴(10)이 형성된다.

[0051] 상기 포토레지스트 패턴(10)은 상기 단위픽셀에 대응하도록 패터닝될 수 있다. 이때, 상기 포토레지스트 패턴(10)의 개구부(15)는 상기 제1 소자분리막(120)의 위치와 대응되는 상기 반도체 기판(100)의 후면을 선택적으로 노출시킬 수 있다.

[0052] 도 3을 참조하여, 상기 반도체 기판(100)의 후면에 트렌치(160)가 형성된다.

[0053] 상기 트렌치(160)는 상기 제1 소자분리막(120)에 대응하도록 상기 반도체 기판(100)의 후면측에 형성될 수 있다.

[0054] 상기 트렌치(160)는 상기 포토레지스트 패턴을 식각마스크로 사용하는 식각공정을 통해 형성될 수 있다.

[0055] 상기 트렌치(160)는 상기 반도체 기판(100)의 고농도 p++영역과 상기 p형 에피층(110)을 소정 깊이로 식각하여 형성할 수 있다.

[0056] 도 4를 참조하여, 상기 트렌치(160)에 제2 소자분리막(170)이 형성된다.

[0057] 상기 제2 소자분리막(170)에 의하여 상기 반도체 기판(100)의 후면은 단위픽셀 별로 분리될 수 있다.

[0058] 상기 제2 소자분리막(170)은 상기 트렌치(160)에 금속물질 또는 절연물질을 갭필하여 형성될 수 있다.

[0059] 예를 들어, 상기 제2 소자분리막(170)은 텅스텐, 알루미늄 및 타이타늄과 같은 금속으로 형성될 수 있다. 특히, 상기 제2 소자분리막(170)이 금속으로 형성되어 입사광은 해당 픽셀이 아닌 인접 픽셀의 광감지부로 입사하는 것을 차단할 수 있다.

[0060] 예를 들어, 상기 제2 소자분리막(170)은 상기 제1 트렌치(160)와 동일한 산화막 또는 질화막으로 형성될 수 있다.

[0061] 도 5 및 도 6에 도시된 바와 같이, 상기 제2 소자분리막(170)은 상기 트렌치(160)의 내부에 서로 다른 굴절률(n)을 가지도록 형성할 수도 있다.

[0062] 도 5를 참조하여, 상기 트렌치(160)의 표면을 따라 제1 절연층(180)이 형성된다.

[0063] 상기 제1 절연층(180)은 제1 굴절률을 가지는 물질로 형성될 수 있다. 예를 들어, 상기 제1 굴절률은 1.0~1.46일 수 있다.

[0064] 도 6을 참조하여, 상기 트렌치(160)가 갭필되도록 상기 제1 절연층(180) 상에 제2 절연층(190)이 형성된다.

[0065] 상기 제2 절연층(190)은 제1 굴절률 보다 큰 제2 굴절률을 가지는 물질로 형성될 수 있다. 예를 들어, 상기 제2 굴절률은 1.68~3.0일 수 있다.

[0066] 예를 들어, 상기 제1 절연층(180)은 SiO$_2$(n=1.46)이고 제2 절연층(190)은 SiN(n=2.05)일 수도 있으나, 이에 한정되는 것은 아니다.

[0067] 상기 트렌치(160)의 외측 표면에 작은 굴절률을 가지는 물질을 채우고, 상기 트렌치(160)의 내측에 큰 굴절률을 가지는 물질을 채움으로써 제2 소자분리막(170)을 형성할 수 있다.

[0068] 상기 제2 소자분리막(170)은 서로 다른 굴절률을 가지는 이중층 구조를 가지므로써, 경사각을 가지고 입사되는 빛은 상기 제2 소자분리막(170)에 의하여 해당픽셀로 굴절되고 광감지부(130)로 입사될 수 있다. 즉, 상기 제2 소자분리막은 전반사 법칙이 적용된 것일 수 있다.

[0069] 이에 따라, 상기 제2 소자분리막(170)에 의하여 입사광을 해당하는 픽셀의 광감지부(130)로 굴절시키고, 단위픽셀의 수광율을 향상시킬 수 있다.

[0070] 도 7을 참조하여, 상기 반도체 기판(100)의 후면 상에 컬러필터(200)가 형성된다.

[0071] 상기 컬러필터(200)는 염색된 포토레지스트를 사용하여 각각의 단위픽셀마다 하나씩 형성되고 입사하는 빛으로

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부터 색을 분리할 수 있다.

[0072] 예를 들어, 상기 컬러필터(200)는 레드(Red), 그린(Green) 및 블루(Blue) 컬러필터 일 수 있다.

[0073] 이후, 상기 컬러필터(200) 상에 마이크로 렌즈(210)가 형성된다.

[0074] 상기 마이크로 렌즈(210)는 볼록렌즈 형태로 형성되고, 해당하는 단위픽셀의 광감지부로 빛을 집광시킬 수 있다.

[0075] 상기 반도체 기판(100)의 전면(front side)측에는 제1 소자분리막(120)이 형성되고, 상기 반도체 기판(100)의 후면(back side)측에는 제2 소자분리막(170)이 형성되어, 상기 반도체 기판(100)의 후면으로 입사되는 광의 크로스 토크를 방지할 수 있다.

[0076] 특히, 후면수광 이미지 센서에서 빛의 입사가 기판의 후면을 통해 이루어지고, 기판 표면으로부터 레드, 그린 및 블루 영역이 형성되기 때문에 광감지부의 가장 아래쪽에 위치한 블루 신호에 대한 크로스 토크를 발생을 방지할 수 있다.

[0077] 이에 따라, 이미지 센서의 광감도가 균일할 수 있다.

[0078] 도 8은 이중측벽 구조를 가지는 제2 소자분리막(170)을 포함하는 상기 반도체 기판(100)의 후면 상에 컬러필터(200) 및 마이크로 렌즈(210)가 형성된 것을 나타내는 단면도이다.

[0079] 도 9는 상기 제2 도전형 층(300) 및 반도체 기판(100)에 선택적으로 이중측벽 구조의 제2 소자분리막(170)이 형성된 것을 나타내는 단면도이다.

[0080] 상기 마이크로 렌즈(210) 및 컬러필터(200)를 통과한 빛은 해당하는 광감지부로 입사될 수 있다. 이때, 경사각을 가지로 입사되는 빛은 상기 제2 소자분리막(170)에 의하여 굴절되고 해당하는 픽셀의 광감지부(130)로 입사될 수 있다. 이에 따라, 이미지 센서의 광 감도를 향상시킬 수 있다.

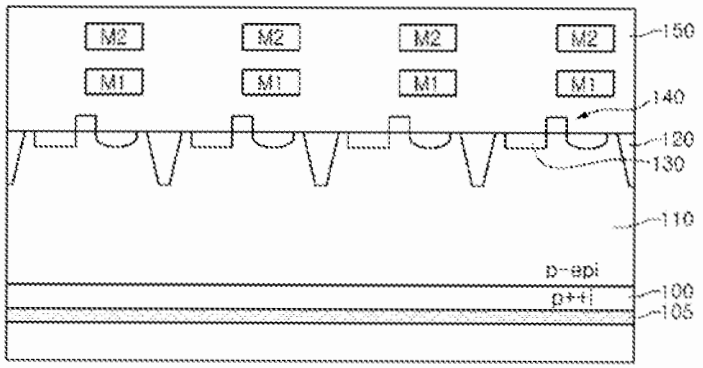
[0081] 본 발명은 기재된 실시예 및 도면에 의해 한정되는 것이 아니고, 청구항의 권리범위에 속하는 범위 안에서 다양한 다른 실시예가 가능하다.

도면의 간단한 설명

[0082] 도 1 내지 도 9는 실시예에 따른 이미지 센서의 제조공정을 나타내는 단면도이다.

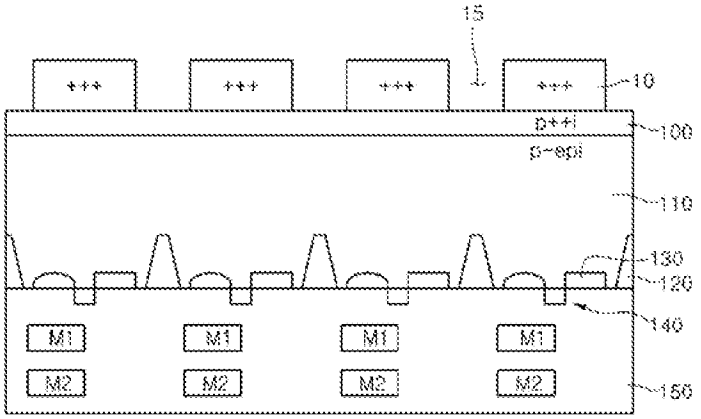
도면

도면1

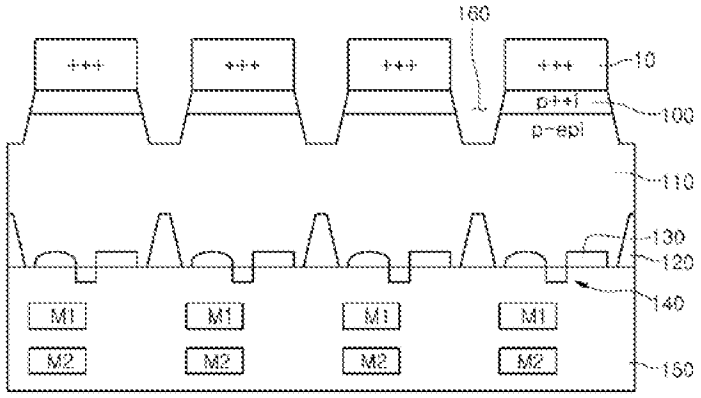


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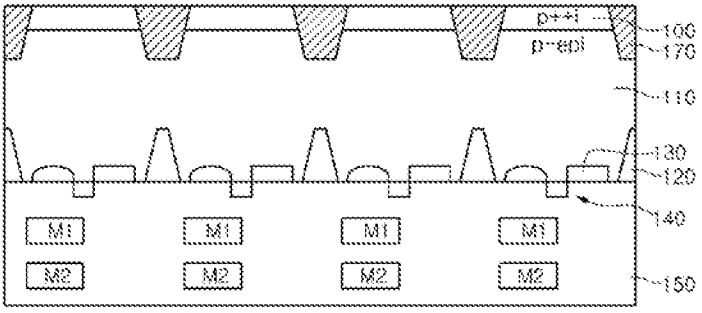
도면2



도면3

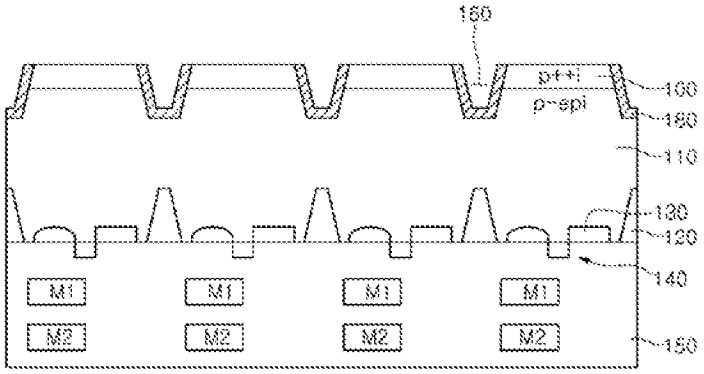


도면4

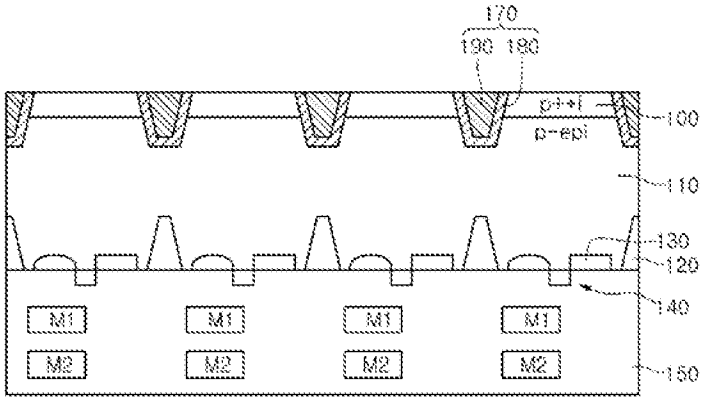


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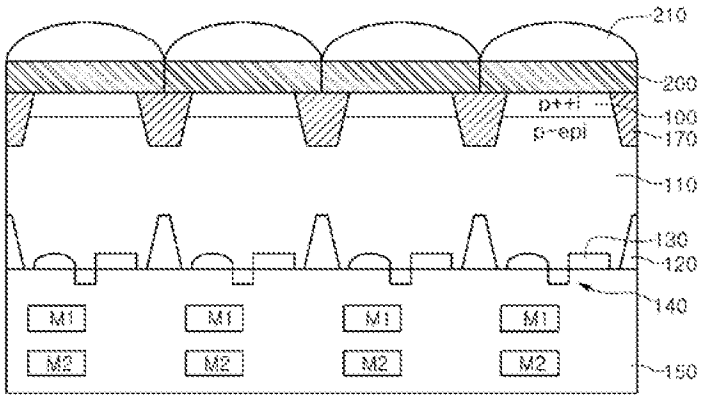
도면5



도면6

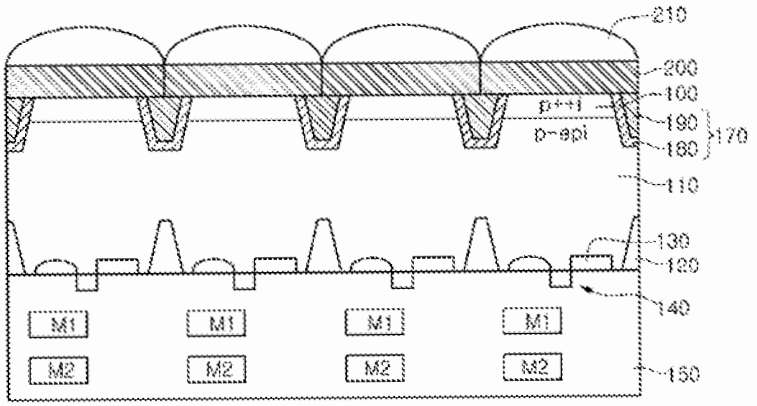


도면7

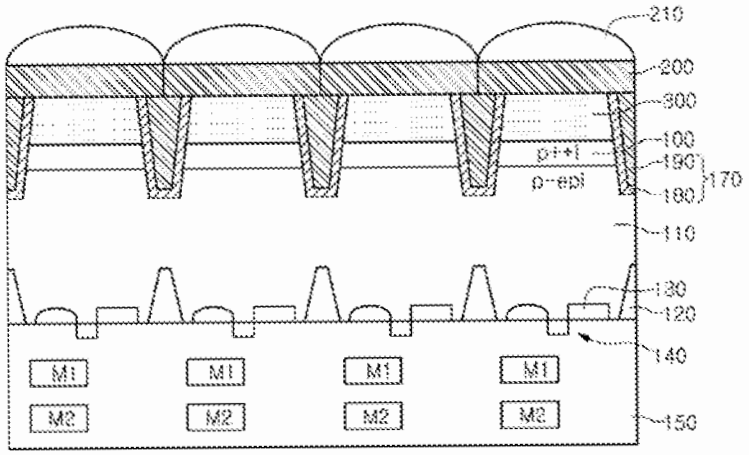


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도면8



도면9



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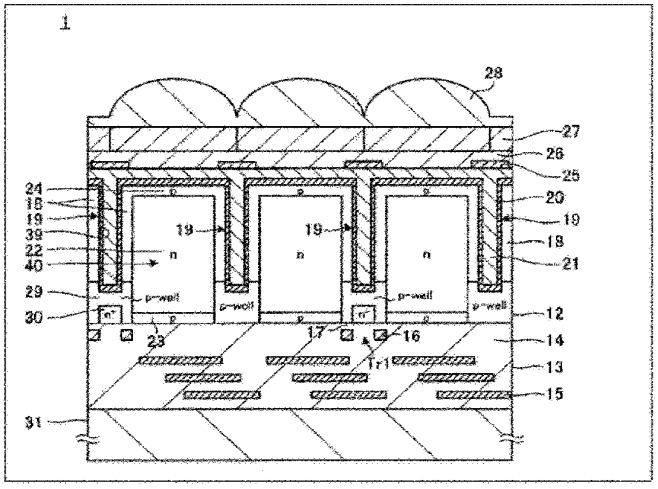
전체 청구항 수 : 총 22 항

(54) 발명의 명칭 **고체 촬상 장치, 고체 촬상 장치의 제조 방법 및 전자 기기**

(57) 요 약

본 기술은, 광학 혼색의 저감 등의 특성을 더욱 향상시킨 고체 촬상 장치를 제공할 수 있는 고체 촬상 장치, 고체 촬상 장치의 제조 방법 및 전자 기기에 관한 것이다. 또한, 그 고체 촬상 장치를 이용한 전자 기기를 제공한다. 기판(12)과, 기판(12)에 형성된 복수의 광전 변환부(40)를 구비한 고체 촬상 장치에서, 절연막(21)이 매입된 소자 분리부(19)를 형성한다. 소자 분리부(19)는, 기판(12)의 광입사측부터 깊이 방향으로 형성된 홈부(30) 내에서, 홈부(30)의 내벽면을 피복하도록 형성된 고정 전하를 갖는 절연막(20)으로 구성되어 있다.

대 표 도 - 도2



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명 세 서

청구범위

청구항 1

반도체 기판과,

상기 반도체 기판의 제1 광전 변환부와,

상기 반도체 기판의 제2 광전 변환부와,

상기 반도체 기판의 제3 광전 변환부와,

상기 제1 광전 변환부와 상기 제2 광전 변환부 사이에 배치된 제1 홈부와,

상기 제1 홈부는 상기 반도체 기판의 깊이 방향으로 연장되고, 고정 전하를 갖는 제1 절연막의 제1 부분을 포함하며,

상기 제2 광전 변환부와 상기 제3 광전 변환부 사이에 배치된 제2 홈부와,

상기 제2 홈부는 상기 반도체 기판의 깊이 방향으로 연장되고, 상기 제1 절연막의 제2 부분을 포함하며,

상기 제1 및 제2 광전 변환부 사이의 제1 절연막 상에 배치되는 제2 절연막과,

상기 제1 홈부의 깊이는 제2 홈부의 깊이보다 깊은 것을 특징으로 하는 고체 촬상 장치.

청구항 2

제1항에 있어서,

상기 제2 절연막은 실리콘 산화물, 실리콘 질화물 또는 실리콘 산 질화물을 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 3

제1항에 있어서,

상기 제1 절연막은, 하프늄(Hf), 알루미늄(Al), 지르코늄(Zr), 탄탈륨(Ta), 티타늄(Ti), 란타넘(La), 프라세오디뮴(Pr), 세륨(Ce), 네오디뮴(Nd), 프로메튬(Pm), 사마륨(Sm), 유로퓸(Eu), 가돌리늄(Gd), 터븀(Tb), 디스프로슘(Dy), 홀뮴(Ho), 툴륨(Tm), 이터븀(Yb), 루테튬(Lu) 또는 이트륨(Y) 중 적어도 어느 하나의 원소를 포함하는 산화물 또는 질화물인 것을 특징으로 하는 고체 촬상 장치.

청구항 4

제1항에 있어서,

상기 제1 절연막은 산화 하프늄을 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 5

제1항에 있어서,

상기 제2 절연막은 산화실리콘을 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 6

제1항에 있어서,

상기 반도체 기판은 광 입사 측인 제1면 및 상기 제1면의 반대측인 제2면을 포함하고, 배선층은 상기 제2면의 반도체 기판에 배치된 것을 특징으로 하는 고체 촬상 장치.

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청구항 7

제6항에 있어서,

상기 반도체 기판의 상기 제1면에 배치된 차광막을 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 8

제7항에 있어서,

상기 차광막상에 배치된 평탄화막을 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 9

제7항에 있어서,

상기 차광막의 상부에 배치된 컬러 필터를 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 10

제9항에 있어서,

상기 컬러 필터상에 배치된 온칩 렌즈를 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 11

제6항에 있어서,

상기 제1 홈부는 상기 반도체 기판의 상기 제2 면상에 형성된 p형 영역에 이르는 깊이로 형성되는 것을 특징으로 하는 고체 촬상 장치.

청구항 12

제1항에 있어서,

상기 제1 홈부는 상기 반도체 기판의 표면 측에 형성된 p형 영역에 이르는 깊이로 형성되는 것을 특징으로 하는 고체 촬상 장치.

청구항 13

제1항에 있어서,

플로팅 디퓨전부와,

상기 제1 광전 변환부는 상기 플로팅 디퓨전부에 연결되고, 상기 플로팅 디 퓨전부는 리셋 트랜지스터 및 증폭 트랜지스터에 연결되는 것을 특징으로 하는 고체 촬상 장치.

청구항 14

제13항에 있어서,

상기 플로팅 디퓨전부, 증폭 트랜지스터 및 리셋 트랜지스터는 상기 제1 광전 변환부 및 상기 제2 광전 변환부에 의해 공유되는 것을 특징으로 하는 고체 촬상 장치.

청구항 15

제13항에 있어서,

상기 증폭 트랜지스터에 연결된 선택 트랜지스터를 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 16

제15항에 있어서,

상기 선택 트랜지스터에 연결된 신호선을 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

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청구항 17

제16항에 있어서,

제1 광전 변환부에 연결된 전송 트랜지스터와,

상기 제1 광전 변환부와 상기 플로팅 디퓨전부 사이에 배치된 전송 게이트 전극을 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 18

제17항에 있어서,

상기 전송 게이트 전극은 상기 제1 광전 변환부와 상기 플로팅 디퓨전부 사이에 대각선 방향으로 배치되는 것을 특징으로 하는 고체 촬상 장치.

청구항 19

제1항에 있어서,

상기 제2 광전 변환부를 둘러싸는 소자 분리부를 포함하고, 상기 소자 분리부는 상기 제1 절연막의 제1 부분 및 상기 제2 절연막을 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 20

제1항에 있어서,

상기 제1 홈부의 적어도 일부 상에 배치된 차광막을 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 21

제1항에 있어서,

플로팅 디퓨전부와, 상기 제1 홈부는 상기 플로팅 디퓨전부 상에 배치되는 것을 특징으로 하는 고체 촬상 장치.

청구항 22

고체 촬상 장치는,

반도체 기판과,

상기 반도체 기판 내의 제1 광전 변환부와,

상기 반도체 기판 내의 제2 광전 변환부와,

상기 반도체 기판 내의 제3 광전 변환부와,

상기 제1 광전 변환부와 상기 제2 광전 변환부 사이에 배치된 제1 홈부와,

상기 제1 홈부는 상기 반도체 기판의 깊이 방향으로 연장되고, 고정 전하를 갖는 제1 절연막의 제1 부분을 포함하며,

상기 제2 광전 변환부와 상기 제3 광전 변환부 사이에 배치된 제2 홈부와,

상기 제2 홈부는 반도체 기판의 깊이 방향으로 연장되고, 상기 제1 절연막의 제2 부분을 포함하며,

상기 제1 및 제2 광전 변환부 사이의 제1 절연막 상에 배치되는 제2 절연막과,

상기 제1 홈부의 깊이는 상기 제2 홈부의 깊이보다 깊으며, 상기 고체 촬상 장치상에 화상을 형성하도록 구성된 광학 렌즈를 포함하는 것을 특징으로 하는 전자 기기.

발명의 설명

기 술 분 야

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[0001] 본 개시는, 이면(裏面) 조사형의 고체 촬상 장치와 그 제조 방법 및 전자 기기에 관한 것이다.

배 경 기 술

[0002] 근래, 기판상의 배선층이 형성되는 측과는 반대측부터 광을 조사하는, 이면 조사형의 고체 촬상 장치가 제안되어 있다(하기 특허 문헌 1 참조). 이면 조사형의 고체 촬상 장치에서는, 광조사측에 배선층이나 회로 소자 등이 형성되지 않기 때문에, 기판에 형성된 수광부의 개구률을 높게 할 수 있는 외에, 입사광이 배선층 등에서 반사되는 일 없이 수광부에 입사되기 때문에, 감도의 향상이 도모된다.

[0003] 특허 문헌 1의 고체 촬상 장치는, 광학 혼색(混色)을 저감하기 위해, 화소 경계에 차광막을 마련하고 있다.

선행기술문헌

특허문헌

[0004] (특허문헌 0001) 일본 특개2010-186818호 공보

발명의 내용

해결하려는 과제

[0005] 이와 같은 고체 촬상 장치에서, 광학 혼색의 저감 등의 한층 더 특성 향상이 요구되고 있다.

[0006] 본 개시는, 광학 혼색의 저감 등의 특성을 더욱 향상시킨 고체 촬상 장치를 제공한다. 또한, 그 고체 촬상 장치를 이용한 전자 기기를 제공한다.

과제의 해결 수단

[0007] 본 개시된 제1의 측면의 고체 촬상 장치는, 기판과, 기판에 형성된 복수의 광전 변환부를 구비한다. 또한, 기판의 광입사측부터 깊이 방향으로 형성된 홈부(溝部) 내에서, 홈부의 내벽면을 피복하도록 형성된 고정 전하를 갖는 절연막으로 구성되는 소자 분리부를 구비한다.

[0008] 본 개시된 제2의 측면의 고체 촬상 장치는, 기판과, 상기 기판에 형성된 복수의 광전 변환부를 구비한다. 또한, 기판의 광입사측부터 깊이 방향으로 형성된 홈부와, 홈부의 내벽면을 피복하도록 마련된 막을 구비하고, 중공(中空) 구조를 갖는 소자 분리부를 구비한다.

[0009] 본 개시된 제1의 측면의 고체 촬상 장치의 제조 방법은, 기판에, 광전 변환부를 갖는 복수의 화소를 형성하는 공정과, 기판의 이면측부터 깊이 방향에 걸쳐서 소망하는 깊이의 홈부를 형성하는 공정을 갖는다. 다음에, 홈부의 내벽면에 고정 전하를 갖는 절연막을 형성하고, 소자 분리부를 형성하는 공정을 갖는다.

[0010] 본 개시된 제2의 측면의 고체 촬상 장치의 제조 방법은, 기판에, 광전 변환부를 갖는 복수의 화소를 형성하는 공정과, 기판의 이면측부터 깊이 방향에 걸쳐서 소망하는 깊이의 홈부를 형성하는 공정을 갖는다. 다음에, 홈부의 내부에 중공부가 형성되도록 상기 홈부의 내벽면에 소망하는 막을 성막함으로써 소자 분리부를 형성하는 공정을 갖는다.

[0011] 본 개시된 전자 기기는, 광학 렌즈와, 광학 렌즈에 집광된 광이 입사되는 상술한 고체 촬상 장치와, 고체 촬상 장치로부터 출력되는 출력 신호를 처리하는 신호 처리 회로를 구비한다.

발명의 효과

[0012] 본 개시에 의하면, 고체 촬상 장치에서, 혼색 저감 등의 특성의 한층 더 향상이 도모된다. 또한, 그 고체 촬상 장치를 이용함에 의해, 화질의 향상이 도모된 전자 기기를 얻을 수 있다.

도면의 간단한 설명

[0013] 도 1은 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치의 전체 구성을 도시하는 도면.

도 2는 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

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도 3은 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치의 평면 레이아웃도.

도 4의 A 및 도 4의 B는, 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 5의 C 및 도 5의 D는, 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 6은 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치와 종래의 고체 촬상 장치의 주요부의 포텐셜 분포도.

도 7은 제1의 실시 형태의 변형례 1에 관한 고체 촬상 장치의 평면 레이아웃도.

도 8은 제1의 실시 형태의 변형례 2에 관한 고체 촬상 장치의 평면 레이아웃도.

도 9는 본 개시된 제2의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 10의 A 내지 도 10의 C는, 본 개시된 제2의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 11은 본 개시된 제3의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 12는 본 개시된 제4의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 13의 A 및 도 13의 B는, 본 개시된 제4의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 14의 C는, 본 개시된 제4의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 15는 본 개시된 제5의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 16은 본 개시된 제6의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 17은 본 개시된 제7의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 18의 A 및 도 18의 B는, 본 개시된 제7의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 19는 본 개시된 제8의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 20의 A 및 도 20의 B는, 본 개시된 제8의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 21은 변형례에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 22는 본 개시된 제9의 실시 형태에 관한 전자 기기의 개략 구성도.

발명을 실시하기 위한 구체적인 내용

[0014] 본 발명자들은, 특허 문헌 1의 고체 촬상 장치에서, 이하의 과제를 발견하였다.

[0015] 이면형의 고체 촬상 장치에서는, 포토 다이오드가 형성되는 반도체층이 표면 조사형의 고체 촬상 장치와 비교하여 얇게 형성된다. 이 때문에, 종래의 표면 조사형의 고체 촬상 장치에서는, 포토 다이오드에서 넘쳐진 신호 전하는 반도체층의 깊이 방향(종방향)으로 오버플로시키는 구성이 채택되어 있지만, 이면 조사형의 고체 촬상 장치에서는, 반도체층의 깊이 방향으로 오버플로시킬 수가 없다. 이 때문에, 이면 조사형의 고체 촬상 장치에서는, 포토 다이오드에서 넘쳐진 전자는, 플로팅 디퓨전에 흐르도록 구성되어 있다(이른바, 래터럴 오버플로).

[0016] 래터럴 오버플로 구조를 채용하는 경우, 포토 다이오드로부터 넘쳐진 전자가, 플로팅 디퓨전측으로 흐르는지, 인접하는 포토 다이오드측으로 흐르는지는, 기판 내의 포텐셜에 의해 정해진다. 따라서 전하 축적시에, 포토 다이오드와 플로팅 디퓨전과의 사이의 포텐셜을, 인접하는 포토 다이오드 사이의 포텐셜보다도 높게 설정함으로써, 넘쳐진 전자를 수시로 플로팅 디퓨전에 전송할 수 있다. 이 때문에, 넘쳐진 전자를 플로팅 디퓨전에 전송 가능한 구성으로 하는 경우, 포화 전하량(Qs)의 저하가 큰 과제로 된다. 한편, 포화 전하량을 크게 한 경우에는, 장시간 축적시에 백점(白点) 화소로부터 넘쳐진 신호 전하가 인접하는 화소에 누입(漏入)되어 감으로써 블루밍(blooming)이 발생하고, 해상도 열화, 화질 열화의 하나의 원인이 된다.

[0017] 또한, 화소 경계에 차광막을 마련하는 구조에서는, 비스듬한 광이 들어온 경우에 차광막의 아래에서 발생하는 혼색을 완전히 억제할 수가 없다.

[0018] 본 개시된 실시 형태에서는, 혼색 저감, 블루밍의 억제나 포화 특성의 향상이 가능한 고체 촬상 장치에 관해 설명한다.

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[0019] 이하에, 본 개시된 실시 형태에 관한 고체 촬상 장치와 그 제조 방법, 및 전자 기기의 한 예를, 도 1 내지 도 22를 참조하면서 설명한다. 본 개시된 실시 형태는 이하의 순서로 설명한다. 또한, 본 개시는 이하의 예로 한정되는 것이 아니다.

[0020] 1. 제1의 실시 형태 : 고체 촬상 장치(4화소로 하나의 플로팅 디퓨전부를 공유하는 예)

[0021] 1-1 고체 촬상 장치 전체의 구성

[0022] 1-2 주요부의 구성

[0023] 1-3 고체 촬상 장치의 제조 방법

[0024] 1-4 변형례 1

[0025] 1-5 변형례 2

[0026] 2. 제2의 실시 형태 : 고체 촬상 장치(소자 분리부 내에 차광막이 형성되는 예)

[0027] 3. 제3의 실시 형태 : 고체 촬상 장치(소자 분리부의 기판 이면측의 단부만이 p형 반도체 영역에 접하는 예)

[0028] 4. 제4의 실시 형태 : 고체 촬상 장치(소자 분리부가 기판을 관통하는 예)

[0029] 5. 제5의 실시 형태 : 고체 촬상 장치(소자 분리부 내에 형성된 차광층이 배선층에 접속되는 예)

[0030] 6. 제6의 실시 형태 : 고체 촬상 장치(소자 분리부에 2층의 고정 전하막을 형성하는 예)

[0031] 7. 제7의 실시 형태 : 고체 촬상 장치(소자 분리부가 중공 구조인 예)

[0032] 8. 제8의 실시 형태 : 고체 촬상 장치(소자 분리부가 중공 구조인 예)

[0033] 8-1 변형례

[0034] 9. 제9의 실시 형태 : 전자 기기

[0035] <1. 제1의 실시 형태 : 고체 촬상 장치>

[0036] [1-1 고체 촬상 장치 전체의 구성]

[0037] 도 1은, 본 개시된 제1의 실시 형태에 관한 CMOS형의 고체 촬상 장치의 전체를 도시하는 개략 구성도이다.

[0038] 본 실시 형태의 고체 촬상 장치(1)는, 실리콘으로 이루어지는 기판(11)상에 배열된 복수의 화소(2)를 갖는 화소 영역(3)과, 수직 구동 회로(4)와, 칼럼 신호 처리 회로(5)와, 수평 구동 회로(6)와, 출력 회로(7)와, 제어 회로(8) 등을 갖고서 구성된다.

[0039] 화소(2)는, 포토 다이오드로 이루어지는 광전 변환부와, 복수의 화소 트랜지스터로 구성되고, 기판(11)상에, 2차원 어레이형상으로 규칙적으로 복수 배열된다. 화소(2)를 구성하는 화소 트랜지스터는, 전송 트랜지스터, 리셋 트랜지스터, 선택 트랜지스터, 앰프 트랜지스터로 구성되는 4개의 MOS 트랜지스터라도 좋고, 또한, 선택 트랜지스터를 제외한 3개의 트랜지스터라도 좋다.

[0040] 화소 영역(3)은, 2차원 어레이형상으로 규칙적으로 배열된 복수의 화소(2)를 갖는다. 화소 영역(3)은, 실제로 광을 수광하고 광전 변환에 의해 생성된 신호 전하를 증폭하여 칼럼 신호 처리 회로(5)에 판독하는 유효 화소 영역과, 흑레벨의 기준이 되는 광학적 흑을 출력하기 위한 흑 기준 화소 영역(도시 생략)으로 구성되어 있다. 흑 기준 화소 영역은, 통상은, 유효 화소 영역의 외주부에 형성되는 것이다.

[0041] 제어 회로(8)는, 수직 동기 신호, 수평 동기 신호 및 마스터 클록에 의거하여, 수직 구동 회로(4), 칼럼 신호 처리 회로(5), 및 수평 구동 회로(6) 등의 동작의 기준이 되는 클록 신호나 제어 신호 등을 생성한다. 그리고, 제어 회로(8)에서 생성된 클록 신호나 제어 신호 등은, 수직 구동 회로(4), 칼럼 신호 처리 회로(5) 및 수평 구동 회로(6) 등에 입력된다.

[0042] 수직 구동 회로(4)는, 예를 들면 시프트 레지스터에 의해 구성되고, 화소 영역(3)의 각 화소(2)를 행 단위로 순차적으로 수직 방향으로 선택 주사한다. 그리고, 각 화소(2)의 포토 다이오드에서 수광량에 응하여 생성한 신호 전하에 의거한 화소 신호를, 수직 신호선을 통하여 칼럼 신호 처리 회로(5)에 공급한다.

[0043] 칼럼 신호 처리 회로(5)는, 예를 들면, 화소(2)의 열마다 배치되어 있고, 1행분의 화소(2)로부터 출력된 신호를 화소열마다 흑 기준 화소 영역(도시하지 않지만, 유효 화소 영역의 주위에 형성된다)으로부터의 신호에 의해,

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노이즈 제거나 신호 증폭 등의 신호 처리를 행한다. 칼럼 신호 처리 회로(5)의 출력단에는, 수평 선택 스위치(도시 생략)가 수평 신호선(10)과의 사이에 마련되어 있다.

[0044] 수평 구동 회로(6)는, 예를 들면 시프트 레지스터에 의해 구성되고, 수평 주사 펄스를 순차적으로 출력함에 의해, 칼럼 신호 처리 회로(5)의 각각을 순번대로 선택하고, 칼럼 신호 처리 회로(5)의 각각으로부터 화소 신호를 수평 신호선(10)에 출력시킨다.

[0045] 출력 회로(7)는, 칼럼 신호 처리 회로(5)의 각각으로부터 수평 신호선(10)을 통하여, 순차적으로 공급되는 신호에 대해 신호 처리를 행하여 출력한다.

[0046] [1-2 주요부의 구성]

[0047] 도 2에, 본 실시 형태의 고체 촬상 장치(1)의 화소 영역(3)에서의 단면 구성을 도시하고, 도 3에, 본 실시 형태의 고체 촬상 장치(1)의 화소 영역(3)의 평면 레이아웃을 도시한다. 본 실시 형태의 고체 촬상 장치(1)는, 이면 조사형의 CMOS형 고체 촬상 장치를 예로 한 것이고, 4개의 광전 변환부에 대해 소요되는 화소 트랜지스터를 공유시킨, 이른바 4화소 공유를 1단위로 한 예이다. 또한, 이하의 설명에서는, 제1 도전형을 p형으로 하고, 제2 도전형을 n형으로 하여 설명한다.

[0048] 도 2에 도시하는 바와 같이, 본 실시 형태의 고체 촬상 장치(1)는, 복수의 화소를 갖는 기판(12)과, 기판(12)의 표면측에 형성된 배선층(13)과, 지지 기판(31)을 구비한다. 또한, 기판(12)의 이면측에 차례로 형성된 고정 전하를 갖는 절연막(이하, 고정 전하막)(20)과, 절연막(21)과, 차광막(25)과, 평탄화막(26)과, 컬러 필터층(27)과, 온칩 렌즈(28)를 또한 구비한다.

[0049] 기판(12)은, 실리콘으로 이루어지는 반도체 기판으로 구성되고, 예를 들면 1㎛ 내지 6㎛의 두께를 갖고서 형성되어 있다. 기판(12)의 화소 영역(3)에는 포토 다이오드로 이루어지는 광전 변환부(40)와, 화소 회로부를 구성하는 복수의 화소 트랜지스터(Tr1 내지 Tr4)로 구성되는 화소가 복수개, 2차원 매트릭스형상으로 형성되어 있다. 그리고, 인접하는 광전 변환부(40) 사이는 소자 분리부(19)에 의해 전기적으로 분리되어 있다. 또한, 도 2에서는 도시를 생략하지만, 기판(12)에 형성된 화소 영역의 주변 영역에는, 주변 회로부가 구성되어 있다.

[0050] 광전 변환부(40)는, 기판(12)의 표면측 및 이면측에 형성되는 제1 도전형(이하 p형) 반도체 영역(23, 24)과, 그 사이에 형성되는 제2 도전형(이하 n형) 반도체 영역(22)으로 구성되어 있다. 광전 변환부(40)에서는, 그 p형 반도체 영역(23, 24)과 n형 반도체 영역(22)와의 사이의 pn 접합으로 주된 포토 다이오드가 구성되어 있다. 광전 변환부(40)에서는, 입사한 광의 광량에 응한 신호 전하가 생성되고, n형 반도체 영역(22)에 축적된다. 또한, 기판(12)의 계면에서 발생하는 암전류의 원인이 되는 전자는 기판(12)의 표면 및 이면에 형성된 p형 반도체 영역(23, 24)의 다수 캐리어인 정공에 흡수됨에 의해, 암전류가 억제된다.

[0051] 또한, 각 광전 변환부(40)는 p형 반도체 영역으로 구성된 화소 분리층(18)과, 그 화소 분리층(18) 내에 형성된 소자 분리부(19)에 의해 전기적으로 분리되어 있다.

[0052] 화소 트랜지스터는, 본 실시 형태에서는, 도 3에 도시하는 바와 같이, 전송 트랜지스터(Tr1), 리셋 트랜지스터(Tr2), 증폭 트랜지스터(Tr3), 선택 트랜지스터(Tr4)의 4개의 트랜지스터로 구성되어 있다.

[0053] 전송 트랜지스터(Tr1)는, 도 3에 도시하는 바와 같이, 2행2열로 형성된 4개의 광전 변환부(40)의 중심부에 형성된 플로팅 디퓨전부(30)와, 전송 게이트 전극(16)으로 구성되어 있다. 플로팅 디퓨전부(30)는, 도 2에 도시하는 바와 같이, 기판(12)의 표면측에 형성된 p-웰층(29)에, n형의 불순물이 고농도로 이온 주입됨으로써 형성된 n형 반도체 영역으로 구성된다. 또한, 전송 게이트 전극(16)은, 광전 변환부(40)와 플로팅 디퓨전부(30)와의 사이의 기판(12) 표면측에, 게이트 절연막(17)을 통하여 형성되어 있다.

[0054] 화소 트랜지스터 중, 리셋 트랜지스터(Tr2), 증폭 트랜지스터(Tr3), 선택 트랜지스터(Tr4)는 플로팅 디퓨전부(30)를 공유하는 4개의 광전 변환부(40)마다 형성되어 있다. 이들의 화소 트랜지스터는, 도 3에 도시하는 바와 같이 4개의 광전 변환부(40)로 구성되는 군의 일방의 측에 배치되어 있다.

[0055] 리셋 트랜지스터(Tr2)는, 대(對)의 소스·드레인 영역(35 및 36)과, 그 소스·드레인 영역(35, 36)의 사이에 형성된 리셋 게이트 전극(32)에 의해 구성된다. 증폭 트랜지스터(Tr3)는, 대의 소스·드레인 영역(36 및 37)과, 그 소스·드레인 영역(36, 37)의 사이에 형성된 증폭 게이트 전극(33)에 의해 구성된다. 선택 트랜지스터(Tr4)는, 대의 소스·드레인 영역(37 및 38)과, 그 소스·드레인 영역(37, 38)의 사이에 형성된 선택 게이트 전극(34)에 의해 구성된다.

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[0056] 리셋 트랜지스터(Tr2), 증폭 트랜지스터(Tr3), 선택 트랜지스터(Tr4)에 관해서는 단면 구성의 도시를 생략하지만, 이들의 화소 트랜지스터에 관해서도 전송 트랜지스터(Tr1)와 같은 구성으로 되어 있다. 즉, 소스·드레인 영역(35 내지 38)은, 플로팅 디퓨전부(30)와 마찬가지로 기판(12)의 표면의 p-웰층(29) 내에 형성된 n형의 고농도 불순물 영역으로 구성된다. 또한, 리셋 게이트 전극(32), 증폭 게이트 전극(33), 선택 게이트 전극(34)은, 기판(12)의 표면측에 게이트 절연막(17)을 통하여 형성되어 있다.

[0057] 소자 분리부(19)는, 기판(12)의 이면측부터 깊이 방향으로 형성된 홈부(39) 내에 차례로 매입하여 형성된 고정 전하막(20), 및 절연막(21)으로 구성되고, 기판(12)에 형성된 화소 분리층(18) 내에 새겨 넣어져서 형성되어 있다. 즉, 소자 분리부(19)는, 도면에 도시하는 바와 같이 화소를 둘러싸도록 격자형상으로 형성되어 있다. 또한, 인접하는 광전 변환부(40)와 광전 변환부(40)의 사이에 화소 트랜지스터가 형성되어 있는 경우에는, 플로팅 디퓨전부(30)나 소스·드레인 영역에 겹쳐지도록 배치되어 있다.

[0058] 또한, 소자 분리부(19)는, 화소 트랜지스터가 형성되는 p-웰층(29)에 달하는 깊이로 형성되고, 플로팅 디퓨전부(30)나 소스·드레인 영역에는 달하지 않는 깊이로 형성되어 있다. 플로팅 디퓨전부(30)나 소스·드레인 영역의 깊이가 1㎛ 미만이라고 하면, 소자 분리부(19)는, 기판(12) 표면부터 0.25 내지 5.0㎛ 정도의 깊이까지 형성할 수 있다. 본 실시 형태에서는, 화소 트랜지스터의 p-웰층(29)에 달하는 깊이로 형성되어 있지만, 소자 분리부(19)의 기판(12) 이면측의 단부가 p형의 반도체층에 접하도록 형성되면 좋고, 반드시 p-웰층(29)에 달하는 깊이가 아니라도 좋다. 본 실시 형태와 같이, p형 반도체층으로 이루어지는 화소 분리층(18) 내에 형성되는 경우에는, p-웰층(29)에 달하지 않는 구성으로도 절연 분리의 효과를 얻을 수 있다.

[0059] 또한, 홈부(39)에 형성되는 고정 전하막(20)은 홈부(39)의 내주면(內周面) 및 저면에 성막됨과 함께, 기판(12)의 이면 전면(全面)에 형성되어 있다. 또한, 이하의 설명에서는, 홈부(30)의 내주면 및 저면을 합쳐서, 「내벽면」으로 하여 설명한다. 고정 전하막(20)으로서는, 실리콘 등의 기판상에 퇴적함에 의해 고정 전하를 발생시켜서 피닝(pining)을 강화시키는 것이 가능한 재료를 사용하는 것이 바람직하고, 부(負)의 전하를 갖는 고굴절률 재료막 또는 고유전체막을 이용할 수 있다. 구체적인 재료로서는, 예를 들면, 하프늄(Hf), 알루미늄(Al), 지르코늄(Zr), 탄탈럼(Ta) 및 타이타늄(Ti) 중 적어도 하나의 원소를 포함하는 산화물 또는 질화물을 적용할 수 있다. 성막 방법으로서는, 예를 들면, 화학기상 성장법(이하, CVD(Chemical Vapor Deposition)법), 스퍼터링법, 원자층 증착법(이하, ALD(Atomic Layer Deposition)법) 등을 들 수 있다. ALD법을 이용하면, 성막중에 계면준위를 저감하는 SiO2막을 동시에 1㎚ 정도의 막두께로 형성할 수 있다. 또한, 상기 이외의 재료로서는, 란타넘(La), 프라세오디뮴(Pr), 세륨(Ce), 네오디뮴(Nd), 프로메튬(Pm), 사마륨(Sm), 유로퓸(Eu), 가돌리늄(Gd), 터븀(Tb), 디스프로슘(Dy), 홀뮴(Ho), 툴륨(Tm), 이터븀(Yb), 루테튬(Lu) 및 이트륨(Y) 중 적어도 하나의 원소를 포함하는 산화물 또는 질화물 등을 들 수 있다. 또한, 상기 고정 전하막은, 산질화하프늄막 또는 산질화알루미늄막으로 형성하는 것도 가능하다.

[0060] 상술한 고정 전하막(20)의 재료에는, 절연성을 손상시키지 않는 범위에서, 막 내에 실리콘(Si)이나 질소(N)가 첨가되어 있어도 좋다. 그 농도는, 막의 절연성이 손상되지 않는 범위에서 적절히 결정된다. 이와 같이, 실리콘(Si)이나 질소(N)가 첨가됨에 의해, 막의 내열성이나 프로세스 중에서 이온 주입의 저지 능력을 올리는 것이 가능해진다.

[0061] 본 실시 형태에서는, 홈부(39)의 내벽면 및 기판(12)의 이면에 부의 전하를 갖는 고정 전하막(20)이 형성되어 있기 때문에, 고정 전하막(20)에 접한 면에 반전층이 형성된다. 이에 의해, 실리콘 계면이 반전층에 의해 피닝되기 때문에, 암전류의 발생이 억제된다. 또한, 기판(12)에 홈부(39)를 형성하는 경우, 홈부(39)의 측벽 및 저면에 물리적 데미지가 발생하고, 홈부(39)의 주변부에서 피닝 어긋남이 발생할 가능성이 있다. 이 문제점에 대해, 본 실시 형태에서는, 홈부(39)의 측벽 및 저면에 고정 전하를 많이 갖는 고정 전하막(20)을 형성함에 의해 피닝 어긋남이 방지된다.

[0062] 절연막(21)은, 고정 전하막(20)이 형성된 홈부(39) 내에 매입됨과 함께, 기판(12)의 이면측 전면에 형성되어 있다. 절연막(21)의 재료로서는, 고정 전하막(20)과는 다른 굴절률을 갖는 재료로 형성하는 것이 바람직하고, 예를 들면, 산화실리콘, 질화실리콘, 산질화실리콘, 수지 등을 사용할 수 있다. 또한, 정(正)의 고정 전하를 갖지 않는, 또는 정의 고정 전하가 적다는 특징을 갖는 재료를 절연막(21)에 이용할 수 있다.

[0063] 그리고, 홈부(39)가 절연막(21)으로 매입됨에 의해, 각 화소를 구성하는 광전 변환부(40)가 절연막(21)을 통하여 분리된다. 이에 의해, 인접 화소에 신호 전하가 누입되기 어려워지기 때문에, 포화 전하량(Qs)을 초과한 신호 전하가 발생한 경우에 있어서, 넘쳐진 신호 전하가 인접하는 광전 변환부(40)에 누입되는 것을 저감할 수 있

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Growth of Ⅲ-nitride light-emitting devices on textured substrates

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Abstract of TW200627675 (A)

A III-nitride light emitting device is grown on a textured substrate, in order to reduce the amount of total internal reflection at the interface between the substrate and the III-nitride layers. In some embodiments, the device includes a first growth region substantially free of voids, and a second growth region that improves the material quality such that high quality layers can be grown over the first and second regions.

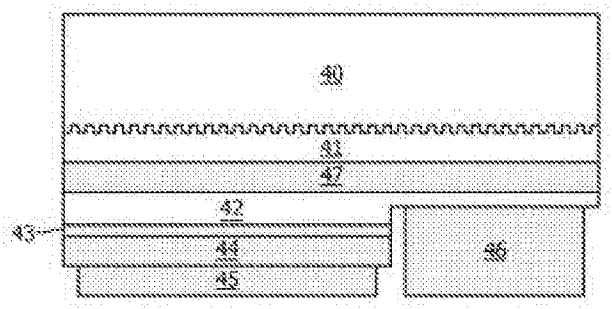


FIG. 1

發明專利說明書

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紋理基底上III族氮化物發光裝置之成長

GROWTH OF III-NITRIDE LIGHT-EMITTING DEVICES ON TEXTURED SUBSTRATES

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四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其事實發生日期為：　年　月　日。

☑ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號　順序註記】

☑ 有主張專利法第二十七條第一項國際優先權：

1. 美國；2004年09月23日；10/950,000

2.

☐ 無主張專利法第二十七條第一項國際優先權：

1.

2.

☐ 主張專利法第二十九條第一項國內優先權：

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☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料　【格式請依：寄存機構、日期、號碼　順序註記】

國外生物材料　【格式請依：寄存國家、機構、日期、號碼　順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

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九、發明說明：

【發明所屬之技術領域】

本發明係關於III族氮化物發光裝置之成長。

【先前技術】

半導體發光二級體(LED)係目前可獲得之最有效光源之一。目前所關注的用於製造能跨越可見光譜操作之高亮度LED的材料系統包括：III-V族化合物半導體，特定言之為鎵、鋁、銦及氮之二元、三元及四元合金，亦稱為III族氮化物材料。該等裝置通常具有一夾於p-摻雜區域與n-摻雜區域之間的發光或活性區域。該活性區域可為一單一發光層或藉由障壁層隔開之多個量子井層。III族氮化物裝置通常係藉由金屬有機化學汽相沈積(MOCVD)、分子束磊晶法(MBE)或其他磊晶技術而於藍寶石、碳化矽或III族氮化物基底上磊晶成長。成長於一傳導性基底上之裝置通常具有形成於基底相對側面上的觸點。或者，該裝置在成長於傳導性較差之基底上時，可經蝕刻以曝露基底同側之n-類型部分及p-類型區域部分兩者，或出於光學或電學原因而如此。然後，該等觸點係形成於曝露區域上。若該等觸點係反射性且光自該裝置之相對於觸點的一側經提取，該裝置稱為覆晶。由於藍寶石的高溫穩定性且相對容易生產，因而III族氮化物LED結構通常成長於藍寶石基底上。

由於半導體層與基底之間的界面上之折射率存在很大差異，因而藍寶石基底之使用可導致提取效率不良。當光入射至兩種材料之界面上時，折射率之差異決定於該界面上

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多少光經反射，且多少光透射穿過該界面。折射率差異愈大，反射的光愈多。藍寶石之折射率(1.8)係低於藍寶石上所成長之III族氮化物裝置層(2.4)之折射率。因此，當III族氮化物裝置層上所產生之光到達半導體層與藍寶石基底之間的界面上時，該光之大部分係經反射。反射光在經提取前係經波導且形成大量穿過該裝置的通道(pass)。歸因於III族氮化物裝置層的任一層內觸點處的光學損失、自由載體吸收及帶間吸收，該等大量通道致使光顯著衰減。

【發明內容】

根據本發明之實施例，一III族氮化物發光裝置係成長於一紋理基底上，以降低該基底與該III族氮化物層之間的界面處的全內反射量。在某些實施例中，該裝置包括一大體上無空隙之第一成長區域，及一第二成長區域；該第二成長區域係用於改良材料品質，使得高品質層可成長於該第一及第二區域之上方。

【實施方式】

藍寶石或其他合適基底與III族氮化物裝置層之間的界面處之全內反射可藉由紋理化或圖案化該基底而降低。如本文所用，"紋理化"意指基底表面歸因於表面任意粗糙化或歸因於表面上形成具重複特徵部分之圖案而不平滑。為節省語言，下述許多實例意指圖案化之基底表面。應理解，相同的原則可應用於具有任意粗糙化之基底表面的裝置。一圖案化基底一般具有隨圖案變化而變化之厚度。如本文所用，一圖案化基底上之"特徵部分(feature)"意指基底上

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比最小基底厚度較厚之圖案部分。舉例而言，若基底上之圖案包括由基底較薄之三角區域介於基底較厚之三角區域中，如圖3A所示，該"特徵部分"係較厚之三角區域。

高品質III族氮化物裝置層很難成長於圖案化基底上。一種將高品質III族氮化物層成長於圖案化基底或圖案化緩衝層上的技術係磊晶橫向過度成長，如(例如)Zheleva等人之題為"Methods of Fabricating Gallium Nitride Semiconductor Layers By Lateral Growth From Sidewalls Into Trenches, and Gallium Nitride Semiconductor Structures Fabricated Thereby"的美國專利第6,265,289號中所描述。磊晶橫向過度成長技術使III族氮化物層自基底上所形成之圖案化區域，或者成長基底上方所形成的III族氮化物緩衝層上之圖案化區域橫向成長。圖案化區域通常係經蝕刻之凸台，其中橫向成長主要源於凸台頂部，或圖案化區域通常為由遮罩層蝕刻之窗，其中成長主要源於窗內部。當磊晶橫向過度成長可導致產生高品質材料時，一主要缺點在於橫向成長條件通常導致橫向成長材料下方之渠溝中的空隙填充有空氣。由於空氣具有比III族氮化物材料及藍寶石兩者之折射率更低的折射率，該等空隙可導致全內反射，潛在地減少自該裝置所提取的光的數量。此外，用於促進磊晶橫向過度成長之圖案，凸台或藉由遮罩層蝕刻之窗，通常無法經優化以改良自該裝置之光提取。

當III族氮化物層在有利於填充圖案化基底上之特徵部分的條件下成長時，歸因於源自圖案化基底不同特徵部分上

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的晶粒碰撞，所得III族氮化物晶體層粗糙，具有小結晶粒度且/或具有高缺陷密度。半導體發光裝置之層的表面粗糙、小結晶粒及所存在之缺陷可使裝置內部發光效率降級，潛在地破壞藉由圖案化基底所產生之任何益處。缺陷一般亦均勻分佈且集中於圖案化特徵部分邊緣附近或自相鄰特徵部分碰撞處之成長，其可引起諸如發光二級體之大面積裝置的漏電問題。

根據本發明之實施例，於一紋理化或圖案化基底上之III族氮化物晶體的成長發生於多個階段。在第一階段中，成長條件有利於形成一符合基底之無空隙且具有平坦平滑表面之層。在第二階段中，自該第一階段中所產生之缺陷被中斷，且材料品質得以改良。然後，額外的層在有利於形成具一定品質之材料的成長條件下得以成長，該材料之品質係適合於半導體發光裝置中之電活性層及光活性層。基底上之圖案係經選擇以便於無空隙地填充圖案並改良光提取。儘管下述實例描述兩個成長階段，但在某些實施例中，可在第一及第二成長階段之後，繼之以類似於下文所述第一或第二成長階段之額外成長階段，以得到所需材料品質。

圖1說明一根據本發明之實施例的裝置。一第一成長區域41成長於一紋理化或圖案化基底40的上方。合適之基底包括(例如)藍寶石及SiC。一第二成長區域47成長於第一成長區域41之上方。然後，包括有一n-類型區域42、一活性區域43及一p-類型區域44之裝置層成長於該第二成長區域

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47上方。p-類型區域44及活性區域43之一部分係經蝕刻掉以曝露出n-類型區域42之一部分。一n-觸點46形成於n-類型區域42之曝露部分上，且一p-觸點45形成於p-類型區域44之剩餘部分上。觸點45及46通常為反射性的。該裝置安裝於一子基板上或觸點朝下之其他結構，使得光可自裝置通過基底40而提取。

圖2說明一形成圖1所示裝置之方法。在步驟20中，提供一紋理化或圖案化基底40。儘管基底40上之紋理係任意的，但該紋理通常為一重複性圖案。圖3A說明一合適圖案之實例。在圖3A所示之圖案中，三角狀凸起區域1係藉由三角狀凹陷區域2而分隔。圖3A所示之柵格對應於一微米。該圖案可藉由(例如)習知掩模及蝕刻步驟而形成，諸如濕式或乾式蝕刻或離子研磨。圖3B說明一合適基底之一部分的橫截面圖，諸如圖3A所示之基底。該圖案之特徵部分通常具有約5微米之長度1且可具有介於約1微米至約10微米之間的長度。該等特徵部分通常具有至少1微米之間距2。該等特徵部分通常具有約0.4微米之高度3且可具有介於約0.1微米至約1微米之間的高度。

在步驟22中，第一成長區域41在有利於填充成長基底上的圖案中之特徵部分的條件下成長，以形成一平滑層。第一成長區域41通常包括一填充成長基底上之圖案的粗糙成長區域(例如，三維成長之晶粒於橫截面上具有峰部及谷部)，繼之以一平滑成長區域(例如，二維成長)。舉例而言，第一成長區域41可包括一厚度介於0.1至1微米之間且

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具有50至175 nm之RMS粗糙度的粗糙成長區域。粗糙成長區域之一般厚度為約0.7微米，RMS粗糙度為約100 nm。該粗糙成長區域繼之以一RMS粗糙度小於20 nm之平滑區域。平滑區域之一般RMS粗糙度為約5 nm。第一成長區域41可於相對高壓、高溫及高的H_2：NH_3比率之條件下形成，以形成一平滑的無空隙層。第一成長區域41可具有一例如介於約10^9 cm^{-2}與10^{10} cm^{-2}之間的高缺陷密度。在某些實施例中，第二成長區域或後續層之成長消除第一成長區域成長期間所存在之缺陷，使得第一成長區域41不會具有較裝置中其他區域大體較高之缺陷密度。第一成長區域41之最小厚度為基底40上圖案特徵部分之高度或約為0.5微米，無論哪個更大。第一成長區域41通常具有約1.5微米的厚度。包括有一粗糙成長區域繼之以一平滑成長區域之合適的第一成長區域之實例包括具有或不具有可選晶粒聚結層之缺陷減少層(defect reduction layer)及具有或不具有可選晶粒聚結層之晶核層，如美國專利第6,630,692號所揭示，該案以引用方式併入本文中，且如下文所述。

在第一成長區域41後，藉由一減少或消除第一成長區域41中之缺陷或至少部分地防止第一成長區域41中之缺陷擴散至裝置區域42、43及44的第二成長區域47而使得材料品質得以改良。第二成長區域47具有一小於第一成長區域41之缺陷密度。類似於第一成長區域41，第二成長區域47可包括一用於改良裝置中材料品質之粗糙成長區域，繼之以一用於提供適合於裝置中後續層成長之表面的平滑成長區

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域。舉例而言，類似於第一成長區域41，第二成長區域可包括一厚度介於0.1與1微米之間且RMS粗糙度介於50與175 nm之間的粗糙成長區域。粗糙成長區域之一般厚度約為0.7微米，RMS粗糙度約為100 nm。粗糙成長區域繼之以一RMS粗糙度小於20 nm之平滑成長區域。平滑區域之一般RMS粗糙度約為5 nm。適用於改良材料品質之第二成長區域47的實例包括Si摻雜層、具有或不具有可選晶粒聚結層之缺陷減少層，及具有或不具有可選晶粒聚結層之晶核層，如美國專利第6,630,692號中所描述。

在第二成長區域47後，n-類型區域42、活性區域43及p-類型區域44成長。一凸台係經蝕刻且形成觸點45及46。

本文所述實施例中之半導體層係藉由MOCVD以三甲基鎵(TMG)或三乙基鎵(TEG)作為鎵源，三甲基鋁(TMAl)作為鋁源、三甲基銦(TMIn)作為銦源、氨(NH_3)作為氮源、矽烷(SiH_4)作為矽源且以氫氣(H_2)或氮氣(N_2)作為載氣之習知單向流MOCVD反應器中成長。亦可使用其他MOCVD反應器、其他源及載氣，及諸如分子束磊晶法(MBE)或氫化物氣相磊晶法(HVPE)之其他成長方法。

在某些實施例中，一或多個低溫GaN晶核層成長於基底40上以覆蓋基底40上之圖案。低溫晶核層(例如)成長至厚度約為20 nm至約50 nm，通常為約25 nm，且其係於約為500℃至約600℃，通常約為550℃之溫度下成長。儘管在此實施例中，低溫晶核層係GaN，但在其他實施例中可使用其他III族氮化物材料。該等晶核層如M. Iwaya等人之日本

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應用物理雜誌(Japanese Journal of Applied Physics) 37,316 (1998)中所描述，其全文以引用方式併入本文中。

在某些實施例中，第一成長區域41包括一缺陷減少層。該缺陷減少層以一般三維粗糙成長而填充基底40上之圖案。缺陷減少層於約900℃至約1175℃，通常約1125℃之溫度條件下在基底40上成長。在缺陷減少層成長期間，NH_3/TMG與NH_3/H_2之分壓比率(更一般而言，V/III與V/H_2，其中V及III代表自元素週期表之V族及III族之元素)係低於彼等維持平滑成長表面形態所要求者之分壓比率，如裝置層42、43及44。在GaN缺陷減少層成長期間之該等分壓比率的範圍及典型值如下文表1之列(a)所列。缺陷減少層在該等條件下成長為厚度約為0.1 μm至約15 μm，通常為約0.5至1 μm。而後停止TMG流，且缺陷減少層可曝露於連續的氫氣及氨氣流中持續約1秒至約1000秒，通常約為一分鐘。H_2及NH_3環境蝕刻缺陷減少層20之表面。該等成長及蝕刻條件有助於形成一包括通常具有約0.1 μm至約1 μm之直徑的個別獨立GaN晶粒或島狀物之粗糙表面。

在粗糙缺陷減少層成長後，III族氮化物材料聚結入平滑層中係所要的。在某些實施例中，缺陷減少層於粗糙成長後展現自然的晶粒聚結狀態。在某些實施例中，可選GaN晶粒聚結層可於約950℃至約1200℃，通常約1160℃之溫度條件下成長於缺陷減少層上。成長溫度及NH_3/TMG與NH_3/H_2分壓比率係經選擇以促進快速橫向(平行於基底表

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面)成長且導致GaN晶粒之晶粒聚結及一平滑磊晶成長表面之形成。在GaN晶粒聚結層成長期間，該等分壓比率之範圍及典型值係如下表1之列(b)中所列。晶粒聚結層具有(例如)約0.5 μm至約20 μm，通常約0.5至1.5 μm之厚度。晶粒聚結層可經矽摻雜至例如約10^{18} cm^{-3}之濃度。

一可選高溫(標準)GaN層可成長於晶粒聚結層上(若存在)，或者成長於缺陷減少層上。標準GaN層於約950℃至約1200℃，通常約1125℃之溫度下成長。標準GaN層成長期間，NH_3/TMG與NH_3/H_2分壓比率之範圍及典型值係如下表1之列(c)所列。該等成長條件係經選擇以促進平滑成長表面形態及高成長速率。標準GaN層具有(例如)約0.1 μm至約10 μm，通常約2 μm之厚度。標準GaN層可不摻雜或經矽之n-類型摻雜至(例如)約10^{18} cm^{-3}或更高之濃度。

缺陷減少層、可選晶粒聚結層及可選高溫GaN層之次序可可多次重複以進一步減少裝置層42、43及44中之缺陷密度。

表1-成長分壓比率

	NH_3/TMG		NH_3/H_2	
層	典型值	範圍	典型值	範圍
a)缺陷減少層	510	200-1500	0.13	0.1-0.3
b)晶粒聚結層	2200	1000-4000*	0.3	≥0.2，通常0.2-0.9
c)標準層	1680	800-4000*	0.5	≥0.35，通常0.35-0.85

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*歸因於緩慢成長速率之實際限制。

在某些實施例中，第二成長區域47包括一類似於上述參考第一成長區域41所描述之缺陷減少層的缺陷減少層。第二成長區域47之缺陷減少層改良材料品質，且可使用或不使用一可選晶粒聚結層及一可選標準III族氮化物層。在第二成長區域47之缺陷減少層成長期間，以及可選晶粒聚結層與可選標準GaN層之成長期間，NH_3/TMG與NH_3/H_2分壓比率之範圍及典型值係如上表1之列(a)-(c)中所列。

在某些實施例中，第二成長區域47包括一Si摻雜層以改良材料品質。該Si摻雜層可為一於約950℃至約1200℃，通常約1160℃之溫度下成長於第一區域41上之高溫GaN層。在該Si摻雜之GaN層成長期間，NH_3/TMG與NH_3/H_2分壓比率之範圍及典型值可與上表1中列(b)及(c)中所列之彼等用於標準GaN層或晶粒聚結層之範圍及典型值大體上相同。該等成長條件係經選擇以促進平滑成長表面形態。Si摻雜層可經矽之n-類型摻雜至例如約10^{18} cm^{-3}或更高之濃度。

Si摻雜層之形成係如下所述：首先一GaN層成長至厚度為(例如)約0.1 μm至約10 μm，通常約1 μm。而後，停止TMG流且將GaN層曝露於SiH_4或Si_2H_6以將約0.1個單層至約3個單層，通常為約一個單層的矽沈積至該層之表面。所沈積之矽可與層28中之氮反應形成覆蓋該層之部分表面的微遮罩(micro mask)(島狀物)。當III族氮化物隨後在該表面上重新開始成長時，III族氮化物材料於該表面之未覆

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蓋部分上成核，垂直地成長，且而後在該遮罩上方橫向成長以形成一低缺陷密度層。在某些實施例中，成長條件及所輸送之矽的量未產生微遮罩，但足以導致類似於第一區域41之缺陷減少層的粗糙成長。

一可選晶粒聚結層可在大體類似於彼等上述條件的條件下成長於Si摻雜之遮罩的上方。一包括Si摻雜GaN層及可選晶粒聚結層之次序可在第一成長區域41上方重複多次以進一步降低裝置區域42、43及44中之缺陷密度。

儘管在上述實例中，第二成長區域47之層係由GaN形成，然而，在其他實施例中，該等層可由其他III族氮化物材料形成，諸如，InGaN、AlGaN、AlInGaN、AlInGaNAs、AlInGaNP或其組合。類似於上述實例之缺陷減少結構在S. Tanaka等人之日本應用物理雜誌(Japanese Journal of Applied Physics) 39, L831 (2000)中得以描述，其全文以引用方式併入本文中。諸如上述實施例中所使用之微遮罩技術在此技術中可稱為"矽摻雜"或抗界面活性劑方法。

在某些實施例中，第二成長區域47包括一用於改良材料品質之晶核層。一適用於第二成長區域47之晶核層係如上文參考第一成長區域41所述。

圖4係一較大接合裝置之平面圖(意即，面積大於或等於一平方毫米)。圖5係圖4所示裝置沿軸70方向之橫截面圖。圖4及圖5說明可用於如圖1-3與附文中所示及所述任何磊晶結構之觸點的排列。磊晶結構59包括圖1之區域

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41、47、42、43及44。磊晶結構59之活性區域係藉由形成有n-觸點46之三個渠溝而分隔成四個區域。各區域係藉由形成於p-觸點45上之四個p-子基板連接件54而連接至一子基板。n-觸點46環繞該等四個活性區域。n-觸點46藉由六個n-子基板連接件53而連接至一子基板。n-及p-觸點可藉由一絕緣層52而電隔絕。

圖6係一封裝發光裝置之分解圖。一散熱片100置於一嵌入模製導線框架106內。該嵌入模製導線框架106係(例如)一經填充之塑料材料成型於提供一電學路徑之金屬框架的周圍。散熱片100可包括一可選反射碗102。發光裝置晶粒104，其可為任何上述裝置，係直接安裝或經由一熱傳導子基板103間接安裝至散熱片100上。可添加一可為光學透鏡之保護蓋108。

儘管已詳細描述本發明，但彼等熟習此項技術者應瞭解，對於本發明而言可進行不脫離本文所述之發明概念之精神的修改。因此，本發明之範疇不應限定於所說明及描述之特定實施例。

【圖式簡單說明】

圖1說明一根據本發明之實施例的III族氮化物發光裝置。

圖2說明一形成圖1之裝置的方法。

圖3A說明一形成於圖1之基底40的表面上之圖案的實例。

圖3B為基底40之一部分的橫截面圖。

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圖4及圖5為圖1所示觸點排列之平面圖及橫截面圖。

圖6為一封裝發光裝置之分解圖。

【主要元件符號說明】

1	三角狀凸起區域
2	三角狀凹陷區域
40	紋理化或圖案化基底
41	第一成長區域
42	n-類型區域
43	活性區域
44	p-類型區域
45	p-觸點
46	n-觸點
47	第二成長區域
52	絕緣層
53	n-子基板連接件
54	p-子基板連接件
59	磊晶結構
70	軸
100	散熱片
102	可選反射碗
103	熱傳導子基板
104	發光裝置晶粒
106	嵌入模製導線框架
108	保護蓋

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五、中文發明摘要：

本發明係揭示一種III族氮化物發光裝置，其係成長於一紋理基底上，以降低該基底與該III族氮化物層之間的界面處之全內反射的量。在某些實施例中，該裝置包括一大體上無空隙之第一成長區域，及一第二成長區域，該第二成長區域用於改良材料品質，使得高品質層可成長於該第一與第二區域的上方。

六、英文發明摘要：

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19.08.2005

ABSTRACT:

A III-nitride light emitting device is grown on a textured substrate, in order to reduce the amount of total internal reflection at the interface between the substrate and the III-nitride layers. In some embodiments, the device includes a first growth region substantially free of voids, and a second growth region that improves the material quality such that high quality layers can be grown over the first and second regions.

Fig. 1

案號：(048)	國外相應案：☑見申請書 ☐其他：		
中說份數：(	☐改中文 Title	☐細則§17 但書	字數：
☑原文說明書檔名：p:\Foreign Spec\ -filing			存檔人：
譯者：	審稿者：	代表圖：	化學式：

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十、申請專利範圍：

1. 一種結構，其包括：

一紋理基底；

一置於該基底之該紋理表面上的第一III族氮化物區域，該第一III族氮化物區域大體上無空隙；

一置於該第一III族氮化物區域上之第二III族氮化物區域，該第二III族氮化物區域具有一小於該第一III族氮化物區域之平均缺陷密度的平均缺陷密度；及

一置於一n-類型區域與一p-類型區域之間的發光區域，該發光區域覆蓋於該第二III族氮化物區域上。

2. 如請求項1之結構，其中該第一III族氮化物區域具有一大於$10^9 cm^{-2}$之缺陷密度。

3. 如請求項1之結構，其中該第一III族氮化物區域具有一介於0.5微米與10微米之間的厚度。

4. 如請求項1之結構，其中該第一III族氮化物區域包含：

一厚度介於0.1微米與15微米之間的缺陷減少層；及

一厚度介於0.4微米與20微米之間的晶粒聚結層；

其中，該晶粒聚結層之一表面比該缺陷減少層之一表面更平滑。

5. 如請求項4之結構，其中：

該缺陷減少層具有一介於0.5微米與1微米之間的厚度；及

該晶粒聚結層具有一介於0.5微米與1.5微米之間的厚度。

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6. 如請求項1之結構，其中該第二III族氮化物區域包含一矽摻雜區域。

7. 如請求項6之結構，其中該矽摻雜區域包含：

一厚度介於0.1微米與1微米之間的GaN層；及

一厚度介於0.1個單層與3個單層之間的矽層。

8. 如請求項1之結構，其中該第二III族氮化物區域包含：

一厚度介於0.1微米與15微米之間的缺陷減少層；及

一厚度介於0.4微米與20微米之間的晶粒聚結層；

其中，該晶粒聚結層之一表面比該缺陷減少層之一表面更平滑。

9. 如請求項8之結構，其中：

該缺陷減少層具有一介於0.5微米與1微米之間的厚度；及

該晶粒聚結層具有一介於0.5微米與1.5微米之間的厚度。

10. 如請求項1之結構，其進一步包含：

一電連接至該n-類型區域之n-觸點；及

一電連接至該p-類型區域之p-觸點。

11. 如請求項10之結構，其進一步包含：

電連接至該等n-及p-觸點之導線；及

一置於該發光區域上方之保護蓋。

12. 如請求項1之結構，其中：

該基底上之該紋理包含一重複特徵部分之圖案；

該等特徵部分具有一至少為1微米之長度；及

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該等特徵部分具有一介於0.1微米與1微米之間的高度。

13. 如請求項12之結構，其中該圖案具有一包含一峰部及一谷部之橫截面。

14. 如請求項12之結構，其中該等特徵部分具有至少1微米之間隔。

15. 一種結構，其包含：

一紋理基底；

一置於該基底之該紋理表面上的第一III族氮化物區域，該第一III族氮化物區域大體上無空隙，該第一III族氮化物區域包含一與該基底相鄰之第一部分及一第二部分；其中該第二部分之RMS粗糙度小於該第一部分之RMS粗糙度；

一置於該第一III族氮化物區域上之第二III族氮化物區域，該第二III族氮化物區域包含一與該第一III族氮化物區域相鄰之第一部分及一第二部分；其中該第二部分之RMS粗糙度小於該第一部分之RMS粗糙度；及

一置於一n-類型區域與一p-類型區域之間的發光區域，該發光區域覆蓋於該第二III族氮化物區域上。

16. 如請求項15之結構，其中：

該第一區域之該第一部分具有一介於50 nm與175 nm之間的RMS粗糙度；及

該第一區域之該第二部分具有一小於20 nm之RMS粗糙度。

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17. 如請求項15之結構，其中：

該第二區域之該第一部分具有一介於50 nm與175 nm之間的RMS粗糙度；及

該第二區域之該第二部分具有一小於20 nm之粗糙度。

18. 如請求項15之結構，其中該第二III族氮化物區域之該第一部分包含一矽摻雜區域。

19. 如請求項18之結構，其中該矽摻雜區域包含：

一厚度介於0.1微米與1微米之間的GaN層；及

一厚度介於0.1個單層與3個單層之間的矽層。

20. 如請求項15之結構，其中：

該第一區域之該第一部分包含一厚度介於0.1微米與15微米之間的缺陷減少層；及

該第一區域之該第二部分包含一厚度介於0.4微米與20微米之間的晶粒聚結層；

其中，該晶粒聚結層之一表面比該缺陷減少層之一表面更平滑。

21. 如請求項20之結構，其中：

該缺陷減少層具有一介於0.5微米與1微米之間的厚度；及

該晶粒聚結層具有一介於0.5微米與1.5微米之間的厚度。

22. 如請求項15之結構，其進一步包含：

一電連接至該n-類型區域之n-觸點；

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一電連接至該p-類型區域之p-觸點。

23. 如請求項22之結構，其進一步包含：

電連接至該等n-及p-觸點之導線；及

一置於該發光區域上方之保護蓋。

24. 如請求項15之結構，其中：

該基底上之該紋理包含一重複特徵部分之圖案；

該等特徵部分具有一至少1微米之長度；及

該等特徵部分具有一介於0.1微米與1微米之間的高度。

25. 一種製造一半導體發光裝置之方法，該方法包含：

提供一紋理成長基底；

將一第一III族氮化物區域成長於該成長基底上方，其中適於成長該第一III族氮化物區域之成長條件係經選擇以填充該紋理成長基底上之特徵部分，使得該第一III族氮化物區域大體上無空隙；及

將一第二III族氮化物區域成長於該第一III族氮化物區域上方，該第二III族氮化物區域包含一與該第一III族氮化物區域相鄰之第一部分及一第二部分；

其中，該第一區域之該第二部分成長期間的一V族來源之分壓係大於該第一區域之該第一部分成長期間的V族來源之分壓。

26. 如請求項25之方法，其中該第二區域之該第二部分成長期間之一V族來源之分壓係大於該第二區域之該第一部分成長期間的V族來源之分壓。

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27. 如請求項25之方法，其中成長該第二III族氮化物區域之該第一部分包含：

成長一第一GaN層；及

將該第一GaN層之表面曝露於一Si源。

28. 如請求項27之方法，其中將該第一GaN層之一表面曝露於一Si源包含將0.1至3個單層Si沈積至該第一GaN層之該表面上。

29. 一種製造一半導體發光裝置之方法，該方法包含：

提供一紋理成長基底；

將一第一III族氮化物區域成長於該成長基底上方，其中適於成長該第一III族氮化物區域之成長條件係經選擇以填充該紋理成長基底上之特徵部分，使得該第一III族氮化物區域大體上無空隙；及

將一第二III族氮化物區域成長於該第一III族氮化物區域上方，該第二III族氮化物區域包含一與該第一III族氮化物區域相鄰之第一部分及一第二部分；

其中，該第一區域之該第二部分成長期間之一成長溫度係高於該第一區域之該第一部分成長期間之成長溫度。

30. 如請求項29之方法，其中該第二區域之該第二部分成長期間之一成長溫度係高於該第二區域之該第一部分成長期間之成長溫度。

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十一、圖式：

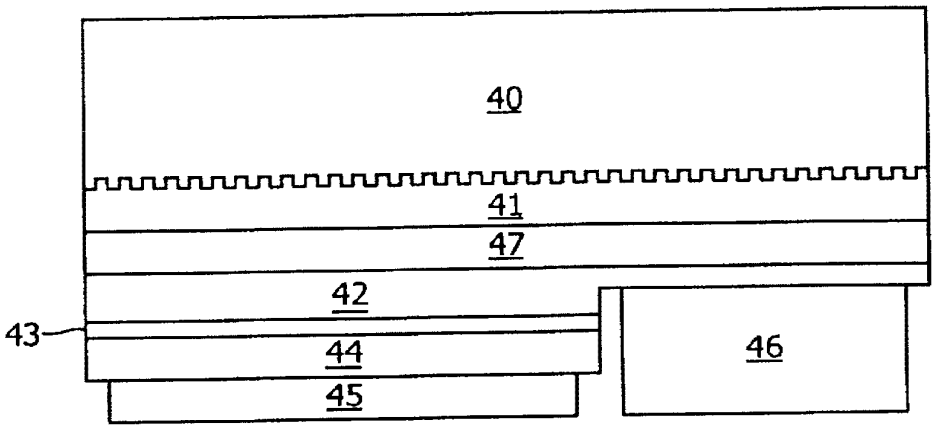


圖 1

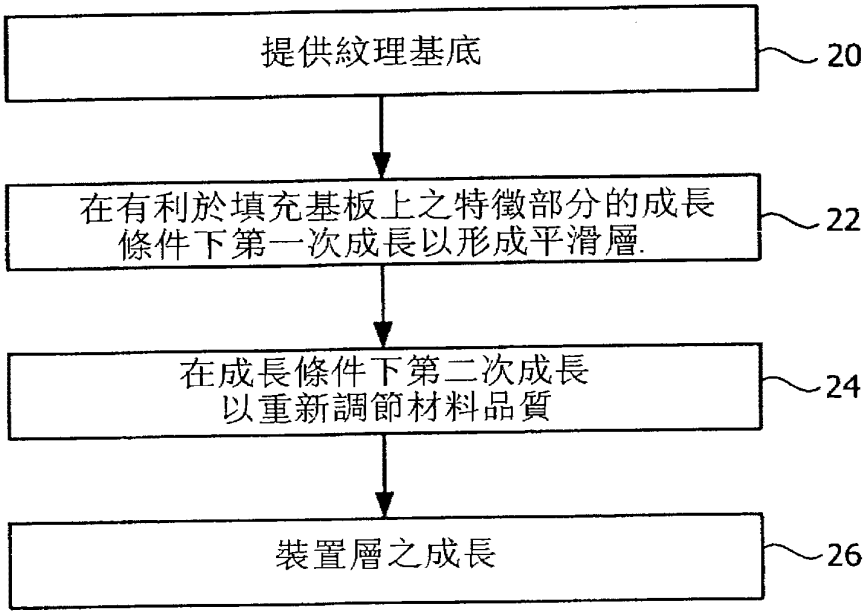


圖 2

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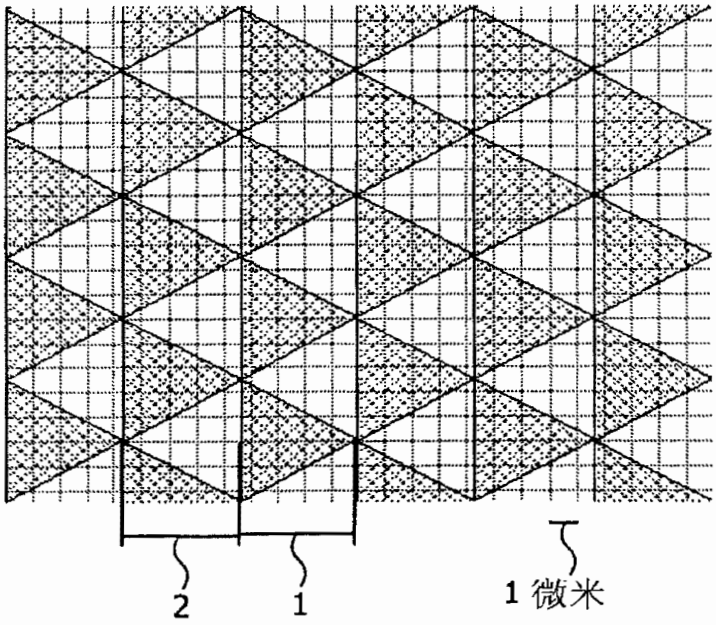


圖 3A

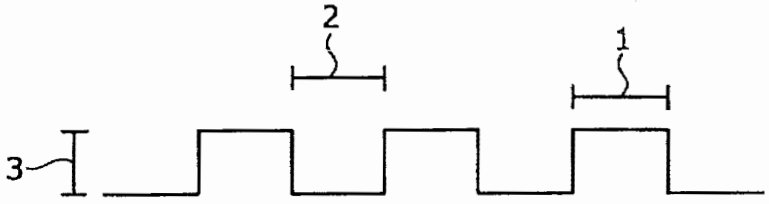


圖 3B

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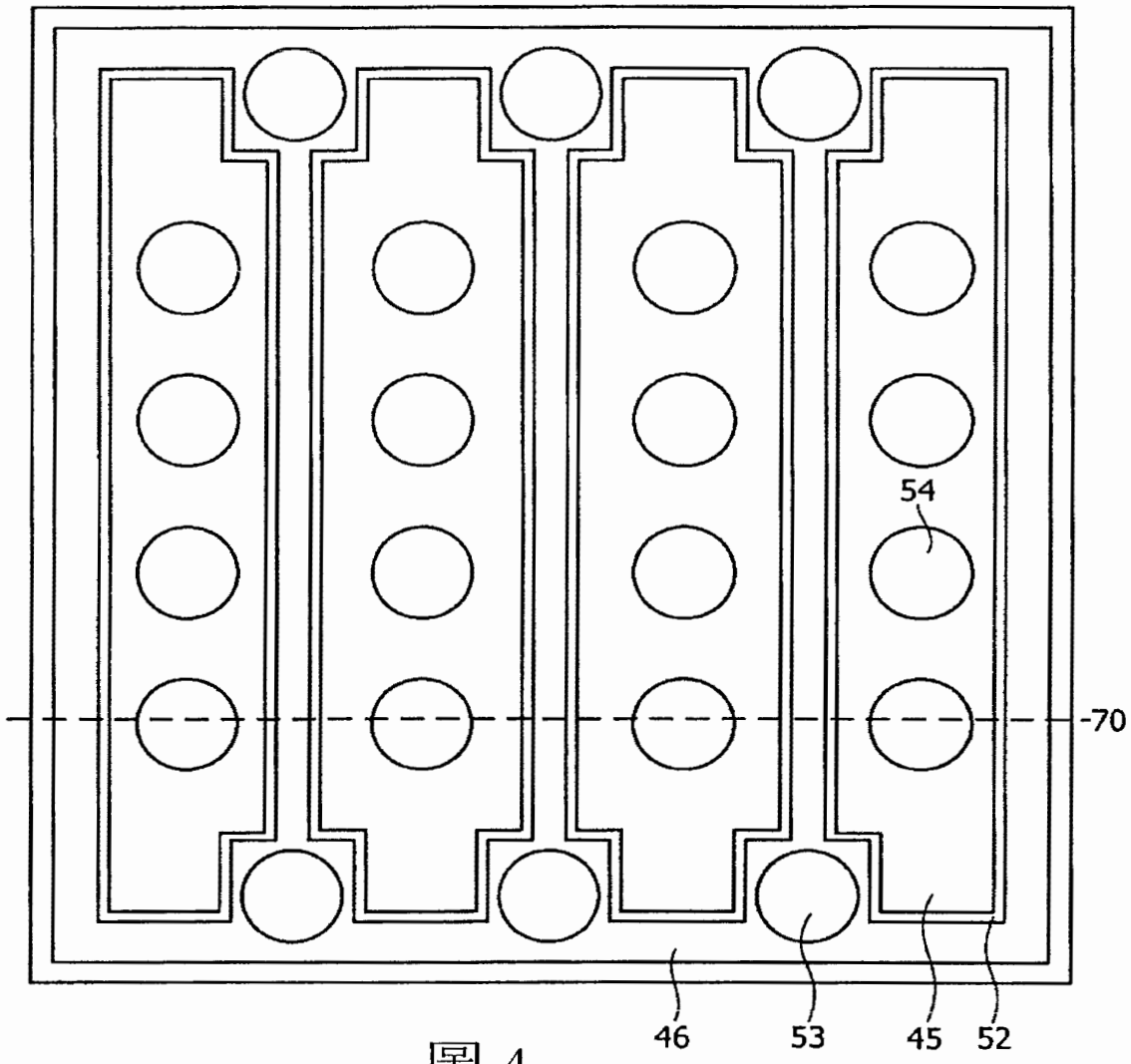


圖 4

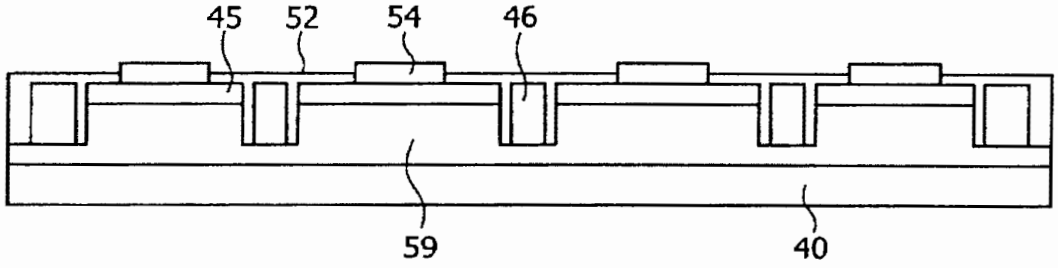


圖 5

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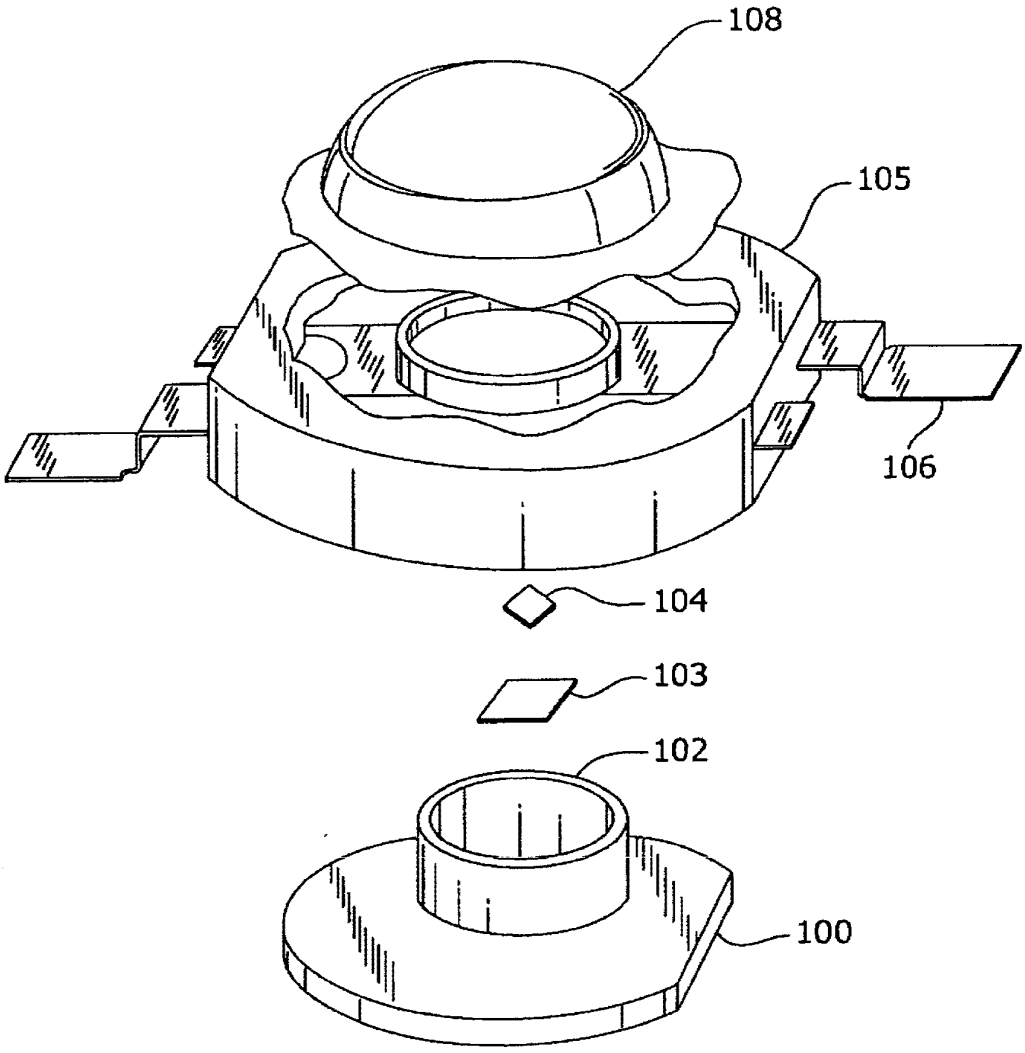


圖 6

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七、指定代表圖：

(一)本案指定代表圖為：第（ 1 ）圖。

(二)本代表圖之元件符號簡單說明：

40	紋理化或圖案化基底
41	第一成長區域
42	n-類型區域
43	活性區域
44	p-類型區域
45	p-觸點
46	n-觸點
47	第二成長區域

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

(無)

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Espacenet

Bibliographic data: TW200818529 (A) — 2008-04-16

Thin-film diode structure using a sacrificial doped dielectric layer

Inventor(s): WIDENBORG PER INGEMAR [SE]; ABERLE ARMIN GERHARD [DE] ± (WIDENBORG, PER INGEMAR, ; ABERLE, ARMIN GERHARD)

Applicant(s): NEWSOUTH INNOVATIONS PTY LTD [AU] ± (NEWSOUTH INNOVATIONS PTY LTD)

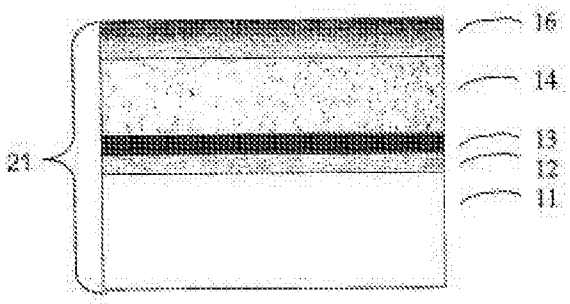
Classification: - international:***H01L31/042***
- cooperative: **H01L29/66113**; **H01L29/868**; **H01L31/0392**; **H01L31/077**; **H01L31/1872**; H01L21/02532; H01L21/02672; H01L21/268; Y02E10/50; Y02P70/521

Application number: TW20070131647 20070827

Priority number (s): AU20060904759 20060831

Also published as: WO2008025057 (A1)

Abstract of TW200818529 (A)



A method of fabricating a thin-film crystalline semiconductor 3-layer diode structure on a foreign supporting substrate or superstrate, and a thin-film crystalline semiconductor 3-layer diode structure on a foreign supporting substrate or superstrate are disclosed. A sacrificial dielectric overlayer (15) containing n or p-type dopant atoms is deposited on an exposed amorphous lightly doped or undoped semiconductor layer of a 2-layer semiconductor structure (13, 14) formed on the substrate or superstrate (11). The amorphous lightly doped or undoped semiconductor layer (13, 14) is crystalised. A heavily doped semiconductor layer is formed by diffusing the n or p-type atoms from the sacrificial dielectric overlayer into a portion of the crystallized lightly doped or

undoped semiconductor layer, whereby the 3-layer diode structure (21) is formed. The sacrificial dielectric overlayer (15) is removed from the 3-layer diode structure.

200818529

發明專利說明書

（本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫）

※ 申請案號：96131607

※ 申請日期：96.8.27　　※IPC 分類：H01L 31/042(2006.01)

一、發明名稱：（中文/英文）

使用一犧牲摻雜介電層之薄膜二極體結構

THIN-FILM DIODE STRUCTURE USING A SACRIFICIAL DOPED DIELECTRIC LAYER

二、申請人：（共 1 人）

姓名或名稱：（中文/英文）

新南革新股份有限公司 / NEWSOUTH INNOVATIONS PTY LTD

代表人：（中文/英文）

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國　籍：（中文/英文）

澳洲 / AUSTRALIA

三、發明人：（共 2 人）

姓　名：（中文/英文）

1. 溫登伯格　伯爾 I. / WIDENBORG, PER INGEMAR
2. 艾伯里　阿銘 G. / ABERLE, ARMIN GERHARD

國　籍：（中文/英文）

1. 瑞典 / SWEDEN
2. 德國 / GERMANY

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四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其事實發生日期為：。

☑ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號　順序註記】

☑ 有主張專利法第二十七條第一項國際優先權：

1. 澳洲、　2006/08/31、　2006904759

☐ 無主張專利法第二十七條第一項國際優先權：

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號　順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料　【格式請依：寄存機構、日期、號碼　順序註記】

國外生物材料　【格式請依：寄存國家、機構、日期、號碼　順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

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九、發明說明：

【發明所屬之技術領域】

發明領域

本發明廣泛有關於一製造一薄膜晶性半導體3層二極體結構於一外異支撐基材或覆材上之方法，且有關一薄膜晶性半導體3層二極體結構。

【先前技術】

發明背景

諸如玻璃等外異支撐材料上之薄膜晶性半導體裝置結構在譬如薄膜太陽能電池及平板顯示器等電子業中變得日益重要。太陽能電池的案例中，由於其相較於傳統、以矽晶圓為基礎的模組只需要一比例部分的半導體材料之事實，薄膜有潛力鉅幅降低太陽能模組的製造成本。尚且，薄膜太陽能電池具有可以在一大面積支撐材料(-1 m^2)上予以製造之優點，使得製程流線化且進一步降低加工成本。

一晶性半導體二極體通常為結構$n^+\pi p^+$或$p^+\pi n^+$的一3層裝置，其中上標"+"代表重度摻雜而π為p(對於輕度p-型摻雜)、n(對於輕度n-型摻雜)或i(對於本徵性，亦即未摻雜材料)。兩表面層的重度摻雜係容許形成低電阻歐姆接觸部且亦有利於降低二極體中之載體重組率(carrier recombination rate)。

由於透明度及低成本，玻璃是電子件中一種特別重要的支撐外異材料，而能夠具有譬如以液晶為基礎的平板顯示器及覆材組態中的薄膜太陽能模組(亦即，日光經由玻璃

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片進入太陽能電池)。然而，由於玻璃的有限穩定度，使裝置品質晶性半導體材料形成於玻璃上係構成一種可觀的挑戰。

至今發展出的低溫多晶矽太陽能電池之最成功方法之一係為松山等人的“部份摻雜方法”[一固相結晶化方法所製備之高品質多晶矽薄膜]，非晶性固體期刊，Vol. 198-200，pp.940-944 (1966)，其中一2層堆積體的非晶矽材料(1至20微米範圍中的厚度)藉由固相結晶化(SPC)以約600℃在數小時期間產生結晶化。若2層非晶性堆積體由一薄、重度n-型(磷) 摻雜層及一遠為較厚、未摻雜或輕度摻雜層所構成，可藉由SPC獲得優良品質的晶矽材料。此方法所產生的優良材料品質之理由係在於整體堆積體的方向性結晶化，開始係為n^+摻雜層(“長晶”層)且隨後進展經過結構的其餘部分(“結晶化層”)。松山等人已經顯示，一重度磷摻雜非晶矽層係遠比輕度摻雜(未摻雜)矽層更為快速地結晶，且因此作為一n*n(或n*i)結構中之優良長晶層。為了以SPC製的n*n結構實現一二極體結構，松山等人以低溫將一重度p+摻雜氫化非晶矽層沉積在結構上，提供一由晶性及非晶性矽所構成之異質接合二極體。標準測試條件下的測量係顯露出，此等低溫製造的異質接合二極體展現出金屬基材上高於9%良好的太陽能電池效率，具有約10微米之吸收器區(“基底”)中的少數載體擴散長度。

雖然松山等人獲得的效率對於一外異基材上的一薄膜晶矽太陽能電池係為合理，缺點係在於形成重度p^+摻雜氫

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化非晶矽需要一分離的半導體沉積步驟(其中因此n或i-型矽層的表面需以小心且可能昂貴的方式來清潔)並由於非晶矽的低側向電導無法藉由簡單放下一金屬格柵而不需要額外沉積具有低薄片電阻(<1000 Ω/平方)的透明傳導性氧化物(TCO)來實現p^+非晶矽層之接觸，故顯著地增添裝置的製造成本。

巴梭爾(Basore)[玻璃模組上的晶矽之簡化加工及改良的效率，第19屆歐洲光伏太陽能會議的會議紀錄，巴黎，2004六月，pp. 455-458(WIP,慕尼黑,2004)]已經建議另一種用於在一外異基材上實現一薄膜晶矽二極體結構之方法。一n^+pp^+堆積體的非晶矽沉積在一玻璃基材上且隨後整體3層堆積體藉由SPC以約600℃在數個小時期間產生結晶化。並且，n^+層之用途係作為長晶層且因此提供整體非晶性堆積體的方向性結晶化。此途徑的利益係為一較流線化、且因此很可能更合乎成本效益之製程。然而，由於表面處出現重度p-摻雜(硼)層，長晶不只開始於埋設n^+層中且亦在p^+層中。因此，整體堆積體的結晶化係從兩側發生，導致相較於三洋方法(Sanyo method)之顯著降低的顆粒尺寸及顯著較大的瑕疵密度。

因此需要提供企圖解決至少一上述缺點之一用於實現一薄膜晶矽二極體結構之方法。

【發明內容】

發明概要

根據本發明的第一態樣，提供一用於製造一薄膜晶性

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半導體3層二極體結構於一外異支撐基材或覆材上之方法，該方法包含將一含有n或p-型摻雜物原子的一犧牲介電覆層沉積在基材或覆材上所形成的一2層半導體結構之一經曝露的非晶性輕度摻雜或未摻雜半導體層上；將非晶性輕度摻雜或未摻雜半導體層結晶化；藉由將來自犧牲介電覆層的n或p-型原子擴散至結晶化輕度摻雜或未摻雜半導體層的一部分內來形成一重度摻雜半導體層，其中因此形成3層二極體結構；及從3層二極體結構移除犧牲介電覆層。

2層半導體結構可包含非晶性輕度摻雜或未摻雜半導體層及一非晶性重度摻雜經埋設半導體層，且用於將非晶性輕度摻雜或未摻雜半導體層結晶化之步驟包含經由固相結晶化將重度摻雜經埋設半導體層結晶化。

可以約500至650℃範圍中的溫度在約6至48小時的期間進行固相結晶化。

該方法可進一步包含藉由形成一晶性半導體籽晶層於基材或覆材上、製備一氫終止式籽晶層表面於晶性半導體籽晶層上、及將輕度摻雜或未摻雜非晶性層沉積在籽晶層表面上來形成2層半導體結構，且用於將非晶性輕度摻雜或未摻雜半導體層結晶化之步驟係包含固相磊晶。

晶性半導體籽晶層可以相較於重度摻雜半導體層呈相反類型的一極性被重度摻雜。

晶性半導體籽晶層可能未經摻雜或以與重度摻雜半導體層相同的極性被摻雜，且形成2層半導體結構係包含將一非晶性半導體膜沉積在籽晶層表面上以使與晶性半導體籽

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晶層相鄰之非晶性半導體膜的一第一部分以相較於重度摻雜半導體層呈相反類型的一極性被重度摻雜，且使非晶性半導體膜的一第二部分身為非晶性輕度摻雜或未摻雜半導體層，且形成重度摻雜半導體層之步驟進一步包含使來自非晶性半導體膜的第一部分之摻雜物原子擴散至晶性半導體籽晶層內以形成3層半導體結構之一重度摻雜經埋設半導體層。

可以約500至650℃範圍中的溫度在約6至48小時期間進行固相磊晶。

籽晶層可以選自由下列各物所組成的群組之一方法製造：鋁引發式結晶化，金屬引發式結晶化，固相結晶化或雷射引發式結晶化。

該方法可包含形成一介電障壁層於基材或覆材上，及形成3層二極體結構於介電障壁層上。

介電障壁層可包含選自由下列各物所組成的群組之一材料：氮化矽，氧化矽，碳化矽及其一合金或一組合。

3層二極體結構可包含選自由下列各物所組成的群組之一材料：矽，鍺，或矽及鍺的一合金。

犧牲介電覆層可選自由下列各物所組成的群組：氮化矽，氧化矽，碳化矽及其一合金或一組合。

犧牲介電覆層可利用選自由下列各物所組成的群組之一方法作沉積：PECVD，濺鍍及蒸鍍。

可以約1秒至15分鐘範圍中的期間利用約800至1050℃範圍中的一溫度所進行之快速熱退火來擴散來自犧牲介電

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覆層的n或p-型原子藉以形成重度摻雜半導體層。

該方法可進一步包含以約350至650℃範圍中的一溫度在移除犧牲介電覆層之後使3層二極體結構曝露於原子性氫。

犧牲介電覆層可在形成輕度摻雜或未摻雜非晶性半導體結構的最後步驟之後作原位沉積而不破壞真空。

輕度摻雜或未摻雜半導體層的摻雜可低於約$10^{18}cm^{-3}$，且重度摻雜經埋設半導體層的摻雜大於約$10^{18}cm^{-3}$。

一其上可支撐3層半導體結構之表面係可被紋理化以輔助光困陷在3層半導體結構中。

根據本發明的第二態樣，提供利用如第一態樣中所界定的一方法形成於一外異支撐基材或覆材上之一薄膜晶性半導體3層二極體結構。

圖式簡單說明

一般熟習該技術者瞭解將連同圖式僅藉由範例從下文描述容易地得知且更加瞭解本發明的實施例，其中:

第1至5圖為顯示利用固相結晶化(SPC)之裝置的製造之示意橫剖視圖；

第6至10圖為顯示利用固相磊晶(SPE)之裝置的製造之示意橫剖視圖。

【實施方式】

較佳實施例之詳細說明

一所描述方法係使用一非晶性$n^+\pi$(或$p^+\pi$) 2層結構上之

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一犧牲摻雜介電覆層，其具有以約600℃藉由SPC之非晶性2層堆積體的一後續結晶化。利用約800至1050℃範圍中的高溫之一分離的快速熱退火(RTA)期間從經摻雜覆層至下方晶矽層內之摻雜物擴散藉以產生$n^+\pi p^+$(或$p^+\pi n^+$)薄膜晶性二極體結構的第三、重度摻雜層。RTA之後係為約500至620℃範圍中利用原子性氫之一瑕疵鈍化處理，其中因此在氫化處理之前以一氫氟酸沾浸來移除經摻雜覆層(經摻雜氧化矽)。第三層中之摻雜物的一大比例部分在氫化處理之後係為電子主動性。

另一所描述方法中，單層的π-型(亦即，輕度摻雜或未摻雜)非晶矽係沉積至一玻璃片上的一氫終止式重度摻雜晶矽籽晶層上，接著係為犧牲摻雜介電覆層之沉積。由於出現晶性籽晶層(其提供長晶表面)，在此例中經由固相磊晶(SPC)發生非晶矽層的結晶化。對於非晶矽層的SPE之詳細描述請參照威登柏格(Widenborg)等人的[藉由固相磊晶之玻璃上的AIC多晶矽籽晶層之磊晶加厚，結晶生長期刊，Vol.276，pp.19-28 (2005)]，其內容合併於本文中以供參考。再度利用約800至1050℃範圍中的高溫之一快速熱退火(RTA)期間從犧牲摻雜覆層至下方晶矽層內之摻雜物擴散藉以生成所需要的第三、重度摻雜層。在約500至620℃範圍中以原子性氫的一處理之前以一氫氟酸沾浸來移除犧牲摻雜覆層(經摻雜氧化矽)。第三層中之摻雜物的一大比例部分在氫化處理之後係為電子主動性。

現在將參照第1至5圖來描述利用SPC之裝置的製造。

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一薄介電障壁層12沉積在一外異支撐材料11上，如第1圖所示。應注意外異支撐材料11可被適當地紋理化以輔助光困陷在經光製3層半導體結構中。為求清楚起見，第1至5圖中已經省略紋理。介電障壁層12包含一介電材料諸如氮化矽，氧化矽，碳化矽或者這些材料的一合金或一組合。譬如，在玻璃覆材的案例中，可利用矽烷、氨及氮的一氣體混合物藉由電漿增強化學氣相沉積(PECVD)方法來沉積一具有約70 nm厚度之SiN膜。接著，非晶性半導體材料之一2層堆積體(13，14)沉積在薄介電層12上，其中第一層13被重度摻雜而第二層14被輕度摻雜或為本徵性，如第2圖所示。層13及14可包含非晶性半導體材料諸如矽，鍺或矽及鍺的一合金。譬如，可以約375至425℃範圍中的一沉積溫度利用矽烷及經摻雜氫的一氣體混合物藉由PECVD方法來沉積非晶矽，其中第一層13在約$1x10^{18}$至$1x10^{21}cm^{-3}$磷原子範圍中被重度摻雜，其具有約$1x10^{20}cm^{-3}$的較佳磷濃度及約50 nm的較佳厚度。第二層14可在約$1x10^{15}$至$1x10^{18}cm^{-3}$範圍中藉由硼被輕度p-型摻雜，其具有約$5x10^{16}$的較佳硼濃度及約1500 nm的較佳厚度。

一薄摻雜介電層15隨後沉積在非晶性半導體層14上，如第3圖所示。介電層15可包含一介電材料，諸如氮化矽，氧化矽，碳化矽或者這些材料的一合金或一組合。介電層15可利用諸如電漿增強式化學氣相沉積(PECVD)、濺鍍或蒸鍍等沉積技術作沉積。一範例中，具有約70 nm厚度之介電層15係包含一含有痕量的碳之經硼摻雜(p-型)氧化矽，其

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在300至350℃基材溫度、一標準平行板組態中經由射頻(13.56 MHz) PECVD (RF PECVD)作沉積。一範例所使用之氣體混合物係由下列所組成(括弧中的氣流): 矽烷(約1 sccm)，氫(約2 sccm)中的0.5%三甲硼，一氧化二氮(約150 sccm)，及氮(約150 sccm)。沉積壓力約為150毫托耳(mTorr)且功率密度約為0.025 W/cm^2。所產生的沉積速率約為10 nm/min。一範例中，介電層15在非晶性半導體沉積步驟(相較第2圖)之後作原位沉積而不破壞一真空沉積室中的真空。

裝置20隨後受到一熱退火，其中非晶性半導體層13及14經由SPC產生結晶化且其中經曝露薄介電層15中的摻雜原子未顯著地擴散至半導體層13及14內。一範例中，在約500至650℃範圍中的溫度以約6至48小時期間進行結晶化。所描述範例中，此熱退火步驟在一氮清除式大氣壓爐具中進行。

接著係使裝置20受到處於高溫的一快速熱退火(RTA)處理，其中因此使經曝露薄介電層15中的摻雜原子顯著地擴散至晶性半導體層14內且因此生成一位於層15與14之間的第三摻雜層16，如第4圖所示。一範例中，RTA在約800至1050℃的一溫度範圍中進行位於約1秒至15分鐘範圍中之一段期間。

隨後，薄摻雜介電層15被移除且裝置21受到一原子性氫處理，如第5圖所示。一範例中，在約350至650℃範圍中的一溫度進行對於原子性氫的曝露。

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已經藉由PECVD(電漿增強式化學氣相沉積)製造利用參照上文第1至5圖所述的方法製成之數個1.5微米厚矽太陽能電池裝置，其中利用一硼矽酸玻璃片11，一氮化矽層12，一重度磷摻雜非晶性Si:H層13，一輕度硼摻雜非晶性Si:H層14，及一原位沉積於基底層14上之重度硼摻雜矽(碳)氧化物層15。非晶矽層13及14隨後以約600℃在約15小時期間產生結晶化。裝置隨後在約900℃以5分鐘受到一RTA處理，在該期間藉由摻雜物擴散生成第三、重度摻雜層16。隨後藉由在氫氟酸中蝕刻來移除犧牲硼摻雜矽(碳)氧化物層15，接著是約610℃玻璃溫度歷時約15分鐘時程之一氫化製程。

所產生的p^+層(層16)被硼重度摻雜，如同低達1000歐姆/平方之所測得的薄片電阻及用於決定摻雜極性之熱探針測量所確認。製成的p-n接面太陽能電池之電性特徵化係顯示，用於形成重度摻雜背表面層(背表面場(BSF)層)之所描述的犧牲摻雜介電覆層方法相較於習知生長的BSF層之裝置而言具有較優品質。具有所描述經擴散BSF層之太陽能電池及一其中唯一差異在於一習知生長的BSF層之均等裝置之開路電壓差係為一顯著的40至50 mV，其中對於所描述經擴散BSF層具有一較高電壓。具有經由犧牲摻雜介電覆層方法所形成的所描述BSF層之太陽能電池係具有高於500 mV之一1-太陽開路電壓(1-sun open circuit voltage)且胞元受到寄生理想性因數n=2重組之可忽略的影響，潛在能夠具有極高的充填因數(且因此具有高的太陽能轉換效率)。一具有一

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經擴散BSF層之金屬化太陽能電池係獲得超過70%的一充填因數，其為對於玻璃上的多晶矽太陽能電池之優良數值。

現在將參照第6至10圖來描述利用SPE之裝置的製造。

一薄介電障壁層112沉積在一外異支撐材料111上且一薄、大顆粒狀重度摻雜($>10^{18}cm^{-3}$)晶性半導體層117形成於層112上，如第6圖所示。應注意外異支撐材料112可被適當地紋理化以輔助光困陷於經光製3層半導體結構中。為求清楚起見，第6至10圖中已經省略紋理。熟習該技術者將瞭解，一薄(<<1微米)晶性半導體層形成於一外異基材上係遠比使用既有沉積技術之一厚(>1微米)晶性層的形成更為容易。確切言之，可利用諸如鋁引發式結晶化、金屬引發式結晶化、固相結晶化、或雷射引發式結晶化等技術來製造晶性半導體層或籽晶層117。介電障壁層112包含一介電材料諸如氮化矽，氧化矽，碳化矽或這些材料的一合金或一組合。譬如，可使用矽烷、氨及氮的一氣體混合物藉由PECVD方法來沉積具有70 nm±10 nm厚度的一SiN膜。接著，生成一潔淨及氫終止式籽晶層表面，接著係為沉積一輕度摻雜非晶性半導體層118，如第7圖所示。一潔淨的氫終止式矽表面譬如由下列步驟實現: (i)矽表面浸於過氧化氫及硫酸之一新鮮1:1混合物中10分鐘；在去離子水中沖洗表面；(iii)晶矽層117的表面浸入一5%氫氟酸溶液中直到表面為斥水性為止，接著在去離子水中作一沖洗。具有潔淨的氫終止式矽表面及其支撐層111及112之晶矽層117在清潔步驟完成的約60分鐘內被裝載至真空機中。層118可包含

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非晶性半導體材料諸如矽，鍺或矽與鍺的一合金。譬如，非晶矽可以約375至425℃範圍的沉積溫度利用矽烷及經摻雜氫的一氣體混合物藉由PECVD方法作沉積，其中層118以位於約$1x10^{15}$至$1x10^{18}cm^{-3}$範圍中被硼輕度p-型摻雜，其具有約$5x10^{16}$的較佳硼濃度及約1500 nm的較佳厚度。

一薄摻雜介電層119隨後沉積在非晶性半導體層118上，如第8圖所示。介電層119可包含一介電材料，諸如氮化矽，氧化矽，碳化矽或這些材料的一合金或一組合。介電層119可利用諸如PECVD、濺鍍或蒸鍍等沉積技術作沉積。一範例中，約有70 nm厚度之介電層119係包含一含有痕量的碳之硼摻雜(p-型)氧化矽，其在約300至350℃的至少一基材溫度以一標準平行板組態經由射頻(13.56 MHz) PECVD(RF PECVD)作沉積。吾人實驗中所使用的氣體混合物係由下列組成: 矽烷(約1 sccm)，氫(約2 sccm)中的0.5%三甲硼，一氧化二氮(約150 sccm)，及氮(約150 sccm)。沉積壓力約為150毫托耳(mTorr)且RF功率密度約為0.025 W/cm^2，導致約10 nm/min的沉積速率。一範例中，介電層119在非晶性半導體沉積步驟(相較第7圖)之後作原位沉積而不破壞一真空沉積室中的真空。

裝置121隨後受到一熱退火，其中非晶性半導體層118經由SPE產生結晶化且其中經曝露薄介電層119中的摻雜原子未顯著地擴散至半導體層118內。一範例中，在約500至650℃範圍中的溫度以約6至48小時期間進行結晶化。

接著使裝置121受到處於高溫的一快速熱退火(RTA)處

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理，其中因此使薄介電層119中的摻雜原子顯著地擴散至晶性半導體層118內且生成一位於層119與118之間的第三、重度摻雜層120，如第9圖所示。一範例中，RTA在約800至1050℃的一溫度範圍中進行約1秒至15分鐘範圍中之一段期間。

隨後，薄摻雜介電層119被移除且裝置122受到一原子性氫處理，如第10圖所示。一範例中，在約350至650℃範圍中的一溫度進行對於原子性氫的曝露。

利用上述參照第6至10圖描述的方法所製造之玻璃上的太陽能電池亦已被製作並相較於用以形成背表面場(BSF)層的習知途徑亦已展現優異之開路電壓。

在上文參照第6至10圖所描述實施例之修改中，不採用一重度摻雜($>10^{18}cm^{-3}$)晶性半導體籽晶層，形成一本徵性(亦即未摻雜)籽晶層、或一具有低摻雜位準及/或不良摻雜極性之籽晶層。非晶性半導體層118可在經修改實施例中沉積為一2摻雜位準結構，而與籽晶層相鄰之層118的一薄區(厚度約50 nm±20nm)含有對於籽晶層貢獻之過多的摻雜原子($5x10^{19}$至$1x10^{21}cm^{-3}$範圍的濃度之n或p-型)。RTA步驟期間，層118中來自相鄰區之過多摻雜物擴散至籽晶層117內且形成籽晶層中所想要的摻雜位準及極性，而與如上述的重度摻雜BSF層120之形成呈現同時。與籽晶層相鄰之層118中的過多摻雜係具有與BSF層120相反之摻雜極性。

所描述的方法經由SPC或SPE提供晶性半導體材料的一3層堆積體($n^+\pi p^+$或$p^+\pi n^+$)之製造，其中只從一側發生整體堆積體的結晶化。這相較於從兩側之整體3層堆積體的結晶

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化而言可提供經改良的顆粒尺寸及較低的瑕疵密度。並且，晶性層中沿著譬如顆粒邊界等較佳區域之來自經摻雜介電質之增強的摻雜物擴散係可在製成的二極體中提供降低的重組率(recombination rate)。

由於非晶矽比起晶矽對於污染曝露而言顯著地更為敏感，所描述方法的一額外利益在於沉積在非晶性半導體上之摻雜介電層亦作為結晶化及樣本處置期間對抗大氣汙染之一保護性擴散障壁。

尚且，摻雜介電層防止來自RTA室的污染物在RTA製程期間擴散至晶性半導體內，其由於RTA製程期間所使用的很高溫度故通常身為重大污染來源。

所描述方法係能夠以一流線化製程來實現玻璃上的$n^+\pi p^+$(或$p^+\pi n^+$)均質接合晶性薄膜二極體結構同時維持高材料品質。這提供顯著潛力來實現更合乎成本效益且仍有效率的薄膜太陽能電池及模組。

熟習該技術者將瞭解，可如特定實施例所顯示對於本發明作出許多變異及/或修改而不脫離如廣泛描述之本發明的精神或範圍。因此該等實施例在各方面被視為示範性而非限制性。

【圖式簡單說明】

第1至5圖為顯示利用固相結晶化(SPC)之裝置的製造之示意橫剖視圖；

第6至10圖為顯示利用固相磊晶(SPE)之裝置的製造之示意橫剖視圖。

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【主要元件符號說明】

11,111…外異支撐材料

12…薄介電障壁層

13…第一層

14…第二層

15,119…薄摻雜介電層

16…第三摻雜層

20…裝置

21,121…裝置

112…薄介電障壁層

117…薄、大顆粒狀重度摻雜晶性半導體層

118…輕度摻雜非晶性半導體層

120…第三、重度摻雜層

122…裝置

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五、中文發明摘要：

本發明揭露一製造一薄膜晶性半導體3層二極體結構於一外異支撐基材或覆材上之方法、及一位於一外異支撐基材或覆材上之薄膜晶性半導體3層二極體結構。一含有n或p-型摻雜物原子之犧牲介電覆層係沉積在基材或覆材上所形成之一2層半導體結構的一經曝露非晶性輕度摻雜或未摻雜半導體層上。非晶性輕度摻雜或未摻雜半導體層係被結晶化。藉由將n或p-型原子從犧牲介電覆層擴散至經結晶輕度摻雜或未摻雜半導體層的一部分內來形成一重度摻雜半導體層，其中因此形成3層二極體結構。犧牲介電覆層自3層二極體結構被移除。

六、英文發明摘要：

A method of fabricating a thin-film crystalline semiconductor 3-layer diode structure on a foreign supporting substrate or superstrate, and a thin-film crystalline semiconductor 3-layer diode structure on a foreign supporting substrate or superstrate are disclosed. A sacrificial dielectric overlayer (15) containing n or p-type dopant atoms is deposited on an exposed amorphous lightly doped or undoped semiconductor layer of a 2-layer semiconductor structure (13, 14) formed on the substrate or superstrate (11). The amorphous lightly doped or undoped semiconductor layer (13, 14) is crystalised. A heavily doped semiconductor layer is formed by diffusing the n or p-type atoms from the sacrificial dielectric overlayer into a portion of the crystallised lightly doped or undoped semiconductor layer, whereby the 3-layer diode structure (21) is formed. The sacrificial dielectric overlayer (15) is removed from the 3-layer diode structure.

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十、申請專利範圍：

1. 一種用於製造一薄膜晶性半導體3層二極體結構於一外異支撐基材或覆材上之方法，該方法包含：將一包含n或p-型摻雜物原子的犧牲介電覆層沉積在該基材或覆材上所形成之一2層半導體結構的一經曝露非晶性輕度摻雜或未摻雜半導體層上；將該非晶性輕度摻雜或未摻雜半導體層結晶化；藉由將來自該犧牲介電覆層的n或p-型原子擴散至該結晶化輕度摻雜或未摻雜半導體層的一部分內來形成一重度摻雜半導體層，其中因此形成3層二極體結構；及從該3層二極體結構移除該犧牲介電覆層。
2. 如申請專利範圍第1項之方法，其中該2層半導體結構包含該非晶性輕度摻雜或未摻雜半導體層及一非晶性重度摻雜經埋設半導體層，且用於將該非晶性輕度摻雜或未摻雜半導體層結晶化之步驟係包含經由固相結晶化將該重度摻雜經埋設半導體層結晶化。
3. 如申請專利範圍第2項之方法，其中以約500至650℃範圍中的溫度在約6至48小時期間進行該固相結晶化。
4. 如申請專利範圍第1項之方法，進一步包含藉由形成一晶性半導體籽晶層於該基材或覆材上、製備一氫終止式籽晶層表面於該晶性半導體籽晶層上、及將該輕度摻雜或未摻雜非晶性層沉積在該籽晶層表面上來形成該2層半導體結構，且用於將該非晶性輕度摻雜或未摻雜半導體層結晶化之步驟係包含固相磊晶。

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5. 如申請專利範圍第4項之方法，其中該晶性半導體籽晶層係以相較於該重度摻雜半導體層呈相反類型的一極性被重度摻雜。

6. 如申請專利範圍第4項之方法，其中該晶性半導體籽晶層係未經摻雜或以與該重度摻雜半導體層相同的一極性被摻雜，且形成該2層半導體結構係包含將一非晶性半導體膜沉積在該籽晶層表面上以使與該晶性半導體籽晶層相鄰之該非晶性半導體膜的一第一部分以相較於該重度摻雜半導體層呈相反類型的一極性被重度摻雜，且使該非晶性半導體膜的一第二部分身為該非晶性輕度摻雜或未摻雜半導體層，且形成該重度摻雜半導體層之步驟進一步包含使來自該非晶性半導體膜的第一部分之摻雜物原子擴散至該晶性半導體籽晶層內以形成該3層半導體結構之一重度摻雜經埋設半導體層。

7. 如申請專利範圍第4至6項中任一項之方法，其中以約500至650℃範圍中的溫度在約6至48小時期間進行該固相磊晶。

8. 如申請專利範圍第4至7項中任一項之方法，其中該籽晶層係以選自由下列各物所組成的群組之一方法製造：鋁引發式結晶化，金屬引發式結晶化，固相結晶化或雷射引發式結晶化。

9. 如前述申請專利範圍任一項之方法，包含形成一介電障壁層於該基材或覆材上，及形成該3層二極體結構於該介電障壁層上。

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10. 如申請專利範圍第9項之方法，其中該介電障壁層包含選自由下列各物所組成的群組之一材料：氮化矽，氧化矽，碳化矽及其一合金或一組合。

11. 如前述申請專利範圍任一項之方法，其中該3層二極體結構包含選自由下列各物所組成的群組之一材料：矽，鍺，或矽及鍺的一合金。

12. 如前述申請專利範圍任一項之方法，其中該犧牲介電覆層選自由下列各物所組成的群組：氮化矽，氧化矽，碳化矽及其一合金或一組合。

13. 如前述申請專利範圍任一項之方法，其中該犧牲介電覆層利用選自由下列各物所組成的群組之一方法作沉積：PECVD，濺鍍及蒸鍍。

14. 如前述申請專利範圍任一項之方法，其中以約1秒至15分鐘範圍中的期間利用約800至1050℃範圍中的一溫度所進行之快速熱退火來擴散來自該犧牲介電覆層的n或p-型原子藉以形成該重度摻雜半導體層。

15. 如前述申請專利範圍任一項之方法，進一步包含以約350至650℃範圍中的一溫度在移除該犧牲介電覆層之後使該3層二極體結構曝露於原子性氫。

16. 如前述申請專利範圍任一項之方法，其中該犧牲介電覆層在形成該輕度摻雜或未摻雜非晶性半導體結構的最後步驟之後作原位沉積而不破壞真空。

17. 如前述申請專利範圍任一項之方法，其中該輕度摻雜或未摻雜半導體層的摻雜係低於約$10^{18}cm^{-3}$，且該重度摻

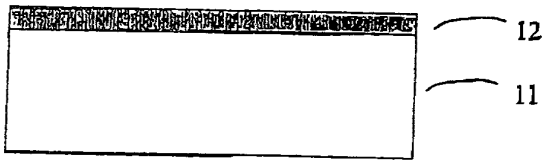
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雜經埋設半導體層的摻雜大於約$10^{18}cm^{-3}$。

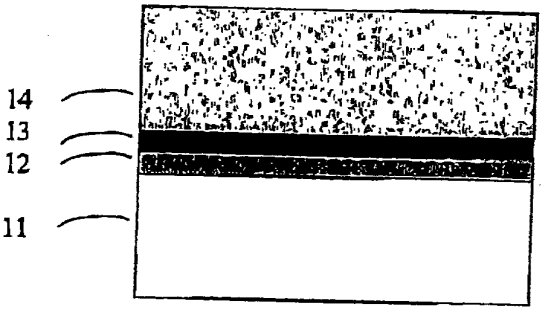
18. 如前述申請專利範圍任一項之方法，其中一其上支撐該3層半導體結構之表面係被紋理化以輔助光困陷在該3層半導體結構中。

19. 一種薄膜晶性半導體3層二極體結構，其利用根據申請專利範圍第1至18項中任一項之方法形成於一外異支撐基材或覆材上。

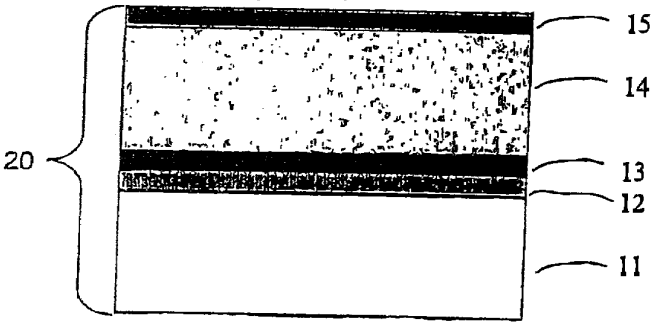
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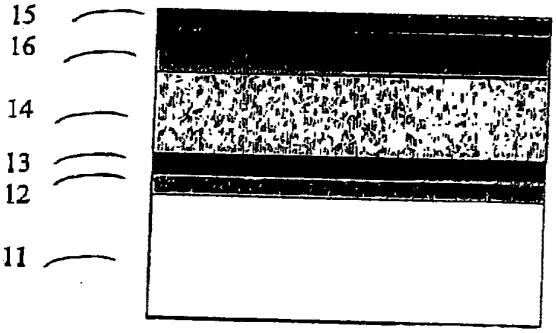
第1圖



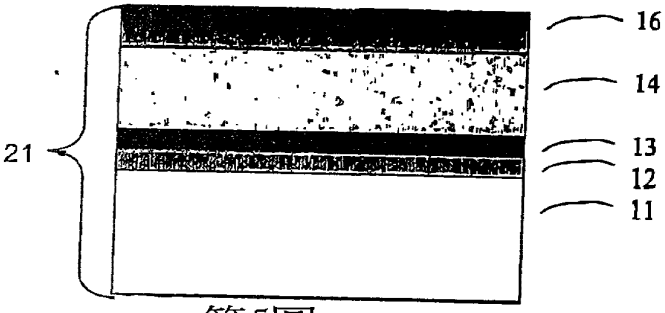
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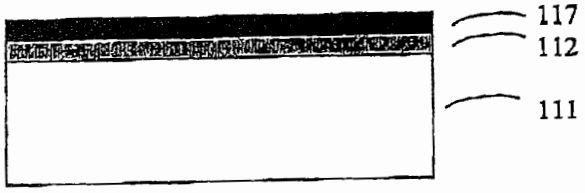
第3圖



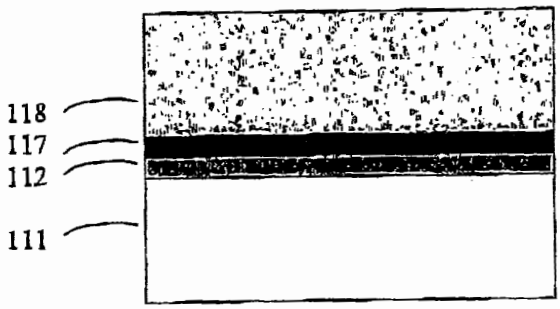
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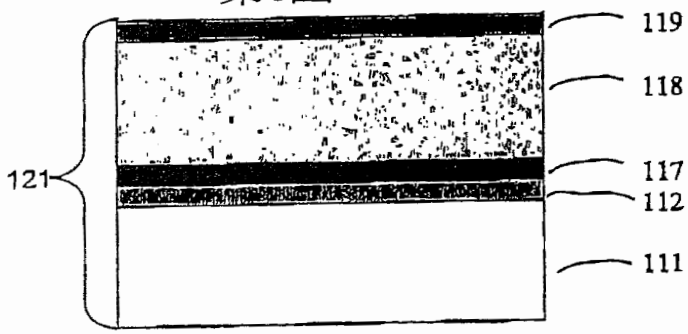
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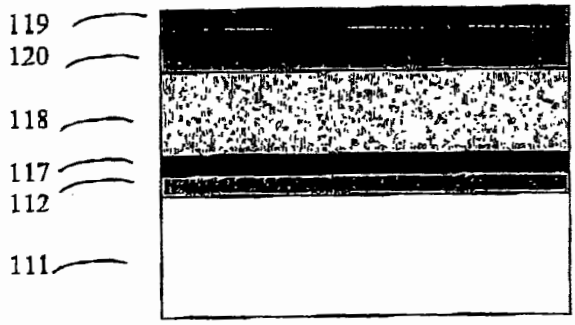
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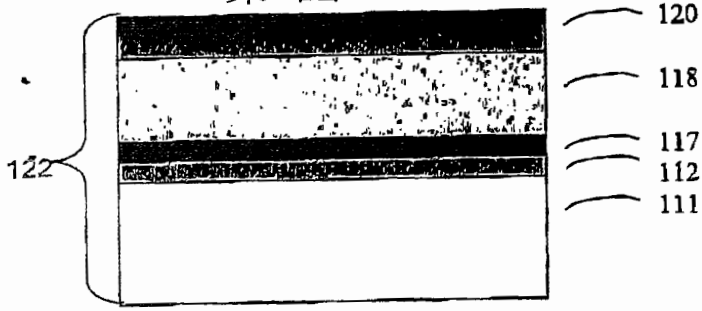
第7圖



第8圖



第9圖



第10圖

七、指定代表圖：

(一)本案指定代表圖為：第（ 5 ）圖。

(二)本代表圖之元件符號簡單說明：

11…外異支撐材料
12…薄介電障壁層
13…一層
14…第二層
16…第三摻雜層
21…裝置

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(54) Title: HIGH DYNAMIC RANGE VIDEO

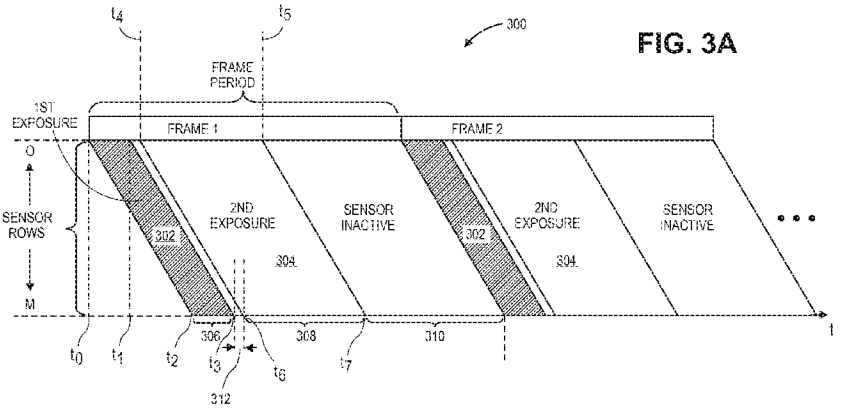


FIG. 3A

(57) Abstract: Certain cameras and systems described herein produce enhanced dynamic range still or video images. The images can also have controlled or reduced motion artifacts. Moreover, the cameras and systems in some cases allow the dynamic range and/or motion artifacts to be tuned to achieve a desired cinematic effect.

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HIGH DYNAMIC RANGE VIDEO

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of priority from U.S. Provisional Application Numbers 61/376,172 filed August 23, 2010, and 61/473,711 filed April 8, 2011, both of which are incorporated in their entirety by reference herein.

BACKGROUND

[0002] The disclosure herein relates to devices for creating improved dynamic range images, such as from images of still or moving scenes detected with a digital camera.

[0003] The dynamic range of a digital image can be characterized as the ratio in intensity between the brightest and the darkest measured values in the image. Thus, an image having a wide dynamic range represents more accurately the wide range of intensity levels found in real scenes.

SUMMARY

[0004] Conventional digital cameras and techniques typically produce relatively low dynamic range images and provide limited flexibility in controlling dynamic range. Dynamic range can be limited by factors including the level of brightness detectable by each sensor element (e.g., the bit-width of each pixel) and the level of exposure. For example, a captured image may accurately represent the intensity of relatively dark regions of the scene, but not relatively bright regions of the same scene, or vice versa.

[0005] Different techniques can be used to enhance the dynamic range of images. However, particularly for moving images, existing techniques are generally overly complex, provide sub-optimal image quality, or allow limited creative flexibility. For example, some techniques produce relatively large, un-controlled motion artifacts (e.g., blurring or flickering). For these and other reasons, certain cameras and systems described herein produce enhanced dynamic range images also having controlled or reduced motion artifacts. Moreover, according to some aspects, the system provides an

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interface allowing users to tune the dynamic range and/or motion artifacts to achieve a desired cinematic effect.

[0006] According to certain aspects, a method is provided of obtaining image data using a digital imaging sensor comprising a picture element array of rows and columns. The method can include using a plurality of picture elements in the picture element array to capture light corresponding to a first image at a first exposure level and using the plurality of picture elements in the picture element array to capture light corresponding to a second image at a second exposure level different than the first exposure level. The method can further include converting the light captured by the plurality of picture elements for the first image to digital measurements and converting the light captured by the plurality of picture elements for the second image to digital measurements. In some embodiments, the step of using the plurality of picture elements in the picture element array to capture light corresponding to the second image at the second exposure level begins prior to the completion of the step of converting the light captured by the plurality of picture elements for the first image to digital measurements. Moreover, in certain embodiments, the step of converting the light captured by the plurality of picture elements for the first image to digital measurements substantially completes prior to the beginning of the step of converting light captured by the plurality of picture elements for the second image to digital measurements.

[0007] According to additional aspects, an imaging system is provided, comprising a plurality of picture elements arranged in an array. The imaging system can further comprise control circuitry configured to capture light corresponding to a first image at a first exposure level with the plurality of picture elements in the picture element array and capture light corresponding to a second image at a second exposure level different than the first exposure level with the plurality of picture elements in the picture element array. The control circuitry can further be configured to convert the light captured by the plurality of picture elements for the first image to digital measurements and convert light captured by the plurality of picture elements for the second image to digital measurements. According to some embodiments, the control circuitry begins the capturing of the light corresponding to the second image at the second exposure level prior to the completion of the converting of the light captured for the first image to digital measurements. The control circuitry may additionally substantially complete the

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converting of the light for the first image to digital measurements prior to the beginning of the converting of the light for the second image to digital measurements.

[0008] According to further aspects, a method is provided of processing image data. The method can include receiving first image data corresponding to a plurality of picture elements in a picture element array used to capture light corresponding to a first image at a first exposure level. The method may further include receiving second image data corresponding to the plurality of picture elements in the picture element array used to capture light corresponding to a second image at a second exposure level. The method can additionally include selectively combining the first image data and the second image data to create combined image data corresponding to a combined image having a wider dynamic range than either of the first image or the second image. In some cases, the using the plurality of picture elements in the picture element array to capture light corresponding to the second image at the second exposure level began prior to the completion of converting the light captured by the plurality of picture elements for the first image to digital measurements. Moreover, the converting the light captured by the plurality of picture elements for the first image to digital measurements substantially completed prior to the beginning of the step of converting light captured by the plurality of picture elements for the second image to digital measurements.

[0009] In yet further embodiments, a method is provided of obtaining image data using a digital imaging sensor. The method can include capturing a first image with the sensor at a first exposure level and capturing a second image with the sensor at a second exposure level different from the first exposure level. The method may additionally include outputting the first image and outputting the second image. The capturing of the first image in some cases begins before said capturing of the second image begins. Additionally, the capturing of the first image and said capturing of the second image overlap in time in some cases. Further, the outputting of the first image and said outputting of the second image do not overlap in time in some embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is a block diagram illustrating an example imaging system according to embodiments described herein.

[0011] Figure 2 is a block diagram illustrating an example sensor architecture capable of generating multiple, closely-timed exposures according to some embodiments.

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[0012] Figures 3A-3D are timing diagrams showing operation of example sensors recording multiple, closely-timed exposures for multiple frames of recorded video in accordance with certain embodiments.

[0013] Figure 3E is a timing diagram showing operation of a sensor operating without recording closely-timed exposures.

[0014] Figures 4A-4C are timing diagrams showing operation of embodiments of sensors recording closely-timed exposures for several rows of an image sensor.

[0015] Figures 5 is a block diagram illustrating an example process for blending tracks of closely timed exposures having different exposure levels in accordance with some embodiments.

[0016] Figures 6A-6B illustrate example operations for blending tracks of closely-timed exposures having different exposure levels in accordance with certain embodiments.

[0017] Figure 7 illustrates another example process for blending tracks having different exposure levels in accordance with some embodiments.

[0018] Figure 8 illustrates an embodiment of a process for blending tracks of closely-timed exposures having different levels of exposure to control motion artifacts.

DETAILED DESCRIPTION

[0019] According to certain aspects, a camera system is provided having a sensor capable of sequentially capturing and outputting first and second image(s) having different exposure levels. Moreover, the system begins capturing the first and second (or more) images within a single frame period, providing controllable or reduced motion artifacts, among other advantages.

[0020] For instance, the first and second images are closely timed with respect to one another. Moreover, while there can be some separation in time between when the system captures pixels for the first image and captures corresponding pixels for the second image, the first and second images may nonetheless be referred to as or "conjoined" with one another in time because the separation does not result in visually significant artifacts when the images are combined. To achieve this effect, the exposure times for at least some portions of the first and second images overlap with one another, in some configurations. When recording video images, some sensors disclosed herein output at least first and second closely-timed (or "conjoined") image streams (also

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referred to herein as "tracks"). According to additional aspects, systems and methods described herein process the first and second image streams (e.g., in-camera or during post-processing) to create a combined output stream.

[0021] For example, for each video frame, the imaging system captures individual exposures in a second (e.g., relatively high exposure) track very soon after the capturing corresponding exposures in the first (e.g., relatively low exposure) track. In this manner, certain techniques described herein reduce or remove the potential for visual separation between objects in an image track having a first exposure level as compared to the same objects in an image track(s) having a different exposure level. Undesirable levels of visual separation between objects could otherwise arise between the objects in the first image and corresponding objects in the second image, due either to movement of objects in scene or of the camera, for example.

[0022] Moreover, the system acquires the individual images from the sensor relatively quickly. Where the system incorporates a rolling shutter, for example, the period of delay from between beginning exposure for the first rows of the sensor for a particular image and beginning the exposure for the last rows of the sensor for the image is relatively short. Similarly, the period of delay from between reading out the first rows for an image to reading out the last rows of the sensor for the image is also relatively short. In this manner, the system limits the amount of motion artifact (e.g., wobble, skew, smear) introduced by the rolling shutter. This is in contrast to configurations where the amount of time it takes to capture and read out an entire exposure consumes a larger period of time.

[0023] Moreover, systems described herein according to some aspects exploit the minimal gap between first and second images, limited rolling shutter artifacts, and other aspects of the techniques described herein to achieve a variety of desirable creative effects. For example, the system can selectively blend or combine the closely-timed image streams to adjust the dynamic range, the character of the motion effect (e.g., amount or quality of blur), or other characteristic.

[0024] In some cases, the blending of the image streams is tailored to achieve a motion effect substantially similar to how motion is perceived by the human eye. In some instances, the blending is adjusted such that the blurring effect is similar to that of a traditional camera. A user may advantageously control the amount or quality of the image

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stream blending, providing additionally creative power and flexibility. Such processes can be partially or fully automated, as well.

[0025] Thus, the techniques described herein provide a variety of benefits. Particularly in the area of recording motion video, certain embodiments provide recordings having improved-dynamic range, customized motion or other visual effects, and combinations thereof.

[0026] While the techniques described herein are discussed primarily with respect to digital motion cameras recording continuous video, it will be understood that various aspects of the inventions described herein are compatible with still cameras, as well as digital still and motion cameras (DSMC's).

System Overview

[0027] **Figure 1** is a block diagram an example system 100 that detects optical data and processes the detected data. The system 100 can include an imaging device 101 that can include an optics module 110, and an image sensor 112, which may further include a multiple exposure generator 113. The device 101 can also include a memory 114 and an image processing module 116. The image processing module 116 may in turn include a blending module 117 that is generally configured to adjust the dynamic range of an output image or stream of images. The blending module 117 may further be configured to adjust the motion effect in the output stream.

[0028] The imaging device 101 may be a camera system, for example, and the optics module 110, image sensor 112, memory 114, and the image processing module 116 or portions thereof may be housed in or supported by the camera housing. Moreover, portions of the system 100 may be included in a separate device. For example, as shown, the blending module 117 or portions thereof in some configurations resides in a separate computing device 102, such as a laptop or other computer.

[0029] The optics module 110 focuses an image on the image sensor 112. Sensors 112 may include, for example, an array of charge-coupled devices (CCD) or Complementary Metal–Oxide–Semiconductor (CMOS) image sensor cells such as active-pixel sensor cells. Such image sensors are typically built on silicon chips and may contain millions of image sensor cells. Each sensor cell detects light reaching its surface and outputs a signal that corresponds to the intensity of the light detected. The detected light is then digitized.

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[0030] Because these image sensors are sensitive to a broad spectrum of wavelengths of light, a color filter array can be disposed over the light sensitive surface of such sensors. One type of color filter array is a Bayer pattern color filter array, which selectively passes red, blue, or green wavelengths to sensor elements. The output of such a sensor, however, is a mosaic image. This mosaic image is formed by the overlapping matrices of red, green, and blue pixels. The mosaic image is usually then demosaiced, so that each picture element has a full set of color image data. The color image data may be expressed in the RGB color format or any other color format.

[0031] Some of the embodiments disclosed herein are described in the context of a video camera having a single sensor device with a Bayer pattern filter. However, the embodiments and inventions herein can also be applied to cameras having other types of image sensors (e.g., CMY Bayer as well as other non-Bayer patterns), other numbers of image sensors, operating on different image format types, and being configured for still and/or moving pictures. It is to be understood that the embodiments disclosed herein are exemplary but non-limiting embodiments, and the inventions disclosed herein are not limited to the disclosed exemplary embodiments.

[0032] The optics hardware 110 can be in the form of a lens system having at least one lens configured to focus an incoming image onto the image sensor 112. The optics hardware 110, optionally, can be in the form of a multi-lens system providing variable zoom, aperture, and focus. Additionally, the optics hardware 110 can be in the form of a lens socket supported by a camera housing and configured to receive a plurality of different types of lens systems for example, but without limitation, the optics hardware 110 include a socket configured to receive various sizes of lens systems including a 50-100 millimeter (T3) zoom lens, a 50-150 millimeter (T3) zoom lens, an 18-50 millimeter (T3) zoom lens, an 18-85 millimeter (T2.9) zoom lens, a 300 millimeter (T2.8) lens, 18 millimeter (T2.9) lens, 25 millimeter (T1.8) lens, 35 millimeter (T1.8) lens, 50 millimeter (T1.8) lens, 85 millimeter (T1.8) lens, 85 millimeter (T1.8) lens, 100 millimeter (T1.8) and/or any other lens or any other lens. In certain embodiments, a 50-100 millimeter (F2.8) zoom lens, an 18-50 millimeter (F2.8) zoom lens, a 300 millimeter (F2.8) lens, 15 millimeter (F2.8) lens, 25 millimeter (F1.9) lens, 35 millimeter (F1.9) lens, 50 millimeter (F1.9) lens, 85 millimeter (F1.9) lens, and/or any other lens. As noted above, the optics hardware 110 can be configured such that despite which lens is attached thereto, images can be focused upon a light-sensitive surface of the image sensor 112.

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[0033] The image sensor 112 can be any type of image sensing device, including, for example, but without limitation, CCD, CMOS, vertically-stacked CMOS devices such as the Foveon® sensor, or a multi-sensor array using a prism to divide light between the sensors. In some embodiments, the image sensor 112 can include a CMOS device having about 12 million photocells. However, other size sensors can also be used. In some configurations, camera 10 can be configured to output video at "5k" (e.g., 5120 x 2700), , Quad HD (e.g., 3840 x 2160 pixels), "4.5k" resolution (e.g., 4,520 x 2540), "4k" (e.g., 4,096 x 2,540 pixels), "2k" (e.g., 2048 x 1152 pixels) or other resolutions. As used herein, in the terms expressed in the format of xk (such as 2k and 4k noted above), the "x" quantity refers to the approximate horizontal resolution. As such, "4k" resolution corresponds to about 4000 or more horizontal pixels and "2k" corresponds to about 2000 or more pixels.

[0034] The camera can also be configured to downsample and subsequently process the output of the sensor 112 to yield video output at 2K, 1080p, 720p, or any other resolution. For example, the image data from the sensor 112 can be "windowed", thereby reducing the size of the output image and allowing for higher readout speeds. However, other size sensors can also be used. Additionally, the camera can be configured to upsample the output of the sensor 112 to yield video output at higher resolutions. Moreover, the camera can be configured to capture and record video at 10, 20, 24, 30, 60, and 120 frames per second, or any other frame rate. Additionally, the blending techniques described herein are generally compatible with a variety resolutions and frame rates, including those listed above.

[0035] The memory 114 can be in the form of any type of digital storage, such as, for example, but without limitation, hard drives, solid-state drives, flash memory, optical discs, or any other type of memory device. In some embodiments, the size of the memory 114 can be sufficiently large to store image data from the compression module corresponding to at least about 30 minutes of video at 12 mega pixel resolution, 12-bit color resolution, and at 60 frames per second. However, the memory 114 can have any size.

[0036] In some embodiments, the memory 114 can be mounted on an exterior of a camera housing. Further, in some embodiments, the memory can be connected to the other components through standard or custom communication ports, including, for example, but without limitation, Ethernet, USB, USB2, USB3, IEEE 1394 (including but

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not limited to FireWire 400, FireWire 800, FireWire S3200, FireWire S800T, i.LINK, DV), SATA and SCSI. Further, in some embodiments, the memory 114 can comprise a plurality of hard drives, such as those operating under a RAID protocol. However, any type of storage device can be used.

[0037] The image processing module 116 may, for example, operate on data that is stored in the memory 114. Alternatively, the image processing module may operate on data as it comes from the image sensor 112, and the processed data may then be stored in the memory 114. The image processing module 116 may perform a variety of operations on the data. Depending on the operation, the processing module 116 may perform the operation on the individual first and second image streams, prior to blending, or alternatively, on the blended HDR output stream.

[0038] For example, the image processing module 116 may compress the data from the image sensor, perform pre-compression data-preparation (e.g., pre-emphasis and/or entropy reduction), format the compressed data, and the like. Examples of such techniques are described in greater detail in U.S. Patent No. 7,830,967 entitled "VIDEO CAMERA" (the '967 patent), which is incorporated by reference herein in its entirety. In some instances, the image processing module 116 processes the individual image stream (or combined image stream) to tune the image streams to perceptual space, as will be described in detail below with respect to Figure 8A. Additional compatible techniques include green data modification and pre-emphasis processes shown and described throughout the '967 patent (e.g., with respect to Figures 8-11 and columns 11-13). In general, certain embodiments described herein are compatible with and/or are components of embodiments described in the '967 patent. Thus, some or all of the features described herein can be used or otherwise combined with various features described in the '967 patent, including features described in the '967 patent which are not explicitly discussed herein.

[0039] The sensor 112 can be configured to sequentially capture and output at least first and second image streams (or tracks) having different exposure levels. For example, the multiple exposure generator 113 may comprise specially designed timing control logic that controls the sensor 112 to output the image streams. In some cases, the sensor 112 can output more than two tracks (e.g., totaling 3, 4, 5, 10 or more) having various exposure levels.

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[0040] Where there is a significant amount of delay between exposures or portions of exposures in a first track and corresponding exposures or portions of exposures in a second track, undesirable motion artifacts can arise. For example, such artifacts can arise where an object in the recorded scene (e.g., an actor or other photographic subject) moves a visually significant distance between the time the first image stream frame is captured and the time the second image stream frame is captured. In such cases, visual separation, or "gaps," can arise between objects in one track as compared to the same object in another track. Such issues can be difficult to correct for or control in post-processing.

[0041] For these and other reasons, the sensor 112 according to certain aspects is configured to sequentially output at least first and second image streams having different exposure levels and which are closely timed with respect to one another. For example, the multiple exposure generator 113 may control a pixel array and output circuitry of the sensor 112 to cause the sensor 112 to output first and second image streams. Each image stream can have multiple frames which are closely-timed and/or at least partially overlapping in time with corresponding frames from the other image stream. For instance, the amount of time from between when the system converts captured data for picture elements in the images from the first stream to digital values and begins to expose the same picture elements for corresponding images in the second image stream is relatively short. Moreover, in some cases, the multiple exposure generator 113 captures at least some of the picture elements for the images in the second stream while capturing other picture elements for the corresponding images in the first stream, during overlapping time periods. In this manner, the visual separation between moving objects in the first image stream and the same moving objects in the second image stream may be relatively insignificant, or may be otherwise substantially reduced. The multiple exposure generator 113 may generally be a specialized timing generator coupled to the sensor 112, and is described in greater detail with respect to Figure 2.

[0042] Because there may be no significant visual separation between objects in a frame in the first image track frame and the corresponding objects in a subsequently captured frame in the second image track, the first and second image tracks may also be referred to as having no "gaps" with respect to one another, or as substantially "touching" one another. For example, while there may be some minor delay between the capture of picture elements for first images and the capture of picture elements in the second images,

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the delay may be so small that there is reduced or substantially no visual object separation at full sensor resolution, at one or more scaled-down resolutions, or a combination thereof. Due to the closely-timed nature of the tracks, the motion artifacts in the combined output track are substantially reduced, removed, or can be controlled in a desired fashion.

[0043] Sensors described herein are referred to herein as having "adjacent read" or "conjoined exposure" capability. Additionally, the images tracks may be referred to as being "adjacent," "closely timed," "conjoined," or the like.

[0044] Moreover, as described above, the individual exposures according to some embodiments are captured and/or output in a compact manner, making efficient use of the frame period.

[0045] The blending module 117 according to certain embodiments selectively combines the closely-timed tracks to produce an output track having a desired visual effect. For instance, the output video stream can have an enhanced dynamic range relative to the dynamic range of the individual first and second image tracks. As an example, the first image stream may have a relatively low exposure level (e.g., short integration time), providing useful data in relatively bright regions of a captured scene, such as highlight detail. The second image stream may have a relatively higher exposure level (e.g., longer integration time), providing useful data in relatively darker regions of the scene, such as detail in the shadows.

[0046] Moreover, in some cases where the sensor 112 outputs more than two tracks, the blending module 117 is capable of combining a corresponding number of tracks. Where the blending module 117 or portions thereof reside in the external computing device 102, the dynamic range and/or motion processing can be done in post-processing. Additionally, depending on the implementation, the blending module 117 may operate on data stored in the memory 114, on data as it is output from the image sensor 112, or on data stored in the external computing device 102.

[0047] As discussed, the combined output stream may be created on camera or alternatively off camera, during post-processing. In one configuration, the user can select on-camera or off camera creation of the output stream, as desired. Moreover, as will be described in further detail below with respect to Figures 5-9, in various embodiments the blending module 117 can combine the closely-timed tracks according to a variety of algorithms. The algorithms can be fixed or user-selectable or adjustable. For example, in

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one embodiment, the image streams are combined on-camera according to a fixed algorithm. In another configuration, the user selects from a variety of algorithms, depending on the desired creative effect.

Generating Tracks of Closely-Timed Images Having Multiple Exposure Levels

[0048] **Figure 2** is a block diagram illustrating example image sensor 200 capable of generating closely-timed exposures according to embodiments described herein. Referring to Figure 2, the image sensor 200 includes a pixel array 202, output circuitry 204, and a multiple exposure generator 206. As will be described in greater detail, the multiple exposure generator 206 generally controls the various components of the sensor 200 to provide closely-timed exposures on the output bus 212 of the sensor 200 for further storage and processing.

[0049] The image sensor 200 may be similar to the image sensor 12 described above with respect to Figure 1, for example, and the pixel array 202 includes a plurality of pixels (e.g., photocells) arranged in a matrix including "M" rows and "N" columns. While a wide variety of values are possible for "M" and "N", an example "5k" sensor includes 5,120 rows and 2,700 columns, an example Quad HD sensor includes 3,840 and 2,160 pixels, an example "4.5k" resolution sensor includes 4,520 rows and 2,540 columns, an example"4k" sensor includes 4,096 rows and 2,540 columns, and an example "2k" sensor includes 2,048 and 1,152 columns.

[0050] In the illustrated example, sensor 200 is configured to output a single row at a given time, and the sensor 200 includes one instance of output circuitry 204 that is configured to process and output image information for a single row. In another embodiment, such as where a Bayer pattern sensor is used, the sensor outputs two rows at a time and can include two instances of the output circuitry 204. In yet other configurations, the sensor 200 outputs other numbers of rows during a given time slot (e.g., 2, 3, 4, 5, 10 or more rows), and can include a corresponding number of instances of the output circuitry 204.

[0051] During operation, the multiple exposure generator 206 provides row select information via input bus 208 to row decode logic (not shown) of the pixel array 202. For each of the selected rows, the pixel array 202 provides the stored values for the N pixels corresponding to the columns of the selected row (or subset of rows) to the output circuitry 204.

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[0052] The output circuitry 204 of the example sensor 200 also receives timing control signals on the bus 210 from the multiple exposure generator 206, and is generally configured to process and digitize the analog pixel values received from the pixel array. The output circuitry 204 of the example sensor 200 includes sets of programmable-gain amplifiers (PGAs) and analog-to-digital converters (ADCs), although a variety components may be used in various implementations. The output circuitry 204 in turn presents the digitized, processed values of the currently selected row on the output bus 212. For example, the sensor 200 may transmit the values to the memory 114, image processing module 116, or other components of the system of Figure 1 for storage and processing. In some instances, the sensor buffers the values for one or more rows before transmission on the output bus 212.

[0053] As shown in Figure 2, the multiple exposure generator 206 may reside outside of the packaging 214. For example, the packaging 214 is an integrated circuit packaging and the pixel array 202 and output circuitry 204 are formed on an integrated circuit housed in the packaging 214. The multiple exposure generator 206, on the other hand, may form a part of a separate integrated circuit that is housed in a separate package. In another embodiment, the multiple exposure generator 206 is included on the same integrated circuit as the other components, and is housed in the sensor package 214.

[0054] In some cases, the multiple exposure generator 206 comprises logic implemented in a field-programmable gate array (FPGA), although the multiple exposure generator 206 can be implemented in a variety of ways, and can include hardware, software, analog and/or digital circuitry, such as custom circuitry, a microprocessor, an application-specific integrated circuit (ASIC), combinations thereof and the like.

[0055] **Figure 3A** is an example timing diagram 300 illustrating two consecutive frames of video for a camera that is recording two closely-timed image tracks (also referred to as image streams) in accordance with an embodiment. Two closely-timed exposures 302, 304 are taken within each video frame, one for each image track. Thus, a first image track corresponds to the first exposures 302 taken over a series of recorded video frames and a second image track 304 corresponds to second exposures 304 taken over the same series of video frames.

[0056] The camera exposes the first exposure 302 for each frame for a first integration period 306, and exposes the second exposure 304 for each frame for a second integration period 308. The timing diagram 300 may be representative of the operation of

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the sensors 112, 200 of Figures 1 and 2, for example. Moreover, while the diagram shows operation for only two frames for the purposes of illustration, it will be appreciated that the camera may record any number of frames, depending on the length of the recording.

[0057] As shown, the camera of the illustrated example exposes the rows 0→M of the sensor in an overlapping fashion. In this manner, the first row (or subset of rows) is exposed for a first integration period beginning at time t_0 and ending at time t_1. The remaining rows (or subsets of rows) are exposed in successive, overlapping time slots, and the first integration period for the last row extends from time t_2 to time t_3. This general exposure scheme, where successive rows (or subsets of rows) are exposed in successive, overlapping time slots, may generally be referred to as a "rolling shutter" technique.

[0058] Picture elements for the second exposure 304 are advantageously captured relatively shortly after capturing the same picture elements for the first exposure 302. For example, the inter-exposure delay 312 between the end of the first exposure period 306 for each row (or subset of rows) and the beginning of the second exposure period 308 for the same row is relatively minimal. For example, as discussed in greater detail with respect to Figure 4A below, the inter-exposure delay 312 may depend in one instance on the reset time for one or more rows of the sensor. In other cases, the inter-exposure delay 312 can depend on some other parameter(s). Referring again to the sensor 200 of Figure 2, the multiple exposure generator 206 is configured to generate control signals for operating the pixel array 202 and output circuitry 204 to generate the closely-timed exposures 302, 304.

[0059] Moreover, the inter-row skew for the individual exposures 302, 304 introduced by the rolling shutter is relatively minimal. This results in a shorter overall image acquisition time, and helps to control any motion artifacts that may otherwise be introduced by the rolling shutter. As will be discussed further with respect to Figure 4A, the inter-row skew and image acquisition time can be related to the readout time for a row (or subset rows).

[0060] As shown, the system additionally makes efficient use of the sensor hardware and frame period by overlapping certain portions of the first and second exposures in time. For instance, the system begins to expose at least some of the rows (or subsets of rows) for the second exposure 304 before all of the rows have been converted and/or read

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out for the first exposure 302. Moreover, at least some rows are exposed for the first exposure 302 concurrently with other rows for the second exposure 304.

[0061] The system in certain embodiments additionally substantially completes the conversion and/or readout of the sensor rows (or subsets of rows) for the first exposure 302 before beginning to convert and/or readout the rows for the second exposure 304. By dedicating the conversion and readout circuitry to each of the respective exposures until they are complete, the system helps maintain a compact overall acquisition time for the individual exposures 302, 304. In the illustrated embodiment, the system completes converting and/or reading out 100 percent of the sensor rows for first exposure 302 before beginning to convert and/or readout any of the rows for the second exposure 304. In other cases, the system completes converting and/or reading out at least 80 percent, at least 90 percent, at least 95 percent, at least 96 percent, at least 97 percent, at least 98 percent or at least 99 percent of the sensor rows for the first exposure 302 before beginning to convert and/or read out the rows for the second exposure 304. In yet further cases, the system substantially completes conversion and/or readout of the rows for the first exposure 302 before reading out any of the rows for the second exposure 304, or before reading out more than 1 percent, more than 2 percent, more than 3 percent, more than 4 percent, more than 5 percent, more than 10 percent, or more than 20 percent of the rows for the second exposure 304, depending on the embodiment. Further details regarding the specifics of the sensor timing are provided below with respect to Figures 4A-4C.

[0062] Depending on the particular configuration, the duration of the various time periods shown in Figure 3A can vary greatly, including the frame period 312, first and second exposure integration times 302, 304, inter-exposure delay 312 and sensor inactive 310. The sensor inactive time 310 may refer to a period where sensor elements are substantially inactive and not being exposed. For example, when capturing the first and second exposures, the sensor electronically activates the appropriate picture elements according to the rolling shutter technique to be sensitive to and capture incident light. In contrast, the appropriate pixel elements are electronically deactivated and therefore not sensitive to incident light during the sensor inactive period 310. In other implementations, where a physical shutter is used, the physical shutter is opened/closed in place of the electronic activation/deactivation. The sensor inactive period can also instead be defined as the period of time from between t_7, when exposure completes for the last row in the second

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exposure 304, to the end of the frame period, immediately before the first row in the first exposure 302 begins to expose for the next frame.

[0063] Figures 3B-3D illustrate timing diagrams for several example configurations. For clarity, the inter-exposure delay 312 is not shown in Figures 3B-3D. In one embodiment, Figure 3B illustrates a scenario where the frame period is about 41.7 milliseconds (24 fps), the first integration time 306 is about 2.6 milliseconds, the second integration time 308 is about 20.8 milliseconds, the inter-exposure delay 312 is about 15.6 microseconds, and the shutter closed time is about 18.2 milliseconds. The second integration time 308 is about half the frame period, and thus generally corresponds to an integration time for a sensor implementing a 180 degree shutter. In another example case, Figure 3C shows a scenario where the frame period 312 is about 41.7 milliseconds (24 fps), the first integration time 306 is about 2.6 milliseconds, the second integration time 308 is about 31.6 milliseconds, the inter-exposure delay 312 is about 15.6 microseconds, and the shutter closed time 310 is about 7.4 milliseconds. In this case, the second integration 308 time corresponds to an integration time for a sensor implementing a 273 degree shutter. In yet another instance, Figure 3D illustrates an case where the frame period 312 is about 41.7 milliseconds (24 fps), the first integration time 306 is about 0.65 milliseconds, the second integration time 308 is about 5.2 milliseconds, the inter-exposure delay 312 is about 15.6 microseconds, and the shutter closed time 310 is about 35.75 milliseconds. Here, the second integration time 308 corresponds to an integration time for a 45 degree shutter.

[0064] For comparison, Figure 3E illustrates a timing diagram for another example camera capturing multiple exposures having different exposure levels. However, unlike the embodiments shown in Figures 3A-3D, the camera of Figure 3E captures the long exposures 304 and short exposures 306 on different, alternating frames. Thus, the exposures 304 and 306 are not closely-timed, and significant undesirable motion artifacts may be present. For example, relatively large gaps of visual separation may exist between image scene objects in the long exposures 304 as compared to image scene objects in the short exposure 306 in the next frame. Thus, it can be difficult in such cases to combine the short and long exposures 304, 306 to create high-dynamic range images with controlled motion artifacts.

[0065] **Figure 4A** shows a timing diagram 400 illustrating closely-timed first and second exposures 402, 404 for one frame of recorded video. For clarity, the timing diagram is shown for only the first three rows R1, R2, R3 (or subsets of rows) of an image

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sensor. For example, the diagram 400 may correspond to one embodiment of a more detailed depiction of the exposure timing for the first three rows of the sensor whose operation is depicted in any of Figures 3A-3D. Referring to the first row R1, before the first exposure 402 begins, the row R1 is initially reset, as indicated by the vertical arrow labeled "RST."

[0066] After a reset period 410 passes corresponding to the amount of time it takes to reset the pixels in the row R1, the photocells in the row R1 begin to accumulate charge during the first integration period 406. Following the first integration period 406, the pixels in the first row R1 have accumulated charge corresponding to the first exposure level. A readout cycle is then initiated for the row R1, along with another reset cycle, as indicated by the vertical arrow labeled "RO/RST". Referring to Figure 2, at the end of the readout period 412, the row R1 is readout of the pixel array 202 by the output circuitry 204, and is provided on the output 212 for storage and/or processing.

[0067] Additionally, once the row R1 has completed the second reset cycle, the second exposure 404 begins. As such, the inter-exposure delay 410 between the first and second exposures in one embodiment depends on the reset time 410 for a row of pixels (or subset of rows where more than one row are read out at once). For example, the inter-exposure delay 410 may correspond to, substantially correspond, or be approximately equal to the reset time 410 for one row (or subset of rows). In other instances, the inter-exposure delay 410 is less than or equal to approximately one, approximately 2, approximately 5, approximately 10, approximately 20, approximately 50 or approximately 100 reset times 410 for a row (or subset of rows). In yet further cases, the inter-exposure delay 410 is some value between approximately one reset time 410 for a row (or subset of rows) and approximately 2, approximately 5, approximately 10, approximately 20, approximately 50 or approximately 100 reset times, depending on the embodiment. As is described in greater detail below, the reset time 410 can advantageously be relatively short, leading to closely timed first and second exposures 402, 404.

[0068] In other configurations, the delay between the first and second exposures 402, 404 can correspond to a variety of values other than the reset time 410. For example, the inter-exposure delay 410 may correspond to, substantially correspond to, or otherwise depend on the readout time 412, such as where the readout time is greater than or equal to the reset time. In one such embodiment, the inter-exposure delay 410 is

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approximately equal to the readout time 412. In other cases, depending on the specific implementation, the inter-exposure delay 410 is less than or equal to approximately one, approximately 2, approximately 5, approximately 10, approximately 20, approximately 50 or approximately 100 readout times 412 for a row (or subset of rows). According to yet further embodiments, the inter-exposure delay 410 is be some value between approximately one readout time 412 for a row (or subset of rows) and approximately 2, approximately 5, approximately 10, approximately 20, approximately 50 or approximately 100 readout times 412. In further cases, the delay 410 between the first and second exposures 402, 404 depends on both the readout time and the reset time. For example, the reset operation in one embodiment is initiated only after completion of the readout operation. In this case, the delay between the first and second exposures 402, 404 may correspond to or substantially correspond to the sum of the readout time 412 and the reset time. In such cases, the inter-exposure delay 410 may be less than or equal to approximately the sum of the reset time 410 and the readout time 412 for a row (or subset of rows), or may alternatively be less than or equal to approximately the sum of the reset time 410 and the readout time 412, multiplied by a factor of 2, 5, 10, 20, 50 or 100. In further embodiments, the inter-exposure delay 410 can be some value between approximately the sum of the reset time 410 and the readout time 412 for a row (or subset of rows) and approximately the sum of the reset time 410 and the readout time 412, multiplied by a factor of 2, 5, 10, 20, 50 or 100.

[0069] As shown, the sensor initiates a similar sequence of operations for the other rows R2, R3...RM. However, as described above, with respect to Figure 2, the sensor may be configured to output only one row (or a subset of two or more rows) at a time. Thus, for each subsequent row, the multiple exposure generator 206 waits at least one readout period 412 before initiating the initial reset cycle. As such, the exposure timing for each row is staggered in time with respect to the other rows. In the illustrated example, each subsequent row is delayed by the readout period 412 with respect to the preceding row. As such, when an integration period 402, 404 is complete for a particular row, the output circuitry 204 will be generally immediately available. In this manner, the utilization of the readout circuitry (e.g., the output circuitry 204 of Figure 2) is relatively high. Referring again to Figure 2, the multiple exposure generator 206 may send the appropriate control signals to the pixel array via the bus 208 and to the output circuitry

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204 via the bus 210, initiating the reset and readout of the rows R1, R2, R3...RM in the manner described.

[0070] Although a variety of values are possible, one example sensor 200 has 2740 rows of pixels configured to be readout two rows at a time, and the readout time 412 for the two rows of the example sensor 200 is about 7.4 microseconds. In this example, the reset time 410 for resetting a subset of two rows is about 15.6 microseconds. Thus, the time between the first and second exposures 402, 404 and the time between the closely-timed image streams is about 15.6 microseconds, or about 0.03 percent of the frame period for a frame rate of 24 fps, and about 0.05, 0.08, 0.09, and 0.16 percent of the frame period for frame rates of 30, 50, 59.94, and 100 fps, respectively. In another configuration, for example, the sensor 200 produces first and second image streams which are temporally spaced by no more than about 7 microseconds. As such, for each frame the sensor 200 captures the a subsequent 404 (corresponding to the second image stream) no more than about 7 microseconds after capturing the preceding exposure 402 for that frame (corresponding to the first image stream). In other embodiments, the first and second exposures 402, 404 and corresponding image streams are temporally spaced by no more than about 4 microseconds, no more than about 2 microseconds, or no more than about 1 microsecond. In yet other embodiments, the first and second exposures 402, 404 are spaced by no more than about 1 millisecond, no more than about 100 microseconds, no more than about 50 microseconds, no more than about 25 microseconds, no more than about 20 microseconds, no more than about 16 microseconds, no more than 15.6 microseconds, no more than about 15 microseconds, or no more than about 10 microseconds. As indicated above, in some embodiments there are more than two exposures within each frame. In such cases, the delay between any two adjacent exposures may correspond to any of the above listed values or ranges of values. In various embodiments, the inter-exposure delay is less than about 0.01, 0.02, 0.03, 0.04, 0.05, 0.1, 0.2, 0.5, 1, 2, 5, 10, 20, or 30 percent of the frame period.

[0071] Additionally, as mentioned previously, because acquisition of each row (or subset of rows) is staggered in time from the immediately preceding row by a relatively minimal amount, the skew and resulting motion artifacts introduced by the rolling shutter are reduced. For example, the inter-row acquisition skew between the time the system begins to acquire image data for a row (or subset of rows) and begins to acquire image data for the immediately subsequent row corresponds to the readout time

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412 for a row (or subset of rows) in the illustrated embodiment. Likewise, an inter-row readout skew between the time the system completes reading out acquired image data for a row (or subset of rows) and completes reading out acquired image data for the subsequent row (or subset of rows) corresponds to the readout time 412 for a row (or subset of rows). In various embodiments, the inter-row acquisition skew and/or the inter-row readout skew is approximately equal to one readout time 412 for a row or subset of rows, or is less than or equal to approximately one, approximately 1.5, approximately 2, approximately 2.5, or approximately 3 readout times 412.

[0072] Extending the inter-row skew across all of the rows for Figure 4A, the total intra-exposure acquisition skew across the entire image from between the time the system begins to acquire a first of the rows (or subset of rows) and begins to acquire all of the rows or substantially all (e.g., at least 90, 95 or 99 percent) of the rows is given by approximately:

$$(M-1)*read\_out\_time, \qquad \text{(Eq. 1)}$$

[0073] Similarly, the intra-exposure readout skew between the time the system completes reading out a first of the rows and completes reading out substantially all of the rows may correspond to the same amount. As a specific example, for the 2740 row sensor described above, the intra-exposure acquisition and readout skews are both equal to about 10.1 milliseconds ((2740/2-1)*7.4 microseconds).

[0074] Further, the acquisition time for an entire exposure, from between the time when the system begins to acquire a first of the rows (or subsets of rows) and completes reading out substantially all of the rows for the exposure is approximately given by:

$$exposure\_time+[(M-1)*read\_out\_time]. \qquad \text{(Eq. 2)}$$

[0075] In further compatible embodiments, the image acquisition time is less than or equal to one of the following:

$$exposure\_time+[(M-1)*read\_out\_time] \qquad \text{(Eq. 3)}$$

$$exposure\_time+[(M-1)*1.5*read\_out\_time], \qquad \text{(Eq. 4)}$$

$$exposure\_time+[(M-1)*2*read\_out\_time], \qquad \text{(Eq. 5)}$$

$$exposure\_time+[(M-1)*2.5*read\_out\_time], \text{ or} \qquad \text{(Eq. 6)}$$

$$exposure\_time+[(M-1)*3*read\_out\_time]. \qquad \text{(Eq. 7)}$$

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[0076] The systems in each of the above-described specific examples record a first relatively lower exposure (e.g., short exposure) followed by a second relatively higher exposure (e.g., long exposure) for each frame. However, the number and order of the inter-frame exposures can vary, and can be customized as desired. For example, in one instance, each frame includes a long track followed by a short track. Additionally, the device can be configured to capture more than two exposures per frame, such as 3, 4, 5, 10 or more exposures. As just a few illustrative examples, the following capture patterns are possible including more than two exposures per frame: (1) long, short, long; (2) short, long, short; (3) short, short+x, short+x*2,...,short+x*k; (4) long, long-x, long-x*2,...long-x*k; (4) short, medium, long; (5) long, medium, short; (6) medium, long, short.

[0077] The diagrams 300, 400 of Figures 3A-3D and 4A correspond to configurations in which the sensor outputs the exposures in the same order for each row. For example, referring to Figure 4, each of the rows R1...RN outputs the short exposure 402 followed by the long exposure 404 for each frame. However, in some cases, the multiple exposure generator 206 is configured to cause the sensor 200 to output the first and second exposures in a different order depending on the row, providing greater creative flexibility.

[0078] Figure 4B shows one such example, where the order of the short and long exposures 402, 404 alternates from row to row (or from subset of rows to subset of rows). Accordingly, the first row R1 outputs the short exposure 402 followed by the long exposure 404, the second row R2 outputs the long exposure 404 followed by the short exposure, the third row outputs the short exposure 402 followed by the long exposure 404, and so on. In another similar embodiment, one or more of the integration times for the short exposure and the long exposure for the odd rows are different than the short exposure and the long exposure for the even rows.

[0079] In yet other instances, one or more of the rows capture only a single exposure per frame, while the remaining rows capture multiple exposures. For example, Figure 4C shows one such case where the odd rows output a single long exposure 402 per frame, while the even rows output three closely-timed exposures (e.g., short, medium, short) 404, 406, 408 per frame. Thus, it can be appreciated that a wide variety of possibilities exist for creating closely-timed exposures.

[0080] For the purposes of clarity, the terms "short" and "long" are used herein to distinguish different exposures, such as where one exposure has an integration time relatively shorter than another exposure(s), or shutter speed that is thus relatively longer than

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the other exposure(s). However, the above-described techniques are compatible with embodiments where other parameters instead of, or in addition to integration time, are manipulated and which affect the degree of exposure. Such parameters can include gain (e.g., analog gain), aperture, and ISO, for example. Thus, depending on the embodiment, where exposures are referred to as being "short" or a "long," it will be appreciated that they may actually be more accurately referred to as "low" or "high." As used herein, the terms "picture element reset time" and "picture element readout time" can refer to one or more of the amount of time it takes to read out a row of picture elements (e.g., pixels), a subset of more than one rows of picture elements, a single picture element, or some other non-row grouping of pixel elements, such as one or more columns of picture elements. In some cases, such as where multiple pixel elements are readout in parallel, for example, the readout time for a particular group (e.g., row or subset of rows of pixel elements) corresponds to the same amount of time as that of a single picture element.

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[0081] **[0078]** Figure 5 is a flow diagram illustrating an example process 500 for creating a blended output track from multiple tracks of closely-timed exposure frames. As will be described, according to the process 500 and other techniques described herein, the blending module 117 generally receives and processes tracks of closely-timed exposure frames. The blending module 117 may receive and or process the tracks on a frame-by-frame basis, or may operate on any portion of the tracks (e.g., 5, 10, 100, 1000 or more frames, or entire tracks) at any given time.

[0082] At block 502, the blending module 117 receives multiple tracks (or portions thereof) of video frames having closely timed exposures (e.g., spaced apart by no more than about 20, 16, 7, 4, or 2 microseconds). The blending module 117 can receive the tracks in a variety of ways. As one example, the blending module 117 resides in software executing on an external computing device. The camera 100 records the closely-timed exposure tracks to the memory device 114 and the tracks are transferred from the memory device 114 to the external computing device, which forwards the recorded tracks to the blending module 117 for processing. As another example, the blending module 117 resides in software or hardware on the camera 100 and receives the recorded tracks directly from the memory device 114 or sensor 112.

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[0083] At block 504, the blending module 117 processes the received exposures according to the desired (e.g., fixed or user-selectable) algorithm. The blending module 117 may blend together the first and second tracks according to the algorithm, generating the output track based on the first and second (or more) tracks. Some example blending techniques are shown and described with respect to Figures 6A-9.

[0084] At block 506, the blending module 117 provides the blended output track. For example, where the blending module 117 resides on-camera, it may provide the output image stream frame to the memory 114 for storage. Alternatively, the camera may stream the blended image track to the computing device 102 for external processing and/or storage. Where the blending module 117 operates on only a frame or other portion of each track at a time, the process 500 may then return to block 502, where the blending module 117 receives the first and second exposures for the next frame or group of frames in the respective track.

[0085] Figures 6A-6B illustrate example blending operations. For example, the blending module 117 may be capable of implementing the blending techniques shown in Figures 6A-6B. Generally, using these and other blending techniques, the blending module 117 is capable of providing an output track that incorporates desired content from the respective images while discarding undesired image content. The discarded image content can include noisy portions of one or more of the tracks, as well as other portions that are not needed to provide the desired aesthetic effect. Moreover, in some cases the user can select which content to include in the output track, providing improved creative flexibility.

[0086] Referring to Figure 6A, the blending operation 600 represents a scenario in which the camera captures first (e.g., long) 604 and second (e.g., short) 606 closely timed exposures, respectively, for each video frame. The width of the bars representing the long and short exposures 604, 606 generally corresponds to the dynamic range of the sensor, which in turn can correspond to the range of possible pixel values for the sensor 112 (e.g., 0 to 1023 for a 10-bit sensor, 0 to 4095 for a 12-bit sensor, 0 to 65,535 for a 16-bit sensor, etc.). Figure 6A corresponds to a configuration in which the output track has an expanded bit-depth as compared to the sensor 112, and has an improved dynamic range as compared to either of the individual tracks 604, 606 due to the selective inclusion of content from the two tracks 604, 606.

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[0087] As shown, for each of the long and short exposures 604, 606 a certain number of captured values will be relatively noisy, having a relatively lower signal-to-noise ratio (SNR). For example, the SNR is relatively low for lower pixel values and gradually increases as the measured pixel values increase. Moreover, the subject scene may include highlights in certain brighter regions. As indicated, the short exposure 606 can capture a significant portion of the highlights because of the shorter integration time, reducing the chance that the highlights will become washed out. On the other hand, as illustrated, the long exposure 604 in some cases does not capture much highlight detail due to the relatively longer integration time, which can lead to wash out.

[0088] The scene may also include darker regions including shadows, which can often be juxtaposed with brighter regions. As shown, the long exposure 604 may capture relatively more detail in these regions due to the long integration time. Conversely, the short exposure 606 may capture less detail in these regions due to the shorter integration time.

[0089] Also, as shown, the long and short exposures 604, 606 can also include content that corresponds to "normal" portions of the image scene. These portions may not be particularly dark or bright, for example, and can have a generally normal or medium brightness level. The labels used with respect to Figures 6A-6B ("shadows," "normal,""highlights") are used only for the purposes of illustrating the blending concepts, and are not limiting. For example, it will be appreciated that the shorter exposure may in some cases capture some amount of shadow content from the image scene. Likewise, the longer exposure in some instances will record some highlight detail.

[0090] In the illustrated example, the blending module 117 matches the light levels between the two exposures 604, 606. For example, the blending module 117 can shift the exposures with respect to one another by N bits (e.g., 1, 2, 4, 8, or more bits) prior to blending, or perform some other mathematical operation on one or more of the exposures. In the illustrated example, the short exposure 606 is shifted up by N bits, and is therefore multiplied by a factor of 2^N. In such cases, the long exposure 604 may be more exposed than the short exposure 606 by a factor of 2^N. As such, after the shifting, the light levels between the two exposures 604, 606 for corresponding image scene regions more closely match. Also, as shown, the noisiest content in the short exposure 606 is discarded in some cases.

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[0091] A variety of other processes are possible for adjusting the exposures 604, 606 with respect to one another prior to blending. For example, in some cases, the long exposure 604 is shifted or otherwise adjusted instead of the shorter exposure 606. In one instance, the long exposure 604 is shifted down by N bits instead of shifting the shorter exposure 606 up by N bits. Figure 3B, discussed below, shows one such embodiment. In other embodiments, the exposures 604, 606 are both shifted. For example, the exposures 604, 606 may be shifted in equal and opposite directions. In yet other cases, the system shifts the exposures 604, 606 in opposite directions but by different values. For example, where the first exposure 604 is exposed by a factor of 2^N greater than the second exposure 606, and where N = X+Y, the first exposure 604 may be shifted down by X bits, and the second exposure may be shifted up by Y bits. A variety of other embodiments are possible. For instance, instead of multiplying or dividing the pixel values for the exposures 604, 606, a subtraction, addition or other appropriate operation can be used.

[0092] After matching the light levels, the blending module blends together the exposures 604, 606. Three blending algorithms (i)-(iv) are shown for the purposes of illustration.

[0093] Referring to the first algorithm (i), the blending module 117 in one embodiment selects the image content of the long exposure 604 that corresponds to the line segment A-B for inclusion in the output track. In one example, the sensor is a 12-bit sensor, the short exposure is shifted up by 2 bits, and the line segment A-B corresponds to pixel values between 0 and 2048. The blending module 117 uses the measured values from long exposure as a reference to determine which pixel values to include in the blended output track. For example, the blending module 117 determines which measured pixels in the long exposure 604 have values from 0 to 2048, and incorporates those pixel values into the corresponding pixels in the blended output image. The values from the long exposure 604 are incorporated substantially directly, unmodified, into the output track while, in some alternative configurations, the blending module 117 performs some mathematical operation on the values prior to incorporation, such as a scaling, shifting or rounding.

[0094] The charts 608, 610 shown for the long and short exposures 604, 606, respectively, indicate the percentage of each track included in the output track according

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to the blending algorithm (i). For example, for pixel values between points A and B, 100% of the output track is composed of content from the long exposure 604.

[0095] The blending module 117 may alternatively use the *short* exposure 606 as a reference to determine which measured pixel values from the *long* exposure 604 to include in the output track for the portion A-B. In the example case, for instance, the blending module 117 determines which pixels in the short exposure 606 have measured values between 0 and 2048, and selects the measured values for the corresponding pixels in the long exposure 604 to include in the output track. In yet other instances, the blending module 117 uses other types of references. For example, the blending module 117 may calculate some combination (e.g., an average) of the measured values for the short and long exposure 606, 604 for each pixel, and use the calculated value as a reference to determine which pixels from the long exposure 604 to include in the output track. Similarly, while the remaining blending operations (e.g., those along the lines B-C, C-D, and those for the other example blending schemes (ii)-(iv)) are described as using the long exposure 604 as a reference, the short exposure 606, some combination of the short and long exposure 606, 604, or some other type of reference may be employed in those cases as well.

[0096] This image content from the long exposure 604 along the line segment A-B may include relatively good detail in the shadows. In some other cases, the blending module 117 blends together the short and long exposures 604, 606 to some degree for values along the line A-B. The amount of blending may be relatively constant, regardless of the input pixel values. Additionally, the blending may be biased in favor of one of the tracks, e.g., the long track 604. For example, the blending module 117 may perform a weighted average of input values from the long track 604 and the short track 606, where the long track has a higher weighting than the short track 606. In some cases, the degree of bias or weighting is controllable by a user, or automatically adjusts depending on the particular mode of operation. Blending algorithm (iv) described below shows an example where weighted averages are used to generate some of the image content in the blended output track.

[0097] Referring still to algorithm (i), the next portion of the output track corresponds to a combination of the image content from both the long and short exposures 604, 606 along the slanted line B-C. Moreover, the degree to which the respective exposures 604, 606 are included in the output exposure varies based on the measured

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input values. This can be in contrast to the portions of the output image corresponding to the line segments A-B and C-D (discussed below). For example, for the segments A-B and C-D, pixels from only one track are selected for inclusion in the output track, or the amount of blending is generally constant (e.g., weighted average), and irrespective of the measured input values.

[0098] A variety of operations are possible for the blending of the exposures 604, 606 for the segment B-C. For example, in some embodiments, the amount of the long track 604 included in the output track is greatest at the point B. Conversely, the amount of the short track 606 used in the blending operation is least at the point B. Moreover, for increasing pixel values x between B and C, the amount of the long track 604 included in the output track gradually decreases. Conversely, the amount of the second track 606 included in the output track increases, reaching a maximum at the point C. This is illustrated in the chart 608, which shows the percentage of the long exposure 604 in the output track decreasing linearly from 100 percent to 0 percent for increasing pixel values B to C. Conversely, the chart 610 shows the percentage of the short exposure 606 in the output track increasing linearly from 0 percent to 100 percent from B to C. In an example case, the sensor is a 12-bit sensor, the short exposure 606 is shifted up by 2 bits, B corresponds to a pixel value of 2048, and C corresponds to a pixel value of 4094. Taking as an example a point midway between B and C corresponding to a pixel value of 3071, the blending module 117 determines which pixels in the long exposure 604 (the reference exposure) have a value of 3071. Because the point is midway between B and C, the blending module 117 calculates the values for corresponding pixels in the output track according to the following equation:

$$out\_pixel\_val = 0.5 * long\_pixel\_val * 0.5 short\_pixel\_val . \quad \text{(Eq. 8)}$$

[0099] A linear interpolation is used for the portion B-C in some instances, and in one case the interpolant is given by:

$$y = 1 + \frac{x - B}{B - C}, \quad \text{(Eq. 9)}$$

where x corresponds to measured input pixel values between B and C, such that $B \le x \le C$, for example. In turn, the interpolant may be used to calculate the interpolated output pixel value for each value of x. For instance, the output pixel values may be calculated according to the following equation:

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$$out\_pixel\_val = y * long\_pixel\_val + (1-y) * short\_pixel\_val \quad \text{(Eq. 10)}$$

[0100] Other types of blending can be used for pixel values corresponding to the line segment B-C. In some cases, and unlike the linear interpolation technique, the amount of the respective exposures 604, 606 included in the blended exposure may not depend on the input values. For example, for this portion of the output track, the blending module 117 may calculate an average of the image content from the long exposure 604 and the image content of the short exposure 606, and include the average in the output track. A variety of other operations can be used instead of an average, including, without limitation, a sum, difference, weighted average, or the like. Blending algorithm (iii) described below incorporates a curved blending function.

[0101] In one embodiment, the blending module 117 selects the image content of the short exposure 606 corresponding to the line C-D to complete the output track, and does not blend the exposures for this portion of the output track. For example, referring to 12-bit sensor example, the point C may correspond to a pixel value of 4095, which corresponds to a saturated value for the long exposure 604. The blending module 117 may therefore determine which pixels in the long exposure 604 have a saturated value of 4095 and incorporate into the output image the values from the corresponding pixels in the short exposure 606. As indicated, the image content along the line C-D includes relatively good highlight detail. In other cases, some degree of blending may be used for the portion of the output track corresponding to the segment C-D. For example, for the portion C-D, the blending module 117 may perform a weighted average or other operation that is similar to those described above with respect to the segment A-B. However, the weighted average may be biased in favor of the short track 606 instead of the long track 604 for the portion C-D, unlike for the portion A-B. Algorithm (iv) described below incorporates a blending function along these lines.

[0102] Thus, according to such blending techniques, the blending module 117 uses the short exposure 606 to preserve the highlights in the resulting output track, correcting for any possible loss of highlight detail. The track that is made up of the short exposure frames may therefore be referred to as a "highlight protection track" or "highlight correction track," for example.

[0103] As indicated by the arrows, one or more of the points A, B, C and D can be adjusted to adjust the blending profile. This can greatly affect both the dynamic

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range and the motion characteristic of the resulting output track. For example, the lengths of the segments A-B and C-D can significantly alter the dynamic range of the image. Moreover, the motion effect can be tuned by adjusting length of the segment B-C or the particular blending operation (e.g., linear interpolation, weighted average, etc.) that is used on this portion. Specific motion control operations are described in greater detail below with respect to Figure 8.

[0104] Blending algorithm (ii) is similar to blending algorithm (i), except that, as indicated by the shorter line segment B-C, the blending module 117 blends together the long and short exposures 604, 606 for a much smaller portion of the output track. Moreover, as indicated by the relatively long line segment A-B, a larger portion of the long track 604 is included directly in the output track as compared as compared to algorithm (i).

[0105] As shown by the charts 608, 610 for algorithm (iii), a blending module 117 implementing algorithm (iii) applies a curve on the measured input values to generate the output track. While a variety of different curves are possible, the blending module 117 in the illustrated example applies an "S" curve over the portion of the output track corresponding to the pixel values between the points B and C. The curve may be a sigmoid curve, or some other type of curve. As with the previous examples, one or more of the points A, B, C, and D can be adjusted to change length of the various segments and corresponding blending profile. In one instance, the curve is applied over the entire output track.

[0106] There may additionally be more than three portions (A-B, B-C, C-D) of the output track having discrete blending profiles. Algorithm (iv) shows such a case where there are separate blending profiles for five different portions of the output track: (1) A-B – direct incorporation of the long track 604; (2) B-C – weighted average, where the long track 604 is weighted heavier than short track 606; (3) C-D – linear interpolation between long track 604 and short track 606; (4) D-E – weighted average, wherein the short track 606 is weighted heavier than the long track 604; and (5) E-F – direct incorporation of the short track 606.

[0107] Referring now to Figure 6B, the illustrated blending operation is similar to that of Figure 6A in that system again captures and blends together first (e.g., long) and second (e.g., long) closely timed exposures 604, 606. However, unlike the operation shown in Figure 6A, Figure 6B shows a configuration where the blending

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module 117 does not expand the bit-width of the output track as compared to the input tracks. Rather, the bit-width remains the same. As one example, the sensor 112 is a 12-bit sensor and thus outputs 12-bit long and short exposures 604, 606, although other bit-widths are possible. The blending module 117 performs light level matching by shifting the long exposure 604 down by a number (e.g., 2, 4, 8, etc.) of bits with respect to the long exposure 604. However, unlike the operation shown in Figure 4A, the shifted portion is preserved in the embodiment of Figure 6B. The first and second tracks 604, 606 are then blended together according to the selected algorithm, creating a 16-bit output track. Three example blending algorithms (i), (ii) and (iii) are shown, although a wide variety of other possibilities exist. As shown, the noisiest content in the long exposure 604 is discarded in some cases, while still preserving some detail in the shadows.

[0108] While described with respect to a number of specific examples in Figures 6A-6B, the blending can occur in a variety of additional manners. For example, the blending can be based on contrast levels, as described below with respect to Figure 9.

[0109] Figure 7 shows a blending process 700 for creating an output exposure from multiple closely-timed exposures. Although described with respect to single first and second exposures for the purposes of illustration, the operations described below with respect to the process 700 may instead be performed on entire tracks of first and second exposures or portions thereof.

[0110] At blocks 702A, 702B, the sensor 112 captures first (e.g., long) and second (e.g., long) exposures. At block 704A, 704B, the blending module 117 or other component processes the captured exposures.

[0111] For example, referring to Figures 6A-6B, in some cases one or more of the exposures 604, 606 is adjusted before blending, e.g., to match the light levels between the two exposures. In some of these cases, the blending module 117 shifts one or both exposures 604, 606 and therefore multiplies or divides the pixel values by a corresponding factor of two. However, sensor pixels in some cases output non-zero values even when no light is incident on the pixels (e.g., when the lens cap is on the sensor), creating "non-zero black" values. It can desirable to take this into account prior to the blending. For example, multiplying these "non-zero black" values in the light matching process can complicate later processing stages or produce other undesirable results.

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[0112] Thus, in one embodiment the module 117 subtracts an offset (e.g., a black offset) from the first and/or second exposures prior to the light matching. The module 117 then performs the light matching or other mathematical operation(s) on the exposures, e.g., multiplying each of the exposures by a predetermined factor. Finally, the blending module 117 can add an offset to the first and second exposures, such as a black offset having the same magnitude as the value that was subtracted prior to the light matching.

[0113] In some configurations, at block 704A, 704B the blending module performs one or more operations on the first and second exposures to improve the compression of the image data. For example, in one instance, the image processing module 116 combines select (e.g., low) frequency components of wavelets from both the first and second exposures to improve compression efficiency. The image processing module 116 may also implement a pre-emphasis curve one or more of the exposures (e.g., the darker, shorter exposure). Example pre-emphasis functions are described in greater detail in the '967 patent (e.g., with respect to Figures 8, 8A, 11 and columns 11-12 of the '967 patent) and are incorporated by reference herein. Such techniques can improve the efficiency or other quality of the compression. For example, in some cases, pre-emphasis or other techniques can avoid or reduce the amount of compression that occurs on lower bits of the particular exposure(s).

[0114] At block 706, the blending module 117 receives parameters for use in the blending operation. For example, the blending parameters generally define how the first and second exposures will be combined. In some cases, for example, the system 100 provides an interface to set one or more of the blending parameters. For example, the system 100 displays a graphical user interface (GUI) to the user that the user can interact with to set the parameter(s). The GUI or other interface can be provided via software on a display of an external computer, or may instead be provided on the camera, depending on the configuration.

[0115] In one instance, the GUI includes a slider or one or more other icons that the user can manipulate to adjust the blending parameters. The graphic 707 is similar to those shown with respect to the algorithms of Figures 6A-6B. Accordingly, the positions of "A," "B," "C," and "D" generally define how to blend the first and second exposures ("EXP. 1," "EXP. 2"). As indicated in Figure 7, the user in some cases be able to adjust the position of "B" and "C" using the interface, thereby setting how much of the

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first and second (or more) exposures to include in the resulting output track, and what portions of the tracks should be blended together. In some cases the user can adjust the position of "A" and/or "D" instead of or in addition to "B" and "C." In addition to the illustrated example, a number of other compatible interfaces are possible. Moreover, the interface can allow users to adjust a variety of other parameters.

[0116] In another configuration, the user can select a "highlight protection" value, which determines the amount of highlight protection to employ. Referring to Figures 6A-6B, the selected "highlight protection" value may generally the exposure (e.g., integration time) of the exposures 606 in the short track. In one embodiment, the user can select a number of stops (e.g., 2, 3, 4, 5, or 6 stops) of highlight protection to include. For example, if the user selects 2 stops of highlight protection, the exposure for the short exposure 606 track will be 2 stops less than that of the long track 604. For example, where the long track 604 exposure value is 1/48 seconds, the exposure for the short track 606 will be set to 1/192 seconds.

[0117] In another configuration, the system provides the user with a menu of pre-set algorithms which each have a particular creative effect. Each of the pre-set algorithms have pre-determined blending parameters (e.g, "B" and "C" values). The particular pre-set algorithms may also determine what type of processing occurs in blocks 704A, 704B (e.g., linear interpolation, weighted average, "S" curve, etc.) in some cases.

[0118] At block 708, the blending module 117 performs the blending operation based on the selected blending parameters. For example, the blending module 117 can perform the blending generally in the manner described above with respect to Figures 5-6B. Finally, at block 710, the blending module 117 outputs the blended exposure (or track of exposures). For example, the blended exposures are provided for storage and/or playback to the user.

[0119] In some embodiments, the system 100 provides the user with generally real-time feedback. For example, as the user changes one or more blending parameters or selects a different pre-set blending algorithm, the system plays back the blended output track or a portion thereof for user review on a camera or computer monitor. Thus, the user can make adjustments on the fly to achieve the desired visual effect.

[0120] Returning to block 708, in some embodiments the blending module 117 blends the closely-timed tracks by determining, according to the selected algorithm, which portions of each track are properly exposed. For example, for each exposure, the

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blending module 117 flags the properly exposed pixels for inclusion in the combined output image. According to another embodiment, the blending module 117 compares pixels from one exposure to corresponding pixel(s) in the other exposure(s), and according to a predetermined algorithm, calculates the corresponding pixel value in the blended output.

[0121] As described, any of the blending techniques can generally be implemented on a frame-by-frame basis, for example, or at some other granularity, and a wide variety of compatible blending techniques are possible. In certain configurations, more than one frame from the first and/or second (or more) tracks are compared or otherwise analyzed in generating the output track. For example, in such cases the blending module 117 compares frames n-w,...,n,...,n+x from the first track to frames n-y,...,n,...n+z from the second track to generate frame n in the output image stream, where n is the current output track frame.

Controlling Motion Effect

[0122] As discussed, the image capture techniques described herein efficiently use the frame period to provide tracks having different exposures levels within individual frames. The inter-exposure delay is relatively small, resulting in substantially reduced or no temporal gap between the differently exposed tracks. For example, there may be substantially no visual separation between objects in one track as compared to the same objects in another track. Moreover, as discussed, the inter-exposure skew for the individual tracks is relatively minimal. According to certain aspects, the system exploits these and other aspects to control the motion effect in the combined output track, such as the amount or quality of blur, in addition to providing the dynamic range benefits described herein. For example, motion artifacts in the combined output stream can be substantially reduced, removed, or controlled in a desired fashion. Additionally, some techniques described herein reduce or eliminate the amount of motion artifact detection and processing that can be necessary with some conventional approaches.

[0123] Figure 8 shows a process 800 of providing an output image track having controlled motion effect. At block 802, the blending module 117 receives at least two closely-timed tracks, which can be recorded according to any of the techniques described herein. For example, the tracks may be any of those shown and described in Figures 3A-6B. At block 804, the blending module 117 receives a set of motion control

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parameters. These parameters generally define the motion control algorithm that the blending module 117 performs when selectively combining tracks. As with the dynamic range blending parameters (e.g., amount of "highlight protection") described above, the motion control parameters may be user-selectable or fixed, depending on the implementation. In some cases, the user is provided a menu having a list of various motion control techniques to choose from. These may be any of the techniques described below with respect to block 806, or some other technique(s).

[0124] At block 806, the process 800 combines the tracks of closely-timed images to create an output image stream having the desired motion effect. A variety of motion control techniques are possible.

[0125] Where multiple, tracks of closely-timed images are recorded at different exposure levels, one of the tracks may be relatively blurry, similar to conventional video recordings. For example, significant blurring may be present in relatively long integration time tracks, such as those shown in Figures 3A-4C and 6A-6B. However, other tracks may be sharper and include reduced or minimal blurring. For example, the short integration time exposures shown in Figures 3A-4C and 6A-6B may be relatively sharper. Typical video recordings (e.g., 24 fps with a 180 degree shutter) show a generally constant blurring for moving objects, without sharper references. However, what the human eye sees when viewing the scene in person is closer to a combination of both the blurred references to the objects as well as discrete, sharper references to the moving objects.

[0126] To mimic this effect, in some embodiments, the blending module 117 uses both the more blurry track(s) and the sharper track(s) to control the motion effect, create an output track that includes both the blurred and sharp references to moving objects. For instance, referring again to Figures 6A-6B, the amount or quality of the motion effect included in the output track can be controlled by adjusting the blending parameters, such as the positions of A, B, C, D or the type of blending operations used.. As one example, a user can control the amount of blurred and sharp references represented in the output track by adjusting the position of B and C, thereby adjusting the length and position of the line segments A-B, B-C, and C-D. In particular, referring to algorithm (i) shown in Figure 6A, for increasing measured pixel values along the line B-C where the blending module 117 implements an interpolation function, the output track will tend to include a varying mixture of blurred references and sharper references.

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Specifically, the output track along the line B-C includes an increasingly significant portion of image content from the short track 606 and a correspondingly lesser portion of the long track 604. As such, portions of the output track corresponding to the line segment B-C will include a varying mixture of relatively more blurred references to image scene objects from the long track 604 and relatively sharper references to the same image scene objects from the short track 606. In this manner, the blending module 117 can create an output track that more closely mimics what the human eye would see if watching the scene in person. The system or a user can additionally adjust the positions of B and C to modify the effect.

[0127] In addition, gradually shifting the relative contributions of the larger track 604 and the shorter track 606 (or vice versa) in an incremental manner, such as by using linear interpolation or a curve function, can help limit or prevent any banding or other undesirable visual artifacts that may occur from a more abrupt change in the relative contributions of the two tracks. In some cases, the gradual shifting can also help to reduce the amount of lower SNR image content that is incorporated in the output track (e.g., from the shorter track 606), improving image quality.

[0128] In another example, the blending module 117 implements a weighted average of the long and short exposures 604, 606 for portions of the output track along the line B-C. For example, a 50/50 weighted average may result in an output track having a generally even mixture of sharper content from the short track 606 and blurred content from the longer track 604. The weightings can be adjusted to tailor the effect. In one embodiment, the system provides the user with an interface to control how much of the motion effect from each track to include in the resulting output track. Generally, the system can employ a wide variety of other functions instead of or in combination with the illustrated ones.

[0129] In yet further configurations, the blending module 117 can set the relative weighting of the short and long tracks 604, 606 in the output track based on a contrast level. For instance, the blending module 117 processes measured input values of the long track 604, the short track 606, or a combination thereof to determine a contrast level in particular image regions, and uses the determined contrast level to select the relative weighting between the long track 604 and the short track 606 for pixels within those image regions. For example, the blending module 117 applies a high-pass filter on the image data for the short track 606 (and/or long track 606) to determine high contrast

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regions. For relatively high contrast regions, the blending module 117 weights the short track 606 heavier than the long track 604 in the output track. For relatively lower contrast regions, the blending module 117 may weight the long track 604 higher, or weight the two tracks equally. In this manner, the resulting output track can include both sharp references to moving objects (from the high contrast regions of the short track 606) and blurred references to moving objects (from adjacent, relatively lower contrast regions of the long track 604). The blending module 117 can identify lower contrast regions instead of, or in addition to, higher contrast regions, by performing a low pass filter on the long and/or short exposures 604, 606, for example.

[0130] Moreover, for portions of the output track corresponding to the line segments A-B and/or C-D, a user in some embodiments adjusts the motion effect by controlling the amount of each image to include in the output track. For example, the user can adjust the bias value in a weighted average blend operation to control the weight each input track is given in the blending operation. For example, the system may provide a slider, other GUI, or another input mechanism to allow the user tailor the effect.

[0131] In another embodiment, the blending module 117 is configured to blend the tracks together in a manner that more closely matches the motion effect of a traditional camera (e.g., 24 fps with a 180 degree shutter). For example, a customized motion estimation algorithm may be used to match the motion blur of one or more of the tracks to that of a traditional camera. For example, referring to Figure 3A, the blur in the shorter integration time track 302 may be increased to match that of the longer integration time track 304. In one embodiment, the blur matching is done before the blending of the exposures, although it can be done afterwards in other implementations.

[0132] At block 908, the blending module 117 outputs the motion-adjusted track for playback or further processing.

Terminology/Additional Embodiments

[0133] Embodiments have been described in connection with the accompanying drawings. However, it should be understood that the figures are not drawn to scale. Distances, angles, etc. are merely illustrative and do not necessarily bear an exact relationship to actual dimensions and layout of the devices illustrated. In addition, the foregoing embodiments have been described at a level of detail to allow one of ordinary skill in the art to make and use the devices, systems, etc. described herein. A

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wide variety of variation is possible. Components, elements, and/or steps can be altered, added, removed, or rearranged. While certain embodiments have been explicitly described, other embodiments will become apparent to those of ordinary skill in the art based on this disclosure.

[0134] Conditional language used herein, such as, among others, "can," "could," "might," "may," "e.g.," and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0135] Depending on the embodiment, certain acts, events, or functions of any of the methods described herein can be performed in a different sequence, can be added, merged, or left out all together (e.g., not all described acts or events are necessary for the practice of the method). Moreover, in certain embodiments, acts or events can be performed concurrently, e.g., through multi-threaded processing, interrupt processing, or multiple processors or processor cores, rather than sequentially. In some embodiments, the algorithms disclosed herein can be implemented as routines stored in a memory device. Additionally, a processor can be configured to execute the routines. In some embodiments, custom circuitry may be used.

[0136] The various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein can be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. The described functionality can be implemented in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the disclosure.

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[0137] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein can be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor can be a microprocessor, but in the alternative, the processor can be any conventional processor, controller, microcontroller, or state machine. A processor can also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0138] The blocks of the methods and algorithms described in connection with the embodiments disclosed herein can be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module can reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer-readable storage medium known in the art. An exemplary storage medium is coupled to a processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium can be integral to the processor. The processor and the storage medium can reside in an ASIC. The ASIC can reside in a user terminal. In the alternative, the processor and the storage medium can reside as discrete components in a user terminal.

[0139] While the above detailed description has shown, described, and pointed out novel features as applied to various embodiments, it will be understood that various omissions, substitutions, and changes in the form and details of the devices or algorithms illustrated can be made without departing from the spirit of the disclosure. As will be recognized, certain embodiments of the inventions described herein can be embodied within a form that does not provide all of the features and benefits set forth herein, as some features can be used or practiced separately from others. The scope of certain inventions disclosed herein is indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

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WHAT IS CLAIMED IS:

1. A method of obtaining image data using a digital imaging sensor comprising a picture element array of rows and columns, the method comprising:

using a plurality of picture elements in the picture element array to capture light corresponding to a first image at a first exposure level;

using the plurality of picture elements in the picture element array to capture light corresponding to a second image at a second exposure level different than the first exposure level;

converting the light captured by the plurality of picture elements for the first image to digital measurements; and

converting the light captured by the plurality of picture elements for the second image to digital measurements,

wherein the step of using the plurality of picture elements in the picture element array to capture light corresponding to the second image at the second exposure level begins prior to the completion of the step of converting the light captured by the plurality of picture elements for the first image to digital measurements,

further wherein the step of converting the light captured by the plurality of picture elements for the first image to digital measurements substantially completes prior to the beginning of the step of converting light captured by the plurality of picture elements for the second image to digital measurements.

2. The method of Claim 1, wherein the plurality of picture elements form subsets of one or more rows of pixels, and wherein the pixels in each of the subsets are captured and converted as a group.

3. The method of Claim 1, wherein, for a picture element, there is an inter-exposure delay of less than approximately 100 picture element reset times between converting light captured by the picture element for the first image and beginning to capture light corresponding to the second image at the second exposure level by the picture element.

4. The method of Claim 3, wherein the inter-exposure delay is less than approximately 10 picture element reset times.

5. The method of Claim 4, wherein the inter-exposure delay is approximately one picture element reset time.

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6. The method of Claim 1, wherein the first and second images are captured using a rolling shutter technique, wherein the capturing of light by each subset of one or more rows of picture elements begins after the capturing of light by the preceding subset of one or more rows of picture elements begins.

7. The method of Claim 6, wherein an inter-picture element delay from when the capturing of light by a particular subset of one or more rows of picture elements begins and when the capturing of light by the subsequent subset of one or more rows of picture elements begins is less than approximately two picture element read out times.

8. The method of Claim 7, wherein the inter-picture element delay is approximately one picture element readout time.

9. The method of Claim 1, further comprising selectively combining the first image and the second image to create a combined image having a wider dynamic range than either of the first image or the second image.

10. The method of Claim 9, wherein an exposure time for the second image is longer than an exposure time for the first image, and wherein the first image provides highlight protection.

11. The method of Claim 9, wherein first and second images are captured for a plurality of video frames to create a first track of first images for the plurality of video frames and to create a second track of second images for the plurality of video frames, and wherein combined images are created for each of the plurality of video frames.

12. The method of Claim 9, wherein the first image has a first bit-depth, the second image has a second bit-depth, and the combined image has a bit-depth that is greater than either of the first or second bit-depths.

13. The method of Claim 9, further comprising selectively incorporating content from the first image and content from the second image into the combined image.

14. The method of Claim 13, wherein said selectively incorporating comprises blending together content from the first image with content from the second image for at least some of the combined image, wherein portions of the captured image scene represented by the blended content include first references from the first image to one or more image scene objects and second references from the second image to the same image scene objects, the second references depicting significantly more motion blur than the first references.

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15. The method of Claim 14, wherein said blending content from the first image and the second image comprises varying the relative amounts of first image content and second image content included in the blended content in response to magnitudes of picture element values from one or more of the first image and the second image.

16. The method of Claim 15, wherein said varying comprises performing a linear interpolation function.

17. The method of Claim 15, wherein said varying comprises performing a weighted averaging function.

18. The method of Claim 14, further comprising adjusting the amount of blended content to include in the combined image in response to user input.

19. The method of Claim 14, wherein said selectively incorporating further comprises substantially directly incorporating content from one or more of the first and second images for at least some of the combined image.

20. The method of Claim 14, wherein said selectively incorporating further comprises discarding relatively low signal-to-noise content from one or more of the first and second images.

21. An imaging system, comprising:

a plurality of picture elements arranged in an array; and

control circuitry configured to:

capture light corresponding to a first image at a first exposure level with the plurality of picture elements in the picture element array;

capture light corresponding to a second image at a second exposure level different than the first exposure level with the plurality of picture elements in the picture element array;

convert the light captured by the plurality of picture elements for the first image to digital measurements; and

convert light captured by the plurality of picture elements for the second image to digital measurements,

wherein the control circuitry begins the capturing of the light corresponding to the second image at the second exposure level prior to the completion of the converting of the light captured for the first image to digital measurements,

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further wherein the control circuitry substantially completes the converting of the light for the first image to digital measurements prior to the beginning of the converting of the light for the second image to digital measurements.

22. The imaging system of Claim 21, wherein the plurality of picture elements form subsets of one or more rows of pixels.

23. The imaging system of Claim 21 wherein, for a picture element, there is an inter-exposure delay of less than approximately 100 picture element reset times between when the control circuitry converts light captured by the picture element for the first image and begins to capture light corresponding to the second image at the second exposure level by the picture element.

24. The imaging system of Claim 23, wherein the inter-exposure delay is less than approximately 10 picture element reset times.

25. The imaging system of Claim 24, wherein the inter-exposure delay is approximately one picture element reset time.

26. The imaging system of Claim 21, wherein the control circuitry is configured to capture the first and second images using a rolling shutter technique, wherein the capturing of light by each subset of one or more rows of picture elements begins after the capturing of light by the preceding subset of one or more rows of picture elements begins.

27. The imaging system of Claim 26, wherein an inter-picture element delay from when the capturing of light by a particular subset of one or more rows of picture elements begins and when the capturing of light by the subsequent subset of one or more rows of picture elements begins is less than approximately two picture element read out times.

28. The imaging system of Claim 27, wherein the inter-picture element delay is approximately one picture element readout time.

29. The imaging system of Claim 21, further comprising a blending module configured to selectively combining the first image and the second image to create a combined image having a wider dynamic range than either of the first image or the second image.

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30. The imaging system of Claim 29, wherein an exposure time for the second image is longer than an exposure time for the first image, and wherein the first image provides highlight protection.

31. The imaging system of Claim 29, wherein the control circuitry is configured to capture first and second images for a plurality of video frames to create a first track of first images for the plurality of video frames and to create a second track of second images for the plurality of video frames, and is further configured to create combined images for each of the plurality of video frames.

32. The imaging system of Claim 29, wherein the first image has a first bit-depth, the second image has a second bit-depth, and the combined image has a bit-depth that is greater than either of the first or second bit-depths.

33. The imaging system of Claim 29, wherein the control circuitry is further configured to selectively incorporate content from the first image and content from the second image into the combined image.

34. The imaging system of Claim 33, wherein the control circuitry selectively incorporates the content by blending together content from the first image with content from the second image for at least some of the combined image, wherein portions of the captured image scene represented by the blended content include first references from the first image to one or more image scene objects and second references from the second image to the same image scene objects, the second references depicting significantly more motion blur than the first references.

35. The imaging system of Claim 34, wherein the control circuitry blends together the content from the first image and the second image by varying the relative amounts of first image content and second image content included in the blended content in response to magnitudes of picture element values from one or more of the first image and the second image.

36. The imaging system of Claim 35, wherein the control circuitry performs a linear interpolation function to vary the relative amounts.

37. The imaging system of Claim 35, wherein the control circuitry performs a weighted averaging function to vary the relative amounts.

38. The imaging system of Claim 34, wherein the control circuitry adjusts the amount of blended content to include in the combined image in response to user input.

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39. The imaging system of Claim 34, wherein the control circuitry further selectively incorporates the content by substantially directly incorporating content from one or more of the first and second images for at least some of the combined image.

40. The imaging system of Claim 34, the control circuitry further selectively incorporates the content by discarding relatively low signal-to-noise content from one or more of the first image and the second image.

41. A method of processing image data, comprising:

receiving first image data corresponding to a plurality of picture elements in a picture element array used to capture light corresponding to a first image at a first exposure level;

receiving second image data corresponding to the plurality of picture elements in the picture element array used to capture light corresponding to a second image at a second exposure level; and

selectively combining the first image data and the second image data to create combined image data corresponding to a combined image having a wider dynamic range than either of the first image or the second image,

wherein using the plurality of picture elements in the picture element array to capture light corresponding to the second image at the second exposure level began prior to the completion of converting the light captured by the plurality of picture elements for the first image to digital measurements, further wherein converting the light captured by the plurality of picture elements for the first image to digital measurements substantially completes prior to the beginning of the step of converting light captured by the plurality of picture elements for the second image to digital measurements.

42. A method of obtaining image data using a digital imaging sensor, the method comprising:

capturing a first image with the sensor at a first exposure level;

capturing a second image with the sensor at a second exposure level different from the first exposure level;

outputting the first image; and

outputting the second image, wherein said capturing of the first image begins before said capturing of the second image begins, said capturing of the first

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image and said capturing of the second image overlap in time, and said outputting of the first image and said outputting of the second image do not overlap in time.

43. The method of Claim 42, wherein the first and second images are captured using a rolling shutter technique.

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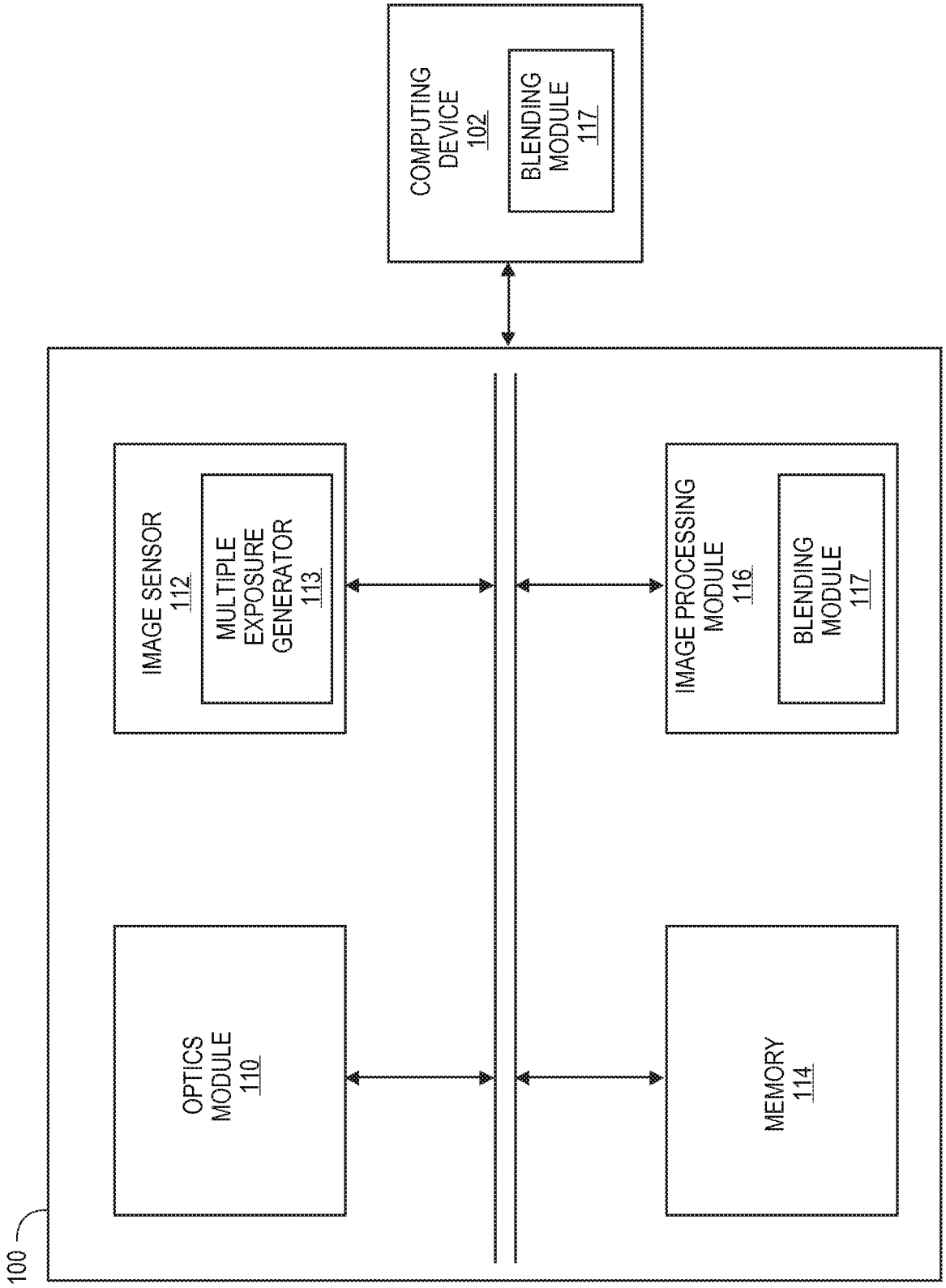

COMPUTING DEVICE 102
BLENDING MODULE 117
IMAGE SENSOR 112
MULTIPLE EXPOSURE GENERATOR 113
IMAGE PROCESSING MODULE 116
BLENDING MODULE 117
OPTICS MODULE 110
MEMORY 114
100

FIG. 1

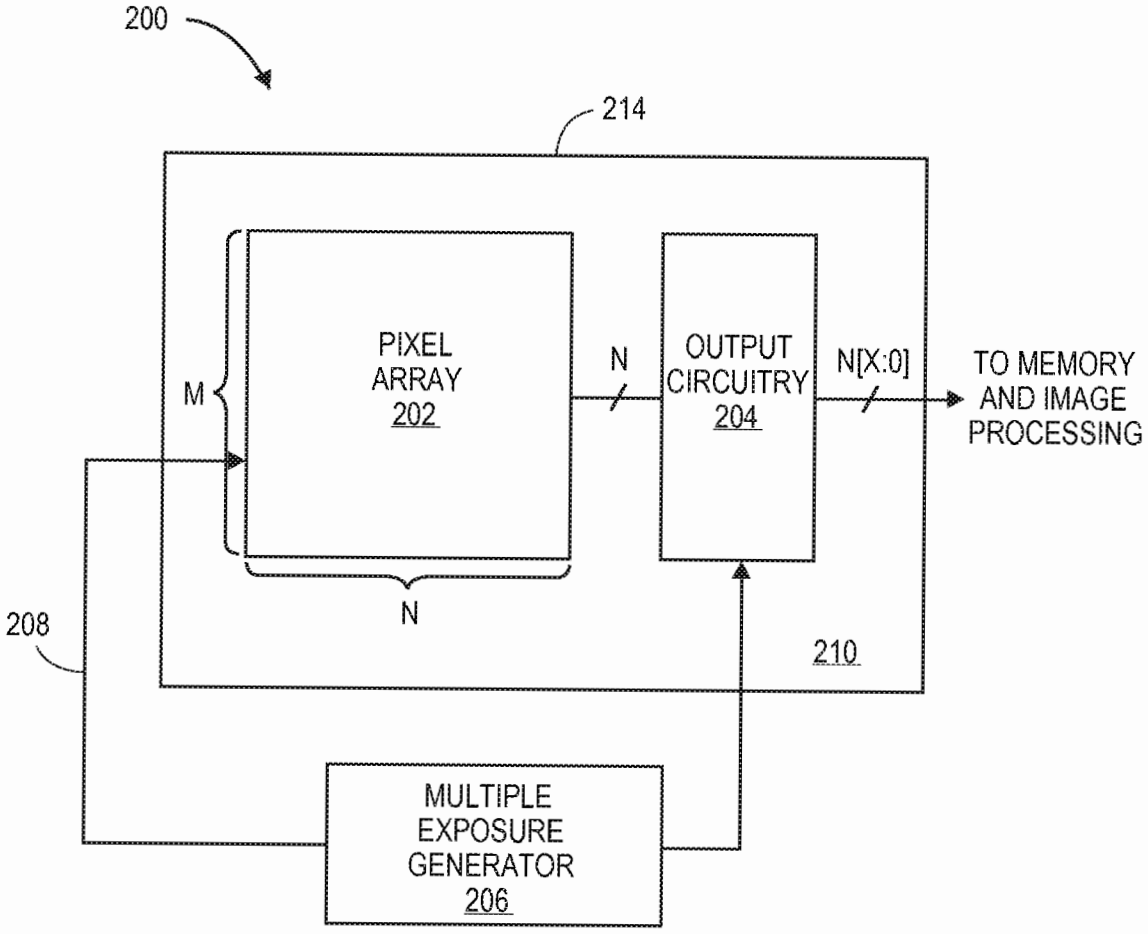

200
214
PIXEL ARRAY 202
M
N
OUTPUT CIRCUITRY 204
N[X:0]
TO MEMORY AND IMAGE PROCESSING
208
210
MULTIPLE EXPOSURE GENERATOR 206

FIG. 2

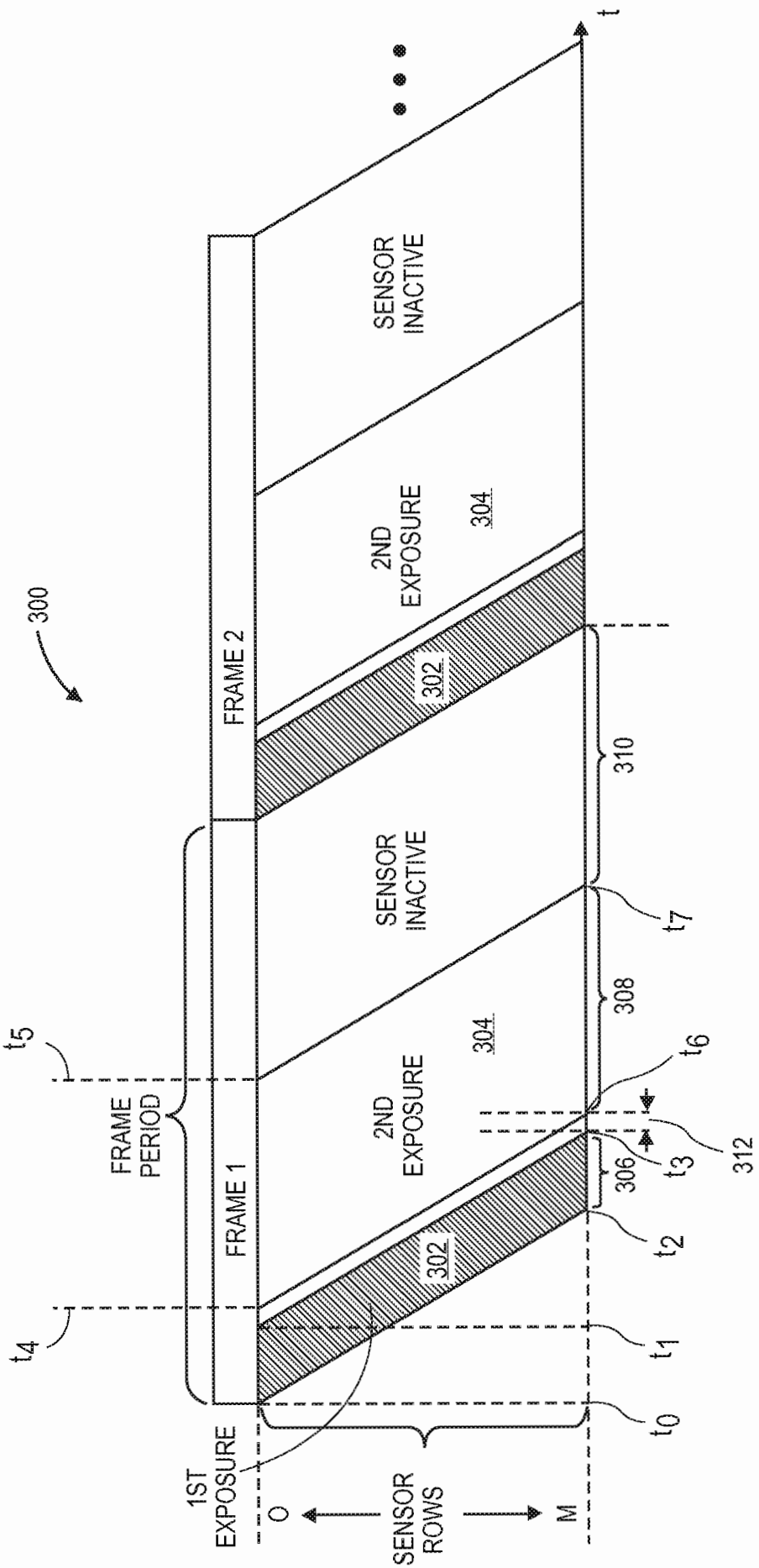

300
t
SENSOR INACTIVE
2ND EXPOSURE
304
302
FRAME 2
310
SENSOR INACTIVE
308
304
2ND EXPOSURE
302
FRAME 1
FRAME PERIOD
t5
t4
t7
t6
312
306
t3
t2
t1
t0
1ST EXPOSURE
0
SENSOR ROWS
M

FIG. 3A

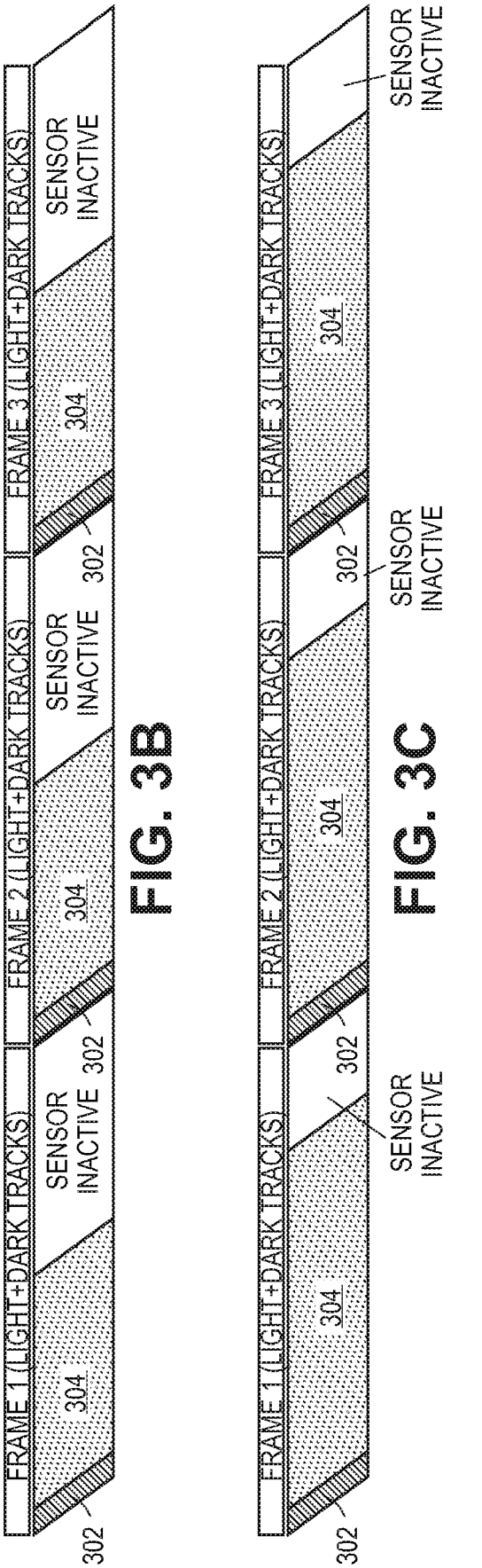


FIG. 3B

FIG. 3C



FIG. 3D



FIG. 3E

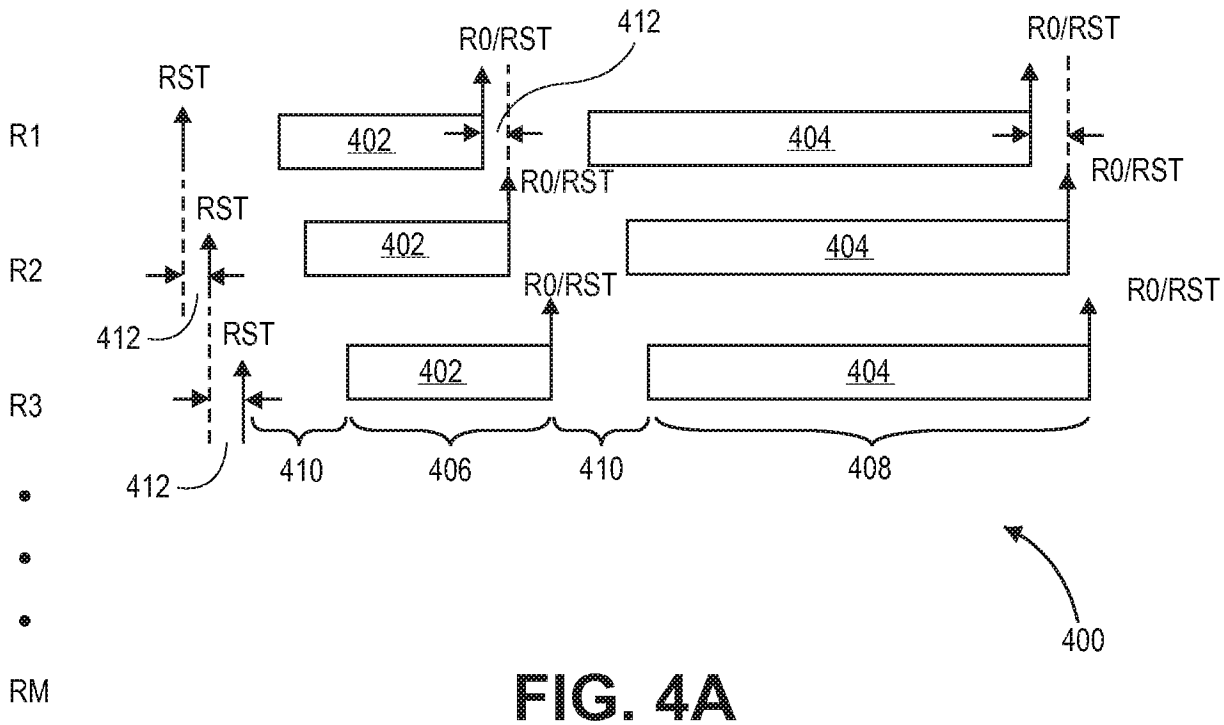


FIG. 4A

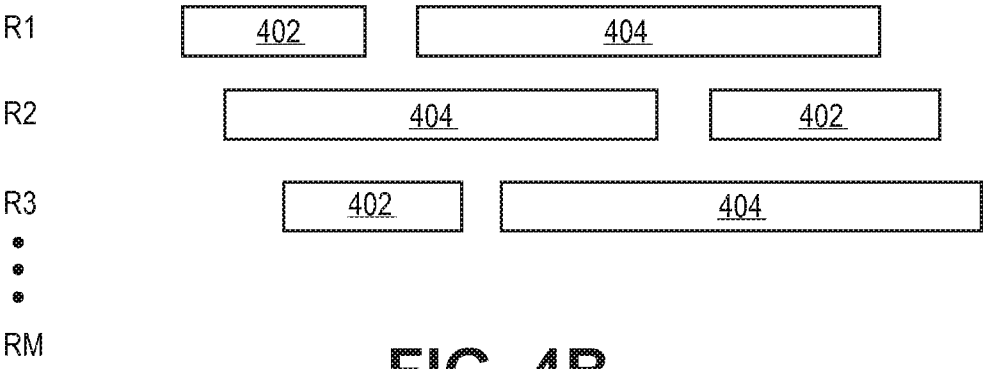


FIG. 4B

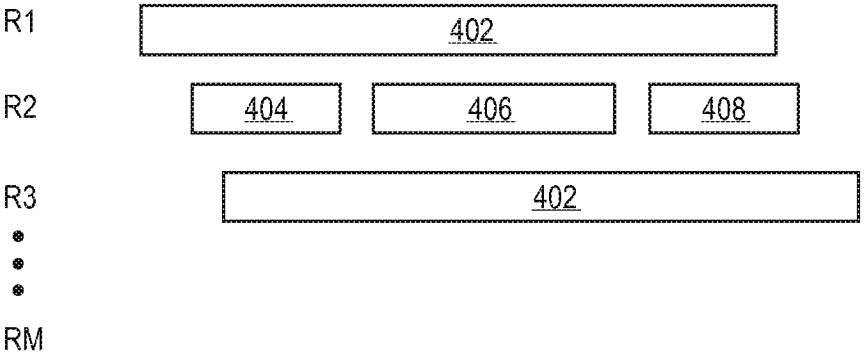


FIG. 4C

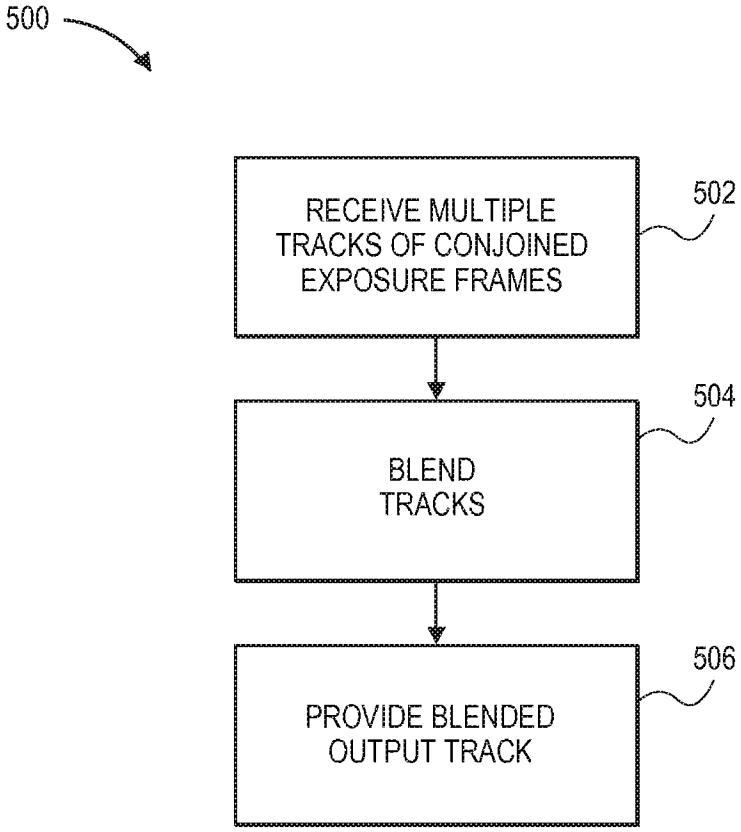

500
RECEIVE MULTIPLE TRACKS OF CONJOINED EXPOSURE FRAMES
502
BLEND TRACKS
504
PROVIDE BLENDED OUTPUT TRACK
506

FIG. 5

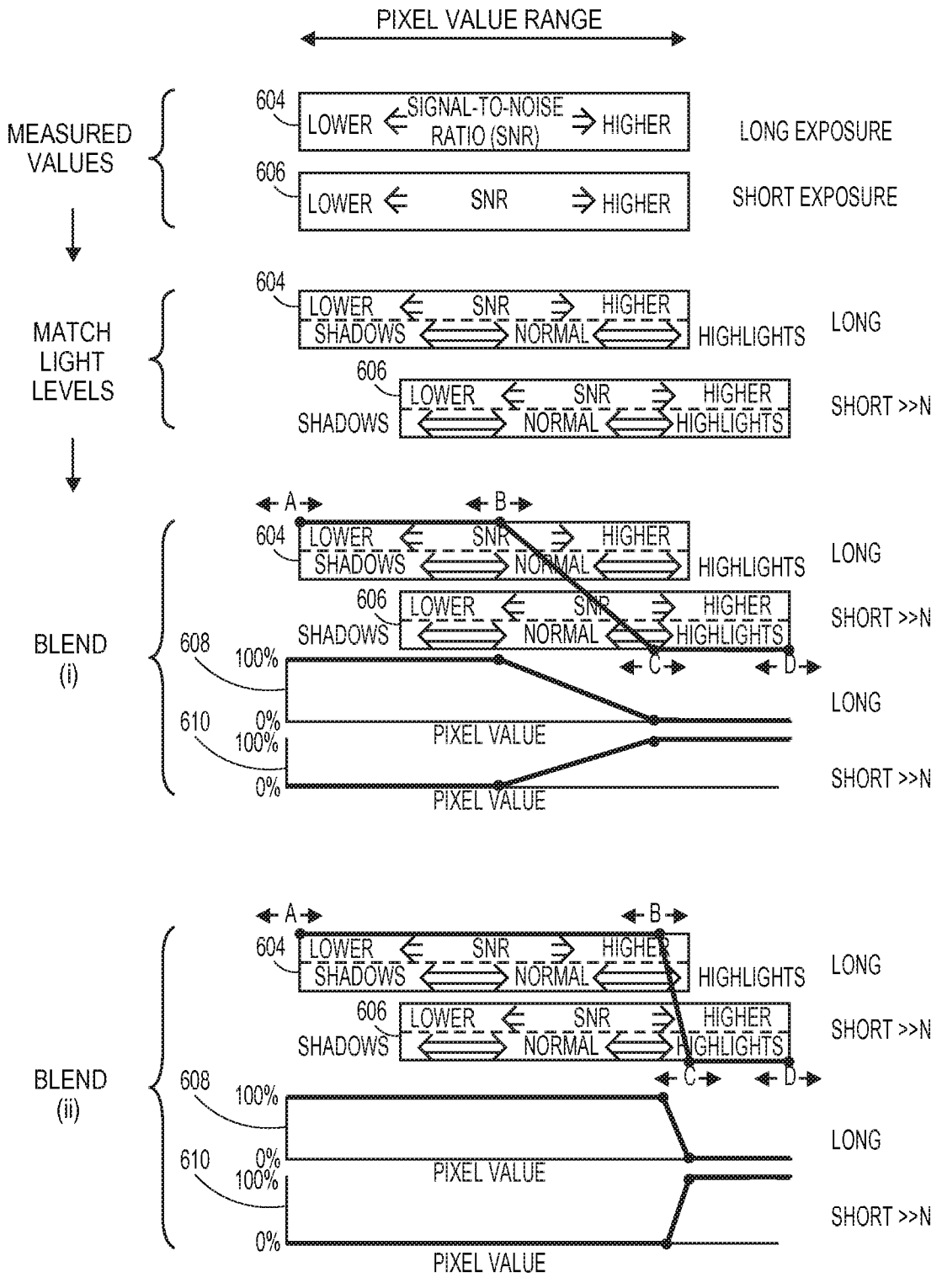

PIXEL VALUE RANGE
MEASURED VALUES
604
LOWER
SIGNAL-TO-NOISE RATIO (SNR)
HIGHER
LONG EXPOSURE
606
LOWER
SNR
HIGHER
SHORT EXPOSURE
MATCH LIGHT LEVELS
604
LOWER
SNR
HIGHER
SHADOWS
NORMAL
HIGHLIGHTS
LONG
606
LOWER
SNR
HIGHER
SHADOWS
NORMAL
HIGHLIGHTS
SHORT >>N
BLEND (i)
A
B
C
D
608
100%
0%
PIXEL VALUE
LONG
610
100%
0%
PIXEL VALUE
SHORT >>N
BLEND (ii)
A
B
C
D
608
100%
0%
PIXEL VALUE
LONG
610
100%
0%
PIXEL VALUE
SHORT >>N

FIG. 6A

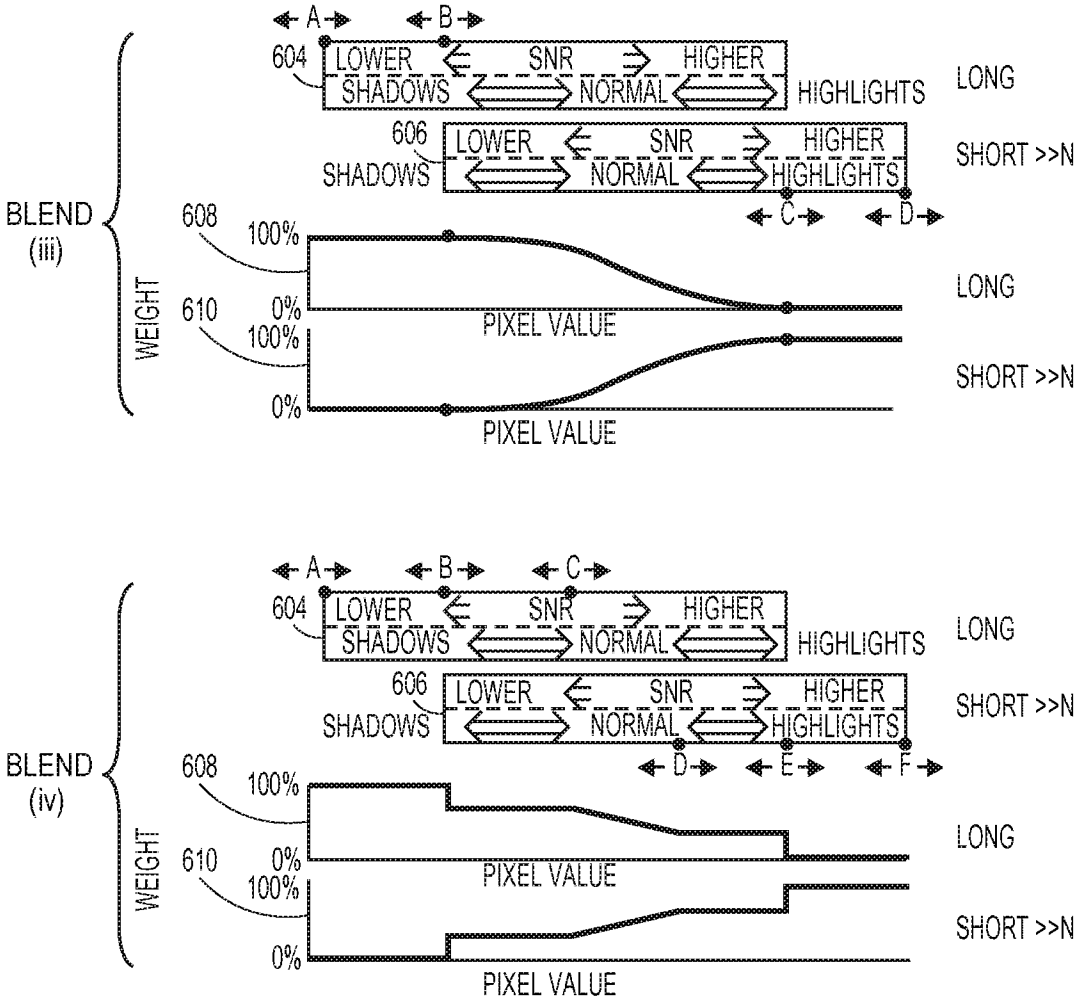

BLEND
(iii)
A
B
604
LOWER
SNR
HIGHER
SHADOWS
NORMAL
HIGHLIGHTS
LONG
606
LOWER
SNR
HIGHER
SHADOWS
NORMAL
HIGHLIGHTS
SHORT >>N
C
D
608
100%
0%
PIXEL VALUE
LONG
610
100%
0%
PIXEL VALUE
SHORT >>N
WEIGHT
BLEND
(iv)
A
B
C
604
LOWER
SNR
HIGHER
SHADOWS
NORMAL
HIGHLIGHTS
LONG
606
LOWER
SNR
HIGHER
SHADOWS
NORMAL
HIGHLIGHTS
SHORT >>N
D
E
F
608
100%
0%
PIXEL VALUE
LONG
610
100%
0%
PIXEL VALUE
SHORT >>N
WEIGHT

FIG. 6A
(CONT.)

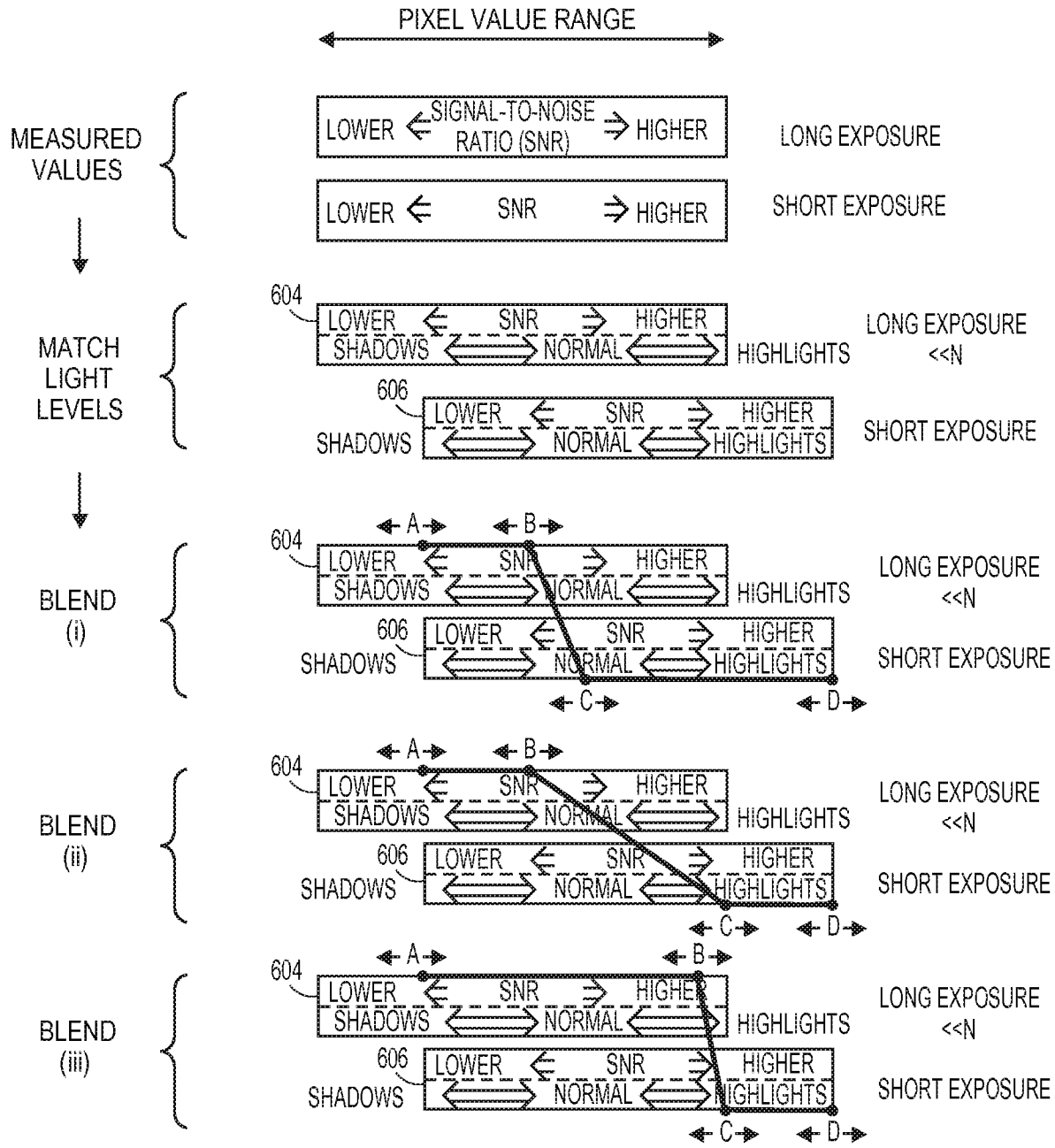

PIXEL VALUE RANGE
MEASURED VALUES
LOWER SIGNAL-TO-NOISE RATIO (SNR) HIGHER
LONG EXPOSURE
LOWER SNR HIGHER
SHORT EXPOSURE
MATCH LIGHT LEVELS
604
LOWER SNR HIGHER
SHADOWS NORMAL HIGHLIGHTS
LONG EXPOSURE <<N
606
LOWER SNR HIGHER
SHADOWS NORMAL HIGHLIGHTS
SHORT EXPOSURE
BLEND (i)
A B C D
BLEND (ii)
BLEND (iii)

FIG. 6B

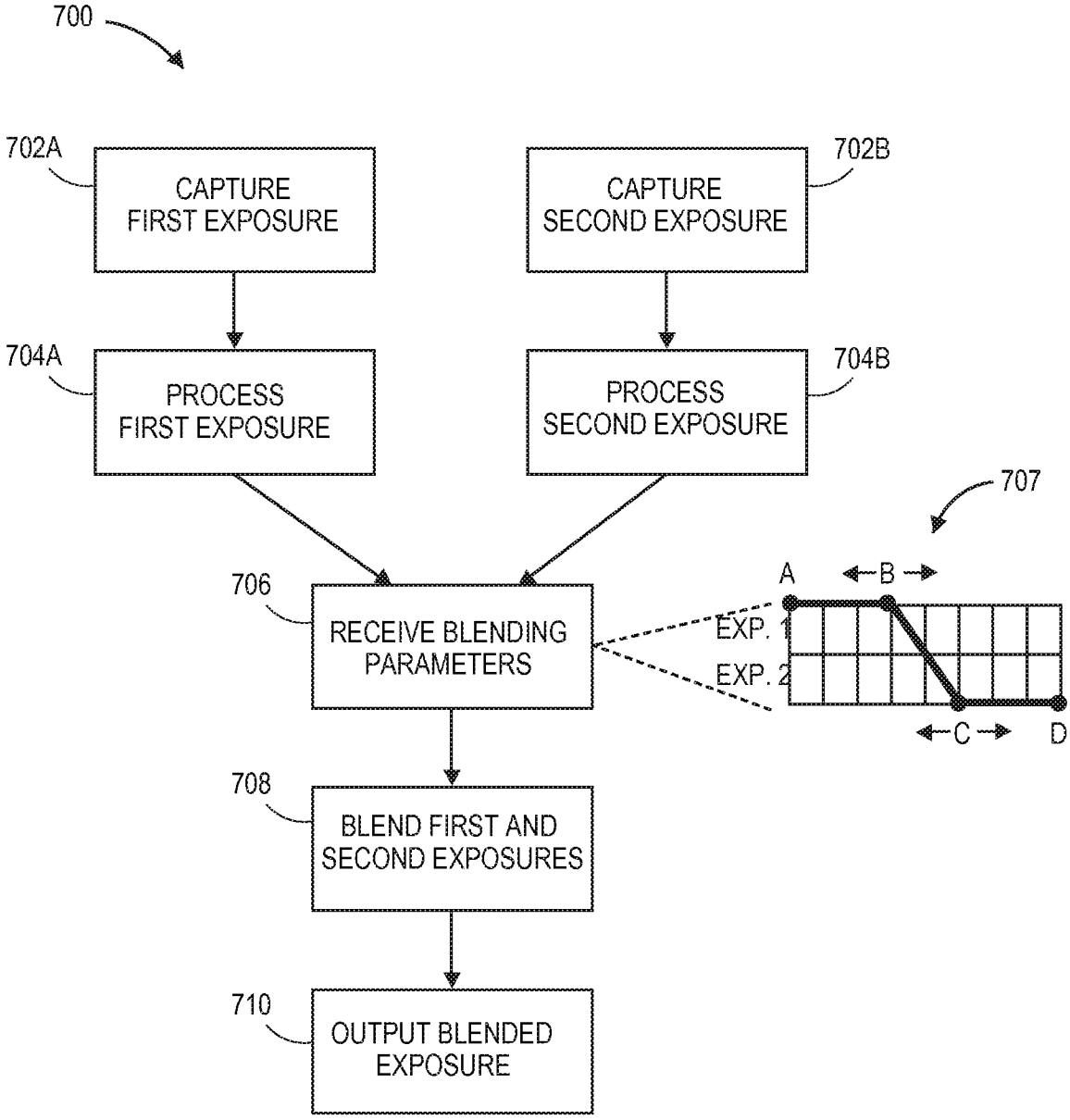

700
702A
CAPTURE FIRST EXPOSURE
702B
CAPTURE SECOND EXPOSURE
704A
PROCESS FIRST EXPOSURE
704B
PROCESS SECOND EXPOSURE
707
706
RECEIVE BLENDING PARAMETERS
A
B
EXP. 1
EXP. 2
C
D
708
BLEND FIRST AND SECOND EXPOSURES
710
OUTPUT BLENDED EXPOSURE

FIG. 7

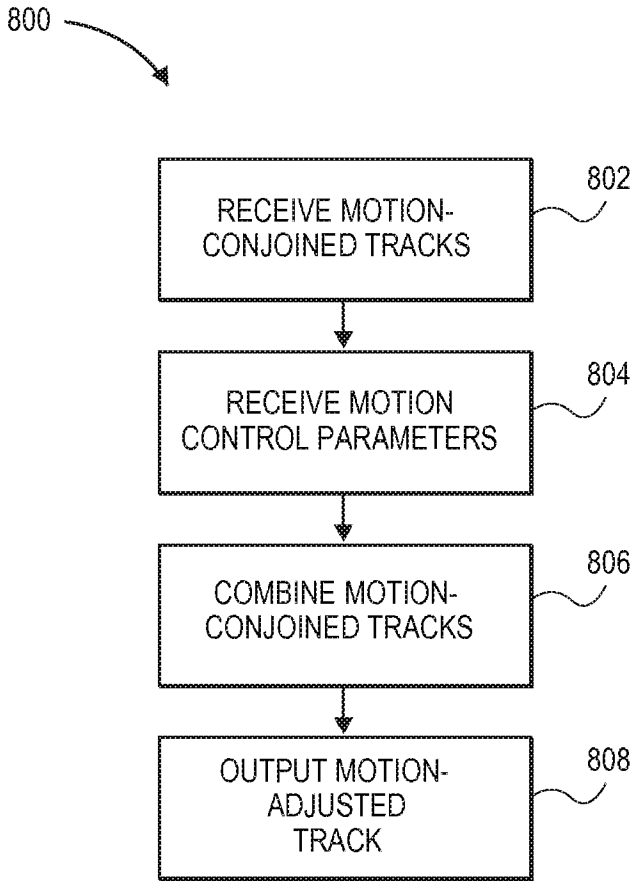

800
RECEIVE MOTION-CONJOINED TRACKS
802
RECEIVE MOTION CONTROL PARAMETERS
804
COMBINE MOTION-CONJOINED TRACKS
806
OUTPUT MOTION-ADJUSTED TRACK
808

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/048670

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N5/235 H04N5/355 H04N5/353
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 278 490 B1 (FUKUDA HIDETOSHI [JP] ET AL) 21 August 2001 (2001-08-21)	1-13, 21-33, 41-43
Y	column 8, line 41 - column 12, line 14 figures 6-8	14-20, 34-40
Y	US 2010/165122 A1 (CASTORINA ALFIO [IT] ET AL) 1 July 2010 (2010-07-01) the whole document	14-20, 34-40
X	US 2005/057674 A1 (KRYMSKI ALEXANDER I [US] ET AL) 17 March 2005 (2005-03-17) paragraph [0005] paragraph [0032] - paragraph [0053] figures 11-15	1-8, 21-28, 41-43

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 October 2011	07/11/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Didierlaurent, P

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International application No
PCT/US2011/048670

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 847 398 B1 (FOSSUM ERIC R [US]) 25 January 2005 (2005-01-25) column 2, line 26 - column 4, line 26 column 5, line 20 - line 23 figures 3-20	1-8, 21-28, 41-43
X	US 2006/109373 A1 (KURANE HARUHISA [JP]) 25 May 2006 (2006-05-25) paragraph [0033] - paragraph [0042] paragraph [0074] - paragraph [0104] figures 1-3,11	1-8, 21-28, 41-43
X	US 2010/187401 A1 (KAWAHITO SHOJI [JP]) 29 July 2010 (2010-07-29) paragraph [0130] paragraph [0175] - paragraph [0198] figures 3,8-16	1-11,13, 21-31, 33,41-43
A	US 2009/153710 A1 (JOHN GEORGE C [US]) 18 June 2009 (2009-06-18) paragraph [0014] - paragraph [0027] figures 1,3-6	14-20, 34-40

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6278490 B1	21-08-2001	NONE	
US 2010165122 A1	01-07-2010	NONE	
US 2005057674 A1	17-03-2005	NONE	
US 6847398 B1	25-01-2005	NONE	
US 2006109373 A1	25-05-2006	JP 4389766 B2 JP 2006148621 A	24-12-2009 08-06-2006
US 2010187401 A1	29-07-2010	WO 2007083704 A1 JP 4649623 B2	26-07-2007 16-03-2011
US 2009153710 A1	18-06-2009	NONE	

(12) 特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
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(43) 国際公開日
2012 年 9 月 7 日(07.09.2012)

WIPO | PCT

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WO 2012/117931 A1

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H04N 5/359 (2011.01)

(21) 国際出願番号: PCT/JP2012/054390

(22) 国際出願日: 2012 年 2 月 23 日(23.02.2012)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

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特願 2012-011405 2012 年 1 月 23 日(23.01.2012) JP

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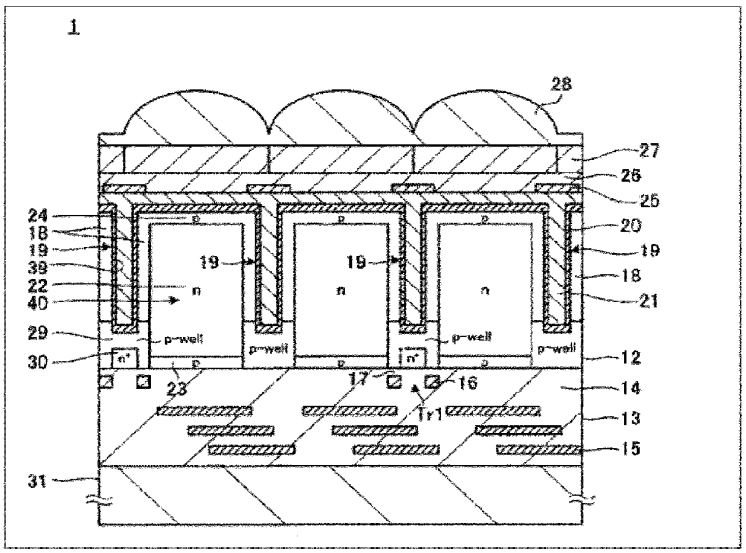
(81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

[続葉有]

(54) **Title**: SOLID STATE IMAGING DEVICE AND FABRICATION METHOD THEREFOR, AND ELECTRONIC INSTRUMENT

(54) 発明の名称 : 固体撮像装置、固体撮像装置の製造方法及び電子機器

[図2]



(57) **Abstract**: The present invention relates to the provision of a solid state imaging device having improved characteristics such as reduced optical color mixing, a fabrication method for the same, and an electronic instrument. An electronic instrument using the solid state imaging device is also provided. A solid state imaging device provided with a substrate (12) and a plurality of photoelectric conversion units (40) formed in the substrate (12), wherein element isolation sections (19) having insulating layers (21) buried therein are formed. The element isolation sections (19) are constituted by insulating layers (20) that have a fixed electrical charge and that are formed so as to cover the surface of the inner walls of groove sections (30), the groove sections (30) being formed in the depth direction from the optical incidence side of the substrate (12).

(57) 要約: 本技術は、光学混色の低減等の特性をさらに向上させた固体撮像装置を提供することができる固体撮像装置、固体撮像装置の製造方法及び電子機器に関する。また、その固体撮像装置を用いた電子機器を提供する。基板１２と、基板１２に形成された複数の光電変換部４０とを備える固体撮像装置において、絶縁膜２１が埋め込まれた素子分離部１９を形成する。素子分離部１９は、基板１２の光入射側から深さ方向に形成された溝部３０内において、溝部３０の内壁面を被覆するように形成された固定電荷を有する絶縁膜２０で構成されている。

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明　細　書

発明の名称 ：

固体撮像装置、固体撮像装置の製造方法及び電子機器

技術分野

[0001] 本開示は、裏面照射型の固体撮像装置とその製造方法及び電子機器に関する。

背景技術

[0002] 近年、基板上の配線層が形成される側とは反対側から光を照射する、裏面照射型の固体撮像装置が提案されている（下記特許文献１参照）。裏面照射型の固体撮像装置では、光照射側に配線層や回路素子等が形成されないため、基板に形成された受光部の開口率を高くできる他、入射光が配線層等に反射されることなく受光部に入射されるので、感度の向上が図られる。

特許文献１の固体撮像装置は、光学混色を低減するために、画素境界に遮光膜を設けている。

先行技術文献

特許文献

[0003] 特許文献1：特開２０１０－１８６８１８号公報

発明の概要

発明が解決しようとする課題

[0004] このような固体撮像装置において、光学混色の低減等のさらなる特性向上が求められている。

[0005] 本開示は、光学混色の低減等の特性をさらに向上させた固体撮像装置を提供する。また、その固体撮像装置を用いた電子機器を提供する。

課題を解決するための手段

[0006] 本開示の第１の側面の固体撮像装置は、基板と、基板に形成された複数の光電変換部とを備える。また、基板の光入射側から深さ方向に形成された溝

部内において、溝部の内壁面を被覆するように形成された固定電荷を有する絶縁膜で構成された素子分離部を備える。

[0007] 本開示の第２の側面の固体撮像装置は、基板と、前記基板に形成された複数の光電変換部とを備える。また、基板の光入射側から深さ方向に形成された溝部と、溝部の内壁面を被覆するように設けられた膜を備え、中空構造を有する素子分離部を備える。

[0008] 本開示の第１の側面の固体撮像装置の製造方法は、基板に、光電変換部を有する複数の画素を形成する工程と、基板の裏面側から深さ方向にかけて所望の深さの溝部を形成する工程を有する。次に、溝部の内壁面に固定電荷を有する絶縁膜を形成し、素子分離部を形成する工程を有する。

[0009] 本開示の第２の側面の固体撮像装置の製造方法は、基板に、光電変換部を有する複数の画素を形成する工程と、基板の裏面側から深さ方向にかけて所望の深さの溝部を形成する工程を有する。次に、溝部の内部に中空部が形成されるように前記溝部の内壁面に所望の膜を成膜することで素子分離部を形成する工程を有する。

[0010] 本開示の電子機器は、光学レンズと、光学レンズに集光された光が入射される上述の固体撮像装置と、固体撮像装置から出力される出力信号を処理する信号処理回路とを備える。

発明の効果

[0011] 本開示によれば、固体撮像装置において、混色低減等の特性のさらなる向上が図られる。また、その固体撮像装置を用いることにより、画質の向上が図られた電子機器が得られる。

図面の簡単な説明

[0012] [図1]本開示の第１の実施形態に係る固体撮像装置の全体構成を示す図である。

[図2]本開示の第１の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図3]本開示の第１の実施形態に係る固体撮像装置の平面レイアウトである。

[図4]図４のＡ及び図４のＢは、本開示の第１の実施形態に係る固体撮像装置の製造方法を示す図である。

[図5]図４のＣ及び図４のＤは、本開示の第１の実施形態に係る固体撮像装置の製造方法を示す図である。

[図6]本開示の第１の実施形態に係る固体撮像装置と従来の固体撮像装置の要部のポテンシャル分布図である。

[図7]第１の実施形態の変形例１に係る固体撮像装置の平面レイアウトである。

[図8]第１の実施形態の変形例２に係る固体撮像装置の平面レイアウトである。

[図9]本開示の第２の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図10]図１０のＡ～図１０のＣは、本開示の第２の実施形態に係る固体撮像装置の製造方法を示す図である。

[図11]本開示の第３の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図12]本開示の第４の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図13]図１３のＡ及び図１３のＢは、本開示の第４の実施形態に係る固体撮像装置の製造方法を示す図である。

[図14]図１４のＣは、本開示の第４の実施形態に係る固体撮像装置の製造方法を示す図である。

[図15]本開示の第５の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図16]本開示の第６の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図17]本開示の第７の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図18]図１８のＡ及び図１８のＢは、本開示の第７の実施形態に係る固体撮像装置の製造方法を示す図である。

[図19]本開示の第８の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図20]図２０のＡ及び図２０のＢは、本開示の第８の実施形態に係る固体撮像装置の製造方法を示す図である。

[図21]変形例に係る固体撮像装置の要部の断面構成を示す図である。

[図22]本開示の第９の実施形態に係る電子機器の概略構成図である。

発明を実施するための形態

[0013] 本発明者らは、特許文献１の固体撮像装置において、以下の課題を発見した。

[0014] 裏面型の固体撮像装置では、フォトダイオードが形成される半導体層が表面照射型の固体撮像装置と比較して薄く形成される。このため、従来の表面照射型の固体撮像装置では、フォトダイオードで溢れた信号電荷は半導体層の深さ方向（縦方向）にオーバーフローさせる構成が採られていたが、裏面照射型の固体撮像装置では、半導体層の深さ方向にオーバーフローさせることができない。このため、裏面照射型の固体撮像装置では、フォトダイオードで溢れた電子は、フローティングディフュージョンへ流れるように構成されている（いわゆる、ラテラルオーバーフロー）。

[0015] ラテラルオーバーフロー構造を採用する場合、フォトダイオードから溢れた電子が、フローティングディフュージョン側に流れるか、隣接するフォトダイオード側に流れるかは、基板内のポテンシャルによって決まる。したがって、電荷蓄積時に、フォトダイオードとフローティングディフュージョンとの間のポテンシャルを、隣接するフォトダイオード間のポテンシャルよりも高く設定することで、溢れた電子を随時フローティングディフュージョンに転送することができる。このため、溢れた電子をフローティングディフュージョンに転送可能な構成とする場合、飽和電荷量（Ｑｓ）の低下が大きな課題となる。一方、飽和電荷量を大きくした場合には、長時間蓄積時に白点

画素から溢れた信号電荷が隣接する画素に漏れ込んでいくことでブルーミングが発生し、解像度劣化、画質劣化の一因となる。

また、画素境界に遮光膜を設ける構造では、斜めの光が入った場合に遮光膜の下で発生する混色を完全に抑制することができない。

本開示の実施形態では、混色低減、ブルーミングの抑制や飽和特性の向上が可能な固体撮像装置について説明する。

[0016] 以下に、本開示の実施形態に係る固体撮像装置とその製造方法、及び電子機器の一例を、図１～図２２を参照しながら説明する。本開示の実施形態は以下の順で説明する。なお、本開示は以下の例に限定されるものではない。

１．第１の実施形態：固体撮像装置（４画素で一つのフローティングディフュージョン部を共有する例）

１－１　固体撮像装置全体の構成

１－２　要部の構成

１－３　固体撮像装置の製造方法

１－４　変形例１

１－５　変形例２

２．第２の実施形態：固体撮像装置（素子分離部内に遮光膜が形成される例）

３．第３の実施形態：固体撮像装置（素子分離部の基板裏面側の端部のみがｐ型半導体領域に接する例）

４．第４の実施形態：固体撮像装置（素子分離部が基板を貫通する例）

５．第５の実施形態：固体撮像装置（素子分離部内に形成された遮光層が配線層に接続される例）

６．第６の実施形態：固体撮像装置（素子分離部に２層の固定電荷膜を形成する例）

７．第７の実施形態：固体撮像装置（素子分離部が中空構造である例）

８．第８の実施形態：固体撮像装置（素子分離部が中空構造である例）

８－１　変形例

９．第９の実施形態：電子機器

[0017] 〈１．第１の実施形態：固体撮像装置〉

［１－１　固体撮像装置全体の構成］

図１は、本開示の第１の実施形態に係るＣＭＯＳ型の固体撮像装置の全体を示す概略構成図である。

本実施形態の固体撮像装置１は、シリコンからなる基板１１上に配列された複数の画素２を有する画素領域３と、垂直駆動回路４と、カラム信号処理回路５と、水平駆動回路６と、出力回路７と、制御回路８等を有して構成される。

[0018] 画素２は、フォトダイオードからなる光電変換部と、複数の画素トランジスタとから構成され、基板１１上に、２次元アレイ状に規則的に複数配列される。画素２を構成する画素トランジスタは、転送トランジスタ、リセットトランジスタ、選択トランジスタ、アンプトランジスタで構成される４つのＭＯＳトランジスタであってもよく、また、選択トランジスタを除いた３つのトランジスタであってもよい。

[0019] 画素領域３は、２次元アレイ状に規則的に配列された複数の画素２を有する。画素領域３は、実際に光を受光し光電変換によって生成された信号電荷を増幅してカラム信号処理回路５に読み出す有効画素領域と、黒レベルの基準になる光学的黒を出力するための黒基準画素領域（図示せず）とから構成されている。黒基準画素領域は、通常は、有効画素領域の外周部に形成されるものである。

[0020] 制御回路８は、垂直同期信号、水平同期信号及びマスタクロックに基づいて、垂直駆動回路４、カラム信号処理回路５、及び水平駆動回路６等の動作の基準となるクロック信号や制御信号などを生成する。そして、制御回路８で生成されたクロック信号や制御信号などは、垂直駆動回路４、カラム信号処理回路５及び水平駆動回路６等に入力される。

[0021] 垂直駆動回路４は、例えばシフトレジスタによって構成され、画素領域３の各画素２を行単位で順次垂直方向に選択走査する。そして、各画素２のフ

ォトダイオードにおいて受光量に応じて生成した信号電荷に基づく画素信号を、垂直信号線を通してカラム信号処理回路５に供給する。

[0022] カラム信号処理回路５は、例えば、画素２の列毎に配置されており、１行分の画素２から出力される信号を画素列毎に黒基準画素領域（図示しないが、有効画素領域の周囲に形成される）からの信号によって、ノイズ除去や信号増幅等の信号処理を行う。カラム信号処理回路５の出力段には、水平選択スイッチ（図示せず）が水平信号線１０とのあいだに設けられている。

[0023] 水平駆動回路６は、例えばシフトレジスタによって構成され、水平走査パルスを順次出力することによって、カラム信号処理回路５の各々を順番に選択し、カラム信号処理回路５の各々から画素信号を水平信号線１０に出力させる。

[0024] 出力回路７は、カラム信号処理回路５の各々から水平信号線１０を通して、順次に供給される信号に対し信号処理を行い出力する。

[0025] ［１－２　要部の構成］

図２に、本実施形態の固体撮像装置１の画素領域３における断面構成を示し、図３に、本実施形態の固体撮像装置１の画素領域３の平面レイアウトを示す。本実施形態の固体撮像装置１は、裏面照射型のＣＭＯＳ型固体撮像装置を例としたものであり、４つの光電変換部に対して所要の画素トランジスタを共有させた、いわゆる４画素共有を１単位とした例である。また、以下の説明では、第１導電型をｐ型とし、第２導電型をｎ型として説明する。

[0026] 図２に示すように、本実施形態の固体撮像装置１は、複数の画素を有する基板１２と、基板１２の表面側に形成された配線層１３と、支持基板３１とを備える。また、基板１２の裏面側に順に形成された固定電荷を有する絶縁膜（以下、固定電荷膜）２０と、絶縁膜２１と、遮光膜２５と、平坦化膜２６と、カラーフィルタ層２７と、オンチップレンズ２８とをさらに備える。

[0027] 基板１２は、シリコンからなる半導体基板で構成され、例えば１μｍ～６μｍの厚みを有して形成されている。基板１２の画素領域３にはフォトダイオードからなる光電変換部４０と、画素回路部を構成する複数の画素トラン

ジスタ（Ｔｒ１～Ｔｒ４）とから構成される画素が複数個、二次元マトリクス状に形成されている。そして、隣接する光電変換部４０間は素子分離部１９により電気的に分離されている。また、図２では図示を省略するが、基板１２に形成された画素領域の周辺領域には、周辺回路部が構成されている。

[0028] 光電変換部４０は、基板１２の表面側及び裏面側に形成される第１導電型（以下ｐ型）半導体領域２３，２４と、その間に形成される第２導電型（以下ｎ型）半導体領域２２とで構成されている。光電変換部４０では、そのｐ型半導体領域２３，２４とｎ型半導体領域２２との間のｐｎ接合で主なフォトダイオードが構成されている。光電変換部４０では、入射した光の光量に応じた信号電荷が生成され、ｎ型半導体領域２２に蓄積される。また、基板１２の界面で発生する暗電流の原因となる電子は基板１２の表面及び裏面に形成されたｐ型半導体領域２３，２４の多数キャリアである正孔に吸収されることにより、暗電流が抑制される。

また、各光電変換部４０はｐ型半導体領域で構成された画素分離層１８と、その画素分離層１８内に形成された素子分離部１９によって電気的に分離されている。

[0029] 画素トランジスタは、本実施形態においては、図３に示すように、転送トランジスタＴｒ１、リセットトランジスタＴｒ２、増幅トランジスタＴｒ３、選択トランジスタＴｒ４の４つのトランジスタで構成されている。

[0030] 転送トランジスタＴｒ１は、図３に示すように、２行２列に形成された４つの光電変換部４０の中心部に形成されたフローティングディフュージョン部３０と、転送ゲート電極１６とで構成されている。フローティングディフュージョン部３０は、図２に示すように、基板１２の表面側に形成されたｐーウェル層２９に、ｎ型の不純物が高濃度にイオン注入されることで形成されたｎ型半導体領域で構成される。また、転送ゲート電極１６は、光電変換部４０とフローティングディフュージョン部３０との間の基板１２表面側に、ゲート絶縁膜１７を介して形成されている。

[0031] 画素トランジスタのうち、リセットトランジスタＴｒ２、増幅トランジス

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(54) Title: MULTI SCENE DEPTH PHOTO SENSITIVE DEVICE, SYSTEM THEREOF, SCENE DEPTH EXPANDING METHOD, AND OPTICAL IMAGING SYSTEM

(54) 发明名称 : 多景深感光器件、系统、景深扩展方法及光学成像系统

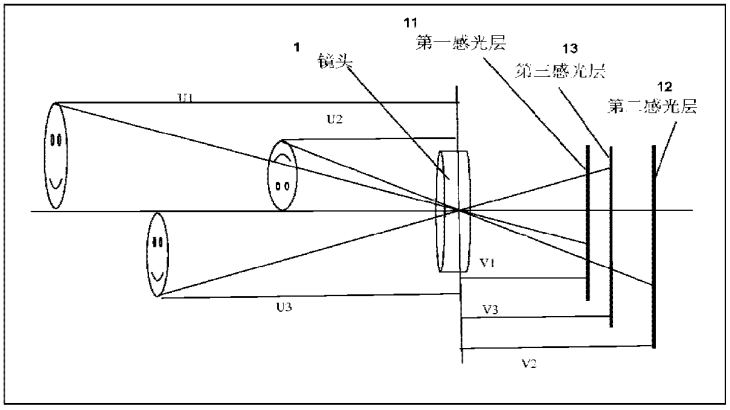


图 13 / FIG. 13

1 LENS
11 THE FIRST PHOTOSENSITIVE LAYER
12 THE SECOND PHOTOSENSITIVE LAYER
13 THE THIRD PHOTOSENSITIVE LAYER

(57) Abstract: A multi scene depth photo sensitive device, system thereof, scene depth expanding method and an optical imaging system are provide. The multi scene depth photo sensitive device comprises at least two photo sensitive pixel layers which can sense a light source, and the at least two photo sensitive pixel layers are disposed at a predetermined distance so that the different optical signals from the lens disposed at a a certain distance from the photo sensitive device can be focused on the different photo sensitive pixel layers. It is possible to realize focus automatically while avoiding utilizing electrodynamic element and mechanical element.

(57) 摘要: 提供一种多景深感光器件、系统、景深扩展方法及光学成像系统。多景深感光器件包括至少两个可感应到光源的感光象素层，至少两个感光象素层之间按预定的距离间隔设置，使来自距离感光器件特定距离的镜头的不同光信号被聚焦到不同的感光象素层。可以避免使用电动机构和机械部件而实现自动对焦。

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说 明 书

多景深感光器件、系统、景深扩展方法及光学成像系统

技术领域

本发明涉及感光领域，具体的说，涉及一种多景深感光器件、利用该多景深感光器件的感光系统、景深扩展方法以及一种光学成像系统与方法。

背景技术

本发明是本发明人稍早一点的《多光谱感光器件及其制作方法》（PCT/CN2007/071262），《多光谱感光器件及其制作方法》（中国申请号：200810217270.2），《多光谱感光器件》（中国申请号：200910105372.X），《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2），《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）的延续，旨在提供更为具体而且优选的多光谱感光器件在芯片及系统级别的实现。

感光系统，是一种通过光学镜头进行景物的捕捉、收集，并由感光器件，例如CMOS感光芯片进行景物的记录的系统。感光系统工作时，调节镜头，使距离镜头一定距离的景物清晰成像的过程，叫做对焦，该景物所在的点，称为对焦点，因为“清晰”具有相对性，所以对焦点前（靠近镜头）、后一定距离内的景物的成像都可以是清晰的，这个前后范围的总和称为景深。通常前景深小于后景深，即精确对焦后，对焦点前只有很短一段距离内的景物能清晰成像，而对焦点后很长一段距离内的景物都是清晰的。

获得宽景深清晰成像的系统是人们长期以来的研究目标之一。研究表明，景深的大小与镜头焦距有关，焦距长的镜头景深小，焦距短的镜头景深大。可见，镜头焦距调整是获得宽景深清晰成像的手段之一；另外，根据几何光学的基本成像公式（$\frac{1}{f}=\frac{1}{u}+\frac{1}{v}$，其中，f为镜头焦距，u为物距，即被摄物到镜头的距离，v为象距，即镜头到感光器件的距离），可见，象距的动态调整也是获得宽景深清晰成像的手段之一。

因此，现有感光系统中的自动对焦方式，都采用上述两种手段之一。例如，镜头由一组镜片构成，通过调整镜片之间的距离，从而可以调整镜头焦距或（镜头与感光器件的）象距（而实现光学变焦或对焦）；或者通过驱

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动例如 CMOS 感光器件位移，从而改变象距（而实现光学对焦）。然而，显然的，这两种方式的对焦，都需要电动机构和复杂、精密的机械部件来进行镜片或感光器件的位移驱动。这样，不仅显著增加了尺寸，也显著增加了成本和功耗。在很多的应用里，如手机照相和医用照相里，这些都是明显的不利因素。

一些不采用运动机构的宽景深系统因此被提出，试图在某些应用里取代自动对焦的需求。这种系统在手机照相的应用里，被称之为 EDoF (Extended Depth of Focus)，例如，DXO 公司提出的一种 EDoF 系统，通过特别的镜头设计，让感光器件中的红色感光象素聚焦在无穷远处，兰色感光象素聚焦在尽可能的近距(例如 50cm) 。而绿色感光象素聚焦在某个中间的位置。这样，无论物体处于哪个位置，总有一个颜色的图像是清楚或相对比较清楚的。之后，通过数学的手段，以比较清楚的颜色为主体，不够清楚的颜色为辅助信息，就能在比较宽的范围，还原和计算出较清楚的图像。

然而，采用单层感光器件，当红色感光象素聚焦在无穷远时，兰色感光象素的聚焦距离一般很难做得比 50cm 更小。此外，对于采用贝叶图案的感光器件，红色象素和兰色象素都只占感光象素的 1/4。因此，当需要以红色或兰色作为清晰度计算的主体时，图像的分辨率已经减少到以绿色为主体时的分辨率的一半以下。可见，这种方案有一定的局限性。

因此，仍然有必要对现有感光器件或系统进行改进。

发明内容

本发明所要解决的技术问题是，提供一种多景深感光器件、利用该多景深感光器件的感光系统、景深扩展方法以及一种光学成像系统与方法，其以物理的手段实现了自动对焦或多距离成像，避免使用电动机构和复杂、精密的机械部件，具有良好的景深扩展性能。

为解决上述技术问题，本发明采用了以下技术方案：

一种多景深感光器件，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

在本发明的一种实施例中，所述感光象素层包括化学镀膜感光象素层和半导体感光象素层中的至少一者。

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在本发明的一种实施例中，所述化学镀膜感光象素层包括量子点感光象素。

在本发明的一种实施例中，所述半导体感光象素层包括 CMOS 光敏二极管、CMOS 感光门、CCD 光敏二极管、CCD 感光门、和具有双向电荷转移功能的 CMOS 和 CCD 感光二极管和感光门。

在本发明的一种实施例中，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

在本发明的一种实施例中，波长更短的光信号被聚焦到离镜头更近的感光象素层。

在本发明的一种实施例中，所述感光象素层为两层，紫色光、兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

在本发明的一种实施例中，所述感光象素层为三层，紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层；兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层；红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层。

在本发明的一种实施例中，更远距离的光信号被聚焦到离镜头更近的感光象素层。

在本发明的一种实施例中，所述感光象素层为两层，无穷远处的光信号被聚焦到离镜头较近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头较远的感光象素层。

在本发明的一种实施例中，无穷远处的紫色光、兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，感兴趣最短距离的绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

在本发明的一种实施例中，所述感光象素层为三层，无穷远处的光信号被聚焦到离镜头最近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的光信号被聚焦到位于中间的感光象素层。

在本发明的一种实施例中，所述感光象素层为三层，无穷远处的紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层，感兴趣最短距离的红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层。

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在本发明的一种实施例中，所述感兴趣最短距离包括 2mm，5mm，7mm，1cm，2cm，3cm，5cm，7cm，10cm，20cm，30cm，40cm，50cm，60cm，70cm，80cm，100cm，或 150cm。

在本发明的一种实施例中，至少两个所述感光象素层之间设置有透光层。

在本发明的一种实施例中，所述感光象素层中的感光象素为正面感光象素、背面感光象素、或双向感光象素。

在本发明的一种实施例中，当感光象素为双向感光象素时，其感光选向方式为隔离选向、分时选向、分区选向、或象素选向。

在本发明的一种实施例中，所述感光象素层中的感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个互补谱段或子谱段；或者所述化学镀膜感光象素和半导体感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个正交谱段或子谱段。

在本发明的一种实施例中，所述互补谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱；

所述正交谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱。

在本发明的一种实施例中，每一感光象素层中的色彩排列包括同一排列、水平排列、垂直排列、对角排列、广义贝叶排列、YUV422 排列、横向 YUV422 排列、蜂窝排列、均布排列。

在本发明的一种实施例中，至少一个所述感光象素层中的部分或全部感光象素的正面、背面或双面设置有滤光膜，所述滤光膜的选频特性包括红外截止滤波、兰色带通、绿色带通、红色带通、青色带通、黄色带通、品红色带通、或可见光带通。

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在本发明的一种实施例中，所述感光象素层中的相邻两层各自设有读取电路；或者所述感光象素层的相邻两层共用读取电路。

在本发明的一种实施例中，所述读取电路为主动象素读取电路、被动象素读取电路、或主动象素与被动象素混合读取电路。

在本发明的一种实施例中，所述主动象素包括 3T、4T、5T 或 6T 主动象素。

在本发明的一种实施例中，所述读取电路的共用方式包括单层或上下层 4 点共享方式、单层或上下层 6 点共享方式、单层或上下层 8 点共享方式、或单层或上下层任意点共享方式。

在本发明的一种实施例中，所述读取电路包括用于对每一感光象素层的象素阵列中的紧邻的同行异列、异行同列、或异行异列的象素间进行两两合并采样，获得第一合并象素的采样数据的第一合并单元；以及用于对第一合并单元得到的第一合并象素的采样数据进行合并采样以获得第二合并象素的采样数据的第二合并单元。

在本发明的一种实施例中，所述读取电路还包括第三合并单元，用于对第二合并单元得到的第二合并象素的采样数据进行合并采样以获得第三合并象素的采样数据。

在本发明的一种实施例中，所述第一合并单元或第二合并单元的象素合并方式为相同或不同色彩象素间的电荷相加方式或信号平均方式，其中不同色彩象素间的象素合并方式遵照色彩空间变换的方式，以满足色彩重建的要求。

在本发明的一种实施例中，所述色彩空间变换包括 RGB 到 CyYeMgX 空间的变换、RGB 到 YUV 空间的变换、或 CyYeMgX 到 YUV 空间的变换，其中 X 为 R(红)、G(绿)、B(兰)中的任一种。

在本发明的一种实施例中，所述电荷相加方式通过象素直接并联或将电荷同时转移到读取电容（FD）中完成。

在本发明的一种实施例中，所述第一合并单元或第二合并单元的基于色彩的合并采样方式包括同色合并方式、异色合并方式、混杂合并方式、或选择性抛弃多余色彩合并方式，且第一合并单元和第二合并单元采用的合并采样方式不同时为同色合并方式。

在本发明的一种实施例中，所述第一合并单元或第二合并单元的基于位置的合并采样方式包括以下几种方式中的至少一种：直接输出到总线的信号自动平均方式、跳行或跳列方式、和逐个采样方式。

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在本发明的一种实施例中，所述第三合并单元的合并采样方式包括：色彩空间变换方式和后端数字图像缩放方式中的至少一种。

在本发明的一种实施例中，包括具有跨层读取功能的全局电子快门，所述全局电子快门包含多个可同时转移并读取一层或多层感光象素层的电荷或电压值的不感光的转移和读取象素。

在本发明的一种实施例中，所述多个不感光的转移和读取象素位于不感光象素转移和读取层；或者位于所述感光象素层。

在本发明的一种实施例中，每一感光象素层，设置有一个紧邻的不感光象素转移和读取层。

在本发明的一种实施例中，所述不感光的转移和读取象素由半导体电路制成。

本发明也提供了一种景深扩展方法，包括：

在感光器件中设置至少两个可感应到光源的感光象素层，并将至少两个所述感光象素层按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

在本发明的一种实施例中，通过来自不同感光象素层的具有不同清晰度的图像而获取一幅清晰图像。

本发明还提供了一种光学成像方法，包括：

设置镜头和包括至少两个可感应到光源的感光象素层的感光器件；将所述感光器件放置在距所述镜头特定距离，且至少两个所述感光象素层之间按预设距离间隔布置，使得来自镜头的不同光信号被聚焦到不同的所述感光象素层。

本发明还提供了一种光学成像系统，包括镜头和多景深感光器件，所述多景深感光器件布置在距所述镜头特定距离，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自所述镜头的不同光信号被聚焦到不同的所述感光象素层。

在本发明的一种实施例中，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

在本发明的一种实施例中，波长更短的光信号被聚焦到离镜头更近的感光象素层。

在本发明的一种实施例中，更远距离的光信号被聚焦到离镜头更近的感光象素层。

本发明还提供了一种感光系统，包括上述的感光器件。

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在本发明的一种实施例中，所述感光系统包括数码相机，照相手机，摄像机，视频或照相监控系统，图像识别系统，医学图像系统，军用、消防或井下图像系统，自动跟踪系统，立体影像系统，机器视觉系统，汽车视觉或辅助驾驶系统，电子游戏系统，网络摄像头，红外和夜视系统，多光谱成像系统，和电脑摄像头中的一种。

现有的感光系统，不仅自动对焦系统需要电动机构和复杂、精密的机械部件，而且对于 6mm 直径以上的镜头而言，为了实现在 10cm 至无穷远的宽距自动对焦，镜头的行程必须在 0.2mm 以上，也就是说，无穷远处清晰成像的象距与 10cm 处清晰成像的象距差，至少是 0.2mm，即 200um。众所周知，硅或其它半导体材料都是不透明的。光进入硅后，大约在 12um 处，就已经被吸收得所剩无几了。因此即使使用自动对焦系统，现有的感光系统也很难获得较宽的景深范围。

本发明的多景深感光器件、利用该多景深感光器件的感光系统、景深扩展方法，以及光学成像系统及方法，通过设置至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距感光器件特定距离的镜头的不同光信号被聚焦到不同的感光象素层，从而不同感光象素层可以得到不同景深的图像。从产品角度，感光器件可以制作成感光芯片独立存在，但从应用角度，例如光学成像，感光器件通常需要与镜头配合使用。镜头，依其大小、材料、曲面设计等具有不同的聚焦特性，例如以普通的手机镜头为例，其景深范围通常是无穷远到 2m，超出该景深范围，则需要采用自动对焦技术，例如通过调整感光器件到镜头的距离，也即调整象距到某一合适数据，才能获得例如 50cm-30cm 的清晰景象。而在本发明中，如果选定的应用镜头是手机镜头，则可以按下例在感光器件中设置两个感光象素层（称第一感光象素层和第二感光象素层），当与该选定的手机镜头配合时，感光器件被放置在距该镜头特定距离，此时，第一感光象素层到镜头的距离为第一象距，第二感光象素层到镜头的距离为第二象距（第一象距小于第二象距），此时，距镜头的特定距离以及两个感光象素层之间的预设距离，使得从无穷远到 2m 的景深范围的景物将可在第一感光象素层清晰成像，从 50cm-30cm 的景深范围的景物将可在第二感光象素层清晰成像。由此，实现了两个景深或景深扩展。需要注意的是，上述说明例中，感光象素层的数量和景深范围均仅为示例性数据，可以理解，通过对感光象素层的数量和相互间的预设距离调整，可以形成连

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续、交叠、互补、或正交的景深范围，多个感光象素层各自的景深范围叠加将使感光器件具有相当宽的景深范围，从而无需自动对焦即可获得宽景深范围内的清晰图像，避免使用电动机构和复杂、精密的机械部件，显著的节约了空间和成本。另一方面，在本发明中，通常至少可以从一个感光象素层获得较为完整的图像信息，从而图像具有相当高的清晰度，且无需繁琐的数学计算。

本发明将通过实施例描述这种新型的、威力巨大的混合多光谱感光象素组、感光器件和系统。这些优选实现方式，仅仅是作为举例来说明本发明的优点和实现方法而已，而不是为了限制这些发明的保护范围。

对于相关业界的有识之士而言，本发明的上述及其它目的和优点，在阅读过下面的优选的带有多个插图解释的实现案例的细节描述之后，将是十分明显的。

附图说明

图 1 是一个光谱分布的示意图。可见光一般是指 390nm 到 760nm 波长的光。一般由棱镜的分光效应而从可见光分出来看到的兰光波长在 440－490nm，绿光波长在 520－570nm，红光波长在 630－740nm，而在感光器件的设计中，一般把 390－500nm 划为兰色区，500-610nm 划为绿色区，610-760nm 划为红色区，但这种红、绿、兰的谱段的划分并不是绝对的。图中的红、绿、兰、青（兰绿复合）、和黄（绿红复合）的波形，是原色感光象素或补色（复合色）感光象素所需求的理想的波长响应曲线。如果作为基色的原色感光象素或补色（复合色）感光象素不具备类似的波长响应曲线，则很难重建人类所能看到绝大部分色彩。

图 2 是感光象素的 3T 读取电路。

图 3 是感光象素的 4T 读取电路。

图 4 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）提出的四点共享读取电路。

图 5 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）提出的两层六点共享读取电路。

图 6 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：

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200910105948.2）和《一种感光器件及其读取方法、读取电路》(中国申请号：200910106477.7)提出的两层八点共享读取电路。

图 7 是本人在《一种感光器件及其读取方法、读取电路》(中国申请号：200910106477.7)提出的任意 N 点共享读取电路。

图 8 是本人在《多光谱感光器件及其制作方法》（中国申请号：200810217270.2）和《多光谱感光器件》（中国申请号：200910105372.X)中提出的，上下层感光象素在感兴趣的光谱上互补或正交的双层感光器件的示意图。这种感光器件通过采用精心选择的彩色图案和排列，可以得到非常多优秀的双层感光器件。这些感光器件可以用于正面感光，背面感光，和双向感光。这些方法和原理，同样也可适用于本发明的多光谱感光器件。

图 9 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）中提出的一种在不同色彩象素间实现电荷合并的子采样方法。这种方法同样适用于本发明的多光谱感光器件。

图 10 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）中提出的采用色彩空间变换来实现的一种象素合并和子采样方法。这种方法同样适用于本发明的多光谱感光器件。

图 11 是本发明提出的一种用于景深扩展的两层感光器件的结构示意图，其中透光层的厚度，由所希望的两个感光平面的象距差（V2-V1）来决定。

图 12 是本发明提出的一种用于景深扩展的三层感光器件的结构示意图，其中透光层的厚度，由所希望的两个感光平面的象距差（V2-V1 或 V3-V2）来决定。

图 13 是第一种利用多层感光器件实现景深扩展的原理示意图。在这个示意图里，位于不同距离的物体，将清晰地聚焦在多层感光器件的不同感光象素层。因此，位于这三个距离之间的任一物体，都将清楚或者比较清楚地聚焦在一个，或者两个感光象素层，从而达到景深扩展的效果。图中，U1，U2，U3 是物距（即物体到镜头的距离），V1，V2，V3 是象距(即感光象素层到镜头的距离)。

图 14 是第二种同时利用特殊的镜头设计方法和多层感光器件来实现更好的景深扩展效果的原理示意图。对一般光学系统而言，波长更短的光，焦距更短。因此，对镜头进行特别的设计，可以让波长更短的光，聚焦在离镜头更近的感光象素层，或者说，离光源更近的感光象素层；而将波长更长

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的光，聚焦在离镜头更远的感光层，或者说，离光源更远的感光象素层；而将波长中等的光，聚焦在中间的感光层。这样，这种成像系统同时结合多光谱和多象距的特点，就能极大地扩展景深。这种系统，对于微距照相，有着无比的优势。

图 15 是实现图 11 所示的多景深感光器件的感光象素级别的原理示意图。通过调整透光层的厚度，可以调整两个感光象素层之间的距离，从而让两个感光象素层的感光象素，分别对应不同的景深。该例中，上下两个感光象素层均采用半导体感光象素层。

图 16（a）、（b）、（c）、（d）是实现图 11 所示的多景深感光器件的另一种感光象素级别的原理示意图。同样，通过调整透光层的厚度，可以调整两个感光象素层之间的距离，从而让两个感光象素层的感光象素，分别对应不同的景深。该例中，上层的感光象素层采用化学镀膜感光象素层，而下层的感光象素层采用半导体感光象素层，显然二者可以互换而不影响其实现多景深的效果。

图 15 和图 16 都只描绘了感光象素的情况，其它读取电路和辅助电路，因为可以与现有的相同，都被省略。

图 17（a）、（b）、（c）、（d）是实现图 11 所示的多景深感光器件的另一种感光象素级别的原理示意图。同样，通过调整透光层的厚度，可以调整上层的一个感光象素层与下层的另两个感光象素层之间的距离，从而让不同感光象素层的感光象素，分别对应不同的景深。在该例中，上层的一个感光象素层采用化学镀膜感光象素层，下层的另两个感光象素层采用半导体感光象素层，注意到，图 17（a）、（b）中的两个半导体感光象素层布置在一个半导体基层的两面，图 17（c）、（d）中的两个半导体感光象素层布置在一个半导体基层的一面。照射方向可以是该半导体基层的正面或是背面。另需注意的是，由于半导体的透光性限制，半导体基层厚度一般较薄，通常不满足景深扩展所需的感光象素层间隔距离的需求。因此，两个半导体感光象素层更多的用来实现多光谱的需求。

图 18（a）、（b）是实现图 11 所示的多景深感光器件的另一种感光象素级别的原理示意图。同样，通过调整透光层的厚度，可以调整上层的一个感光象素层与下层的另两个感光象素层之间的距离，从而让不同感光象素层的感光象素，分别对应不同的景深。在该例中，上层的一个感光象素层采用化学镀膜感光象素层，下层的另两个感光象素层分别采用半导体感

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光象素层和化学镀膜感光象素层。中间的半导体感光象素层（的两面）可以含有读取三个感光象素层所必需的读取象素和采样电路。

图 19（a）、（b）是实现图 12 所示的多景深感光器件的一种感光象素级别的原理示意图。注意到，在该例中，从上到下依次布置化学镀膜感光象素层、第一透光层、第一半导体感光象素层、第二透光层、第二半导体感光象素层。第一半导体感光象素层和第二半导体感光象素层分别实现在不同的两个半导体基层上，化学镀膜感光象素层与第一半导体感光象素层之间的距离通过调整第一透光层的厚度实现，第一半导体感光象素层与第二半导体感光象素层之间的距离通过调整第二透光层的厚度实现。读取和采样电路可以在位于中间的第一半导体感光象素层实现，也可以分布在两个半导体感光象素层。

对于具有两层半导体感光象素层的实施例，例如图 8 和图 15 等，如果将其中一个感光象素层中的感光象素去掉，做成专门用于读取电路和信号处理的层，则可以得到如图 20-23 所示的本发明提出的带有(具有跨层读取功能的)全局电子快门的感光器件。图 20-23 仅是展示了该带有(具有跨层读取功能的)全局电子快门的感光器件的感光象素层和不感光的转移和读取象素层，显然，结合前述，当保留定焦在不同景深的多个感光象素层时，则可以得到带有(具有跨层读取功能的)全局电子快门的多景深感光器件。

图 20 是本发明提出的两行共用一行转移象素（读取电容）的示意图。这实际上是《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7)中隔行扫描方式的一种新的实现。在这里，转移象素和感光象素不在同一层，因而可以获得更好的感光面积的使用效率，但同时增加了一倍的快门速度。重要的是，这种方式可以用于以化学感光材料(如量子感光膜)为感光象素层的感光器件。

图 21 是利用半导体的不良透光性能，将半导体基层厚度增加到一定厚度，使得下层的象素感不到光。然后，利用金属穿孔或是表面走线，外部连接的方式，将上层的感光象素信号，通过二极管或读取放大开关电路引到不感光象素层的读取象素上，在那里进行采样读取，从而将一个两层的感光器件退化成一个(具有跨层读取功能的)全局电子快门的单层感光器件。这个器件在结构上是双层的，但在效果上却是单层的。当这种方式用于图 17(a)所示的多层感光器件时，就能得到(具有跨层读取功能的)全局

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电子快门的多景深感光器件。

图 22 是本发明提出的以传统的(CMOS 和 CCD)半导体电路为基础的带有（具有跨层读取功能的）全局电子快门的多光谱两层感光器件的示意图。同样地，感光象素信号到不感光读取象素上的转移，由二极管或放大开关电路来控制的。

图 23 是本发明提出的另一种以化学感光材料(如量子感光膜)为基础的带有（具有跨层读取功能的）全局电子快门的多光谱两层感光器件的示意图，其中感光象素层采用化学感光材料(如量子感光膜)，而读取电路和信号处理层则是 CMOS 半导体层。注意到在该图示例中，每一个感光象素都对应有一个不感光的电荷转移象素，用于实现全局电子快门。这也是多层感光器件的为简单实现全局电子快门而特意进行的一种退化。

图 24 是本人在《一种感光器件及其读取方法、读取电路》(中国申请号：200910106477.7)提出的一种同时采用主动象素和被动象素来读取感光象素信号的读取电路。采用这种方法的好处是，能够极大地扩大感光器件的动态范围，并且成倍地节省图像预览时的功耗。这种混合读取电路在高灵敏度的多层多光谱感光器件和带有全局电子快门的多光谱感光器件里尤其有用。

图 25 是《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）中用来描述该发明中提出的象素合并和子采样方法的采样控制电路示意图。本发明也将用到这种新型的象素合并和子采样方法。

具体实施方式

下面通过具体实施方式结合附图对本发明作进一步详细说明。

本发明将提出的多景深感光器件，其主要用途是景深扩展，即手机行业里目前所称的 EDoF(即 Extended Depth of Focus)。景深扩展尤其在照相手机中有着非常广泛的应用，然而，目前的景深扩展主要使用光学和数学手段，通常是利用光学变焦或自动对焦的方式实现景深调整，这要求电动机构和复杂、精密的机械部件的配合，因而将显著增加空间和成本。

本发明实施例所提出的多景深感光器件，结合多层感光器件的实现，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距感光器件特定距离的镜头的不同光信号被聚焦到不同的感光象素层，从而不同感光象素层构成了具有不同象距的

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感光平面，可以定焦不同的景深，由此扩展了感光器件的景深范围，相当于从多点光学对焦这一物理手段上实现了自动对焦，相应可以去除电动机构和复杂、精密的机械部件的配合，显著地节省了空间和成本。

所述感光象素层，包括化学镀膜感光象素层和半导体感光象素层中的至少一者。即上述至少两个感光象素层，可以全部是化学镀膜感光象素层，或者全部是半导体感光象素层，或者部分是化学镀膜感光象素层，部分是半导体感光象素层。其中，化学镀膜感光象素层包括量子点感光象素。半导体感光象素层包括 CMOS 光敏二极管、CMOS 感光门、CCD 光敏二极管、CCD 感光门、和具有双向电荷转移功能的 CMOS 和 CCD 感光二极管和感光门。

上述的感光象素层，分别用来感应不同的光信号。本发明中，关注的光信号特性主要包括光信号的频谱特性，即光的波长，以及光信号的距离特性，即光信号到镜头的距离。因此，光信号的不同，是指两个光信号之间，上述两个特性中至少有一者不同，即两个光信号之间，可能是波长不同，或者距离不同，或者波长和距离都不同。当然，由于自然界常见复色光，例如白光，因此如果需要得到不同波长的光，一般需要配合镜头设计，利用例如棱镜的分光效应，镜头材料或曲面设计对不同波长的光的不同折射率从而使不同波长的光分离并聚焦在不同的感光象素层上。

在聚焦不同波长的光信号的时候，一般地，波长更短的光信号被聚焦到离镜头更近的感光象素层。例如，感光象素层为两层，则聚焦在离镜头较近的感光象素层的光信号是紫色、兰色光、青色、或绿色光，聚焦在离镜头较远的感光象素层的光信号是绿色光、红色光、黄色光、可见光(白色光)、或红外光。又如，感光象素层为三层，则聚焦在离镜头最近的感光象素层的光信号是紫外光、兰色光、或青色光；聚焦在位于中间的感光象素层的光信号是绿色光、兰色光、黄色光、红色光、或可见光(白色光)；聚焦在离光源最远的感光象素层的光信号是红色光、黄色光、可见光、或红外光。

在聚焦不同距离的光信号的时候，一般地，更远距离的光信号被聚焦到离镜头更近的感光象素层。例如，感光象素层为两层，聚焦在离光源较近的感光象素层的是无穷远处的光信号，聚焦在离光源较远的感光象素层的是感兴趣最短距离的光信号。结合聚焦不同波长的光，还可以进一步设置为：无穷远处的紫外光、兰色光、青色光、或绿色光被聚焦到离光源较近的感光象素层；感兴趣最短距离的绿色光、红色光、黄色光、可见光(白

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色光)、或红外光被聚焦到离光源较远的感光象素层。

又如，感光象素层为三层，聚焦在离光源最近的感光象素层的是无穷远处的光信号，聚焦在离光源最远的感光象素层的是感兴趣最短距离的光信号，聚焦在位于中间的感光象素层的是无穷远处与感兴趣最短距离的一个中间距离的光信号。结合聚焦不同波长的光，还可以进一步设置为：无穷远处的紫外光、兰色光、青色光、或绿色光被聚焦到离光源最近的感光象素层；无穷远处与感兴趣最短距离的一个中间距离的绿色光、兰色光、黄色光、红色光、或可见光(白色光)被聚焦到位于中间的感光象素层；感兴趣最短距离的红色光、黄色光、可见光、或红外光被聚焦到离光源最远的感光象素层。

实施方式中，感兴趣最短距离包括 2mm，5mm，7mm，1cm，2cm，3cm，5cm，7cm，10cm，20cm，30cm，40cm，50cm，60cm，70cm，80cm，100cm，150cm。所谓感兴趣最短距离，是指用户关注的景物到镜头的最近距离。例如，感兴趣最短距离是 2mm，是指用户关注的景物到镜头的最近距离是 2mm，当景物到镜头的距离小于 2mm，则不再关注。

图 13 显示了距离与聚焦平面的关系。在该图中，位于不同距离的物体，将清晰地聚焦在多层感光器件的不同感光象素层。因此，位于这三个距离之间的任一物体，都将清楚或者比较清楚地聚焦在一个，或者两个感光象素层，从而从同一个感光器件，能够同时得到它们的清晰图像。

图 14 显示了波长与聚焦平面的关系，对一般光学系统而言，波长更短的光，焦距更短。因此，通过对镜头进行设计，可以让波长更短的光，聚焦在离镜头更近的感光象素层；波长更长的光，聚焦在离镜头更远的感光象素层；波长中等的光，聚焦在中间的感光象素层。这样，处于不同距离的物体，总有一个颜色，在一个感光层中是清楚的。于是，这种成像系统同时结合了多光谱和多象距的特点，每个感光层有自己的景深范围，并且对于不同波长的光，景深距离和范围不同，可以将各个感光层的景深范围进行整合，能够极大地扩展景深，对于微距照相，有着无比的优势。

由于可以从不同感光象素层得到具有不同清晰度的多个图像，因而这些图像之间可以相互参照，通过图像的整合、选用和舍弃，以及插值、增强、或反卷积等数学处理，而获得清晰的图像。

实施方式还包括在上述多景深感光器件中，实现一种具有跨层读取功能的全局电子快门，包括多个不感光的转移和读取象素，所述不感光的转移和

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读取象素的每一个能够用来转移和读取处在其它层的至少一个感光象素的电荷或电压值。从而多个不感光的转移和读取象素可同时转移并读取一层或多层感光象素层的电荷或电压值。多个不感光的转移和读取象素可以与感光象素位于同一象素层，显然，这意味着该象素层的感光灵敏度的下降。多个不感光的转移和读取象素也可以与感光象素位于不同的象素层，即形成独立的感光象素层和独立的不感光的转移和读取象素层，显然，这意味该具有跨层读取功能的全局电子快门只能在两层或多层感光器件中实现。

可以为每一个感光象素层设置一个紧邻的对应的不感光象素转移和读取层，所述不感光象素转移和读取层可同时转移对应的感光象素层的所有象素的电荷或电压值；或者可同时转移对应的感光象素层的奇数行或偶数行象素的电荷或电压值。图 20 显示了两行共用一行读取电容的设计，以实现逐行扫描的功能。不感光的转移和读取象素层，可以半导体电路做成。

图 21 显示了一种两层感光器件的退化实现，以获得单层的带有全局电子快门的单层感光器件。这种方法利用了半导体材料的不良透光性，将两半导体基层加厚，使得底层感不到光，而只能用于做象素读取。将这个方法用于图 17(a)所示的三层感光器件时，就能得到带全局电子快门的两层多景深感光器件。

图 22 和图 23 显示了一种具有跨层读取功能的全局电子快门的象素级别的实现。

文中出现的远近，上下等位置关系，均是指以光源为基准的相对位置。例如，上层感光象素层和下层感光象素层的描述，是指感光象素层水平放置，光源从上方垂直照射向感光象素层而言。显而易见，本文中的上下关系实际上具有更加广泛的含义，即，例如感光面垂直放置，光源从左侧或右侧，或者从前侧或后侧垂直照射向感光面，则所谓的上下关系，则等同于前后关系或者左右关系。不失一般性，本领域技术人员可以理解，其中的上方、下方等描述，可以用左侧、右侧、前侧、后侧等描述进行等同的替代。不同种类的感光象素层，如化学镀膜感光象素层或半导体感光象素层，其上下关系并无限制，何者处于上方，何者处于下方是可以根据需要任意设置的。下文所述的基层顶面和底面，同样表达类似含义，即以水平放置，光源从上方垂直照射向基层而言，此时，位于上方的基层表面称为顶面，位于下方的基层表面称为底面。可以理解，当基层垂直放置，光源从左侧或右侧，或者从前侧或后侧垂直照射向基层时，可等同替代为前侧

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面和后侧面，左侧面和右侧面的表述。

此外，也需特别注意术语“可感应到光源”和“感光”之间的差异，感光象素层的“感光”，指的是该象素具有感光能力，“可感应到光源”，指的是感光象素是否能够感应到光源的结果，即感光象素的感光能力是否得到发挥，例如，由于半导体的透光性限制，当在一个半导体基层的顶面和底面各布置一个半导体感光象素层时，如果该半导体基层厚度超出半导体的透光性限制，则光源向该半导体基层照射时，只有顶面的半导体感光象素层能够感应到光源，而底面的半导体感光象素层受半导体基层厚度限制而无法感应到光源，则称顶面的半导体感光象素层为可感应到光源的感光象素层，即感光象素的感光能力得以发挥；称底面的半导体感光象素层为不可感应到光源的感光象素层，即感光象素的感光能力未能发挥。注意到在后文中，利用不可感应到光源的感光象素层，可以形成不感光的转移和读取象素层。

当化学镀膜感光象素或半导体感光象素为双向感光象素时，则涉及到感光选向问题，即尽管能够双向感光，但不能接受同一时刻两个方向的光照，需要在一个时刻选择一个方向的光源照射，感光选向方式可以为隔离选向、分时选向、分区选向、或象素选向等等，也就是说，可以通过例如遮光膜遮挡等方式来实现分时刻、分区域、分象素的感光选向。双向照射的情况，例如图 8 所示。

感光象素层，大致相当于垂直于光源照射方向的感光平面，在这样的感光平面中，布置有多个感光象素（通常形成为多行多列的象素阵列），对于多个感光象素层中的每一感光象素层，其可能是平面混合型，也就是既布置有化学镀膜感光象素，也布置有半导体感光象素。另外的情形是，同一感光象素层中仅布置一种感光象素，如此，将形成化学镀膜感光象素层，或者半导体感光象素层。

在实施方式中，感光器件的同一位置（即由一层感光象素层的该象素位置上穿透而来的光照射到另一感光象素层上的位置）但不同层的感光象素，分别感应包含紫外线、可见光、近红外、和远红外中的一个互补谱段或子谱段；或者分别感应包含紫外线、可见光、近红外、和远红外中的一个正交谱段或子谱段。其中，互补谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近

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红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱；

正交谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱。

实施方式包括让感光器件中至少一层感应两个不同的光谱(即射频)谱段。对于每一感光象素层而言，其象素阵列的色彩排列包括同一排列(象素阵列中的象素色彩相同)、水平排列(象素阵列中的同一行象素色彩相同)、垂直排列(象素阵列中的同一列象素色彩相同)、对角排列(象素阵列中的同一对角线的象素色彩相同)、广义贝叶排列(象素阵列中的一条对角线上的象素色彩相同，另外一条对角线上的象素色彩不同)、YUV422 排列、横向 YUV422 排列、蜂窝排列、均布排列(四个象素均匀交错等距排列)等。

需要注意的是，本文中的术语“布置”，包含了各种在例如半导体基层或透光层上形成化学镀膜感光象素层或半导体感光象素层的制作工艺。例如，半导体基层为一个 N 型硅晶体基板，在该基板一面上的一个象素位置，根据色彩的深度需求，由该象素位置表面向基板内部做一定深度的 P 杂质置入，形成一个 P 掺杂层，该 P 掺杂层即形成为一个半导体象素，如果在该 P 掺杂层做另一定深度的 N 杂质置入，形成在 P 掺杂层中的 N 掺杂层，该 N 掺杂层即形成为另一半导体感光象素(与前一 P 掺杂层的半导体感光象素在不同感光象素层，但象素位置相对应)，可以按照《多光谱感光器件及其制作方法》(PCT/CN2007/071262)提供的方法，在 390nm 附近，500nm 附近，610nm 附近，和 760nm 附近设置分层线，使得任一分层线上下的对应点象素感应互补或正交的光谱。图 1 给出了一个分层线的设置的例子，即通过不同深度的杂质掺入，形成不同的色彩。在基板的该面进行化学镀膜溶液的涂抹加工，可以形成化学镀膜感光象素层，由于制作或者加工工艺的多样性，在本文中均以“布置”进行表述。

上述的两层半导体感光象素在不同深度上的布置，实现了在基板一个

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表面上的同一象素位置可以感应到至少两个谱段，从而提供了在该表面上的象素图案排列上的更好的灵活性以及更多的象素布置，能够大幅提高感光器件的灵敏度,解析度,和动态范围。

对于上述在半导体基板某一面的不同深度的掺杂加工，其同一位置最多布置两层感光象素，这是由于在同一位置布置 3 层，加工上难度极大，同时在布线上，由于各层间的引线需要相互隔离，3 层引线显然造成了布线上的困难。而在本发明中，采用同一面上最多布置两层上述的半导体感光象素层，并可结合平面上的象素图案排列完成彩色重建，因而可以实现更好的彩色感光性能。由于同一面上最多以深度掺杂方式布置两个半导体感光象素层，因而明显降低了立体加工工艺的难度，且在布线上，也相对简单。

对于基板，可以采用单面或者双面加工工艺，从而形成单面感光器件或者双面感光器件。双面感光器件，对于上述的深度掺杂加工，如果采用两个半导体感光象素层一者布置在基板的顶面，另一者布置在基板底面的双面布置方式，则对于每一面而言，其都简化为平面加工工艺，可以在一面上完成一个感光象素层的平面加工后，将基板进行翻转而在另一面同样以平面加工工艺完成另一感光象素层的加工，使得加工工艺近似于现有的单面单层感光器件的加工工艺，相对于上述的同一面的两层掺杂的立体加工而言，更为简单。另一方面，沿光照方向，在基板的某一位置，可以布置多层感光象素。

半导体感光象素层通常制作在半导体基层上，为了实现景深扩展，在实际制作中，通常采用增设透光层（例如透明玻璃层）来调整不同感光象素层之间的距离，例如，在一半导体基层上制作一层或多层半导体感光象素层，而后在该半导体基层上放置一透光层，而后，在该透光层上涂抹加工出一层化学镀膜感光象素层。通过透光层的不同厚度设置，相当于预设化学镀膜感光象素层和半导体感光象素层之间的间隔距离，进而实现景深扩展。

在很多的应用里，在化学镀膜感光象素层或半导体感光象素层的正面，背面，或双面并不涂任何滤光膜。但在另外一些应用里，如对于色彩还原要求特别高的专业相机或摄像机，实施方式包括使用滤光膜的方式。滤光膜设置在化学镀膜感光象素层或半导体感光象素层中的全部或部分感光象素的正面，背面，或双面。滤光膜的选频特性包括红外截止滤波、兰

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色带通、绿色带通、红色带通、青色带通、黄色带通、品红色带通、或可见光带通。滤光膜的使用是通过牺牲少数象素的灵敏度，来去除不想要的光谱的影响，减少上下左右象素之间的干涉（crosstalk），或者获得正交性更好的三原色或是更纯正的补色信号。

实施方式包括让所述多景深感光器件的多层感光象素层的相邻两层各自使用自己的读取电路。

实施方式包括让所述多景深感光器件的多层感光象素层的相邻两层共用置于其中一层的读取电路。

实施方式包括让所述多景深感光器件的读取电路位于半导体感光象素层，或独立的读取电路层。

所述多景深感光器件的读取电路的实施方式包括采用《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）中的象素读取和子采样方法。

实施方式包括在所述多景深感光器件的信号读取电路里采用主动象素读取电路、被动象素读取电路、或主动象素与被动象素混合读取电路。

所述主动象素包括 3T、4T、5T、或 6T 主动象素。3T 和 4T 的主动象素结构分别如图 2 和图 3 所示。

所述读取电路的共享方式包括无共享方式、单层或上下层 4 点共享方式、单层或上下层 6 点共享方式、单层或上下层 8 点共享方式、或单层或上下层任意点共享方式。4 点共享方式，6 点共享方式，8 点共享方式，和任意点共享方式，分别如图 4，图 5，图 6，和图 7 所示。

实施方式中，多景深感光器件的所述读取电路包括用于对每一感光象素层的象素阵列中的紧邻的同行异列、异行同列、或异行异列的象素间进行两两合并采样，获得第一合并象素的采样数据的第一合并单元；以及用于对第一合并单元得到的第一合并象素的采样数据进行合并采样以获得第二合并象素的采样数据的第二合并单元。

实施方式还包括：读取电路还包括第三合并单元，用于对第二合并单元得到的第二合并象素的采样数据进行合并采样以获得第三合并象素的采样数据。

在本发明的一种实施例中，所述的感光器件，所述第一合并单元或第二合并单元的象素合并方式为相同或不同色彩象素间的电荷相加方式或信号平均方式，其中不同色彩象素间的象素合并方式遵照色彩空间变换的方

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式，以满足色彩重建的要求。

上述的第一合并象素和第二合并象素来自于将子采样至少分为两个过程的处理，即第一合并采样过程和第二合并采样过程。第一合并采样过程和第二合并采样过程，通常发生在象素的行（合并）采样和列（合并）采样之间，主要对模拟信号进行，除电荷相加部分通常只在第一合并采样过程中做以外，其次序和内容通常是可以交换的。此外，也可以包括第三合并采样过程，第三合并采样过程发生在模数转换之后，主要对数字信号进行。

对于第一合并采样过程，是取象素阵列中两个紧邻的象素来进行合并。一方面，完成了紧邻象素的合并，将合并后的象素称为第一合并象素，需要理解的是，第一合并象素只是为本发明描述之便，利用该概念来指代进行第一合并过程后的象素，而不代表物理上，在象素阵列中存在一个“第一合并象素”;将两个紧邻象素合并采样后的数据称为第一合并象素的采样数据。紧邻，系指两个象素之间从水平，垂直，或对角方向上来看紧挨着，中间没有其它象素。紧邻的情况包含同行异列，异行同列，或异行异列。一般而言，在这种合并中，信号将至少是两个象素的信号平均，而噪声则会降低$\sqrt{N}$，因此，合并后，至少可以将信噪比提高$\sqrt{N}$倍，且这种合并可以在相同或不同色彩的象素之间进行。另一方面，由于两个合并的色彩可以不同，即色彩相加或平均，从色彩的三原色原理可知，两种原色的相加是另一种原色的补色，就是说，两个不同原色的象素合并，产生另一种原色的补色，从原色空间，变换到了补色空间，仅仅是发生了色彩空间变换，仍然可以通过不同的补色而完成彩色重建。也即通过这种方式，既能实现不同色彩的象素合并以提高信噪比，同时又能够进行彩色重建。整个子采样过程也因此得到优化，更加适应大数据量的象素阵列的高速需求。色彩空间变换的一个基本要求是，变换后的色彩的组合，能够（通过插值等手段）重建所需要的 RGB（或 YUV，或 CYMK）色彩。

需要了解，由于通常象素阵列包含多个象素，第一合并采样只是将两个象素进行合并，显然，合并形成的第一合并象素也具有多个。对于不同的第一合并象素，其采用的色彩合并方式可以相同，也可以不同。当第一合并全部在相同的色彩间进行时，我们将之称为同色合并方式；当第一合并全部在不同的色彩间进行时，我们将之称为异色合并方式；当第一合并部分在相同色彩间进行、部分在不同色彩间进行，我们将之称为混杂合并

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方式；当对象素阵列中的一些多余的色彩进行抛弃（当然，抛弃是选择性的，例如，不能因此而影响到彩色重建），这样的色彩合并方式称为选择性抛弃多余彩色方式。

显然的，第二合并过程是对多个第一合并象素的操作，同样的，可以将色彩相同的第一合并象素进行合并；也可以将色彩不同的第一合并象素进行合并（当然，这种情况下可能导致三原色的全部相加而无法重建出彩色）。

上述的同色合并、异色合并、混杂合并等方式，是将合并采样做基于色彩的分类，另外，从合并采样的位置选取的角度，第一合并过程和第二合并过程的合并采样方式包括：直接输出到总线的信号自动平均方式、跳行或跳列方式，逐个采样方式，以及这些方式的两种或三种的同时使用。除电荷相加部分通常只能在第一合并采样过程中做以外，第一合并过程和第二合并过程，除了次序的不同外，其方式都是相同和可以交换的。

所谓直接输出到总线的信号自动平均方式，就是，将需要合并的信号(色彩相同或是不同)，同时输出到数据采集总线上去，通过（电压）信号的自动平衡，来获得需要合并信号的平均值。所谓跳行或跳列方式就是跳过一些行或列，从而通过减少数据量的方式来实现（合并）采样。所谓逐个采样方式，实际上就是不做任何合并，依此读取原来的象素或第一合并象素。这三个方式有一些是可以同时使用的，例如，跳行或跳列方式可与直接输出到总线的信号自动平均方式或逐个采样方式同时使用。

第三合并采样过程的子采样方式包括色彩空间变换方式、后端数字图像缩放方式、以及这两个方式的串行使用。第一和第二合并过程主要是在模拟信号上进行，而第三子采样过程主要是在数字信号上进行，即模数转换之后进行。通过将处于不同空间位置的三个或四个色彩象素，当作同一个点上的值而转换到另一个色彩空间，就又可实现水平和（或）垂直方向上的数据减少，从而达到子采样的效果。而数字图像缩放方式，是最为直观常用的子采样方式。

在合并采样时可以实现电荷相加。目前的合并采样几乎都是只做到了电压或电流信号的平均，这种方式在合并 N 点时，最多只能将信噪比提高 $\sqrt{N}$ 倍。这是因为现有的合并采样都是 N 个相同色彩的象素共用一根输出线的方式进行合并采样，在这根输出线上，各个象素的电压或电流信号必然要进行（自动的）平均，因此，其信噪比的提高只是在于噪声合并后降

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低了$\sqrt{N}$，从而使信噪比提高最多$\sqrt{N}$倍。而采用本发明的电荷相加方式，例如通过读取电容存储电荷，实现电荷的累加，从而信号可以进行叠加而使得信噪比可以提高至少 N 倍， 比信号平均的方法高至少$\sqrt{N}$倍。也就是说，将 N 个信号以电荷相加的方法合并，理论上最高可以达到N^2个信号相平均的效果或更好(如下面所述)，这是效果非常显著的提高信噪比的手段。

紧邻象素相加，还带来另外一个显著的效果，就是，象素之间的相互干扰(cross-talking)效果被减弱。这是由于本来相互干扰的色彩，现在是合法的一体，也就是说，原来属于噪声的一部分信号，现在成了有效的信号部分，因此，N 个信号电荷相加带来信噪比的改进，可以接近理论上的上限，即$N\sqrt{N}$倍，从而，相当于N^3个信号相平均的效果。

在全图采样（即对一个图像的按最高分辨率进行采样）时，可以采用逐行扫描、隔行或跨行读取的方式，不需要提高时钟速度和采用帧缓存器，将大阵列图像的全图读取帧率在拍单张照时翻倍。如果增加 AD 转换器和行缓存，那么，全图读取帧率还可以提高更多。这个方法对于省去机械快门有非常重要的价值。

请注意本发明的逐行扫描、隔行或跨行读取的方式，与传统电视系统里的场扫描方式（interleaved scanning）是不同的。传统的场扫描方式，是隔行扫描，隔行读取，因此，奇数场和偶数场（无论是感光还是读取）在时间上差了一场，即半帧。而本发明的逐行扫描、隔行或跨行读取的方式，象素在感光时间顺序上却是与逐行扫描、逐行读取方式是完全一样的，只是行的读取次序做了变化。细节描述请见《一种多光谱感光器件及其采样方法》(中国申请号: 200910105948.2)和《一种感光器件及其读取方法、读取电路》(中国申请号: 200910106477.7) 。

在本发明的一种实施例中，所述的感光器件，所述色彩空间变换包括 RGB 到 CyYeMgX 空间的变换、RGB 到 YUV 空间的变换、或 CyYeMgX 到 YUV 空间的变换，其中 X 为 R(红)、G(绿)、B(兰)中的任一种。图 10 显示了一种利用色彩空间变换来实现子采样的一种方式。

实施方式中包括，上述电荷相加方式通过象素直接并联或将电荷同时转移到读取电容（FD）中完成。

如上所述，多景深感光器件中，第一合并单元或第二合并单元的基于色彩的合并采样方式包括同色合并方式、异色合并方式、混杂合并方式、或选择性抛弃多余色彩合并方式，且第一合并单元和第二合并单元采用的

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合并采样方式不同时为同色合并方式，也即两个合并单元中至少有一个合并单元不采用同色合并方式。

如上所述，第一合并单元或第二合并单元的基于位置的合并采样方式包括以下几种方式中的至少一种：直接输出到总线的信号自动平均方式、跳行或跳列方式、和逐个采样方式。亦即这几种基于位置的合并采样方式可以单独使用，也可以组合使用。

如上所述，在上述感光器件中，可以用色彩空间变换方式和后端数字图像缩放方式中的至少一种来实现所述第三合并采样单元的合并采样方式。

图 9 显示了一种异色象素电荷合并的方式。

实现上述子采样功能的是如图 25 所示的行地址解码控制器和列地址解码控制器。行地址解码控制器将输出两类信号，行选信号 Row[i]（每行一条线）和行控制矢量信号 RS[i]（每行一条或多条线），其中 i 为行的标号。类似地，列地址解码控制器将输出两类信号，列选信号 Col[j]（每列一条线）和列控制矢量信号 T[j]（每列一条或多条线），其中 j 为列的标号。

行选信号 Row[i]是用来做行的选择，而列选信号 Col[j]是用来做列的选择。这是两组相对标准的信号。行控制矢量信号 RS[i]是对现有 CMOS 行控制信号的扩展（每行一条线扩展到每行多条线），而列控制矢量信号 T[j]，有的 CMOS 感光器件根本没有，即使有，也是一列只有一个。

RS[i]和 T[j]用来控制感光象素的复位，清零，感光时间控制，电荷转移，象素合并，和象素读取。由于行列的对称性，RS[i]和 T[j]有很多种具体的实现方式。这些信号的具体实现方式并不受限。

如上所述，多光谱感光器件的全图采样方式包括逐行扫描、逐行读取方式或逐行扫描、隔行或跨行读取方式。

实施方式还包括制作一种感光系统，包括上述的多景深感光器件。

所述感光系统用于获取正面，背面，或双向的图像。

所述感光系统包括数码相机，照相手机，摄像机，视频或照相监控系统，图像识别系统，医学图像系统，军用、消防、和井下图像系统，自动跟踪系统，立体影像系统，机器视觉系统，汽车视觉或辅助驾驶系统，电子游戏系统，网络摄像头，红外和夜视系统，多光谱成像系统，和电脑摄像头。

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实施方式还包括实现一种景深扩展方法，包括步骤：在感光器件中设置至少两个可感应到光源的感光象素层，并将至少两个所述感光象素层按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号，被聚焦到不同的感光象素层。

景深扩展方法中，通过来自不同感光象素层的具有不同清晰度的图像而获取一幅清晰图像。

实施方式中还包括一种成像方法，或者说所述感光器件在成像中的应用，是设置镜头和包括至少两个可感应到光源的感光象素层的感光器件；将所述感光器件放置在距所述镜头特定距离，且至少两个所述感光象素层之间按预设距离间隔布置，使得来自镜头的不同光信号被聚焦到不同的所述感光象素层。

参见图 11-14，实施方式中还包括了一种光学成像系统，包括镜头和多景深感光器件，所述多景深感光器件布置在距所述镜头特定距离，包括至少两个可感应到光源的感光象素层；至少所述感光象素层之间按预设距离间隔布置，来自距所述感光器件特定距离的镜头的不同光信号，被聚焦到不同的感光象素层。

如图 13，可以是不同距离上的所有感兴趣波长的光，分别聚焦在每一感光象素层；或者如图 14，可以是相同距离上的不同波长的光，分别聚焦在每一感光象素层；也可以是不同距离上的不同波长的光，分别聚焦在每一感光象素层。

实施方式包括各个感光象素层聚焦的光，其波长按各个感光象素层距所述光学镜头从近到远逐渐增长。或者在各个感光象素层中，更远距离的光信号，被聚焦在离镜头更近的感光象素层。

例如，当包括两个可感应到光源的感光象素层，两个感光象素层分别位于镜头的第一象距和第二象距，可以通过光学镜头设计，将紫外光、兰色光、绿色光、青色光、或白色光聚焦在离镜头最近的感光象素层；相应的，将兰色光、绿色光、红色光、黄色光、或红外光聚焦在离镜头最远的感光象素层。

又如，当包括三个可感应到光源的感光象素层，三个感光象素层分别位于镜头的第一象距、第二象距、第三象距，可以通过光学镜头设计，将紫外光、兰色光、绿色光、或青色光聚焦在离镜头最近的感光象素层；相应的，将红色光、黄色光、可见光、或红外光聚焦在离镜头最远的感光象素层；相应的，将绿色光、黄色光、可见光、或红色光聚焦在中间的感光象素

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层。

又如，当包括四个可感应到光源的感光象素层，四个感光象素层分别位于镜头的第一象距、第二象距、第三象距、第四象距，可以通过光学镜头设计，将紫外光、兰色光、绿色光、或青色光聚焦在离镜头最近的感光象素层；相应的，将红色光、黄色光、白色光、或红外光聚焦在离镜头最远的感光象素层；相应的，将兰色光、绿色光、或青色光聚焦在离镜头第二近的感光象素层；相应的，将绿色光、红色光、白色光、或黄色光聚焦在离镜头第三近的感光象素层。

又如，当包括两个可感应到光源的感光象素层，两个感光象素层分别位于镜头的第一象距、第二象距，可以通过光学镜头设计，将紫外光或可见光聚焦在离镜头最近的感光象素层；将可见光或红外光聚焦在离镜头最远的感光象素层。

又如，当包括三个可感应到光源的感光象素层，三个感光象素层分别位于镜头的第一象距、第二象距、第三象距，可以通过光学镜头设计，将紫外光或白色光聚焦在离镜头最近的感光象素层；将白色光或红外光聚焦在离镜头最远的感光象素层；将白色光聚焦在中间的感光象素层。

又如，当包括四个可感应到光源的感光象素层，四个感光象素层分别位于镜头的第一象距、第二象距、第三象距、第四象距，可以通过光学镜头设计，将紫外光或白色光聚焦在离镜头最近的感光象素层；将白色光或红外光聚焦在离镜头最远的感光象素层；将白色光聚焦在离镜头第二近的感光象素层；将白色光聚焦在离镜头第三近的感光象素层。

需要注意的是，在上述例子中，对于包括所有感兴趣波长的光，例如白色光，如果说明白色光被聚焦到不同感光象素层，则其一般来源于不同距离，即例如离镜头最近的感光象素层聚焦的是无穷远处的白色光，离镜头最远的感光象素层聚焦的是感兴趣最短距离的白色光。即当两个感光象素层聚焦的光信号的频谱特性相同，则其必须具有不同的距离特性。

本发明的多景深感光器件，兼具多光谱的优异特性，可同时获得众多的彩色信号和其它光谱信号，例如在一种四层感光器件中，可沿光路按距光源从近到远布置一个感应紫外光的第一化学镀膜感光象素层、一个感应兰光，绿光，或青光的第一半导体感光象素层，一个感应红光，黄光，或绿光的第二半导体感光象素层，一个感应红外光的第二化学镀膜感光象素层。其中，第一半导体感光象素层和第二半导体感光象素层分别实现在两个半导体基层上，两个半导体基层之间设置一个具有预设厚度的透光层，

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第一化学镀膜感光象素层布置在第一半导体感光象素层所在基层的顶面上方；第二化学镀膜感光象素层布置在第二半导体感光象素层所在基层的底面下方。由此，不仅实现了景深扩展，且可几乎最大程度的利用入射光能量，在得到彩色的同时，也得到全光谱的信息，充分发挥不同感光材料的特点。这样一种四层多光谱感光器件，制作难度并不太高。如果结合采用前文中本人之前发明的先进采样和以电荷合并和色彩变换为显著特征的子采样电路和方法，更能够大幅地降低感光器件和系统的复杂度，从而为各种应用提供巨大的方便和崇高的性能。

本发明的多景深感光器件，首先实现的第一种特殊用途是景深扩展，现有的 EDoF 主要是使用了光学和数学的手段实现景深扩展，一般需要借助例如镜头等进行自动对焦，相比之下，本发明是直接的通过器件内的不同感光象素层按预设距离间隔设置这样的物理手段实现景深扩展。其次实现的第二种特殊用途是实现全局电子快门，现有的全局电子快门 (Global Shutter) 主要是使用了读取电路的手段，相比之下，本发明利用不感光的转移和读取象素，可以在不用机械快门的情况下，实现高象素的高速拍照。当这两种实现(即景深扩展和全局电子快门)，在同一个感光器件上得以集成的时候，多层多光谱感光器件的巨大威力就得以充分的发挥。因此，本发明在很多指标和性能上，大幅超越现有的方法。

本发明的多景深感光器件，借助于调整不同感光象素层的距离，除了大幅提高灵敏度以外，还能大幅提高系统景深范围，从而让图像更清楚，系统反应速度更快，应用面更宽，乃至消除某些应用中的自动对焦需求。本发明的多景深感光器件在其涵盖的景深范围，能够快速地获取清晰的图像，而不需要经过一个调焦的过程。景深扩展除了能够降低自动对焦的难度和成本外，甚至在某些应用中如手机照相，微距照相，或远距照相，能够彻底消除自动对焦的需求。景深扩展还能让同一张照片里处于不同距离的物体同时清楚，这在一些特殊应用中也是极有用的，而这是自动对焦所不能做到的，因为现有的自动对焦系统，只能让某个距离内的物体清楚成像，而不能让非常宽的一个范围内的物体都清楚。因此，本发明的景深扩展实现，在具有自动对焦能力的系统里，也仍然具备有很大的价值

由于本发明的多景深感光器件的高灵敏度，其感光速度也可大幅提高，从而为在很多应用中取下机械快门提供了可能。由此，在本发明的多景深感光器件中，还提出一种具有跨层读取功能的全局电子快门的实现，以期

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取代某些应用中可能需要的机械快门。全局电子快门作用是在一瞬间，将感光象素里的电荷或电压值拷贝到不感光的读取象素里去，以便读取电路从容的读出。

结合景深扩展全局电子快门的实现，将二者集成在一个感光器件上时，一个不需要自动对焦和机械快门的高性能、高速度、高象素感光系统，就可以芯片的方式来实现，大大地降低系统的尺寸、复杂度、功耗和成本，为很多新的应用提供了可能。

这种带有全局电子快门的或多景深的感光器件，可为感光系统省去机械快门或者省去自动对焦系统(或者降低对自动对焦系统的要求)，并在不加快感光器件时钟的情况下，实现高速的电子快门或清晰成像。

在极大地简化了感光系统的机械复杂度的要求的同时，本发明采用两层或多层的布局，结合先进的两层或多层互补或正交色彩图案排列的方法，能够最大化的利用入射光子的能量，不用或只用少许的彩色滤光膜，从而达到或接近到达光电转换效率的理论上限，并在完整地重建彩色的同时，获得其它光谱的图像，包括紫外线图像，近红外图像，和远红外图像。

当感光象素层与读取电路分层后，读取电路层的读取电路和处理计算可以做得非常精细和复杂，为单芯片感光系统的制作，提供了巨大的便利。

这种多景深感光器件可同时获得众多的彩色信号和其它光谱信号，采用本人之前发明的先进的采样和以电荷合并和色彩变换为显著特征的子采样电路和方法，能够大幅地降低感光器件和系统的复杂度，从而为各种应用提供巨大的方便和崇高的性能。

这种多景深感光器件，可用于正面感光，背面感光，或双向感光。通过精细布置各层感光器件的象素感应光谱段和各层色彩图案的合理布局，可以产生各种优选的多光谱感光器件，如高灵敏度彩色感光器件，高灵敏度彩色和红外感光器件，无杂色（杂色由插值引起的）的高灵敏度彩色或多光谱感光器件等等。

采用主动象素和被动象素读取相结合的手段，可以获得超低功耗感光器件，超高动态范围感光器件。

以上内容是结合具体的实施方式对本发明所作的进一步详细说明，不能认定本发明的具体实施只局限于这些说明。对于本发明所属技术领域的普通技术人员来说，在不脱离本发明构思的前提下，还可以做出若干简单推演或替换，都应当视为属于本发明的保护范围。

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权 利 要 求 书

1. 一种多景深感光器件，其特征在于，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

2. 如权利要求 1 所述的感光器件，其特征在于，所述感光象素层包括化学镀膜感光象素层和半导体感光象素层中的至少一者。

3. 如权利要求 2 所述的感光器件，其特征在于，所述化学镀膜感光象素层包括量子点感光象素。

4. 如权利要求 2 所述的感光器件，其特征在于，所述半导体感光象素层包括 CMOS 光敏二极管、CMOS 感光门、CCD 光敏二极管、CCD 感光门、和具有双向电荷转移功能的 CMOS 和 CCD 感光二极管和感光门。

5. 如权利要求 1-4 任一所述的感光器件，其特征在于，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

6. 如权利要求 5 所述的感光器件，其特征在于，波长更短的光信号被聚焦到离镜头更近的感光象素层。

7. 如权利要求 6 所述的感光器件，其特征在于，所述感光象素层为两层，紫色光、兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

8. 如权利要求 6 所述的感光器件，其特征在于，所述感光象素层为三层，紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层；兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层；红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层。

9. 如权利要求 5 所述的感光器件，其特征在于，更远距离的光信号被聚焦到离镜头更近的感光象素层。

10. 如权利要求 9 所述的感光器件，其特征在于，所述感光象素层为两层，无穷远处的光信号被聚焦到离镜头较近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头较远的感光象素层。

11. 如权利要求 10 所述的感光器件，其特征在于，无穷远处的紫色光、

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兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，感兴趣最短距离的绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

12. 如权利要求 9 所述的感光器件，其特征在于，所述感光象素层为三层，无穷远处的光信号被聚焦到离镜头最近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的光信号被聚焦到位于中间的感光象素层。

13. 如权利要求 12 所述的感光器件，其特征在于，所述感光象素层为三层，无穷远处的紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层，感兴趣最短距离的红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层。

14. 如权利要求 10-13 任一所述的感光器件，其特征在于，所述感兴趣最短距离包括 2mm, 5mm, 7mm, 1cm, 2cm, 3cm, 5cm, 7cm, 10cm, 20cm, 30cm, 40cm, 50cm, 60cm, 70cm, 80cm, 100cm, 或 150cm。

15. 如权利要求 1-14 任一所述的感光器件，其特征在于，至少两个所述感光象素层之间设置有透光层。

16. 如权利要求 1-15 任一所述的感光器件，其特征在于，所述感光象素层中的感光象素为正面感光象素、背面感光象素、或双向感光象素。

17. 如权利要求 16 所述的感光器件，其特征在于，当感光象素为双向感光象素时，其感光选向方式为隔离选向、分时选向、分区选向、或象素选向。

18. 如权利要求 1-17 任一所述的感光器件，其特征在于，所述感光象素层中的感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个互补谱段或子谱段；或者所述化学镀膜感光象素和半导体感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个正交谱段或子谱段。

19. 如权利要求 18 所述的感光器件，其特征在于，所述互补谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，

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黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱；

所述正交谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱。

20. 如权利要求 1-19 任一所述的感光器件，其特征在于，每一感光象素层中的色彩排列包括同一排列、水平排列、垂直排列、对角排列、广义贝叶排列、YUV422 排列、横向 YUV422 排列、蜂窝排列、均布排列。

21. 如权利要求 1-20 任一所述的感光器件，其特征在于，至少一个所述感光象素层中的部分或全部感光象素的正面、背面或双面设置有滤光膜，所述滤光膜的选频特性包括红外截止滤波、兰色带通、绿色带通、红色带通、青色带通、黄色带通、品红色带通、或可见光带通。

22. 如权利要求 1-21 任一所述的感光器件，其特征在于，所述感光象素层中的相邻两层各自设有读取电路；或者所述感光象素层的相邻两层共用读取电路。

23. 如权利要求 22 所述的感光器件，其特征在于，所述读取电路为主动象素读取电路、被动象素读取电路、或主动象素与被动象素混合读取电路。

24. 如权利要求 23 所述的感光器件，其特征在于，所述主动象素包括 3T、4T、5T 或 6T 主动象素。

25. 如权利要求 22 所述的感光器件，其特征在于，所述读取电路的共用方式包括单层或上下层 4 点共享方式、单层或上下层 6 点共享方式、单层或上下层 8 点共享方式、或单层或上下层任意点共享方式。

26. 如权利要求 22-25 所述的感光器件，其特征在于，所述读取电路包括用于对每一感光象素层的象素阵列中的紧邻的同行异列、异行同

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列、或异行异列的象素间进行两两合并采样，获得第一合并象素的采样数据的第一合并单元；以及用于对第一合并单元得到的第一合并象素的采样数据进行合并采样以获得第二合并象素的采样数据的第二合并单元。

27. 如权利要求 26 所述的感光器件，其特征在于，所述读取电路还包括第三合并单元，用于对第二合并单元得到的第二合并象素的采样数据进行合并采样以获得第三合并象素的采样数据。

28. 如权利要求 26 或 27 所述的感光器件，其特征在于，所述第一合并单元或第二合并单元的象素合并方式为相同或不同色彩象素间的电荷相加方式或信号平均方式，其中不同色彩象素间的象素合并方式遵照色彩空间变换的方式，以满足色彩重建的要求。

29. 如权利要求 28 所述的感光器件，其特征在于，所述色彩空间变换包括 RGB 到 CyYeMgX 空间的变换、RGB 到 YUV 空间的变换、或 CyYeMgX 到 YUV 空间的变换，其中 X 为 R(红)、G(绿)、B(兰)中的任一种。

30. 如权利要求 29 所述的感光器件，其特征在于，所述电荷相加方式通过象素直接并联或将电荷同时转移到读取电容（FD）中完成。

31. 如权利要求 26-30 所述的感光器件，其特征在于，所述第一合并单元或第二合并单元的基于色彩的合并采样方式包括同色合并方式、异色合并方式、混杂合并方式、或选择性抛弃多余色彩合并方式，且第一合并单元和第二合并单元采用的合并采样方式不同时为同色合并方式。

32. 如权利要求 26-31 所述的感光器件，其特征在于，所述第一合并单元或第二合并单元的基于位置的合并采样方式包括以下几种方式中的至少一种：直接输出到总线的信号自动平均方式、跳行或跳列方式、和逐个采样方式。

33. 如权利要求 27-32 所述的感光器件，其特征在于，所述第三合并单元的合并采样方式包括：色彩空间变换方式和后端数字图像缩放方式中的至少一种。

34. 如权利要求 1-33 所述的感光器件，其特征在于，包括具有跨层读取功能的全局电子快门，所述全局电子快门包含多个可同时转移并读取一层或多层感光象素层的电荷或电压值的不感光的转移和读取象素。

35. 如权利要求 34 所述的感光器件，其特征在于，所述多个不感光的转

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移和读取象素位于不感光象素转移和读取层；或者位于所述感光象素层。

36. 如权利要求 35 所述的感光器件，其特征在于，每一感光象素层，设置有一个紧邻的不感光象素转移和读取层。

37. 如权利要求 34-36 任一所述的感光器件，所述不感光转移和读取象素由半导体电路制成。

38. 一种景深扩展方法，其特征在于，包括:
在感光器件中设置至少两个可感应到光源的感光象素层，并将至少两个所述感光象素层按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

39. 如权利要求 38 所述的景深扩展方法，其特征在于，通过来自不同感光象素层的具有不同清晰度的图像而获取一幅清晰图像。

40. 一种光学成像方法，其特征在于，包括:
设置镜头和包括至少两个可感应到光源的感光象素层的感光器件;
将所述感光器件放置在距所述镜头特定距离，且至少两个所述感光象素层之间按预设距离间隔布置，使得来自镜头的不同光信号被聚焦到不同的所述感光象素层。

41. 一种光学成像系统，其特征在于，包括镜头和多景深感光器件，所述多景深感光器件布置在距所述镜头特定距离，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自所述镜头的不同光信号被聚焦到不同的所述感光象素层。

42. 如权利要求 41 所述的光学成像系统，其特征在于，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

43. 如权利要求 42 所述的光学成像系统，其特征在于，波长更短的光信号被聚焦到离镜头更近的感光象素层。

44. 如权利要求 42 所述的光学成像系统，其特征在于，更远距离的光信号被聚焦到离镜头更近的感光象素层。

45. 一种感光系统，其特征在于，包括如权利要求 1-35 任一所述的感光器件。

46. 如权利要求 45 所述的感光系统，其特征在于，所述感光系统包括数码相机，照相手机，摄像机，视频或照相监控系统，图像识别系统，医学图像系统，军用、消防或井下图像系统，自动跟踪系统，立体

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影像系统，机器视觉系统，汽车视觉或辅助驾驶系统，电子游戏系统，网络摄像头，红外和夜视系统，多光谱成像系统，和电脑摄像头中的一种。

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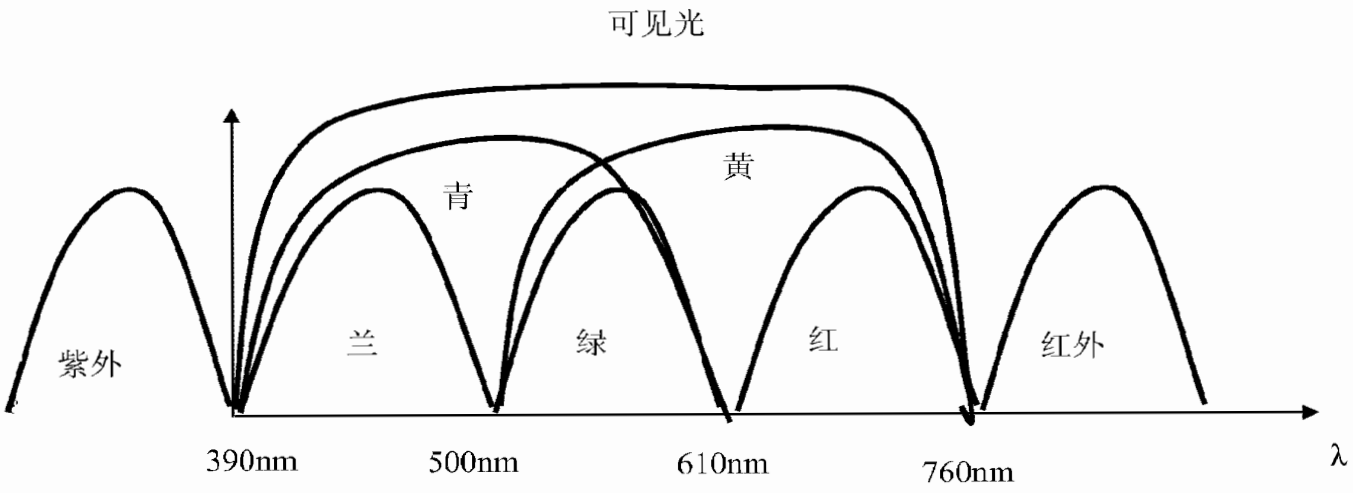

可见光
紫外
兰
青
绿
黄
红
红外
390nm
500nm
610nm
760nm
λ

图 1

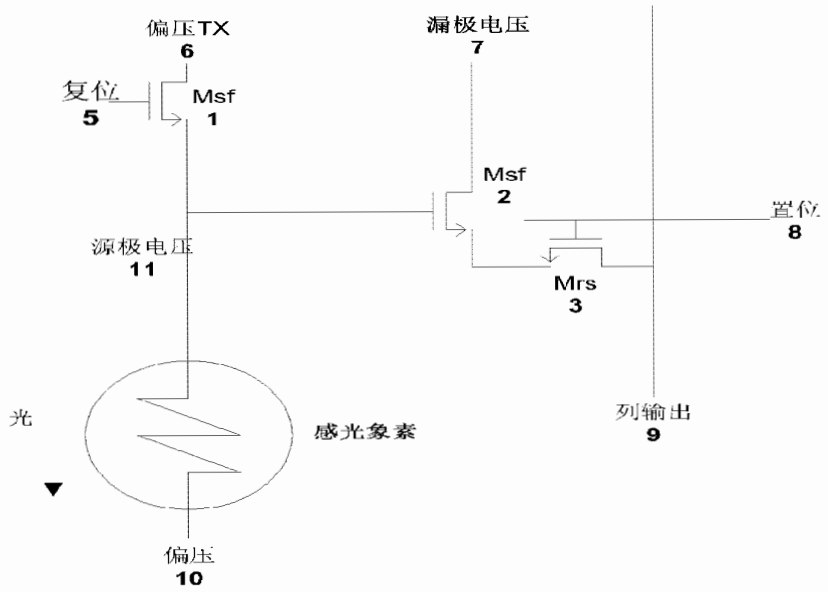

偏压TX
6
复位
5
Msf
1
漏极电压
7
Msf
2
置位
8
源极电压
11
Mrs
3
光
感光象素
列输出
9
偏压
10

图 2

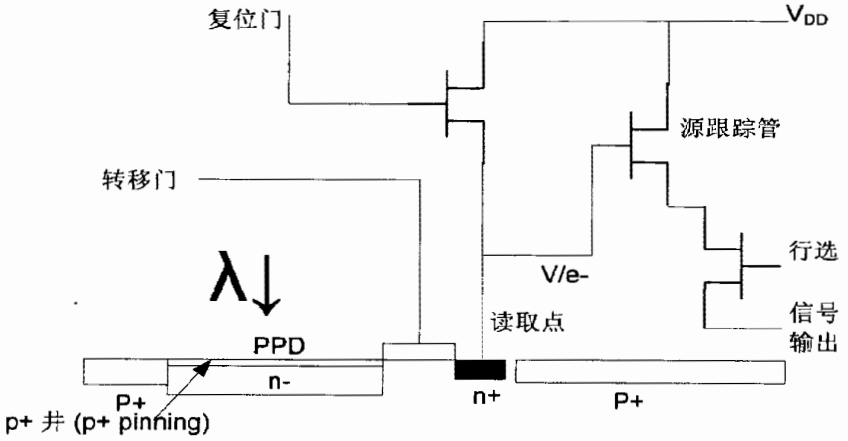


图 3

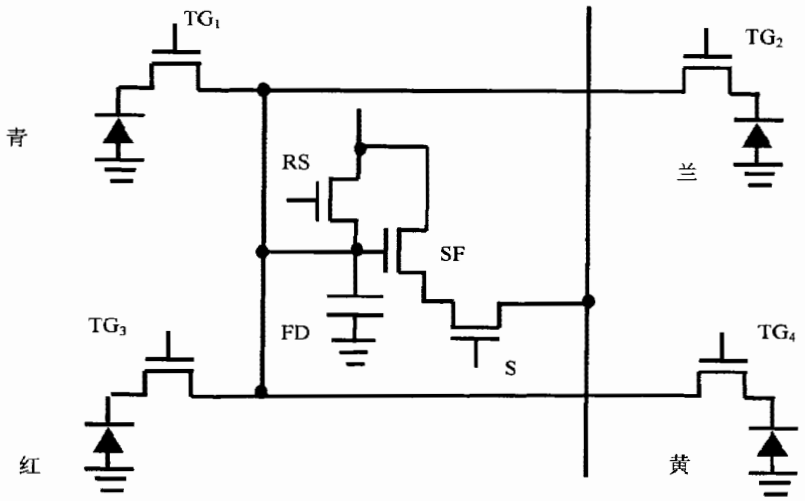


图 4

SAMSUNG EX. 1002 - 1553/1684

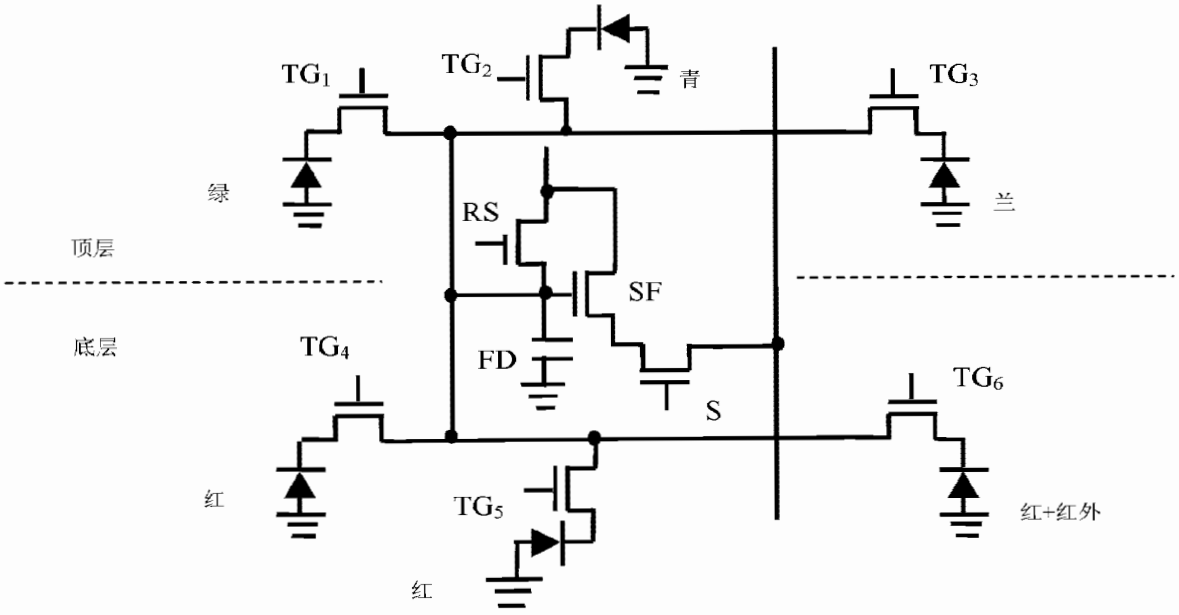


图 5

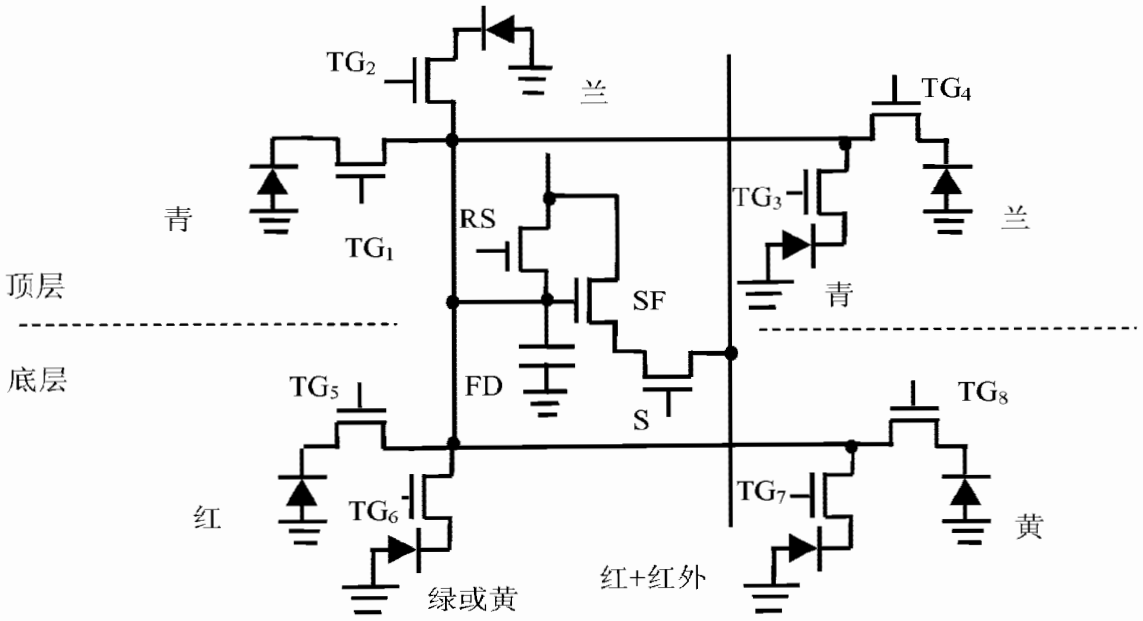


图 6

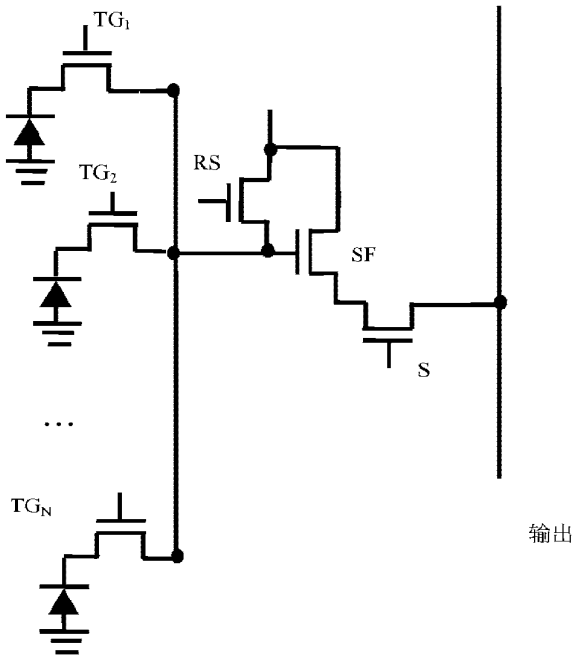

TG1
TG2
RS
SF
S
TGN
输出

图 7

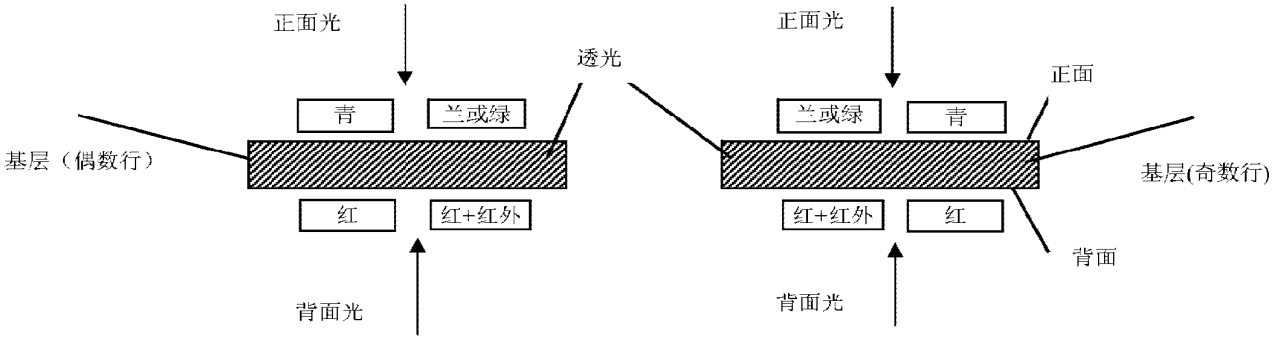

正面光
透光
青
兰或绿
基层（偶数行）
红
红+红外
背面光
正面光
正面
兰或绿
青
基层(奇数行)
红+红外
红
背面
背面光

图 8

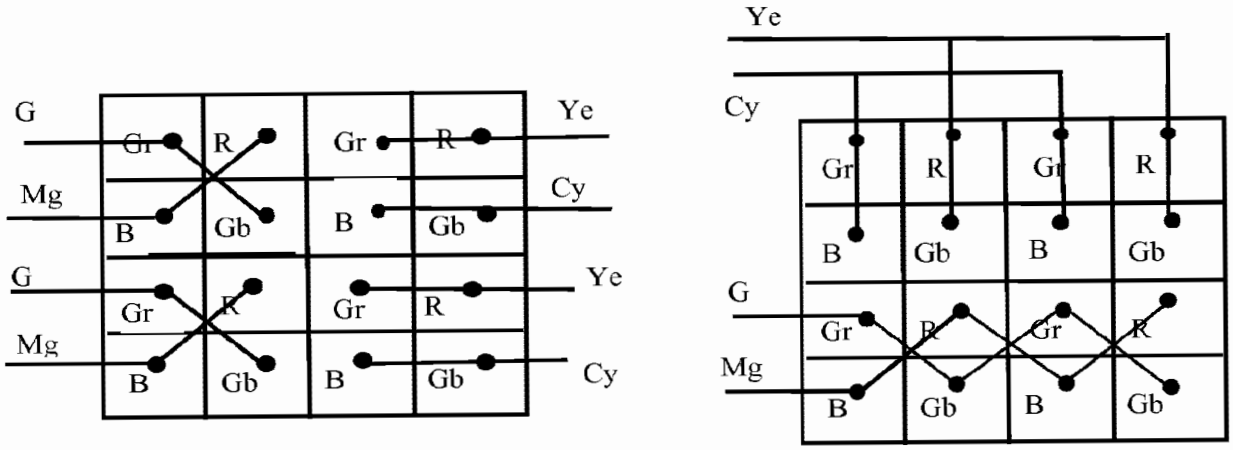


图 9

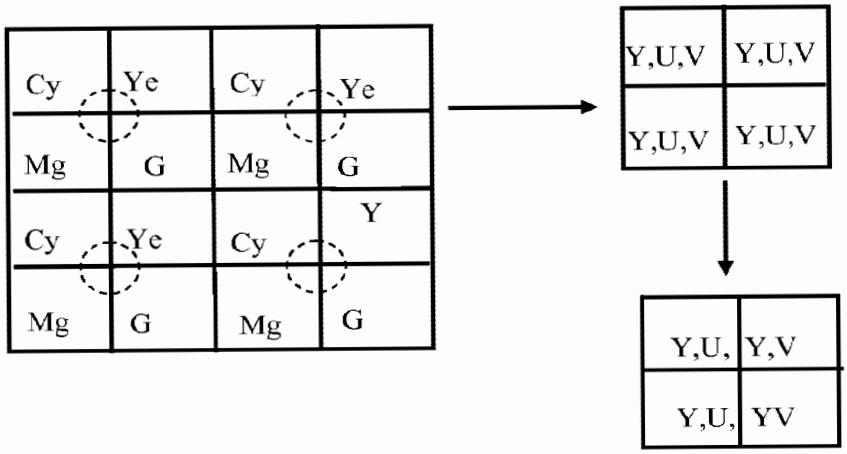


图 10

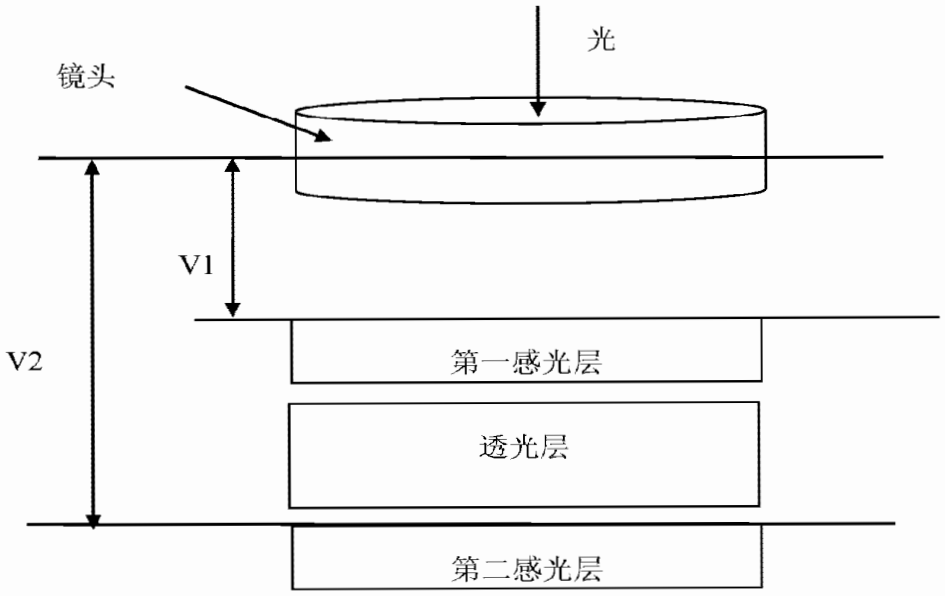


图 11

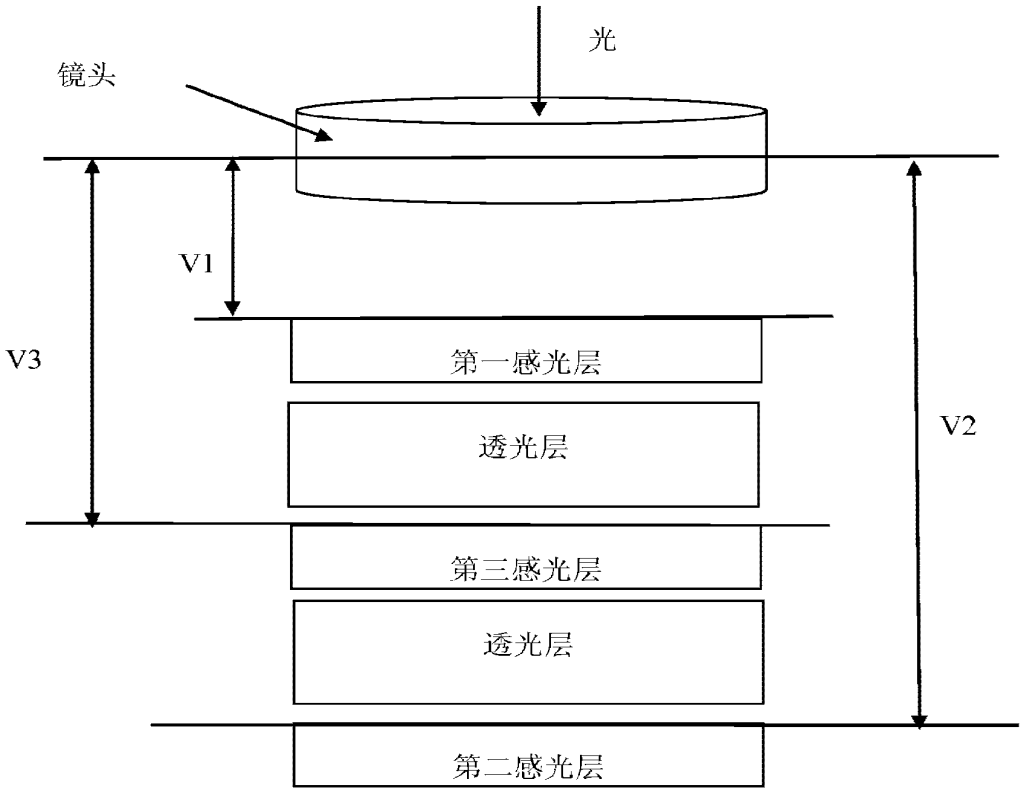


图 12

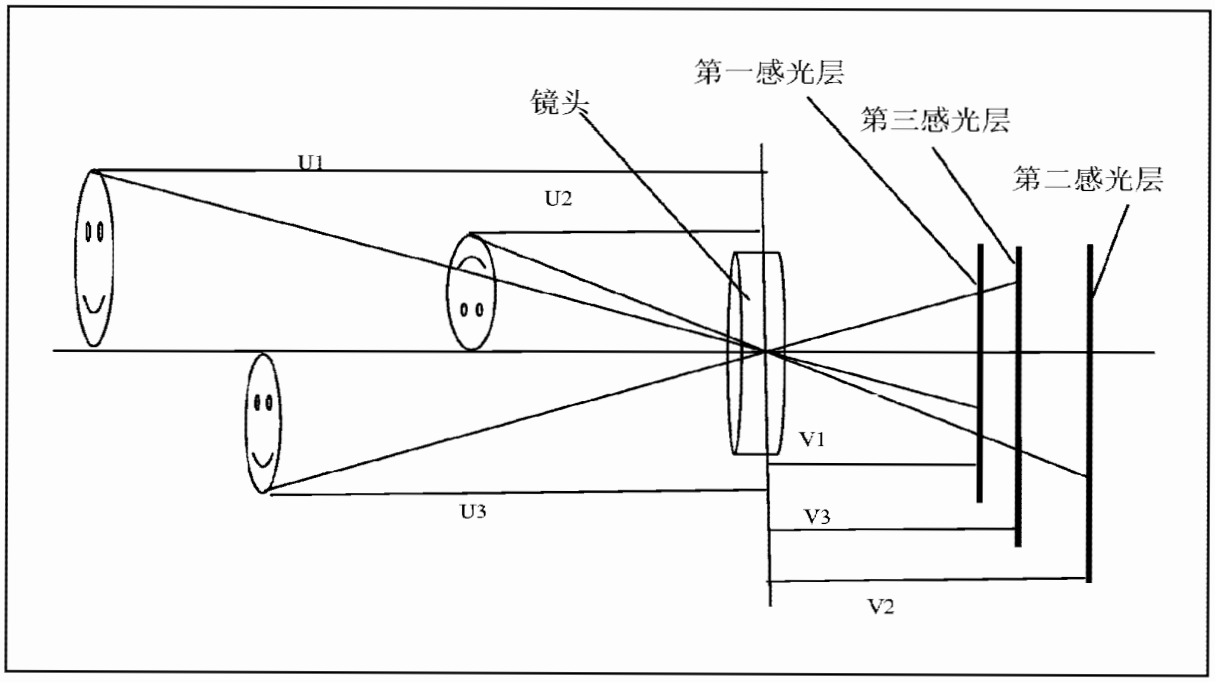


图 13

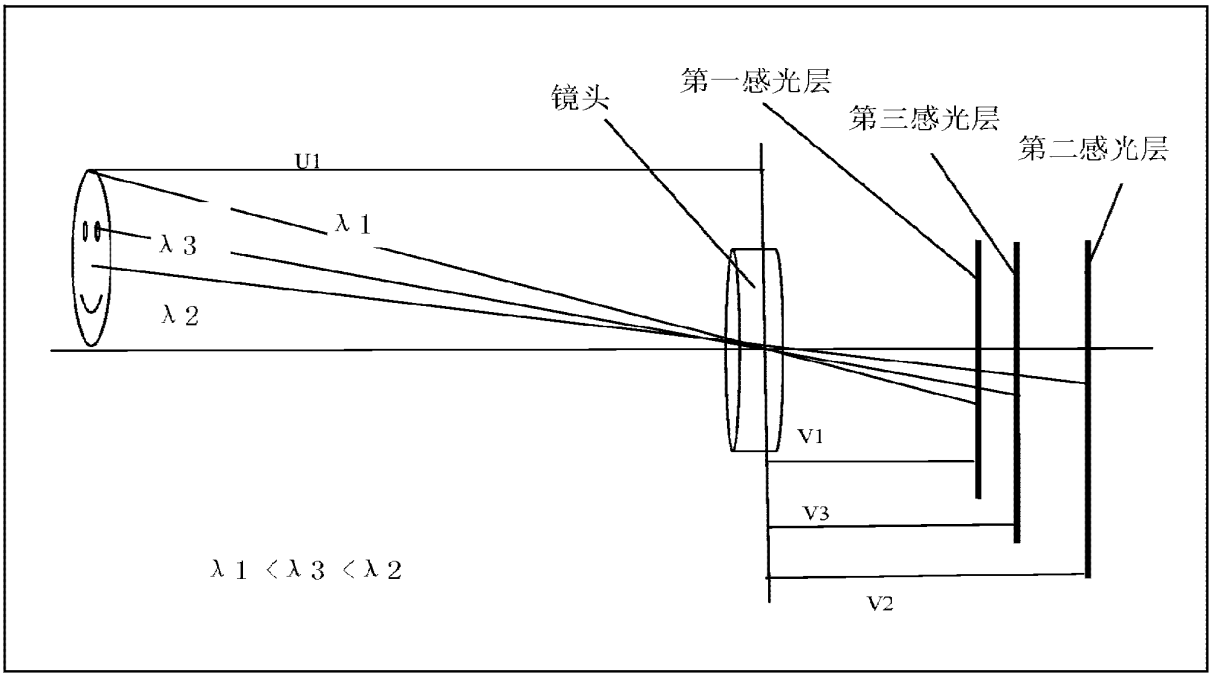


图 14

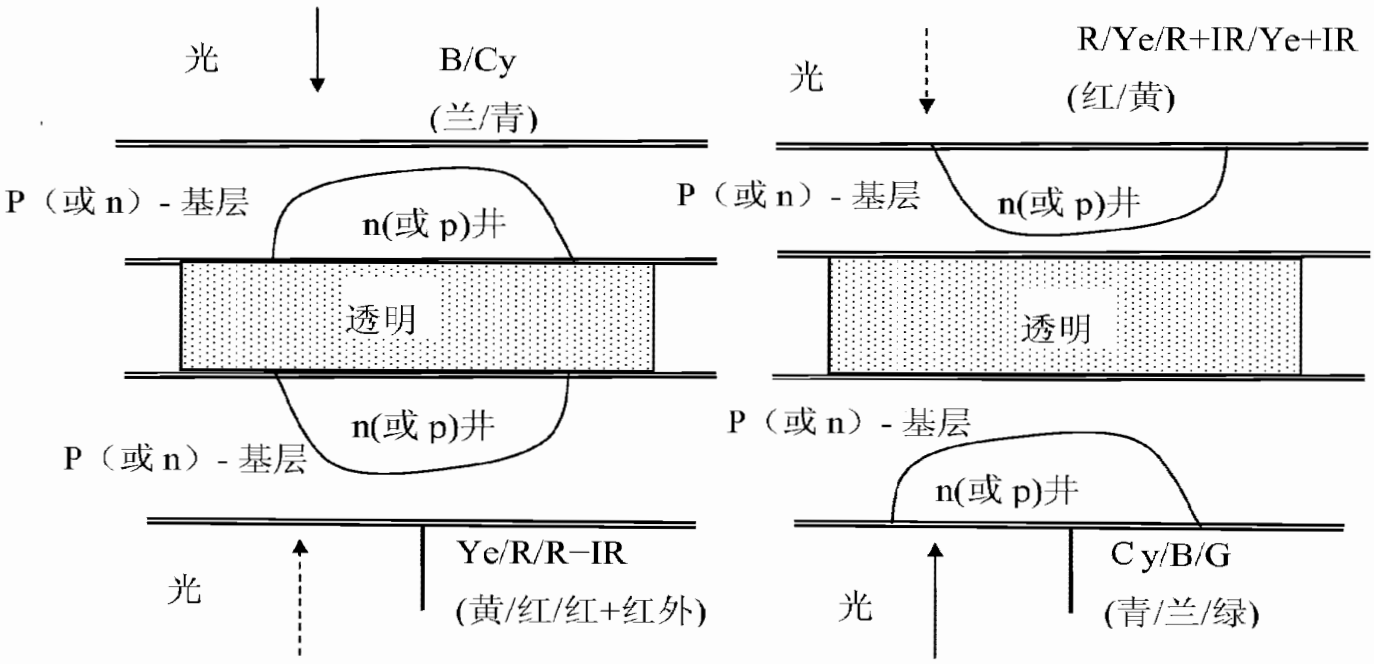

光
B/Cy
(兰/青)
P（或 n）- 基层
n(或 p)井
透明
n(或 p)井
P（或 n）- 基层
光
Ye/R/R−IR
(黄/红/红+红外)
光
R/Ye/R+IR/Ye+IR
(红/黄)
P（或 n）- 基层
n(或 p)井
透明
P（或 n）- 基层
n(或 p)井
光
Cy/B/G
(青/兰/绿)

图 15

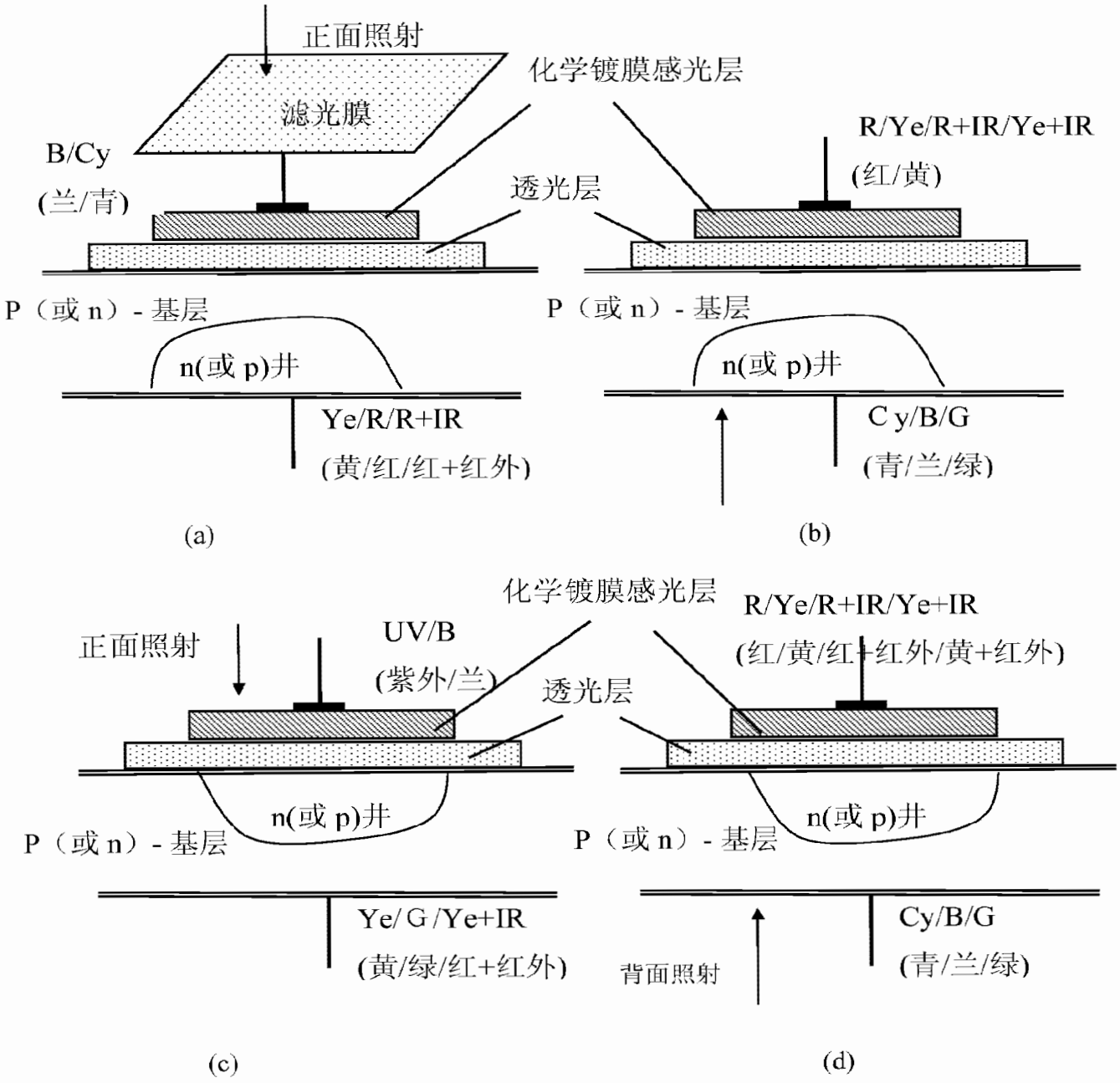

正面照射
化学镀膜感光层
滤光膜
B/Cy
(兰/青)
透光层
R/Ye/R+IR/Ye+IR
(红/黄)
P（或 n）- 基层
n(或 p)井
Ye/R/R+IR
(黄/红/红+红外)
(a)
P（或 n）- 基层
n(或 p)井
C y/B/G
(青/兰/绿)
(b)
化学镀膜感光层
R/Ye/R+IR/Ye+IR
(红/黄/红+红外/黄+红外)
正面照射
UV/B
(紫外/兰)
透光层
n(或 p)井
P（或 n）- 基层
Ye/ G /Ye+IR
(黄/绿/红+红外)
(c)
n(或 p)井
P（或 n）- 基层
Cy/B/G
(青/兰/绿)
背面照射
(d)

图 16

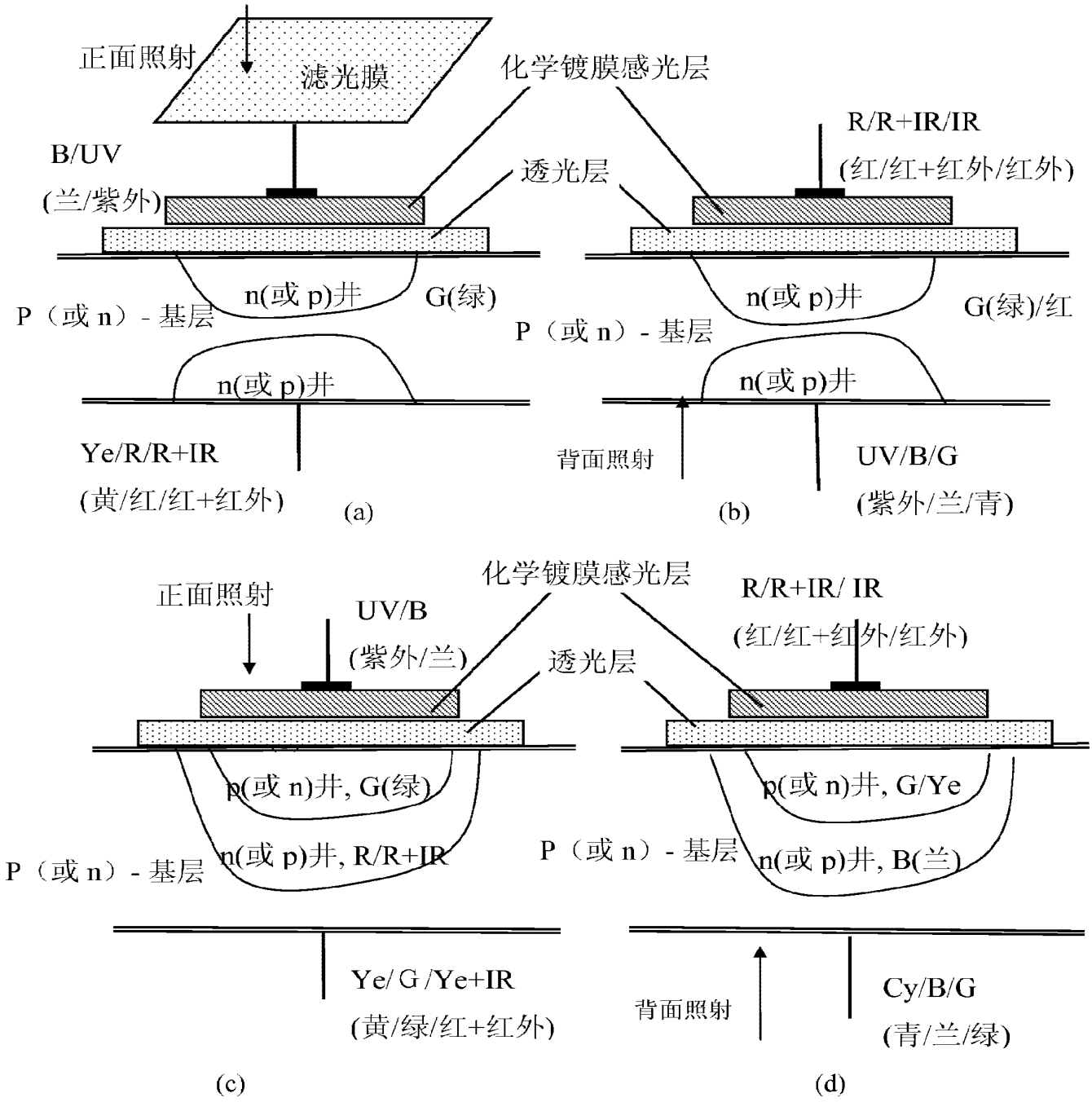

正面照射
滤光膜
化学镀膜感光层
B/UV
(兰/紫外)
透光层
n(或 p)井
G(绿)
P（或 n）- 基层
n(或 p)井
Ye/R/R+IR
(黄/红/红+红外)
(a)
R/R+IR/IR
(红/红+红外/红外)
n(或 p)井
G(绿)/红
P（或 n）- 基层
n(或 p)井
背面照射
UV/B/G
(紫外/兰/青)
(b)
正面照射
UV/B
(紫外/兰)
化学镀膜感光层
透光层
R/R+IR/ IR
(红/红+红外/红外)
p(或 n)井, G(绿)
n(或 p)井, R/R+IR
P（或 n）- 基层
Ye/ G /Ye+IR
(黄/绿/红+红外)
(c)
p(或 n)井, G/Ye
n(或 p)井, B(兰)
P（或 n）- 基层
背面照射
Cy/B/G
(青/兰/绿)
(d)

图 17

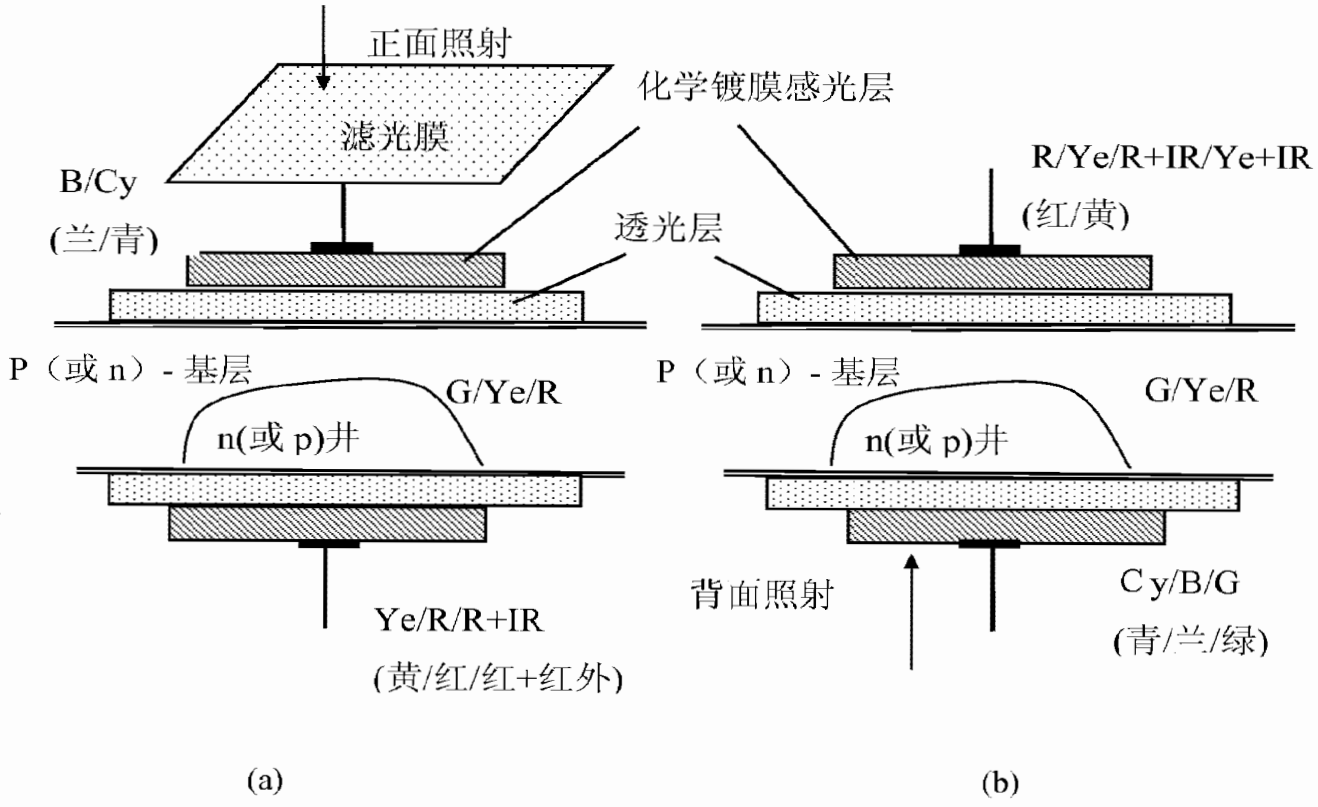

正面照射
滤光膜
化学镀膜感光层
B/Cy
(兰/青)
透光层
R/Ye/R+IR/Ye+IR
(红/黄)
P（或 n）- 基层
G/Ye/R
n(或 p)井
Ye/R/R+IR
(黄/红/红+红外)
P（或 n）- 基层
G/Ye/R
n(或 p)井
背面照射
Cy/B/G
(青/兰/绿)
(a)
(b)

图 18

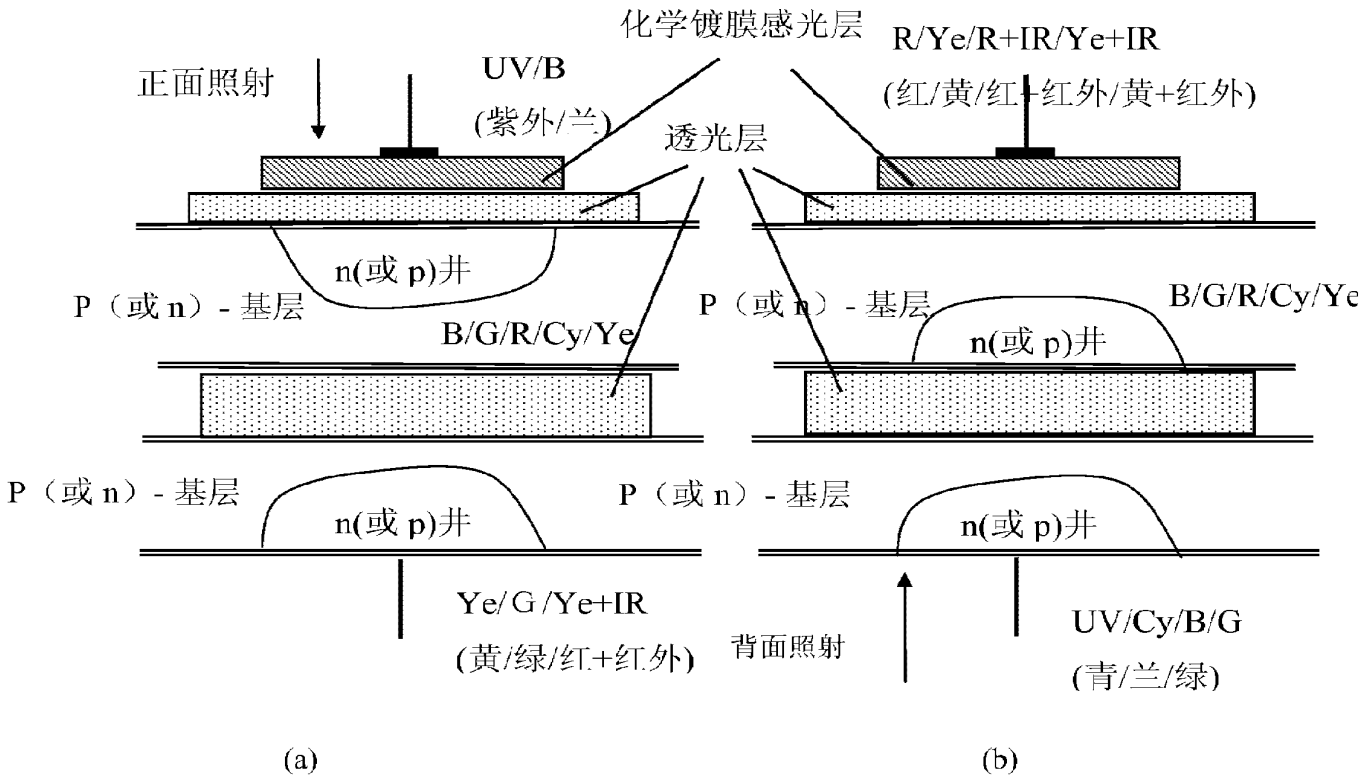

化学镀膜感光层
R/Ye/R+IR/Ye+IR
(红/黄/红+红外/黄+红外)
正面照射
UV/B
(紫外/兰)
透光层
n(或 p)井
P（或 n）- 基层
B/G/R/Cy/Ye
n(或 p)井
P（或 n）- 基层
B/G/R/Cy/Ye
P（或 n）- 基层
n(或 p)井
P（或 n）- 基层
n(或 p)井
Ye/G/Ye+IR
(黄/绿/红+红外)
背面照射
UV/Cy/B/G
(青/兰/绿)
(a)
(b)

图 19

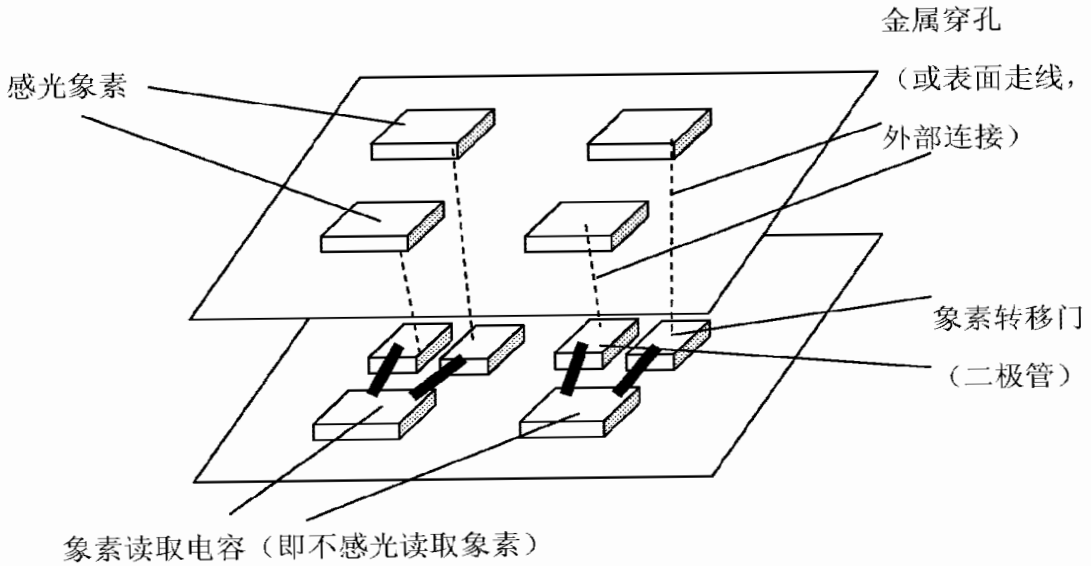


图 20

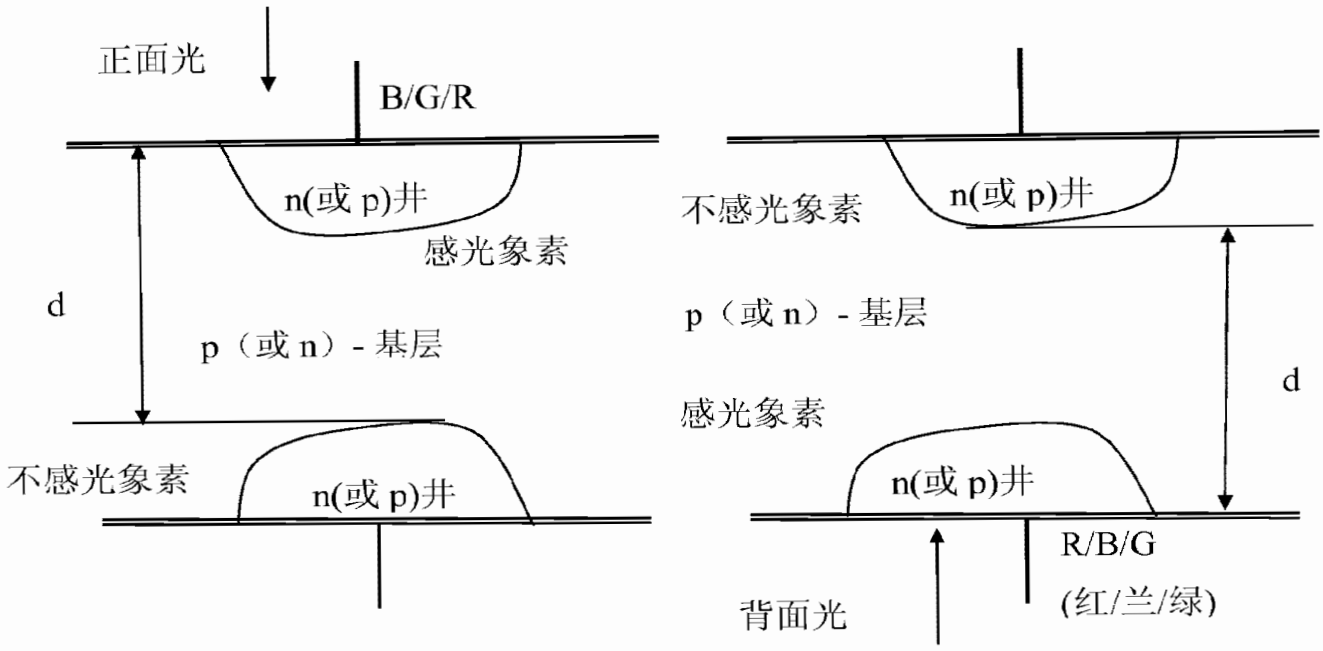

正面光
B/G/R
n(或 p)井
感光象素
d
p（或 n）- 基层
不感光象素
n(或 p)井
不感光象素
n(或 p)井
p（或 n）- 基层
d
感光象素
n(或 p)井
R/B/G
(红/兰/绿)
背面光

图 21

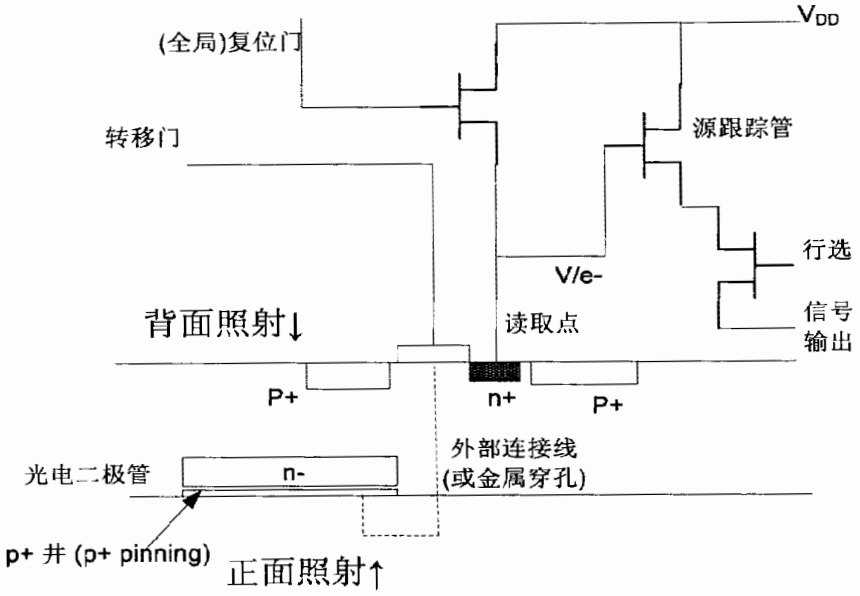


图 22

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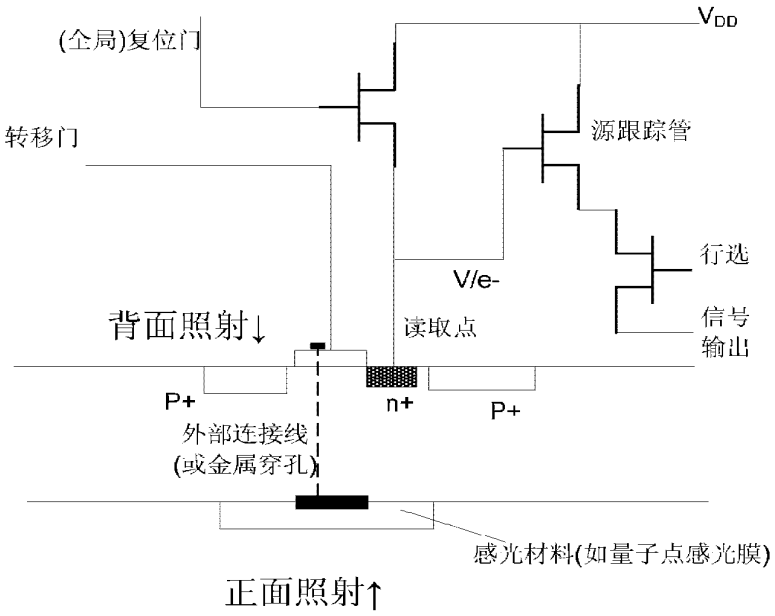

(全局)复位门
V_{DD}
转移门
源跟踪管
行选
V/e-
背面照射↓
读取点
信号
输出
P+
n+
P+
外部连接线
(或金属穿孔)
感光材料(如量子点感光膜)
正面照射↑

图 23

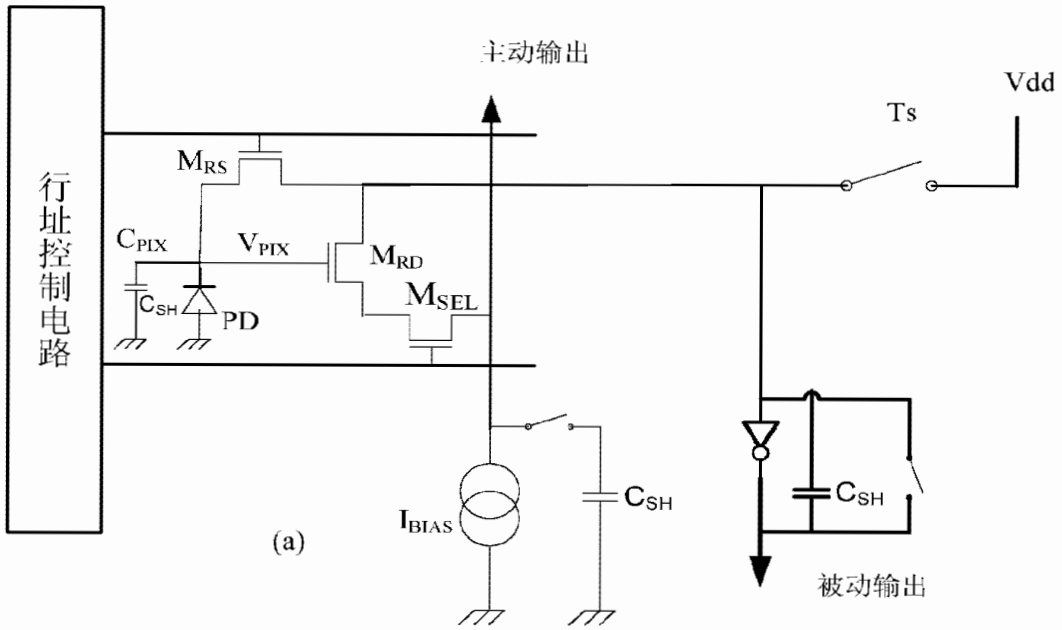

行址控制电路
主动输出
Vdd
Ts
M_{RS}
C_{PIX}
V_{PIX}
M_{RD}
M_{SEL}
C_{SH}
PD
I_{BIAS}
C_{SH}
C_{SH}
被动输出
(a)

图 24

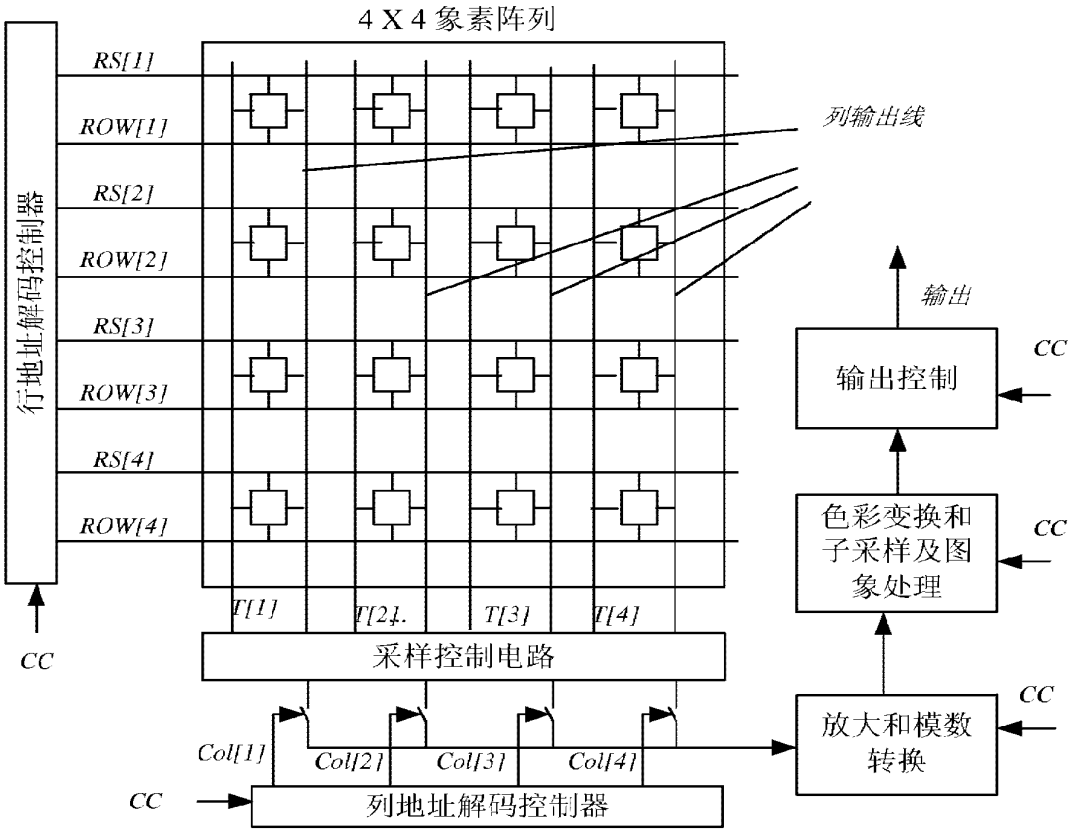

4 X 4 象素阵列
RS[1]
ROW[1]
RS[2]
ROW[2]
RS[3]
ROW[3]
RS[4]
ROW[4]
行地址解码控制器
列输出线
输出
输出控制
CC
色彩变换和
子采样及图
象处理
CC
T[1]
T[2]
T[3]
T[4]
采样控制电路
CC
放大和模数
转换
CC
Col[1]
Col[2]
Col[3]
Col[4]
CC
列地址解码控制器

图 25

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/076338

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS,CNKI,WPI,EPODOC: photo sensitive pixel lens signal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN101345248B (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD et al) 14 Jul.2010 (14.07.2010) embodiment of the description figs. 5-16	1,4-14,18-21,38-46
Y		2-3,15-17,22-37
Y	CN101740587A (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD) 16 Jun.2010 (16.06.2010) figs. 9-14	15-17
Y	CN101807590A (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD) 18 Aug.2010 (18.08.2010) [0043]-[0057] of the description, figs. 7-17	15-17,22-25

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 Mar.2012 (21.03.2012)	**29 Mar. 2012 (29.03.2012)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer ZHONG, Yi Telephone No. (86-10)62411594

Form PCT/ISA /210 (second sheet) (July 2009)

SAMSUNG EX. 1002 - 1573/1684

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/076338

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN101834974A (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD) 15 Sep.2010 (15.09.2010) claims, [0076]-[0091] of the description, figs. 1-26	25-37
Y	WO2008131313A2 (TIAN et al) 30 Oct.2008 (30.10.2008) The whole document	2-3, 25-37
X	US2006266921A1 (KANG et al) 30 Nov.2006 (30.11.2006) Figs.7-10	1,38,40,41,45
X	JP2005526458A (MICRON TECHNOLOGY INC) 2 Sep.2005 (02.09.2005) Fig. 3	1,38,40,41,45
E	CN102244083A (BORIS MULTI-MEDIA HOLDINGS INC) 16 Nov.2011 (16.11.2011) The whole document	1-5,20-33
E	CN102263114A (BORIS MULTI-MEDIA HOLDINGS INC) 30 Nov.2011 (30.11.2011) The whole document	1-46

SAMSUNG EX. 1002 - 1574/1684

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/076338

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN101345248B	14.07.2010	CN101345248A	14.01.2009
		WO2009006776A1	15.01.2009
		EP2172973A1	07.04.2010
		US2010141771A1	10.06.2010
		KR20100057599A	31.05.2010
		CA2705315A1	15.01.2009
		INMUMNP201000137E	16.07.2010
		JP2010532869A	14.10.2010
CN101740587A	16.06.2010	None	
CN101807590A	18.08.2010	None	
CN101834974A	22.09.2010	None	
CN102244083A	16.11.2011	None	
CN102263114A	30.11.2011	None	
WO2008131313A2	30.10.2008	WO2008131313A3	11.12.2008
		US2009152664A1	18.06.2009
		EP2143141A2	13.01.2010
		US2010187404A1	29.07.2010
		US2010187408A1	29.07.2010
		US7923801B2	12.04.2011
		CN102017147A	13.04.2011
		US8013412B2	06.09.2011
		US8004057B2	23.08.2011
		US2011297915A1	08.12.2011
		US2011297815A1	08.12.2011
		US2011303897A1	15.12.2011
		US2011303898A1	15.12.2011
		US2011309238A1	22.12.2011
		US2011309236A1	22.12.2012
US2006266921A1	30.11.2006	JP2006332602A	07.12.2006
		CN1870282A	29.11.2006

SAMSUNG EX. 1002 - 1575/1684

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/076338

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
		KR20060122136A	30.11.2006
		KR100665177B1	09.01.2007
		US7348539B2	25.03.2008
		TW200642077A	01.12.2006
		CN100481479C	22.04.2009
		TW306308B1	11.02.2009
		JP4418443B2	17.02.2010
JP2005526458A	02.09.2005	US2003211405A1	13.11.2003
		WO3098940A1	27.11.2003
		AU2003269305A1	02.12.2003
		US6783900B2	31.08.2004
		EP1506679A1	16.02.2005
		KR20050003456A	10.01.2005
		CN1669332A	14.09.2005
		EP1506679B1	27.12.2006
		KR100621086B1	14.09.2006
		DE60310706E	08.02.2007
		DE60310706T2	11.10.2007
		CN100375539C	12.03.2008

SAMSUNG EX. 1002 - 1576/1684

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/076338

A. CLASSIFICATION OF SUBJECT MATTER

H01L27/146（2006.01）i
H04N5/335（2011.01）i

SAMSUNG EX. 1002 - 1577/1684

国际检索报告

国际申请号
PCT/CN2011/076338

A. 主题的分类

见附加页

按照国际专利分类(IPC)或者同时按照国家分类和 IPC 两种分类

B. 检索领域

检索的最低限度文献(标明分类系统和分类号)

IPC： H01L

包含在检索领域中的除最低限度文献以外的检索文献

在国际检索时查阅的电子数据库(数据库的名称，和使用的检索词（如使用）)

CNABS，CNKI，WPI，EPODOC：感光 象素 镀膜 纳米 颗粒 pixel photo sensitive lens signal

C. 相关文件

类 型*	引用文件，必要时，指明相关段落	相关的权利要求
X	CN101345248B（博立码杰通讯（深圳）有限公司等）14.7 月 2010（14.07.2010）说明书实施例，附图 5-16	1，4-14，18-21，38-46
Y		2-3，15-17，22-37
Y	CN101740587A（博立码杰通讯（深圳）有限公司）16.6 月 2010（16.06.2010）附图 9-14	15-17
Y	CN101807590A（博立码杰通讯（深圳）有限公司）18.8 月 2010（18.08.2010）说明书第[0043]-[0057]，附图 7-17	15-17，22-25
Y	CN101834974A（博立码杰通讯（深圳）有限公司）15.9 月 2010（15.09.2010）权利要求书，说明书第[0076]-[0091]，附图 1-26	25-37

☒ 其余文件在 C 栏的续页中列出。　　☒ 见同族专利附件。

* 引用文件的具体类型：

"A" 认为不特别相关的表示了现有技术一般状态的文件

"E" 在国际申请日的当天或之后公布的在先申请或专利

"L" 可能对优先权要求构成怀疑的文件，或为确定另一篇引用文件的公布日而引用的或者因其他特殊理由而引用的文件（如具体说明的）

"O" 涉及口头公开、使用、展览或其他方式公开的文件

"P" 公布日先于国际申请日但迟于所要求的优先权日的文件

"T" 在申请日或优先权日之后公布，与申请不相抵触，但为了理解发明之理论或原理的在后文件

"X" 特别相关的文件，单独考虑该文件，认定要求保护的发明不是新颖的或不具有创造性

"Y" 特别相关的文件，当该文件与另一篇或者多篇该类文件结合并且这种结合对于本领域技术人员为显而易见时，要求保护的发明不具有创造性

"&" 同族专利的文件

国际检索实际完成的日期	国际检索报告邮寄日期
21.3 月 2012（21.03.2012）	**29.3 月 2012 (29.03.2012)**
ISA/CN 的名称和邮寄地址： 中华人民共和国国家知识产权局 中国北京市海淀区蓟门桥西土城路 6 号 100088 传真号： (86-10)62019451	受权官员 钟翊 电话号码：(86-10) **62411594**

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C(续). 相关文件

类 型	引用文件，必要时，指明相关段落	相关的权利要求
Y	WO2008131313A2（TIAN 等）30.10 月 2008（30.10.2008） 全文	2-3, 25-37
X	US2006266921A1（KANG 等）30.11 月 2006（30.11.2006） 图 7-10	1，38，40，41，45
X	JP2005526458A（微米技术有限公司）02.9 月 2005（02.09.2005） 附图 3	1，38，40，41，45
E	CN102244083A（博立多媒体控股有限公司）16.11 月 2011（16.11.2011） 全文	1-5，20-33
E	CN102263114A（博立多媒体控股有限公司）30.11 月 2011（30.11.2011） 全文	1-46

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国际检索报告
关于同族专利的信息

国际申请号
PCT/CN2011/076338

检索报告中引用的专利文件	公布日期	同族专利	公布日期
CN101345248B	14.07.2010	CN101345248A	14.01.2009
		WO2009006776A1	15.01.2009
		EP2172973A1	07.04.2010
		US2010141771A1	10.06.2010
		KR20100057599A	31.05.2010
		CA2705315A1	15.01.2009
		INMUMNP201000137E	16.07.2010
		JP2010532869A	14.10.2010
CN101740587A	16.06.2010	无	
CN101807590A	18.08.2010	无	
CN101837974A	22.09.2010	无	
CN102244083A	16.11.2011	无	
CN102263114A	30.11.2011	无	
WO2008131313A2	30.10.2008	WO2008131313A3	11.12.2008
		US2009152664A1	18.06.2009
		EP2143141A2	13.01.2010
		US2010187404A1	29.07.2010
		US2010187408A1	29.07.2010
		US7923801B2	12.04.2011
		CN102017147A	13.04.2011
		US8013412B2	06.09.2011
		US8004057B2	23.08.2011
		US2011297915A1	08.12.2011
		US2011297815A1	08.12.2011
		US2011303897A1	15.12.2011
		US2011303898A1	15.12.2011
		US2011309238A1	22.12.2011
		US2011309236A1	22.12.2012
US2006266921A1	30.11.2006	JP2006332602A	07.12.2006
		CN1870282A	29.11.2006
		KR20060122136A	30.11.2006
		KR100665177B1	09.01.2007
		US7348539B2	25.03.2008
		TW200642077A	01.12.2006
		CN100481479C	22.04.2009
		TW306308B1	11.02.2009
		JP4418443B2	17.02.2010
JP2005526458A	02.09.2005	CN100375539C	12.03.2008

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国际检索报告
关于同族专利的信息

国际申请号
PCT/CN2011/076338

检索报告中引用的专利文件	公布日期	同族专利	公布日期
		US2003211405A1	13.11.2003
		WO3098940A1	27.11.2003
		AU2003269305A1	02.12.2003
		US6783900B2	31.08.2004
		EP1506679A1	16.02.2005
		KR20050003456A	10.01.2005
		CN1669332A	14.09.2005
		EP1506679B1	27.12.2006
		KR100621086B1	14.09.2006
		DE60310706E	08.02.2007
		DE60310706T2	11.10.2007

SAMSUNG EX. 1002 - 1581/1684

国际申请号
PCT/CN2011/076338

A. 主题的分类

H01L27/146（2006.01）i
H04N5/335（2011.01）i

SAMSUNG EX. 1002 - 1582/1684

Electronic Acknowledgement Receipt

EFS ID:	34706929
Application Number:	15614256
International Application Number:	
Confirmation Number:	4345
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	136549
Filer:	Andrew W. Schultz
Filer Authorized By:	
Attorney Docket Number:	143705.06021
Receipt Date:	28-DEC-2018
Filing Date:	05-JUN-2017
Time Stamp:	14:32:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	1_CN101241923A.pdf	767032 6ea5522a3466bcbb3e8f28c4911ff5e10a3eba20	no	11

Warnings:

Information:					
2	Foreign Reference	CN101404307A.pdf	1306957 add805a95c86be0e1ffd2f103cd891dc6a95528f	no	9
Warnings:					
Information:					
3	Foreign Reference	CN101423942A.pdf	1856740 154c2dd2a60833248ea336ce86d8fe0825772b35	no	9
Warnings:					
Information:					
4	Foreign Reference	2_CN101465361A_w_Trans.pdf	8822663 1d8c53765d3a72bacdd6cd137d3c2cc10176b31a	no	26
Warnings:					
Information:					
5	Foreign Reference	CN101478013A.pdf	1705264 37e536c854785298aefc7464e7bd217028c45857	no	13
Warnings:					
Information:					
6	Foreign Reference	CN101634026A.pdf	1439252 00dd4d0fdd0b9dccd38356ad14f98095a6f0ebee	no	8
Warnings:					
Information:					
7	Foreign Reference	CN101634027A.pdf	1468680 b270e9616fd10ab8628588d67453cd77e2ecd11a	no	7
Warnings:					
Information:					
8	Foreign Reference	3_CN101740597A_US20101281 61.pdf	772339 0b5431189b97a50f178ace3c4dad26bc57894ce2	no	10
Warnings:					
Information:					

9	Foreign Reference	CN101818348A.pdf	1233164 56286366277c5c6e2bb967f57b8e200176a57283	no	9
Warnings:					
Information:					
10	Foreign Reference	4_CN101978498A_US20092000625.pdf	602808 7b6358fa9358d718ecd55ad0fcfe7c187a170ae5	no	10
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Information:					
11	Foreign Reference	5_CN102270646_w_Trans.pdf	9287155 dfb8aa37a1752ff9aa3fcfdcf81f6fa5bdb1ae16	no	29
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12	Foreign Reference	CN1507075A.pdf	1523049 1daafbc7f68593947ce212cb64b9843280826f16	no	8
Warnings:					
Information:					
13	Foreign Reference	CN1614789A.pdf	1800107 c4eac0b2f7a6998e563ae3d364b55ec68807a66b	no	11
Warnings:					
Information:					
14	Foreign Reference	6_CN201725796U_w_Trans.pdf	6090769 d9d71d37839d3b78bbaa6b8eaf8a80b67ee154cf	no	21
Warnings:					
Information:					
15	Foreign Reference	DE19838439.pdf	1680083 1bbd6553cd61e869de070de2645cd4308d79229f	no	9
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16	Foreign Reference	EP2509107A1.pdf	1361527 7ce82ba536ff3d53d0413875489e5475a614a1d7	no	39
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Information:					
17	Foreign Reference	JP2003058269A.pdf	896218 e36b8cebd7c1a09fa9f62ba72d8d78f6f2615bb1	no	8
Warnings:					
Information:					
18	Foreign Reference	JP2003104121A.pdf	793798 60c826b487a7ee6363849a26c9074760066c52fa	no	8
Warnings:					
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19	Foreign Reference	JP2003258285A.pdf	2303631 8d3d6eb46904c0fa2755f292e2e52cb050a9f4c5	no	7
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Information:					
20	Foreign Reference	JP2004047682.pdf	2135147 2403ebf337c885db2ae3d7a3e7b7b0cef17890ef	no	33
Warnings:					
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21	Foreign Reference	JP2006033493.pdf	1563749 f6676622d7dd6ff57ed1040ba601e8e3b387820b	no	29
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22	Foreign Reference	JP2006147991.pdf	1838635 7ce445e5a38336c3d72c6ce0075095baa059d5de	no	34
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23	Foreign Reference	JP2006210701.pdf	1419860 3b98c6444ba2e5d481d7c16a6d5b2056b264eda6	no	24
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24	Foreign Reference	JP2006261372.pdf	5095699 631c12ddf77530ae14abf664862f358a8bf12e52	no	63
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25	Foreign Reference	JP2007122237.pdf	2099837 34e0f000c56e6a92f3d16f4ebfc1cdc00ebc0606	no	23
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26	Foreign Reference	17_JP2007258684_US2012147241.pdf	1760436 947374f91cc40b6c1f477c4abdbee8573b0a20ff	no	37
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27	Foreign Reference	JP2008099158A.pdf	3041926 f52a8355281ca19abef1de8fbeec297396d5f739	no	34
Warnings:					
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28	Foreign Reference	JP2008167004A.pdf	1828745 fbb4052928e29dde4aeb8304808a2c5814fc79c5	no	21
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29	Foreign Reference	JP2008294698A.pdf	2162585 dac2df85c60f35408eda518fc1bc4bf7afed749b	no	26
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30	Foreign Reference	JP2009152569A.pdf	9060022 97e43310fc047ce7d04d9f7f24b0ed130ea7b43f	no	25
Warnings:					
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31	Foreign Reference	JP2009253683A.pdf	1489939 71b6fd64236c6b00e3ff50401860041 0f32ed553	no	18
Warnings:					
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32	Foreign Reference	7_JP2011003860A_US2010201834A1.pdf	488526 dc852adb9361629f1d3a5f83cb0123f523696fe3	no	10
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Information:					
33	Foreign Reference	8_JP2012054321A_US2012049306.pdf	490286 29a122c14c0806d973b124c0b607fdbe00575d66	no	10
Warnings:					
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34	Foreign Reference	9_JP2012169530A_W_Trans.pdf	24050452 8f6c80f913843acca27f9c236ae0b2a8982e6ef5	no	94
Warnings:					
Information:					
35	Foreign Reference	10_JP2012191005A_US2012228473.pdf	473261 6fa90bd1fa2c31252461677281c3e3e0d2467f8f	no	10
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Information:					
36	Foreign Reference	JP2012212349A.pdf	599034 fc176cccb48443b9aa33a47259bce2f2b114806b	no	7
Warnings:					
Information:					

37	Foreign Reference	JPH07235658.pdf	1194297 5cd86a0973bcb28f8d14310778669d37079e8b32	no	20
Warnings:					
Information:					
38	Foreign Reference	JPH0774240.pdf	326221 52025081741d08d130ad94c9936f4ca287b9d33e	no	4
Warnings:					
Information:					
39	Foreign Reference	11_KR20060020400A_w_Trans.pdf	4118885 0a5085d231a16921cc0b6cdf6840cd4742a0036d	no	18
Warnings:					
Information:					
40	Foreign Reference	12_KR20080014301A_w_Trans.pdf	4757084 739ad4d9907277b71cd834b34113fe916318fce4	no	17
Warnings:					
Information:					
41	Foreign Reference	13_KR20080097709A_w_Trans.pdf	5530638 b7c1a34490431693724c8e29bd20155dbc349d8d	no	20
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42	Foreign Reference	KR2009077274.pdf	1463669 60ca30c6321a2ce0f15a3d172394ee35f9732bd5	no	20
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43	Foreign Reference	KR20100026463.pdf	1033002 5cf0ceb4437297c8a977e9cf4f7559c3f2b701d7	no	13
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44	Foreign Reference	14_KR20110079323A_w_Trans.pdf	5471824 a26ce5dd0b17470b216c5f4af4adf1557884d4f9	no	20
Warnings:					
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45	Foreign Reference	15_KR20170070266A_US20140054662.pdf	496397 bafff2840a467f539211d3aa07e5ef870b47b045	no	10
Warnings:					
Information:					
46	Foreign Reference	TW200627675.pdf	2216562 208dd9813e9baed8124c8d9cce5f719b74867157	no	30
Warnings:					
Information:					
47	Foreign Reference	TW200818529.pdf	2198415 ff6438f89efacc49cc528aa6d617efb4933ed873	no	27
Warnings:					
Information:					
48	Foreign Reference	WO2012027290A1.pdf	6953990 ef0a7ae88bf75332ae0ceb06cc58367549e1afb1	no	60
Warnings:					
Information:					
49	Foreign Reference	16_WO2012117931A1_US2014054662.pdf	461332 5d8cf73bd0cfee50d2e86e1c8c2c2375e3ea33aa	no	10
Warnings:					
Information:					
50	Foreign Reference	WO2012174752A1.pdf	2917593 b5a400d6ee9594d956b1729384d5bc03eddf04cb	no	65
Warnings:					
Information:					

51	Non Patent Literature	10l_Agranov_et_al.pdf	1886824 b5aaefe4565a6d578a20e7261c73e8206787a4ac	no	4
Warnings:					
Information:					
52	Non Patent Literature	1_Byung_et_al.pdf	515268 8ca788ca683394c2b2c7b94f9ec65dc299b7add3	no	5
Warnings:					
Information:					
53	Non Patent Literature	Campbell_2001.pdf	1578476 594485326236798ed7002e1d055457711851a68d	no	5
Warnings:					
Information:					
54	Non Patent Literature	CareyPG_1989.pdf	1535156 47a5cb16160430c66c5062052f010c4741441583	no	8
Warnings:					
Information:					
55	Non Patent Literature	11_Fontaine.pdf	1951727 d3e22a46c3f8fc77136c0248d0bf1112df9b381f	no	4
Warnings:					
Information:					
56	Non Patent Literature	3_Fontaine_2017.pdf	5524486 a3dee3fd5cce8b4c2fc5e1a9d7bd9d9eb20b53ab	no	13
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57	Non Patent Literature	Gibbons_1972.pdf	14804775 5e1c22a1c76a9da7b1e0ba78313bc891d2854de6	no	45
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58	Non Patent Literature	17_electroiq_com_insights_from_leading_edge_2016.pdf	1013528 796d1c9fcc425e935a0efe08fd875d3fbb6e7cdd	no	6
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59	Non Patent Literature	18_joseph_tang_blogspot_com_2017.pdf	2104246 f34b920354210b35e6344887014418cd3fb4e172	no	18
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60	Non Patent Literature	9_yahoo_co_jpmiyabiman_now25628945_html.pdf	3637415 c162a6605d4d83291a08f7017b27d54ab6fab33a	no	14
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		Total Files Size (in bytes):	179001185		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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				Group Art Unit:	2895
(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
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(a) U. S. PATENT DOCUMENTS						
Examiner's Initials	**Cite No.**	**U.S. Patent Document** Number Kind Code (if known)	**Name of Patentee or Applicant of Cited Document**	**Date of Publication of Cited Document MM-DD-YYYY**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	
	A1	3487223	St. John	12/30/1969		
	A2	3922571	Smith	11/25/1975		
	A3	3973994	Redfield	8/10/1976		
	A4	3994012	Warner, Jr.	11/23/1976		
	A5	4017887	Davies et al.	4/12/1977		
	A6	4149174	Shannon	4/10/1979		
	A7	4176365	Kroger	11/27/1979		
	A8	4201450	Trapani	5/6/1980		
	A9	4242149	King et al.	12/30/1980		
	A10	4253882	Dalal	3/3/1981		
	A11	4277793	Webb	7/7/1981		
	A12	4322571	Stanbery	3/30/1982		
	A13	4419533	Czubatyj et al.	12/6/1983		
	A14	4452826	Shields et al.	6/5/1984		
	A15	4493942	Sheng et al.	1/15/1985		
	A16	4514582	Tiedje et al.	4/30/1985		
	A17	4536608	Sheng et al.	8/20/1985		
	A18	4546945	Nessfield	10/15/1985		
	A19	4568960	Petroff et al.	2/4/1986		
	A20	4593303	Dyck et al.	6/3/1986		
	A21	4593313	Nagasaki	6/3/1986		
	A22	4617593	Dudley	10/14/1986		
	A23	4630082	Sakai	12/16/1986		
	A24	4648936	Ashby et al.	3/10/1987		
	A25	4663188	Kane	5/5/1987		
	A26	4672206	Suzuki	6/9/1987		
	A27	4673770	Mandelkorn	6/16/1987		
	A28	4679068	Lillquist et al.	7/7/1987		
	A29	4751571	Lillquist	6/14/1988		
	A30	4775425	Guha et al.	10/4/1988		
	A31	4777490	Sharma et al.	10/11/1988		
	A32	4829013	Yamazaki	5/9/1989		
	A33	4883962	Elliot	11/28/1989		
	A34	4886958	Merryman	12/12/1989		
	A35	4887255	Handa et al.	12/12/1989		

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	A36	4894526	Bethea et al.	1/16/1990		
	A37	4910568	Taki, et al.	3/20/1990		
	A38	4910588	Kinoshita, et al.	3/20/1990		
	A39	4964134	Westbrook et al.	10/16/1990		
	A40	4965784	Land et al.	10/23/1990		
	A41	4968372	Maass	11/6/1990		
	A42	4999308	Nishiura et al.	3/12/1991		
	A43	5021100	Ishihara et al.	6/4/1991		
	A44	5021854	Huth	6/4/1991		
	A45	5080725	Green et al.	1/14/1992		
	A46	5081049	Green et al.	1/14/1992		
	A47	5101260	Nath	3/31/1992		
	A48	5114876	Weiner	5/19/1992		
	A49	5127964	Hamakawa et la.	7/7/1992		
	A50	5164324	Russell et al.	11/17/1992		
	A51	5208822	Haus et al	5/4/1993		
	A52	5223043	Olson et al.	6/29/1993		
	A53	5234790	Lang, et al.	8/10/1993		
	A54	5244817	Hawkins et al.	9/14/1993		
	A55	5296045	Banerjee et al.	3/22/1994		
	A56	5309275	Nishimura et al.	5/3/1994		
	A57	5322988	Russell et al.	6/21/1994		
	A58	5346850	Kaschmitter et al.	9/13/1994		
	A59	5351446	Langsdorf	10/4/1994		
	A60	5373182	Norton	12/13/1994		
	A61	5381431	Zayhowski	1/10/1995		
	A62	5383217	Uemura	1/17/1995		
	A63	5390201	Tomono et al.	2/14/1995		
	A64	5410168	Hisa	4/25/1995		
	A65	5413100	Barthelemy et al.	5/9/1995		
	A66	5449626	Hezel	9/12/1995		
	A67	5454347	Shibata et al.	10/3/1995		
	A68	5502329	Pezzani	3/26/1996		
	A69	5523570	Hairston	6/4/1996		
	A70	5559361	Pezzani	9/24/1996		
	A71	5569615	Yamazaki et al.	10/29/1996		
	A72	5578858	Mueller et al.	11/26/1996		
	A73	5580615	Itoh et al.	12/3/1996		
	A74	5583704	Fujii	12/10/1996		
	A75	5589008	Kepper	12/31/1996		
	A76	5589704	Levine	12/31/1996		
	A77	5597621	Hummel et al.	1/18/1997		
	A78	5600130	VanZeghbroeck	2/4/1997		
	A79	5626687	Campbell	5/6/1997		
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	A80	5627081	Tsuo et al.	5/6/1997		
	A81	5635089	Singh et al.	6/3/1997		
	A82	5640013	Ishikawa, et al.	6/17/1997		
	A83	5641362	Meier	6/24/1997		
	A84	5641969	Cooke et al.	6/24/1997		
	A85	5705413	Harkin et al.	1/6/1998		
	A86	5705828	Noguchi et al.	1/6/1998		
	A87	5708486	Miyawaki et al.	1/13/1998		
	A88	5710442	Watanabe et al.	1/20/1998		
	A89	5714404	Mititsky et al.	2/3/1998		
	A90	5727096	Ghirardi et al	3/10/1998		
	A91	5731213	Ono	3/24/1998		
	A92	5751005	Wyles et al.	5/12/1998		
	A93	5758644	Diab et el.	6/2/1998		
	A94	5766127	Pologe et al.	6/16/1998		
	A95	5766964	Rohatgi et al.	6/16/1998		
	A96	5773820	Osajda, et al.	6/30/1998		
	A97	5779631	Chance	7/14/1998		
	A98	5781392	Clark	7/14/1998		
	A99	5792280	Ruby et al	8/11/1998		
	A100	5802091	Chakrabarti et al	8/1/1998		
	A101	5808350	Jack et al	9/15/1998		
	A102	5859446	Nagasu et al.	1/12/1999		
	A103	5861639	Bernier	1/19/1999		
	A104	5923071	Saito	7/13/1999		
	A105	5935320	Graf et al.	8/10/1999		
	A106	5942789	Morikawa	8/24/1999		
	A107	5943584	Shim et al	8/24/1999		
	A108	5963790	Matsuno et al	10/5/1999		
	A109	5977603	Ishikawa	11/2/1999		
	A110	6071796	Voutsas	6/6/2000		
	A111	6072117	Matsuyama et al.	6/6/2000		
	A112	6080988	Ishizuya et al.	6/27/2000		
	A113	6082858	Grace et al.	7/4/2000		
	A114	6097031	Cole	8/1/2000		
	A115	6106689	Matsuyama	8/22/2000		
	A116	6107618	Fossum et al.	8/22/2000		
	A117	6111300	Cao et al.	8/29/2000		
	A118	6131511	Wachi et al	10/17/2000		
	A119	6131512	Verlinden et al	10/17/2000		
	A120	6147297	Wettling et al.	11/14/2000		
	A121	6160833	Floyd et al.	12/12/2000		
	A122	6168965	Malinovich, et al.	1/2/2001		
	A123	6194722	Fiorini et al.	2/27/2001		
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	A124	6204506	Akahori et al.	3/20/2001		
	A125	6229192	Gu	5/8/2001		
	A126	6252256	Ugge et al.	6/26/2001		
	A127	6290713	Russell	9/18/2001		
	A128	6291302	Yu	9/18/2001		
	A129	6313901	Cacharelis	11/6/2001		
	A130	6320296	Fujii et al.	11/20/2001		
	A131	6327022	Nishi	12/4/2001		
	A132	6331445	Janz et al	12/18/2001		
	A133	6331885	Nishi	12/18/2001		
	A134	6340281	Haraguchi	1/22/2002		
	A135	6372591	Mineji et al.	4/16/2002		
	A136	6372611	Horikawa	4/16/2002		
	A137	6379979	Connolly	4/30/2002		
	A138	6420706	Lurie, et al.	7/16/2002		
	A139	6429036	Nixon, et al.	8/6/2002		
	A140	6429037	Wenham et al.	8/6/2002		
	A141	6465860	Shigenaka, et al.	10/15/2002		
	A142	6475839	Zhang, et al.	11/5/2002		
	A143	6479093	Lauffer et al	11/12/2002		
	A144	6483116	Kozlowski et al.	11/19/2002		
	A145	6483929	Marakami et al.	11/19/2002		
	A146	6486522	Bishay et al.	11/26/2002		
	A147	6493567	Krivitski et al.	12/10/2002		
	A148	6498336	Tian et al.	12/24/2002		
	A149	6500690	Yamagishi et al.	12/31/2002		
	A150	6504178	Carlson et al.	1/7/2003		
	A151	6580053	Voutsas	6/17/2003		
	A152	6583936	Kaminsky et al.	6/24/2003		
	A153	6597025	Lauter et al	7/22/2003		
	A154	6607927	Ramappa et al.	8/19/2003		
	A155	6624049	Yamazaki	9/23/2003		
	A156	6639253	Duane et al.	10/28/2003		
	A157	6667528	Cohen et al.	12/23/2003		
	A158	6677655	Fitzgerald	1/13/2004		
	A159	6677656	Francois	1/13/2004		
	A160	6683326	Iguchi, et al.	1/27/2004		
	A161	6689209	Falster et el.	2/10/2004		
	A162	6690968	Mejia	2/10/2004		
	A163	6753585	Kindt	6/22/2004		
	A164	6759262	Theil et al.	7/6/2004		
	A165	6790701	Shigenaka, et al.	9/14/2004		
	A166	6800541	Okumura	10/5/2004		
	A167	6801799	Mendelson	10/5/2004		
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	A168	6803555	Parrish et al.	10/12/2004		
	A169	6815685	Wany	11/9/2004		
	A170	6818535	Lu et al.	11/16/2004		
	A171	6822313	Matsushita	11/23/2004		
	A172	6825057	Heyers, et al.	11/30/2004		
	A173	6864156	Conn	3/8/2005		
	A174	6864190	Han et al.	3/8/2005		
	A175	6867806	Lee et al.	3/15/2005		
	A176	6900839	Kozlowski et al.	5/31/2005		
	A177	6907135	Gifford	6/14/2005		
	A178	6911375	Guarini et al.	6/28/2005		
	A179	6919587	Ballon et al.	7/19/2005		
	A180	6923625	Sparks	8/2/2005		
	A181	6927432	Holm, et al.	8/9/2005		
	A182	6984816	Holm, et al.	1/10/2006		
	A183	7008854	Forbes	3/7/2006		
	A184	7041525	Clevenger et al.	5/9/2006		
	A185	7057256	Carey, III et al.	6/6/2006		
	A186	7075079	Wood	7/11/2006		
	A187	7091411	Falk et al.	8/15/2006		
	A188	7109517	Zaidi	9/19/2006		
	A189	7126212	Enquist et al.	10/24/2006		
	A190	7132724	Merrill	11/7/2006		
	A191	7202102	Yao	4/10/2007		
	A192	7211501	Liu et al	5/1/2007		
	A193	7235812	Chu, et al.	6/26/2007		
	A194	7247527	Shimomura et al.	7/24/2007		
	A195	7247812	Tsao	7/24/2007		
	A196	7256102	Nakata, et al.	8/14/2007		
	A197	7271445	Forbes	9/18/2007		
	A198	7271835	Iizuka et al.	9/18/2007		
	A199	7285482	Ochi	10/23/2007		
	A200	7314832	Kountz et al.	1/1/2008		
	A201	7315014	Lee et al	1/1/2008		
	A202	7354792	Carey, III et al.	4/8/2008		
	A203	7358498	Geng et al.	4/15/2008		
	A204	7375378	Manivannan et al.	5/20/2008		
	A205	7390689	Mazur et al.	6/24/2008		
	A206	7432148	Li et al.	10/7/2008		
	A207	7442629	Mazur et al.	10/28/2008		
	A208	7446359	Lee, et al.	11/4/2008		
	A209	7446807	Hong	11/7/2008		
	A210	7456452	Wells et al.	11/25/2008		
	A211	7482532	Yi et al.	1/27/2009		
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	A212	7498650	Lauxtermann	3/3/2009		
	A213	7504325	Koezuka et al.	3/17/2009		
	A214	7504702	Mazur et al.	3/17/2009		
	A215	7511750	Murakami	3/31/2009		
	A216	7521737	Augusto	4/21/2009		
	A217	7528463	Forbes	5/5/2009		
	A218	7542085	Altice, Jr. et al.	6/2/2009		
	A219	7547616	Fogel et al.	6/16/2009		
	A220	7551059	Farrier	6/23/2009		
	A221	7560750	Niira et al.	7/14/2009		
	A222	7564631	Li, et al.	7/21/2009		
	A223	7582515	Choi et al.	9/1/2009		
	A224	7592593	Kauffman, et al.	9/22/2009		
	A225	7595213	Kwon et al.	9/29/2009		
	A226	7605397	Kindem et al.	10/20/2009		
	A227	7615808	Pain, et al.	11/10/2009		
	A228	7618839	Rhodes	11/17/2009		
	A229	7619269	Ohkawa	11/17/2009		
	A230	7629582	Hoffman, et al.	12/8/2009		
	A231	7648851	Fu, et al.	1/19/2010		
	A232	7649156	Lee	1/19/2010		
	A233	7705879	Kerr et al.	4/27/2010		
	A234	7728274	Pilla et al	6/1/2010		
	A235	7731665	Lee et al	6/8/2010		
	A236	7741666	Nozaki, et al.	6/22/2010		
	A237	7745901	McCaffrey et al	6/29/2010		
	A238	7763913	Fan et al	7/27/2010		
	A239	7772028	Adkisson et al	8/10/2010		
	A240	7781856	Mazur et al.	8/24/2010		
	A241	7800192	Venezia, et al.	9/21/2010		
	A242	7800684	Tatani	9/21/2010		
	A243	7816220	Mazur et al.	10/19/2010		
	A244	7847253	Carey et al.	12/7/2010		
	A245	7847326	Park, et al.	12/7/2010		
	A246	7855406	Yamaguchi et al	12/21/2010		
	A247	7875498	Elbanhawy, et al.	1/25/2011		
	A248	7880168	Lenchenkov	2/1/2011		
	A249	7884439	Mazur et al.	2/8/2011		
	A250	7884446	Mazur et al.	2/8/2011		
	A251	7897942	Bereket	3/1/2011		
	A252	7910964	Kawahito et al.	3/22/2011		
	A253	7923801	Tian et al.	4/12/2011		
	A254	7968834	Veeder	6/28/2011		
	A255	8008205	Fukushima et al.	8/30/2011		
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	A256	8013411	Cole	9/6/2011		
	A257	8030726	Sumi	10/4/2011		
	A258	8035343	Seman Jr.	10/11/2011		
	A259	8058615	McCaffrey	11/15/2011		
	A260	8076746	McCarten et al.	12/13/2011		
	A261	8080467	Carey et al.	12/20/2011		
	A262	8088219	Knerer et al.	1/3/2012		
	A263	8093559	Rajavel	1/10/2012		
	A264	8164126	Moon, et al.	4/24/2012		
	A265	8207051	Sickler et al.	6/26/2012		
	A266	8247259	Grolier et al.	8/21/2012		
	A267	8259293	Andreou et al.	9/4/2012		
	A268	8268403	Akiyama et al	4/30/2007		
	A269	8288702	Veeder	10/16/2012		
	A270	8355545	Corcoran et al.	1/15/2013		
	A271	8445950	Iida et al	5/21/2013		
	A272	8445985	Hiyama et al	5/21/2013		
	A273	8456546	Oike	6/4/2013		
	A274	8470619	Bour	6/1/2013		
	A275	8476681	Haddad et al.	7/2/2013		
	A276	8530264	De Munck et al	9/10/2013		
	A277	8564087	Yamamura et al.	10/22/2013		
	A278	8603902	Mazur et al.	12/10/2013		
	A279	8604405	Liu et al	12/10/2013		
	A280	8629485	Yamamura et al.	1/14/2014		
	A281	8649568	Sato	2/11/2014		
	A282	8680591	Haddad et al.	3/25/2014		
	A283	8729678	Shim et al	5/20/2014		
	A284	8742528	Yamamura et al.	6/3/2014		
	A285	8884226	Miyazaki, et al.	11/11/2014		
	A286	8906670	Gray	12/1/2014		
	A287	8916945	Sakamoto et al	12/23/2014		
	A288	8928784	Watanabe et al	1/6/2015		
	A289	8994135	Yamamura et al.	6/31/2015		
	A290	9064762	Yamaguchi	6/23/2015		
	A291	9184204	Hu	11/10/2015		
	A292	9190551	Yamamura et al.	11/17/2015		
	A293	9369641	Hu	6/14/2016		
	A294	9419159	Sakamoto et al.	8/16/2016		
	A295	9478572	Miyanami	10/25/2016		
	A296	9659984	Ohkubo et al	5/23/2017		
	A297	20010017344	Aebi	8/30/2001		
	A298	20010022768	Takahashi	9/20/2001		
	A299	20010044175	Barret et al.	11/22/2001		
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	A300	20010044266	Katsuoka	11/22/2001		
	A301	20020020893	Lhorte	2/21/2002		
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	A303	20020056845	Iguchi et al.	5/16/2002		
	A304	20020060322	Tanabe et al.	5/23/2002		
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	A307	20020148964	Dausch et al.	10/17/2002		
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	A387	20070178672	Tanaka, et al.	8/2/2007		
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	A474	20090242933	Hu, et al.	10/1/2009		
	A475	20090256156	Hsieh	10/15/2009		
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	A493	20100040981	Kiesel et al.	2/18/2010		
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	A496	20100052088	Carey	3/4/2010		
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	A579	20120313205	Haddad et al.	12/13/2012		
	A580	20120326008	Mckee et al.	12/27/2012		
	A581	20130001553	Vineis et al.	1/3/2013		
	A582	20130020468	Mitsuhashi et al	1/24/2013		
	A583	20130026531	Seo et al.	1/31/2013		
	A584	20130082343	Fudaba, et al.	4/4/2013		
	A585	20130135439	Kakuko et al.	5/30/2013		
	A586	20130168792	Haddad et al.	7/4/2013		
	A587	20130168803	Haddad et al.	7/4/2013		
	A588	20130200251	Velichko	8/8/2013		
	A589	20130207212	Mao et al	8/15/2013		
	A590	20130207214	Haddad et al.	8/15/2013		
	A591	20130285130	Ting	10/31/2013		
	A592	20140054662	Yanagita et al	2/27/2014		
	A593	20140198240	Rhoads	7/17/2014		
	A594	20140247378	Sharma et al.	9/4/2014		
	A595	20140374868	LEE et al	12/25/2014		
	A596	20170244920	Ohkubo et al	8/24/2017		
	A597	RE43169	Parker	2/7/2012		

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Cite No.	Foreign Patent Document Number Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear			T
	B1	AU 3666484	Wenham et al.	6/27/1985				
	B2	CN 101241923	TSMC	8/13/2008				

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				Group Art Unit:	2895
(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
Sheet	15	of	26	Attorney Docket No.:	143705.06021(S)

	B3	CN 101404307	Univ. Zhongshan	4/8/2009				
	B4	CN 101423942	Dong Jiang	5/6/2009				
	B5	CN 101465361	TSMC	6/24/2009				
	B6	CN 101478013	Suntech Power Co Ltd	7/8/2009				
	B7	CN 101634026	Beijing Solar Energy Res Inst	1/27/2010				
	B8	CN 101634027	Beijing Solar Energy Res Inst	1/27/2010				
	B9	CN 101740597	Sony Corp.	6/16/2010				
	B10	CN 101818348	Univ Shejiang	9/1/2010				
	B11	CN 101978498	OMNIVISION TECH INC	2/16/2011				
	B12	CN 102270646	NA	12/7/2011				
	B13	CN 1507075	Beijing Linuosangpu Photovolta	6/23/2004				
	B14	CN 1614789	Shangde Solar Electric Power	5/11/2005				
	B15	CN 201725796	GALAXYCORE INC	1/26/2011				
	B16	DE 19838439	Fraunhofer-Gesellschaft Zur Faurderung Der Angewandten	4/27/2000				
	B17	EP 0473439	Cooper Industries	3/4/1992				
	B18	EP 0566156	Terumo Kabushiki Kaisha	10/20/1993				
	B19	EP 1630871	Matsushita Electric Industrial Co. Ltd.	1/3/2006				
	B20	EP 1873840	Neil et al.	1/2/2008				
	B21	EP 2073270	Hirota, et al.	5/16/2012				
	B22	EP 2509107	Boly Media Comm.	10/10/2012				
	B23	FR 2827707	FR De Detecteurs Infrarouges S	1/24/2003				
	B24	GB 2030766	Plessey Co. Ltd.	4/10/1980				
	B25	JP 11077348	Cannon KK	3/23/1999				
	B26	JP 11097724	Citizen Watch Co. Ltd.	4/9/1999				
	B27	JP 2000164914	Electrowatt Technol Innov AG	6/16/2000				
	B28	JP 2001007381	Japan Broadcasting Corp.	1/12/2001				
	B29	JP 2001024936	Matsushita Electric Industrial Co. Ltd.	1/26/2001				
	B30	JP 2001189478	Sanyo Electric Co.	7/10/2001				
	B31	JP 2001257927	Technosonic KK	9/21/2001				
	B32	JP 2001339057	Fuji Xerox Co. Ltd.	12/7/2001				
	B33	JP 2002043594	Sharp KK	2/8/2002				
	B34	JP 2002134640	United Test CT Inc.	5/10/2002				
	B35	JP 2002513176	Grace et al.	5/8/2002				

Examiner Signature		Date Considered	

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	B36	JP 2003058269	Mitsubishi	2/28/2003				
	B37	JP 2003104121	Matsushita Electric Industrial Co. Ltd.	4/9/2003				
	B38	JP 2003163360	Seiko Epson Corp.	6/6/2003				
	B39	JP 2003242125	Canon KK	8/29/2003				
	B40	JP 2003258285	Sharp KK	9/12/2003				
	B41	JP 2003308130	Matsushita Electric Industrial Co. Ltd.	10/31/2003				
	B42	JP 2004047682	Toshiba Corp.	2/12/2004				
	B43	JP 2004273886	Hatachi Cable	9/3/2004				
	B44	JP 2004273887	Hatachi Cable Ltd.	9/30/2004				
	B45	JP 2005339425	Sanyo Electric Co.	12/8/2005				
	B46	JP 2006033493	Matsushita Electric Industrial Co. Ltd.	2/2/2006				
	B47	JP 2006147991	Canon Inc.	6/8/2006				
	B48	JP 2006173381	Toyota Motor Corp.	6/29/2006				
	B49	JP 2006210701	Sayno Electric Co.	8/10/2006				
	B50	JP 2006255430	Fujitsu Ltd.	9/28/2006				
	B51	JP 2006261372	Sony Corp.	9/28/2006				
	B52	JP 2007122237	Mitsubishi Electric Corp.	5/17/2007				
	B53	JP 2007165909	Icemos Technology Corp.	6/28/2007				
	B54	JP 2007180642	SWCC Showa Device Tech Co. Ltd.	7/12/2007				
	B55	JP 2007180643	Sony Corp.	7/12/2007				
	B56	JP 2007258684	Sony Corp.	10/4/2007				
	B57	JP 2007305675	Sony, Corp.	11/22/2007				
	B58	JP 2008099158	Sony Corp.	4/24/2008				
	B59	JP 2008167004	Sony Corp.	7/17/2008				
	B60	JP 2008187003	Fujitsu Ltd.	8/14/2008				
	B61	JP 2008283219	Toshiba Corp.	11/20/2008				
	B62	JP 2008294698	Sony Corp.	12/4/2008				
	B63	JP 2009021479	Omron Tteisi Electronics Co.	1/29/2009				
	B64	JP 2009152569	Semiconductor Energy Lab	7/9/2009				
	B65	JP 2009253683	Konica Minolta Holdings Inc.	10/29/2009				
	B66	JP 2010278472	Sony, Corp.	12/9/2010				
	B67	JP 2011003860	Sony Corp.	1/6/2011				
	B68	JP 2011091128	Cannon KK	5/6/2011				
	B69	JP 2012054321	Sony Corp.	3/15/2012				
	B70	JP 2012169530	Sony Corp.	9/6/2012				
	B71	JP 2012191005	Sony Corp.	10/4/2012				
	B72	JP 2012212349	Hitachi Solutions Ltd.	11/1/2012				

Examiner Signature		Date Considered	

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Sheet	17	of	26	Attorney Docket No.:	143705.06021(S)

	B73	JP 9148594	Sanyo Electric Co.	6/6/1997				
	B74	JP H02152226	Fujitsu Ltd.	6/12/1990				
	B75	JP H02237026	Sony, Corp.	9/19/1990				
	B76	JP H03183037	Nec Corp.	8/9/1991				
	B77	JP H04318970	Mitsubishi Electric Corp.	11/10/1992				
	B78	JP H06104414	Toshiba Corp.	4/15/1994				
	B79	JP H06244444	Hatachi Ltd. (Hammamatsu)	9/2/1994				
	B80	JP H06267868	Fuji Electric Co LTD	9/22/1994				
	B81	JP H06275641	Semiconductor Energy Lab Co. LTD.	9/30/1994				
	B82	JP H07183484	Centre Nat ETD Telecomm	7/21/1995				
	B83	JP H07235658	Sony Corp.	5/9/1995				
	B84	JP H0774240	Nec Corp.	3/17/1995				
	B85	JP H09298308	Sharp KK	11/18/1997				
	B86	JP S57173966	Fuji Photo Film Co. Ltd.	10/26/1982				
	B87	JP S5771188	Mitsubishi Electric Corp.	5/1/1982				
	B88	JP S63116421	Mitsubishi Electric Corp.	5/20/1988				
	B89	KR 100825808	Samsung Electronics CO. Ltd.	4/29/2008				
	B90	KR 20010061058	Hynix Semiconductor Inc.	4/7/2001				
	B91	KR 2005039273	Jin- Sin Lee	4/29/2005				
	B92	KR 20060020400	MAGNACHIP SEMICONDUCTOR LTD	3/6/2006				
	B93	KR 20060052278	Sony Corp.	5/16/2016				
	B94	KR 20080014301	Samsung Elec. Co. Ltd.	2/14/2008				
	B95	KR 20080097709	Dongbu Elec. Co. Ltd.	11/6/2008				
	B96	KR 20090077274	LG Electronics Inc.	7/15/2009				
	B97	KR 20100026463	LG Electronics Inc.	3/10/2010				
	B98	KR 20100118864	Hyosung Corp	11/8/2010				
	B99	KR 20110079323	DONGBU HITEK CO LTD	7/7/2011				
	B100	KR 20170070266	SONY CORP	6/21/2017				
	B101	TW 200627675	Lumileds Lighting U.S. LLC	8/1/2006				
	B102	TW 200818529	Newsouth Innovations PTY. LTD	4/16/2008				
	B103	WO 2003059390	Dong Wha Pharm Ind Co. Ltd	7/24/2003				
	B104	WO 2000031679	Iriscan Inc.	6/2/2000				
	B105	WO 2002041363	Solarflex Technologies Inc.	5/23/2002				

Examiner Signature		Date Considered	

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Sheet	18	of	26	Attorney Docket No.:	143705.06021(S)

	B106	WO 2006/086014	President and Fellows of Harvard College	8/17/2006				
	B107	WO 2008091242	UVA Patent Foundation	7/31/2008				
	B108	WO 2008099524	Mitsubishi Heavy Industries Ltd.	8/21/2008				
	B109	WO 2008145097	Fraunhofer-Gesellschaft Zur Faurderung Der Angewandten	12/8/2008				
	B110	WO 2009016846	Panasonic Corp.	2/5/2009				
	B111	WO 2009100023	President and Fellows of Harvard College	8/13/2009				
	B112	WO 2009147085	Thiel et al.	12/10/2009				
	B113	WO 2010033127	Sionyx, Inc.	3/25/2010				
	B114	WO 2011003871	International Business Machines Corporation	1/13/2011				
	B115	WO 2011035188	Sionyx, Inc.	3/24/2011				
	B116	WO 2011119618	Sionyx, Inc.	3/22/2011				
	B117	WO 2012027290	Red.Com, Inc.	3/1/2012				
	B118	WO 2012117931	SONY CORPORATION	9/7/2012				
	B119	WO 2012174752	Boly Media Comm.	12/27/2012				
	B120	WO 2014110484	Digimarc Corp.	7/17/2014				
	B121	WO 91/14284	Theden, Ulrich	9/19/1991				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
Examiner's Initials	**Cite No.**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or county where published**	**T**
	C1	A. Arndt, J.F. Allison, J.G. Haynos, and A. Meulenberg, Jr., "Optical Properties of the COMSAT Non-reflective Cell," 11th IEEE Photovoltaic Spec. Conf., p. 40, 1975	
	C2	Agranov, et al., Pixel continues to shrink….Small Pixels for Novel CMOS Image Sensors, 4 pages.	
	C3	Asom et al., Interstitial Defect Reactions in Silicon; Appl. Phys. Lett.; 07/27/1987; pp. 256-258; vol. 51(4); American Institute of Physics.	
	C4	BERGER, Michael; Moth Eyes Inspire Self-Cleaning Antireflection Nanotechnology Coatings; 2008; 3 pages; Nanowerk LLC	
	C5	Berger, O., Inns, D. and Aberle, A.E. "Commercial White Paint as Back Surface Reflector for Thin-Film Solar Cells", Solar Energy Materials & Solar Cells, vol. 91, pp. 1215-1221,2007.	
	C6	Bernhard, C.G., "Structural and Functional Adaptation in a Visual System" Endevor Vol. 26, pp. 79-84, May 1967	
	C7	Betta et al.; Si-PIN X-Ray Detector Technology; Nuclear Instruments and Methods in Physics Research; 1997; pp. 344-348; vol. A, No. 395; Elsevier Science B.V. cited by applicant.	
	C8	BODEN, S.A. et al.; Nanoimprinting for Antireflective Moth-Eye Surfaces; 4 pages; 2008	
	C9	Bogue: "From bolometers to beetles: the development of the thermal imaging sensors;" sensor Review; 2007; pp. 278-281; Emerald Group Publishing Limited (ISSN 0260-2288).	

Examiner Signature		Date Considered	

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Sheet	19	of	26	Attorney Docket No.:	143705.06021(S)

	C10	Borghesi et al.; "Oxygen Precipitation in Silicon," J. Appl. Phys., v. 77(9), pp. 4169-4244 (May 1, 1995).	
	C11	Born, M. and E.Wolf, "Princip les of Optics, 7th Ed.", Cambridge University Press, 1999, pp. 246-255.	
	C12	Brieger,S., O.Dubbers, S.Fricker, A.Manzke, C.Pfahler, A.Plettl, and P.Zlemann, "An Approach for the Fabrication of Hexagonally Ordered Arrays of Cylindrical Nanoholes in Crystalline and Amorphous Silicon Based on the Self-Organization of Polymer Micelles", Nanotechnology, vol. 17, pp. 4991-4994, 2006, doi:10.1088/0957-4884/17/19/036.	
	C13	Buttgen, B.; "Demodulation Pixel Based on Static Drift Fields"; IEEE Transactions on Electron Devices, vol. 53, No. 11, Nov. 2006.	
	C14	Byung Jun Park et al, Jpn. J. Appl. Phys. 46 2454, 2007, 5 pages.	
	C15	Campbell, Stephen A., "The Science and Engineering of Microeletronic Fabrication, 2nd Ed.", Oxford University Press, 2001, pp. 406-411.	
	C16	Carey et al., "Femtosecond-Laser-Assisted Microstructuring of Silicon Surfaces", Optics and Photonics News, 2003. 14, 32-36.	
	C17	Carey, et al. "Femtosecond Laser-Assisted Microstructuring of Silicon for Novel Detector, Sensing and Display Technologies", LEOS 2003, 481-482, Tuscon, AR.	
	C18	Carey, et al. "Femtosecond Laser-Assisted Microstructuring of Silicon for Novel Detector, Sensing and Display Technologies", LEOS; 2002, 97-98, Glasgos, Scotland, 2002.	
	C19	Carey, et al., "Fabrication of Micrometer-Sized Conical Field Emitters Using Femtosecond Laser-Assisted Etching of Silicon," Proc. IVMC 2001, 75-76, UC Davis, Davis, CA.	
	C20	Carey, et al., "Field Emission from Silicon. Microstructures Formed by Femtosecond Laser Assisted Etching," Proc. CLEO 2001 (Baltimore, MD 2001) 555-557.	
	C21	Carey, et al., "High Sensitivity Silicon-Based VIS/NIR Photodetectors", Optical Society of America (2003) 1-2.	
	C22	CAREY, III; “Femtosecond-laser Microstructuring of Silicon for Novel Optoelectronic Devices”; Harvard University, July 2004; (Thesis)	
	C23	Carey, P.G. et al., "In-situ Doping of Silicon Using Gas Immersion Laser Doping (GILD) Process," Appl. Surf. Sci. 43, 325-332 (1989)	
	C24	Chang, S.W., V.P.Chuang, S.T.Boles, and C.V.Thompson, "Metal-Catalyzed Etching of Vertically Aligned Polysilicon and Amorphous Silicon Nanowire Arrays by Etching Direction Confinement", Advanced Functional Materials, vol. 20, No. 24, pp. 4364-4370, 2010	
	C25	CHEN, Q. et al.; Broadband moth-eye antireflection coatings fabricated by low-cost nanoimprinting; Applied Physics Letters 94; pgs. 263118-1 - 263118-3; 2009; American Institute of Physics	
	C26	CHIANG, Wen Jen Et al., "Silicon Nanocrystal-Based Photosensor on Low-Temperature Polycrystalline-Silicone Panels", Applied Physics Letters, 2007, 51120-1-51120-3, Ltt. 91, American Inst. Of Physics, Melville, NY.	
	C27	CHICHKOV, B.N. et al, "Femtosecond, picosecond and nanosecond laser ablation of solids" Appl. Phys. A 63, 109-115; 1996.	
	C28	Chien et al, "Pulse Width Effect in Ultrafast Laser Processing of Materials," Applied Physics A, 2005, 1257-1263, 81, Springer Berlin, Heidelberg, Germany.	
	C29	Choubey et al., On Evolution of CMOS Image Sensors, Proceedings of the 8th International Conference on Sensing Technology, Sep. 2-4, 2014, Liverpool, UK, pages.	
	C30	CILINGIROGLU et al., "An evaluation of MOS Interface-Trap Charge Pump as and Ultralow Constant-Current Generator," IEEE Journal of Solid-State Circuit, 2003, Vol. 38, No. 1, Jan. 2003, 71-83.	
	C31	Clapham, P.B. et al, "Reduction of Lens Reflexion by the Moth Eye Principle" Nature, Vol 244. Aug. 1973, pp. 281-282	

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
Sheet	20	of	26	Attorney Docket No.:	143705.06021(S)

	C32	CMOSIS; "Global Shutter Image Sensors for Machine Vision Application"; Image Sensors Europe 2010, Mar. 23-25, 2010; .COPYRGT. copyright 2010.	
	C33	Cotter, Jeffrey E.; Optical intensity of light in layers of silicon with rear diffuse reflectors; Journal of Applied Physics; Jul. 1, 1998; pp. 618-624; vol. 84, No. 1; American Institute of Physics.	
	C34	Crouch et al., "Comparison of Structure and Properties of Femtosecond and Nanosecond Laser-Structured Silicon" Appl. Phys. Lett., 2004, 84,1850-1852.	
	C35	Crouch et al., "Infrared Absorption by Sulfur-Doped Silicon Formed by Femtosecond Laser Irradiation", Appl. Phys. A, 2004, 79, 1635-1641.	
	C36	Despeisse, et al.; "Thin Film Silicon Solar Cell on Highly Textured Substrates for High Conversion Efficiency"; 2004.	
	C37	Detection of X-ray and Gamma-ray Photons Using Silicon Diodes; Dec. 2000; Detection Technology, Inc.; Micropolis, Finland.	
	C38	DEWAN, Rahul et al.; Light Trapping in Thin-Film Silicon Solar Cells with Submicron Surface Texture; Optics Express; Vol. 17, No. 25; December 7, 2009; Optical Society of America	
	C39	Deych et al.; Advances in Computed Tomography and Digital Mammography; Power Point; Nov. 18, 2008; Analogic Corp.; Peabody, MA	
	C40	Dobie, et al.; "Minimization of reflected light in photovoltaic modules"; Mar. 1, 2009.	
	C41	DOBRZANSKI, L.A. et al.; Laser Surface Treatment of Multicrystalline Silicon for Enhancing Optical Properties; Journal of Materials Processing Technology; page 291 - 296; 2007; Elsevier B.V.	
	C42	Dolgaev et al., "Formation of Conical Microstructures Upon Laser Evaporation of Solids", Appl. Phys. A, 2001, 73, 177-181.	
	C43	Duerinckx, et al.; "Optical Path Length Enhancement for >13% Screenprinted Thin Film Silicon Solar Cells"; 2006.	
	C44	Dulinski, Wojciech et al.; Tests of backside illumincated monolithic CMOS pixel sensor in an HPD set-up; Nuclear Instruments and methods in Physics Research; Apr. 19, 2005; pp. 274-280; Elsevier B.V.	
	C45	Fontaine, A Review of the 1.4 µm Pixel Generation, Technology Analysis Group Chipworks Inc., 2011, 4 pages.	
	C46	Fontaine, Ray, A Survey of Enabling Technologies in Successful Consumer Digital Imaging Products (Part 3: Pixel Isolation Structures), http://www.techinsights.com,July 24, 2017, 13 pages.	
	C47	Forbes, L. and M.Y. Louie, "Backside Nanoscale Texturing to Improve IR Response of Silicon Photodetectors and Solar Cells," Nanotech, vol. 2, pp. 9-12, Jun. 2010.	
	C48	FORBES; "Texturing, reflectivity, diffuse scattering and light trapping in silicon solar cells"; 2012	
	C49	Fowlkes et al., "Surface Microstructuring and Long-Range Ordering of Silicon Nanoparticles", Appl. Phys. Lett., 2002, 80 (20), 3799-3801.	
	C50	Gibbons, J., "Ion Implantation in Semiconductors-Part II; Damage Production and Annealing", proceedings of the IEEE Vol. 60, No. 9 pp. 1062-1096. Jun. 1972.	
	C51	Gjessing, J. et al.; 2D back-side diffraction grating for impored light trapping in thin silicon solar cells; Optics Express; vol. 18, No. 6; pp. 5481-5495; Mar. 15, 2010; Optical Society of America.	
	C52	Gjessing, J. et al.; 2D blazed grating for light trapping in thin silicon solar cells; 3 pages; 2010; Optical Society of America.	
	C53	Gloeckler et al. Band-Gap Grading in CU(In,GA)Se2 Solar Cells, Journal of Physics and Chemistry of Solids; 2005; pages 189-194; vol. 66.	
	C54	Goetzberger, et al.; "Solar Energy Materials & Solar Cells"; vol. 92 (2008) pp. 1570-1578.	
	C55	HAN et al., "Evaluation of a Small Negative Transfer Gate Bias on the Performance of 4T CMOS Image Sensor Pixels," 2007 International Image Sensor Workshop, 238-240, Ogunquit, Maine.	

Examiner Signature		Date Considered	

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Sheet	21	of	26	Attorney Docket No.:	143705.06021(S)

	C56	HAUG, et al.; "Light Trapping effects in thin film silicon solar cells"; 2009	
	C57	Her et al., "Microstructuring of Silicon with Femtosecond Laser Pulses," Applied Physics Letters, 1998, 1673-1675, vol. 73, No. 12, American Institute of Physics.	
	C58	Her et al., "Novel Conical Microstructures Created in Silicon With Femtosecond Laser Pulses", CLEO 1998, 511-512, San Francisco, CA.	
	C59	Her, et al., "Femtosecond laser-induced formation of spikes on silicon," Applied Physics A, 2000, 70, 383-385.	
	C60	HERMANN, S. et al.; Impact of Surface Topography and Laser Pulse Duration for Laser Ablation of Solar Cell Front Side Passivating SiNx Layers; Journal of Applied Physics; Vol. 108, No. 11; pages 114514-1 - 114514-8; 2010; American Institute of Physics	
	C61	High--Performance Technologies for Advanced Biomedical Applications; .COPYRGT. 2004Brochure; pp. 1-46; PerkinElmerOptoelectronics	
	C62	Holland; Fabrication of Detectors and Transistors on High-Resistivity Silicon; Nuclear Instruments and Methods in Physics Research, vol. A275, pp. 537-541 (1989).	
	C63	HONG et al., "Cryogenic processed metal-semiconductor-metal (MSM) photodetectors on MBE grown ZnSe,", 1999, IEEE Transactions on Electron Devices, vol. 46, No. 6, pp. 1127-1134.	
	C64	HSIEH et al., "Focal-Plane-Arrays and CMOS Readout Techniques of Infrared Imaging Systems," IEE Transactions on Circuits and Systems for Video Technology, 1997, vol. 7, no. 4, Aug. 1997, 594-605.	
	C65	http://electroiq.com/insights-from-leading-edge/2016/09/iftle-303-sony-introduces-ziptronix-dbi-technology-in-samsung-galaxy-s7, "Omnivision was the first to sample BSI in 2007 but costs were too high and adoption was thus very low", (2016)	
	C66	http://joseph-tang.blogspot.com/2017/, Oshiyama et al. , Near-infrared Sensitivity Enhancement of a Back-illuminated Complementary Metal Oxide Semiconductor Image Sensor with a Pyramid Surface for Diffraction Structure,(2017)	
	C67	https://blogs.yahoo.co.jp/miyabiman_now/25628945.html	
	C68	Hu et al., "Solar Cells from Basic to Advanced Systems," McGraw Hill Book Co., 1983, 39, New York, New York.	
	C69	Huang, et al.; "Key Technique for texturing a uniform pyramid structure with a layer of silicon nitride on monocrystalline silicon wafer" Applied Surface Science; 2013 pp. 245-249	
	C70	HUANG, et al.; "Microstructured silicon photodetector"; Applied Physics Letters 89, 033506; 2006 American Institute of Physics; 2006	
	C71	HÜPKES, J. et al.; Light Scattering and Trapping in Different Thin Film Photovoltaic Devices; 24th European Photovoltaic Solar Energy Conference, Hamburg, Germany (Sept. 21-25, 2009); pgs. 2766-2769	
	C72	Igalson et al. Defect States in the CIGS Solar cells by Photocapacitance and Deep Level Optical Spectroscopy; Bulletin of the Polish Academy of Sciences Technical Sciences; 2005; pp. 157-161; vol. 53(2).	
	C73	IMEC, 3D INTEGRATED IMAGE SENSORS FOR SMART IMAGING SYSTEMS, PIET DE MOOR, 2010, 32 pages.	
	C74	Itonaga et al., "Extremely-low-noise CMOS Image Sensor with high saturation capacity," 2011 International Electron Devices Meeting, Washington, DC, 2011, pp. 8.1.1-8.1.4.	
	C75	Jansen, H. et al., "The Black Silicon Method: a universal method for determining the parameter setting of a flourine-based reactive ion etcher in deep silicon trench etching with profile control",J. Micromech. Microeng. Vol. 5, 1995 pp.115-120.	
	C76	Job et al., "Doping of Oxidized Float Zone Silincon by Thermal Donors - A low Thermal Budget Doping Method for Device Applications?" Mat. Res. Soc. Symp. Pro.; v. 719, F9.5.1-F9.5.6 (2002).	
	C77	Joy, T. et al.; Development of a Production-Ready, Back-Illuminated CMOS Image Sensor with	

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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Sheet	22	of	26	Attorney Docket No.:	143705.06021(S)

		Small Pixels; Electron Devices Meeting; pp. 1007-1010; 2007; IEEE.	
	C78	Juntunen et al.; Advanced Photodiode Detector for Medical CT Imaging: Design and Performance; 2007; pp. 2730-2735; IEEE.	
	C79	KIM et al.; "Strong Sub-Band-Gap Infrared Absorption in Silicon Supersaturated with Sulfur"; 2006 Appl. Phys. Lett. 88, 241902-1 – 241902-3	
	C80	Kitamura et al., "Suppression of crosstalk by using backside deep trench isolation for 1.12μm backside illuminated CMOS image sensor," 2012 International Electron Devices Meeting, San Francisco, CA, 2012, pp. 24.2.1-24.2.4.	
	C81	Koh et al., "Simple nanostructuring on silicon surfaceby means of focused beam patterning and wet etching", Applied Surface Science, 2000 pp. 599-603.	
	C82	Kolasinski et al., "Laser Assisted and Wet Chemical Etching of Silicon Nanostructures," J. Vac. Sci. Technol., A 24(4), Jul/Aug 2006, 1474-1479.	
	C83	Konstantatos et al., "Engineering the Temproal Response of Photoconductive Photodetectors via Selective Introduction of Surface Trap States," Nano Letters, v. 8(5), pp. 1446-1450 (Apr. 2, 2008).	
	C84	Konstantatos et al., "PbS Colloidal Quantum Dot Photoconductive Photodetectors: Transport, Traps, and Gain," Appl. Phys. Lett., v. 91, pp. 173505-1-173505-3 (Oct. 23, 2007).	
	C85	KOREAN INTELLECTUAL PROPERTY OFFICE (KIPO), CMOS Image Sensor, KIPO, 2004, 29 pages.	
	C86	Kray, D. et al.; Laser-doped Silicon Soalr Cells by Laser Chemical Processing (LCP) exceeding 20% Efficiency; 33rd IEEE Photovoltaic Specialist Conference; 3 pages; May 2008; IEEE.	
	C87	Kroning et al.; X-ray Imaging Systems for NDT and General Applications; 2002; Fraunhofer Institute for Nondestructive Testing; Saarbrucken and Dresden, Germany.	
	C88	Kryski; A High Speed 4 Megapixel Digital CMOS Sensor; 2007 International Image Sensor Workshop; Jun. 6-10, 2007.	
	C89	Lee et al., SNR Performance Comparison of 1.4um Pixel : FSI, Light-guide, and BSI, 2011, 3 pages.	
	C90	Li et al., "Gettering in High Resistive Float Zone Silicon Wafers," Transaction on Nuclear Science," vol. 36(1), pp. 290-294 (Feb. 1, 1989).	
	C91	Li, "Design and Simulation of an Uncooled Double-Cantilever Microbolometer with the Potential for .about.mK NETD," 2004, Sensors and Actuators A, 351-359, vol. 112, Elsevier B.V.	
	C92	Li, Hongsong et al.; An experimental study of the correlation between surface roughness and light scattering for rough metallic surfaces; Advanced Characterization Techniques for Optics, Semiconductors, and Nanotechnologies II; 2005; pp. 25780V-1-25780V-15; vol. 5878; SPIE Bellingham, WA.	
	C93	Lin, A. et al.; Optimization of Random Diffraction Gratings in Thin-Film Solar Cells Using Genetic Algorithms; 2007; 1 page; SSEL Annual Report. cited by applicant .	
	C94	Low Dose Technologies; Power Point	
	C95	Madzharov, et al.; "Light trapping in thin-firm silicon solar cells for superstrate and substrate configuration" Abstract #1614, 218.sup.th ECS Meeting .COPYRGT. 2010 the Electrochemical Society.	
	C96	"Masimo Rainbow SET Pulse CO-Oximetry," 2010, Masimo Corporation, Irvine, California, http://www.masimo.com/Rainbow/about.htm.	
	C97	Mateus; C.F.R. et al.; Ultrabroadband Mirror Using Low-Index Cladded Subwavelength Grating; Photonics Technology Letters; vol. 16, Issue No. 2; pp. 518-520; Feb. 2004; IEEE.	
	C98	Matsuno, Shigeru et al.; Advanced Technologies for High Efficiency Photovoltaic Systems; Mitsubishi Electric Advance; vol. 122; pp. 17-19; Jun. 2008	
	C99	Meynants, et al.; "Backside illuminated global shutter COMOS image sensors"; 2011 International Image Sensor Workshop; Jun. 11, 2011.	

Examiner Signature		Date Considered	

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Sheet	23	of	26	Attorney Docket No.:	143705.06021(S)

	C100	Minoglou et al., "Reduction of Electrical Crosstalk in Hybrid Backside Illuminated CMOS Imagers using Deep Trench Isolation," 2008 International Interconnect Technology Conference, Burlingame, CA, USA, 2008, pp. 129-131.	
	C101	MOLONEY, A.M. et al.; Novel Black Silicon PIN Photodiodes; 8 pages; January 25, 2006; SPIE.	
	C102	Moon et al. Selective emitter using porous silicon for crystalline silicon solar cells. Solar Energy Materials & Solar Cells, v. 93, pp. 846-850 (2009).	
	C103	Moses; Nuclear Medical Imaging--Techniques and Challenges; Power Point; Feb. 9, 2005; Lawrence Berkeley National Laboratory Department of Functional Imaging.	
	C104	MUNCK, Generic building blocks for 3D integration and their application on hybrid CMOS image sensors, KATHOLIEKE UNIVERSITEIT LEUVEN, Kapeldreef 75 — B-3001 Heverlee, September 2008, 328 pages.	
	C105	Munday, J.N. et al.; Large Integrated Absorption Enhancement in Plasmonic Solar Cells by Combining Metallic Gratings and Antireflection Coatings; Nano Letters; vol. 11, No. 6; pp. 2195-2201; Oct. 14, 2010; American Chemical Society	
	C106	Murkin, JM and Arangol, M, "Near Infrared spectroscopy as an index of rain and tissue oxygenation," Bri. J. of Anathesia (BJA/PGA Supplement):13-il3 (2009).	
	C107	Myers, Richard et al., "Enhancing Near-IR Avalanche Photodiodes Performance by Femtosecond Laser Microstructuring" Harvard Dept. Of Physics.	
	C108	Nauka et al., "New Intrinsic Gettering Process in Silicon Based on Interactions of Silicon Interstitials," J. App. Phys., vol. 60(2), pp. 615-621, July 15, 1986.	
	C109	Nauka et al., Intrinsic Gettering in Oxygen-Free Silicon; App. Phys. Lett., vol. 46(7), Apr. 4, 1985.	
	C110	Nayak et al, "Semiconductor Laesr Crystallization of a--Si:H," SPIE Digital Library, 2003, 277-380, vol. 4977, Bellingham, Washington. 2003.	
	C111	Nayak et al, "Semiconductor Laser Crystallization of a--Si:H on Conducting Tin-Oxide-Coated Glass for Solar Cell and Display Applications," Applied Physics A, 2005, 1077-1080, 80, Springer Berlin, Heidelberg, Germany	
	C112	Nayak et al, "Ultrafast-Laser-Assisted Chemical Restructuring of Silicon and Germanium Surfaces," Applied Surface Science, 2007, 6580-6583, vol. 253, Issue 15, Elsevier B.V.	
	C113	NAYAK, B.K. et al.; Ultrafast Laser Textured Silicon Solar Cells; Mater. Res. Soc. Symp. Proc.; Vol. 1123; 6 pages; 2009; Materials Research Society	
	C114	NAYAK, et al.; "Efficient light trapping in silicon solar cells by ultrafast-laser-induced self-assembled micro/nano structures"; Progress in Photovoltaics: Research and Applications; 2011	
	C115	Oden, et al.; "Optical and Infrared Detection Using Microcantilevers;" SPIE Digital Library on Oct. 13, 2010; vol. 2744; 10 pages.	
	C116	Ohring, Milton." The Materials of Science of Thin Films"; pp.176-179; Academic Press, 1992.	
	C117	Pain, Bedabrata; "A Back-Illuminated Megapixel CMOS Image Sensor"; http://hdl.handle.net/2014/39312; May 1, 2005	
	C118	Pain, Bedabrata; Backside Illumination Technology for SOI-CMOS Image Sensors; 2009 IISW Symposium on Backside Illujination of Solid-State Image Sensors, Bergen Norway; Jun. 25, 2009; pp. 1-23.	
	C119	Palm et al. CIGSSe Thin Film PB Modules: From Fundamental Investigators to Advanced Performance and Stability; Thin Solid Films; 2004; pp. 544-551; vol. 451-2.	
	C120	Park et al., "Deep Trench Isolation for Crosstalk Suppression in Active Pixel Sensors with 1.7μm Pixel Pitch", in Japanese Journal of Applied Physics, Vol. 46, No. 4B, pp. 2454-5457, 2007	
	C121	Payne, D.N.R. et al.; Characterization of Experimental Textured ZnO:Al Films for Thin Film Solar Cell Applications and Comparison with Commercial and Plasmonic Alternatives; Photovoltaic Specialists Conference (PVSC); pp. 1560-1564; 2010; IEEE.	
	C122	Pedraza et al., "Silicon Microcolumn Arrays Grown by Nanosecond Pulsed-Excimer Laser	

Examiner Signature		Date Considered	

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Sheet	24	of	26	Attorney Docket No.:	143705.06021(S)

		Irradiation", Appl. Phys. Lett., 1999, 74 (16), 2322-2324, American Institute of Physics. cited by applicant .	
	C123	Pedraza et al., "Surface Nanostructuring of Silicon", Appl. Phys. A, 2003, 77, 277-284.	
	C124	Rao, et al., Monolithic and Fully-Hybrid Backside Illuminated CMOS Imagers for Smart Sensing, IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 4 pages.	
	C125	Rashkeev et al., "Hydrogen passivation and Activation of Oxygen Complexes in Silicon," American Institute of Physics, vol. 78(11), pp. 1571-1573 (Mar. 12, 2001).	
	C126	RUSSELL, et al.; “Nanosecond Eximer Laser Processing for Novel Microelectronic Fabrication”; Nanosecond Excimer Laser Processing; 6 pages; 1989	
	C127	Russell, Ramirez and Kelley, "Nanosecond Excimer Laser Processing for Novel Microelectronic Devices," US Navy, SPAWAR, San Diego, Techical Report, 2003.	
	C128	Russell, Ramirez, Kelley, "Nanosecond Excimer Laser Processing for Novel Microelectronic Fabrication," SSC Pacific Technical Reports , pp. 228-233, 2003, vol. 4, US Navy.	
	C129	Sai, H. et al.; Enhancement of Light Trapping in Thin-Film Hydrogenated Microcrystalline Si Solar Cells Using Back Reflectors with Self-Ordered Dimple Pattern; Applied Physics Letters; vol. 93; 2008; American Institute of Physics.	
	C130	Sanchez et al., "Dynamics of the Hydrodynamical Growth of Columns on Silicon Exposed to ArF Excimer-Laser Irradiation ", Appl. Phys. A, 66, 83-86 (1998). cited by other .	
	C131	Sanchez et al., "Whiskerlike Structure Growth on Silicon Exposed to ArF Excimer Laser Irradiation", Appl. Phys. Lett., 1996, 69 (5), 620-622.	
	C132	Sarnet et al.; “Femtosecond laser for black silicon and photovoltaic cells”; February 21, 2008, Proc. Of SPIE; Vol. 6881; pags 1-15	
	C133	Senoussaoui, N. et al.; Thin-Film Solar Cells with Periodic Grating Coupler; Thin Solid Films; pp. 397-401; 2003; Elsevier B.V.	
	C134	Serpenguzel et al., "Temperature Dependence of Photluminescence in Non-Crystalline Silicon", Photonics West (San Jose, CA, 2004) 454-462.	
	C135	Shen et al., "Formation of Regular Arrays of Silicon Micorspikes by Femotsecond Laser Irradiation Through A Mask", Appl. Phys. Lett., 82, 1715-1717 (2003).	
	C136	Solar Energy Research Institute, "Basic Photovoltaic Principles and Methods," Van Nostrand Reinhold Co., NY 1984, pp. 45-47 and 138-142.	
	C137	Solhusvik, J. et al. “A 1280x960 3.75um pixel CMOS imager with Triple Exposure HDR,” Proc. of 2009 International Image Sensor Workshop, Bergen, NORWAY, June 22-28, 2009.	
	C138	STMicroelctronics, BSI – technical challenges, IISW-2009, Bergen. 25th June 2009, 37 pages.	
	C139	Stone et al.; The X-ray Sensitivity of Amorphous Selenium for Mammography;.Am. Assoc. Phys. Med.; Mar. 2002; pp. 319-324; vol. 29 No. 3; Am. Assoc. Phys. Med.	
	C140	Szlufcik, J. et al.; Simple Integral Screenprinting process for selective emitter polycrystalline silicon solar cells; Applied Physics Letters; vol. 59, No. 13; Sep. 23, 1991; American Institute of Physics.	
	C141	TABBAL et al., “Formation of Single Crystal Sulfur Supersaturated Silicon Based Junctions by Pulsed Laser Melting”. 2007, J. Vac. Sci. Technol. B25(6), 1847-1852	
	C142	Takayanagi, et al.; "A 600.times.600 Pixel, 500, fps CMOS Image Sensor with a 4.4 jum Pinned Photodiode 5-Transistor Global Shutter Pixel"; 2007 International Image Sensor Workshop; Jun. 6-10, 2007.	
	C143	Tournier, et al., Pixel-to-Pixel isolation by Deep Trench technology, STMicroelectronics, 850, rue Jean Monnet – F-38926 Crolles Cedex – France, 2011, 4 pages.	
	C144	Tournier, et al., Pixel-to-Pixel isolation by Deep Trench technology: Application to CMOS Image Sensor, https://www.researchgate.net/publication/268300742, 2011, 5 pages.	
	C145	Tower, John R. et al.; Large Format Backside Illuminated CCD Imager for Space Surveillance; IEEE Transactions on Electron Devices, vol. 50, No. 1; Jan. 2003; pp. 218-224.	

Examiner Signature		Date Considered	

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Sheet	25	of	26	Attorney Docket No.:	143705.06021(S)

	C146	TULL; "Femtosecond Laser Ablation of Silicon: Nanoparticles, Doping and Photovotaics"; Harvard University, June 2007 (Thesis)	
	C147	UEHARA et al., "A High-Sensitive Digital Photosensor Using MOS Interface-Trap Charge Pumping," IEICE Electronics Express, 2004, vol. 1, no. 18, 556-561.	
	C148	Wilson, "Depth Distributions of Sulfur Implanted Into Silicon as a Function of Ion energy, Ion Fluence, and Anneal Temperature," 1984, Appl. Phys. 55(10, 3490-3494.	
	C149	Winderbaum, S. et al.; Reactive ion etching (RIE) as a method for texturing polycrystalline silicon solar cells; Solar Energy Materials and Solar Cells; 1997; pp. 239-248; Elsevier Science B.V.	
	C150	Wu et al., "Black Silicon" Harvard UPS 1999	
	C151	Wu et al., "Black Silicon: A New Light Absorber," APS Centennial Meeting (Mar. 23, 1999).	
	C152	Wu et al., "Femtosecond laser-gas-solid interactions," Thesis presented to the Department of Physics at Harvard University, pp. 1-113, 126-136, Aug. 2000.	
	C153	Wu et al., "Visible Luminescence From Silicon Surfaces Microstructured in Air". Appl. Phys. Lett., vol. 81, No. 11, 1999-2001 (2002).	
	C154	Wu, et al "Near-Unity Below-Band-Gap Absorption by Microstructured Silicon," 2001, Applied Physics Letters, 1850-1852, vol. 78, No. 13, American Institute of Physics.	
	C155	XIONG , Y., et al, "Depth from focusing and defocusing", COMPUTER VISION AND PATTERN RECOGNITION, 1993. PROCEEDINGS CVPR '93., 1993 IEEE , LOS ALAMITOS, CA, USA.IEEE COMPUT. SOC, 15 June 1993 (1993-06-15), pages 68-73,	
	C156	Xu, Y., et al, "Infrared Detection Using Thermally Isolated Diode," Sensors and Actuators A, Elsevier Sequoia S.A., 1993, vol. 36, 209-217, Lausanne, Switzerland.	
	C157	Yablonovitch, et al.; "Intensity Enhancement in Textured Optical Sheets for Solar Cells"; .COPYRGT. 1982 IEEE.	
	C158	YAMAMOTO, K. et al.; NIR Sensitivity Enhancement by Laser Treatment for Si Detectors; Nuclear Instruments and Methods in Physics Research A; pages 520 - 523; March 31, 2010; Elsevier	
	C159	Yan, B.; Light Trapping Effect from Randomized Textures of Ag/ZnO Back Reflector on Hyrdrogenated Amorphous and Nanocrystalline Silicon Based Solar Cells; Thin Film Solar Technology II; vol. 7771; 2010; SPIE.	
	C160	Yasutomi, et al.; "Two-Stage Charge Transfer Pixel Using Pinned Diodes for Low-Noise Global Shutter Imaging"; 2009 International Image Sensor Workshop; Mar. 28, 2009.	
	C161	Yaung et al., "High performance 300mm backside illumination technology for continuous pixel shrinkage," 2011 International Electron Devices Meeting, Washington, DC, 2011, pp. 8.2.1-8.2.4.	
	C162	Younkin et al., "Infrared Absorption by Conical Silicon Microstructures Made in a Variety of Background Gases Using Femtosecond-Laser Pulses", J. Appl. Phys., 93, 2626-2629 (2003).	
	C163	Younkin, "Surface Studies and Microstructure Fabrication Using Femtosecond Laser Pulses," Thesis presented to the Division of Engineering & Applied sciences at Harvard University (Aug. 2001).	
	C164	YUAN, et al.; "Efficient black silicon solar cell with a density-graded nanoporous surface: Optical properties, performance limitations, and design rules"; American Institute of Physics; Applied Physics Letters 95. 1230501 (2009) 3 pages	
	C165	Zaidi, S.H. et al.; Diffraction Grating Structures in Solar Cells; Photovoltaic Specialists Conference, 2000; 4 pages; Sep. 2000; IEEE.	
	C166	Zhang et al, "Ultra-Shallow P+-Junction Formation in Silicon by Excimer Laser Doping: a Heat and Mass Transfer Perspective," Int. J. Heat Mass Transfer, 1996, 3835-3844, vol. 39, No. 18, Elsevier Science Ltd., Great Britain.	
	C167	Zhong, S. et al. "Excellent Light Trapping in Ultrathin Solar Cells," AFM-Journal, May 2016 pp.	

Examiner Signature		Date Considered	

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		1-11.	
	C168	Zhu et al., "Evolution of Silicon Surface Microstructures by Picosecond and Femtosecond Laser Irradiations," Applied Surface Science, 2005, 102-108, Elsevie, Amsterdam, NL.Ultra-Shallow P+-Junction Formation in Silicon by Excimer Laser Doping: a Heat and Mass Transfer Perspective," Int. J. Heat Mass Transfer, 1996, 3835-3844, vol. 39, No. 18, Elsevier Science Ltd., Great Britain.	
	C169	Ziou et al., "Depth from defocus using the hermite transform", IMAGE PROCESSING, 1998. ICIP 98. Intl. Conference on Chicago, IL. October 1998 pp. 958 - 962.	

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International Application Number:	
Confirmation Number:	4345
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	136549
Filer:	Andrew W. Schultz
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Information:					
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Information:					
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15	Non Patent Literature	16_Yaung_8.pdf	340363 268c30957d82d66a02348acd4c79c864ac269d50	no	4
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

136549 7590 03/07/2019

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER
EVERHART, CARIDAD

ART UNIT	PAPER NUMBER
2895	

DATE MAILED: 03/07/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/614,256	06/05/2017	Homayoon Haddad	143705.06021	4345

TITLE OF INVENTION: SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	06/07/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

SAMSUNG EX. 1002 - 1623/1684

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

136549 7590 03/07/2019

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/614,256	06/05/2017	Homayoon Haddad	143705.06021	4345

TITLE OF INVENTION: SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	06/07/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
EVERHART, CARIDAD	2895	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

SAMSUNG EX. 1002 - 1624/1684

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/614,256	06/05/2017	Homayoon Haddad	143705.06021	4345

136549 7590 03/07/2019

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER	
EVERHART, CARIDAD	
ART UNIT	PAPER NUMBER
2895	

DATE MAILED: 03/07/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

SAMSUNG EX. 1002 - 1625/1684

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/614,256	Applicant(s) Haddad et al.	
	Examiner CARIDAD EVERHART	Art Unit 2895	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to amendment filed with filing of RCE 12/26/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-2,5-6,8-14,17-18,21-30 and 33-53 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/CARIDAD EVERHART/
Primary Examiner, Art Unit 2895

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/26/2018 has been entered.

Allowable Subject Matter

Claims 1-2, 5-6, 8-14, 17-18, 21-30, and 33-53 are allowed.

The following is an examiner's statement of reasons for allowance: The two IDS filed 12/28/2018 have been considered. The prior art of record does not disclose nor suggest all of the limitations of the allowed claims. For example, Okuno (JP 2006-147991 A) discloses an image pickup device with a rugged structure in the light incidence side of the optoelectric transducer (para. 0001-0010 of the machine translation which was provided with the reference cited in the IDS). Okuno also discloses in Fig. 1 a silicon substrate 2, an oxide film 4, a gate electrode 5, an interlayer insulation film 6, wiring 7, and color filter 8, and a rugged structured portion 10, which is made ofa plurality of fine unevenness which is formed by lithography for providing antirefection (para. 0017 and 0019 of the

machine translation) However, Okuno does not disclose nor suggest the limitation "a support substrate coupled to said semiconductor layer and a first bonding layer disposed between the semiconductor layer and the support substrate" nor the limitation "bonding the first bonding layer to a second bonding layer disposed on the support substrate", among other limitations of the allowed claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARIDAD EVERHART whose telephone number is (571)272-1892. The examiner can normally be reached on M-F 6:00 AM-4:00 PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on 571-272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CARIDAD EVERHART/
Primary Examiner, Art Unit 2895

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/614,256	Haddad et al.
	Examiner	Art Unit
	CARIDAD EVERHART	2895

CPC - Searched*		
Symbol	Date	Examiner
H01L31/02363, 0236, 02327, 028	9/14/2017	ce
H01L27/14629, 14627, 14643, 1463	03/01/2019	ce
H01L31/0236, 028, 02327	03/01/2019	ce

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST attached	9/14/2017	ce
Reviewed parents	9/14/2017	ce
EAST attached	6/18/18; 6/19/18	ce
Reviewed parents	03/01/2019	ce
EAST attached	03/01/2019	ce

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
EAST	attached	9/14/2017	ce
EAST	attached	03/01/2019	ce

SAMSUNG EX. 1002 - 1631/1684

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/614,256	Haddad et al.
	Examiner	**Art Unit**
	CARIDAD EVERHART	2895

SAMSUNG EX. 1002 - 1632/1684

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/614,256	Haddad et al.
	Examiner	**Art Unit**
	CARIDAD EVERHART	2895

CPC						
Symbol					**Type**	**Version**
H01L	/	27	/	14643	F	2013-01-01
H01L	/	31	/	028	I	2013-01-01
H01L	/	27	/	14629	I	2013-01-01
H01L	/	31	/	182	I	2013-01-01
H01L	/	27	/	14625	I	2013-01-01
H01L	/	27	/	14632	I	2013-01-01
H01L	/	27	/	1464	I	2013-01-01
H01L	/	31	/	02327	I	2013-01-01
H01L	/	27	/	1463	I	2013-01-01
H01L	/	27	/	14689	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	44	
/CARIDAD EVERHART/ Primary Examiner, Art Unit 2895	01 March 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office

Part of Paper No.: 20190301

SAMSUNG EX. 1002 - 1633/1684

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/614,256	Haddad et al.
	Examiner	**Art Unit**
	CARIDAD EVERHART	2895

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L	/	31	/	0232
H01L	/	31	/	028
H01L	/	27	/	146
H01L	/	31	/	18

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	44	
/CARIDAD EVERHART/ Primary Examiner, Art Unit 2895	01 March 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office

Part of Paper No.: 20190301

SAMSUNG EX. 1002 - 1634/1684

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/614,256	Haddad et al.
	Examiner	Art Unit
	CARIDAD EVERHART	2895

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	22	10		19	12	28	28	37	32	46				
2	2	23	11		20	13	29	29	38	33	47				
	3	4	12	26	21	14	30	30	39	34	48				
	4	5	13	27	22		31	31	40	35	49				
19	5	6	14	7	23		32	40	41	36	50				
20	6		15	8	24	15	33	41	42	37	51				
	7		16	9	25	16	34	42	43	38	52				
3	8	24	17	10	26	17	35	43	44	39	53				
21	9	25	18	11	27	18	36	44	45						

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	44	
/CARIDAD EVERHART/ Primary Examiner, Art Unit 2895	01 March 2019	O.G. Print Claim(s)	O.G. Print Figure
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	245	"5236863" | "20120235268" | "7828983" | "20070204902" | "20150076468" | "5100478" | "20120001293" | "6413135" | "5370747" | "9209345" | "9673250" | "20100181014" | "20140138785" | "20140352779" | "20020173119" | "20090286347" | "20110201177"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/01 14:39
L2	502	"20030214595" | "20030228883" | "20060086956" | "7828983" | "20070189583" | "20080192133" | "5626687" | "5727096" | "9184204" | "20100059803" | "5100478" | "20060128087" | "20110292380" | "6082858" | "20050093100" | "5370747" | "9209345" | "20080284884" | "20140198240" | "9369641" | "20080158398" | "5101260" | "5600130" | "6204506" | "20090256226" | "20100200658" | "20070237504" | "7800684" | "20130285130" | "20050093100" | "20110194100" | "5635089" | "6907135"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/01 14:48

EAST Search History (Interference)

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Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	15/614,256
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	06-05-2017
				First Named Inventor:	Homayoon Haddad
				Group Art Unit:	2895
(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
Sheet	1	of	6	Attorney Docket No.:	143705.06021(H)

(a) U. S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document Number Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
	A1	4105955	Hayashi	8/8/1978		
	A2	4181538	Narayan et al.	1/1/1980		
	A3	4343832	Smith	8/10/1992		
	A4	4346164	Tabarelli et al.	8/24/1982		
	A5	4703996	Glass et al.	11/1/1987		
	A6	4723086	Leibovich et al.	2/2/1988		
	A7	4773944	Nath et al.	9/1/1988		
	A8	4838952	Dill et al.	6/1/1989		
	A9	5089437	Shima et al.	2/1/1992		
	A10	5182231	Hongo et al.	1/26/1993		
	A11	5507881	Sichanugrist et al.	4/16/1996		
	A12	5569624	Weiner	10/29/1996		
	A13	5871826	Mei	2/16/1999		
	A14	5898672	Ginzboorg	4/1/1999		
	A15	5918140	Wickboldt et al.	6/29/1999		
	A16	5977515	Uraki et al.	11/2/1999		
	A17	5995606	Civanlar et al.	11/30/1999		
	A18	6019796	Mei	2/1/2000		
	A19	6048588	Engelsberg	4/11/2000		
	A20	6049058	Dulaney et al.	4/11/2000		
	A21	6117499	Wong et al.	9/1/2000		
	A22	6121130	Chua et al.	9/1/2000		
	A23	6128379	Smyk	10/1/2000		
	A24	6242291	Kusumoto et al.	6/1/2001		
	A25	6272768	Danese	8/1/2001		
	A26	6333485	Haight et al.	12/25/2001		
	A27	6372536	Fischer et al.	4/1/2002		
	A28	6457478	Danese	10/1/2002		
	A29	6486046	Fttjimura et al.	11/1/2002		
	A30	6562705	Ohara	5/1/2003		
	A31	6586318	Lu	7/1/2003		
	A32	6653554	Ishihara	11/25/2003		
	A33	6734455	Li	5/11/2004		
	A34	6756104	Sokol et al.	6/1/2004		
	A35	6796144	Shepard et al.	9/1/2004		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.E/

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	A36	6876003	Nakamura et al.	4/5/2005		
	A37	6897118	Poon et al.	5/24/2005		
	A38	7112545	Railkar et al.	9/1/2006		
	A39	7211214	Chou	10/28/3301		
	A40	7413909	Hutchens et al.	8/1/2008		
	A41	7425471	Bruland et al.	9/1/2008		
	A42	7569503	Pan	8/4/2009		
	A43	7586601	Eb stein	9/8/2009		
	A44	7605064	Kizilyalli et al.	10/1/2009		
	A45	7629234	Bruland	12/1/2009		
	A46	7687740	Bruland et al.	3/1/2010		
	A47	7935941	Bruland et al.	5/1/2011		
	A48	8698272	Vineis	4/15/2014		
	A49	9276143	Mazur	3/1/2016		
	A50	9559215	Ahmed	1/31/2017		
	A51	20010044251	Cho et al.	11/1/2001		
	A52	20020034845	Fujimura et al.	3/21/2002		
	A53	20020126333	Hosono et al.	9/12/2002		
	A54	20020176650	Zhao et al.	11/28/2002		
	A55	20030016708	Albrecht et al.	1/23/2003		
	A56	20030024269	Shepard et al.	2/6/2003		
	A57	20030025156	Y arnazaki et al.	2/6/2003		
	A58	20030045074	Seibel et al.	3/6/2003		
	A59	20030132449	Hosono et al.	7/17/2003		
	A60	20030183270	Falk et al.	10/2/2003		
	A61	20040169834	Richter et al.	9/2/2004		
	A62	20050032249	Im et al.	2/10/2005		
	A63	20050226287	Shah et al.	10/13/2005		
	A64	20050227457	Kondo et al.	10/13/2005		
	A65	20060102901	Im et al.	5/18/2006		
	A66	20060231853	Tanaka	10/19/2006		
	A67	20070102709	Burgener et al.	5/10/2007		
	A68	20070131275	Kinsey et al.	6/14/2007		
	A69	20070243701	Ito et al	10/18/2007		
	A70	20070293056	Setsuhara et al.	12/20/2007		
	A71	20080135099	Yu	6/12/2008		
	A72	20090151785	Namn et al.	6/18/2009		
	A73	20090179199	Sano et al	7/16/2009		
	A74	20100171948	Mazur et al.	7/8/2010		
	A75	20100190292	Alberts	7/29/2010		
	A76	20100213582	Coullard et al.	8/26/2010		
	A77	20170141258	McFarland	5/18/2017		

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FOREIGN PATENT DOCUMENTS

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	B1	CN 101053065 A	Werner Jurgen H	10/10/2007				
	B2	EP 1347670 A1	Kitaguchi et al.	9/24/2003				
	B3	JP1994244444 A	Hitachi, Ltd.	9/2/1994				
	B4	JP2002190386	Kitaguchi et al.	7/5/2002				
	B5	JPH06267868 A	Fuji Electric Co Ltd	9/22/1994				
	B6	WO 0131842	Telefonaktiebolaget LM Ericson (publ)	3/5/2001				
	B7	WO 0135601	Rainfinity Inc et al.	5/17/2001				
	B8	WO 2005029599	Matsushita Electric Works Ltd	3/31/2005				
	B9	WO 2006043690	Semiconductor Energy Lab	4/27/2006				
	B10	WO 2006054758	Semiconductor Energy Lab	5/26/2006				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or county where published	T
	C1	Aberle, Progress with polycrystalline silicon thin-film solar cells on glass at UNSW. Journal of Crystal Growth 287,386-390 (2006).	
	C2	Amoruso et al., Emission of nanoparticles during ultrashort laser irradiation of silicon targets. Europhysics Letters 67, 404-410 (2004).	
	C3	Arango et al., Charge transfer in photovoltaics consisting of interpenetrating networks of conjugated polymer and Ti02 nanoparticles. Applied Physics Letters 74, 1698-1700 (1999).	
	C4	Beek et al., Efficient hybrid solar cells from zinc oxide nanoparticles and a conjugated polymer. Advanced Materials 16, 1009-1013 (2004).	
	C5	Bentini et al., Surface doping of semiconductors by pulsed-laser irradiation in reactive atmosphere. Applied Physics A: Materials Science & Processing. 1988;45(4):317-324.	
	C6	Blood et al., Electrical Characterization of Semiconductors. Reports on Progress in Physics 41, 157-257 (1978)..	
	C7	Bouhdata, A. et al. "Modeling Of The Spectral Response Of PIN Photodetectors Impact of Exposed Zone Thickness, Surface Recombination Velocity And Trap Concentration", Microelectronics Reliability 44, pp. 223-228 (2004);	
	C8	Brus, Luminescence of Silicon Materials-Chains, Sheets, Nanoc1ystals, Nanowires, Microcrystals, and Porous Silicon. Journal of Physical Chemistry 98,3575-3581 (1994).	
	C9	Bucksbaum et al., Rapid Melting and Regrowth Velocities in Silicon Heated by Ultraviolet Picosecond Laser-Pulses, Physical Review Letters 53, 182-185 (1984).	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.E/

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Sheet	4	of	6	Attorney Docket No.:	143705.06021(H)

	C10	Bulgakov et al., Silicon clusters produced by femtosecond laser ablation: non-thermal emission and gas-phase condensation. Applied Physics AMaterials Science & Processing 79, 1591-1594 (2004).	
	C11	Campbell et al., Light Trapping Properties of Pyramidally Textured Surfaces. Journal of Applied Physics 62, 243-249 (1987).	
	C12	Carey et al, "High Sensitivity Silicon-Based VIS/NIR Photodetectors", CLEO 2004 (San Francisco, CA 2004) pp. 1-2 cited by other.	
	C13	Carey et al., In-situ doping of silicon using the gas immersion laser doping (GILD) process. Applied Surface Science. vol. 43, Issues 1-4, Dec. 2, 1989, pp. 325-332.	
	C14	Carey et al., Visible and near-infared responsivity of femtosecondlaser microstrnctured silicon photodiodes. Opt. Lett. 2005;30: 1773- 5.	
	C15	Carey, Femtosecond-laser microstructuring of silicon for novel optoelectronic devices. Thesis. The Division of Engineering and Applied Sciences. Harvard University. Cambridge, MA. Jul. 2004 162 pages.	
	C16	Cifre, Polycrystalline Silicon Films Obtained by Hot-Wire Chemical- Vapor-Deposition. Applied Physics aMaterials Science & Processing 59, 645-651 (1994).	
	C17	Contreras et al., Progress toward 20% efficiency in Cu(In,Ca)Se-2 polycrystalline thin-film solar cells. Progress in Photovoltaics 7, 311-316 (1999).	
	C18	Cuadra et al., Present status of intermediate band solar cell research. Thin Solid Films 451-52, 593-599 (2004).	
	C19	Curtins et al., High-Rate Deposition of Amorphous Hydrogenated Silicon-Effect of Plasma Excitation-Frequency. Electronics Letters 23, 228-230 (1987).	
	C20	Delley et al., Quantum Confinement in Si Nanocrystals. Physical Review B 47, 1397-1400 (1993).	
	C21	Glezer et al., Ultrafast-laser driven micro-explosions in transparent materials. Applied Physics Letters 71, 882-884 (1997).	
	C22	Glover et al., Probing paiticle synthesis during femtosecond laser ablation: initial phase transition kinetics. Applied Physics B Lasers and Optics 78, 995-1000 (2004).	
	C23	Glover, Hydrodynamics of particle formation following femtosecond laser ablation. Journal of the Optical Society of America B-Optical Physics 20, 125-131 (2003).	
	C24	Goetzbergeret al., Crystalline Silicon Solar Cells (ed.), Chapter 6, High Efficiency Solar Cells. New York: John Wiley& Sons Ltd, 1994.	
	C25	Green, Recent developments in photovoltaics. Solar Energy 76, 3-8 (2004).	
	C26	Greenham et al.,Charge sepai·ation and transport in conjugatedpolymerjsemiconductor-nanocrystal composites studied by photoluminescence quenching and photoconductivity. Physical Review B 54, 17628-17637 (1996).	
	C27	Halls et al., Efficient Photodiodes from Interpenel:rating Polymer Networks. Nature 376, 498-500 (1995).	
	C28	Hansen, Henri et al. "The Black Silicon Method: A Universal Method For determining The Parameter Setting Of A Fluorine-Based Reactive Ion Etcher In Depp Silicon Trench Etching With Profile Control", J. Micromedch. Microeng. 5 (1`995) pp 115-120	
	C29	Heisterkamp et al., Pulse energy dependence of subcellular dissection by femtosecond laser pulses. Optics Express 13, 3690-3696 (2005).	
	C30	Henry, Limiting Efficiencies of Ideal Single and Multiple Energy Gap Terrestrial Solar-Cells. Journal of Applied Physics 51, 4494-4500 (1980).	
	C31	Huang et al., "A uniform 290 nm periodic Square Strcuture on ZnO Fabricated by Two-Beam Femtosecond Laser Ablation," Nanotechnolgoy, 8 pp. 1-6 (2007);	
	C32	Keppner et al., Passivation Properties of Amorphous and Microcrystalline Silicon Layers Deposited by Vhf-Gd for Crystalline Silicon Solar-Cells. Solar Energy Materials and Solar Cells	

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Sheet	5	of	6	Attorney Docket No.:	143705.06021(H)

		34, 201-209 (1994)".	
	C33	Luque et al., Increasing the efficiency of ideal solar cells by photon induced transitions at intermediate levels. Physical Review Letters 78, 5014-5017 (1997).	
	C34	Marti et al., Limiting efficiencies for photovoltaic energy conversion in multigap systems. Solar Energy Materials and Solar Cells 43, 203-222 (1996).	
	C35	Meier et al., Recent progress in micromorph solar cells. Journal of Non-Crystalline Solids 230, 1250-1256 (1998).	
	C36	Meier etal., Complete Microc1ystalline P-1-N. SolarCell-Crystalline or Amorphous Cell Behavior. Applied Physics Letters 65, 860-862 (1994).	
	C37	Mo et al., Sulfm point defects in crystalline and amorphous silicon. Physical Review B 70 (2004).	
	C38	Morneault, K. et al., "ISDN Q.921-User Adaptation Layer," Network Working Group, Request for Comments: 3057, The Internet Society, pp. 1-66, (2001).	
	C39	Morneault, K. et al., "SS7 MTP2-User Adaptation Layer," Network Working Group, Internet Draft, The Internet Engineering Task Force, pp. 1-94, (Feb. 2001).	
	C40	Myers et al., Enhancing nearinfrared avalanche photodiode performance by femtosecond laser microstructuring. Applied Optics 45, 8825-8831 (2006).	
	C41	Nayak et al.; "Femtosecond Laser-Induced Micro-Structuring of Thin a-Si:H Films", Material Research Society Symposium proceeedings; volume 850; November 28-December 2, 2004; pages MM1.8.1-MM 1.8.5	
	C42	Nirmal et al., Lwninescence photophysics in semiconductor nanocrystals. Accounts of Chemical Research 32. 407-414 (1999).	
	C43	Ong et al., "Framework Architecture for Signaling Transport," Network Working Group, Request for Comments: 2719, The Internet Society, pp. 1-24, (Oct. 1999).	
	C44	O'Regan et al., A Low-Cost, High-Efficiency Solar-Cell Based on DyeSensitized Colloidal Tio2 Films. Nature 353, 737-740 (1991)..	
	C45	Pavesi, Optical gain in silicon nanocrystals. Nature 408, 440-444 (2000).	
	C46	Rath et al., Limited influence of grain boundary defects in hot-wire CVD polysilicon films on solar cell performance. Journal of Noncrystalline Solids 230, 1277-1281 (1998).	
	C47	Reber et al., Crystalline silicon thin-film solar cellsrecent results at Fraunhofer ISE, Solar Energy 77, 865-875 (2004).	
	C48	Sarnet et al., Laser doping for microelectronics and microtechnology. Proc.of SPIE Vol. 5448 pp. 669-680	
	C49	Schaffer et al., Micromachining bulk glass by use offemtosecond laser pulses with nanojoule energy. Optics Letters 26, 93-95(2001).	
	C50	Schuppler et al., Size, Shape, and Composition of Luminescent Species in Oxidized Si Nanocrystals and H-Passivated Porous Si. Physical Review B 52, 4910-4925 (1995).	
	C51	Serpenguzel et al., "Temperature Dependence Of Photoluminescence In Non-Crystalline Silicon", Photonics West (San Jose, CA, 2004) 454-462.	
	C52	Seto, Electrical Properties of Polyc1ystalline Silicon Films. Jomnal of Applied Physics 46, 5247-5254 (1975)..	
	C53	Shali et al., Thin-film silicon solar cell technology. Progress in Photovoltaics 12, 113-142 (2004)..	
	C54	Sheehy et al., Chalcogen doping of silicon via intense femtosecondlaser irradiation. Materials Science and Engineering B-Solid State Materials for Advanced Technology 137, 289-294 (2007).	
	C55	Sheehy et al., Role of the Background Gas in the Morphology and Optical Properties of Laser-Microstructured Silicon. Chem Mater. 2005; 17(14):3582-6.	
	C56	Shen et al., "Femtosecond laser-induced formation of submicrometer spikes on silicon in water", Appllied Physics Letter, vol. 85(23), p.5694 (2004).	

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Sheet	6	of	6	Attorney Docket No.:	143705.06021(H)

	C57	Shockley et al., Detailed Balance Limit ofEfficiency of p-n Junction Solar Cells. Journal of Applied Physics 32,510-519 (1961).	
	C58	Sidebottom, G. et al., "SS7 MTP3-User Adaptation Layer (M3UA)," Network Working Group, Internet Draft, The Internet Engineering Task Force, pp. 1-128, (Feb. 2001).	
	C59	Sipe et al., Laser-Induced Periodic Surface-Structure .1. Theory. Physical Review B 27, 1141-1154 (1983).	
	C60	Slaoui et al., Advanced inorganic materials for photovoltaics. Mrs Bulletin 32, 211-218 (2007).	
	C61	Staebler et al., Stability of N-I-P. Amorphous-Silicon Solar-Cells. Applied Physics Letters 39, 733-735 (1981).	
	C62	Stalmans et al. Porous silicon in crystalline silicon solar cells: A review and the effect on the internal quantum efficiency. Progress in Photovoltaics 6 233-246 (1998).	
	C63	Stewart, R. et al. "Stream Control Transmission Protocol", Network Working Group, pp. 1-134 (October 2000).	
	C64	Stocks et al., Texturing ofpolycrystalline silicon. Solar Energy Materials and Solar Cells 40, 33-42 (1996).	
	C65	Stupca et al., Enhancement of polycrystalline silicon solar cells using ultrathin films of silicon nanoparticle. Applied Physics Letters 91, 063107 (2007).	
	C66	Svrcek et al., Ex situ prepared Si nanocrystals embedded in silica glass: Formation and characterization. Journal of Applied Physics 95, 3158-3163 (2004).	
	C67	Svrcek et al., Silicon nanocrystals as light converter for solar cells. Thin Solid Films 451-52, 384-388 (2004).	
	C68	Tiwari et al., A silicon nanocrystals based memo1y. Applied Physics Letters 68, 1377-1379 (1996).	
	C69	Torres et al., Device grade microcrystalline silicon owing to reduced oxygen contamination, Applied Physics Letters 69, 1373-1375 (1996).	
	C70	Tull et al., Formation of silicon nanoparticles and web-like aggregates by femtosecond laser ablation in a background gas. Applied Physics a-Materials Science & Processing 83, 341-346 (2006).	
	C71	Tull et al., Silicon surface morphologies after femtosecond laser irradiation, Mrs Bulletin 31, 626-633 (2006).	
	C72	van der Zel, L. "SF6 and the Environment," EPRI, November 2003.	
	C73	Vigue, F. et al. "Visible-blind Ultraviolet Photodetectors based on ZnMgBeSe" Journal of Electronic Materials, Vol. 30, No. 6, pp. 4190-4192 (2001);	
	C74	Wilson et al., Quantum Confinement in Size-Selected, Surface-Oxidized Silicon Nanocrystals. Science 262, 1242-1244 (1993).	
	C75	Wronski, Electronic Properties of Amorphous Silicon in Solar-Cell Operation Ieee Transactions on Electron Devices 24, 351-357 (1977).	
	C76	Wu et al., "13.9% - efficient CdTe polycrystalline thin-film solar cells with an infrared transmission of ~so%", Progress in Photovoltaics 14, 471-483 (2006).	
	C77	Younkin, R. et al. "Infrared absorption by conical silicon microstrnctures made in a variety of background gases using femtosecond-laserpulses," Proc. CLEO 2001 (Baltimore, MD, 2001) p. 556.	
	C78	Yu et al., Polymer Photovoltaic CellsEnhanced Efficiencies Via a Network oflnternal Donor-Acceptor Heterojunctions. Science 270, 1789-1791 (1995).	
	C79	Zhao et al., 19.8% efficient "honeycomb" textured multicrystalline and 24.4% monocrystalline silicon solar cells. Applied Physics Letters 73, 1991-1993 (1998).	

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	A1	3487223	St. John	12/30/1969		
	A2	3922571	Smith	11/25/1975		
	A3	3973994	Redfield	8/10/1976		
	A4	3994012	Warner, Jr.	11/23/1976		
	A5	4017887	Davies et al.	4/12/1977		
	A6	4149174	Shannon	4/10/1979		
	A7	4176365	Kroger	11/27/1979		
	A8	4201450	Trapani	5/6/1980		
	A9	4242149	King et al.	12/30/1980		
	A10	4253882	Dalal	3/3/1981		
	A11	4277793	Webb	7/7/1981		
	A12	4322571	Stanbery	3/30/1982		
	A13	4419533	Czubatyj et al.	12/6/1983		
	A14	4452826	Shields et al.	6/5/1984		
	A15	4493942	Sheng et al.	1/15/1985		
	A16	4514582	Tiedje et al.	4/30/1985		
	A17	4536608	Sheng et al.	8/20/1985		
	A18	4546945	Nessfield	10/15/1985		
	A19	4568960	Petroff et al.	2/4/1986		
	A20	4593303	Dyck et al.	6/3/1986		
	A21	4593313	Nagasaki	6/3/1986		
	A22	4617593	Dudley	10/14/1986		
	A23	4630082	Sakai	12/16/1986		
	A24	4648936	Ashby et al.	3/10/1987		
	A25	4663188	Kane	5/5/1987		
	A26	4672206	Suzuki	6/9/1987		
	A27	4673770	Mandelkorn	6/16/1987		
	A28	4679068	Lillquist et al.	7/7/1987		
	A29	4751571	Lillquist	6/14/1988		
	A30	4775425	Guha et al.	10/4/1988		
	A31	4777490	Sharma et al.	10/11/1988		
	A32	4829013	Yamazaki	5/9/1989		
	A33	4883962	Elliot	11/28/1989		
	A34	4886958	Merryman	12/12/1989		
	A35	4887255	Handa et al.	12/12/1989		

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	A36	4894526	Bethea et al.	1/16/1990		
	A37	4910568	Taki, et al.	3/20/1990		
	A38	4910588	Kinoshita, et al.	3/20/1990		
	A39	4964134	Westbrook et al.	10/16/1990		
	A40	4965784	Land et al.	10/23/1990		
	A41	4968372	Maass	11/6/1990		
	A42	4999308	Nishiura et al.	3/12/1991		
	A43	5021100	Ishihara et al.	6/4/1991		
	A44	5021854	Huth	6/4/1991		
	A45	5080725	Green et al.	1/14/1992		
	A46	5081049	Green et al.	1/14/1992		
	A47	5101260	Nath	3/31/1992		
	A48	5114876	Weiner	5/19/1992		
	A49	5127964	Hamakawa et la.	7/7/1992		
	A50	5164324	Russell et al.	11/17/1992		
	A51	5208822	Haus et al	5/4/1993		
	A52	5223043	Olson et al.	6/29/1993		
	A53	5234790	Lang, et al.	8/10/1993		
	A54	5244817	Hawkins et al.	9/14/1993		
	A55	5296045	Banerjee et al.	3/22/1994		
	A56	5309275	Nishimura et al.	5/3/1994		
	A57	5322988	Russell et al.	6/21/1994		
	A58	5346850	Kaschmitter et al.	9/13/1994		
	A59	5351446	Langsdorf	10/4/1994		
	A60	5373182	Norton	12/13/1994		
	A61	5381431	Zayhowski	1/10/1995		
	A62	5383217	Uemura	1/17/1995		
	A63	5390201	Tomono et al.	2/14/1995		
	A64	5410168	Hisa	4/25/1995		
	A65	5413100	Barthelemy et al.	5/9/1995		
	A66	5449626	Hezel	9/12/1995		
	A67	5454347	Shibata et al.	10/3/1995		
	A68	5502329	Pezzani	3/26/1996		
	A69	5523570	Hairston	6/4/1996		
	A70	5559361	Pezzani	9/24/1996		
	A71	5569615	Yamazaki et al.	10/29/1996		
	A72	5578858	Mueller et al.	11/26/1996		
	A73	5580615	Itoh et al.	12/3/1996		
	A74	5583704	Fujii	12/10/1996		
	A75	5589008	Kepper	12/31/1996		
	A76	5589704	Levine	12/31/1996		
	A77	5597621	Hummel et al.	1/18/1997		
	A78	5600130	VanZeghbroeck	2/4/1997		
	A79	5626687	Campbell	5/6/1997		

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	A80	5627081	Tsuo et al.	5/6/1997		
	A81	5635089	Singh et al.	6/3/1997		
	A82	5640013	Ishikawa, et al.	6/17/1997		
	A83	5641362	Meier	6/24/1997		
	A84	5641969	Cooke et al.	6/24/1997		
	A85	5705413	Harkin et al.	1/6/1998		
	A86	5705828	Noguchi et al.	1/6/1998		
	A87	5708486	Miyawaki et al.	1/13/1998		
	A88	5710442	Watanabe et al.	1/20/1998		
	A89	5714404	Mititsky et al.	2/3/1998		
	A90	5727096	Ghirardi et al	3/10/1998		
	A91	5731213	Ono	3/24/1998		
	A92	5751005	Wyles et al.	5/12/1998		
	A93	5758644	Diab et el.	6/2/1998		
	A94	5766127	Pologe et al.	6/16/1998		
	A95	5766964	Rohatgi et al.	6/16/1998		
	A96	5773820	Osajda, et al.	6/30/1998		
	A97	5779631	Chance	7/14/1998		
	A98	5781392	Clark	7/14/1998		
	A99	5792280	Ruby et al	8/11/1998		
	A100	5802091	Chakrabarti et al	8/1/1998		
	A101	5808350	Jack et al	9/15/1998		
	A102	5859446	Nagasu et al.	1/12/1999		
	A103	5861639	Bernier	1/19/1999		
	A104	5923071	Saito	7/13/1999		
	A105	5935320	Graf et al.	8/10/1999		
	A106	5942789	Morikawa	8/24/1999		
	A107	5943584	Shim et al	8/24/1999		
	A108	5963790	Matsuno et al	10/5/1999		
	A109	5977603	Ishikawa	11/2/1999		
	A110	6071796	Voutsas	6/6/2000		
	A111	6072117	Matsuyama et al.	6/6/2000		
	A112	6080988	Ishizuya et al.	6/27/2000		
	A113	6082858	Grace et al.	7/4/2000		
	A114	6097031	Cole	8/1/2000		
	A115	6106689	Matsuyama	8/22/2000		
	A116	6107618	Fossum et al.	8/22/2000		
	A117	6111300	Cao et al.	8/29/2000		
	A118	6131511	Wachi et al	10/17/2000		
	A119	6131512	Verlinden et al	10/17/2000		
	A120	6147297	Wettling et al.	11/14/2000		
	A121	6160833	Floyd et al.	12/12/2000		
	A122	6168965	Malinovich, et al.	1/2/2001		
	A123	6194722	Fiorini et al.	2/27/2001		

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	A124	6204506	Akahori et al.	3/20/2001		
	A125	6229192	Gu	5/8/2001		
	A126	6252256	Ugge et al.	6/26/2001		
	A127	6290713	Russell	9/18/2001		
	A128	6291302	Yu	9/18/2001		
	A129	6313901	Cacharelis	11/6/2001		
	A130	6320296	Fujii et al.	11/20/2001		
	A131	6327022	Nishi	12/4/2001		
	A132	6331445	Janz et al	12/18/2001		
	A133	6331885	Nishi	12/18/2001		
	A134	6340281	Haraguchi	1/22/2002		
	A135	6372591	Mineji et al.	4/16/2002		
	A136	6372611	Horikawa	4/16/2002		
	A137	6379979	Connolly	4/30/2002		
	A138	6420706	Lurie, et al.	7/16/2002		
	A139	6429036	Nixon, et al.	8/6/2002		
	A140	6429037	Wenham et al.	8/6/2002		
	A141	6465860	Shigenaka, et al.	10/15/2002		
	A142	6475839	Zhang, et al.	11/5/2002		
	A143	6479093	Lauffer et al	11/12/2002		
	A144	6483116	Kozlowski et al.	11/19/2002		
	A145	6483929	Marakami et al.	11/19/2002		
	A146	6486522	Bishay et al.	11/26/2002		
	A147	6493567	Krivitski et al.	12/10/2002		
	A148	6498336	Tian et al.	12/24/2002		
	A149	6500690	Yamagishi et al.	12/31/2002		
	A150	6504178	Carlson et al.	1/7/2003		
	A151	6580053	Voutsas	6/17/2003		
	A152	6583936	Kaminsky et al.	6/24/2003		
	A153	6597025	Lauter et al	7/22/2003		
	A154	6607927	Ramappa et al.	8/19/2003		
	A155	6624049	Yamazaki	9/23/2003		
	A156	6639253	Duane et al.	10/28/2003		
	A157	6667528	Cohen et al.	12/23/2003		
	A158	6677655	Fitzgerald	1/13/2004		
	A159	6677656	Francois	1/13/2004		
	A160	6683326	Iguchi, et al.	1/27/2004		
	A161	6689209	Falster et el.	2/10/2004		
	A162	6690968	Mejia	2/10/2004		
	A163	6753585	Kindt	6/22/2004		
	A164	6759262	Theil et al.	7/6/2004		
	A165	6790701	Shigenaka, et al.	9/14/2004		
	A166	6800541	Okumura	10/5/2004		
	A167	6801799	Mendelson	10/5/2004		

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	A168	6803555	Parrish et al.	10/12/2004		
	A169	6815685	Wany	11/9/2004		
	A170	6818535	Lu et al.	11/16/2004		
	A171	6822313	Matsushita	11/23/2004		
	A172	6825057	Heyers, et al.	11/30/2004		
	A173	6864156	Conn	3/8/2005		
	A174	6864190	Han et al.	3/8/2005		
	A175	6867806	Lee et al.	3/15/2005		
	A176	6900839	Kozlowski et al.	5/31/2005		
	A177	6907135	Gifford	6/14/2005		
	A178	6911375	Guarini et al.	6/28/2005		
	A179	6919587	Ballon et al.	7/19/2005		
	A180	6923625	Sparks	8/2/2005		
	A181	6927432	Holm, et al.	8/9/2005		
	A182	6984816	Holm, et al.	1/10/2006		
	A183	7008854	Forbes	3/7/2006		
	A184	7041525	Clevenger et al.	5/9/2006		
	A185	7057256	Carey, III et al.	6/6/2006		
	A186	7075079	Wood	7/11/2006		
	A187	7091411	Falk et al.	8/15/2006		
	A188	7109517	Zaidi	9/19/2006		
	A189	7126212	Enquist et al.	10/24/2006		
	A190	7132724	Merrill	11/7/2006		
	A191	7202102	Yao	4/10/2007		
	A192	7211501	Liu et al	5/1/2007		
	A193	7235812	Chu, et al.	6/26/2007		
	A194	7247527	Shimomura et al.	7/24/2007		
	A195	7247812	Tsao	7/24/2007		
	A196	7256102	Nakata, et al.	8/14/2007		
	A197	7271445	Forbes	9/18/2007		
	A198	7271835	Iizuka et al.	9/18/2007		
	A199	7285482	Ochi	10/23/2007		
	A200	7314832	Kountz et al.	1/1/2008		
	A201	7315014	Lee et al	1/1/2008		
	A202	7354792	Carey, III et al.	4/8/2008		
	A203	7358498	Geng et al.	4/15/2008		
	A204	7375378	Manivannan et al.	5/20/2008		
	A205	7390689	Mazur et al.	6/24/2008		
	A206	7432148	Li et al.	10/7/2008		
	A207	7442629	Mazur et al.	10/28/2008		
	A208	7446359	Lee, et al.	11/4/2008		
	A209	7446807	Hong	11/7/2008		
	A210	7456452	Wells et al.	11/25/2008		
	A211	7482532	Yi et al.	1/27/2009		

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	A212	7498650	Lauxtermann	3/3/2009		
	A213	7504325	Koezuka et al.	3/17/2009		
	A214	7504702	Mazur et al.	3/17/2009		
	A215	7511750	Murakami	3/31/2009		
	A216	7521737	Augusto	4/21/2009		
	A217	7528463	Forbes	5/5/2009		
	A218	7542085	Altice, Jr. et al.	6/2/2009		
	A219	7547616	Fogel et al.	6/16/2009		
	A220	7551059	Farrier	6/23/2009		
	A221	7560750	Niira et al.	7/14/2009		
	A222	7564631	Li, et al.	7/21/2009		
	A223	7582515	Choi et al.	9/1/2009		
	A224	7592593	Kauffman, et al.	9/22/2009		
	A225	7595213	Kwon et al.	9/29/2009		
	A226	7605397	Kindem et al.	10/20/2009		
	A227	7615808	Pain, et al.	11/10/2009		
	A228	7618839	Rhodes	11/17/2009		
	A229	7619269	Ohkawa	11/17/2009		
	A230	7629582	Hoffman, et al.	12/8/2009		
	A231	7648851	Fu, et al.	1/19/2010		
	A232	7649156	Lee	1/19/2010		
	A233	7705879	Kerr et al.	4/27/2010		
	A234	7728274	Pilla et al	6/1/2010		
	A235	7731665	Lee et al	6/8/2010		
	A236	7741666	Nozaki, et al.	6/22/2010		
	A237	7745901	McCaffrey et al	6/29/2010		
	A238	7763913	Fan et al	7/27/2010		
	A239	7772028	Adkisson et al	8/10/2010		
	A240	7781856	Mazur et al.	8/24/2010		
	A241	7800192	Venezia, et al.	9/21/2010		
	A242	7800684	Tatani	9/21/2010		
	A243	7816220	Mazur et al.	10/19/2010		
	A244	7847253	Carey et al.	12/7/2010		
	A245	7847326	Park, et al.	12/7/2010		
	A246	7855406	Yamaguchi et al	12/21/2010		
	A247	7875498	Elbanhawy, et al.	1/25/2011		
	A248	7880168	Lenchenkov	2/1/2011		
	A249	7884439	Mazur et al.	2/8/2011		
	A250	7884446	Mazur et al.	2/8/2011		
	A251	7897942	Bereket	3/1/2011		
	A252	7910964	Kawahito et al.	3/22/2011		
	A253	7923801	Tian et al.	4/12/2011		
	A254	7968834	Veeder	6/28/2011		
	A255	8008205	Fukushima et al.	8/30/2011		

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	A256	8013411	Cole	9/6/2011		
	A257	8030726	Sumi	10/4/2011		
	A258	8035343	Seman Jr.	10/11/2011		
	A259	8058615	McCaffrey	11/15/2011		
	A260	8076746	McCarten et al.	12/13/2011		
	A261	8080467	Carey et al.	12/20/2011		
	A262	8088219	Knerer et al.	1/3/2012		
	A263	8093559	Rajavel	1/10/2012		
	A264	8164126	Moon, et al.	4/24/2012		
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	A269	8288702	Veeder	10/16/2012		
	A270	8355545	Corcoran et al.	1/15/2013		
	A271	8445950	Iida et al	5/21/2013		
	A272	8445985	Hiyama et al	5/21/2013		
	A273	8456546	Oike	6/4/2013		
	A274	8470619	Bour	6/1/2013		
	A275	8476681	Haddad et al.	7/2/2013		
	A276	8530264	De Munck et al	9/10/2013		
	A277	8564087	Yamamura et al.	10/22/2013		
	A278	8603902	Mazur et al.	12/10/2013		
	A279	8604405	Liu et al	12/10/2013		
	A280	8629485	Yamamura et al.	1/14/2014		
	A281	8649568	Sato	2/11/2014		
	A282	8680591	Haddad et al.	3/25/2014		
	A283	8729678	Shim et al	5/20/2014		
	A284	8742528	Yamamura et al.	6/3/2014		
	A285	8884226	Miyazaki, et al.	11/11/2014		
	A286	8906670	Gray	12/1/2014		
	A287	8916945	Sakamoto et al	12/23/2014		
	A288	8928784	Watanabe et al	1/6/2015		
	A289	8994135	Yamamura et al.	6/31/2015		
	A290	9064762	Yamaguchi	6/23/2015		
	A291	9184204	Hu	11/10/2015		
	A292	9190551	Yamamura et al.	11/17/2015		
	A293	9369641	Hu	6/14/2016		
	A294	9419159	Sakamoto et al.	8/16/2016		
	A295	9478572	Miyanami	10/25/2016		
	A296	9659984	Ohkubo et al	5/23/2017		
	A297	20010017344	Aebi	8/30/2001		
	A298	20010022768	Takahashi	9/20/2001		
	A299	20010044175	Barret et al.	11/22/2001		

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	A300	20010044266	Katsuoka	11/22/2001		
	A301	20020020893	Lhorte	2/21/2002		
	A302	20020024618	Imai	2/28/2002		
	A303	20020056845	Iguchi et al.	5/16/2002		
	A304	20020060322	Tanabe et al.	5/23/2002		
	A305	20020079290	Holdermann	6/27/2002		
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	A307	20020148964	Dausch et al.	10/17/2002		
	A308	20020182769	Campbell	12/5/2002		
	A309	20030029495	Mazur et al.	2/13/2003		
	A310	20030030083	Lee et al.	2/13/2003		
	A311	20030045092	Shin	3/6/2003		
	A312	20030057357	Uppal et al.	3/27/2003		
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	A315	20030213515	Sano et al.	11/20/2003		
	A316	20030214595	Mabuchi	11/20/2003		
	A317	20030228883	Kusakari et al.	12/11/2003		
	A318	20040014307	Shin et al.	1/22/2004		
	A319	20040016886	Ringermacher et al.	1/29/2004		
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	A321	20040046224	Rossel et al.	3/11/2004		
	A322	20040077117	Ding et al.	4/22/2004		
	A323	20040080638	Lee	4/29/2004		
	A324	20040112426	Hagino	6/17/2004		
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	A326	20040161868	Hong	8/19/2004		
	A327	20040222187	Lin	11/11/2004		
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	A329	20040256561	Beuhler et al.	12/23/2004		
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	A331	20050051822	Manning	3/10/2005		
	A332	20050062041	Terakawa et al.	3/24/2005		
	A333	20050063566	Beek et al.	3/24/2005		
	A334	20050088634	Kosugi	4/28/2005		
	A335	20050093100	Chen et al.	5/5/2005		
	A336	20050101100	Kretchmer et al.	5/12/2005		
	A337	20050101160	Garg et al.	5/12/2005		
	A338	20050127401	Mazur et al.	6/16/2005		
	A339	20050134698	Schroeder et al.	6/23/2005		
	A340	20050150542	Madan	7/14/2005		
	A341	20050158969	Binnis et al.	7/21/2005		
	A342	20050184291	Cole et al	8/25/2005		
	A343	20050184353	Mouli	8/25/2005		

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	A344	20050211996	Krishna, et al.	9/29/2005		
	A345	20050227390	Shtein et al.	10/13/2005		
	A346	20060006482	Rieve, et al.	1/12/2006		
	A347	20060011954	Ueda et al.	1/19/2006		
	A348	20060011955	Baggenstoss	1/19/2006		
	A349	20060060848	Chang et al.	3/23/2006		
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	A352	20060086956	Furukawa et al.	4/27/2006		
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	A360	20060145148	Hirai, et al.	7/6/2006		
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	A362	20060160343	Chong et al.	7/20/2006		
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	A364	20060175529	Harmon et al.	8/10/2006		
	A365	20060180885	Rhodes	8/17/2006		
	A366	20060181627	Farrier	8/17/2006		
	A367	20060210122	Cleveland	9/21/2006		
	A368	20060214121	Schrey et al.	9/28/2006		
	A369	20060228897	Timans	10/12/2006		
	A370	20060231914	Carey, III et al.	10/19/2006		
	A371	20060238632	Shah	10/26/2006		
	A372	20060244090	Roy, et al.	11/2/2006		
	A373	20060255340	Manivannan et al.	11/16/2006		
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	A375	20070035849	Li et al.	2/15/2007		
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	A379	20070063219	Sa'ar et al.	3/22/2007		
	A380	20070076481	Tennant	4/5/2007		
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	A383	20070123005	Hiura et al.	5/31/2007		
	A384	20070125951	Snider et al.	6/7/2007		
	A385	20070138590	Wells, et al.	6/21/2007		
	A386	20070145505	Kim et al.	6/28/2007		
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	A388	20070187670	Hsu et al.	8/16/2007		
	A389	20070189583	Shimada et al	8/16/2007		
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	A401	20070298533	Yang et al.	12/27/2007		
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	A407	20080076240	Yannick Veschtti et al.	3/27/2008		
	A408	20080099804	Venezia	5/1/2008		
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	A410	20080121805	Tweet et al.	5/29/2008		
	A411	20080142686	Konno et al.	6/19/2008		
	A412	20080158398	Yaffe et al.	7/3/2008		
	A413	20080170173	Park et al.	7/17/2008		
	A414	20080173620	Grek	7/24/2008		
	A415	20080174685	Shan et al.	7/24/2008		
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	A417	20080179762	Cho et al.	7/31/2008		
	A418	20080191296	Wang et al.	8/14/2008		
	A419	20080191310	Wu et al.	8/14/2008		
	A420	20080192132	Bechtel et al.	8/14/2008		
	A421	20080192133	Abiru et al.	8/14/2008		
	A422	20080196761	Nakano et al.	8/21/2008		
	A423	20080198251	Xu et al.	8/21/2008		
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	A426	20080223436	den Boer et al.	9/18/2008		
	A427	20080242005	Dozen et al.	10/2/2008		
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	A429	20080257409	Li et al.	10/23/2008		
	A430	20080258604	Mazur et al.	10/23/2008		
	A431	20080266434	Sugawa et al.	10/30/2008		

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	A444	20090050944	Hong	2/26/2009		
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	A446	20090057536	Hirose	3/5/2009		
	A447	20090065051	Chan et al.	3/12/2009		
	A448	20090078316	Khazeni et al.	3/26/2009		
	A449	20090090988	OHGISHI	4/9/2009		
	A450	20090095887	Saveliev	4/16/2009		
	A451	20090096049	Oshiyama et al	4/16/2009		
	A452	20090101197	Morikawa	4/23/2009		
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	A454	20090114630	Hawryluk	5/7/2009		
	A455	20090142879	Isaka et al.	6/4/2009		
	A456	20090146240	Carey III et al.	6/11/2009		
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	A460	20090194671	Nozaki et al.	8/6/2009		
	A461	20090200454	Barbier et al.	8/13/2009		
	A462	20090200586	Mao et al.	8/13/2009		
	A463	20090200625	Venezia et al.	8/13/2009		
	A464	20090200626	Qian, et al.	8/13/2009		
	A465	20090200631	Tai, et al.	8/13/2009		
	A466	20090206237	Shannon et al.	8/20/2009		
	A467	20090211627	Meier et al.	8/27/2009		
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	A470	20090223561	Kim et al.	9/10/2009		
	A471	20090227061	Bateman et al.	9/10/2009		
	A472	20090242019	Ramamoorthy et al.	10/1/2009		
	A473	20090242032	Yamazaki et al.	10/1/2009		
	A474	20090242933	Hu, et al.	10/1/2009		
	A475	20090256156	Hsieh	10/15/2009		

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	A476	20090256226	Tatani	10/15/2009		
	A477	20090261255	Nakamura et al.	10/22/2009		
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	A508	20100102366	Lee et el	4/29/2010		
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	A517	20100140733	Lee et al.	6/10/2010		
	A518	20100140768	Zafiropoulo	6/10/2010		
	A519	20100143744	Gupta	6/10/2010		

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	A561	20120049306	Ohba et al.	3/1/2012		
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	A563	20120111396	Saylor et al.	5/10/2012		

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	A583	20130026531	Seo et al.	1/31/2013		
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	A591	20130285130	Ting	10/31/2013		
	A592	20140054662	Yanagita et al	2/27/2014		
	A593	20140198240	Rhoads	7/17/2014		
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	A595	20140374868	LEE et al	12/25/2014		
	A596	20170244920	Ohkubo et al	8/24/2017		
	A597	RE43169	Parker	2/7/2012		

FOREIGN PATENT DOCUMENTS								
Examiner's Initials	**Cite No.**	**Foreign Patent Document** Number Kind Code (if known)	**Name of Patentee or Applicant of Cited Document**	**Date of Publication of Cited Document MM-DD-YYYY**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**			**T**
	B1	AU 3666484	Wenham et al.	6/27/1985				
	B2	CN 101241923	TSMC	8/13/2008				

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				Group Art Unit:	2895
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	B3	CN 101404307	Univ. Zhongshan	4/8/2009				
	B4	CN 101423942	Dong Jiang	5/6/2009				
	B5	CN 101465361	TSMC	6/24/2009				
	B6	CN 101478013	Suntech Power Co Ltd	7/8/2009				
	B7	CN 101634026	Beijing Solar Energy Res Inst	1/27/2010				
	B8	CN 101634027	Beijing Solar Energy Res Inst	1/27/2010				
	B9	CN 101740597	Sony Corp.	6/16/2010				
	B10	CN 101818348	Univ Shejiang	9/1/2010				
	B11	CN 101978498	OMNIVISION TECH INC	2/16/2011				
	B12	CN 102270646	NA	12/7/2011				
	B13	CN 1507075	Beijing Linuosangpu Photovolta	6/23/2004				
	B14	CN 1614789	Shangde Solar Electric Power	5/11/2005				
	B15	CN 201725796	GALAXYCORE INC	1/26/2011				
	B16	DE 19838439	Fraunhofer-Gesellschaft Zur Faurderung Der Angewandten	4/27/2000				
	B17	EP 0473439	Cooper Industries	3/4/1992				
	B18	EP 0566156	Terumo Kabushiki Kaisha	10/20/1993				
	B19	EP 1630871	Matsushita Electric Industrial Co. Ltd.	1/3/2006				
	B20	EP 1873840	Neil et al.	1/2/2008				
	B21	EP 2073270	Hirota, et al.	5/16/2012				
	B22	EP 2509107	Boly Media Comm.	10/10/2012				
	B23	FR 2827707	FR De Detecteurs Infrarouges S	1/24/2003				
	B24	GB 2030766	Plessey Co. Ltd.	4/10/1980				
	B25	JP 11077348	Cannon KK	3/23/1999				
	B26	JP 11097724	Citizen Watch Co. Ltd.	4/9/1999				
	B27	JP 2000164914	Electrowatt Technol Innov AG	6/16/2000				
	B28	JP 2001007381	Japan Broadcasting Corp.	1/12/2001				
	B29	JP 2001024936	Matsushita Electric Industrial Co. Ltd.	1/26/2001				
	B30	JP 2001189478	Sanyo Electric Co.	7/10/2001				
	B31	JP 2001257927	Technosonic KK	9/21/2001				
	B32	JP 2001339057	Fuji Xerox Co. Ltd.	12/7/2001				
	B33	JP 2002043594	Sharp KK	2/8/2002				
	B34	JP 2002134640	United Test CT Inc.	5/10/2002				
	B35	JP 2002513176	Grace et al.	5/8/2002				

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	B36	JP 2003058269	Mitsubishi	2/28/2003				
	B37	JP 2003104121	Matsushita Electric Industrial Co. Ltd.	4/9/2003				
	B38	JP 2003163360	Seiko Epson Corp.	6/6/2003				
	B39	JP 2003242125	Canon KK	8/29/2003				
	B40	JP 2003258285	Sharp KK	9/12/2003				
	B41	JP 2003308130	Matsushita Electric Industrial Co. Ltd.	10/31/2003				
	B42	JP 2004047682	Toshiba Corp.	2/12/2004				
	B43	JP 2004273886	Hatachi Cable	9/3/2004				
	B44	JP 2004273887	Hatachi Cable Ltd.	9/30/2004				
	B45	JP 2005339425	Sanyo Electric Co.	12/8/2005				
	B46	JP 2006033493	Matsushita Electric Industrial Co. Ltd.	2/2/2006				
	B47	JP 2006147991	Canon Inc.	6/8/2006				
	B48	JP 2006173381	Toyota Motor Corp.	6/29/2006				
	B49	JP 2006210701	Sayno Electric Co.	8/10/2006				
	B50	JP 2006255430	Fujitsu Ltd.	9/28/2006				
	B51	JP 2006261372	Sony Corp.	9/28/2006				
	B52	JP 2007122237	Mitsubishi Electric Corp.	5/17/2007				
	B53	JP 2007165909	Icemos Technology Corp.	6/28/2007				
	B54	JP 2007180642	SWCC Showa Device Tech Co. Ltd.	7/12/2007				
	B55	JP 2007180643	Sony Corp.	7/12/2007				
	B56	JP 2007258684	Sony Corp.	10/4/2007				
	B57	JP 2007305675	Sony, Corp.	11/22/2007				
	B58	JP 2008099158	Sony Corp.	4/24/2008				
	B59	JP 2008167004	Sony Corp.	7/17/2008				
	B60	JP 2008187003	Fujitsu Ltd.	8/14/2008				
	B61	JP 2008283219	Toshiba Corp.	11/20/2008				
	B62	JP 2008294698	Sony Corp.	12/4/2008				
	B63	JP 2009021479	Omron Tteisi Electronics Co.	1/29/2009				
	B64	JP 2009152569	Semiconductor Energy Lab	7/9/2009				
	B65	JP 2009253683	Konica Minolta Holdings Inc.	10/29/2009				
	B66	JP 2010278472	Sony, Corp.	12/9/2010				
	B67	JP 2011003860	Sony Corp.	1/6/2011				
	B68	JP 2011091128	Cannon KK	5/6/2011				
	B69	JP 2012054321	Sony Corp.	3/15/2012				
	B70	JP 2012169530	Sony Corp.	9/6/2012				
	B71	JP 2012191005	Sony Corp.	10/4/2012				
	B72	JP 2012212349	Hitachi Solutions Ltd.	11/1/2012				

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	B73	JP 9148594	Sanyo Electric Co.	6/6/1997				
	B74	JP H02152226	Fujitsu Ltd.	6/12/1990				
	B75	JP H02237026	Sony, Corp.	9/19/1990				
	B76	JP H03183037	Nec Corp.	8/9/1991				
	B77	JP H04318970	Mitsubishi Electric Corp.	11/10/1992				
	B78	JP H06104414	Toshiba Corp.	4/15/1994				
	B79	JP H06244444	Hatachi Ltd. (Hammamatsu)	9/2/1994				
	B80	JP H06267868	Fuji Electric Co LTD	9/22/1994				
	B81	JP H06275641	Semiconductor Energy Lab Co. LTD.	9/30/1994				
	B82	JP H07183484	Centre Nat ETD Telecomm	7/21/1995				
	B83	JP H07235658	Sony Corp.	5/9/1995				
	B84	JP H0774240	Nec Corp.	3/17/1995				
	B85	JP H09298308	Sharp KK	11/18/1997				
	B86	JP S57173966	Fuji Photo Film Co. Ltd.	10/26/1982				
	B87	JP S5771188	Mitsubishi Electric Corp.	5/1/1982				
	B88	JP S63116421	Mitsubishi Electric Corp.	5/20/1988				
	B89	KR 100825808	Samsung Electronics CO. Ltd.	4/29/2008				
	B90	KR 20010061058	Hynix Semiconductor Inc.	4/7/2001				
	B91	KR 2005039273	Jin- Sin Lee	4/29/2005				
	B92	KR 20060020400	MAGNACHIP SEMICONDUCTOR LTD	3/6/2006				
	B93	KR 20060052278	Sony Corp.	5/16/2016				
	B94	KR 20080014301	Samsung Elec. Co. Ltd.	2/14/2008				
	B95	KR 20080097709	Dongbu Elec. Co. Ltd.	11/6/2008				
	B96	KR 20090077274	LG Electronics Inc.	7/15/2009				
	B97	KR 20100026463	LG Electronics Inc.	3/10/2010				
	B98	KR 20100118864	Hyosung Corp	11/8/2010				
	B99	KR 20110079323	DONGBU HITEK CO LTD	7/7/2011				
	B100	KR 20170070266	SONY CORP	6/21/2017				
	B101	TW 200627675	Lumileds Lighting U.S. LLC	8/1/2006				
	B102	TW 200818529	Newsouth Innovations PTY. LTD	4/16/2008				
	B103	WO 2003059390	Dong Wha Pharm Ind Co. Ltd	7/24/2003				
	B104	WO 2000031679	Iriscan Inc.	6/2/2000				
	B105	WO 2002041363	Solarflex Technologies Inc.	5/23/2002				

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	B106	WO 2006/086014	President and Fellows of Harvard College	8/17/2006				
	B107	WO 2008091242	UVA Patent Foundation	7/31/2008				
	B108	WO 2008099524	Mitsubishi Heavy Industries Ltd.	8/21/2008				
	B109	WO 2008145097	Fraunhofer-Gesellschaft Zur Faurderung Der Angewandten	12/8/2008				
	B110	WO 2009016846	Panasonic Corp.	2/5/2009				
	B111	WO 2009100023	President and Fellows of Harvard College	8/13/2009				
	B112	WO 2009147085	Thiel et al.	12/10/2009				
	B113	WO 2010033127	Sionyx, Inc.	3/25/2010				
	B114	WO 2011003871	International Business Machines Corporation	1/13/2011				
	B115	WO 2011035188	Sionyx, Inc.	3/24/2011				
	B116	WO 2011119618	Sionyx, Inc.	3/22/2011				
	B117	WO 2012027290	Red.Com, Inc.	3/1/2012				
	B118	WO 2012117931	SONY CORPORATION	9/7/2012				
	B119	WO 2012174752	Boly Media Comm.	12/27/2012				
	B120	WO 2014110484	Digimarc Corp.	7/17/2014				
	B121	WO 91/14284	Theden, Ulrich	9/19/1991				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
Examiner's Initials	**Cite No.**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or county where published**	**T**
	C1	A. Arndt, J.F. Allison, J.G. Haynos, and A. Meulenberg, Jr., "Optical Properties of the COMSAT Non-reflective Cell," 11th IEEE Photovoltaic Spec. Conf., p. 40, 1975	
	C2	Agranov, et al., Pixel continues to shrink….Small Pixels for Novel CMOS Image Sensors, 4 pages.	
	C3	Asom et al., Interstitial Defect Reactions in Silicon; Appl. Phys. Lett.; 07/27/1987; pp. 256-258; vol. 51(4); American Institute of Physics.	
	C4	BERGER, Michael; Moth Eyes Inspire Self-Cleaning Antireflection Nanotechnology Coatings; 2008; 3 pages; Nanowerk LLC	
	C5	Berger, O., Inns, D. and Aberle, A.E. "Commercial White Paint as Back Surface Reflector for Thin-Film Solar Cells", Solar Energy Materials & Solar Cells, vol. 91, pp. 1215-1221,2007.	
	C6	Bernhard, C.G., "Structural and Functional Adaptation in a Visual System" Endevor Vol. 26, pp. 79-84, May 1967	
	C7	Betta et al.; Si-PIN X-Ray Detector Technology; Nuclear Instruments and Methods in Physics Research; 1997; pp. 344-348; vol. A, No. 395; Elsevier Science B.V. cited by applicant.	
	C8	BODEN, S.A. et al.; Nanoimprinting for Antireflective Moth-Eye Surfaces; 4 pages; 2008	
	C9	Bogue: "From bolometers to beetles: the development of the thermal imaging sensors;" sensor Review; 2007; pp. 278-281; Emerald Group Publishing Limited (ISSN 0260-2288).	

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Sheet	19	of	26	Attorney Docket No.:	143705.06021(S)

	C10	Borghesi et al.; "Oxygen Precipitation in Silicon," J. Appl. Phys., v. 77(9), pp. 4169-4244 (May 1, 1995).	
	C11	Born, M. and E.Wolf, "Princip les of Optics, 7th Ed.", Cambridge University Press, 1999, pp. 246-255.	
	C12	Brieger,S., O.Dubbers, S.Fricker, A.Manzke, C.Pfahler, A.Plettl, and P.Zlemann, "An Approach for the Fabrication of Hexagonally Ordered Arrays of Cylindrical Nanoholes in Crystalline and Amorphous Silicon Based on the Self-Organization of Polymer Micelles", Nanotechnology, vol. 17, pp. 4991-4994, 2006, doi:10.1088/0957-4884/17/19/036.	
	C13	Buttgen, B.; "Demodulation Pixel Based on Static Drift Fields"; IEEE Transactions on Electron Devices, vol. 53, No. 11, Nov. 2006.	
	C14	Byung Jun Park et al, Jpn. J. Appl. Phys. 46 2454, 2007, 5 pages.	
	C15	Campbell, Stephen A., "The Science and Engineering of Microeletronic Fabrication, 2nd Ed.", Oxford University Press, 2001, pp. 406-411.	
	C16	Carey et al., "Femtosecond-Laser-Assisted Microstructuring of Silicon Surfaces", Optics and Photonics News, 2003. 14, 32-36.	
	C17	Carey, et al. "Femtosecond Laser-Assisted Microstructuring of Silicon for Novel Detector, Sensing and Display Technologies", LEOS 2003, 481-482, Tuscon, AR.	
	C18	Carey, et al. "Femtosecond Laser-Assisted Microstructuring of Silicon for Novel Detector, Sensing and Display Technologies", LEOS; 2002, 97-98, Glasgos, Scotland, 2002.	
	C19	Carey, et al., "Fabrication of Micrometer-Sized Conical Field Emitters Using Femtosecond Laser-Assisted Etching of Silicon," Proc. IVMC 2001, 75-76, UC Davis, Davis, CA.	
	C20	Carey, et al., "Field Emission from Silicon. Microstructures Formed by Femtosecond Laser Assisted Etching," Proc. CLEO 2001 (Baltimore, MD 2001) 555-557.	
	C21	Carey, et al., "High Sensitivity Silicon-Based VIS/NIR Photodetectors", Optical Society of America (2003) 1-2.	
	C22	CAREY, III; “Femtosecond-laser Microstructuring of Silicon for Novel Optoelectronic Devices”; Harvard University, July 2004; (Thesis)	
	C23	Carey, P.G. et al., "In-situ Doping of Silicon Using Gas Immersion Laser Doping (GILD) Process," Appl. Surf. Sci. 43, 325-332 (1989)	
	C24	Chang, S.W., V.P.Chuang, S.T.Boles, and C.V.Thompson, "Metal-Catalyzed Etching of Vertically Aligned Polysilicon and Amorphous Silicon Nanowire Arrays by Etching Direction Confinement", Advanced Functional Materials, vol. 20, No. 24, pp. 4364-4370, 2010	
	C25	CHEN, Q. et al.; Broadband moth-eye antireflection coatings fabricated by low-cost nanoimprinting; Applied Physics Letters 94; pgs. 263118-1 - 263118-3; 2009; American Institute of Physics	
	C26	CHIANG, Wen Jen Et al., "Silicon Nanocrystal-Based Photosensor on Low-Temperature Polycrystalline-Silicone Panels", Applied Physics Letters, 2007, 51120-1-51120-3, Ltt. 91, American Inst. Of Physics, Melville, NY.	
	C27	CHICHKOV, B.N. et al, "Femtosecond, picosecond and nanosecond laser ablation of solids" Appl. Phys. A 63, 109-115; 1996.	
	C28	Chien et al, "Pulse Width Effect in Ultrafast Laser Processing of Materials," Applied Physics A, 2005, 1257-1263, 81, Springer Berlin, Heidelberg, Germany.	
	C29	Choubey et al., On Evolution of CMOS Image Sensors, Proceedings of the 8th International Conference on Sensing Technology, Sep. 2-4, 2014, Liverpool, UK, pages.	
	C30	CILINGIROGLU et al., "An evaluation of MOS Interface-Trap Charge Pump as and Ultralow Constant-Current Generator," IEEE Journal of Solid-State Circuit, 2003, Vol. 38, No. 1, Jan. 2003, 71-83.	
	C31	Clapham, P.B. et al, "Reduction of Lens Reflexion by the Moth Eye Principle" Nature, Vol 244. Aug. 1973, pp. 281-282	

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Sheet	20	of	26	Attorney Docket No.:	143705.06021(S)

	C32	CMOSIS; "Global Shutter Image Sensors for Machine Vision Application"; Image Sensors Europe 2010, Mar. 23-25, 2010; .COPYRGT. copyright 2010.	
	C33	Cotter, Jeffrey E.; Optical intensity of light in layers of silicon with rear diffuse reflectors; Journal of Applied Physics; Jul. 1, 1998; pp. 618-624; vol. 84, No. 1; American Institute of Physics.	
	C34	Crouch et al., "Comparison of Structure and Properties of Femtosecond and Nanosecond Laser-Structured Silicon" Appl. Phys. Lett., 2004, 84,1850-1852.	
	C35	Crouch et al., "Infrared Absorption by Sulfur-Doped Silicon Formed by Femtosecond Laser Irradiation", Appl. Phys. A, 2004, 79, 1635-1641.	
	C36	Despeisse, et al.; "Thin Film Silicon Solar Cell on Highly Textured Substrates for High Conversion Efficiency"; 2004.	
	C37	Detection of X-ray and Gamma-ray Photons Using Silicon Diodes; Dec. 2000; Detection Technology, Inc.; Micropolis, Finland.	
	C38	DEWAN, Rahul et al.; Light Trapping in Thin-Film Silicon Solar Cells with Submicron Surface Texture; Optics Express; Vol. 17, No. 25; December 7, 2009; Optical Society of America	
	C39	Deych et al.; Advances in Computed Tomography and Digital Mammography; Power Point; Nov. 18, 2008; Analogic Corp.; Peabody, MA	
	C40	Dobie, et al.; "Minimization of reflected light in photovoltaic modules"; Mar. 1, 2009.	
	C41	DOBRZANSKI, L.A. et al.; Laser Surface Treatment of Multicrystalline Silicon for Enhancing Optical Properties; Journal of Materials Processing Technology; page 291 - 296; 2007; Elsevier B.V.	
	C42	Dolgaev et al., "Formation of Conical Microstructures Upon Laser Evaporation of Solids", Appl. Phys. A, 2001, 73, 177-181.	
	C43	Duerinckx, et al.; "Optical Path Length Enhancement for >13% Screenprinted Thin Film Silicon Solar Cells"; 2006.	
	C44	Dulinski, Wojciech et al.; Tests of backside illumincated monolithic CMOS pixel sensor in an HPD set-up; Nuclear Instruments and methods in Physics Research; Apr. 19, 2005; pp. 274-280; Elsevier B.V.	
	C45	Fontaine, A Review of the 1.4 µm Pixel Generation, Technology Analysis Group Chipworks Inc., 2011, 4 pages.	
	C46	Fontaine, Ray, A Survey of Enabling Technologies in Successful Consumer Digital Imaging Products (Part 3: Pixel Isolation Structures), http://www.techinsights.com,July 24, 2017, 13 pages.	
	C47	Forbes, L. and M.Y. Louie, "Backside Nanoscale Texturing to Improve IR Response of Silicon Photodetectors and Solar Cells," Nanotech, vol. 2, pp. 9-12, Jun. 2010.	
	C48	FORBES; “Texturing, reflectivity, diffuse scattering and light trapping in silicon solar cells”; 2012	
	C49	Fowlkes et al., "Surface Microstructuring and Long-Range Ordering of Silicon Nanoparticles", Appl. Phys. Lett., 2002, 80 (20), 3799-3801.	
	C50	Gibbons, J., "Ion Implantation in Semiconductors-Part II; Damage Production and Annealing", proceedings of the IEEE Vol. 60, No. 9 pp. 1062-1096. Jun. 1972.	
	C51	Gjessing, J. et al.; 2D back-side diffraction grating for impored light trapping in thin silicon solar cells; Optics Express; vol. 18, No. 6; pp. 5481-5495; Mar. 15, 2010; Optical Society of America.	
	C52	Gjessing, J. et al.; 2D blazed grating for light trapping in thin silicon solar cells; 3 pages; 2010; Optical Society of America.	
	C53	Gloeckler et al. Band-Gap Grading in CU(In,GA)Se2 Solar Cells, Journal of Physics and Chemistry of Solids; 2005; pages 189-194; vol. 66.	
	C54	Goetzberger, et al.; "Solar Energy Materials & Solar Cells"; vol. 92 (2008) pp. 1570-1578.	
	C55	HAN et al., "Evaluation of a Small Negative Transfer Gate Bias on the Performance of 4T CMOS Image Sensor Pixels," 2007 International Image Sensor Workshop, 238-240, Ogunquit, Maine.	

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Sheet	21	of	26	Attorney Docket No.:	143705.06021(S)

	C56	HAUG, et al.; "Light Trapping effects in thin film silicon solar cells"; 2009	
	C57	Her et al., "Microstructuring of Silicon with Femtosecond Laser Pulses," Applied Physics Letters, 1998, 1673-1675, vol. 73, No. 12, American Institute of Physics.	
	C58	Her et al., "Novel Conical Microstructures Created in Silicon With Femtosecond Laser Pulses", CLEO 1998, 511-512, San Francisco, CA.	
	C59	Her, et al., "Femtosecond laser-induced formation of spikes on silicon," Applied Physics A, 2000, 70, 383-385.	
	C60	HERMANN, S. et al.; Impact of Surface Topography and Laser Pulse Duration for Laser Ablation of Solar Cell Front Side Passivating SiNx Layers; Journal of Applied Physics; Vol. 108, No. 11; pages 114514-1 - 114514-8; 2010; American Institute of Physics	
	C61	High--Performance Technologies for Advanced Biomedical Applications; .COPYRGT. 2004Brochure; pp. 1-46; PerkinElmerOptoelectronics	
	C62	Holland; Fabrication of Detectors and Transistors on High-Resistivity Silicon; Nuclear Instruments and Methods in Physics Research, vol. A275, pp. 537-541 (1989).	
	C63	HONG et al., "Cryogenic processed metal-semiconductor-metal (MSM) photodetectors on MBE grown ZnSe,", 1999, IEEE Transactions on Electron Devices, vol. 46, No. 6, pp. 1127-1134.	
	C64	HSIEH et al., "Focal-Plane-Arrays and CMOS Readout Techniques of Infrared Imaging Systems," IEE Transactions on Circuits and Systems for Video Technology, 1997, vol. 7, no. 4, Aug. 1997, 594-605.	
	C65	http://electroiq.com/insights-from-leading-edge/2016/09/iftle-303-sony-introduces-ziptronix-dbi-technology-in-samsung-galaxy-s7, "Omnivision was the first to sample BSI in 2007 but costs were too high and adoption was thus very low", (2016)	
	C66	http://joseph-tang.blogspot.com/2017/, Oshiyama et al. , Near-infrared Sensitivity Enhancement of a Back-illuminated Complementary Metal Oxide Semiconductor Image Sensor with a Pyramid Surface for Diffraction Structure,(2017)	
	C67	https://blogs.yahoo.co.jp/miyabiman_now/25628945.html	
	C68	Hu et al., "Solar Cells from Basic to Advanced Systems," McGraw Hill Book Co., 1983, 39, New York, New York.	
	C69	Huang, et al.; "Key Technique for texturing a uniform pyramid structure with a layer of silicon nitride on monocrystalline silicon wafer" Applied Surface Science; 2013 pp. 245-249	
	C70	HUANG, et al.; "Microstructured silicon photodetector"; Applied Physics Letters 89, 033506; 2006 American Institute of Physics; 2006	
	C71	HÜPKES, J. et al.; Light Scattering and Trapping in Different Thin Film Photovoltaic Devices; 24th European Photovoltaic Solar Energy Conference, Hamburg, Germany (Sept. 21-25, 2009); pgs. 2766-2769	
	C72	Igalson et al. Defect States in the CIGS Solar cells by Photocapacitance and Deep Level Optical Spectroscopy; Bulletin of the Polish Academy of Sciences Technical Sciences; 2005; pp. 157-161; vol. 53(2).	
	C73	IMEC, 3D INTEGRATED IMAGE SENSORS FOR SMART IMAGING SYSTEMS, PIET DE MOOR, 2010, 32 pages.	
	C74	Itonaga et al., "Extremely-low-noise CMOS Image Sensor with high saturation capacity," 2011 International Electron Devices Meeting, Washington, DC, 2011, pp. 8.1.1-8.1.4.	
	C75	Jansen, H. et al., "The Black Silicon Method: a universal method for determining the parameter setting of a flourine-based reactive ion etcher in deep silicon trench etching with profile control",J. Micromech. Microeng. Vol. 5, 1995 pp.115-120.	
	C76	Job et al., "Doping of Oxidized Float Zone Silincon by Thermal Donors - A low Thermal Budget Doping Method for Device Applications?" Mat. Res. Soc. Symp. Pro.; v. 719, F9.5.1-F9.5.6 (2002).	
	C77	Joy, T. et al.; Development of a Production-Ready, Back-Illuminated CMOS Image Sensor with	

Examiner Signature	/CARIDAD EVERHART/	Date Considered	03/01/2019

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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Sheet	22	of	26	Attorney Docket No.:	143705.06021(S)

		Small Pixels; Electron Devices Meeting; pp. 1007-1010; 2007; IEEE.	
	C78	Juntunen et al.; Advanced Photodiode Detector for Medical CT Imaging: Design and Performance; 2007; pp. 2730-2735; IEEE.	
	C79	KIM et al.; "Strong Sub-Band-Gap Infrared Absorption in Silicon Supersaturated with Sulfur"; 2006 Appl. Phys. Lett. 88, 241902-1 – 241902-3	
	C80	Kitamura et al., "Suppression of crosstalk by using backside deep trench isolation for 1.12μm backside illuminated CMOS image sensor," 2012 International Electron Devices Meeting, San Francisco, CA, 2012, pp. 24.2.1-24.2.4.	
	C81	Koh et al., "Simple nanostructuring on silicon surfaceby means of focused beam patterning and wet etching", Applied Surface Science, 2000 pp. 599-603.	
	C82	Kolasinski et al., "Laser Assisted and Wet Chemical Etching of Silicon Nanostructures," J. Vac. Sci. Technol., A 24(4), Jul/Aug 2006, 1474-1479.	
	C83	Konstantatos et al., "Engineering the Temproal Response of Photoconductive Photodetectors via Selective Introduction of Surface Trap States," Nano Letters, v. 8(5), pp. 1446-1450 (Apr. 2, 2008).	
	C84	Konstantatos et al., "PbS Colloidal Quantum Dot Photoconductive Photodetectors: Transport, Traps, and Gain," Appl. Phys. Lett., v. 91, pp. 173505-1-173505-3 (Oct. 23, 2007).	
	C85	KOREAN INTELLECTUAL PROPERTY OFFICE (KIPO), CMOS Image Sensor, KIPO, 2004, 29 pages.	
	C86	Kray, D. et al.; Laser-doped Silicon Soalr Cells by Laser Chemical Processing (LCP) exceeding 20% Efficiency; 33rd IEEE Photovoltaic Specialist Conference; 3 pages; May 2008; IEEE.	
	C87	Kroning et al.; X-ray Imaging Systems for NDT and General Applications; 2002; Fraunhofer Institute for Nondestructive Testing; Saarbrucken and Dresden, Germany.	
	C88	Kryski; A High Speed 4 Megapixel Digital CMOS Sensor; 2007 International Image Sensor Workshop; Jun. 6-10, 2007.	
	C89	Lee et al., SNR Performance Comparison of 1.4um Pixel : FSI, Light-guide, and BSI, 2011, 3 pages.	
	C90	Li et al., "Gettering in High Resistive Float Zone Silicon Wafers," Transaction on Nuclear Science," vol. 36(1), pp. 290-294 (Feb. 1, 1989).	
	C91	Li, "Design and Simulation of an Uncooled Double-Cantilever Microbolometer with the Potential for .about.mK NETD," 2004, Sensors and Actuators A, 351-359, vol. 112, Elsevier B.V.	
	C92	Li, Hongsong et al.; An experimental study of the correlation between surface roughness and light scattering for rough metallic surfaces; Advanced Characterization Techniques for Optics, Semiconductors, and Nanotechnologies II; 2005; pp. 25780V-1-25780V-15; vol. 5878; SPIE Bellingham, WA.	
	C93	Lin, A. et al.; Optimization of Random Diffraction Gratings in Thin-Film Solar Cells Using Genetic Algorithms; 2007; 1 page; SSEL Annual Report. cited by applicant .	
	C94	Low Dose Technologies; Power Point	
	C95	Madzharov, et al.; "Light trapping in thin-firm silicon solar cells for superstrate and substrate configuration" Abstract #1614, 218.sup.th ECS Meeting .COPYRGT. 2010 the Electrochemical Society.	
	C96	"Masimo Rainbow SET Pulse CO-Oximetry," 2010, Masimo Corporation, Irvine, California, http://www.masimo.com/Rainbow/about.htm.	
	C97	Mateus; C.F.R. et al.; Ultrabroadband Mirror Using Low-Index Cladded Subwavelength Grating; Photonics Technology Letters; vol. 16, Issue No. 2; pp. 518-520; Feb. 2004; IEEE.	
	C98	Matsuno, Shigeru et al.; Advanced Technologies for High Efficiency Photovoltaic Systems; Mitsubishi Electric Advance; vol. 122; pp. 17-19; Jun. 2008	
	C99	Meynants, et al.; "Backside illuminated global shutter COMOS image sensors"; 2011 International Image Sensor Workshop; Jun. 11, 2011.	

Examiner Signature	/CARIDAD EVERHART/	Date Considered	03/01/2019

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
Sheet	23	of	26	Attorney Docket No.:	143705.06021(S)

	C100	Minoglou et al., "Reduction of Electrical Crosstalk in Hybrid Backside Illuminated CMOS Imagers using Deep Trench Isolation," 2008 International Interconnect Technology Conference, Burlingame, CA, USA, 2008, pp. 129-131.	
	C101	MOLONEY, A.M. et al.; Novel Black Silicon PIN Photodiodes; 8 pages; January 25, 2006; SPIE.	
	C102	Moon et al. Selective emitter using porous silicon for crystalline silicon solar cells. Solar Energy Materials & Solar Cells, v. 93, pp. 846-850 (2009).	
	C103	Moses; Nuclear Medical Imaging--Techniques and Challenges; Power Point; Feb. 9, 2005; Lawrence Berkeley National Laboratory Department of Functional Imaging.	
	C104	MUNCK, Generic building blocks for 3D integration and their application on hybrid CMOS image sensors, KATHOLIEKE UNIVERSITEIT LEUVEN, Kapeldreef 75 — B-3001 Heverlee, September 2008, 328 pages.	
	C105	Munday, J.N. et al.; Large Integrated Absorption Enhancement in Plasmonic Solar Cells by Combining Metallic Gratings and Antireflection Coatings; Nano Letters; vol. 11, No. 6; pp. 2195-2201; Oct. 14, 2010; American Chemical Society	
	C106	Murkin, JM and Arangol, M, "Near Infrared spectroscopy as an index of rain and tissue oxygenation," Bri. J. of Anathesia (BJA/PGA Supplement):13-il3 (2009).	
	C107	Myers, Richard et al., "Enhancing Near-IR Avalanche Photodiodes Performance by Femtosecond Laser Microstructuring" Harvard Dept. Of Physics.	
	C108	Nauka et al., "New Intrinsic Gettering Process in Silicon Based on Interactions of Silicon Interstitials," J. App. Phys., vol. 60(2), pp. 615-621, July 15, 1986.	
	C109	Nauka et al., Intrinsic Gettering in Oxygen-Free Silicon; App. Phys. Lett., vol. 46(7), Apr. 4, 1985.	
	C110	Nayak et al, "Semiconductor Laesr Crystallization of a--Si:H," SPIE Digital Library, 2003, 277-380, vol. 4977, Bellingham, Washington. 2003.	
	C111	Nayak et al, "Semiconductor Laser Crystallization of a--Si:H on Conducting Tin-Oxide-Coated Glass for Solar Cell and Display Applications," Applied Physics A, 2005, 1077-1080, 80, Springer Berlin, Heidelberg, Germany	
	C112	Nayak et al, "Ultrafast-Laser-Assisted Chemical Restructuring of Silicon and Germanium Surfaces," Applied Surface Science, 2007, 6580-6583, vol. 253, Issue 15, Elsevier B.V.	
	C113	NAYAK, B.K. et al.; Ultrafast Laser Textured Silicon Solar Cells; Mater. Res. Soc. Symp. Proc.; Vol. 1123; 6 pages; 2009; Materials Research Society	
	C114	NAYAK, et al.; "Efficient light trapping in silicon solar cells by ultrafast-laser-induced self-assembled micro/nano structures"; Progress in Photovoltaics: Research and Applications; 2011	
	C115	Oden, et al.; "Optical and Infrared Detection Using Microcantilevers;" SPIE Digital Library on Oct. 13, 2010; vol. 2744; 10 pages.	
	C116	Ohring, Milton." The Materials of Science of Thin Films"; pp.176-179; Academic Press, 1992.	
	C117	Pain, Bedabrata; "A Back-Illuminated Megapixel CMOS Image Sensor"; http://hdl.handle.net/2014/39312; May 1, 2005	
	C118	Pain, Bedabrata; Backside Illumination Technology for SOI-CMOS Image Sensors; 2009 IISW Symposium on Backside Illujination of Solid-State Image Sensors, Bergen Norway; Jun. 25, 2009; pp. 1-23.	
	C119	Palm et al. CIGSSe Thin Film PB Modules: From Fundamental Investigators to Advanced Performance and Stability; Thin Solid Films; 2004; pp. 544-551; vol. 451-2.	
	C120	Park et al., "Deep Trench Isolation for Crosstalk Suppression in Active Pixel Sensors with 1.7μm Pixel Pitch", in Japanese Journal of Applied Physics, Vol. 46, No. 4B, pp. 2454-5457, 2007	
	C121	Payne, D.N.R. et al.; Characterization of Experimental Textured ZnO:Al Films for Thin Film Solar Cell Applications and Comparison with Commercial and Plasmonic Alternatives; Photovoltaic Specialists Conference (PVSC); pp. 1560-1564; 2010; IEEE.	
	C122	Pedraza et al., "Silicon Microcolumn Arrays Grown by Nanosecond Pulsed-Excimer Laser	

Examiner Signature	/CARIDAD EVERHART/	Date Considered	03/01/2019

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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Sheet	24	of	26	Attorney Docket No.:	143705.06021(S)

		Irradiation", Appl. Phys. Lett., 1999, 74 (16), 2322-2324, American Institute of Physics. cited by applicant .	
	C123	Pedraza et al., "Surface Nanostructuring of Silicon", Appl. Phys. A, 2003, 77, 277-284.	
	C124	Rao, et al., Monolithic and Fully-Hybrid Backside Illuminated CMOS Imagers for Smart Sensing, IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 4 pages.	
	C125	Rashkeev et al., "Hydrogen passivation and Activation of Oxygen Complexes in Silicon," American Institute of Physics, vol. 78(11), pp. 1571-1573 (Mar. 12, 2001).	
	C126	RUSSELL, et al.; "Nanosecond Eximer Laser Processing for Novel Microelectronic Fabrication"; Nanosecond Excimer Laser Processing; 6 pages; 1989	
	C127	Russell, Ramirez and Kelley, "Nanosecond Excimer Laser Processing for Novel Microelectronic Devices," US Navy, SPAWAR, San Diego, Techical Report, 2003.	
	C128	Russell, Ramirez, Kelley, "Nanosecond Excimer Laser Processing for Novel Microelectronic Fabrication," SSC Pacific Technical Reports , pp. 228-233, 2003, vol. 4, US Navy.	
	C129	Sai, H. et al.; Enhancement of Light Trapping in Thin-Film Hydrogenated Microcrystalline Si Solar Cells Using Back Reflectors with Self-Ordered Dimple Pattern; Applied Physics Letters; vol. 93; 2008; American Institute of Physics.	
	C130	Sanchez et al., "Dynamics of the Hydrodynamical Growth of Columns on Silicon Exposed to ArF Excimer-Laser Irradiation ", Appl. Phys. A, 66, 83-86 (1998). cited by other .	
	C131	Sanchez et al., "Whiskerlike Structure Growth on Silicon Exposed to ArF Excimer Laser Irradiation", Appl. Phys. Lett., 1996, 69 (5), 620-622.	
	C132	Sarnet et al.; "Femtosecond laser for black silicon and photovoltaic cells"; February 21, 2008, Proc. Of SPIE; Vol. 6881; pags 1-15	
	C133	Senoussaoui, N. et al.; Thin-Film Solar Cells with Periodic Grating Coupler; Thin Solid Films; pp. 397-401; 2003; Elsevier B.V.	
	C134	Serpenguzel et al., "Temperature Dependence of Photluminescence in Non-Crystalline Silicon", Photonics West (San Jose, CA, 2004) 454-462.	
	C135	Shen et al., "Formation of Regular Arrays of Silicon Micorspikes by Femotsecond Laser Irradiation Through A Mask", Appl. Phys. Lett., 82, 1715-1717 (2003).	
	C136	Solar Energy Research Institute, "Basic Photovoltaic Principles and Methods," Van Nostrand Reinhold Co., NY 1984, pp. 45-47 and 138-142.	
	C137	Solhusvik, J. et al. "A 1280x960 3.75um pixel CMOS imager with Triple Exposure HDR," Proc. of 2009 International Image Sensor Workshop, Bergen, NORWAY, June 22-28, 2009.	
	C138	STMicroelctronics, BSI – technical challenges, IISW-2009, Bergen. 25th June 2009, 37 pages.	
	C139	Stone et al.; The X-ray Sensitivity of Amorphous Selenium for Mammography;.Am. Assoc. Phys. Med.; Mar. 2002; pp. 319-324; vol. 29 No. 3; Am. Assoc. Phys. Med.	
	C140	Szlufcik, J. et al.; Simple Integral Screenprinting process for selective emitter polycrystalline silicon solar cells; Applied Physics Letters; vol. 59, No. 13; Sep. 23, 1991; American Institute of Physics.	
	C141	TABBAL et al., "Formation of Single Crystal Sulfur Supersaturated Silicon Based Junctions by Pulsed Laser Melting". 2007, J. Vac. Sci. Technol. B25(6), 1847-1852	
	C142	Takayanagi, et al.; "A 600.times.600 Pixel, 500, fps CMOS Image Sensor with a 4.4 jum Pinned Photodiode 5-Transistor Global Shutter Pixel"; 2007 International Image Sensor Workshop; Jun. 6-10, 2007.	
	C143	Tournier, et al., Pixel-to-Pixel isolation by Deep Trench technology, STMicroelectronics, 850, rue Jean Monnet – F-38926 Crolles Cedex – France, 2011, 4 pages.	
	C144	Tournier, et al., Pixel-to-Pixel isolation by Deep Trench technology: Application to CMOS Image Sensor, https://www.researchgate.net/publication/268300742, 2011, 5 pages.	
	C145	Tower, John R. et al.; Large Format Backside Illuminated CCD Imager for Space Surveillance; IEEE Transactions on Electron Devices, vol. 50, No. 1; Jan. 2003; pp. 218-224.	

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Sheet	25	of	26	Attorney Docket No.:	143705.06021(S)

	C146	TULL; "Femtosecond Laser Ablation of Silicon: Nanoparticles, Doping and Photovotaics"; Harvard University, June 2007 (Thesis)	
	C147	UEHARA et al., "A High-Sensitive Digital Photosensor Using MOS Interface-Trap Charge Pumping," IEICE Electronics Express, 2004, vol. 1, no. 18, 556-561.	
	C148	Wilson, "Depth Distributions of Sulfur Implanted Into Silicon as a Function of Ion energy, Ion Fluence, and Anneal Temperature," 1984, Appl. Phys. 55(10, 3490-3494.	
	C149	Winderbaum, S. et al.; Reactive ion etching (RIE) as a method for texturing polycrystalline silicon solar cells; Solar Energy Materials and Solar Cells; 1997; pp. 239-248; Elsevier Science B.V.	
	C150	Wu et al., "Black Silicon" Harvard UPS 1999	
	C151	Wu et al., "Black Silicon: A New Light Absorber," APS Centennial Meeting (Mar. 23, 1999).	
	C152	Wu et al., "Femtosecond laser-gas-solid interactions," Thesis presented to the Department of Physics at Harvard University, pp. 1-113, 126-136, Aug. 2000.	
	C153	Wu et al., "Visible Luminescence From Silicon Surfaces Microstructured in Air". Appl. Phys. Lett., vol. 81, No. 11, 1999-2001 (2002).	
	C154	Wu, et al "Near-Unity Below-Band-Gap Absorption by Microstructured Silicon," 2001, Applied Physics Letters, 1850-1852, vol. 78, No. 13, American Institute of Physics.	
	C155	XIONG , Y., et al, "Depth from focusing and defocusing", COMPUTER VISION AND PATTERN RECOGNITION, 1993. PROCEEDINGS CVPR '93., 1993 IEEE , LOS ALAMITOS, CA, USA.IEEE COMPUT. SOC, 15 June 1993 (1993-06-15), pages 68-73,	
	C156	Xu, Y., et al, "Infrared Detection Using Thermally Isolated Diode," Sensors and Actuators A, Elsevier Sequoia S.A., 1993, vol. 36, 209-217, Lausanne, Switzerland.	
	C157	Yablonovitch, et al.; "Intensity Enhancement in Textured Optical Sheets for Solar Cells"; .COPYRGT. 1982 IEEE.	
	C158	YAMAMOTO, K. et al.; NIR Sensitivity Enhancement by Laser Treatment for Si Detectors; Nuclear Instruments and Methods in Physics Research A; pages 520 - 523; March 31, 2010; Elsevier	
	C159	Yan, B.; Light Trapping Effect from Randomized Textures of Ag/ZnO Back Reflector on Hyrdrogenated Amorphous and Nanocrystalline Silicon Based Solar Cells; Thin Film Solar Technology II; vol. 7771; 2010; SPIE.	
	C160	Yasutomi, et al.; "Two-Stage Charge Transfer Pixel Using Pinned Diodes for Low-Noise Global Shutter Imaging"; 2009 International Image Sensor Workshop; Mar. 28, 2009.	
	C161	Yaung et al., "High performance 300mm backside illumination technology for continuous pixel shrinkage," 2011 International Electron Devices Meeting, Washington, DC, 2011, pp. 8.2.1-8.2.4.	
	C162	Younkin et al., "Infrared Absorption by Conical Silicon Microstructures Made in a Variety of Background Gases Using Femtosecond-Laser Pulses", J. Appl. Phys., 93, 2626-2629 (2003).	
	C163	Younkin, "Surface Studies and Microstructure Fabrication Using Femtosecond Laser Pulses," Thesis presented to the Division of Engineering & Applied sciences at Harvard University (Aug. 2001).	
	C164	YUAN, et al.; "Efficient black silicon solar cell with a density-graded nanoporous surface: Optical properties, performance limitations, and design rules"; American Institute of Physics; Applied Physics Letters 95. 1230501 (2009) 3 pages	
	C165	Zaidi, S.H. et al.; Diffraction Grating Structures in Solar Cells; Photovoltaic Specialists Conference, 2000; 4 pages; Sep. 2000; IEEE.	
	C166	Zhang et al, "Ultra-Shallow P+-Junction Formation in Silicon by Excimer Laser Doping: a Heat and Mass Transfer Perspective," Int. J. Heat Mass Transfer, 1996, 3835-3844, vol. 39, No. 18, Elsevier Science Ltd., Great Britain.	
	C167	Zhong, S. et al. "Excellent Light Trapping in Ultrathin Solar Cells," AFM-Journal, May 2016 pp.	

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Sheet	26	of	26	Attorney Docket No.:	143705.06021(S)

		1-11.	
	C168	Zhu et al., "Evolution of Silicon Surface Microstructures by Picosecond and Femtosecond Laser Irradiations," Applied Surface Science, 2005, 102-108, Elsevie, Amsterdam, NL.Ultra-Shallow P+-Junction Formation in Silicon by Excimer Laser Doping: a Heat and Mass Transfer Perspective," Int. J. Heat Mass Transfer, 1996, 3835-3844, vol. 39, No. 18, Elsevier Science Ltd., Great Britain.	
	C169	Ziou et al., "Depth from defocus using the hermite transform", IMAGE PROCESSING, 1998. ICIP 98. Intl. Conference on Chicago, IL. October 1998 pp. 958 - 962.	

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		semiconductor))) and ((optoelectronic or photosensor or sensor or photosensitive) and (imager or imaging)))	DERWENT; IBM_TDB			
L13	25	9 or 10 or 11 or 12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/01 11:11
L14	24	7 AND ((H01L27/14629 OR H01L27/14625 OR H01L27/14643 OR H01L27/1463 OR H01L31/0236 OR H01L31/028 OR H01L31/02327).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/01 11:18

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	51	HADDAD-HOMAYOON	US-PGPUB; USPAT	OR	ON	2019/03/01 10:23
L2	38	JIANG-JUTAO	US-PGPUB; USPAT	OR	ON	2019/03/01 10:23
L3	6	(1 or 2) and (((nanostructure$2 or concavities or nanotrenches or textur$4 or nanotextur$4) near8 (oxide or "sio.sub.2" or insulat$4 or dielectric)) same ((wafer or substrate) near6 (si or silicon or semiconductor))).clm.	US-PGPUB; USPAT	OR	ON	2019/03/01 10:27
L4	243	(((nanostructure$2 or concavities or nanotrenches or textur$4 or nanotextur$4) near8 (oxide or "sio.sub.2" or insulat$4 or dielectric)) same ((wafer or substrate) near6 (si or silicon or semiconductor))).clm.	US-PGPUB; USPAT	OR	ON	2019/03/01 10:28
L5	24	4 and ((optoelectronic or photosensor or sensor or photosensitive) and (imager or imaging))	US-PGPUB; USPAT	OR	ON	2019/03/01 10:30

3/1/2019 11:20:24 AM

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

136549 7590 03/07/2019

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/614,256	06/05/2017	Homayoon Haddad	143705.06021	4345

TITLE OF INVENTION: SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	06/07/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
EVERHART, CARIDAD	2895	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Pepper Hamilton LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Sionyx, LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Beverly, Massachusetts

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 500436

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Alison L. McCarthy/ Date May 24, 2019

Typed or printed name Alison L. McCarthy Registration No. 51998

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

SAMSUNG EX. 1002 - 1671/1684

Electronic Patent Application Fee Transmittal

Application Number:	15614256
Filing Date:	05-Jun-2017
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Filer:	Alison L. McCarthy
Attorney Docket Number:	143705.06021

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	36108991
Application Number:	15614256
International Application Number:	
Confirmation Number:	4345
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	136549
Filer:	Alison L. McCarthy
Filer Authorized By:	
Attorney Docket Number:	143705.06021
Receipt Date:	24-MAY-2019
Filing Date:	05-JUN-2017
Time Stamp:	13:31:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	052819INTEFSW13324100
Deposit Account	500436
Authorized User	Sharon Calhoun

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.20 (Post Issuance fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	143705-6021-Issue-Fee-Transmittal.pdf	88550 9be59ce3e7d319e9a04ee63de659c9b9708122ed	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30229 f8010e1644be0730af5dbd2f7ee5b0872350 6c1a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	118779		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	15/614,256
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	06-05-2017
				First Named Inventor:	Homayoon Haddad
				Group Art Unit:	2895
(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
Sheet	7	of	26	Attorney Docket No.:	143705.06021(S)

	A256	8013411	Cole	9/6/2011		
	A257	8030726	Sumi	10/4/2011		
	A258	8035343	Seman Jr.	10/11/2011		
	A259	8058615	McCaffrey	11/15/2011		
	A260	8076746	McCarten et al.	12/13/2011		
	A261	8080467	Carey et al.	12/20/2011		
	A262	8088219	Knerer et al.	1/3/2012		
	A263	8093559	Rajavel	1/10/2012		
	A264	8164126	Moon, et al.	4/24/2012		
	A265	8207051	Sickler et al.	6/26/2012		
	A266	8247259	Grolier et al.	8/21/2012		
	A267	8259293	Andreou et al.	9/4/2012		
Change(s) applied to document, /J.M./ 4/15/2019	A268	8268403	Akiyama et al	~~4/30/2007~~ 09/2012		
	A269	8288702	Veeder	10/16/2012		
	A270	8355545	Corcoran et al.	1/15/2013		
	A271	8445950	Iida et al	5/21/2013		
	A272	8445985	Hiyama et al	5/21/2013		
	A273	8456546	Oike	6/4/2013		
	A274	8470619	Bour	6/1/2013		
	A275	8476681	Haddad et al.	7/2/2013		
	A276	8530264	De Munck et al	9/10/2013		
	A277	8564087	Yamamura et al.	10/22/2013		
	A278	8603902	Mazur et al.	12/10/2013		
	A279	8604405	Liu et al	12/10/2013		
	A280	8629485	Yamamura et al.	1/14/2014		
	A281	8649568	Sato	2/11/2014		
	A282	8680591	Haddad et al.	3/25/2014		
	A283	8729678	Shim et al	5/20/2014		
	A284	8742528	Yamamura et al.	6/3/2014		
	A285	8884226	Miyazaki, et al.	11/11/2014		
	A286	8906670	Gray	12/1/2014		
	A287	8916945	Sakamoto et al	12/23/2014		
	A288	8928784	Watanabe et al	1/6/2015		
	A289	8994135	Yamamura et al.	6/31/2015		
	A290	9064762	Yamaguchi	6/23/2015		
	A291	9184204	Hu	11/10/2015		
	A292	9190551	Yamamura et al.	11/17/2015		
	A293	9369641	Hu	6/14/2016		
	A294	9419159	Sakamoto et al.	8/16/2016		
	A295	9478572	Miyanami	10/25/2016		
	A296	9659984	Ohkubo et al	5/23/2017		
	A297	20010017344	Aebi	8/30/2001		
	A298	20010022768	Takahashi	9/20/2001		
	A299	20010044175	Barret et al.	11/22/2001		

Examiner Signature	/CARIDAD EVERHART/	Date Considered	03/01/2019

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.E/

Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	15/614,256
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	06-05-2017
				First Named Inventor:	Homayoon Haddad
				Group Art Unit:	2895
(use as many sheets as necessary)				Examiner Name:	Caridad Everhard
Sheet	2	of	6	Attorney Docket No.:	143705.06021(H)

	A36	6876003	Nakamura et al.	4/5/2005		
	A37	6897118	Poon et al.	5/24/2005		
	A38	7112545	Railkar et al.	9/1/2006		
Change(s) applied to document, /J.M./ 4/15/2019	A39	7211214	Chou	~~10/28/3301~~ 05/2007		
	A40	7413909	Hutchens et al.	8/1/2008		
	A41	7425471	Bruland et al.	9/1/2008		
	A42	7569503	Pan	8/4/2009		
	A43	7586601	Eb stein	9/8/2009		
	A44	7605064	Kizilyalli et al.	10/1/2009		
	A45	7629234	Bruland	12/1/2009		
	A46	7687740	Bruland et al.	3/1/2010		
	A47	7935941	Bruland et al.	5/1/2011		
	A48	8698272	Vineis	4/15/2014		
	A49	9276143	Mazur	3/1/2016		
	A50	9559215	Ahmed	1/31/2017		
	A51	20010044251	Cho et al.	11/1/2001		
	A52	20020034845	Fujimura et al.	3/21/2002		
	A53	20020126333	Hosono et al.	9/12/2002		
	A54	20020176650	Zhao et al.	11/28/2002		
	A55	20030016708	Albrecht et al.	1/23/2003		
	A56	20030024269	Shepard et al.	2/6/2003		
	A57	20030025156	Y amazaki et al.	2/6/2003		
	A58	20030045074	Seibel et al.	3/6/2003		
	A59	20030132449	Hosono et al.	7/17/2003		
	A60	20030183270	Falk et al.	10/2/2003		
	A61	20040169834	Richter et al.	9/2/2004		
	A62	20050032249	Im et al.	2/10/2005		
	A63	20050226287	Shah et al.	10/13/2005		
	A64	20050227457	Kondo et al.	10/13/2005		
	A65	20060102901	Im et al.	5/18/2006		
	A66	20060231853	Tanaka	10/19/2006		
	A67	20070102709	Burgener et al.	5/10/2007		
	A68	20070131275	Kinsey et al.	6/14/2007		
	A69	20070243701	Ito et al	10/18/2007		
	A70	20070293056	Setsuhara et al.	12/20/2007		
	A71	20080135099	Yu	6/12/2008		
	A72	20090151785	Namn et al.	6/18/2009		
	A73	20090179199	Sano et al	7/16/2009		
	A74	20100171948	Mazur et al.	7/8/2010		
	A75	20100190292	Alberts	7/29/2010		
	A76	20100213582	Coullard et al.	8/26/2010		
	A77	20170141258	McFarland	5/18/2017		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.E/

Examiner Signature	/CARIDAD EVERHART/	Date Considered	03/01/2019

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.E/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/614,256	07/09/2019	10347682	143705.06021	4345

136549 7590 06/19/2019

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

SiOnyx, LLC, Beverly, MA;
Homayoon Haddad, Beaverton, OR;
Jutao Jiang, Tigard, OR;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	15/614,256
Filing Date	05-Jun-2017
First Named Inventor	Homayoon HADDAD
Title	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
Art Unit	
Examiner Name	
Attorney Docket Number	143705.000366

SIGNATURE of Applicant or Patent Practitioner

Signature	/Gunnar G. Leinberg/	Date (Optional)	2022-09-01
Name	Gunnar G. Leinberg	Registration Number	35,584
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 11951

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

SiOnyx, LLC

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Steven D. Saylor		
Title	President and CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	46534937
Application Number:	15614256
International Application Number:	
Confirmation Number:	4345
Title of Invention:	SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	136549
Filer:	Gunnar G. Leinberg/Mary Frances Heeks
Filer Authorized By:	Gunnar G. Leinberg
Attorney Docket Number:	143705.06021
Receipt Date:	01-SEP-2022
Filing Date:	05-JUN-2017
Time Stamp:	13:28:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	20220901_Corrected_POA_with_Transmittal_143705_000366.pdf	328407 e275dea4dcb5372fd49b943f7e0bac002f4300bd	no	2

Warnings:

Information:	
Total Files Size (in bytes):	328407

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/614,256	06/05/2017	Homayoon Haddad	143705.06021

CONFIRMATION NO. 4345

POWER OF ATTORNEY NOTICE

136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

OC000000136285650

Date Mailed: 09/16/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/01/2022.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ylueng/

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/614,256	06/05/2017	Homayoon Haddad	143705.000366

CONFIRMATION NO. 4345

POA ACCEPTANCE LETTER

11951
Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625

OC000000136285654

Date Mailed: 09/16/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/01/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ylueng/

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