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PROVISIONAL APPLICATION FOR PATENT COVER SHEET – Page 1 of 2

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Susan	Alie	Beverly, MA
<i>Additional inventors are being named on the _____ separately numbered sheets attached hereto.</i>		
TITLE OF THE INVENTION (500 characters max):		
Substrates and Devices for Enhanced Light Detection and Methods of Making the Same		
CORRESPONDENCE ADDRESS		
<i>Direct all correspondence to:</i> ☒ The address corresponding to Customer Number: 20,551		
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ENCLOSED APPLICATION PARTS (check all that apply)		
☐ Application Data Sheet. See 37 CFR 1.76 ☐ CD(s), Number of CDs _____		
☒ Drawing(s) <i>Number of Sheets</i> <u>8</u> ☐ Other (specify) _____		
☒ Specification (e.g. description of the invention) <i>Number of Pages</i> <u>7</u>		
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☒ A check or money order made payable to the <i>Director of the United States Patent and Trademark Office</i> is enclosed to cover the filing fee and application size fee (if applicable).		110
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PROVISIONAL APPLICATION COVER SHEET
Page 2 of 2

PTO/SB/16 (12-08)

Approved for use through 06/30/2010. OMB 0651-0032

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SIGNATURE /Todd B. Alder/ Date March 24, 2010

TYPED or PRINTED NAME Todd B. Alder, Ph.D. REGISTRATION NO. 54598
(if appropriate)

TELEPHONE (801) 566-6633 Docket Number: 3035-013.PROV

SUBSTRATES AND DEVICES FOR ENHANCED LIGHT DETECTION AND METHODS OF MAKING THE SAME

TECHNICAL FIELD

The present disclosure relates to substrates, devices and methods for enhanced light detection. More specifically, the present invention relates to devices having a textured surface disposed within a semiconductor substrate that can enhance infrared light detection and methods of making the same.

BACKGROUND

Semiconductor on Insulator (SOI) wafer technology is an outgrowth of MicroElectroMechanical Systems (MEMS) technologies. An SOI wafer is a stacked wafer substrate where a device wafer (typically silicon) is bonded to a dielectric layer that is bonded to a support wafer, otherwise known as a handle wafer. The process flow for the fabrication of SOI wafers can be as follows: Two wafers are polished and coated with an oxide or other dielectric material. The wafers are mounted polished side face to face and bonded under high temperature and pressure. Then one of the two wafers is ground down using mechanical grinding and chemical mechanical polishing to a specific thickness. In this way it is possible to generate semiconductor wafers that are electrically isolated from the underlying substrate.

This approach is commonly utilized in applications where thin semiconductor device layers are required. More recently, these wafer architectures have been utilized for the development and fabrication of image sensors using Backside Illuminated (BSI) architectures. BSI is an image sensor architecture where Complementary Metal-Oxide Semiconductor (CMOS) circuitry is fabricated on one side of a wafer and photodetectors are fabricated on the opposite side of the wafer such that the photodetectors cover virtually all of the available surface area (i.e. high fill factor). State of the art BSI image sensors are fabricated using the SOI approach because they provide an excellent low defect substrate upon which to fabricate the CMOS circuitry. Once the CMOS processing is complete, the wafer can be flipped over and ground down without imparting significant damage to the wafer due to the isolation of the buried dielectric. The mechanical thinning process can stop

on the dielectric and then chemical etching can fully reveal the device layer semiconductor material.

SUMMARY

The following disclosure provides semiconductor structures and devices with enhanced light detection properties. In such a semiconductor structure, a silicon layer, laser processed layer, dielectric layer, and a handle wafer layer can be included. In addition, a polysilicon material can further be included in the structure.

Devices that can be formed from such a device may include photodiodes and CMOS imagers. Notably, the difference between structure, photodiode and imager are the photodiode junctions, contacts and circuitry for making the structures into devices. Such devices are able to absorb wavelengths in the infrared spectrum (i.e. greater than 1000nm). Methods for making such structures and devices are also disclosed by the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

For a further understanding of the nature and advantage of the present invention, reference is being made to the following detailed description of preferred embodiments and in connection with the accompanying drawings, in which:

Fig. 1 is a cross-sectional view of a semiconductor structure in accordance with an embodiment of the present invention;

Fig. 2 is a cross-sectional view of a semiconductor structure according to another embodiment of the present invention;

Fig. 3 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present invention;

Fig. 4 is a cross-sectional view of a semiconductor photodiode according to one embodiment of the present invention;

Fig. 5 is a cross-sectional view of a semiconductor photodetecting imager according to one embodiment of the present invention;

Figs. 6a – d are steps showing a cross-sectional view of a semiconductor structure being formed according to another embodiment of the present invention;

Figs. 7a – e are steps illustrating a cross-sectional view of a semiconductor structure being formed according to one embodiment of the present invention;

Fig. 8 is a cross-sectional view of a semiconductor photodetecting imager according to another embodiment of the present invention;

Fig. 9 is a cross-sectional view of a semiconductor structure according to another embodiment of the present invention.

Fig. 10a – e are steps illustrating the formation of a semiconductor structure according to yet another embodiment of the present invention.

DETAILED DESCRIPTION

The present invention seeks to improve the light detection of silicon photosensing devices by utilizing a SOI wafer with an enhanced absorbing layer located within the semiconductor structure. This device and method of manufacture provides a low cost and ease of integration approach for the fabrication and application of laser processed silicon for the enhancement of image sensors and photodetectors. It has been demonstrated previously that ultrafast laser processed silicon enhances the spectral bandwidth, absorption and quantum efficiency of silicon. This invention improves on the performance of photodetectors and imagers that use a laser processed layer by improving on the architecture of the device. Furthermore, the device invention has additional benefits such as significantly improving the process integration of this device architecture with traditional CMOS process flows. For example, the design of a laser processed region located on the back surface of a photodetector provides significant performance benefits. The laser processed layer can have surface features also known as surface roughness. The laser processed layer can be substituted for a textured layer or an otherwise enhanced absorbing layer created by many known methods, including photolithography, wet or dry etches, such as isotropic or anisotropic etches, nanoimprinting, and material deposition. The roughened surface can lead to higher recombination of photocarriers for short wavelengths (in the blue green part of the spectrum) due to the very shallow penetration of those wavelengths into the detecting volume. Therefore, by physically locating the laser processed layer on the back surface a pristine surface is provided for the collection of short wavelengths on the top surface (light incident surface) and the longer wavelengths that penetrate deep into or through the detecting volume are collected by or with the help of the laser processed layer on the back surface. While aspects are contemplated for use in backside illumination architectures,

aspects are also contemplated that utilize front side illuminated architectures that will greatly benefit from the semiconductor structures according to aspects of the present invention. The use of the SOI wafer structure can reduce the negative effects of the laser processed layer on the backside of a thin device layer.

Figure 1 illustrates a cross-sectional view of a semiconductor structure 100 with enhanced light detection according to one embodiment of the present invention. The semiconductor structure can include a silicon layer 104 disposed on top of a laser processed layer 106. In one embodiment, the laser processed layer can be a Black Silicon layer. In another embodiment, the semiconductor layer can have a grown epitaxial layer 102 on top of the silicon layer 104 with specific material specifications suitable for CMOS processing. The laser processed layer can be disposed on a dielectric layer 108. The dielectric layer can be disposed on a semiconductor handle wafer 110 that acts as a substrate to support the entire structure. In another embodiment the semiconductor handle wafer can alternatively be comprised of a suitable dielectric material like glass.

In another embodiment, the laser processed material can be located below the dielectric layer rather than above it as shown in Figure 2. In this configuration, the laser processed material does not electrically interact with the photodetector device (or imager device). The laser processed region can act as an optical scattering reflector for the photons that reach this surface. By scattering the photons back into the bulk silicon, the chance for absorption can be increased.

In another embodiment a dielectric layer 108 and a polysilicon layer 112 are inserted between the laser processed layer 106 and the dielectric, as shown in Figure 3. The addition of these layers provides an improved method of manufacture. The rough surface of the laser processed material presents a challenging surface for wafer bonding. By depositing a thin dielectric layer followed by a thick polysilicon layer it is possible to yield a surface that can be polished. The polysilicon can be ground back to a planar surface and polished until smooth. The resultant surface can then be bonded to a dielectric coated handle wafer.

Figures 4 and 5, depict other embodiments of the present invention. Figure 4 shows a cross-sectional view of a photodiode with enhanced light detection performance. Figure 5 shows a cross-sectional view of a CMOS image sensor having improved light detection performance. The actual contacts 114, photodiode junctions 116, and circuitry 118, can be fabricated on the top surface of the semiconductor silicon layer 104. The silicon can include

a laser processed layer 106, all of which can be disposed on a dielectric material 108 being bonded to a semiconductor handle layer 110. In this configuration, all of the CMOS circuitry 118 can be fabricated on the top surface of the multilayer stack substrate. In this way, the laser processed layer can be introduced into fabrication process at the start of the flow, at a lower cost and lower technical risk approach. In this embodiment the laser processed material can be encapsulated deep within the silicon substrate. This reduces the risk of contamination for process integration with standard CMOS process equipment.

In another embodiment a method of manufacture is illustrated in Figures 6a – d. The process flow can begin with the laser processing of a silicon wafer 104 to create a laser processed region 106. A dielectric material 108 can be deposited on to the laser processed layer as shown in figure 6b. Subsequently, the dielectric material can be polished until smooth. The semiconductor structure can then be bonded to a second wafer, the handle wafer 110, with the dielectric layer in contact with the second wafer as shown in figure 6c. In another embodiment the second wafer can be coated with a dielectric. After bonding the wafers together, the device wafer can be mechanically polished and chemical-mechanical polished to a specified thickness. In another embodiment an epitaxial layer 102 of silicon can be grown on the device wafer surface to generate a low defect silicon region as illustrated in figure 6d.

Figures 7a – e illustrate a process flow having a similar starting point as figures 6a and 6b. In this embodiment a polysilicon material 112 can be deposited on the dielectric material 108 as shown in Figure 7c. It should be understood that an alternative semiconductor or dielectric can be substituted for the polysilicon layer. Subsequently, the silicon layer can be thinned to a desired thickness as evidenced by comparing figures 7d to 7e.

A manufacturing process for a detector or imaging device is also contemplated herein. The process can start with a substrate described above and processing that substrate through a standard CMOS image sensor or detector process flow.

In another embodiment a semiconductor structure as disclosed herein can be bisected by dielectric material 120 to electrically isolate each pixel (detector) element from its neighbor, this is commonly referred to by those skilled in the art as trench isolation as shown in Figure 8. The isolation can be fabricated at the substrate level prior to fabrication of the CMOS circuitry, the detector device, or the imaging array. The cross section view in figure 8

is shows a device with a dielectric isolation. The method of manufacture for this device cross section follows the mainline process for the SOI wafer with the integrated laser processed material as described above. At the conclusion of this process, the device layer surface (with or without an epitaxial layer) can be photolithographically patterned thereby the silicon layer can be vertically etched down to the dielectric layer. Dielectric material can be deposited conformally on all surfaces and fill the trenches with the dielectric material. Finally, the device layer surface can be chemically etched or mechanically polished to remove the dielectric material on the front surface. It should also be understood that the trench isolation does not need to fully bisect the semiconductor structure but rather only a portion can be isolated, this is known as shallow trench isolation as opposed to deep trench isolation. In addition, the above described dielectric isolation between elements geometry can be applied to all of the different layer structures shown in Figures 1 to 5 and 9.

In another embodiment, an epitaxial grown semiconductor material with a laser processed region can be used instead of standard silicon as shown in Figure 9. In figure 9, an epitaxial semiconductor layer 102 can include a laser processed layer 106. The laser processed layer can be disposed on about a dielectric layer 108 which can subsequently be bonded to a handle wafer layer 110. The process to achieve such a device or semiconductor structure is shown in Figures 10a – e.

In figure 10a a silicon material can be epitaxial grown on a silicon material 104. Then the laser process layer 106 can be formed on or near the surface of the epitaxial layer. Further, a dielectric material 108 can be deposited on the laser processed layer 106. The wafer can then be flipped over and bonded to a handle wafer 110. Then the device layer wafer can be mechanically and chemical-mechanical grinding and polishing down to the epitaxial layer until the desired thickness is achieved. In this way, the standard silicon material is removed and the epitaxial material remains in the device layer. This can be beneficial because no defects that remain from the laser would be transferred or grown into the epitaxial layer when grown.

ABSTRACT

Semiconductor structures and devices with enhanced infrared light detecting properties are disclosed. In particular, the present invention teaches using a semiconductor on insulator (SOI) material and laser processed silicon layers to create such a device. Methods and process flows for making such a device is also disclosed.

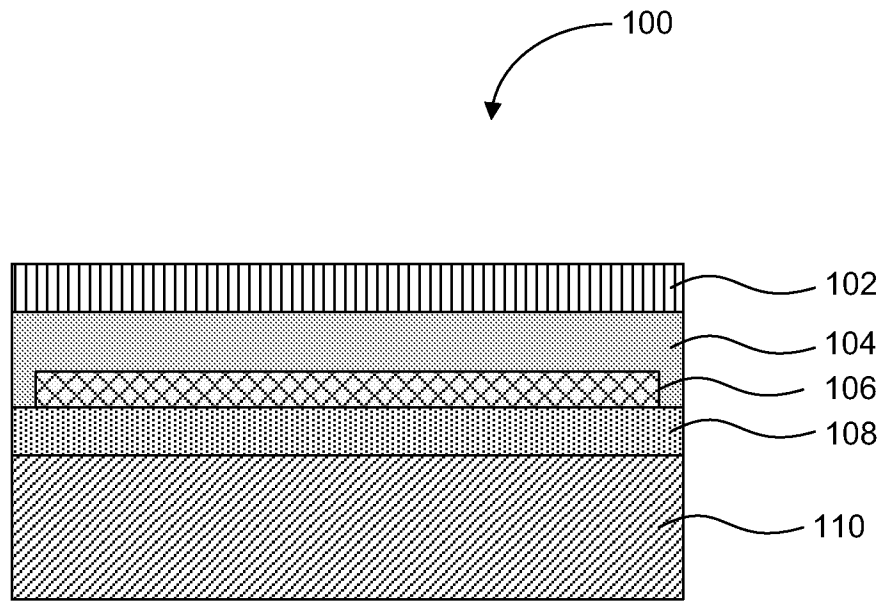


FIG. 1

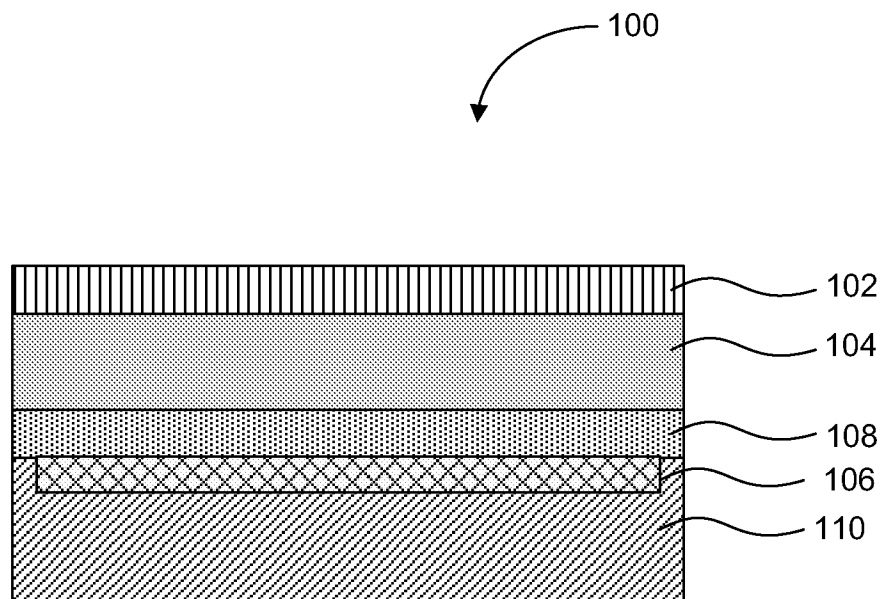


FIG. 2

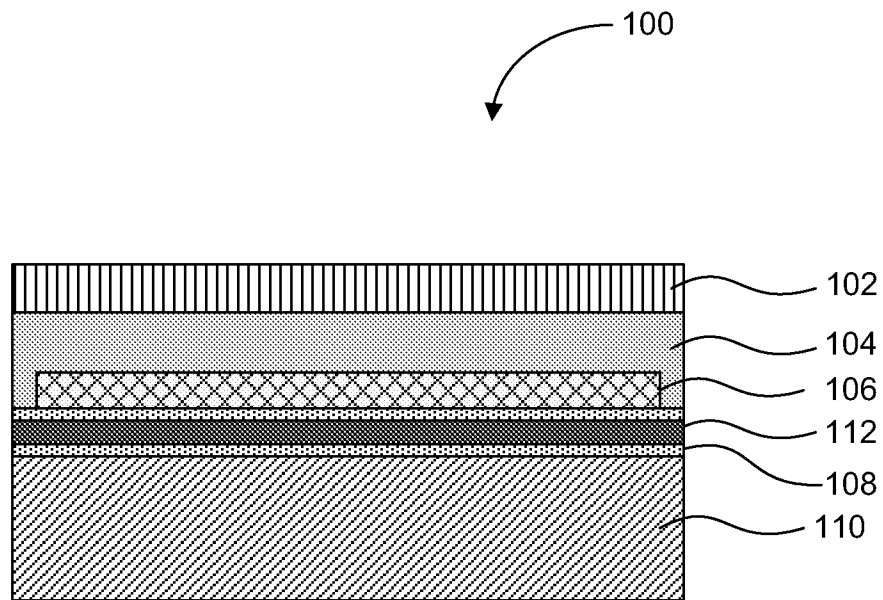


FIG. 3

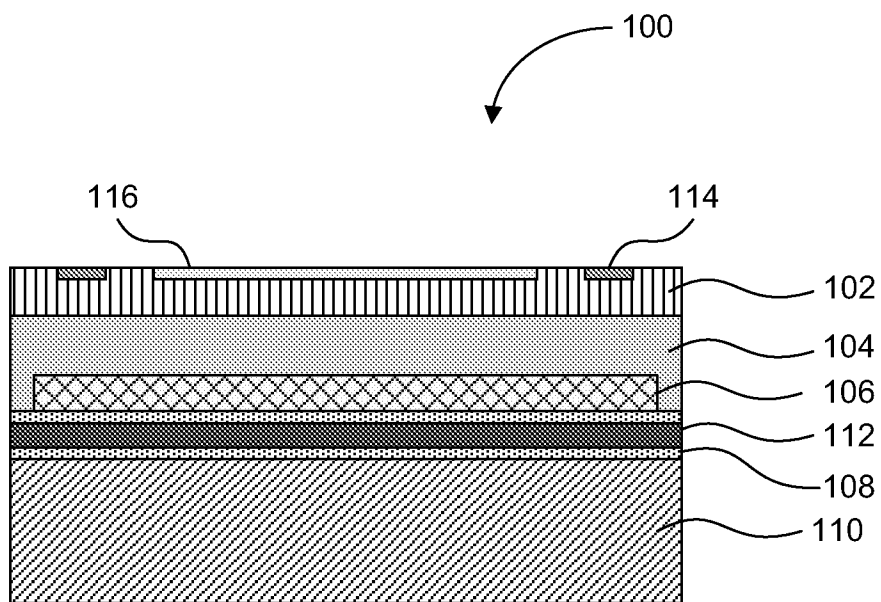


FIG. 4

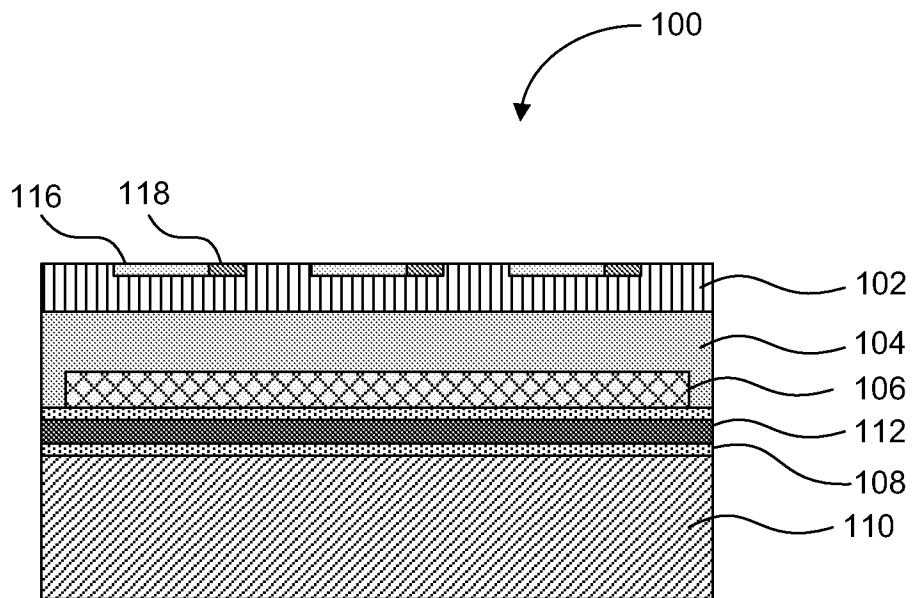


FIG. 5

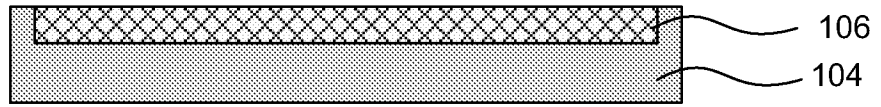


FIG. 6a

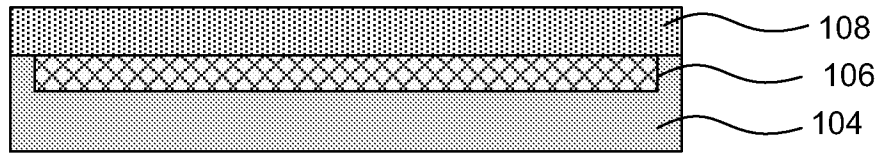


FIG. 6b

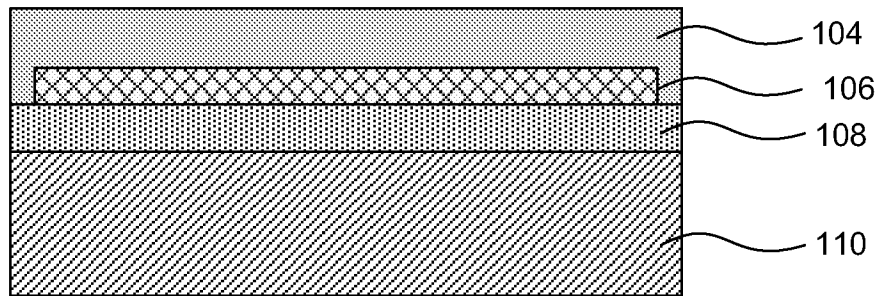


FIG. 6c

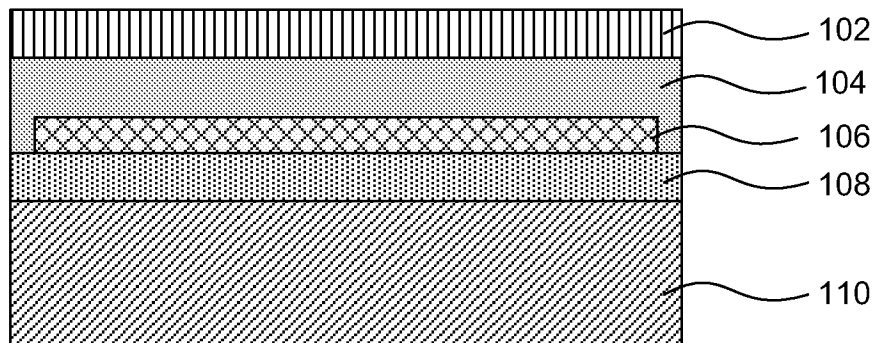


FIG. 6d

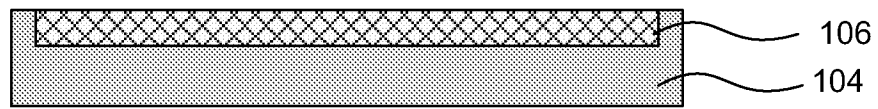


FIG. 7a

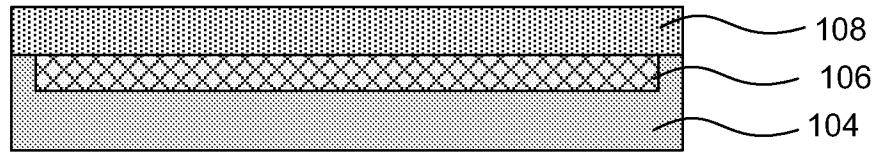


FIG. 7b

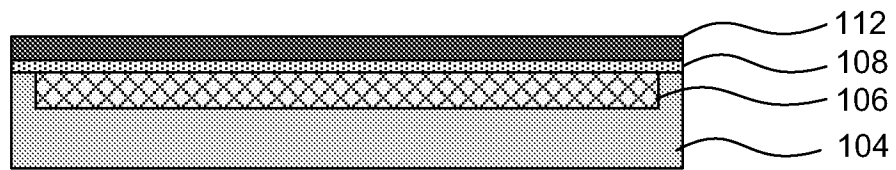


FIG. 7c

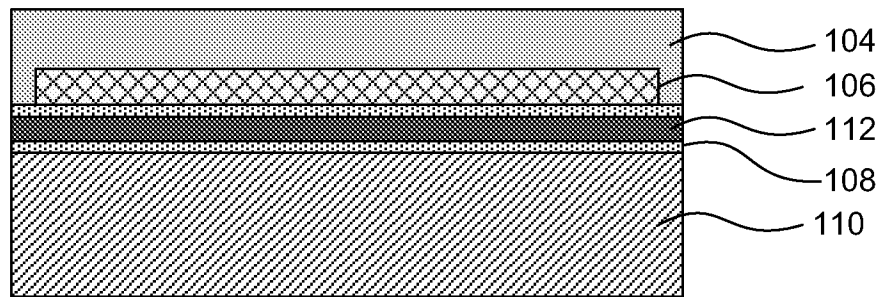


FIG. 7d

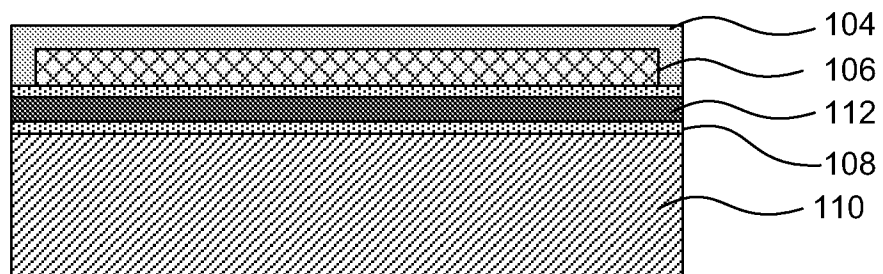


FIG. 7e

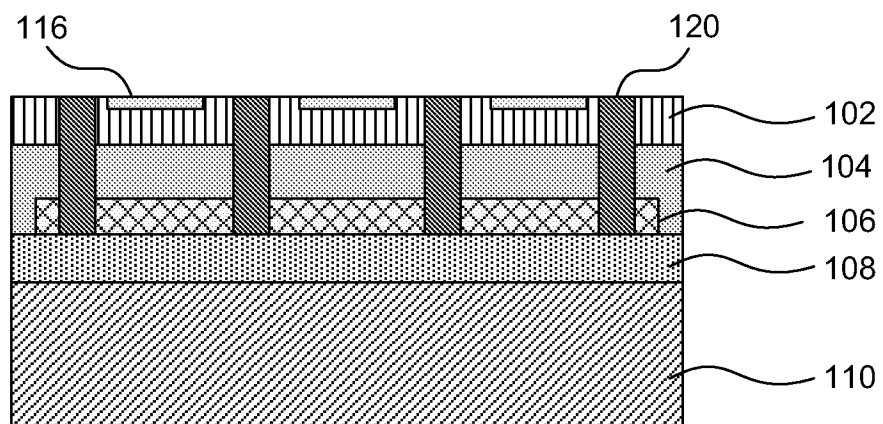


FIG. 8

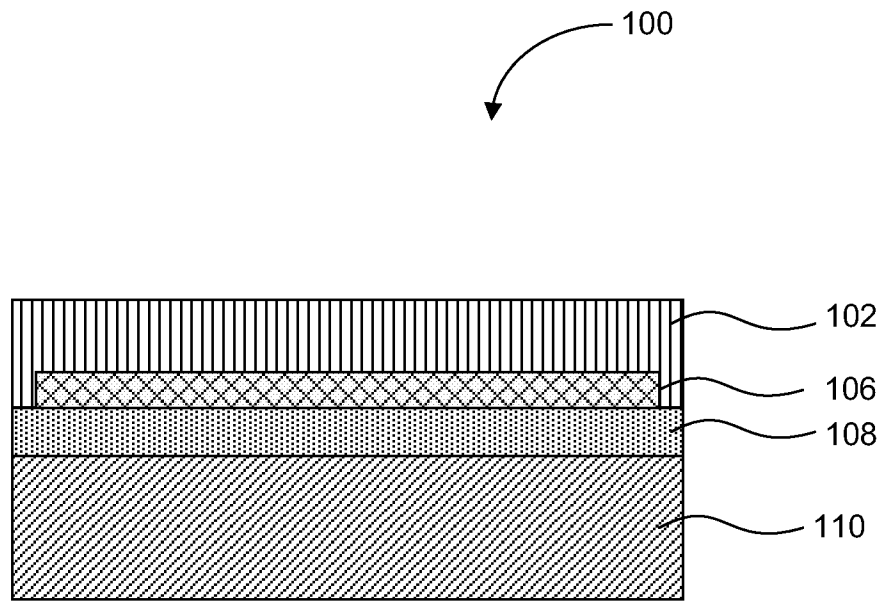


FIG. 9

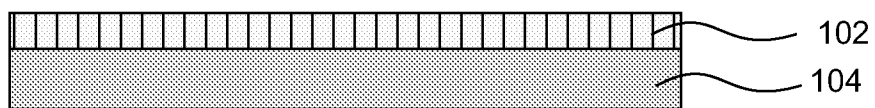


FIG. 10a

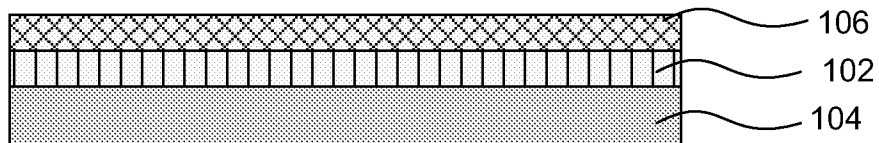


FIG. 10b

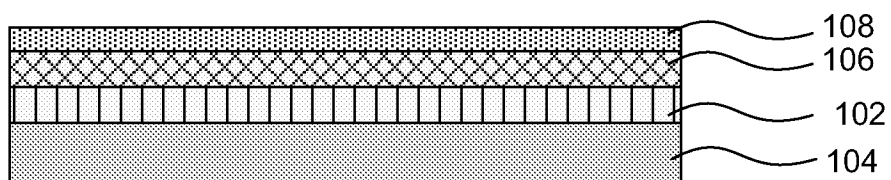


FIG. 10c

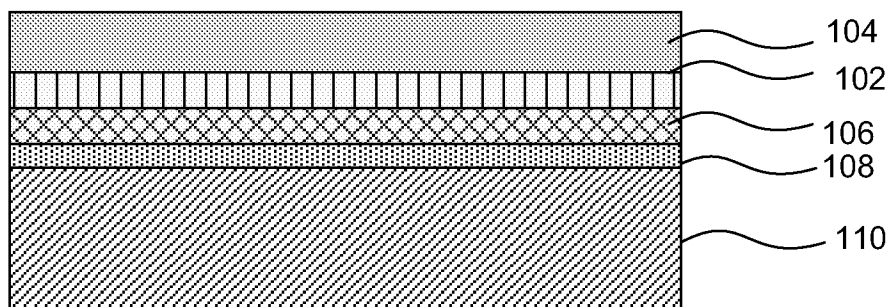


FIG. 10d

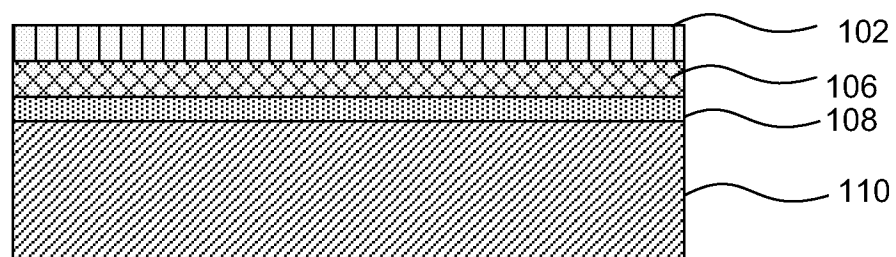


FIG. 10e

Electronic Patent Application Fee Transmittal

Application Number:

Filing Date:

Title of Invention:

Substrates and Devices for Enhanced Light Detection and Methods of Making the Same

First Named Inventor/Applicant Name:

Susan Alie

Filer:

Todd Brent Alder/Nicole Solomon

Attorney Docket Number:

3035-013.PROV

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Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				110

Electronic Acknowledgement Receipt

EFS ID:	7279248
Application Number:	61317147
International Application Number:	
Confirmation Number:	1150
Title of Invention:	Substrates and Devices for Enhanced Light Detection and Methods of Making the Same
First Named Inventor/Applicant Name:	Susan Alie
Customer Number:	20551
Filer:	Todd Brent Alder/Nicole Solomon
Filer Authorized By:	Todd Brent Alder
Attorney Docket Number:	3035-013.PROV
Receipt Date:	24-MAR-2010
Filing Date:	
Time Stamp:	17:57:48
Application Type:	Provisional

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Payment Type	Electronic Funds Transfer
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
61/317,147	03/24/2010		110	3035-013.PROV		

CONFIRMATION NO. 1150

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

FILING RECEIPT



OC000000040986443

Date Mailed: 04/12/2010

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Susan Alie, Beverly, MA;

Power of Attorney:

Todd Alder--54598

If Required, Foreign Filing License Granted: 04/06/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/317,147**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

Substrates and Devices for Enhanced Light Detection and Methods of Making the Same

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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