

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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Samsung Electronics Co., Ltd.,  
Petitioner,

v.

SiOnyx, LLC,  
Patent Owner.

Case No. IPR2025-00065  
Patent No. 10,347,682

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**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO.  
10,347,682 UNDER 35 U.S.C. §§ 311–319 AND 37 C.F.R. § 42.100 *et seq.***

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**List of Exhibits**

| <b>Exhibit</b> | <b>Description</b>                                                                                     |
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| 1001           | U.S. Patent No. 10,347,682 (the “’682 patent”)                                                         |
| 1002           | File History for U.S. Patent No. 10,347,682                                                            |
| 1003           | Provisional Application No. 61/841,326                                                                 |
| 1004           | Declaration of Dr. Michael Lebby                                                                       |
| 1005           | Curriculum Vitae of Dr. Michael Lebby                                                                  |
| 1006           | U.S. Patent Application Publication No. 2012/0068289 (Alie)                                            |
| 1007           | U.S. Patent Application Publication No. 2006/0081900 (Baggenstoss)                                     |
| 1008           | Intentionally Left Blank                                                                               |
| 1009           | U.S. Patent Application Publication No. 2012/0313204 (Haddad204)                                       |
| 1010           | U.S. Patent Application Publication No. 2010/0006969 (Park)                                            |
| 1011           | U.S. Patent No. 7,928,389 (Yap)                                                                        |
| 1012           | U.S. Patent Application Publication No. 2011/0227138 (Haddad138)                                       |
| 1013           | Samsung’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)                                 |
| 1014           | SiOnyx’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)                                  |
| 1015           | Email from N. Subhedar re: Claim Construction M&C Follow-Up (Sept. 8, 2024)                            |
| 1016           | U.S. Patent No. 8,680,591 (Haddad138 Issued Patent)                                                    |
| 1017           | U.S. Patent No. 9,496,308 (Haddad204 Issued Patent)                                                    |
| 1018           | The Authoritative Dictionary of IEEE Standard Terms (7th ed. 2000)                                     |
| 1019           | Stephen Y. Chou et al., <i>Nanoimprint Lithography</i> , J. Vac. Sci. Technol. B 14(6), 4129-33 (1996) |
| 1020           | Gary S. May & Simon M. Sze, <i>Fundamentals of Semiconductor Fabrication</i> (2003)                    |
| 1021           | Provisional Application No. 61/311,004 (Haddad138-Provisional004)                                      |
| 1022           | Provisional Application No. 61/243,434 (Haddad138-Provisional434)                                      |
| 1023           | Provisional Application No. 61/311,107 (Haddad138-Provisional107)                                      |
| 1024           | U.S. Patent Application Publication No. 2012/0146172 (Carey)                                           |
| 1025           | U.S. Patent No. 7,442,629 (Mazur)                                                                      |
| 1026           | U. Gösele & Q.-Y. Tong, <i>Semiconductor Wafer Bonding</i> (1998)                                      |
| 1027           | U.S. Patent Application Publication No. 2011/0304003 (Tanida)                                          |
| 1028           | S. Wolf, <i>Microchip Manufacturing</i> (2004)                                                         |
| 1029           | <i>Encyclopedia of Physical Science and Technology</i> (3rd ed. 2002)                                  |

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| <b>Exhibit</b> | <b>Description</b>                                                                                                   |
|----------------|----------------------------------------------------------------------------------------------------------------------|
| 1030           | Christoph Posch, <i>Detectors, Pixels, and Signal Processing, in SMART CAMERAS</i> (Ahmed Nabil Belbachir ed., 2010) |
| 1031           | E. Fred Schubert, <i>LIGHT-EMITTING DIODES</i> (2nd ed. 2006)                                                        |
| 1032           | U.S. Patent Application Publication No. 2006/0216904 (Tong)                                                          |
| 1033           | Provisional Application No. 61/317,147 (Alie-Provisional)                                                            |
| 1034           | U.S. Patent Application Publication No. 2013/0207168 (Edwards)                                                       |
| 1035           | Maik Wiemer, et al., <i>Plasma-Activated Bonding, in Handbook of Wafer Bonding</i> (Peter Ramm, et al., eds., 2012)  |

## I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Samsung” or “Petitioner”) petitions for *inter partes* review seeking cancellation of claims 1-44 (the “Challenged Claims”) of U.S. Patent No. 10,347,682 (Ex. 1001, the “’682 patent”).

The ’682 patent purports to improve upon traditional optoelectronic devices by adding a textured layer. Figure 2 depicts an embodiment:

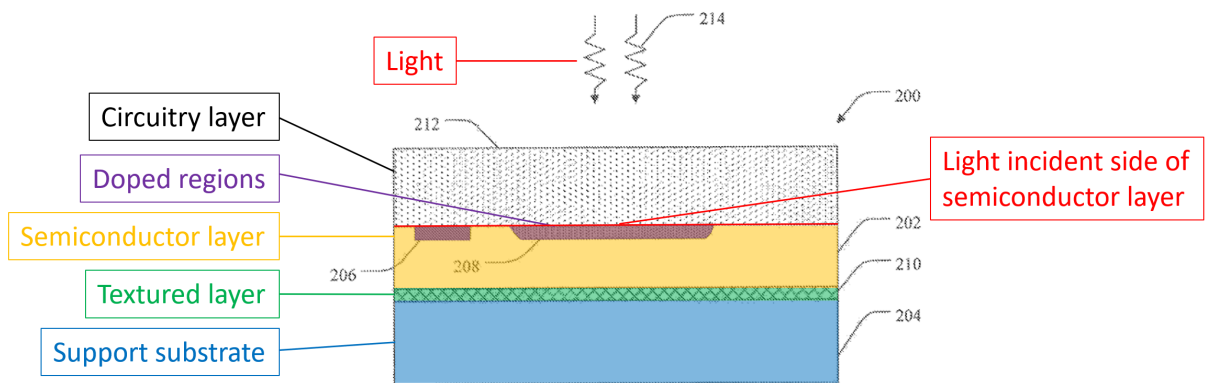


FIG. 2

’682 patent, Fig. 2 (annotated).

Light 214 comes from the top, passing through a circuitry layer 212 to reach a semiconductor layer 202. ’682 patent, 6:44-47. The semiconductor layer 202 has doped regions 206 and 208 that form a junction for sensing light. ’682 patent, 6:36-40. On the bottom side of the semiconductor layer is a textured layer containing surface features. ’682 patent, 6:40-42. The surface features of a textured layer include shapes such as “cones, pillars, pyramids, inverted features, trenches, gratings, protrusions, and the like.” ’682 patent, 9:34-36. The textured layer allegedly

functions to “diffuse light, to redirect light, and to thus increase the quantum efficiency.” ’682 patent, 9:25-27.

Although Figure 2 depicts the textured layer 210 as being located on the side of the semiconductor layer 202 *opposite* the light incident side, the independent claims of the ’682 patent require an optoelectronic device having a textured region with surface features *on* the light incident side or a method of making the same. The ’682 patent does not identify any advantage to having a textured region on the light incident side. This feature, however, was known in the prior art, and all of the prior art references relied on in this Petition explain that having a textured region on the light incident side provides additional scattering of light into the semiconductor layer or reduces reflection away from the semiconductor layer.

For example, Alie, which is prior art to the ’682 patent, discloses an optoelectronic device having a textured region with surface features on the light incident side of a semiconductor layer, including to provide additional scattering of incident light. Alie, [0094]. Like the textured region of the ’682 patent, Alie’s textured region includes surface features in the shapes of “cones, pillars, pyramids, microlenses, quantum dots, inverted features, gratings, protrusions, sphere-like structures, and the like.” Alie, [0068]. Alie’s “textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb

electromagnetic radiation, thus increasing the quantum efficiency of the device.”  
Alie, [0068].

Grounds 1 to 4 show how Alie alone or in combination with other references renders obvious claims 1-44.

## **II. STANDING, MANDATORY NOTICES, AND FEE AUTHORIZATION**

### **A. Grounds for Standing**

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the ’682 patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the ’682 patent on the grounds identified in this petition.

### **B. Real Parties-in-Interest**

The real parties-in-interest are Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

### **C. Related Matters**

Petitioner identifies the following related matter.

- *SiOnyx, LLC v. Samsung Electronics, Co., Ltd.*, 2:24-cv-00408 (E.D. Tex.)

### **D. Counsel Information**

Petitioner designates the following counsel:

| <b>Lead Counsel</b>                                                                            | <b>Back-Up Counsel</b>                                                         |
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Pursuant to 37 C.F.R. § 42.10 (b), Petitioner has filed a power of attorney with the above designation of counsel.

**E. Service Information**

Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail at the email addresses above and at Samsung-SiOnyx-IPR-Cov@cov.com.

**F. Payment of Fees Under 37 C.F.R. §42.103**

This petition is accompanied by the fees set forth in 37 C.F.R. § 42.15(a). Please charge or credit Deposit Account No. 60-3160 with any shortage or overpayment of fees associated with this petition and any other fees incurred by Petitioner.

**III. SUMMARY OF CHALLENGE**

- **Ground 1:** Claims 1-3, 5-22, 24-31, and 33-43 are obvious based on Alie.

- **Ground 2:** Claims 4-5, 14, 21-22, 25, 32-33, and 42-43 are obvious based on Alie and Baggenstoss.
- **Ground 3:** Claims 23 and 44 are obvious based on Alie and Haddad204.
- **Ground 4:** Claims 23 and 44 are obvious based on Alie and Park.

The '682 patent was filed on June 5, 2017 and claims priority to a provisional application filed on June 29, 2013. Each of the asserted references is available as prior art under 35 U.S.C. § 102 (AIA),<sup>1</sup> as shown in the following table.

| Exhibit | Reference                                                          | Date(s)                       | Availability as Prior Art |
|---------|--------------------------------------------------------------------|-------------------------------|---------------------------|
| 1006    | U.S. Patent Application Publication No. 2012/0068289 (Alie)        | March 22, 2012 (published)    | § 102(a)(1) & (2)         |
| 1007    | U.S. Patent Application Publication No. 2006/0081900 (Baggenstoss) | April 20, 2006 (published)    | § 102(a)(1) & (2)         |
| 1009    | U.S. Patent Application Publication No. 2012/0313204 (Haddad204)   | December 13, 2012 (published) | § 102(a)(1)& (2)          |
| 1010    | U.S. Patent Application Publication No. 2010/0006969 (Park)        | January 14, 2010 (published)  | § 102(a)(1) & (2)         |

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<sup>1</sup> Because both the application and the provisional application for the '682 patent were filed after March 16, 2013, the AIA conditions for patentability apply.

## IV. THE '682 PATENT

### A. Overview of the '682 Patent

The '682 patent states that silicon imaging devices were widely used, including in both front side illumination (FSI) and backside illumination (BSI) configurations. '682 patent, 1:16-29; *see also* Ex-1004 ¶¶41-47. In an FSI device, incident light enters the device by “first passing by transistors and metal circuitry.” '682 patent, 5:60-62. In a BSI device, on the other hand, “incident light enters the device via the light sensitive region opposite the circuitry.” '682 patent, 6:4-6.

The '682 patent purports to improve upon traditional optoelectronic devices by adding a textured layer, as discussed above in Section I. Figure 2 depicts an FSI embodiment with a textured layer:

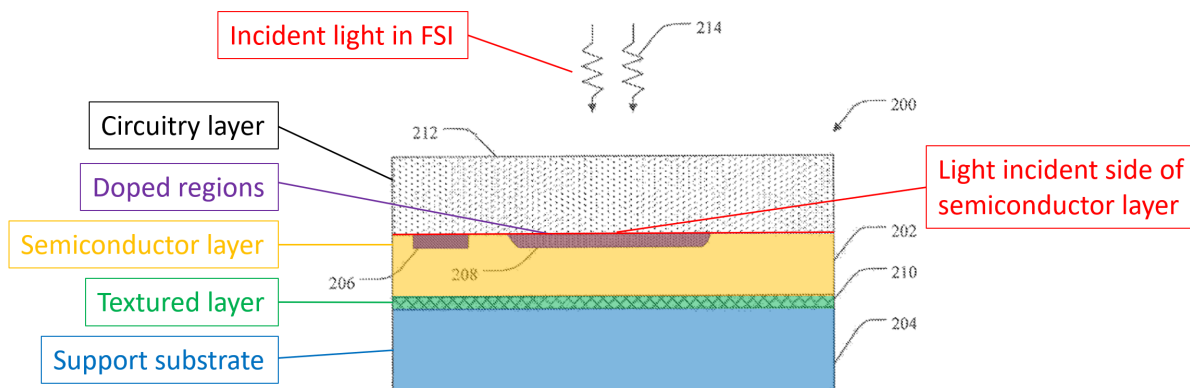
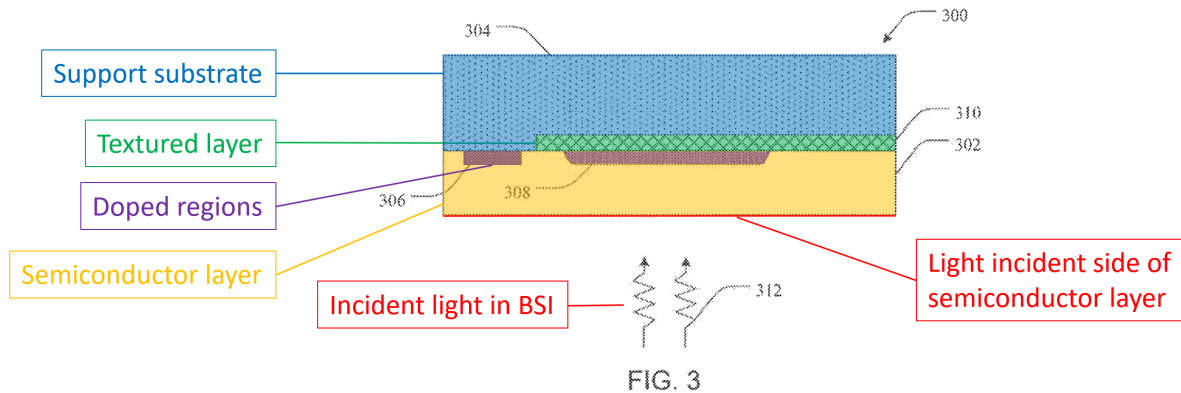


FIG. 2

'682 patent, Fig. 2 (annotated).

The Figure 2 device is an FSI device because light 214 enters the device from the top, first passing through a circuitry layer 212 before reaching a semiconductor layer 202. '682 patent, 6:44-47.

Figure 3 depicts a BSI embodiment with a textured layer:



'682 patent, Fig. 3 (annotated).

The Figure 3 device is a BSI device because light 312 enters the device from the bottom, reaching a semiconductor layer 302 without passing through a circuitry layer. '682 patent, 6:63-65.

Unlike the independent claims of the '682 patent, which all require a textured region *on* the light incident side, both Figures 2 and 3 depict a textured layer (green) on a side of the semiconductor layer (yellow) *opposite* the light incident side. The '682 patent does not include a figure with a textured layer or region *on* the light incident side or identify any advantage to such a configuration. The '682 patent, though, notes that “the textured region can be located on the light incident side of the semiconductor material,” as well as being located “on a side of the

semiconductor material opposite the light incident side, or both on the light incident side and opposite the light incident side.” ’682 patent, 7:43-48.

**B. Prosecution History**

The ’682 patent was filed on June 5, 2017, claiming priority to Provisional Application No. 61/841,326, filed on June 29, 2013.

Following an office rejection, the applicant added to claim 1 two limitations in an attempt to overcome the cited prior art: (1) shallow trench isolation surface features being located on the light incident side, and (2) a first bonding layer. Ex-1002 at 70. After another office rejection, the applicant added to claim 1 the limitation of “wherein said optoelectronic device is a photosensitive imager device capable of detecting visible and infrared electromagnetic radiation.” Ex-1002 at 110. The applicant also added to claim 17 (issued as claim 24) the limitation of bonding a first bonding layer to a second bonding layer. Ex-1002 at 111.

The examiner issued a notice of allowance, noting that the cited prior art did not disclose “a support substrate coupled to said semiconductor layer and a first bonding layer disposed between the semiconductor layer and the support substrate” and “bonding the first bonding layer to a second bonding layer disposed on the support substrate.” Ex-1002 at 1629.

## **V. LEVEL OF ORDINARY SKILL**

A person of ordinary skill in the art (“POSITA”) as of June 2013 would have had a bachelor’s degree in engineering, physics, or a related or equivalent field, and two or more years of experience researching, developing, designing, and/or evaluating image sensors using photonics. Ex-1004 ¶52. A person with less or different education but more relevant practical experience, or vice versa, may also meet this standard. Ex-1004 ¶52.

## **VI. CLAIM CONSTRUCTION**

In IPR proceedings, claims are construed in accordance with their “ordinary and customary meaning” in light of the specification. 37 C.F.R. § 42.100(b); *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005). For purposes of this petition, Petitioner does not believe that any specialized constructions are necessary.

U.S. Patent No. 11,069,737 (the “’737 patent”) is a continuation of the ’682 patent, and shares the same specification and the same or similar claim terms with the ’682 patent. SiOnyx, LLC (“SiOnyx” or “Patent Owner”) asserted the ’737 patent against Petitioner in *Sensors with Pixels and Products Containing the Same*, Inv. No. 337-TA-1403 (ITC) (“’737 Case”). In the ’737 Case, Petitioner and Patent Owner have proposed competing constructions for certain terms of the ’737 patent. *See* Ex-1013; Ex-1014; Ex-1015. For the limitations of the ’682 patent that include

a term that is the same as or similar to a disputed term from the 737 Case, both Petitioner's and Patent Owner's proposed constructions are identified and addressed in Section VIII below.

## **VII. OVERVIEW OF THE PRIOR ART**

### **A. Alie (Ex-1006)**

Alie is prior art because it was published on March 22, 2012, which is more than one year before the '682 patent's provisional application filing date of June 29, 2013.

Alie was not listed in an information disclosure statement (IDS) and was not discussed during prosecution.

The '682 patent incorporates by reference—but does not claim priority to—Alie's patent application, referring to Alie for “[f]urther details regarding substrates, bonding, and various imager details.” '682 patent, 7:21-24. Like the '682 patent, Alie discloses an optoelectronic device having a textured region with surface features. Ex-1004 ¶¶58-63.

Figure 5 depicts an example optoelectronic device with a textured region 36. Alie, [0096].

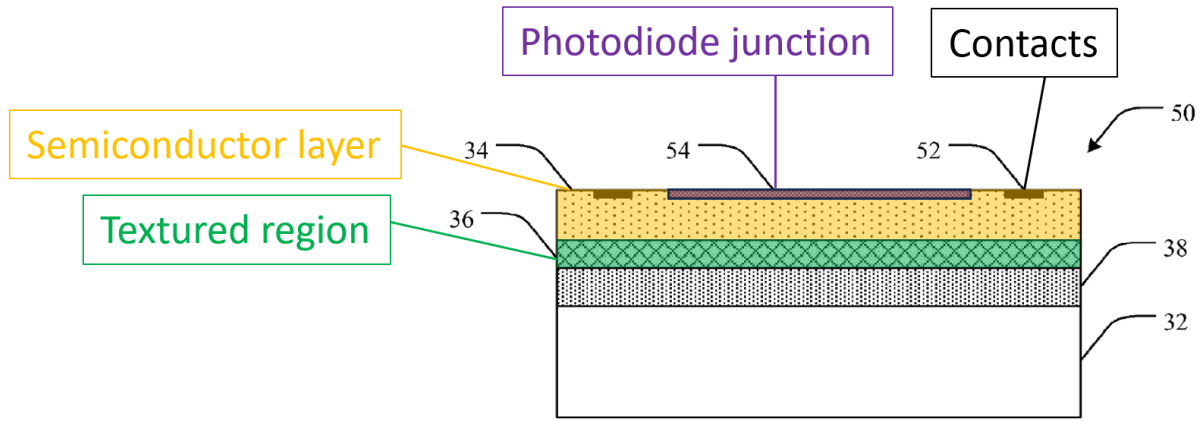


FIG. 5

Alie, Fig. 5 (annotated).

Like the '682 patent, Alie discloses that its devices can be adapted for either an FSI architecture or a BSI architecture. Alie, [0053] (“in addition to backside illuminated, front side illuminated architectures are also contemplated to be within the present scope”). When the Figure 5 device is adapted for an FSI architecture, incident light would enter from the top (where photodiode junction 54 is located), similar to the FSI device depicted in Figure 2 of the '682 patent. Ex-1004 ¶62; *see also* Ex-1004 ¶¶39-40. Alie discloses that a textured forward scattering layer can be added “on the side of the device that receives incident electromagnetic radiation” for additional scattering of incident light. Alie, [0094].

When the Figure 5 device is adapted for a BSI architecture, incident light would enter from the bottom (the opposite side of where photodiode junction 54 is located), similar to the BSI device depicted in Figure 3 of the '682 patent. Ex-1004

¶63; *see also* Ex-1004 ¶¶39-40. A BSI adaptation of the Figure 5 device is further discussed below regarding limitation 1[b].

**B. Baggenstoss (Ex-1007)**

Baggenstoss is prior art because it was published on April 20, 2006, which is more than one year before the '682 patent's provisional application filing date of June 29, 2013.

Baggenstoss was not listed in an IDS and was not discussed during prosecution. A parent application (of which Baggenstoss is a divisional) was listed in an IDS along with almost 900 other documents, but it was not discussed during prosecution.

Baggenstoss discloses an optoelectronic device with a textured region in the form of a grated interface formed by trenches (elements 144 in Figure 4, below). Baggenstoss, [0031]-[0032], [0009]; *see also* Ex-1004 ¶¶64-68.

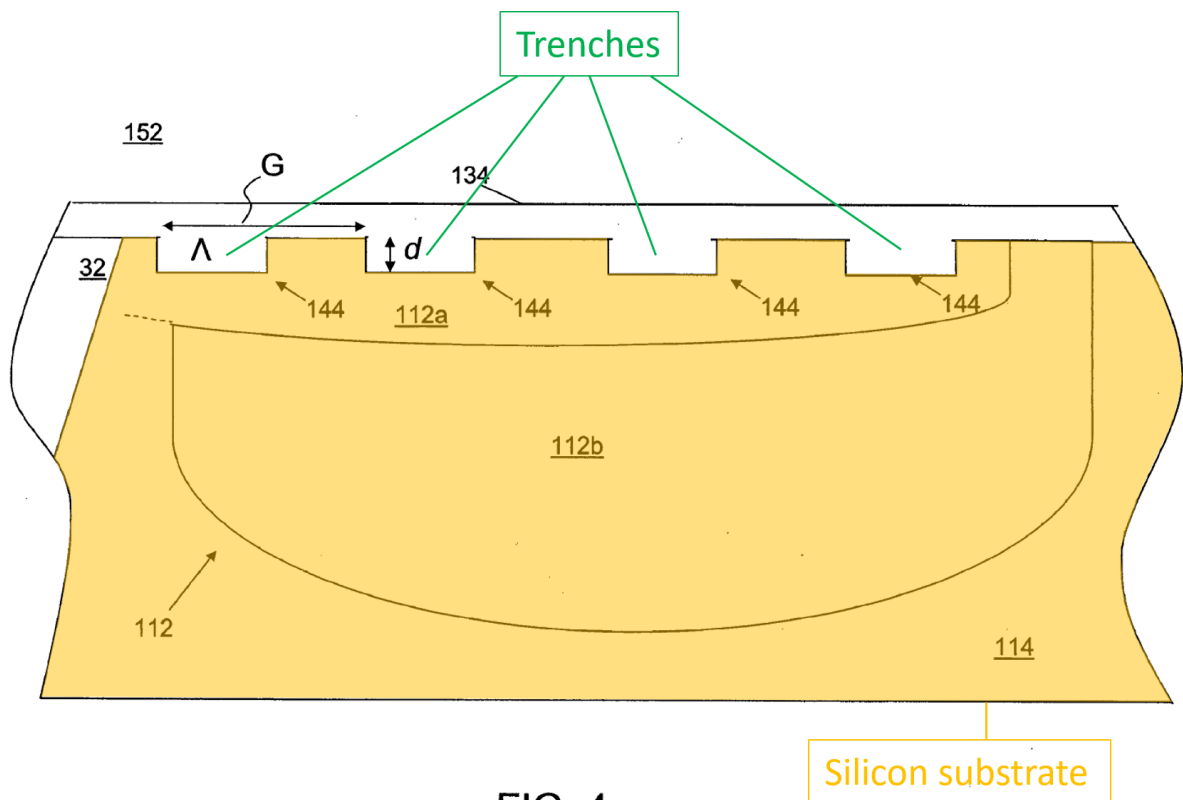


FIG. 4

Baggenstoss, Fig. 4 (annotated).

In another embodiment, Baggenstoss discloses an optoelectronic device with a textured region in the form of “blazed (or step-wise)” gratings formed of trenches (elements 244 in Figure 11, below). Baggenstoss, [0042].

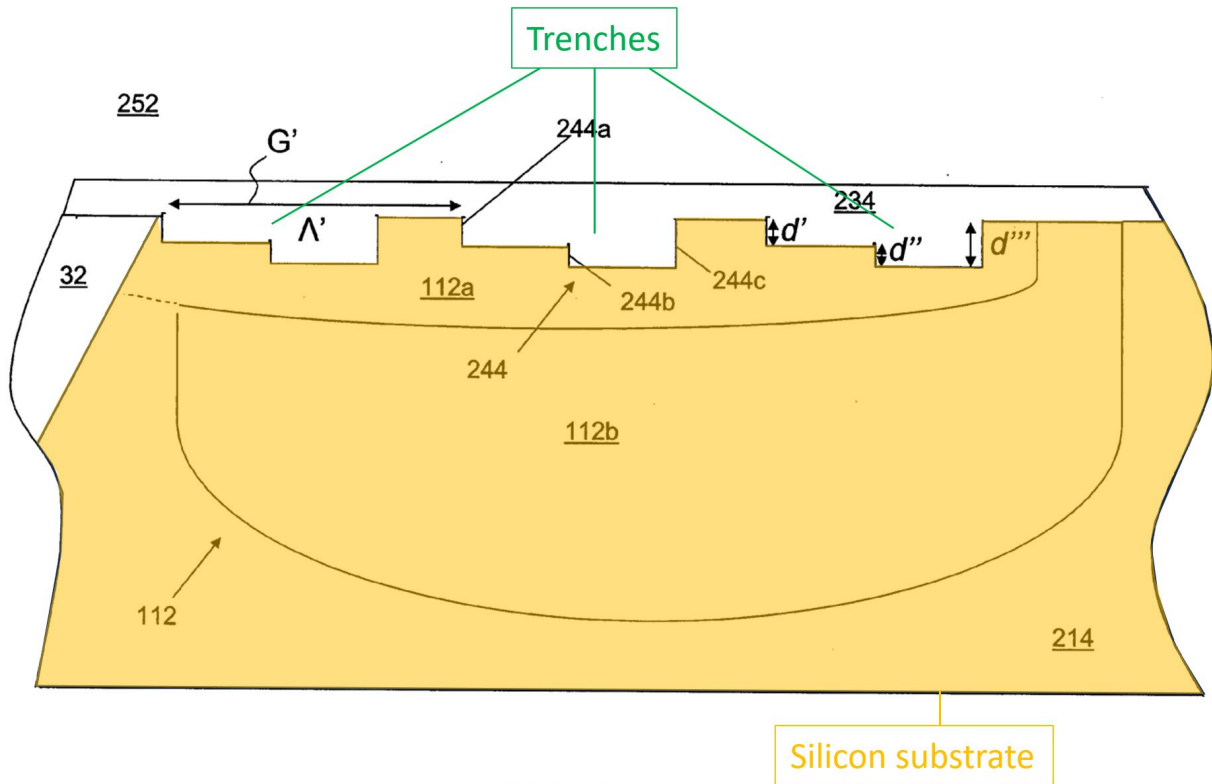


FIG. 11

Baggenstoss, Fig. 11 (annotated).

Baggenstoss's grating interface is located on the light incident side of a silicon substrate. Baggenstoss, Fig. 3, [0008]; *see also* Ex-1004 ¶68. Baggenstoss teaches that its "grating interface allows a greater percentage of incident light to be captured, which is a vast improvement over the art." Baggenstoss, [0014].

### C. Haddad204 (Ex-1009)

Haddad204 is prior art because it was published on December 13, 2012, which predates the '682 patent's provisional application filing date of June 29, 2013.

Although Haddad204 was listed in an IDS along with almost 900 other documents, it was not discussed during prosecution.

The named inventors of the '682 patent, Homayoon Haddad and Jutao Jiang, are also joint inventors of Haddad204. Like the '682 patent, Haddad204 discloses an optoelectronic device with a textured region including surface features. Haddad204, [0073], [0053]; *see also* Ex-1004 ¶¶69-72. In particular, Haddad204 discloses “a plurality of pillars of variable sizes ... arranged in a non-uniform array.” Haddad204, [0112]; *see also* Ex-1004 ¶71. Figure 9a shows a top view and Figure 9b shows a cross-sectional view of such “pillars etched into a semiconductor material.” Haddad204, [0112].

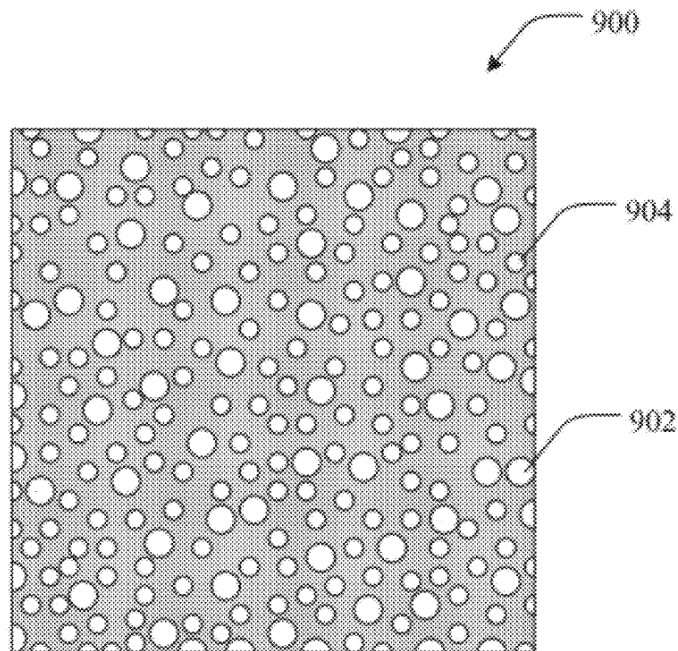


FIG. 9a

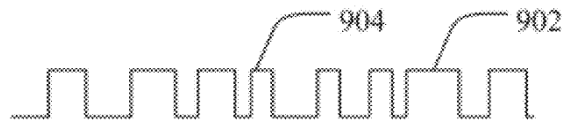


FIG. 9b

Haddad204, Figs. 9a-b.

Haddad204 discloses that textured regions can be placed on both sides of a semiconductor layer. Haddad204, [0111] (disclosing that in addition to texturing the side opposite the light incident side, “texturing can be applied to the light-incident surface of the semiconductor substrate in order to facilitate additional scattering as light enters the device”).

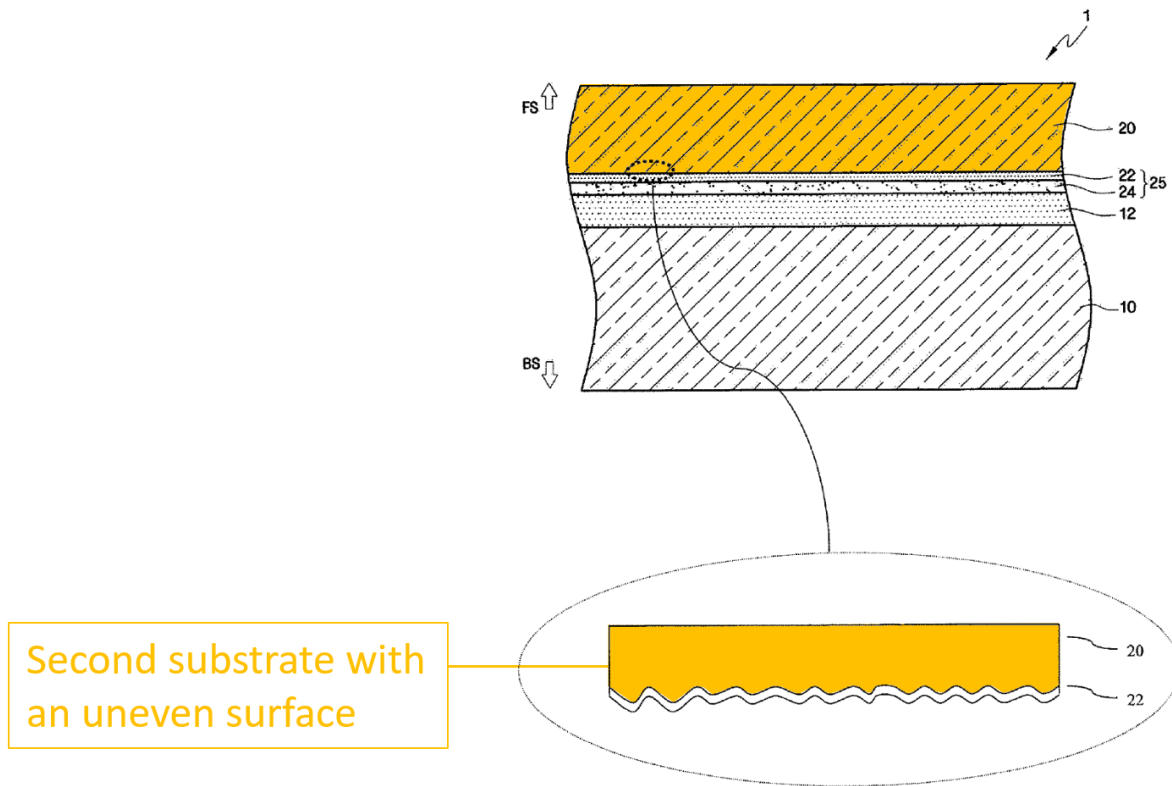
**D. Park (Ex-1010)**

Park is prior art because it was published on January 14, 2010, which is more than one year before the '682 patent's provisional application filing date of June 29, 2013.

Park was not listed in an IDS and was not discussed during prosecution.

Like the '682 patent, Park discloses an optoelectronic device with a textured region including surface features. Park, [0072] (“Referring to the inset in FIG. 1 ... reflections may also be reduced by processing the second substrate 20 to have an uneven surface facing the oxide layer 22.”), [0059] (“FIGS. 1 to 7 illustrate cross-sectional views of stages in a method of fabricating an image sensor”); *see also* Ex-1004 ¶¶73-76.

FIG. 1



Park, Fig. 1.

Park's uneven surface is located on the light incident side of a semiconductor layer. Park, Figs. 1 & 7. Park teaches that the uneven surface helps with absorbing incident light by reducing reflection. Park, [0072].

## VIII. APPLICATION OF PRIOR ART TO THE CHALLENGED CLAIMS

### A. Ground 1: Claims 1-3, 5-22, 24-31, and 33-43 Are Obvious Based on Alie

#### 1. Claim 1

- a) 1[pre]: "An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:"

Alie discloses the preamble to the extent it is limiting. Ex-1004 ¶¶77-78.

Alie discloses an optoelectronic device with a textured region. Alie, [0096], Fig. 5; *see also* Ex-1004 ¶78. “The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to ***absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.***” Alie, [0068];<sup>2</sup> *see also* Alie, [0052] (“Specific types of semiconductor texturing can ***enhance*** the spectral bandwidth, ***absorption***, and quantum efficiency of a semiconductor material.”), [0077] (“the textured surface can ***increase the probability of incident radiation being absorbed***”).

- b) 1[a]: “a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,”

Alie discloses this limitation. Ex-1004 ¶¶79-82.

Figure 5 depicts a photodiode 50 with a semiconductor layer 34 having a top side and a bottom side. Alie, [0096]; *see also* Ex-1004 ¶80.

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<sup>2</sup> All emphases in quotes have been added, unless otherwise stated.

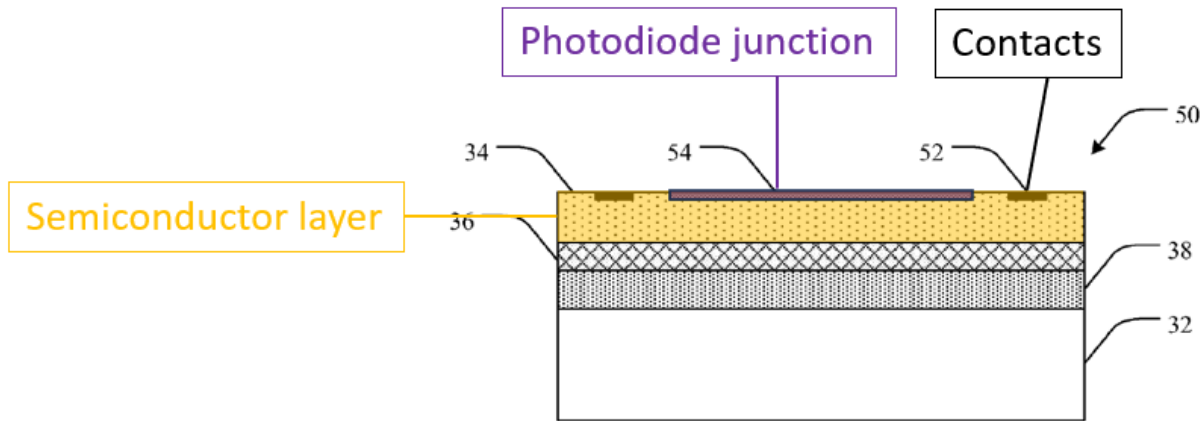


FIG. 5

Alie, Fig. 5 (annotated).

The top side and the bottom side correspond to the claimed light incident side and the opposed side. Ex-1004 ¶81. The side corresponding to the claimed light incident side depends on whether the Figure 5 device is adapted for an FSI architecture (in which case the top side is the light incident side) or for a BSI architecture (in which case the bottom side is the light incident side), as discussed above in Section VII.A. Ex-1004 ¶81.

Alie discloses “forming a p-i-n semiconductor material stack that creates a junction” (i.e., the claimed multiple doped regions forming at least one junction). Alie, [0066]; *see also* Alie, [0066] (“the semiconductor material may include multiple junctions”); Ex-1004 ¶82. This semiconductor material stack corresponds to the claimed multiple doped regions, as the p-region and the n-region in the p-i-n stack are doped regions. Ex-1004 ¶82.

- c) **1[b]: “a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,”**

Alie renders this limitation obvious. Ex-1004 ¶¶83-107.

- (1) **“a textured region comprising a plurality of shallow trench isolation surface features”**

Alie discloses a textured region having surface features (i.e., the claimed shallow trench isolation surface features). Alie, [0068]. As Dr. Lebby explains, Alie’s surface features have the same structures as the shallow trench isolation surface features described in the specification of the ’682 patent. Ex-1004 ¶84. Alie discloses that “[n]on-limiting examples of shapes and configurations of surface features include cones, pillars, pyramids, ... inverted features, gratings, protrusions ... and the like, including combinations thereof.” Alie, [0068]. These are the same shapes and configurations that the ’682 patent provides as examples of shallow trench isolation surface features. ’682 patent, 9:34-37 (“Non-limiting examples of such shapes and configurations include cones, pillars, pyramids, inverted features ... gratings, protrusions, and the like, including combinations thereof.”); *see also* ’682 patent, cl. 12 (“The device of claim 1, wherein said shallow trench isolation surface features comprise pyramids.”). Alie also discloses that its surface features can have a height of “from about 50 nm to about 2  $\mu$ m,” Alie, [0068], just like the surface features of the ’682 patent, ’682 patent, 11:27-28; *see also* Ex-1004 ¶84.

Both Alie and the '682 patent describe the same or similar processes for creating the shallow trench isolation surface features. Ex-1004 ¶85. Alie discloses forming surface features using “plasma etching, reactive ion etching, porous silicon etching ... chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, selective epitaxial growth.” Alie, [0074]. These are the same methods used to create shallow trench isolation surface features in the '682 patent, as explained in the provisional application for the '682 patent. Ex-1003, 11:16-22 (“Various methods can be utilized to form shallow trench isolation features.... Non-limiting examples can include chemical etching (e.g. anisotropic etching, isotropic etching) ... porous silicon etching, nanoimprinting, material deposition, selective epitaxial growth, reactive ion etching, plasma etching or any other technique that can be used to form such a topology.”); *see also* Ex-1004 ¶85.

Both Alie and the '682 patent explain that their shallow trench isolation surface features serve the same function. Ex-1004 ¶86. Just as the '682 patent states that its “surface features of the textured layer ... facilitate an increase [in] the effective optical path length of the semiconductor layer,” '682 patent, 9:29-31, Alie discloses that its “textured region can include surface features to further increase the effective absorption length of the device,” Alie, [0068].

Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in

a given device, it would have been obvious to use the same process to form both the surface features and the shallow trench isolation in Alie. Ex-1004 ¶87. Alie discloses forming shallow trench isolation. Alie, [0098]. As Dr. Lebby explains, the process for creating shallow trench isolation was well known. Ex-1004 ¶87. Creating the surface features using the same process as the process for the shallow trench isolation would generate predictable results, and reduce the costs associated with developing a new process. Ex-1004 ¶87. This would involve employing a known technique to improve similar devices in the same way. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007); Ex-1004 ¶87. A POSITA would have had a reasonable expectation of success because Alie already discloses using shallow trench isolation in its devices, and, as Dr. Lebby discusses, it was well known how to use a shallow trench isolation process to form surface features. Alie, [0098]; Ex-1012, [0066]; Ex-1034, [0010]-[0012]; *see also* Ex-1004 ¶87.

**(2) “located on the light incident side of the semiconductor layer”**

Alie explains placing the claimed shallow trench isolation surface features on the light incident side of the semiconductor layer. Figure 5 depicts a textured region 36 having surface features. Alie, [0096], [0068]; *see also* Ex-1004 ¶88.

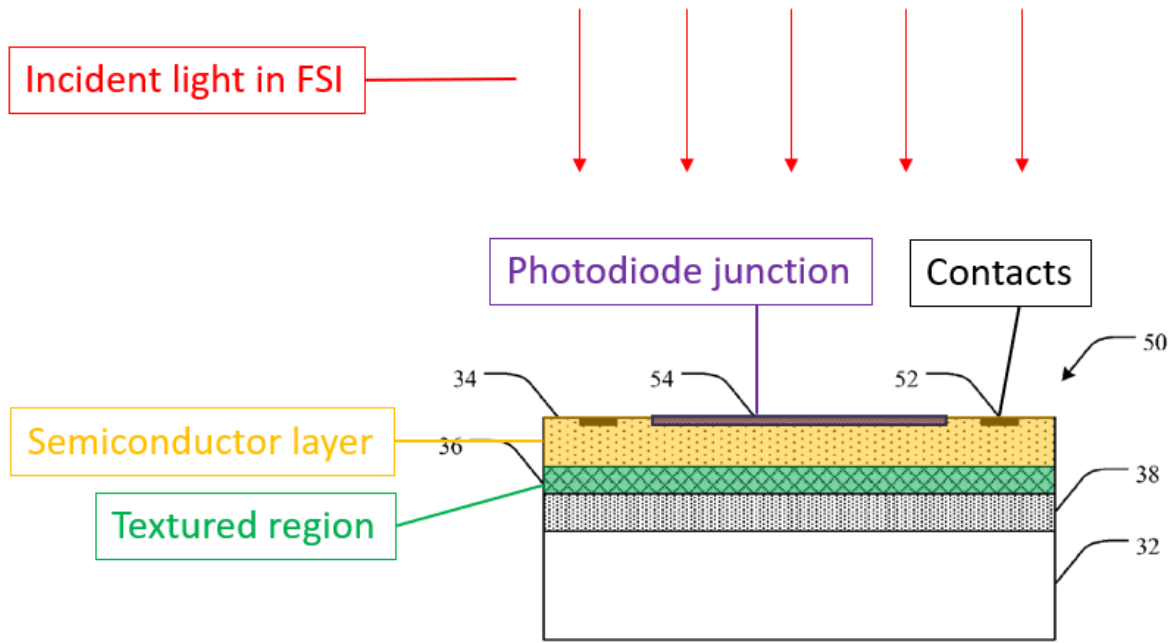


FIG. 5

Alie, Fig. 5 (annotated and modified to show incident light).

In an FSI architecture, incident light enters the Figure 5 device from the top, as discussed above in Section VII.A. Ex-1004 ¶89.

Alie discloses that a “textured forward scattering layer” can be added “on the side of the device that receives incident electromagnetic radiation.” Alie, [0094]. In an FSI architecture, a textured forward scattering layer would be added as depicted in annotated and modified Figure 5 below:

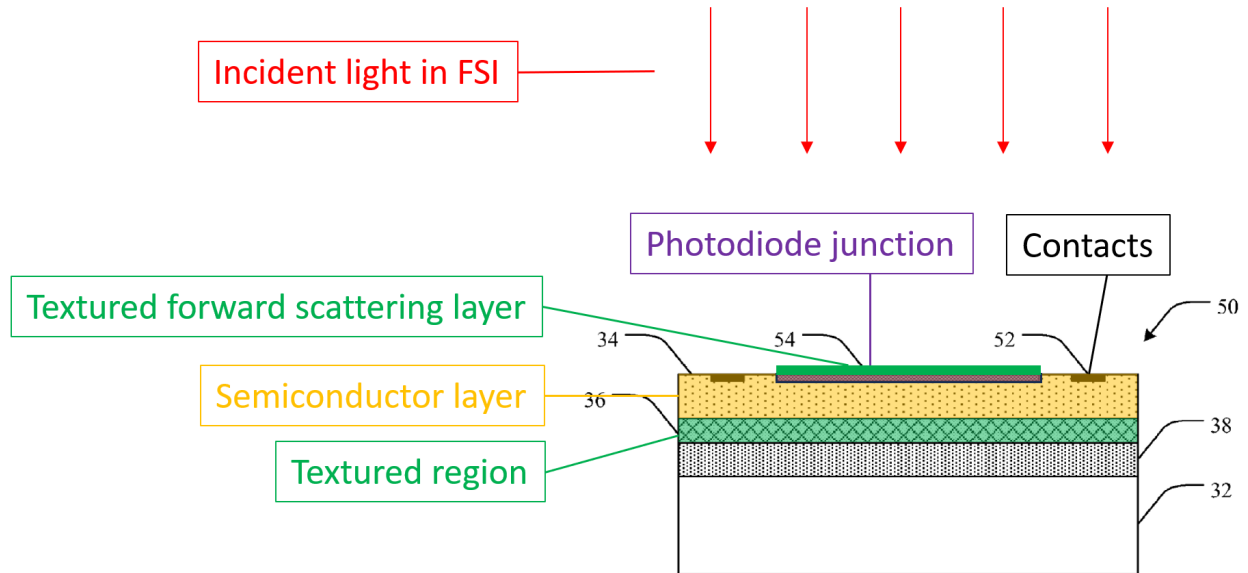


FIG. 5

Alie, Fig. 5 (annotated and modified to show the addition of a textured forward scattering layer, as well as incident light); *see also* Ex-1004 ¶90.

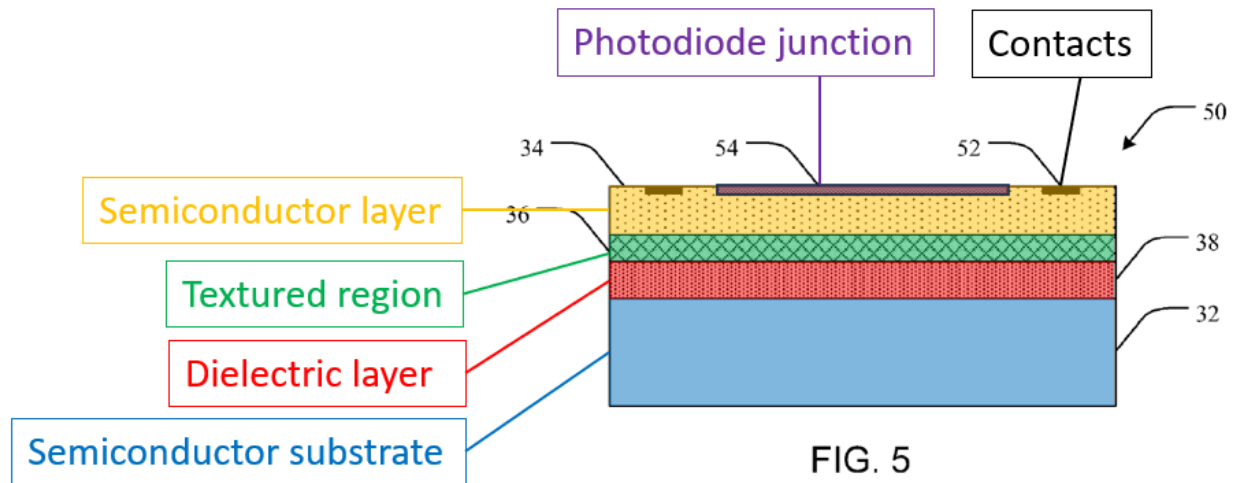
The textured forward scattering layer may get its texture from its own surface features, or by conforming to the surface features formed on the top surface of the semiconductor layer. Alie, [0069]; *see also* Ex-1004 ¶91. For example, Alie explains that a textured layer can be formed by creating surface features and covering them with a layer that conforms to the shape of the surface features. Alie, [0069], [0071]. As Dr. Lebby explains, in an FSI architecture, the surface features that give texture to the textured forward scattering layer correspond to the claimed shallow trench isolation surface features located on the light incident side of the semiconductor layer. Ex-1004 ¶91.

Alternatively, the Figure 5 device can be configured for a BSI architecture. Alie, [0053]; *see also* Ex-1004 ¶¶92-93. Indeed, Alie specifically states that both FSI and BSI architectures are “contemplated to be within the present scope,” thus motivating and suggesting to a POSITA to configure the Figure 5 device for a BSI architecture. Alie, [0053]. As Dr. Lebby explains, BSI devices “offer superior performance because the incident light directly reaches the photodiode junction without passing through the metallization layer.” Ex-1004 ¶¶39-40, 92. When configured for a BSI architecture, incident light would enter the Figure 5 device from the bottom, as discussed above in Section VII.A. As another prior art patent teaches about a similar device with a textured region on the bottom side, the device “can be configured with a BSI architecture, and thus *electromagnetic radiation would enter the semiconductor substrate from the direction of the textured region,*” i.e., from the bottom side. Ex-1012, [0049]; Ex-1004 ¶93.

Because the textured region 36 of the Figure 5 device would be located on the bottom side of the semiconductor layer (i.e., the claimed light incident side in a BSI architecture), the surface features of the textured region 36 correspond to the claimed shallow trench isolation surface features located on the light incident side of the semiconductor layer, where the Figure 5 device is configured for a BSI architecture. Ex-1004 ¶102. As Dr. Lebby explains, such BSI devices having a textured region on

the light incident side were commonplace at the time of the '682 patent. Ex-1004 ¶¶103-05.

This configuration would involve a modification to the Figure 5 device, which includes a dielectric layer 38 (red below) that bonds a semiconductor substrate 32 (blue below) to the bottom of the device. Alie, [0089], [0096], [0055]; *see also* Ex-1004 ¶¶94.



Alie, Fig. 5 (annotated).

As Dr. Lebby explains, in a BSI architecture, the semiconductor substrate 32 would instead be bonded to the top of the device via the dielectric layer 38. Ex-1004 ¶¶94-100. Bonding the semiconductor substrate 32 to the top side would locate it out of the way of incident light from the bottom, allowing more incident light to reach the semiconductor layer 34, while still providing structural support. Ex-1004 ¶¶95. Alie teaches that absorbing more light leads to an increase in the quantum efficiency, which in turn, leads to an improvement in the signal to noise ratio. Alie, [0068],

[0070]; *see also* *KSR*, 550 U.S. at 418; Ex-1004 ¶95. For these reasons, it was common to bond a support substrate to a device on the side opposite the light incident side. *See, e.g.*, Ex-1010, Fig. 7; *see also* Ex-1004 ¶95. The side from which incident light enters a device would determine the side to which a support substrate is bonded. Ex-1004 ¶95. A POSITA would have had a reasonable expectation of success in bonding the semiconductor substrate 32 to the top side because it was a routine process to bond a support substrate to either side of a device. Ex-1012, [0086] (another prior art publication teaching that a support substrate “can be disposed on any surface of the device”), Fig. 9 (depicting a support substrate on top of a device), Fig. 11 (depicting a support substrate on bottom of a device); *see also* Ex-1004 ¶101.

**(3) “configured to interact with incident electromagnetic radiation”**

Alie discloses that “[t]he textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation,” i.e., interact with incident electromagnetic radiation. Alie, [0068]. Alie discloses that the interaction with incident electromagnetic radiation is facilitated by surface features of the textured region, i.e., the surface features are configured to interact with incident electromagnetic radiation. Alie, [0068]; *see also* Ex-1004 ¶106.

Moreover, specifically for textured regions located on the light incident side, Alie further discloses that they can provide “[a]dditional scattering,” i.e., interact with incident electromagnetic radiation. Alie, [0094]; *see also* Ex-1004 ¶107.

**d) 1[c]: “a support substrate coupled to said semiconductor layer, and”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶108-10.

Figure 5 depicts a semiconductor substrate 32 (i.e., the claimed support substrate) that is coupled to the semiconductor layer 34. Alie, [0089] (describing the same layers depicted in Figure 3 as “a semiconductor substrate 32 and a semiconductor layer 34 coupled to the semiconductor substrate”), [0096] (“It should be noted that all reference numbers in FIGS. 5 and 6 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided.”); *see also* Ex-1004 ¶109.

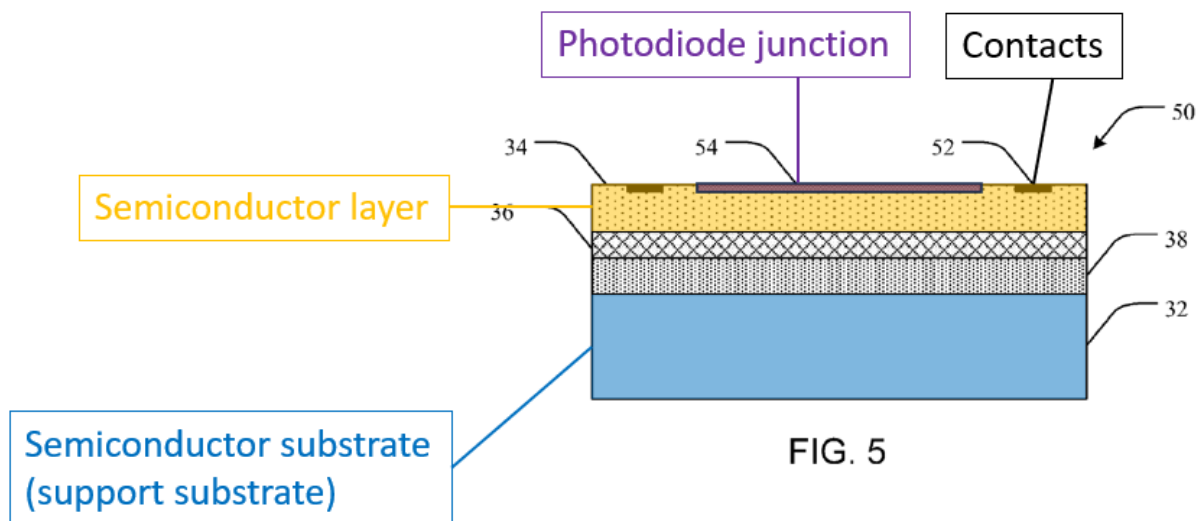


FIG. 5

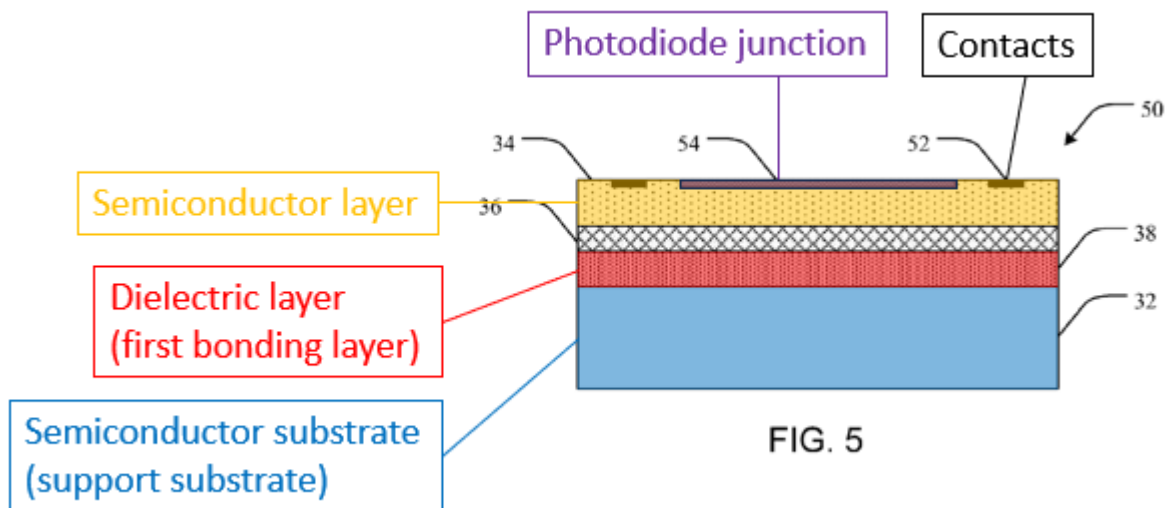
Alie, Fig. 5 (annotated).

As discussed above regarding limitation 1[b], in a BSI architecture, the support substrate would be coupled to the top of the device (which includes the semiconductor layer), rather than to the bottom of the device. Ex-1004 ¶110.

e) **1[d]: “a first bonding layer disposed between the semiconductor layer and the support substrate,”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶111-14.

Figure 5 depicts a dielectric layer 38 (i.e., the claimed first bonding layer) disposed between the semiconductor layer 34 and the semiconductor substrate 32 (i.e., the claimed support substrate). Alie, [0089] (describing the same layers depicted in Figure 3 as “a semiconductor substrate 32 and a semiconductor layer 34 coupled to the semiconductor substrate” and a “dielectric layer 38 coupled between the semiconductor substrate and the semiconductor layer”); *see also* Ex-1004 ¶112.



Alie, Fig. 5 (annotated).

The dielectric layer 38 corresponds to the claimed first bonding layer because it is used to “*wafer bond* the semiconductor layer to the semiconductor substrate.” Alie, [0055]; *see also* Alie, [0087]; Ex-1004 ¶113.

As discussed above regarding limitation 1[b], in a BSI architecture, the support substrate would be coupled to the top of the device via the dielectric layer (i.e., the claimed first bonding layer) below it. Ex-1004 ¶114. Thus, in a BSI architecture, the first bonding layer would still be disposed between the semiconductor layer and the support substrate (located at the top of the device). Ex-1004 ¶114.

**f) 1[e]: “wherein said optoelectronic device is a photosensitive imager device capable of detecting visible and infrared electromagnetic radiation.”**

Alie discloses this limitation under both Petitioner’s and Patent Owner’s proposed constructions in the 737 Case. Ex-1004 ¶¶115-19.

The preambles of claims 1 and 32 of the ’737 patent have the same recitation of this limitation, “a photosensitive imager device capable of detecting visible and infrared electromagnetic radiation.” In the 737 Case, Petitioner proposed that the preambles of claims 1 and 32 of the ’737 patent are limiting and means, “An image sensor pixel capable of detecting visible and infrared electromagnetic radiation.” Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning, and

that to the extent a construction is required, it means, “A device with multiple pixels arranged to capture an image from visible and/or infrared light.” Ex-1014, 3-4.

Alie discloses an image sensor pixel. Alie discloses a photodiode or a photodetector having enhanced light detection. Alie, [0096]-[0097], [0006], Fig. 5; *see also* Ex-1004 ¶¶37-38, 117. Alie discloses that its photodiodes/photodetectors are part of an image sensor. Alie, [0096] (“a CMOS *image sensor* having improved light detection performance is provided”). Accordingly, Alie’s provisional application refers to its “detector” as a “pixel.” Ex-1033, 5. Moreover, the ’682 patent itself refers to Alie for “[f]urther details regarding ... various *imager* details,” incorporating Alie’s patent application by reference, ’682 patent, 7:21-24, and the ’682 patent’s and Alie’s devices share a similar structure. *Compare* ’682 patent, Fig. 2 *with* Alie, Fig. 5.

In addition, Alie discloses a device with multiple pixels. Specifically, Alie discloses a device including an array of photodetectors. Alie, [0006]; *see also* Ex-1004 ¶¶37-38, 118. For example, Figure 7 depicts an array of photodetectors, each of which is similar to the Figure 5 device. Alie, [0097].

Alie’s devices are capable of detecting visible and infrared electromagnetic radiation and are arranged to capture an image from visible and/or infrared light. Alie, [0006], [0052]-[0053], [0070]; *see also* Ex-1004 ¶119. Specifically, Alie discloses that using a textured region in its devices enhances detection of “the blue

green part of the spectrum,” which corresponds to the claimed detection of visible electromagnetic radiation. Alie, [0053]; *see also* Ex-1004 ¶119. Alie also discloses that using a textured region enhances detection of “infrared,” which corresponds to the claimed detection of infrared electromagnetic radiation. Alie, [0070]; *see also* Ex-1004 ¶.

**2. Claim 2**

- a) “The device of claim 1, wherein the semiconductor layer is single crystal silicon.”**

Alie discloses this limitation. Ex-1004 ¶¶120-21.

Alie discloses that “[a] variety of semiconductor materials are contemplated for use,” including “monocrystalline silicon” (i.e., the claimed single crystal silicon). Alie, [0060]; *see also* Ex-1004 ¶121.

**3. Claim 3**

- a) “The device of claim 1, wherein the shallow trench isolation surface features are formed in the semiconductor layer.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶122-24.

As discussed above for limitation 1[b], Alie’s surface features correspond to the claimed shallow trench isolation surface features. Ex-1004 ¶123.

Alie discloses that surface features of its textured region “can be formed by wet etching the semiconductor material.” Alie, [0105]; *see also* Alie, [0104] (“a

method of making a semiconductor device can include *wet etch texturing at least a portion of a surface of a semiconductor layer* to form a textured region”), [0072] (“a substrate such as *the semiconductor layer can be textured* and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern”); Ex-1004 ¶124. Alie also discloses chemically and/or structurally *altering the surface of a substrate such as the semiconductor layer*, “result[ing] in the formation of surface features appearing as structures or patterned areas on the surface.” Alie, [0077].

#### 4. Claim 5

- a) **“The device of claim 1, wherein the shallow trench isolation surface features are not uniform in height.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶125-27.

As discussed above for limitation 1[b], Alie’s surface features correspond to the claimed shallow trench isolation surface features. Ex-1004 ¶126.

Alie discloses that its surface features, for example, “cones, pyramids, protrusions, and the like can have an *average height*.” That the surface features have an “average height” rather than one height shows that the surface features are not uniform in height, as required by this limitation. Alie, [0068]; *see also* Ex-1004 ¶127.

**5. Claim 6**

- a) **“The device of claim 1, further comprising a device layer coupled to the semiconductor layer on said side opposed to the light incident side.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶128-29.

As discussed above in Section VII.A, Alie discloses that its devices can be configured for both BSI and an FSI architecture. Alie, [0053]. In a BSI architecture, a circuitry or a metallization layer (i.e., the claimed device layer) is coupled to a semiconductor layer on the side opposed to the light incident side. Ex-1004 ¶129. As another prior art patent publication explains, in a BSI architecture, “incident light enters the device via the light sensing portion and is mostly absorbed *prior to reaching the circuitry*.” Ex-1012, [0048]; *see also* Ex-1004 ¶129. This understanding is consistent with the specification of the ’682 patent, which states, “BSI imagers ... are configured such that incident light enters the device via the light sensitive region opposite the circuitry.” ’682 patent, 6:4-6. The provisional application to the ’682 patent refers to such a circuitry or a metallization layer as a device layer. Ex-1003, Fig. 3.

6. Claim 7

- a) **“The device of claim 1, wherein said first bonding layer comprises any of silicon oxide, silicon nitride and amorphous silicon.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶130-34.

Alie discloses that its dielectric layer (i.e., the claimed first bonding layer) can include “oxides” and “nitrides.” Alie, [0088]. A POSITA would have understood that silicon oxides and silicon nitrides are among the most common oxides and nitrides used for bonding. *See, e.g.*, Ex-1027, [0032]; Ex-1026, 228; *see also KSR*, 550 U.S. at 416; Ex-1004 ¶131.

It would also have been obvious to use silicon oxide or silicon nitride as the bonding layer because they can be easily polished and bonded. Ex-1026, 228 (“Materials that are too rough or difficult to polish may be covered by process-compatible intermediate layers such as spun-on or chemical vapor-deposited *silicon dioxide or silicon nitride, which may be easily polished and bonded.*”); *see also KSR*, 550 U.S. at 418; Ex-1004 ¶132.

It would also have been obvious to apply the known technique of using silicon oxide or silicon nitride as bonding layers to Alie’s device to yield predictable results. *KSR*, 550 U.S. at 417; Ex-1004 ¶133. Silicon oxide and silicon nitride were routinely used as bonding layers. Ex-1026, 216 (“SOI [silicon-on-insulator] structures consist

of a thin, top layer of single-crystal silicon, a layer of silicon dioxide (SiO<sub>2</sub>), and a silicon handle substrate that acts as mechanical support.”); Ex-1027, [0032] (“The bonding layer 9 is, for example, formed of at least any one of a silicon oxide film (SiO<sub>2</sub>), a silicon nitride film (SiN<sub>x</sub>) ... as a single layer or a plurality of stacked layers.”); Ex-1028, 317; *see also* Ex-1004 ¶133. The use of silicon oxide and silicon nitride would have yielded predictable results because they were commonly used in semiconductor manufacturing and their properties were well known. Ex-1026, 228; Ex-1020, 155-162; *see also* Ex-1004 ¶133.

A POSITA would have had a reasonable expectation of success. Ex-1004 ¶134. It would have been well within the abilities of a POSITA to use silicon oxide and silicon nitride because the methods of manufacturing them were well known and involved routine semiconductor manufacturing steps. Ex-1020, 155-162; *see also* Ex-1004 ¶134.

## 7. Claim 8

- a) **“The device of claim 1, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.”**

Alie discloses this limitation. Ex-1004 ¶¶135-36.

Alie discloses a semiconductor material (i.e., the claimed semiconductor layer) with “a thickness of from about 1 μm to about 10 μm.” Alie, [0063].

**8. Claim 9**

- a) **“The device of claim 1, wherein said bonding layer has a thickness in a range of about 30 nm to about 3 microns.”**

Alie renders this limitation obvious. Ex-1004 ¶¶137-38.

Alie discloses a dielectric layer (i.e., the claimed bonding layer) with “a thickness of from about 500 nm to about 2 microns,” which is a range fully encompassed by the claimed range of about 30 nm to about 3 microns. Alie, [0088]; *see also* Ex-1004 ¶138. Alie does not teach away from the claimed range and the claimed range does not produce any new or unexpected result. Ex-1004 ¶138; *see also UCB v. Actavis*, 65 F.4th 679, 689-90 (Fed. Cir. 2023).

**9. Claim 10**

- a) **“The device of claim 1, wherein said bonding layer has a thickness in a range of about 40 nm to about 2 microns.”**

Alie renders this limitation obvious. Ex-1004 ¶¶139-40.

Alie discloses a dielectric layer (i.e., the claimed bonding layer) with “a thickness of from about 500 nm to about 2 microns,” which is a range fully encompassed by the claimed range of about 40 nm to about 2 microns. Alie, [0088]; *see also* Ex-1004 ¶140. Alie does not teach away from the claimed range and the claimed range does not produce any new or unexpected result. Ex-1004 ¶140; *see also UCB v. Actavis*, 65 F.4th at 689-90.

**10. Claim 11**

- a) **“The device of claim 1, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.”**

Alie renders this limitation obvious. Ex-1004 ¶¶141-42.

Alie discloses surface features with “a height of from about 50 nm to about 2 μm,” which is a range fully encompassed by the claimed range of about 50 nm to about 20 microns. Alie, [0068]; *see also* Ex-1004 ¶142. Alie does not teach away from the claimed range and the claimed range does not produce any new or unexpected result. Ex-1004 ¶142; *see also* *UCB v. Actavis*, 65 F.4th at 689-90.

**11. Claim 12**

- a) **“The device of claim 1, wherein said shallow trench isolation surface features comprise pyramids.”**

Alie discloses this limitation. Ex-1004 ¶¶143-44.

Alie discloses that “[n]on-limiting examples of shapes and configurations of surface features include ... pyramids.” Alie, [0068].

**12. Claim 13**

- a) **“The device of claim 1, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.”**

Alie discloses this limitation. Ex-1004 ¶¶145-46.

Alie discloses that “a substrate such as the semiconductor layer can be textured and patterned [to form surface features] across only a portion of a surface

by using a selective etching technique, such as a mask, photolithography, and an etch ... to define a specific structure or pattern.” Alie, [0072]; *see also* Ex-1004 ¶146.

### 13. Claim 14

- a) **“The device of claim 1, wherein said plurality of shallow trench isolation surface features comprise multiple etched levels.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶147-48.

As discussed above regarding claim 5, Alie discloses that its surface features are not uniform in height. Alie, [0068]. And as discussed above regarding claim 13, Alie discloses that its surface features can be formed by etching. Alie, [0072]. That Alie’s surface features formed by etching have differing heights shows that the surface features comprise multiple etched levels, as required by this limitation. Ex-1004 ¶148.

### 14. Claim 15

- a) **“The device of claim 1, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.”**

Alie discloses this limitation. Ex-1004 ¶¶149-50.

Alie discloses that “[t]he textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to *absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.*” Alie, [0068]; *see also* Alie, [0052] (“Specific types of semiconductor texturing can

*enhance* the spectral bandwidth, *absorption*, and quantum efficiency *of a semiconductor material.*”), [0077] (“the textured surface can *increase the probability of incident radiation being absorbed*”).

**15. Claim 16**

- a) **“The device of claim 1, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶151-54.

Alie discloses a textured region that “allow[s] a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared).” Alie, [0070]. Infrared includes the claimed electromagnetic spectrum range of at least about 700 nm to about 1100 nm. Ex-1029, 807 (“The region of the near infrared spectrum extends from about 700 nm ( $14,000\text{ cm}^{-1}$ ) near the end of the visible region, to 2500 nm ( $4,000\text{ cm}^{-1}$ ), which is the beginning of the infrared fundamental region.”); *see also* Ex-1004 ¶152. Alie further discloses that “[s]uch internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer.” Alie, [0070]. An increase in the effective absorption length increases the optical absorption of the semiconductor layer, as required by this limitation. Alie, [0070] (“This increase in

absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.”); *see also* Ex-1004 ¶152.

In sum, because Alie discloses that its textured region increases optical absorption over the infrared spectrum, which was known to include the range of about 700 nm to 2500 nm, Ex-1029, 807, Alie discloses that its textured region increases optical absorption of the spectrum range “of at least about 700 nm to about 1100 nm,” as required by this limitation. Ex-1004 ¶153.

In addition, Alie does not teach away from the claimed range and the claimed range does not produce any new or unexpected result. Ex-1004 ¶154; *see also UCB v. Actavis*, 65 F.4th at 689-90.

#### **16. Claim 17**

- a) “The device of claim 1, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.”**

Alie discloses this limitation. Ex-1004 ¶¶155-56.

Alie discloses that its “textured region can include surface features to further increase the effective absorption length of the device,” i.e., increase the effective optical path length of light as it passes through the semiconductor layer. Alie, [0068]. This result is achieved by the textured region “diffus[ing]” and “redirect[ing]” light within the semiconductor layer. Alie, [0068].

**17. Claim 18**

- a) **“The device of claim 1, wherein said textured region allows the semiconductor layer to experience multiple passes of light.”**

Alie discloses this limitation. Ex-1004 ¶¶157-58.

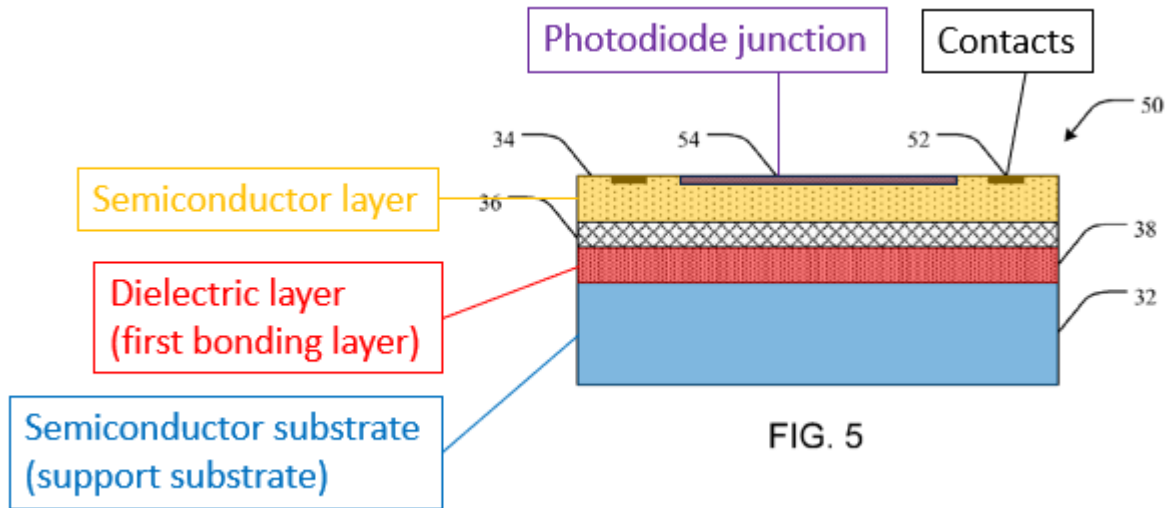
Alie discloses that its textured region “can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared).” Alie, [0070].

**18. Claim 19**

- a) **“The device of claim 1, further comprising a second bonding layer positioned between the first bonding layer and the support substrate.”**

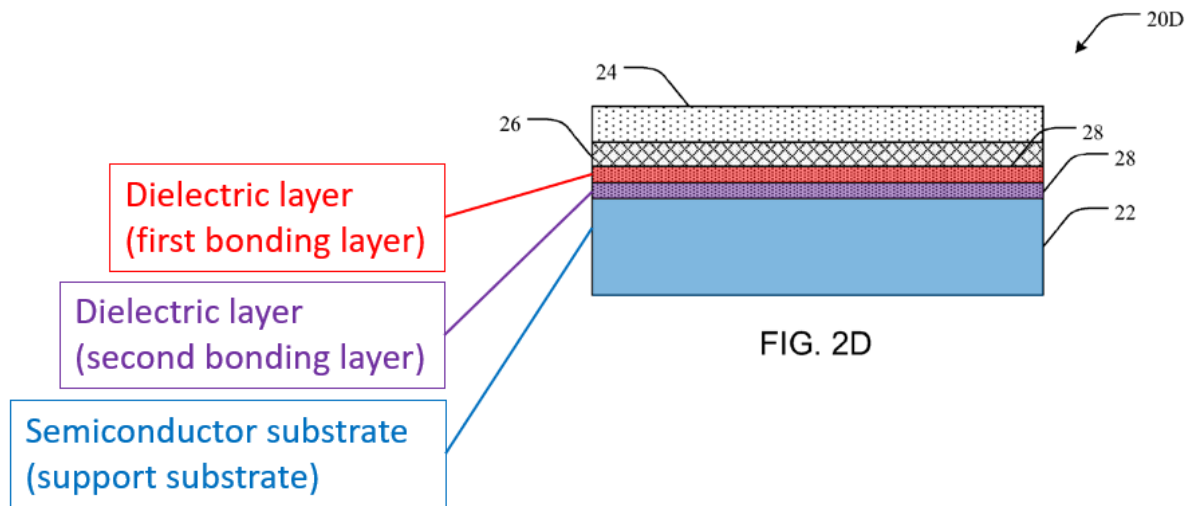
Alie discloses, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶159-63.

Alie discloses that, instead of using just one dielectric layer for bonding, two dielectric layers can be used. Alie, [0059], [0105]. As discussed above regarding limitation 1[d], Figure 5 depicts a dielectric layer 38 (i.e., the claimed first bonding layer) disposed between the semiconductor layer 34 and the semiconductor substrate 32 (i.e., the claimed support substrate). Alie, [0089]; *see also* Ex-1004 ¶160.



Alie, Fig. 5 (annotated).

In discussing a manufacturing method for a device similar to the Figure 5 device, Alie discloses that there can be “a second dielectric layer formed on the semiconductor substrate (not shown)” in addition to the existing dielectric layer. Alie, [0105]. The second dielectric layer corresponds to the claimed second bonding layer positioned between the first bonding layer and the support substrate. Figure 2D illustrates how such a second bonding layer (purple) is positioned between the first bonding layer (red) and the support substrate (blue). Alie, [0055], [0059]; *see also* Ex-1004 ¶161.



Alie, Fig. 2D (annotated).

A POSITA would have known that using two bonding layers was a common technique to ensure the strength, uniformity, thermal performance, and reliability of the bond. *See, e.g.*, Ex-1032, [0041]-[0042]; Ex-1035, 113-14; *see also* Ex-1004 ¶162.

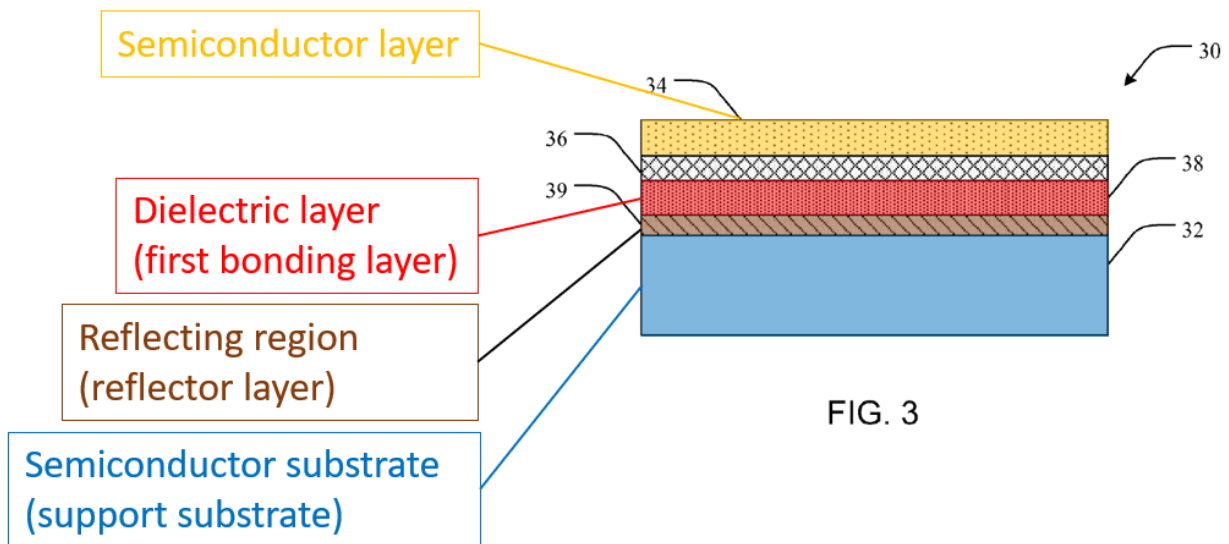
As discussed above regarding limitation 1[b], in a BSI architecture, the semiconductor substrate would be coupled to the top of the device via the dielectric layers below it. Ex-1004 ¶163. Thus, in a BSI architecture, the claimed second bonding layer would still be positioned between the first bonding layer and the support substrate (located at the top of the device). Ex-1004 ¶163.

**19. Claim 20**

- a) **“The device of claim 19, further comprising a reflector layer disposed between the first bonding layer and the second bonding layer.”**

Alie renders this limitation obvious. Ex-1004 ¶¶164-67.

Figure 3 depicts a device similar to that in Figure 5 discussed above regarding claim 19, but it also depicts the use of a reflecting region 39 (i.e., the claimed reflector layer) directly beneath the first bonding layer. Alie, [0089]; *see also* Ex-1004 ¶165.



Alie, Fig. 3 (annotated).

In discussing a manufacturing method for a device similar to the Figure 3 device, Alie discloses that there can be “a second dielectric layer formed on the semiconductor substrate (not shown)” in addition to the existing dielectric layer. Alie, [0105]. The second dielectric layer formed on the semiconductor substrate

corresponds to the claimed second bonding layer. Arranged as described in Alie, the reflector layer (brown) directly below the first bonding layer (red) would be sandwiched between the first bonding layer (red) and the second bonding layer formed on the semiconductor substrate (not shown). Ex-1004 ¶166.

As discussed above regarding limitation 1[b], in a BSI architecture, the support substrate would be coupled to the top of the device via the bonding layers below it. Ex-1004 ¶167. As Dr. Lebby explains, the reflector layer, which is disposed between the first bonding layer and the second bonding layer would be located at the top of the device along with the bonding layers and the support substrate. Ex-1004 ¶167.

## **20. Claim 21**

- a) “The device of claim 1, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case. Ex-1004 ¶¶168-70.

In the 737 Case, Petitioner proposed that the ’737 patent term “the surface features are arranged according to a pattern” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning and that, to the extent a construction is required, it means “features coincident with at least one surface that are arranged in a repeating manner.” Ex-1014, 4.

As discussed above for limitation 1[b], Alie's surface features correspond to the claimed shallow trench isolation surface features. Alie discloses that the surface features of its textured region can be arranged according to a pattern under Patent Owner's proposed construction in the 737 Case. Alie, [0072]; *see also* Ex-1004 ¶170. Specifically, Alie discloses that "a substrate such as the semiconductor layer can be textured and ***patterned*** across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or ***pattern***." Alie, [0072]. Alie also discloses that "[n]on-limiting examples of shapes and configurations of surface features include ... gratings," Alie, [0068], which are features coincident with at least one surface that are arranged in a repeating manner, and are an example of a pattern provided by the provisional application for the '682 patent. Ex-1003, 13:2-4 ("[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a uniform ***grid pattern*** comprised of [trenches] that form ***a series of spaces and lines*** or pillars."); *see also* Ex-1004 ¶170.

**21. Claim 22**

- a) **"The device of claim 21, wherein the pattern is an at least substantially uniform grid."**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶171-72.

Alie discloses that "[n]on-limiting examples of shapes and configurations of surface features include ... gratings." Alie, [0068]. The gratings could be uniform or

non-uniform. *See* '682 patent, 9:18-24 (providing as examples of a pattern “a uniform or substantially uniform grid,” as well as “a non-uniform or a substantially non-uniform pattern”). As Dr. Lebby explains, it would have been obvious to try uniform gratings, i.e., the claimed substantially uniform grid, given the limited number of options, i.e., two, uniform or non-uniform. *KSR*, 550 U.S. at 421; Ex-1004 ¶172.

## **22. Claim 24**

### **a) 24[pre]: “A method of making an optoelectronic device, comprising:”**

Alie discloses the preamble to the extent it is limiting. Ex-1004 ¶¶173-74.

Figures 11A and 11B depict a method of making Alie’s optoelectronic device. Alie, [0105] (“FIGS. 11A-C show one method of manufacturing a semiconductor device”); *see also* Alie, Abstract (“Photosensitive semiconductor devices and associated methods are provided.”); Ex-1004 ¶174. A photosensitive semiconductor device corresponds to the claimed optoelectronic device. Ex-1004 ¶174.

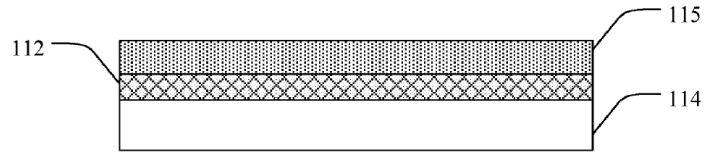


FIG. 11A

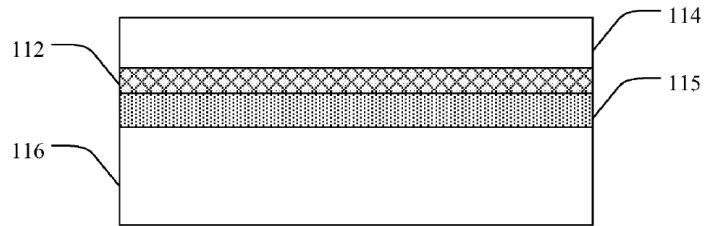


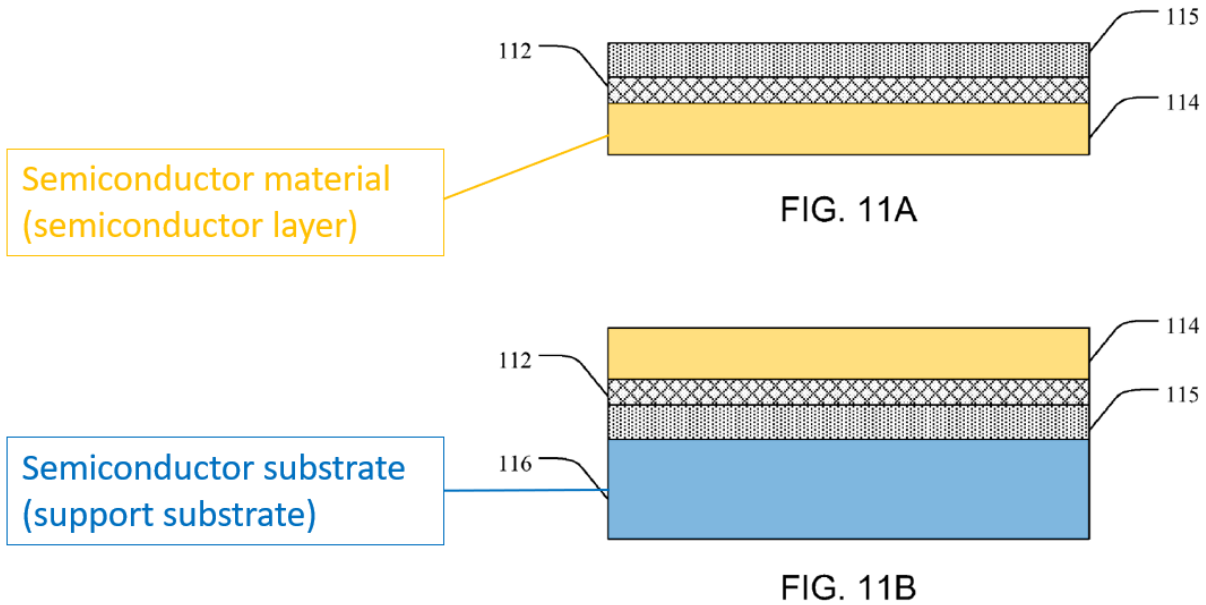
FIG. 11B

Alie, Figs. 11A-B.

- b) **24[a]: “bonding a semiconductor layer to a support substrate, wherein bonding the semiconductor layer to the support substrate includes:”**

Alie discloses this limitation. Ex-1004 ¶¶175-76.

Alie discloses that “[t]he resulting structure [shown in Figure 11A and including a semiconductor material 114, i.e., the claimed semiconductor layer] can then be *wafer bonded* to a semiconductor substrate 116 [i.e., the claimed support substrate], as is shown rotated 180° in FIG. 11B.” Alie, [0105]; *see also* Ex-1004 ¶176.

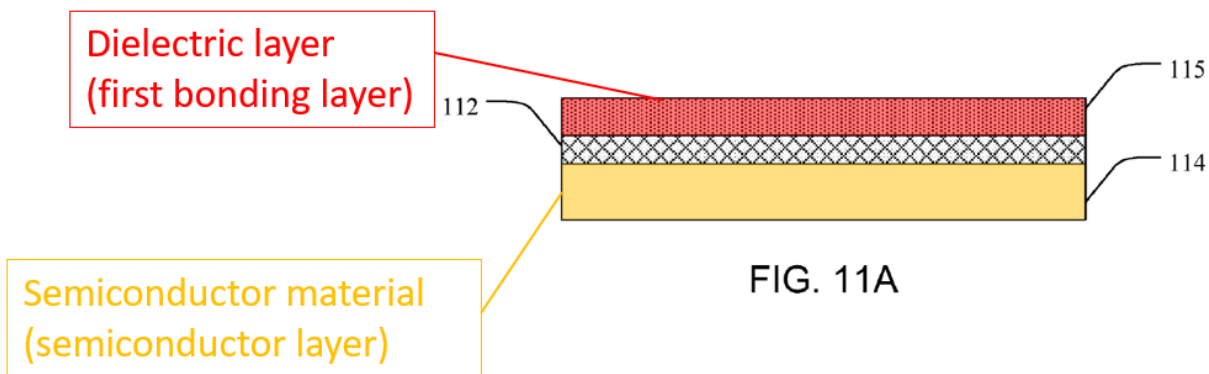


Alie, Figs. 11A-B (annotated).

**c) 24[b]: “depositing a first bonding layer onto the semiconductor layer; and”**

Alie discloses this limitation. Ex-1004 ¶¶177-79.

Figure 11A depicts depositing a dielectric layer 115 (i.e., the claimed first bonding layer) onto the semiconductor material 114 (i.e., the claimed semiconductor layer). Alie, [0105]; *see also* Ex-1004 ¶178.



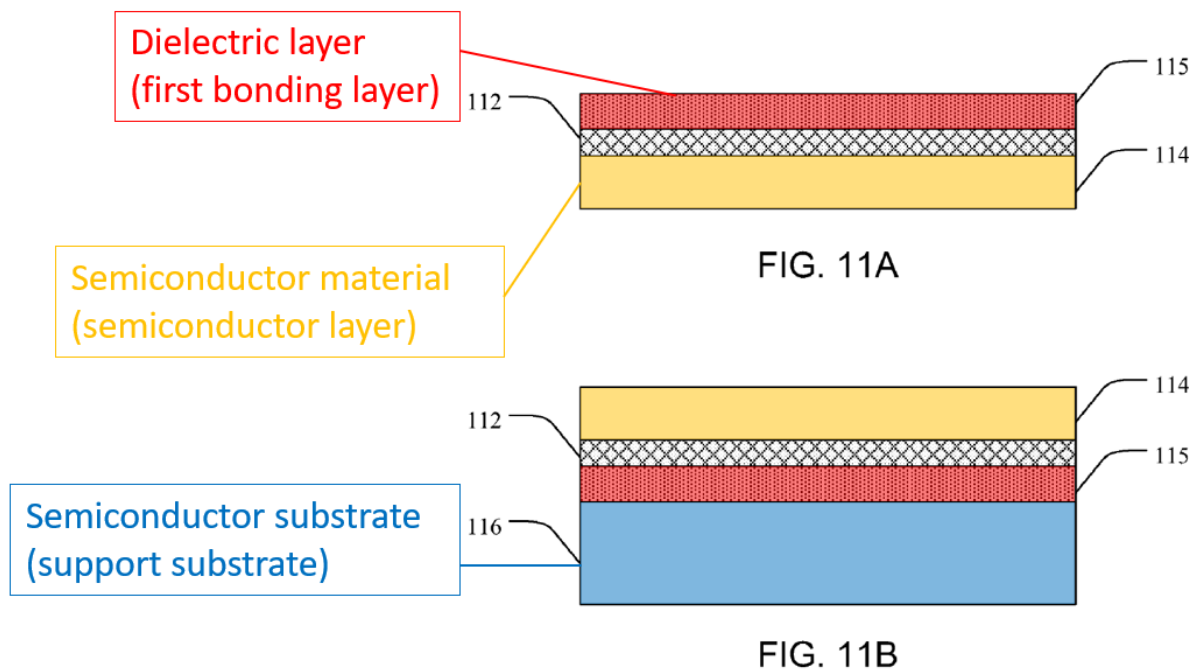
Alie, Figs. 11A-B (annotated).

The dielectric layer 115 corresponds to the claimed first bonding layer because it is used to “*wafer bond* the semiconductor layer to the semiconductor substrate.” Alie, [0055]; *see also* Alie, [0087]; Ex-1004 ¶179.

**d) 24[c]: “bonding the first bonding layer to a second bonding layer disposed on the support substrate; and”**

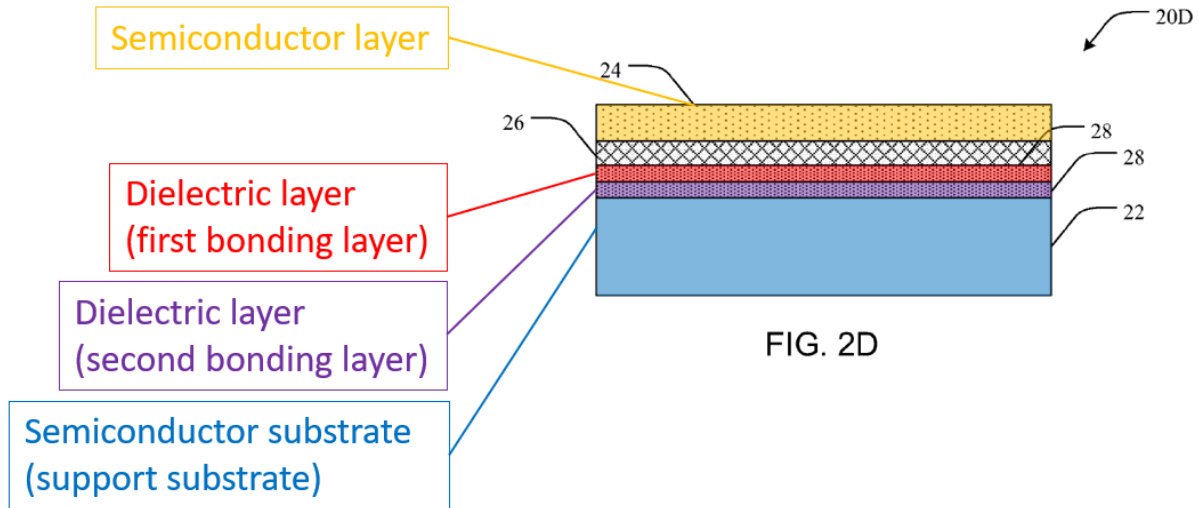
Alie discloses this limitation. Ex-1004 ¶¶180-82.

Alie discloses that “[t]he dielectric layer [i.e., the claimed first bonding layer] can be bonded directly to the semiconductor substrate [after being rotated 180° as shown in Figure 11B], *or to a second dielectric layer [i.e., the claimed second bonding layer] formed on the semiconductor substrate (not shown).*” Alie, [0105]; *see also* Ex-1004 ¶181.



Alie, Figs. 11A-B (annotated).

Figure 2D illustrates Alie's device with two bonding layers. Alie, [0059]; *see also* Ex-1004 ¶182.



Alie, Fig. 2D (annotated); *see also* Ex-1004 ¶.

- e) **24[d]: “creating a plurality of shallow trench isolation surface features on a light incident side of said semiconductor layer.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.<sup>3</sup> Ex-1004 ¶¶183-85.

As discussed above for limitation 1[b], Alie's surface features correspond to the claimed shallow trench isolation surface features on a light incident side of said semiconductor layer. Ex-1004 ¶184.

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<sup>3</sup> Claim 24 does not require limitation 24[d] to be performed after limitations 24[a]-[c]. *See Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1371 (Fed. Cir. 2003).

Alie discloses that surface features of its textured region “can be formed by wet etching the semiconductor material,” producing the claimed shallow trench isolation surface features. Alie, [0105]; *see also* Alie, [0104] (“a method of making a semiconductor device can include **wet etch texturing at least a portion of a surface of a semiconductor layer** to form a textured region”), [0072] (“a substrate such as **the semiconductor layer can be textured** and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern”); Ex-1004 ¶185. Alie also discloses chemically and/or structurally **altering the surface of a substrate such as the semiconductor layer**, “result[ing] in the formation of surface features appearing as structures or patterned areas on the surface.” Alie, [0077].

### 23. Claim 25

- a) **“The method of claim 24, wherein the step of creating the plurality of shallow trench isolation surface features comprises generating an array of surface features using shallow trench isolation etching.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case. Ex-1004 ¶¶186-89.

In the 737 Case, Petitioner proposed that the ’737 patent term “shallow trench isolation etching” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning, and to the extent a construction is required, it means, “etching a pattern of shallow trenches.” Ex-1014, 4; Ex-1015, 2-3.

As discussed above regarding limitation 24[d], Alie discloses etching a plurality of shallow trench isolation surface features. Alie, [0068], [0105]. Alie also discloses that “[n]on-limiting examples of shapes and configurations of surface features include ... gratings,” Alie, [0068], which are a series of trenches, i.e., the claimed array of surface features. *See* Ex-1003, 13:3-4 (“the shallow trench isolation can be a uniform grid pattern comprised of [trenches] that form a series of spaces and lines or pillars”); *see also* Ex-1004 ¶188.

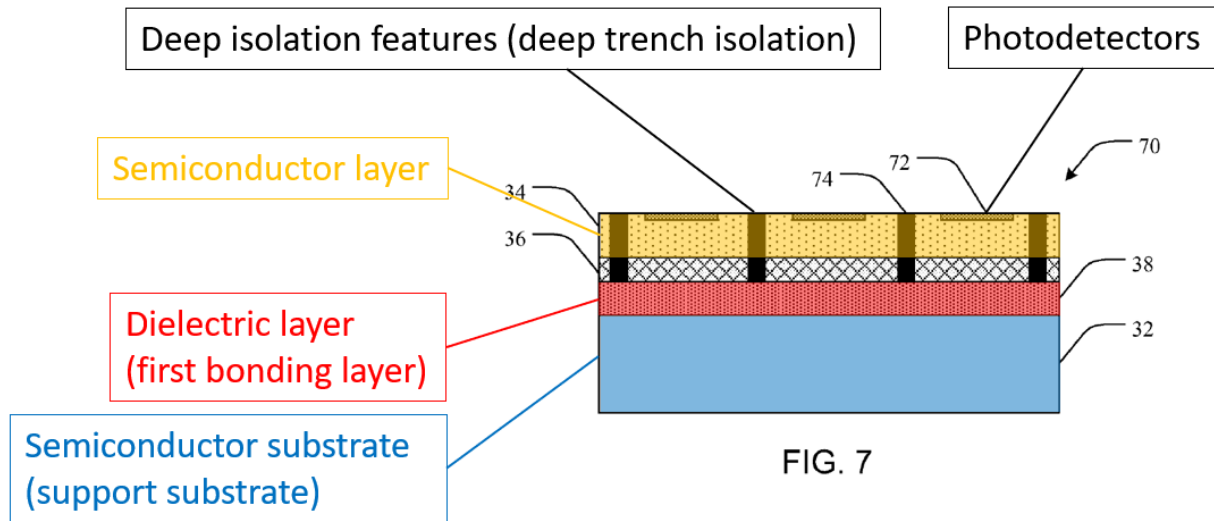
Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the surface features and the shallow trench isolation in Alie, as discussed above regarding limitation 1[b]. Ex-1004 ¶189.

#### **24. Claim 26**

**a) “The device of claim 1, further comprising deep trench isolation for isolating the device.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶190-95.

Figure 7 discloses deep isolation features (i.e., the claimed deep trench isolation) isolating each photodetector 72. Alie, [0097]; *see also* Ex-1004 ¶191.



Alie, Fig. 7 (annotated).

Other than having deep isolation features, the Figure 7 device is similar to the Figure 5 device discussed above regarding claim 1 (from which claim 26 depends) and meets claim 1 for the same reason. Ex-1004 ¶192.

It would also have been obvious to use the deep isolation features of Figure 7 to isolate Alie’s device disclosed in Figure 5. Ex-1004 ¶193. Alie teaches that “[t]he isolation features isolate each photodetector electrically, optically, or both electrically and optically” and “[i]solation features can thus maintain uniformity across an array by reducing optical and electrical crosstalk between the photodetectors.” Alie, [0097]; *see also KSR*, 550 U.S. at 418; Ex-1004 ¶193. A POSITA would have recognized the benefits of the deep isolation features of Figure 7 and used them to isolate Alie’s device disclosed in Figure 5. Ex-1004 ¶193.

This would have involved use of a known technique (i.e., deep isolation features) to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶194. Alie’s Figure 5 device and Figure 7 device share the same semiconductor layer 34, textured region 36, dielectric layer 38, and semiconductor substrate 32. *Compare* Alie, Fig. 5 *with* Alie, Fig. 7.

A POSITA would have had a reasonable expectation of success. Ex-1004 ¶195. It would have been well within the abilities of a POSITA to use deep trench isolation features to isolate the Figure 5 device, given that it would have involved routine manufacturing steps that Alie was already using for the embodiment depicted in Figure 7. Ex-1004 ¶195.

## **25. Claim 27**

### **a) “The device of claim 26, wherein said deep trench isolation provides light trapping functionality.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶196-97.

Alie discloses that its “isolation features isolate each photodetector ... optically,” i.e., the isolation features provide the claimed light trapping functionality. Alie, [0006]; *see also* Ex-1004 ¶197. Specifically, Alie discloses that its “isolation features regions can be configured to reflect incident electromagnetic radiation until it is absorbed, thereby increas[ing] the effective absorption length of the device.” Alie, [0099].

**26. Claim 28**

- a) **28[pre]: “An optoelectronic device having enhanced absorption of electromagnetic radiation, comprising:”**

Alie discloses the preamble to the extent it is limiting. Ex-1004 ¶¶198-99.

See discussion above regarding limitation 1[pre].

- b) **28[a]: “a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,”**

Alie discloses this limitation. Ex-1004 ¶¶200-01.

See discussion above regarding limitation 1[a].

- c) **28[b]: “a textured region comprising a plurality of shallow trench isolation surface features located on the light incident side of the semiconductor layer and configured to interact with incident electromagnetic radiation,”**

Alie renders this limitation obvious. Ex-1004 ¶¶202-03.

See discussion above regarding limitation 1[b].

- d) **28[c]: “a support substrate coupled to said semiconductor layer, and”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶204-05.

See discussion above regarding limitation 1[c].

- e) **28[d]: “a first bonding layer disposed between the semiconductor layer and the support substrate,”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶206-07.

See discussion above regarding limitation 1[d].

- f) **28[e]: “a second bonding layer positioned between the first bonding layer and the support substrate, and”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶208-09.

See discussion above regarding claim 19.

- g) **28[f]: “a reflector layer disposed between the first bonding layer and the second bonding layer.”**

Alie renders this limitation obvious. Ex-1004 ¶¶210-11.

See discussion above regarding claim 20.

## **27. Claim 29**

- a) **“The device of claim 28, wherein said shallow trench isolation surface features comprise pyramids.”**

Alie discloses this limitation. Ex-1004 ¶¶212-13.

See discussion above regarding claims 12 and 28.

## **28. Claim 30**

- a) **“The device of claim 28, wherein said plurality of shallow trench isolation surface features are formed by using a patterned mask and photolithography followed by etching.”**

Alie discloses this limitation. Ex-1004 ¶¶214-15.

See discussion above regarding claims 13 and 28.

**29. Claim 31**

- a) **“The device of claim 28, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.”**

Alie discloses this limitation. Ex-1004 ¶¶216-17.

See discussion above regarding claims 8 and 28.

**30. Claim 33**

- a) **“The device of claim 28, wherein the shallow trench isolation surface features are not uniform in height.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶218-19.

See discussion above regarding claims 5 and 28.

**31. Claim 34**

- a) **“The device of claim 28, wherein said plurality of shallow trench isolation surface features have a height in a range of about 50 nm to about 20 microns.”**

Alie renders this limitation obvious. Ex-1004 ¶¶220-21.

See discussion above regarding claims 11 and 28.

**32. Claim 35**

- a) **“The device of claim 28, wherein said photosensitive imager device is capable of detecting visible and infrared electromagnetic radiation.”**

Alie discloses this limitation under both Petitioner’s and Patent Owner’s proposed constructions in the 737 Case. Ex-1004 ¶¶222-23.

See discussion above regarding limitation 1[e] and claim 28.

**33. Claim 36**

- a) **“The device of claim 28, wherein said textured region enhances absorption of electromagnetic radiation within said semiconductor layer.”**

Alie discloses this limitation. Ex-1004 ¶¶224-25.

See discussion above regarding claims 15 and 28.

**34. Claim 37**

- a) **“The device of claim 28, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶226-27.

See discussion above regarding claims 16 and 28.

**35. Claim 38**

- a) **“The device of claim 28, wherein said textured region increases effective optical path length of light as it passes through the semiconductor layer.”**

Alie discloses this limitation. Ex-1004 ¶¶228-29.

See discussion above regarding claims 17 and 28.

**36. Claim 39**

- a) **“The device of claim 28, wherein said textured region allows the semiconductor layer to experience multiple passes of light.”**

Alie discloses this limitation. Ex-1004 ¶¶230-31.

See discussion above regarding claims 18 and 28.

**37. Claim 40**

- a) **“The device of claim 28, further comprising deep trench isolation for isolating the device.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶232-33.

See discussion above regarding claims 26 and 28.

**38. Claim 41**

- a) **“The device of claim 40, wherein said deep trench isolation provides light trapping functionality.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶234-35.

See discussion above regarding claims 27 and 28.

**39. Claim 42**

- a) **“The device of claim 28, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case. Ex-1004 ¶¶236-37.

See discussion above regarding claims 21 and 28.

**40. Claim 43**

- a) **“The device of claim 42, wherein the pattern is an at least substantially uniform grid.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶238-39.

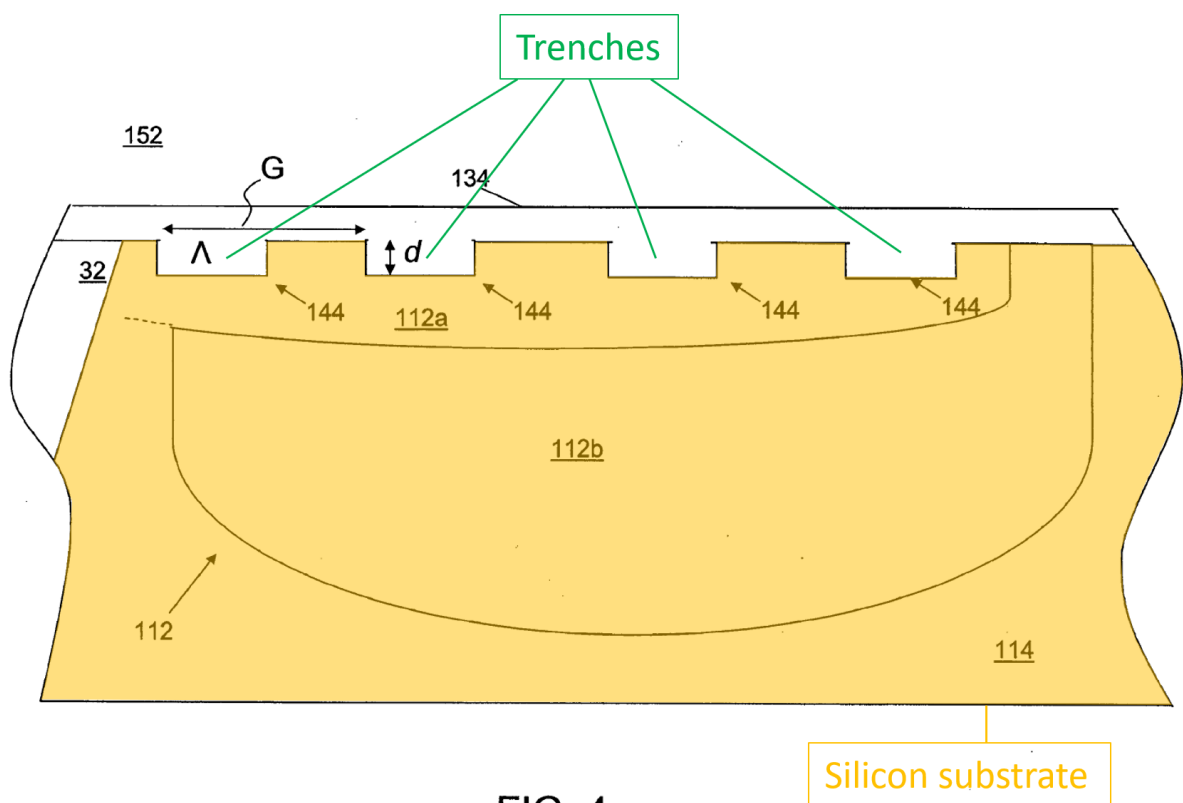
See discussion above regarding claims 22 and 28.

**B. Ground 2: Claims 4-5, 14, 21-22, 25, 32-33, and 42-43 Are Obvious Based on Alie and Baggenstoss**

**1. The Combination of Alie and Baggenstoss**

As discussed above regarding limitation 1[b], Alie discloses an optoelectronic device with a textured region. Alie, [0052], [0096], [0006]; *see also* Ex-1004 ¶240. Alie discloses that its textured region can include surface features. Alie, [0068]. “Non-limiting examples of shapes and configurations of surface features include ... gratings....” Alie, [0068].

Similarly, Baggenstoss discloses an optoelectronic device with a grated interface formed by trenches 144. Baggenstoss, [0031]-[0032], [0009]; Ex-1004 ¶241.



Baggenstoss, Fig. 4 (annotated).

In another embodiment, Baggenstoss discloses an optoelectronic device with a “blazed (or step-wise)” gratings formed of trenches 244. Baggenstoss, [0042]; *see also* Ex-1004 ¶242.

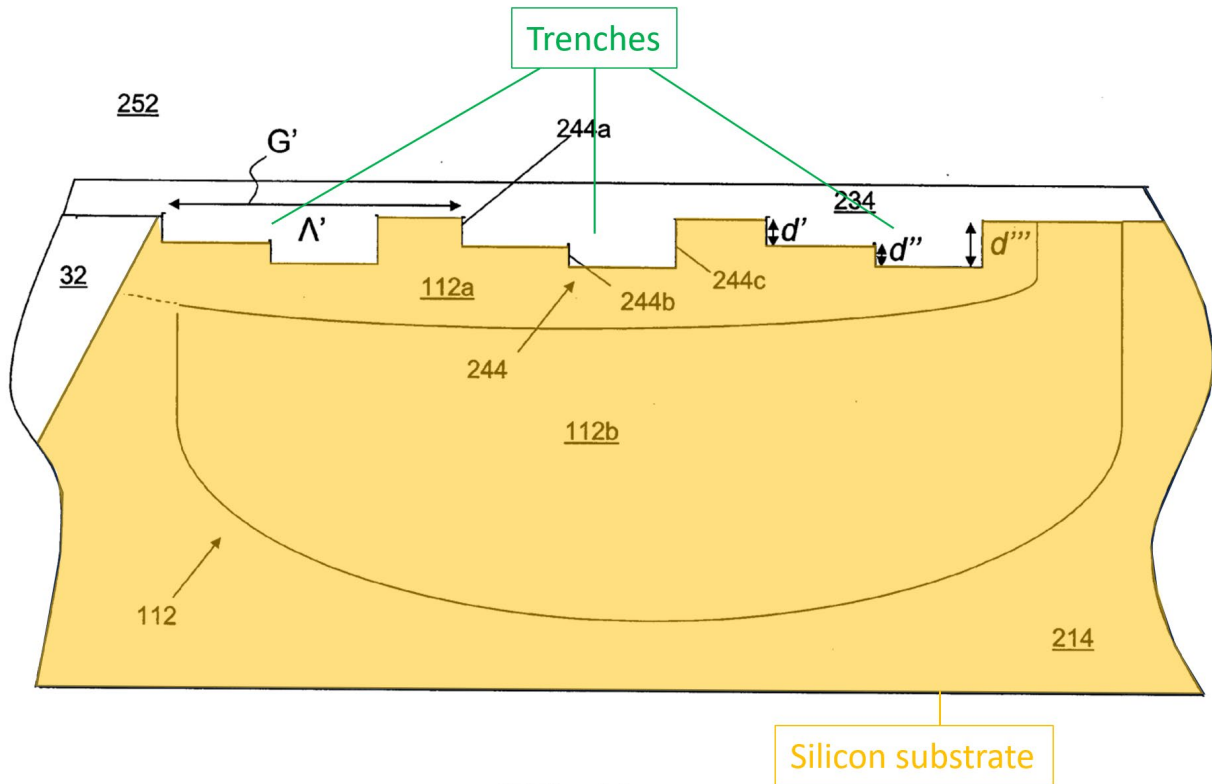


FIG. 11

Baggenstoss, Fig. 11 (annotated).

A POSITA would have looked to Baggenstoss’s discussion of trenches for more details on how to implement the surface features including gratings disclosed in *Alie. Ex-1004* ¶243. Baggenstoss teaches that its grated interface formed of trenches “allows a greater percentage of incident light to be captured, which is a vast improvement over the art.” Baggenstoss, [0014]; *see also KSR*, 550 U.S. at 418. Baggenstoss explains that its grated interface “serves to create a hybrid index of refraction ... thereby decreasing the percentage of incident light reflection.” Baggenstoss, [0031]. With the grated interface formed of trenches 144, the incident light reflection is “nearly eliminated” with a trench depth  $d$  of 100 nm. Baggenstoss,

[0035]. The “blazed” gratings formed of trenches 244 can decrease the incident light reflection even further. Baggenstoss, [0042]-[0043]. As Dr. Lebby explains, whether to use Baggenstoss’s trenches 144 or 244 would have depended on the particular design needs regarding the cost of manufacture and the desired amount of reduction in incident light reflection. Ex-1004 ¶243.

The use of Baggenstoss’s trenches in Alie’s devices would have involved use of a known technique to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶244. Both Alie and Baggenstoss disclose photodetectors. Alie, Abstract, [0006]; Baggenstoss, [0014], [0009]. Both Alie and Baggenstoss have the same goal of improving the efficiency of photodetectors in capturing incident light. Alie, [0068]; Baggenstoss, [0014]. Both Alie and Baggenstoss achieve that goal by using a textured region including surface features arranged as gratings. Alie, [0068]; Baggenstoss, [0031]-[0032], [0042]. Both Alie and Baggenstoss disclose placing the textured region on the light incident side. Alie, [0094] (“Additional scattering can be provided by positioning a textured forward scattering layer on the side of the device that receives incident electromagnetic radiation.”); Baggenstoss, [0038], Fig. 3 (depicting light source 38 on the side of the grated interface). Both Alie and Baggenstoss disclose forming the surface features using chemical etching. Alie, [0074]; Baggenstoss, [0038].

In addition, the use of Baggenstoss's trenches in Alie's devices would have been, at most, a simple substitution of one known element (i.e., Baggenstoss's trenches) for another (Alie's surface features) to obtain predictable results. *KSR*, 550 U.S. at 417; Ex-1004 ¶245. Again, because Alie discloses gratings, a POSITA would have understood that Baggenstoss's trenches, which are gratings, would work in Alie. Ex-1004 ¶245.

A POSITA would have had a reasonable expectation of success in arriving at this combination. Ex-1004 ¶246. As Dr. Lebby explains, it would have been well within the abilities of a POSITA to use the implementation details of Baggenstoss's trenches for Alie's surface features, given that it would have involved routine manufacturing steps, such as chemical etching, that Alie was already using for its surface features. Alie, [0074]; *see also* Ex-1004 ¶246.

## **2. Claim 4**

- a) “The device of claim 1, wherein the shallow trench isolation surface features have a substantially uniform height.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶247-53.

As discussed above in Section VIII.B.1, Baggenstoss discloses an optoelectronic device with a grated interface formed by trenches 144. Baggenstoss, [0031]-[0032], [0009]; Ex-1004 ¶248.

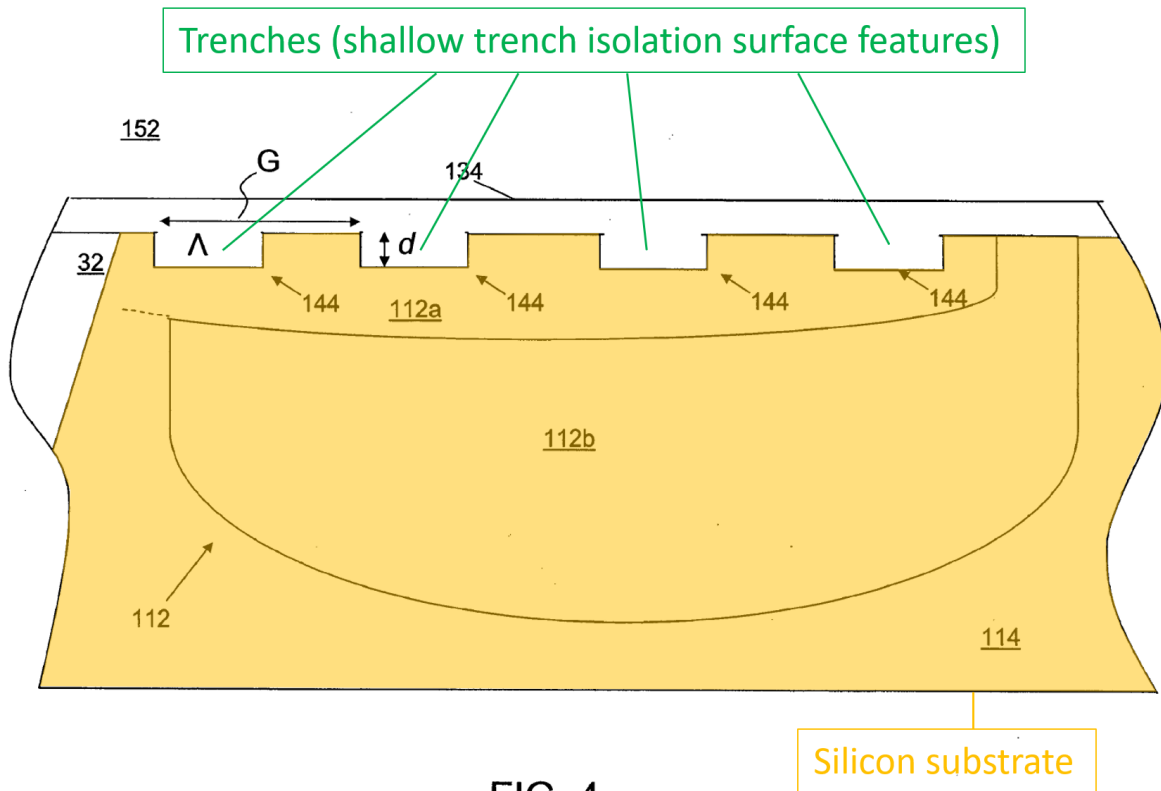


FIG. 4

Baggenstoss, Fig. 4 (annotated).

Baggenstoss's trenches 144 correspond to the claimed shallow trench isolation surface features. Ex-1004 ¶249. As Dr. Lebby explains, Baggenstoss's trenches 144 have the same structures as the shallow trench isolation surface features described in the specification of the '682 patent. Ex-1004 ¶249. Baggenstoss's trenches 144 form a grating, which is the same shape and configuration that the '682 patent provides as an example of shallow trench isolation surface features. '682 patent, 9:34-37 ("Non-limiting examples of such shapes and configurations include ... gratings...."). Baggenstoss also discloses that its trenches 144 can have a depth

of 100 nm (i.e., 0.1 micron), Baggenstoss, [0034], similar to the surface features of the '682 patent, '682 patent, 11:27-28; *see also* Ex-1004 ¶249.

Both Baggenstoss and the '682 patent describe the same or similar processes for creating the shallow trench isolation surface features. Ex-1004 ¶250. Baggenstoss discloses forming its trenches using “chemical etching, reactive ion etching (RIE), or other techniques for creating a recess in the silicon substrate.” Baggenstoss, [0038]. These are the same methods used to create shallow trench isolation surface features in the '682 patent, as explained in the provisional application for the '682 patent. Ex-1003, 11:16-22 (“Various methods can be utilized to form shallow trench isolation features.... Non-limiting examples can include chemical etching (e.g. anisotropic etching, isotropic etching) ... reactive ion etching ... or any other technique that can be used to form such a topology.”); *see also* Ex-1004 ¶250.

Both Baggenstoss and the '682 patent explain that their shallow trench isolation surface features serve the same function. Ex-1004 ¶251. Just as the '682 patent states that its “surface features ... interact with light,” '682 patent, 9:9-13, Baggenstoss discloses that its trenches 144 interact with light to decrease incident light reflection, Baggenstoss, [0035].

Baggenstoss discloses that the trenches 144 have a predetermined depth (i.e., the claimed height), represented by  $d$  in Figure 4. Baggenstoss, [0032]. The

predetermined depth  $d$  can be, for example, a constant depth of 100 nm. Baggenstoss, [0034]-[0035]. Baggenstoss's shallow trench isolation surface features, therefore, have a substantially uniform height, as required by this limitation. Ex-1004 ¶252.

Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the trenches and the shallow trench isolation in Baggenstoss. Ex-1004 ¶253. Baggenstoss discloses forming shallow trench isolation, e.g., element 32 in Figure 4. Baggenstoss, [0009]. As Dr. Lebby explains, the process for creating shallow trench isolation was well known. Ex-1004 ¶253. Creating the surface features using the same process as the process for the shallow trench isolation would generate predictable results, and reduce the costs associated with developing a new process. Ex-1004 ¶253. This would involve employing a known technique to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶253. A POSITA would have had a reasonable expectation of success because Baggenstoss already discloses using shallow trench isolation in its devices, and, as Dr. Lebby discusses, it was well known how to use a shallow trench isolation process to form surface features. Baggenstoss, [0009]; Ex-1012, [0066]; Ex-1034, [0010]-[0012]; *see also* Ex-1004 ¶253.

3. Claim 5

- a) “The device of claim 1, wherein the shallow trench isolation surface features are not uniform in height.”

As in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶254-60.

In another embodiment, Baggenstoss discloses an optoelectronic device with a “blazed (or step-wise)” gratings formed of trenches 244. Baggenstoss, [0042]; *see also* Ex-1004 ¶255.

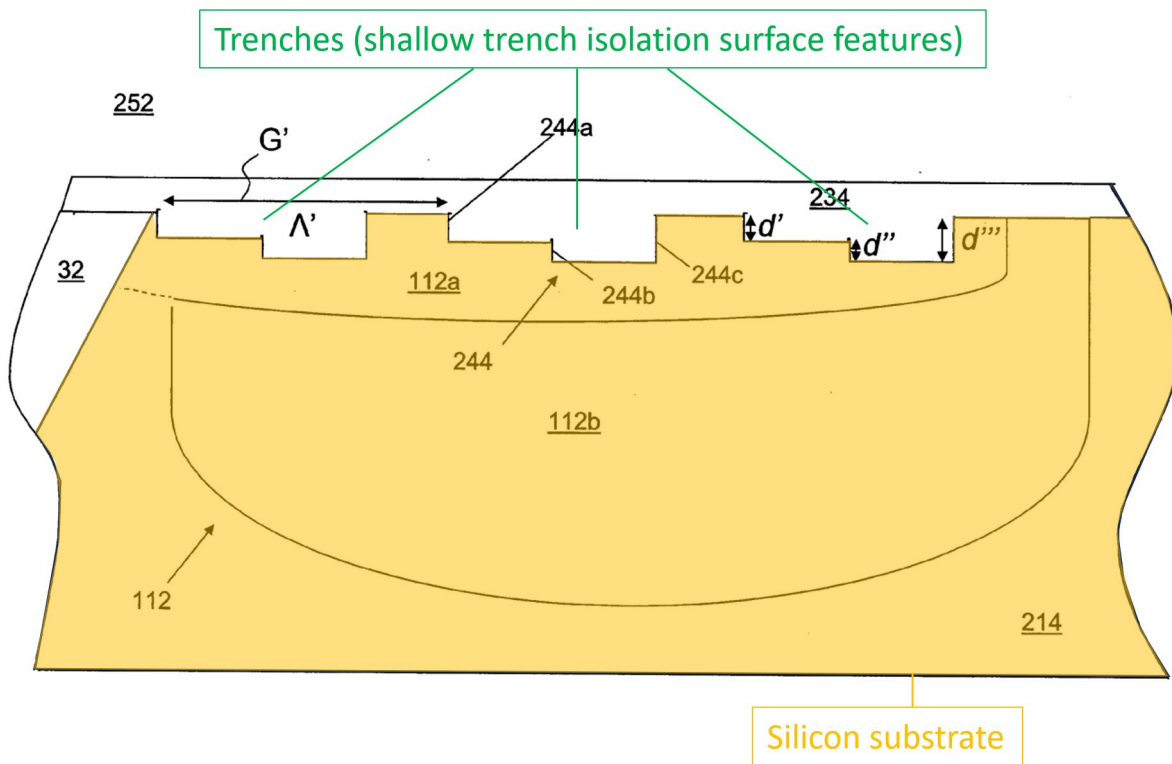


FIG. 11

Baggenstoss, Fig. 11 (annotated).

Baggenstoss’s trenches 244 correspond to the claimed shallow trench isolation surface features. Ex-1004 ¶256. As Dr. Lebby explains, Baggenstoss’s

trenches 244 have the same structures as the shallow trench isolation surface features described in the specification of the '682 patent. Ex-1004 ¶256. Baggenstoss's trenches 244 form a grating, which is the same shape and configuration that the '682 patent provides as an example of shallow trench isolation surface features. '682 patent, 9:34-37 ("Non-limiting examples of such shapes and configurations include ... gratings...."). Baggenstoss also discloses that the trenches 244 may have predetermined depths ranging "from about 10 nm to about 250 nm" (i.e., 0.01 to 0.25 microns). Baggenstoss, [0043], similar to the surface features of the '682 patent, '682 patent, 11:27-28; *see also* Ex-1004 ¶256.

Both Baggenstoss and the '682 patent describe the same or similar processes for creating the shallow trench isolation surface features. Ex-1004 ¶257. Baggenstoss discloses forming its trenches using "chemical etching, reactive ion etching (RIE), or other techniques for creating a recess in the silicon substrate." Baggenstoss, [0038]; *see also* Baggenstoss, [0043] ("The trenches 244 could be formed by any of the methods described above with respect to [trenches 144 in] FIG. 4"). These are the same methods used to create shallow trench isolation surface features in the '682 patent, as explained in the provisional application for the '682 patent. Ex-1003, 11:16-22 ("Various methods can be utilized to form shallow trench isolation features.... Non-limiting examples can include chemical etching (e.g.

anisotropic etching, isotropic etching) ... reactive ion etching ... or any other technique that can be used to form such a topology.”); *see also* Ex-1004 ¶257.

Both Baggenstoss and the ’682 patent explain that their shallow trench isolation surface features serve the same function. Ex-1004 ¶258. Just as the ’682 patent states that its “surface features ... interact with light,” ’682 patent, 9:9-13, Baggenstoss discloses that its trenches 244 interact with light to decrease incident light reflection, Baggenstoss, [0042].

As shown in Figure 11, the trenches 244 have two different depths (i.e., the claimed heights). Baggenstoss, [0043]. Thus, the shallow trench isolation surface features are not uniform in height, as required by this limitation. Ex-1004 ¶259. Baggenstoss discloses that its trenches can be formed by chemical etching. Baggenstoss, [0038], [0043]; *see also* Ex-1004 ¶259. Typically, two masks would be required to etch the two different depths of the trenches 244. Ex-1004 ¶259.

Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the trenches and the shallow trench isolation in Baggenstoss, for the same reason discussed above regarding claim 4. Ex-1004 ¶260.

#### 4. Claim 14

- a) “The device of claim 1, wherein said plurality of shallow trench isolation surface features comprise multiple etched levels.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶261-63.

As discussed above regarding claim 5, Baggenstoss discloses trenches 244 (i.e., the claimed shallow trench isolation surface features) with two different depths. Baggenstoss, [0043]; *see also* Ex-1004 ¶262.

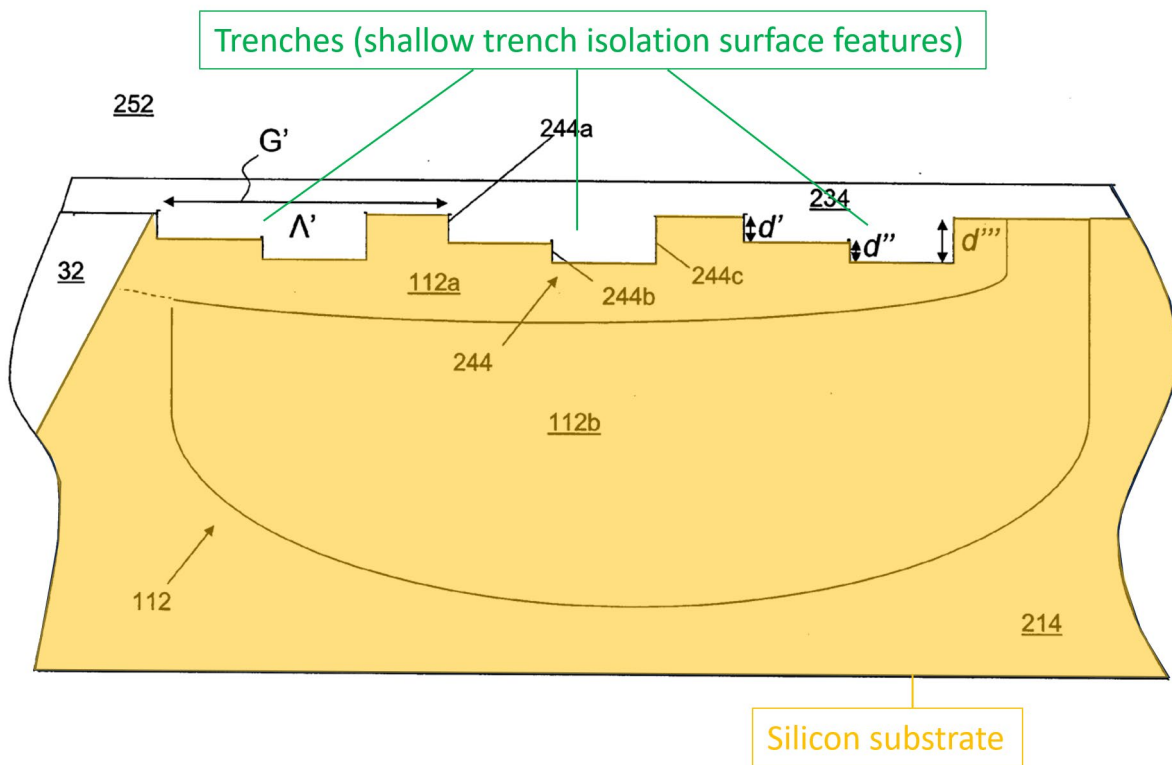


FIG. 11

Baggenstoss, Fig. 11 (annotated).

The different depths correspond to the claimed multiple etched levels because Baggenstoss's trenches 244 can be formed via chemical etching. Baggenstoss, [0038], [0043]; *see* Ex-1004 ¶263. Typically, two masks would be required to etch the two different depths of the trenches 244. Ex-1004 ¶263.

**5. Claim 21**

- a) “The device of claim 1, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

Alie in view of Baggenstoss renders this limitation obvious under Patent Owner's proposed construction in the 737 Case. Ex-1004 ¶¶264-67.

In the 737 Case, Petitioner proposed that the '737 patent term “the surface features are arranged according to a pattern” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning and that, to the extent a construction is required, it means “features coincident with at least one surface that are arranged in a repeating manner.” Ex-1014, 4.

As discussed above regarding claim 4, Figure 4 of Baggenstoss depicts a grated interface formed by trenches 144 (i.e., the claimed shallow trench isolation surface features). Baggenstoss, [0031]-[0032]; *see also* Ex-1004 ¶266.

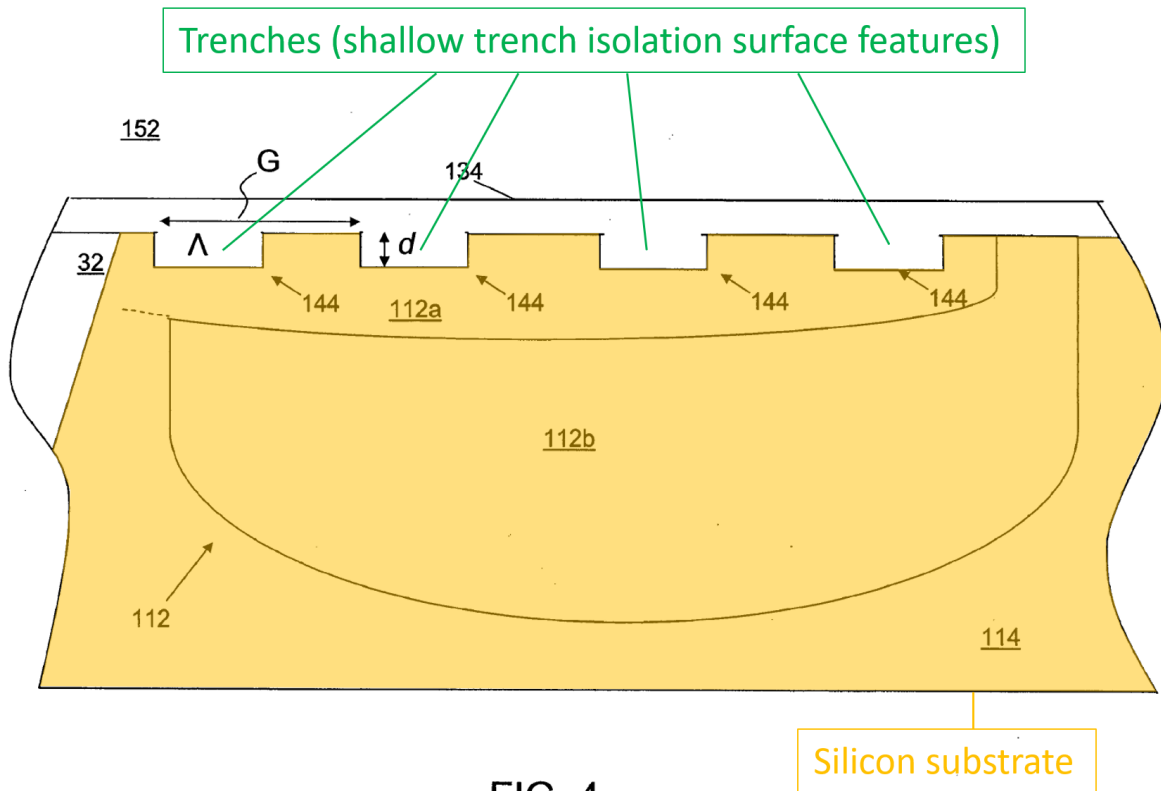


FIG. 4

Baggenstoss, Fig. 4 (annotated).

“Each grating (measured as the distance from the beginning of one trench 144 to the beginning of the next trench 144 (shown by arrow G)) has a predetermined period that is represented by  $\Lambda$ .” Baggenstoss, [0032]. The predetermined period  $\Lambda$  can be, for example, 340 nm. Baggenstoss, [0034]. Baggenstoss’s trenches are features coincident with at least one surface that are arranged in a repeating manner, and are an example of a pattern provided by the provisional application for the ’682 patent. Ex-1003, 13:2-4 (“[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a *uniform grid pattern* comprised of [trenches] that form *a series of spaces and lines* or pillars.”); see also Ex-1004 ¶267.

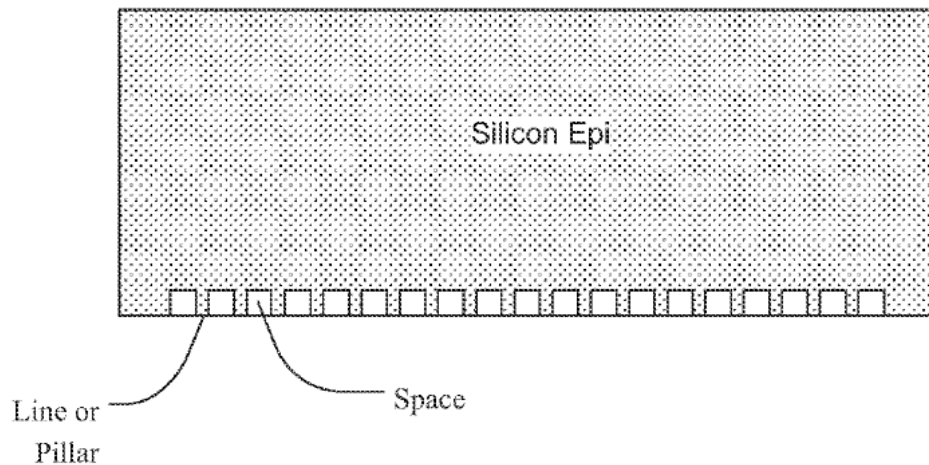


FIG. 5

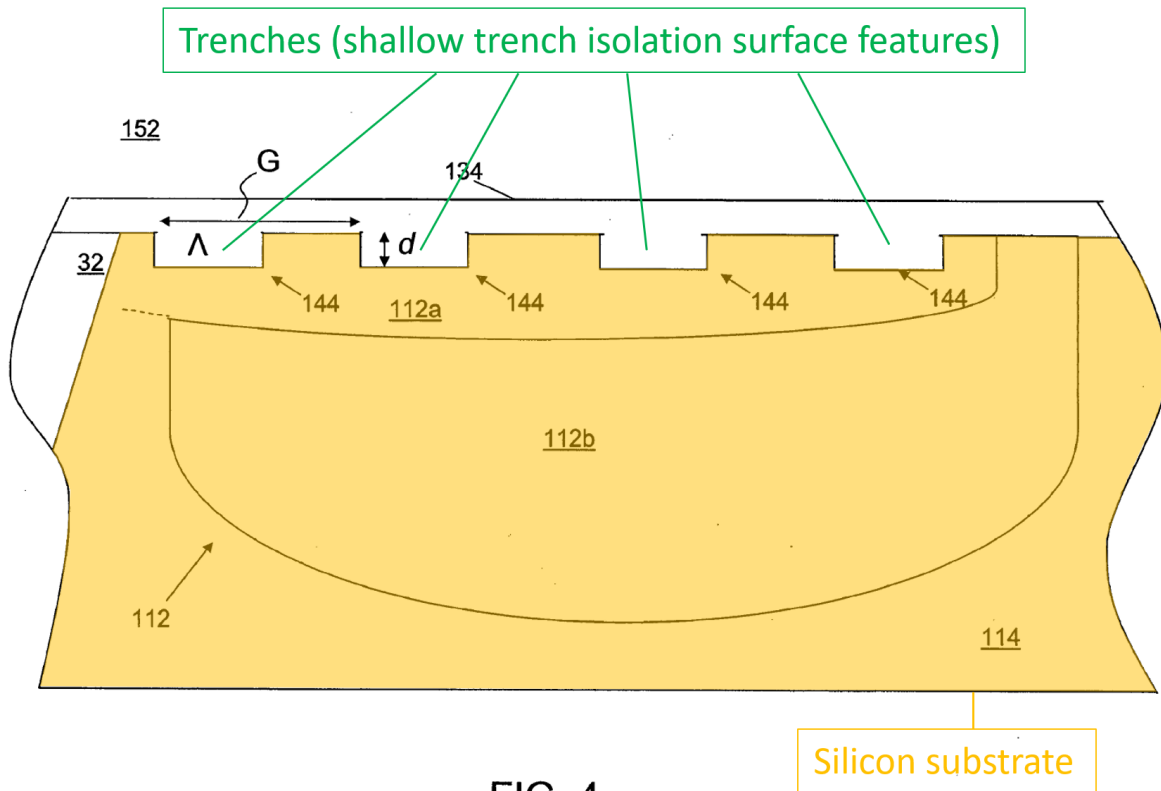
Ex-1003, Fig. 5.

**6. Claim 22**

- a) **“The device of claim 21, wherein the pattern is an at least substantially uniform grid.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶268-70.

As discussed above regarding claim 4, Figure 4 of Baggenstoss depicts a grated interface formed by trenches 144 (i.e., the claimed shallow trench isolation surface features). Baggenstoss, [0031]-[0032]; *see also* Ex-1004 ¶269.



Baggenstoss, Fig. 4 (annotated).

“Each grating (measured as the distance from the beginning of one trench 144 to the beginning of the next trench 144 (shown by arrow G) has a predetermined period that is represented by  $\Lambda$ ,” i.e., the trenches form the claimed substantially uniform grid. Baggenstoss, [0032]; *see also* Ex-1004 ¶270. The provisional application for the ’682 patent identifies such gratings as an example of a “uniform grid pattern.” Ex-1003, 13:2-4 (“[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a *uniform grid pattern* comprised of [trenches] that form *a series of spaces and lines* or pillars.”).

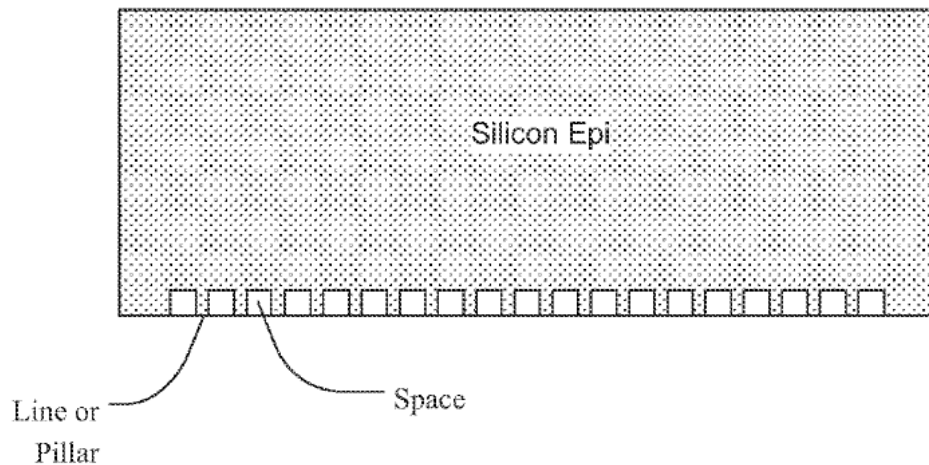


FIG. 5

Ex-1003, Fig. 5.

**7. Claim 25**

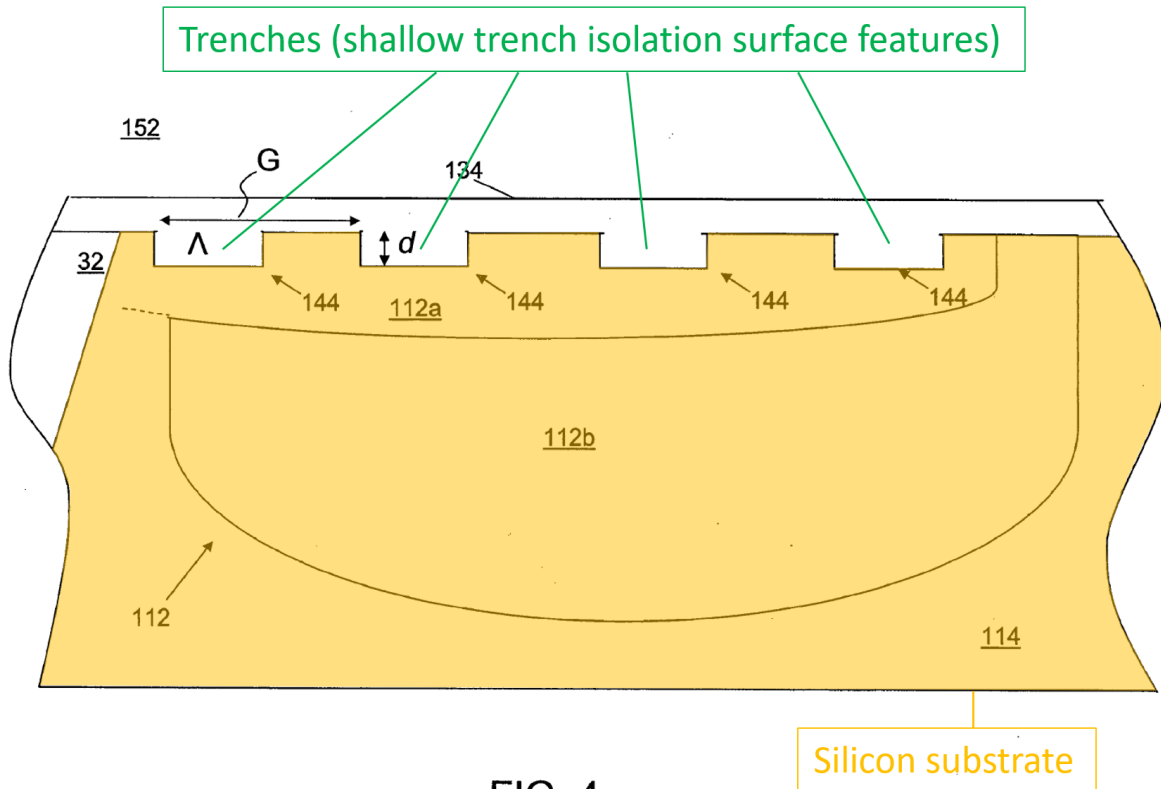
- a) **“The method of claim 24, wherein the step of creating the plurality of shallow trench isolation surface features comprises generating an array of surface features using shallow trench isolation etching.”**

Alie in view of Baggenstoss renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case. Ex-1004 ¶¶271-75.

In the 737 Case, Petitioner proposed that the ’737 patent term “shallow trench isolation etching” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning, and to the extent a construction is required, it means, “etching a pattern of shallow trenches.” Ex-1014, 4; Ex-1015, 2-3.

As discussed above regarding claim 4, Baggenstoss discloses creating an optoelectronic device with a grated interface formed by trenches 144 (i.e., the

claimed plurality of shallow trench isolation surface features comprising an array of surface features). Baggenstoss, [0031]-[0032], [0009]; Ex-1004 ¶273.



Baggenstoss, Fig. 4 (annotated).

As discussed above regarding claim 4, Baggenstoss discloses that its shallow trench isolation surface features are formed by etching a pattern of shallow trenches. Baggenstoss, [0038]; *see also* Ex-1004 ¶274.

Moreover, to the extent the claim requires the shallow trench isolation surface features to be formed by the same process used to create shallow trench isolation in a given device, it would have been obvious to use the same process to form both the

trenches and the shallow trench isolation in Baggenstoss, as discussed above regarding claim 4. Ex-1004 ¶¶275.

**8. Claim 32**

- a) **“The device of claim 28, wherein the shallow trench isolation surface features have a substantially uniform height.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶276-77.

See discussion above regarding claims 4 and 28.

**9. Claim 33**

- a) **“The device of claim 28, wherein the shallow trench isolation surface features are not uniform in height.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶278-79.

See discussion above regarding claims 5 and 28.

**10. Claim 42**

- a) **“The device of claim 28, wherein the shallow trench isolation surface features are arranged according to a pattern.”**

Alie in view of Baggenstoss renders this limitation obvious under Patent Owner’s proposed construction in the 737 Case. Ex-1004 ¶¶280-81.

See discussion above regarding claims 21 and 28.

**11. Claim 43**

- a) **“The device of claim 42, wherein the pattern is an at least substantially uniform grid.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶282-83.

See discussion above regarding claims 22 and 28.

**C. Ground 3: Claims 23 and 44 Are Obvious Based on Alie and Haddad204**

**1. Claim 23**

- a) **“The device of claim 21, wherein the pattern is a non-uniform arrangement.”**

Alie in view of Haddad204 renders this limitation obvious. Ex-1004 ¶¶284-89.

As discussed above regarding limitation 1[b] in Ground 1, Alie discloses an optoelectronic device with a textured region. Alie, [0052], [0096], [0006]; *see also* Ex-1004 ¶285. Alie discloses that its textured region can include surface features such as pillars. Alie, [0068].

Similarly, Haddad204 discloses an optoelectronic device with a textured region including surface features such as pillars. Haddad204, [0073], [0053]. Importantly, Haddad204 discloses “a plurality of pillars of variable sizes ... arranged in a non-uniform array.” Haddad204, [0112]; *see also* Ex-1004 ¶286. Figure 9a

shows a top view and Figure 9b shows a cross-sectional view of such “pillars etched into a semiconductor material.” Haddad204, [0112].

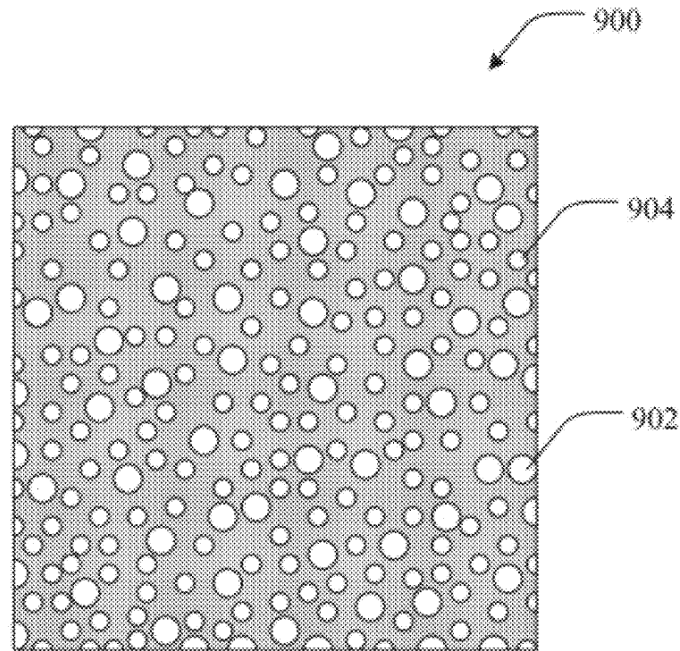


FIG. 9a

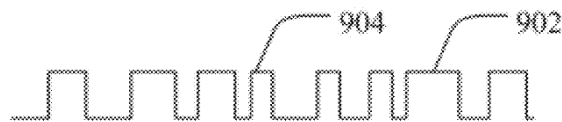


FIG. 9b

Haddad204, Figs. 9a-b.

A POSITA would have looked to Haddad204 for more details on how to implement the surface features including pillars disclosed in Alie. Haddad204 teaches that its surface features “increase the effective absorption length of the photosensitive pixel,” which in turn, increases the quantum efficiency. Haddad204,

[0073], [0076]; *see also KSR*, 550 U.S. at 418; Ex-1004 ¶287. Increasing quantum efficiency using surface features is the same goal shared by Alie. Alie, [0070]. Haddad204 teaches that “[a]ny increase in the quantum efficiency makes a large difference in the signal to noise ratio.” Haddad204, [0058]. Alie similarly teaches that an increase in the quantum efficiency “lead[s] to an improved signal to noise ratio.” Alie, [0070].

Combining Alie with Haddad204 would have involved use of a known technique (i.e., Haddad204’s non-uniform arrangement) to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶288. Both Alie and Haddad204 share the same two joint inventors: Jeffrey McKee and Chintamani Palsule. Both Alie and Haddad204 concern photodetectors with textured regions that increase quantum efficiency. Alie, [0068], [0006]; Haddad204, [0073], [0053]. The textured regions in both references include similarly shaped surface features such as pillars. Alie, [0068]; Haddad204, [0073]. The textured regions in both references can be formed by chemical etching. Alie, [0074]; Haddad204, [0093]. Both Alie and Haddad204 disclose placing the textured regions on the light incident side. Alie, [0094] (“Additional scattering can be provided by positioning a textured forward scattering layer on the side of the device that receives incident electromagnetic radiation.”); Haddad204, [0111] (“texturing can be applied to the light-incident

surface of the semiconductor substrate in order to facilitate additional scattering as light enters the device”).

A POSITA would have had a reasonable expectation of success in making this combination. Ex-1004 ¶289. As Dr. Lebby explains, it would have been well within the abilities of a POSITA to use Haddad204’s non-uniform arrangement of pillars for Alie’s arrangement of pillars, given that it would have involved routine manufacturing steps that Haddad204 had already used in its devices with predictable results. Ex-1004 ¶289.

**2. Claim 44**

- a) “The device of claim 42, wherein the pattern is a non-uniform arrangement.”**

Alie in view of Haddad204 renders this limitation obvious. Ex-1004 ¶¶290-91.

See discussion above regarding claims 23 and 28.

**D. Ground 4: Claims 23 and 44 Are Obvious Based on Alie and Park**

**1. Claim 23**

- a) “The device of claim 21, wherein the pattern is a non-uniform arrangement.”**

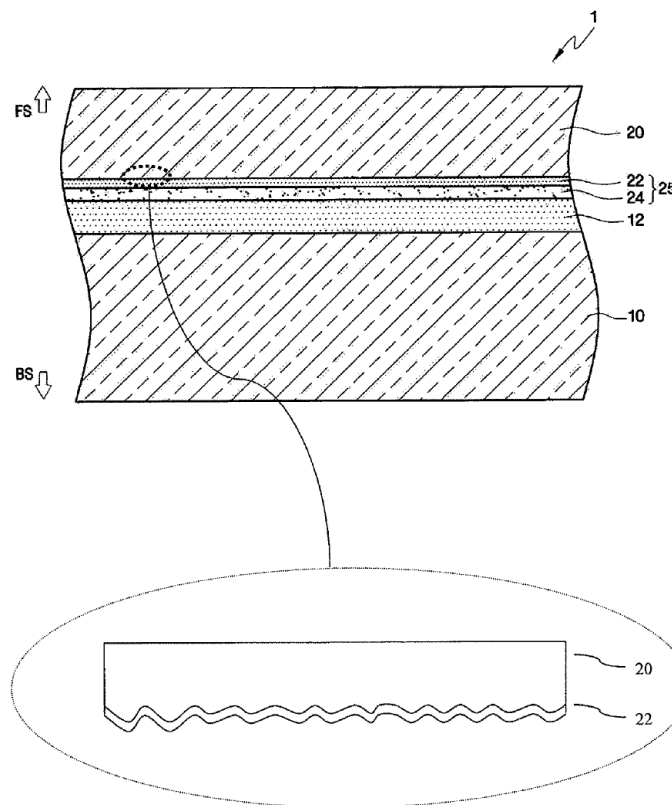
Alie in view of Park renders this limitation obvious. Ex-1004 ¶¶292-97.

As discussed above regarding limitation 1[b], Alie discloses an optoelectronic device with a textured region. Alie, [0052], [0096], [0006]; *see also* Ex-1004 ¶293.

Alie discloses that its textured region can include surface features such as protrusions. Alie, [0068].

Similarly, Park discloses an optoelectronic device with a textured region including surface features with protrusions. Park, [0072] (“Referring to the inset in FIG. 1 ... reflections may also be reduced by processing the second substrate 20 to have an *uneven surface* facing the oxide layer 22.”), [0059] (“FIGS. 1 to 7 illustrate cross-sectional views of stages in a method of fabricating an image sensor”); *see also* Ex-1004 ¶294.

FIG. 1



Park, Fig. 1. “The oxide layer 22 may have an uneven surface where it meets the

second substrate 20.” Park, [0072]. “The oxide layer 22 may also have an uneven surface at the opposing surface.” Park, [0072]. As its name suggests, and as depicted in Figure 1, Park’s uneven surface has protrusions in a non-uniform arrangement. Ex-1004 ¶294.

A POSITA would have looked to Park for more details on how to implement the surface features including protrusions disclosed in Alie. Park teaches that its uneven surface helps with absorbing incident light by reducing reflection. Park, [0072]; *see also KSR*, 550 U.S. at 418; Ex-1004 ¶295. Decreasing reflection of incident light means more light entering the silicon substrate to be absorbed. Ex-1004 ¶295. Alie teaches that increased absorption of incident light increases quantum efficiency, Alie, [0068], and that an increase in the quantum efficiency “lead[s] to an improved signal to noise ratio.” Alie, [0070]. Based on the teachings of Park and Alie, a POSITA would have been motivated to use Park’s non-uniform arrangement. Ex-1004 ¶295.

Combining Alie with Park would have involved use of a known technique (i.e., Park’s non-uniform arrangement) to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶296. Both Alie and Park concern increasing quantum efficiency of photodetectors. Alie, [0068], [0070], [0006]; Park, [0004]-[0005], Fig. 7. To achieve this goal, Alie uses a textured region with protrusions and Park similarly uses an uneven surface with protrusions. Alie, [0068]; Park, [0072].

Both Alie and Park disclose placing the textured region or the uneven surface on the light incident side. Alie, [0094] (“Additional scattering can be provided by positioning a textured forward scattering layer on the side of the device that receives incident electromagnetic radiation.”); Park, Figs. 1, 7.

A POSITA would have had a reasonable expectation of success in making this combination. Ex-1004 ¶297. As Dr. Lebby explains, it would have been well within the abilities of a POSITA to use Park’s non-uniform arrangement of protrusions for Alie’s arrangement of protrusions, given that it would have involved routine manufacturing steps that Park had already used in its devices with predictable results. Ex-1004 ¶297.

## **2. Claim 44**

### **a) “The device of claim 42, wherein the pattern is a non-uniform arrangement.”**

Alie in view of Park renders this limitation obvious. Ex-1004 ¶¶298-99.

See discussion above regarding claims 23 and 28.

## **IX. SECONDARY CONSIDERATIONS**

Petitioner is unaware of evidence of secondary considerations of non-obviousness. Petitioner reserves the right to rebut any purported objective evidence of non-obviousness raised by Patent Owner.

**X. THE BOARD SHOULD NOT USE ITS DISCRETION TO DENY INSTITUTION**

**A. 35 U.S.C. § 314(a)**

The Board should not exercise its discretion to deny institution under 35 U.S.C. §314(a). No other petitions have been filed against the '682 patent and thus the *General Plastic* factors for serial petitions do not weigh against institution. Under *Apple Inc. v. Fintiv, Inc.*, IPR2020-0019, Paper 11 (March 20, 2020) (precedential), the district court litigation is still at an early stage, and trial on issues including the validity of the '682 patent is scheduled for April 2026. In addition, the other *Fintiv* factors would not justify denying institution. By the time of institution, the district court's claim construction briefing would not have even begun, and the fact discovery deadline would be about five months away. Discretionary denial is further inappropriate here because this petition presents compelling evidence of unpatentability. Accordingly, the *Fintiv* factors should not be applied to deny institution of this proceeding.

**XI. CONCLUSION**

Petitioner respectfully requests *inter partes* review and cancellation of the Challenged Claims of the '682 patent.

Petition for *Inter Partes* Review of U.S. Pat. No. 10,347,682

Date: November 22, 2024

Respectfully submitted,

By: /Scott C. Weidenfeller/

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## **CERTIFICATION OF WORD COUNT**

I certify that the foregoing complies with the type-volume limitation of 37 C.F.R. § 42.24 and contains 13,951 words based on the word count indicated by the word-processing system used to prepare the paper, and excluding those portions exempted by § 42.24(a).

Date: November 22, 2024

/Scott C. Weidenfeller/

Scott C. Weidenfeller (Reg. No. 54,531)

## CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6 and 42.105, I hereby certify that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,347,682 under U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq.*, together with its supporting exhibits, Petitioner’s Explanation of Parallel Petitions, and Power of Attorney was served by Federal Express for Saturday delivery, a means at least as fast and reliable as Priority Mail Express®, on the following correspondence address of record for patent owner:

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Date: November 22, 2024

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