

U.S. Patent No. 8,549,339 (“’339 Patent”)

Accused Products

MediaTek’s SoC products comprising two or more sets of processors supporting or based on the DynamIQ Shared Unit architecture (*e.g.*, ARMv8.2, ARMv9 ARMv9.2, and successors), including without limitation the Helio X20 (MT6797), Helio X23 (MT6797D), Helio X25 (MT6797T), Helio X27 (MT6797X), Helio X30 (MT6799), Helio P60 (MT6771), Helio P65 (MT6768), Helio P70 (MT6771V/CT, MT6771V/WT), Helio P90 (MT6779V/CU), Helio G70 (MT6769V/CB), Helio G80 (MT6769T, MT6769V/CT, MT6769V/CU), Helio G85 (MT6769Z, MT6769V/CZ), Helio G88 (MT6769H), Helio G91 (MT6769G), Helio G90 (MT6785V/CD), Helio G90T (MT6785V/CC), Helio G95 (MT6785V/CD), Helio G96 (MT6781, MT6781V/CD), Helio G99 (MT6789, MT6789G, MT6789U, MT6789V/CD, MT8781, MT8781V/CA, MT8781V/NA), Helio G100, Dimensity 700 aka Dimensity 6020 (MT6833, MT6833G, MT6833V/ZA, MT6833V/NZA), Dimensity 720 (MT6853V/ZA, MT6853V/NZA), Dimensity 800 (MT6853T, MT6853V/TNZA), Dimensity 800 (MT6873), Dimensity 810 aka Dimensity 6080 (MT6833P, MT6833GP, MT6833V/PNZA), Dimensity 820 (MT6875), Dimensity 900 (MT6877, MT6877V/ZA), Dimensity 920 (MT6877, MT6877T, MT6877V/TZA), Dimensity 930 aka Dimensity 7020 (MT6855, MT6855V/AZA), Dimensity 1000C (MT6883Z/CZA), Dimensity 1000L (MT6885Z/CZA), Dimensity 1000 (MT6889), Dimensity 1000+ (MT6889Z/CZA), Dimensity 1050 aka Dimensity 7030 (MT6879, MT6879V/ZA, MT6879V_T/ZA), Dimensity 1080 aka Dimensity 7050 (MT6877, MT6877V/TTZA, MT6877V_T/TTZA), Dimensity 1100 aka Dimensity 8020 (MT6891, MT6891Z/CZA, MT6891Z_Z/CZA), Dimensity 1200 (MT6893, MT6893Z/CZA, MT6893Z_A/CZA), Dimensity 1300 aka Dimensity 8050 (MT6893Z, MT6893Z_T/CZA), Dimensity 6100+ (MT6835 MT6835V/ZA MT8755V/TZB), Dimensity 6300 (MT6835T), Dimensity 7025, Dimensity 7200 (MT6886, MT6886V_A/CZA, MT6886V_B/CZA), Dimensity 7300 (MT6878), Dimensity 7300X, Dimensity 7350, Dimensity 8000 (MT6895, MT6895Z/CZA), Dimensity 8100 (MT6895Z, MT6895Z/TCZA, MT6895Z_A/TCZA, MT6895Z_B/TCZA, MT6895ZB, MT8795, MT8795Z/TNZA), Dimensity 8200 (MT6896, MT6896Z, MT6896Z/CZA, MT6896Z_B/CZA), Dimensity 8250, Dimensity 8300 (MT6897, MT6897Z_A/ZA), Dimensity 9000 (MT6983, MT6983Z/CZA, MT8798, MT8798Z/CNZA), Dimensity 9000+ (MT6983, MT6983W/CZA, MT8798, MT8798Z/TNZA), Dimensity 9200 (MT6985), Dimensity 9200+ (MT6985, MT6985W/TCZA), Dimensity 9300 (MT6989, MT6989W/CZA, MT8796, MT8796W/CNZA), Dimensity 9300+, Kompanio 500 aka Helio P60T (MT8183), Kompanio 520 (MT8186), Kompanio 528 (MT8186T), Kompanio 800T, Kompanio 820 (MT8192), Kompanio 828, Kompanio 838, Kompanio 900T (MT8791), Kompanio 1200 (MT8195), Kompanio 1380 (MT8195T), Kompanio 1300T (MT8797), MT8135, MT8135V, MT8173, MT8176, MT8693, MT5329, MT8385 (i500), and all variants and iterations thereof (collectively, “Accused Products”), infringe at least Claims 1, 5, 8, 9, 10, 14, and 21 of the ’339 Patent.

Each Accused Product infringes the claims in substantially the same way, and the evidence shown in this chart is similarly applicable to each Accused Product. For example, each Accused Product includes a DynamIQ Shared Unit or big.LITTLE architecture and, on information and belief, implements substantially the same architectural features described in the reference documentation cited in this chart. Thus, the descriptions and evidence below relating to the MT6983 and Kompanio 1380 (MT8195T) representative products are similarly applicable to the remaining Accused Products listed above (for DynamIQ and big.LITTLE architectures

respectively). Each claim limitation is literally infringed by each Accused Product. However, to the extent any claim limitation is not met literally, it is nonetheless met under the doctrine of equivalents because the differences between the claim limitation and each Accused Product would be insubstantial, and each Accused Product performs substantially the same function, in substantially the same way, to achieve the same result as the claimed invention. Notably, MediaTek has not yet articulated which, if any, particular claim limitations it believes are not met by the Accused Products.

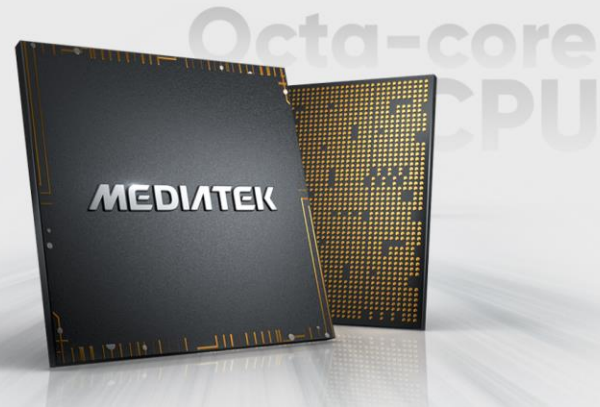
Claim 1

Claim 1	Accused Products
1. A multi-core processor, comprising:	To the extent the preamble is limiting, each Accused Product comprises a multi-core processor. For example, the MT6983 comprises eight cores implementing the ARM DynamIQ Shared Unit-110 architecture. In a further example, the MT8195T comprises ten cores implementing the ARM big.LITTLE architecture. <i>See, e.g.:</i>

Claim 1	Accused Products
	Elevated Speed. Maximized Gaming. • Industry-leading TSMC N4 (4nm-class) chip production process • Our fastest ever Arm Mali-G710 MC10 graphics processor • Ultra-Core - 1x Arm Cortex-X2 at 3.2GHz • Super-Cores - 3x Arm Cortex-A710 up to 2.85GHz • Efficiency Cores - 4x Arm Cortex-A510 • Big in-chip caches: 8MB CPU L3 cache + 6MB system-level cache (SLC) • LPDDR5X 7500Mbps support – 20% more power efficient than LPDDR5 Our fastest ever flagship chip: We've increased peak clock speeds of the Arm Cortex-X2 CPU and Arm Mali-G710 MC10 graphics engine even further to raise performance to the next level! https://www.mediatek.com/products/smartphones-2/mediatek-dimension-9000plus

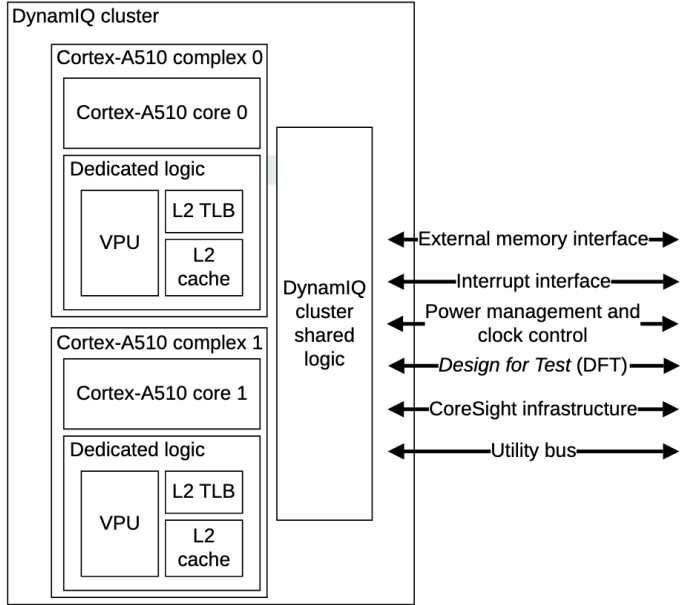
Claim 1	Accused Products								
	Arm DynamIQ Shared Unit-110 ▪DSU-110 for Cache Coherency & Shared L3\$ ▪Optimized Ring Transport Network –Bi-directional, Dual-ring ▪2X Bandwidth and 25% Lower Leakage –Support Partial SRAM & Logic Shutdown ▪Cache Partition for QoS <table border="1"> <thead> <tr> <th>Scenario</th> <th>Leakage Power (Relative)</th> </tr> </thead> <tbody> <tr> <td>Previous generation fully active</td> <td>100%</td> </tr> <tr> <td>DSU-110 fully active</td> <td>25% lower</td> </tr> <tr> <td>DSU-110 Partial powerdown</td> <td>75% lower</td> </tr> </tbody> </table> MEDIATEK 11 Presentation “Dimensity 9000 – A Flagship Smartphone SoC” by Ericbill Wang of MediaTek and Stefan Rosinger and Saurabh Pradhan of ARM, <i>available at</i> https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/HC2022.Mediatek.EricbillWang.v08.pptx.pdf	Scenario	Leakage Power (Relative)	Previous generation fully active	100%	DSU-110 fully active	25% lower	DSU-110 Partial powerdown	75% lower
Scenario	Leakage Power (Relative)								
Previous generation fully active	100%								
DSU-110 fully active	25% lower								
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Claim 1	Accused Products
	Built on the first ever Armv9 CPUs Dimensity 9000 is the first chipset announced that adopts Armv9 Cortex CPUs. The ‘Ultra Core’ features 1x Cortex-X2 at 3.05GHz, which is Arm’s most powerful CPU to date. Built for ultimate peak performance demands, Cortex-X2 supports performance improvements of 35% and power efficiency improvements of 37% on Dimensity 9000 compared to current Android flagship devices. The ‘Super Cores’ consist of 3x Cortex-A710 up to 2.85GHz, which delicately balances performance and efficiency demands to provide sustained performance benefits while also maximizing battery life. Finally, the ‘Efficiency Cores’ of 4x Cortex-A510 maintains the efficiency benefits of Arm’s “LITTLE” CPUs, but raises the performance floor so more compute can take place on these cores. The backbone of the CPU configuration is Arm’s DynamIQ Shared Unit (DSU), which supports the wide range of performance points required for the best consumer experiences. Press release by Paul Williamson, SVP and GM, Client Line of Business, Arm, <i>available at</i> https://www.edge-ai-vision.com/2021/12/mediatek-dimensity-9000-uses-armv9-technology-for-unparalleled-performance/

Claim 1	Accused Products
	Great Technology for Everyone MediaTek Kompanio enables incredible Chromebook experiences from a family of chips that are designed expressly to combine innovative features like AI processors and HDR cameras, fast and reliable Wi-Fi connectivity, and ultra-efficient performance for true, long lasting battery life in novel mobile computing platforms that can open, flip, fold, or even detach. MediaTek Kompanio 1380 MediaTek Kompanio 1200 MediaTek Kompanio 838 MediaTek Kompanio 828 MediaTek Kompanio 820 MediaTek Kompanio 520 MediaTek Kompanio 500  Made for Power Users If you're expecting peak performance, get ready to experience it. With an Octa-core big.LITTLE CPU of four Arm Cortex-A78 and four Arm Cortex-A55 MP cores operating at up to 3GHz paired with a high-performance Mali-G57 GPU, you get super-fast start-up times, multiple application operation and long battery life. MEDIATEK arm  https://i.mediatek.com/chromebook

Claim 1	Accused Products
	Processor CPU Type • 4x Arm Cortex-A78 up to 3GHz • 4x Arm Cortex-A55 up to 2GHz CPU Cores Octa (8) CPU bit 64-bit Heterogeneous Multi-Processing Yes https://www.mediatek.com/products/chromebooks/mediatek-kompanio-1380

Claim 1	Accused Products
	DynamiQ Shared Unit-110 First DynamiQ Shared Unit of the Armv9 generation, up to 12 cores supported, up to 16MB L3, and enhanced power management features. Supporting: • Cortex-X3 • Cortex-X2 • Cortex-A715 • Cortex-A710 • Cortex-A510 https://www.arm.com/technologies/dynamiq

Claim 1	Accused Products
	Figure 2-2: Example configuration with two Cortex®-A510 single-core complexes  Arm Cortex-A510 Core Technical Reference Manual at p. 23

Claim 1	Accused Products
	1.2 Document scope This application note focuses on the following processors and highlights important issues when powering up or powering down processor cores and clusters on an SoC. • Cortex®-A7. • Cortex®-A15. • Cortex®-A17. • Cortex®-A53. • Cortex®-A57. • Cortex®-A72. • Cortex®-A73. “High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at https://developer.arm.com/documentation/dai0424/a/ 2.1 ARM® big.LITTLE™ system example A big.LITTLE system uses two different types of cores that are combined in a coherent system. big cores are designed for high performance while LITTLE cores are designed for high energy efficiency. The big cores are used for resource-intensive software threads, and energy-efficient LITTLE cores handle low-intensity software threads that use fewer compute resources. The result is high energy efficiency and high performance. “High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at https://developer.arm.com/documentation/dai0424/a/

Claim 1

Accused Products

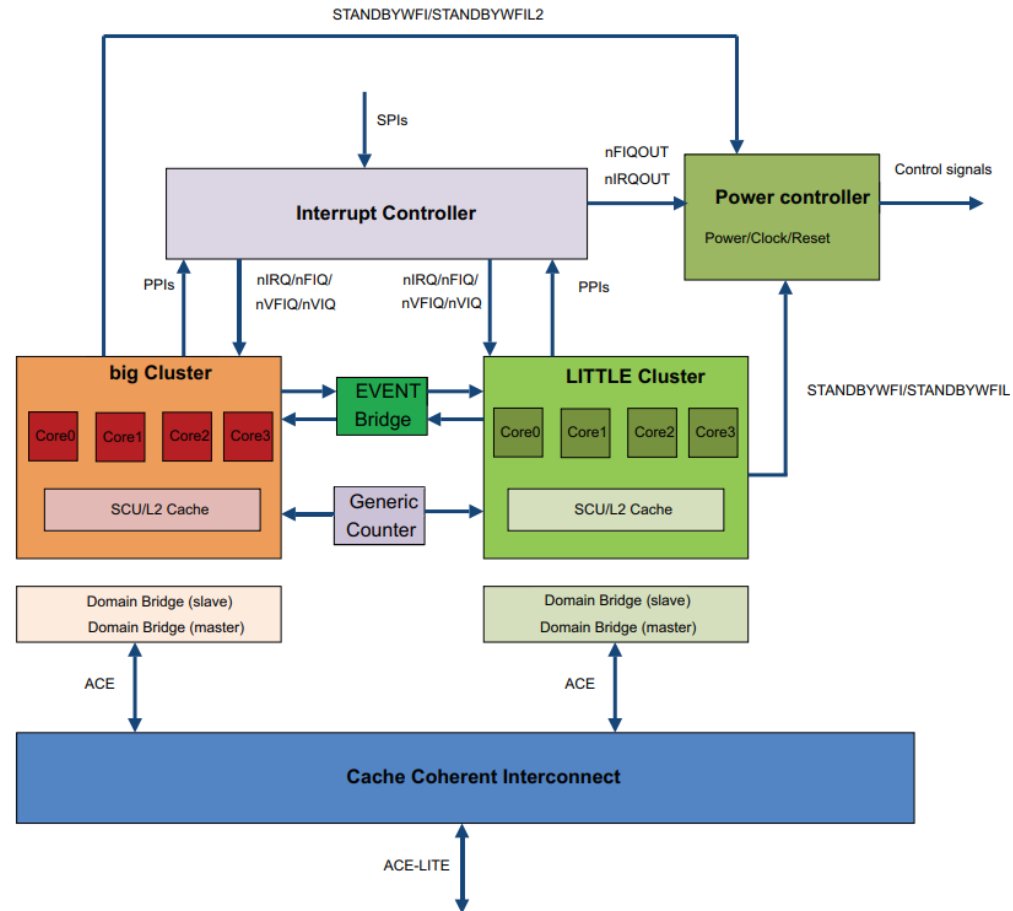
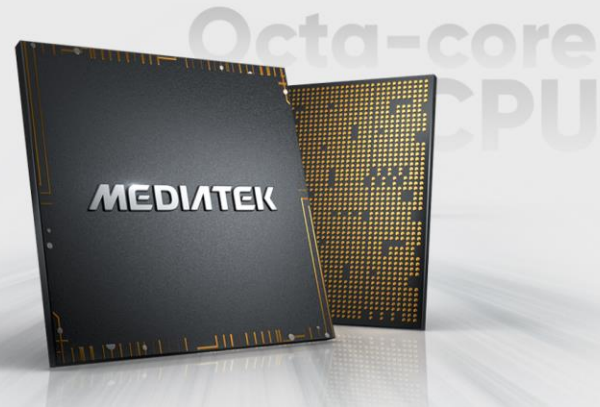


Figure 2-1 A typical big.LITTLE system

“High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at <https://developer.arm.com/documentation/dai0424/a/>

Claim 1	Accused Products
[1a] a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;	Each Accused Product comprises a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input. For example, the MT6983 includes a first set of high efficiency processor cores (ARM Cortex-A710 cores). The processor cores in the first set receive a dynamic supply voltage and a first output clock signal of a first PLL. For another example, MT8195T includes a first core complex comprising 4 ARM Cortex-A55 cores. The processor cores in the first set receive a dynamic supply voltage and a first output clock signal of a first PLL. <i>See, e.g.:</i>

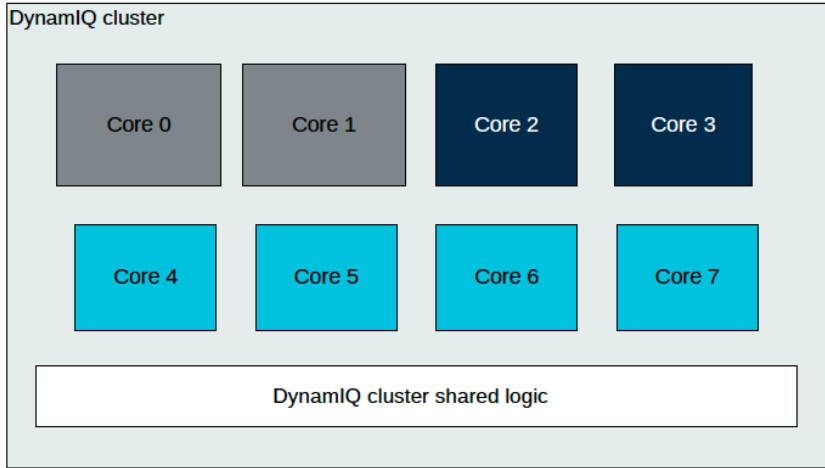
Claim 1	Accused Products
	Elevated Speed. Maximized Gaming. • Industry-leading TSMC N4 (4nm-class) chip production process • Our fastest ever Arm Mali-G710 MC10 graphics processor • Ultra-Core - 1x Arm Cortex-X2 at 3.2GHz • Super-Cores - 3x Arm Cortex-A710 up to 2.85GHz • Efficiency Cores - 4x Arm Cortex-A510 • Big in-chip caches: 8MB CPU L3 cache + 6MB system-level cache (SLC) • LPDDR5X 7500Mbps support – 20% more power efficient than LPDDR5 Our fastest ever flagship chip: We've increased peak clock speeds of the Arm Cortex-X2 CPU and Arm Mali-G710 MC10 graphics engine even further to raise performance to the next level! https://www.mediatek.com/products/smartphones-2/mediatek-dimension-9000plus

Claim 1	Accused Products
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Claim 1	Accused Products
	Processor CPU Type • 4x Arm Cortex-A78 up to 3GHz • 4x Arm Cortex-A55 up to 2GHz CPU Cores Octa (8) CPU bit 64-bit Heterogeneous Multi-Processing Yes https://www.mediatek.com/products/chromebooks/mediatek-kompanio-1380 Cluster features The DSU-110 has the following cluster features: • Support for Arm®v9.0-A architecture cores • Support for up to four types of core, and a maximum of 12 cores in the cluster • <i>Power Policy Units</i> (PPUs) providing autonomous power management of the L3 cache and the cores • Support for cores running independently at different frequencies and voltages known as <i>Dynamic Voltage Frequency Scaling</i> (DVFS). For cores in a complex, DVFS is only possible for the whole complex not for individual cores.

Claim 1	Accused Products
	Arm DynamIQ™ Shared Unit-110 Technical Reference Manual, available at https://documentation-service.arm.com/static/62bb28beb334256d9ea8cc32, at p. 19 A cluster can be configured with up to four different types of cores in the same cluster. Each core type targeting different power efficiency and performance levels. This arrangement allows for an intermediate core that has an intermediate performance and efficiency level. The cluster also supports complexes. A cluster can be configured in many arrangements. Examples of cluster arrangements are: • One or more cores of the same type. • Various arrangements of two types of cores. For example, one or more cores targeting either a high-performance level or a higher power efficiency level. • Various arrangements of three or four types of cores. For example, one or more high-performance cores, power-efficient cores, and intermediate cores. • One or more complexes and no individual cores. For information on complexes, see 2.3.1 What is a complex? on page 25. • One or more complexes and individual cores. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 22

Claim 1	Accused Products
	The diagram illustrates a DynamIQ cluster. It contains eight cores arranged in two rows of four. The top row consists of Core 0, Core 1, Core 2, and Core 3, which are labeled as 'High performance core' and are represented by grey boxes. The bottom row consists of Core 4, Core 5, Core 6, and Core 7, which are labeled as 'High efficiency core' and are represented by blue boxes. Below the cores is a white box labeled 'DynamIQ cluster shared logic'. A legend at the bottom left of the diagram area shows a blue square for 'High efficiency core' and a grey square for 'High performance core'. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 23

Claim 1	Accused Products
	 High performance core Balanced performance core High efficiency core Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 24

Claim 1	Accused Products
	DynamiQ cluster <pre> graph TD subgraph "DynamiQ cluster" subgraph "Complex 0" C0[Core 0] C1[Core 1] SL0[Shared logic] C0 --- SL0 C1 --- SL0 end subgraph "Complex 1" C2[Core 2] C3[Core 3] SL1[Shared logic] C2 --- SL1 C3 --- SL1 end subgraph "Complex 2" C4[Core 4] C5[Core 5] SL2[Shared logic] C4 --- SL2 C5 --- SL2 end subgraph "Complex 3" C6[Core 6] C7[Core 7] SL3[Shared logic] C6 --- SL3 C7 --- SL3 end SL4[DynamiQ cluster shared logic] SL0 --- SL4 SL1 --- SL4 SL2 --- SL4 SL3 --- SL4 end </pre> Complex 0: Core 0, Core 1, Shared logic Complex 1: Core 2, Core 3, Shared logic Complex 2: Core 4, Core 5, Shared logic Complex 3: Core 6, Core 7, Shared logic DynamiQ cluster shared logic ■ Supported core in complex Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 24 The DSU-110 DynamIQ™ cluster supports blocks that are called complexes which contain up to two cores of the same type and some shared logic. Sharing some logic between the two cores of a dual core complex can make the dual core complex area efficient. However, this area efficiency is at the cost of reduced performance compared with using two single-core complexes. Arm® DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 25

Claim 1	Accused Products
	The <i>DynamIQ™ Shared Unit-110</i> (DSU-110) has multiple clock domains. Each core or complex can be implemented in a separate clock domain. The following figure shows the clock domains for an example cluster with four standalone cores. Figure 4-1: DSU-110 clock domains Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 46 The <i>DynamIQ™ Shared Unit-110</i> (DSU-110) <i>Power Policy Units</i> (PPUs) control power management for the Cortex®-A510 core. A Cortex®-A510 complex supports separate gated power domains for the complex, for each core inside the complex, and for the <i>Vector Processing Unit</i> (VPU). It also supports a dedicated voltage domain for each complex, and a voltage domain for the DSU-110 DynamIQ™ cluster. Arm Cortex-A510 Core Technical Reference Manual at p. 39

Claim 1	Accused Products						
	The cluster contains several clock domains for functionality that is likely to be connected to different clocks in the system. Within each core, the CPU bridge contains asynchronous bridges for all crossings between the core and cluster clock domains. Each CPU bridge is split, with one half of each bridge in the core clock domain and the other half in the relevant cluster domain. At the cluster level, there is the <i>Snoop Control Unit</i> (SCU) bridge which contains crossings between the cluster clock domains as required. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 46 The DynamIQ Shared Unit-110 (DSU-110) has a separate clock signal for each standalone core or complex. There are also separate clocks for the internal logic, and some of the e interfaces. The following table describes the clock signals of the DSU-110. <table data-bbox="636 659 1908 1016"> <caption>Table 1. DSU-110 clock signals</caption> <thead> <tr> <th>Signal</th><th>Description</th></tr> </thead> <tbody> <tr> <td>COREyCLK</td><td> The clocks for each of the cores in the cluster that are not part of a complex. y is the core instance number, for example, CORE0CLK is the clock for core 0. These signals clock all core logic, including L1 and L2 caches. </td></tr> <tr> <td>COMPLEXxCLK</td><td> The clocks for each complex in the cluster. Each clock is connected to all cores in the respective complex. x is the complex instance number, for example, COMPLEX0CLK is the clock for complex 0. </td></tr> </tbody> </table> https://developer.arm.com/documentation/101381/0400/Clocks-and-resets/Clocks-	Signal	Description	COREyCLK	The clocks for each of the cores in the cluster that are not part of a complex. y is the core instance number, for example, CORE0CLK is the clock for core 0. These signals clock all core logic, including L1 and L2 caches.	COMPLEXxCLK	The clocks for each complex in the cluster. Each clock is connected to all cores in the respective complex. x is the complex instance number, for example, COMPLEX0CLK is the clock for complex 0.
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Claim 1	Accused Products
	Voltage domains The voltage supply to a domain might be scaled or removed for power or performance reasons. Except for low complexity solutions, it is rare to use a single logic voltage supply for the whole SoC. The primary reason for additional voltage domains is to support DVFS for functional areas of the SoC. The second reason is to enable external supply switch-off, or reduction to non-functional state retention levels, to some logic areas while maintaining an operational level supply to others. However, the cost for additional voltage domains is significant, because additional voltage regulators, extra effort, and complexity are required in the SoC physical implementation. Therefore, you must carefully assess the value of the addition of each voltage domain against the performance and power requirements for the design. In a big.LITTLE system, each cluster must have a dedicated voltage supply. This is a critical success factor when combined with big.LITTLE software. “High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at https://developer.arm.com/documentation/dai0424/a/

Claim 1

Accused Products

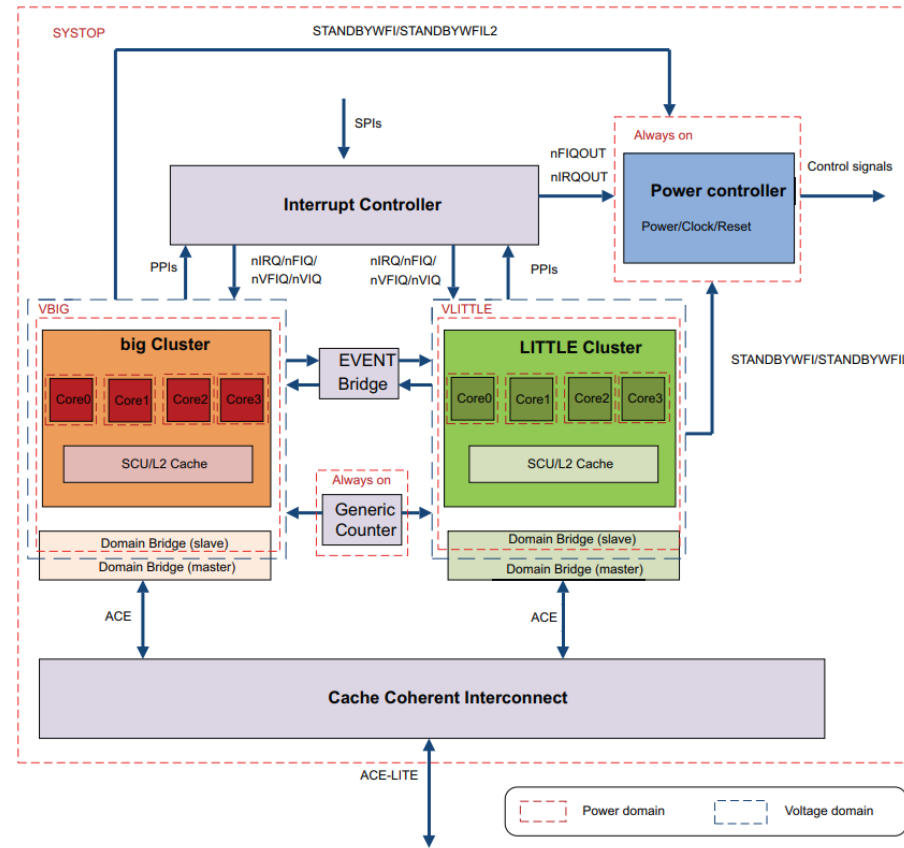


Figure 2-2 Power domain hierarchy

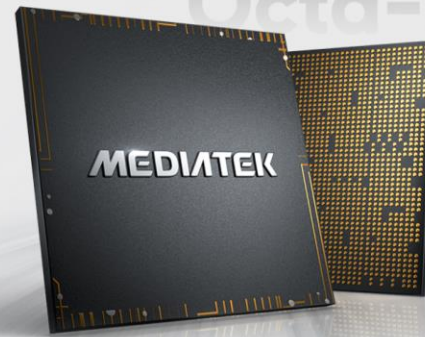
In Figure 2-2, two processor clusters are implemented with per-core and cluster power domains. The big cluster is in the VBIG voltage domain, while the LITTLE cluster is in the VLITTLE voltage domain. The system controller is in an always-on power domain. All the other components are in the system logic power domain (SYSTOP).

“High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at <https://developer.arm.com/documentation/dai0424/a/>

Claim 1	Accused Products
	Clock domains Clock domains can interact with each other synchronously or asynchronously. Synchronous clock domains can have independent source activity. Each cluster requires an independent clock, and the CCI requires a clock. “High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
[1b] a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and	Each Accused Product comprises a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal. For example, in addition to the first set of processor cores, the MT6983 has a second set of efficiency processor cores (ARM Cortex-A510 cores). For another example, MT8195T includes a second core complex comprising 4 ARM Cortex-A78 cores. The processor cores in the second set receive a second, independent dynamic supply voltage and a second, independent output clock signal of a second PLL, and the first and second clock signals are independent. <i>See, e.g.:</i>

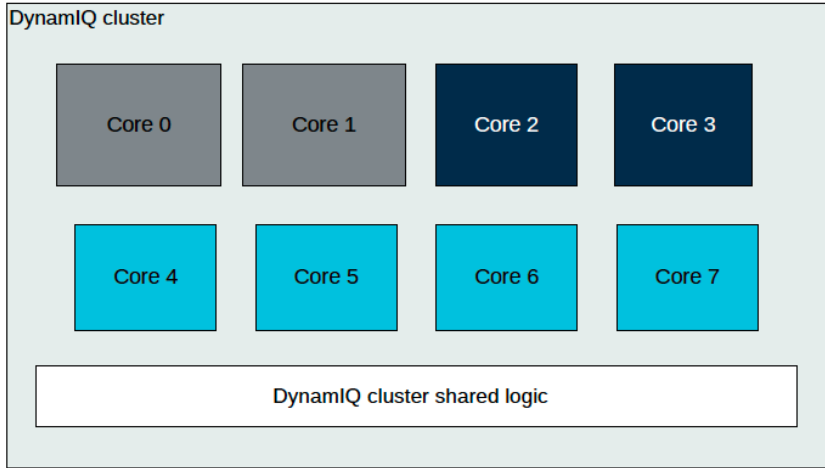
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	Processor CPU Type • 4x Arm Cortex-A78 up to 3GHz • 4x Arm Cortex-A55 up to 2GHz CPU Cores Octa (8) CPU bit 64-bit Heterogeneous Multi-Processing Yes https://www.mediatek.com/products/chromebooks/mediatek-kompanio-1380 Cluster features The DSU-110 has the following cluster features: • Support for Arm®v9.0-A architecture cores • Support for up to four types of core, and a maximum of 12 cores in the cluster • <i>Power Policy Units</i> (PPUs) providing autonomous power management of the L3 cache and the cores • Support for cores running independently at different frequencies and voltages known as <i>Dynamic Voltage Frequency Scaling</i> (DVFS). For cores in a complex, DVFS is only possible for the whole complex not for individual cores.

Claim 1	Accused Products
	Arm DynamIQ™ Shared Unit-110 Technical Reference Manual, available at https://documentation-service.arm.com/static/62bb28beb334256d9ea8cc32, at p. 19 A cluster can be configured with up to four different types of cores in the same cluster. Each core type targeting different power efficiency and performance levels. This arrangement allows for an intermediate core that has an intermediate performance and efficiency level. The cluster also supports complexes. A cluster can be configured in many arrangements. Examples of cluster arrangements are: • One or more cores of the same type. • Various arrangements of two types of cores. For example, one or more cores targeting either a high-performance level or a higher power efficiency level. • Various arrangements of three or four types of cores. For example, one or more high-performance cores, power-efficient cores, and intermediate cores. • One or more complexes and no individual cores. For information on complexes, see 2.3.1 What is a complex? on page 25. • One or more complexes and individual cores. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 22

Claim 1	Accused Products
	The diagram illustrates a DynamIQ cluster. It contains eight cores arranged in two rows of four. The top row consists of Core 0, Core 1, Core 2, and Core 3, which are grey boxes representing high performance cores. The bottom row consists of Core 4, Core 5, Core 6, and Core 7, which are blue boxes representing high efficiency cores. Below the cores is a white rectangular box labeled 'DynamIQ cluster shared logic'. A legend below the diagram indicates that blue squares represent 'High efficiency core' and grey squares represent 'High performance core'. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 23

Claim 1	Accused Products
	 High performance core Balanced performance core High efficiency core Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 24

Claim 1	Accused Products
	DynamiQ cluster <pre> graph TD subgraph "DynamiQ cluster" subgraph "Complex 0" C0[Core 0] C1[Core 1] SL0[Shared logic] C0 --- SL0 C1 --- SL0 end subgraph "Complex 1" C2[Core 2] C3[Core 3] SL1[Shared logic] C2 --- SL1 C3 --- SL1 end subgraph "Complex 2" C4[Core 4] C5[Core 5] SL2[Shared logic] C4 --- SL2 C5 --- SL2 end subgraph "Complex 3" C6[Core 6] C7[Core 7] SL3[Shared logic] C6 --- SL3 C7 --- SL3 end SL4[DynamiQ cluster shared logic] SL0 --- SL4 SL1 --- SL4 SL2 --- SL4 SL3 --- SL4 end </pre> ■ Supported core in complex Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 24 The DSU-110 DynamIQ™ cluster supports blocks that are called complexes which contain up to two cores of the same type and some shared logic. Sharing some logic between the two cores of a dual core complex can make the dual core complex area efficient. However, this area efficiency is at the cost of reduced performance compared with using two single-core complexes. Arm® DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 25

Claim 1	Accused Products
	The <i>DynamiQ™ Shared Unit-110</i> (DSU-110) has multiple clock domains. Each core or complex can be implemented in a separate clock domain. The following figure shows the clock domains for an example cluster with four standalone cores. Figure 4-1: DSU-110 clock domains Arm <i>DynamiQ™ Shared Unit-110</i> Technical Reference Manual at p. 46 The <i>DynamiQ™ Shared Unit-110</i> (DSU-110) <i>Power Policy Units</i> (PPUs) control power management for the Cortex®-A510 core. A Cortex®-A510 complex supports separate gated power domains for the complex, for each core inside the complex, and for the <i>Vector Processing Unit</i> (VPU). It also supports a dedicated voltage domain for each complex, and a voltage domain for the DSU-110 <i>DynamiQ™</i> cluster. Arm Cortex-A510 Core Technical Reference Manual at p. 39

Claim 1	Accused Products						
	The cluster contains several clock domains for functionality that is likely to be connected to different clocks in the system. Within each core, the CPU bridge contains asynchronous bridges for all crossings between the core and cluster clock domains. Each CPU bridge is split, with one half of each bridge in the core clock domain and the other half in the relevant cluster domain. At the cluster level, there is the <i>Snoop Control Unit</i> (SCU) bridge which contains crossings between the cluster clock domains as required. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 46 The DynamIQ Shared Unit-110 (DSU-110) has a separate clock signal for each standalone core or complex. There are also separate clocks for the internal logic, and some of the e interfaces. The following table describes the clock signals of the DSU-110. <table data-bbox="703 659 1908 1016"> <caption>Table 1. DSU-110 clock signals</caption> <thead> <tr> <th>Signal</th><th>Description</th></tr> </thead> <tbody> <tr> <td>COREyCLK</td><td> The clocks for each of the cores in the cluster that are not part of a complex. y is the core instance number, for example, CORE0CLK is the clock for core 0. These signals clock all core logic, including L1 and L2 caches. </td></tr> <tr> <td>COMPLEXxCLK</td><td> The clocks for each complex in the cluster. Each clock is connected to all cores in the respective complex. x is the complex instance number, for example, COMPLEX0CLK is the clock for complex 0. </td></tr> </tbody> </table> https://developer.arm.com/documentation/101381/0400/Clocks-and-resets/Clocks-	Signal	Description	COREyCLK	The clocks for each of the cores in the cluster that are not part of a complex. y is the core instance number, for example, CORE0CLK is the clock for core 0. These signals clock all core logic, including L1 and L2 caches.	COMPLEXxCLK	The clocks for each complex in the cluster. Each clock is connected to all cores in the respective complex. x is the complex instance number, for example, COMPLEX0CLK is the clock for complex 0.
Signal	Description						
COREyCLK	The clocks for each of the cores in the cluster that are not part of a complex. y is the core instance number, for example, CORE0CLK is the clock for core 0. These signals clock all core logic, including L1 and L2 caches.						
COMPLEXxCLK	The clocks for each complex in the cluster. Each clock is connected to all cores in the respective complex. x is the complex instance number, for example, COMPLEX0CLK is the clock for complex 0.						

Claim 1	Accused Products
	1.2 Document scope This application note focuses on the following processors and highlights important issues when powering up or powering down processor cores and clusters on an SoC. • Cortex[®]-A7. • Cortex[®]-A15. • Cortex[®]-A17. • Cortex[®]-A53. • Cortex[®]-A57. • Cortex[®]-A72. • Cortex[®]-A73. “High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	Voltage domains The voltage supply to a domain might be scaled or removed for power or performance reasons. Except for low complexity solutions, it is rare to use a single logic voltage supply for the whole SoC. The primary reason for additional voltage domains is to support DVFS for functional areas of the SoC. The second reason is to enable external supply switch-off, or reduction to non-functional state retention levels, to some logic areas while maintaining an operational level supply to others. However, the cost for additional voltage domains is significant, because additional voltage regulators, extra effort, and complexity are required in the SoC physical implementation. Therefore, you must carefully assess the value of the addition of each voltage domain against the performance and power requirements for the design. In a big.LITTLE system, each cluster must have a dedicated voltage supply. This is a critical success factor when combined with big.LITTLE software. “High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at https://developer.arm.com/documentation/dai0424/a/

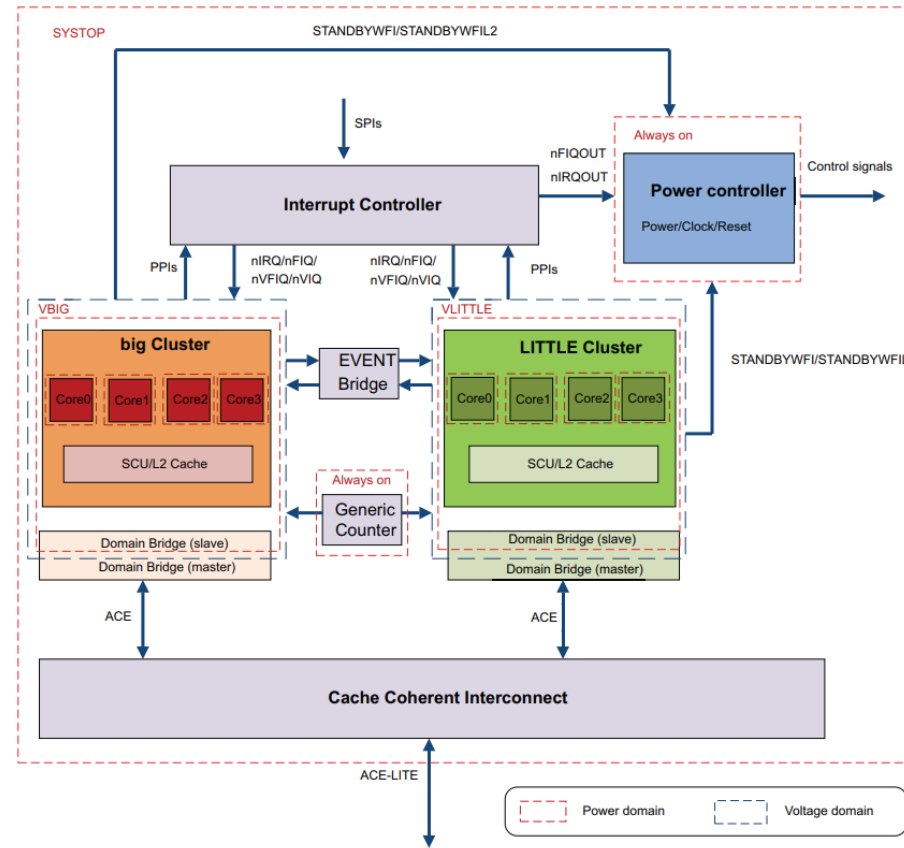


Figure 2-2 Power domain hierarchy

In Figure 2-2, two processor clusters are implemented with per-core and cluster power domains. The big cluster is in the VBIG voltage domain, while the LITTLE cluster is in the VLITTLE voltage domain. The system controller is in an always-on power domain. All the other components are in the system logic power domain (SYSTOP).

“High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at <https://developer.arm.com/documentation/dai0424/a/>

Claim 1	Accused Products
	Clock domains Clock domains can interact with each other synchronously or asynchronously. Synchronous clock domains can have independent source activity. Each cluster requires an independent clock, and the CCI requires a clock. “High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at https://developer.arm.com/documentation/dai0424/a/

Claim 1

Accused Products

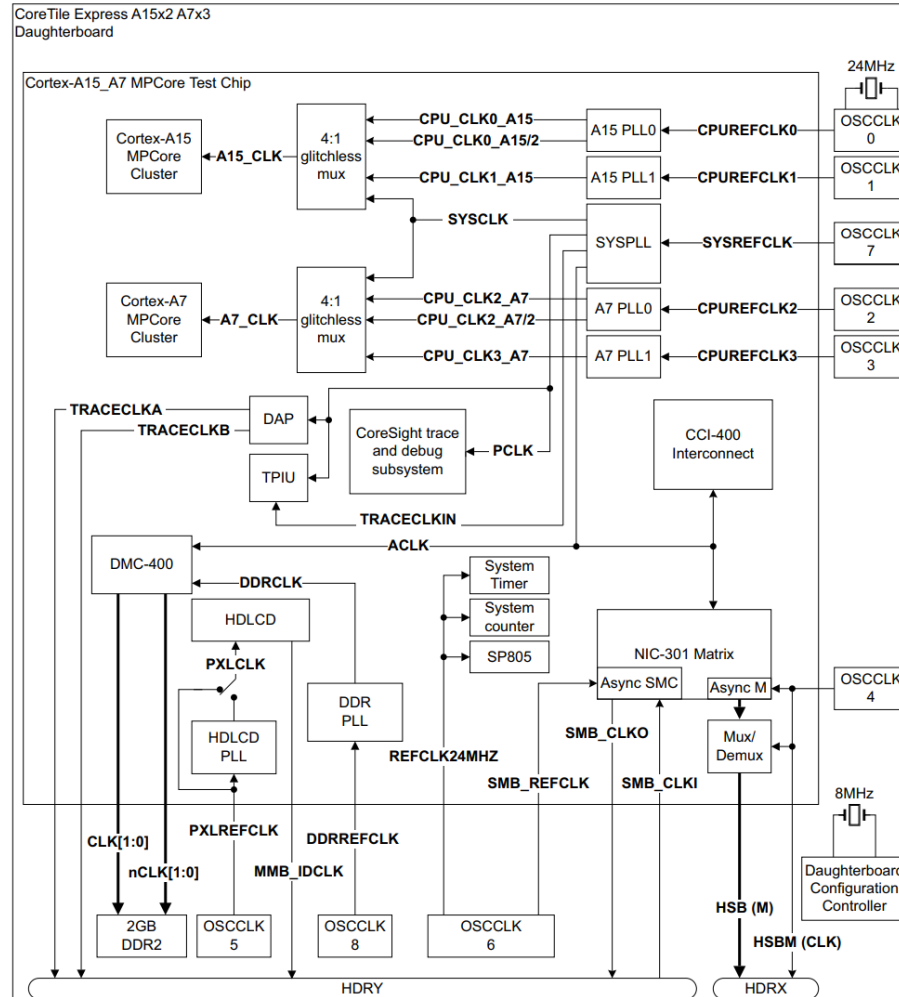


Figure 2-10 CoreTile Express A15x2 A7x3 daughterboard clocks

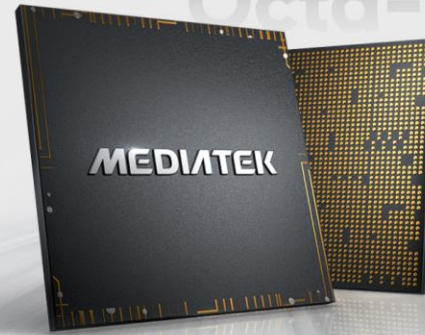
ARM® CoreTile Express A15x2 A7x3 Technical Reference Manual, available at <https://developer.arm.com/documentation/ddi0503/i/>

Claim 1	Accused Products
[1c] an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.	Each Accused Product comprises an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores. For example, the MT6983 includes a Snoop Control Unit (SCU) that is coupled to each core or to each set of processor cores and is configured to maintains coherency between caches in the cores or complexes and L3 shared memory implemented DynamIQ Shared Unit. For another example, the MT8195T includes a cache coherent interconnect, such as a CCI-400 or CCI-550, that is coupled to each core or to each set of processor cores and is configured to communicate between the sets of processor cores, for example by maintaining coherency between caches in the cores or complexes. <i>See, e.g.:</i>

Claim 1	Accused Products																	
	<table><tr><td rowspan="2">Cortex-X2 1MB L2</td><td>Cortex-A7 10 512KB L2</td><td>Cortex-A5 10</td><td>Cortex-A5 10</td><td>Cortex-A5 10</td><td>Cortex-A5 10</td></tr><tr><td>Cortex-A7 10 512KB L2</td><td>Cortex-A7 10 512KB L2</td><td colspan="2">Shared 512KB L2\$ Shared VPU</td><td>Shared 512KB L2\$ Shared VPU</td></tr><tr><td colspan="6">DynamIQ Shared Unit equipped 8MB L3\$</td></tr></table>	Cortex-X2 1MB L2	Cortex-A7 10 512KB L2	Cortex-A5 10	Cortex-A5 10	Cortex-A5 10	Cortex-A5 10	Cortex-A7 10 512KB L2	Cortex-A7 10 512KB L2	Shared 512KB L2\$ Shared VPU		Shared 512KB L2\$ Shared VPU	DynamIQ Shared Unit equipped 8MB L3\$					
Cortex-X2 1MB L2	Cortex-A7 10 512KB L2		Cortex-A5 10	Cortex-A5 10	Cortex-A5 10	Cortex-A5 10												
	Cortex-A7 10 512KB L2	Cortex-A7 10 512KB L2	Shared 512KB L2\$ Shared VPU		Shared 512KB L2\$ Shared VPU													
DynamIQ Shared Unit equipped 8MB L3\$																		
	Presentation “Dimensity 9000 – A Flagship Smartphone SoC” by Ericbill Wang of MediaTek and Stefan Rosinger and Saurabh Pradhan of ARM, <i>available at</i> https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/HC2022.Mediatek.EricbillWang.v08.pptx.pdf																	

Claim 1	Accused Products								
	Arm DynamIQ Shared Unit-110 ▪DSU-110 for Cache Coherency & Shared L3\$ ▪Optimized Ring Transport Network –Bi-directional, Dual-ring ▪2X Bandwidth and 25% Lower Leakage –Support Partial SRAM & Logic Shutdown ▪Cache Partition for QoS <table border="1"> <thead> <tr> <th>Scenario</th> <th>Leakage Power (Relative)</th> </tr> </thead> <tbody> <tr> <td>Previous generation fully active</td> <td>100%</td> </tr> <tr> <td>DSU-110 fully active</td> <td>25% lower</td> </tr> <tr> <td>DSU-110 Partial powerdown</td> <td>75% lower</td> </tr> </tbody> </table> MEDIATEK 11 Presentation “Dimensity 9000 – A Flagship Smartphone SoC” by Ericbill Wang of MediaTek and Stefan Rosinger and Saurabh Pradhan of ARM, <i>available at</i> https://hc34.hotchips.org/assets/program/conference/day2/Mobile%20and%20Edge/HC2022.Mediatek.EricbillWang.v08.pptx.pdf	Scenario	Leakage Power (Relative)	Previous generation fully active	100%	DSU-110 fully active	25% lower	DSU-110 Partial powerdown	75% lower
Scenario	Leakage Power (Relative)								
Previous generation fully active	100%								
DSU-110 fully active	25% lower								
DSU-110 Partial powerdown	75% lower								

Claim 1	Accused Products
	Built on the first ever Armv9 CPUs Dimensity 9000 is the first chipset announced that adopts Armv9 Cortex CPUs. The ‘Ultra Core’ features 1x Cortex-X2 at 3.05GHz, which is Arm’s most powerful CPU to date. Built for ultimate peak performance demands, Cortex-X2 supports performance improvements of 35% and power efficiency improvements of 37% on Dimensity 9000 compared to current Android flagship devices. The ‘Super Cores’ consist of 3x Cortex-A710 up to 2.85GHz, which delicately balances performance and efficiency demands to provide sustained performance benefits while also maximizing battery life. Finally, the ‘Efficiency Cores’ of 4x Cortex-A510 maintains the efficiency benefits of Arm’s “LITTLE” CPUs, but raises the performance floor so more compute can take place on these cores. The backbone of the CPU configuration is Arm’s DynamIQ Shared Unit (DSU), which supports the wide range of performance points required for the best consumer experiences. Press release by Paul Williamson, SVP and GM, Client Line of Business, Arm, <i>available at</i> https://www.edge-ai-vision.com/2021/12/mediatek-dimensity-9000-uses-armv9-technology-for-unparalleled-performance/

Claim 1	Accused Products
	Great Technology for Everyone MediaTek Kompanio enables incredible Chromebook experiences from a family of chips that are designed expressly to combine innovative features like AI processors and HDR cameras, fast and reliable Wi-Fi connectivity, and ultra-efficient performance for true, long lasting battery life in novel mobile computing platforms that can open, flip, fold, or even detach. MediaTek Kompanio 1380 MediaTek Kompanio 1200 MediaTek Kompanio 838 MediaTek Kompanio 828 MediaTek Kompanio 820 MediaTek Kompanio 520 MediaTek Kompanio 500  Made for Power Users If you're expecting peak performance, get ready to experience it. With an Octa-core big.LITTLE CPU of four Arm Cortex-A78 and four Arm Cortex-A55 MP cores operating at up to 3GHz paired with a high-performance Mali-G57 GPU, you get super-fast start-up times, multiple application operation and long battery life. MEDIATEK arm  Octa-core CPU https://i.mediatek.com/chromebook

Claim 1	Accused Products
	Processor CPU Type • 4x Arm Cortex-A78 up to 3GHz • 4x Arm Cortex-A55 up to 2GHz CPU Cores Octa (8) CPU bit 64-bit Heterogeneous Multi-Processing Yes https://www.mediatek.com/products/chromebooks/mediatek-kompanio-1380 When you implement a DSU-110 DynamIQ™ cluster, all interfacing between the cores, complexes, and the <i>DynamIQ™ Shared Unit-110</i> (DSU-110) is implemented automatically. All the external signal inputs and outputs pass through the DSU-110. The DSU-110 buffers and resynchronizes many of these signals to allow cores and complexes to be clocked at different speeds. The memory interfacing of each core is internally connected to the DSU-110 L3 memory system. Where necessary, the DSU-110 implements additional buffering to compensate for different clock rates of the core and DSU-110 L3 memory system. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 34

Claim 1	Accused Products
	All cores in the DSU-110 DynamIQ™ cluster, including those in complexes, are coherently connected to an L3 memory system that includes an L3 cache and a <i>Snoop Control Unit</i> (SCU). The SCU maintains coherency between caches in the cores and the L3 cache, and includes a snoop filter to optimize coherency maintenance operations. The shared L3 cache simplifies process migration between the cores. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 18 Snoop Control Unit The <i>Snoop Control Unit</i> (SCU) maintains coherency between all the data caches in the cluster. The SCU contains buffers that can handle direct cache-to-cache transfers between cores without having to read or write data to the L3 cache. Cache line migration enables dirty lines to be moved between cores. Also, there is no requirement to write back transferred cache line data to the L3 cache. The SCU contains a set of snoop filters that track the addresses for locations cached in the core caches. Including the snoop filters means that the SCU does not need to request a look up in the core caches when it receives a coherent memory request. These snoop filters are accessed by coherent requests from the other cores or from the system. If there is a simultaneous hit in the L3 tags and the SCU snoop filters, then the L3 cache normally provides the data in preference to a core. The size of the snoop filter is automatically determined from the configured number of cores and the cache sizes in those cores. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 35

Claim 1	Accused Products
	The diagram illustrates the Arm DynamIQ Shared Unit-110 architecture. It is enclosed in a dashed box. Inside, there is a 'DynamIQ cluster' and a 'DynamIQ cluster shared logic' block. The cluster contains six cores (Core 0 through Core 5) arranged in two columns, each with a 'CPU bridge' below it. To the right of these is 'Complex 0', which contains 'Core 4' and 'Core 5' with a 'Shared logic' block and a 'CPU bridge' below them. Below the cluster is the 'DynamIQ cluster shared logic' block, which includes 'Power Policy Units (PPUs)', 'Snoop Control Unit (SCU) and L3 cache' (containing 'L3 cache' and 'Snoop filters'), 'Accelerator Coherency Port (ACP)', 'DebugBlock interface', 'Peripheral Port', 'Memory interface', 'Utility bus', and 'DSU-110 bridges'. A 'DebugBlock' is shown to the right of the cluster shared logic block. Arm DynamIQ™ Shared Unit-110 Technical Reference Manual at p. 17 1.2 Document scope This application note focuses on the following processors and highlights important issues when powering up or powering down processor cores and clusters on an SoC. • Cortex®-A7. • Cortex®-A15. • Cortex®-A17. • Cortex®-A53. • Cortex®-A57. • Cortex®-A72. • Cortex®-A73. “High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	2.1 ARM® big.LITTLE™ system example A big.LITTLE system uses two different types of cores that are combined in a coherent system. big cores are designed for high performance while LITTLE cores are designed for high energy efficiency. The big cores are used for resource-intensive software threads, and energy-efficient LITTLE cores handle low-intensity software threads that use fewer compute resources. The result is high energy efficiency and high performance. “High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at https://developer.arm.com/documentation/dai0424/a/

Claim 1

Accused Products

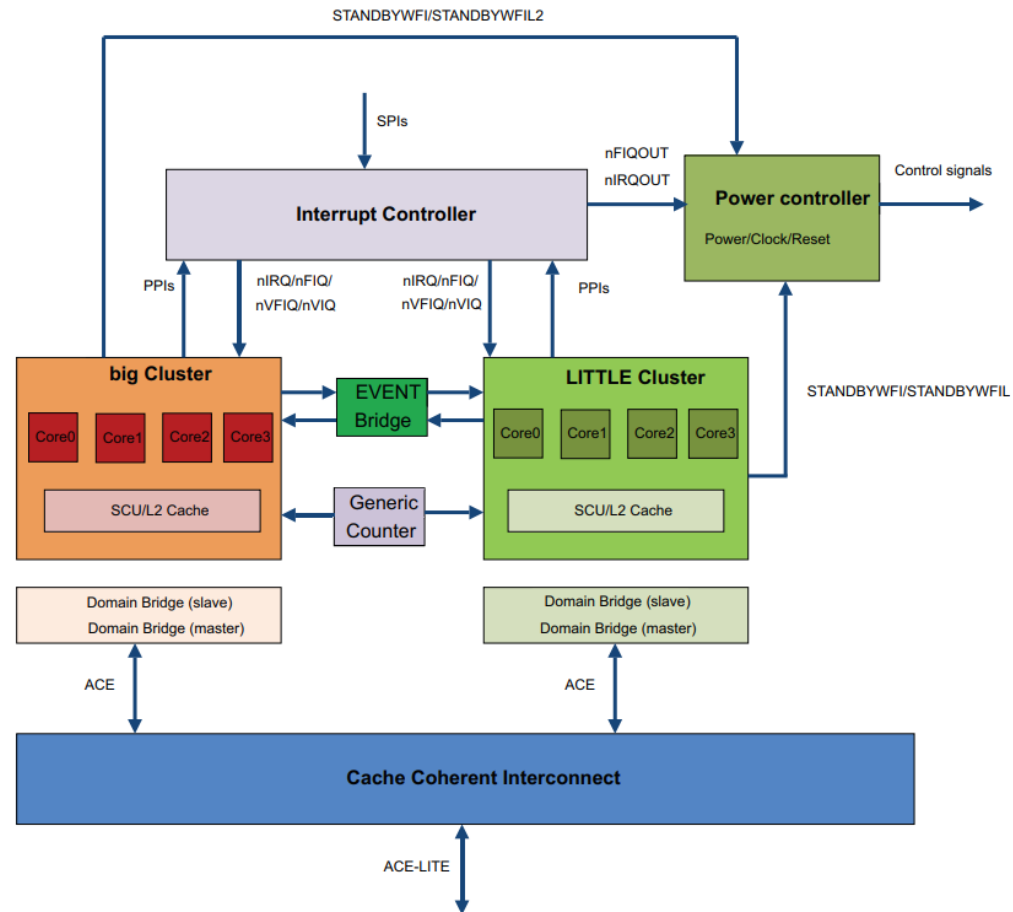


Figure 2-1 A typical big.LITTLE system

“High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at <https://developer.arm.com/documentation/dai0424/a/>

Claim 1	Accused Products
	<pre> graph TD GIC400[GIC-400] subgraph Cluster1 [] direction TB C1_1[Cortex-A15 Core] C1_2[Cortex-A15 Core] L2_1[L2] C1_1 <--> L2_1 C1_2 <--> L2_1 end subgraph Cluster2 [] direction TB C2_1[Cortex-A7 Core] C2_2[Cortex-A7 Core] L2_2[L2] C2_1 <--> L2_2 C2_2 <--> L2_2 end ICM[IO Coherent Master] CCI400[CCI-400 Cache Coherent Interconnect] MCP[Memory Controller Ports] SP[System Port] GIC400 <--> Interrupts Cluster1 GIC400 <--> Interrupts Cluster2 L2_1 <--> CCI400 L2_2 <--> CCI400 ICM <--> CCI400 CCI400 <--> MCP CCI400 <--> SP </pre> Fig 1: Typical big.LITTLE system As an example, Figure 2 describes the pipeline designs for the Cortex-A15 and Cortex-A7 cores. The Cortex-A15 core is designed to achieve high performance by running more instructions in parallel on a bigger and more complex pipeline. On the other hand, the Cortex-A7 core's pipeline is relatively simple and is designed to be extremely power efficient. The Cortex-A7 core's performance is lower than the Cortex-A15 core's but it is sufficient for most common usage scenarios executed by modern mobile devices. In fact, the Cortex-A7 core's performance is close to Cortex-A9 core, which powers most smartphones today. ARM White Paper “big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency,” available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf

Claim 1	Accused Products
	Cache Coherency Interface and big.LITTLE Technology The key ingredient that makes big.LITTLE technology possible is coherency. big.LITTLE software models require transparent and performant transfer of data between big and LITTLE processors. Hardware coherency enables this, transparently to the software. Without hardware coherency, the transfer of data between big and LITTLE cores would always occur through main memory - this would be slow and not power efficient. In addition, it would require complex cache management software, to enable data coherency between big and LITTLE processors Figure 4 is an example of CPU subsystem consisting of a Cortex-A7 cluster, a Cortex-A15 cluster and a set of system fabric components which enable the seamless data transfer between clusters. This fabric is collectively referred to as a "Cache Coherent Interconnect" – in this case the ARM CoreLink™ CCI-400 interconnect IP. The system is completed by the CoreLink GIC-400, which provides dynamically configurable interrupt distribution to all the cores. ARM White Paper “big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency,” available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf

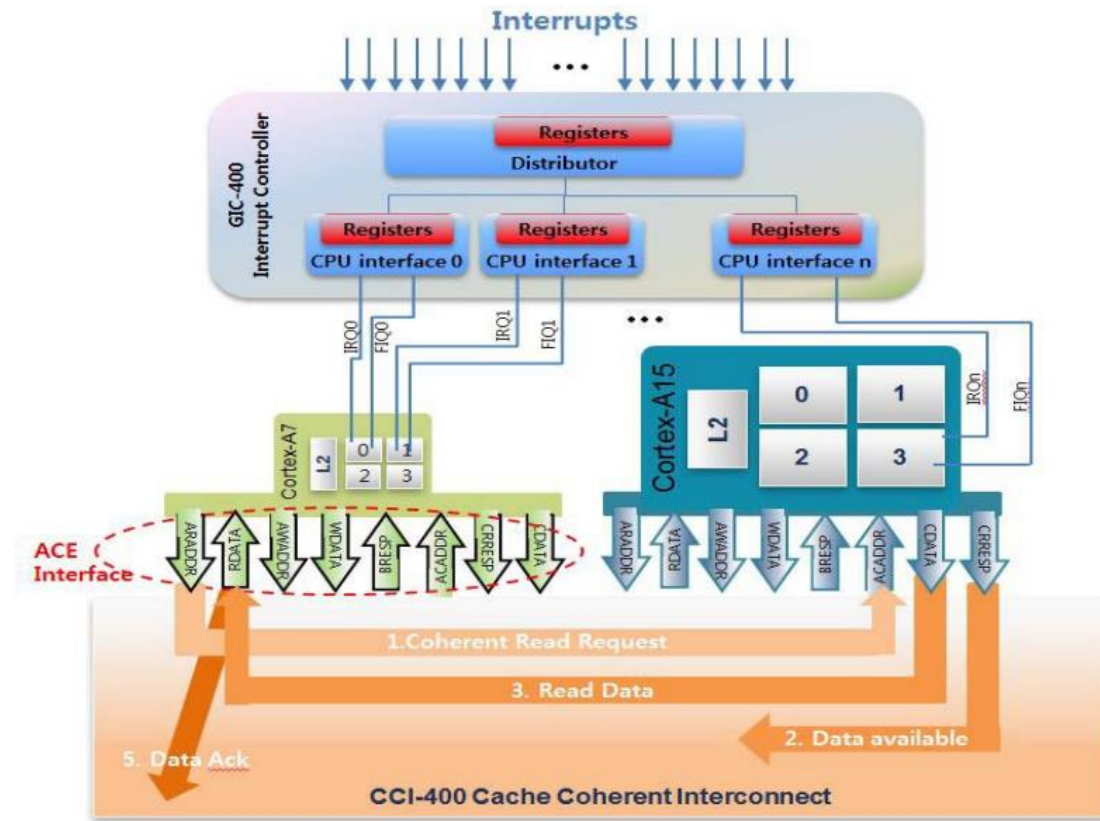


Figure 3: Cache coherency in a big.LITTLE system

ARM White Paper “big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency,” available at <https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf>

Claim 1	Accused Products
	As shown in Figure 3, the bus interfaces of Cortex-A15 and Cortex-A7 processors make use of the AMBA® AXI Coherency Extensions (ACE) to the widely-used AMBA AXI protocol. This protocol provides for coherent data transfer at the bus level. In the AMBA ACE protocol, three coherency channels are added in addition to the normal five channels of AMBA AXI. As an example, the lower part of Figure shows the steps in a coherent data read from the Cortex-A7 cluster to the Cortex-A15 cluster. This starts with the Cortex-A7 cluster issuing a Coherent Read Request through the RADDR channel. The CCI-400 hands over the request to the Cortex-A15 processor's ACADDR channel to snoop into Cortex-A15 processor's cache. On receiving the request from CCI-400, the Cortex-A15 processor checks the data availability and reports this information back through the CRRESP channel. If the requested data is in the cache, the Cortex-A15 processor places it on the CDATA channel. Then the CCI-400 moves the data from the Cortex-A15 processor's CDATA channel to the Cortex-A7 processor's RDATA channel, resulting in a cache linefill in the Cortex-A7 processor. The CCI-400 and the ACE protocol enable full coherency between the Cortex-A15 and Cortex-A7 clusters, allowing data sharing to take place without external memory transactions. ARM White Paper “big.LITTLE Technology: The Future of Mobile Making very high performance available in a mobile envelope without sacrificing energy efficiency,” available at https://armkeil.blob.core.windows.net/developer/Files/pdf/white-paper/big-little-technology-the-future-of-mobile.pdf

Claim 5

Claim 5	Accused Products
5. The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor.	Each Accused Product comprises a multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor. For example, according to ARM's documents and reference design, the multi-core processor should contain a system control processor (SCP) to control voltage, power, and clocks, and power policy units (PPUs) to manage power states on each voltage domain. On information and belief, the processor in the MT6983 contains an SCP and one or more PPUs as described. Identification of the physical location of the control blocks is proprietary information of MediaTek and/or ARM that is the proper subject of fact discovery.

Claim 5	Accused Products
	For another example, according to ARM's documents and reference design, a big.LITTLE multi-core processor should contain a power controller and other controllers for supplying control signals as claimed. Identification of the physical location of the control blocks is proprietary information of MediaTek and/or ARM that is the proper subject of fact discovery. <i>See, e.g.:</i>

Claim 5	Accused Products
	6.1 The Power Policy Unit Power mode control for the <i>DynamiQ™ Shared Unit-110</i> (DSU-110) is provided by the <i>Power Policy Units</i> (PPUs) that are integrated into the cluster. These PPU control all the PPU modes for all components in the cluster. A PPU is a standard component for abstracting software-controlled power domain policy to low-level hardware control signaling. There is one PPU for controlling the DSU-110 DynamiQ™ cluster power domain (PDCLUSTER). Also, each core has its own individual PPU for controlling its respective core power domain (for example, a PPU for PDCORE0 and a PPU for PDCORE1). This includes any cores included as part of a complex. A component in the system such as a <i>System Control Processor</i> (SCP) can program the PPUs through the utility bus to set the required power policy. The PPUs control the low-level details of powering up, powering down, and resetting domains as necessary to implement the requested policy. The hardware performs any actions to reach the requested power mode, such as gating clocks, cleaning and invalidating caches, or disabling coherency. Note - Although the cluster and each core in the cluster has their own PPU, the shared logic of a complex does not have a dedicated PPU. Instead, power management of the complex is controlled as a combination of the PPUs for the cores it contains. See Table 5-8: PPU mode and power domain states for a dual-core complex on page 74. - The cluster and all the core PPUs are provided as part of the DSU-110. - The implementation process automatically creates the PPU for the cluster and each core PPU, and connects these into the DSU-110 DynamiQ™ cluster. Each PPU has a set of memory-mapped control registers which is accessed using the utility bus. Arm DynamiQ™ Shared Unit-110 Technical Reference Manual at p. 78

Claim 5	Accused Products
	4.3 Power control Good power management is key to reduce system power consumption while maintaining a high performance. An RD-TC21 reference subsystem contains the following power management features: • Multiple voltage domains to allow for <i>Dynamic Voltage and Frequency Scaling</i> (DVFS) on application processors and the GPU • Multiple power-gated regions provide comprehensive leakage management • Multiple power modes for different system scenarios • A <i>System Control Processor</i> (SCP) based on a Cortex®-M3 processor controls power, clock, reset, and the static configuration of the system • <i>Power Policy Units</i> (PPUs) are used to manage power states of each voltage and power domain under the control of the SCP Arm® Total Compute 2021 Reference Design Software Developer Guide at 47-48

Claim 5	Accused Products
	SCP runtime firmware The SCP runtime firmware executes after <i>Trusted Firmware for A-profile</i> (TF-A) BL2 has authenticated and copied it from flash. The SCP runtime firmware performs the following functions: • Responds to <i>System Control and Management Interface</i> (SCMI) messages through <i>Message Handling Unit</i> (MHU) version 2.0 for processor power control and <i>Dynamic Voltage and Frequency Scaling</i> (DVFS) • Power domain management • Clock management <i>Id.</i> at p. 65

Claim 5

Accused Products

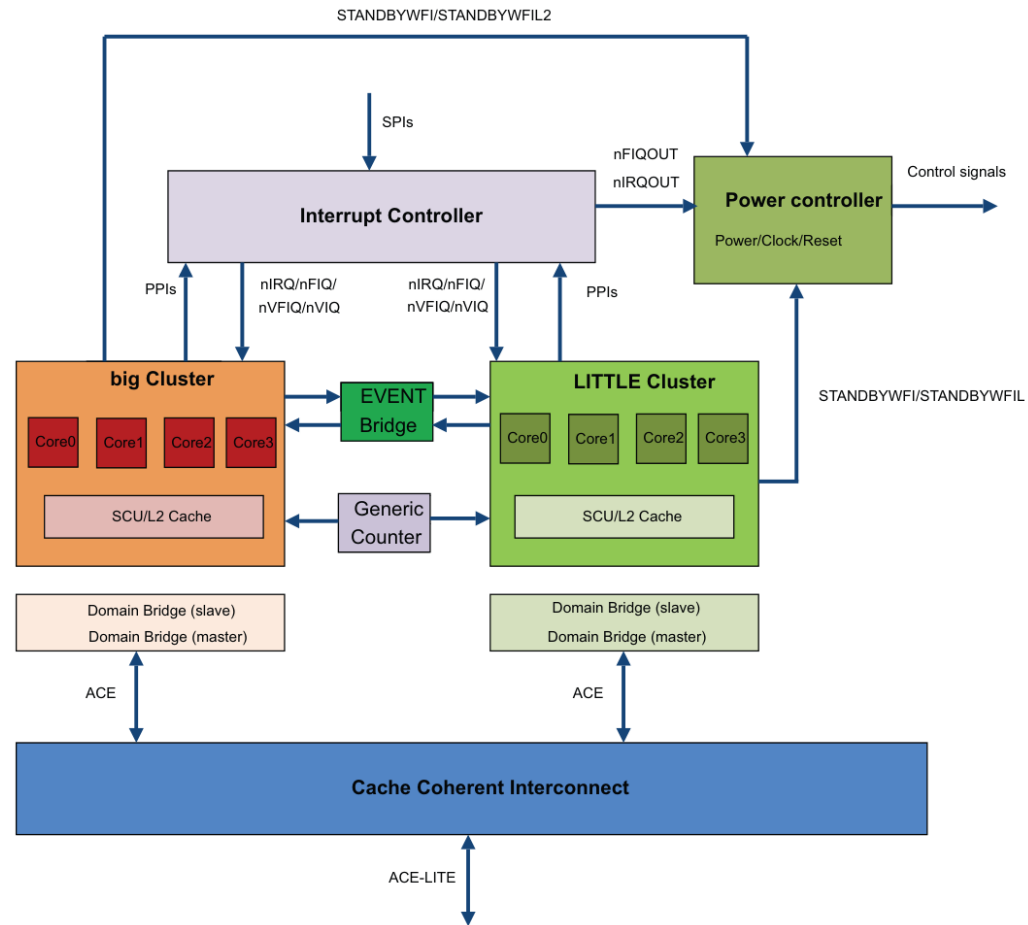


Figure 2-1 A typical big.LITTLE system

“High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at <https://developer.arm.com/documentation/dai0424/a/>, at 15 (2-3)

Claim 5	Accused Products
	2.1.1 big cluster and LITTLE cluster This example system uses a big cluster and a LITTLE cluster, and each cluster consists of four cores. There are five power domains for each cluster. Each core is in its own power domain to enable individual powerdown. The rest of the logic within a cluster is in a different power domain. Isolation cells exist between power domains for isolation. Each cluster is implemented in an independent voltage domain with an independent clock source. Each of the clusters has a unique Dynamic Voltage and Frequency Scaling (DVFS) curve. Therefore, cores in the same cluster must traverse an <i>Operating Performance Point</i> (OPP) together. You can change the OPP of cores in a cluster, without affecting the cores in the other cluster. <i>Id.</i> 2.1.2 Power controller The power controller contains the hardware power control functions of the SoC. The operations of the power controller are both directed by the <i>Operating System Power Management</i> (OSPM) software and hardware events in the system. The power controller works closely with relevant signals of ARM IPs and other system components for power saving. <i>Id.</i>

Claim 8

Claim 8	Accused Products
8. The multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.	Each Accused Product comprises a multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor. For example, on information and belief each core is located a region of the multi-core processor. Identification of the physical arrangement of the cores is proprietary information of MediaTek and/or ARM that is the proper subject of fact discovery. <i>See, e.g.:</i>

Claim 8	Accused Products
	The diagram illustrates a multi-processor system architecture. It features three distinct core types within a single system: ELP core (x1): A single ELP core Cortex[®]-X3. It includes L1I and L1D caches, and an L2 cache. "big" core (x3): Three "big" cores Cortex[®]-A715. Each core includes L1I and L1D caches, and an L2 cache. "LITTLE" core (x4): Four "LITTLE" cores Cortex[®]-A510. Each core includes L1I and L1D caches, and an L2 cache. Each core type is connected to a shared DSU (DynamIQ[™] Shared Unit-110). The DSU contains an L3 cache. The system is connected to external components via CHI (Crossbar Interconnect) interfaces.

Claim 8

Accused Products

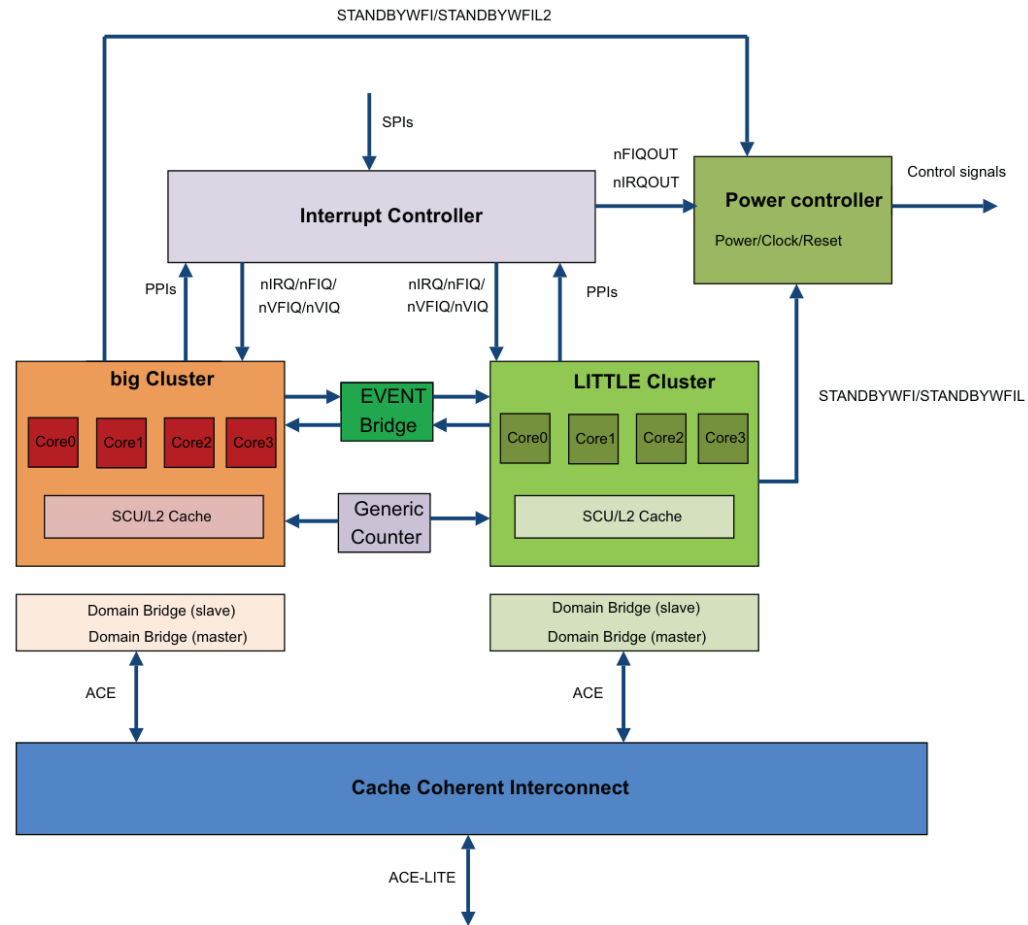


Figure 2-1 A typical big.LITTLE system

“High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at <https://developer.arm.com/documentation/dai0424/a/>, at 15 (2-3)

Claim 9

Claim 9	Accused Products
9. The multi-core processor of claim 8, wherein the first region and the second region are overlapping regions of the multi-core processor.	Each Accused Product comprises a multi-core processor of claim 8, wherein the first region and the second region are overlapping regions of the multi-core processor. For example, on information and belief there is either some overlap or no overlap of the first and second regions. Identification of the physical arrangement of the cores is proprietary information of MediaTek and/or ARM that is the proper subject of fact discovery.

Claim 10

Claim 10	Accused Products
10. The multi-core processor of claim 8, wherein the first region and the second region are non-overlapping regions of the multi-core processor.	Each Accused Product comprises a multi-core processor of claim 8, wherein the first region and the second region are non-overlapping regions of the multi-core processor. For example, on information and belief there is either some overlap or no overlap of the first and second regions. Identification of the physical arrangement of the cores is proprietary information of MediaTek and/or ARM that is the proper subject of fact discovery.

Claim 14

Claim 14	Accused Products
14. The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores	Each Accused Product comprises a multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores. See evidence and explanation of claim 5. For example, on information and belief the PPU and SCP are located in a common region that is substantially central to the processor cores. Identification of the physical arrangement of the cores is proprietary information of MediaTek and/or ARM that is the proper subject of fact discovery.

Claim 14	Accused Products
and the second set of processor cores.	

Claim 21

Claim 21	Accused Products
[21pre]. A multi-core processor, comprising:	To the extent the preamble is limiting, each Accused Product comprises a multi-core processor. <i>See analysis and evidence of claim 1 preamble above.</i>
[21a] a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block;	Each Accused Product comprises a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block. <i>See analysis and evidence of claim element [1a] above.</i> Furthermore, the MT6983 includes a power control block and a clock control block. For example, according to ARM's documents and reference design, the multi-core processor should contain a system control processor (SCP) to control voltage, power, and clocks, and power policy units (PPUs) to manage power states on each voltage domain. On information and belief, the processor in the MT6983 contains an SCP and one or more PPUs as described. For another example, according to ARM's documents and reference design, a big.LITTLE multi-core processor should contain a power controller and other controllers for supplying the voltage and clock signals as claimed. <i>See, e.g.:</i>

Claim 21	Accused Products
	6.1 The Power Policy Unit Power mode control for the <i>DynamiQ™ Shared Unit-110</i> (DSU-110) is provided by the <i>Power Policy Units</i> (PPUs) that are integrated into the cluster. These PPU control all the PPU modes for all components in the cluster. A PPU is a standard component for abstracting software-controlled power domain policy to low-level hardware control signaling. There is one PPU for controlling the DSU-110 DynamiQ™ cluster power domain (PDCLUSTER). Also, each core has its own individual PPU for controlling its respective core power domain (for example, a PPU for PDCORE0 and a PPU for PDCORE1). This includes any cores included as part of a complex. A component in the system such as a <i>System Control Processor</i> (SCP) can program the PPUs through the utility bus to set the required power policy. The PPUs control the low-level details of powering up, powering down, and resetting domains as necessary to implement the requested policy. The hardware performs any actions to reach the requested power mode, such as gating clocks, cleaning and invalidating caches, or disabling coherency. Note - Although the cluster and each core in the cluster has their own PPU, the shared logic of a complex does not have a dedicated PPU. Instead, power management of the complex is controlled as a combination of the PPUs for the cores it contains. See Table 5-8: PPU mode and power domain states for a dual-core complex on page 74. - The cluster and all the core PPUs are provided as part of the DSU-110. - The implementation process automatically creates the PPU for the cluster and each core PPU, and connects these into the DSU-110 DynamiQ™ cluster. Each PPU has a set of memory-mapped control registers which is accessed using the utility bus. Arm DynamiQ™ Shared Unit-110 Technical Reference Manual at p. 78

Claim 21	Accused Products
	4.3 Power control Good power management is key to reduce system power consumption while maintaining a high performance. An RD-TC21 reference subsystem contains the following power management features: • Multiple voltage domains to allow for <i>Dynamic Voltage and Frequency Scaling</i> (DVFS) on application processors and the GPU • Multiple power-gated regions provide comprehensive leakage management • Multiple power modes for different system scenarios • A <i>System Control Processor</i> (SCP) based on a Cortex®-M3 processor controls power, clock, reset, and the static configuration of the system • <i>Power Policy Units</i> (PPUs) are used to manage power states of each voltage and power domain under the control of the SCP Arm® Total Compute 2021 Reference Design Software Developer Guide at 47-48

Claim 21	Accused Products
	SCP runtime firmware The SCP runtime firmware executes after <i>Trusted Firmware for A-profile</i> (TF-A) BL2 has authenticated and copied it from flash. The SCP runtime firmware performs the following functions: • Responds to <i>System Control and Management Interface</i> (SCMI) messages through <i>Message Handling Unit</i> (MHU) version 2.0 for processor power control and <i>Dynamic Voltage and Frequency Scaling</i> (DVFS) • Power domain management • Clock management <i>Id.</i> at p. 65

Claim 21

Accused Products

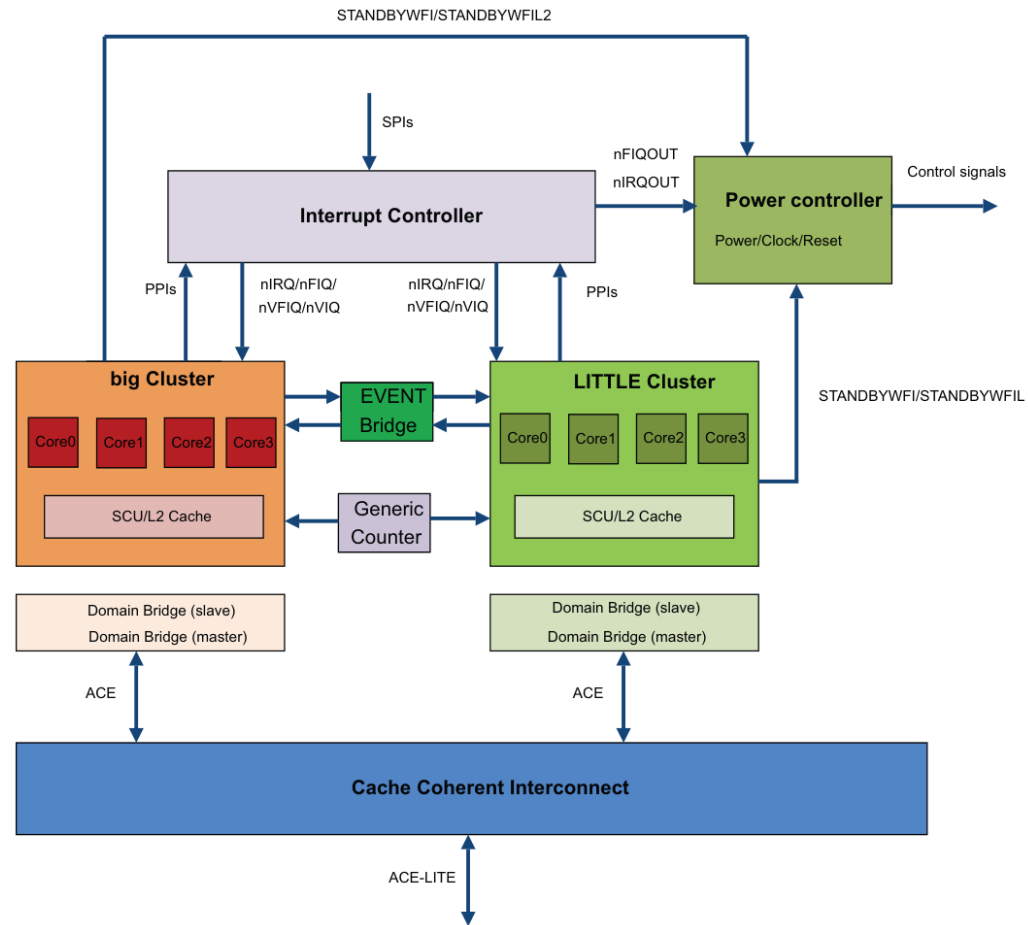


Figure 2-1 A typical big.LITTLE system

“High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at <https://developer.arm.com/documentation/dai0424/a/>, at 15 (2-3)

Claim 21	Accused Products
	2.1.1 big cluster and LITTLE cluster This example system uses a big cluster and a LITTLE cluster, and each cluster consists of four cores. There are five power domains for each cluster. Each core is in its own power domain to enable individual powerdown. The rest of the logic within a cluster is in a different power domain. Isolation cells exist between power domains for isolation. Each cluster is implemented in an independent voltage domain with an independent clock source. Each of the clusters has a unique Dynamic Voltage and Frequency Scaling (DVFS) curve. Therefore, cores in the same cluster must traverse an <i>Operating Performance Point</i> (OPP) together. You can change the OPP of cores in a cluster, without affecting the cores in the other cluster. <i>Id.</i> 2.1.2 Power controller The power controller contains the hardware power control functions of the SoC. The operations of the power controller are both directed by the <i>Operating System Power Management</i> (OSPM) software and hardware events in the system. The power controller works closely with relevant signals of ARM IPs and other system components for power saving. <i>Id.</i>
[21b] a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock signal as input in the clock	Each Accused Product comprises a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock signal as input in the clock control block, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal See analysis and evidence of claim element [1b] above. Furthermore, the MT6983 includes a power control block and a clock control block. For example, according to ARM's documents and reference design, the multi-core processor should contain a system control processor (SCP) to control voltage, power, and clocks, and power policy units

Claim 21	Accused Products
control block, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and	(PPUs) to manage power states on each voltage domain. On information and belief, the processor in the MT6983 contains an SCP and one or more PPUs as described. For another example, according to ARM's documents and reference design, a big.LITTLE multi-core processor should contain a power controller and other controllers for supplying the voltage and clock signals as claimed. <i>See, e.g.:</i>

Claim 21	Accused Products
	6.1 The Power Policy Unit Power mode control for the <i>DynamiQ™ Shared Unit-110</i> (DSU-110) is provided by the <i>Power Policy Units</i> (PPUs) that are integrated into the cluster. These PPU control all the PPU modes for all components in the cluster. A PPU is a standard component for abstracting software-controlled power domain policy to low-level hardware control signaling. There is one PPU for controlling the DSU-110 DynamiQ™ cluster power domain (PDCLUSTER). Also, each core has its own individual PPU for controlling its respective core power domain (for example, a PPU for PDCORE0 and a PPU for PDCORE1). This includes any cores included as part of a complex. A component in the system such as a <i>System Control Processor</i> (SCP) can program the PPUs through the utility bus to set the required power policy. The PPUs control the low-level details of powering up, powering down, and resetting domains as necessary to implement the requested policy. The hardware performs any actions to reach the requested power mode, such as gating clocks, cleaning and invalidating caches, or disabling coherency. Note • Although the cluster and each core in the cluster has their own PPU, the shared logic of a complex does not have a dedicated PPU. Instead, power management of the complex is controlled as a combination of the PPUs for the cores it contains. See Table 5-8: PPU mode and power domain states for a dual-core complex on page 74. • The cluster and all the core PPUs are provided as part of the DSU-110. • The implementation process automatically creates the PPU for the cluster and each core PPU, and connects these into the DSU-110 DynamiQ™ cluster. Each PPU has a set of memory-mapped control registers which is accessed using the utility bus. Arm DynamiQ™ Shared Unit-110 Technical Reference Manual at p. 78

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Claim 21	Accused Products
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Claim 21

Accused Products

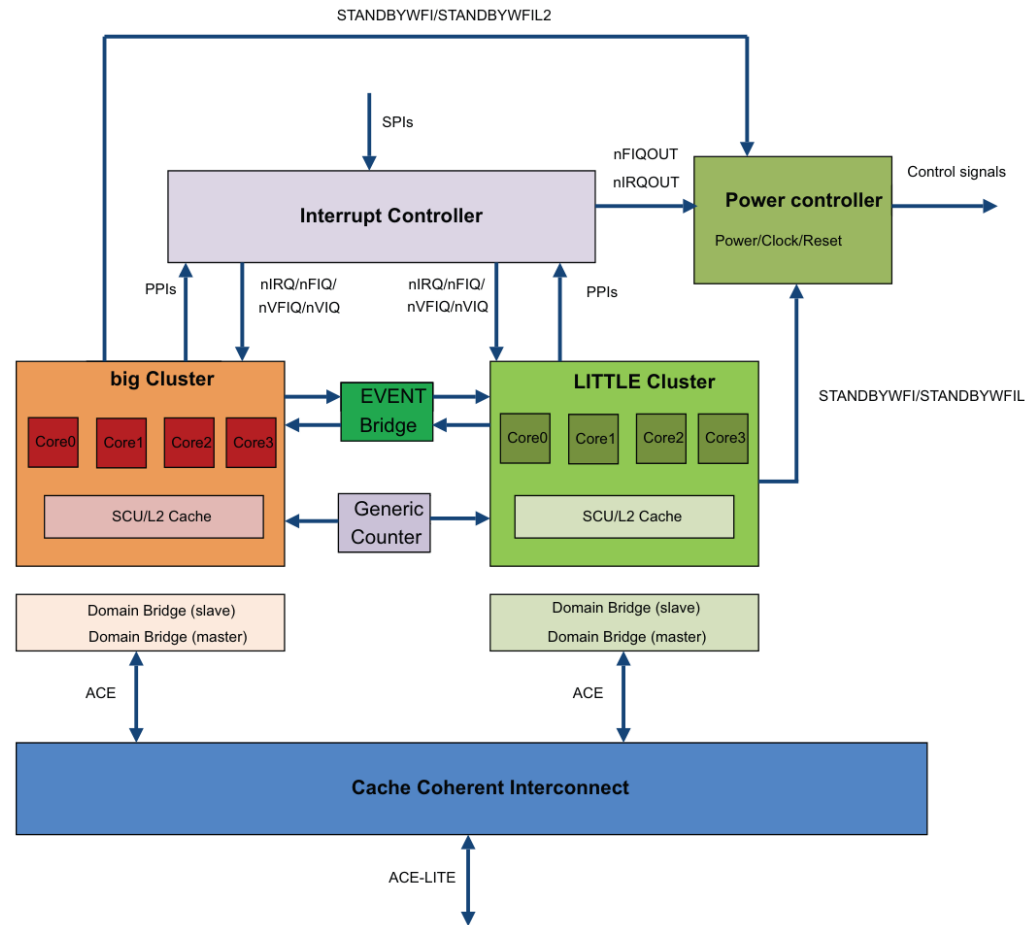


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“High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424,” available at <https://developer.arm.com/documentation/dai0424/a/>, at 15 (2-3)

Claim 21	Accused Products
	2.1.1 big cluster and LITTLE cluster This example system uses a big cluster and a LITTLE cluster, and each cluster consists of four cores. There are five power domains for each cluster. Each core is in its own power domain to enable individual powerdown. The rest of the logic within a cluster is in a different power domain. Isolation cells exist between power domains for isolation. Each cluster is implemented in an independent voltage domain with an independent clock source. Each of the clusters has a unique Dynamic Voltage and Frequency Scaling (DVFS) curve. Therefore, cores in the same cluster must traverse an <i>Operating Performance Point</i> (OPP) together. You can change the OPP of cores in a cluster, without affecting the cores in the other cluster. <i>Id.</i> 2.1.2 Power controller The power controller contains the hardware power control functions of the SoC. The operations of the power controller are both directed by the <i>Operating System Power Management</i> (OSPM) software and hardware events in the system. The power controller works closely with relevant signals of ARM IPs and other system components for power saving. <i>Id.</i>
[21c] an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.	Each Accused Product comprises an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores. See analysis and evidence of claim element [1c] above.