

'339 Patent Challenged Claim Elements

Element Designation	Claim Element
1[pre]	A multi-core processor, comprising:
1[a1]	a first set of processor cores of the multi-core processor,
1[a2]	wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;
1[b1]	a second set of processor cores of the multi-core processor,
1[b2]	wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input,
1[b3]	wherein the first supply voltage is independent from the second supply voltage, and
1[b4]	the first clock signal is independent from the second clock signal; and
1[c1]	an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores,
1[c2]	wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.
2[pre]	The multi-core processor of claim 1,
2[a]	wherein the interface block further comprises a first level shifter that is referenced to the second supply voltage and adapted to translate first logic levels associated with the first set of processor cores to second logic levels associated with the second set of processor cores for a first signal traveling from the first set of processor cores to the second set of processor cores.
3[pre]	The multi-core processor of claim 1,

3[a]	wherein the interface block further comprises a second level shifter that is referenced to the first supply voltage and adapted to translate second logic levels associated with the second set of processor cores to first logic levels associated with the first set of processor cores for a second signal traveling from the second set of processor cores to the first set of processor cores.
4[pre]	The multi-core processor of claim 1,
4[a]	wherein the interface block further comprises a synchronizer configured to synchronize the first clock signal and the second clock signal for communication between one or more processor cores of the first set of processor cores and one or more processor cores of the second set of processor cores.
5[pre]	The multi-core processor of claim 1,
5[a]	wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor.
6[pre]	The multi-core processor of claim 5,
6[a1]	wherein the first set of processor cores is adjacent to the second set of processor cores, and
6[a2]	the one or more control blocks are configured to select the first supply voltage and the second supply voltage to maintain a differential relationship between the first supply voltage and the second supply voltage.
8[pre]	The multi-core processor of claim 1,
8[a]	wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.
9[pre]	The multi-core processor of claim 8,
9[a]	wherein the first region and the second region are overlapping regions of the multi-core processor.
10[pre]	The multi-core processor of claim 8,

10[a]	wherein the first region and the second region are non-overlapping regions of the multi-core processor.
11[pre]	The multi-core processor of claim 8,
11[a]	wherein the first region corresponds to a first row of the multi-core processor, and wherein the second region corresponds to a second row of the multi-core processor.
14[pre]	The multi-core processor of claim 1,
14[a]	wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores.
21[pre]	A multi-core processor, comprising:
21[a1]	a first set of processor cores of the multi-core processor,
21[a2]	wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block;
21[b1]	a second set of processor cores of the multi-core processor,
21[b2]	wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock signal as input in the clock control block,
21[b3]	wherein the first supply voltage is independent from the second supply voltage, and
21[b4]	the first clock signal is independent from the second clock signal; and
21[c1]	an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores,
21[c2]	wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.