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| APPLICATION NUMBER | PATENT NUMBER | GROUP ART UNIT | REQUEST ID |
|---|---|---|---|
| 11/688,338 | 8264003 | 2826 | 20726 |

## PAIR Correspondence Address/Fee Address Change

The following fields have been changed to Customer Number 138391 on 06/30/2016 via Private PAIR in view of the certification copied below that authorized the change.

- Correspondence Address

The address for Customer Number 138391 is:
138391
Farjami & Farjami LLP
26522 La Almeda Ave.
Suite 360
Mission Viejo, CA 92691

**I certify, in accordance with 37 CFR 1.4(d)(4) that I am:**

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

| | |
|---|---|
| **Signature:** | /MF/ |
| **Name:** | Michael Farjami |
| **Registration Number:** | 38135 |

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| APPLICATION NUMBER | PATENT NUMBER | GROUP ART UNIT | REQUEST ID |
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| 11/688,338 | 8264003 | 2826 | 20726 |

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- Maintenance Fee Address

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138391
Farjami & Farjami LLP
26522 La Almeda Ave.
Suite 360
Mission Viejo, CA 92691

**I certify, in accordance with 37 CFR 1.4(d)(4) that I am:**

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United States Patent and Trademark Office
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| APPLICATION NO. | ISSUE DATE | PATENT NO. | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/688,338 | 09/11/2012 | 8264003 | 0400131 | 9886 |

25700 7590 08/22/2012

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

# ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Thomas Herman, Manhattan Beach, CA;

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1 Fax

# PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail** Mail Stop ISSUE FEE
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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25700 7590 05/04/2012
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26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

OPAP IAP11 AUG 03 2012 PATENT & TRADEMARK OFFICE

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Nicole Humphers (Depositor's name)
NHumphers (Signature)
August 3, 2012 (Date)

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | Thomas Herman | 0400131 | 9886 |

TITLE OF INVENTION: MERGED GATE CASCODE TRANSISTOR

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | NO | $1740 | $300 | $0 | $2040 | 08/06/2012 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| AHMED, SELIM U | 2826 | 257-147000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 FARJAMI & FARJAMI LLP
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: **International Rectifier Corporation**

(B) RESIDENCE: (CITY and STATE OR COUNTRY): **El Segundo, CA**

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies 2

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-0731 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date August 3, 2012

Typed or printed name Michael Farjami Registration No. 38,135

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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08/06/2012 EEKUBAY2 00000028 11688338
01 FC:1501 1740.00 OP
02 FC:1504 300.00 OP
03 FC:8001 6.00 OP



PAGE 6/6 * RCVD AT 8/3/2012 2:52:42 PM [Eastern Daylight Time] * SVR:W-PTOFAX-003/4 * DNIS:2732885 * CSID:949 282 1002 * DURATION (mm-ss):01-35

FARJAMI & FARJAMI LLP
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www.farjami.com

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26522 La Alameda Avenue, Suite 360
Mission Viejo, California 92691
tel: (949) 282-1000
fax: (949) 282-1002

## FACSIMILE TRANSMISSION COVER SHEET

Date: August 3, 2012

To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826

Fax: (571) 273-2885

Re: **Application Serial No.: 11/688,338**
Filing Date: 03/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 6

Message:

Enclosed please find the Issue Fee, Publication Fee, and Fee for Two (2) Copies of the Issued Patent.

Payment for Issue Fee in the Amount of $2,046.00 is hereby enclosed on Form PTO-2038.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication, or credit any overpayment to deposit Account No. 50-0731.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.




Attorney Docket No.: 0400131

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| Applicant(s): **Herman, Thomas** | Group Art Unit: **2826** |
| Application Serial No.: **11/688,338** | Examiner: **Ahmed, Selim U.** |
| Filed: **03/20/2007** | Notice of Allowance: **May 4, 2012** |
| Title: **Merged Gate Cascode Transistor** | |

## ISSUE FEE, PUBLICATION FEE AND FEE FOR TWO COPIES OF THE ISSUED PATENT

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

Enclosed, please find the completed "Issue Fee Transmittal" form and a "Payment by Credit Card" form (PTO-2038) in the amount of $2,046.00 to cover the issue fee, publication fee, and fee for two (2) copies of the issued patent. The drawings filed in the present application have been accepted as formal drawings by the Examiner.

## COMMENTS ON STATEMENTS OF REASONS FOR ALLOWANCE

The Applicant recognizes that in accordance with M.P.E.P. § 1302.14, the reasons for allowance provided by the Examiner do not necessarily include all of the reasons why the claims are allowed. The Applicant does not concede that the stated reasons for allowance are the only grounds for patentability of the allowed claims or that any element excluded from the Examiner's Reasons for Allowance is taught or suggested by the art of record.

Further, the Applicant does not concede that all of the elements identified by the Examiner are required to distinguish the prior art of record or to satisfy the requirements of 35 U.S.C. § 112. In addition, the Examiner does not assert, and the Applicant would not agree, that the stated reasons for allowance have any bearing on the patentability of claims in any other applications.

Each dependent claim stands on its own and is allowable based on its own elements or in combination with one or more elements recited in its base claim(s). The combination of elements need not include all of the elements identified in the stated reasons for allowance.

The Commissioner is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number **50-0731**.



PAGE 3/6 * RCVD AT 8/3/2012 2:52:42 PM [Eastern Daylight Time] * SVR:W-PTOFAX-003/4 * DNIS:2732885 * CSID:949 282 1002 * DURATION (mm-ss):01-35

An early issuance of the present application is respectfully requested.

Respectfully Submitted;
FARJAMI & FARJAMI LLP

Dated: 8/3/12

Michael Farjami, Esq.
Reg. No. 38,135
FARJAMI & FARJAMI LLP
Attorneys for Applicant

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Tel: (949) 282-1000
Fax: (949) 282-1002

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Date: 8.3.12

Nicole Humphers
Name of Person Mailing or Transmitting Paper and/or Fee

NHumphers
Signature



PAGE 4/6 * RCVD AT 8/3/2012 2:52:42 PM [Eastern Daylight Time] * SVR:W-PTOFAX-003/4 * DNIS:2732885 * CSID:949 282 1002 * DURATION (mm-ss):01-35

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| APPLICATION NUMBER | FILING or 371(c) DATE | GRP ART UNIT | FIL FEE REC'D | ATTY.DOCKET.NO | TOT CLAIMS | IND CLAIMS |
|---|---|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | 2826 | 1130 | 0400131 | 16 | 2 |

**CONFIRMATION NO. 9886**

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

**CORRECTED FILING RECEIPT**




Date Mailed: 06/15/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

**Applicant(s)**

Thomas Herman, Manhattan Beach, CA;

**Power of Attorney:** The patent practitioners associated with Customer Number 25700

**Domestic Priority data as claimed by applicant**

This appln claims benefit of 60/783,934 03/20/2006

**Foreign Applications** (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

**If Required, Foreign Filing License Granted:** 03/29/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 11/688,338**

**Projected Publication Date:** Not Applicable

**Non-Publication Request:** No

**Early Publication Request:** No

**Title**

MERGED CASCODE TRANSISTOR

**Preliminary Class**

257

## PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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## Title 37, Code of Federal Regulations, 5.11 & 5.15

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# NOTICE OF ALLOWANCE AND FEE(S) DUE

25700 7590 05/04/2012

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

| EXAMINER |
|---|
| AHMED, SELIM U |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 05/04/2012

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | Thomas Herman | 0400131 | 9886 |

TITLE OF INVENTION: MERGED GATE CASCODE TRANSISTOR

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | NO | $1740 | $300 | $0 | $2040 | 08/06/2012 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

**HOW TO REPLY TO THIS NOTICE:**

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25700 7590 05/04/2012

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

| |
|---|
| (Depositor's name) |
| (Signature) |
| (Date) |

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | Thomas Herman | 0400131 | 9886 |

TITLE OF INVENTION: MERGED GATE CASCODE TRANSISTOR

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | NO | $1740 | $300 | $0 | $2040 | 08/06/2012 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| AHMED, SELIM U | 2826 | 257-147000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



PTOL-85 (Rev. 02/11) Approved for use through 08/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | Thomas Herman | 0400131 | 9886 |

25700 7590 05/04/2012

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

| EXAMINER | |
|---|---|
| AHMED, SELIM U | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 05/04/2012

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

## Privacy Act Statement

**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 11/688,338 | HERMAN, THOMAS | |
| | Examiner | Art Unit | |
| | SELIM AHMED | 2826 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/21/2012*.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-16*.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4/23/2012.
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/VICTOR A MANDALA/
Primary Examiner, Art Unit 2826

## DETAILED ACTION

1. The office action responds to the amendment filed on 3/21/2012.

### Acknowledgement

**2.** The amendment filed on 3/21/2012, responding to the office action mailed on 12/21/2011, has been entered into the record. The present office action is made with all the suggested amendments being fully considered. Accordingly, pending in this office action are claims 1-16.

## EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as per telephone authorization from applicant's attorney Mr. Michael Farjami on 4/30/2012 as follows:

- In line 30 (last line) of claim 1, "enhancement" has been replaced with --depletion--.
- In line 32 (last line) of claim 10, "enhancement" has been replaced with --depletion--.

***Allowable Subject Matter***

4. Claims 1-16 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 1-9 are allowed because the prior art of record neither anticipates nor renders obvious the limitations of the base claim 1 that recites a merged cascade transistor circuit particularly with wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element in combination with other elements of the base claim 1.

Claims 10-16 are allowed because the prior art of record neither anticipates nor renders obvious the limitations of the base claim 10 that recites a merged cascade high electron mobility transistor circuit particularly with wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element in combination with other elements of the base claim 10.

Any comments considered necessary by applicant must be submitted no later than the payment of issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Davienne Monbleau can be reached on (571)272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SELIM AHMED/
Examiner, Art Unit 2826
/VICTOR A MANDALA/
Primary Examiner, Art Unit 2826

PAP
APR 23 2012
PATENT & TRADEMARK OFFICE

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| In re Application of: | Art Unit: 2826 |
| **Herman, Thomas** | Examiner: Ahmed, Selim U. |
| Serial No.: **11/688,338** | |
| Filed: **March 20, 2007** | |
| For: **Merged Gate Cascode Transistor** | |

## INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

In this Information Disclosure Statement and pursuant to 37 C.F.R. §§ 1.56 and 1.97, Applicants hereby disclose to the Patent Office patents, publications or other information of which Applicants are aware. A list of references is included in Form 1449 submitted herewith.

The items identified in this Information Disclosure Statement may or may not be "material" as defined in 37 C.F.R. § 1.56, and the submission thereof by Applicants is not to be construed as an admission that any such patent, publication or other information referred to is material or considered to be material (37 C.F.R. § 1.97(h)), or even qualifies as "prior art" under 35 U.S.C. § 102 with respect to the present invention unless specifically designated by Applicants as such. Identification of any reference or patent herein is not an admission, nor is it to be construed as an admission, that it was invented prior to the invention disclosed herein.



REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.A./

The filing of this Information Disclosure Statement is not to be construed to mean that a search has been made or that no other material information, as defined in 37 C.F.R. § 1.56, exists.

In accordance with 37 C.F.R. § 1.97 no fee is believed due at this time, since this Information Disclosure Statement is filed in accordance with 37 C.F.R. §§ 1.97(c) and 1.97(e)(1). This information disclosure statement is being filed before the mailing date of any of a final action under § 1.113, a notice of allowance under § 1.311, or an action that otherwise closes prosecution in the application and each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. The Assistant Commissioner is hereby authorized to charge or credit Deposit Account Number **50-0731** for any deficiency or overpayment in the fees required for the filing of this Information Disclosure Statement.

Respectfully submitted,

Farjami & Farjami LLP

Dated: 4/19/12

By: _____
Michael Farjami
Reg. No. 38, 135
Attorneys for Applicants

*CERTIFICATE OF MAILING*
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on:

4.19.12
Date

Nhumphers
Signature

Nicole Humphers
Typed or Printed Name of Person Mailing Paper and/or Fee

Michael Farjami, Esq.
Farjami & Farjami LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, CA 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002



REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.A./

PATENT & TRADEMARK OFFICE APR 23 2012 OPAP
OPAP APR 23 2012 PATENT & TRADEMARK OFFICE

| FORM PTO-1449 LIST OF PATENTS AND OTHER ITEMS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) | ATTY. DOCKET NO. 0400131 | SERIAL NO. 11/688,338 |
|---|---|---|
| | APPLICANTS: Herman, Thomas | |
| | FILING DATE: March 20, 2007 | GROUP ART: 2826 |

| U.S. PATENT DOCUMENTS | | | | | | | |
|---|---|---|---|---|---|---|---|
| Exam. Initials | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
| | AA | | | | | | |

| FOREIGN PATENT DOCUMENT | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Exam. Initials | | DOCUMENT NUMBER | PUBLICATION DATE | COUNTRY OR PATENT OFFICE | CLASS | SUB CLASS | TRANSLATION YES | TRANSLATION NO |
| | BA | JP 2001-210657 | 8/03/01 | JAPAN | | | | |
| | BB | JP 2002-076020 | 3/15/02 | JAPAN | | | | |
| | BC | WO 2005/079370 | 9/01/05 | WIPO | | | | |
| | BD | JP 2008-522436 | 6/26/08 | JAPAN | | | | |

| OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.) | | |
|---|---|---|
| | CA | |

| EXAMINER: /Selim Ahmed/ | DATE CONSIDERED: 04/30/2012 |
|---|---|

**EXAMINER: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.**





REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.A./

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11688338 | HERMAN, THOMAS |
| | Examiner | Art Unit |
| | SELIM AHMED | 2826 |

## SEARCHED

| Class | Subclass | Date | Examiner |
|---|---|---|---|
| 257 | 192, 194, 195, E29.14, E29.144, E29.246, E29.249 | 5/22/08 | SA |
| | Updated search | 12/8/08 | /sa/ |
| | Updated search | 3/20/2009 | /sa/ |
| | Updated search | 6/20/2009 | /sa/ |
| | Updated search | 9/24/2010 | /sa/ |
| | Updated search | 4/9/2011 | /sa/ |
| | Updated search | 12/17/2011 | /sa/ |

## SEARCH NOTES

| Search Notes | Date | Examiner |
|---|---|---|
| Text search such as two dimensional electron gas, Cascode transistor, HEMT/High electron mobility transistor, source, drain, gate and their boolean combinations were searched. | 5/22/08 | SA |
| Updated search | 12/8/2008 | /sa/ |
| Updated search | 3/20/2009 | /sa/ |
| Updated search | 9/24/2010 | /sa/ |
| Updated search | 4/9/2011 | /sa/ |
| Updated search | 12/11/2011 | /sa/ |

## INTERFERENCE SEARCH

| Class | Subclass | Date | Examiner |
|---|---|---|---|
| 257 | 192, 194, 195, | 5/22/08 | SA |
| | Claim, Inventor, assignee interference search | 4/21/2012 | /sa/ |

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

# BIB DATA SHEET

**CONFIRMATION NO. 9886**

| SERIAL NUMBER | FILING or 371(c) DATE<br>RULE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | 257 | 2826 | 0400131 |

**APPLICANTS**
Thomas Herman, Manhattan Beach, CA;

**** CONTINUING DATA ***************************
This appln claims benefit of 60/783,934 03/20/2006

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/29/2007

| Foreign Priority claimed ☐ Yes ☑ No<br>35 USC 119(a-d) conditions met ☐ Yes ☑ No<br>Verified and Acknowledged /SELIM U AHMED/ Examiner's Signature | ☐ Met after Allowance<br>Initials | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|
| | | CA | 4 | 16 | 2 |

**ADDRESS**

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691
UNITED STATES

**TITLE**

MERGED GATE CASCODE TRANSISTOR

| FILING FEE RECEIVED | FEES: Authority has been given in Paper | ☐ All Fees |
|---|---|---|
| 1130 | No._____ to charge/credit DEPOSIT ACCOUNT | ☐ 1.16 Fees (Filing) |
| | No._____ for following: | ☐ 1.17 Fees (Processing Ext. of time) |
| | | ☐ 1.18 Fees (Issue) |
| | | ☐ Other _____ |
| | | ☐ Credit |

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11688338 | HERMAN, THOMAS |
| | **Examiner** | **Art Unit** |
| | SELIM AHMED | 2826 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 05/22/2008 | 12/08/2008 | 03/20/2009 | 06/20/2009 | 09/25/2010 | 04/09/2011 | 12/17/2011 | 04/21/2012 | |
| | 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 3 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 5 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 6 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 7 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 8 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 9 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 10 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 11 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 12 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 13 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 14 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 15 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |
| | 16 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | = | |

**EAST Search History**

**EAST Search History (Prior Art)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L5 | 1 | 11/688338 | US-PGPUB; USPAT | OR | OFF | 2012/04/21 20:16 |
| L24 | 83 | ((THOMAS) near2 (HERMAN)).INV. | US-PGPUB; USPAT | OR | OFF | 2012/04/21 21:03 |
| L25 | 1413 | (international near rectifier near corporation).asn. | US-PGPUB; USPAT | OR | ON | 2012/04/21 21:07 |
| L26 | 101 | l25 and (HEMT or (high near electron near mobility near transistor)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2012/04/21 21:07 |
| S3 | 4541 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:21 |
| S4 | 7876 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S5 | 314831 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S6 | 73 | S3 and S4 and S5 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S7 | 96 | S3 and S4 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:23 |
| S8 | 63 | S6 and @ad<"20060320" | US-PGPUB; USPAT; | OR | ON | 2008/05/21 17:23 |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S9 | 82 | S7 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:24 |
| S10 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 17:33 |
| S11 | 9 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 17:34 |
| S12 | 1404 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:53 |
| S13 | 1116 | S5 and S12 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:54 |
| S14 | 356 | S5 and S12 and S4 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:54 |
| S15 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:00 |
| S16 | 5 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:01 |
| S17 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:05 |
| S18 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| | US-PGPUB; USPAT; USOCR; | OR | OFF | 2008/05/21 18:20 |

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|---|---|---|---|---|---|---|
| | | "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S19 | 16 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:25 |
| S20 | 1635 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:28 |
| S21 | 1200 | S5 and S20 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:29 |
| S22 | 773 | S5 and S20 and S4 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:29 |
| S23 | 706 | S22 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:30 |
| S24 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:45 |
| S25 | 275 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:46 |
| S26 | 232 | S25 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:46 |
| S27 | 232 | S25 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:46 |
| S28 | 121 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/22 10:38 |
| S29 | 310043 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | OFF | 2008/05/22 15:10 |

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|---|---|---|---|---|---|---|
| | | | IBM_TDB | | | |
| S30 | 556 | S29 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/22 15:11 |
| S31 | 852 | S29 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/22 15:11 |
| S32 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S33 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S34 | 4811 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S35 | 8419 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S36 | 332843 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S37 | 80 | S34 and S35 and S36 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S38 | 107 | S34 and S35 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2008/12/08 09:49 |

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|---|---|---|---|---|---|---|
| | | | JPO; DERWENT; IBM_TDB | | | |
| S39 | 65 | S37 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S40 | 85 | S38 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S41 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S42 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S43 | 1425 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S44 | 1137 | S36 and S43 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S45 | 365 | S36 and S43 and S35 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S46 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S47 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S48 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |

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|---|---|---|---|---|---|---|
| | | "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | | | | |
| S49 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S50 | 18 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S51 | 1782 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S52 | 1310 | S36 and S51 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S53 | 847 | S36 and S51 and S35 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S54 | 725 | S53 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S55 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S56 | 312 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S57 | 244 | S56 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S58 | 244 | S56 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S59 | 125 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S60 | 321547 | "257"/("192", "194", "195", "E29.14", | US-PGPUB; | OR | OFF | 2008/12/08 |

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| | | "E29.144", "E29.246", "E29.249").ccls. | USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | 09:49 |
| S61 | 596 | S60 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S62 | 915 | S60 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S63 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S64 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S65 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S66 | 82 | S63 and S64 and S65 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S67 | 66 | S66 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S68 | 1 | S67 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | ON | 2009/03/19 18:03 |

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| | | | IBM_TDB | | | |
| S69 | 8 | S67 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:05 |
| S70 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:13 |
| S71 | 944 | S70 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:13 |
| S72 | 549 | S71 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:13 |
| S73 | 213 | S72 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:14 |
| S74 | 15 | S73 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:15 |
| S75 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:27 |
| S76 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:27 |
| S77 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/19 18:31 |

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|---|---|---|---|---|---|---|
| | | "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | | | | |
| S78 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S79 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S80 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S81 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S82 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S83 | 82 | S80 and S81 and S82 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S84 | 109 | S80 and S81 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S85 | 66 | S83 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S86 | 86 | S84 and @ad<"20060320" | US-PGPUB; | OR | ON | 2009/03/20 |

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|---|---|---|---|---|---|---|
| | | | USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | 00:20 |
| S87 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S88 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S89 | 1438 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S90 | 1150 | S82 and S89 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S91 | 373 | S82 and S89 and S81 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S92 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S93 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S94 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S95 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |

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|---|---|---|---|---|---|---|
| S96 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S97 | 1868 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S98 | 1378 | S82 and S97 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S99 | 896 | S82 and S97 and S81 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S100 | 737 | S99 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S101 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S102 | 334 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S103 | 246 | S102 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S104 | 246 | S102 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S105 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S106 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S107 | 622 | S106 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | OFF | 2009/03/20 00:20 |

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| | | | IBM_TDB | | | |
| S108 | 944 | S106 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S109 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S110 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S111 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S112 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S113 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S114 | 82 | S111 and S112 and S113 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S115 | 109 | S111 and S112 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S116 | 66 | S114 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/03/20 00:20 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S117 | 86 | S115 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S118 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S119 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S120 | 1438 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S121 | 1150 | S113 and S120 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S122 | 373 | S113 and S120 and S112 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S123 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S124 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S125 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S126 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | OFF | 2009/03/20 00:20 |

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|---|---|---|---|---|---|---|
| | | "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | DERWENT; IBM_TDB | | | |
| S127 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S128 | 1868 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S129 | 1378 | S113 and S128 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S130 | 896 | S113 and S128 and S112 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S131 | 737 | S130 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S132 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S133 | 334 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S134 | 246 | S133 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S135 | 246 | S133 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S136 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S137 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S138 | 622 | S137 and ((two near dimension$3 near | US-PGPUB; | OR | OFF | 2009/03/20 |

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| | | electron near gas) or 2DEG) | USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | 00:20 |
| S139 | 944 | S137 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S140 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S141 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S142 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S143 | 82 | S140 and S141 and S142 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S144 | 66 | S143 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S145 | 1 | S144 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S146 | 8 | S144 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | ON | 2009/03/20 00:20 |

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| | | | IBM_TDB | | | |
| S147 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S148 | 944 | S147 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S149 | 549 | S148 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S150 | 213 | S149 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S151 | 15 | S150 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S152 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S153 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S154 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S155 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; | OR | ON | 2009/06/18 12:52 |

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| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S156 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S157 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S158 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S159 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S160 | 85 | S157 and S158 and S159 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S161 | 116 | S157 and S158 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S162 | 67 | S160 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S163 | 89 | S161 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S164 | 5 | ("5155449" \| "5774792" \| "5939945" \| | US-PGPUB; | OR | OFF | 2009/06/18 |

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| | | "6137367" \| "6515547").PN. OR ("7071786").URPN. | USPAT; USOCR | | | 12:52 |
| S165 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S166 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S167 | 1162 | S159 and S166 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S168 | 378 | S159 and S166 and S158 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S169 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S170 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S171 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S172 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S173 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S174 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; | OR | OFF | 2009/06/18 12:52 |

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| | | | USOCR | | | |
| S175 | 1427 | S159 and S174 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S176 | 930 | S159 and S174 and S158 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S177 | 745 | S176 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S178 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S179 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S180 | 248 | S179 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S181 | 248 | S179 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S182 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S183 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S184 | 641 | S183 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S185 | 977 | S183 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | OFF | 2009/06/18 12:52 |

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| | | | DERWENT; IBM_TDB | | | |
| S186 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S187 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S188 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S189 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S190 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S191 | 85 | S188 and S189 and S190 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S192 | 116 | S188 and S189 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S193 | 67 | S191 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S194 | 89 | S192 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; | OR | ON | 2009/06/18 12:52 |

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|---|---|---|---|---|---|---|
| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S195 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S196 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S197 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S198 | 1162 | S190 and S197 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S199 | 378 | S190 and S197 and S189 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S200 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S201 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S202 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S203 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S204 | 19 | ("4764796" \| "5099295" \| "5192987" \| | US-PGPUB; | OR | OFF | 2009/06/18 |

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|---|---|---|---|---|---|---|
| | | "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | USPAT; USOCR | | | 12:52 |
| S205 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S206 | 1427 | S190 and S205 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S207 | 930 | S190 and S205 and S189 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S208 | 745 | S207 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S209 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S210 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S211 | 248 | S210 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S212 | 248 | S210 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S213 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S214 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S215 | 641 | S214 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |

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|---|---|---|---|---|---|---|
| S216 | 977 | S214 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S217 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S218 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S219 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S220 | 85 | S217 and S218 and S219 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S221 | 67 | S220 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S222 | 1 | S221 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S223 | 8 | S221 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S224 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | OFF | 2009/06/18 12:52 |

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| | | | DERWENT; IBM_TDB | | | |
| S225 | 977 | S224 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S226 | 567 | S225 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S227 | 217 | S226 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S228 | 18 | S227 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S229 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S230 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S231 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S232 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S233 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; | OR | ON | 2009/06/18 12:52 |

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| | | | USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S234 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S235 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S236 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S237 | 85 | S234 and S235 and S236 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S238 | 116 | S234 and S235 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S239 | 67 | S237 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S240 | 89 | S238 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S241 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S242 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |

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| | | ("7026669").URPN. | | | | |
| S243 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S244 | 1162 | S236 and S243 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S245 | 378 | S236 and S243 and S235 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S246 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S247 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S248 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S249 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S250 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S251 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S252 | 1427 | S236 and S251 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S253 | 930 | S236 and S251 and S235 | US-PGPUB; USPAT; | OR | OFF | 2009/06/18 12:52 |

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| | | | USOCR | | | |
| S254 | 745 | S253 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S255 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S256 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S257 | 248 | S256 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S258 | 248 | S256 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S259 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S260 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S261 | 641 | S260 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S262 | 977 | S260 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S263 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/18 12:52 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S264 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S265 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S266 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S267 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S268 | 85 | S265 and S266 and S267 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S269 | 116 | S265 and S266 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S270 | 67 | S268 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S271 | 89 | S269 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S272 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR | US-PGPUB; USPAT; | OR | OFF | 2009/06/18 12:52 |

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| | | ("7071786").URPN. | USOCR | | | |
| S273 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S274 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S275 | 1162 | S267 and S274 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S276 | 378 | S267 and S274 and S266 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S277 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S278 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S279 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S280 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S281 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S282 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |

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| S283 | 1427 | S267 and S282 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S284 | 930 | S267 and S282 and S266 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S285 | 745 | S284 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S286 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S287 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S288 | 248 | S287 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S289 | 248 | S287 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S290 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S291 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S292 | 641 | S291 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S293 | 977 | S291 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | OFF | 2009/06/18 12:52 |

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| | | | IBM_TDB | | | |
| S294 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S295 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S296 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S297 | 85 | S294 and S295 and S296 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S298 | 67 | S297 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S299 | 1 | S298 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S300 | 8 | S298 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S301 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S302 | 977 | S301 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | OFF | 2009/06/18 12:52 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S303 | 567 | S302 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S304 | 217 | S303 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S305 | 18 | S304 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S306 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S307 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S308 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S310 | 8 | ("5629539" \| "5691252" \| "5990507" \| "6174735" \| "6245631" \| "6278150" \| "6291292" \| "6337274").PN. OR ("6707088").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 13:08 |
| S314 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S315 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/20 16:18 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S316 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S317 | 85 | S314 and S315 and S316 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S318 | 116 | S314 and S315 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S323 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S324 | 1162 | S316 and S323 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S331 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S332 | 1427 | S316 and S331 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S333 | 930 | S316 and S331 and S315 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S335 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S337 | 248 | S336 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S340 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; | OR | OFF | 2009/06/20 16:18 |

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| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S342 | 977 | S340 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S345 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S346 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S347 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S348 | 85 | S345 and S346 and S347 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S349 | 116 | S345 and S346 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S354 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S355 | 1162 | S347 and S354 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S362 | 1932 | (two near dimensional near electron | US-PGPUB; | OR | OFF | 2009/06/20 |

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| | | near gas) or 2DEG | USPAT; USOCR | | | 16:18 |
| S363 | 1427 | S347 and S362 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S364 | 930 | S347 and S362 and S346 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S366 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S368 | 248 | S367 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S371 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S373 | 977 | S371 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S374 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S375 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S376 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S377 | 85 | S374 and S375 and S376 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |

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| S378 | 67 | S377 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S381 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S382 | 977 | S381 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S383 | 567 | S382 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S391 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S392 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S393 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S394 | 85 | S391 and S392 and S393 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S395 | 116 | S391 and S392 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | ON | 2009/06/20 16:18 |

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| | | | DERWENT; IBM_TDB | | | |
| S400 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S401 | 1162 | S393 and S400 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S408 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S409 | 1427 | S393 and S408 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S410 | 930 | S393 and S408 and S392 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S412 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S414 | 248 | S413 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S417 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S419 | 977 | S417 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S422 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S423 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/20 16:18 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S424 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S425 | 85 | S422 and S423 and S424 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S426 | 116 | S422 and S423 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S431 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S432 | 1162 | S424 and S431 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S439 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S440 | 1427 | S424 and S439 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S441 | 930 | S424 and S439 and S423 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S443 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S445 | 248 | S444 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S448 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; | OR | OFF | 2009/06/20 16:18 |

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| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S450 | 977 | S448 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S451 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S452 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S453 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S454 | 85 | S451 and S452 and S453 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S455 | 67 | S454 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S458 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S459 | 977 | S458 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S460 | 567 | S459 and (epi or epitaxial) | US-PGPUB; | OR | ON | 2009/06/20 |

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| | | | USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | 16:18 |
| S468 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S469 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S470 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S471 | 85 | S468 and S469 and S470 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S472 | 116 | S468 and S469 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S477 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S478 | 1162 | S470 and S477 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S485 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S486 | 1427 | S470 and S485 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |

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| S487 | 930 | S470 and S485 and S469 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S489 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S491 | 248 | S490 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S494 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S496 | 977 | S494 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S499 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S500 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S501 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S502 | 85 | S499 and S500 and S501 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S503 | 116 | S499 and S500 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | ON | 2009/06/20 16:18 |

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| | | | IBM_TDB | | | |
| S508 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S509 | 1162 | S501 and S508 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S516 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S517 | 1427 | S501 and S516 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S518 | 930 | S501 and S516 and S500 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S520 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S522 | 248 | S521 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S525 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S527 | 977 | S525 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S528 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S529 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | ON | 2009/06/20 16:18 |

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| | | | DERWENT; IBM_TDB | | | |
| S530 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S531 | 85 | S528 and S529 and S530 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S532 | 67 | S531 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S535 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S536 | 977 | S535 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S537 | 567 | S536 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S545 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S546 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S549 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; | OR | ON | 2009/06/20 16:22 |

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| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S550 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S551 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S552 | 85 | S549 and S550 and S551 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S553 | 116 | S549 and S550 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S558 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S559 | 1162 | S551 and S558 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S566 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S567 | 1427 | S551 and S566 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S568 | 930 | S551 and S566 and S550 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S570 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S572 | 248 | S571 and @ad<"20060320" | US-PGPUB; USPAT; | OR | ON | 2009/06/20 16:22 |

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| | | | USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S575 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S577 | 977 | S575 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S580 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S581 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S582 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S583 | 85 | S580 and S581 and S582 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S584 | 116 | S580 and S581 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S589 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |

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| S590 | 1162 | S582 and S589 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S597 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S598 | 1427 | S582 and S597 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S599 | 930 | S582 and S597 and S581 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S601 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S603 | 248 | S602 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S606 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S608 | 977 | S606 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S609 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S610 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S611 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | ON | 2009/06/20 16:22 |

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| | | | IBM_TDB | | | |
| S612 | 85 | S609 and S610 and S611 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S613 | 67 | S612 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S616 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S617 | 977 | S616 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S618 | 567 | S617 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S626 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S627 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S628 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S629 | 85 | S626 and S627 and S628 | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/20 16:22 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S630 | 116 | S626 and S627 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S635 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S636 | 1162 | S628 and S635 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S643 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S644 | 1427 | S628 and S643 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S645 | 930 | S628 and S643 and S627 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S647 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S649 | 248 | S648 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S652 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S654 | 977 | S652 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S657 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; | OR | ON | 2009/06/20 16:22 |

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| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S658 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S659 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S660 | 85 | S657 and S658 and S659 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S661 | 116 | S657 and S658 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S666 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S667 | 1162 | S659 and S666 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S674 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S675 | 1427 | S659 and S674 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S676 | 930 | S659 and S674 and S658 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S678 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S680 | 248 | S679 and @ad<"20060320" | US-PGPUB; USPAT; | OR | ON | 2009/06/20 16:22 |

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| | | | USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S683 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S685 | 977 | S683 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S686 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S687 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S688 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S689 | 85 | S686 and S687 and S688 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S690 | 67 | S689 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S693 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |

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| S694 | 977 | S693 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S695 | 567 | S694 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S703 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S704 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S705 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S706 | 85 | S703 and S704 and S705 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S707 | 116 | S703 and S704 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S712 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S713 | 1162 | S705 and S712 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | ON | 2009/06/20 16:22 |

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| | | | DERWENT; IBM_TDB | | | |
| S720 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S721 | 1427 | S705 and S720 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S722 | 930 | S705 and S720 and S704 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S724 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S726 | 248 | S725 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S729 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S731 | 977 | S729 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S734 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S735 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S736 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S737 | 85 | S734 and S735 and S736 | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/20 16:22 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S738 | 116 | S734 and S735 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S743 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S744 | 1162 | S736 and S743 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S751 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S752 | 1427 | S736 and S751 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S753 | 930 | S736 and S751 and S735 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S755 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S757 | 248 | S756 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S760 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S762 | 977 | S760 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S763 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; | OR | ON | 2009/06/20 16:22 |

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| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S764 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S765 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S766 | 85 | S763 and S764 and S765 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S767 | 67 | S766 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S770 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S771 | 977 | S770 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S772 | 567 | S771 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S780 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S781 | 8964 | HEMT or (high near electron near | US-PGPUB; | OR | ON | 2009/06/20 |

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| | | mobility near transistor) | USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | 16:22 |
| S782 | 7165 | HEMT or (high near electron near mobility near transistor) or HFET | US-PGPUB; USPAT | OR | ON | 2010/09/24 16:32 |
| S783 | 816 | S782 and input and (Vdd or power adj supply) and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 16:33 |
| S784 | 593 | S783 and (gate and drain and source) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 16:34 |
| S785 | 79 | S784 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/09/24 16:34 |
| S786 | 79 | S783 and ((gate near4 input) and (drain near4 (Vdd or power adj supply))) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 17:39 |
| S787 | 108 | S782 and ((gate near4 input) and (drain near4 (Vdd or power adj supply))) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 17:46 |
| S788 | 79 | S787 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 17:47 |
| S789 | 37 | ((gate adj voltage) near5 (depletion adj mode)) same ((gate adj voltage) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 17:55 |
| S790 | 2 | 257/192.ccls. and ((gate adj voltage) near5 (depletion adj mode)) and ((gate adj voltage) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 18:03 |
| S791 | 9 | HEMT and ((gate adj voltage) near5 (depletion adj mode)) and ((gate adj | US-PGPUB; USPAT | OR | ON | 2010/09/25 18:04 |

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|---|---|---|---|---|---|---|
| | | voltage) near5 (enhancement adj mode)) and @ad<"20060320" | | | | |
| S792 | 26 | HEMT and ((voltage bias) near5 (depletion adj mode)) and ((voltage bias) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 19:59 |
| S793 | 12 | ((voltage bias) with (depletion adj mode) with ground) same ((gate adj voltage) with (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 20:36 |
| S794 | 484 | ((voltage bias) near5 (depletion adj mode)) and ((voltage bias) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 20:39 |
| S795 | 7 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2011/04/09 01:31 |
| S796 | 0 | 2005/000700 | US-PGPUB; USPAT; USOCR | OR | ON | 2011/04/09 11:35 |
| S797 | 2 | 2005/0007200 | US-PGPUB; USPAT; USOCR | OR | ON | 2011/04/09 11:35 |
| S798 | 0 | 2005/0007200 | US-PGPUB | OR | ON | 2011/04/09 11:36 |
| S799 | 2 | 10/873291 | US-PGPUB; USPAT; USOCR | OR | ON | 2011/04/09 11:37 |
| S800 | 23 | ((voltage bias) with (depletion adj mode) with ground) and ((gate adj voltage) with (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:48 |
| S801 | 6181 | HEMT or (high near electron near mobility near transistor) and ((voltage bias) with (depletion adj mode)) and ((gate adj voltage) with (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:51 |
| S802 | 6180 | HEMT or (high near electron near mobility near transistor) and (((voltage bias) with (depletion adj mode)) with ((gate adj voltage) with (enhancement adj mode))) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:52 |
| S803 | 0 | S802 and merged near cascode | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:54 |
| S804 | 234 | S802 and cascode | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:54 |
| S805 | 11916 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2011/12/13 14:46 |
| S806 | 7652 | S805 | US-PGPUB; USPAT | OR | ON | 2011/12/13 14:46 |
| S807 | 18 | S805 and (filed adj plat$3 with gate) | US-PGPUB; USPAT | OR | ON | 2011/12/13 14:46 |
| S808 | 329 | S805 and (field adj plat$3 with gate) | US-PGPUB; | OR | ON | 2011/12/13 |

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| | | | USPAT | | | 14:46 |
| S809 | 155 | S808 and (@ad<"20060320" or @rlad<"20060320") | US-PGPUB; USPAT | OR | ON | 2011/12/13 14:48 |
| S810 | 4 | "10930160" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2011/12/13 17:00 |
| S811 | 15 | "10/930160" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2011/12/13 17:00 |

**EAST Search History (Interference)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L27 | 0 | ((input near (voltage bias)) and (constant near (voltage bias)) and source and drain and (first adj gate) and (second adj gate) and transistor and (enhancement adj mode or "normally on") and (depletion adj mode "normally off")).clm. | US-PGPUB; USPAT; UPAD | OR | ON | 2012/04/21 21:15 |

**4/ 21/ 2012 9:25:16 PM**
**C:\ Users\ sahmed7\ Documents\ EAST\ Workspaces\ 11688338.wsp**

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11688338 | HERMAN, THOMAS |
| | **Examiner** | **Art Unit** |
| | SELIM AHMED | 2826 |

| ORIGINAL | | INTERNATIONAL CLASSIFICATION | |
|---|---|---|---|
| CLASS | SUBCLASS | CLAIMED | NON-CLAIMED |
| 257 | 194 | H 0 1 L 29 / 66 () | |

| CROSS REFERENCE(S) | | | | | |
|---|---|---|---|---|---|
| CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) | | | | |
| 257 | E29.246 | | | | |

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original |
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| 1 | 1 | | | | | | | | | | | | | | |
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| /SELIM AHMED/<br>Examiner.Art Unit 2826<br><br>(Assistant Examiner) | 4/21/2012<br><br>(Date) | **Total Claims Allowed:**<br>16 | |
| /VICTOR A MANDALA/<br>Primary Examiner.Art Unit 2826<br><br>(Primary Examiner) | 05/02/2012<br><br>(Date) | O.G. Print Claim(s)<br>1 | O.G. Print Figure<br>4 |

OPAP IAP18 APR 23 2012 PATENT & TRADEMARK OFFICE



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | |
|---|---|
| In re Application of: | Art Unit: 2826 |
| **Herman, Thomas** | Examiner: Ahmed, Selim U. |
| Serial No.: **11/688,338** | |
| Filed: **March 20, 2007** | |
| For: **Merged Gate Cascode Transistor** | |

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Respectfully submitted,

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Dated: 4/19/12

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| FORM PTO-1449 LIST OF PATENTS AND OTHER ITEMS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) | ATTY. DOCKET NO. 0400131 | SERIAL NO. 11/688,338 |
|---|---|---|
| | APPLICANTS: Herman, Thomas | |
| | FILING DATE: March 20, 2007 | GROUP ART: 2826 |

| U.S. PATENT DOCUMENTS | | | | | | | |
|---|---|---|---|---|---|---|---|
| Exam. Initials | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
| | AA | | | | | | |

| FOREIGN PATENT DOCUMENT | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Exam. Initials | | DOCUMENT NUMBER | PUBLICATION DATE | COUNTRY OR PATENT OFFICE | CLASS | SUB CLASS | TRANSLATION YES | TRANSLATION NO |
| | BA | JP 2001-210657 | 8/03/01 | JAPAN | | | | |
| | BB | JP 2002-076020 | 3/15/02 | JAPAN | | | | |
| | BC | WO 2005/079370 | 9/01/05 | WIPO | | | | |
| | BD | JP 2008-522436 | 6/26/08 | JAPAN | | | | |

| OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.) | | |
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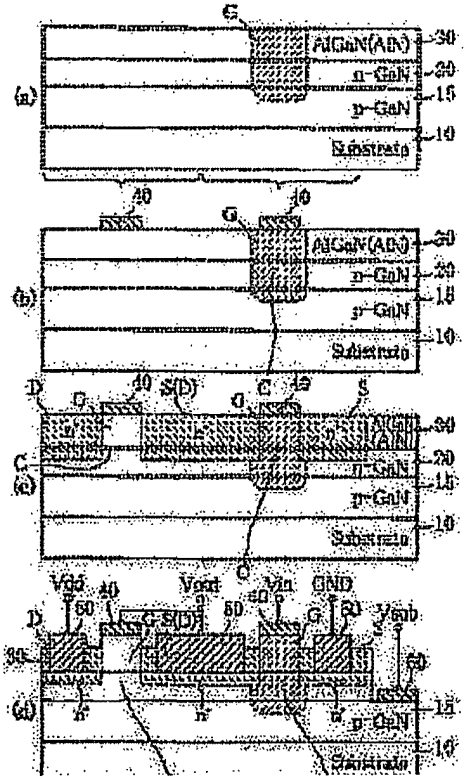
# Bibliographic data: JP2001210657 (A) — 2001-08-03

## SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

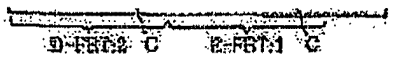
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|---|---|
| **Inventor(s):** | ISHII HIROTATSU ± |
| **Applicant(s):** | FURUKAWA ELECTRIC CO LTD ± |
| **Classification:** - international: | ***H01L21/265; H01L21/338; H01L29/812; H01L29/20;*** (IPC1-7): H01L21/265; H01L21/338; H01L29/812 |
| **Classification:** - European: | |
| **Application number:** | JP20000015878 20000125 |
| **Priority number(s):** | JP20000015878 20000125 |
| **Also published as:** | JP4850993 (B2) |

### Abstract of JP2001210657 (A)

PROBLEM TO BE SOLVED: To provide a field effect transistor of a GaN system, which is superior in an operation characteristic in a high-temperature environment, and to provide a semiconductor device suitable for realizing an inverter circuit and the manufacturing method. SOLUTION: An AlN or AlGaN layer 30 is formed by the heterojunction of them on a GaN layer 20. The prescribed quantity of impurity atoms are ion implanted into a channel region formed in the GaN layer, prior to the formation of a gate electrode 40. The gate electrode is formed on the AlN or AlGaN layer at the upper part of the channel, to which the ions are implanted. A source region S and a drain region a D are formed by making them position on both sides of the channel region. The carriers of high concentration are ion implanted only to one of channel regions in a FET, which



are installed adjacently.; Thus,
depression-type FET and
enhancement-type FET are manufactured simultaneously.




Last updated: 14.03.2012 Worldwide Database 5.7.38; 93p

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報**（Ａ）　(11)特許出願公開番号
特開2001－210657
（P2001－210657A）
(43)公開日　平成13年８月３日(2001.8.3)

| (51)Int.Cl.' | 識別記号 | ＦＩ | | テーマコード'（参考） |
|---|---|---|---|---|
| Ｈ０１Ｌ　21/338 | | Ｈ０１Ｌ　21/265 | ６０４Ｚ | ５Ｆ１０２ |
| 29/812 | | 29/80 | Ｂ | |
| 21/265 | ６０４ | | | |

審査請求　未請求　請求項の数６　ＯＬ　（全７頁）

(21)出願番号　特願2000－15878(P2000－15878)

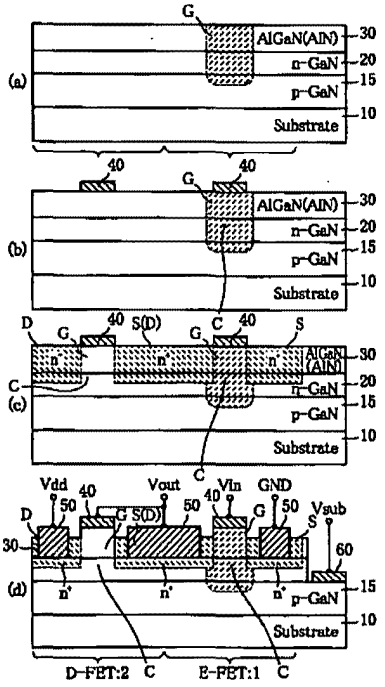
(22)出願日　平成12年１月25日(2000.1.25)

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Ｆターム(参考)　5F102 GA02 GB01 GC01 GD10 GJ02 GJ03 GJ10 GL04 GQ01 HC07

(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】
【課題】　高温環境での動作特性に優れたＧａＮ系の電界効果トランジスタ、更にはインバータ回路を実現するに好適な半導体装置とその製造方法を提供する。
【解決手段】　ＧａＮ層２０上にヘテロ接合させてＡｌＮまたはＡｌＧａＮ層３０を形成した後、ゲート電極４０の形成に先立ってＧａＮ層に形成するチャネル領域に所定量の不純物原子をイオン注入する。しかる後、イオン注入したチャネル領域の上部のＡｌＮまたはＡｌＧａＮ層上にゲート電極を形成し、更にチャネル領域の両側に位置付けてソース領域Ｓおよびドレイン領域Ｄをそれぞれ形成する。特に隣接して設けるＦＥＴの一方のチャネル領域にだけ、予め高濃度のキャリアをイオン注入することで、デプレッション型のＦＥＴとエンハンスメント型のＦＥＴとを同時に製作する。



【特許請求の範囲】
【請求項1】 GaN層上にヘテロ接合したAlNまたはAlGaN層を介してＭＩＳ構造のゲートを形成してなる半導体装置であって、
前記ゲートの直下のチャネル領域は、イオン注入によりキャリア濃度が調整された領域からなることを特徴とする半導体装置。
【請求項2】 GaN層上にヘテロ接合したAlNまたはAlGaN層を介してＭＩＳ構造をなす複数のゲートを隣接させて形成してなる半導体装置であって、
互いに隣接するゲートの一方は、そのゲート直下のチャネル領域がイオン注入によりキャリア濃度が調整された領域からなることを特徴とする半導体装置。
【請求項3】 前記互いに隣接するゲートは、エンハンスメント動作する電界効果トランジスタのゲート、およびデプレッション動作する電界効果トランジスタのゲートからなる請求項2に記載の半導体装置。
【請求項4】 GaN層上にヘテロ接合させてAlNまたはAlGaN層を形成した後、前記GaN層に形成するチャネル領域に所定量の不純物原子をイオン注入し、しかる後、イオン注入したチャネル領域の上部の前記AlNまたはAlGaN層上にゲート電極を形成し、更に前記チャネル領域の両側に位置付けて前記AlNまたはAlGaN層にソース領域およびドレイン領域をそれぞれ形成してなることを特徴とする半導体装置の製造方法。
【請求項5】 GaN層上にヘテロ接合させてAlNまたはAlGaN層を形成した後、前記GaN層に形成する複数のチャネル領域中の互いに隣接するチャネル領域の一方に所定量の不純物原子をイオン注入し、しかる後、前記各チャネル領域の上部の前記AlNまたはAlGaN層上にそれぞれゲート電極を形成すると共に、前記各チャネル領域の両側に位置付けて前記AlNまたはAlGaN層にソース領域およびドレイン領域をそれぞれ形成してなることを特徴とする半導体装置の製造方法。
【請求項6】 前記チャネル領域への所定量の不純物原子のイオン注入は、前記GaN層を形成した基板の温度を４００℃程度、またはそれ以上に加熱して行われることを特徴とする請求項4または5に記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、高温環境での動作特性に優れたGaN系材料からなる半導体装置、特に論理回路素子をなす電界効果トランジスタを実現するに好適な半導体装置およびその製造方法に関する。
【０００２】
【関連する背景技術】デジタル回路技術で用いられる基本論理回路は、一般に入力信号値を反転するインバータ回路により実現され、このインバータ回路を組み合わせることで種々の論理演算回路が構築される。このような基本論理回路（インバータ回路）を構成する論理回路素子は、一般的にはSiを材料とするバイポーラトランジスタや電界効果トランジスタ（ＦＥＴ）からなるが、最近では高速動作可能なGaAsやＩｎＰを材料としたものも注目されている。
【０００３】しかしながらこれらの半導体材料は、そのバンドギャップが１．０～１．５eV程度と小さいために、例えば２００℃を越える温度環境においては真性キャリアが増大し、いわゆる熱暴走が生じると言う不具合がある。これに対してGaNを材料とする半導体装置、例えば電界効果トランジスタ（ＦＥＴ）は、４００℃に近い高温下でも熱暴走を招来することなく動作することが知られている。
【０００４】この種のGaN系のＦＥＴは、例えばｎ型またはアンドープのGaNの上にAlNまたはAlGaN層を成長させたヘテロ構造を有し、AlNまたはAlGaNによるＭＩＳ構造のゲートを設けた素子構造を備える。このGaN系のＦＥＴの動作特性については未だに解明されていない点もあるが、AlN（またはAlGaN）とGaNとの界面にピエゾ分極や自発分極が発生し、高濃度のキャリアが誘起された界面を利用することで高い駆動能力を備えるものと考えられている。
【０００５】尚、AlGaAs／GaAs系のヘテロ接合においては、AlGaAsに対して高濃度のドーピングを行っても、その電子濃度（キャリア面密度）は高々$10^{12}$／$cm^2$のオーダーである。これに対してAlGaN／GaN系のヘテロ接合では、故意にドーピングを行わなくても$10^{13}$／$cm^2$のオーダーの電子濃度が得られる。しかも短ゲート化した場合にはその移動度の差が殆ど問題とならないので、専ら、AlGaN／GaN系材料の電子濃度が大きい分、半導体素子（ＦＥＴ）としての駆動能力が高いと考えられている。
【０００６】
【発明が解決しようとする課題】ところでGaN系のＦＥＴを実現する場合、一般にその動作閾値を制御することが困難であると言う問題がある。例えばAlGaAs／GaAs系のヘテロ接合を利用したＦＥＴにおいては、AlGaAs層の上部をエッチングする等して、ゲートショットキ接合とヘテロ接合界面との距離を調整し、これによって閾値の設定が行われる。しかしながらAlGaN／GaN系のＦＥＴにおいては、AlGaN層のエッチング自体が困難である。仮にプラズマプロセスを利用してAlGaN層をエッチングしても、そのエッチング表面にプラズマダメージが生じ易い。しかもAlGaN層は、その格子整合が大きいことから、通常、２０ｎｍ程度以下の薄い膜として形成されるので、エッチング後の閾値の制御が困難である。
【０００７】これに対してAlGaNよりもプラズマエッチング性の良好なGaN層をAlGaN層の上部に形成しておき、このGaN層にゲートショットキ電極を形成す

ることも考えられている。しかしGaN／AlGaN界面には、AlGaN／GaN界面とは逆向きの分極が生じるので、ゲート電極に印加する電圧によりキャリア濃度を良好に制御することが困難になると言う不具合がある。

【０００８】本発明はこのような事情を考慮してなされたもので、その目的は、高温環境での動作特性に優れたGaN系の電界効果トランジスタ（ＦＥＴ）を実現するに好適で、特にその動作閾値を簡易に、しかも制御性良く最適設定した、或いは最適設定することのできる素子構造の半導体装置およびその製造方法を提供することにある。

【０００９】

【課題を解決するための手段】上述した目的を達成するべく本発明に係る半導体装置は、請求項１に記載するようにGaN層上にヘテロ接合するAlNまたはAlGaN層を成長させてなり、このAlNまたはAlGaN層を介してＭＩＳ構造のゲートを形成してなるものであって、特にゲートの直下に形成されるチャネル領域を、イオン注入によりそのキャリア濃度を調整した領域としたことを特徴としている。

【００１０】また或いは本発明に係る半導体装置は、請求項２に記載するようにGaN層上にヘテロ接合するAlNまたはAlGaN層を成長させてなり、このAlNまたはAlGaN層を介してＭＩＳ構造をなす複数のゲートを隣接させて形成してなるものであって、互いに隣接するゲートの一方の、そのゲート直下に形成されるチャネル領域を、イオン注入によりキャリア濃度を調整した領域としたことを特徴としている。

【００１１】特に好ましくは、請求項３に記載するように前記互いに隣接するゲートは、エンハンスメント動作する電界効果トランジスタのゲート、およびデプレッション動作する電界効果トランジスタのゲートからなり、エンハンスメント型の電界効果トランジスタとデプレッション型の電界効果トランジスタとを隣接して設けることを特徴としている。

【００１２】また本発明に係る半導体装置の製造方法は、請求項４に記載するようにGaN層上にヘテロ接合させてAlNまたはAlGaN層を形成した後、前記GaN層に形成するチャネル領域に所定量の不純物原子をイオン注入してそのキャリア濃度を調整した後、イオン注入したチャネル領域の上部の前記AlNまたはAlGaN層上にゲート電極を形成し、更に前記チャネル領域の両側にソース領域およびドレイン領域をそれぞれ形成することを特徴としている。

【００１３】また或いは本発明に係る半導体装置の製造方法は、請求項５に記載するようにGaN系材料からなる基板上にヘテロ接合させてAlNまたはAlGaN層を形成した後、前記基板に設定する複数のチャネル領域中の互いに隣接するチャネル領域の一方に所定量の不純物原子をイオン注入して該チャネル領域のキャリア濃度を調整した後、前記各チャネル領域の上部の前記AlNまたはAlGaN層上にそれぞれゲート電極を形成すると共に、前記各チャネル領域の両側にソース領域およびドレイン領域をそれぞれ形成することを特徴としている。

【００１４】即ち、本発明に係る半導体装置の製造方法は、AlNまたはAlGaN層上にゲート電極を設けてＭＩＳ構造のゲートを形成するに先立ち、該ゲート直下のチャネル領域に所定量の不純物原子をイオン注入してそのキャリア濃度を調整し、これによって上記ゲートを備えて構成される電界効果トランジスタ（ＦＥＴ）の閾値を最適設定することを特徴としている。尚、キャリア濃度を調整するべくイオン注入する不純物原子の所定量とは、イオン注入を施さない場合にチャネル領域に誘起されているキャリアをほぼ補償する、つまり電気的に相殺するに足るイオン化不純物を発生させる不純物原子量である。

【００１５】具体的にはキャリアが電子である場合にはMgやC等のアクセプタ型の不純物元素を、またキャリアが正孔である場合にはSi等のドナー型不純物元素を、主としてキャリアが発生している領域、即ち、GaN層の上部にピークを有して分布するようにイオン注入する。この際、イオン注入する不純物原子の面密度については該不純物原子の活性化率を考慮し、イオン注入前のキャリア面密度と概略一致するようにする。

【００１６】ちなみにソース領域およびドレイン領域の形成は、前記チャネル領域の両側に位置付けられる領域に誘起されているキャリアの濃度をより高める不純物原子を、つまり上記キャリアが電子の場合にはドナー型の不純物原子を、また上記キャリアが正孔の場合にはアクセプタ型の不純物原子をイオン注入することによって達せられる。

【００１７】但し、不純物原子の活性化率が低い場合、所望とするイオン化不純物量を発生させるためには極めて多量の不純物原子を注入しなければならないことがある。するとイオン注入により導入される結晶欠陥の量が増大し、デバイスの特性が劣化することが懸念される。そこでこのような不具合を回避するべく、請求項６に記載するように基板温度を４００℃程度、或いはそれ以上に加熱した状態で上述したイオン注入を行うようにし、注入不純物原子の活性化率を上昇させるようにすることが望ましい。

【００１８】

【発明の実施の形態】以下、図面を参照して本発明に係る半導体装置およびその製造方法の一実施形態について、エンハンスメント型の電界効果トランジスタ（Ｅ・ＦＥＴ）とデプレッション型の電界効果トランジスタ（Ｄ・ＦＥＴ）とを隣接して設けた素子構造を有し、所謂ＥＤ型インバータ回路を構築した半導体装置を例に説明する。

【００１９】図１はエンハンスメント型の電界効果トラ

ンジスタ（E・FET）1をドライバとし、デプレッション型の電界効果トランジスタ（D・FET）2をその負荷として構成されるインバータ回路の例を示している。このインバータ回路は、ソースを接地したE・FET1のドレインにD・FET2のソースを接続し、D・FET2のドレインを電源電圧Vddに接続すると共に、該D・FET2のゲートにそのドレインと同じ電位を与えるように共通接続することで、D・FET2をE・FET1の負荷とし、E・FET1のゲートに加えられる入力電圧Vinの反転出力Voutをそのドレインから得るように構成される。

【0020】ちなみにエンハンスメント動作するE・FET1の閾値は、例えば0.5Vに設定され、入力電圧Vinが上記閾値を上回ったときにオン（導通）し、上記閾値よりも低いときにはオフ（遮断）する。これに対してデプレッション動作するD・FET2の閾値は、例えば−1.0Vに設定され、そのソース電位に対してマイナスの電位がゲートに加えられない限りオン（導通）状態が保たれる。従ってこのようなE・FET1とD・FET2とを同一基板上に隣接させて形成してインバータ回路を実現する場合、特に前述したように高温環境下における動作特性に優れたGaNを用いてFET1,2を実現する場合、各FET1,2の閾値を如何にして設定（調整）するかが大きな課題となる。

【0021】そこで本発明においては次のようにしてE・FET1とD・FET2とを製作することで各FET1,2の閾値をそれぞれ最適化し、動作特性に優れたインバータ回路を実現するものとなっている。図2は第1の実施形態に係る半導体装置の製造方法の概略的な手順を分解して示している。半導体装置の製造に際しては、先ず、例えばサファイヤ、SiC、SiまたはGaNの単結晶基板（サブストレイト）10上に、アンドープまたはアクセプタ（MgやC等）をドープした半絶縁性またはp型のGaN層15を形成し、このGaN層15上にSi等のドナーをドープしたn型のGaN層20を積層してなり、更にこのGaN層20上にヘテロ接合させてAlGaN層30を積層形成したエピタキシャル層を素子形成材料として準備する。尚、上記AlGaN層30に代えてAlN層を形成したものを用いることも可能である。またAlGaN（AlN）層30の膜厚は、10〜30nm程度に設定される。

【0022】しかしてFETは、基本的には上記AlGaN層30の上にゲート電極（金属電極）40を設けることで、該AlGaN層30を介するMIS構造のゲートを形成することにより実現される。即ち、図2(b)に示すようにFETを形成する領域のAlGaN層30上に金属からなるゲート電極40を形成してMIS構造のゲートGを構成し、その後、図2(c)に示すように上記ゲートGの両側に高濃度のドナーをイオン注入してn+型のソース領域Sとドレイン領域Dとを形成する。次いで図2(d)に示すようにソース領域Sおよびドレイン領域D上にソース電極およびドレイン電極をなすオーミック電極50を形成することでFETが製作される。尚、ソース電極およびドレイン電極をなすオーミック電極50は、ソース領域Sおよびドレイン領域DのAlGaN層30を、アルカリ性のウェットエッチング等を利用してエッチング除去した後に形成される。

【0023】ちなみにこのようにして製作されるFETによれば、ゲート電極40の直下のヘテロ界面には、ゲート電極40に0V（接地電位）を加えた場合であってもキャリア（電子）が蓄積されているので、このFETは常にオン状態をとり、ソース電位に比較してマイナスとなる電位をゲート電極40に加えたときにだけオフ状態となる。従ってデプレッション動作するD型のFETが実現されることになる。

【0024】そこでこの実施形態においてはゲート電極40を形成するに先立ち、図2(a)に示すようにエンハンスメント動作するE・FET1を実現するべく、該E・FET1のゲートGを形成する予定の領域の直下（ゲート直下のチャネル領域C）にアクセプタをイオン注入し、チャネル領域のヘテロ界面に誘起されるキャリア（電子）を打ち消すようにしている。このイオン注入は、ヘテロ界面に誘起されている電子濃度と同量のアクセプタを、AlGaN層30に近いGaN層20の上部にピークを持つように行われる。尚、D・FET2を形成する予定の領域には、アクセプタのイオン注入を行わないことは勿論のことである。

【0025】このようにしてE・FET1のゲート直下に予めアクセプタをイオン注入して当該領域のキャリア濃度を調整した後、前述した図2(b)〜(d)に示す手順に従ってE・FET1およびD・FET2の各ゲート電極40を設け、これらのゲート電極40により形成されるゲートGの両側に高濃度のドナーを注入してn+型のソース領域とSとドレイン領域Dとをそれぞれ形成する。そしてソース領域とSとドレイン領域D上にオーミック電極50を形成することで、E・FET1およびD・FET2がそれぞれ製作される。

【0026】かくして上述した如くゲート直下のチャネル領域Cにアクセプタをイオン注入して製作されるE・FET1によれば、そのヘテロ界面に誘起されていた電子がイオン化アクセプタにより打ち消されるので、ゲート電極40に0V（接地電位）を加えることにより該E・FET1はオフ状態となる。そしてソース電位に比較してプラスとなる電位をゲート電極40に加えると、これによって電子が誘起されて該E・FET1がオン状態となる。従ってエンハンスメント動作するE型のFETが実現されることになる。しかも上述した製作手順に従えば、E・FET1とD・FET2とを隣接させて形成することが可能となる。

【0027】尚、上記E・FET1とD・FET2とを

電気的に接続して図１に示す如きインバータ回路を実現する場合には、図２(d)に示すようにＥ・ＦＥＴ１のドレイン領域ＤとＤ・ＦＥＴ２のソース領域Ｓとを共通に形成し、更にこれらの領域の上に形成されるオーミック電極５０をＤ・ＦＥＴ２のゲート電極４０に電気的に配線接続するようにすれば良い。

【００２８】また実際には図２(d)に示すように、GaN層２０にサブストレイト電極６０を設け、Ｅ・ＦＥＴ１およびＤ・ＦＥＴ２に対して共通にサブストレイト電位Vsubを加えるように構成される。更にインバータ回路としての適切な動作特性を確保する上で、Ｅ・ＦＥＴ１およびＤ・ＦＥＴ２のゲート長やイオン注入濃度等を適切に設定（設計）する必要があることは言うまでもない。

【００２９】ところで上述した第１の実施形態は、ｎ型のGaN層２０をベースとしてＥ・ＦＥＴ１およびＤ・ＦＥＴ２を形成したが、ｐ型のGaN層をベースとしてＥ・ＦＥＴ１およびＤ・ＦＥＴ２を形成するようにしても良い。図３はこのｐ型のGaN層２１をベースとして製作される第２の実施形態を示している。この場合には、サファイア、SiC、SiまたはGaNの単結晶基板（サブストレイト）１０上に、アンドープまたはドナー（Si等）をドープした半絶縁性またはｎ型のGaN層１６を形成し、このGaN層１６上にMgやCをドープしたｐ型のGaN層２１を積層してなり、更にこのGaN層２１上にヘテロ接合させてAlGaN層３０を積層形成したエピタキシャル層を素子形成材料として準備する。そして基本的には先の第１の実施形態と同様にして図３(b)に示すようにゲート電極４０を形成してＭＩＳ構造のゲートＧを形成し、次いで図３(c)に示すようにイオン注入によりソース領域Ｓとドレイン領域Ｄを形成し、その上で図３(d)に示すようにソース領域ＳおよびドレインD上にオーミック電極５０を形成することでＦＥＴが製作される。

【００３０】但し、この場合には、予めGaN層２１に導入されているイオン化アクセプタにより電子が打ち消されるので、ゲート電極４０に電圧を加えない状態においてはゲート直下のヘテロ界面には電子が誘起されることはない。そしてゲート電極４０にプラスの電圧を印加すると、これによってイオン化アクセプタにより打ち消されていた電子が誘起されてＦＥＴがオン動作することになる。即ち、エンハンスメント型のＦＥＴが構成されることになる。

【００３１】そこでこの第２の実施形態においては、ゲート電極４０を形成するに先立ち、図３(a)に示すようにデプレッション動作するＤ・ＦＥＴ２を実現するべく、該Ｄ・ＦＥＴ２のゲートＧを形成する予定の領域の直下（ゲート直下のチャネル領域Ｃ）にドナーをイオン注入し、チャネル領域のヘテロ界面に存在するイオン化アクセプタを打ち消すようにしている。このイオン注入は、イオン化アクセプタの濃度と同量のドナーを、AlGaN層３０に近いGaN層２０の上部にピークを持つように行われる。そしてゲートＧに電圧を加えない状態で、そのヘテロ界面に最初から電子が誘起されているように設定される。尚、Ｅ・ＦＥＴ１を形成する予定の領域には、上述したドナーのイオン注入を行わないことは勿論のことである。

【００３２】このようにしてＤ・ＦＥＴ２のゲートＧを形成する予定の領域の直下に予めドナーをイオン注入し、当該領域におけるイオン化アクセプタを打ち消して電子が誘起されるように設定することで、当該領域に形成されるＦＥＴをデプレッション型のものに変更することが可能となり、先の実施形態と同様にＥ・ＦＥＴ１とＤ・ＦＥＴ２とを隣接して形成することができる等の効果が奏せられる。

【００３３】また上述した第１および第２の実施形態に示したイオン注入は、その注入元素の打ち込み深さや注入量を制御性良く、しかも高精度に制御することができるので、イオン注入の制御によりＦＥＴとしての動作閾値を精度良くコントロールすることができる。従ってエッチングによりゲートＧの厚みを変えてその閾値を調整することに比較して、格段に高い精度で、しかも広範囲に亘ってその閾値を調整することができる。

【００３４】また上述したイオン注入を行うに際して、例えばその基板温度を４００℃程度、或いはそれ以上に加熱して行えば、イオン注入の活性効率が著しく上昇する。但し、このイオン注入はＦＥＴのチャネル領域に対して行われるため、チャネル領域における注入損傷やイオン化不純物量の増加が避けられない。これ故、チャネル長等の構造的（幾何的）条件を同じくして製作されたAlGaAs／GaAs系や、Si-MOS系のＦＥＴに比較して、その動作応答性（動作速度）が劣ることが否めない。

【００３５】しかしながらこれらのＦＥＴに比較してGaN系のＦＥＴによれば、その動作可能温度が圧倒的に高く、例えば４００℃の動作環境においてもインバータ動作が可能なので、動作応答性（動作速度）が劣ることを踏まえても、高温環境下での使用が可能である等の絶大なる効果が発揮される。特にＥ・ＦＥＴ１とＤ・ＦＥＴ２とを隣接して形成して、デジタル処理における基本論理回路であるインバータ回路を容易に構成することができるので、その用途は極めて広い。

【００３６】尚、本発明は上述した実施形態に限定されるものではない。例えばソース領域ＳおよびドレインD領域Ｄを形成する上での高濃度不純物のドーピングは、必要に応じて行うようにすれば良い。またドナーをドーピングすることでチャネル電子密度を高めたり、逆にアクセプタをドーピングすることでチャネル電子密度を低下させるようにしても良い。またこれらのドナーまたはアクセプタのドーピングを、前述したチャネル領域Ｃへの

イオン注入によるドーピング量とバランスさせることで、その動作特性（インバータ特性）の最適化を図るようにすることも可能である。

【００３７】またここではｎチャネル型のＦＥＴを例に説明したが、ｐチャネル型のＦＥＴを製作する場合にも、同様な技術思想を適用することができる。更にはＤＥ型のインバータ回路のみならず、ＥＥ型のインバータ回路を構成する場合でも、チャネル領域にイオン注入するドナー／アクセプタの調整により、その動作閾値を最適化するようにすれば良い。その他、本発明はその要旨を逸脱しない範囲で種々変形して実施することができる。

【００３８】

【発明の効果】以上説明したように本発明によれば、GaN層上にヘテロ接合したAlNまたはAlGaN層を介してＭＩＳ構造のゲートを形成して電界効果トランジスタを製作するに際し、ゲート電極の形成に先立ってゲートの直下のチャネル領域にイオン注入してそのキャリア濃度を調整するので、その閾値を容易に、しかも精度良く調整することができる。この結果、デプレッション動作する電界効果トランジスタまたはエンハンスメント動作する電界効果トランジスタを選択的に、しかも容易に製作することができる。更には高温環境下でデプレッション動作する電界効果トランジスタとエンハンスメント動作する電界効果トランジスタとを隣接させて製作することが可能となる等の実用上多大なる効果が奏せられる。

【図面の簡単な説明】

【図１】デジタル処理における基本論理回路として用いられるインバータ回路の構成例を示す図。

【図２】本発明の第１の実施形態に係る半導体装置（電界効果トランジスタ）と、その製造手順を示す図。

【図３】本発明の第２の実施形態に係る半導体装置（電界効果トランジスタ）と、その製造手順を示す図。

【符号の説明】

１　エンハンスメント型の電界効果トランジスタ（Ｅ・ＦＥＴ）

２　デプレッション型の電界効果トランジスタ（Ｄ・ＦＥＴ）

１０　単結晶基板（サブストレイト）

１５　半絶縁性またはｎ型のGaN層

１６　半絶縁性またはｐ型のGaN層

２０　ｎ型のGaN層

２１　ｐ型のGaN層

３０　AlGaN層（AlN層）

４０　ゲート電極（金属電極）

５０　オーミック電極

６０　サブストレイト電極

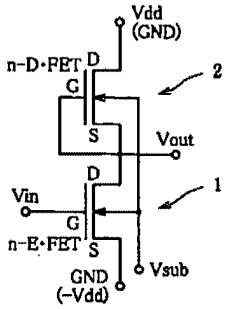
Ｇ　ゲート

Ｓ　ソース領域

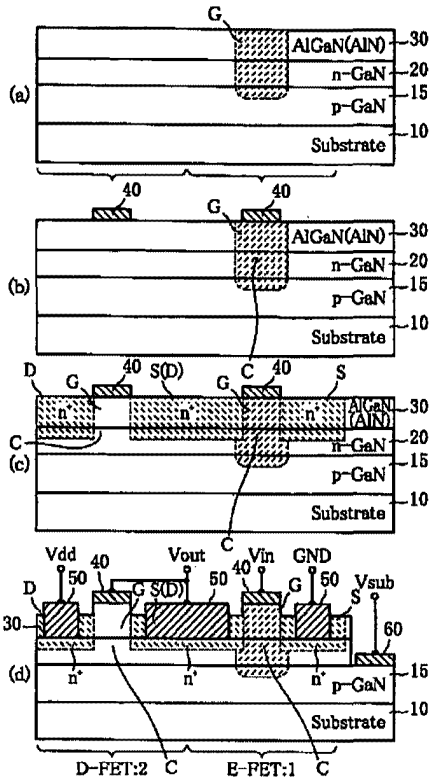
Ｄ　ドレイン領域

Ｃ　チャネル領域

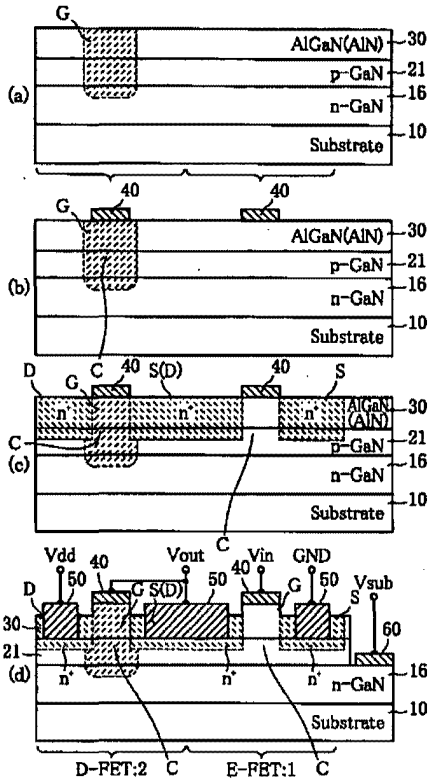
【図１】



【図2】


G
AlGaN(AlN)
n-GaN
p-GaN
Substrate
30
20
15
10
(a)
(b)
(c)
(d)
40
S(D)
C
D
S
n+
Vdd
Vout
Vin
GND
Vsub
50
60
D-FET:2
E-FET:1

【図3】


G
AlGaN(AlN)
p-GaN
n-GaN
Substrate
30
21
16
10
(a)
(b)
(c)
(d)
40
S(D)
C
D
S
n+
Vdd
Vout
Vin
GND
Vsub
50
60
D-FET:2
E-FET:1

Espacenet

# Bibliographic data: JP2002076020 (A) — 2002-03-15

## SEMICONDUCTOR DEVICE

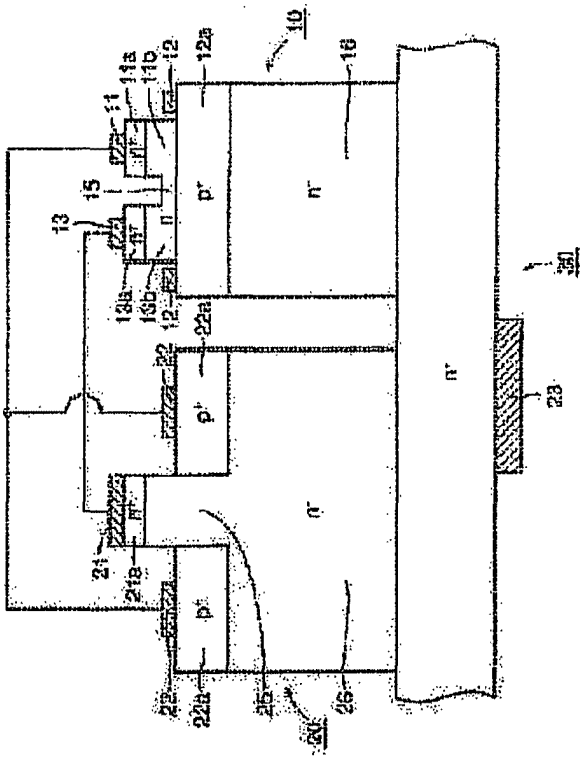

| | | |
|---|---|---|
| **Inventor(s):** | HARADA MAKOTO; HIROTSU KENICHI ± | |
| **Applicant(s):** | SUMITOMO ELECTRIC INDUSTRIES ± | |
| **Classification:** | **- international:** | ***H01L21/337; H01L29/161; H01L29/808;*** (IPC1-7): H01L21/337; H01L29/161; H01L29/808 |
| | **- European:** | |



| | |
|---|---|
| **Application number:** | JP20000262627 20000831 |
| **Priority number(s):** | JP20000262627 20000831 |


### Abstract of JP2002076020 (A)


PROBLEM TO BE SOLVED: To provide a normally-off-type SiC semiconductor device which can be used at a higher operating temperature, has a high switching speed, and makes a space of circuit compact. SOLUTION: A normally-off-type JFET 10 and a normally-on-type JFET 20 are combined with each other, the source electrode 11 of the normally-off-type JFET is connected with the gate electrode 22 of the normally-on-type JFET, and the drain electrode 13 of the normally-off-type JFET is connoted with the source electrode 21 of the normally-on-type JFET.

Last updated: 14.03.2012 Worldwide Database 5.7.38; 93p

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2002－76020
（P2002－76020A）
(43)公開日　平成14年３月15日(2002.3.15)

| (51)Int.Cl.' | 識別記号 | ＦＩ | | テーマコード'(参考) |
|---|---|---|---|---|
| Ｈ０１Ｌ 21/337 | | Ｈ０１Ｌ 29/161 | | ５Ｆ１０２ |
| 29/808 | | | 29/80 | Ｃ |
| 29/161 | | | | |

審査請求　未請求　請求項の数５　ＯＬ　（全６頁）

(21)出願番号　特願2000－262627(P2000－262627)

(22)出願日　平成12年８月31日(2000.8.31)

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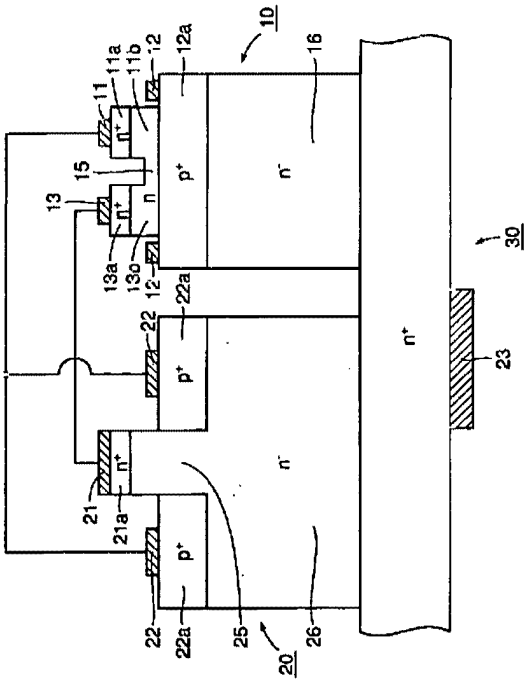
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(54)【発明の名称】　半導体装置

(57)【要約】
【課題】　使用温度を高め、高いスイッチング速度を有し、回路スペースをコンパクトにできる、ノーマリーオフ型のＳｉＣの半導体装置を提供する。
【解決手段】　ノーマリーオフ型のＪＦＥＴ１０とノーマリーオン型のＪＦＥＴ２０とが組み合わされ、ノーマリーオフ型のＪＦＥＴのソース電極１１とノーマリーオン型のＪＦＥＴのゲート電極２２とが接続され、ノーマリーオフ型のＪＦＥＴのドレイン電極１３とノーマリーオン型のＪＦＥＴのソース電極２１とが接続されている。



【特許請求の範囲】
【請求項１】　ノーマリーオフ型の接合型電界効果トランジスター（JFET:Junction Field Effect Transistor）とノーマリーオン型の接合型電界効果トランジスターとが組み合わされた半導体装置であって、
前記ノーマリーオフ型の接合型電界効果トランジスターのソース電極と前記ノーマリーオン型の接合型電界効果トランジスターのゲート電極とが接続され、
前記ノーマリーオフ型の接合型電界効果トランジスターのドレイン電極と前記ノーマリーオン型の接合型電界効果トランジスターのソース電極とが接続された、半導体装置。
【請求項２】　前記ノーマリーオフ型の接合型電界効果トランジスターでは、チャネル領域とゲート領域との間の接合面において、拡散電位によって空乏層が形成され、当該空乏層がチャネル領域を遮断している、請求項１に記載の半導体装置。
【請求項３】　前記ノーマリーオフ型の接合型電界効果トランジスターおよびノーマリーオン型の接合型電界効果トランジスターは、ともに同じ基板上に配置されている、請求項１または２に記載の半導体装置。
【請求項４】　前記ノーマリーオフ型の接合型電界効果トランジスターが横型接合型電界効果トランジスターである、請求項１～３のいずれかに記載の半導体装置。
【請求項５】　前記ノーマリーオン型の接合型電界効果トランジスターが縦型接合型電界効果トランジスターである、請求項１～３のいずれかに記載の半導体装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置に関し、より具体的には、複数のＳｉＣ接合型電界効果トランジスタ（JFET:Junction Field Effect Transistor）を組み合わせて、ノーマリーオフ動作を可能とする半導体装置に関するものである。
【０００２】
【従来の技術】ＳｉＣのＪＦＥＴは、耐圧が高くスイッチング速度が速く、使用できる温度も高温まで可能なので、大電力用スイッチング素子として使用が増大している。一般に、ＪＦＥＴでは、オンオフ動作は、チャネル領域を遮断する空乏層の除去と形成とによって行われる。
【０００３】チャネル領域をキャリアが通過している状態であるオン状態は、ゲート電位をソース電位（通常、接地電位）に対してゼロまたはわずかにプラス電位を印加したときに、実現される構造とするほうが製造しやすい。ゲートにゼロまたはわずかにプラスの電位を与え、空乏層によるチャネル領域の遮断を実現するためには、チャネル領域の厚さを薄くしたり、ゲート領域の不純物濃度を非常に高めたりするなど、製造工程における困難度が増大する。このため、大電力のスイッチングに用いるＪＦＥＴは、通常、ノーマリーオンの動作を行うことを想定した構造とされている。
【０００４】
【発明が解決しようとする課題】しかしながら、ノーマリーオン型のＪＦＥＴを、例えば回転機制御等に用いる場合、ゲート回路構成が複雑になる。すなわち、ノーマリーオン型のＪＦＥＴでは、ゲートに電圧を加えていないときにオン状態になるので、ゲート回路が故障した場合、回転機は回転したままとなり危険である。このため、故障に備えて、ゲート回路に故障の際にオフさせるための機構を設ける必要がある。また、オフ状態で電圧を印加しつづける必要があるので、オフの期間に、電力消費が生じるという問題がある。
【０００５】これを解決するため、図４に示すように、ノーマリーオン型のＳｉＣ ＪＦＥＴ１２０と、ノーマリーオフ型のＳｉ ＭＯＳＦＥＴ(Metal Oxide Semiconductor Field Effect Transistor)１００とを組み合わせて、ノーマリーオフ型の半導体装置を形成する提案がなされた（H.Mitlehner et al: Dynamic characteristics of high voltage 4H-SiC vertical JFETs, 1999 IEEE）。この半導体装置では、縦型ＪＦＥＴ１２０のソース１２１にＭＯＳＦＥＴ１００のドレイン１０３を接続するとともに、ＭＯＳＦＥＴのソース１０１とＪＦＥＴのゲート１２２とを接続する。この構成によれば、ＭＯＳＦＥＴのゲートに信号が入力されない限り、ＪＦＥＴがオン状態にならないので、ノーマリーオフ型となる。
【０００６】しかしながら、上記のＳｉ ＭＯＳＦＥＴとＳｉＣ ＪＦＥＴとを組み合わせた半導体装置は、次の問題を有している。
（１）　使用可能な温度範囲が狭い。Ｓｉ ＭＯＳＦＥＴの上限温度は１５０℃程度であり、上記半導体装置は１５０℃を超えて使用することができない。
（２）　ＳｉＣ ＪＦＥＴの良好なスイッチング特性を生かすことができない。すなわち、ＳｉＣ ＪＦＥＴに比べてＳｉ ＭＯＳＦＥＴのほうが、スイッチング速度が遅く、２つを接続した場合、遅いほうの素子によりスイッチング速度が律速される。
（３）　回路スペースが大きい。ＪＦＥＴとＭＯＳＦＥＴとを、別々の材料で作製するため、１つの基板上で形成することは困難となる。このため、２つの基板に形成された端子電極を配線で接続しなければならず、回路スペースが大きくなる。
【０００７】上記の（１）、（２）、（３）の問題を解決したノーマリーオフ型のＳｉＣＪＦＥＴを提供することができれば、各種回転機の制御に非常に有用になる。また、電力用パワーデバイスに用いて、オフ時に電力消費を発生させないようにすることができる。さらに、高温環境下で使用可能、または冷却設備の簡素化という効果を得ることができる。
【０００８】そこで、本発明は、使用可能温度を高め、

ＳｉＣの良好なスイッチング速度を利用でき、回路スペースをコンパクトにすることができる、ノーマリーオフ型のＳｉＣの半導体装置を提供することを目的とする。

【０００９】

【課題を解決するための手段】本発明の半導体装置は、ノーマリーオフ型のＪＦＥＴとノーマリーオン型のＪＦＥＴとが組み合わされた半導体装置である。この半導体装置では、ノーマリーオフ型のＪＦＥＴのソース電極とノーマリーオン型のＪＦＥＴのゲート電極とが接続され、ノーマリーオフ型のＪＦＥＴのドレイン電極とノーマリーオン型のＪＦＥＴのソース電極とが接続されている（請求項１）。

【００１０】上記構成によれば、ノーマリーオン型ＪＦＥＴのドレインを当該半導体装置のドレインとし、ノーマリーオフ型ＪＦＥＴのゲートを当該半導体装置のゲートとし、ノーマリーオフ型ＪＦＥＴのソースを当該半導体装置のソースとする。ノーマリーオフ型ＪＦＥＴがオフ状態のとき、そのＪＦＥＴのチャネルは遮断されているので、そのＪＦＥＴのドレインをキャリアが移動することはない。したがって、ノーマリーオン型ＪＦＥＴのソースをキャリアが移動することがないので、ノーマリーオン型ＪＦＥＴがオン状態になることはない。このとき、ノーマリーオフ型ＪＦＥＴのソースードレイン間電圧により、ノーマリーオン型ＪＦＥＴのチャネルは空乏化している。

【００１１】一方、ノーマリーオフ型ＪＦＥＴがオン状態のとき、キャリアがそのＪＦＥＴのドレインを通過し、したがって、ノーマリーオン型ＪＦＥＴのソースをキャリアが通過する。ノーマリーオン型のゲートはノーマリーオフ型ＪＦＥＴのソースと導通しているので、例えば接地電位とすれば、ノーマリーオン型ＪＦＥＴでは、オン状態が実現される。

【００１２】上記の動作は、上記２つのＪＦＥＴを組み合わせた半導体装置が、ノーマリーオフの動作をすることを示している。したがって、回転機制御にコンパクトな回路構造で用いることができ、パワーデバイスに用いた場合、オフ時に電力消費が発生することがなくなる。また、上記のＪＦＥＴは2つともＳｉＣで形成することができるので、使用温度を高くすることができ、大きなスイッチング速度を確保することができ、さらに同じ共通のＳｉＣ基板に小型化して形成することができる。さらに、上記ノーマリーオン型ＪＦＥＴの耐圧を高め、ノーマリーオフ型ＪＦＥＴにオン抵抗の低い構造、例えば、横型ＪＦＥＴでチャネル長の短いものを用いることにより、高耐圧低オン抵抗のＪＦＥＴを得ることができる。

【００１３】上記本発明の半導体装置では、ノーマリーオフ型のＪＦＥＴでは、チャネル領域とゲート領域との間の接合面において、拡散電位によって空乏層が形成され、当該空乏層がチャネル領域を遮断している（請求項２）。

【００１４】上記構成により、ノーマリーオフ型のＳｉＣ ＪＦＥＴを形成することができる。このノーマリーオフ型のＳｉＣ ＪＦＥＴを形成するには、チャネル領域の厚みを薄くし、チャネル領域に接して接合面を形成するゲート領域の不純物濃度をチャネル領域の不純物濃度に比して、非常に高濃度にする。これらの構造により、ゲート領域とチャネル領域との接合面には、拡散電位により空乏層が形成され、ゲートに電圧を印加しなくてもチャネル領域を遮断してオフ状態が実現する。すなわち、ノーマリーオフ型ＪＦＥＴが形成される。このノーマリーオフ型ＪＦＥＴは、オン抵抗を低くすることにより、半導体装置全体のオン抵抗を低下することができる。また、ノーマリーオン型の耐圧は容易に高くすることができるので、ノーマリーオフ型の耐圧は大きくなくても、半導体装置としては大きな耐圧を有することができる。

【００１５】上記本発明の半導体装置では、ノーマリーオフ型のＪＦＥＴおよびノーマリーオン型のＪＦＥＴは、ともに同じ基板上に配置されている（請求項３）。

【００１６】この結果、半導体装置をコンパクトに構成することができる。また、製造工程の成膜工程等を両方のＪＦＥＴに共通の１工程で行うことができる場合が多いので、製造工程の省略、製造期間の短縮等をすることができる。

【００１７】上記本発明の半導体装置では、ノーマリーオフ型のＪＦＥＴが横型ＪＦＥＴである（請求項４）。

【００１８】横型ＪＦＥＴは、チャネル長を短くすることにより、オン抵抗を減少させることができる。また、耐圧はそれほど高くすることができないので、耐圧をノーマリーオン型ＪＦＥＴに負担させて、低オン抵抗で高耐圧の半導体装置を形成することが可能となる。

【００１９】上記本発明の半導体装置では、ノーマリーオン型のＪＦＥＴが縦型ＪＦＥＴである（請求項５）。

【００２０】縦型ＪＦＥＴは、ソースとドレインとが同一面にないので、高耐圧とすることができ、沿面放電を防止することができる。また、低オン抵抗のノーマリーオフ型の横型ＪＦＥＴと組み合わせて高耐圧、低オン抵抗の半導体装置を形成することが可能となる。

【００２１】

【発明の実施の形態】次に図面を用いて、本発明の実施の形態について説明する。図１は、本発明の実施の形態における半導体装置の断面図である。同図において、ＳｉＣのノーマリーオフ型のＪＦＥＴ１０とＳｉＣのノーマリーオン型のＪＦＥＴ２０とが組み合わされている。ノーマリーオフ型のＳｉＣのＪＦＥＴ１０のソース１１とノマリーオン型のＳｉＣのＪＦＥＴ２０のゲート２２とが接続され、また同じくＪＦＥＴ１０のドレイン１３とＪＦＥＴ２０のソース２１とが接続されている。

【００２２】図２は、図１に示した回路構成を１つのＳ

ｉＣ基板に形成した具体例を示す図である。ｎ+型ＳｉＣ基板１の上に、ＳｉＣのノーマリーオフ型のＪＦＥＴ１０とＳｉＣのノーマリーオン型のＪＦＥＴ２０とが形成されている。

【００２３】まず、ＳｉＣのノーマリーオフ型のＪＦＥＴ１０について説明する。このＪＦＥＴ１０は横型であり、キャリアである電子は、チャネル領域１５を基板面に平行に駆動される。ｎ+型ＳｉＣ基板１の上にキャリアの通過を阻止する低濃度のｎ型不純物を含むｎ-ＳｉＣエピタキシャル膜１６が形成され、その上にチャネル領域１５とｎｐ+接合面を形成するゲート領域１２ａが形成される。このゲート領域１２ａの両端上にゲート電極１２が設けられる。このゲート領域１２ａの上には、チャネル領域１５と、そのチャネル領域１５を間にはさんでソース領域１１ｂ、ドレイン領域１３ｂが配置される。これらソース領域１１ｂ、ドレイン領域１３ｂの上には、オーミック接触を実現するための高濃度不純物領域であるソース電極下部１１ａ、ドレイン電極下部１３ａが形成され、その上にソース電極１１、ドレイン電極１３が形成されている。

【００２４】このＳｉＣのノーマリーオフ型のＪＦＥＴ１０においては、ゲート電極１２がゼロ電位であっても、拡散電位によりゲート領域１２ａとのｎｐ+接合面からチャネル領域に向けて空乏層が延びて、チャネル領域を遮断している。このため、ノーマリーオフの動作を行うことができる。すなわち、ゲートがゼロ電位のときオフ状態であり、ゲートが所定のプラス電位になってオン状態が実現する。

【００２５】次に、ＳｉＣのノーマリーオン型のＪＦＥＴ２０について説明する。このＪＦＥＴ２０は縦型であり、キャリアである電子は基板面に交差する厚み方向に駆動される。この縦型ＪＦＥＴのドレイン電極２３は、ＳｉＣ基板の裏面に形成されている。ＳｉＣ基板１の上には低濃度不純物領域であるｎ-ＳｉＣエピタキシャル膜２６が形成され、その上端面の中央がチャネル領域２５に連続している。チャネル領域２５の両側にはゲート領域２２ａが配置され、その上にゲート電極２２が設けられている。また、チャネル領域２５の上には、オーミック接触を実現する高濃度のｎ型不純物を含むソース領域２１ａが設けられ、ソース電極２１と接続している。

【００２６】このノーマリーオンの縦型ＪＦＥＴ２０では、ゲート電圧がゼロ電位のとき、チャネル領域２５を遮断する空乏層は形成されないので、電子はソース領域２１ａからドレインに向かって駆動され、オン状態となる。オフ状態にするには、ゲート領域２２ａとチャネル領域２５との接合面に逆バイアス電圧を印加して空乏層をチャネル領域に延ばして遮断する。

【００２７】配線は、横型ＪＦＥＴ１０のソース電極１１と縦型ＪＦＥＴ２０のゲート電極２２とが、また、横型ＪＦＥＴ１０のドレイン電極１３と縦型ＪＦＥＴ２０のソース電極２１とが、それぞれ接続されている。

【００２８】上記の半導体装置３０は、そのゲート電極として横型ＪＦＥＴ１０のゲート電極１２を有し、そのソース電極として横型ＪＦＥＴ１０のソース電極１１を有し、そのドレイン電極として縦型ＪＦＥＴ２０のドレイン電極２３を有しているとみることができる。横型ＪＦＥＴのチャネル１５はゲート電極１２に所定のプラス電位を印加しないとオン状態にならない。このため、ゲート電位がゼロの状態では、ドレイン電極１３を通って、縦型ＪＦＥＴのソース領域２１ａに電子が流れ込まないので、ソース領域２１ａからドレイン電極２３に電子が流れない。したがって、この半導体装置３０は、ゲート電極１２の電位がゼロの場合、ドレイン電極に流れ込む電子はない。このとき、ノーマリーオフ型ＪＦＥＴのソース－ドレイン間電圧によりノーマリーオン型ＪＦＥＴのチャネルは空乏化している。

【００２９】一方、ゲート電極１２ｂに所定のプラス電位を印加した場合、チャネル領域１５を経由してソース領域１１ｂからドレイン領域へ電子が駆動される。この駆動された電子は配線を通って、縦型ＪＦＥＴ２０のソース電極２１に流れ込む。、縦型ＪＦＥＴ２０のゲート電極は横型ＪＦＥＴ１０のソース電極１１に接続しており、マイナス電位になっていない。そこで、上記電子の流れは、チャネル領域２５、ドリフト領域２６およびＳｉＣ基板１を経由してドレイン電極２３に流れる。

【００３０】上記の半導体装置３０の動作は、まさにノーマリーオフの動作であり、上記の構成により、ノーマリーオフ動作を実現できるようになった。

【００３１】この半導体装置は、ＳｉＣのみによって構成される。図３に示すように、ＳｉＣのイントリンシックな電子濃度の温度依存性によれば、１１００Ｋでも電子濃度は、$1\times10^{12}cm^{-3}$と低い値にとどまっている。このため、使用可能な温度も８００℃程度くらいまで上げることができる。

【００３２】また、上記の半導体装置では、半導体装置のゲート電極によるスイッチング動作は、ＳｉＣの横型ＪＦＥＴ１０のゲート電極によって行われる。図４に示した従来の半導体装置におけるＳｉのＭＯＳＦＥＴでは、スイッチングに要する時間は１００ｎｓ程度であったが、上記ノマリーオフ型ＪＦＥＴをＳｉＣによって構成することにより、スイッチング時間を１ｎｓ以下にすることができる。このスイッチング速度の向上は、実に１００倍以上に達するものである。

【００３３】さらに、図２に示すように、１つのＳｉＣ基板の上に、ノーマリーオフ型のＪＦＥＴとノーマリーオン型のＪＦＥＴとが形成されるので、半導体装置をコンパクトに形成することができ、小型化することができる。

【００３４】また、上記の縦型ＪＦＥＴ２０の耐圧は、例えば、５００Ｖ程度であり、横型ＪＦＥＴ１０の耐圧

は５０Ｖ程度あるので、この半導体装置は高い耐圧を得ることができる。また、縦型ＪＦＥＴのオン抵抗は、上記ノーマリーオン型の場合を、１とすれば、ノーマリーオフ型の場合、１０程度となる。また、横型ＪＦＥＴのオン抵抗は、上記ノーマリーオフ型の場合であっても、チャネル長さを短くすることにより、０．１程度にすることができる。このため、縦型のノーマリーオフ型ＪＦＥＴのみを用いるより、縦型のノーマリーオン型ＪＦＥＴと横型のノーマリーオフ型ＪＦＥＴとを組み合わせた本発明の半導体装置のほうが、高耐圧で、低オン抵抗を容易に実現することができる。

【００３５】上記において、本発明の実施の形態について説明を行ったが、上記に開示された本発明の実施の形態は、あくまで例示であって、本発明の範囲はこれら発明の実施の形態に限定されない。本発明の範囲は、特許請求の範囲の記載によって示され、さらに特許請求の範囲の記載と均等の意味および範囲内でのすべての変更を含むものである。

【００３６】

【発明の効果】本発明により、高温使用でき、スイッチング速度が速く、回路スペースを小さくできる、高耐圧で、低オン抵抗のＳｉＣのＪＦＥＴを得ることができる。

【図面の簡単な説明】

【図１】　本発明の実施の形態における半導体装置の回路図である。

【図２】　図１の回路を１つのＳｉＣ基板に具体的に形成した構造を示す断面図である。

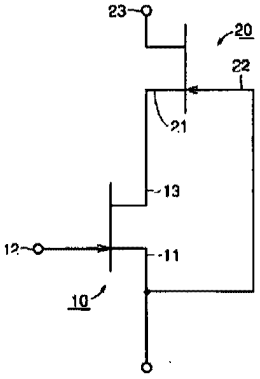
【図３】　ＳｉＣのイントリンシックな電子濃度の温度依存性を示す図である。

【図４】　従来のノーマリーオフ型の半導体装置を示す回路図である。

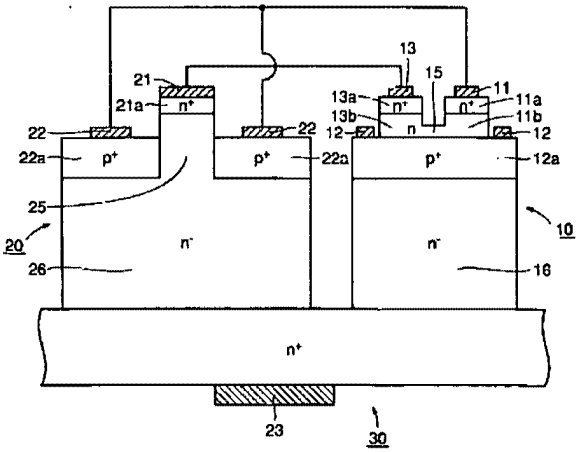
【符号の説明】

１　ｎ+ＳｉＣ基板、１０　ノーマリーオフ型ＪＦＥＴ、１１　ソース電極、１１ａ　ソース電極下部、１１ｂ　ソース領域、１２　ゲート電極、１２ａ　ゲート領域、１３　ドレイン電極、１３ａ　ドレイン電極下部、１３ｂ　ドレイン領域、１５　チャネル領域、１６　抵抗層、２０　ノーマリーオン型ＪＦＥＴ、２１　チャネル電極、２１ａ　チャネル領域、２２　ゲート電極、２２ａ　ゲート領域、２３　ドレイン電極、２５　チャネル領域、２６　ドリフト領域、３０半導体装置。

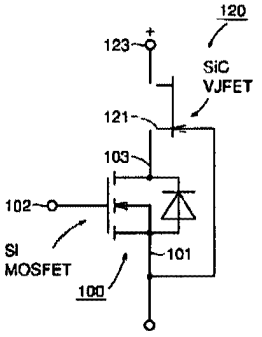
【図１】



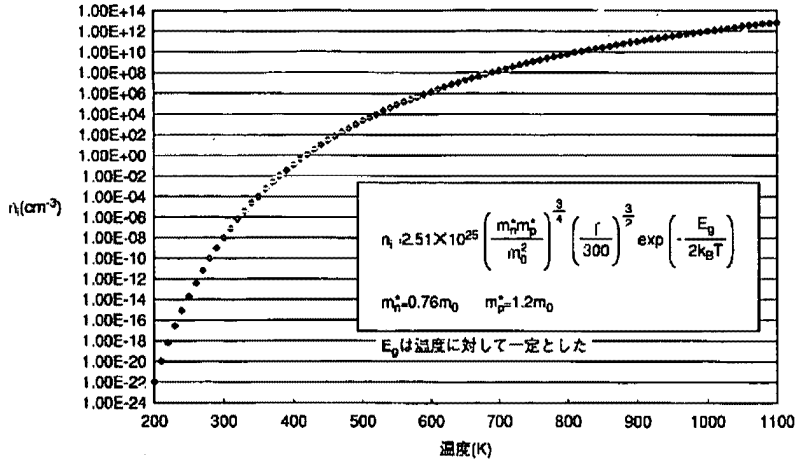

【図２】




【図４】



【図3】




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フロントページの続き

Fターム(参考) 5F102 FA00 FA01 FA04 GA01 GA02
GB01 GB02 GC01 GC07 GD04
GJ02 GL02 GM02 GN02 GR04
GS03 HC01

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 September 2005 (01.09.2005)

PCT

(10) International Publication Number
WO 2005/079370 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2005/004615

(22) International Filing Date: 14 February 2005 (14.02.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/544,626 12 February 2004 (12.02.2004) US
11/056,062 11 February 2005 (11.02.2005) US

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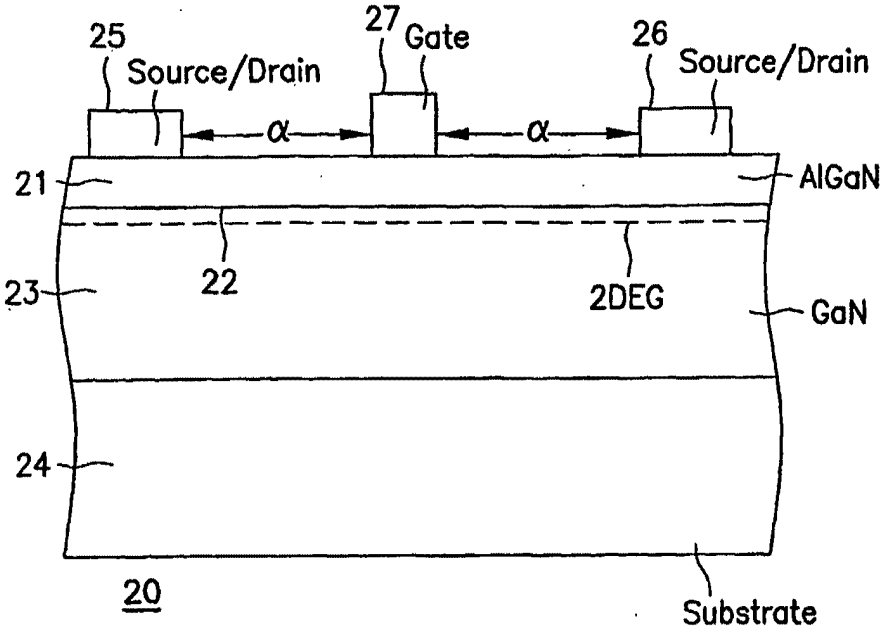
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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

*[Continued on next page]*

(54) Title: III-NITRIDE BIDIRECTIONAL SWITCH




(57) Abstract: A III-nitride bidirectional switch which includes an AlGaN/GaN interface that obtains a high current currying channel. The bidirectional switch operates with at least one gate that prevents or permits the establishment of a two dimensional electron gas to form the current carrying channel for the bidirectional switch.

WO 2005/079370 A2

**Published:**
— *without international search report and to be republished upon receipt of that report*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# III-NITRIDE BIDIRECTIONAL SWITCH

## CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application is based on and claims benefit of U.S. Provisional Application No. 60/544,626 filed February 12, 2004, entitled III-NITRIDE BIDIRECTIONAL SWITCH, to which a claim of priority is hereby made and the disclosure of which is hereby incorporated by this reference.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

[0002] The present invention relates generally to semiconductor switches, and relates more particularly to bidirectional semiconductor switches produced in a III-Nitride material system.

### 2. Description of Related Art

[0003] Development of devices based on III-nitride materials has generally been aimed at high power-high frequency applications such as emitters for cell phone base stations. The devices fabricated for these types of applications are based on general device structures that exhibit high electron mobility and are referred to variously as heterojunction field effect transistors (HFETs), high electron mobility transistors (HEMTs) or modulation doped field effect transistors (MODFETs). These types of devices are typically able to withstand high voltages in the range of 100 Volts or higher, while operating at high frequencies, typically in the range of 2-100 GHz. These types of devices may be modified for a number of types of applications, but typically operate

through the use of piezoelectric polarization to generate a two dimensional electron gas (2DEG) that allows transport of very high currents with very low resistive losses. A typical HEMT includes a substrate, which is formed from sapphire, silicon, or SiC, a GaN layer formed over the substrate, an AlGaN layer formed over the GaN layer, two spaced ohmic electrodes and a gate electrode formed therebetween on the AlGaN layer. Thus, a typical HEMT is a planar device meaning that current between its two power electrodes travels in a lateral direction.

[0004] The specific on resistance of a planar HEMT that exhibits, for example, a 300V breakdown voltage is approximately 1/100 that of a silicon-based device with a vertical geometry of the same voltage rating. Thus, a planar HEMT is a good candidate for power applications. However, these conventional devices block voltage only in one direction.

[0005] Due to a strong need for more efficient circuit topologies in applications such as PDP and PFC, it is desirable to have a bidirectional semiconductor device that is capable of high current, low on resistance and high voltage applications in order to reduce the number of devices.

## SUMMARY OF THE INVENTION

[0006] A semiconductor switch according to the present invention is bidirectional and thus blocks voltage in both directions. This symmetry with respect to voltage blocking capability is achieved without sacrificing wafer material and, therefore, allows for cost reduction as well.

[0007] Furthermore, in contrast to conventional designs that block voltage in one direction, a bidirectional switch according to the present invention can replace four unidirectional switches for the same overall resistance.

[0008] A bidirectional semiconductor switch according to one variation of the present invention includes two ohmic electrodes and a gate electrode so positioned between the

two ohmic electrodes in order to achieve a symmetric voltage blocking capability. Thus, in one preferred embodiment the gate electrode is formed in a position that is equally spaced from the first ohmic electrode and the second ohmic electrode.

[0009] In another variation, a bidirectional switch according to the present invention includes two gate electrodes disposed between two ohmic electrodes. In this embodiment, each gate electrode is spaced from a respective ohmic electrode by the same distance. The use of two gate electrodes is advantageous in that it allows the voltage standoff region to be shared, thereby allowing for the reduction of the wafer area required for the transistor.

[0010] Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 is a III-nitride nominally on bi-directional switch element in accordance with the present invention.

[0012] Figure 2 is a nominally off III-nitride bi-directional switch element in accordance with the present invention.

[0013] Figure 3 is a dual gated nominally on III-nitride bi-directional switch element in accordance with the present invention.

[0014] Figure 4 is a dual gated nominally off III-nitride bi-directional switch element in accordance with the present invention.

[0015] Figure 5 is a plan view of a single gated bi-directional switch in accordance with the present invention.

[0016] Figure 6 is a plan view of a dual gated bi-directional switch in accordance with the present invention.

[0017] Figure 7 is a plan view of a dual gated bi-directional switch structure in accordance with the present invention.

[0018] Figure 8 is a plan view of a gate structure for a bi-directional switch in accordance with the present invention.

[0019] Figures 9-18 illustrate a process for fabricating a device according to the present invention.

[0020] Figure 19 is a top plan view of a variation of a dual gated bidirectional device according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] Referring now to Figure 1, a bi-directional III-nitride switch according to the first embodiment of the present invention is illustrated generally as a device structure 20. Device 20 includes substrate 24, which may be composed of Si, SiC, Sapphire, or the like, a first semiconductor body 23 formed over substrate 24 comprised of one III-nitride material, and a second semiconductor body 21 formed over first semiconductor body 23 and composed of another III-nitride semiconductor material having a band gap that is different from the one semiconductor material. It should be noted that first semiconductor body 23 need not be directly formed over substrate 24, but that a bottom layer may be interposed therebetween without deviating from the present invention. In the preferred embodiment, the one III-nitride semiconductor material is GaN and the another semiconductor material is AlGaN. As is known, the heterojunction 22 of GaN and AlGaN produces a highly conductive two-dimensional electron gas (2DEG) at or near heterojunction 22. The 2DEG is formed due to the spontaneous polarization effect as is known in the field.

[0022] Device 20 further includes ohmic power electrodes 25, 26 which are ohmically connected to second semiconductor body 21, and gate electrode 27 which is disposed between ohmic electrodes 25, 26. Ohmic electrodes may be formed from any suitable metal such as gold, silver, aluminum, titanium, or indium, any suitable metal stack of different metals, or non-metallic material such as a heavily doped semiconductor (P or N type) polysilicon or metal silicides.

[0023] In the preferred embodiment, gate electrode 27 makes a schottky contact with second semiconductor body 21, and may be composed of metallic material such as titanium, gold, aluminum, silver, chromium, tungsten, platinum, nickel, palladium, or indium, a metallic stack of different metals, or a non-metallic material such as a doped semiconductor (P or N type depending on the desired threshold voltage), polysilicon, or metal silicide. A device according to the present invention is not limited to a schottky gate, but may include instead a gate which is comprised of a gate electrode, and a gate insulator such as SiN, $Al_2O_3$, Si02 or the like interposed between the gate electrode and second semiconductor body 21.

[0024] Device 20 according to the first embodiment is a depletion mode device, i.e., a device that is nominally on. The application of a suitable voltage to gate electrode 27 acts to interrupt the 2DEG to turn device 20 off giving device 20 its power switching capability.

[0025] According to the present invention, gate electrode 27 is disposed between ohmic electrodes 25, 26 and positioned such that device exhibits a symmetric voltage blocking capability. That is, device 20 is capable of blocking the same voltage regardless of which ohmic electrode 25, 26 is at a higher potential.

[0026] According to an aspect of the present invention, to achieve a symmetric voltage blocking capability, gate electrode 27 is spaced an equal distance $\alpha$ from ohmic electrode 25 and ohmic electrode 26 (i.e. in a central position with respect to ohmic electrodes 25, 26). It should, however, be noted that gate electrode 27 need not be

centrally located, but can be offset from the center position to compensate for spurious fields from substrate 24, and still achieve the symmetric voltage blocking capability that is desired.

**[0027]** Device 20 is capable of carrying large amounts of current from/to ohmic electrodes 25, 26 due to the 2DEG near heterojunction 22. Typically, the electrical potential applied to gate electrode 27 will be a negative potential that is more negative than any potential applied to ohmic electrodes 25, 26. It should be noted that due to its symmetric voltage blocking capability, either ohmic electrode 25, 26 can serve as a drain or a source.

**[0028]** Referring now to Figure 2, in which like numerals identify like features, device 30 according to the present invention includes all of the features of device 20 according to the first embodiment except that gate electrode 27 in device 30 is disposed within recess 38 formed in second semiconductor layer 21. As a result, device 30, according to the second embodiment of the present invention is an enhancement mode device; i.e., it is a nominally off device. Specifically, recess 38 causes an interruption in the 2DEG, which can be restored upon application of an appropriate voltage to gate electrode 27. The principles of the operation of an enhancement mode device in a III-nitride heterojunction device is explained in U.S. Application No. 11/040,657, entitled Enhancement Mode III-Nitride FET, filed on January 21, 2005, in the name of Robert Beach, and assigned to the assignee of the present application, the contents of which are incorporated by reference.

**[0029]** Gate electrode 27 in device 30 preferably makes schottky contact to second semiconductor layer 21 at the bottom of recess 38. Gate electrode 27, however, may be replaced with a gate conductor and a gate insulator disposed between gate conductor and second semiconductor body 21 without deviating from the present invention. Furthermore, according to the present invention gate electrode 27 in device 30 is positioned in order to achieve symmetry in voltage blocking capability. In the preferred embodiment, gate electrode 27 in device 30 is spaced an equal distance $\alpha$ from ohmic

electrode 25 and ohmic electrode 26, i.e. centrally located with respect to the two ohmic electrodes, in order to achieve symmetry.

[0030] Referring now to Figure 3, in which like numerals identify like features, device 40 according to the third embodiment of the present invention includes two gate electrodes, first gate electrode 32 and second gate electrode 34. First gate electrode 32 is nearest to first ohmic electrode 25 and spaced from the same by a distance $\beta$. Second gate electrode 34 is nearest second ohmic electrode 26 and spaced from the same by a distance $\beta$ as well. That is, first gate electrode 32 is spaced the same distance from first ohmic electrode 25 as second gate electrode 34 is from second ohmic electrode 26.

[0031] Device 40, according to the third embodiment is also a depletion mode device, meaning that it is nominally on. Specifically, the application of an appropriate voltage to either gate electrode 32, 34 causes an interruption in the 2DEG, whereby device 40 is turned off.

[0032] According to one aspect of the present invention, first gate electrode 32 and second gate electrode 34 are independently operable, meaning that each gate electrode receives a voltage pulse from a respective gate pad (shown later). Due to the fact that the distance $\beta$ between each gate electrode 32, 34 and a nearest ohmic electrode 25, 26 is the same, device 40 is also symmetric. That is, device 40 exhibits the same voltage blocking characteristic regardless of which ohmic electrode is at a higher potential.

[0033] Gate electrodes 32, 34 in the preferred embodiment make schottky contacts with second semiconductor body 21. However, gate contacts 32, 34 may be replaced with an insulated gate that includes a gate electrode, and a gate insulator interposed between the gate electrode and second semiconductor body 21 without deviating from the present invention..

[0034] Device 40 is a bi-directional switch that functions as two switches in one location. Each gate electrode 32, 34 in device 40 can operate independently to turn the device ON/OFF. Accordingly, device 40 can be made to operate like a NOR gate, in

which when any one of the two gate electrodes 32, 34 is active the device is off. If either or both of gate electrodes 32, 34 have an electrical potential applied to cause a switching event, the channel between source/drain electrodes 45, 46 is interrupted.

[0035] Device 40 includes a shared drift region to improve the conduction capabilities of the device, while increasing the functionality through the use of the dual gate structure. Referring for a moment to Figures 1 and 2, the single gate device has two drift regions in series with each other. Therefore, a device according to the present invention which includes a single gate electrode 27 requires twice as much semiconductor material. On the other hand, by providing a shared drift region in the dual gate structure of device 40, the device area is reduced nearly in half and the device has additional functionality due to the two separate channels with the two separate gate electrodes. In device 40, each gate electrode 47, 48 is referenced to the nearby ohmic electrode 25, 26. Specifically, for a given blocking voltage, the separation between the gate edge and the drain is the relevant factor. Thus, in a single gate device the separation from source to drain is 2A + width of the gate, where A is the distance between the edge of the gate and the source or the drain. For a dual-gated device the length A is between the two gates to withstand the voltage, and the total length for the device is A + 2 gate widths + 2 gate to drain/source spaces. The length A is the largest space and only occurs once in a dual-gated design.

[0036] Referring to Figure 4, in which like numerals identify like features, a device 50 according to the fourth embodiment of the present invention is an enhancement mode device, which means that it is nominally off. Similar to the second embodiment, device 50 includes gate electrodes 32, 34, each of which is disposed within a respective recess 38 in second semiconductor body 21. Each recess 38 causes an interruption in the 2DEG, which can be restored upon application of a suitable voltage to gate electrodes 32, 34.

[0037] Accordingly, device 50 acts like a power logic AND gate, in which current flows to/from electrodes 25, 26 when both gate electrodes 32, 34 have a potential applied to them.

[0038] Because of the shared drift region used by the two channels controlled through gate electrodes 32, 34 device 50 can be made smaller than device 30.

[0039] Similar to device 40, first gate electrode 32 is a distance β from first ohmic electrode 25, and second gate electrode 34 is the same distance β from second ohmic electrode 26, whereby device 50 is rendered symmetric. That is, the voltage blocking capability of the device is the same regardless of which ohmic electrode is at the higher potential.

[0040] Furthermore, similar to the third embodiment, each gate electrode 32, 34 is independently operable.

[0041] Similar to the other three embodiments, gate electrodes 32, 34 preferably make schottky contacts with second semiconductor body 21, but can be replaced with insulated gates that include a gate electrode and a gate insulator without deviating from the present invention.

[0042] Referring to Figure 5, a device according to either the first embodiment or the second embodiment is preferably arranged to have interdigitated ohmic electrodes 25, 26. Specifically, a device according to the preferred embodiment includes two opposing and preferably parallel runners 40, 42. Each runner 40, 42 is electrically connected with one of the two ohmic electrode 25, 26. Thus, runner 40 is electrically connected to first ohmic electrodes 25, and runner 42 is electrically connected to second ohmic electrodes 26. It should be noted that ohmic electrodes 25, 26 are arranged parallel to one another whereby an interdigitated arrangement is achieved. Each gate electrodes 27 is disposed between an opposing pair of first and second ohmic electrodes 25, 26. It should be noted that a gate runner 44 is also provided to electrically connect gate electrodes 27 to one another.

[0043] Referring next to Figure 6, in which like numerals identify like features, a device according to either the third or the fourth embodiment of the present invention

includes two gate runners 46, 48. Each gate runner 46, 48 is electrically connected only to one of the gate electrodes 32, 34.

[0044] Referring to Figure 7, in a device according to either the third or the fourth embodiment, each gate runner 46, 48 is electrically connected to a respective gate pad 50, 52, whereby each one of the gate electrodes 32, 34 becomes capable of independent operation. Also, it should be noted that all runners 40 connected to first ohmic electrode 25 are electrically connected to a respective common pad 54, and all runners 42 connected to second ohmic electrodes 26 are electrically connected to a respective common pad 56.

[0045] Referring now to Figure 8, an alternate arrangement for gate electrodes and ohmic electrode 26, 25 is illustrated as structure 60. Structure 90 includes two gate electrodes, gate electrodes 32, 34. Gate electrodes 32, 34 are provided without insulation and are formed to have a smooth rounded edges to prevent crowding of the electric fields. Gate electrodes 32, 34 can be formed without the need for implant operations, thereby reducing damage to the structure that can potentially decrease the breakdown resistance of the device. Device 60 is formed with fewer etching operations to reduce the amount of material that is removed. Accordingly, the volume of conductive pathways for carriers through the material is increased, which in turn lowers the overall resistance of device 90.

[0046] Referring now to Figures 9-18, an example of a process for fabrication of a single gate bidirectional switch in the III-nitride material system is illustrated. Although a single gate device is illustrated, it should be apparent that the process is equally applicable to the construction of a dual gate device. Referring to Figure 9, the process commences with a prepared GaN wafer that can be obtained through known methods. Wafer 70 includes a substrate 72 composed of sapphire, a compensated GaN layer 74 disposed on substrate 72, an AlGaN layer 76 over the compensated GaN layer 74 and finally a doped GaN layer 78 overlaying AlGaN layer 76. Wafer 70 is constructed to compensate for strain to prevent dislocations and cracking in compensated GaN layer 74.

[0047] Referring now to Figure 10, wafer 70 has a mask layered 80 deposited thereon to define an active region. Referring to Figure 11, wafer 70 is etched down to substrate 72. After mask 80 is stripped, a metal layer 82 is deposited over doped GaN layer 78. Metal layer 82 may be composed of an ohmic metal alloy, such as Ti/Al/TiW, for example. Device 160 is then annealed, for example at 850°C for one minute.

[0048] Referring now to Figure 13, ohmic electrodes are patterned with mask portions 84 and an etch is performed to remove the exposed metal and doped GaN layers after which the mask is removed resulting in the structure of Figure 14.

[0049] Referring next to Figure 15, a layer of SiN 85, and a layer of $SiO_2$ 86 are deposited over the structure shown in Figure 14. Thereafter, a mask 88 is formed which includes window 90 to define the region which is to receive a gate electrode. Window 90 is used to etch away a portion of the $SiO_2$ layer 86, leaving behind a thin portion of the SiN 85 (e.g. about 200Å). Mask 88 is then stripped and gate metal 92, such as TiW. is deposited to result in the structure shown in Figure 16. Next, gate metal 92 is etched to leave gate electrode 27 in place. Referring next to Figure 17, an insulation layer 94 is formed, and etched to include openings 96 therein over the ohmic electrodes. Then, contact metal is deposited to fill openings 96 and make contact with the ohmic electrodes. Thereafter, the deposited contact metal is etched to form contacts 98 as seen in Figure 18.

[0050] It should be apparent that the above described process for forming a single gate bidirectional III-nitride switch is equally applicable to forming a dual bidirectional III-nitride switch. It should also be apparent that a number of devices maybe formed in a single wafer to form a number of useful components for a given application. For example, a number of useful devices may be connected to together to form a larger bidirection switching device capable of carrying high amounts of current. Alternately, a number of so formed high current devices may be connected to form a bidirectional 3 phase bridge, a bidirectional full bridge or a bidirectional half bridge. In addition, variations on the device may be realized to form such useful devices as a Schottky bridge or a bidirectional half bridge with a common drain node. Each of the above devices is

capable of carrying large amounts of current in a smaller area then that possible with conventional semiconductor devices. Because of the greater capability of the III-nitride devices the bidirectional switches may be made smaller and still perform as well larger conventional devices.

[0051] The bi-directional switch of the present invention can also be formed using other known techniques for construction of III-nitride devices including the interposition of super lattice layer structures and varying alloy layers, including InAlGaN with particular qualities to balance and in-plane lattice structure constant for example. Thus, although the preferred embodiments shown herein include a layer of AlGaN formed over GaN, the present invention is not restricted to such a combination. For example, an AlGaN/InGaN/GaN can be used without deviating from the present invention.

[0052] Furthermore, a device according to the present invention can be modified to include other features. Referring, for example, to Figure 19, a bidirectional device according to the present invention may include a current sense pad 57 which is electrically connected to the channel to detect the amount of current crossing the channel.

[0053] It should be noted that in the device fabricated through the method illustrated by Figures 9-18, gate electrode 27 is insulated from the AlGaN layer by an SiN insulation layer. A device according to the present invention may be formed with a gate electrode that forms schottky or ohmic contact with the AlGaN layer without deviating from the present invention.

[0054] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

WHAT IS CLAIMED IS:

1. A bidirectional semiconductor switch comprising:

a substrate;

a first semiconductor body composed of one III-nitride semiconductor material;

a second semiconductor body formed over said first semiconductor body and composed of another III-nitride semiconductor material, having a band gap that is different from that of said one III-nitride semiconductor material;

a first ohmic electrode formed on and ohmically connected to a first portion of said second semiconductor body;

a second ohmic electrode formed on and ohmically connected to a second portion of said second semiconductor body; and

a gate electrode formed on said second semiconductor body and disposed between said first ohmic electrode and said second ohmic electrode, wherein said gate electrode is positioned such that said device exhibits a symmetric voltage blocking capability.

2. A semiconductor switch according to claim 1, wherein said one semiconductor body is comprised of GaN and said another semiconductor body is comprised of AlGaN.

3. A semiconductor switch according to claim 1, wherein said gate electrode either makes a schottky contact with said second semiconductor body or is insulated from said second semiconductor body by a gate insulation body.

4. A semiconductor switch according to claim 1, wherein said gate electrode is comprised of either titanium, gold, aluminum, silver, chromium, tungsten, platinum, nickel, palladium and indium.

5. A semiconductor switch according to claim 1, wherein said ohmic electrodes are comprised of either gold, silver, aluminum, titanium or indium.

6. A semiconductor switch according to claim 1, further comprising a recess formed in said another semiconductor layer and said gate electrode resides in said recess.

7. A semiconductor switch according to claim 1, wherein said gate electrode is spaced an equal distance from said first ohmic electrode and said second ohmic electrode.

8. A semiconductor switch according to claim 1, wherein said substrate is comprised of either silicon, SiC, or sapphire.

9. A semiconductor switch according to claim 1, wherein said switch operates in depletion mode.

10. A semiconductor switch according to claim 1, wherein said switch operates in enhancement mode.

11. A bidirectional semiconductor switch comprising:

a substrate;

a first semiconductor body composed of one III-nitride semiconductor material;

a second semiconductor body formed over said first semiconductor body and composed of another III-nitride semiconductor material, having a band gap that is different from that of said one III-nitride semiconductor material;

a first ohmic electrode formed on and ohmically connected to a first portion of said second semiconductor body;

a second ohmic electrode formed on and ohmically connected to a second portion of said second semiconductor body;

a first gate electrode formed on said second semiconductor body and disposed between said first ohmic electrode and said second ohmic electrode; and

a second gate electrode formed on said second semiconductor body and disposed between said first ohmic electrode and said second ohmic electrode, wherein said gate

electrodes are positioned such that said device exhibits a symmetric voltage blocking capability.

12. A semiconductor switch according to claim 11, wherein said one semiconductor body is comprised of GaN and said another semiconductor body is comprised of AlGaN.

13. A semiconductor switch according to claim 11, wherein said gate electrodes make a schottky contact with said second semiconductor body.

14. A semiconductor switch according to claim 11, wherein said gate electrodes are comprised of either titanium, gold, aluminum, silver, chromium, tungsten, and indium.

15. A semiconductor switch according to claim 11, wherein said ohmic electrodes are comprised of either gold, silver, aluminum, or indium.

16. A semiconductor switch according to claim 11, further comprising a recess formed in said another semiconductor layer , wherein at least one of said gate electrodes resides in said recess.

17. A semiconductor switch according to claim 11, further comprising a first recess and a second recess formed in said another semiconductor layer, wherein said first gate electrode resides in said first recess and said second gate electrode resides in said second recess.

18. A semiconductor switch according to claim 11, wherein said first gate electrode and said second gate electrode are independently operable.

19. A semiconductor switch according to claim 11, wherein said first gate electrode is spaced a first distance from said first ohmic electrode and said second gate electrode is spaced a second distance from said second ohmic electrode, said first distance and said second distance being equal.

20. A semiconductor switch according to claim 11, wherein said substrate is comprised of either silicon, SiC, or sapphire.

21. A semiconductor switch according to claim 11, wherein said at least one of said gate electrodes is insulated from said second semiconductor body by a gate insulation body.

22. A semiconductor switch according to claim 11, wherein at least one of said gate electrodes make a schottky contact with said second semiconductor body.

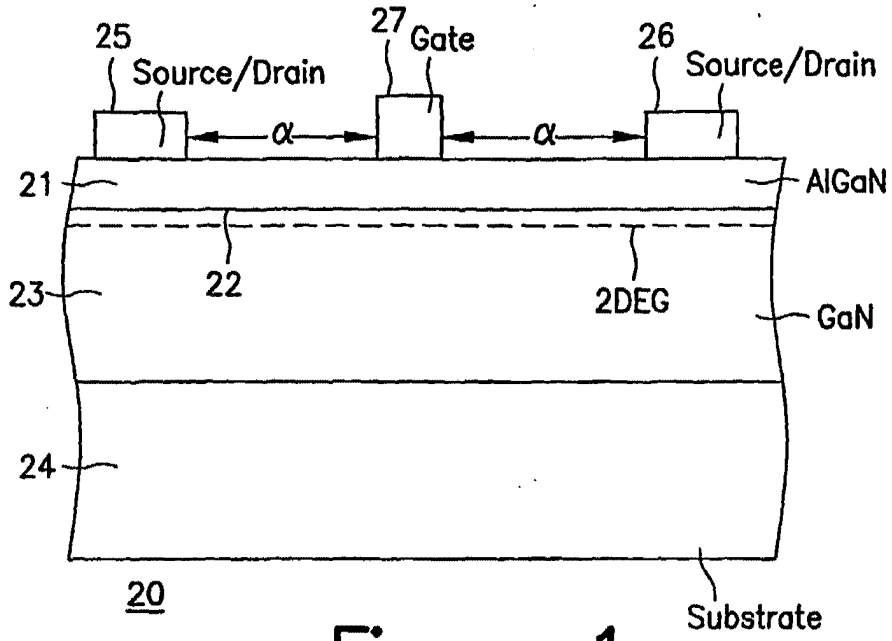



Figure 1

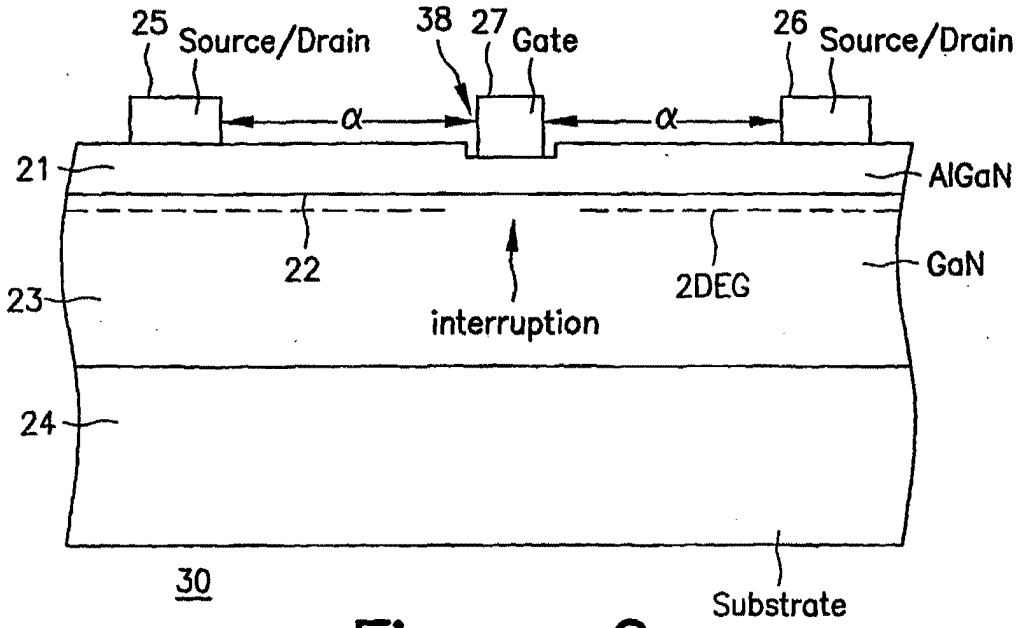



Figure 2

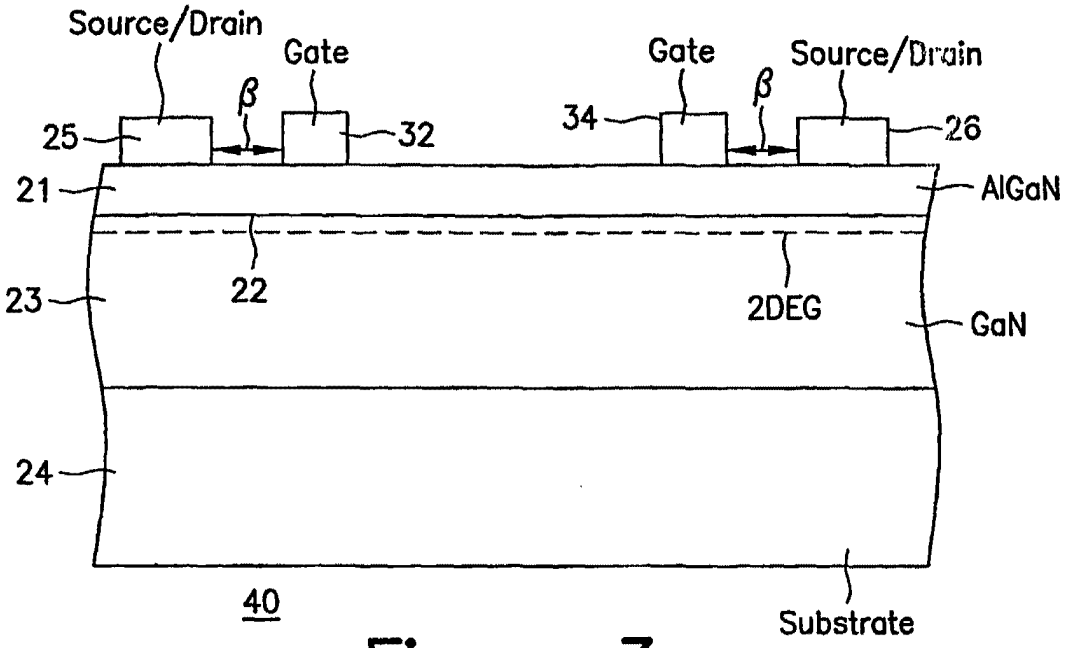



Figure 3

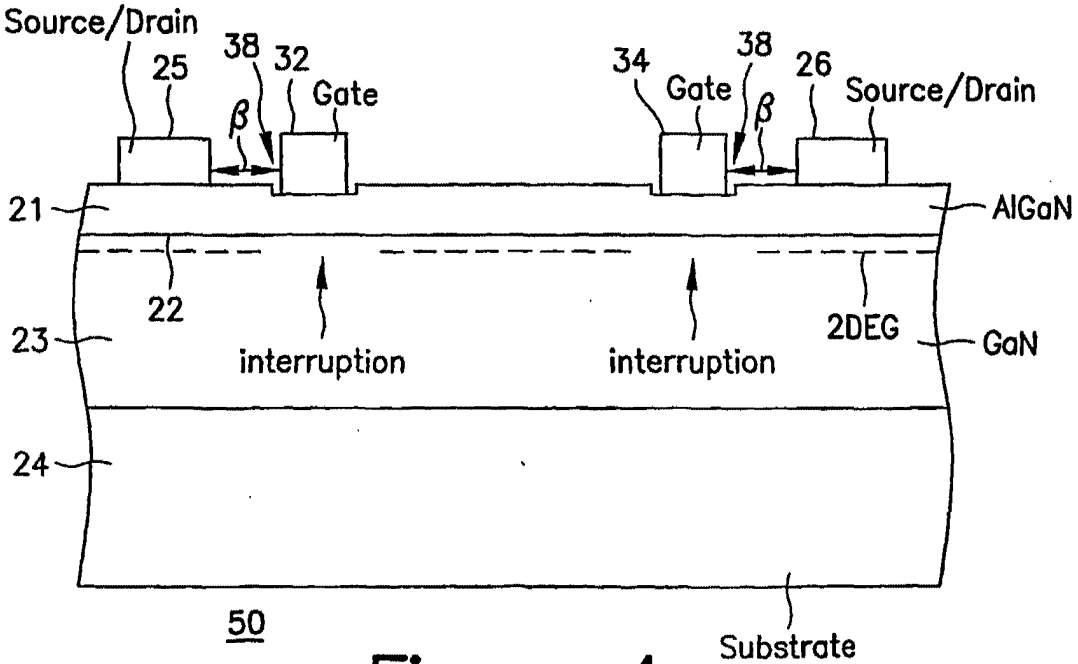



Figure 4

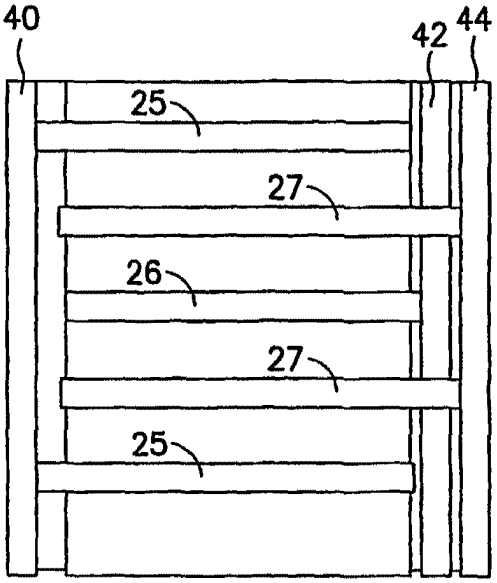



Figure 5

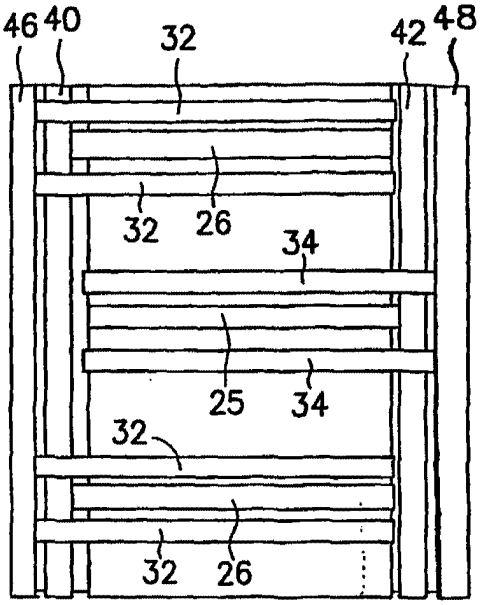



Figure 6

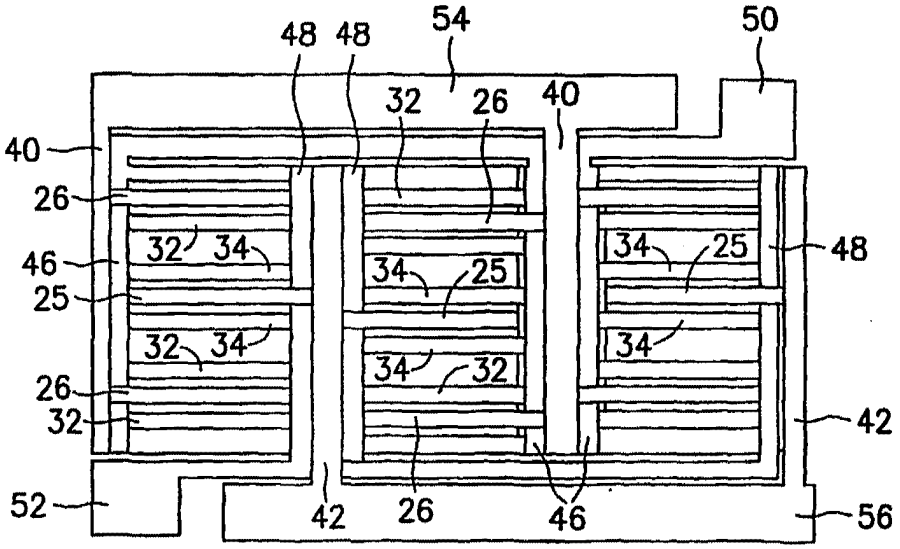



Figure 7

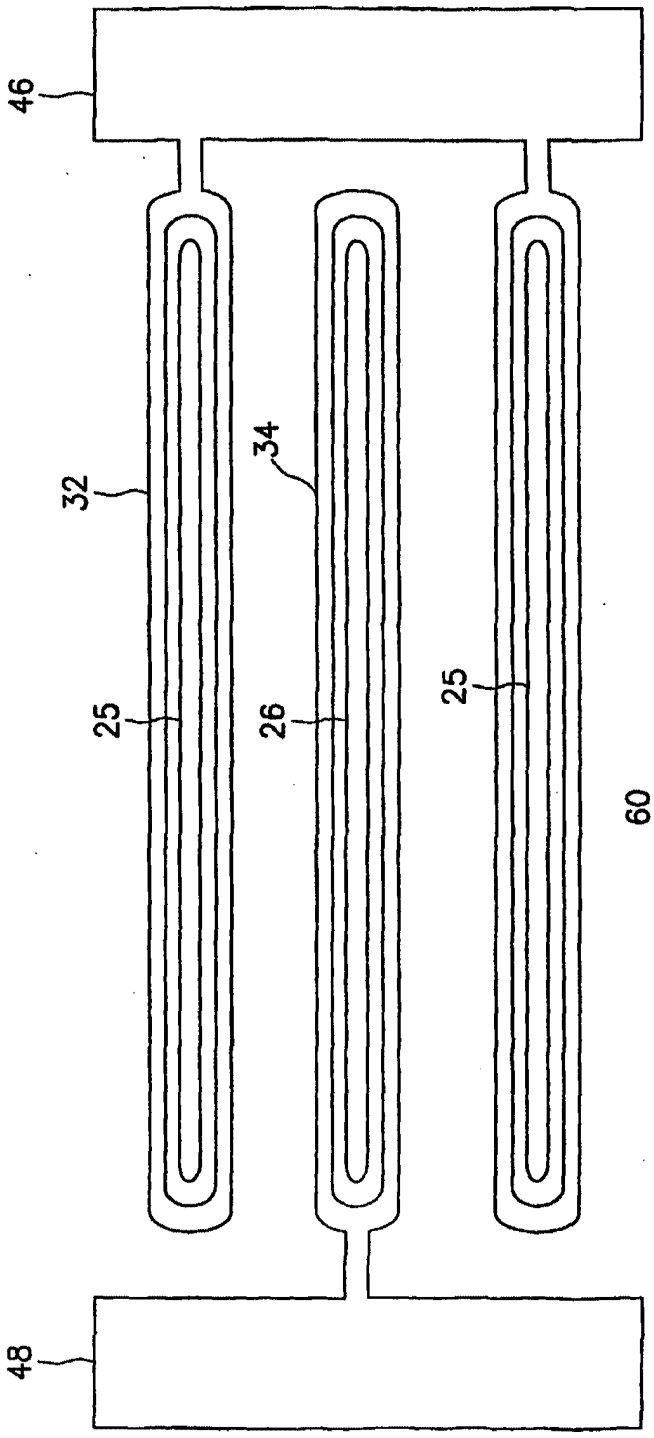



Figure 8

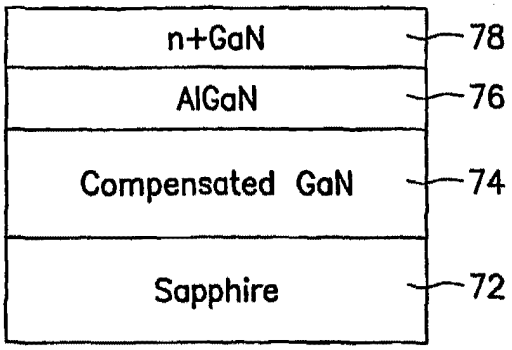



Figure 9

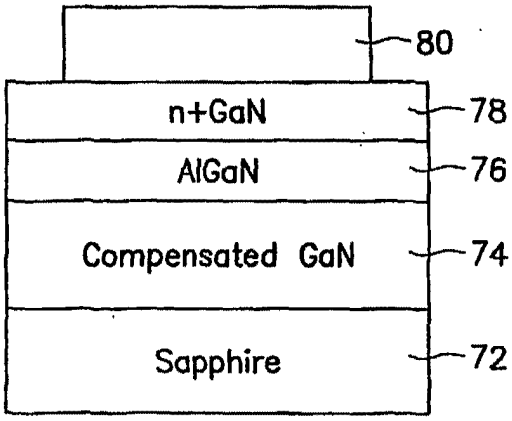



Figure 10

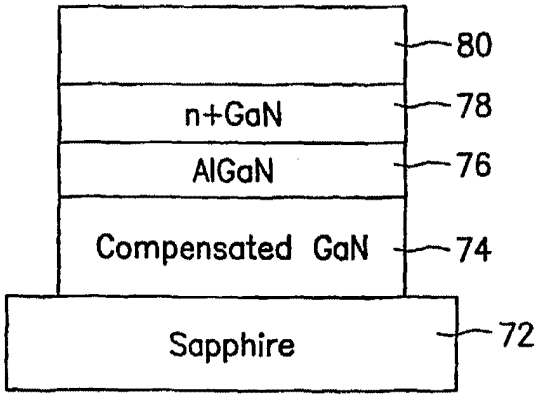



Figure 11

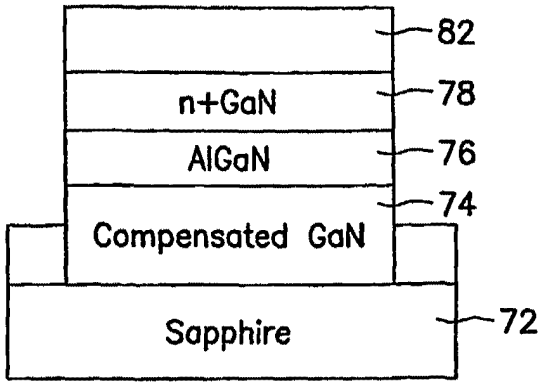



Figure 12

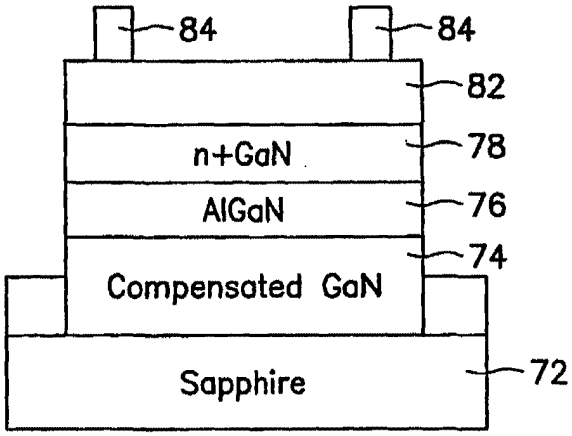



Figure 13

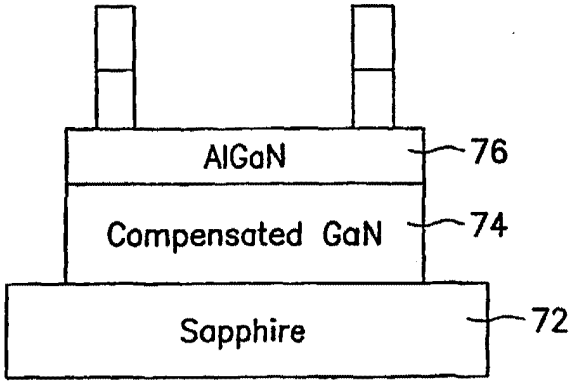



Figure 14

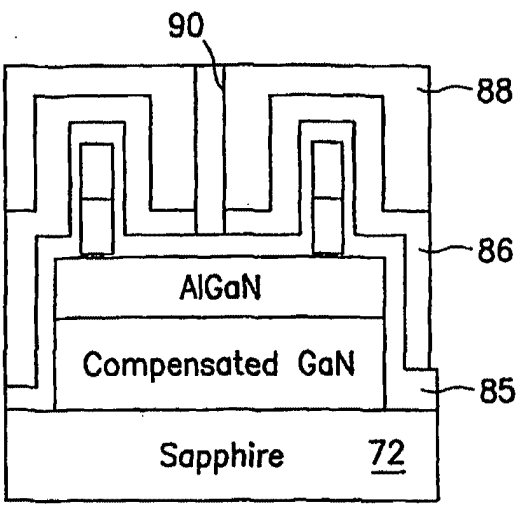



Figure 15

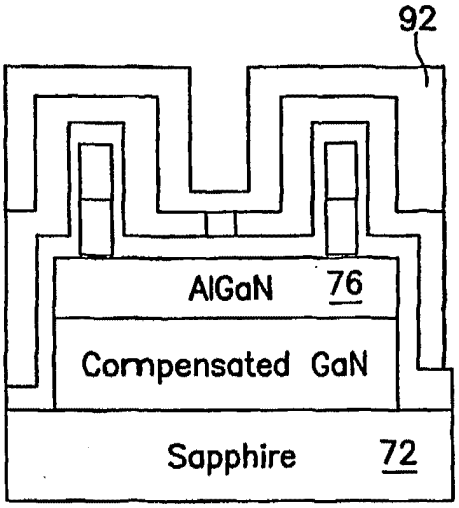



Figure 16

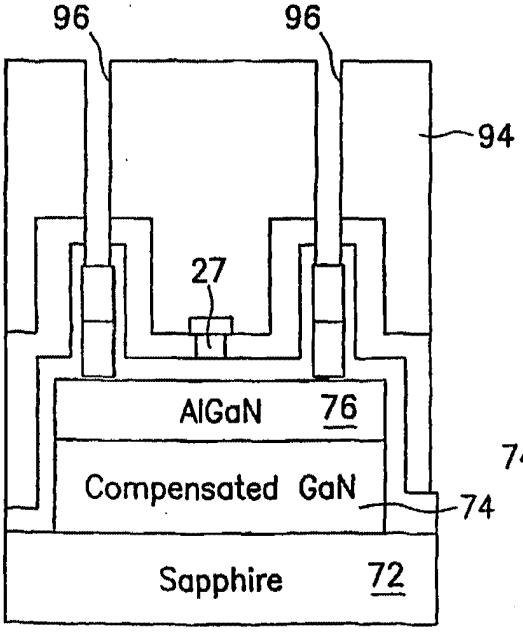



Figure 17

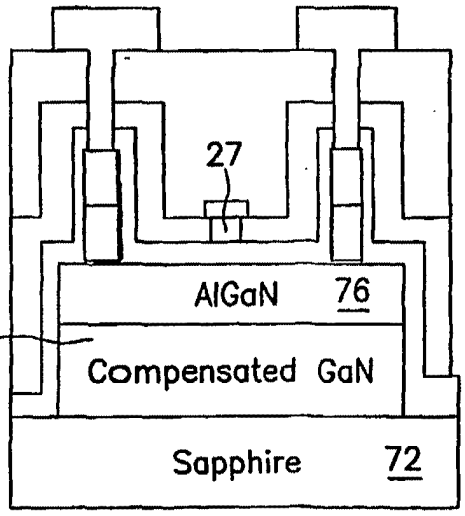



Figure 18

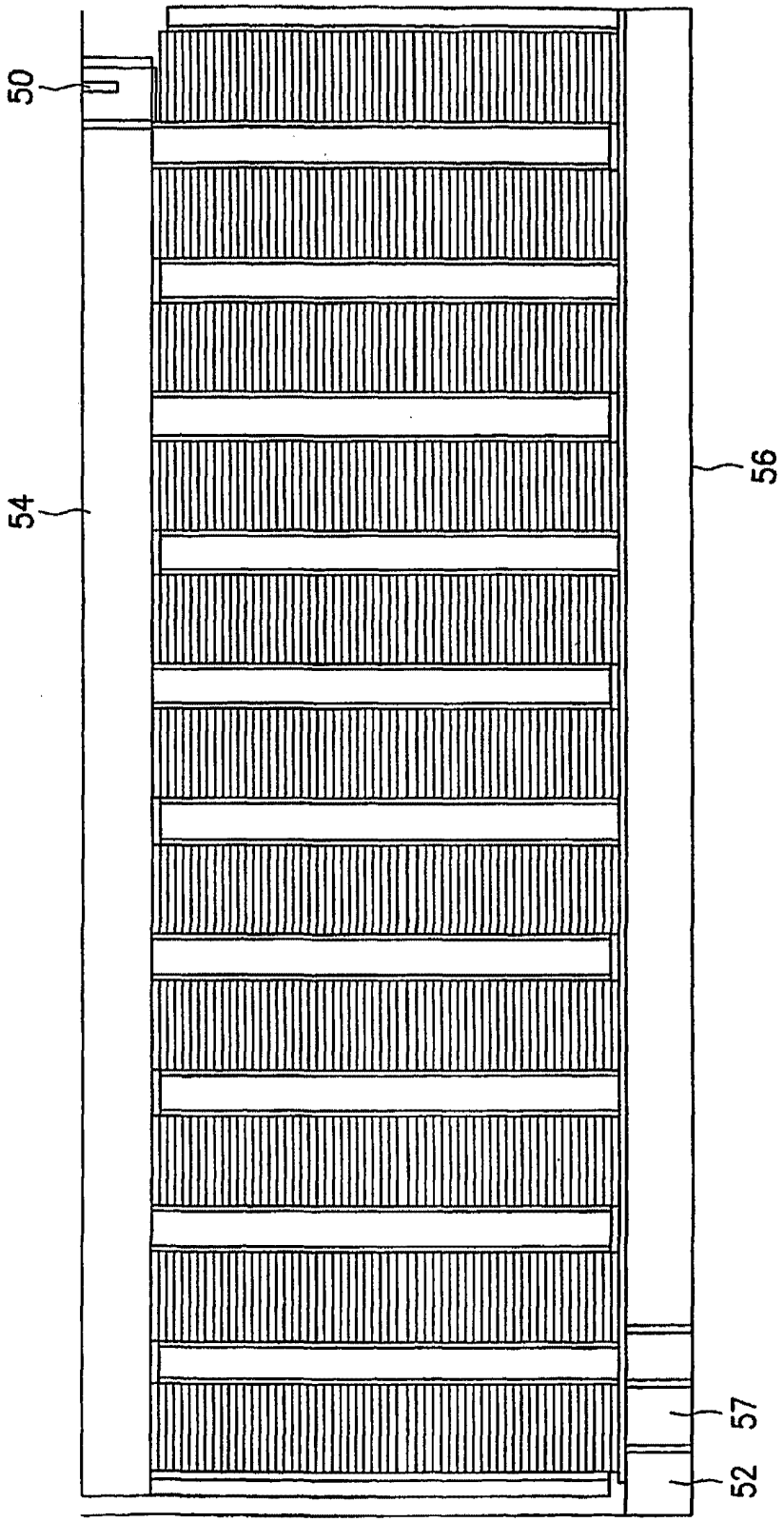



Figure 19

Espacenet

# Bibliographic data: JP2008522436 (A) — 2008-06-26

## NORMALLY-OFF INTEGRATED JFET POWER SWITCHES IN WIDE BANDGAP SEMICONDUCTORS AND METHODS OF MAKING

| | | |
|---|---|---|
| **Inventor(s):** | | |
| **Applicant(s):** | | |
| **Classification:** | **- international:** | ***H01L21/28; H01L21/337; H01L27/095; H01L29/417; H01L29/80; H01L29/808; H01L29/861*** |
| | **- European:** | H01L27/098; H01L29/808B; H01L29/808C |
| **Application number:** | JP20070544421T 20051130 | |
| **Priority number(s):** | US20040000222 20041201; WO2005US42982 20051130 | |
| **Also published as:** | WO2006060337 (A2) WO2006060337 (A3) US2006113593 (A1) US7202528 (B2) NZ555629 (A) more | |

**Abstract not available for JP2008522436 (A)**
**Abstract of corresponding document: WO2006060337 (A2)**

Wide bandgap semiconductor devices including normally-off VJFET integrated power switches are described. The power switches can be implemented monolithically or hybridly, and may be integrated with a control circuit built in a single-or multi-chip wide bandgap power semiconductor module. The devices can be used in high-power, temperature-tolerant and radiation-resistant electronics components. Methods of making the devices are also described.

Last updated: 14.03.2012 Worldwide Database 5.7.38; 93p

(19)日本国特許庁(JP)　(12)公表特許公報(A)　(11)特許出願公表番号
特表2008-522436
(P2008-522436A)
(43)公表日　平成20年6月26日(2008.6.26)

| (51)Int.Cl. | | F I | | | テーマコード（参考） |
|---|---|---|---|---|---|
| H01L 27/095 | (2006.01) | H01L | 29/80 | E | 4M104 |
| H01L 21/337 | (2006.01) | H01L | 29/80 | C | 5F102 |
| H01L 29/808 | (2006.01) | H01L | 29/80 | V | |
| H01L 29/80 | (2006.01) | H01L | 29/91 | K | |
| H01L 29/861 | (2006.01) | H01L | 29/50 | J | |

審査請求 未請求　予備審査請求 未請求　（全 45 頁）　最終頁に続く

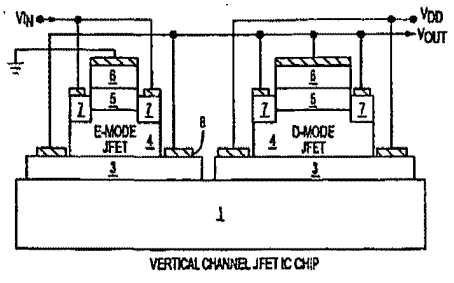
(21)出願番号　特願2007-544421 (P2007-544421)
(86)(22)出願日　平成17年11月30日 (2005.11.30)
(85)翻訳文提出日　平成19年6月22日 (2007.6.22)
(86)国際出願番号　PCT/US2005/042982
(87)国際公開番号　WO2006/060337
(87)国際公開日　平成18年6月8日 (2006.6.8)
(31)優先権主張番号　11/000,222
(32)優先日　平成16年12月1日 (2004.12.1)
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(54)【発明の名称】ワイドバンドギャップ半導体における常時オフ集積ＪＦＥＴ電源スイッチおよび作成方法

(57)【要約】
常時オフＶＪＦＥＴ集積電源スイッチを含むワイドバンドギャップ半導体デバイスが、記述される。電源スイッチは、モノリシックまたはハイブリッドに実装され得、シングルまたはマルチチップのワイドバンドギャップ電源半導体モジュールにビルトインされた制御回路と一体化され得る。該デバイスは、高電力で温度に対する許容性があり、耐放熱性のエレクトロニクスコンポーネントにおいて用いられ得る。該デバイスを作成する方法もまた、記述される。



【特許請求の範囲】
【請求項1】
互いに対向する第１および第２の主要表面を有する基板と、
該基板上の該第１の主要表面上の隔たっている位置にある第１および第２のジャンクション電界効果型トランジスタと
を備えている、モノリシック集積回路であって、
該第１および第２のジャンクション電界効果型トランジスタのそれぞれは、
該基板の第１の主要表面上にあり、該基板の第１の主要表面と同一でない広がりを有するｎ型半導体材料のドレイン層であって、該ドレイン層を囲む該基板の部分は露出している、ドレイン層と、
該ドレイン層上にあり、該基板の第１の主要表面と同一でない広がりを有するｎ型半導体材料のドリフト層であって、該ドレイン層の部分は露出しており、該ドリフト層は、該ドレイン層よりも低い導電性を有する、ドリフト層と、
該ドリフト層上の隔たっている位置上にある１つ以上の隆起した領域であって、該１つ以上の隆起した領域のそれぞれは、該ドリフト層上のｎ型半導体材料のチャネル領域と該チャネル領域上のｎ型半導体のソース領域とを含み、該ソース領域の該半導体材料は、該チャネル層の導電性よりも高い導電性を有する、１つ以上の隆起した領域と、
該１つ以上の隆起した領域と隣接し、該ドリフト層および該チャネル領域のｎ型材料と整流ジャンクションを形成している、該ドリフト層上のｐ型半導体材料のゲート領域と、
該ゲート領域および該ソース領域上および該ドレイン層の露出した部分上のオーミックコンタクトと、
該第１のジャンクション電界効果型トランジスタの該ソースのオーミックコンタクトと、該第２のジャンクション電界効果型トランジスタの該ゲートのオーミックコンタクトとの間の第１の電気接続と、
該第１のジャンクション電界効果型トランジスタの該ドレインのオーミックコンタクトと、第２のジャンクション電界効果型トランジスタの該ソースのオーミックコンタクトとの間の第２の電気接続と
を備えている、モノリシック集積回路。
【請求項2】
前記ドレイン層、ドリフト層、ゲート領域、チャネル領域、およびソース領域のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項１に記載の集積回路。
【請求項3】
前記ドレイン層、ドリフト層、ゲート領域、チャネル領域、およびソース領域のそれぞれの前記半導体材料は、ＳｉＣ、または、ＩＩＩ属窒素化合物半導体材料である、請求項２に記載の集積回路。
【請求項4】
前記ドレイン層は、０．２～５μｍの厚さを有し、前記ドリフト層は、０．５～１０μｍの厚さを有し、前記チャネル領域は、０．２～１．５μｍの厚さを有し、前記ソース領域は、０．２～１．５μｍの厚さを有し、前記ゲート領域は、０．１μｍまたはそれ以上の厚さを有する、請求項１に記載の集積回路。
【請求項5】
前記ドレイン層は、$5\times10^{18}\ cm^{-3}$よりも大きいドーパント濃度を有し、前記ドリフト層は、$5\times10^{15}$～$5\times10^{17}\ cm^{-3}$のドーパント濃度を有し、前記チャネル領域は、$5\times10^{15}$～$5\times10^{17}\ cm^{-3}$のドーパント濃度を有し、前記ソース領域は、$5\times10^{18}\ cm^{-3}$よりも大きいドーパント濃度を有し、前記ゲート領域は、$5\times10^{18}\ cm^{-3}$よりも大きいドーパント濃度を有する、請求項１に記載の集積回路。
【請求項6】
前記基板は、半絶縁基板である、請求項１に記載の集積回路。
【請求項7】

前記第２の電界効果型トランジスタは、前記ゲート領域に隣接し、該ゲート領域と電気的に通信する、前記ドリフト層上のｎ型半導体材料のショットキーチャネル領域と、該ショットキーチャネル領域とともに金属半導体整流ジャンクションを形成している、該ショットキーチャネル領域上の金属層とを備えているショットキージャンクションをさらに備え、該集積回路は、該ショットキー金属接触と、前記第１の電気接続との間の第３の電気接続をさらに備えている、請求項１に記載の集積回路。

【請求項8】

前記ショットキーチャネル領域は、０．２～１．５μｍの厚さ、および５ｘ１０$^{15}$～５ｘ１０$^{17}$ｃｍ$^{-3}$のドーパント濃度を有する、請求項１に記載の集積回路。

【請求項9】

互いに対向する第１および第２の主要表面を有する基板と、

該基板上の該第１の主要表面上にあるｐ型半導体材料のバッファ層と、

ｎ型半導体材料のそれぞれが該バッファ層上で間隔を置いた関係にある、第１および第２の隔たっているチャネル領域であって、該第２のチャネル領域は、該バッファ層上のベース部分と上側部分とを含み、該ベース部分は、肩部を形成するように該上側部分を越えてラテラルに広がる、第１および第２の隔たっているチャネル領域と、

該第１のチャネル領域と隣接し、該第１のチャネル領域と電気的に通信する、該バッファ層上のｎ型半導体材料のソース領域と、

該第１のチャネル領域と該第２のチャネル領域との間の該バッファ層上の、該第１のチャネル領域および該第２のチャネル領域の両方と電気的に通信する、ｎ型半導体材料のソース／ドレイン領域であって、該ソース／ドレイン領域の一部は、該第２のチャネル領域の肩部部分とオーバーラップしている、ソース／ドレイン領域と、

ドレイン領域であって、該ドレイン領域は、該バッファ層と直接的に接触しないように、該第２のチャネル領域の該肩部の上にある、ドレイン領域と、

該第１のチャネル領域上の、該第１のチャネル領域と整流ジャンクションを形成しているｐ型半導体材料の第１のゲート領域と、

該第２のチャネル領域のトップ部分の上側の表面上の、該第２のチャネル領域と整流ジャンクションを形成しているｐ型半導体材料の第２のゲート領域と、

該ソース領域、該第１および第２のゲート領域、該ソース／ドレイン領域、および該ドレイン領域上のオーミックコンタクトと

を備えている、モノリシック集積回路。

【請求項10】

前記バッファ層は、少なくとも０．１μｍの厚さを有し、前記第１および第２のチャネル領域のそれぞれは、０．２～１．５μｍの厚さを有し、前記ソース、ソース／ドレイン、およびドレイン領域のそれぞれは、少なくとも０．１μｍの厚さを有し、前記第１および第２のゲート領域のそれぞれは、０．２～１．５μｍ以上の厚さを有する、請求項９に記載の集積回路。

【請求項11】

前記バッファ層は、１ｘ１０$^{15}$～１ｘ１０$^{17}$ｃｍ$^{-3}$のドーパント濃度を有し、前記第１および第２のチャネル領域のそれぞれは、５ｘ１０$^{15}$～２ｘ１０$^{17}$ｃｍ$^{-3}$のドーパント濃度を有し、前記ソース、ソース／ドレイン、およびドレイン領域のそれぞれは、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有し、前記第１および第２のゲート領域のそれぞれは、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有する、請求項９に記載の集積回路。

【請求項12】

前記基板は、半絶縁基板である、請求項９に記載の集積回路。

【請求項13】

前記第２のチャネル領域は、前記第１のチャネル領域よりも大きい厚さを有する、請求項９に記載の集積回路。

【請求項14】

前記第２のゲート接触と前記ソース／ドレイン接触との間の電気接続をさらに備えている、請求項９に記載の集積回路。

【請求項15】

前記第２のゲート領域と前記ソース領域との間の電気接続をさらに備えている、請求項９に記載の集積回路。

【請求項16】

前記ドレイン領域は、前記第２のゲート領域からラテラルに間隔を置かれ、前記第２のチャネル領域の前記トップ部分にラテラルドリフト領域を形成している、請求項９に記載の集積回路。

【請求項17】

前記バッファ層、ドレイン領域、ソース／ドレイン領域、ドリフト層、第１および第２のゲート領域、第１および第２のチャネル領域、およびソース領域のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項９に記載の集積回路。

【請求項18】

前記バッファ層、ドレイン領域、ソース／ドレイン領域、ドリフト層、第１および第２のゲート領域、第１および第２のチャネル領域、およびソース領域のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項１７に記載の集積回路。

【請求項19】

第１のバーチカルチャネルＪＦＥＴを含む集積回路であって、

該第１のバーチカルチャネルＪＦＥＴは、

互いに対向する第１および第２の表面を有する基板と、

該基板の該第１の表面上の、ｎ型半導体材料のドレイン層と、

前記ドレイン層上にあり、該ドレイン層と同一でない広がりを有するｎ型半導体材料のドリフト層であり、該ドレイン層の部分は露出しており、該ドリフト層は、該ドレイン層よりも低い導電性を有する、ドリフト層と、

該ドリフト層上のｎ型半導体材料のチャネル領域と該チャネル領域上のｎ型半導体のソース領域とを含む１つ以上の隆起した領域であって、該ソース領域の該材料は、該チャネル領域の導電性よりも高い導電性を有する、１つ以上の隆起した領域と、

該１つ以上の隆起した領域と隣接し、該ドリフト層および該チャネル領域と整流ジャンクションを形成する、該ドリフト層上のｐ型半導体材料のゲート領域と、

該ゲート領域および該ソース領域上および該ドレイン層の露出した部分上のオーミックコンタクトと

を備えている、第１のバーチカルチャネルＪＦＥＴと、

該第１のバーチカルチャネルＪＦＥＴから隔たっている第２のバーチカルチャネルＪＦＥＴであって、

該第２のバーチカルチャネルＪＦＥＴは、

互いに対向する第１および第２の主要表面を有するｎ型半導体材料の基板と、

該基板の該第１の主要表面上のｎ型半導体材料のドレイン層と、

該ドレイン層上のｎ型半導体材料のドリフト層であって、該ドリフト層は、該ドレイン層よりも低い導電性を有する、ドリフト層と、

該ドリフト層上のｎ型半導体材料のチャネル領域と該チャネル領域上のｎ型半導体のソース領域とを含む１つ以上の隆起した領域であって、該ソース領域の該材料は、該チャネル領域の導電性よりも高い導電性を有する、１つ以上の隆起した領域と、

該１つ以上の隆起した領域と隣接し、該ドリフト層および該チャネル領域と整流ジャンクションを形成する、該ドリフト層上のｐ型半導体材料のゲート領域と、

該ゲートおよびソース領域上および該基板の該第２の主要表面上のオーミックコンタクトと

を備えている、第２のバーチカルチャネルＪＦＥＴと、

該第１のバーチカルチャネルＪＦＥＴの該ドレインオーミックコンタクトと該第２のバ

ーチカルチャネルＪＦＥＴの該ソースオーミックコンタクトとの間の第１の電気接続と、
該第１のバーチカルチャネルＪＦＥＴの該ソースオーミックコンタクトと該第２のバーチカルチャネルＪＦＥＴの該ゲートオーミックコンタクトとの間の第２の電気接続と
を備えている、集積回路。

【請求項20】

前記第１のバーチカルチャネルＪＦＥＴに対して、前記ドレイン層は、０．２～５μｍの厚さを有し、前記ドリフト層は、０．５～１０μｍの厚さを有し、前記チャネル領域は、０．２～１．５μｍの厚さを有し、前記ソース領域は、０．２～１．５μｍの厚さを有し、前記ゲート領域は、０．１μｍ以上の厚さを有する、請求項１９に記載の集積回路。

【請求項21】

前記第１のバーチカルチャネルＪＦＥＴに対して、前記ドレイン層は、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有し、前記ドリフト層は、５ｘ１０$^{15}$～５ｘ１０$^{17}$ｃｍ$^{-3}$のドーパント濃度を有し、前記チャネル領域は、５ｘ１０$^{15}$～５ｘ１０$^{17}$ｃｍ$^{-3}$を有し、前記ソース領域は、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有し、前記ゲート領域は、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有する、請求項１９に記載の集積回路。

【請求項22】

前記第１のバーチカルチャネルＪＦＥＴに対して、前記基板は、半絶縁基板である、請求項１９に記載の集積回路。

【請求項23】

前記第２のバーチカルチャネルＪＦＥＴに対して、前記ドレイン層は、０．５～１μｍの厚さを有し、前記ドリフト層は、５～３５０μｍの厚さを有し、前記チャネル領域は、０．２～１．５μｍの厚さを有し、前記ソース領域は、０．２～１．５μｍの厚さを有し、前記ゲート領域は、０．１μｍ以上の厚さを有する、請求項１９に記載の集積回路。

【請求項24】

前記第２のバーチカルチャネルＪＦＥＴに対して、前記ドレイン層は、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有し、前記ドリフト層は、２ｘ１０$^{14}$～２ｘ１０$^{16}$ｃｍ$^{-3}$のドーパント濃度を有し、前記チャネル領域は、５ｘ１０$^{15}$～５ｘ１０$^{17}$ｃｍ$^{-3}$のドーパント濃度を有し、前記ソース領域は、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有し、前記ゲート領域は、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有する、請求項１９に記載の集積回路。

【請求項25】

前記第２のバーチカルチャネルＪＦＥＴに対して、前記基板は、１ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有するｎ型基板である、請求項１９に記載の集積回路。

【請求項26】

前記第２のバーチカルチャネルＪＦＥＴは、前記ゲート領域に隣接し、該ゲート領域と電気的に通信する、前記ドリフト層上のｎ型半導体材料のショットキーチャネル領域と、ショットキーチャネル領域とともに金属半導体整流ジャンクションを形成している、前記ショットキーチャネル領域上の金属層とを備えているショットキージャンクションをさらに備え、前記集積回路は、ショットキー金属接触と、前記第１の電気接続との間の第３の電気接続をさらに備えている、請求項１９に記載の集積回路。

【請求項27】

前記ショットキーチャネル領域は、０．２～１．５μｍの厚さ、および５ｘ１０$^{15}$～５ｘ１０$^{17}$ｃｍ$^{-3}$のドーパント濃度を有する、請求項１９に記載の集積回路。

【請求項28】

前記第１および第２のバーチカルチャネルＪＦＥＴのそれぞれに対して、前記ドレイン層、ドリフト層、チャネル領域、ソース領域、およびゲート領域のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項１９に記載の集積回路。

【請求項29】

前記第１および第２のバーチカルチャネルＪＦＥＴのそれぞれに対して、前記ドレイン

層、ドリフト層、チャネル領域、ソース領域、およびゲート領域のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項２８に記載の集積回路。

【請求項30】

ディスクリートラテラルチャネルＪＦＥＴであって、

該ディスクリートラテラルチャネルＪＦＥＴは、

互いに対向する第１および第２の主要表面を有する基板と、

該基板の該第１の主要表面上の、ｐ型半導体材料のバッファ層と、

それぞれが該バッファ層上で間隔を置いた関係にあるｎ型半導体材料の、ディスクリートソースおよびドレイン領域と、

該ソースおよびドレイン領域の間の該バッファ層上の、該ソースおよびドレイン領域のそれぞれと電気的に通信する、ｎ型半導体材料のチャネル領域と、

該チャネル領域上の、該チャネル領域と整流ジャンクションを形成しているｐ型半導体材料のゲート領域と、

該ソース、ゲート、およびドレイン領域上のオーミックコンタクトと

を備えている、ディスクリートラテラルチャネルＪＦＥＴと、

ディスクリートバーチカルチャネルＪＦＥＴであって、

該ディスクリートバーチカルチャネルＪＦＥＴは、

互いに対向する第１および第２の主要表面を有するｎ型半導体材料の基板と、

該基板の該第１の主要表面上の、ｎ型半導体材料のドレイン層と、

該ドレイン層上のｎ型半導体材料のドリフト層であって、該ドリフト層は、該ドレイン層よりも低い導電性を有する、ドリフト層と、

該ドリフト層上のｎ型半導体材料のチャネル領域と該チャネル領域上のｎ型半導体のソース領域とをそれぞれが含む１つ以上の隔たっている隆起した領域であって、該ソース領域の該材料は、該チャネル領域の導電性よりも高い導電性を有する、１つ以上の隔たっている隆起した領域と、

該１つ以上の隆起した領域と隣接し、該ドリフト層および該チャネル領域と整流ジャンクションを形成している、該ドリフト層上のｐ型半導体材料のゲート領域と、

該ゲートおよびソース領域上、および該基板の該第２の主要表面上のオーミックコンタクトと

を備えている、ディスクリートバーチカルチャネルＪＦＥＴと、

該ラテラルチャネルＪＦＥＴの該ドレインオーミックコンタクトと該バーチカルチャネルＪＦＥＴの該ソースオーミックコンタクトとの間の第１電気接続と、

該ラテラルチャネルＪＦＥＴの該ソースオーミックコンタクトと該バーチカルチャネルＪＦＥＴの該ゲートオーミックコンタクトとの間の第２電気接続と

を備えている、集積回路。

【請求項31】

前記ラテラルチャネルＪＦＥＴに対して、前記バッファ層は、少なくとも０．１μｍの厚さを有し、前記チャネル領域は、０．２～１．５μｍの厚さを有し、前記ソースおよびドレイン領域のそれぞれは、少なくとも０．１μｍの厚さを有し、前記ゲート領域は、０．２～１．５μｍ以上の厚さを有する、請求項３０に記載の集積回路。

【請求項32】

前記ラテラルチャネルＪＦＥＴに対して：前記バッファ層は、$1\times10^{15}$～$1\times10^{17}$ $cm^{-3}$のドーパント濃度を有し、前記チャネル領域は、$5\times10^{15}$～$2\times10^{17}$ $cm^{-3}$のドーパント濃度を有し、前記ソースおよびドレイン領域のそれぞれは、$5\times10^{18}$ $cm^{-3}$よりも大きいドーパント濃度を有し、前記ゲート領域は、$5\times10^{18}$ $cm^{-3}$よりも大きいドーパント濃度を有する、請求項３０に記載の集積回路。

【請求項33】

前記ラテラルチャネルＪＦＥＴに対して、前記基板は、半絶縁基板である、請求項３０に記載の集積回路。

【請求項34】
前記バーチカルチャネルＪＦＥＴに対して、前記ドレイン層は、０．５～１μｍの厚さを有し、前記ドリフト層は、５～３５０μｍの厚さを有し、前記チャネル領域は、０．２～１．５μｍの厚さを有し、前記ソース領域は、０．２～１．５μｍの厚さを有し、前記ゲート領域は、０．１μｍ以上の厚さを有する、請求項３０に記載の集積回路。
【請求項35】
前記バーチカルチャネルＪＦＥＴに対して：前記ドレイン層は、$5\times10^{18}cm^{-3}$よりも大きいドーパント濃度を有し、前記ドリフト層は、$2\times10^{14}$～$2\times10^{16}cm^{-3}$のドーパント濃度を有し、前記チャネル領域は、$5\times10^{15}$～$5\times10^{17}cm^{-3}$のドーパント濃度を有し、前記ソース領域は、$5\times10^{18}cm^{-3}$よりも大きいドーパント濃度を有し、前記ゲート領域は、$5\times10^{18}cm^{-3}$よりも大きいドーパント濃度を有する、請求項３０に記載の集積回路。
【請求項36】
前記バーチカルチャネルＪＦＥＴに対して、前記基板は、$1\times10^{18}cm$よりも大きいドーパント濃度を有するｎ型基板である、請求項３０に記載の集積回路。
【請求項37】
前記ラテラルチャネルＪＦＥＴに対して、前記バッファ層、ドレイン領域、ソース領域、ゲート領域、およびチャネル領域のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項３０に記載の集積回路。
【請求項38】
前記ラテラルチャネルＪＦＥＴに対して、前記バッファ層、ドレイン領域、ソース領域、ゲート領域、およびチャネル領域のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項３７に記載の集積回路。
【請求項39】
前記バーチカルチャネルＪＦＥＴに対して、前記ドレイン層、ドリフト層、チャネル領域、ソース領域、およびゲート領域のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項３０に記載の集積回路。
【請求項40】
前記バーチカルチャネルＪＦＥＴに対して、前記ドレイン層、ドリフト層、チャネル領域、ソース領域、およびゲート領域のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項３９に記載の集積回路。
【請求項41】
互いに対向する第１および第２の主要表面を有する基板と、
該基板の該第１の主要表面上の、ｐ型半導体材料のバッファ層と、
該バッファ層上のｎ型半導体材料のチャネル層と、
該チャネル層上で間隔を置いた関係にある、ｎ型半導体材料の隔たっている該ソース領域および該ドレイン領域と、
該ソース領域と該ドレイン領域との間の該チャネル層上の、該ソース領域および該ドレイン領域のそれぞれから間隔を置いたｎ型半導体材料のソース／ドレイン領域と、
該ソース領域と該ソース／ドレイン領域との間の該チャネル層内で形成され、該チャネル層と整流ジャンクションを形成しているｐ型半導体材料の第１ゲート領域と、
該ソース／ドレイン領域と該ドレイン領域との間の該チャネル層内で形成され、該チャネル層と整流ジャンクションを形成しているｐ型半導体材料の第２のゲート領域と、
該ソース領域、該第１および第２のゲート領域、該ソース／ドレイン領域、および該ドレイン領域上のオーミックコンタクトと
を備えている、モノリシックラテラルチャネルジャンクション電界効果型トランジスタ（ＪＦＥＴ）。
【請求項42】
前記バッファ層は、少なくとも０．１μｍの厚さを有し、前記チャネル層は、０．３～１．５μｍの厚さを有し、前記ソース、ソース／ドレイン、およびドレイン領域のそれぞ

れは、０．２～１．５μｍの厚さを有し、前記第１および第２のゲート領域のそれぞれは、０．１μｍまたはそれ以上の厚さを有する、請求項４１に記載のトランジスタ。

【請求項43】

前記バッファ層は、１ｘ１０$^{15}$～１ｘ１０$^{17}$ｃｍ$^{-3}$のドーパント濃度を有し、前記チャネル領域は、５ｘ１０$^{15}$～５ｘ１０$^{17}$ｃｍ$^{-3}$のドーパント濃度を有し、前記ソース、ソース／ドレイン、およびドレイン領域のそれぞれは、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有し、前記第１および第２のゲート領域のそれぞれは、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有する、請求項４１に記載のトランジスタ。

【請求項44】

前記基板は、半絶縁基板である、請求項４１に記載のトランジスタ。

【請求項45】

前記ソース／ドレインオーミックコンタクトと前記第２のゲート領域との間の電気接続をさらに備えている、請求項４１に記載のトランジスタ。

【請求項46】

前記ソースオーミックコンタクトと前記第２のゲート領域との間の電気接続をさらに備えている、請求項４１に記載のトランジスタ。

【請求項47】

前記ドレイン領域は、前記第２のゲート領域からラテラルに間隔を置かれ、前記第２のゲート領域と前記ドレイン領域との間の前記チャネル層にラテラルドリフト領域を形成している、請求項４１に記載のトランジスタ。

【請求項48】

前記ラテラルチャネルＪＦＥＴに対して、前記バッファ層、ドレイン領域、ソース／ドレイン領域、ソース領域、第１および第２のゲート領域、およびチャネル層のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項４１に記載のトランジスタ。

【請求項49】

前記ラテラルチャネルＪＦＥＴに対して、前記バッファ層、ドレイン領域、ソース／ドレイン領域、ソース領域、第１および第２のゲート領域、およびチャネル層のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項４８に記載のトランジスタ。

【請求項50】

ディスクリートラテラルチャネルＪＦＥＴを含む集積回路であって、

該ディスクリートラテラルチャネルＪＦＥＴは、

互いに対向する第１および第２の主要表面を有する基板と、

該基板の該第１の表面上の、ｐ型半導体材料のバッファ層と、

該バッファ層上のｎ型半導体材料のチャネル層と、

該チャネル層上で間隔を置いた関係にある、ｎ型半導体材料の隔たっているソースおよびドレイン領域と、

該ソース領域と該ドレイン領域との間の該チャネル層内で形成され、該チャネル層と整流ジャンクションを形成しているｐ型半導体材料のゲート領域と、

該ソース領域、該ゲート領域、および該ドレイン領域上のオーミックコンタクトと

を備えている、ディスクリートラテラルＪＦＥＴと、

ディスクリートバーチカルチャネルＪＦＥＴであって、

該ディスクリートバーチカルチャネルＪＦＥＴは、

互いに対向する第１および第２の主要表面を有するｎ型半導体材料の基板と、

該基板の該第１の主要表面上の、ｎ型半導体材料のドレイン層と、

該ドレイン層上のｎ型半導体材料のドリフト層であって、該ドリフト層は、該ドレイン層よりも低い導電性を有する、ドリフト層と、

該ドリフト層上のｎ型半導体材料のチャネル領域と該チャネル領域上のｎ型半導体のソ

ース領域とをそれぞれが含む１つ以上の隔たっている隆起した領域であって、該ソース領域の該材料は、該チャネル領域の導電性よりも高い導電性を有する、１つ以上の隔たっている隆起した領域と、

該１つ以上の隆起した領域と隣接し、該ドリフト層および該チャネル領域と整流ジャンクションを形成している、該ドリフト層上のｐ型半導体材料のゲート領域と、

該ゲートおよびソース領域上および、該基板の該第２の主要表面上のオーミックコンタクトと

を備えている、ディスクリートバーチカルチャネルＪＦＥＴと、

該ラテラルチャネルＪＦＥＴの該ソースオーミックコンタクトと該バーチカルチャネルＪＦＥＴの該ゲートオーミックコンタクトとの間の第１電気接続と、

該ラテラルチャネルＪＦＥＴの該ドレインオーミックコンタクトと該バーチカルチャネルＪＦＥＴの該ソースオーミックコンタクトとの間の第２電気接続と

を備えている、集積回路。

【請求項51】

前記ラテラルチャネルＪＦＥＴに対して、前記バッファ層は、少なくとも０．１μｍの厚さを有し、前記チャネル層は、０．３～１．５μｍの厚さを有し、前記ソース、ソース／ドレイン、およびドレイン領域のそれぞれは、０．２～１．５μｍの厚さを有し、前記第１および第２のゲート領域のそれぞれは、０．１μｍまたはそれ以上の厚さを有する、請求項５０に記載の集積回路。

【請求項52】

前記ラテラルチャネルＪＦＥＴに対して、前記バッファ層は、$1\times10^{15}$～$1\times10^{17}$ $cm^{-3}$のドーパント濃度を有し、前記チャネル層は、$5\times10^{15}$～$5\times10^{17}$ $cm^{-3}$のドーパント濃度を有し、前記ソース、ソース／ドレイン、およびドレイン領域のそれぞれは、$5\times10^{18}$ $cm^{-3}$よりも大きいドーパント濃度を有し、前記第１および第２のゲート領域のそれぞれは、$5\times10^{18}$ $cm^{-3}$よりも大きいドーパント濃度を有する、請求項５０に記載の集積回路。

【請求項53】

前記ラテラルチャネルＪＦＥＴに対して、前記基板は、半絶縁基板である、請求項５０に記載の集積回路。

【請求項54】

前記バーチカルチャネルＪＦＥＴに対して、前記ドレイン層は、０．５～１μｍの厚さを有し、前記ドリフト層は、５～３５０μｍの厚さを有し、前記チャネル領域は、０．２～１．５μｍの厚さを有し、前記ソース領域は、０．２～１．５μｍの厚さを有し、前記ゲート領域は、０．１μｍ以上の厚さを有する、請求項５０に記載の集積回路。

【請求項55】

前記バーチカルチャネルＪＦＥＴに対して：前記ドレイン層は、$5\times10^{18}$ $cm^{-3}$よりも大きいドーパント濃度を有し、前記ドリフト層は、$2\times10^{14}$～$2\times10^{16}$ $cm^{-3}$のドーパント濃度を有し、前記チャネル領域は、$5\times10^{15}$～$5\times10^{17}$ $cm^{-3}$のドーパント濃度を有し、前記ソース領域は、$5\times10^{18}$ $cm^{-3}$よりも大きいドーパント濃度を有し、前記ゲート領域は、$5\times10^{18}$ $cm^{-3}$よりも大きいドーパント濃度を有する、請求項５０に記載の集積回路。

【請求項56】

前記バーチカルチャネルＪＦＥＴに対して、前記基板は、$1\times10^{18}$ $cm^{-3}$よりも大きいドーパント濃度を有するｎ型基板である、請求項５０に記載の集積回路。

【請求項57】

前記ラテラルチャネルＪＦＥＴに対して、前記バッファ層、ドレイン領域、ソース領域、ゲート領域、およびチャネル層のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項５０に記載の集積回路。

【請求項58】

前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項５７に

記載の集積回路。
【請求項59】
前記バーチカルチャネルＪＦＥＴに対して、前記ドレイン層、ドリフト層、チャネル領域、ソース領域、およびゲート領域のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項５０に記載の集積回路。
【請求項60】
前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項５９に記載の集積回路。
【請求項61】
ラテラルジャンクション電界効果型トランジスタおよびバーチカルジャンクション電界効果型トランジスタを備えているモノリシック集積回路であって、
該ラテラルジャンクション電界効果型トランジスタは、
ドリフト層の第１の主要表面の部分に形成されるｐ型半導体材料のバッファ層と、
該バッファ層上にあり、該バッファ層と同一でない広がりを有するｎ型半導体材料のチャネル層であり、該バッファ層の部分は露出している、チャネル層と、
該チャネル層上で間隔を置いた関係にある、ｎ型半導体材料の隔たっているソース領域およびドレイン領域と、
該ソース領域と該ドレイン領域との間の該チャネル層内で形成され、該チャネル層と整流ジャンクションを形成しているｐ型半導体材料のゲート領域と、
該ソース領域、該ゲート領域、該ドレイン領域、および該バッファ層の該露出した部分上のオーミックコンタクトと
を備え、
該バーチカルジャンクション電界効果型トランジスタは、
該ドリフト層の該第１の主要表面上の、該バッファ層からラテラルに間隔を置かれたｎ型半導体材料のチャネル層と、
該チャネル層上で間隔を置いた関係にある、ｎ型半導体材料の１つ以上の隔たっているソース領域と、
該チャネル層に形成され、該１つ以上の隆起した領域と隣接し、該チャネル領域と整流ジャンクションを形成する、ｐ型半導体材料のゲート領域と、
該ゲートおよびソース領域上のオーミックコンタクトと
を備え、
該ドリフト層は、基板の第１の主要表面上にあるｎ型半導体材料のドレイン層上にあり、電気接続は、該基板の該第１の主要表面と互いに対向する該基板の第２の主要表面上にある
モノリシック集積回路。
【請求項62】
前記ドレイン層は、０．５～１μｍの厚さを有し、前記ドリフト層は、５～３５０μｍの厚さを有する、請求項６１に記載の集積回路。
【請求項63】
前記ドレイン層は、$5\times10^{18}cm^{-3}$よりも大きいドーパント濃度を有し、前記ドリフト層は、$2\times10^{14}$～$2\times10^{16}cm^{-3}$のドーパント濃度を有する、請求項６１に記載の集積回路。
【請求項64】
前記基板は、$1\times10^{18}cm^{-3}$よりも大きいドーパント濃度を有するｎ型基板である、請求項６１に記載の集積回路。
【請求項65】
前記ラテラルジャンクション電界効果型トランジスタに対して、前記チャネル領域は、０．２～１．５μｍの厚さを有し、前記ソースおよびドレイン領域のそれぞれは、０．２～１．５μｍの厚さを有し、前記ゲート領域およびバッファ層のそれぞれは、０．１μｍ以上の厚さを有する、請求項６１に記載の集積回路。

【請求項66】
前記ラテラルジャンクション電界効果型トランジスタに対して、前記チャネル領域は、５ｘ１０$^{15}$～５ｘ１０$^{17}$ｃｍ$^{-3}$のドーパント濃度を有し、前記ソース領域は、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有し、前記ゲート領域およびバッファ層のそれぞれは、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有する、請求項１に記載の集積回路。
【請求項67】
前記ラテラルチャネルＪＦＥＴの前記ソース接触と前記バーチカルチャネルＪＦＥＴの前記ゲート接触との間の第１の電気接続と、
前記ラテラルチャネルＪＦＥＴの前記ゲート層接触と前記バッファ層接触との間の第２の電気接続と、
前記ラテラルチャネルＪＦＥＴの前記ドレイン接触と前記バーチカルチャネルＪＦＥＴの前記ソース接触との間の第３の電気接続と
をさらに備えている請求項６１に記載の集積回路。
【請求項68】
前記ドリフト層に形成され前記ラテラルジャンクション電界効果型トランジスタの周りを囲む、１つ以上のｐ型半導体材料のリングをさらに備えている、請求項６１に記載の主席回路。
【請求項69】
前記ドリフト層に形成され前記バーチカルジャンクション電界効果型トランジスタの周りを囲む、１つ以上のｐ型半導体材料のリングをさらに備えている、請求項６１に記載の集積回路。
【請求項70】
前記ラテラルジャンクション電界効果型トランジスタに対して、前記バッファ層、ドレイン領域、ソース領域、ゲート領域、およびチャネル層のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項６１に記載の集積回路。
【請求項71】
前記ラテラルジャンクション電界効果型トランジスタに対して、前記バッファ層、ドレイン領域、ソース領域、ゲート領域、およびチャネル層のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項７０に記載の集積回路。
【請求項72】
前記バーチカルジャンクション電界効果型トランジスタに対して、前記チャネル層、ソース領域、およびゲート領域のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項６１に記載の集積回路。
【請求項73】
前記バーチカルジャンクション電界効果型トランジスタに対して、前記チャネル層、ソース領域、およびゲート領域のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項７２に記載の集積回路。
【請求項74】
前記ドリフト層および前記ドレイン層のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項６１に記載の集積回路。
【請求項75】
前記ドリフト層および前記ドレイン層のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩ属窒素化合物半導体材料である、請求項７４に記載の集積回路。
【請求項76】
ラテラルジャンクション電界効果型トランジスタおよびバーチカルジャンクション電界効果型トランジスタを備えているモノリシック集積回路であって、
該ラテラルジャンクション電界効果型トランジスタは、
ドリフト層の第１の主要表面の部分に形成されるｐ型半導体材料のバッファ層と、
該バッファ層上にあり、該バッファ層と同一でない広がりを有するｎ型半導体材料のチ

ャネル層であり、該バッファ層の部分は露出している、チャネル層と、
隔たっているソース領域およびドレイン領域であって、該ソース領域および該ドレイン領域のそれぞれは、該チャネル層上で間隔を置いた関係にあるｎ型半導体材料である、隔たっているソース領域およびドレイン領域と、
該ソース領域と該ドレイン領域との間の該チャネル層上の、該チャネル層と金属半導体整流ジャンクションを形成している金属層と、
該ソース領域、該ドレイン領域、および該バッファ層の該露出した部分上のオーミックコンタクトと
を備え、
該バーチカルジャンクション電界効果型トランジスタは、
該ドリフト層の該第１の主要表面上の、該バッファ層からラテラルに間隔を置かれた１つ以上の隆起した領域であって、該隆起した領域のそれぞれは、
該ドリフト層の該第１の主要表面上の、該ラテラルジャンクション電界効果型トランジスタの該バッファ層から間隔を置いたｎ型半導体材料のチャネル層と、
該チャネル領域上のｎ型半導体材料のソース領域と
を備える、隆起した領域と、
該ドリフト層上で該１つ以上の隆起した領域に隣接し、該ドリフト層および該チャネル領域と金属半導体整流ジャンクションを形成している金属層と、
該ソース領域上のオーミックコンタクトと
を備え、
該ドリフト層は、基板の第１の主要表面上にあるｎ型半導体材料の層上にあり、電気接続は、該基板の該第１の主要表面と互いに対向する該基板の第２の主要表面上にある、モノリシック集積回路。
【請求項77】
前記ドレイン層は、０．５～１μｍの厚さを有し、前記ドリフト層は、５～３５０μｍの厚さを有する、請求項７６に記載の集積回路。
【請求項78】
前記ドレイン層は、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有し、前記ドリフト層は、２ｘ１０$^{14}$～２ｘ１０$^{16}$ｃｍ$^{-3}$のドーパント濃度を有する、請求項７６に記載の集積回路。
【請求項79】
前記基板は、１ｘ１０$^{18}$ｃｍよりも大きいドーパント濃度を有するｎ型基板である、請求項７６に記載の集積回路。
【請求項80】
前記ラテラルジャンクション電界効果型トランジスタに対して、前記チャネル領域は、０．２～１．５μｍの厚さを有し、前記ソースおよびドレイン領域のそれぞれは、０．２～１．５μｍの厚さを有し、前記ゲート領域およびバッファ層のそれぞれは、０．１μｍ以上の厚さを有する、請求項７６に記載の集積回路。
【請求項81】
前記ラテラルジャンクション電界効果型トランジスタに対して、前記チャネル領域は、５ｘ１０$^{15}$～５ｘ１０$^{17}$ｃｍ$^{-3}$のドーパント濃度を有し、前記ソース領域は、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有し、前記ゲート領域およびバッファ層のそれぞれは、５ｘ１０$^{18}$ｃｍ$^{-3}$よりも大きいドーパント濃度を有する、請求項７６に記載の集積回路。
【請求項82】
前記ラテラルジャンクション電界効果型トランジスタの前記ソース接触と前記バーチカルジャンクション電界効果型トランジスタの前記金属層との間の第１の電気接続と、
前記ラテラルジャンクション電界効果型トランジスタの前記金属層と前記バッファ接触との間の第２の電気接続と、
前記ラテラルジャンクション電界効果型トランジスタの前記ドレイン接触と前記バーチ

カルジャンクション電界効果型トランジスタの前記ソース接触との間の第３の電気接続とをさらに備えている、請求項７６に記載の集積回路。

【請求項83】

前記ドリフト層に形成され前記ラテラルジャンクション電界効果型トランジスタ周りを囲む、１つ以上のｐ型半導体材料のリングをさらに備えている、請求項７６に記載の集積回路。

【請求項84】

前記ドリフト層に形成され前記バーチカルチャネルジャンクション電界効果型トランジスタの周りを囲む、１つ以上のｐ型半導体材料のリングをさらに備えている、請求項７６に記載の集積回路。

【請求項85】

前記ラテラルジャンクション電界効果型トランジスタに対して、前記バッファ層、ドレイン領域、ソース領域、ゲート領域、およびチャネル層のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項７６に記載の集積回路。

【請求項86】

前記ラテラルジャンクション電界効果型トランジスタに対して、前記バッファ層、ドレイン領域、ソース領域、ゲート領域、およびチャネル層のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項８５に記載の集積回路。

【請求項87】

前記バーチカルジャンクション電界効果型トランジスタに対して、前記チャネル層、ソース領域、およびゲート領域のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項７６に記載の集積回路。

【請求項88】

前記バーチカルジャンクション電界効果型トランジスタに対して、前記チャネル層、ソース領域、およびゲート領域のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩＩ属窒素化合物半導体材料である、請求項８７に記載の集積回路。

【請求項89】

前記ドリフト層および前記ドレイン層のそれぞれの前記半導体材料は、少なくとも２ｅＶの$E_G$を有する、請求項７６に記載の集積回路。

【請求項90】

前記ドリフト層および前記ドレイン層のそれぞれの前記半導体材料は、ＳｉＣまたはＩＩ属窒素化合物半導体材料である、請求項８９に記載の集積回路。

【発明の詳細な説明】

【技術分野】

【0001】

この出願は、２００４年７月８日出願の米国特許出願第６０／５８５，８８１号、および「Ｌａｔｅｒａｌ　Ｔｒｅｎｃｈ　Ｆｉｅｌｄ－Ｅｆｆｅｃｔ　Ｔｒａｎｓｉｓｔｏｒｓ　ｉｎ　Ｗｉｄｅ　Ｂａｎｄｇａｐ　Ｓｅｍｉｃｏｎｄｕｃｔｏｒ　Ｍａｔｅｒｉａｌｓ，　Ｍｅｔｈｏｄｓ　ｏｆ　Ｍａｋｉｎｇ，　Ａｎｄ　Ｉｎｔｅｇｒａｔｅｄ　Ｃｉｒｃｕｉｔｓ　Ｉｎｃｏｒｐｏｒａｔｉｎｇ　ｔｈｅ　Ｔｒａｎｓｉｓｔｏｒｓ」という名称の、２００４年１２月１日出願の米国特許出願第１０／９９９，９５４号に関する。上述の各出願は、その全体が本明細書中に参考として援用される。

【0002】

本発明は、概括的に電界効果型トランジスタ（ＦＥＴ）に関し、特にワイドバンドギャップ半導体材料で形成されたそのようなトランジスタに関する。さらに、本発明は、低電圧制御回路網を備えているモノリシックおよびハイブリッドな集積回路、および上記トランジスタを用いて組み立てられた電源スイッチに関する。

【背景技術】

【0003】

炭化珪素（ＳｉＣ）またはＩＩＩ属窒素化合物半導体（例えば、ガリウム窒素またはＧａＮ）のようなワイドバンドギャップ半導体材料（$E_G$＞２ｅＶという条件）は、高電力

、耐高温および／または耐放射線性の電子工学における使用にとって非常に魅力的である。シングルまたはマルチチップのワイドバンドギャップパワー半導体モジュール内へのパワートランジスタおよび制御回路網のモノリシックまたはハイブリッドな集積化は、システムの効率性および信頼性を向上させるためにそのようなアプリケーションに対して大変望ましい。

【0004】

ＳｉＣスマートパワー技術は、近年における議論の話題となっているが、限られた科学的調査しか行われていない。電源スイッチおよび制御回路網の両方の操作に関して提案される解決法に対しては、懐疑的な意見が出されている。

【0005】

材料の特性および処理技術の基本的な違いのせいで、相補型金属酸化物半導体（ＣＭＯＳ）または直接結合ＦＥＴロジック（ＤＣＦＬ）のような従来のＳｉまたはＧａＡｓ回路（ＩＣ）技術は、多くの場合においてワイドバンドギャップ半導体に簡単には移転され得ない。ＳｉＣ　ＮＭＯＳおよびＣＭＯＳのデジタルおよびアナログＩＣ製作に対するいくつかの試みが、過去１０年間に報告されてきた（例えば、非特許文献１［１］、非特許文献２［２］）。ＳｉＣを用いたモノリシックＣＭＯＳ集積デバイスおよび該デバイスの製作方法は、特許文献１［３］に開示される。さらに、ＳｉＣラテラルＤＭＯＳ電界効果型トランジスタ（ＬＤＭＯＳＦＥＴ）に対する最近の開発（例えば、特許文献２［４］、非特許文献３［５］）は、理論的には、スマートパワーエレクトロニクスにおける使用に対し、ＭＯＳＦＥＴベースの制御回路網および電源スイッチのモノリシック集積化を考慮している。しかし、様々な問題が、高温および／または大きな熱を寛容することが要求されるアプリケーションにおけるＭＯＳＦＥＴベースのＳｉＣ集積回路の使用を制限する。そのような最初の問題は、オン状態絶縁体の信頼性であって、$SiO_2$ に対するＳｉＣの伝導帯オフセットが、珪素の伝導帯オフセットと比較してはるかに小さいという結果による。この問題はさらに、高温および極度の放熱環境においてより重大になる。他の問題は、ＳｉＣ／$SiO_2$ 界面における高界面状態密度による低インバージョンチャネルモビリティ、および界面状態のイオン化による温度を伴った顕著な閾値電圧のシフトを含む。

【0006】

ＳｉＣスマートパワーエレクトロニクスで使用する別のトランジスタ候補であるＳｉＣバイポーラジャンクショントランジスタ（ＢＪＴ）もまた、低電流ゲインおよび高制御ロスを招く、エミッタとベースとの間の表面上の高再結合速度などの界面関連の問題から障害を受ける。

【0007】

ＳｉＣスマートパワーエレクトロニクスで使用する別のトランジスタ候補は、金属半導体電界効果型トランジスタ（ＭＥＳＦＥＴ）である。ＳｉＣ　ＭＥＳＦＥＴモノリシックマイクロ波集積回路（ＭＭＩＣ）は、最近１０年間に目覚しい発達を遂げたにもかかわらず（例えば、非特許文献４［６］）、ＳｉＣ　ＭＥＳＦＥＴロジックおよびアナログ回路を組み立てるための公表された試みは殆んどない（例えば、非特許文献５［７］）。

【0008】

ＭＯＳＦＥＴおよびＭＥＳＦＥＴによる取り組みの代替案は、（特許文献３［８］に開示されるｎ型およびｐ型チャネルの）相補型またはエンハンスト・デプレーション型（ｎ型チャネル）のいずれかで実装されるラテラルＪＦＥＴベースの集積回路の使用である。ＳｉＣ　ＪＦＥＴは、放熱に対して耐性があることが分かっており、温度に伴う閾値電圧シフトは極めて僅かであることを表している。高温常時オンパワーバーチカルジャンクション電界効果型トランジスタ（ＶＪＦＥＴ）の開発に関する有望な結果が、近年公表された（例えば、非特許文献［９］）。しかし、該トランジスタの優れた電流電導率および電圧ブロッキング能力にもかかわらず、これらのトランジスタの主要な欠点は、該トランジスタは「常時オン」デバイスであるということである。システムレベルにおいて、これはよく、追加の（負の）供給電圧および短絡回路保護を要求する。

【0009】

常時オフＳｉＣ高電圧ＶＪＦＥＴスイッチを作る数度の試みが、近年報告された。通常、これらのデバイスは、ラテラルおよびバーチカルの両方のチャネル領域を含む（例えば、特許文献４［１０］、特許文献５［１１」、特許文献６［１２］）。しかし、これらのデバイスは、デバイスブロッキング能力と固有オン抵抗との間で大きな矛盾を示す。例えば、７５μｍで７ｘ１０$^{14}$ｃｍ$^{-3}$のｎ型ドリフト領域を有するＶＪＦＥＴは、ゼロのゲートーソース間電圧で５．５ｋＶを超えるブロックが可能であった（非特許文献７［１３］）。同時に、このデバイスは、２００ｍΩ* ｃｍ$^{3}$より多い固有オン抵抗（$R_{sp-on}$）を表した。この厚さおよびドーピングから概算されるこのドリフト層の本来の抵抗は、６０ｍΩ* ｃｍ$^{3}$を僅かに超えるものであり、オン抵抗の残りは、チャネル領域の寄与によるものである。

【0010】

ＳｉＣ電力ＶＪＦＥＴの固有オン抵抗を減らすために、これらのデバイスは、高ポジティブゲートーソース間電圧を印加することによってバイポーラ型で駆動され得る。例えば、上述され、非特許文献７［１３］に開示されるデバイスは、５Ｖのゲートーソース間バイアスが印加されたときには、６６．７ｍΩ* ｃｍ$^{3}$の$R_{sp-on}$を表した（非特許文献８［１４］）。しかし、この取り組みは、高ゲート電流による重大な電力損失を導き得る。

【0011】

別の取り組みは、常時オンデバイスが常時オフ型で動作され得るように、常時オンデバイスを制御するための特別な回路および方法を用いることである。高電圧ＪＦＥＴを伴う低電圧制御ＪＦＥＴのカスコード接続は、制御ＪＦＥＴのドレインが高電圧デバイスのソースに接続され、高電圧ＪＦＥＴのゲートが制御ＪＦＥＴのソースに接続されているが、特許文献７［１５］に開示される。そのようなカスコード接続をモノリシックに実装するコンパウンド電界効果型トランジスタもまた、特許文献８［１６］に開示される。同類タイプのカスコード回路が、特許文献９［１７］に開示されており、それは、低電圧常時オフデバイスが、高電圧常時オンデバイスを制御する。より最近において、上記の構成のＳｉ　ＭＯＳＦＥＴによって制御される常時オンＳｉＣ　ＶＪＦＥＴが、いくつかのグループによって報告される（例えば、非特許文献９［１８］）。この集積電力スイッチは、優秀な電圧ブロッキングおよび電流伝導能力、および高スイッチングスピードを証明した。しかし、常時オンＳｉＣ　ＶＪＦＥＴにおける電力の制御のためのシリコンＭＯＳＦＥＴの使用は、カスコードの温度範囲および放熱に対する耐性の両方を著しく制限する。従って、一般的に、ワイドバンド常時オフ電源スイッチングデバイス、特にワイドバンドギャップ半導体内に組み立てられた制御回路網と一体化されたそのような電源スイッチに対するニーズが今もある。

【特許文献1】米国特許第６，３４４，６６３号明細書
【特許文献2】米国特許第５，７１０，４５５号明細書
【特許文献3】米国特許第６，５０３，７８２号明細書
【特許文献4】米国特許第６，６００，１９２号明細書
【特許文献5】米国特許第６，６９３，３２２号明細書
【特許文献6】米国特許出願公開第２００３／００８９９３０号明細書
【特許文献7】米国特許第３，７６７，９４６号明細書
【特許文献8】米国特許第４，１０７，７２５号明細書
【特許文献9】米国特許第４，６６３，５４７号明細書
【非特許文献1】W. Xieら、「Monolithic NMOS Digital Integrated Circuits in 6H-SiC」、IEEE Electron Device Letters、1994年11月11日、第15巻、第11号、p. 455-457
【非特許文献2】D. M. Brownら、「High temperature silicon carbide planar IC technology and first monolithic SiC operational amplifier

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【非特許文献4】S. T. Sheppardら、「High power hybrid and MMIC amplifiers using wide-bandgap semiconductor devices on semi-insulating SiC substrates」、Digest of 60th Device Research Conference、2002年6月24～26日、p. 175-178
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【非特許文献7】K. Asanoら、「5. 5kV normally-off low RonS 4H-SiC SEJFET」、Power Semiconductor Devices and ICs, 2001、ISPSD '01、Proceedings of the 13th International Symposium、2001年6月4～7日、p. 23-26
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【非特許文献9】P. Friedrichsら、「SiC power devices with low on-resistance for fast switching applications」、Power Semiconductor Devices and ICs, 2000、Proceedings of the 12th International Symposium、2000年5月22～25日、p. 213-216

【発明の開示】

【課題を解決するための手段】

【0012】

第1の実施形態によって、モノリシック集積回路が提供され、該モノリシック集積回路は、

互いに対向する第1および第2の主要表面を有する基板と、

該基板上の該第1の主要表面上の隔たっている位置にある第1および第2のジャンクション電界効果型トランジスタと

を備えている、モノリシック集積回路であって、

該第1および第2のジャンクション電界効果型トランジスタのそれぞれは、

該基板の第1の主要表面上にあり、該基板の第1の主要表面と同一でない広がりを有す

るｎ型半導体材料のドレイン層であって、該ドレイン層を囲む該基板の部分は露出している、ドレイン層と、
該ドレイン層上にあり、該基板の第１の主要表面と同一でない広がりを有するｎ型半導体材料のドリフト層であって、該ドレイン層の部分は露出しており、該ドリフト層は、該ドレイン層よりも低い導電性を有する、ドリフト層と、
該ドリフト層上の隔たっている位置上にある１つ以上の隆起した領域であって、該１つ以上の隆起した領域のそれぞれは、該ドリフト層上のｎ型半導体材料のチャネル領域と該チャネル領域上のｎ型半導体のソース領域とを含み、該ソース領域の該半導体材料は、該チャネル層の導電性よりも高い導電性を有する、１つ以上の隆起した領域と、
該１つ以上の隆起した領域と隣接し、該ドリフト層および該チャネル領域のｎ型材料と整流ジャンクションを形成している、該ドリフト層上のｐ型半導体材料のゲート領域と、
該ゲート領域および該ソース領域上および該ドレイン層の露出した部分上のオーミックコンタクトと、
該第１のジャンクション電界効果型トランジスタの該ソースのオーミックコンタクトと、該第２のジャンクション電界効果型トランジスタの該ゲートのオーミックコンタクトとの間の第１の電気接続と、
該第１のジャンクション電界効果型トランジスタの該ドレインのオーミックコンタクトと、第２のジャンクション電界効果型トランジスタの該ソースのオーミックコンタクトとの間の第２の電気接続と
を備えている、モノリシック集積回路。
【0013】
第２の実施形態によって、モノリシック集積回路が提供され、該モノリシック集積回路は、
互いに対向する第１および第２の主要表面を有する基板と、
該基板上の該第１の主要表面上にあるｐ型半導体材料のバッファ層と、
ｎ型半導体材料のそれぞれが該バッファ層上で間隔を置いた関係にある、第１および第２の隔たっているチャネル領域であって、該第２のチャネル領域は、該バッファ層上のベース部分と上側部分とを含み、該ベース部分は、肩部を形成するように該上側部分を越えてラテラルに広がる、第１および第２の隔たっているチャネル領域と、
該第１のチャネル領域と隣接し、該第１のチャネル領域と接触する、該バッファ層上のｎ型半導体材料のソース領域と、
該第１のチャネル領域と該第２のチャネル領域との間の該バッファ層上の、該第１のチャネル領域および該第２のチャネル領域の両方と接触する、ｎ型半導体材料のソース／ドレイン領域であって、該ソース／ドレイン領域の一部は、該第２のチャネル領域の肩部部分とオーバーラップしている、ソース／ドレイン領域と、
ドレイン領域であって、該ドレイン領域は、該バッファ層と直接的に接触しないように、該第２のチャネル領域の該肩部の上にある、ドレイン領域と、
該第１のチャネル領域上の、該第１のチャネル領域と整流ジャンクションを形成しているｐ型半導体材料の第１のゲート領域と、
該第２のチャネル領域のトップ部分の上側の表面上の、該第２のチャネル領域と整流ジャンクションを形成しているｐ型半導体材料の第２のゲート領域と、
該ソース領域、該第１および第２のゲート領域、該ソース／ドレイン領域、および該ドレイン領域上のオーミックコンタクトと
を備えている、モノリシック集積回路。
【0014】
第３の実施形態によって、集積回路が提供され、該集積回路は、
第１のバーチカルチャネルＪＦＥＴを含む集積回路であって、
該第１のバーチカルチャネルＪＦＥＴは、
互いに対向する第１および第２の表面を有する基板と、
該基板の該第１の表面上の、ｎ型半導体材料のドレイン層と、

前記ドレイン層上にあり、該ドレイン層と同一でない広がりを有するｎ型半導体材料のドリフト層であり、該ドレイン層の部分は露出しており、該ドリフト層は、該ドレイン層よりも低い導電性を有する、ドリフト層と、
該ドリフト層上のｎ型半導体材料のチャネル領域と該チャネル領域上のｎ型半導体のソース領域とを含む１つ以上の隆起した領域であって、該ソース領域の該材料は、該チャネル領域の導電性よりも高い導電性を有する、１つ以上の隆起した領域と、
該１つ以上の隆起した領域と隣接し、該ドリフト層および該チャネル領域と整流ジャンクションを形成する、該ドリフト層上のｐ型半導体材料のゲート領域と、
該ゲート領域および該ソース領域上および該ドレイン層の露出した部分上のオーミックコンタクトと
を備えている、第１のバーチカルチャネルＪＦＥＴと、
該第１のバーチカルチャネルＪＦＥＴから隔たっている第２のバーチカルチャネルＪＦＥＴであって、
該第２のバーチカルチャネルＪＦＥＴは、
互いに対向する第１および第２の主要表面を有するｎ型半導体材料の基板と、
該基板の該第１の主要表面上のｎ型半導体材料のドレイン層と、
該ドレイン層上のｎ型半導体材料のドリフト層であって、該ドリフト層は、該ドレイン層よりも低い導電性を有する、ドリフト層と、
該ドリフト層上のｎ型半導体材料のチャネル領域と該チャネル領域上のｎ型半導体のソース領域とを含む１つ以上の隆起した領域であって、該ソース領域の該材料は、該チャネル領域の導電性よりも高い導電性を有する、１つ以上の隆起した領域と、
該１つ以上の隆起した領域と隣接し、該ドリフト層および該チャネル領域と整流ジャンクションを形成する、該ドリフト層上のｐ型半導体材料のゲート領域と、
該ゲートおよびソース領域上および該基板の該第２の主要表面上のオーミックコンタクトと
を備えている、第２のバーチカルチャネルＪＦＥＴと、
該第１のバーチカルチャネルＪＦＥＴの該ドレインオーミックコンタクトと該第２のバーチカルチャネルＪＦＥＴの該ソースオーミックコンタクトとの間の第１の電気接続と、
該第１のバーチカルチャネルＪＦＥＴの該ソースオーミックコンタクトと該第２のバーチカルチャネルＪＦＥＴの該ゲートオーミックコンタクトとの間の第２の電気接続と
を備えている、集積回路。

【0015】

第４の実施形態によって、集積回路が提供され、該集積回路は、
ディスクリートラテラルチャネルＪＦＥＴであって、
該ディスクリートラテラルチャネルＪＦＥＴは、
互いに対向する第１および第２の主要表面を有する基板と、
該基板の該第１の主要表面上の、ｐ型半導体材料のバッファ層と、
それぞれが該バッファ層上で間隔を置いた関係にあるｎ型半導体材料の、ディスクリートソースおよびドレイン領域と、
該ソースおよびドレイン領域の間の該バッファ層上の、該ソースおよびドレイン領域のそれぞれと接触する、ｎ型半導体材料のチャネル領域と、
該チャネル領域上の、該チャネル領域と整流ジャンクションを形成しているｐ型半導体材料のゲート領域と、
該ソース、ゲート、およびドレイン領域上のオーミックコンタクトと
を備えている、ディスクリートラテラルチャネルＪＦＥＴと、
ディスクリートバーチカルチャネルＪＦＥＴであって、
該ディスクリートバーチカルチャネルＪＦＥＴは、
互いに対向する第１および第２の主要表面を有するｎ型半導体材料の基板と、
該基板の該第１の主要表面上の、ｎ型半導体材料のドレイン層と、
該ドレイン層上のｎ型半導体材料のドリフト層であって、該ドリフト層は、該ドレイン

層よりも低い導電性を有する、ドリフト層と、
該ドリフト層上のｎ型半導体材料のチャネル領域と該チャネル領域上のｎ型半導体のソース領域とをそれぞれが含む１つ以上の隔たっている隆起した領域であって、該ソース領域の該材料は、該チャネル領域の導電性よりも高い導電性を有する、１つ以上の隔たっている隆起した領域と、
該１つ以上の隆起した領域と隣接し、該ドリフト層および該チャネル領域と整流ジャンクションを形成している、該ドリフト層上のｐ型半導体材料のゲート領域と、
該ゲートおよびソース領域上、および該基板の該第２の主要表面上のオーミックコンタクトと
を備えている、ディスクリートバーチカルチャネルＪＦＥＴと、
該ラテラルチャネルＪＦＥＴの該ドレインオーミックコンタクトと該バーチカルチャネルＪＦＥＴの該ソースオーミックコンタクトとの間の第１電気接続と、
該ラテラルチャネルＪＦＥＴの該ソースオーミックコンタクトと該バーチカルチャネルＪＦＥＴの該ゲートオーミックコンタクトとの間の第２電気接続と
を備えている、集積回路。
【0016】
第５の実施形態によって、モノリシックラテラルチャネルジャンクション電界効果型トランジスタ（ＪＦＥＴ）が提供され、該モノリシックラテラルジャンクション電界効果型トランジスタは、
互いに対向する第１および第２の主要表面を有する基板と、
該基板の該第１の主要表面上の、ｐ型半導体材料のバッファ層と、
該バッファ層上のｎ型半導体材料のチャネル層と、
該チャネル層上で間隔を置いた関係にある、ｎ型半導体材料の隔たっている該ソース領域および該ドレイン領域と、
該ソース領域と該ドレイン領域との間の該チャネル層上の、該ソース領域および該ドレイン領域のそれぞれから間隔を置いたｎ型半導体材料のソース／ドレイン領域と、
該ソース領域と該ソース／ドレイン領域との間の該チャネル層内で形成され、該チャネル層と整流ジャンクションを形成しているｐ型半導体材料の第１ゲート領域と、
該ソース／ドレイン領域と該ドレイン領域との間の該チャネル層内で形成され、該チャネル層と整流ジャンクションを形成しているｐ型半導体材料の第２のゲート領域と、
該ソース領域、該第１および第２のゲート領域、該ソース／ドレイン領域、および該ドレイン領域上のオーミックコンタクトと
を備えている、モノリシックラテラルチャネルジャンクション電界効果型トランジスタ（ＪＦＥＴ）。
【0017】
第６の実施形態によって、集積回路が提供され、該集積回路は、
ディスクリートラテラルチャネルＪＦＥＴを含む集積回路であって、
該ディスクリートラテラルチャネルＪＦＥＴは、
互いに対向する第１および第２の主要表面を有する基板と、
該基板の該第１の表面上の、ｐ型半導体材料のバッファ層と、
該バッファ層上のｎ型半導体材料のチャネル層と、
該チャネル層上で間隔を置いた関係にある、ｎ型半導体材料の隔たっているソースおよびドレイン領域と、
該ソース領域と該ドレイン領域との間の該チャネル層内で形成され、該チャネル層と整流ジャンクションを形成しているｐ型半導体材料のゲート領域と、
該ソース領域、該ゲート領域、および該ドレイン領域上のオーミックコンタクトと
を備えている、ディスクリートラテラルＪＦＥＴと、
ディスクリートバーチカルチャネルＪＦＥＴであって、
該ディスクリートバーチカルチャネルＪＦＥＴは、
互いに対向する第１および第２の主要表面を有するｎ型半導体材料の基板と、

該基板の該第１の主要表面上の、ｎ型半導体材料のドレイン層と、
該ドレイン層上のｎ型半導体材料のドリフト層であって、該ドリフト層は、該ドレイン層よりも低い導電性を有する、ドリフト層と、
該ドリフト層上のｎ型半導体材料のチャネル領域と該チャネル領域上のｎ型半導体のソース領域とをそれぞれが含む１つ以上の隔たっている隆起した領域であって、該ソース領域の該材料は、該チャネル領域の導電性よりも高い導電性を有する、１つ以上の隔たっている隆起した領域と、
該１つ以上の隆起した領域と隣接し、該ドリフト層および該チャネル領域と整流ジャンクションを形成している、該ドリフト層上のｐ型半導体材料のゲート領域と、
該ゲートおよびソース領域上および、該基板の該第２の主要表面上のオーミックコンタクトと
を備えている、ディスクリートバーチカルチャネルＪＦＥＴと、
該ラテラルチャネルＪＦＥＴの該ソースオーミックコンタクトと該バーチカルチャネルＪＦＥＴの該ゲートオーミックコンタクトとの間の第１電気接続と、
該ラテラルチャネルＪＦＥＴの該ドレインオーミックコンタクトと該バーチカルチャネルＪＦＥＴの該ソースオーミックコンタクトとの間の第２電気接続と
を備えている、集積回路。
【0018】
第７の実施形態によって、ラテラルジャンクション電界効果型トランジスタおよびバーチカルジャンクション電界効果型トランジスタを備えるモノリシック集積回路が提供され、
ラテラルジャンクション電界効果型トランジスタおよびバーチカルジャンクション電界効果型トランジスタを備えているモノリシック集積回路であって、
該ラテラルジャンクション電界効果型トランジスタは、
ドリフト層の第１の主要表面の部分に形成されるｐ型半導体材料のバッファ層と、
該バッファ層上にあり、該バッファ層と同一でない広がりを有するｎ型半導体材料のチャネル層であり、該バッファ層の部分は露出している、チャネル層と、
該チャネル層上で間隔を置いた関係にある、ｎ型半導体材料の隔たっているソース領域およびドレイン領域と、
該ソース領域と該ドレイン領域との間の該チャネル層内で形成され、該チャネル層と整流ジャンクションを形成しているｐ型半導体材料のゲート領域と、
該ソース領域、該ゲート領域、該ドレイン領域、および該バッファ層の該露出した部分上のオーミックコンタクトと
を備え、
該バーチカルジャンクション電界効果型トランジスタは、
該ドリフト層の該第１の主要表面上の、該バッファ層からラテラルに間隔を置かれたｎ型半導体材料のチャネル層と、
該チャネル層上で間隔を置いた関係にある、ｎ型半導体材料の１つ以上の隔たっているソース領域と、
該チャネル層に形成され、該１つ以上の隆起した領域と隣接し、該チャネル領域と整流ジャンクションを形成する、ｐ型半導体材料のゲート領域と、
該ゲートおよびソース領域上のオーミックコンタクトと
を備え、
該ドリフト層は、基板の第１の主要表面上にあるｎ型半導体材料のドレイン層上にあり、電気接続は、該基板の該第１の主要表面と互いに対向する該基板の第２の主要表面上にある
モノリシック集積回路。
【0019】
第８の実施形態によって、ラテラルジャンクション電界効果型トランジスタおよびバーチカルジャンクション電界効果型トランジスタを備えるモノリシック集積回路が提供され

ラテラルジャンクション電界効果型トランジスタおよびバーチカルジャンクション電界効果型トランジスタを備えているモノリシック集積回路であって、
該ラテラルジャンクション電界効果型トランジスタは、
ドリフト層の第１の主要表面の部分に形成されるｐ型半導体材料のバッファ層と、
該バッファ層上にあり、該バッファ層と同一でない広がりを有するｎ型半導体材料のチャネル層であり、該バッファ層の部分は露出している、チャネル層と、
隔たっているソース領域およびドレイン領域であって、該ソース領域および該ドレイン領域のそれぞれは、該チャネル層上で間隔を置いた関係にあるｎ型半導体材料である、隔たっているソース領域およびドレイン領域と、
該ソース領域と該ドレイン領域との間の該チャネル層上の、該チャネル層と金属半導体整流ジャンクションを形成している金属層と、
該ソース領域、該ドレイン領域、および該バッファ層の該露出した部分上のオーミックコンタクトと
を備え、
該バーチカルジャンクション電界効果型トランジスタは、
該ドリフト層の該第１の主要表面上の、該バッファ層からラテラルに間隔を置かれた１つ以上の隆起した領域であって、該隆起した領域のそれぞれは、
該ドリフト層の該第１の主要表面上の、該ラテラルジャンクション電界効果型トランジスタの該バッファ層から間隔を置いたｎ型半導体材料のチャネル層と、
該チャネル領域上のｎ型半導体材料のソース領域と
を備える、隆起した領域と、
該ドリフト層上で該１つ以上の隆起した領域に隣接し、該ドリフト層および該チャネル領域と金属半導体整流ジャンクションを形成している金属層と、
該ソース領域上のオーミックコンタクトと
を備え、
該ドリフト層は、基板の第１の主要表面上にあるｎ型半導体材料の層上にあり、電気接続は、該基板の該第１の主要表面と互いに対向する該基板の第２の主要表面上にある、モノリシック集積回路。

【発明を実施するための最良の形態】

【0020】

本発明は、付随する図面および写真を参照しながら、これよりさらに詳細に記述され、本発明の好ましい実施形態は、実施例として炭化珪素（ＳｉＣ）半導体を用いて記述される。

【0021】

炭化珪素は非常に多くの（すなわち２００よりも多い）異なる変形（ポリタイプ）で結晶する。最重要なことは、３Ｃ－ＳｉＣ（立方単位格子、閃亜鉛鉱型）、２Ｈ－ＳｉＣ、４Ｈ－ＳｉＣ、６Ｈ－ＳｉＣ（六角形単位格子、ウルツ鉱型）、１５Ｒ－ＳｉＣ（斜方六面体単位格子）である。４Ｈポリタイプは、電源デバイスにとってより魅力的であるが、それは、そのより高い電子移動度による。４Ｈ－ＳｉＣがより好まれるのだが、本発明は、例として、ガリウム窒化物および炭化珪素の他のポリタイプなどの他のワイドバンドギャップ半導体材料（Ｗｉｄｅ　ｂａｎｄｇａｐ　ｓｅｍｉｃｏｎｄｕｃｔｏｒ　ｍａｔｅｒｉａｌｓ）から作られる、本明細書中に記述されるデバイスおよび集積回路に適応可能であることが理解される。

【0022】

図１は、ラテラルトレンチジャンクション電界効果型トランジスタ（Ｌａｔｅｒａｌ　Ｔｒｅｎｃｈ　Ｊｕｎｃｔｉｏｎ　Ｆｉｅｌｄ－Ｅｆｆｅｃｔ　Ｔｒａｎｓｉｓｔｏｒｓ）（ＬＴＪＦＥＴ）と呼ばれる、エンハンスト・デプレーション型の半導体デバイス（ｅｎｈａｎｃｅｄ　ａｎｄ　ｄｅｐｌｅｔｉｏｎ　ｍｏｄｅ　ｓｅｍｉｃｏｎｄｕｃｔｏｒ　ｄｅｖｉｃｅｓ）の概略断面図、およびモノリシックインバータ回路を形成するために

用いられる電気的接続の該略図を示す。示されるように、インバータを形成するために用いられるデバイスは、ワイドバンドギャップ半導体材料基板上（１）に築かれ、該基板は、半絶縁、ｐ型、またはｐ型バッファ層を伴うｎ型のいずれかであり得る。図１に示されるように、デバイスは、ドレイン（３）、ドリフト（４）、チャネル（５）およびソース（６）のエピタキシャルに成長したｎ型、およびｐ型のインプラントゲート領域（７）を備えている。デバイス構造は、プラズマエッチングおよびイオン注入を用いて規定され得る。図１に示される回路において、ソース、ゲート、およびドレイン領域に対するオーミックコンタクトは、ウェーハの同一側に形成され得、該デバイスがモノリシック集積回路で用いられることを可能にする。上述され図１に示されるデバイスの完全な記述およびこのデバイスに対する例示的な製作方法は、本明細書と同日に出願された、「Ｌａｔｅｒａｌ Ｔｒｅｎｃｈ Ｆｉｅｌｄ－Ｅｆｆｅｃｔ Ｔｒａｎｓｉｓｔｏｒｓ ｉｎ Ｗｉｄｅ Ｂａｎｄｇａｐ Ｓｅｍｉｃｏｎｄｕｃｔｏｒ Ｍａｔｅｒｉａｌｓ，ｍｅｔｈｏｄｓ ｏｆ Ｍａｋｉｎｇ，ａｎｄ Ｉｎｔｅｇｒａｔｅｄ Ｃｉｒｃｕｉｔｓ Ｉｎｃｏｒｐｏｒａｔｉｎｇ ｔｈｅ Ｔｒａｎｓｉｓｔｏｒｓ」と題する、米国特許出願第１０／９９９，９５４号に見られ、該出願は、その全体が本明細書中に参考として援用される。

【0023】

図２は、シングルフィンガー（ｓｉｎｇｌｅ－ｆｉｎｇｅｒ）エンハンストメント・デプレーション型ＬＴＪＦＥＴを含み、かつビルトインＰｉＮダイオードを有する、モノリシック常時オフＪＦＥＴの概略図である。電気的接続の概略図も、図２に示される。図２に示されるように、該デバイスは、カスコード型の構成で接続されており、それによってエンハンストメント型トランジスタ（「ＥＪＦＥＴ」と参照される）のドレインが、デプレーション型トランジスタ（「ＤＪＦＥＴ」と参照される）のソースに接続され、ＤＪＦＥＴのゲートが、制御ＥＪＦＥＴのソースと接続される。このデバイスのＤＪＦＥＴのゲート領域（７）とドリフト層（４）との間に形成されるｐ－ｎジャンクション部は、アンチパラレルフリーホイーリングＰｉＮダイオードと呼ばれるものを形成する。このダイオードの大きさは、インプラントゲート領域の幅によって規定され得る。

【0024】

図２は、常時オフＪＦＥＴのシングルフィンガーデバイスの実装を示すが、実際はマルチフィンガーＬＴＪＦＥＴが用いられ得、電源スイッチを形成する。図３Ａおよび３Ｂは、モノリシックマルチフィンガー常時オフ電源スイッチの概略的な回路図（図３Ａ）および例示的なレイアウト設計（図３Ｂ）を示す。

【0025】

スイッチによる損失を減らすために、図３Ａおよび図３Ｂに示されるＰｉＮダイオードは、ショットキーバリアダイオード（ＳＢＤ）またはジャンクションバリアショットキー（ＪＢＳ）ダイオードと取り替えられ得る。トレンチ構造にショットキーゲートを形成する方法は、２００４年７月８日に出願された、米国特許出願第６０／５８５，８８１号に開示されており、その全体が本明細書中に参考として援用される。図４は、集積フリーホイーリングＳＢＤまたはＪＢＳダイオードを有するモノリシック常時オフＪＦＥＴ電源スイッチの概略断面図を提供し、図５Ａおよび図５Ｂは、マルチフィンガーＬＴＪＦＥＴを用いてモノリシックに形成されるそのようなスイッチの概略的な回路図（図５Ａ）および例示的なレイアウト設計（図５Ｂ）を提供する。

【0026】

図６および図７は、シングルフィンガー常時オフＪＦＥＴ電源スイッチの概略断面図であり、図中では、エンハンスメントモード低電圧ＬＴＪＦＥＴが、高電圧ディスクリート常時オンデプレーション型ＶＪＦＥＴを制御する。図６は、ビルトインアンチパラレルＰｉＮダイオードを有するハイブリッドＪＦＥＴ電源スイッチを示し、図７は、高電圧ＶＪＦＥＴとモノリシックに集積したアンチパラレルＳＢＤまたはＪＢＳダイオードを備えているＪＦＥＴ電源スイッチを示す。

【0027】

上述された技術の例示的な実装が、図８に示される。図８に示されるように、モノリシックＬＴＪＦＥＴタイマー回路は、ディスクリート高電圧常時オン電源ＶＪＦＥＴとカスコードで接続されるビルトオンチップ低電圧高電流エンハンストメント型ＬＴＪＦＥＴを駆動する。

【0028】

該ＬＴＪＦＥＴの低い固有オン抵抗およびワイドバンドギャップ半導体に共通するトラッピング効果が無いので、高電圧適用においては、バーチカルチャネルマルチフィンガーＬＴＪＦＥＴが好ましいが、代替的なＪＦＥＴ構造（例えば、ラテラルチャネルを有するもの）もまた、常時オフ電源ＪＦＥＴスイッチを形成するために用いられ得る。図９～図１７は、エンハンストメント・デプレーション型ラテラルトレンチジャンクション電界効果型トランジスタ（ＬＪＦＥＴ）を用いて組み立てられた集積ＪＦＥＴスイッチの様々な例示的実施形態を例証する。

【0029】

図９は、エピタキシャルに過剰成長したゲートを有するエンハンストメント・デプレーション型ＬＪＦＥＴを含むラテラルチャネルＪＦＥＴ集積回路の電気的な接続の概略断面図である。図９に示されるように、集積回路は、モノリシックインバータ回路を形成する。インバータを形成するために用いられるＬＪＦＥＴは、ワイドバンドギャップ半導体基板（１）上に組み立てられ、該基板は、半絶縁、ｐ型、またはｐ型バッファ層を有するｎ型のいずれかであり得る。図９に示されるように、集積回路は、バッファ（２）およびチャネル（５ａ）のエピタキシャルに成長したｎ型層、ならびにインプラントされたソースおよびドレイン（６ａ）領域、およびエピタキシャルに成長したｐ型ゲート領域（７ａ）を備えている。デバイス構造は、プラズマエッチおよびイオン注入を用いて規定され得る。ソース、ゲートおよびドレイン領域に対するオーミックコンタクト（８）は、ウェーハの同一側に形成され得、モノリシック集積回路における該デバイスの使用を考慮している。

【0030】

図１０は、過剰成長したゲート領域を有するエンハンストメント・デプレーション型ＬＪＦＥＴを用いて組み立てられる、モノリシック常時オフＪＦＥＴ電源スイッチのピッチの該略図である。電気的な接続の該略図から分かり得るように、該デバイスは、カスコード型の構成で接続されており、それによって低電圧エンハンストメント型ＬＪＦＥＴ（「ＥＬＪＦＥＴ」と参照される）が、高電圧デプレーション型トランジスタ（「ＤＬＪＦＥＴ」と参照される）のソースに接続され、ＤＬＪＦＥＴのゲートが、制御ＥＬＪＦＥＴのソースと接続される。

【0031】

図１１は、ハイブリッド常時オフＪＦＥＴ電源スイッチの概略断面図を示し、図中において、低電圧ＥＬＪＦＥＴは、高電圧ディスクリート常時オンデプレーション型ＶＪＦＥＴを制御する。

【0032】

ソースおよびドレイン領域が、エピタキシャルに成長したｎ型層およびゲート領域に形成される、そのような代替的ＬＪＦＥＴ構造もまた、用いられ得る。このタイプのデバイスは、図１２から図１７に示される。

【0033】

図１２は、エンハンストメント・デプレーション型インプラントゲートＬＪＦＥＴを含むモノリシックインバータ回路の電気的な接続の概略断面図を示す。示されるように、インバータを形成するために用いられるデバイスは、ワイドバンドギャップ半導体基板（１）上に組み立てられ、該基板は、半絶縁、ｐ型、またはｐ型バッファ層を有するｎ型のいずれかであり得る。さらに示されるように、該デバイスは、バッファ（２）、チャネル（５ｂ）、ソースおよびドレイン（６）のエピタキシャルに成長したｎ型層、ならびにインプラントゲート（７）領域を含む。

【0034】

図１３は、エンハンストメント・デプレーション型インプラントゲートＬＪＦＥＴを用いて組み立てられたモノリシック常時オフＪＦＥＴ電源スイッチのピッチの概略断面図である。図１３に示されるように、ＤモードＬＪＦＥＴのドレインは、チャネル層（５ｂ）上のゲートからラテラルに間隔を置き、該デバイスの中でラテラルドリフト領域を形成する。

【0035】

図１４は、常時オフＪＦＥＴ電源スイッチの概略断面図であり、図中において、エンハンスメント型低電圧インプラントゲートＬＪＦＥＴが、高電圧ディスクリート常時オンデプレーション型ＶＪＦＥＴを制御する。

【0036】

図１５は、モノリシック常時オフＪＦＥＴ電源スイッチの概略断面図であり、図中において、エンハンストメント型低電圧デュアルゲートＬＪＦＥＴが、高電圧ディスクリート常時オンデプレーション型ＶＪＦＥＴを制御する。図１５に示されるように、ＬＪＦＥＴの底部ゲートは、チャネル領域がドリフト領域（４）上に成長する前に、該領域にインプラントされる。

【0037】

図１６は、図３Ｄに示されるデバイスの概略断面図であり、図中において、ＬＪＦＥＴの底部ゲートは、ガードリングとともにドリフト領域４にインプラントされる。ガードリングは、スイッチの電圧遮断能力を増すために用いられ得る。

【0038】

インプラントｐ型ゲートを有するＦＥＴデバイスが上述されているが、ショットキーゲートもまた、常時オフＦＥＴ電源スイッチの製作に用いられ得る。図１７は、図１６に示されるように、デバイスの概略断面図であり、図中において、ＬＪＦＥＴのインプラントｐ型上部ゲートおよびディスクリート常時オンデプレーション型ＶＪＦＥＴのインプラントゲートは、ショットキーゲートと置き換えられる。示されるように、ディスクリート常時オンＦＥＴのショットキーゲートは、集積アンチパラレルフリーホイーリングダイオードとしても適する。

【0039】

図１８Ａから図１８Ｄは、模擬のデバイス構造（図１８Ａ）、概略断面図（図１８Ｂ）およびＳｉＣ　ＬＴＪＦＥＴ集積スイッチの出力ＤＣ特性を示すグラフ（図１８Ｃおよび図１８Ｄ）であり、ＥＪＦＥＴおよびＤＪＦＥＴの両方は、１ｃｍのチャネル外周を有する。

【0040】

上述されたカスコード型電源スイッチの可能性の立証を行うために、該スイッチのハイブリッドの実施形態が、ディスクリートノンターミネートエンハンストメント・デプレーション型バーチカルＪＦＥＴを用いて構築された。図１９Ａから図１９Ｄは、写真（図１９Ａ）、該略図（図１９Ｂ）およびハイブリッド常時オフ９００Ｖ電源スイッチの計測特性を示すグラフ（図１９Ｃおよび図１９Ｄ）である。図１９Ｃおよび図１９Ｄから分かり得るように、デプレーション型デバイスによって誘導される比較的高い漏れ電流（$I_D$＝３３０μＡ@$V_{DS}$＝９００Ｖおよび$V_{GS}$＝０Ｖ）にもかかわらず、電圧制御ＳｉＣ電源スイッチは、わずか２．７５Ｖで制御された。

【0041】

該スイッチの基本的な機能は、以下に記述され得る。ＨＩＧＨの制御レベルにおいて（例えば$V_{GS}$＝２．７５Ｖ）、エンハンストモードトランジスタ（ＥＪＦＥＴ）が点けられる（ｔｕｒｎｅｄ　ｏｎ）。デプレーション型トランジスタ（ＤＪＦＥＴ）のゲートとソースの間では、僅かな電圧降下しか起きず、従ってＤＪＦＥＴもまた点いている。ＥＪＦＥＴがＬＯＷの制御レベル（$V_{GS}$＝０．２５Ｖ）で消される場合には、そのドレインからソースへの電圧は、図２０Ｂに示されるように、４０～５０Ｖに増える。この電圧は、ＤＪＦＥＴをピンチオフする。

【0042】

集積スイッチの固有オン抵抗は、以下のように最小化され得る。第１に、ピンチオフ電圧の比率および両方のトランジスタ（例えばＥＪＦＥＴおよびＤＪＦＥＴ）のチャネル周囲は、調整され得、その結果として、該両方のトランジスタは、おおよそ等しいオン抵抗を有し、それゆえにどちらのトランジスタも全体的な電流を制限しない。第２に、デバイスは、ＤＪＦＥＴのゲートからソースへの破壊電圧（ｂｒｅａｋｄｏｗｎ　ｖｏｌｔａｇｅ）が、ＥＪＦＥＴのドレインからソースへの破壊電圧と同一またはそれよりも高くなるように構成され得る。

【0043】

さらに、高電流マルチフィンガーＬＴＪＦＥＴの指の長さは、縮小され得、変更できる（ａｌｔｅｒａｌ）ドレイン領域の抵抗を、バーチカル$n^+$基板の抵抗と適合性を持たせた状態にする。図２１Ａおよび図２１Ｂは、ＬＴＪＦＥＴ（図２１Ａ）およびＶＪＦＥＴ（図２１Ｂ）の分散ドレイン抵抗の該略図、および、ラテラルドレイン層の異なるドーピングに対する指の長さの関数として、ＶＪＦＥＴのバーチカルドレインの抵抗に対して正規化されたＬＴＪＦＥＴのラテラルドレイン層の抵抗を示すグラフ（図２１Ｃ）である。図２１Ｃから分かり得るように、多量にドープされた１－$\mu$ｍ厚のラテラルドレイン層（３）に対して、ＬＴＪＦＥＴの指の長さは、好ましくも１００$\mu$ｍの長さを超えない。しかし、指の長さは、ドレイン層（３）の厚みおよび／またはドーピングレベルを増すことによって増加し得る。

【0044】

図２２Ａから図２２Ｈは、図９で述べられたようなデバイスを作成する方法を例証する。図２２Ａは、基板（１）、エピタキシャルに成長したｐ型層（２）、およびエピタキシャルに成長したｎ型層（５ａ）を含むマルチ層構造を示す。エッチマスク（１０）は、図２２Ｂに示されるように、エピタキシャルに成長したｎ型層（５ａ）の露出した表面に置かれる。エピタキシャルに成長したｎ型層（５ａ）は、次いで図２２Ｂに示されるように、選択的にエッチされる（１２）。エッチマスク（１０）は、次いで取り除かれ、イオン注入マスク（１４）は、次いで図２２Ｄに示されるように、エピタキシャルに成長したｎ型層（５ａ）のエッチされた表面上に配置される。マスク（１４）を介したｎ型ドーパントのイオン注入は、図２２Ｅに示されるように、エピタキシャルに成長したｎ型層（５ａ）の中に高度にｎ－ドープされた領域（６ａ）の形成をもたらす。マスク（１４）は、次いで取り除かれ、ｐ型半導体材料（７ａ）の層が、図２２Ｆに示されるように、エピタキシャルに成長したｎ型層（５ａ）のエッチおよびインプラントされた表面上に成長する。エッチマスク（１６）が、次いで図２２Ｇに示されるように、層（７ａ）の露出した表面上に置かれる。マスク（１６）を介したエッチングは、図２２Ｇに示されるように、層（７ａ）の選択的な除去および高いｐ型の形状の形成をもたらす。最後に、マスク（１６）が取り除かれ、オーミックコンタクトが、高いｐ型の形状およびインプラント領域（６ａ）の露出した表面上に形成される。

【0045】

上記に概略を述べた方法はまた、適切なマスクを選択することによって、図１０に示されるような構造を形成するために用いられ得る。

【0046】

図２３Ａから図２３Ｈは、図１２に示されるような構造を作成する方法を例証する。図２３Ａは、基板（１）、基板（１）上のエピタキシャルに成長したｐ型層（２）、および層（２）上のエピタキシャルに成長したｎ型層（５ｂ）を示す。図２３Ｂに示されるように、エッチマスク（１８）が、層（５ｂ）の露出した層に置かれる。エッチング（２０）は、図２３Ｃに示されるように、層（５ｂ）からの材料の選択的な除去をもたらす。マスク（１８）の除去の後に、ｎ型のエピタキシャルな層（６）は、図２３Ｄに示されるように、層（５ｂ）のエッチされた表面に成長する。エッチマスク（２２）は、図２３Ｅに示されるように、層（６）の露出した表面上に位置し、エッチング（２４）は、図２３Ｆに示されるように、層（６）からの材料の選択的な除去および下位層（５ｂ）の露出をもたらす。マスク（２２）は、次いで層（５ｂ）の露出した表面にｐ型のドナーを選択的にイ

ンプラントするために用いられ、図２３Ｇに示されるように、インプラントゲート領域（７）を形成する。オーミックコンタクト（８）は、図２３Ｈに示されるように、インプラントｐ型ゲート領域（７）上にゲート接触を形成するために、かつ、高くしたｎ型領域（６）上にデバイスに対するソースおよびドレイン接触を形成するために、次いで形成される。

【0047】

上記に概略を述べた方法はまた、適切なマスクを選択することによって、図１３に示されるような構造を形成するために用いられ得る。

【0048】

図２４Ａから図２４Ｊは、図１５に示されるような構造を作成する方法を例証する。図２４Ａは、ｎ型構造（１ａ）、基板（１ａ）上にエピタキシャルに成長したｎ型層（３ａ）、および層（３ａ）上にエピタキシャルに成長したｎ型層（４ａ）を示す。イオン注入マスク（２６）もまた、層（４ａ）の露出した上表面に示される。図２４Ｂに示されるように、層（４ａ）は、マスク（２６）を介して選択的にｐ型ドナー原子が注入され、ゲート領域（７）を形成する。マスク（２６）の除去の後に、ｎ型のエピタキシャルな層（５）およびｎ型のエピタキシャルな層（６）は、図２４Ｃおよび図２４Ｄに示されるように、層（４ａ）のインプラントされた表面の上に連続的に成長する。エッチマスク（３０）は、次いで図２４Ｄに示されるように層（６）の露出した表面上に置かれ、層（６）および部分的に下位層（５）のエッチング（３１）が続いて行われる。層（５）の露出した部分は、次いでマスク（３０）を介してｐ型ドナー原子がインプラントされ、図２４Ｆに示されるように追加のゲート領域（７）が形成される。エッチマスク（３４）は次いで、エッチかつインプラントされた構造の表面上に位置し、エッチング（３６）は、ｐ型のインプラントされたゲート領域を含む、層（５）の選択的な除去をもたらす（図２４Ｈ）。層（４ａ）の露出した部分は、次いで図２４Ｉに示されるように、マスク（３８）を介してエッチされる（４０）。オーミックコンタクト（８）は、次いで図２４Ｊに示されるように、エッチかつインプラントされた構造上に形成され、デバイスを形成する。

【0049】

上記に概略を述べた方法もまた、図１６に示されるような構造を形成するために用いられ得る。

【0050】

図２５Ａから図２５Ｄは、図１７に示されるような構造を作成する方法を例証する。図２５Ａに示されるように、図２４Ｅに示されるような構造は、マスク（４２）を介してエッチされ（４４）、下位層（４ａ）の一部を露出させる（図２５Ｂ）。ショットキー接触（９）は、次いで図２５Ｃに示されるように、エッチされた／インプラントされた構造上に形成される。オーミックコンタクト（８）の形成は、図２５Ｄに示されるようなデバイスをもたらす。

【0051】

例示的な実施形態が上述されたが、他の代替的な実施形態もまた、可能である。例えば、ＧａＮ　ｎ型のエピタキシャルな層もまた、炭化珪素、サファイア、またはシリコン基板上に成長させられ得、提案されるデバイス構造の製造のための開始材料スタックを形成する。あるいは、半絶縁のエピタキシャルに成長したバッファ層を有する導電性ＳｉＣ基板を含む基板材料もまた、２００２年１月３日に出願された米国特許出願第１０／０３３，７８５号（米国特許公開番号第２００２－０１４９０２１号として公開される）に開示されるように、用いられ得る。

【0052】

ＳｉＣ層は、公知の技術を用いてドナーまたはアクセプタの材料で層をドープすることによって、形成され得る。例示的なドナーの材料は、窒素およびリンを含む。窒素は、好ましいドナーの材料である。ＳｉＣのドーピングのための例示的なアクセプタの材料は、ホウ素およびアルミニウムを含む。アルミニウムは、好ましいアクセプタの材料である。しかし、上記の材料は単に例示的なものであり、炭化珪素にドープされ得る任意のアクセ

プタおよびドナーの材料が用いられ得る。本明細書中に記述されるＬＴＪＦＥＴ、ＬＪＦＥＴ、およびＶＪＦＥＴの様々な層のドーピングのレベルおよび厚みは、特定のアプリケーションに対する所望の特性を有するデバイスを生成するために変更され得る。同様に、デバイスの様々な形状の寸法もまた、特定のアプリケーションに対する所望の特性を有するデバイスを生成するために変更され得る。

【0053】

ＳｉＣ層は、適切な基板上でのエピタキシャルな成長によって形成され得る。層は、エピタキシャルな成長の間にドープされ得る。

【0054】

前述の本明細書が、例証の目的のために提供される実施例とともに本発明の原理を教示するが、この開示を読むことによって、形状および詳細の様々な変更が、本発明の真の範囲から逸脱することなくなされ得ることが当業者によって認識される。

（参照数字）

図中において用いられる参照数字は、以下に述べられるように定義される。基板、インプラントされた領域、およびエピタキシャルに成長した層に対して、代表的な厚みおよびドーピング濃度もまた、提供される。

【0055】

【表1】

| # | 材料 |
|---|---|
| 1 | 基板（例えば、半絶縁基板） |
| 1a | Ｎ型基板（例えば、ドーピングレベルは $1x10^{18}$ $cm^{-3}$ よりも大きい |
| 2 | エピタキシャルに<br>成長した層（ｐ型）（例えば 0.1 μm以上の厚さ、$1x10^{15}$ - $1x10^{17}$ $cm^{-3}$ ） |
| 3 | エピタキシャルに<br>成長した層（ｎ型）（例えば 0.2-5 μm, $5x10^{18}$ $cm^{-3}$ より大きい） |

【0056】

【表2】

| | |
|---|---|
| 3a | エピタキシャルに<br>成長した層（ｎ型）(例えば 0.5～1 μm、$5x10^{18}$ $cm^{-3}$ よりも大きい) |
| 4 | エピタキシャルに<br>成長した層（ｎ型）(例えば 0.5～10 μm 、$5x10^{15}$ -$5x10^{17}$ $cm^{-3}$) |
| 4a | エピタキシャルに<br>成長した層（ｎ型）(例えば 5～350 μm、$2x10^{14}$ -$2x10^{16}$ $cm^{-3}$) |
| 5 | エピタキシャルに<br>成長した層（ｎ型）(例えば 0.2～1.5 μm、$5x10^{15}$ -$5x10^{17}$ $cm^{-3}$) |
| 5a | エピタキシャルに<br>成長した層（ｎ型）(例えば 0.2～1.5 μm、$5x10^{15}$ -$2x10^{17}$ $cm^{-3}$) |
| 5b | エピタキシャルに<br>成長した層（ｎ型）(例えば 0.3～1.5 μm、$5x10^{15}$ -$2x10^{17}$ $cm^{-3}$) |
| 6 | エピタキシャルに<br>成長した層（ｎ型）(例えば 0.2～1.5 μm 、$5x10^{18}$ $cm^{-3}$ よりも大きい) |
| 6a | インプラントされた<br>領域（ｎ型）　　(例えば 0.1 μm 以上、$5x10^{18}$ $cm^{-3}$ 以上) |
| 7 | インプラントされた<br>領域（ｐ型）　　(例えば 0.1 μm 以上、$5x10^{18}$ $cm^{-3}$ 以上) |
| 7a | エピタキシャルに<br>成長した層（ｐ型）(例えば 0.2～1.5 μm、$5x10^{18}$ $cm^{-3}$ よりも大きい) |
| 8 | オーミックコンタクト |
| 9 | ショットキーコンタクト |

【0057】

【表3】

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【0058】

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【0059】

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【図面の簡単な説明】

【0060】

【図1】図１は、エンハンスト・デプレーション型ＬＴＪＦＥＴを備えているモノリシックインバータ回路の概略断面図である。

【図2】図２は、ビルトインＰｉＮダイオードを有するエンハンスト・デプレーション型ＬＴＪＦＥＴを備えている、モノリシック常時オフＪＦＥＴの概略断面図である。

【図3A】図３Ａは、ビルトインＰｉＮダイオードを有するエンハンスト・デプレーション型ＬＴＪＦＥＴを備えている、モノリシック常時オフＪＦＥＴ集積回路の回路表示である。

【図3B】図３Ｂは、ビルトインＰｉＮダイオードを有するエンハンスト・デプレーション型ＬＴＪＦＥＴを備えている、モノリシック常時オフＪＦＥＴ集積回路の実施例のレイアウトである。

【図4】図４は、ＳＢＤまたはＪＢＳダイオードと一体化となったエンハンスト・デプレーション型ＬＴＪＦＥＴを用いて組み立てられたモノリシック常時オフＪＦＥＴの概略断面図の表示である。

【図5A】図５Ａは、ＳＢＤまたはＪＢＳダイオードと一体化されたエンハンスト・デプレーション型ＬＴＪＦＥＴを備えているモノリシック常時オフＪＦＥＴ集積回路の回路表示である。

【図5B】図５Ｂは、ＳＢＤまたはＪＢＳダイオードと一体化されたエンハンスト・デプレーション型ＬＴＪＦＥＴを備えるモノリシック常時オフＪＦＥＴ集積回路の実施例のレイアウトである。

【図6】図６は、ビルトインＰｉＮダイオードを有するエンハンスト型ＬＴＪＦＥＴおよびデプレーション型ＶＪＦＥＴを用いて組み立てられたハイブリッド常時オフＪＦＥＴの概略断面図である。

【図7】ＳＢＤまたはＪＢＳダイオードと一体化されたエンハンスト型ＬＴＪＦＥＴまたはデプレーション型ＶＪＦＥＴを用いて組み立てられたハイブリッド常時オフＪＦＥＴの概略断面図である。

【図8】図８は、ビルトオンチップ低電圧高電流エンハンストメント型ＬＴＪＦＥＴを駆動し、ディスクリート高電圧常時オン電源ＶＪＦＥＴとカスコードで接続されるモノリシックＬＴＪＦＥＴタイマー回路の回路図である。

【図9】図９は、エンハンスト・デプレーション型過剰成長ゲートＬＪＦＥＴを用いて組み立てられたモノリシックインバータ回路の概略断面図である。

【図10】図１０は、エンハンスト型過剰成長ゲートＬＪＦＥＴおよびデプレーション型ＶＪＦＥＴを備えている、ハイブリッド常時オフＪＦＥＴの概略断面図である。

【図11】図１１は、低電圧エンハンスト型ＬＪＦＥＴおよび高電圧ディスクリート常時オンデプレーション型ＶＪＦＥＴを備えている、ハイブリッド常時オフＪＦＥＴ電源スイッチの概略断面図の表示である。
【図12】エンハンスト・デプレーション型インプラントゲートＬＪＦＥＴを用いて組み立てられたモノリシックインバータ回路の概略断面図の表示である。
【図13】図１３は、エンハンスト・デプレーション型インプラントゲートＬＪＦＥＴを用いて組み立てられたモノリシック常時オフＪＦＥＴ集積回路の概略断面図の表示である。
【図14】図１４は、エンハンスト型インプラントゲートＬＪＦＥＴおよびデプレーション型ＶＪＦＥＴを用いて組み立てられたハイブリッド常時オフＪＦＥＴ集積回路の概略断面図である。
【図15】図１５は、エンハンスト型デュアルゲートＬＪＦＥＴおよびデプレーション型ＶＪＦＥＴを用いて組み立てられたハイブリッド常時オフＪＦＥＴ集積回路の概略断面図であり、ＬＪＦＥＴの底部ゲートは、ドリフト領域にインプラントされている。
【図16】図１６は、エンハンスト型デュアルゲートＬＪＦＥＴおよびデプレーション型ＶＪＦＥＴを用いて組み立てられるハイブリッドガードリング限界常時オフＪＦＥＴの概略断面図の表示であり、ＬＪＦＥＴの底部ゲートおよびガードリングは、ドリフト領域にインプラントされる。
【図17】図１７は、ショットキーゲートを有するエンハンスト型デュアルゲートＬＪＦＥＴおよびデプレーション型ＶＪＦＥＴを用いて組み立てられる、ハイブリッドガードリング限界常時オフＪＦＥＴの概略断面図の表示であり、ＬＪＦＥＴの底部ゲートおよびガードリングは、ドリフト領域にインプラントされる。
【図18A】図１８Ａは、ＳｉＣ　ＬＴＪＦＥＴ集積スイッチの模擬のデバイス構造図である。
【図18B】図１８Ｂは、ＳｉＣ　ＬＴＪＦＥＴ集積スイッチの模擬の概略断面図である。
【図18C】図１８Ｃは、ＳｉＣ　ＬＴＪＦＥＴ集積スイッチの模擬の出力ＤＣ特性を示すグラフである。
【図18D】図１８Ｄは、ＳｉＣ　ＬＴＪＦＥＴ集積スイッチの模擬の出力ＤＣ特性を示すグラフである。
【図19A】図１９Ａは、ハイブリッド常時オフ９００Ｖ電源スイッチの写真である。
【図19B】図１９Ｂは、ハイブリッド常時オフ９００Ｖ電源スイッチの回路の表示図である。
【図19C】図１９Ｃは、ハイブリッド常時オフ９００Ｖ電源スイッチの測定特性を示すグラフである。
【図19D】図１９Ｄは、ハイブリッド常時オフ９００Ｖ電源スイッチの測定特性を示すグラフである。
【図20A】図２０Ａは、ハイブリッド常時オフ９００Ｖ電源スイッチの回路図である。
【図20B】図２０Ｂは、ハイブリッド常時オフ９００Ｖ電源スイッチの測定内部電圧を示すグラフである。
【図21A】ＬＴＪＦＥＴの分散ドレイン抵抗の概略図である。
【図21B】ＶＪＦＥＴの分散ドレイン抵抗の概略図である。
【図21C】ラテラルドレイン層の異なるドーピングレベルに対する指の長さの関数として、ＶＪＦＥＴのバーチカルドレインの抵抗に対して正規化されたＬＴＪＦＥＴのラテラルドレイン層の抵抗を示すグラフである。
【図22】図２２Ａ～図２２Ｈは、図９および図１０に述べられるようなモノリシック集積回路を作成するための方法を例示する。
【図23】図２３Ａ～図２３Ｈは、図１２および図１３に述べられるようなモノリシック集積回路を作成するための方法を例示する。
【図24】図２４Ａ～図２４Ｊは、図１５に述べられるようなモノリシック集積回路を作成するための方法を例示する。
【図25】図２５Ａ～図２５Ｄは、図１７に述べられるようなモノリシック集積回路を作成

するための方法を例示する。

【図1】

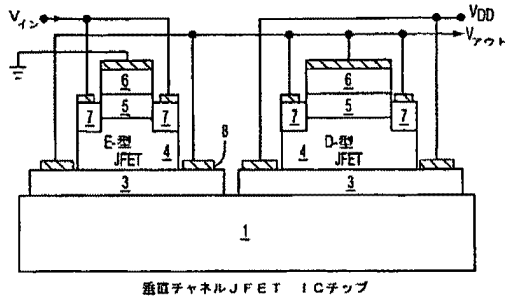



FIG. 1

【図2】

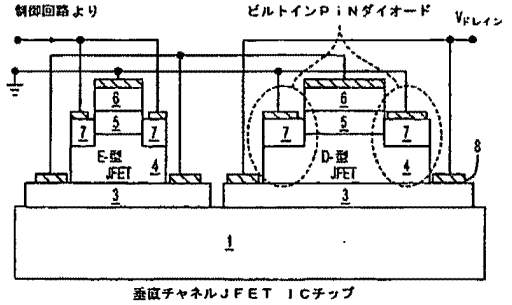



FIG. 2

【図3A】

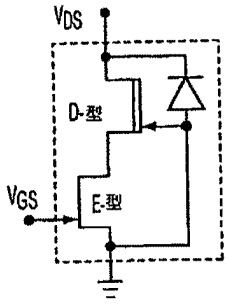



FIG. 3A

【図3B】

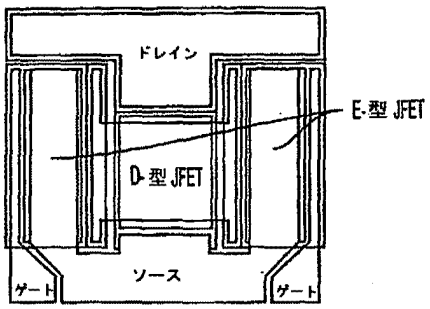



FIG. 3B

【図4】

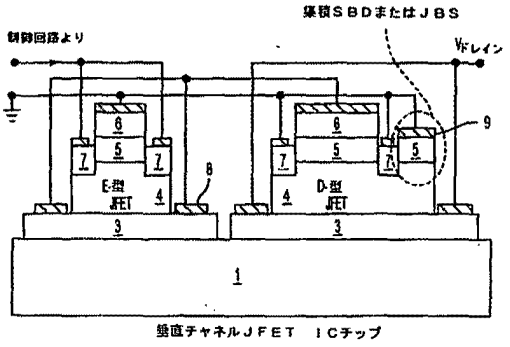



FIG. 4

【図5A】

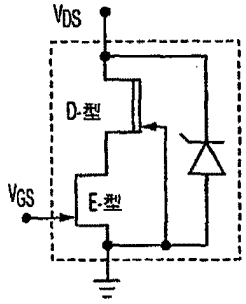



FIG. 5A

【図5B】

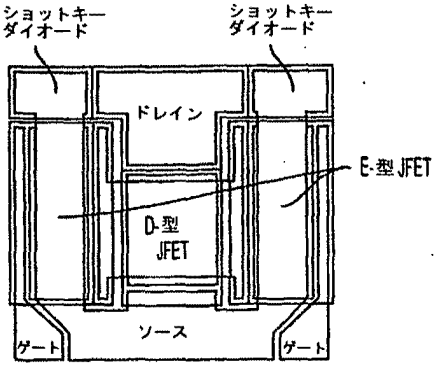



FIG. 5B

【図6】

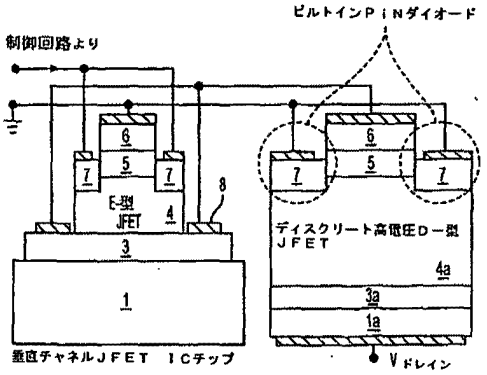



FIG. 6

【図7】

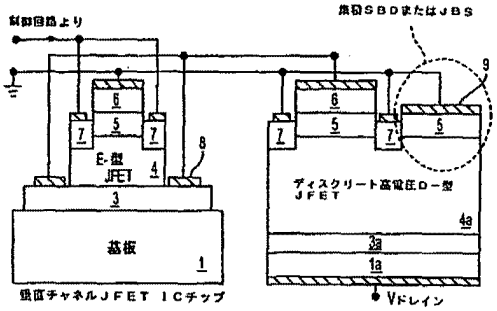



FIG. 7

【図8】

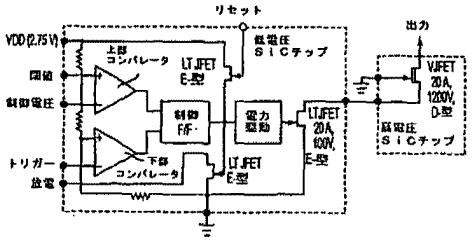



FIG. 8

【図9】

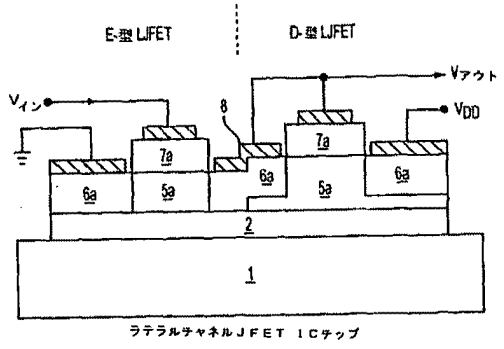



FIG. 9

【図10】

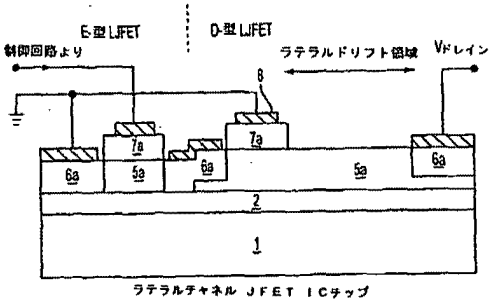



FIG. 10

【図11】

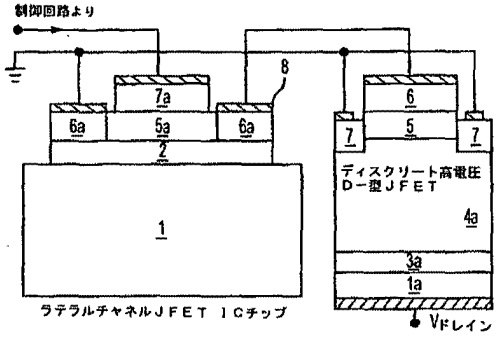



FIG. 11

【図12】

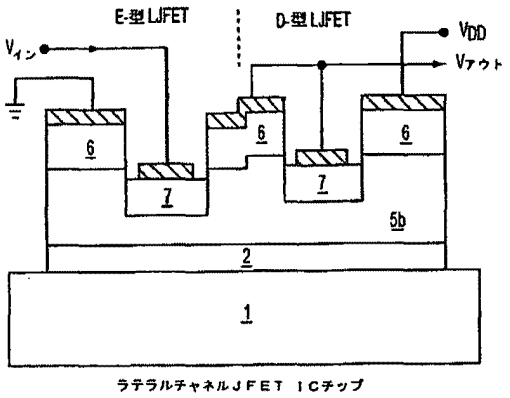



FIG. 12

【図13】

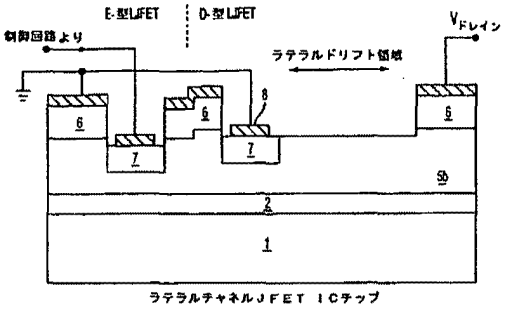



FIG. 13

【図14】

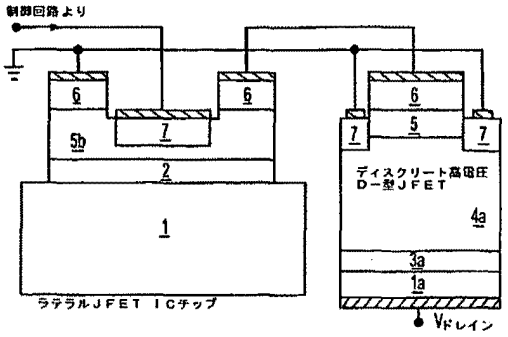



FIG. 14

【図15】

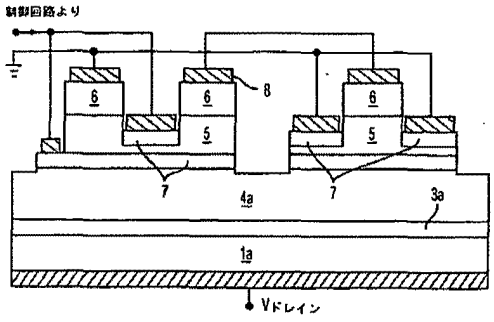



FIG. 15

【図16】

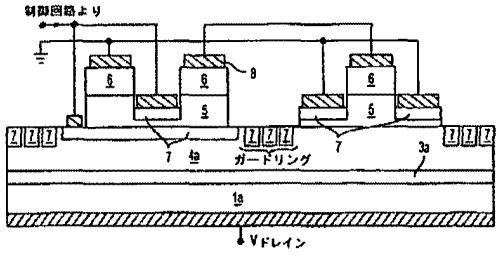



FIG. 16

【図17】

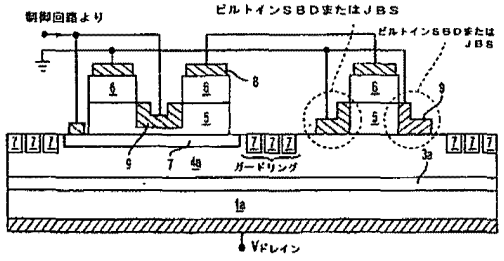



FIG. 17

【図18A】

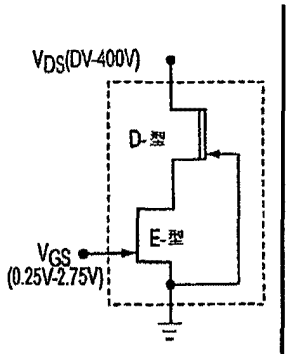



FIG. 18A

【図18B】

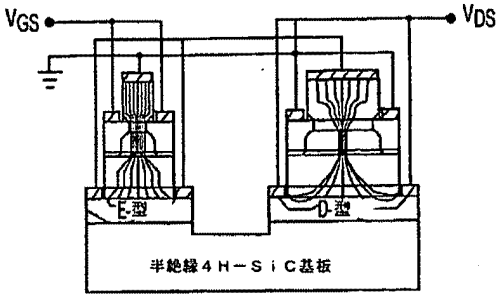



FIG. 18B

【図18C】

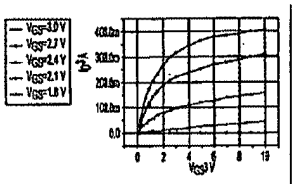
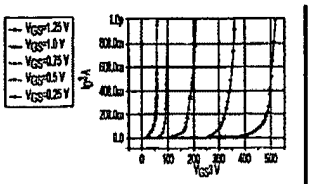


FIG. 18C

【図18D】



SUBSTITUTE SHEET (RULE 26)

【図19A】

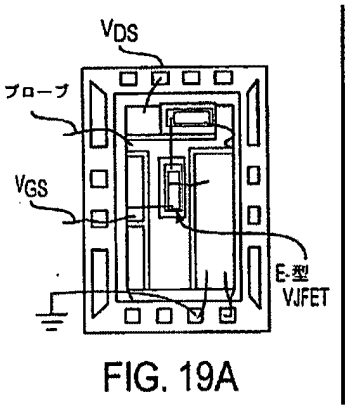



FIG. 19A

【図19B】

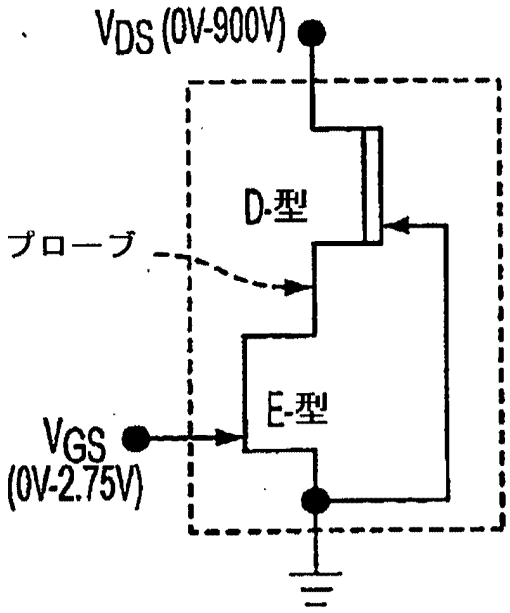



FIG. 19B

【図19C】

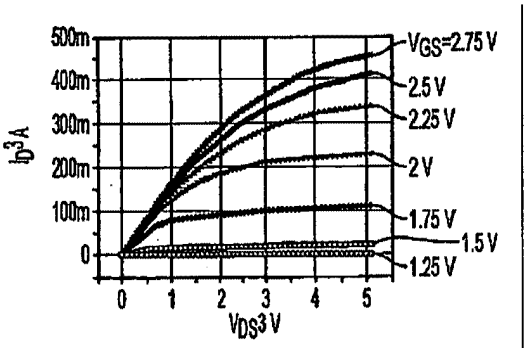



FIG. 19C

【図19D】

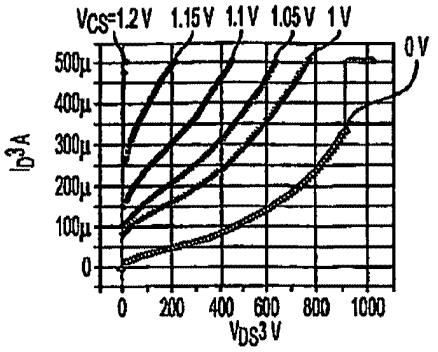



FIG. 19D

SUBSTITUTE SHEET (RULE 26)

【図20A】

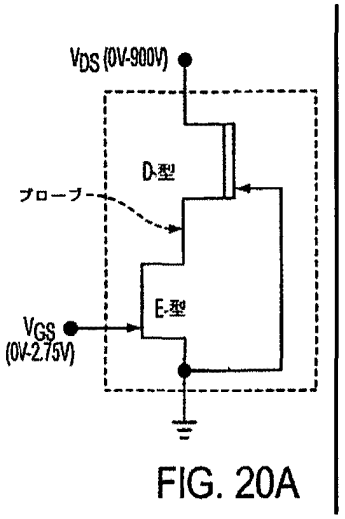



FIG. 20A

【図20B】

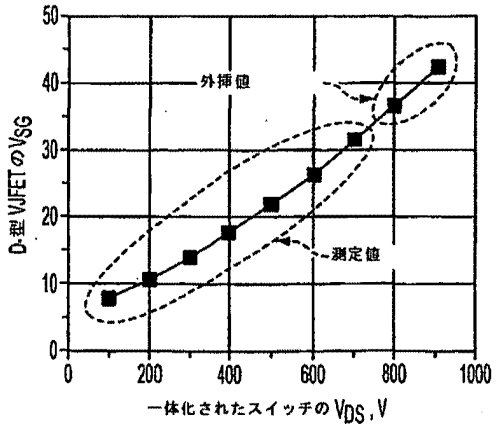



FIG. 20B

【図21A】

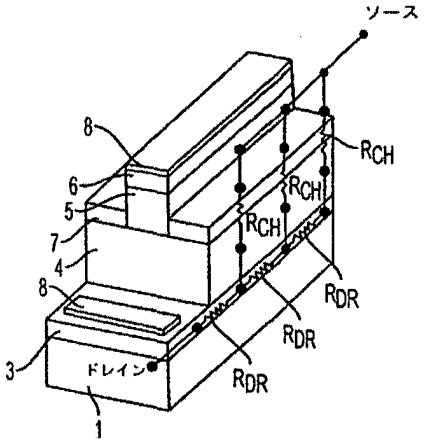



FIG. 21A

【図21B】

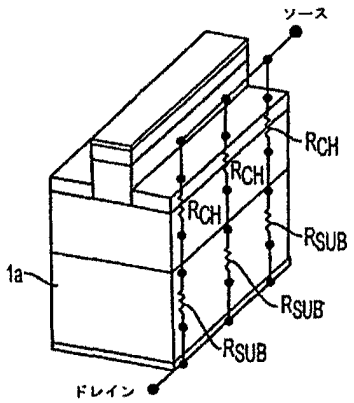



FIG. 21B

【図21C】

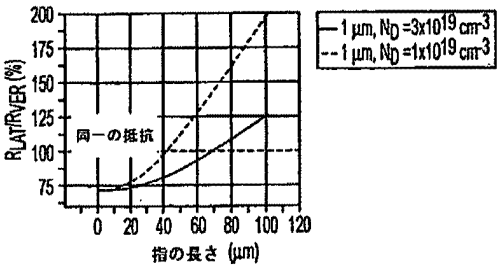



FIG. 21C

【図22A】

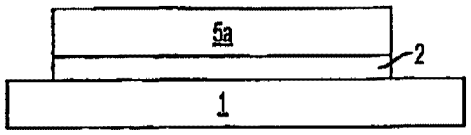



FIG. 22A

【図22B】

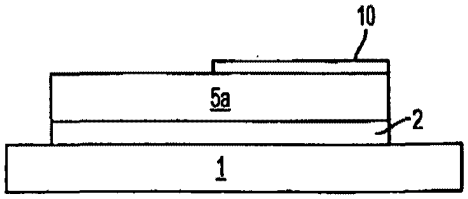



FIG. 22B

【図22C】

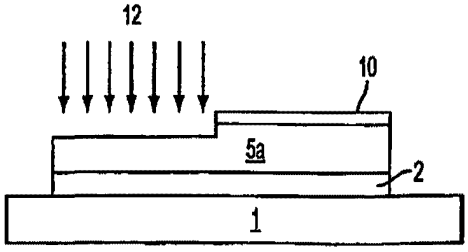



FIG. 22C

【図22D】

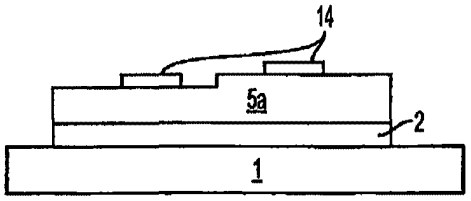



FIG. 22D

【図22E】

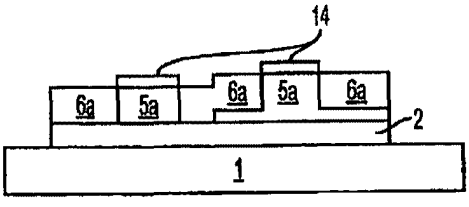



FIG. 22E

【図22F】

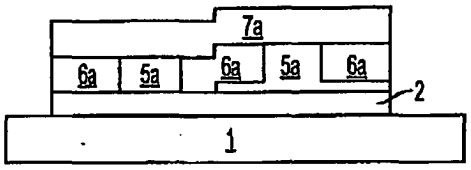



FIG. 22F

【図22G】

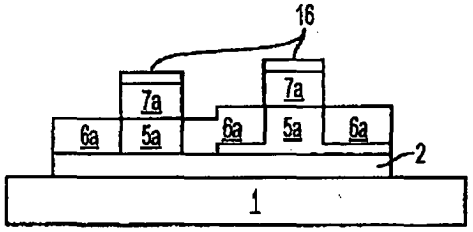



FIG. 22G

【図22H】

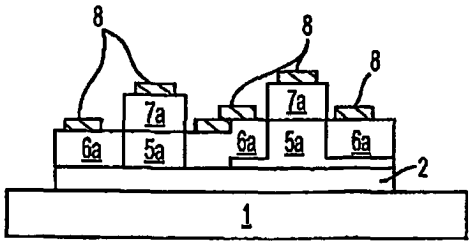



FIG. 22H

【図23A】

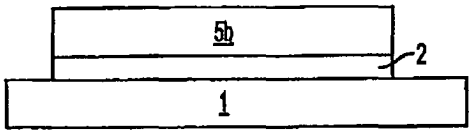



FIG. 23A

【図23B】

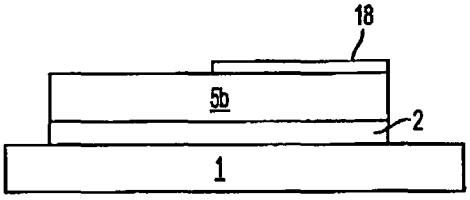



FIG. 23B

【図23C】

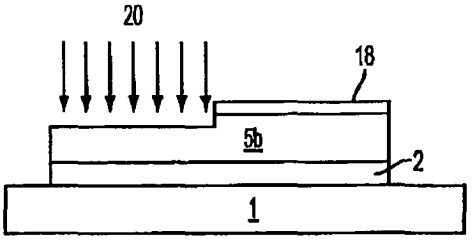



FIG. 23C

【図23D】

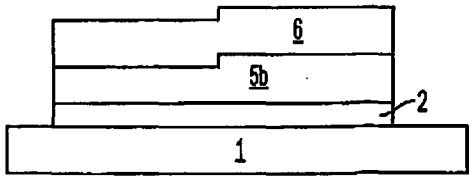



FIG. 23D

【図23E】

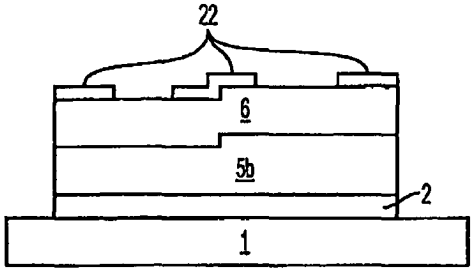



FIG. 23E

【図23F】

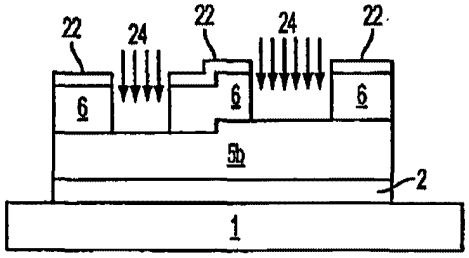



FIG. 23F

【図23H】

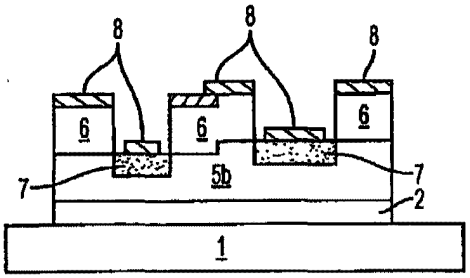



FIG. 23H

【図23G】

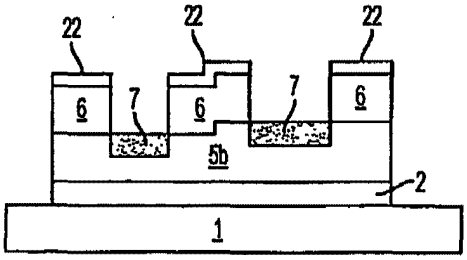



FIG. 23G

【図24A】

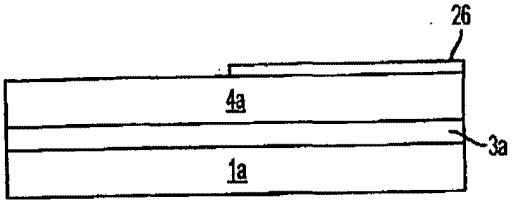



FIG. 24A

【図24B】

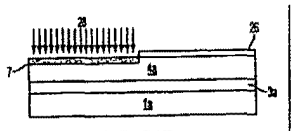


FIG. 24B

【図24C】

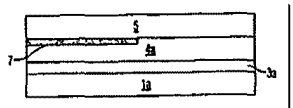


FIG. 24C

【図24D】

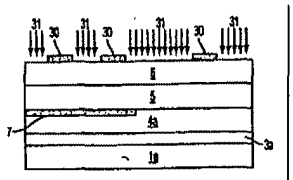


FIG. 24D

【図24E】

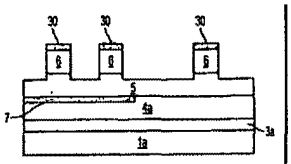


FIG. 24E

【図24F】

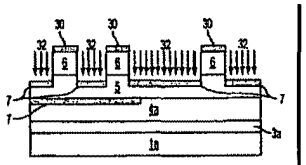


FIG. 24F

【図24G】

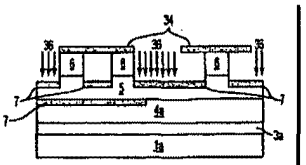


FIG. 24G

【図24H】

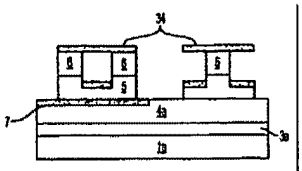


FIG. 24H

【図24I】

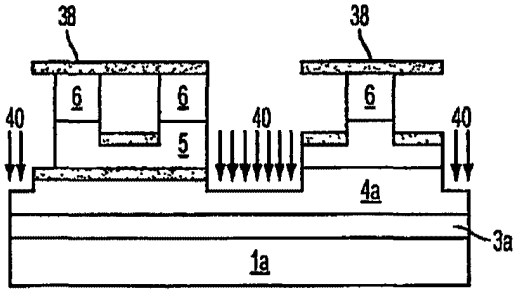



FIG. 24I

【図24J】

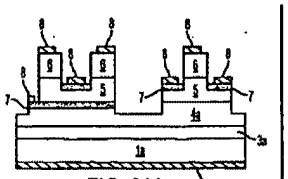


FIG. 24J

【図25A】

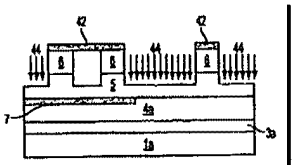


FIG. 25A

【図25B】

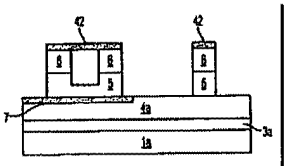


FIG. 25B

【図25C】

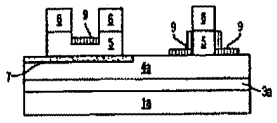


FIG. 25C

【図25D】

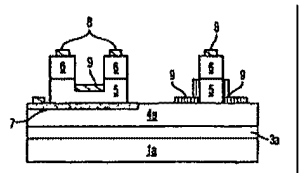


FIG. 25D

## INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/42982

A. CLASSIFICATION OF SUBJECT MATTER
IPC: H01L 29/76( 2006.01)

USPC: 257/341
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/341

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | US 6,545,297 B1 (NOBLE, JR. et al) 08 April 2003 (08.04.2003), see entire document. | 1-90 |
| A,E | US 6,943,407 B2 (OUYANG et al) 13 September 2005 (13.09.2005), see entire document. | 1-90 |
| A,P | US 6,958,275 B2 (METZLER) 25 October 2005 (25.10.2005), see entire document. | 1-90 |
| A,P | US 2005/0067630 A1 (ZHAO) 31 March 2005 (31.03.2005), see entire document. | 1-90 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 25 June 2006 (25.06.2006) | 19 JUL 2006 |
| Name and mailing address of the ISA/US<br>Mail Stop PCT, Attn: ISA/US<br>Commissioner for Patents<br>P.O. Box 1450<br>Alexandria, Virginia 22313-1450<br>Facsimile No. (571) 273-3201 | Authorized officer<br>JOSE G. DEES<br>Telephone No. (571) 272-1607 |

Form PCT/ISA/210 (second sheet) (April 2005)

**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/US05/42982

Continuation of B. FIELDS SEARCHED Item 3:
EAST: US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
search terms:
("20020149021"|"20030089930"|"3767946"|"4107725"|"4587712"|"4663547"|"5264713"|"5610085"|"5710455"|"5945701"|"6156611"|"6344663"|"6503782"|"6600192"|"6693322").PN.; (buffer with p) and (lateral with channel) and (gate with p with second); 257/341.ccls.

Form PCT/ISA/210 (extra sheet) (April 2005)

(51)Int.Cl. FI テーマコード（参考）
H01L 29/417 (2006.01) H01L 21/28 301B
H01L 21/28 (2006.01)

(81)指定国 AP(BW,GH,GM,KE,LS,MW,MZ,NA,SD,SL,SZ,TZ,UG,ZM,ZW),EA(AM,AZ,BY,KG,KZ,MD,RU,TJ,TM),EP(AT,BE,BG,CH,CY,CZ,DE,DK,EE,ES,FI,FR,GB,GR,HU,IE,IS,IT,LT,LU,LV,MC,NL,PL,PT,RO,SE,SI,SK,TR),OA(BF,BJ,CF,CG,CI,CM,GA,GN,GQ,GW,ML,MR,NE,SN,TD,TG),AE,AG,AL,AM,AT,AU,AZ,BA,BB,BG,BR,BW,BY,BZ,CA,CH,CN,CO,CR,CU,CZ,DE,DK,DM,DZ,EC,EE,EG,ES,FI,GB,GD,GE,GH,GM,HR,HU,ID,IL,IN,IS,JP,KE,KG,KM,KN,KP,KR,KZ,LC,LK,LR,LS,LT,LU,LV,LY,MA,MD,MG,MK,MN,MW,MX,MZ,NA,NG,NI,NO,NZ,OM,PG,PH,PL,PT,RO,RU,SC,SD,SE,SG,SK,SL,SM,SY,TJ,TM,TN,TR,TT,TZ,UA,UG,US,UZ,VC,VN,YU,ZA,ZM,ZW

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アメリカ合衆国 ミシシッピ 39759， スタークビル， プリソック ロード 1258

Fターム(参考) 4M104 AA03 CC01 FF03 GG11 GG13 GG18
5F102 FA00 GA02 GA14 GB01 GB04 GC01 GC08 GD04 GJ02 GJ03
GJ04 GJ10 GK02 GK04 GL04 GR09 GS07 HC01 HC07 HC15

Attorney Docket No.: 0400131

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| | |
|---|---|
| In re Application of: **Herman, Thomas** | Art Unit: 2826 |
| Serial No.: 11/688,338 | Examiner: Ahmed, Selim U. |
| Filed: 03/20/2007 | |
| For: **Merged Gate Cascode Transistor** | |

## AMENDMENT AND RESPONSE TO NON-FINAL OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the Non-Final Office Action dated December 21, 2011 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.



PAGE 2/17 * RCVD AT 3/21/2012 9:01:57 PM [Eastern Daylight Time] * SVR:W-PTOFAX-001/12 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):03-30

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**In the Claims:**

**Claim 1 (currently amended):** A merged cascode transistor circuit comprising:

an input voltage signal source having an input voltage signal;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a semiconductor element;

a source electrode electrically connected to a top surface of the semiconductor element;

a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;

a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;



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wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at ~~the source electrode~~ a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level, [[and]] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and wherein a drain region of the enhancement mode transistor is merged with a source region of the enhancement mode transistor at the node in the semiconductor element.

**Claim 2 (previously presented):** The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:

a first III-Nitride layer; and

a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

**Claim 3 (previously presented):** The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 4 (previously presented):** The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

**Claim 5 (previously presented):** The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 6 (previously presented):** The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claim 7 (previously presented):** The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.

**Claim 8 (previously presented):** The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

**Claim 9 (previously presented):** The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

**Claim 10 (currently amended):** A merged cascode high electron mobility transistor circuit comprises:

an input voltage signal source having an input voltage signal;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a first epitaxial layer of III-Nitride material;

a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

a source electrode electrically connected to the first epitaxial layer;

a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;



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a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and

a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;

wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at ~~the source electrode~~ a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level, [[and]] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and wherein a drain region of the enhancement mode transistor is merged with a source region of the enhancement mode transistor at the node in the semiconductor element.



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**Claim 11 (original):** The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

**Claim 12 (previously presented):** The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGaN material and the second epitaxial layer comprises a GaN material.

**Claim 13 (original):** The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claim 14 (previously presented):** The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

**Claim 15 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

**Claim 16 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.

## REMARKS

Prior to the present amendment and response, claims 1-16 were pending in the present application. By the present amendment and response, Applicant has amended claims 1 and 10. Thus, after the present amendment and response, claims 1-16 remain in the present application. Applicant respectfully requests reconsideration and allowance of pending claims 1-16 in view of the above amendments and the following remarks.

### A. Rejection of Claims 1-9 under 35 U.S.C. § 103(a)

In the Non-Final Office Action dated December 21, 2011 (hereinafter "Office Action"), the Examiner rejects claims 1-9 under 35 U.S.C. § 103(a) as being unpatentable for purported obviousness over U.S. Patent Application Publication Number 2005/0189561 A1 by Kinzer et al. (hereinafter "Kinzer") in view of U.S. Patent Application Publication Number 2004/0188761 A1 by Jun Koyama (hereinafter "Koyama"), and further in view of U.S. Patent Application Publication Number 2005/0051796 A1 by Parikh et al. (hereinafter "Parikh"). *See* pages 2-9, item 3 of the Office Action. For the reasons discussed below, Applicant respectfully submits that amended independent claim 1 is patentably distinguishable over Kinzer, Koyama, and Parikh, either singly or in any combination thereof.

The present application is directed, in part, to a novel merged gate cascode transistor that is useful for high voltage, high speed applications. *See*, e.g., page 1, paragraph [0003] of the present application. For example, in one implementation, as





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shown and described with respect to Figure 3 of the present application, exemplary merged gate cascode high electron mobility transistor 30 (HEMT 30) includes first portion Q1 in enhancement mode having source contact 31 positioned on a top surface of semiconductor element 29, gate 32 (G1), and Q1 drain, which is merged with Q2 source of second portion Q2 in depletion mode having gate 33 (G2) and drain contact 34 positioned on the top surface of semiconductor element 29. *Id.*, e.g., at page 2, paragraphs [0022] and [0023] with Figure 3. As further shown in Figure 3, G1 is connected to an input voltage source providing gate voltage Vg1, and G2 is connected to a constant voltage source providing a predetermined constant voltage Vg2 (e.g., 0 volt). *Id.*, e.g., at paragraph [0017] with Figure 3.

As disclosed in the present application, in operation, when the input voltage signal source provides a high voltage Vg1 at G1 that meets or exceeds enhancement threshold voltage Vt1 of first portion Q1, first portion Q1 starts conducting. *Id.* Because second portion Q2 is in depletion mode with voltage Vg2 at G2 being set to 0 volt, second portion Q2 is fully ON and conducting. *Id.* Thus, first portion Q1 and second portion Q2 of HEMT 30 are both ON and conducting. When the input voltage signal source provides a low voltage Vg1 at G1 that is below enhancement threshold voltage Vt1 of first portion Q1, first portion Q1 turns OFF and stops conducting. *Id.*, e.g., at paragraph [0018] with Figure 3. As a result, the voltage at Node d1s2 rises until the gate-source voltage (Vgs) of second portion Q2 reaches pinch off voltage Vp2, then second portion Q2 turns OFF and stops conducting. *Id.*

As Q1 drain of first portion Q1 and Q2 source of second portion Q2 are merged at Node d1s2 (e.g., represented by arrow 39 in Figure 3) in semiconductor element 29, the voltage Vd1s2 at Node d1s2 never rises above the magnitude of pinch off voltage Vp2 of second portion Q2. *Id.*, e.g., at paragraphs [0019]-[0021]. As such, by setting a low pinch off voltage Vp2 of second portion Q2, the drain swing of first portion Q1 can be substantially reduced, thereby, improving switching performance. *Id.*

Amended independent claim 1 emphasizes similar abovementioned advantageous features by reciting, in part, "wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and wherein a drain region of the enhancement mode transistor is merged with a source region of the enhancement mode transistor at the node in the semiconductor element." *See* claim 1 above. Support for amended independent claim 1 can be found at least on page 2, paragraphs [0017] and [0023], and Figure 4 of the present application.

In the Office Action, the Examiner asserts that Kinzer discloses various features as recited in independent claim 1. *See* page 3 of the Office Action. Specifically, the Examiner refers to device 50 having gate electrodes 32 and 34, as shown in Figure 4 of Kinzer, as "a merged cascode transistor" as recited in independent claim 1 of the present application. *Id.* Applicant respectfully disagrees with the Examiner's assertion above.

Figure 4 of Kinzer describes a specific dual gated nominally off III-nitride bi-directional switch element. *See* page 1, paragraph [0016] of Kinzer. As shown in Figure 4 of Kinzer, enhancement mode device 50 includes a single source having source

electrode 25, a single drain having drain electrode 26, and gate electrodes 32 and 34 each disposed within a respective recess 38 in second semiconductor body 21. *Id.* at page 3, paragraph [0038] with Figure 4. As can be seen in Figure 4 of Kinzer, each recess 38 causes an interruption in 2DEG, thereby rendering enhancement mode device 50 nominally off, which can be restored upon application of a suitable voltage to gate electrodes 32 and 34. *Id.* As disclosed in Kinzer, enhancement mode device 50 acts as a power logic AND gate, in which current flows to/from electrodes 25 and 26 when both gate electrodes 32 and 34 have a potential applied to them. *Id.* at paragraph [0038].

In the Office Action, the Examiner further asserts that Figure 4 of Kinzer discloses:

> a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and capacitively coupled to the semiconductor element (para[0035]) to form a first portion of the transistor (e.g. Fig. 4, portion of transistor 32); and a second gate 34 positioned adjacent to the first gate 32, and between the source electrode 25 and the drain electrode 26 to form a second portion of the transistor (e.g. Fig. 4, portion of transistor 34), wherein the second portion of the transistor (e.g. Fig. 4, portion of transistor 34), wherein the second gate 34 is also capacitively coupled to the semiconductor element (para[0035]); wherein in the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9). *See* page 3 of the Office Action.

Applicant respectfully disagrees with the Examiner's assertions above.

As discussed above, enhancement mode device 50, as shown in Figure 4 of Kinzer, is a single III-nitride bi-directional switch that includes a single source having source electrode 25, a single drain having drain electrode 26, and a dual gate structure having



PAGE 12/17 * RCVD AT 3/21/2012 9:01:57 PM [Eastern Daylight Time] * SVR:W-PTOFAX-001/12 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):03-30

gate electrodes 32 and 34. *See* page 3, paragraph [0038] with Figure 4 of Kinzer. As an enhancement mode switch, device 50 is nominally off when no voltage (e.g., 0 volt) is applied to gate electrodes 32 and 34. *Id.* Thus, "portion of transistor 32" and "portion of transistor 34," which are referred to by the Examiner as "a first portion of the transistor" and "a second portion of the transistor," respectively, cannot be equated to "an enhancement mode transistor" and "a depletion mode transistor" as described by amended independent claim 1 of the present application.

Furthermore, in the Office Action, the Examiner asserts that paragraph [0038] and claim 10 of Kinzer describe a switch operating in enhancement mode, and paragraphs [0033] and [0026] and claim 9 describe a switch operating in depletion mode. *See* above. Applicant respectfully notes that the abovementioned paragraphs (i.e., paragraphs [0026], [0033] and [0036]) of Kinzer each describe a distinct device (e.g., device 20, device 40, and device 50, respectively) that has **a single source and a single drain**, and operates **either** in depletion mode **or** in enhancement mode. Consequently, Applicant respectfully submits that each of devices 20, 40, and 50 of Kinzer has fundamental structural differences with implementations as described by amended independent claim 1. Thus, Applicant respectfully submits that Kinzer fails to disclose or suggest, for example, "wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor," as is expressly required by amended independent claim 1 of the present application.

Furthermore, nowhere does Kinzer disclose or suggest, for example, "wherein a drain region of the enhancement mode transistor is merged with a source region of the enhancement mode transistor at the node in the semiconductor element," as is expressly required by amended independent claim 1. Applicant respectfully asserts that the abovementioned feature is also not disclosed by Koyama or Parikh.

For the foregoing reasons, Applicant respectfully submits that, amended independent claim 1 is neither anticipated by, nor is obvious in light of, the disclosures provided by Kinzer, Koyama, and Parikh, either singly or in any combination thereof. Thus, Applicant respectfully submits independent claim 1 is patentably distinguishable over Kinzer, Koyama, and Parikh, and, as such, claims 2-9 depending from and further limiting patentable independent claim 1, are, *a fortiori*, also patentably distinguishable over Kinzer, Koyama, and Parikh for at least the reasons presented above and also for the additional limitations contained in each dependent claim.

**B. Rejection of Claims 10-16 under 35 U.S.C. §103(a)**

In the Office Action, the Examiner rejects claims 10-16 under 35 U.S.C. § 103(a) as being unpatentable for purported obviousness over Kinzer in view of Koyama, U.S. Patent Number 7,052,942 B1 to Smart et al. (hereinafter "Smart"), and Parikh. *See* pages 9-14, item 4 of the Office Action. For the reasons discussed below, Applicant respectfully submits that amended independent claim 10 is patentably distinguishable over Kinzer, Koyama, Smart, and Parikh, either singly or in any combination thereof.



PAGE 14/17 * RCVD AT 3/21/2012 9:01:57 PM [Eastern Daylight Time] * SVR:W-PTOFAX-001/12 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):03-30

By the present response, Applicant has amended independent claim 10 to recite, in part, "wherein a drain region of the enhancement mode transistor is merged with a source region of the enhancement mode transistor at the node in the semiconductor element." For reasons similar to those presented in Section A of the present response, Applicant respectfully asserts that Kinzer fails to disclose or suggest, for example, "wherein a drain region of the enhancement mode transistor is merged with a source region of the enhancement mode transistor at the node in the semiconductor element," as is expressly required by independent claim 10 of the present application, a feature that is also not disclosed by Koyama, Smart, or Parikh.

For the foregoing reasons, Applicant respectfully submits that, amended independent claim 10 is neither anticipated by, nor is obvious in light of, the disclosures provided by Kinzer, Koyama, Smart, and Parikh, either singly or in any combination thereof. Thus, Applicant respectfully submits independent claim 10 is patentably distinguishable over Kinzer, Koyama, Smart, and Parikh, and, as such, claims 11-16 depending from and further limiting patentable independent claim 10, are, *a fortiori*, also patentably distinguishable over Kinzer, Koyama, Smart, and Parikh for at least the reasons presented above and also for the additional limitations contained in each dependent claim.

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C. **Conclusion**

For all the foregoing reasons, Applicant respectfully submits that amended independent claims 1 and 10, and claims depending therefrom, are patentably novel and inventive. Moreover, Applicant asserts that no new matter has been introduced herein. Accordingly, an early allowance of pending claims 1-16 is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.



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Attorney Docket No.: 0400131

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 3/21/12

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Signature Date



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## FACSIMILE TRANSMISSION COVER SHEET

Date: March 21, 2012

To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826

Fax: (571) 273-8300

Re: **Application Serial No.: 11/688,338**
Filing Date: 3/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 17

Message:

Enclosed please find the Amendment and Response to Non-Final Office Action dated December 21, 2011.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account **50-0731**.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

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| **PATENT APPLICATION FEE DETERMINATION RECORD**<br>Substitute for Form PTO-875 | Application or Docket Number<br>11/688,338 | Filing Date<br>03/20/2007 | ☐ To be Mailed |
|---|---|---|---|

## APPLICATION AS FILED – PART I

| | (Column 1) | (Column 2) | SMALL ENTITY ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE ($) | FEE ($) | | RATE ($) | FEE ($) |
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| AMENDMENT | 03/21/2012 | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE ($) | ADDITIONAL FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * 16 | Minus | ** 20 | = 0 | X $ = | | OR | X $60= | 0 |
| | Independent (37 CFR 1.16(h)) | * 2 | Minus | ***3 | = 0 | X $ = | | OR | X $250= | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | 0 |

| AMENDMENT | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DESHONNE T. MARTINO/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | Thomas Herman | 0400131 | 9886 |

25700 7590 12/21/2011

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| EXAMINER | |
|---|---|
| AHMED, SELIM U | |
| **ART UNIT** | **PAPER NUMBER** |
| 2826 | |
| **MAIL DATE** | **DELIVERY MODE** |
| 12/21/2011 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 11/688,338 | HERMAN, THOMAS | |
| | Examiner | Art Unit | |
| | SELIM AHMED | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 September 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

5)☒ Claim(s) *1-16* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-16* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *20 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/13/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/12/2011 has been entered.

### *Information Disclosure Statement*

2. The Information Disclosure Statements filed on 4/13/2011 have been considered.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer ET al (2005/0189561; Kinzer hereinafter) in view of Koyama (US 2004/0188761; Koyama hereinafter) and further in view of Parikh et al (US 2005/0051796; Parikh hereinafter).

With regard to claim 1, Fig. 4 of Kinzer discloses a merged gate transistor circuit 50 comprising: a merged cascode transistor 32, 34 (Fig.4) comprising: a semiconductor element (element comprising of 21, 22, 23, and 24 i.e. substrate); a source electrode 25 electrically connected to a top surface (top surface of 21 in Fig. 4) of the semiconductor element; a drain electrode 26 electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode 25; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and capacitively coupled to the semiconductor element (para[0035]) to form a first portion of the transistor (e.g. Fig. 4, portion of transistor 32); and a second gate 34 positioned adjacent to the first gate 32, and between the source electrode 25 and the drain electrode 26 to form a second portion of the transistor (e.g. Fig. 4, portion of transistor 34), wherein the second gate 34 is also capacitively coupled to the semiconductor element (para[0035]); wherein in the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, Kinzer discloses the claim 1 limitations but does not explicitly disclose, “an input voltage signal source, a constant voltage source having a predetermined constant voltage; wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the

constant voltage source such that the second portion of the transistor conducts until a voltage difference between to the constant voltage source and a voltage at the source electrode reaches a predetermined level". However, applicant's above limitations directed to functional or method of operating the device for depletion mode and enhancement mode transistor. The above limitations, particularly, an input voltage signal source and a constant voltage source having a predetermined constant voltage are nothing but bias voltages to the enhancement and depletion mode transistors that are required to operate/function of the device. Although Kinzer does not explicitly disclose an input voltage signal source and a constant voltage source having a predetermined constant voltage, Kinzer depletion mode and enhancement mode devices inherently require these bias conditions to operate/function. However, for example, Figs. 1, 2, 5 and para[0008, 0049] of Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 devices. Since it is common knowledge to apply bias voltages to the gates of the depletion and enhancement mode devices for device operation, it would have been obvious to one having ordinary skill in the art at the time of the invention to include an input voltage signal source and a constant voltage source having a predetermined constant voltage within Kinzer device to operate/function of the device.

As discussed above, Kinzer in view of Koyama discloses the limitations of the claim 1 with the exception of wherein the second gate includes a field plate. However, Fig.6 of Parikh discloses wherein the second gate 26 includes a field plate 28. According to para[0031] of Parikh, the field plate arrangement for both the HEMT and MESFET can reduce the peak electric field in the device, compared to a device without a field plate, which can result in increased breakdown voltage and reduced trapping. The reduction of the electric field can also yield other benefits such as reduced leakage currents and enhanced reliability. It would have been obvious to one having ordinary skill in the art at the time of the invention to include a field plate within second gate as shown by Parikh within Kinzer's device to reduce leakage current and enhance reliability of the device.

Furthermore, Kinzer discloses all of the limitation of claim 1 but does not explicitly say "a merged cascode transistor circuit" as recited in the preamble. As disclosed in the MPEP 2111.02, preamble statement reciting purpose or intended use not given significant patentable weight if there is no structural difference between the claimed invention and prior art. Kinzer discloses a bi-directional switch that is structurally identical claimed by applicant. The exception is that Kinzer does not explicitly say merged cascode transistor. However, this feature is a purpose/intended use of the Applicant's device and does not structurally limit feature of the claim. The structure of the claim device is the same as that of the

prior art. Therefore, the claimed invention does not distinguish over the Kinzer's device. Note that a recitation of the purpose/intended use such as "merged gate cascode transistor" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the purpose/intended use, it meets the claim.

With regard to claim 2, Kinzer discloses (Fig.4) the merged gate transistor circuit 50 of claim 1, wherein the semiconductor element further comprises: a first III-Nitride layer 21; and a second III-Nitride layer 23 on which the first III-Nitride layer is positioned such that a 2DEG conduction layer 22 forms between the first and second III-Nitride layers, wherein the source electrode 25/26 and the drain electrode 25/26 are ohmically connected to the first III-Nitride layer (e.g. para [00320]).

With regard to claim 3, Kinzer discloses (Fig.4) the merged gate transistor circuit 50 of claim 2, further comprising an insulating layer (para[0035]) positioned between the first 32 and second gates 34 and the first III-Nitride layer 21 such that the first 32 and second gates 34 are capacitively coupled to the first III-Nitride layer 21.

With regard to claim 4, Kinzer disclose the merged gate transistor circuit 50 of claim 3, wherein the first III-Nitride layer 21 comprises AlGaN material (Fig.4), and the second III-Nitride layer 23 comprises GaN material (Fig.4).

With regard to claim 5, Kinzer disclose the merged gate transistor circuit 50 of claim 4, further comprising an insulating layer (para[0035]) positioned between the first 32 and second gates 34 and the first III-Nitride layer 21 such that the first and second gates 32/34 are capacitively coupled to the first III-Nitride layer 21 (Fig.4).

With regard to claims 6 and 7, applicant's claims 6, 7 do not distinguish over the Kinzer reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of "wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage and wherein the predetermined level is a pinch off voltage of the second portion of the transistor". Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device is, not what a device does" [emphasis in original]); In re King, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does

not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); In re Best, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and Ex parte Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

With regard to claim 8, Kinzer disclose the merged gate transistor circuit 50 of claim 7, wherein the insulation layer is comprised of silicon dioxide (para [0025]).

With regard to claim 9, Kinzer disclose the merged gate transistor circuit 50 of claim 8, wherein the insulation layer is comprised of silicon nitride (para [0025]).

4. Claims 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer in views of Koyama, Smart et al (US 7,052,942; Smart hereinafter) and Parikh.

With regard to claim 10, Kinzer et al discloses a merged cascade high electron mobility transistor circuit 50 (Fig.4) comprises: a first epitaxial layer 21 of III-Nitride material; a second epitaxial layer 23 of a III-Nitride material, in contact with the first epitaxial layer 21 such that a 2-dimensional electron gas conducting layer 22 is formed between the first 21 and second 23 epitaxial layers; a source electrode 25 electrically connected to the first epitaxial layer 21; a drain electrode 26 electrically connected to the first epitaxial layer 21 and spaced laterally from the source electrode; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and coupled to the first epitaxial layer to form a first portion (e.g. Fig. 4, portion of transistor 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode 26 and source electrode 25 and coupled to the first epitaxial layer 21 to form a second portion (e.g. Fig. 4, portion of transistor 34) of the transistor; and wherein the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, Kinzer discloses the claim limitations but does not explicitly disclose “an input voltage signal source, a constant voltage source having a predetermined constant voltage; wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between to the constant voltage source and a voltage at the source electrode reaches a predetermined level”. However, applicant’s above limitations directed to functional limitations as to depletion mode and enhancement mode transistor. The above limitations, particularly, an input voltage signal source and a constant voltage source having a predetermined constant voltage are bias voltages to the enhancement and depletion mode transistors that are required to operate/function of the device. Although Kinzer does not explicitly disclose an input voltage signal source and a constant voltage source having a predetermined constant voltage, Kinzer device inherently requires these bias condition to operate/function. However, for example, Figs. 1, 2, 5 and para[0008, 0049] of Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 devices. Since it is common knowledge to apply bias voltages to the gates of the depletion and enhancement mode devices for device operation, it would have been obvious to one having ordinary skill in the art at the time of the invention to include an input

voltage signal source and a constant voltage source having a predetermined constant voltage within Kinzer device to operate/function of the device.

As discussed above, Kinzer discloses all of the structural limitations of claims 10-16 with the exception of the device disclosed by Kinzer et al and that claimed lies in the recital of “epitaxial” layer, i.e. layers formed by epitaxy. However, Smart discloses forming an AlGaN layer by epitaxy over a GaN layer, also formed by epitaxy (col.1/2, lines 66-2). Smart’s epitaxially formed AlGaN and GaN layers create a 2DEG layer between them that creates the thin, high mobility channel (col.3/4, lines 64-1) needed for proper performance of the device disclosed by Kinzer. It therefore seems clear that one of ordinary skill in the art could have applied Smart’s known "improvement" technique to Kinzer’s "base" device in the same way Smart applies it to a “comparable” device and that in the view of one of skill in the art, the results would have predictably produced the 2DEG layer required by Kinzer’s device. See MPEP § 2143, part “C”.

As discussed above, Kinzer in views of Koyama and Smart discloses the limitations of the claim 10 with the exception of wherein the second gate includes a field plate. However, Fig.6 of Parikh discloses wherein the second gate 26 includes a field plate 28. According to para[0031] of Parikh, the field plate arrangement for both the HEMT and MESFET can reduce the peak electric field in the device, compared to a device without a field plate, which can result in

increased breakdown voltage and reduced trapping. The reduction of the electric field can also yield other benefits such as reduced leakage currents and enhanced reliability. It would have been obvious to one having ordinary skill in the art at the time of the invention to include a field plate within second gate as shown by Parikh within Kinzer's device to reduce leakage current and enhance reliability of the device.

Furthermore, Kinzer in views of Koyma, Smart and Parikh disclose all of the limitation of claim 10 but do not explicitly say "merged cascode high electron mobility transistor circuit" as recited in the preamble. As disclosed in the MPEP 2111.02, preamble statement reciting purpose or intended use not given significant patentable weight if there is no structural difference between the claimed invention and prior art. Kinzer discloses a bi-directional switch that is structurally identical claimed by applicant. The exception is that Kinzer does not explicitly say "merged cascode high electron mobility transistor". However, this feature is a purpose/intended use of the Applicant's device and does not structurally limit feature of the claim. The structure of the claim device is the same as that of the prior art. Therefore, the claimed invention does not distinguish over the Kinzer's device. Note that a recitation of the purpose/intended use such as "merged cascode high electron mobility transistor" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed

invention from the prior art. If the prior art structure is capable of performing the purpose/intended use, it meets the claim.

With regard to claim 11, Kinzer discloses (Fig.4) the merged cascode high electron mobility transistor circuit 50 of claim 10, further comprising an insulating layer (para[0035]) positioned between the first 32 and second gates 34 and the first epitaxial layer 21.

With regard to claim 12, Kinzer disclose the merged gate transistor circuit 50 of claim 11, wherein the first III-Nitride layer 21 comprises AlGaN material (Fig.4), and the second III-Nitride layer 23 comprises GaN material (Fig.4).

With regard to claims 13 and 14, applicant's claims 13, 14 do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of "wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage and wherein the predetermined level is a pinch off voltage of the second portion of the transistor". Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover

what a device is, not what a device does" [emphasis in original]); In re King, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); In re Best, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and Ex parte Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

With regard to claim 15, Kinzer disclose the merged gate transistor 50 of claim 14, wherein the insulation layer is comprised of silicon dioxide (para [0025]).

With regard to claim 16, Kinzer et al disclose the merged gate transistor of claim 14, wherein the insulation layer is comprised of silicon nitride (para [0025]).

**Conclusion**

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on (571)272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SELIM AHMED/
Examiner, Art Unit 2826

/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2826

| Notice of References Cited | Application/Control No. 11/688,338 | Applicant(s)/Patent Under Reexamination HERMAN, THOMAS | |
|---|---|---|---|
| | Examiner SELIM AHMED | Art Unit 2826 | Page 1 of 1 |

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| * | B | US-2005/0051796 A1 | 03-2005 | Parikh et al. | 257/192 |
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| | E | US- | | | |
| | F | US- | | | |
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11688338 | HERMAN, THOMAS |
| | **Examiner** | **Art Unit** |
| | SELIM AHMED | 2826 |

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|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 05/22/2008 | 12/08/2008 | 03/20/2009 | 06/20/2009 | 09/25/2010 | 04/09/2011 | 12/17/2011 | | |
| | 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 3 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 5 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 6 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 7 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 8 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 9 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 10 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 11 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 12 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 13 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 14 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 15 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | 16 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11688338 | HERMAN, THOMAS |
| | Examiner | Art Unit |
| | SELIM AHMED | 2826 |

## SEARCHED

| Class | Subclass | Date | Examiner |
|---|---|---|---|
| 257 | 192, 194, 195, E29.14, E29.144, E29.246, E29.249 | 5/22/08 | SA |
| | Updated search | 12/8/08 | /sa/ |
| | Updated search | 3/20/2009 | /sa/ |
| | Updated search | 6/20/2009 | /sa/ |
| | Updated search | 9/24/2010 | /sa/ |
| | Updated search | 4/9/2011 | /sa/ |
| | Updated search | 12/17/2011 | /sa/ |

## SEARCH NOTES

| Search Notes | Date | Examiner |
|---|---|---|
| Text search such as two dimensional electron gas, Cascode transistor, HEMT/High electron mobility transistor, source, drain, gate and their boolean combinations were searched. | 5/22/08 | SA |
| Updated search | 12/8/2008 | /sa/ |
| Updated search | 3/20/2009 | /sa/ |
| Updated search | 9/24/2010 | /sa/ |
| Updated search | 4/9/2011 | /sa/ |
| Updated search | 12/11/2011 | /sa/ |

## INTERFERENCE SEARCH

| Class | Subclass | Date | Examiner |
|---|---|---|---|
| 257 | 192, 194, 195, | 5/22/08 | SA |

**EAST Search History**

**EAST Search History (Prior Art)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| S3 | 4541 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:21 |
| S4 | 7876 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S5 | 314831 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S6 | 73 | S3 and S4 and S5 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S7 | 96 | S3 and S4 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:23 |
| S8 | 63 | S6 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:23 |
| S9 | 82 | S7 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:24 |
| S10 | 5 | ("5155449" \| "5774792" \| "5939945" \| | US-PGPUB; | OR | OFF | 2008/05/21 |

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| S12 | 1404 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:53 |
| S13 | 1116 | S5 and S12 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:54 |
| S14 | 356 | S5 and S12 and S4 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:54 |
| S15 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:00 |
| S16 | 5 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:01 |
| S17 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:05 |
| S18 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/21 18:20 |
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| S22 | 773 | S5 and S20 and S4 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:29 |
| S23 | 706 | S22 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:30 |
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| S25 | 275 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:46 |
| S26 | 232 | S25 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:46 |
| S27 | 232 | S25 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:46 |
| S28 | 121 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/22 10:38 |
| S29 | 310043 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/22 15:10 |
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| S31 | 852 | S29 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | OFF | 2008/05/22 15:11 |

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| S32 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
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| S34 | 4811 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S35 | 8419 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S36 | 332843 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S37 | 80 | S34 and S35 and S36 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S38 | 107 | S34 and S35 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S39 | 65 | S37 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
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| S44 | 1137 | S36 and S43 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S45 | 365 | S36 and S43 and S35 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
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| S47 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S48 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
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| S52 | 1310 | S36 and S51 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S53 | 847 | S36 and S51 and S35 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S54 | 725 | S53 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S55 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S56 | 312 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S57 | 244 | S56 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S58 | 244 | S56 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S59 | 125 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S60 | 321547 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S61 | 596 | S60 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |

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| S63 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S64 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S65 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S66 | 82 | S63 and S64 and S65 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S67 | 66 | S66 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S68 | 1 | S67 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S69 | 8 | S67 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:05 |
| S70 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | OFF | 2009/03/19 18:13 |

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| | | | DERWENT; IBM_TDB | | | |
| S71 | 944 | S70 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:13 |
| S72 | 549 | S71 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:13 |
| S73 | 213 | S72 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:14 |
| S74 | 15 | S73 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:15 |
| S75 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:27 |
| S76 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:27 |
| S77 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/19 18:31 |
| S78 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S79 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; | OR | ON | 2009/03/20 00:20 |

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| | | | USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S80 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S81 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S82 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S83 | 82 | S80 and S81 and S82 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S84 | 109 | S80 and S81 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S85 | 66 | S83 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S86 | 86 | S84 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S87 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S88 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |

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| | | ("7026669").URPN. | | | | |
| S89 | 1438 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S90 | 1150 | S82 and S89 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S91 | 373 | S82 and S89 and S81 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S92 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S93 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S94 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S95 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S96 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S97 | 1868 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S98 | 1378 | S82 and S97 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S99 | 896 | S82 and S97 and S81 | US-PGPUB; USPAT; | OR | OFF | 2009/03/20 00:20 |

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| | | | USOCR | | | |
| S100 | 737 | S99 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S101 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S102 | 334 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S103 | 246 | S102 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S104 | 246 | S102 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S105 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S106 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S107 | 622 | S106 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S108 | 944 | S106 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S109 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/03/20 00:20 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S110 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S111 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S112 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S113 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S114 | 82 | S111 and S112 and S113 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S115 | 109 | S111 and S112 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S116 | 66 | S114 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S117 | 86 | S115 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S118 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR | US-PGPUB; USPAT; | OR | OFF | 2009/03/20 00:20 |

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| | | ("7071786").URPN. | USOCR | | | |
| S119 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S120 | 1438 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S121 | 1150 | S113 and S120 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S122 | 373 | S113 and S120 and S112 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S123 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S124 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S125 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S126 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S127 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S128 | 1868 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |

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| S129 | 1378 | S113 and S128 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S130 | 896 | S113 and S128 and S112 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S131 | 737 | S130 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S132 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S133 | 334 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S134 | 246 | S133 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S135 | 246 | S133 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S136 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S137 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S138 | 622 | S137 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S139 | 944 | S137 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | OFF | 2009/03/20 00:20 |

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| | | | IBM_TDB | | | |
| S140 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S141 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S142 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S143 | 82 | S140 and S141 and S142 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S144 | 66 | S143 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S145 | 1 | S144 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S146 | 8 | S144 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S147 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S148 | 944 | S147 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | OFF | 2009/03/20 00:20 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S149 | 549 | S148 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S150 | 213 | S149 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S151 | 15 | S150 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S152 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S153 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S154 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S155 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S156 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S157 | 5068 | cascode near3 transistor$1 | US-PGPUB; | OR | ON | 2009/06/18 |

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| | | | USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | 12:52 |
| S158 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S159 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S160 | 85 | S157 and S158 and S159 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S161 | 116 | S157 and S158 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S162 | 67 | S160 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S163 | 89 | S161 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S164 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S165 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S166 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | ON | 2009/06/18 12:52 |

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| | | | DERWENT; IBM_TDB | | | |
| S167 | 1162 | S159 and S166 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S168 | 378 | S159 and S166 and S158 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S169 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S170 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S171 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S172 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S173 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S174 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S175 | 1427 | S159 and S174 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S176 | 930 | S159 and S174 and S158 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S177 | 745 | S176 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | ON | 2009/06/18 12:52 |

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| | | | DERWENT; IBM_TDB | | | |
| S178 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S179 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S180 | 248 | S179 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S181 | 248 | S179 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S182 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S183 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S184 | 641 | S183 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S185 | 977 | S183 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S186 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S187 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; | OR | ON | 2009/06/18 12:52 |

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| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S188 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S189 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S190 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S191 | 85 | S188 and S189 and S190 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S192 | 116 | S188 and S189 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S193 | 67 | S191 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S194 | 89 | S192 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S195 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S196 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |

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| S197 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S198 | 1162 | S190 and S197 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S199 | 378 | S190 and S197 and S189 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S200 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S201 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S202 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S203 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S204 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S205 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S206 | 1427 | S190 and S205 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S207 | 930 | S190 and S205 and S189 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |

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| S208 | 745 | S207 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S209 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S210 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S211 | 248 | S210 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S212 | 248 | S210 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S213 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S214 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S215 | 641 | S214 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S216 | 977 | S214 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S217 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | ON | 2009/06/18 12:52 |

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| | | | IBM_TDB | | | |
| S218 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S219 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S220 | 85 | S217 and S218 and S219 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S221 | 67 | S220 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S222 | 1 | S221 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S223 | 8 | S221 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S224 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S225 | 977 | S224 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S226 | 567 | S225 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/18 12:52 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S227 | 217 | S226 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S228 | 18 | S227 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S229 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S230 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S231 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S232 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S233 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S234 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S235 | 8964 | HEMT or (high near electron near | US-PGPUB; | OR | ON | 2009/06/18 |

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| | | mobility near transistor) | USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | 12:52 |
| S236 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S237 | 85 | S234 and S235 and S236 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S238 | 116 | S234 and S235 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S239 | 67 | S237 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S240 | 89 | S238 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S241 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S242 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S243 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S244 | 1162 | S236 and S243 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | ON | 2009/06/18 12:52 |

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| | | | DERWENT; IBM_TDB | | | |
| S245 | 378 | S236 and S243 and S235 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S246 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S247 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S248 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S249 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S250 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S251 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S252 | 1427 | S236 and S251 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S253 | 930 | S236 and S251 and S235 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S254 | 745 | S253 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S255 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S256 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; | OR | OFF | 2009/06/18 12:52 |

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| | | | USOCR | | | |
| S257 | 248 | S256 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S258 | 248 | S256 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S259 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S260 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S261 | 641 | S260 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S262 | 977 | S260 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S263 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S264 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S265 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/18 12:52 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S266 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S267 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S268 | 85 | S265 and S266 and S267 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S269 | 116 | S265 and S266 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S270 | 67 | S268 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S271 | 89 | S269 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S272 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S273 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S274 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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| S275 | 1162 | S267 and S274 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S276 | 378 | S267 and S274 and S266 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S277 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S278 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S279 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S280 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S281 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S282 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S283 | 1427 | S267 and S282 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S284 | 930 | S267 and S282 and S266 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S285 | 745 | S284 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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| S286 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S287 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S288 | 248 | S287 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S289 | 248 | S287 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S290 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S291 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S292 | 641 | S291 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S293 | 977 | S291 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S294 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S295 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | ON | 2009/06/18 12:52 |

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|---|---|---|---|---|---|---|
| | | | IBM_TDB | | | |
| S296 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S297 | 85 | S294 and S295 and S296 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S298 | 67 | S297 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S299 | 1 | S298 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S300 | 8 | S298 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S301 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S302 | 977 | S301 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S303 | 567 | S302 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S304 | 217 | S303 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | OFF | 2009/06/18 12:52 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S305 | 18 | S304 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S306 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S307 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S308 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S310 | 8 | ("5629539" \| "5691252" \| "5990507" \| "6174735" \| "6245631" \| "6278150" \| "6291292" \| "6337274").PN. OR ("6707088").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 13:08 |
| S314 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S315 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S316 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S317 | 85 | S314 and S315 and S316 | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/20 16:18 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S318 | 116 | S314 and S315 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S323 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S324 | 1162 | S316 and S323 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S331 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S332 | 1427 | S316 and S331 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S333 | 930 | S316 and S331 and S315 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S335 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S337 | 248 | S336 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S340 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S342 | 977 | S340 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S345 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; | OR | ON | 2009/06/20 16:18 |

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| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S346 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S347 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S348 | 85 | S345 and S346 and S347 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S349 | 116 | S345 and S346 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S354 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S355 | 1162 | S347 and S354 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S362 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S363 | 1427 | S347 and S362 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S364 | 930 | S347 and S362 and S346 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S366 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S368 | 248 | S367 and @ad<"20060320" | US-PGPUB; USPAT; | OR | ON | 2009/06/20 16:18 |

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| | | | USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S371 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S373 | 977 | S371 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S374 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S375 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S376 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S377 | 85 | S374 and S375 and S376 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S378 | 67 | S377 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S381 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |

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| S382 | 977 | S381 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S383 | 567 | S382 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S391 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S392 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S393 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S394 | 85 | S391 and S392 and S393 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S395 | 116 | S391 and S392 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S400 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S401 | 1162 | S393 and S400 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | ON | 2009/06/20 16:18 |

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| | | | DERWENT; IBM_TDB | | | |
| S408 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S409 | 1427 | S393 and S408 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S410 | 930 | S393 and S408 and S392 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S412 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S414 | 248 | S413 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S417 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S419 | 977 | S417 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S422 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S423 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S424 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S425 | 85 | S422 and S423 and S424 | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/20 16:18 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S426 | 116 | S422 and S423 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S431 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S432 | 1162 | S424 and S431 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S439 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S440 | 1427 | S424 and S439 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S441 | 930 | S424 and S439 and S423 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S443 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S445 | 248 | S444 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S448 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S450 | 977 | S448 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S451 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; | OR | ON | 2009/06/20 16:18 |

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| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S452 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S453 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S454 | 85 | S451 and S452 and S453 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S455 | 67 | S454 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S458 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S459 | 977 | S458 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S460 | 567 | S459 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S468 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S469 | 8964 | HEMT or (high near electron near | US-PGPUB; | OR | ON | 2009/06/20 |

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|---|---|---|---|---|---|---|
| | | mobility near transistor) | USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | 16:18 |
| S470 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S471 | 85 | S468 and S469 and S470 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S472 | 116 | S468 and S469 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S477 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S478 | 1162 | S470 and S477 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S485 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S486 | 1427 | S470 and S485 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S487 | 930 | S470 and S485 and S469 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S489 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S491 | 248 | S490 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |

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| S494 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S496 | 977 | S494 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S499 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S500 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S501 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S502 | 85 | S499 and S500 and S501 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S503 | 116 | S499 and S500 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S508 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S509 | 1162 | S501 and S508 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; | OR | ON | 2009/06/20 16:18 |

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| | | | DERWENT; IBM_TDB | | | |
| S516 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S517 | 1427 | S501 and S516 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S518 | 930 | S501 and S516 and S500 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S520 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S522 | 248 | S521 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S525 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S527 | 977 | S525 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S528 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S529 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S530 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S531 | 85 | S528 and S529 and S530 | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/20 16:18 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S532 | 67 | S531 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S535 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S536 | 977 | S535 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S537 | 567 | S536 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S545 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S546 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S549 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S550 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S551 | 349967 | source and drain and gate | US-PGPUB; USPAT; | OR | ON | 2009/06/20 16:22 |

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| | | | USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S552 | 85 | S549 and S550 and S551 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S553 | 116 | S549 and S550 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S558 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S559 | 1162 | S551 and S558 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S566 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S567 | 1427 | S551 and S566 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S568 | 930 | S551 and S566 and S550 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S570 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S572 | 248 | S571 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S575 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S577 | 977 | S575 and HEMT | US-PGPUB; | OR | OFF | 2009/06/20 |

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| | | | USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | 16:22 |
| S580 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S581 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S582 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S583 | 85 | S580 and S581 and S582 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S584 | 116 | S580 and S581 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S589 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S590 | 1162 | S582 and S589 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S597 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S598 | 1427 | S582 and S597 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |

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| S599 | 930 | S582 and S597 and S581 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S601 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S603 | 248 | S602 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S606 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S608 | 977 | S606 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S609 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S610 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S611 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S612 | 85 | S609 and S610 and S611 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S613 | 67 | S612 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | ON | 2009/06/20 16:22 |

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| | | | IBM_TDB | | | |
| S616 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S617 | 977 | S616 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S618 | 567 | S617 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S626 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S627 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S628 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S629 | 85 | S626 and S627 and S628 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S630 | 116 | S626 and S627 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S635 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/20 16:22 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S636 | 1162 | S628 and S635 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S643 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S644 | 1427 | S628 and S643 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S645 | 930 | S628 and S643 and S627 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S647 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S649 | 248 | S648 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S652 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S654 | 977 | S652 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S657 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S658 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S659 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; | OR | ON | 2009/06/20 16:22 |

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| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S660 | 85 | S657 and S658 and S659 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S661 | 116 | S657 and S658 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S666 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S667 | 1162 | S659 and S666 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S674 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S675 | 1427 | S659 and S674 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S676 | 930 | S659 and S674 and S658 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S678 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S680 | 248 | S679 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S683 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S685 | 977 | S683 and HEMT | US-PGPUB; USPAT; | OR | OFF | 2009/06/20 16:22 |

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| | | | USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S686 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S687 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S688 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S689 | 85 | S686 and S687 and S688 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S690 | 67 | S689 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S693 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S694 | 977 | S693 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S695 | 567 | S694 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |

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| S703 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S704 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S705 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S706 | 85 | S703 and S704 and S705 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S707 | 116 | S703 and S704 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S712 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S713 | 1162 | S705 and S712 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S720 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S721 | 1427 | S705 and S720 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S722 | 930 | S705 and S720 and S704 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S724 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; | OR | OFF | 2009/06/20 16:22 |

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| | | | USOCR | | | |
| S726 | 248 | S725 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S729 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S731 | 977 | S729 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S734 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S735 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S736 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S737 | 85 | S734 and S735 and S736 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S738 | 116 | S734 and S735 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S743 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2009/06/20 16:22 |

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| | | | JPO; DERWENT; IBM_TDB | | | |
| S744 | 1162 | S736 and S743 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S751 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S752 | 1427 | S736 and S751 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S753 | 930 | S736 and S751 and S735 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S755 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S757 | 248 | S756 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S760 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S762 | 977 | S760 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S763 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S764 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S765 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; | OR | ON | 2009/06/20 16:22 |

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|---|---|---|---|---|---|---|
| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |
| S766 | 85 | S763 and S764 and S765 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S767 | 67 | S766 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S770 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S771 | 977 | S770 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S772 | 567 | S771 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S780 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S781 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S782 | 7165 | HEMT or (high near electron near mobility near transistor) or HFET | US-PGPUB; USPAT | OR | ON | 2010/09/24 16:32 |
| S783 | 816 | S782 and input and (Vdd or power adj supply) and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; | OR | ON | 2010/09/24 16:33 |

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|---|---|---|---|---|---|---|
| | | | IBM_TDB | | | |
| S784 | 593 | S783 and (gate and drain and source) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 16:34 |
| S785 | 79 | S784 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/09/24 16:34 |
| S786 | 79 | S783 and ((gate near4 input) and (drain near4 (Vdd or power adj supply))) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 17:39 |
| S787 | 108 | S782 and ((gate near4 input) and (drain near4 (Vdd or power adj supply))) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 17:46 |
| S788 | 79 | S787 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 17:47 |
| S789 | 37 | ((gate adj voltage) near5 (depletion adj mode)) same ((gate adj voltage) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 17:55 |
| S790 | 2 | 257/192.ccls. and ((gate adj voltage) near5 (depletion adj mode)) and ((gate adj voltage) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 18:03 |
| S791 | 9 | HEMT and ((gate adj voltage) near5 (depletion adj mode)) and ((gate adj voltage) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 18:04 |
| S792 | 26 | HEMT and ((voltage bias) near5 (depletion adj mode)) and ((voltage bias) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 19:59 |
| S793 | 12 | ((voltage bias) with (depletion adj mode) with ground) same ((gate adj voltage) with (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 20:36 |
| S794 | 484 | ((voltage bias) near5 (depletion adj mode)) and ((voltage bias) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 20:39 |

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|---|---|---|---|---|---|---|
| S795 | 7 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2011/04/09 01:31 |
| S796 | 0 | 2005/000700 | US-PGPUB; USPAT; USOCR | OR | ON | 2011/04/09 11:35 |
| S797 | 2 | 2005/0007200 | US-PGPUB; USPAT; USOCR | OR | ON | 2011/04/09 11:35 |
| S798 | 0 | 2005/0007200 | US-PGPUB | OR | ON | 2011/04/09 11:36 |
| S799 | 2 | 10/873291 | US-PGPUB; USPAT; USOCR | OR | ON | 2011/04/09 11:37 |
| S800 | 23 | ((voltage bias) with (depletion adj mode) with ground) and ((gate adj voltage) with (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:48 |
| S801 | 6181 | HEMT or (high near electron near mobility near transistor) and ((voltage bias) with (depletion adj mode)) and ((gate adj voltage) with (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:51 |
| S802 | 6180 | HEMT or (high near electron near mobility near transistor) and (((voltage bias) with (depletion adj mode)) with ((gate adj voltage) with (enhancement adj mode))) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:52 |
| S803 | 0 | S802 and merged near cascode | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:54 |
| S804 | 234 | S802 and cascode | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:54 |
| S805 | 11916 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2011/12/13 14:46 |
| S806 | 7652 | S805 | US-PGPUB; USPAT | OR | ON | 2011/12/13 14:46 |
| S807 | 18 | S805 and (filed adj plat$3 with gate) | US-PGPUB; USPAT | OR | ON | 2011/12/13 14:46 |
| S808 | 329 | S805 and (field adj plat$3 with gate) | US-PGPUB; USPAT | OR | ON | 2011/12/13 14:46 |
| S809 | 155 | S808 and (@ad<"20060320" or @rlad<"20060320") | US-PGPUB; USPAT | OR | ON | 2011/12/13 14:48 |
| S810 | 4 | "10930160" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2011/12/13 17:00 |
| S811 | 15 | "10/930160" | US-PGPUB; USPAT; USOCR; FPRS; EPO; | OR | ON | 2011/12/13 17:00 |

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|---|---|---|---|---|---|---|
| | | | JPO; DERWENT; IBM_TDB | | | |

**EAST Search History (Interference)**

< This search history is empty>

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# BIB DATA SHEET

**CONFIRMATION NO. 9886**

| SERIAL NUMBER | FILING or 371(c) DATE<br>RULE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | 257 | 2826 | 0400131 |

**APPLICANTS**
Thomas Herman, Manhattan Beach, CA;

**** CONTINUING DATA ***************************
This appln claims benefit of 60/783,934 03/20/2006

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/29/2007

| Foreign Priority claimed ☐ Yes ☑ No<br>35 USC 119(a-d) conditions met ☐ Yes ☑ No<br>Verified and Acknowledged /SELIM U AHMED/ Examiner's Signature | ☐ Met after Allowance<br>Initials | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|
| | | CA | 4 | 16 | 2 |

**ADDRESS**

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691
UNITED STATES

**TITLE**

MERGED GATE CASCODE TRANSISTOR

| FILING FEE RECEIVED | FEES: Authority has been given in Paper | ☐ All Fees |
|---|---|---|
| 1130 | No._____ to charge/credit DEPOSIT ACCOUNT | ☐ 1.16 Fees (Filing) |
| | No._____ for following: | ☐ 1.17 Fees (Processing Ext. of time) |
| | | ☐ 1.18 Fees (Issue) |
| | | ☐ Other _____ |
| | | ☐ Credit |

| FORM PTO-1449 | ATTY. DOCKET NO. 0400131 | SERIAL NO. 11/688,338 |
|---|---|---|
| LIST OF PATENTS AND OTHER ITEMS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT | APPLICANTS: Herman, Thomas | |
| (Use several sheets if necessary) | FILING DATE: March 20, 2007 | GROUP ART: 2826 |

**U.S. PATENT DOCUMENTS**

| Exam. Initials | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|---|---|---|---|---|---|---|---|
| | AA | | | | | | |
| | AB | | | | | | |

**FOREIGN PATENT DOCUMENT**

| Exam. Initials | | DOCUMENT NUMBER | PUBLICATION DATE | COUNTRY OR PATENT OFFICE | CLASS | SUB CLASS | TRANSLATION YES | TRANSLATION NO |
|---|---|---|---|---|---|---|---|---|
| | BA | | | | | | | |
| | BB | | | | | | | |

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)**

| | | |
|---|---|---|
| | CA | Tietze, et al., Halbleiter-Schaltungstechnik, 12. Auflage, Berlin: Springer, 2002, Pages 316-317 |

| EXAMINER: /Selim Ahmed/ | DATE CONSIDERED: 12/13/2011 |
|---|---|

EXAMINER: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.



PAGE 5/11 * RCVD AT 4/13/2011 1:20:07 PM [Eastern Daylight Time] * SVR:W-PTOFAX-001/25 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):02-59

 REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.A./

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SEP 12 2011

# REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

| | |
|---|---|
| *Application Number* | 11/688,338 |
| *Filing Date* | 3/20/2007 |
| *First Named Inventor* | Herman |
| *Group Art Unit* | 2826 |
| *Examiner Name* | Ahmed, Selim U. |
| *Attorney Docket Number* | 0400131 |

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

*NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53 (d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice,* Final Rule, 65 *Fed Reg.* 50092 (Aug. 16, 2000); Interim Rule, 65 *Fed. Reg.* 14865 (Mar. 20, 2000), 1233 *Off. Gaz. Pat Office* 47 (Apr. 11, 2000), which established RCE practice.

1. Submission required under 37 C.F.R. § 1.114

a. ☐ Previously submitted
   i. ☐ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on _____ (Any unentered amendment(s) referred to above will be entered).
   ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
   iii. ☐ Other _____

b. ☒ Enclosed
   i. ☒ Amendment/Reply
   ii. ☐ Affidavit(s)/Declaration(s)
   iii. ☐ Information Disclosure Statement (IDS)
   iv. ☐ Other _____

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R.§ 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months, Fee under 37 C.F.R. § 1.17(i) required).

b. ☐ Other _____

3. Fees The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-0731
   i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)
   ii. ☒ Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)
   iii. ☒ Other _____

b. ☐ Check in the amount of $ _____ enclosed.

c. ☒ Payment by credit card for the amount of $ **1,300.00** (Form PTO-2038 enclosed).

| *SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED* | | | |
|---|---|---|---|
| *Name (Print/Type)* | Michael Farjami, Esq. | *Registration No. (Attorney/Agent)* | 38135 |
| *Signature* | | *Date* | 9/12/11 |

*CERTIFICATE OF MAILING OR TRANSMISSION*

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office on:

| | | | |
|---|---|---|---|
| *Name (Print/Type)* | Nicole Humphers | | |
| *Signature* | NHumphers | *Date* | 9.12.11 |

09/13/2011 HMARZI1 00000011 11688338

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Attorney Docket No.: 0400131

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| | |
|---|---|
| In re Application of: **Herman, Thomas** | Art Unit: 2826 |
| Serial No.: 11/688,338 | Examiner: Ahmed, Selim U. |
| Filed: 03/20/2007 | |
| For: **Merged Gate Cascode Transistor** | |

## AMENDMENT AND RESPONSE TO *ADVISORY ACTION*

**Mail Stop RCE**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the ***Advisory Action*** dated August 18, 2011 in the above-referenced patent application. Please enter and consider the following amendments and remarks in light of the attached ***Request for Continued Examination*** filed under 37 CFR § 1.114 in the above-identified application.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

09/13/2011 HMARZI1 00000011 11688338
02 FC:1252 490.00 OP

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**In the Claims:**

**Claim 1 (currently amended):** A merged cascode transistor circuit comprising:

an input voltage signal source;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a semiconductor element;

a source electrode electrically connected to a top surface of the semiconductor element;

a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;

a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;



PAGE 5/23 * RCVD AT 9/12/2011 7:27:24 PM [Eastern Daylight Time] * SVR:W-PTOFAX-002/12 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):09-16

wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

**Claim 2 (previously presented):** The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:

a first III-Nitride layer; and

a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

**Claim 3 (previously presented):** The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates





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and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 4 (previously presented):** The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

**Claim 5 (previously presented):** The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 6 (previously presented):** The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claim 7 (previously presented):** The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.

**Claim 8 (previously presented):** The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

**Claim 9 (previously presented):** The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

**Claim 10 (currently amended):** A merged cascode high electron mobility transistor circuit comprises:

an input voltage signal source;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a first epitaxial layer of III-Nitride material;

a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

a source electrode electrically connected to the first epitaxial layer;

a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;





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a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and

a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;

wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

**Claim 11 (original):** The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

**Claim 12 (previously presented):** The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGaN material and the second epitaxial layer comprises a GaN material.

**Claim 13 (original):** The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claims 14 (previously presented):** The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

**Claim 15 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

**Claim 16 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.





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## REMARKS

Prior to the present response, claims 1-16 were pending in the present application. By the present amendment and response, Applicant has amended independent claims 1 and 10. Thus, claims 1-16 remain in the present application. Applicant respectfully requests reconsideration and allowance of pending claims 1-16 in view of the above amendments and the following remarks.

### A. Rejection of Claims 1-16 under 35 U.S.C. § 103(a)

In the Advisory Action dated August 18, 2011 (hereinafter "Advisory Action") the Examiner has reapplied the rejections asserted against claims 1-16 by the Office Action dated April 12, 2011 (hereinafter "Final Rejection"), by which claims 1-16 were held to be unpatentable for purported obviousness under 35 U.S.C. § 103(a) over U.S. Patent Application Publication Number 2005/0189561 by Kinzer et al. (hereinafter "Kinzer") in view of U.S. Patent Application Publication Number 2004/0188761 by Koyama et al. (hereinafter "Koyama"). *See* page 1, items 1, 3, and 7 of the Advisory Action, and pages 2-14, item 2 of the Final Rejection. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by currently amended independent claims 1 and 10, is patentably distinguishable over Kinzer and Koyama.

The present invention, as defined by currently amended independent claims 1 and 10, provides a circuit including an input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor including a first





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gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor, and a second gate, including a field plate, positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, where the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate includes a field plate and is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. *See* currently amended independent claims 1 and 10 above. Claim 10 further defines that the transistor is a high electron mobility transistor (HEMT) wherein first and second epitaxial layers of III-nitride material in contact with each other such that a 2-dimensional electron gas conducting layer is formed between the layers are in place of the semiconductor element. *See* currently amended independent claim 10 above. Claims 1 and 10 have been amended such that the second gate electrode includes a field plate. Support for these amendments can be found in at least paragraph [0021] and figures 3 and 4 of the present application.

In an embodiment of the invention shown in Figure 3 of the present application, HEMT 30 includes first portion Q1 including gate 32, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source

contact 31 and drain contact 34. *See* paragraph [0023] and Figure 3 of the present application. HEMT 30 also includes second portion Q2 including gate 33, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source contact 31 and drain contact 34. In HEMT 30, node 24 is between first portion Q1 and second portion Q2. *See id.* at Figure 3, Figure 2 and related text, and paragraph [0023].

As disclosed in the present application, in an embodiment of the present invention, first portion Q1 is an enhancement mode transistor (normally OFF) and second portion Q2 is a depletion mode transistor (normally ON). *See* paragraph [0023] and Figure 3 of the present application. Further disclosed in the present application, an input voltage signal is connected to gate 32 provide a gate voltage Vg1. *See id.* at paragraph [0016]. Furthermore, a voltage is connected to gate 33 to provide a set voltage to Vg2, for example 0v. *See id.* at Figure 3 and paragraphs [0025] and [0017]. When the input voltage at Vg1 goes low, the first portion Q1 turns OFF. As a result, the voltage at the node 24 rises until the gate-source voltage of second portion Q2 reaches a set pinch off voltage and the second portion Q2 turns OFF. *See id.* at paragraph [0018]. Thus, an embodiment of the present invention advantageously provides for a circuit where the drain swing of the first portion Q1 is substantially reduced. *Id.*

In contrast to the present invention as defined by currently amended independent claims 1 and 10, Kinzer fails to disclose a circuit including an input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode

transistor where the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Kinzer specifically discloses device 40 in Figure 3 and device 50 in Figure 4.

The Examiner has asserted that an input voltage signal source connected to the gates of Kinzer's enhancement mode transistor and a constant voltage source having a predetermined constant voltage connected to the gates of Kinzer's depletion mode transistor are specifically required for devices 40 and 50 to operate or function. *See* pages 3-4 of the Final Rejection. Applicant respectfully maintains that this is incorrect. Although some bias must be applied to the gates of the two above described circuits of Kinzer, the specific arrangement where an input voltage signal source, and not a constant voltage source, is connected to the gates of the enhancement mode transistor and vice versa for the gates of the depletion mode transistor are not the only arrangements that would allow Kinzer's two embodiments to each function. Further, Applicant respectfully points out that applying a constant voltage source to one of the gates of enhancement mode transistor 50 would permanently block conduction through the transistor unless that constant voltage were a positive value sufficient enough to create a channel under that

gate. Thus, Applicant respectfully asserts that the specific arrangement disclosed in the present application is not required for Kinzer's structures to function.

Additionally, the Examiner has asserted that the requirement that the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor is a functional distinction. *See* pages 4-5 of the Final Rejection. Applicant respectfully disagrees and maintains that whether a device includes an enhancement mode transistor or a depletion mode transistor is a structural distinction. Inherently, an enhancement mode portion and a depletion mode portion must be structurally different from either two enhancement mode portions or two depletion mode portions, as specifically disclosed in Kinzer. For example, in the present application, first portion Q1 can be an enhancement mode transistor by using a recessed gate, fluorine implants, or other suitable means. *See* paragraph [0023] and Figure 3 of the present application. Thus, whether a device includes an enhancement mode transistor or a depletion mode transistor is a tangible distinction and not a functional distinction.

The Examiner has further asserted that it is reasonable to assume that Kinzer's devices 32, 34 are capable of performing in enhancement mode or depletion mode respectively because a comparison of Applicant's specification to Kinzer's disclosures reveals that Kinzer discloses a device that is apparently identical to the present invention. *See* pages 5-6 of the present application. However, as disclosed in Kinzer, device 40 is a depletion mode device (i.e. normally ON), having a logic NOR gate principle of operation, wherein an appropriate voltage applied to *either or both* gate electrode 32 or

gate electrode 34 causes an interruption in the 2DEG, thereby turning device 40 off. *See id.* at paragraphs [0033] and [0036], and Figure 3. Kinzer further discloses that device 40 displays symmetrical operation whereas the present invention, according to one embodiment, discloses that the drain voltage swing of the enhancement mode portion is substantially reduced and optimized for ultra-low voltage operation and the depletion mode portion may be optimized for stable higher voltage operation due to the specific arrangement of the depletion mode and enhancement mode portions of an embodiment of the present invention. *See* paragraphs [0020] and [0021] of the present application.

Further, Kinzer teaches that device 50 is an enhancement mode device (i.e. a normally off device) specifically due to the structural feature of two recesses 38 and is defined as performing an AND gate logic function such that current flows between electrodes 25, 26 when *both* gate electrodes 32, 34 have a potential applied to them. *See* paragraph [0039] of the present application. Similar to device 40, device 50 also displays symmetrical operation, contrary to the present invention. *See id.* at paragraph [0041]. It is important to note that nowhere does Kinzer disclose a device having both an enhancement mode portion and a depletion mode portion. Thus, Applicant respectfully asserts that Kinzer fails to disclose the present invention, according to either currently amended independent claim 1 or 10 of the present application.

Moreover, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *See*

*In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959) and MPEP §2143.01(VI). Applicant respectfully asserts that the combination of device 40 and device 50 of Kinzer to create a merged cascode transistor, wherein a first portion of the merged cascode transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor would change the principles of operation of both devices 40 and 50 such that the combination would could not function as a NOR gate or an AND gate, respectively, and further, that the combined device would lose its operational symmetry. Thus, because the proposed modification would change the principle of operation of both devices 40 and 50, their combination is insufficient to render the claims prima facie obvious. Further, Applicant respectfully asserts, for the same reasons, that devices 40 and 50 of Kinzer do not necessarily or inherently possess the characteristics of the present invention.

Finally, the Examiner has asserted that, in stating that first and second gate electrodes 32, 34 are independently operable, Kinzer discloses that one gate may be of an enhancement mode while the other may be of a depletion mode. *See* page 20, item 4 of the Final Rejection. Applicant respectfully disagrees. In context, the specification of Kinzer simply teaches that each gate may be individually activated. Nowhere does Kinzer disclose or even suggest that a device containing both an enhancement mode portion and a depletion mode portion, rather only two separate devices 40 and 50, one having two enhancement mode portions, and the other having two depletion mode

portions. Additionally, Applicant respectfully asserts that Kinzer fails to disclose a second gate electrode including a field plate.

Turning to Koyama, Koyama is directed toward a source follower circuit, which can be operated without increasing a power supply voltage higher than a desired value, thus maintaining a low power supply voltage and low power consumption. *See* paragraph [0031] of Koyama. The Examiner states that Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 device, respectively. *See* page 4 of the Final Rejection. However, Koyama also fails to disclose or suggest a merged gate cascode transistor wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Applicant respectfully asserts that Koyama also fails to disclose or suggest a second gate including a field plate.

Thus, each of Kinzer and Koyama fail to disclose or suggest a merged gate cascode transistor wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor as well as a second gate including a field plate. Consequently, even if the Final Rejection had provided a reasonable incentive for one skilled in the art to combine the cited art references Kinzer and Koyama, Applicant respectfully submits that the resulting combination would still fail to disclose or suggest the present invention as defined by currently amended independent claims 1 and 10.

For the foregoing reasons, Applicant respectfully submits that at the time the present invention, as defined by currently amended independent claims 1 and 10, was made, the invention would not have been rendered obvious to one of ordinary skill in the art by the disclosures of Kinzer and Koyama, singly or in combination. Consequently, Applicant respectfully asserts that the invention described by currently amended independent claims 1 and 10 is patentably novel and inventive over Kinzer and Koyama. As such, claims 2-9 depending from and further limiting patentable independent claim 1, and claims 11-16, depending from and further limiting patentable independent claim 10 are also patentably novel and inventive over Kinzer and Koyama for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

**B. Rejection of Claims 10-16 under 35 U.S.C. §103(a)**

The Examiner has rejected claims 10-16 under 35 U.S.C. § 103(a) for purported obviousness over Kinzer in view of Koyama and in further view of U.S. Patent Number 7,052,942 to Smart et al. (hereinafter "Smart"). *See* page 1, items 1, 3, and 7 of the Advisory Action, and pages 14-19, item 3 of the Final Rejection. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by currently amended independent claim 10, is patentably distinguishable over Kinzer, Koyama, and Smart.

The present invention, as defined by amended independent claim 10, provides a circuit including input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor including a first epitaxial layer of III-Nitride material, a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers, a source electrode electrically connected to the first epitaxial layer, a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode, a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor, and a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor, where the first gate is connected the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. *See* currently amended independent claim 10 above.

For reasons similar to those presented above, Applicant respectfully asserts that neither Kinzer nor Koyama, or any combination of Kinzer and Koyama, discloses or





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suggests a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate including a field plate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, as specifically required by currently amended independent claim 10.

In the Final Rejection, the Examiner has suggested combining Kinzer and Koyama with Smart to overcome the omission from the combination of Kinzer and Koyama of any express teaching that the described III-Nitride (AlGaN and GaN) layers are epitaxial. *See* pages 16-17 of the Final Rejection. Smart specifically discloses HEMT 28 including GaN buffer layer 22 and AlGaN Schottky layer 24. *See* Figure 2 and related text of Smart. However, in Smart, HEMT 28 includes only a single gate contact 32. *Id.*

Thus, Smart, like Kinzer and Koyama, fails to disclose or suggest a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate, including a field plate, positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, as specified in currently amended independent claim 10. Consequently, Smart fails to cure the aforementioned deficiencies of Kinzer and Koyama. As such, Applicant submits that

the combination of Kinzer, Koyama and Smart suggested by the Examiner does not and cannot result in the present invention, as defined by currently amended independent claim 10.

For the foregoing reasons, Applicant respectfully submits that at the time the present invention as defined by currently amended independent claim 10 was made, the invention would not have been rendered obvious to one of ordinary skill in the art by the disclosures of Kinzer, Koyama, and Smart, singly or in combination. Consequently, Applicant respectfully asserts that the invention described by currently amended independent claim 10 is patentably novel and inventive over Kinzer, Koyama, and Smart. As such, claims 11-16, depending from and further limiting patentable independent claim 10 are also patentably novel and inventive over Kinzer, Koyama, and Smart for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

### C. Conclusion

Based on the foregoing reasons, Applicant respectfully submits that the present invention, as defined by currently amended independent claims 1 and 10, and claims depending therefrom, is patentably novel and inventive. Moreover, Applicant asserts that no new matter has been introduced herein. Thus, for all of the reasons presented above, Applicant respectfully requests an early allowance of claims 1-16 pending in the present application.

Attorney Docket No.: 0400131

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 9/12/11

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Date of Facsimile: 9.12.11

Nicole Humphers
Name of Person Performing Facsimile Transmission

N Humphers 9.12.11
Signature Date



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## FACSIMILE TRANSMISSION COVER SHEET

Date: September 12, 2011

To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826

Fax: (571) 273-8300

Re: **Application Serial No.: 11/688,338**
Filing Date: 3/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 23

Message:

Enclosed please find:

1) Request for Continued Examination
2) Amendment and Response to Advisory Action

Payment for Request for Continued Examination fee and Second Month Extension in the amount of $1,300.00 is hereby enclosed on form PTO-2038.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

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# REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

| | |
|---|---|
| *Application Number* | 11/688,338 |
| *Filing Date* | 3/20/2007 |
| *First Named Inventor* | Herman |
| *Group Art Unit* | 2826 |
| *Examiner Name* | Ahmed, Selim U. |
| *Attorney Docket Number* | 0400131 |

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

*NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53 (d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Final Rule, 65 Fed Reg. 50092 (Aug. 16, 2000); Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 Off. Gaz. Pat Office 47 (Apr. 11, 2000), which established RCE practice.*

1. Submission required under 37 C.F.R. § 1.114
   - a. ☐ Previously submitted
     - i. ☐ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on _____ (Any unentered amendment(s) referred to above will be entered).
     - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - iii. ☐ Other _____
   - b. ☒ Enclosed
     - i. ☒ Amendment/Reply
     - ii. ☐ Affidavit(s)/Declaration(s)
     - iii. ☐ Information Disclosure Statement (IDS)
     - iv. ☐ Other _____
2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months. Fee under 37 C.F.R. § 1.17(i) required)
   - b. ☐ Other _____
3. Fees — The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-0731
     - i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)
     - ii. ☒ Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)
     - iii. ☒ Other _____
   - b. ☐ Check in the amount of $ _____ enclosed.
   - c. ☒ Payment by credit card for the amount of **$ 1,300.00** (Form PTO-2038 enclosed).

| *SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED* | | | |
|---|---|---|---|
| *Name (Print/Type)* | Michael Farjami, Esq. | *Registration No. (Attorney/Agent)* | 38135 |
| *Signature* | | *Date* | 9/12/11 |

*CERTIFICATE OF MAILING OR TRANSMISSION*

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office on:

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| *Name (Print/Type)* | Nicole Humphers | | |
| *Signature* | Nhumphers | *Date* | 9.12.11 |

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Attorney Docket No.: 0400131

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| In re Application of: **Herman, Thomas** | Art Unit: 2826 |
| Serial No.: 11/688,338 | Examiner: Ahmed, Selim U. |
| Filed: 03/20/2007 | |
| For: **Merged Gate Cascode Transistor** | |

**AMENDMENT AND RESPONSE TO *ADVISORY ACTION***

**Mail Stop RCE**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the ***Advisory Action*** dated August 18, 2011 in the above-referenced patent application. Please enter and consider the following amendments and remarks in light of the attached ***Request for Continued Examination*** filed under 37 CFR § 1.114 in the above-identified application.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.



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**In the Claims:**

**Claim 1 (currently amended):** A merged cascode transistor circuit comprising:

an input voltage signal source;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a semiconductor element;

a source electrode electrically connected to a top surface of the semiconductor element;

a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;

a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;





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wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

**Claim 2 (previously presented):** The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:

a first III-Nitride layer; and

a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

**Claim 3 (previously presented):** The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates

and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 4 (previously presented):** The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

**Claim 5 (previously presented):** The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 6 (previously presented):** The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claim 7 (previously presented):** The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.

**Claim 8 (previously presented):** The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

**Claim 9 (previously presented):** The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

**Claim 10 (currently amended):** A merged cascode high electron mobility transistor circuit comprises:

an input voltage signal source;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a first epitaxial layer of III-Nitride material;

a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

a source electrode electrically connected to the first epitaxial layer;

a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;





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a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and

a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;

wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

**Claim 11 (original):** The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

**Claim 12 (previously presented):** The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGaN material and the second epitaxial layer comprises a GaN material.

**Claim 13 (original):** The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claims 14 (previously presented):** The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

**Claim 15 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

**Claim 16 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.





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## REMARKS

Prior to the present response, claims 1-16 were pending in the present application. By the present amendment and response, Applicant has amended independent claims 1 and 10. Thus, claims 1-16 remain in the present application. Applicant respectfully requests reconsideration and allowance of pending claims 1-16 in view of the above amendments and the following remarks.

### A. Rejection of Claims 1-16 under 35 U.S.C. § 103(a)

In the Advisory Action dated August 18, 2011 (hereinafter "Advisory Action") the Examiner has reapplied the rejections asserted against claims 1-16 by the Office Action dated April 12, 2011 (hereinafter "Final Rejection"), by which claims 1-16 were held to be unpatentable for purported obviousness under 35 U.S.C. § 103(a) over U.S. Patent Application Publication Number 2005/0189561 by Kinzer et al. (hereinafter "Kinzer") in view of U.S. Patent Application Publication Number 2004/0188761 by Koyama et al. (hereinafter "Koyama"). *See* page 1, items 1, 3, and 7 of the Advisory Action, and pages 2-14, item 2 of the Final Rejection. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by currently amended independent claims 1 and 10, is patentably distinguishable over Kinzer and Koyama.

The present invention, as defined by currently amended independent claims 1 and 10, provides a circuit including an input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor including a first





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gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor, and a second gate, including a field plate, positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, where the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate includes a field plate and is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. *See* currently amended independent claims 1 and 10 above. Claim 10 further defines that the transistor is a high electron mobility transistor (HEMT) wherein first and second epitaxial layers of III-nitride material in contact with each other such that a 2-dimensional electron gas conducting layer is formed between the layers are in place of the semiconductor element. *See* currently amended independent claim 10 above. Claims 1 and 10 have been amended such that the second gate electrode includes a field plate. Support for these amendments can be found in at least paragraph [0021] and figures 3 and 4 of the present application.

In an embodiment of the invention shown in Figure 3 of the present application, HEMT 30 includes first portion Q1 including gate 32, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source

contact 31 and drain contact 34. *See* paragraph [0023] and Figure 3 of the present application. HEMT 30 also includes second portion Q2 including gate 33, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source contact 31 and drain contact 34. In HEMT 30, node 24 is between first portion Q1 and second portion Q2. *See id.* at Figure 3, Figure 2 and related text, and paragraph [0023].

As disclosed in the present application, in an embodiment of the present invention, first portion Q1 is an enhancement mode transistor (normally OFF) and second portion Q2 is a depletion mode transistor (normally ON). *See* paragraph [0023] and Figure 3 of the present application. Further disclosed in the present application, an input voltage signal is connected to gate 32 provide a gate voltage Vg1. *See id.* at paragraph [0016]. Furthermore, a voltage is connected to gate 33 to provide a set voltage to Vg2, for example 0v. *See id.* at Figure 3 and paragraphs [0025] and [0017]. When the input voltage at Vg1 goes low, the first portion Q1 turns OFF. As a result, the voltage at the node 24 rises until the gate-source voltage of second portion Q2 reaches a set pinch off voltage and the second portion Q2 turns OFF. *See id.* at paragraph [0018]. Thus, an embodiment of the present invention advantageously provides for a circuit where the drain swing of the first portion Q1 is substantially reduced. *Id.*

In contrast to the present invention as defined by currently amended independent claims 1 and 10, Kinzer fails to disclose a circuit including an input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode

transistor where the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Kinzer specifically discloses device 40 in Figure 3 and device 50 in Figure 4.

The Examiner has asserted that an input voltage signal source connected to the gates of Kinzer's enhancement mode transistor and a constant voltage source having a predetermined constant voltage connected to the gates of Kinzer's depletion mode transistor are specifically required for devices 40 and 50 to operate or function. *See* pages 3-4 of the Final Rejection. Applicant respectfully maintains that this is incorrect. Although some bias must be applied to the gates of the two above described circuits of Kinzer, the specific arrangement where an input voltage signal source, and not a constant voltage source, is connected to the gates of the enhancement mode transistor and vice versa for the gates of the depletion mode transistor are not the only arrangements that would allow Kinzer's two embodiments to each function. Further, Applicant respectfully points out that applying a constant voltage source to one of the gates of enhancement mode transistor 50 would permanently block conduction through the transistor unless that constant voltage were a positive value sufficient enough to create a channel under that

gate. Thus, Applicant respectfully asserts that the specific arrangement disclosed in the present application is not required for Kinzer's structures to function.

Additionally, the Examiner has asserted that the requirement that the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor is a functional distinction. *See* pages 4-5 of the Final Rejection. Applicant respectfully disagrees and maintains that whether a device includes an enhancement mode transistor or a depletion mode transistor is a structural distinction. Inherently, an enhancement mode portion and a depletion mode portion must be structurally different from either two enhancement mode portions or two depletion mode portions, as specifically disclosed in Kinzer. For example, in the present application, first portion Q1 can be an enhancement mode transistor by using a recessed gate, fluorine implants, or other suitable means. *See* paragraph [0023] and Figure 3 of the present application. Thus, whether a device includes an enhancement mode transistor or a depletion mode transistor is a tangible distinction and not a functional distinction.

The Examiner has further asserted that it is reasonable to assume that Kinzer's devices 32, 34 are capable of performing in enhancement mode or depletion mode respectively because a comparison of Applicant's specification to Kinzer's disclosures reveals that Kinzer discloses a device that is apparently identical to the present invention. *See* pages 5-6 of the present application. However, as disclosed in Kinzer, device 40 is a depletion mode device (i.e. normally ON), having a logic NOR gate principle of operation, wherein an appropriate voltage applied to *either or both* gate electrode 32 or

gate electrode 34 causes an interruption in the 2DEG, thereby turning device 40 off. *See id.* at paragraphs [0033] and [0036], and Figure 3. Kinzer further discloses that device 40 displays symmetrical operation whereas the present invention, according to one embodiment, discloses that the drain voltage swing of the enhancement mode portion is substantially reduced and optimized for ultra-low voltage operation and the depletion mode portion may be optimized for stable higher voltage operation due to the specific arrangement of the depletion mode and enhancement mode portions of an embodiment of the present invention. *See* paragraphs [0020] and [0021] of the present application.

Further, Kinzer teaches that device 50 is an enhancement mode device (i.e. a normally off device) specifically due to the structural feature of two recesses 38 and is defined as performing an AND gate logic function such that current flows between electrodes 25, 26 when *both* gate electrodes 32, 34 have a potential applied to them. *See* paragraph [0029] of the present application. Similar to device 40, device 50 [illegible]



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## FACSIMILE TRANSMISSION COVER SHEET

Date: September 12, 2011

To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826

Fax: (571) 273-8300

Re: **Application Serial No.: 11/688,338**
Filing Date: 3/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 23

Message:

Enclosed please find:

1) Request for Continued Examination
2) Amendment and Response to Advisory Action

Payment for Request for Continued Examination fee and Second Month Extension in the amount of $1,300.00 is hereby enclosed on form PTO-2038.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

PTO/SB/06 (07-06)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

# PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

| Application or Docket Number | Filing Date | ☐ To be Mailed |
|---|---|---|
| 11/688,338 | 03/20/2007 | |

## APPLICATION AS FILED – PART I

| FOR | (Column 1) NUMBER FILED | (Column 2) NUMBER EXTRA | SMALL ENTITY ☐ RATE ($) | SMALL ENTITY ☐ FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | OTHER THAN SMALL ENTITY FEE ($) |
|---|---|---|---|---|---|---|---|
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| AMENDMENT 09/12/2011 | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE ($) | SMALL ENTITY ADDITIONAL FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | OTHER THAN SMALL ENTITY ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|
| Total (37 CFR 1.16(i)) | * 16 | Minus | ** 20 | = 0 | X $ = | | OR | X $52= | 0 |
| Independent (37 CFR 1.16(h)) | * 2 | Minus | ***3 | = 0 | X $ = | | OR | X $220= | 0 |
| ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | 0 |

| AMENDMENT | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|
| Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DEBORAH SCOTT/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | Thomas Herman | 0400131 | 9886 |

25700 7590 08/18/2011

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

| EXAMINER | |
|---|---|
| AHMED, SELIM U | |
| ART UNIT | PAPER NUMBER |
| 2826 | |
| MAIL DATE | DELIVERY MODE |
| 08/18/2011 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| **Advisory Action Before the Filing of an Appeal Brief** | **Application No.** 11/688,338 | **Applicant(s)** HERMAN, THOMAS | |
|---|---|---|---|
| | **Examiner** SELIM AHMED | **Art Unit** 2826 | |

***--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

THE REPLY FILED 12 July 2011 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *Amendment filed on 7/12/2011, applicant added the new limitation, "includes a field plate" to claims 1 and 10. The added limitations in claims 1 and 10 change the scope of the claims that would require further consideration and/or search*. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-16*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Evan Pert/
Primary Examiner, Art Unit 2826

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JUL 12 2011

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08/03/2011

Attorney Docket No.: 0400131

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| In re Application of: **Herman, Thomas** | Art Unit: 2826 |
| Serial No.: 11/688,338 | Examiner: Ahmed, Selim U. |
| Filed: 03/20/2007 | |
| For: **Merged Gate Cascode Transistor** | |

## AMENDMENT AND RESPONSE TO NON-FINAL OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the Non-Final Office Action dated April 12, 2011 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

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JUL 12 2011

Attorney Docket No.: 0400131

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | |
|---|---|
| In re Application of: **Herman, Thomas** | Art Unit: 2826 |
| Serial No.: 11/688,338 | Examiner: Ahmed, Selim U. |
| Filed: 03/20/2007 | |
| For: **Merged Gate Cascode Transistor** | |

## AMENDMENT AND RESPONSE TO NON-FINAL OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the Non-Final Office Action dated April 12, 2011 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.



PAGE 2/21 * RCVD AT 7/12/2011 9:16:04 PM [Eastern Daylight Time] * SVR:W-PTOFAX-003/9 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):03-56

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**In the Claims:**

**Claim 1 (currently amended):** A merged cascode transistor circuit comprising:

an input voltage signal source;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a semiconductor element;

a source electrode electrically connected to a top surface of the semiconductor element;

a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;

a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;





PAGE 3/21 * RCVD AT 7/12/2011 9:16:04 PM [Eastern Daylight Time] * SVR:W-PTOFAX-003/9 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):03-56

wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

**Claim 2 (previously presented):** The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:

a first III-Nitride layer; and

a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

**Claim 3 (previously presented):** The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates

and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 4 (previously presented):** The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

**Claim 5 (previously presented):** The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 6 (previously presented):** The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claim 7 (previously presented):** The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.



PAGE 5/21 * RCVD AT 7/12/2011 9:16:04 PM [Eastern Daylight Time] * SVR:W-PTOFAX-003/9 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):03-56

**Claim 8 (previously presented):** The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

**Claim 9 (previously presented):** The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

**Claim 10 (currently amended):** A merged cascode high electron mobility transistor circuit comprises:

an input voltage signal source;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a first epitaxial layer of III-Nitride material;

a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

a source electrode electrically connected to the first epitaxial layer;

a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;

a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and

a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;

wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

**Claim 11 (original):** The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

**Claim 12 (previously presented):** The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGaN material and the second epitaxial layer comprises a GaN material.

**Claim 13 (original):** The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claims 14 (previously presented):** The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

**Claim 15 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

**Claim 16 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.





PAGE 8/21 * RCVD AT 7/12/2011 9:16:04 PM [Eastern Daylight Time] * SVR:W-PTOFAX-003/9 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):03-56

## REMARKS

Prior to the present response, claims 1-16 were pending in the present application. By the present amendments, Applicant has amended claims 1 and 10. Thus, claims 1-16 remain in the present application. Reconsideration and allowance of pending claims 1-16 in view of the following remarks are requested.

### A. Rejection of Claims 1-16 under 35 U.S.C. § 103(a)

In the Non-Final Office Action dated April 12, 2011 (hereinafter "Office Action") the Examiner has rejected claims 1-16 under 35 U.S.C. § 103(a) for purported obviousness over U.S. Patent Application Publication Number 2005/0189561 by Kinzer et al. (hereinafter "Kinzer") in view of U.S. Patent Application Publication Number 2004/0188761 by Koyama et al. (hereinafter "Koyama"). *See* pages 2-14, item 2 of the Office Action. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by currently amended independent claims 1 and 10, is patentably distinguishable over Kinzer and Koyama.

The present invention, as defined by currently amended independent claims 1 and 10, provides a circuit including an input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor, and a second gate, including a field plate, positioned adjacent to the first gate, and between the source





PAGE 9/21 * RCVD AT 7/12/2011 9:16:04 PM [Eastern Daylight Time] * SVR:W-PTOFAX-003/9 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):03-56

electrode and the drain electrode to form a second portion of the transistor, where the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate includes a field plate and is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. *See* currently amended independent claims 1 and 10 above. Claim 10 further defines that the transistor is a high electron mobility transistor (HEMT) wherein first and second epitaxial layers of III-nitride material in contact with each other such that a 2-dimensional electron gas conducting layer is formed between the layers are in place of the semiconductor element. *See* currently amended independent claim 10 above. Claims 1 and 10 have been amended such that the second gate electrode includes a field plate. Support for these amendments can be found in at least paragraph [0021] and figures 3 and 4 of the present application.

In an embodiment of the invention shown in Figure 3 of the present application, HEMT 30 includes first portion Q1 including gate 32, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source contact 31 and drain contact 34. *See* paragraph [0023] and Figure 3 of the present application. HEMT 30 also includes second portion Q2 including gate 33, which is situated over semiconductor element 29 and insulating layer 38 and also situated between

source contact 31 and drain contact 34. In HEMT 30, node 24 is between first portion Q1 and second portion Q2. *See id.* at Figure 3, Figure 2 and related text, and paragraph [0023].

As disclosed in the present application, in an embodiment of the present invention, first portion Q1 is an enhancement mode transistor (normally OFF) and second portion Q2 is a depletion mode transistor (normally ON). *See* paragraph [0023] and Figure 3 of the present application. Further disclosed in the present application, an input voltage signal is connected to gate 32 provide a gate voltage Vg1. *See id.* at paragraph [0016]. Furthermore, a voltage is connected to gate 33 to provide a set voltage to Vg2, for example 0v. *See id.* at Figure 3 and paragraphs [0025] and [0017]. When the input voltage at Vg1 goes low, the first portion Q1 turns OFF. As a result, the voltage at the node 24 rises until the gate-source voltage of second portion Q2 reaches a set pinch off voltage and the second portion Q2 turns OFF. *See id.* at paragraph [0018]. Thus, an embodiment of the present invention advantageously provides for a circuit where the drain swing of the first portion Q1 is substantially reduced. *Id.*

In contrast to the present invention as defined by currently amended independent claims 1 and 10, Kinzer fails to disclose a circuit including an input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor where the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the

transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Kinzer specifically discloses device 40 in Figure 3 and device 50 in Figure 4.

The Examiner asserts that an input voltage signal source connected to the gates of Kinzer's enhancement mode transistor and a constant voltage source having a predetermined constant voltage connected to the gates of Kinzer's depletion mode transistor are specifically required for devices 40 and 50 to operate or function. *See* pages 3-4 of the Office Action. Applicant respectfully maintains that this is incorrect. Although some bias must be applied to the gates of the two above described circuits of Kinzer, the specific arrangement where an input voltage signal source, and not a constant voltage source, is connected to the gates of the enhancement mode transistor and vice versa for the gates of the depletion mode transistor are not the only arrangements that would allow Kinzer's two embodiments to each function. Further, Applicant respectfully points out that applying a constant voltage source to one of the gates of enhancement mode transistor 50 would permanently block conduction through the transistor unless that constant voltage were a positive value sufficient enough to create a channel under that gate. Thus, Applicant respectfully asserts that the specific arrangement disclosed in the present application is not required for Kinzer's structures to function.

Additionally, the Examiner asserts the requirement that the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor is a functional distinction. *See* pages 4-5 of the Office Action. Applicant respectfully disagrees and maintains that whether a device includes an enhancement mode transistor or a depletion mode transistor is a structural distinction. Inherently, an enhancement mode portion and a depletion mode portion must be structurally different from either two enhancement mode portions or two depletion mode portions, as specifically disclosed in Kinzer. For example, in the present application, first portion Q1 can be an enhancement mode transistor by using a recessed gate, fluorine implants, or other suitable means. *See* paragraph [0023] and Figure 3 of the present application. Thus, whether a device includes an enhancement mode transistor or a depletion mode transistor is a tangible distinction and not a functional distinction.

The Examiner further asserts that it is reasonable to assume that Kinzer's devices 32, 34 are capable of performing in enhancement mode or depletion mode respectively because a comparison of Applicant's specification to Kinzer's disclosures reveals that Kinzer discloses a device that is apparently identical to the present invention. *See* pages 5-6 of the present application. However, as disclosed in Kinzer, device 40 is a depletion mode device (i.e. normally ON), having a logic NOR gate principle of operation, wherein an appropriate voltage applied to *either or both* gate electrode 32 or gate electrode 34 causes an interruption in the 2DEG, thereby turning device 40 off. *See id.* at paragraphs [0033] and [0036], and Figure 3. Kinzer further discloses that device 40 displays

symmetrical operation whereas the present invention, according to one embodiment, discloses that the drain voltage swing of the enhancement mode portion is substantially reduced and optimized for ultra-low voltage operation and the depletion mode portion may be optimized for stable higher voltage operation due to the specific arrangement of the depletion mode and enhancement mode portions of an embodiment of the present invention. *See* paragraphs [0020] and [0021] of the present application.

Further, Kinzer teaches that device 50 is an enhancement mode device (i.e. a normally off device) specifically due to the structural feature of two recesses 38 and is defined as performing an AND gate logic function such that current flows between electrodes 25, 26 when *both* gate electrodes 32, 34 have a potential applied to them. *See* paragraph [0039] of the present application. Similar to device 40, device 50 also displays symmetrical operation, contrary to the present invention. *See id.* at paragraph [0041]. It is important to note that nowhere does Kinzer disclose a device having both an enhancement mode portion and a depletion mode portion. Thus, Applicant respectfully asserts that Kinzer fails to disclose the present invention, according to either currently amended independent claim 1 or 10 of the present application.

Moreover, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *See In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959) and MPEP §2143.01(VI). Applicant respectfully asserts that the combination of device 40 and device 50 of Kinzer

to create a merged cascode transistor, wherein a first portion of the merged cascode transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor would change the principles of operation of both devices 40 and 50 such that the combination would could not function as a NOR gate or an AND gate, respectively, and further, that the combined device would lose its operational symmetry. Thus, because the proposed modification would change the principle of operation of both devices 40 and 50, their combination is insufficient to render the claims prima facie obvious. Further, Applicant respectfully asserts, for the same reasons, that devices 40 and 50 of Kinzer do not necessarily or inherently possess the characteristics of the present invention.

Finally, the Examiner asserts that, in stating that first and second gate electrodes 32, 34 are independently operable, Kinzer discloses that one gate may be of an enhancement mode while the other may be of a depletion mode. *See* page 20, item 4 of the Office Action. Applicant respectfully disagrees. In context, the specification of Kinzer simply teaches that each gate may be individually activated. Nowhere does Kinzer disclose or even suggest that a device containing both an enhancement mode portion and a depletion mode portion, rather only two separate devices 40 and 50, one having two enhancement mode portions, and the other having two depletion mode portions. Additionally, Applicant respectfully asserts that Kinzer fails to disclose a second gate electrode including a field plate.



PAGE 15/21 * RCVD AT 7/12/2011 9:16:04 PM [Eastern Daylight Time] * SVR:W-PTOFAX-003/9 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):03-56

Turning to Koyama, Koyama is directed toward a source follower circuit, which can be operated without increasing a power supply voltage higher than a desired value, thus maintaining a low power supply voltage and low power consumption. *See* paragraph [0031] of Koyama. The Examiner states that Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 device, respectively. *See* page 4 of the Office Action. However, Koyama also fails to disclose or suggest a merged gate cascode transistor wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Applicant respectfully asserts that Koyama also fails to disclose or suggest a second gate including a field plate.

Thus, each of Kinzer and Koyama fail to disclose or suggest a merged gate cascode transistor wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor as well as a second gate including a field plate. Consequently, even if the Office Action provided a reasonable incentive for one skilled in the art to combine the cited art references Kinzer and Koyama, Applicant respectfully submits that the resulting combination would still fail to disclose or suggest the present invention as defined by currently amended independent claims 1 and 10.

For the foregoing reasons, Applicant respectfully submits that at the time the present invention as defined by currently amended independent claims 1 and 10 was made, the invention would not have been rendered obvious to one of ordinary skill in the





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art by the disclosures of Kinzer and Koyama, singly or in combination. Consequently, Applicant respectfully asserts that the invention described by currently amended independent claims 1 and 10 is patentably novel and inventive over Kinzer and Koyama. As such, claims 2-9 depending from and further limiting patentable independent claim 1, and claims 11-16, depending from and further limiting patentable independent claim 10 are also patentably novel and inventive over Kinzer and Koyama for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim. Accordingly, Applicant respectfully requests allowance of claims 1-16.

**B. Rejection of Claims 10-16 under 35 U.S.C. §103(a)**

The Examiner has rejected claims 10-16 under 35 U.S.C. § 103(a) for purported obviousness over Kinzer in view of Koyama and in further view of U.S. Patent Number 7,052,942 to Smart et al. (hereinafter "Smart"). *See* pages 14-19, item 3 of the Office Action. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by currently amended independent claim 10, is patentably distinguishable over Kinzer, Koyama and Smart.

The present invention, as defined by amended independent claim 10, provides a circuit including input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor including a first epitaxial layer of III-Nitride material, a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is

formed between the first and second epitaxial layers, a source electrode electrically connected to the first epitaxial layer, a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode, a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor, and a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor, where the first gate is connected the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. *See* currently amended independent claim 10 above.

For reasons similar to those presented above, Applicant respectfully asserts that neither Kinzer nor Koyama, or any combination of Kinzer and Koyama, discloses or suggests a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate including a field plate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a

depletion mode transistor, as specifically required by currently amended independent claim 10.

In the Office Action, the Examiner suggests combining Kinzer and Koyama with Smart to overcome the omission from the combination of Kinzer and Koyama of any express teaching that the described III-Nitride (AlGaN and GaN) layers are epitaxial. *See* pages 16-17 of the Office Action. Smart specifically discloses HEMT 28 including GaN buffer layer 22 and AlGaN Schottky layer 24. *See* Figure 2 and related text of Smart. However, in Smart, HEMT 28 includes only a single gate contact 32. *Id.*

Thus, Smart, like Kinzer and Koyama, fails to disclose or suggest a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate, including a field plate, positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, as specified in currently amended independent claim 10. Consequently, Smart fails to cure the aforementioned deficiencies of Kinzer and Koyama. As such, Applicant submits that the combination of Kinzer, Koyama and Smart suggested by the Examiner does not and cannot result in the present invention, as defined by currently amended independent claim 10.

For the foregoing reasons, Applicant respectfully submits that at the time the present invention as defined by currently amended independent claim 10 was made, the

invention would not have been rendered obvious to one of ordinary skill in the art by the disclosures of Kinzer, Koyama and Smart, singly or in combination. Consequently, Applicant respectfully asserts that the invention described by currently amended independent claim 10 is patentably novel and inventive over Kinzer, Koyama and Smart. As such, claims 11-16, depending from and further limiting patentable independent claim 10 are also patentably novel and inventive over Kinzer, Koyama and Smart for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim. Accordingly, Applicant respectfully requests allowance of claims 10-16.

C. **Conclusion**

For all the foregoing reasons, Applicant respectfully submit that the present invention, as defined by currently amended independent claims 1 and 10, and claims depending therefrom, is patentably novel and inventive. Moreover, Applicant asserts that no new matter has been introduced herein. Accordingly, an early allowance of pending claims 1-16 is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.



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Attorney Docket No.: 0400131

Respectfully Submitted,
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Date: 7/12/11

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## FACSIMILE TRANSMISSION COVER SHEET

Date: July 12, 2011

To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826

Fax: (571) 273-8300

Re: **Application Serial No.: 11/688,338**
Filing Date: 3/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 21

Message:

Enclosed please find the Amendment and Response to Non-Final Office Action dated April 12, 2011.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account **50-0731**.

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# PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

| Application or Docket Number | Filing Date | ☐ To be Mailed |
|---|---|---|
| 11/688,338 | 03/20/2007 | |

## APPLICATION AS FILED – PART I

| FOR | (Column 1) NUMBER FILED | (Column 2) NUMBER EXTRA | SMALL ENTITY ☐ RATE ($) | SMALL ENTITY FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | OTHER THAN SMALL ENTITY FEE ($) |
|---|---|---|---|---|---|---|---|
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| AMENDMENT | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE ($) | SMALL ENTITY ADDITIONAL FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | OTHER THAN SMALL ENTITY ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|---|
| | 07/12/2011 | | | | | | | | | |
| | Total (37 CFR 1.16(i)) | * 16 | Minus | ** 20 | = 0 | X $ = | | OR | X $52= | 0 |
| | Independent (37 CFR 1.16(h)) | * 2 | Minus | ***3 | = 0 | X $ = | | OR | X $220= | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | 0 |

| AMENDMENT | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/CAROL BARNES/

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|---|---|---|
| | APPLICANTS:<br>Herman, Thomas | |
| | FILING DATE:<br>March 20, 2007 | GROUP ART:<br>2826 |

| U.S. PATENT DOCUMENTS | | | | | | | |
|---|---|---|---|---|---|---|---|
| Exam. Initials | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
| | AA | | | | | | |
| | AB | | | | | | |

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| Exam. Initials | | DOCUMENT NUMBER | PUBLICATION DATE | COUNTRY OR PATENT OFFICE | CLASS | SUB CLASS | TRANSLATION YES | TRANSLATION NO |
| | BA | | | | | | | |
| | BB | | | | | | | |

| OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.) | | |
|---|---|---|
| | CA | Tietze, et al., Halbleiter-Schaltungstechnik, 12. Auflage, Berlin: Springer, 2002, Pages 316-317 |

| EXAMINER: | DATE CONSIDERED: |
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Date: April 13, 2011

To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826

Fax: (571) 273-8300

Re: **Application Serial No.: 11/688,338**
Filing Date: 3/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 11

Message:

Enclosed please find Information Disclosure Statement, Form PTO-1449 and Cited Reference.

Payment for Filing of Information Disclosure in the Amount of $180.00 is hereby enclosed on Form PTO-2038.

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| In re Application of: | Art Unit: 2826 |
| **Herman, Thomas** | Examiner: Ahmed, Selim U. |
| Serial No.: **11/688,338** | |
| Filed: **March 20, 2007** | |
| For: **Merged Gate Cascode Transistor** | |

## INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

In this Information Disclosure Statement and pursuant to 37 C.F.R. §§ 1.56 and 1.97, Applicants hereby disclose to the Patent Office patents, publications or other information of which Applicants are aware. A list of references is included in Form 1449 submitted herewith.

The items identified in this Information Disclosure Statement may or may not be "material" as defined in 37 C.F.R. § 1.56, and the submission thereof by Applicants is not to be construed as an admission that any such patent, publication or other information referred to is material or considered to be material (37 C.F.R. § 1.97(h)), or even qualifies as "prior art" under 35 U.S.C. § 102 with respect to the present invention unless specifically designated by Applicants as such. Identification of any reference or patent herein is not an admission, nor is it to be construed as an admission, that it was invented prior to the invention disclosed herein.

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This Information Disclosure Statement is filed in accordance with 37 C.F.R. §§ 1.97(d) and 1.97(e)(1). This information disclosure statement is being filed on or before payment of the issue fee and each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. In accordance with 37 C.F.R. § 1.97(d)(2), the required fee of $180.00 for filing this Information Disclosure Statement is also enclosed (Form PTO-2038 for Payment by Credit Card). The Assistant Commissioner is hereby authorized to charge or credit Deposit Account Number 50-0731 for any deficiency or overpayment in the fees required for the filing of this Information Disclosure Statement.

Respectfully submitted,

Farjami & Farjami LLP

Dated: 4/13/11

By: _____
Michael Farjami
Reg. No. 38, 135
Attorneys for Applicants

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | Thomas Herman | 0400131 | 9886 |

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| EXAMINER | |
|---|---|
| AHMED, SELIM U | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 04/12/2011 | PAPER |

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The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 11/688,338 | HERMAN, THOMAS | |
| | Examiner | Art Unit | |
| | SELIM AHMED | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 February 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's remark filed on 02/03/2011 is acknowledged. The claims 1-16 remain original as no amendment was made with the remark. Applicant's arguments have been fully considered but they are not persuasive. So, the rejection made on 10/06/2010 is repeated here and arguments made by applicant are rebutted under this office action.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer ET al (2005/0189561; Kinzer hereinafter) in view of Koyama (US 2004/0188761; Koyama hereinafter).

With regard to claim 1, Fig. 4 of Kinzer discloses a merged gate transistor circuit comprising: a merged cascode transistor (Fig.4) comprising: a semiconductor element (element comprising of 21, 22, 23, and 24 i.e. substrate); a source electrode 25 electrically connected to a top surface (top surface of 21 in Fig. 4) of the semiconductor element; a drain electrode 26 electrically connected to the top surface of the semiconductor element and spaced laterally away from

the source electrode 25; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and capacitively coupled to the semiconductor element (para[0035]) to form a first portion of the transistor (e.g. Fig. 4, portion of transistor 32); and a second gate 34 positioned adjacent to the first gate 32, and between the source electrode 25 and the drain electrode 26 to form a second portion of the transistor (e.g. Fig. 4, portion of transistor 34), wherein the second gate 34 is also capacitively coupled to the semiconductor element (para[0035]); wherein in the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, Kinzer discloses the claim 1 limitations but does not explicitly disclose an input voltage signal source, a constant voltage source having a predetermined constant voltage; wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between to the constant voltage source and a voltage at the source electrode reaches a predetermined level. However, applicant's above limitations directed to functional or method of operating limitations as to depletion mode and enhancement mode transistor. The above limitations, particularly, an input voltage signal source and a constant voltage source having a

predetermined constant voltage are bias voltages to the enhancement and depletion mode transistors that are required to operate/function of the device. Although Kinzer does not explicitly disclose an input voltage signal source and a constant voltage source having a predetermined constant voltage, Kinzer depletion mode and enhancement mode devices inherently require these bias conditions to operate/function. However, for example, Figs. 1, 2, 5 and para[0008, 0049] of Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 devices. Since it is common knowledge to apply bias voltages to the gates of the depletion and enhancement mode devices for device operation, it would have been obvious to one having ordinary skill in the art at the time of the invention to include an input voltage signal source and a constant voltage source having a predetermined constant voltage within Kinzer device to operate/function of the device.

The applicant's claims **1, 6, 7** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of using the first portion of the transistor for conducting while using the input voltage signal for providing an input voltage above a predetermined threshold voltage that is a pinch off voltage of the second portion of the transistor and running the first portion of the transistor and the second portion of the transistor in enhancement

and depletion mode, respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer**'s devices 32, 34 are capable of performing in enhancement mode or depletion mode respectively (refer to claims 9 &10 and para[0026, 0033, 0038]), because a comparison of Applicant's specification to **Kinzer**'s disclosure reveals that **Kinzer** discloses a

device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode as indicated in the claims 9, 10, and para[0026, 0033, 0038]). Because it is reasonable to assume that **Kinzer**'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

Furthermore, Kinzer discloses all of the limitation of claim 1 with the exception of "a merged cascode transistor circuit" as recited in the preamble. As disclosed in the MPEP 2111.02, preamble statement reciting purpose or intended use not given significant patentable weight if there is no structural difference between the claimed invention and prior art. Kinzer discloses a bi-directional switch that is structurally identical claimed by applicant. The exception is that the merged cascode transistor. However, this feature is a purpose/intended use of the Applicant's device and does not structurally limit feature of the claim. The structure of the claim device is the same as that of the prior art. Therefore, the claimed invention does not distinguish over the Kinzer's device. Note that a recitation of the purpose/intended use such as "merged gate cascode transistor" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the purpose/intended use, it meets the claim.

With regard to claim 2, Fig. 4 of Kinzer et al discloses the merged gate transistor circuit of claim 1, wherein the semiconductor element further comprises: a first III-Nitride layer 21; and a second III-Nitride layer 23 on which the first III-Nitride layer is positioned such that a 2DEG conduction layer 22 forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer (e.g. para [00320]).

With regard to claim 3, figure 4 of Kinzer et al discloses the merged gate transistor circuit of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 4, Fig. 4 and elements 21, 23 of Kinzer et al disclose the merged gate transistor circuit of claim 3, wherein the first III-Nitride layer comprises AlGaN material, and the second III-Nitride layer comprises GaN material.

With regard to claim 5, figure 4 and claim 3 of Kinzer et al disclose the merged gate transistor circuit of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such

that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 8, para [0025] of Kinzer et al disclose the merged gate transistor circuit of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 9, para [0025] of Kinzer et al disclose the merged gate transistor circuit of claim 8, wherein the insulation layer is comprised of silicon nitride.

With regard to claim 10, Fig.4 of Kinzer et al discloses a merged cascade high electron mobility transistor circuit comprises: a first epitaxial layer 21 of III-Nitride material; a second epitaxial layer 23 of a III-Nitride material, in contact with the first epitaxial layer 21 such that a 2-dimensional electron gas conducting layer 22 is formed between the first 21 and second 23 epitaxial layers; a source electrode 25 electrically connected to the first epitaxial layer 21; a drain electrode 26 electrically connected to the first epitaxial layer 21 and spaced laterally from the source electrode; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and coupled to the first epitaxial layer to form a first portion (e.g. Fig. 4, portion of transistor 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode 26 and

source electrode 25 and coupled to the first epitaxial layer 21 to form a second portion (e.g. Fig. 4, portion of transistor 34) of the transistor; and wherein the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, Kinzer discloses the claim limitations but does not explicitly disclose an input voltage signal source, a constant voltage source having a predetermined constant voltage; wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between to the constant voltage source and a voltage at the source electrode reaches a predetermined level. However, applicant's above limitations directed to functional limitations as to depletion mode and enhancement mode transistor. The above limitations, particularly, an input voltage signal source and a constant voltage source having a predetermined constant voltage are bias voltages to the enhancement and depletion mode transistors that are required to operate/function of the device. Although Kinzer does not explicitly disclose an input voltage signal source and a constant voltage source having a predetermined constant voltage, Kinzer device inherently requires these bias condition to operate/function. However, for example, Figs. 1,

2, 5 and para[0008, 0049] of Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 devices. Since it is common knowledge to apply bias voltages to the gates of the depletion and enhancement mode devices for device operation, it would have been obvious to one having ordinary skill in the art at the time of the invention to include an input voltage signal source and a constant voltage source having a predetermined constant voltage within Kinzer device to operate/function of the device.

As discussed above, Kinzer discloses all of the structural limitations of claims 10-16 with the exception of not explicitly disclosing that the III-Nitride (AlGaN and GaN) layers are formed by an epitaxial process. Applicant's claims, however, do not distinguish over the Kinzer reference by virtue of the process used to form the III-Nitride layers, since only the final product is relevant, not the process of forming the III-Nitride material epitaxially. Note that a "product by process claim" is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or

obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Furthermore, Kinzer discloses all of the limitation of claim 10 with the exception of “merged cascode high electron mobility transistor circuit” as recited in the preamble. As disclosed in the MPEP 2111.02, preamble statement reciting purpose or intended use not given significant patentable weight if there is no structural difference between the claimed invention and prior art. Kinzer discloses a bi-directional switch that is structurally identical claimed by applicant. The exception is that the merged cascode high electron mobility transistor. However, this feature is a purpose/intended use of the Applicant's device and does not structurally limit feature of the claim. The structure of the claim device is the same as that of the prior art. Therefore, the claimed invention does not distinguish over the Kinzer’s device. Note that a recitation of the purpose/intended use such as “merged cascode high electron mobility transistor” of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the purpose/intended use, it meets the claim.

Furthermore, applicant's claims 10, 13, 14 do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed

and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer**'s devices 32, 34 are capable of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively, because a comparison of Applicant's specification to **Kinzer**'s disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively. Because it is reasonable to

assume that **Kinzer**'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 11, figure 4 and claim 3 of Kinzer et al disclose the merged cascode high electron mobility transistor circuit of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

With regard to claim 15, para [0025] of Kinzer et al disclose the merged gate transistor circuit of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 16, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

3. Claims 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer in view of Koyama and further in view of Smart et al (US 7,052,942; Smart hereinafter).

With regard to claims 10, 12, 13, 14, e.g. Fig.4 of Kinzer in view of Komaya discloses a merged cascode high electron mobility transistor circuit comprises: a first layer 21 of III-Nitride material; a second layer 23 of a III-Nitride material, in

contact with the first layer 21 such that a 2-dimensional electron gas conducting layer 22 is formed between the first 21 and second 23 layers; a source electrode 25 electrically connected to the first layer 21; a drain electrode 26 electrically connected to the first layer 21 and spaced laterally from the source electrode; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and coupled to the first layer to form a first portion (e.g. Fig. 4, portion of transistor 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode 26 and source electrode 25 and coupled to the first layer 21 to form a second portion (e.g. Fig. 4, portion of transistor 34) of the transistor; and wherein the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, Kinzer discloses the claim limitations but does not explicitly disclose an input voltage signal source, a constant voltage source having a predetermined constant voltage; wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between to the constant voltage source and a voltage at the source electrode reaches a predetermined level. However, applicant's above limitations directed to functional limitations as to depletion mode and

enhancement mode transistor. The above limitations, particularly, an input voltage signal source and a constant voltage source having a predetermined constant voltage are bias voltages to the enhancement and depletion mode transistors that are required to operate/function of the device. Although Kinzer does not explicitly disclose an input voltage signal source and a constant voltage source having a predetermined constant voltage, Kinzer device requires these bias condition to operate/function. However, for example, Figs. 1, 2, 5 and para[0008, 0049] of Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 devices. Since it is common knowledge to apply bias voltages to the gates of the depletion and enhancement mode devices for device operation, it would have been obvious to one having ordinary skill in the art at the time of the invention to include an input voltage signal source and a constant voltage source having a predetermined constant voltage within Kinzer device to operate/function of the device.

As discussed above, the difference between the device disclosed by Kinzer et al and that claimed lies in the recital of “epitaxial” layer, i.e. layers formed by epitaxy. Smart discloses forming an AlGaN layer by epitaxy over a GaN layer, also formed by epitaxy. Smart’s epitaxially formed AlGaN and GaN layers create a 2DEG layer between them that creates the thin, high mobility channel needed for proper performance of the device disclosed by Kinzer. It therefore seems

clear that one of ordinary skill in the art could have applied Smart's known "improvement" technique to Kinzer's "base" device in the same way Smart applies it to a "comparable" device and that in the view of one of skill in the art, the results would have predictably produced the 2DEG layer required by Kinzer's device. See MPEP § 2143, part "C".

With regard to claims 10 and 12, as discussed above, Kinzer et al disclose all of the structural limitations with the exception of not disclosing the III-Nitride (AlGaN and GaN) layers being epitaxial explicitly. However, e.g. Fig.2, elements 24, 22 of Smart discloses the AlGaN and GaN layers. It would have been obvious to one having ordinary skill in the art at the time of the invention to substitute Smart's epitaxial III-Nitride (AlGaN and GaN) layers with Kinzer's III—Nitride (AlGaN and GaN) layers for predictable results such as, low leakage characteristics of the HEMT device.

Furthermore, applicant's claims **10, 13, 14** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined

constant voltage and a voltage at the source electrode reaches a predetermined level. In another words, first portion or transistor 32 and second portion or transistor 34 are functioning as an enhancement and depletion mode respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer**'s devices 32, 34 are capable of performing as an enhancement mode and depletion mode respectively (refer to claims 9 &10 and para [0026, 0033, 0038]), because a comparison of Applicant's specification to **Kinzer**'s disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode. Because it is reasonable to assume that **Kinzer**'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 11, figure 4 of Kinzer et al discloses the merged cascode high electron mobility transistor circuit of claim 10, further comprising an insulating layer positioned between the first and second gates and the first layer.

With regard to claim 15, para [0025] of Kinzer et al disclose the merged gate transistor circuit of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 16, para [0025] of Kinzer et al disclose the merged gate transistor circuit of claim 8, wherein the insulation layer is comprised of silicon nitride.

***Response to Arguments***

4. Applicant's arguments with respect to claims 1-16 have been considered but they are not persuasive.

On page 3 of the remark filed on 02/03/2011 applicant mainly argued that Kinzer does not discloses where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

However, as indicated in the rejection, **Kinzer**'s devices 32, 34 are capable of performing as an enhancement mode and depletion mode respectively (refer to claims 9 &10 and para[0026, 0033, 0038]). Furthermore, in para[0034] of Kinzer discloses that "first gate electrode 32 and second gate electrode 34 are independently operable, meaning that each gate electrode receives a voltage pulse from a respective gate pad". Additionally, a comparison of Applicant's specification to **Kinzer**'s disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes. And applicant has failed to provide the specific structural difference between Kinzer device and claimed device. Applicant's argument rather directed to method of operating the device rather than the structural missing claimed parts within Kinzer. Since Kinzer explicitly discloses that the devices 32, 34 can

independently operate as enhancement mode or depletion mode, the examiner still believes that Kinzer's teaches the claimed limitation.

On page 15 of the remark filed on 02/03/2011 applicant argued that neither Kinzer nor Komaya discloses a constant voltage source. Firstly, para[0034] of Kinzer teaches that each gate electrode receives a voltage pulse from a respective gate pad. Secondly, para[0049] of Komaya discloses, "the depletion mode TFT has a characteristic that the threshold voltage is on its negative voltage side and a voltage (V.sub.GS) between the gate and source is approximately 0 V". Please note that applicant is also applying the same constant voltage i.e. 0V. Furthermore, applicant's claimed limitation "a constant voltage source having a predetermined constant voltage" is a functional/intended use limitation. Since Komaya discloses a gate voltage node 103, it is within the scope of an ordinary skill in the art to apply a constant voltage depending on the specific device parameters.

In response to applicant's argument (page 12) that device being not a merged cascade (or HEMT) transistor, as indicated in the rejection, a recitation of the purpose/intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

***Conclusion***

5. **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SELIM AHMED/

Examiner, Art Unit 2826

/Evan Pert/
Primary Examiner, Art Unit 2826

| Notice of References Cited | Application/Control No. 11/688,338 | Applicant(s)/Patent Under Reexamination HERMAN, THOMAS | |
|---|---|---|---|
| | Examiner SELIM AHMED | Art Unit 2826 | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| * | A | US-2004/0188761 A1 | 09-2004 | Koyama, Jun | 257/348 |
| * | B | US-2005/0189561 A1 | 09-2005 | Kinzer et al. | 257/192 |
| * | C | US-7,052,942 B1 | 05-2006 | Smart et al. | 438/162 |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
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**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
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| | V | |
| | W | |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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**CONFIRMATION NO. 9886**

| SERIAL NUMBER | FILING or 371(c) DATE / RULE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | 257 | 2826 | 0400131 |

**APPLICANTS**

Thomas Herman, Manhattan Beach, CA;

**** CONTINUING DATA ***************************

This appln claims benefit of 60/783,934 03/20/2006

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

03/29/2007

| Foreign Priority claimed | 35 USC 119(a-d) conditions met | Verified and Acknowledged | Met after Allowance | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|---|---|
| ☐ Yes ☑ No | ☐ Yes ☑ No | /SELIM U AHMED/ Examiner's Signature | ☐ Initials | CA | 4 | 16 | 2 |

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UNITED STATES

**TITLE**

MERGED GATE CASCODE TRANSISTOR

| FILING FEE RECEIVED | FEES: Authority has been given in Paper | |
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| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11688338 | HERMAN, THOMAS |
| | **Examiner** | **Art Unit** |
| | SELIM AHMED | 2826 |

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|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 05/22/2008 | 12/08/2008 | 03/20/2009 | 06/20/2009 | 09/25/2010 | 04/09/2011 | | | |
| | 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 3 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 5 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 6 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 7 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 8 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 9 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 10 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 11 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 12 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 13 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 14 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 15 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | 16 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11688338 | HERMAN, THOMAS |
| | Examiner | Art Unit |
| | SELIM AHMED | 2826 |

| SEARCHED | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| 257 | 192, 194, 195, E29.14, E29.144, E29.246, E29.249 | 5/22/08 | SA |
| | Updated search | 12/8/08 | /sa/ |
| | Updated search | 3/20/2009 | /sa/ |
| | Updated search | 6/20/2009 | /sa/ |
| | Updated search | 9/24/2010 | /sa/ |
| | Updated search | 4/9/2011 | /sa/ |

| SEARCH NOTES | | |
|---|---|---|
| Search Notes | Date | Examiner |
| Text search such as two dimensional electron gas, Cascode transistor, HEMT/High electron mobility transistor, source, drain, gate and their boolean combinations were searched. | 5/22/08 | SA |
| Updated search | 12/8/2008 | /sa/ |
| Updated search | 3/20/2009 | /sa/ |
| Updated search | 9/24/2010 | /sa/ |
| Updated search | 4/9/2011 | /sa/ |

| INTERFERENCE SEARCH | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| 257 | 192, 194, 195, | 5/22/08 | SA |

## EAST Search History

### EAST Search History (Prior Art)

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| S3 | 4541 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:21 |
| S4 | 7876 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S5 | 314831 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S6 | 73 | S3 and S4 and S5 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S7 | 96 | S3 and S4 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:23 |
| S8 | 63 | S6 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:23 |
| S9 | 82 | S7 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:24 |
| S10 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 17:33 |

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| S11 | 9 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 17:34 |
| S12 | 1404 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:53 |
| S13 | 1116 | S5 and S12 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:54 |
| S14 | 356 | S5 and S12 and S4 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:54 |
| S15 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:00 |
| S16 | 5 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:01 |
| S17 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:05 |

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| S18 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/21 18:20 |
| S19 | 16 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:25 |
| S20 | 1635 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:28 |
| S21 | 1200 | S5 and S20 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:29 |
| S22 | 773 | S5 and S20 and S4 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:29 |
| S23 | 706 | S22 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:30 |
| S24 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:45 |
| S25 | 275 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:46 |
| S26 | 232 | S25 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:46 |
| S27 | 232 | S25 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 18:46 |

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|---|---|---|---|---|---|---|
| S28 | 121 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/22 10:38 |
| S29 | 310043 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/22 15:10 |
| S30 | 556 | S29 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/22 15:11 |
| S31 | 852 | S29 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/05/22 15:11 |
| S32 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S33 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S34 | 4811 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S35 | 8419 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S36 | 332843 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |

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| S37 | 80 | S34 and S35 and S36 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S38 | 107 | S34 and S35 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S39 | 65 | S37 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S40 | 85 | S38 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S41 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S42 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842"). PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S43 | 1425 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S44 | 1137 | S36 and S43 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S45 | 365 | S36 and S43 and S35 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |

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| S46 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S47 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S48 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S49 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S50 | 18 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S51 | 1782 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S52 | 1310 | S36 and S51 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S53 | 847 | S36 and S51 and S35 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |

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| S54 | 725 | S53 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S55 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S56 | 312 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
| S57 | 244 | S56 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S58 | 244 | S56 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S59 | 125 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S60 | 321547 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S61 | 596 | S60 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S62 | 915 | S60 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S63 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |

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| S64 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S65 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S66 | 82 | S63 and S64 and S65 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S67 | 66 | S66 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S68 | 1 | S67 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S69 | 8 | S67 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:05 |
| S70 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:13 |
| S71 | 944 | S70 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:13 |
| S72 | 549 | S71 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:13 |

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| S73 | 213 | S72 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:14 |
| S74 | 15 | S73 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:15 |
| S75 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:27 |
| S76 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:27 |
| S77 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/19 18:31 |
| S78 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S79 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S80 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |

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| S81 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S82 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S83 | 82 | S80 and S81 and S82 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S84 | 109 | S80 and S81 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S85 | 66 | S83 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S86 | 86 | S84 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S87 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S88 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S89 | 1438 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |

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|---|---|---|---|---|---|---|
| S90 | 1150 | S82 and S89 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S91 | 373 | S82 and S89 and S81 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S92 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S93 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S94 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S95 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S96 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |

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|---|---|---|---|---|---|---|
| S97 | 1868 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S98 | 1378 | S82 and S97 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S99 | 896 | S82 and S97 and S81 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S100 | 737 | S99 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S101 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S102 | 334 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S103 | 246 | S102 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S104 | 246 | S102 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S105 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S106 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S107 | 622 | S106 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |

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|---|---|---|---|---|---|---|
| S108 | 944 | S106 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S109 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S110 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S111 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S112 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S113 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S114 | 82 | S111 and S112 and S113 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S115 | 109 | S111 and S112 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S116 | 66 | S114 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |

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|---|---|---|---|---|---|---|
| S117 | 86 | S115 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S118 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S119 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842"). PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S120 | 1438 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S121 | 1150 | S113 and S120 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S122 | 373 | S113 and S120 and S112 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S123 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900"). PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S124 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S125 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |

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|---|---|---|---|---|---|---|
| S126 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945"). PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S127 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732"). PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S128 | 1868 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S129 | 1378 | S113 and S128 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S130 | 896 | S113 and S128 and S112 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S131 | 737 | S130 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S132 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S133 | 334 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S134 | 246 | S133 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S135 | 246 | S133 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |

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|---|---|---|---|---|---|---|
| S136 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S137 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S138 | 622 | S137 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S139 | 944 | S137 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S140 | 4932 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S141 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S142 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S143 | 82 | S140 and S141 and S142 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S144 | 66 | S143 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |

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|---|---|---|---|---|---|---|
| S145 | 1 | S144 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S146 | 8 | S144 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S147 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S148 | 944 | S147 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S149 | 549 | S148 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/20 00:20 |
| S150 | 213 | S149 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S151 | 15 | S150 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S152 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |
| S153 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/20 00:20 |

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|---|---|---|---|---|---|---|
| S154 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/20 00:20 |
| S155 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S156 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S157 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S158 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S159 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S160 | 85 | S157 and S158 and S159 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S161 | 116 | S157 and S158 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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|---|---|---|---|---|---|---|
| S162 | 67 | S160 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S163 | 89 | S161 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S164 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S165 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S166 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S167 | 1162 | S159 and S166 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S168 | 378 | S159 and S166 and S158 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S169 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S170 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |

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|---|---|---|---|---|---|---|
| S171 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S172 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S173 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S174 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S175 | 1427 | S159 and S174 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S176 | 930 | S159 and S174 and S158 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S177 | 745 | S176 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S178 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S179 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |

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|---|---|---|---|---|---|---|
| S180 | 248 | S179 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S181 | 248 | S179 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S182 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S183 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S184 | 641 | S183 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S185 | 977 | S183 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S186 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S187 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S188 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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| S189 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S190 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S191 | 85 | S188 and S189 and S190 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S192 | 116 | S188 and S189 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S193 | 67 | S191 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S194 | 89 | S192 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S195 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S196 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S197 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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| S198 | 1162 | S190 and S197 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S199 | 378 | S190 and S197 and S189 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S200 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S201 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S202 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S203 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S204 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |

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|---|---|---|---|---|---|---|
| S205 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S206 | 1427 | S190 and S205 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S207 | 930 | S190 and S205 and S189 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S208 | 745 | S207 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S209 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S210 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S211 | 248 | S210 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S212 | 248 | S210 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S213 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S214 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S215 | 641 | S214 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |

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| S216 | 977 | S214 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S217 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S218 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S219 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S220 | 85 | S217 and S218 and S219 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S221 | 67 | S220 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S222 | 1 | S221 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S223 | 8 | S221 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S224 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |

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| S225 | 977 | S224 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S226 | 567 | S225 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S227 | 217 | S226 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S228 | 18 | S227 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S229 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S230 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S231 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S232 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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| S233 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S234 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S235 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S236 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S237 | 85 | S234 and S235 and S236 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S238 | 116 | S234 and S235 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S239 | 67 | S237 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S240 | 89 | S238 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S241 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |

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| S242 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S243 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S244 | 1162 | S236 and S243 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S245 | 378 | S236 and S243 and S235 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S246 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S247 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S248 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |

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|---|---|---|---|---|---|---|
| S249 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945"). PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S250 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732"). PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S251 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S252 | 1427 | S236 and S251 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S253 | 930 | S236 and S251 and S235 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S254 | 745 | S253 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S255 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S256 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S257 | 248 | S256 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S258 | 248 | S256 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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| S259 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S260 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S261 | 641 | S260 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S262 | 977 | S260 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S263 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S264 | 4 | ("20060043415" \| "20060043415" \| "6320205").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S265 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S266 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S267 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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| S268 | 85 | S265 and S266 and S267 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S269 | 116 | S265 and S266 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S270 | 67 | S268 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S271 | 89 | S269 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S272 | 5 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S273 | 10 | ("20030168704" \| "5264713" \| "5510632" \| "6281521" \| "6285046" \| "6373318" \| "6573128" \| "6822275" \| "6822842").PN. OR ("7026669").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S274 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S275 | 1162 | S267 and S274 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S276 | 378 | S267 and S274 and S266 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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|---|---|---|---|---|---|---|
| S277 | 14 | ("20020047177" \| "5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790" \| "7294900").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S278 | 6 | ("5504353" \| "5610410" \| "6072203" \| "6281528" \| "6534790").PN. OR ("7294900").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S279 | 14 | ("20010023964" \| "20020041003" \| "20020139995" \| "20020167023" \| "20060060871" \| "4424525" \| "4511813" \| "5387880" \| "5808332" \| "6177685" \| "6329677" \| "6465814" \| "6492669" \| "6690042").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S280 | 45 | ("20020017648" \| "20030160269" \| "20030218183" \| "20040021152" \| "20040036086" \| "20040192043" \| "20050110054" \| "20050170574" \| "20050189561" \| "20050189562" \| "20050285098" \| "4615102" \| "5349214" \| "5594262" \| "6248666" \| "6342411" \| "6423986" \| "6465814" \| "6521961" \| "6552373" \| "6646293" \| "6710379" \| "6830945").PN. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S281 | 19 | ("4764796" \| "5099295" \| "5192987" \| "5670798" \| "5677553" \| "5929467" \| "6064082" \| "6114732").PN. OR ("6465814").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S282 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S283 | 1427 | S267 and S282 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S284 | 930 | S267 and S282 and S266 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |

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| S285 | 745 | S284 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S286 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S287 | 349 | ((two near dimensional near electron near gas) or 2DEG).clm. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S288 | 248 | S287 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S289 | 248 | S287 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S290 | 130 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S291 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S292 | 641 | S291 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S293 | 977 | S291 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S294 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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| S295 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S296 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S297 | 85 | S294 and S295 and S296 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S298 | 67 | S297 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S299 | 1 | S298 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S300 | 8 | S298 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |
| S301 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S302 | 977 | S301 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S303 | 567 | S302 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/18 12:52 |

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| S304 | 217 | S303 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S305 | 18 | S304 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S306 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S307 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/18 12:52 |
| S308 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 12:52 |
| S310 | 8 | ("5629539" \| "5691252" \| "5990507" \| "6174735" \| "6245631" \| "6278150" \| "6291292" \| "6337274"). PN. OR ("6707088").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/18 13:08 |
| S314 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S315 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |

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| S316 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S317 | 85 | S314 and S315 and S316 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S318 | 116 | S314 and S315 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S323 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S324 | 1162 | S316 and S323 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S331 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S332 | 1427 | S316 and S331 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S333 | 930 | S316 and S331 and S315 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S335 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S337 | 248 | S336 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S340 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |

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| S342 | 977 | S340 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S345 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S346 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S347 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S348 | 85 | S345 and S346 and S347 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S349 | 116 | S345 and S346 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S354 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S355 | 1162 | S347 and S354 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S362 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S363 | 1427 | S347 and S362 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |

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| S364 | 930 | S347 and S362 and S346 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S366 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S368 | 248 | S367 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S371 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S373 | 977 | S371 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S374 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S375 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S376 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S377 | 85 | S374 and S375 and S376 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S378 | 67 | S377 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |

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| S381 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S382 | 977 | S381 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S383 | 567 | S382 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S391 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S392 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S393 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S394 | 85 | S391 and S392 and S393 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S395 | 116 | S391 and S392 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S400 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |

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| S401 | 1162 | S393 and S400 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S408 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S409 | 1427 | S393 and S408 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S410 | 930 | S393 and S408 and S392 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S412 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S414 | 248 | S413 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S417 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S419 | 977 | S417 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S422 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S423 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S424 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |

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| S425 | 85 | S422 and S423 and S424 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S426 | 116 | S422 and S423 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S431 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S432 | 1162 | S424 and S431 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S439 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S440 | 1427 | S424 and S439 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S441 | 930 | S424 and S439 and S423 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S443 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S445 | 248 | S444 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S448 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S450 | 977 | S448 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |

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| S451 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S452 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S453 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S454 | 85 | S451 and S452 and S453 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S455 | 67 | S454 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S458 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S459 | 977 | S458 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S460 | 567 | S459 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S468 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |

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| S469 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S470 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S471 | 85 | S468 and S469 and S470 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S472 | 116 | S468 and S469 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S477 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S478 | 1162 | S470 and S477 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S485 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S486 | 1427 | S470 and S485 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S487 | 930 | S470 and S485 and S469 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S489 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S491 | 248 | S490 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |

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| S494 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S496 | 977 | S494 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S499 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S500 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S501 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S502 | 85 | S499 and S500 and S501 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S503 | 116 | S499 and S500 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S508 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S509 | 1162 | S501 and S508 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |

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| S516 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S517 | 1427 | S501 and S516 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S518 | 930 | S501 and S516 and S500 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S520 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:18 |
| S522 | 248 | S521 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S525 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S527 | 977 | S525 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S528 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S529 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S530 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S531 | 85 | S528 and S529 and S530 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |

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| S532 | 67 | S531 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S535 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S536 | 977 | S535 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:18 |
| S537 | 567 | S536 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S545 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S546 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:18 |
| S549 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S550 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S551 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |

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| S552 | 85 | S549 and S550 and S551 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S553 | 116 | S549 and S550 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S558 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S559 | 1162 | S551 and S558 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S566 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S567 | 1427 | S551 and S566 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S568 | 930 | S551 and S566 and S550 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S570 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S572 | 248 | S571 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S575 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S577 | 977 | S575 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |

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| S580 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S581 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S582 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S583 | 85 | S580 and S581 and S582 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S584 | 116 | S580 and S581 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S589 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S590 | 1162 | S582 and S589 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S597 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S598 | 1427 | S582 and S597 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S599 | 930 | S582 and S597 and S581 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S601 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |

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| S603 | 248 | S602 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S606 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S608 | 977 | S606 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S609 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S610 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S611 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S612 | 85 | S609 and S610 and S611 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S613 | 67 | S612 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S616 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |

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| S617 | 977 | S616 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S618 | 567 | S617 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S626 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S627 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S628 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S629 | 85 | S626 and S627 and S628 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S630 | 116 | S626 and S627 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S635 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S636 | 1162 | S628 and S635 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |

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| S643 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S644 | 1427 | S628 and S643 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S645 | 930 | S628 and S643 and S627 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S647 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S649 | 248 | S648 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S652 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S654 | 977 | S652 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S657 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S658 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S659 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S660 | 85 | S657 and S658 and S659 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |

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| S661 | 116 | S657 and S658 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S666 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S667 | 1162 | S659 and S666 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S674 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S675 | 1427 | S659 and S674 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S676 | 930 | S659 and S674 and S658 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S678 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S680 | 248 | S679 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S683 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S685 | 977 | S683 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S686 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |

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| S687 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S688 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S689 | 85 | S686 and S687 and S688 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S690 | 67 | S689 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S693 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S694 | 977 | S693 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S695 | 567 | S694 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S703 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S704 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |

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| S705 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S706 | 85 | S703 and S704 and S705 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S707 | 116 | S703 and S704 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S712 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S713 | 1162 | S705 and S712 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S720 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S721 | 1427 | S705 and S720 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S722 | 930 | S705 and S720 and S704 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S724 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S726 | 248 | S725 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S729 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |

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| S731 | 977 | S729 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S734 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S735 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S736 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S737 | 85 | S734 and S735 and S736 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S738 | 116 | S734 and S735 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S743 | 1450 | 257/192.ccls. and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S744 | 1162 | S736 and S743 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S751 | 1932 | (two near dimensional near electron near gas) or 2DEG | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S752 | 1427 | S736 and S751 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |

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| S753 | 930 | S736 and S751 and S735 | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S755 | 0 | ((two near dimensional near electron near gas) or 2DEG).abst. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/06/20 16:22 |
| S757 | 248 | S756 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S760 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S762 | 977 | S760 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S763 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S764 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S765 | 349967 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S766 | 85 | S763 and S764 and S765 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S767 | 67 | S766 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |

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| S770 | 333788 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S771 | 977 | S770 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/06/20 16:22 |
| S772 | 567 | S771 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S780 | 5068 | cascode near3 transistor$1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S781 | 8964 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/06/20 16:22 |
| S782 | 7165 | HEMT or (high near electron near mobility near transistor) or HFET | US-PGPUB; USPAT | OR | ON | 2010/09/24 16:32 |
| S783 | 816 | S782 and input and (Vdd or power adj supply) and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 16:33 |
| S784 | 593 | S783 and (gate and drain and source) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 16:34 |
| S785 | 79 | S784 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/09/24 16:34 |

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| S786 | 79 | S783 and ((gate near4 input) and (drain near4 (Vdd or power adj supply))) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 17:39 |
| S787 | 108 | S782 and ((gate near4 input) and (drain near4 (Vdd or power adj supply))) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 17:46 |
| S788 | 79 | S787 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2010/09/24 17:47 |
| S789 | 37 | ((gate adj voltage) near5 (depletion adj mode)) same ((gate adj voltage) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 17:55 |
| S790 | 2 | 257/192.ccls. and ((gate adj voltage) near5 (depletion adj mode)) and ((gate adj voltage) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 18:03 |
| S791 | 9 | HEMT and ((gate adj voltage) near5 (depletion adj mode)) and ((gate adj voltage) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 18:04 |
| S792 | 26 | HEMT and ((voltage bias) near5 (depletion adj mode)) and ((voltage bias) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 19:59 |
| S793 | 12 | ((voltage bias) with (depletion adj mode) with ground) same ((gate adj voltage) with (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 20:36 |
| S794 | 484 | ((voltage bias) near5 (depletion adj mode)) and ((voltage bias) near5 (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2010/09/25 20:39 |

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|---|---|---|---|---|---|---|
| S795 | 7 | ("5155449" \| "5774792" \| "5939945" \| "6137367" \| "6515547").PN. OR ("7071786").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2011/04/09 01:31 |
| S796 | 0 | 2005/000700 | US-PGPUB; USPAT; USOCR | OR | ON | 2011/04/09 11:35 |
| S797 | 2 | 2005/0007200 | US-PGPUB; USPAT; USOCR | OR | ON | 2011/04/09 11:35 |
| S798 | 0 | 2005/0007200 | US-PGPUB | OR | ON | 2011/04/09 11:36 |
| S799 | 2 | 10/873291 | US-PGPUB; USPAT; USOCR | OR | ON | 2011/04/09 11:37 |
| S800 | 23 | ((voltage bias) with (depletion adj mode) with ground) and ((gate adj voltage) with (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:48 |
| S801 | 6181 | HEMT or (high near electron near mobility near transistor) and ((voltage bias) with (depletion adj mode)) and ((gate adj voltage) with (enhancement adj mode)) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:51 |
| S802 | 6180 | HEMT or (high near electron near mobility near transistor) and (((voltage bias) with (depletion adj mode)) with ((gate adj voltage) with (enhancement adj mode))) and @ad<"20060320" | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:52 |
| S803 | 0 | S802 and merged near cascode | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:54 |
| S804 | 234 | S802 and cascode | US-PGPUB; USPAT | OR | ON | 2011/04/09 12:54 |

**4/9/2011 6:10:51 PM**
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Attorney Docket No.: 0400131

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | |
|---|---|
| In re Application of: **Herman, Thomas** | Art Unit: 2826 |
| Serial No.: 11/688,338 | Examiner: Ahmed, Selim U. |
| Filed: 03/20/2007 | |
| For: **Merged Gate Cascode Transistor** | |

## RESPONSE TO NON-FINAL OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the Non-Final Office Action dated October 6, 2010 in the above-referenced patent application. Please enter and consider the following remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

02/04/2011 HMARZI1 00000032 500731 11688338
01 FC:1251 130.00 DA



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**In the Claims:**

**Claim 1 (previously presented):** A merged cascode transistor circuit comprising:

an input voltage signal source;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a semiconductor element;

a source electrode electrically connected to a top surface of the semiconductor element;

a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;

a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate is also coupled to the semiconductor element;





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wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

**Claim 2 (previously presented):** The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:

a first III-Nitride layer; and

a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

**Claim 3 (previously presented):** The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates

and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 4 (previously presented):** The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

**Claim 5 (previously presented):** The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 6 (previously presented):** The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claim 7 (previously presented):** The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.



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**Claim 8 (previously presented):** The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

**Claim 9 (previously presented):** The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

**Claim 10 (previously presented):** A merged cascode high electron mobility transistor circuit comprises:

an input voltage signal source;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a first epitaxial layer of III-Nitride material;

a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

a source electrode electrically connected to the first epitaxial layer;

a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;





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a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;

wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

**Claim 11 (original):** The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.



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**Claim 12 (previously presented):** The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGaN material and the second epitaxial layer comprises a GaN material.

**Claim 13 (original):** The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claims 14 (previously presented):** The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

**Claim 15 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

**Claim 16 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.





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## REMARKS

Prior to the present response, claims 1-16 were pending in the present application. Applicant has amended no claims by the present response. Thus, claims 1-16 remain in the present application. Reconsideration and allowance of pending claims 1-16 in view of the following remarks are requested.

### A. Rejection of Claims 1-16 under 35 U.S.C. § 103(a)

In the Non-Final Office Action dated October 6, 2010 (hereinafter "Office Action") the Examiner has rejected claims 1-16 under 35 U.S.C. § 103(a) for purported obviousness over U.S. Patent Application Publication Number 2005/0189561 by Kinzer et al. (hereinafter "Kinzer") in view of U.S. Patent Application Publication Number 2004/0188761 by Koyama et al. (hereinafter "Koyama"). *See* pages 2-14, item 2 of the Office Action. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by previously presented claims 1 and 10, is patentably distinguishable over Kinzer and Koyama.

The present invention, as defined by independent claims 1 and 10, provides a circuit including an input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor, and a second gate positioned adjacent to the first gate, and between the source electrode and the drain



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electrode to form a second portion of the transistor, where the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. *See* claims 1 and 10 above. Claim 10 further defines that the transistor is a high electron mobility transistor (HEMT) wherein first and second epitaxial layers of III-nitride material in contact with each other such that a 2-dimensional electron gas conducting layer is formed between said layers are in place of said semiconductor element. *See* claim 10 above.

In an embodiment of the invention shown in Figure 3 of the present application, HEMT 30 includes first portion Q1 including gate 32, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source contact 31 and drain contact 34. *See, e.g.,* paragraph [0023] and Figure 3 of the present application. HEMT 30 also includes second portion Q2 including gate 33, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source contact 31 and drain contact 34. In HEMT 30, node 24 is between first portion Q1 and second portion Q2. *See, e.g., id.* at Figure 3, Figure 2 and related text, and paragraph [0023].

As disclosed in the present application, in an embodiment of the present invention, first portion Q1 is an enhancement mode transistor (normally OFF) and second portion Q2 is a depletion mode transistor (normally ON). *See, e.g., id.* at paragraph [0023] and Figure 3. Further disclosed in the present application, an input voltage signal is connected to gate 32 provide a gate voltage Vg1. *See, e.g., id.* at paragraph [0016]. Furthermore, a voltage is connected to gate 33 to provide a set voltage to Vg2, for example 0v. *See, e.g., id.* at Figure 3 and paragraphs [0025] and [0017. When the input voltage at Vg1 goes low, the first portion Q1 turns OFF. As a result, the voltage at the node 24 rises until the gate-source voltage of second portion Q2 reaches a set pinch off voltage and the second portion Q2 turns OFF. *See, e.g., id.* at paragraph [0018]. Thus, an embodiment of the present invention advantageously provides for a circuit where the drain swing of the first portion Q1 is substantially reduced. *Id.*

In contrast to the present invention as defined by independent claims 1 and 10, Kinzer does not disclose a circuit including an input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor where the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the

transistor is a depletion mode transistor. Kinzer specifically discloses device 40 in Figure 3 and device 50 in Figure 4. As disclosed in Kinzer, device 40 includes first gate electrode 32 and second gate electrode 34, which are situated between source/drain electrodes 25 and 26. *See, e.g.*, paragraph [0032] and Figure 3 of Kinzer.

However, as disclosed in Kinzer, device 50 includes gate electrodes 32 and 34, which are situated between source/drain electrodes 25 and 26. *See, e.g., id.* at Figure 4 and related text. In Kinzer both gate electrode 32 and gate electrode 34 are disposed within a recess 38 in second semiconductor body 21. *See id.* at paragraph [0038] and Figure 4. Kinzer teaches that in its device, each recess 38 causes an interruption in the 2DEG, which can be restored by applying a suitable voltage to gate electrodes 32 and 34. *See id.* at paragraphs [0038] and [0030]. Furthermore, Kinzer teaches that device 50 is an enhancement mode device (i.e. a normally off device) specifically because of having the structural feature of two recesses 38 and is defined as performing an AND gate logic function such that current flows between electrodes 25, 26 when both gate electrodes 32, 34 have a potential applied to them. *See id.* at paragraph [0039]. Thus, what the Examiner appears to allege as a first portion of a merged cascode transistor cannot be a depletion mode transistor and what the Examiner appears to allege as a second portion of a merged cascode transistor also cannot be a depletion mode transistor regardless of voltages applied to respective gates. Thus, device 50 cannot be a merged cascode transistor, wherein a first portion of the merged cascode transistor is an enhancement

mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor, as specified in independent claims 1 and 10.

As disclosed in Kinzer, device 40 is a depletion mode device (i.e. normally ON), acting as a logic NOR gate, wherein an appropriate voltage applied to either gate electrode 32 or gate electrode 34 causes an interruption in the 2DEG, thereby turning device 40 off. *See, e.g., id.* at paragraphs [0033] and [0036], and Figure 3. Kinzer teaches that device 50 is a depletion mode device specifically because it has no recess 38 to interrupt 2DEG. *See id.* at paragraphs [0038] and [0030]. Thus, once again, what the Examiner appears to allege as a first portion of a merged cascode transistor is cannot be a enhancement mode transistor and what the Examiner appears to allege as a second portion of a merged cascode transistor also cannot be an enhancement mode transistor regardless of voltages applied to respective gates. Thus, device 40 cannot be a merged cascode transistor, wherein a first portion of the merged cascode transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor, as specified in independent claims 1 and 10.

Thus, Kinzer fails to disclose a merged cascode transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, as specified in independent claims 1 and 10. Rather, Kinzer discloses separate devices 40 and 50, where device 40 is a depletion mode device and device 50 is an enhancement mode device. However, independent claims 1 and 10 specify a merged cascode transistor wherein a first portion of the merged cascode

transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor. Thus, independent claims 1 and 10 require the merged cascode transistor include an enhancement mode transistor and a depletion mode transistor. Consequently, Applicant submits that devices 40 and 50 disclosed in Kinzer are significantly different than the merged cascode transistor specified in independent claims 1 and 10. As such, Applicant submits that Kinzer fails to disclose or suggest the present invention, as defined by independent claims 1 and 10.

In the Office Action, the Examiner asserts that the requirement that the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor is a purely functional distinction. *See, e.g.,* page 4-5 of the Office Action. Applicant respectfully disagrees and submits that whether a device includes an enhancement mode transistor or a depletion mode transistor is a structural distinction. For example, in the present application, first portion Q1 can be an enhancement mode transistor by using a recessed gate, fluorine implants, or other suitable means. *See* paragraph [0023] and Figure 3 of the present application. By the Examiner's logic, device 40 and device 50 in Kinzer are identical, which, they clearly are not. Thus, whether a device includes an enhancement mode transistor or a depletion mode transistor is a tangible distinction and the devices in Kinzer would require significant and tangible modification in order to disclose an identical device.

The Examiner further asserts that an input voltage signal source connected to the gates of Kinzer's enhancement mode transistor and a constant voltage source having a

predetermined constant voltage connected to the gates of Kinzer's depletion mode transistor are specifically required to operate or function. *See* page 4 of the Office Action. Applicant respectfully asserts that this is inaccurate. Although some bias must be applied to the gates of the two above described circuits of Kinzer, the specific arrangement where an input voltage signal source, and not a constant voltage source, is connected to the gates of the enhancement mode transistor and vice versa for the gates of the depletion mode transistor are not the only arrangements that would allow Kinzer's two embodiments to function. Further, Applicant respectfully points out that applying a constant voltage source to one of the gates of enhancement mode transistor 50 would permanently block conduction through the transistor unless that constant voltage were a positive value sufficient enough to create a channel under that gate. Thus, this specific arrangement is not required for Kinzer's structures to function.

The Examiner additionally asserts that if a prior art structure is capable of performing the purpose or intended use of the present invention, it meets the claim and further, that it is reasonable to assume that either of the above described embodiments of Kinzer are capable of performing in enhancement mode or depletion mode. *See* pages 5-6 of the Office Action. However, as stated above, because neither of Kinzer's embodiments include both an enhancement mode and a depletion mode portion in a single transistor, rather two depletion mode or two enhancement mode portions, applying voltages, as defined in claims 1 and 10 of the present invention, to either of Kinzer's above described embodiments would not yield the same structure with the same function

as the present invention. Thus Applicant respectfully asserts that Kinzer does not meet claims 1 and 10 of the present application.

Turning to Koyama, that disclosure is directed toward a source follower circuit, which can be operated without increasing a power supply voltage than the desired value, thus maintaining a low power supply voltage and low power consumption. *See* paragraph [0031] of Koyama. The Examiner states that Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 device, respectively. *See* page 4 of the Office Action. However, upon close examination, it can be seen that input terminal 103 is specified only as an input terminal. *See* paragraph [0040] of Koyama. Nowhere does Koyama state that input 103 is a constant voltage source. Further, applying a constant voltage to the source follower as in Figure 1A of Koyama would not result in selective switching of any kind. The source follower would either always conduct or never conduct depending on the value of the constant voltage input at 103. Thus, contrary to the Examiner's assertion, Applicant respectfully submits that Koyama does not specifically disclose a constant voltage source input to a depletion mode transistor.

Thus, each of Kinzer and Koyama fail to disclose a circuit including a constant voltage source having a predetermined constant voltage, and/or a merged cascode transistor where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Consequently, even if the Office Action provided a reasonable incentive for one skilled in the art to combine the

cited art references Kinzer and Koyama, Applicant respectfully submits that the resulting combination would still fail to disclose or suggest the present invention as defined by independent claims 1 and 10.

For the foregoing reasons, Applicant respectfully submits that at the time the invention defined by independent claims 1 and 10 was made, the invention would not have been obvious to a person of ordinary skill in the art through application of Kinzer and Koyama, either singly or in any combination. Thus, Applicant respectfully submits that independent claims 1 and 10 are patentably distinguishable over Kinzer and Koyama. As such, claims 2-9 and 11-16, depending respectively from patentable independent claims 1 and 10 are also patentably novel and inventive over Kinzer and Koyama for at least the reasons presented above, and also for the additional limitations contained in each dependent claim.

**B. Rejection of Claims 10-16 under 35 U.S.C. §103(a)**

The Examiner has rejected claims 10-16 under 35 U.S.C. § 103(a) for purported obviousness over Kinzer in view of Koyama and in further view of U.S. Patent Number 7,052,942 to Smart et al. (hereinafter "Smart"). *See* pages 14-19, item 3 of the Office Action. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by previously presented independent claim 10, is patentably distinguishable over Kinzer, Koyama and Smart.



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The present invention, as defined by amended independent claim 10, provides a circuit including input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor including a first epitaxial layer of III-Nitride material, a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers, a source electrode electrically connected to the first epitaxial layer, a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode, a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor, and a second gate positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor, where the first gate is connected the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. *See* claim 10 of the present invention.

For reasons similar to those presented above, Applicant respectfully asserts that neither Kinzer nor Koyama, or any combination of Kinzer and Koyama, discloses or





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suggests a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, as specifically required by independent claim 10.

In the Office Action, the Examiner suggests combining Kinzer and Koyama with Smart to overcome the omission from the combination of Kinzer and Koyama of any express teaching that the described III-Nitride (AlGaN and GaN) layers are epitaxial. *See* page 16 of the Office Action. Smart specifically discloses HEMT 28 including GaN buffer layer 22 and AlGaN Schottky layer 24. *See, e.g.*, Figure 2 and related text of Smart. However, in Smart, HEMT 28 includes only a single gate contact 32. *See id.*

Thus, Smart, like Kinzer and Koyama, fails to disclose or suggest a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, as specified in independent claim 10. Consequently, Smart fails to cure the aforementioned deficiencies of Kinzer and Koyama. As such, Applicant submits that the combination of Kinzer,

Koyama and Smart suggested by the Examiner does not and cannot result in the present invention, as defined by independent claim 10.

For the foregoing reasons, Applicant respectfully submits that at the time the invention defined by independent claim 10 was made, the invention would not have been obvious to a person of ordinary skill in the art by Kinzer, Koyama and Smart, either singly or in any combination. Thus, Applicant respectfully asserts that independent claim 10 is patentably distinguishable over Kinzer, Koyama and Smart and, as such, claims 11-16 depending from patentable independent claim 10 are, *a fortiori*, also patentably distinguishable over Kinzer, Koyama and Smart for at least the reasons presented above, and also for additional limitations contained in each dependent claim.

### C. Conclusion

For all the foregoing reasons, Applicants respectfully submit that the present invention, as defined by independent claims 1 and 10, and claims depending therefrom, is patentably novel and inventive. Moreover, Applicant asserts that no new matter has been introduced herein. Accordingly, an early allowance of pending claims 1-16 is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Attorney Docket No.: 0400131

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 2/3/11

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Signature Date



IR-3234

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Date: February 3, 2011

To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826

Fax: (571) 273-8300

Re: **Application Serial No.: 11/688,338**
Filing Date: 3/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 23

Message:

Enclosed please find the Response to Non-Final Office Action dated October 6, 2010

Authorization is hereby given to the Director to charge any fees associated with this communication or credit any overpayment to Deposit Account **50-0731**.

Thank you.

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Attorney Docket No.: 0400131

# AMENDMENT COVER SHEET

IN RE APPLICATION OF: Herman, Thomas

SERIAL NO.: 11/688,338 FILED: 3/20/2007

FOR: Merged Gate Cascode Transistor

HONORABLE COMMISSIONER FOR PATENTS
P.O. Box 1450, Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith is a paper in the above-identified application. Any necessary extension of time period set for this paper is hereby requested.

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☒ The fee has been calculated as shown below:

☒ EXTENSION FEE

| | RATE Non-Small Entity | RATE Small-Entity | FEE |
|---|---|---|---|
| FIRST MONTH AFTER TIME PERIOD SET | 130.00 | 65.00 | $ 130.00 |
| SECOND MONTH AFTER TIME PERIOD SET | 490.00 | 245.00 | $ |
| THIRD MONTH AFTER TIME PERIOD SET | 1,110.00 | 555.00 | $ |
| FOURTH MONTH AFTER TIME PERIOD SET | 1,730.00 | 865.00 | $ |

☒ TOTAL EXTENSION FEE $ 130.00

☐ FEE FOR EXTRA CLAIMS added by Amendment in this response:

| | Column 1 Number of Claims after Amendment | Column 2 Number Previously Paid for | Column 3 Number of Extra Claims | RATE Non-Small Entity | RATE Small Entity | FEE |
|---|---|---|---|---|---|---|
| TOTAL CLAIMS | | MINUS ** | * = 0 | x 52 | x 26 | $ |
| INDEPENDENT | | MINUS ** | * = 0 | x 220 | x 110 | $ |
| First presentation of multiple dependent claim | | | | + 390 | + 195 | $ |

TOTAL FEE FOR EXTRA CLAIMS $ 0.00

* If the entry in Column 1 is less than the entry of Column 2, write "0" in Column 3.
** If the number of Total Claims previously paid for is less than 20, write "20" in this space.
*** If the number of Independent Claims previously paid for is less than 3, write "3" in this space.



PAGE 2/23 * RCVD AT 2/3/2011 6:16:43 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-5/32 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):04-32

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Attorney Docket No.: 0400131

☐ Total fee for Supplemental Information Disclosure Statement $

☐ Enclosed is the total fee of $0.00 (Payment by Credit Card, Form PTO-2038 Enclosed).

☒ Please charge Deposit Account No. 50-0731 in the amount of $130.00

☒ The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Date: 2/3/11

By: _____
Michael Farjami, Reg. No. 38,135

*CERTIFICATE OF FACSIMILE TRANSMISSION*
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2/3/11
Date

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EVAN C. GUNDERMAN
Name of Person Performing Facsimile Transmission

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PAGE 3/23 * RCVD AT 2/3/2011 6:16:43 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-5/32 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):04-32

PTO/SB/06 (07-06)
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# PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

| Application or Docket Number | Filing Date | ☐ To be Mailed |
|---|---|---|
| 11/688,338 | 03/20/2007 | |

## APPLICATION AS FILED – PART I

| FOR | (Column 1) NUMBER FILED | (Column 2) NUMBER EXTRA | SMALL ENTITY ☐ RATE ($) | SMALL ENTITY ☐ FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | OTHER THAN SMALL ENTITY FEE ($) |
|---|---|---|---|---|---|---|---|
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| AMENDMENT | 02/03/2011 | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE ($) | SMALL ENTITY ADDITIONAL FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | OTHER THAN SMALL ENTITY ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * 16 | Minus | ** 20 | = 0 | X $ = | | OR | X $52= | 0 |
| | Independent (37 CFR 1.16(h)) | * 2 | Minus | ***3 | = 0 | X $ = | | OR | X $220= | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | 0 |

| AMENDMENT | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/BURNELL L. ROSS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | Thomas Herman | 0400131 | 9886 |

25700 7590 10/06/2010

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

| EXAMINER | |
|---|---|
| AHMED, SELIM U | |
| **ART UNIT** | **PAPER NUMBER** |
| 2826 | |
| **MAIL DATE** | **DELIVERY MODE** |
| 10/06/2010 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 11/688,338 | HERMAN, THOMAS | |
| | Examiner | Art Unit | |
| | SELIM AHMED | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 December 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/17/2009 has been entered.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer ET al (2005/0189561; Kinzer hereinafter) in view of Koyama (US 2004/0188761; Koyama hereinafter).

With regard to claim 1, Fig. 4 of Kinzer discloses a merged gate transistor circuit comprising: a merged cascode transistor (Fig.4) comprising: a semiconductor element (element comprising of 21, 22, 23, and 24 i.e. substrate); a source electrode 25 electrically connected to a top surface (top surface of 21 in Fig. 4) of the semiconductor element; a drain electrode 26 electrically connected

to the top surface of the semiconductor element and spaced laterally away from the source electrode 25; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and capacitively coupled to the semiconductor element (para[0035]) to form a first portion of the transistor (e.g. Fig. 4, portion of transistor 32); and a second gate 34 positioned adjacent to the first gate 32, and between the source electrode 25 and the drain electrode 26 to form a second portion of the transistor (e.g. Fig. 4, portion of transistor 34), wherein the second gate 34 is also capacitively coupled to the semiconductor element (para[0035]); wherein in the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, Kinzer discloses the claim 1 limitations but does not explicitly disclose an input voltage signal source, a constant voltage source having a predetermined constant voltage; wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between to the constant voltage source and a voltage at the source electrode reaches a predetermined level. However, applicant's above limitations directed to functional limitations as to depletion mode and enhancement mode transistor. The above limitations, particularly, an input

voltage signal source and a constant voltage source having a predetermined constant voltage are bias voltages to the enhancement and depletion mode transistors that are required to operate/function of the device. Although Kinzer does not explicitly disclose an input voltage signal source and a constant voltage source having a predetermined constant voltage, Kinzer depletion mode and enhancement mode devicea require these bias conditions to operate/function. However, for example, Figs. 1, 2, 5 and para[0059] of Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 devices. Since it is common knowledge to apply bias voltages to the gates of the depletion and enhancement mode devices for device operation, it would have been obvious to one having ordinary skill in the art at the time of the invention to include an input voltage signal source and a constant voltage source having a predetermined constant voltage within Kinzer device to operate/function of the device.

The applicant's claims **1, 6, 7** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of using the first portion of the transistor for conducting while using the input voltage signal for providing an input voltage above a predetermined threshold voltage that is a pinch off voltage of the second portion of the transistor and running the first

portion of the transistor and the second portion of the transistor in enhancement and depletion mode, respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer**'s devices 32, 34 are capable of performing in enhancement mode or depletion mode respectively (refer to claims 9 &10 and para[0026, 0033, 0038]), because a comparison of

Applicant's specification to **Kinzer**'s disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode as indicated in the claims 9, 10, and para[0026, 0033, 0038]). Because it is reasonable to assume that **Kinzer**'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

Furthermore, Kinzer discloses all of the limitation of claim 1 with the exception of "a merged cascode transistor circuit" as recited in the preamble. As disclosed in the MPEP 2111.02, preamble statement reciting purpose or intended use not given significant patentable weight if there is no structural difference between the claimed invention and prior art. Kinzer discloses a bi-directional switch that is structurally identical claimed by applicant. The exception is that the merged cascode transistor. However, this feature is a purpose/intended use of the Applicant's device and does not structurally limit feature of the claim. The structure of the claim device is the same as that of the prior art. Therefore, the claimed invention does not distinguish over the Kinzer's device. Note that a recitation of the purpose/intended use such as "merged gate cascode transistor" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the purpose/intended use, it meets the claim.

With regard to claim 2, Fig. 4 of Kinzer et al discloses the merged gate transistor circuit of claim 1, wherein the semiconductor element further comprises: a first III-Nitride layer 21; and a second III-Nitride layer 23 on which the first III-Nitride layer is positioned such that a 2DEG conduction layer 22 forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer (e.g. para [00320]).

With regard to claim 3, figure 4 of Kinzer et al discloses the merged gate transistor circuit of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 4, Fig. 4 and elements 21, 23 of Kinzer et al disclose the merged gate transistor circuit of claim 3, wherein the first III-Nitride layer comprises AlGaN material, and the second III-Nitride layer comprises GaN material.

With regard to claim 5, figure 4 and claim 3 of Kinzer et al disclose the merged gate transistor circuit of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such

that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 8, para [0025] of Kinzer et al disclose the merged gate transistor circuit of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 9, para [0025] of Kinzer et al disclose the merged gate transistor circuit of claim 8, wherein the insulation layer is comprised of silicon nitride.

With regard to claim 10, Fig.4 of Kinzer et al discloses a merged cascade high electron mobility transistor circuit comprises: a first epitaxial layer 21 of III-Nitride material; a second epitaxial layer 23 of a III-Nitride material, in contact with the first epitaxial layer 21 such that a 2-dimensional electron gas conducting layer 22 is formed between the first 21 and second 23 epitaxial layers; a source electrode 25 electrically connected to the first epitaxial layer 21; a drain electrode 26 electrically connected to the first epitaxial layer 21 and spaced laterally from the source electrode; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and coupled to the first epitaxial layer to form a first portion (e.g. Fig. 4, portion of transistor 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode 26 and

source electrode 25 and coupled to the first epitaxial layer 21 to form a second portion (e.g. Fig. 4, portion of transistor 34) of the transistor; and wherein the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, Kinzer discloses the claim limitations but does not explicitly disclose an input voltage signal source, a constant voltage source having a predetermined constant voltage; wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between to the constant voltage source and a voltage at the source electrode reaches a predetermined level. However, applicant's above limitations directed to functional limitations as to depletion mode and enhancement mode transistor. The above limitations, particularly, an input voltage signal source and a constant voltage source having a predetermined constant voltage are bias voltages to the enhancement and depletion mode transistors that are required to operate/function of the device. Although Kinzer does not explicitly disclose an input voltage signal source and a constant voltage source having a predetermined constant voltage, Kinzer device requires these bias condition to operate/function. However, for example, Figs. 1, 2, 5 and

para[0059] of Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 devices. Since it is common knowledge to apply bias voltages to the gates of the depletion and enhancement mode devices for device operation, it would have been obvious to one having ordinary skill in the art at the time of the invention to include an input voltage signal source and a constant voltage source having a predetermined constant voltage within Kinzer device to operate/function of the device.

As discussed above, Kinzer discloses all of the structural limitations of claims 10-16 with the exception of not explicitly disclosing that the III-Nitride (AlGaN and GaN) layers are formed by an epitaxial process. Applicant's claims, however, do not distinguish over the Kinzer reference by virtue of the process used to form the III-Nitride layers, since only the final product is relevant, not the process of forming the III-Nitride material epitaxially. Note that a "product by process claim" is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or

obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Furthermore, Kinzer discloses all of the limitation of claim 10 with the exception of “merged cascode high electron mobility transistor circuit” as recited in the preamble. As disclosed in the MPEP 2111.02, preamble statement reciting purpose or intended use not given significant patentable weight if there is no structural difference between the claimed invention and prior art. Kinzer discloses a bi-directional switch that is structurally identical claimed by applicant. The exception is that the merged cascode high electron mobility transistor. However, this feature is a purpose/intended use of the Applicant's device and does not structurally limit feature of the claim. The structure of the claim device is the same as that of the prior art. Therefore, the claimed invention does not distinguish over the Kinzer’s device. Note that a recitation of the purpose/intended use such as “merged cascode high electron mobility transistor” of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the purpose/intended use, it meets the claim.

Furthermore, applicant's claims 10, 13, 14 do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed

and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer**'s devices 32, 34 are capable of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively, because a comparison of Applicant's specification to **Kinzer**'s disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively. Because it is reasonable to

assume that **Kinzer**'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 11, figure 4 and claim 3 of Kinzer et al disclose the merged cascode high electron mobility transistor circuit of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

With regard to claim 15, para [0025] of Kinzer et al disclose the merged gate transistor circuit of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 16, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

3. Claims 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer in view of Koyama and further in view of Smart et al (US 7,052,942; Smart hereinafter).

With regard to claims 10, 12, 13, 14, e.g. Fig.4 of Kinzer in view of discloses a merged cascode high electron mobility transistor circuit comprises: a first layer 21 of III-Nitride material; a second layer 23 of a III-Nitride material, in contact with

the first layer 21 such that a 2-dimensional electron gas conducting layer 22 is formed between the first 21 and second 23 layers; a source electrode 25 electrically connected to the first layer 21; a drain electrode 26 electrically connected to the first layer 21 and spaced laterally from the source electrode; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and coupled to the first layer to form a first portion (e.g. Fig. 4, portion of transistor 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode 26 and source electrode 25 and coupled to the first layer 21 to form a second portion (e.g. Fig. 4, portion of transistor 34) of the transistor; and wherein the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, Kinzer discloses the claim limitations but does not explicitly disclose an input voltage signal source, a constant voltage source having a predetermined constant voltage; wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between to the constant voltage source and a voltage at the source electrode reaches a predetermined level. However, applicant's above limitations directed to functional limitations as to depletion mode and

enhancement mode transistor. The above limitations, particularly, an input voltage signal source and a constant voltage source having a predetermined constant voltage are bias voltages to the enhancement and depletion mode transistors that are required to operate/function of the device. Although Kinzer does not explicitly disclose an input voltage signal source and a constant voltage source having a predetermined constant voltage, Kinzer device requires these bias condition to operate/function. However, for example, Figs. 1, 2, 5 and para[0059] of Koyama discloses an input voltage signal source 503 and a constant voltage source having a predetermined constant voltage 103 for a depletion mode 101 and enhancement mode 501 devices. Since it is common knowledge to apply bias voltages to the gates of the depletion and enhancement mode devices for device operation, it would have been obvious to one having ordinary skill in the art at the time of the invention to include an input voltage signal source and a constant voltage source having a predetermined constant voltage within Kinzer device to operate/function of the device.

As discussed above, the difference between the device disclosed by Kinzer et al and that claimed lies in the recital of “epitaxial” layer, i.e. layers formed by epitaxy. Smart discloses forming an AlGaN layer by epitaxy over a GaN layer, also formed by epitaxy. Smart’s epitaxially formed AlGaN and GaN layers create a 2DEG layer between them that creates the thin, high mobility channel needed for proper performance of the device disclosed by Kinzer. It therefore seems

clear that one of ordinary skill in the art could have applied Smart's known "improvement" technique to Kinzer's "base" device in the same way Smart applies it to a "comparable" device and that in the view of one of skill in the art, the results would have predictably produced the 2DEG layer required by Kinzer's device. See MPEP § 2143, part "C".

With regard to claims 10 and 12, as discussed above, Kinzer et al disclose all of the structural limitations with the exception of not disclosing the III-Nitride (AlGaN and GaN) layers being epitaxial explicitly. However, e.g. Fig.2, elements 24, 22 of Smart discloses the AlGaN and GaN layers. It would have been obvious to one having ordinary skill in the art at the time of the invention to substitute Smart's epitaxial III-Nitride (AlGaN and GaN) layers with Kinzer's III—Nitride (AlGaN and GaN) layers for predictable results such as, low leakage characteristics of the HEMT device.

Furthermore, applicant's claims **10, 13, 14** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined

constant voltage and a voltage at the source electrode reaches a predetermined level. In another words, first portion or transistor 32 and second portion or transistor 34 are functioning as an enhancement and depletion mode respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer**'s devices 32, 34 are capable of performing as an enhancement mode and depletion mode respectively (refer to claims 9 &10 and para [0026, 0033, 0038]), because a comparison of Applicant's specification to **Kinzer**'s disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode. Because it is reasonable to assume that **Kinzer**'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 11, figure 4 of Kinzer et al discloses the merged cascode high electron mobility transistor circuit of claim 10, further comprising an insulating layer positioned between the first and second gates and the first layer.

With regard to claim 15, para [0025] of Kinzer et al disclose the merged gate transistor circuit of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 16, para [0025] of Kinzer et al disclose the merged gate transistor circuit of claim 8, wherein the insulation layer is comprised of silicon nitride.

### *Response to Arguments*

10. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

### Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SELIM AHMED/
Examiner, Art Unit 2826

/Sue A. Purvis/

Supervisory Patent Examiner, Art Unit 2826

| Notice of References Cited | Application/Control No. 11/688,338 | Applicant(s)/Patent Under Reexamination HERMAN, THOMAS | |
|---|---|---|---|
| | Examiner SELIM AHMED | Art Unit 2826 | Page 1 of 1 |

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| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
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| * | B | US-6,903,383 B2 | 06-2005 | Yokogawa et al. | 257/192 |
| * | C | US-2005/0189561 A1 | 09-2005 | Kinzer et al. | 257/192 |
| * | D | US-7,052,942 B1 | 05-2006 | Smart et al. | 438/162 |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
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| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

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| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11688338 | HERMAN, THOMAS |
| | Examiner | Art Unit |
| | SELIM AHMED | 2826 |

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|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 05/22/2008 | 12/08/2008 | 03/20/2009 | 06/20/2009 | 09/25/2010 | | | | |
| | 1 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 2 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 3 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 4 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 5 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 6 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 7 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 8 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 9 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 10 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 11 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 12 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 13 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 14 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 15 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | 16 | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11688338 | HERMAN, THOMAS |
| | Examiner | Art Unit |
| | SELIM AHMED | 2826 |

## SEARCHED

| Class | Subclass | Date | Examiner |
|---|---|---|---|
| 257 | 192, 194, 195, E29.14, E29.144, E29.246, E29.249 | 5/22/08 | SA |
| | Updated search | 12/8/08 | /sa/ |
| | Updated search | 3/20/2009 | /sa/ |
| | Updated search | 6/20/2009 | /sa/ |
| | Updated search | 9/24/2010 | /sa/ |

## SEARCH NOTES

| Search Notes | Date | Examiner |
|---|---|---|
| Text search such as two dimensional electron gas, Cascode transistor, HEMT/High electron mobility transistor, source, drain, gate and their boolean combinations were searched. | 5/22/08 | SA |
| Updated search | 12/8/2008 | /sa/ |
| Updated search | 3/20/2009 | /sa/ |
| Updated search | 9/24/2010 | /sa/ |

## INTERFERENCE SEARCH

| Class | Subclass | Date | Examiner |
|---|---|---|---|
| 257 | 192, 194, 195, | 5/22/08 | SA |

## EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
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| S1 | 1 | "11688338" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/15 18:55 |
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| S3 | 4541 | cascode near3 transistor $1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:21 |
| S4 | 7876 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S5 | 314831 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S6 | 73 | S3 and S4 and S5 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:22 |
| S7 | 96 | S3 and S4 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:23 |
| S8 | 63 | S6 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:23 |

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| S13 | 1116 | S5 and S12 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:54 |
| S14 | 356 | S5 and S12 and S4 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/05/21 17:54 |
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| S22 | 773 | S5 and S20 and S4 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/05/21 18:29 |
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| S37 | 80 | S34 and S35 and S36 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S38 | 107 | S34 and S35 and cascode | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
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| S45 | 365 | S36 and S43 and S35 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
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| S52 | 1310 | S36 and S51 | US-PGPUB; USPAT; USOCR | OR | OFF | 2008/12/08 09:49 |
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| S54 | 725 | S53 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
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| S58 | 244 | S56 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/12/08 09:49 |
| S59 | 125 | (daniel near kinzer).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S60 | 321547 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |

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|---|---|---|---|---|---|---|
| S61 | 596 | S60 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S62 | 915 | S60 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2008/12/08 09:49 |
| S63 | 4932 | cascode near3 transistor $1 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S64 | 8697 | HEMT or (high near electron near mobility near transistor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S65 | 341649 | source and drain and gate | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S66 | 82 | S63 and S64 and S65 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S67 | 66 | S66 and @ad<"20060320" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |
| S68 | 1 | S67 and epi | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:03 |

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|---|---|---|---|---|---|---|
| S69 | 8 | S67 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:05 |
| S70 | 327776 | "257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:13 |
| S71 | 944 | S70 and HEMT | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:13 |
| S72 | 549 | S71 and (epi or epitaxial) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2009/03/19 18:13 |
| S73 | 213 | S72 and ((two near dimension$3 near electron near gas) or 2DEG) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:14 |
| S74 | 15 | S73 and ((AlN and GaN) with (epi epitaxial)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:15 |
| S75 | 2 | "7052942".pn. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:27 |
| S76 | 2 | "10689980" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2009/03/19 18:27 |

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|---|---|---|---|---|---|---|
| S77 | 19 | ("20020031851" \| "20020048302" \| "20040070003" \| "5698870" \| "5834326" \| "5843590" \| "5874747" \| "6110757" \| "6384433" \| "6387733" \| "6448793" \| "6455877" \| "6560452" \| "6633073" \| "6706576" \| "6750482" \| "6802902" \| "6815722").PN. OR ("7052942").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2009/03/19 18:31 |

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# BIB DATA SHEET

**CONFIRMATION NO. 9886**

| SERIAL NUMBER | FILING or 371(c) DATE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007<br>RULE | 257 | 2826 | 0400131 |

**APPLICANTS**

Thomas Herman, Manhattan Beach, CA;

**** CONTINUING DATA ***************************

This appln claims benefit of 60/783,934 03/20/2006

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

03/29/2007

| Foreign Priority claimed | 35 USC 119(a-d) conditions met | Verified and Acknowledged | Met after Allowance | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|---|---|
| ☐ Yes ☑ No | ☐ Yes ☑ No | /SELIM U AHMED/ Examiner's Signature | ☐ Initials | CA | 4 | 16 | 2 |

**ADDRESS**

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691
UNITED STATES

**TITLE**

MERGED GATE CASCODE TRANSISTOR

| FILING FEE RECEIVED | FEES: Authority has been given in Paper | |
|---|---|---|
| 1130 | No._____ to charge/credit DEPOSIT ACCOUNT<br>No._____ for following: | ☐ All Fees<br>☐ 1.16 Fees (Filing)<br>☐ 1.17 Fees (Processing Ext. of time)<br>☐ 1.18 Fees (Issue)<br>☐ Other _____<br>☐ Credit |

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# REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

| | |
|---|---|
| *Application Number* | 11/688,338 |
| *Filing Date* | 03/20/2007 |
| *First Named Inventor* | Herman |
| *Group Art Unit* | 2826 |
| *Examiner Name* | Ahmed, Selim U. |
| *Attorney Docket Number* | 0400131 |

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

*NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53 (d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Final Rule, 65 Fed Reg. 50092 (Aug. 16, 2000); Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 Off. Gaz. Pat Office 47 (Apr. 11, 2000), which established RCE practice.*

1. Submission required under 37 C.F.R. § 1.114
   - a. ☐ Previously submitted
     - i. ☐ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on _____ (Any unentered amendment(s) referred to above will be entered).
     - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - iii. ☐ Other _____
   - b. ☒ Enclosed
     - i. ☒ Amendment/Reply
     - ii. ☐ Affidavit(s)/Declaration(s)
     - iii. ☐ Information Disclosure Statement (IDS)
     - iv. ☐ Other _____
2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R.§ 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months. Fee under 37 C.F.R. § 1.17(i) required)
   - b. ☐ Other _____
3. Fees — The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-0731
     - i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)
     - ii. ☒ Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)
     - iii. ☒ Other _____
   - b. ☐ Check in the amount of $ _____ enclosed.
   - c. ☒ Payment by credit card for the amount of $ 1,920.00 (Form PTO-2038 enclosed).

| *SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED* | | | |
|---|---|---|---|
| *Name (Print/Type)* | Michael Farjami, Esq. | *Registration No. (Attorney/Agent)* | 38135 |
| *Signature* | | *Date* | 12/17/09 |

*CERTIFICATE OF MAILING OR TRANSMISSION*

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office on:

| | | | |
|---|---|---|---|
| *Name (Print/Type)* | Christina Carter Ellis | | |
| *Signature* | Christina Carter Ellis | *Date* | 12/17/09 |

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Attorney Docket No.: 0400131

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| In re Application of: **Thomas Herman** | Art Unit: 2826 |
| Serial No.: 11/688,338 | Examiner: Ahmed, Selim U. |
| Filed: 03/20/2007 | |
| For: **Merged Gate Cascode Transistor** | |

## AMENDMENT AND RESPONSE TO *FINAL OFFICE ACTION*

**Mail Stop RCE**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the ***Final Office Action*** dated June 25, 2009 in the above-referenced patent application. Please enter and consider the following amendments and remarks in light of the attached ***Request for Continued Examination*** filed under 37 CFR §1.114 in the above-identified application.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

12/18/2009 HMARZI1 00000025 11688338
02 FC:1253 1110.00 OP



PAGE 4/21 * RCVD AT 12/17/2009 8:01:36 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-5/28 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):04-48

**In the Claims:**

**Claim 1 (currently amended):** A merged cascode transistor circuit comprising:

an input voltage signal source;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a semiconductor element;

a source electrode electrically connected to a top surface of the semiconductor element;

a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;

a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate is also coupled to the semiconductor element;

wherein the first gate is connected to ~~an input voltage signal~~ the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to ~~a predetermined constant voltage~~ the constant voltage source such that the second portion of the transistor





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conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

**Claim 2 (previously presented):** The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:

a first III-Nitride layer; and

a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein

the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

**Claim 3 (previously presented):** The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 4 (previously presented):** The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.



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**Claim 5 (previously presented):** The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

**Claim 6 (previously presented):** The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claim 7 (previously presented):** The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.

**Claim 8 (previously presented):** The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

**Claim 9 (previously presented):** The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.



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**Claim 10 (currently amended):** A merged cascode high electron mobility transistor circuit comprises:

an input voltage signal source;

a constant voltage source having a predetermined constant voltage;

a merged cascode transistor comprising:

a first epitaxial layer of III-Nitride material;

a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

a source electrode electrically connected to the first epitaxial layer;

a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;

a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;

wherein the first gate is connected to ~~an input voltage signal~~ the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to ~~a predetermined constant voltage~~ the constant voltage source such that the second portion of the transistor conducts until a



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voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

**Claim 11 (original):** The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

**Claim 12 (previously presented):** The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGaN material and the second epitaxial layer comprises a GaN material.

**Claim 13 (original):** The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

**Claims 14 (previously presented):** The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.



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**Claim 15 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

**Claim 16 (previously presented):** The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.



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## REMARKS

Prior to the present response, claims 1-16 were pending in the present application, and remain in the present application after the present response. By this amendment, Applicants have amended claims 1 and 10. Reconsideration and allowance of pending claims 1-16 in view of the above amendments and following remarks are requested.

### A. Rejection of Claims 1-16 under 35 USC §102(b)

The Examiner has rejected claims 1-16 under 35 USC §102(b) as being anticipated by U.S. patent application publication number 2005/0189561 A1 to Kinzer et al. (hereinafter "Kinzer"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 10, is patentably distinguishable over Kinzer.

The present invention, as defined by amended independent claim 1, provides a circuit including an input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor, and a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, where the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage





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source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

In an embodiment of the invention shown in Figure 3 of the present application, high electron mobility transistor (HEMT) 30 includes first portion Q1 including gate 32, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source contact 31 and drain contact 34. *See*, e.g., paragraph [0023] and Figure 3 of the present application. HEMT 30 also includes second portion Q2 including gate 33, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source contact 31 and drain contact 34. In HEMT 30, node 24 is between first portion Q1 and second portion Q2. *See*, e.g., Figure 3, Figure 2 and related text and [0023], lines 13-17 of the present application.

As disclosed in the present application, in an embodiment of the present invention, first portion Q1 is in enhancement mode transistor (normally OFF) and second portion Q2 is a depletion mode transistor (normally ON). *See*, e.g., paragraph [0023] and Figure 3 of the present application. Further disclosed in the present application, an input voltage signal is connected to gate 32 provide a gate voltage Vg1. *See*, e.g., [0016], lines 3-5 of the present application. Furthermore, a voltage is connected to gate 33 to provide a set voltage to Vg2, for example 0v. *See*, e.g., Figure 3, [0025] and [0017], lines 5-9 of the present application. When the input voltage at Vg1 goes low, the first portion Q1 turns



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OFF. As a result, the voltage at the node 24 rises until the gate-source voltage of second portion Q2 reaches a set pinch off voltage and the second portion Q2 turns OFF. *See*, e.g., [0018]. Thus, an embodiment of the present invention advantageously provides for a circuit where the drain swing of the first portion Q1 is substantially reduced. *See*, e.g., [0020].

In contrast to the present invention as defined by amended independent claim 1, Kinzer does not disclose a circuit including an input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor, and a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, where the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Kinzer specifically discloses device 40 in Figure 3 and device 50 in Figure 4. As disclosed in Kinzer, device 40 includes first gate electrode 32 and second gate electrode

34, which are situated between source/drain electrodes 25 and 26. *See*, e.g., paragraph [0032] and Figure 3 of Kinzer.

However, as disclosed in Kinzer, device 50 includes gate electrodes 32 and 34, which are situated between source/drain electrodes 25 and 26. *See*, e.g., Figure 4 and related text of Kinzer. In Kinzer both gate electrode 32 and gate electrode 34 are disposed within a recess 38 in second semiconductor body 21. *See*, e.g., paragraph [0038] and Figure 4 of Kinzer. Kinzer, teaches that in its device, each recess 38 causes an interruption in the 2DEG, which can be restored by applying a suitable voltage to gate electrodes 32 and 34. *See*, e.g., paragraphs [0038], [0030] of Kinzer. Furthermore, Kinzer teaches that device 50 is an enhancement mode device (i.e. a normally off device) specifically because of having the structural feature of two recess 38. Thus, what the Examiner appears to allege as a first portion of a merged cascode transistor cannot be a depletion mode transistor and what the Examiner appears to allege as a second portion of a merged cascode transistor also cannot be a depletion mode transistor regardless of voltages applied to respective gates. Thus, device 50 cannot be a merged cascode transistor, wherein a first portion of the merged cascode transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor, as specified in amended independent claim 1.

As disclosed in Kinzer, device 40 is a depletion mode device (i.e. normally ON), wherein an appropriate voltage applied to either gate electrode 32 or gate electrode 34 causes an interruption in the 2DEG, thereby turning device 40 off. *See*, e.g., paragraph

[0033] and Figure 3 of Kinzer. Kinzer teaches that device 50 is a depletion mode device specifically because it has no recess 38 to interrupt 2DEG. *See*, e.g., paragraphs [0038], [0030] of Kinzer. Thus, what the Examiner appears to allege as a first portion of a merged cascode transistor is cannot be a enhancement mode transistor and what the Examiner appears to allege as a second portion of a merged cascode transistor also cannot be an enhancement mode transistor regardless of voltages applied to respective gates. Thus, device 40 cannot be a merged cascode transistor, wherein a first portion of the merged cascode transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor, as specified in amended independent claim 1.

Thus, Kinzer fails to disclose a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, as specified in amended independent claim 1.

Thus, Kinzer discloses separate devices 40 and 50, where device 40 is a depletion mode device and device 50 is an enhancement mode device. However, amended independent claim 1 specifies a merged cascode transistor wherein a first portion of the merged cascode transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor. Thus, amended independent

claim 1 requires the merged cascode transistor include an enhancement mode transistor and a depletion mode transistor. Thus, Applicant submits that devices 40 and 50 disclosed in Kinzer are significantly different than the merged cascode transistor specified in amended independent claim 1. Furthermore, Kinzer does not describe a circuit in accordance with amended independent claim 1. As such, Applicant submits that Kinzer fails to make obvious the present invention as defined by amended independent claim 1.

In the outstanding Office Action, the Examiner asserts that the requirement that the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor is a purely functional distinction. *See*, e.g., page 4, and page 19, second paragraph of the outstanding Office Action. The Applicant respectfully disagrees and submits that whether a device includes an enhancement mode transistor or a depletion mode transistor is a structural distinction. For example, in the present application, first portion Q1 can be an enhancement mode transistor by using a recessed gate, fluorine implants, or other suitable means. *See*, e.g., paragraph [0023] and Figure 3 of the present application. By the Examiner's logic, device 40 and device 50 in Kinzer are identical, which, they clearly are not. Thus, whether a device includes an enhancement mode transistor or a depletion mode transistor is a tangible distinction and the devices in Kinzer would require significant and tangible modification in order to disclose an identical device.

For the foregoing reasons, Applicant respectfully submits that, at the time the invention defined by amended independent claim 1 was made, the invention would not

have been obvious to a person of ordinary skill in the art by Kinzer. Thus, amended independent claim 1 is patentably distinguishable over Kinzer and, as such, claims 2-9 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Kinzer for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Amended independent claim 10 includes similar limitations as amended independent claim 1. Thus, for similar reasons as discussed above, amended independent claim 10 is also patentably distinguishable over Kinzer and, as such, claims 11-16 depending from amended independent claim 10 are, *a fortiori*, also patentably distinguishable over Kinzer for at least the reasons presented above and also for additional limitations contained in each dependent claim.

**B. Rejection of Claims 10-16 under 35 USC §103(a)**

The Examiner has rejected claims 10-16 under 35 USC §103(a) as being unpatentable over Kinzer in view of U.S. Patent No. 7,052,942 to Smart et al. (hereinafter "Smart"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 10, is patentably distinguishable over Kinzer and Smart, either singly or in combination.

The present invention, as defined by amended independent claim 10, provides a circuit including input voltage signal source, a constant voltage source having a predetermined constant voltage, and a merged cascode transistor including a first epitaxial

layer of III-Nitride material, a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers, a source electrode electrically connected to the first epitaxial layer, a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode, a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor, and a second gate positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor, where the first gate is connected the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

Amended independent claim 10 defines substantially similar subject matter as amended independent claim 1, with a difference being that amended independent claim 10 specifies a first epitaxial layer of a III-Nitride material in contact with a second epitaxial layer of a III-Nitride material such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers.

Thus, for similar reasons as discussed above, Kinzer also fails to disclose a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Also, Kinzer fails to disclose a circuit in accordance with amended independent claim 10.

In the outstanding Final Rejection, the Examiner suggests combining Kinzer with Smart to overcome Kinzer's lack of explicitly disclosing the III-Nitride (AlGaN and GaN) layers being epitaxial. Specifically, in the outstanding Final Rejection, the Examiner asserts that "Kinzer et al disclose all of the structural limitations with the exception of not disclosing the III-Nitride (AlGaN and GaN) layers being epitaxial explicitly." *See* page 11 of the Final Rejection dated March 25, 2009. Smart specifically discloses HEMT 28 including GaN buffer layer 22 and AlGaN Schottky layer 24. *See*, e.g., Figure 2 and related text of Smart. However, in Smart, HEMT 28 includes only a single gate contact 32. *See*, e.g., Figure 2 and related text of Smart.

Thus, Smart fails to disclose a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the

transistor is a depletion mode transistor, as specified in amended independent claim 10. Thus, Smart fails to cure the aforementioned deficiencies of Kinzer. As such, Applicant submits that the combination of Kinzer and Smart suggested by the Examiner does not and cannot result in the present invention as defined by amended independent claim 10.

For the foregoing reasons, Applicant respectfully submits that, at the time the invention defined by amended independent claim 10 was made, the invention would not have been obvious to a person of ordinary skill in the art by Kinzer and Smart, either singly or in combination. Thus, amended independent claim 10 is patentably distinguishable over Kinzer and Smart and, as such, claims 11-16 depending from amended independent claim 10 are, *a fortiori*, also patentably distinguishable over Kinzer and Smart for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. **Conclusion**

For all the foregoing reasons pending claims 1-16 are patentably distinguishable over the cited art, and an early allowance of pending claims 1-16 is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Attorney Docket No.: 0400131

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 12/17/09

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IR-3234

PAGE 21/21 * RCVD AT 12/17/2009 8:01:38 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-5/28 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):04-48

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## FACSIMILE TRANSMISSION COVER SHEET

Date: December 17, 2009

To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826

Fax: (571) 273-8300

Re: **Application Serial No.: 11/688,338**
Filing Date: 3/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 21

Message:

Enclosed please find:

1) Request for Continued Examination
2) Amendment and Response to Final Office Action

Payment for Filing Fee for Request for Continued Examination and Third Month Extension Fee in the Amount of $1,920.00 is hereby enclosed on Form PTO-2038.

Thank you.

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/688,338 | 03/20/2007 | Thomas Herman | 0400131 | 9886 |

25700 7590 06/25/2009

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| EXAMINER | |
|---|---|
| AHMED, SELIM U | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/25/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 11/688,338 | HERMAN, THOMAS | |
| | Examiner | Art Unit | |
| | SELIM AHMED | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's arguments see page 1 of the remarks filed 06/05/2009, with respect to the finality of rejection(s) of claim(s) 10-16 have been fully considered and are persuasive. Therefore, the finality of the rejection has been withdrawn. However, applicant's arguments with respect to the rejection of claim(s) 1-16 under Kinzer or Kinzer in view Smart found to be not persuasive. Therefore, rejection sent on 03/25/2009 repeated under this office action.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kinzer ET al (2005/0189561; Kinzer hereinafter).

With regard to claim 1, Fig. 4 of Kinzer discloses a merged gate transistor comprising: a semiconductor element (element comprising of 21, 22, 23, and 24); a source electrode 25 electrically connected to a top

surface (top surface of 21 in Fig. 4) of the semiconductor element; a drain electrode 26 electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode 25; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and capacitively coupled to the semiconductor element (para[0035]) to form a first portion of the transistor (e.g. Fig. 4, portion of transistor 32); and a second gate 34 positioned adjacent to the first gate 32, and between the source electrode 25 and the drain electrode 26 to form a second portion of the transistor (e.g. Fig. 4, portion of transistor 34), wherein the second gate 34 is also capacitively coupled to the semiconductor element (para[0035]); wherein the first gate 32 is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate 34 is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level and wherein in the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

The applicant's claims **1, 6, 7** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed

device, because only the device per se is relevant, not the recited functions of using the first portion of the transistor for conducting while using the input voltage signal for providing an input voltage above a predetermined threshold voltage that is a pinch off voltage of the second portion of the transistor and running the first portion of the transistor and the second portion of the transistor in enhancement and depletion mode, respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily

or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer**'s devices 32, 34 are capable of performing in enhancement mode or depletion mode respectively (refer to claims 9 &10 and para[0026, 0033, 0038]), because a comparison of Applicant's specification to **Kinzer**'s disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode as indicated in the claims 9, 10, and para[0026, 0033, 0038]). Because it is reasonable to assume that **Kinzer**'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

Furthermore, Kinzer discloses all of the limitation of claim 1 with the exception of "a merged cascode transistor" as recited in the preamble. As disclosed in the MPEP 2111.02, preamble statement reciting purpose or intended use not given significant patentable weight if there is no structural difference between the claimed invention and prior art. Kinzer discloses a bi-directional switch that is structurally identical claimed by applicant. The exception is that the merged cascode transistor. However, this feature is a purpose/intended use of the Applicant's device and does not structurally limit feature of the claim. The structure of the claim device