

is the same as that of the prior art. Therefore, the claimed invention does not distinguish over the Kinzer's device. Note that a recitation of the purpose/intended use such as "merged gate cascode transistor" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the purpose/intended use, it meets the claim.

With regard to claim 2, Fig. 4 of Kinzer et al discloses the merged gate transistor of claim 1, wherein the semiconductor element further comprises: a first III-Nitride layer 21; and a second III-Nitride layer 23 on which the first III-Nitride layer is positioned such that a 2DEG conduction layer 22 forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer (e.g. para [00320]).

With regard to claim 3, figure 4 of Kinzer et al discloses the merged gate transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 4, Fig. 4 and elements 21, 23 of Kinzer et al disclose the merged gate transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material, and the second III-Nitride layer comprises GaN material.

With regard to claim 5, figure 4 and claim 3 of Kinzer et al disclose the merged gate transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 8, para [0025] of Kinzer et al disclose the merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 9, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

With regard to claim 10, Fig.4 of Kinzer et al discloses a merged cascade high electron mobility transistor comprises: a first epitaxial layer 21 of III-Nitride material; a second epitaxial layer 23 of a III-Nitride material, in contact with the first epitaxial layer 21 such that a 2-

dimensional electron gas conducting layer 22 is formed between the first 21 and second 23 epitaxial layers; a source electrode 25 electrically connected to the first epitaxial layer 21; a drain electrode 26 electrically connected to the first epitaxial layer 21 and spaced laterally from the source electrode; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and coupled to the first epitaxial layer to form a first portion (e.g. Fig. 4, portion of transistor 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode 26 and source electrode 25 and coupled to the first epitaxial layer 21 to form a second portion (e.g. Fig. 4, portion of transistor 34) of the transistor; wherein the first gate 32 is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate 34 is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level and wherein the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, Kinzer discloses all of the structural limitations of claims 10-16 with the exception of not explicitly disclosing that the III-

Art Unit: 2826

Nitride (AlGa_N and Ga_N) layers are formed by an epitaxial process.

Applicant's claims, however, do not distinguish over the Kinzer reference by virtue of the process used to form the III-Nitride layers, since only the final product is relevant, not the process of forming the III-Nitride material epitaxially. Note that a "product by process claim" is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Furthermore, Kinzer discloses all of the limitation of claim 10 with the exception of "merged cascode high electron mobility transistor" as recited in the preamble. As disclosed in the MPEP 2111.02, preamble statement reciting purpose or intended use not given significant patentable weight if there is no structural difference between the claimed invention and prior art. Kinzer discloses a bi-directional switch that is structurally

identical claimed by applicant. The exception is that the merged cascode high electron mobility transistor. However, this feature is a purpose/intended use of the Applicant's device and does not structurally limit feature of the claim. The structure of the claim device is the same as that of the prior art. Therefore, the claimed invention does not distinguish over the Kinzer's device. Note that a recitation of the purpose/intended use such as "merged cascode high electron mobility transistor" of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the purpose/intended use, it meets the claim.

Furthermore, applicant's claims 10, 13, 14 do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte Smith*, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer's** devices 32, 34 are capable of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a

voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively, because a comparison of Applicant's specification to **Kinzer's** disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively. Because it is reasonable to assume that **Kinzer's** device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 11, figure 4 and claim 3 of Kinzer et al disclose the merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

With regard to claim 15, para [0025] of Kinzer et al disclose the merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 16, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer in view of Smart et al (US 7,052,942; Smart hereinafter).

With regard to claims 10, 12, 13, 14, e.g. Fig.4 of Kinzer et al discloses a merged cascode high electron mobility transistor comprises: a first layer 21 of III-Nitride material; a second layer 23 of a III-Nitride material, in contact with the first layer 21 such that a 2-dimensional electron gas conducting layer 22 is formed between the first 21 and second 23 layers; a source electrode 25 electrically connected to the first layer 21; a drain

electrode 26 electrically connected to the first layer 21 and spaced laterally from the source electrode; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and coupled to the first layer to form a first portion (e.g. Fig. 4, portion of transistor 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode 26 and source electrode 25 and coupled to the first layer 21 to form a second portion (e.g. Fig. 4, portion of transistor 34) of the transistor; wherein the first gate 32 is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate 34 is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level and wherein the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, the difference between the device disclosed by Kinzer et al and that claimed lies in the recital of “epitaxial” layer, i.e. layers formed by epitaxy. Smart discloses forming an AlGa_N layer by epitaxy over a Ga_N layer, also formed by epitaxy. Smart’s epitaxially formed AlGa_N and Ga_N layers create a 2DEG layer between them that

creates the thin, high mobility channel needed for proper performance of the device disclosed by Kinzer. It therefore seems clear that one of ordinary skill in the art could have applied Smart's known "improvement" technique to Kinzer's "base" device in the same way Smart applies it to a "comparable" device and that in the view of one of skill in the art, the results would have predictably produced the 2DEG layer required by Kinzer's device. See MPEP § 2143, part "C".

With regard to claims 10 and 12, as discussed above, Kinzer et al disclose all of the structural limitations with the exception of not disclosing the III-Nitride (AlGaN and GaN) layers being epitaxial explicitly. However, e.g. Fig.2, elements 24, 22 of Smart discloses the AlGaN and GaN layers. It would have been obvious to one having ordinary skill in the art at the time of the invention to substitute Smart's epitaxial III-Nitride (AlGaN and GaN) layers with Kinzer's III—Nitride (AlGaN and GaN) layers for predictable results such as, low leakage characteristics of the HEMT device.

Furthermore, applicant's claims **10, 13, 14** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the first gate is connected to an input voltage signal

such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level. In another words, first portion or transistor 32 and second portion or transistor 34 are functioning as an enhancement and depletion mode respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte Smith*, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily

or inherently possess the characteristics of his claimed product”). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer**'s devices 32, 34 are capable of performing as an enhancement mode and depletion mode respectively (refer to claims 9 & 10 and para [0026, 0033, 0038]), because a comparison of Applicant's specification to **Kinzer**'s disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode. Because it is reasonable to assume that **Kinzer**'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 11, figure 4 of Kinzer et al discloses the merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first layer.

With regard to claim 15, para [0025] of Kinzer et al disclose the merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 16, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

Response to Arguments

4. Applicant's arguments filed on 6/05/2009 have been fully considered but they are not persuasive.

On page 1 of the remark, applicant argued, "As such, a good and sufficient reason exists, as contemplated by 37 CFR §1.116(c), for withdrawing the finality of the present rejection". However, examiner reviews of 37 CFR §1.116(c) found that 1.116(c) does not indicate anything about withdrawing the finality of the rejection. Therefore, applicant's quotation of 37 CFR §1.116(c) regarding withdrawal of finality of rejection appears to be inaccurate.

On page 4 of the remark, applicant argued, "As disclosed in Kinzer, device 50 includes gate electrodes 32 and 34, which are situated between source/drain electrodes 25 and 26. See, e.g., Figure 4 and related text of Kinzer. In Kinzer both gate electrode 32 and gate electrode 34 are disposed within a recess 38 in second semiconductor body 21. See, e.g., paragraph [0038] and Figure 4 of Kinzer. In Kinzer, each recess 38 causes an interruption in the 2 DEG, which can be restored by applying a suitable voltage to gate electrodes 32 and 34. See, e.g., paragraph [0038]

Art Unit: 2826

of Kinzer. Thus, as disclosed in Kinzer, device 50 is an enhancement mode device (i.e. a normally off device). Thus, device 50 is not a merged cascode transistor, wherein a first portion of the merged cascode transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor, as specified in independent claim 1".

In response to applicant's above argument that device being not a merged cascade (or HEMT) transistor, as indicated in the rejection, a recitation of the purpose/intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH**

Art Unit: 2826

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information With regard to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Art Unit: 2826

Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SA

/Sue A. Purvis/

Supervisory Patent Examiner, Art Unit 2826

Notice of References Cited	Application/Control No. 11/688,338		Applicant(s)/Patent Under Reexamination HERMAN, THOMAS	
	Examiner SELIM AHMED		Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0189561 A1	09-2005	Kinzer et al.	257/192
*	B	US-7,052,942 B1	05-2006	Smart et al.	438/162
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 11688338	Applicant(s)/Patent Under Reexamination HERMAN, THOMAS
	Examiner SELIM AHMED	Art Unit 2826

SEARCHED			
Class	Subclass	Date	Examiner
257	192, 194, 195, E29.14, E29.144, E29.246, E29.249	5/22/08	SA
	Updated search	12/8/08	/sa/
	Updated search	3/20/2009	/sa/
	Updated search	6/20/2009	/sa/

SEARCH NOTES		
Search Notes	Date	Examiner
Text search such as two dimensional electron gas, Cascode transistor, HEMT/High electron mobility transistor, source, drain, gate and their boolean combinations were searched.	5/22/08	SA
Updated search	12/8/2008	/sa/
Updated search	3/20/2009	/sa/

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	192, 194, 195,	5/22/08	SA

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/15 18:55
S2	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/16 11:22
S3	4541	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:21
S4	7876	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22
S5	314831	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22
S6	73	S3 and S4 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22
S7	96	S3 and S4 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:23
S8	63	S6 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:23

S9	82	S7 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:24
S10	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 17:33
S11	9	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 17:34
S12	1404	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:53
S13	1116	S5 and S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:54
S14	356	S5 and S12 and S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:54
S15	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:00
S16	5	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:01
S17	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:05

S18	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/21 18:20
S19	16	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:25
S20	1635	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:28
S21	1200	S5 and S20	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:29
S22	773	S5 and S20 and S4	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:29
S23	706	S22 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:30
S24	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:45
S25	275	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:46
S26	232	S25 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:46
S27	232	S25 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:46

S28	121	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 10:38
S29	310043	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 15:10
S30	556	S29 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 15:11
S31	852	S29 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 15:11
S32	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S33	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S34	4811	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S35	8419	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S36	332843	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49

S37	80	S34 and S35 and S36	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S38	107	S34 and S35 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S39	65	S37 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S40	85	S38 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S41	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S42	10	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S43	1425	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S44	1137	S36 and S43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S45	365	S36 and S43 and S35	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49

S46	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S47	6	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S48	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S49	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49
S50	18	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S51	1782	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S52	1310	S36 and S51	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S53	847	S36 and S51 and S35	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49

S54	725	S53 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S55	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S56	312	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S57	244	S56 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S58	244	S56 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S59	125	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49
S60	321547	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49
S61	596	S60 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49
S62	915	S60 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49
S63	4932	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03

S64	8697	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03
S65	341649	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03
S66	82	S63 and S64 and S65	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03
S67	66	S66 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03
S68	1	S67 and epi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03
S69	8	S67 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:05
S70	327776	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:13
S71	944	S70 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:13
S72	549	S71 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:13

S73	213	S72 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:14
S74	15	S73 and ((AlN and GaN) with (epi epitaxial))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:15
S75	2	"7052942".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:27
S76	2	"10689980"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:27
S77	19	("20020031851" "20020048302" "20040070003" "5698870" "5834326" "5843590" "5874747" "6110757" "6384433" "6387733" "6448793" "6455877" "6560452" "6633073" "6706576" "6750482" "6802902" "6815722").PN. OR ("7052942").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/19 18:31
S78	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S79	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S80	4932	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20

S81	8697	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S82	341649	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S83	82	S80 and S81 and S82	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S84	109	S80 and S81 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S85	66	S83 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S86	86	S84 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S87	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S88	10	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S89	1438	257/192.ccls. and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20

S90	1150	S82 and S89	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S91	373	S82 and S89 and S81	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S92	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S93	6	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S94	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S95	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S96	19	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20

S97	1868	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S98	1378	S82 and S97	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S99	896	S82 and S97 and S81	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S100	737	S99 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S101	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S102	334	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S103	246	S102 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S104	246	S102 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S105	130	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S106	327776	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S107	622	S106 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20

S108	944	S106 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S109	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S110	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S111	4932	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S112	8697	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S113	341649	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S114	82	S111 and S112 and S113	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S115	109	S111 and S112 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S116	66	S114 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20

S117	86	S115 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S118	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S119	10	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S120	1438	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S121	1150	S113 and S120	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S122	373	S113 and S120 and S112	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S123	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S124	6	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S125	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20

S126	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S127	19	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S128	1868	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S129	1378	S113 and S128	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S130	896	S113 and S128 and S112	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S131	737	S130 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S132	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S133	334	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S134	246	S133 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S135	246	S133 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20

S136	130	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S137	327776	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S138	622	S137 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S139	944	S137 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S140	4932	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S141	8697	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S142	341649	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S143	82	S140 and S141 and S142	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S144	66	S143 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20

S145	1	S144 and epi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S146	8	S144 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S147	327776	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S148	944	S147 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S149	549	S148 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
S150	213	S149 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S151	15	S150 and ((AlN and GaN) with (epi epitaxial))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S152	2	"7052942".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
S153	2	"10689980"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20

S154	19	("20020031851" "20020048302" "20040070003" "5698870" "5834326" "5843590" "5874747" "6110757" "6384433" "6387733" "6448793" "6455877" "6560452" "6633073" "6706576" "6750482" "6802902" "6815722").PN. OR ("7052942").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S155	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S156	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S157	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S158	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S159	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S160	85	S157 and S158 and S159	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S161	116	S157 and S158 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52

S162	67	S160 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S163	89	S161 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S164	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S165	10	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S166	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S167	1162	S159 and S166	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S168	378	S159 and S166 and S158	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S169	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S170	6	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52

S171	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S172	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S173	19	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S174	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S175	1427	S159 and S174	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S176	930	S159 and S174 and S158	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S177	745	S176 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S178	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S179	349	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52

S180	248	S179 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S181	248	S179 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S182	130	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S183	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S184	641	S183 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S185	977	S183 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S186	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S187	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S188	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52

S189	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S190	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S191	85	S188 and S189 and S190	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S192	116	S188 and S189 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S193	67	S191 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S194	89	S192 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S195	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S196	10	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S197	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52

S198	1162	S190 and S197	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S199	378	S190 and S197 and S189	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S200	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S201	6	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S202	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S203	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S204	19	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52

S205	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S206	1427	S190 and S205	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S207	930	S190 and S205 and S189	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S208	745	S207 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S209	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S210	349	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S211	248	S210 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S212	248	S210 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S213	130	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S214	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S215	641	S214 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52

S216	977	S214 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S217	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S218	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S219	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S220	85	S217 and S218 and S219	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S221	67	S220 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S222	1	S221 and epi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S223	8	S221 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S224	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52

S225	977	S224 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S226	567	S225 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S227	217	S226 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S228	18	S227 and ((AlN and GaN) with (epi epitaxial))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S229	2	"7052942".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S230	2	"10689980"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S231	19	("20020031851" "20020048302" "20040070003" "5698870" "5834326" "5843590" "5874747" "6110757" "6384433" "6387733" "6448793" "6455877" "6560452" "6633073" "6706576" "6750482" "6802902" "6815722").PN. OR ("7052942").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S232	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52

S233	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S234	5068	cascodes near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S235	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S236	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S237	85	S234 and S235 and S236	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S238	116	S234 and S235 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S239	67	S237 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S240	89	S238 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S241	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52

S242	10	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S243	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S244	1162	S236 and S243	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S245	378	S236 and S243 and S235	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S246	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S247	6	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S248	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52

S249	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S250	19	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S251	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S252	1427	S236 and S251	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S253	930	S236 and S251 and S235	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S254	745	S253 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S255	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S256	349	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S257	248	S256 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S258	248	S256 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52

S259	130	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S260	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S261	641	S260 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S262	977	S260 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S263	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S264	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S265	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S266	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S267	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52

S268	85	S265 and S266 and S267	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S269	116	S265 and S266 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S270	67	S268 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S271	89	S269 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S272	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S273	10	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S274	1450	257/192.ccls. and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S275	1162	S267 and S274	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S276	378	S267 and S274 and S266	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52

S277	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S278	6	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S279	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S280	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S281	19	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S282	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S283	1427	S267 and S282	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S284	930	S267 and S282 and S266	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52

S285	745	S284 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S286	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S287	349	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S288	248	S287 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S289	248	S287 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S290	130	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S291	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S292	641	S291 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S293	977	S291 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S294	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52

S295	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S296	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S297	85	S294 and S295 and S296	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S298	67	S297 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S299	1	S298 and epi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S300	8	S298 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52
S301	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S302	977	S301 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S303	567	S302 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/18 12:52

S304	217	S303 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S305	18	S304 and ((AlN and GaN) with (epi epitaxial))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S306	2	"7052942".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S307	2	"10689980"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/18 12:52
S308	19	("20020031851" "20020048302" "20040070003" "5698870" "5834326" "5843590" "5874747" "6110757" "6384433" "6387733" "6448793" "6455877" "6560452" "6633073" "6706576" "6750482" "6802902" "6815722").PN. OR ("7052942").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 12:52
S310	8	("5629539" "5691252" "5990507" "6174735" "6245631" "6278150" "6291292" "6337274"). PN. OR ("6707088").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/18 13:08
S314	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S315	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18

S316	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S317	85	S314 and S315 and S316	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S318	116	S314 and S315 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S323	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S324	1162	S316 and S323	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S331	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S332	1427	S316 and S331	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S333	930	S316 and S331 and S315	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S335	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S337	248	S336 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S340	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18

S342	977	S340 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S345	5068	cascocode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S346	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S347	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S348	85	S345 and S346 and S347	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S349	116	S345 and S346 and cascocode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S354	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S355	1162	S347 and S354	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S362	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S363	1427	S347 and S362	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18

S364	930	S347 and S362 and S346	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S366	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S368	248	S367 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S371	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S373	977	S371 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S374	5068	cascade near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S375	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S376	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S377	85	S374 and S375 and S376	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S378	67	S377 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18

S381	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S382	977	S381 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S383	567	S382 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S391	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S392	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S393	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S394	85	S391 and S392 and S393	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S395	116	S391 and S392 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S400	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18

S401	1162	S393 and S400	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S408	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S409	1427	S393 and S408	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S410	930	S393 and S408 and S392	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S412	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S414	248	S413 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S417	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S419	977	S417 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S422	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S423	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S424	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18

S425	85	S422 and S423 and S424	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S426	116	S422 and S423 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S431	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S432	1162	S424 and S431	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S439	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S440	1427	S424 and S439	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S441	930	S424 and S439 and S423	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S443	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S445	248	S444 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S448	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S450	977	S448 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18

S451	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S452	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S453	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S454	85	S451 and S452 and S453	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S455	67	S454 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S458	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S459	977	S458 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S460	567	S459 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S468	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18

S469	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S470	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S471	85	S468 and S469 and S470	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S472	116	S468 and S469 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S477	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S478	1162	S470 and S477	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S485	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S486	1427	S470 and S485	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S487	930	S470 and S485 and S469	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S489	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S491	248	S490 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18

S494	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S496	977	S494 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S499	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S500	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S501	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S502	85	S499 and S500 and S501	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S503	116	S499 and S500 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S508	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S509	1162	S501 and S508	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18

S516	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S517	1427	S501 and S516	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S518	930	S501 and S516 and S500	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S520	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:18
S522	248	S521 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S525	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S527	977	S525 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S528	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S529	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S530	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S531	85	S528 and S529 and S530	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18

S532	67	S531 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S535	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S536	977	S535 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:18
S537	567	S536 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S545	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S546	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:18
S549	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S550	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S551	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22

S552	85	S549 and S550 and S551	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S553	116	S549 and S550 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S558	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S559	1162	S551 and S558	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S566	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S567	1427	S551 and S566	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S568	930	S551 and S566 and S550	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S570	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S572	248	S571 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S575	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S577	977	S575 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22

S580	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S581	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S582	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S583	85	S580 and S581 and S582	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S584	116	S580 and S581 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S589	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S590	1162	S582 and S589	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S597	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S598	1427	S582 and S597	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S599	930	S582 and S597 and S581	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S601	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22

S603	248	S602 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S606	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S608	977	S606 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S609	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S610	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S611	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S612	85	S609 and S610 and S611	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S613	67	S612 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S616	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22

S617	977	S616 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S618	567	S617 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S626	5068	cascocode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S627	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S628	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S629	85	S626 and S627 and S628	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S630	116	S626 and S627 and cascocode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S635	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S636	1162	S628 and S635	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22

S643	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S644	1427	S628 and S643	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S645	930	S628 and S643 and S627	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S647	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S649	248	S648 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S652	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S654	977	S652 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S657	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S658	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S659	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S660	85	S657 and S658 and S659	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22

S661	116	S657 and S658 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S666	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S667	1162	S659 and S666	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S674	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S675	1427	S659 and S674	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S676	930	S659 and S674 and S658	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S678	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S680	248	S679 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S683	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S685	977	S683 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S686	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22

S687	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S688	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S689	85	S686 and S687 and S688	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S690	67	S689 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S693	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S694	977	S693 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S695	567	S694 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S703	5068	cascade near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S704	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22

S705	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S706	85	S703 and S704 and S705	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S707	116	S703 and S704 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S712	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S713	1162	S705 and S712	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S720	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S721	1427	S705 and S720	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S722	930	S705 and S720 and S704	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S724	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S726	248	S725 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S729	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22

S731	977	S729 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S734	5068	cascocode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S735	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S736	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S737	85	S734 and S735 and S736	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S738	116	S734 and S735 and cascocode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S743	1450	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S744	1162	S736 and S743	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S751	1932	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S752	1427	S736 and S751	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22

S753	930	S736 and S751 and S735	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S755	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/20 16:22
S757	248	S756 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S760	333788	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S762	977	S760 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S763	5068	cascocode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S764	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S765	349967	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S766	85	S763 and S764 and S765	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S767	67	S766 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22

S770	333788	"257"/(("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S771	977	S770 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/06/20 16:22
S772	567	S771 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S780	5068	cascode near3 transistor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22
S781	8964	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/20 16:22

6/ 20/ 2009 4:27:47 PM

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<i>Index of Claims</i> 	Application/Control No. 11688338	Applicant(s)/Patent Under Reexamination HERMAN, THOMAS
	Examiner SELIM AHMED	Art Unit 2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	05/22/2008	12/08/2008	03/20/2009	06/20/2009				
	1	✓	✓	✓	✓				
	2	✓	✓	✓	✓				
	3	✓	✓	✓	✓				
	4	✓	✓	✓	✓				
	5	✓	✓	✓	✓				
	6	✓	✓	✓	✓				
	7	✓	✓	✓	✓				
	8	✓	✓	✓	✓				
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	10	✓	✓	✓	✓				
	11	✓	✓	✓	✓				
	12	✓	✓	✓	✓				
	13	✓	✓	✓	✓				
	14	✓	✓	✓	✓				
	15	✓	✓	✓	✓				
	16	✓	✓	✓	✓				

Attorney Docket No.: 0400131

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Thomas Herman

Serial No.: 11/688,338

Filed: March 20, 2007

For: Merged Cascode Transistor

Art Unit: 2826

Examiner: Ahmed, Selim U.

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RESPONSE TO FINAL OFFICE ACTION

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P.O. Box 1450
Alexandria, VA 22313-1450

06/20/2009

Dear Sir/Madam:

This is in response to the Final Office Action dated March 25, 2009 in the above-referenced patent application. Please enter and consider the following remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Attorney Docket No.: 0400131

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Thomas Herman**

Serial No.: 11/688,338

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Dear Sir/Madam:

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Attorney Docket No. 003/017

**RECEIVED
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JUN 05 2009****In the Claims:**

Claim 1 (previously presented): A merged cascode transistor comprising:

- a semiconductor element;
- a source electrode electrically connected to a top surface of the semiconductor element;
- a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
- a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
- a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate is also coupled to the semiconductor element; wherein

the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

Claim 2 (previously presented): The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:

- a first III-Nitride layer; and
- a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

Claim 3 (previously presented): The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

Claim 4 (previously presented): The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

Claim 5 (previously presented): The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

Attorney Docket No.: 0400131

Claim 6 (previously presented): The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

Claim 7 (previously presented): The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.

Claim 8 (previously presented): The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

Claim 9 (previously presented): The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

Claim 10 (previously presented): A merged cascode high electron mobility transistor comprises:

- a first epitaxial layer of III-Nitride material;
- a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

Attorney Docket No.: 0400131

a source electrode electrically connected to the first epitaxial layer;

a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;

a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor; wherein

the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

Claim 11 (original): The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

Attorney Docket No.: 0400131

Claim 12 (previously presented): The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGaN material and the second epitaxial layer comprises a GaN material.

Claim 13 (original): The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

Claims 14 (previously presented): The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

Claim 15 (previously presented): The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

Claim 16 (previously presented): The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.

Attorney Docket No.: 0400131

REMARKS

Prior to the present response, claims 1-16 were pending in the present application, and remain in the present application after the present response. Reconsideration and allowance of pending claims 1-16 in view of the following remarks are requested.

At the outset, it is noted that in the Office Action dated March 25, 2009, the Examiner has *finally rejected* claims 1-16 pending in the application on the basis of new ground(s) of rejection and newly cited art. Applicant respectfully requests reconsideration and withdrawal of the finality of the rejection of the Office Action dated March 25, 2009.

A good and sufficient reason why the present response is necessary and was not earlier presented is that a new reference has been cited in the present final rejection dated March 25, 2009. The new reference is U.S. patent number 7,052,942 B1 to Smart et al. (hereinafter "Smart"). Since Smart is a new reference upon which the Examiner has now relied, Applicant believes that it would be manifestly unfair for the Patent Office not to withdraw the finality of the present rejection and not to consider Applicant's arguments which are necessitated due to the newly cited reference, Smart. As such, a good and sufficient reason exists, as contemplated by 37 CFR §1.116(c), for withdrawing the finality of the present rejection.

A. Rejection of Claims 1-16 under 35 USC §102(e)

The Examiner has rejected claims 1-16 under 35 USC §102(e) as being anticipated by U.S. patent application publication number 2005/0189561 A1 to Kinzer et al. (hereinafter "Kinzer"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1 and 10, is patentably distinguishable over Kinzer.

The present invention, as defined by independent claim 1, provides a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. In an embodiment of the invention shown in Figure 3 of the present application, high electron mobility transistor (HEMT) 30 includes first portion Q1 including gate 32, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source contact 31 and drain contact 34. *See, e.g.,* paragraph [0023] and Figure 3 of the present application. HEMT 30 also includes second portion Q2 including gate 33, which is situated over semiconductor element 29 and insulating layer 38 and also situated between source contact 31 and drain contact 34.

As disclosed in the present application, in one embodiment, the first portion Q1 is in enhancement mode such that a two-dimensional electron gas (2DEG) conducting layer

Attorney Docket No.: 0400131

is typically not present under gate 32 (G1) when $V_{g1}=0$, where the enhancement mode can be accomplished by using a recessed gate, fluorine implants, or other suitable means. *See, e.g.,* paragraph [0023] and Figure 3 of the present application. Thus, first portion Q1 is formed so as to be in the enhancement mode when $V_{g1}=0$. As disclosed in the present application, in one embodiment, the second portion Q2 is in depletion mode (i.e. normally ON) and voltage V_{g2} at gate 33 (G2) can be set at some non-zero value. *See, e.g.,* paragraph [0025] and Figure 3 of the present application.

Thus, in one embodiment of the invention, first portion Q1 and second portion Q2 of HEMT 30 are formed such that gate 32 and source and drain contacts 31, 34 form an enhancement mode transistor and gate 33 and source and drain contacts 31, 34 form a depletion mode transistor. Thus, in one embodiment, the invention advantageously provides a merged cascode HEMT that includes an enhancement mode transistor and a depletion mode transistor.

In contrast to the present invention as defined by independent claim 1, Kinzer does not disclose a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Kinzer specifically discloses device 40 in Figure 3 and device 50 in Figure 4. As disclosed in Kinzer, device 40 includes first gate electrode 32 and second gate

Attorney Docket No.: 0400131

electrode 34, which are situated between source/drain electrodes 25 and 26. *See, e.g.,* paragraph [0032] and Figure 3 of Kinzer.

However, as disclosed in Kinzer, device 40 is a depletion mode device (i.e. normally on), wherein an appropriate voltage applied to either gate electrode 32 or gate electrode 34 causes an interruption in the 2DEG, thereby turning device 40 off. *See, e.g.,* paragraph [0033] and Figure 3 of Kinzer. Thus, device 40 is not a merged cascode transistor, wherein a first portion of the merged cascode transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor, as specified in independent claim 1.

As disclosed in Kinzer, device 50 includes gate electrodes 32 and 34, which are situated between source/drain electrodes 25 and 26. *See, e.g.,* Figure 4 and related text of Kinzer. In Kinzer both gate electrode 32 and gate electrode 34 are disposed within a recess 38 in second semiconductor body 21. *See, e.g.,* paragraph [0038] and Figure 4 of Kinzer. In Kinzer, each recess 38 causes an interruption in the 2DEG, which can be restored by applying a suitable voltage to gate electrodes 32 and 34. *See, e.g.,* paragraph [0038] of Kinzer. Thus, as disclosed in Kinzer, device 50 is an enhancement mode device (i.e. a normally off device). Thus, device 50 is not a merged cascode transistor, wherein a first portion of the merged cascode transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor, as specified in independent claim 1.

Thus, Kinzer fails to disclose a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, as specified in independent claim 1.

In the outstanding Final Rejection, the Examiner asserts the Kinzer discloses “a merged gate transistor ... wherein in the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).” See pages 2 and 3 of the Final Rejection dated March 25, 2009. However, in the aforementioned quoted portion of the Final Rejection, the Examiner refers to paragraph [0033] of Kinzer to show that Kinzer discloses a depletion mode transistor and the Examiner refers to paragraphs [0026] and [0033] to show that Kinzer discloses an enhancement mode transistor. However, paragraph [0033] of Kinzer disclose device 40, which is a depletion mode device, and paragraphs [0026] and [0033] disclose device 50, which is an enhancement mode device.

Thus, Kinzer discloses separate devices 40 and 50, where device 40 is a depletion mode device and device 50 is an enhancement mode device. However, independent claim 1 specifies a merged cascode transistor wherein a first portion of the merged cascode transistor is an enhancement mode transistor and a second portion of the merged cascode transistor is a depletion mode transistor. Thus, independent claim 1 requires the merged

Attorney Docket No.: 0400131

cascode transistor include an enhancement mode transistor and a depletion mode transistor. Thus, Applicant submits that devices 40 and 50 disclosed in Kinzer are significantly different than the merged cascode transistor specified in independent claim 1. As such, Applicant submits that Kinzer fails to make obvious the present invention as defined by independent claim 1.

For the foregoing reasons, Applicant respectfully submits that, at the time the invention defined by independent claim 1 was made, the invention would not have been obvious to a person of ordinary skill in the art by Kinzer. Thus, independent claim 1 is patentably distinguishable over Kinzer and, as such, claims 2-9 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Kinzer for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Independent claim 10 includes similar limitations as independent claim 1. Thus, for similar reasons as discussed above, independent claim 10 is also patentably distinguishable over Kinzer and, as such, claims 11-16 depending from independent claim 10 are, *a fortiori*, also patentably distinguishable over Kinzer for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Rejection of Claims 10-16 under 35 USC §103(a)

The Examiner has rejected claims 10-16 under 35 USC §103(a) as being unpatentable over Kinzer in view of Smart. For the reasons discussed below, Applicant

respectfully submits that the present invention, as defined by independent claim 10, is patentably distinguishable over Kinzer and Smart, either singly or in combination.

The present invention, as defined by independent claim 10, provides a merged cascode HEMT including a first epitaxial layer of a III-Nitride material in contact with a second epitaxial layer of a III-Nitride material such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers, and a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Independent claim 10 defines substantially similar subject matter as independent claim 1, with a difference being that independent claim 10 specifies a first epitaxial layer of a III-Nitride material in contact with a second epitaxial layer of a III-Nitride material such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers.

Thus, for similar reasons as discussed above, Kinzer also fails to disclose a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

Attorney Docket No.: 0400131

In the outstanding Final Rejection, the Examiner suggests combining Kinzer with Smart to overcome Kinzer's lack of explicitly disclosing the III-Nitride (AlGaIn and GaN) layers being epitaxial. Specifically, in the outstanding Final Rejection, the Examiner asserts that "Kinzer et al disclose all of the structural limitations with the exception of not disclosing the III-Nitride (AlGaIn and GaN) layers being epitaxial explicitly." *See* page 11 of the Final Rejection dated March 25, 2009. Smart specifically discloses HEMT 28 including GaN buffer layer 22 and AlGaIn Schottky layer 24. *See*, e.g., Figure 2 and related text of Smart. However, in Smart, HEMT 28 includes only a single gate contact 32. *See*, e.g., Figure 2 and related text of Smart.

Thus, Smart fails to disclose a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, as specified in independent claim 10. Thus, Smart fails to cure the aforementioned deficiencies of Kinzer. As such, Applicant submits that the combination of Kinzer and Smart suggested by the Examiner does not and cannot result in the present invention as defined by independent claim 10.

For the foregoing reasons, Applicant respectfully submits that, at the time the invention defined by independent claim 10 was made, the invention would not have been obvious to a person of ordinary skill in the art by Kinzer and Smart, either singly or in

combination. Thus, independent claim 10 is patentably distinguishable over Kinzer and Smart and, as such, claims 11-16 depending from independent claim 10 are, *a fortiori*, also patentably distinguishable over Kinzer and Smart for at least the reasons presented above and also for additional limitations contained in each dependent claim.

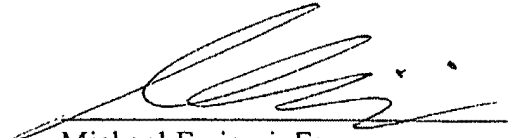
C. Conclusion

For all the foregoing reasons pending claims 1-16 are patentably distinguishable over the cited art, and an early allowance of pending claims 1-16 is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Attorney Docket No.: 0400131

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 6/5/09

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Reg. No. 38,135

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FACSIMILE TRANSMISSION COVER SHEET

Date: June 5, 2009

To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826

Fax: (571) 273-8300

Re: **Application Serial No.: 11/688,338**
Filing Date: 3/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 17

Message:

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/688,338		Filing Date 03/20/2007		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=	OR	X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT	06/05/2009	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
Total (37 CFR 1.16(i))	* 16	Minus	** 20	= 0	X \$	=	OR	X \$52=	0	
Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$	=	OR	X \$220=	0	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	OR	X \$	=	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	OR	X \$	=	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

Legal Instrument Examiner:
/ANNETTE SMITH/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/688,338	03/20/2007	Thomas Herman	0400131	9886
25700 7590 03/25/2009 FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691			EXAMINER AHMED, SELIM U	
			ART UNIT 2826	PAPER NUMBER
			MAIL DATE 03/25/2009	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/688,338	Applicant(s) HERMAN, THOMAS	
	Examiner SELIM AHMED	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 March 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

1. Applicant's arguments, see pages 14-15 of the remarks filed 2/27/2009, with respect to the rejection(s) of claim(s) 10-16 under §103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Smart et al 7,052,942.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kinzer ET al (2005/0189561; Kinzer hereinafter).

Fig. 4 of Kinzer discloses a merged gate transistor comprising: a semiconductor element (element comprising of 21, 22, 23, and 24); a source electrode 25 electrically connected to a top surface (top surface of 21 in Fig. 4) of the semiconductor element; a drain electrode 26 electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode 25; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and capacitively coupled to the semiconductor element (para[0035]) to form a first portion of the transistor (e.g. Fig. 4, portion of transistor

32); and a second gate 34 positioned adjacent to the first gate 32, and between the source electrode 25 and the drain electrode 26 to form a second portion of the transistor (e.g. Fig. 4, portion of transistor 34), wherein the second gate 34 is also capacitively coupled to the semiconductor element (para[0035]); wherein the first gate 32 is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate 34 is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level and wherein in the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

The applicant's claims **1, 6, 7** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of using the first portion of the transistor for conducting while using the input voltage signal for providing an input voltage above a predetermined threshold voltage that is a pinch off voltage of the second portion of the transistor and running the first portion of the transistor and the second portion of the transistor in enhancement and depletion mode, respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir.

Art Unit: 2826

1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte Smith*, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer's** devices 32, 34 are capable of performing in enhancement mode or depletion mode respectively (refer to claims 9 & 10 and para[0026, 0033, 0038]), because a comparison of Applicant's specification to **Kinzer's** disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode as indicated in the claims 9, 10, and para[0026, 0033, 0038]). Because it is reasonable to assume that **Kinzer's** device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 2, Fig. 4 of Kinzer et al discloses the merged gate transistor of claim 1, wherein the semiconductor element further comprises: a first III-Nitride layer 21; and a second III-Nitride layer 23 on which the first III-Nitride layer is positioned such that a 2DEG conduction layer 22 forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer (e.g. para [00320]).

With regard to claim 3, figure 4 of Kinzer et al discloses the merged gate transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 4, Fig. 4 and elements 21, 23 of Kinzer et al disclose the merged gate transistor of claim 3, wherein the first III-Nitride layer comprises AlGaIn material, and the second III-Nitride layer comprises GaN material.

With regard to claim 5, figure 4 and claim 3 of Kinzer et al disclose the merged gate transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 8, para [0025] of Kinzer et al disclose the merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 9, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

3. Claims 10-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Kinzer ET al (2005/0189561; Kinzer hereinafter).

Fig.4 of Kinzer et al discloses a merged cascode high electron mobility transistor comprises: a first epitaxial layer 21 of III-Nitride material; a second epitaxial layer 23 of a III-Nitride material, in contact with the first epitaxial layer 21 such that a 2-dimensional electron gas conducting layer 22 is formed between the first 21 and second 23 epitaxial layers; a source electrode 25 electrically connected to the first epitaxial layer 21; a drain electrode 26 electrically connected to the first epitaxial layer 21 and spaced laterally from the source electrode; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and coupled to the first epitaxial layer to form a first portion (e.g. Fig. 4, portion of transistor 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode 26 and source electrode 25 and coupled to the first epitaxial layer 21 to form a second portion (e.g. Fig. 4, portion of transistor 34) of the transistor; wherein the first gate 32 is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate 34 is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level and wherein the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

As discussed above, Kinzer discloses all of the structural limitations of claims 10-16 with the exception of not explicitly disclosing that the III-Nitride (AlGaN and GaN) layers are formed by an epitaxial process. Applicant's claims, however, do not distinguish over the Kinzer reference by virtue of the process used to form the III-Nitride layers, since only the final product is relevant, not the process of forming the III-Nitride material epitaxially. Note that a "product by process claim" is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Furthermore, applicant's claims 10, 13, 14 do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant

Art Unit: 2826

voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte Smith*, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer's** devices 32, 34 are capable of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second

portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively, because a comparison of Applicant's specification to **Kinzer's** disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of basing the conduction of the first portion on a value of the input voltage signal, connecting second gate to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and running the first portion or transistor and the second portion or transistor in enhancement and depletion mode respectively. Because it is reasonable to assume that **Kinzer's** device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 11, figure 4 and claim 3 of Kinzer et al disclose the merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

With regard to claim 15, para [0025] of Kinzer et al disclose the merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 16, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

Claim Rejections - 35 USC § 103

Art Unit: 2826

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer in view of Smart et al (US 7,052,942; Smart hereinafter).

With regard to claims 10, 12, 13, 14, e.g. Fig.4 of Kinzer et al discloses a merged cascode high electron mobility transistor comprises: a first layer 21 of III-Nitride material; a second layer 23 of a III-Nitride material, in contact with the first layer 21 such that a 2-dimensional electron gas conducting layer 22 is formed between the first 21 and second 23 layers; a source electrode 25 electrically connected to the first layer 21; a drain electrode 26 electrically connected to the first layer 21 and spaced laterally from the source electrode; a first gate 32 positioned between the source electrode 25 and the drain electrode 26 and coupled to the first layer to form a first portion (e.g. Fig. 4, portion of transistor 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode 26 and source electrode 25 and coupled to the first layer 21 to form a second portion (e.g. Fig. 4, portion of transistor 34) of the transistor; wherein the first gate 32 is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate 34 is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the

Art Unit: 2826

source electrode reaches a predetermined level and wherein the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

With regard to claims 10 and 12, as discussed above, Kinzer et al disclose all of the structural limitations with the exception of not disclosing the III-Nitride (AlGa_N and Ga_N) layers being epitaxial explicitly. However, e.g. Fig.2, elements 24, 22 of Smart discloses the AlGa_N and Ga_N layers. It would have been obvious to one having ordinary skill in the art at the time of the invention to substitute Smart's epitaxial III-Nitride (AlGa_N and Ga_N) layers with Kinzer's III—Nitride (AlGa_N and Ga_N) layers for predictable results such as, low leakage characteristics of the HEMT device.

Furthermore, applicant's claims **10, 13, 14** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level. In another words, first portion or transistor 32 and second portion or transistor 34 are functioning as an enhancement and depletion mode respectively. Note that functional language in a

Art Unit: 2826

device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte Smith*, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer's** devices 32, 34 are capable of performing as an enhancement mode and depletion mode respectively (refer to claims 9 & 10 and para [0026, 0033, 0038]), because a comparison of Applicant's specification to **Kinzer's** disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode. Because

it is reasonable to assume that **Kinzer's** device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 11, figure 4 of Kinzer et al discloses the merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first layer.

With regard to claim 15, para [0025] of Kinzer et al disclose the merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 16, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

The difference between the device disclosed by Kinzer et al and that claimed lies in the recital of "epitaxial" layer, i.e. layers formed by epitaxy. Smart discloses forming an AlGa_N layer by epitaxy over a Ga_N layer, also formed by epitaxy. Smart's epitaxially formed AlGa_N and Ga_N layers create a 2DEG layer between them that creates the thin, high mobility channel needed for proper performance of the device disclosed by Kinzer. It therefore seems clear that one of ordinary skill in the art could have applied Smart's known "improvement" technique to Kinzer's "base" device in the same way Smart applies it to a "comparable" device and that in the view of one of skill in the art, the results would have predictably produced the 2DEG layer required by Kinzer's device. See MPEP § 2143, part "C".

Conclusion

5. Applicant's amendment (filed 09/02/2008) necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE**

FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information With regard to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>.

Art Unit: 2826

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SA/

**/Thomas L Dickey/
Primary Examiner, Art Unit 2826**

Notice of References Cited	Application/Control No. 11/688,338		Applicant(s)/Patent Under Reexamination HERMAN, THOMAS	
	Examiner SELIM AHMED		Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0189561 A1	09-2005	Kinzer et al.	257/192
*	B	US-7,052,942 B1	05-2006	Smart et al.	438/162
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 11688338	Applicant(s)/Patent Under Reexamination HERMAN, THOMAS
	Examiner SELIM AHMED	Art Unit 2826

SEARCHED			
Class	Subclass	Date	Examiner
257	192, 194, 195, E29.14, E29.144, E29.246, E29.249	5/22/08	SA
	Updated search	12/8/08	/sa/
	Updated search	3/20/2009	/sa/

SEARCH NOTES		
Search Notes	Date	Examiner
Text search such as two dimensional electron gas, Cascode transistor, HEMT/High electron mobility transistor, source, drain, gate and their boolean combinations were searched.	5/22/08	SA
Updated search	12/8/2008	/sa/
Updated search	3/20/2009	/sa/

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	192, 194, 195,	5/22/08	SA

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<i>Index of Claims</i> 	Application/Control No. 11688338	Applicant(s)/Patent Under Reexamination HERMAN, THOMAS
	Examiner SELIM AHMED	Art Unit 2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	05/22/2008	12/08/2008	03/20/2009						
	1	✓	✓	✓						
	2	✓	✓	✓						
	3	✓	✓	✓						
	4	✓	✓	✓						
	5	✓	✓	✓						
	6	✓	✓	✓						
	7	✓	✓	✓						
	8	✓	✓	✓						
	9	✓	✓	✓						
	10	✓	✓	✓						
	11	✓	✓	✓						
	12	✓	✓	✓						
	13	✓	✓	✓						
	14	✓	✓	✓						
	15	✓	✓	✓						
	16	✓	✓	✓						

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L2	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L3	4932	cascode near3 transistor \$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L4	8697	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L5	341649	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L6	82	L3 and L4 and L5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L7	109	L3 and L4 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L8	66	L6 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20

L9	86	L7 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L10	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L11	10	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L12	1438	257/192.ccls. and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L13	1150	L5 and L12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L14	373	L5 and L12 and L4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L15	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L16	6	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20

L17	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L18	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L19	19	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L20	1868	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L21	1378	L5 and L20	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L22	896	L5 and L20 and L4	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L23	737	L22 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L24	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L25	334	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20

L26	246	L25 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L27	246	L25 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L28	130	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L29	327776	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L30	622	L29 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L31	944	L29 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L32	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L33	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20

L34	4932	cascocode near3 transistor \$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L35	8697	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L36	341649	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L37	82	L34 and L35 and L36	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L38	109	L34 and L35 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L39	66	L37 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L40	86	L38 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L41	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L42	10	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20

L43	1438	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L44	1150	L36 and L43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L45	373	L36 and L43 and L35	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L46	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L47	6	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L48	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L49	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20

		"6710379" "6830945"). PN.				
L50	19	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L51	1868	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L52	1378	L36 and L51	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L53	896	L36 and L51 and L35	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L54	737	L53 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L55	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L56	334	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
L57	246	L56 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L58	246	L56 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L59	130	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L60	327776	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20

L61	622	L60 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L62	944	L60 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L63	4932	cascade near3 transistor \$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L64	8697	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L65	341649	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L66	82	L63 and L64 and L65	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L67	66	L66 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L68	1	L67 and epi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20

L69	8	L67 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L70	327776	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L71	944	L70 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L72	549	L71 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/20 00:20
L73	213	L72 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L74	15	L73 and ((AlN and GaN) with (epi epitaxial))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L75	2	"7052942".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20
L76	2	"10689980"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/20 00:20

L77	19	("20020031851" "20020048302" "20040070003" "5698870" "5834326" "5843590" "5874747" "6110757" "6384433" "6387733" "6448793" "6455877" "6560452" "6633073" "6706576" "6750482" "6802902" "6815722").PN. OR ("7052942").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/20 00:20
S1	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/15 18:55
S2	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/16 11:22
S3	4541	cascode near3 transistor \$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:21
S4	7876	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22
S5	314831	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22
S6	73	S3 and S4 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22
S7	96	S3 and S4 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:23

S8	63	S6 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:23
S9	82	S7 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:24
S10	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 17:33
S11	9	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 17:34
S12	1404	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:53
S13	1116	S5 and S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:54
S14	356	S5 and S12 and S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:54
S15	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:00
S16	5	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:01

S17	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:05
S18	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/21 18:20
S19	16	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:25
S20	1635	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:28
S21	1200	S5 and S20	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:29
S22	773	S5 and S20 and S4	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:29
S23	706	S22 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:30
S24	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:45
S25	275	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:46

S26	232	S25 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:46
S27	232	S25 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:46
S28	121	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 10:38
S29	310043	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 15:10
S30	556	S29 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 15:11
S31	852	S29 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 15:11
S32	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S33	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49

S34	4811	cascocode near3 transistor \$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S35	8419	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S36	332843	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S37	80	S34 and S35 and S36	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S38	107	S34 and S35 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S39	65	S37 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S40	85	S38 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S41	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S42	10	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49

S43	1425	257/192.ccls. and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S44	1137	S36 and S43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S45	365	S36 and S43 and S35	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S46	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900"). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S47	6	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S48	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S49	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49

		"6710379" "6830945"). PN.				
S50	18	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732"). PN. OR ("6465814"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S51	1782	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S52	1310	S36 and S51	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S53	847	S36 and S51 and S35	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S54	725	S53 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S55	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S56	312	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/08 09:49
S57	244	S56 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S58	244	S56 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
S59	125	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49
S60	321547	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49

S61	596	S60 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49
S62	915	S60 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49
S63	4932	cascode near3 transistor \$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03
S64	8697	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03
S65	341649	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03
S66	82	S63 and S64 and S65	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03
S67	66	S66 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03
S68	1	S67 and epi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:03

S69	8	S67 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:05
S70	327776	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").cls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:13
S71	944	S70 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:13
S72	549	S71 and (epi or epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/19 18:13
S73	213	S72 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:14
S74	15	S73 and ((AlN and GaN) with (epi epitaxial))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:15
S75	2	"7052942".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:27
S76	2	"10689980"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/03/19 18:27

S77	19	("20020031851" "20020048302" "20040070003" "5698870" "5834326" "5843590" "5874747" "6110757" "6384433" "6387733" "6448793" "6455877" "6560452" "6633073" "6706576" "6750482" "6802902" "6815722").PN. OR ("7052942").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/03/19 18:31
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FACSIMILE TRANSMISSION COVER SHEET

Date: February 27, 2009

To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826

Fax: (571) 273-8300

Re: **Application Serial No.: 11/688,338**
Filing Date: 3/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 17

Message:

Enclosed please find the Amendment and Response to Final Office Action dated December 11, 2008.

Thank you.

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Attorney Docket No.: 0400131

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Thomas Herman**

Serial No.: 11/688,338

Filed: March 20, 2007

For: **Merged Cascode Transistor**

Art Unit: 2826

Examiner: Ahmed, Selim U.

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AMENDMENT AND RESPONSE TO FINAL OFFICE ACTION

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the Final Office Action dated December 11, 2008 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Attorney Docket No.: 0400131

In the Attorney Docket No.:

Please replace the old Attorney Docket No. "IR-3234 (2-6008) V3753" with new
Attorney Docket No. --0400131--.

Attorney Docket No.: 0400131

In the Claims:

Claim 1 (currently amended): A merged cascode transistor comprising:

a semiconductor element;

a supply source electrode electrically connected to a top surface of the semiconductor element;

a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the supply source electrode;

a first gate positioned between the supply source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the supply source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate is also coupled to the semiconductor element; wherein

the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

Attorney Docket No.: 0400131

Claim 2 (previously presented): The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:

- a first III-Nitride layer; and
- a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

Claim 3 (previously presented): The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

Claim 4 (previously presented): The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

Claim 5 (previously presented): The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

Attorney Docket No.: 0400131

Claim 6 (previously presented): The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

Claim 7 (previously presented): The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.

Claim 8 (previously presented): The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

Claim 9 (previously presented): The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

Claim 10 (currently amended): A merged cascode high electron mobility transistor comprises:

a first epitaxial layer of III-Nitride material;

a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

Attorney Docket No.: 0400131

a supply source electrode electrically connected to the first epitaxial layer;

a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the supply source electrode;

a first gate positioned between the supply source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the drain electrode and supply source electrode and coupled to the first epitaxial layer to form a second portion of the transistor; wherein

the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

Claim 11 (original): The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

Attorney Docket No.: 0400131

Claim 12 (previously presented): The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGa_N material and the second epitaxial layer comprises a Ga_N material.

Claim 13 (original): The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

Claims 14 (previously presented): The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

Claim 15 (previously presented): The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

Claim 16 (previously presented): The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.

Attorney Docket No.: 0400131

REMARKS

Prior to the present amendment, claims 1-16 were pending in the present application. By the present amendment and response, claims 1 and 10 have been amended to correct for an informality. Entry of the formality amendments is respectfully requested. Reconsideration and allowance of pending claims 1-16 in view of the above amendment and the following remarks are requested.

A. Rejection of Claims 1-9 under 35 USC §103(a)

The Examiner has rejected claims 1-9 under 35 USC §103(a) as being unpatentable over U.S. patent application publication number 2005/0189561 A1 to Kinzer et al. (hereinafter "Kinzer"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claim 1, is patentably distinguishable over Kinzer.

The present invention, as defined by independent claim 1, provides a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. In an embodiment of the invention shown in Figure 3 of the present application, high electron mobility transistor (HEMT) 30 includes first portion Q1, which includes gate 32, and second

Attorney Docket No.: 0400131

portion Q2, which includes gate 33, where gates 32 and 33 are situated over semiconductor element 29 and also situated between source contact 31 and drain contact 34. *See*, e.g., paragraph [0023] and Figure 3 of the present application.

As disclosed in the present application, in one embodiment, the first portion Q1 is in enhancement mode (i.e. normally OFF), where a two-dimensional electron gas (2DEG) conducting layer is typically not present under gate 32 (G1) when $V_{g1}=0$. *See*, e.g., paragraph [0023] and Figure 3 of the present application. In one embodiment, the second portion Q2 is in depletion mode (i.e. normally ON), where voltage V_{g2} at gate 33 (G2) can be set at some non-zero value. *See*, paragraph [0025] and Figure 3 of the present application. Thus, in an embodiment of the invention, gate 32, source contact 31 and drain contact 34 of HEMT 30 form an enhancement mode transistor and gate 33, source 31 and drain contact 34 of HEMT 30 form a depletion mode transistor.

In contrast to the present invention as defined by independent claim 1, Kinzer does not disclose a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to a semiconductor element to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Kinzer specifically discloses device 50 including gate electrodes 32 and 34 and source/drain electrodes 25 and 26, where gate electrodes 32 and 34 are disposed within a respective recess 38 in second semiconductor body 21, and where gate electrode

Attorney Docket No.: 0400131

32 is situated adjacent to source/drain electrode 32 and gate electrode 34 is situated adjacent to source/drain electrode 34. *See, e.g.,* paragraph [0038] and Figure 4 of Kinzer. In Kinzer, device 50 is an enhancement mode device (i.e. nominally off), where each recess 38 causes an interruption in the 2DEG, which can be restored upon application of a suitable voltage to gate electrodes 32, 34. *See, e.g.,* paragraph [0038] of Kinzer. Thus, in Kinzer, device 50 acts like a power logic AND gate, in which current flows to/from electrodes 25, 26 when both gate electrodes 32, 34 have a potential applied to them. *See, e.g.,* paragraph [0039] of Kinzer.

However, as shown in Figure 3 of Kinzer, gate electrode 32 is situated adjacent to source/drain electrode 25 and is spaced apart from gate electrode 34, which is situated adjacent to source/drain electrode 26. Thus, Kinzer fails to disclose a merged cascode transistor including a first gate and a second gate positioned between a source electrode and a drain electrode, where the second gate is positioned adjacent to the first gate, as specified by independent claim 1. Also, as discussed above, device 50 is an enhancement mode device (i.e. nominally off), where each recess 38 causes an interruption in the 2DEG, which can be restored upon application of a suitable voltage to gate electrodes 32, 34. Thus, in device 50, Kinzer fails to disclose a merged cascode transistor, wherein a first portion of the transistor is an enhancement mode transistor and a second portion of the transistor is a depletion mode transistor, as specified in independent claim 1.

Furthermore, as discussed above, each of gate electrodes 32 and 34 is disposed within a respective recess 38, which causes an interruption in the 2DEG. Thus, by

Attorney Docket No.: 0400131

forming each of gate electrodes 32 and 34 in a respective recess 38, Kinzer teaches away from a merged cascode transistor, wherein a first portion of the transistor is an enhancement mode transistor and a second portion of the transistor is a depletion mode transistor, as specified in independent claim 1.

Kinzer also discloses device 40 including first gate electrode 32 and second gate electrode 34, where device 40 is a depletion mode device (i.e. nominally on). *See*, e.g., paragraph [0032] and Figure 3 of Kinzer. In device 40 of Kinzer, the application of an appropriate voltage to either gate electrode 32, 34 causes an interruption in the 2DEG, whereby device 40 is turned off. *See*, e.g., paragraph [0033] of Kinzer. Thus, in device 40, Kinzer fails to disclose a merged cascode transistor, wherein a first portion of the transistor is an enhancement mode transistor and a second portion of the transistor is a depletion mode transistor, as specified in independent claim 1. Also, gates 32 and 34 in device 40 are spaced apart. Thus, in device 40, Kinzer fails to disclose a merged cascode transistor including a first gate and a second gate positioned between a source electrode and a drain electrode, where the second gate is positioned adjacent to the first gate, as specified by independent claim 1.

Thus, Applicant submits that devices 40 and 50 disclosed in Kinzer are significantly different than the merged cascode transistor specified in independent claim 1. As such, Applicant submits that Kinzer fails to make obvious the present invention as defined by independent claim 1.

Attorney Docket No.: 0400131

For the foregoing reasons, Applicant respectfully submits that, at the time the invention defined by independent claim 1 was made, the invention would not have been obvious to a person of ordinary skill in the art by Kinzer. Thus, independent claim 1 is patentably distinguishable over Kinzer and, as such, claims 2-9 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Kinzer for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Rejection of Claims 10-16 under 35 USC §103(a)

The Examiner has rejected claims 10-16 under 35 USC §103(a) as being unpatentable over Kinzer in view of U.S. patent application publication number 2006/0060871 A1 to Robert Beach (hereinafter "Beach"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claim 10, is patentably distinguishable over Kinzer and Beach, either singly or in combination.

The present invention, as defined by independent claim 10, provides a merged cascode high electron mobility transistor (HEMT) including a first epitaxial layer of a III-Nitride material in contact with a second epitaxial layer of a III-Nitride material such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers, and a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor

Attorney Docket No.: 0400131

and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor. Independent claim 10 defines substantially similar subject matter as independent claim 1, with a difference being that independent claim 10 specifies a first epitaxial layer of a III-Nitride material in contact with a second epitaxial layer of a III-Nitride material such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers.

Thus, for similar reasons as discussed above, Kinzer also fails to disclose a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

In the outstanding Final Rejection, the Examiner asserts "[w]ith regard to claims 10 and 12, as discussed above, Kinzer et al disclose all of the limitations with the exception of not disclosing the III-Nitride (AlGa_N and Ga_N) layers being epitaxial explicitly." See page 7 of the Final Rejection dated December 11, 2008. To overcome the lack of disclosing the III-Nitride (AlGa_N and Ga_N) layers being epitaxial explicitly, the Examiner suggests combining Kinzer with Beach. Beach discloses that planar devices have been fabricated with Ga_N and AlGa_N alloys through a number of

Attorney Docket No.: 0400131

techniques, including hydride vapor phase epitaxy (HVPE). *See*, e.g., paragraph [0011] of Beach.

However, Beach fails to disclose a merged cascode transistor including a first gate positioned between a source electrode and a drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor and a second gate positioned adjacent to the first gate to form a second portion of the transistor, where the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, as specified in independent claim 10. Thus, Beach fails to cure the aforementioned deficiencies of Kinzer. As such, Applicant submits that the combination of Kinzer and Beach suggested by the Examiner does not and cannot result in the present invention as defined by independent claim 10.

For the foregoing reasons, Applicant respectfully submits that, at the time the invention defined by independent claim 10 was made, the invention would not have been obvious to a person of ordinary skill in the art by Kinzer and Beach, either singly or in combination. Thus, independent claim 10 is patentably distinguishable over Kinzer and Beach and, as such, claims 11-16 depending from independent claim 10 are, *a fortiori*, also patentably distinguishable over Kinzer and Beach for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Moreover, the present application claims priority to US provisional application Serial No. 60/783,934, filed on March 20, 2006. Thus, Beach can qualify as "prior art" only under §102(e), since Beach was published on March 23, 2006 which is after the

Attorney Docket No.: 0400131

effective filing date of the present application, i.e. March 20, 2006. It is noted that the Beach reference and the present application are both assigned to a common assignee, i.e. International Rectifier Corporation. Therefore, Applicant asserts that Beach is disqualified as a §103(a) "prior art" and cannot be cited under §103(a) against the present application.

C. Conclusion

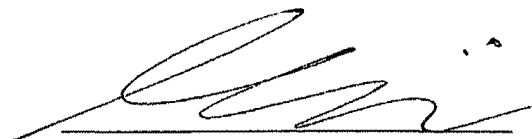
For all the foregoing reasons pending claims 1-16 are patentably distinguishable over the cited art, and an early allowance of pending claims 1-16 is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

***** IMPORTANT NOTE!! *****: PLEASE NOTE that Applicants' attorneys have changed. Please forward all correspondences in this application to Applicants' new attorneys of record using the contact information provided below. Thank you.

Attorney Docket No.: 0400131

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 2/27/09

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/688,338		Filing Date 03/20/2007		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=	OR	X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT	02/27/2009	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
Total (37 CFR 1.16(i))	* 16	Minus	** 20	= 0	X \$	=	OR	X \$52=	0	
Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$	=	OR	X \$220=	0	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	OR	X \$	=	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	OR	X \$	=	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

Legal Instrument Examiner:
/AMANDA FORD/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/688,338	03/20/2007	Thomas Herman	0400131

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

CONFIRMATION NO. 9886
POA ACCEPTANCE LETTER



Date Mailed: 02/18/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/06/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/llam/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/688,338	03/20/2007	Thomas Herman	IR-3234(2-6008) V3753

CONFIRMATION NO. 9886

POWER OF ATTORNEY NOTICE

2352
OSTROLENK FABER GERB & SOFFEN
1180 AVENUE OF THE AMERICAS
NEW YORK, NY 100368403



Date Mailed: 02/18/2009

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/06/2009.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/llam/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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Mission Viejo, California 92691
tel: (949) 282-1000
fax: (949) 282-1002

FACSIMILE TRANSMISSION COVER SHEET

Date: February 6, 2009
To: United States Patent and Trademark Office
Examiner: Ahmed, Selim U.; Art Unit: 2826
Fax: (571) 273-8300
Re: Application Serial No.: 11/688,338
Filing Date: 3/20/2007; First-Named Inventor: Herman
Attorney Docket No.: 0400131
From: Farjami & Farjami LLP

Number of pages including the cover sheet: 3

Message:

Enclosed please find a Revocation and Power of Attorney.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

Attorney Docket No.: 0400131

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Herman, Thomas

Serial No.: **11/688,338**

Filing Date: **3/20/2007**

For: **Merged Cascode Transistor**

Art Unit: 2826

Examiner: Ahmed, Selim U.

Customer Number 25700

REVOCATION AND POWER OF ATTORNEY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

Applicants of the above-identified patent application hereby revoke all previous powers of attorney given in this application and appoint attorneys associated with the:

Customer Number 25700

to represent the Applicants before the United States Patent and Trademark Office, with full power of substitution and revocation, to prosecute this application, to make alterations and amendments thereto, to receive communications from the Patent and Trademark Office and to transact all business in the Patent and Trademark Office connected therewith.

Attorney Docket No.: 0400131

Please change the correspondence address for this application and direct all communications to the address associated with:

Customer Number 25700

International Rectifier Corporation, a Delaware corporation, certifies that it is the assignee of the entire right, title, and interest in the patent application identified above by virtue of an assignment from the inventor(s) of the patent application identified above. The assignment was recorded at the Patent and Trademark Office at Reel 019249, Frame 0874. The undersigned, whose title is supplied below, is authorized to act on behalf of assignee (37 CFR §3.73(b)).

Signed this 5 day of February 2009

Pedram Sameni
(Signature)

On behalf of International Rectifier Corporation

Pedram Sameni
(Print Name)

Manager, Intellectual Property and Licensing
(Title)

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being filed by facsimile transmission to United States Patent and Trademark Office at facsimile number **571-273-8300** on the date stated below. The facsimile transmission report indicated that the facsimile transmission was successful.

Date of Facsimile: 2/6/09

Marci M. Sweda
Name of Person Performing Facsimile Transmission

[Signature] 2/6/09
Signature Date

-2-

IR-3234



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/688,338	03/20/2007	Thomas Herman	IR-3234(2-6008) V3753	9886
2352 7590 12/11/2008 OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403			EXAMINER AHMED, SELIM U	
			ART UNIT 2826	PAPER NUMBER
			MAIL DATE 12/11/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/688,338	Applicant(s) HERMAN, THOMAS	
	Examiner SELIM AHMED	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 September 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 September 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

1. Applicant's response filed on 09/02/2008 is acknowledged. Applicant has amended independent claims 1 and 10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer ET al (2005/0189561).

With regard to claims 1, 6, 7, e.g. Fig. 4 of Kinzer et al discloses a merged gate transistor comprising: a semiconductor element (21, 22, 23, and 24); a supply electrode 25 electrically connected to a top surface e.g. Fig. 4 of the semiconductor element; a drain electrode 26 electrically connected to the top surface of the semiconductor element and spaced laterally away from the supply electrode 25; a first gate 32 positioned between the supply electrode 25 and the drain electrode 26 and capacitively coupled to the semiconductor element to form a first portion of the transistor (e.g. Fig. 4, portion of transistor 32); and a second gate 34 positioned adjacent to the first gate 32, and between the supply

electrode 25 and the drain electrode 26 to form a second portion of the transistor (e.g. Fig. 4, portion of transistor 34), wherein the second gate 34 is also capacitively coupled to the semiconductor element; wherein the first gate 32 is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate 34 is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level and wherein in the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

The applicant's claims **1, 6, 7** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level. In another words, first portion or transistor 32 and second portion or transistor 34 are functioning as an enhancement and depletion mode

respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir. 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte Smith*, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer's** devices 32, 34 are capable of performing as an enhancement mode and depletion mode respectively (refer to claims 9 & 10 and para[0026, 0033, 0038]), because a comparison of Applicant's specification to **Kinzer's** disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes

Art Unit: 2826

as being capable of performing the functioning as an enhancement mode and depletion mode as indicated in the claims 9, 10, and para[0026, 0033, 0038]).

Because it is reasonable to assume that **Kinzer**'s device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 2, Fig. 4 of Kinzer et al discloses the merged gate transistor of claim 1, wherein the semiconductor element further comprises: a first III-Nitride layer 21; and a second III-Nitride layer 23 on which the first III-Nitride layer is positioned such that a 2DEG conduction layer 22 forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer (e.g. para[00320]).

With regard to claim 3, figure 4 and claim 3 of Kinzer et al disclose the merged gate transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 4, Fig. 4 and elements 21, 23 of Kinzer et al disclose the merged gate transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

With regard to claim 5, figure 4 and claim 3 of Kinzer et al disclose the merged gate transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 8, para [0025] of Kinzer et al disclose the merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 9, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

3. Claims 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer ET al (2005/0189561) in view of Beach (US 2006/0060871).

With regard to claims 10, 12, 13, 14, e.g. Fig.4 of Kinzer et al discloses a merged cascode high electron mobility transistor comprises: a first epitaxial layer 21 of III-Nitride material; a second epitaxial layer 23 of a III-Nitride material, in

contact with the first epitaxial layer 21 such that a 2-dimensional electron gas conducting layer 22 is formed between the first 21 and second 23 epitaxial layers; a supply electrode 25 electrically connected to the first epitaxial layer 21; a drain electrode 26 electrically connected to the first epitaxial layer 21 and spaced laterally from the supply electrode; a first gate 32 positioned between the supply electrode 25 and the drain electrode 26 and coupled to the first epitaxial layer to form a first portion (e.g. Fig. 4, portion of transistor 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode 26 and supply electrode 25 and coupled to the first epitaxial layer 21 to form a second portion (e.g. Fig. 4, portion of transistor 34) of the transistor; wherein the first gate 32 is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate 34 is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level and wherein the first portion of the transistor is an enhancement mode transistor (para[0038], claim 10) and the second portion of the transistor is a depletion mode transistor (e.g. para[0033, 0026] claim 9).

With regard to claims 10 and 12, as discussed above, Kinzer et al disclose all of the structural limitations with the exception of not disclosing the III-Nitride (AlGaIn and GaN) layers being epitaxial explicitly. However, para [0011] or para [0021] of Beach discloses the AlGaIn and GaN epitaxial layers. It would have

been obvious to one having ordinary skill in the art at the time of the invention to substitute Beach's epitaxial III-Nitride (AlGaN and GaN) layers with Kinzer's III—Nitride (AlGaN and GaN) layers for predictable results such as, low leakage characteristics of the HEMT device.

Furthermore, applicant's claims **10, 13, 14** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level. In another words, first portion or transistor 32 and second portion or transistor 34 are functioning as an enhancement and depletion mode respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such

tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte Smith*, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer's** devices 32, 34 are capable of performing as an enhancement mode and depletion mode respectively (refer to claims 9 &10 and para[0026, 0033, 0038]), because a comparison of Applicant's specification to **Kinzer's** disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode. Because it is reasonable to assume that **Kinzer's** device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 11, figure 4 and claim 3 of Kinzer et al disclose the merged cascode high electron mobility transistor of claim 10, further comprising

Art Unit: 2826

an insulating layer positioned between the first and second gates and the first epitaxial layer.

With regard to claim 15, para [0025] of Kinzer et al disclose the merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 16, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

Response to Arguments

4. Applicant's arguments filed on 09/02/2008 have been fully considered but they are not persuasive.

Applicant argued, "... claims 1 and 10 have been amended to call for the first portion of the transistor (which includes the first gate) to be an enhancement mode transistor and the second portion of transistor (which include the second gate) to be a depletion mode transistor. Neither Kinzer nor Beach discloses a device which includes an enhancement mode transistor and a depletion mode transistor sharing source and drain electrodes in combination with other limitations set forth in either claim 1 or claim 10. Thus, neither Kinzer, nor Beach,

Art Unit: 2826

nor a combination of Kinzer and Beach can render claims 1 and 10 obvious.

Reconsideration is requested”.

However, as indicated in the rejection, **Kinzer**’s devices 32, 34 are capable of performing as an enhancement mode and depletion mode respectively (refer to claims 9 &10 and para[0026, 0033, 0038]). Furthermore, in para[0034] of Kinzer discloses that “first gate electrode 32 and second gate electrode 34 are independently operable, meaning that each gate electrode receives a voltage pulse from a respective gate pad”. Additionally, a comparison of Applicant’s specification to **Kinzer**’s disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes. So, it is reasonable to believe that Kinzer’s device is capable of functioning as an enhancement mode and depletion mode.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory

action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information With regard to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service

Art Unit: 2826

Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SA

/Evan Pert/

Primary Examiner, Art Unit 2826

Notice of References Cited	Application/Control No. 11/688,338		Applicant(s)/Patent Under Reexamination HERMAN, THOMAS	
	Examiner SELIM AHMED		Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0189561 A1	09-2005	Kinzer et al.	257/192
*	B	US-2006/0060871 A1	03-2006	Beach, Robert	257/094
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 11688338	Applicant(s)/Patent Under Reexamination HERMAN, THOMAS
	Examiner SELIM AHMED	Art Unit 2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	05/22/2008	12/08/2008						
	1	✓	✓						
	2	✓	✓						
	3	✓	✓						
	4	✓	✓						
	5	✓	✓						
	6	✓	✓						
	7	✓	✓						
	8	✓	✓						
	9	✓	✓						
	10	✓	✓						
	11	✓	✓						
	12	✓	✓						
	13	✓	✓						
	14	✓	✓						
	15	✓	✓						
	16	✓	✓						

Search Notes 	Application/Control No. 11688338	Applicant(s)/Patent Under Reexamination HERMAN, THOMAS
	Examiner SELIM AHMED	Art Unit 2826

SEARCHED			
Class	Subclass	Date	Examiner
257	192, 194, 195, E29.14, E29.144, E29.246, E29.249	5/22/08	SA
	Updated search	12/8/08	/sa/

SEARCH NOTES		
Search Notes	Date	Examiner
Text search such as two dimensional electron gas, Cascode transistor, HEMT/High electron mobility transistor, source, drain, gate and their boolean combinations were searched.	5/22/08	SA
Updated search	12/8/2008	/sa/

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	192, 194, 195,	5/22/08	SA

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BIB DATA SHEET

CONFIRMATION NO. 9886

SERIAL NUMBER 11/688,338	FILING or 371(c) DATE 03/20/2007 RULE	CLASS 257	GROUP ART UNIT 2826	ATTORNEY DOCKET NO. IR-3234(2-6008) V3753		
APPLICANTS Thomas Herman, Manhattan Beach, CA; ** CONTINUING DATA ***** This appln claims benefit of 60/783,934 03/20/2006 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/29/2007						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/SELIM U AHMED/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 4	TOTAL CLAIMS 16	INDEPENDENT CLAIMS 2
ADDRESS OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403						
TITLE MERGED GATE CASCODE TRANSISTOR						
FILING FEE RECEIVED 1130	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
L2	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
L3	4811	cascode near3 transistor \$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
L4	8419	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
L5	332843	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
L6	80	L3 and L4 and L5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
L7	107	L3 and L4 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
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L14	365	L5 and L12 and L4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/08 09:49
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L28	125	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49
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L31	915	L29 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/08 09:49
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S2	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/16 11:22

S3	4541	cascocode near3 transistor \$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:21
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S5	314831	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22
S6	73	S3 and S4 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22
S7	96	S3 and S4 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:23
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S11	9	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 17:34

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S14	356	S5 and S12 and S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:54
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12/ 8/ 2008 9:56:48 AM

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IR-3234 (2-6008)

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Confirmation No. 9886

Thomas HERMAN

Date: August 28, 2008

U.S. Serial No.: 11/688,338

Group Art Unit: 2826

U.S. Filed: March 20, 2007

Examiner: Selim U. Ahmed

For: **MERGED CASCODE TRANSISTOR (As Amended)**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT/SUBMISSION

Sir:

This is a response to the Office Action mailed May 29, 2008 in the above-identified application. Reconsideration of the application is respectfully requested.

FEE CALCULATION

Any additional fee required has been calculated as follows:

_____ If checked, "Small Entity" status is claimed.

	NO. CLAIMS AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR		EXTRA PRESENT		RATE	ADDIT. FEE
TOTAL	16	MINUS	20	* =	0	X	(\$25 SE or \$50)	\$0
INDEP.	2	MINUS	3	** =	0	X	(\$105 SE or \$210)	\$0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM						X	(\$185 SE or \$370)	\$0
								TOTAL \$0

* not less than 20 ** not less than 3

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

00960476.1

CONTINGENT EXTENSION REQUEST

If this communication is filed after the shortened statutory time period had elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. § 1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 C.F.R. § 1.135. The fee under 37 C.F.R. § 1.17 should be charged to our Deposit Account No. 15-0700.

SUMMARY OF AMENDMENTS

1. ☐ If checked, an abstract (an amended abstract) is submitted herewith.
2. ☒ If checked, amendment(s) to the drawings are submitted herewith.
3. ☐ If checked, amendment(s) to the specification are submitted herewith.
4. ☒ If checked, amendment(s) to the claims are submitted herewith.

LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A merged cascode transistor comprising:
 - a semiconductor element;
 - a supply electrode electrically connected to a top surface of the semiconductor element;
 - a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the supply electrode;
 - a first gate positioned between the supply electrode and the drain electrode and ~~capacitively~~ coupled to the semiconductor element to form a first portion of the transistor; and
 - a second gate positioned adjacent to the first gate, and between the supply electrode and the drain electrode to form a second portion of the transistor, wherein the second gate is also ~~capacitively~~ coupled to the semiconductor element; wherein
 - the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level, and wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.
2. (Previously Presented) The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:
 - a first III-Nitride layer; and
 - a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein
 - the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer .

3. (Previously Presented) The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

4. (Previously Presented) The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

5. (Previously Presented) The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

6. (Previously Presented) The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

7. (Previously Presented) The merged cascode transistor of claim 6, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

8. (Previously Presented) The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

9. (Previously Presented) The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

10. (Currently Amended) A merged cascode high electron mobility transistor comprises:

a first epitaxial layer of III-Nitride material;
 a second epitaxial layer of a III-Nitride material, ~~positioned on top of said~~ in contact with
the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed
 between the first and second epitaxial layers;
 a supply electrode electrically connected to the first epitaxial layer;
 a drain electrode electrically connected to the first epitaxial layer and spaced laterally
 from the supply electrode;
 a first gate positioned between the supply electrode and the drain electrode and
~~capacitively~~ coupled to the first epitaxial layer to form a first portion of the transistor; and
 a second gate positioned adjacent to the first gate, and between the drain electrode and
 supply electrode and ~~capacitively~~ coupled to the first epitaxial layer to form a second portion of
 the transistor; wherein
 the first gate is connected to an input voltage signal such that conduction of the first
 portion is based on a value of the input voltage signal and the second gate is connected to a
 predetermined constant voltage such that the second portion of the transistor conducts until a
 voltage difference between the predetermined constant voltage and a voltage at the source
 electrode reaches a predetermined level, and wherein the first portion of the transistor is an
enhancement mode transistor and the second portion of the transistor is a depletion mode
transistor.

11. (Original) The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

12. (Currently Amended) The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGaN material and the ~~second~~ second epitaxial layer comprises a GaN material.

13. (Original) The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

14. (Previously Presented) The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

15. (Previously Presented) The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

16. (Previously Presented) The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.

AMENDMENT TO THE DRAWINGS

Fig. 1 has been amended. The attached sheet of formal drawings replaces the original sheet including Fig.1.

REMARKS/ARGUMENTS

The applicant's attorneys appreciate the Examiner's thorough search and remarks.

Responsive to Par. 5 of the Office Action, Fig. 1 has been corrected. Withdrawal of the objection is requested.

Claims 1-9 have been rejected as obvious over Kinzer et al. (Kinzer), U.S. Patent Publication No. 2005/0189561.

Claims 10-16 have been rejected as obvious over Kinzer in view of Beach, U.S. Patent Publication 2006/0060871.

Reconsideration is requested.

According to one aspect of the present invention, a first gate of the device is disposed over an interrupted region of a 2-DEG, which is restorable upon application of an appropriate threshold voltage and another second gate of a device is over a 2-DEG region, which can be interrupted upon the application of an appropriate voltage. See Fig. 3. Thus, the first gate, the source electrode and the drain electrode of the device form an enhancement mode transistor, while the second gate, the source electrode, and the drain electrode of the device form a depletion mode transistor. Paragraphs [0023] - [0024].

Accordingly, claims 1 and 10 have been amended to call for the first portion of the transistor (which includes the first gate) to be an enhancement mode transistor and the second portion of transistor (which include the second gate) to be a depletion mode transistor.

Neither Kinzer nor Beach discloses a device which includes an enhancement mode transistor and a depletion mode transistor sharing source and drain electrodes in combination with other limitations set forth in either claim 1 or claim 10. Thus, neither Kinzer, nor Beach, nor a combination of Kinzer and Beach can render claims 1 and 10 obvious. Reconsideration is requested.

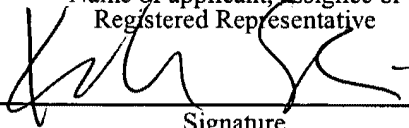
Each of the remaining claims depends from one of claim 1 or claim 10, and, therefore, includes the limitations thereof as well as additional limitations, which in combination with those of its base claim are not shown or suggested by the art of record. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450, on August 28, 2008

Kourosh Salehi

Name of applicant, assignee or
Registered Representative



Signature

August 28, 2008

Date of Signature

KS:gl

Respectfully submitted,



Kourosh Salehi

Registration No.: 43,898

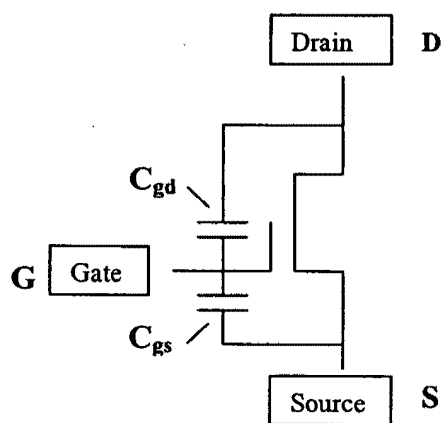
OSTROLENK, FABER, GERB & SOFFEN, LLP

1180 Avenue of the Americas

New York, New York 10036-8403

Telephone: (212) 382-0700

Fig. 1

10

PRIOR ART

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/688,338		Filing Date 03/20/2007		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A		N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A		N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A		N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=	OR	X \$	=	X \$	=	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=	OR	X \$	=	X \$	=	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT	09/02/2008	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
Total (37 CFR 1.16(i))	* 16	Minus	** 20	= 0	X \$	=	OR	X \$50=	0	
Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$	=	OR	X \$210=	0	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT	Total (37 CFR 1.16(i))	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	OR	X \$	=	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	OR	X \$	=	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/DEBORAH NASH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/688,338	03/20/2007	Thomas Herman	IR-3234(2-6008) V3753	9886
2352 7590 05/29/2008 OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403			EXAMINER AHMED, SELIM U	
			ART UNIT 2826	PAPER NUMBER
			MAIL DATE 05/29/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/688,338	Applicant(s) HERMAN, THOMAS	
	Examiner SELIM AHMED	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

1. This is an initial non-final office action based on the application filed on 03/20/2007. Claims 1-16 as originally filed and are examined.

Priority

2. Priority for the provisional Application No. 60/783934 filed on 03/20/2006 is acknowledged.

Information Disclosure Statement

3. No Information Disclosure Statement has been filed.

Oath/Declaration

4. The oath or declaration filed on 05/04/2007 is acceptable.

Drawings

5. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer ET al (2005/0189561).

With regard to claims 1, 6, 7, figure 4 of Kinzer et al discloses a merged gate transistor comprising: a semiconductor element (21, 22, 23, and 24); a supply electrode 25 electrically connected to a top surface of the semiconductor element; a drain electrode 26 electrically connected to the top surface of the semiconductor element and spaced laterally away from the supply electrode 25; a first gate 32 positioned between the supply electrode 25 and the drain electrode 26 and capacitively coupled to the semiconductor element to form a first portion of the transistor; and a second gate 34 positioned adjacent to the first gate 32, and between the supply electrode 25 and the drain electrode 26 to form a second portion of the transistor, wherein the second gate 34 is also capacitively coupled to the semiconductor element; wherein the first gate 32 is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate 34 is connected to a predetermined constant voltage such that the second portion of the transistor

conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level.

The applicant's claims **1, 6, 7** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level. In another words, first portion or transistor 32 and second portion or transistor 34 are functioning as an enhancement and depletion mode respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently

present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) (“Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product”). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer**’s devices 32, 34 are capable of performing as an enhancement mode and depletion mode respectively (refer to claims 9 &10), because a comparison of Applicant’s specification to **Kinzer**’s disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode. Because it is reasonable to assume that **Kinzer**’s device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 2, Fig. 4 of Kinzer et al discloses the merged gate transistor of claim 1, wherein the semiconductor element further comprises: a first III-Nitride layer 21; and a second III-Nitride layer 23 on which the first III-Nitride layer is positioned such that a 2DEG conduction layer 22 forms between

the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

With regard to claim 3, figure 4 and claim 3 of Kinzer et al disclose the merged gate transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 4, Fig. 4 and elements 21, 23 of Kinzer et al disclose the merged gate transistor of claim 3, wherein the first III-Nitride layer comprises AlGa_N material and the second III-Nitride layer comprises GaN material.

With regard to claim 5, figure 4 and claim 3 of Kinzer et al disclose the merged gate transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

With regard to claim 8, para [0025] of Kinzer et al disclose the merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 9, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

7. Claims 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer ET al (2005/0189561) in view of Beach (US 2006/0060871).

With regard to claims 10, 12, 13, 14, figure 4 of Kinzer et al discloses a merged cascode high electron mobility transistor comprises: a first epitaxial layer 21 of III-Nitride material; a second epitaxial layer 23 of a III-Nitride material, positioned on top of said first epitaxial layer such that a 2-dimensional electron gas conducting layer 22 is formed between the first and second epitaxial layers; a supply electrode 25 electrically connected to the first epitaxial layer; a drain electrode 26 electrically connected to the first epitaxial layer and spaced laterally from the supply electrode; a first gate 32 positioned between the supply electrode and the drain electrode and capacitively coupled to the first epitaxial layer to form a first portion (Fig. 32) of the transistor; and a second gate 34 positioned adjacent to the first gate, and between the drain electrode and supply electrode and capacitively coupled to the first epitaxial layer to form a second portion (Fig. 4) of the transistor; wherein the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level.

With regard to claims 10 and 12, as discussed above, Kinzer et al disclose all of the structural limitations with the exception of not disclosing the III-Nitride (AlGa_N and GaN) layers being epitaxial explicitly. However, para [0011] or para [0021] of

Beach discloses the AlGaN and GaN epitaxial layers. It would have been obvious to one having ordinary skill in the art at the time of the invention to substitute Beach's epitaxial III-Nitride (AlGaN and GaN) layers with Kinzer's III—Nitride (AlGaN and GaN) layers for low leakage characteristics of the HEMT device.

The applicant's claims **10, 13, 14** do not distinguish over the Kinzer et al reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level. In another words, first portion or transistor 32 and second portion or transistor 34 are functioning as an enhancement and depletion mode respectively. Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977)

(claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007) (“Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product”). See MPEP § 2114.

In this case, it is reasonable to assume that **Kinzer’s** devices 32, 34 are capable of performing as an enhancement mode and depletion mode respectively (refer to claims 9 & 10), because a comparison of Applicant’s specification to **Kinzer’s** disclosure reveals that **Kinzer** discloses a device that is apparently identical to the device Applicant describes as being capable of performing the functioning as an enhancement mode and depletion mode. Because it is reasonable to assume that **Kinzer’s** device is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

With regard to claim 11, figure 4 and claim 3 of Kinzer et al disclose the merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

With regard to claim 15, para [0025] of Kinzer et al disclose the merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

With regard to claim 16, para [0025] of Kinzer et al disclose the merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

CONCLUSION

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SA
05/08

/Minh-Loan T. Tran/
Primary Examiner
Art Unit 2826

Notice of References Cited	Application/Control No. 11/688,338		Applicant(s)/Patent Under Reexamination HERMAN, THOMAS	
	Examiner SELIM AHMED		Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0189561 A1	09-2005	Kinzer et al.	257/192
*	B	US-2006/0060871 A1	03-2006	Beach, Robert	257/094
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	310043	"257"/("192", "194", "195", "E29.14", "E29.144", "E29.246", "E29.249").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 15:10
L2	556	l1 and ((two near dimension\$3 near electron near gas) or 2DEG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 15:11
L3	852	l1 and HEMT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 15:11
S1	1	"11688338"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/15 18:55
S2	4	("20060043415" "20060043415" "6320205").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/16 11:22
S3	4541	cascode near3 transistor \$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:21
S4	7876	HEMT or (high near electron near mobility near transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22
S5	314831	source and drain and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22

S6	73	S3 and S4 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:22
S7	96	S3 and S4 and cascode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:23
S8	63	S6 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:23
S9	82	S7 and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:24
S10	5	("5155449" "5774792" "5939945" "6137367" "6515547").PN. OR ("7071786").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 17:33
S11	9	("20030168704" "5264713" "5510632" "6281521" "6285046" "6373318" "6573128" "6822275" "6822842"). PN. OR ("7026669"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 17:34
S12	1404	257/192.ccls. and @ad<"20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:53
S13	1116	S5 and S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:54
S14	356	S5 and S12 and S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 17:54

S15	14	("20020047177" "5504353" "5610410" "6072203" "6281528" "6534790" "7294900").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:00
S16	5	("5504353" "5610410" "6072203" "6281528" "6534790").PN. OR ("7294900").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:01
S17	14	("20010023964" "20020041003" "20020139995" "20020167023" "20060060871" "4424525" "4511813" "5387880" "5808332" "6177685" "6329677" "6465814" "6492669" "6690042").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:05
S18	45	("20020017648" "20030160269" "20030218183" "20040021152" "20040036086" "20040192043" "20050110054" "20050170574" "20050189561" "20050189562" "20050285098" "4615102" "5349214" "5594262" "6248666" "6342411" "6423986" "6465814" "6521961" "6552373" "6646293" "6710379" "6830945").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/21 18:20
S19	16	("4764796" "5099295" "5192987" "5670798" "5677553" "5929467" "6064082" "6114732").PN. OR ("6465814").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:25
S20	1635	(two near dimensional near electron near gas) or 2DEG	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:28
S21	1200	S5 and S20	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:29
S22	773	S5 and S20 and S4	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:29

S23	706	S22 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:30
S24	0	((two near dimensional near electron near gas) or 2DEG).abst.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:45
S25	275	((two near dimensional near electron near gas) or 2DEG).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/05/21 18:46
S26	232	S25 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:46
S27	232	S25 and @ad< "20060320"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/21 18:46
S28	121	(daniel near kinzer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/22 10:38

5/ 22/ 2008 3:26:02 PM

C:\Documents and Settings\sahmed7\My Documents\EAST\Workspaces\11688338.wsp



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BIB DATA SHEET

CONFIRMATION NO. 9886

SERIAL NUMBER 11/688,338	FILING or 371(c) DATE 03/20/2007 RULE	CLASS 257	GROUP ART UNIT 2826	ATTORNEY DOCKET NO. IR-3234(2-6008) V3753		
APPLICANTS Thomas Herman, Manhattan Beach, CA; ** CONTINUING DATA ***** This appln claims benefit of 60/783,934 03/20/2006 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/29/2007						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/SELIM U AHMED/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 4	TOTAL CLAIMS 16	INDEPENDENT CLAIMS 2
ADDRESS OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403						
TITLE MERGED GATE CASCODE TRANSISTOR						
FILING FEE RECEIVED 1130	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

<i>Index of Claims</i> 	Application/Control No. 11688338	Applicant(s)/Patent Under Reexamination HERMAN, THOMAS
	Examiner SELIM AHMED	Art Unit 2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	05/22/2008							
	1	✓							
	2	✓							
	3	✓							
	4	✓							
	5	✓							
	6	✓							
	7	✓							
	8	✓							
	9	✓							
	10	✓							
	11	✓							
	12	✓							
	13	✓							
	14	✓							
	15	✓							
	16	✓							

Search Notes 	Application/Control No. 11688338	Applicant(s)/Patent Under Reexamination HERMAN, THOMAS
	Examiner SELIM AHMED	Art Unit 2826

SEARCHED			
Class	Subclass	Date	Examiner
257	192, 194, 195, E29.14, E29.144, E29.246, E29.249	5/22/08	SA

SEARCH NOTES		
Search Notes	Date	Examiner
Text search such as two dimensional electron gas, Cascode transistor, HEMT/High electron mobility transistor, source, drain, gate and their boolean combinations were searched.	5/22/08	SA

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	192, 194, 195,	5/22/08	SA



APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/688,338	03/20/2007	Thomas Herman	IR-3234(2-6008) V3753

CONFIRMATION NO. 9886

2352

OSTROLENK FABER GERB & SOFFEN
1180 AVENUE OF THE AMERICAS
NEW YORK, NY100368403**Title:** MERGED GATE CASCODE TRANSISTOR**Publication No.** US-2007-0215899-A1**Publication Date:** 09/20/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Thomas HERMAN

Date: August 6, 2007

U.S. Serial No.: 11/688,338

Group Art Unit: 2811

U.S. Filed: March 20, 2007

Examiner: ---

For: **MERGED CASCODE TRANSISTOR (As Amended)**

VIA EFS-WEB

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits, kindly amend the application as follows:.

FEE CALCULATION

Any additional fee required has been calculated as follows:

_____ If checked, "Small Entity" status is claimed.

	NO. CLAIMS AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR		EXTRA PRESENT		RATE	ADDIT. FEE
TOTAL	16	MINUS	20	* =	0	X	(\$25 SE or \$50)	\$0
INDEP.	2	MINUS	3	** =	0	X	(\$100 SE or \$200)	\$0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM						X	(\$180 SE or \$360)	\$0
* not less than 20 ** not less than 3								TOTAL \$0

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

CONTINGENT EXTENSION REQUEST

If this communication is filed after the shortened statutory time period had elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. § 1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 C.F.R. § 1.135. The fee under 37 C.F.R. § 1.17 should be charged to our Deposit Account No. 15-0700.

SUMMARY OF AMENDMENTS

1. ☐ If checked, an abstract (an amended abstract) is submitted herewith.
2. ☐ If checked, amendment(s) to the drawings are submitted herewith.
3. ☒ If checked, amendment(s) to the specification are submitted herewith.
4. ☒ If checked, amendment(s) to the claims are submitted herewith.

AMENDMENT(S) TO THE SPECIFICATION

Please amend the specification as follows:

Please delete the title of the invention and replace it with the following:

MERGED CASCODE TRANSISTOR

LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A merged gate cascode transistor comprising:
 - a semiconductor element;
 - a supply electrode electrically connected to a top surface of the semiconductor element;
 - a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the supply electrode;
 - a first gate positioned between the supply electrode and the drain electrode and capacitively coupled to the semiconductor element to form a first portion of the transistor; and
 - a second gate positioned adjacent to the first gate, and between the supply electrode and the drain electrode to form a second portion of the transistor, wherein the second gate is also capacitively coupled to the semiconductor element; wherein
 - the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level.
2. (Currently Amended) ~~A~~ The merged gate cascode transistor of claim 1, wherein the semiconductor element further comprises:
 - a first III-Nitride layer; and
 - a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein
 - the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer .

3. (Currently Amended) ~~A~~ The merged gate cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

4. (Currently Amended) ~~A~~ The merged gate cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

5. (Currently Amended) ~~A~~ The merged gate cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

6. (Currently Amended) ~~A~~ The merged gate cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

7. (Currently Amended) ~~A~~ The merged gate cascode transistor of claim 6, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

8. (Currently Amended) ~~A~~ The merged gate cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

9. (Currently Amended) ~~A~~ The merged gate cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

10. (Currently Amended) A merged cascode high electron mobility transistor comprises:
a first epitaxial layer of III-Nitride material;

a second epitaxial layer of a III-Nitride material, positioned on top of said first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

a supply electrode electrically connected to the first epitaxial layer;

a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the supply electrode;

a first gate positioned between the supply electrode and the drain electrode and capacitively coupled to the first epitaxial layer to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the drain electrode and supply electrode and capacitively coupled to the first epitaxial layer to form a second portion of the transistor; wherein

the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level.

11. (Original) The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

12. (Original) The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGaN material and the second epitaxial layer comprises a GaN material.

13. (Original) The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

14. (Currently Amended) ~~A~~ The merged gate cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

15. (Currently Amended) ~~A~~ The merged gate cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

16. (Currently Amended) ~~A~~ The merged gate cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.

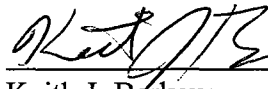
REMARKS/ARGUMENTS

Claims 1-16 are pending in the application. The title has been amended to better describe the subject matter of the present application. The claims have been amended to correspond to the title and to place them in more appropriate form for U.S. practice. None of the amendments adds any new matter to the application.

Entry of this Amendment into the file of the application is respectfully requested.

Respectfully submitted,

THIS CORRESPONDENCE IS BEING
SUBMITTED ELECTRONICALLY
THROUGH THE UNITED STATES
PATENT AND TRADEMARK OFFICE
EFS FILING SYSTEM
ON AUGUST 6, 2007



Keith J. Barkaus

Registration No.: 51,431

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New York, New York 10036-8403

Telephone: (212) 382-0700

LCD:KJB/jl

Electronic Acknowledgement Receipt

EFS ID:	2052695
Application Number:	11688338
International Application Number:	
Confirmation Number:	9886
Title of Invention:	MERGED GATE CASCODE TRANSISTOR
First Named Inventor/Applicant Name:	Thomas Herman
Customer Number:	2352
Filer:	Samuel H. Weiner/Jane Lim
Filer Authorized By:	Samuel H. Weiner
Attorney Docket Number:	IR-3234(2-6008) V3753
Receipt Date:	06-AUG-2007
Filing Date:	20-MAR-2007
Time Stamp:	17:28:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		00857969.pdf	204091 a7349f24d2757488cea58d8753a2e29b33c71615	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Preliminary Amendment	1	2
	Specification	3	3
	Claims	4	7
	Applicant Arguments/Remarks Made in an Amendment	8	8

Warnings:

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 11/688,338	
APPLICATION AS FILED – PART I					
(Column 1)		(Column 2)		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OTHER THAN SMALL ENTITY
BASIC FEE (37 CFR 1.16(a), (b), or (c))					300
SEARCH FEE (37 CFR 1.16(k), (l), or (m))					500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))					200
TOTAL CLAIMS (37 CFR 1.16(i))	16	minus 20 = *	X\$ 25		X\$50
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	X\$100		X\$200
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			N/A		N/A
			TOTAL		TOTAL 1000
* If the difference in column 1 is less than zero, enter "0" in column 2.					
APPLICATION AS AMENDED – PART II					
(Column 1)		(Column 2)		(Column 3)	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	Minus **	=		
	Independent (37 CFR 1.16(h))	Minus ***	=		
	Application Size Fee (37 CFR 1.16(s))				
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				
(Column 1)		(Column 2)		(Column 3)	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	Minus **	=		
	Independent (37 CFR 1.16(h))	Minus ***	=		
	Application Size Fee (37 CFR 1.16(s))				
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				
(Column 1)		(Column 2)		(Column 3)	
SMALL ENTITY		OTHER THAN SMALL ENTITY		SMALL ENTITY	
RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
X =		X =		X =	
X =		X =		X =	
N/A		N/A		N/A	
TOTAL ADD'T FEE		TOTAL ADD'T FEE		TOTAL ADD'T FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.					

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
11/688,338	03/20/2007	2811	1130	IR-3234(2-6008) V3753	16	2

CONFIRMATION NO. 9886

2352
OSTROLENK FABER GERB & SOFFEN
1180 AVENUE OF THE AMERICAS
NEW YORK, NY100368403

UPDATED FILING RECEIPT

Date Mailed: 05/14/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Thomas Herman, Manhattan Beach, CA;

Power of Attorney: The patent practitioners associated with Customer Number 2352

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/783,934 03/20/2006

Foreign Applications

If Required, Foreign Filing License Granted: 03/29/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is
US11/688,338

Projected Publication Date: 09/20/2007

Non-Publication Request: No

Early Publication Request: No

Title

MERGED GATE CASCODE TRANSISTOR

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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NEW YORK, NY100368403

UPDATED FILING RECEIPT

Date Mailed: 05/11/2007

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Applicant(s)

Thomas Herman, Manhattan Beach, CA;

Power of Attorney: The patent practitioners associated with Customer Number 2352

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Non-Publication Request: No

Early Publication Request: No

Title

MERGED GATE CASCODE TRANSISTOR

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of

Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Thomas HERMAN

Date: May 4, 2007

Serial No.: 11/688,338

Group Art Unit: 2811

Filed: March 20, 2007

Examiner: ---

For: **MERGED GATE CASCODE TRANSISTOR**

VIA EFS-WEB

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

**RESPONSE TO NOTICE TO FILE MISSING
PARTS OF NONPROVISIONAL APPLICATION**

Sir:

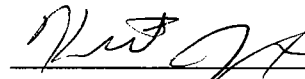
In response to the Notice to File Missing Parts of Nonprovisional Application mailed March 30, 2007, submitted herewith is the Inventor(s) Declaration and our credit card payment in the amount of \$130.00, being submitted via EFS-WEB, in payment of the surcharge.

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account #15-0700.

If this communication is filed after the time period had elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing a response by the number of months which will avoid abandonment under 37 C.F.R. §1.135. The fee under 37 C.F.R. § 1.17 should be charged to our Deposit Account No. 15-0700.

Respectfully submitted,

THIS CORRESPONDENCE IS BEING
SUBMITTED ELECTRONICALLY
THROUGH THE UNITED STATES
PATENT AND TRADEMARK OFFICE
EFS FILING SYSTEM
ON MAY 4, 2007



Keith J. Barkaus

Registration No.: 51,431

OSTROLENK, FABER, GERB & SOFFEN, LLP

1180 Avenue of the Americas

New York, New York 10036-8403

Telephone: (212) 382-0700

SHW:KJB/jl



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/688,338	03/20/2007	Thomas Herman	IR-3234(2-6008) V3194

CONFIRMATION NO. 9886

FORMALITIES
 LETTER

2352
 OSTROLENK FABER GERB & SOFFEN
 1180 AVENUE OF THE AMERICAS
 NEW YORK, NY 100368403

Date Mailed: 03/30/2007

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

*Filing Date Granted***Items Required To Avoid Abandonment:**

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$130** for a non-small entity

- \$130** Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
 Commissioner for Patents

P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebs>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.



Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199
PART 1 - ATTORNEY/APPLICANT COPY

UNITED STATES OF AMERICA COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION		OFGS FILE NO. IR-3234 (2-6008)																																															
<p>As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:</p> <p>MERGED GATE CASCODE TRANSISTOR</p>																																																	
<p>the specification of which is attached hereto, unless the following box is checked:</p> <p>☒ was filed on <u>March 20, 2007</u> as United States patent Application Number or PCT International patent application number <u>11/688,338</u> and was amended on _____ (if any).</p> <p>I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.</p> <p>I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.</p> <p>I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:</p> <p>Prior Foreign or Provisional Application(s)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">COUNTRY</th> <th style="width: 25%;">APPLICATION NUMBER</th> <th style="width: 25%;">DATE OF FILING (day, month, year)</th> <th style="width: 25%;">PRIORITY CLAIMED UNDER 35 U.S.C. 119</th> </tr> </thead> <tbody> <tr> <td>United States</td> <td>60/783,934</td> <td>20 March 2006</td> <td>YES <u>X</u> NO ____</td> </tr> <tr> <td> </td> <td> </td> <td> </td> <td>YES ____ NO ____</td> </tr> <tr> <td> </td> <td> </td> <td> </td> <td>YES ____ NO ____</td> </tr> </tbody> </table> <p>I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">UNITED STATES APPLICATION NUMBER</th> <th style="width: 30%;">DATE OF FILING (day, month, year)</th> <th style="width: 40%;">STATUS (patented, pending, abandoned)</th> </tr> </thead> <tbody> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> </tbody> </table> <p>I hereby appoint customer no. 2352 OSTROLENK, FABER, GERB & SOFFEN, LLP, and the members of the firm, Samuel H. Weiner - Reg. No. 18,510; Robert C. Faber - Reg. No. 24,322; Max Moskowitz - Reg. No. 30,576; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944; Louis C. Dujmich - Reg. No. 30,625; Douglas A. Miro - Reg. No. 31,643, and Kourosh Salehi - Reg. No. 43,898 as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.</p> <p>SEND CORRESPONDENCE TO: OSTROLENK, FABER, GERB & SOFFEN, LLP 1180 AVENUE OF THE AMERICAS NEW YORK, NEW YORK 10036-8403 CUSTOMER NO. 2352</p> <p style="text-align: right;">DIRECT TELEPHONE CALLS TO: (212) 382-0700</p> <p>I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">FULL NAME OF SOLE OR FIRST INVENTOR Thomas Herman</td> <td style="width: 30%;">INVENTOR'S SIGNATURE <i>Thomas Herman</i></td> <td style="width: 30%;">DATE 4-30-2007</td> </tr> <tr> <td colspan="2">RESIDENCE (City and either State or Foreign Country) Manhattan Beach, California 90266</td> <td>COUNTRY OF CITIZENSHIP United States</td> </tr> <tr> <td colspan="3">POST OFFICE ADDRESS 3113 Palm Avenue, Manhattan Beach, California 90266</td> </tr> <tr> <td>FULL NAME OF SECOND JOINT INVENTOR (IF ANY)</td> <td>INVENTOR'S SIGNATURE</td> <td>DATE</td> </tr> <tr> <td colspan="2">RESIDENCE (City and either State or Foreign Country)</td> <td>COUNTRY OF CITIZENSHIP</td> </tr> <tr> <td colspan="3">POST OFFICE ADDRESS</td> </tr> </table>				COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119	United States	60/783,934	20 March 2006	YES <u>X</u> NO ____				YES ____ NO ____				YES ____ NO ____	UNITED STATES APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)										FULL NAME OF SOLE OR FIRST INVENTOR Thomas Herman	INVENTOR'S SIGNATURE <i>Thomas Herman</i>	DATE 4-30-2007	RESIDENCE (City and either State or Foreign Country) Manhattan Beach, California 90266		COUNTRY OF CITIZENSHIP United States	POST OFFICE ADDRESS 3113 Palm Avenue, Manhattan Beach, California 90266			FULL NAME OF SECOND JOINT INVENTOR (IF ANY)	INVENTOR'S SIGNATURE	DATE	RESIDENCE (City and either State or Foreign Country)		COUNTRY OF CITIZENSHIP	POST OFFICE ADDRESS		
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POST OFFICE ADDRESS																																																	

Electronic Patent Application Fee Transmittal

Application Number:	11688338			
Filing Date:	20-Mar-2007			
Title of Invention:	MERGED GATE CASCODE TRANSISTOR			
First Named Inventor/Applicant Name:	Thomas Herman			
Filer:	Samuel H. Weiner/Jane Lim			
Attorney Docket Number:	IR-3234(2-6008) V3194			
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				130

Electronic Acknowledgement Receipt

EFS ID:	1744390
Application Number:	11688338
International Application Number:	
Confirmation Number:	9886
Title of Invention:	MERGED GATE CASCODE TRANSISTOR
First Named Inventor/Applicant Name:	Thomas Herman
Customer Number:	2352
Filer:	Samuel H. Weiner/Jane Lim
Filer Authorized By:	Samuel H. Weiner
Attorney Docket Number:	IR-3234(2-6008) V3194
Receipt Date:	04-MAY-2007
Filing Date:	20-MAR-2007
Time Stamp:	12:19:11
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 130
RAM confirmation Number	1748
Deposit Account	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
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1	Applicant Response to Pre-Exam Formalities Notice	00838139.pdf	101711	no	3
Warnings:					
Information:					
2	Oath or Declaration filed	00838140.pdf	67823	no	1
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8162	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			177696		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
11/688,338	03/20/2007	2811	1000	IR-3234(2-6008) V3194	16	2

CONFIRMATION NO. 9886

2352

OSTROLENK FABER GERB & SOFFEN
1180 AVENUE OF THE AMERICAS
NEW YORK, NY 100368403

FILING RECEIPT

Date Mailed: 03/30/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Thomas Herman, Manhattan Beach, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/783,934 03/20/2006

Foreign Applications

If Required, Foreign Filing License Granted: 03/29/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is
US11/688,338

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

MERGED GATE CASCODE TRANSISTOR

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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Title 35, United States Code, Section 184

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GRANTED

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the

Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).



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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/688,338	03/20/2007	Thomas Herman	IR-3234(2-6008) V3194

2352
 OSTROLENK FABER GERB & SOFFEN
 1180 AVENUE OF THE AMERICAS
 NEW YORK, NY 100368403

CONFIRMATION NO. 9886

FORMALITIES
 LETTER

Date Mailed: 03/30/2007

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

*Filing Date Granted***Items Required To Avoid Abandonment:**

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

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- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$130** for a non-small entity

- \$130** Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
 Commissioner for Patents

P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
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In re Patent Application of:

Thomas HERMAN

Date: March 20, 2007

Serial No.: Not Yet Known

Filed: Herewith

For: **MERGED GATE CASCODE TRANSISTOR**

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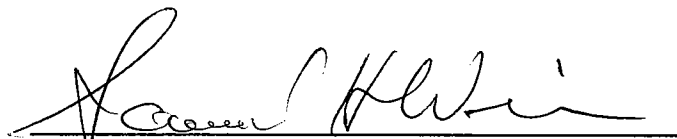
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IR-3234(2-6008) V3194
		Application Number	
Title of Invention	MERGED GATE CASCODE TRANSISTOR		
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Title of the Invention	MERGED GATE CASCODE TRANSISTOR		
Attorney Docket Number	IR-3234(2-6008) V3194	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IR-3234(2-6008) V3194
		Application Number	
Title of Invention	MERGED GATE CASCODE TRANSISTOR		

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	non provisional of	60783934	2006-03-20

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IR-3234(2-6008) V3194
		Application Number	
Title of Invention	MERGED GATE CASCODE TRANSISTOR		

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MERGED GATE CASCODE TRANSISTOR

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims benefit of and priority to United States Provisional Application Serial No. 60/783,934, filed on March 20, 2006, entitled MERGED CASCODE TRANSISTOR (III-NITRIDE, COMPOUND, OR SILICON SEMICONDUCTOR) FOR LOW Q_g, FAST SWITCHING AND HIGH VOLTAGE, the entire contents of which are hereby incorporated by reference herein.

[0002] The present application is also related to U.S. Patent Application Serial No. 11/345,753 entitled III-NITRIDE INTEGRATED SCHOTTKY AND POWER DEVICE filed February 2, 2006, which claims benefit of and priority to U.S. Provisional Patent Application Serial No 60/649,393 entitled GaN MONOLITHIC FETKY SYNCHRONOUS RECTIFIER FOR BOOST DIODE filed February 2, 2005, the entire contents of both of which are hereby incorporate by reference herein.

BACKGROUND OF THE INVENTION

[0003] The present invention relates to a transistor for use in high voltage, high speed switching applications. More specifically, the present application relates to a merged gate transistor that is useful for high voltage, high speed applications.

[0004] Fig. 1 illustrates a schematic representation of a conventional field effect transistor (FET) **1**. The FET **1** includes a drain **D**, a source **S** and a gate **G** to control current flow between the drain and the source. When FETs, like FET **1** in Fig. 1 are used in used in large switching applications, for example, in DC-DC power converters, low gate charge/capacitance and low gate-drain capacitance are important parameters in providing high frequency and high efficiency. Large drain-

source voltage (V_{ds}) swings during switching create a large “Miller effect” and as a result, excessive switching losses.

[0005] In addition, high dV/dt changes at the drain (D) may result in a voltage transient V_{G1} at the gate (G). The magnitude of the transient V_{G1} is proportional to the ratio of the gate-drain capacitance (C_{gd}) to the gate-source capacitance (C_{gs}) C_{gd}/C_{gs} . As a result, the transient V_{G1} may turn the transistor 1 ON briefly when not desired. This unwanted period of conduction may result in rather large power and efficiency losses. These problems are common in all FET devices whether they are silicon, non-silicon or HEMT devices.

[0006] Accordingly, it would be desirable to provide a transistor suitable for use in high voltage, high speed switching applications that avoids the problems discussed above.

SUMMARY OF THE INVENTION

[0007] A merged gate transistor in accordance with an embodiment of the present invention includes a semiconductor element, a supply electrode electrically connected to a top surface of the semiconductor element, drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the supply electrode, a first gate positioned between the supply electrode and the drain electrode and capacitively coupled to the semiconductor element to form a first portion of the transistor and a second gate positioned adjacent to the first gate, and between the supply electrode and the drain electrode to form a second portion of the transistor, wherein the second gate is also capacitively coupled to the semiconductor element. The first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level.

[0008] A merged cascode high electron mobility transistor in accordance with an embodiment of the present invention includes a first epitaxial layer of III- Nitride

material, a second epitaxial layer of a III-Nitride material, positioned on top of said first epitaxial layer such that a 2 dimensional electron gas conducting layer is formed between the first and second epitaxial layers, a supply electrode electrically connected to the first epitaxial layer, a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the supply electrode, a first gate positioned between the supply electrode and the drain electrode and capacitively coupled to the first epitaxial layer to form a first portion of the transistor and a second gate positioned adjacent to the first gate, and between the drain electrode and the supply electrode and capacitively coupled to the first epitaxial layer to form a second portion of the transistor. The first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level.

[0009] Embodiments and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Fig. 1 illustrates a schematic view of a conventional FET.

[0011] Fig. 2 illustrates a merged gate transistor in accordance with an embodiment of the present invention.

[0012] Fig. 3 illustrates an operative configuration for a transistor device in accordance with an embodiment of the present invention.

[0013] Fig. 4 illustrates an operative configuration for a transistor device in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0014] A transistor **20** suitable for use in high voltage, high speed switching applications in accordance with an embodiment of the present invention is described

with reference to Fig. 2. A single FET **20** with two merged gates **22**, **22¹** is illustrated in Fig. 2. That is, the FET **20** of Fig. 2 is a single device and not two separate FETs.

[0015] The top portion Q2 is in depletion mode, that is, normally ON with a depletion pinchoff voltage V_{p2} . The gate voltage V_{g2} at the gate **22¹** of the top portion Q2 is set to 0, as illustrated. However, depending on the specific application, the gate voltage V_{g2} may be set at any desired value.

[0016] The bottom portion Q1 of FET **20** is preferably in enhancement mode, that is, normally OFF, with an enhancement threshold voltage V_{t1} . An input voltage signal is preferably connected to the gate **22** to provide the gate voltage V_{g1} at the gate **22** of the bottom portion Q1.

[0017] In operation, when the input voltage signal provides a high voltage at V_{g1} , the bottom portion Q1 is conducting. That is, the level of the input voltage signal is sufficiently high such that the enhancement threshold voltage V_{t1} is met or exceeded and conduction occurs. The voltage at the node **24** (V_{d1s2}) at this time is low, substantially 0V. As noted above, the voltage at the gate **22¹** (V_{g2}) is set to 0, and thus, the gate-source voltage of the top portion Q2 is approximately 0V, as well. Since the top portion Q2 is in depletion mode, Q2 is fully ON and is fully conducting. Thus, both the top and bottom portions Q1, Q2 of device **20** are both ON and conducting. Further, the voltage at the drain (V_{d2}) of portion Q2 is close to 0 as well.

[0018] When the input voltage at V_{g1} and provided to the gate **22** of the bottom portion Q1 (V_{g1}) goes low, the bottom portion Q1 turns OFF and the bottom portion Q2 stops conducting. As a result, the voltage at the node **24** (V_{d1s2}) rises until the gate-source voltage (V_{gs}) of the top portion Q2 reaches the pinch off voltage V_{p2} and the top portion Q2 turns OFF. Thereafter, the drain voltage V_{d2} of the top portion Q1 rises to the full supply voltage.

[0019] Thus, in the device **20**, the voltage at node **24** (V_{d1s2}) never rises above the magnitude of the pinchoff voltage V_{p2} . The pinchoff voltage V_{p2} is preferably

set low, on the order of a few volts and is typically much lower than the peak drain voltage V_{d2} , or supply voltage, which is generally 10s - 100s of volts.

[0020] As a result, the drain swing of the bottom portion Q1 is substantially reduced, that is, a swing of only a few volts. This is a much smaller swing than would occur if a single FET were used alone as a switching device. As a result, Q1 need only be optimized for ultra-low voltage operation.

[0021] The FET **20** of the present invention offers several advantages. First, the “Miller effect” is greatly reduced, and thus power losses are also substantially reduced as well. The dV/dt at the drain (D1) of the bottom portion Q1 is also reduced, and thus, the capacitively coupled voltage transient V_{G1} is also reduced. As a result, the danger of shoot through is also substantially reduced. Further, since Q1 can be optimized for ultra-low voltage operation, short gate lengths (L_g) can be used which further reduce the overall gate charge of Q1 and improve switching performance. Since Q1 never has a high voltage on its drain (D1), Q1's gate does not need field plating which also reduces its capacitance. Q2 can be optimized for stable higher voltage operation, for example by field plating the gate. Ordinarily field plating the gate creates higher gate drain charge and high gate drain capacitance, however, since the gate G2 is grounded, any capacitively coupled shoot through voltage transient at G2 is relatively harmless such that unwanted conduction in the top portion Q2 is unlikely. While the configuration of Fig. 2 may lead to higher static R_{dson} , or DC conduction losses, the overall improved lower R Q figure of merit will result in lower overall power losses and higher efficiency.

[0022] Fig. 3 illustrates an exemplary embodiment of a transistor **30** in accordance with an embodiment of the present invention preferably implemented as a high electron mobility transistor (HEMT). Specifically, Fig. 3 illustrated a merged cascode HEMT **30** in accordance with an embodiment of the present invention that may be fabricated with insulated gates and a semiconductor element **29** including two III-Nitride epitaxial layers (**37, 37b**) with a 2DEG conducting layer (**28**) at the interface of the epitaxial layers (**37, 37b**).

[0023] Generally, in the HEMT **30** of Fig. 3, the first (or bottom) portion Q1 is in enhancement mode such that the 2DEG is typically not present under the gate G1 when $V_{g1}=0$, as illustrated. This may be accomplished by using a recessed gate, fluorine implants or any other suitable means. As illustrated, a source contact **31** is positioned on a top surface of a semiconductor element **29**, which may include the first epitaxial layer **37**. The gates G1, G2 (**32, 33**) are positioned adjacent to the source contact **31** and are separated from the top surface of the first epitaxial layer **37** by an insulating layer **38**. A drain contact **34** is positioned on the other side of the gates **32, 33** on the top surface of the first epitaxial layer **37**. The node **24** of Fig. 2 is represented by the arrow **39** in the area of the merged Q1 drain and Q2 source. That is, on the drain side of the gate **32** (G1) of the first portion Q1 and on the source side of the gate **33** (G2) of the second portion.

[0024] While specifically illustrated as an HEMT device in Fig. 3, it is noted that the first and second portions Q1, Q2 of the FET **20** may be fabricated using silicon, III-Nitride or may be a compound semiconductor, if desired. While the top portion Q2 is described as being in depletion mode and the bottom portion Q1 is described as being in enhancement mode, Q1 and Q2 may be in either depletion mode or in enhancement mode. Alternatively, both the first and second portion Q1, Q2 may be in the same mode, if desired.

[0025] The first and second portions Q1, Q2 may include insulated gates, Schottky gates, or junction gates. Further, the polarity of the conducting channel may be either N-type or P-type. The voltage V_{g2} at the gate **33** (G2) of portion Q2 may be set at some non-zero value, if desired, as is mentioned above.

[0026] The device of Fig. 3 may include a III-nitride base heterojunction **10** disposed over a support body **12**. Fig. 4 illustrates this embodiment and common reference numbers refer to common elements. The transistor **40** of Fig. 4 is similar to the switching device described in U.S. Patent Application Serial No. 11/345,753, mentioned above. Heterojunction **11** includes a first III-nitride semiconductor body **14**, and a second III-nitride semiconductor body **16** over first III-nitride semiconductor body **14**. A first power electrode **31** (i.e. source electrode) and a

second power electrode **34** (i.e. drain electrode) are electrically connected to second III-nitride semiconductor body 16 through a direct ohmic connection or any other suitable means. Two gate structures **32, 33** are disposed between electrodes **31, 34** over second III-nitride semiconductor body 16. In the preferred embodiment of the present invention, the gates **32, 33** are capacitively connected, or coupled, to second III-nitride semiconductor layer 16 through an insulating layer **38**, for example. Alternatively, gate structures **32, 33** may include a schottky gate electrode connected to second III-nitride semiconductor body 16.

[0027] In a device according to any one of the embodiments of the present invention, the first III-nitride semiconductor body is preferably an alloy from the InAlGaN system, such as GaN, and the second III-nitride semiconductor body 16 is another alloy from the InAlGaN system having a band gap that is different from that of first III-nitride semiconductor 14, whereby a two-dimensional electron gas (2DEG) is formed due to the heterojunction of the first and the second III-nitride semiconductor bodies as is well known in the art. For example, the second III-nitride semiconductor body may be formed with AlGaN. However, other materials may be used if desired.

[0028] In addition, support body 12 may be a combination of a substrate material, and if required, a buffer layer (not shown) on the substrate to compensate for the lattice and thermal mismatch between the substrate and first III-nitride semiconductor body 14. For economic reasons, the preferred material for the substrate is silicon. Other substrate materials such as sapphire, and SiC can also be used without deviating from the scope and the spirit of the present invention.

[0029] AlN is a preferred material for a buffer layer, if necessary. However, a multi-layer or graded transitional III-nitride semiconductor body may also be used as a buffer layer without deviating from the scope and the spirit of the present invention.

[0030] It is also possible to have the substrate made from the same material as first III-nitride semiconductor body and thus avoid the need for a buffer layer. For

example, a GaN substrate may be used when first III-nitride semiconductor body 14 is formed with GaN.

[0031] The gate electrodes **32, 33** may be composed of n type or p type silicon, or polysilicon of any desired conductivity, or TiW, aluminum, Ti/Al, refractory silicides, or other metallic layer. Ohmic electrodes **31, 34** may be composed of Ti/Al and may further include other metallic bodies over the top surface thereof such as Ti/TiW, Ni/Au, Mo/Au, or the like. Any other metal system that makes low resistance contact to the 2DEG may be employed. Gate insulating layer **38** may be composed of SiN, Al₂O₃, SiO₂, HfO, MgO, Sc₂O₃, or the like. Schottky metal for schottky electrode 26 may include nickel, platinum, palladium, silicides of those metals, or any other metal with sufficient barrier height to keep leakage low.

[0032] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

WHAT IS CLAIMED IS:

1. A merged gate transistor comprising:
 - a semiconductor element;
 - a supply electrode electrically connected to a top surface of the semiconductor element;
 - a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the supply electrode;
 - a first gate positioned between the supply electrode and the drain electrode and capacitively coupled to the semiconductor element to form a first portion of the transistor; and
 - a second gate positioned adjacent to the first gate, and between the supply electrode and the drain electrode to form a second portion of the transistor, wherein the second gate is also capacitively coupled to the semiconductor element; wherein the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level.
2. The merged gate transistor of claim 1, wherein the semiconductor element further comprises:
 - a first III-Nitride layer; and
 - a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer .

3. The merged gate transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

4. The merged gate transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

5. The merged gate transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

6. The merged gate transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

7. The merged gate transistor of claim 6, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

8. The merged gate transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

9. The merged gate transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

10. A merged cascode high electron mobility transistor comprises:
a first epitaxial layer of III-Nitride material;
a second epitaxial layer of a III-Nitride material, positioned on top of said first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;
a supply electrode electrically connected to the first epitaxial layer;

a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the supply electrode;

a first gate positioned between the supply electrode and the drain electrode and capacitively coupled to the first epitaxial layer to form a first portion of the transistor; and

a second gate positioned adjacent to the first gate, and between the drain electrode and supply electrode and capacitively coupled to the first epitaxial layer to form a second portion of the transistor; wherein

the first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level.

11. The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.

12. The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGa_N material and the second epitaxial layer comprises a Ga_N material.

13. The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

14. The merged gate transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

15. The merged gate transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

16. The merged gate transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.

ABSTRACT OF THE DISCLOSURE

A merged gate transistor in accordance with an embodiment of the present invention includes a semiconductor element, a supply electrode electrically connected to a top surface of the semiconductor element, drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the supply electrode, a first gate positioned between the supply electrode and the drain electrode and capacitively coupled to the semiconductor element to form a first portion of the transistor and a second gate positioned adjacent to the first gate, and between the supply electrode and the drain electrode to form a second portion of the transistor, wherein the second gate is also capacitively coupled to the semiconductor element. The first gate is connected to an input voltage signal such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to a predetermined constant voltage such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at the source electrode reaches a predetermined level.

Fig. 1

10

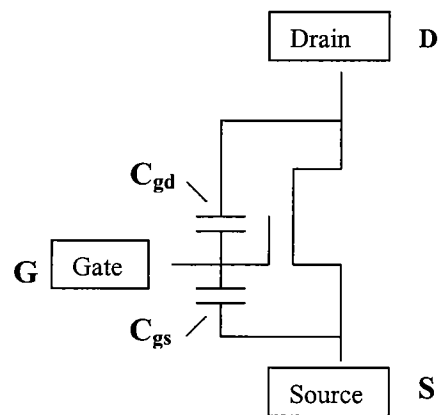


Fig. 2

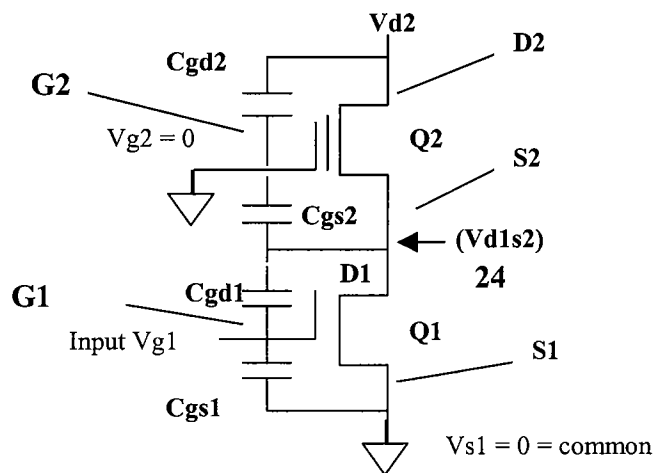


Fig. 3

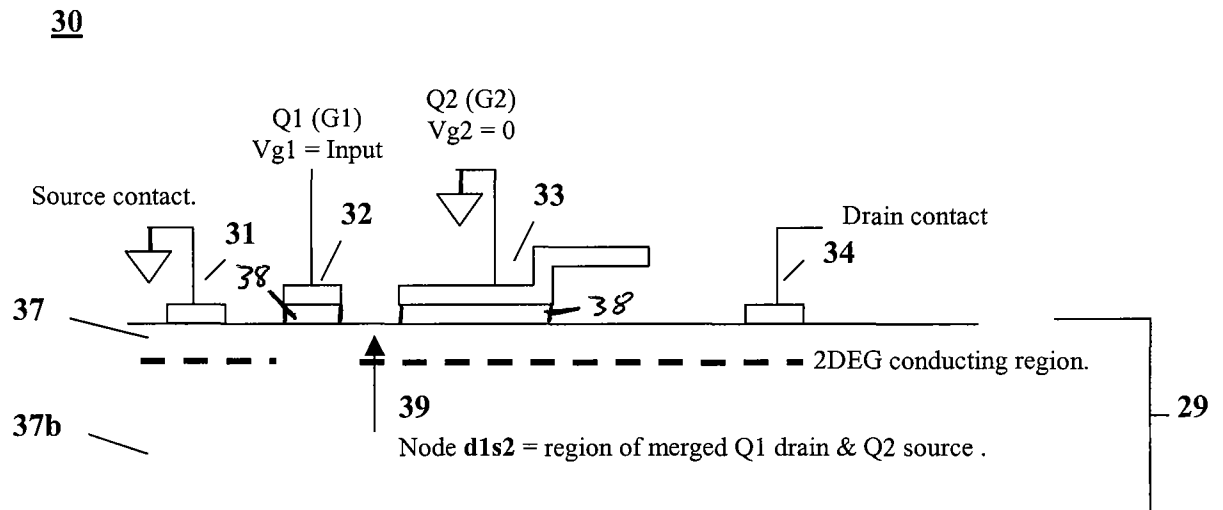
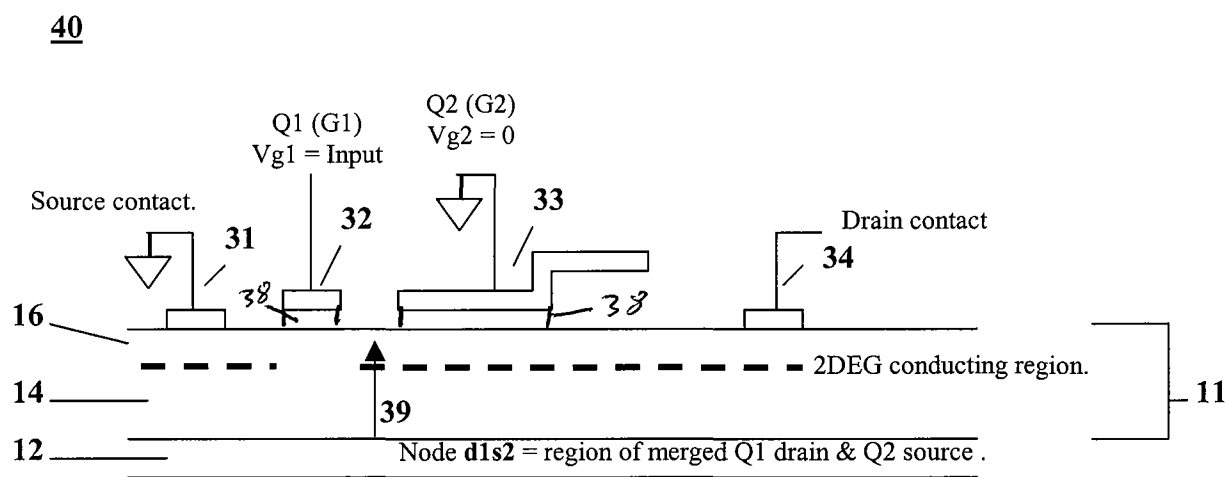


Fig. 4



Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	MERGED GATE CASCODE TRANSISTOR			
First Named Inventor/Applicant Name:	Thomas Herman			
Filer:	Samuel H. Weiner/Jane Lim			
Attorney Docket Number:	IR-3234(2-6008) V3194			
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	300	300
Utility Search Fee	1111	1	500	500
Utility Examination Fee	1311	1	200	200
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt

EFS ID:	1606600
Application Number:	11688338
International Application Number:	
Confirmation Number:	9886
Title of Invention:	MERGED GATE CASCODE TRANSISTOR
First Named Inventor/Applicant Name:	Thomas Herman
Customer Number:	02352
Filer:	Samuel H. Weiner/Jane Lim
Filer Authorized By:	Samuel H. Weiner
Attorney Docket Number:	IR-3234(2-6008) V3194
Receipt Date:	20-MAR-2007
Filing Date:	
Time Stamp:	12:09:55
Application Type:	Utility

Payment information:

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Payment was successfully received in RAM	\$ 1000
RAM confirmation Number	1980
Deposit Account	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
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1	Miscellaneous Incoming Letter	00826574.pdf	37513	no	1
Warnings:					
Information:					
2	Application Data Sheet	00826553.pdf	902869	no	4
Warnings:					
Information:					
3		00826559.pdf	499403	yes	13
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	8	
	Claims		9	12	
	Abstract		13	13	
Warnings:					
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4	Drawings	00826575.pdf	21899	no	4
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number

11/688,338**APPLICATION AS FILED – PART I**

(Column 1) (Column 2)

SMALL ENTITY

OR

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FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		
TOTAL CLAIMS (37 CFR 1.16(i))	16 minus 20 =	*
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

RATE (\$)	FEE (\$)
X\$ 25	
X\$100	
N/A	
TOTAL	

RATE (\$)	FEE (\$)
	300
	500
	200
X\$50	
X\$200	
N/A	
TOTAL	1000

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

(Column 1) (Column 2) (Column 3)

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AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	* Minus **	=	
Independent (37 CFR 1.16(h))	* Minus ***	=	
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL	
ADD'T FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL	
ADD'T FEE	

(Column 1) (Column 2) (Column 3)

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AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	* Minus **	=	
Independent (37 CFR 1.16(h))	* Minus ***	=	
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL	
ADD'T FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL	
ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

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