

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Professional Summary

Professor Bernstein's expertise lie in several areas of micro-electronic devices, packaging and system reliability, including failure analysis and reliability prediction. He is a world recognized expert in Microelectronics Devices, including GaN and SiC power device physics and reliability as well as electronic packaging. He is a member of the Standards Institutions of Israel (SII), he has worked directly with companies producing GaN power devices, DRAM, SDRAM, SRAM, and Flash memories. Included in his physics of failure research are power devices, gate oxide integrity and radiation effects. He has licensed his own technology and consulted for RFID, Flash, and other memory related companies. He directs the Laboratory for Failure Analysis and Reliability of Electronic Systems, teaches VLSI design courses and heads the VLSI program at Ariel University. His Laboratory is a center of research activity dedicated to serving the needs of manufacturers of highly reliable electronic systems and power electronics using commercially available off the shelf parts. Research areas include thermal, mechanical, and electrical interactions of failure mechanisms of ultra-thin gate dielectrics, Non-Volatile memory, advanced metallization and power devices. He also works extensively with the semiconductor industry on projects relating to failure analysis, defect avoidance and degradation in microelectronic circuits and packaging. He has developed an important method for predicting device failure rates based on new JEDEC standards for multiple failure rate-based prediction. Professor Bernstein was a Fulbright Senior Researcher/Lecturer, Honored lecturer at "Nanorun," and at IEEE Summer-School in Toulouse, France. Professor Bernstein is a senior member of IEEE.

Expertise

- Microelectronics and Electronic Device and System Design and Reliability
- Power Electronics Devices and Architecture
- Advanced Packaging of Electronic Devices
- SiC and GaN Power Device Reliability
- DRAM, SDRAM, SRAM & Flash (NAND and NOR) Memory Cells
- Electronics Lifetime Prediction
- Failure Analysis of Electronic Circuits
- Fuse Processing for Redundancy and Memory Repair
- Gate Oxide Integrity of in Ultra-Thin Gate Dielectrics
- Hot Carrier Degradation of Nanometer Scale Devices
- Processing of Semiconductor Devices and Wafers and Packaging (Ball Grid Array).
- Materials Processing for Advanced Semiconductor Devices
- Materials Processing for MEMS Applications
- Multiple Failure Rate Modeling and Lifetime Prediction
- Programmable Gate array architecture, layout and redundancy
- Semiconductor Device Processing Materials and Technologies
- Thermal Fatigue of Electronic Circuit Boards
- GaN Power Semiconductor Devices

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Education

<u>Year</u>	<u>College or University</u>	<u>Degree</u>
1990	Massachusetts Institute of Technology	Ph.D., Electrical Engineering and Computer Science, GPA: 5.0/5.0
1987	Massachusetts Institute of Technology	E.E., Electrical Engineer, GPA: 5.0/5.0
1986	Massachusetts Institute of Technology	M.S., Electrical Engineering and Computer Science, GPA: 5.0/5.0
1984	Union College, Schenectady, NY	B.S., Electrical Engineering, GPA: 3.9/4.0 Summa Cum Laude

Professional Experience

From:	2012
To:	Present
Organization:	Ariel University, Israel
Title:	Professor, Faculty of Engineering
From:	2009
To:	Present
Organization:	Reliability International Associates LLC, Reliability consulting company
Title:	Founder and Owner
From:	2007
To:	2012
Organization:	Bar Ilan University, Israel
Title:	Professor, Faculty of Engineering
From:	2003
To:	2005
Organization:	Tel-Aviv University, Israel
Summary:	
2003 – 2005	Visiting Associate Professor of Engineering, Faculty of Engineering
2004 – 2005	Fulbright Senior Scholar
From:	1995
To:	2008
Organization:	University of Maryland

Joseph B. Bernstein, Ph.D. Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Summary:

2001 – 2007 Associate Professor, Mechanical Engineering
1995 – 2001 Assistant Professor of Reliability, Materials and Nuclear Engineering Dept.
Summer 1998 NASA/ASEE Summer Faculty Research Fellow, JPL, Pasadena, CA.

From: 2002
To: 2006
Organization: LaserLink Technology, LLC (Maryland based)
Title: Owner

From: 1995
To: 1997
Organization: Lightspeed Semiconductor, Inc.
Title: Founder and Chief Scientist

From: 1991
To: 1993
Organization: Boston University
Title: Adjunct Professor

From: 1990
To: 1995
Organization: MIT Lincoln Library, Lexington, MA
Title: Research Staff

Litigation Support Experience

Expert Engagement:

Type of Matter: Jury Trial for Patent Infringement
Law Firm: Winston & Strawn LLP | <https://www.winston.com/>
255 Shoreline Drive, Suite 520; Redwood City, CA 94065
Case Name: **Netlist Vs. Micron Semiconductors**
UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS Case No. 2:22-cv-294-JRG
Services Provided: Engaged as an alternate expert providing expert analysis and testimony for the
defendant, Micron Semiconductors
Disposition: Original witness served at trial.
Date: 2024

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Expert Engagement:

Type of Matter: Inter-Parte Review defending patent owner.
Law Firm: DEVLIN LAW FIRM LLC
Case Name: NXP USA, INC., Petitioner, v. BELL SEMICONDUCTOR, LLC, Patent Owner. IPR2024-00142, 00167, 00168
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony.
Disposition: 2 Patent was found unpatentable, one went to trial
Date: 2024

Expert Engagement:

Type of Matter: Jury Trial for Trade Secret Violation under and NDA
Law Firm: Bejin Bieneman PLC | 2000 Town Center, Suite 800 | Southfield, MI 48075 313-528-4882 | www.b2iplaw.com
Case Name: **MERSEN USA EP CORP., v. TDK ELECTRONICS INC.**
UNITED STATES DISTRICT COURT
SOUTHERN DISTRICT OF NEW YORK **Case No. 21-cv-00763**
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony for the plaintiff, Mersen USA
Disposition: Settled highly favorably for the Plaintiff!
Date: 2023

Expert Engagement:

Type of Matter: District Court Trial for Patent Invalidity and Breach of Contract
Law Firm: Covington & Burling LLP
Salesforce Tower, 415 Mission Street, Suite 5400
San Francisco, CA 94105-2533
Case Name: **SAMSUNG ELECTRONICS CO., LTD. AND SAMSUNG SEMICONDUCTOR, INC. Vs. NETLIST INC. Del case: 21-1453-RGA**
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony for the Plaintiff, Samsung Electronics Inc.
Disposition: Judge put a Stay on the case due to IPR wins from Plaintiff.
Date: 2023

Expert Engagement:

Type of Matter: District Court Jury Trial for Product Fraud
Law Firm: ORRICK HERRINGTON & SUTCLIFFE
405 Howard Street San Francisco, California 94105-2675
Case Name: **Allied Telesis K.K. v. Micron Technology, Inc.**
Santa Clara County, CA Case No. 2015-1-CV-282977
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony for the defendant, Micron Technology, Inc.
Disposition: Settled favorably for the Defendant
Date: 2021-2022

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Expert Engagement:

Type of Matter: Due-Diligence Consulting and Patent Analysis
Law Support Firm: Papst Licensing GmbH, Germany and Detroit
Case Name: Trolling software development
Services Provided: Engaged as Expert providing consulting and analysis of a portfolio of IBM patents to validate a developing software and provide due-diligence support.
Disposition: Found none of hundreds of patents useful to pursue.
Date: 2021-2022

Expert Engagement:

Type of Matter: Inter-Parte Review defending patent owner.
Law Firm: SKIERMONT DERBY LLP
Case Name: ADVANCED SEMICONDUCTOR ENGINEERING, INC., PETITIONER,
V. BELL SEMICONDUCTOR LLC, PATENT OWNER.
Case No. IPR2021-00180, U.S. Patent No. 6,624,007
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony.
Disposition: Patent was found unpatentable.
Date: 2021-2022

Expert Engagement:

Type of Matter: Inter-Parte Review defending patent owner.
Law Firm: Mishcon De Reya New York, LLP
Case Name: RPX CORPORATION and AMD, INC. vs. IYM Technologies, LLC.
IPR2017-01886 and 88
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony.
Disposition: Patent was found unpatentable.
Date: 2018

Expert Engagement:

Type of Matter: Patent Infringement defending patent owner.
Law Firm: Lowenstein and Weatherwax, LLP
Case Name: KINGSTON Technology v. POLARIS Innovations
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony.
Disposition: 01623 resolved as NOT un-patentable.
Date: 2017

Expert Engagement:

Type of Matter: Patent Infringement defending patent owner.
Law Firm: TENSEGRITY LAW GROUP, LLP
Case Name: KINGSTON Technology v. POLARIS Innovations
Services Provided: Engaged as Expert providing expert reports, depositions, expert analysis and testimony.
Disposition: Case was dropped after IPR results
Date: 2017

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Expert Engagement:

Type of Matter: Patent Infringement defending patent owner.
Law Firm: DLA Piper
Case Name: MIPOX Corp. v. International Test Solutions, Inc. Inter Partes Reviews of
US patents 8,801,869; 7,202,683; and 6,777,966
Services Provided: Engaged as Expert providing expert reports, expert analysis and testimony.
Disposition: Brought to successful settlement and non-institution of necessary claims.
Date: 2017

Expert Engagement:

Type of Matter: Patent Infringement and validity
Law Firm: Dowling Aaron Incorporated
Case Name: *Beco Dairy Automation, Inc. v. Global Tech Systems, Inc.* (Eastern District of
California; 1:12-cv-01310-LJO-SMS
Services Provided: Engaged as Expert providing expert reports, expert circuit analysis and
testimony, Claim chart construction and expert testimony covering 8 patents
Disposition: Brought to successful and beneficial settlement
Date: 2016

Expert Engagement:

Type of Matter: Patent Infringement
Law Firm: Nix Patterson, LLP
Case Name: DSS Technology Management, LLC v. Intel Corp., Hynix, Samsung.
Services Provided: Engaged as Expert providing expert reports, expert circuit analysis and
testimony.
Disposition: Client pulled out after institution at IPR
Date: 2015

Expert Engagement:

Type of Matter: Patent Infringement
Law Firm: Desmarais, LLP
Case Name: Round Rock Research, LLC v. ACER, INC., and Gateway, Inc.,
Services Provided: Engaged as Expert providing expert reports, expert circuit analysis and
testimony, these cases successfully, were settled out of court.
Disposition: Settled
Date: 2014

Expert Engagement:

Type of Matter: Patent Interference
Law Firm: Oblong, Spivak, McClelland, Maier, & Neustadt, PC, for Defendant
Case Name: Yunlong Sun, Edward J. Swenson and Richard S. Harris v. Donald V. Smart
Services Provided: Engaged as Expert for over 6 years supporting patent interferences cases
involving laser processing in semiconductor devices. Numerous expert reports
and depositions as well as interviews at the patent office and testimony.
Disposition: Company was purchased by the competition.
Date: 2008-2012

Joseph B. Bernstein, Ph.D. Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Expert Engagement:

Type of Matter: Patent Re-Examination
Law Firm: Law Office of Andrew D. Fortney
Case Name: MIT/UMD appeal to USPTO
Services Provided: Engaged as Expert writing expert testimony in defense of a patent in the semiconductor field
Disposition: Successful defense of patent
Date: 2012

Expert Engagement:

Type of Matter: Patent Infringement
Law Firm: Townsend Townsend and Crew, LLC
Case Name: Agere v. Samsung
Services Provided: Engaged as Expert providing expert reports and testimony, the case was successfully settled out of court.
Disposition: Settled
Date: 2006

Expert Engagement:

Type of Matter: Patent Infringement
Law Firm: Brown & Bain, PA, for Defendant
Case Name: EMI Group North America, Inc. v. Cypress Semiconductor Corporation
Services Provided: Engaged as Expert over 3 years providing numerous expert reports and trial testimony defending the company's use of technology in alleged violation of a patent, which we proved in court to have been invalid.
Disposition: We defeated the patent at trial and sustained on appeal
Date: 2001, 2003

Expert Engagement:

Type of Matter: Patent Infringement
Law Firm: Choate Hall & Stewart
Case Name: GSI v. A-B Lasers
Services Provided: Engaged as Expert providing hands-on consulting, expert testimony and reports relating to laser processing of silicon wafers for marking technology.
Disposition: Settled
Date: 2001

Industrial Consultation and Involvement

Consulting Project:

Client: EPC Corporation
Services Provided: GaN Power Circuit Design, Evaluation and Qualification

Consulting Project:

Client: Sandisk
Services Provided: Test and Reliability Consultant.

Joseph B. Bernstein, Ph.D. Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Consulting Project:

Client: Maradin Corp.
Services Provided: Accelerated Reliability and Qualification Consulting.

Consulting Project:

Client: Camtek Corp.
Services Provided: Reliability Testing and Qualification Consulting.

Consulting Project:

Client: Essence Corp.
Services Provided: Test and Reliability Consultant providing device lifetime characterization.

Consulting Project:

Client: Marvel Corp.
Services Provided: Test and Reliability Consultant providing important device lifetime characterization.

Consulting Project:

Client: Camtek
Services Provided: System Reliability Consultant providing models and accelerated tests

Consulting Project:

Client: Israel Aircraft Industries
Services Provided: Lecturer and Consultant

Consulting Project:

Client: Cypress Semiconductor
Services Provided: Laser processing consultation and trial expert witness

Consulting Project:

Client: Teradyne Corporation
Services Provided: Device and system reliability consultant

Consulting Project:

Client: Freescale Semiconductor
Services Provided: Device qualification and reliability testing and modeling

Consulting Project:

Client: GSI Lumonics
Services Provided: Improving laser cut and link technologies and expert witness

Professional Affiliations, Achievements & Awards

Laboratory and Programmatic Affiliations

- Laboratory for Reliability of Advanced Microelectronic Systems, Ariel University – current head
- Standards Institutions of Israel, Central Board 5800 for Electrical Standards
- Founder and Faculty Advisor: Israel Electronics Manufacturers Working Group on Reliability, ILTAM.

Joseph B. Bernstein, Ph.D. Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Awards and Honors

- Member of Israel Institute of Standards
- Expert Panelist and Invited Lecturer for GaN and SiC Power MOSFET, ISTFA 2023
- Excellence in Teaching Award, Ariel University 2021
- 32nd MIEL Serbia, Best Paper Award, 2021
- Tech-Connect Innovation Award 2018 (Through Ariel Scientific Innovations)
- Nanorun, distinguished lecturer and contributor, IRT-Saint Exupery, Feb. 2016
- Windows on Science researcher/lecturer, US Air Force, March 2015
- ChipEx 2014, best paper/lecturer award 2014
- Fulbright Senior Researcher. Lecturer, 2004 – 2005
- IEEE Senior Member, 2003

Teaching and Advising

- Courses Taught in the Last 5 Years
 - Reliability Prediction based on Multiple Accelerated Life Tests – Hobbs, IEEE, NASA, STMicro
 - Why Weibull, Why Not! – Hobbs, IEEE Summer School, Toulouse
 - VLSI Design – Ariel University (Advanced Undergraduate)
 - Reliability Engineering Fundamentals - Ariel University
 - Microelectronics Device Reliability – Ariel University
 - VLSI Analog (1 semester) and Digital VLSI (1 semester) Laboratories – Ariel University

<u>Project Title</u>	<u>Organization</u>	<u>PI or Co-PI</u>	<u>Funding Amount</u>	<u>Year</u>
Reliability of V-GaN	US ONR	PI	\$400,000	2023-2026
Microwave GaN Rel	MAFAT (Isr.)	PI	\$60,000	2023-2024
Power SOC	Israel Innov.	PI/2	\$400,000	2022-2025
Gate Drive for SiC	US ONR	PI/2	\$450,000	2021-2024
DSM/WBG Reliability	IRT Saint-Exupery	PI	\$200,000	2018-2020
GaN Class-D Amplifier	Kamin Israel	PI/2	\$200,000	2019-2021
GaN Microwave Device	Israel DOD	PI	\$150,000	2018-2022
GaN Device Reliability	ONR	PI	\$500,000	2015-2019
Wide Bandgap Device	AFOSR	PI	\$135,000	2015-2018
FPGA Reliability	USAF	PI	\$150,000	2014-2015
System Reliability	Magnetron Israel	PI	\$100,000	2012-2013
Power Electronic System Reliability	ONR	PI	\$200,000	2010-2011
Systems Reliability in Nanotechnology	ONR	PI	\$200,000	2009-2010
Methods to Account for Early Wear-out	AVSI consortium	PI	\$286,000	2007 - 2010
MIL HDBK 217 Replacement	Wyle Labs	PI	\$86,608	2007

Joseph B. Bernstein, Ph.D. Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Advanced Gate Dielectric Reliability	NIST	PI	\$69,965 (1st year)	2006-2009
JPL NASA Research Program	JPL	PI	\$65,000	2006-2007
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	\$180,000 (5th year)	2006
Ultra Thin Dielectric Metrology	NIST	PI	\$56,000	2005
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	\$210,000 (4th year)	2005
EDCOT Research Consortium	MAGNET (Tel-Aviv Univ.)	Co-PI (50%)	\$100,000	2004-2005
Laser programmable device design	NSA	PI	\$50,000	2004-2005
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	\$157,000 (3rd year)	2004
Power Device Reliability	ONR	Co-PI (60%)	\$150,000 per year	2004-2008
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	\$198,000 (2nd year)	2003
Laser programmable device design	NSA	PI	\$50,000	2002-2003
Place and Route for LPAA	Mission Research Corporation	PI	\$198,000	2002-2003
Laser MAKELINK development	MIPS (Matrics Corporation)	PI	\$77,000	2001-2002
Alternate Gate Dielectric Analysis	NIST	PI	\$150,000	2001-2005
Microelectronic Systems Reliability	AVSI (Aerospace Corporations)	PI	\$175,000 (1st year)	2002
Design and Layout of LPGA: Phase I.	BAE Systems Co.	PI	\$43,070	2000-2001
Wide band-gap power device reliability	ONR	Co-PI (50%)	\$314,804	2000 - 2003
Laser Process Development	DOD - NSA	PI	\$75,000	2000 - 2001
Thin Dielectric Metrology	NIST	PI	\$234,000	1999 - 2005
Laser Process Development	DOD - NSA	PI	\$146,680	1999 - 2000
Power Semiconductor	NIST	PI	\$42,300	1999 - 2000
Dielectric Metrology	NIST	PI	\$39,231	1999 - 2000
Laser Process Reliability	NASA / JPL	PI	\$54,080	1998
Metrology for Power Device Reliability	COMM - NIST	PI	\$6,000	1998
W Contact evaluation	DOD - NSA	PI	\$5,270	1998
Power Device Reliability	ONR	PI	\$150,000	1997 - 2000
Metal Cut Evaluation	General Scanning	PI	\$25,000	1997
Gate-Oxide Metrology	NIST	PI	\$124,330	1996 - 1999
Laser Restructuring / Evaluation	DOD - NSA	PI	\$200,000	1996 - 1997

Joseph B. Bernstein, Ph.D. Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Equipment Donated:

<u>Donated Item</u>	<u>Donating Agency</u>	<u>Value of Donation</u>
Cold/Hot Burn-In Ovens	Anonymous	\$200,000
Laser Timing Probe Microscope	Semicaps	\$3.5 Million
Laser Semiconductor Process Equipment	XRL Corporation	\$300,000
Laser Semiconductor Process Equipment	Electro Scientific Industries	\$700,000
Electromigration Test Equipment	Aetrium Corporation	\$150,000

Patents & Publications

<u>Patent</u>	<u>Date</u>	<u>Description</u>
11,996,845	9/15/2022	Power converter suitable for high frequencies
US202063039002P	15/06/2020	Control circuit for ring oscillator-based power controller
10,746,781	18/08/2020	Ring oscillator test circuit
PCT/IL2016/050476	05/01/2017	Enhancement mode only ring oscillator test circuit
US2014/0052392	02/20/2014	Solder joint life measurement for prognostics
US2015/0039244	02/15/2015	Failure Rate Estimation from Multiple Mechanisms
6,541,868	04/01/2003	Interconnecting Conductive Links
6,057,221	05/02/2000	Laser-Induced Cutting of Metal Interconnect
5,920,727	07/06/1999	Technique for Producing Interconnecting Conductive Links
5,920,789	07/06/1999	Technique for Producing Interconnecting Conductive Links
5,861,325	01/19/1999	Technique for Producing Interconnecting Conductive Links
5,585,602	12/17/1996	Structure for Providing One or More Conductive Paths

Publications

Book Authorship and Editorship

1. Joseph B. Bernstein, Alain Bensoussan, Emmanuel Bender, *Reliability Prediction for Microelectronics*, 8 chapters. Wiley, 2024, ISBN: 978-139421093-0
2. Joseph B. Bernstein, *Reliability Prediction from Burn-In Data Fit to Reliability Models*, Academic Press, 2014, ISBN: 978-0-12-800747-1
3. Joseph B. Bernstein et.al, *Physics-of-Failure Based Handbook of Microelectronic Systems*, Reliability Information Analysis Center, Utica, NY, 2008, ISBN-10: 1-933904-29-1.
4. Mark White, Joseph B. Bernstein, *Microelectronics Reliability: Physics-of-Failure Based Modeling and Lifetime Evaluation*, NASA JPL Publication, 2008.
5. Mark White, Joseph B. Bernstein, *Microelectronics Reliability Modeling and Lifetime Evaluation Handbook: Derating and Reliability Prediction Guidelines*, NASA JPL Publication, 2007.
6. Pecht, M., Bernstein, J.B., Searls, D., and Peckerar, M., *The Korean Electronics Industry*, CRC Press, 1997 and 2020
7. Hoang, H.H., Schutz, R., Bernstein, J.B., Vasquez, B., *Multi-level Interconnection: Issues that Impact Competitiveness*, Proceedings of SPIE 2090, 1993.

Book Chapters

1. Alain Bensoussan, Joseph B. Bernstein and Alain Bravix, Chapter 1, *Basic Reliability Tools for SHM Protocols*, in "Reliability and Physics-of-Healthy in Mechatronics, Volume 15 - Reliability of Multiphysical Systems Set." ISBN : 978-178-63-0881-8, November 2022.
2. Alain Bensoussan, Joseph B. Bernstein and Alain Bravix, Chapter 2, *Applied Engineering on Physics-of-Healthy and SHM of Microelectronic Equipment for Aeronautic, Space, Automotive and transport operations*, in "Reliability and Physics-of-Healthy in Mechatronics, Volume 15 - Reliability of Multiphysical Systems Set." ISBN : 978-178-63-0881-8, November 2022.
3. Joseph B. Bernstein, *Reliability Prediction Considering Multiple Failure Mechanisms*, Chapter in "System Reliability", INTECH Publication, 2017, ISBN 978-953-51-5532-4.
5. Bernstein, J.B., "Laser Link-Making," in *LIA Handbook of Laser Materials Processing*, Magnolia Publishing, 2001.
6. Stark, B., Bernstein, J.B., "Reliability Overview," *MEMS Reliability Assurance Guidelines for Space Applications*, NASA Publication, 1998.

Articles in Refereed Journals

1. E Bender, JB Bernstein, DS Boning, "Modern Trends in Microelectronics Packaging Reliability Testing," *Micromachines* 15 Vol. 3 (2024), pp. 398
2. A Chaturvedi, M Sarma, SK Chaturvedi, J Bernstein, "Performance assessment and RUL prediction of power converters under the multiple components degradation," *Microelectronics Reliability* Vol.144, (2023) pp. 144958
3. E Bender, JB Bernstein, DS Boning, "Mitigation of Thermal Stability Concerns in FinFET Devices," *Electronics* 11 (20), (2022) pp.3305
4. Clay Mayberry, Joseph Bernstein, "*Reliability and Survivability of Advanced Electronics Technologies*," AFRL Space Vehicles Directorate, (2022) 3/1
5. E Bender, JB Bernstein, "Microchip Health Monitoring System Using the FLL Circuit," *Sensors* vol.7, (2021) pp.2285
6. E Bender, JB Bernstein, A Bensoussan, "Reliability prediction of FinFET FPGAs by MTOL," *Microelectronics Reliability*, vol.114, (2020) pp.113809
7. S. Shaheen, G. Golan, M. Azoulay, J. B. Bernstein, "A COMPARATIVE STUDY OF RELIABILITY FOR FINFET," *Facta Universitatis, Series: Electronics and Energetics* Vol. 31, No 3, September 2018, pp. 343-366
8. G. Golan, M. Azoulay, T. Avraham, I. Kremenetsky, J. B. Bernstein, "An improved reliability model for Si and GaN power FET," *Microelectronics Reliability* Vol. 81 pp. 77-89 (2018)
9. J. B. Bernstein, A. Bensoussan, E. Bender, "Reliability Prediction with MTOL," *Microelectronics Reliability* Vol. 68 pp. 91-97 (2017)
10. J. B. Bernstein, M. Gabbay, O. Delly, "Reliability matrix solution to multiple mechanism prediction," *Microelectronics Reliability* pp. 2951-2955 (2014).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

11. Chung, Kuan-Jung, Martin Peckerar, and Joseph B. Bernstein. "*Design Optimization of Laser-Induced Microbridges for Low Resistance Interline Connections in ICs.*" *Microelectronic Engineering*, Vol. 103, Pages 70–75 (2013).
12. I. Gershman and J. B. Bernstein, "*Structural health monitoring of solder joints in QFN package,*" *Microelectronics Reliability*, Volume 52, Issue 12, Pages 3011–3016 (2012).
13. L. Yang and J. Bernstein, "*Reliability Evaluation and Modeling of High Density Electronic Packages,*" *Microelectronics International*, vol. 29, no. 1, pp. 15-21 (2012).
14. I. Gershman and J. B. Bernstein, "*Solder-Joint Quantitative Crack Analysis—Ohmic Resistance Approach,*" *IEEE Transaction on Components, Packaging and Manufacturing Technology*, vol. 2, no. 5, pp. 748 - 755 (2012).
15. L. Yang, R. Niu, J. Xie, B. Qian, B. Song, Q. Rong, J.B. Bernstein, "*Design-for-reliability implementation in microelectronics packaging development,*" *Microelectronics International*, vol. 28, no. 1, pp. 29-40 (2011).
16. B. Huang, M. Rodriguez, M. Li, J.B. Bernstein, C.S. Smidts, "*Hardware Error Likelihood Induced by the Operation of Software,*" *IEEE Trans. on Reliability*, vol. 60, no. 3, pp. 622-639 (2011).
17. Kuan-Jung Chung and J.B. Bernstein, "*Experimental investigation of the optimal laser-induced microbridges,*" *Precision Engineering*, vol. 34, no. 3, pp. 578-585 (2010).
18. B. Yan, J. Qin, J. Dai, Q. Fan, and J.B. Bernstein, "*Reliability Simulation and Circuit-Failure Analysis in Analog and Mixed-Signal Applications,*" *IEEE Trans. on Device and Mat. Rel.*, vol. 9, no. 3, pp. 339-347 (2009).
19. M. Gurfinkel, P. Livshits, A. Rozen, J.B. Bernstein, "*Local Oscillations of On-Die Supply Voltage-A Reliability Issue,*" *IEEE Trans. on Device and Mat. Rel.*, vol. 9, no. 3, pp. 476-482 (2009).
20. L. Yang, Joseph B. Bernstein, T. Koschmieder, "*Assessment of acceleration models used for BGA solder joint reliability studies,*" *Microelectronics Reliability* Vol. 49, pp. 1546–1554 (2009).
21. L. Yang, Joseph B. Bernstein, "*Failure rate estimation of known failure mechanisms of electronic packages,*" *Microelectronics Reliability* Vol. 49, pp. 1563-1572 (2009).
22. X. Li, J. Qin, and J.B. Bernstein, "*Compact Modeling of MOSFET Wearout Mechanisms for Circuit-Reliability Simulation,*" *IEEE Trans. on Device and Mat. Rel.*, vol. 8, no. 1, pp. 98-121 (2008).
23. M. Gurfinkel, H.D. Xiong, K.P. Cheung, J.S. Suehle, J.B. Bernstein, Y. Shapira, A.J. Lelis, D. Habersat, N. Goldsman, "*Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I-V Techniques,*" *IEEE Transactions on Electron Devices*, vol. 55, no.8, pp. 2004-12 (2008).
24. L. Yang, J.B. Bernstein, "*Reliability Study of High-Density EBGA Packages Using the Cu Metalized Silicon,*" *IEEE Transaction on Components and Packaging Technology*, vol. 31, no. 3, pp. 702-11 (2008).
25. M. Gurfinkel, J.C. Horst, J.S. Suehle, J.B. Bernstein, Y. Shapira, K.S. Matocha, G. Dunne, R.A. Beaupre, "*Time-Dependent Dielectric Breakdown of 4H-SiC/SiO₂ MOS Capacitors,*" *IEEE Trans. on Device and Mat. Rel.*, vol. 8, no. 4, pp. 635-641 (2008).
26. D. Heh, C.D. Young, G.A. Brown, P.Y. Hung, A. Diebold, E. Vogel, J.B. Bernstein, and G. Bersuker, "*Spatial Distributions of Trapping Centers in HfO₂/SiO₂ Gate Stack,*" *IEEE Transactions on Electron Devices*, vol. 54, no.6, pp. 1338-45 (2007).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

27. Joseph B. Bernstein, Moshe Gurfinkel, Xiaojun Li, Jörg Walters, Yoram Shapira and Michael Talmor, "*Electronic circuit reliability modeling*," Microelectronics Reliability, vol. 46, pp. 1957-1979 (2006).
28. Heh D, Young CD, Brown GA, Hung PY, Diebold A, Bersuker G, Vogel EM, Bernstein JB, "*Spatial distributions of trapping centers in HfO₂/SiO₂ gate stacks*," Applied Physics Letters, vol. 88, no.15, pp. 152907 (2006).
29. X. Li, J. Qin, B. Huang, X. Zhang, and J.B. Bernstein, "*SRAM Circuit Failure Modeling and Reliability Simulation with SPICE*," IEEE Trans. on Device and Mat. Rel., vol. 6, no. 2, pp.235-246 (2006).
30. X. Li, J. Qin, B. Huang, X. Zhang, and J.B. Bernstein, "*A New SPICE Reliability Simulation Method for Deep Submicron VLSI Circuits*," IEEE Trans. on Device and Mat. Rel., vol. 6, no. 2, pp. 247-257 (2006).
31. J.S. Suehle, B. Zhu, Y. Chen and J.B. Bernstein, "*Detailed study and projection of hard breakdown evolution in ultra-thin gate oxides*," Microelectronics Reliability, vol. 45, pp. 419-426 (2005).
32. J. Lee, W. Zhang, J.B Bernstein, "*Analysis of Energy Process Window of Laser Metal Pad Cut Link Structure*," IEEE Transactions on Semiconductor Manufacturing, vol. 16, no. 2, pp. 299-307 (2003).
33. L. Yang, C.K. King, J.B. Bernstein, "*Liquid Dispensing Encapsulation in Semiconductor Packaging*," Microelectronics International, vol. 20, no. 3, pp. 29-35 (2003).
34. D.W. Heh, E.M. Vogel, J.B. Bernstein, "*Impact of Substrate Hot Hole Injection on Ultra-thin Silicon-dioxide Breakdown*," Applied Physics Letters, vol. 82, no. 19, pp. 3242-3244 (2003).
35. J.S. Suehle, E.M. Vogel, P. Roitman, J.F. Conley Jr., A.H. Johnston, B. Wang, J.B. Bernstein, and C.E. Weintraub, "*Observation of Latent Reliability Degradation in Ultra-Thin Oxides after Heavy-Ion Irradiation*," Applied Physics letters, vol. 80, no. 7, pp. 1282-4 (18 Feb 2002).
36. E.M., Vogel, D. Heh, J.B. Bernstein, "*Interaction between low-energy electrons and defects created by hot holes in ultrathin Silicon Dioxide*," Applied Physics letters, vol. 80, no. 18, pp. 3343-5 (6 May 2002).
37. L.-S. Yang and J.B. Bernstein, "*Encapsulation Process Development for Flexible-Circuit Based Chip Scale Packages*," IEEE Trans. Electronics Packaging Manufacturing, vol. 25, no. 4, pp. 344-354 (October 2002).
38. L.-S. Yang, J.B. Bernstein and K.C. Leong, "*Effect of the Plasma Cleaning Process on Plastic Ball Grid Array Package Assembly Reliability*," IEEE Trans. Electronics Packaging Manufacturing, vol. 25, no. 2, pp. 91-99 (April 2002).
39. E.M., Vogel, D. Heh, J.B. Bernstein, J.S. Suehle, "*Impact of the Trapping of Anode Holes in Silicon Dioxide Breakdown*," IEEE Electron Device Letters, vol. 23, no. 11, pp. 667-669 (November 2002).
40. Yang, L., Bernstein, J.B., Chung, K, "*The Impact of Lead-free Soldering on Electronics packages*," Microelectronics International, vol. 18, no. 3, pp. 20-26 (2001).
41. Wang, B., Suehle J.S., Vogel E.M., Bernstein, J.B., "*Time-Dependent Breakdown of Ultra-thin SiO₂ Gate Dielectrics under Pulsed Biased Stress*," IEEE Electron Device Letters, vol. 22, no. 5, pp. 224-226 (2001).
42. Zhang, W., J.-H. Lee, Bernstein, J.B, "*Energy Effect of the Laser Induced Vertical Metallic Link*," IEEE Transactions on Semiconductor Manufacturing, vol. 14, no. 2, pp. 163-169 (2001).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

43. J.F. Conley Jr., J.S. Suehle, A.H. Johnston, B.Wang, T. Miyahara, E.M. Vogel, J.B. Bernstein, "*Heavy-Ion Induced soft breakdown of thin gate oxides*," IEEE Transactions on Nuclear Science, vol. 48, no. 6, pp. 1913-16 (Dec. 2001).
44. Shen, C.C., Hefner, A.R., Jr., Berning, D.W., Bernstein, J.B., "*Failure Dynamics of the IGBT During Turn-off For Unclamped Inductive Loading Conditions*," IEEE Transactions on Industry Applications, Vol. 36, no.2, pp.614-24 (2000).
45. Bernstein, J.B., Lee, J., Yang, G., Dahmas, T., "*Analysis of Laser Metal-Cut Energy Process Window*," IEEE Transactions on Semiconductor Manufacturing, vol.13, no. 2, pp. 228-34 (2000).
46. Vogel, E., Suehle, J.S., Edelstein, M.D., Wang, B., Chen, Y., Bernstein, J.B., "*Reliability of Ultra-thin Silicon Dioxide Under Combined Substrate Hot Electron and Constant Voltage Tunneling Stress*," IEEE Transactions on Electron Devices, vol. 47, no.6, pp.1183-91 (2000).
47. Lee, J., Zhang, W., Bernstein, J.B., "*Scalability Study of Laser-induced Vertical Make-link Structure*," IEEE Transactions on Semiconductor Manufacturing, vol. 13, no. 4, pp. 442-447 (2000).
48. Zhang, W., Lee, J.H., Chen, Y., Bernstein, J.B., Suehle, J.S., "*Reliability of laser-induced metallic vertical links*," IEEE Transactions on Advanced Packaging, vol. 22, no.4, pp. 614-19 (1999).
49. Bernstein, J.B., Hua, Y., Zhang, W., "*Laser energy limitation for buried metal cuts*," IEEE Electron Device Letters, vol. 19, no. 1, pp. 4-6 (1998).
50. Bernstein, J.B., Zhang, W., Nicholas, C.H., "*Laser formed metallic connections*," IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, vol. 21, no. 2, pp. 194-8 (1998).
51. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., Chaparala, P., "*A new technique for determining long-term TDDb acceleration parameters of thin gate oxides*," IEEE Electron Device Letters, vol. 19, no. 7, pp. 218-21 (1998).
52. Shen, Y-L, Suresh, S., Bernstein, J.B., "*Laser linking of metal interconnect: analysis and design considerations*," IEEE Transactions on Electron Devices, vol. 43, no. 3, pp. 402-10 (1996).
53. Rasera, R.L., Bernstein, J.B., "*Laser linking of metal interconnect: linking dynamics and failure analysis*," IEEE Transactions on Components, Packaging, and Manufacturing Technology, vol. 19, no. 4, pp. 554-61 (1996).
54. Bernstein, J.B., Ventura, T.M., Radomski, A.T., "*Laser induced microfracture leading to high density metal-to-metal connections*," Proceedings of the SPIE, The International Society for Optical Engineering, vol. 2335, pp. 165-76 (1995).
55. Bernstein, J.B., Colella, B.D., "*Laser-formed metallic connections employing a lateral link structure*," IEEE Transaction on Components, Packaging, and Manufacturing Technology, Part A, vol. 18, no. 3, pp.690-2 (1995).
56. Bernstein, J.B., Ventura, T.M., Radomski, A.T., "*Laser induced microfracture leading to high density metal-to-metal connections*," Proceedings of the SPIE, The International Society for Optical Engineering, vol. 2335, pp. 165-76 (1995).
57. Bernstein, J.B., Colella, B.D., "*Laser-formed metallic connections employing a lateral link structure*," IEEE Transaction on Components, Packaging, and Manufacturing Technology, Part A, vol. 18, no. 3, pp.690-2 (1995).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

58. Bernstein, J.B., Ventura, T.M., Radomski, A.I., "High-density laser linking of metal interconnect," IEEE Transactions on Components, Packaging and Manufacturing Technology, Part A, vol. 17, no.4, pp. 590-3 (1994).
59. Murguia, J.E., Bernstein, J.B., "Short-time failure of metal interconnect caused by current pulses," IEEE Electron Device Letters, vol. 14, no. 10, pp. 481-3 (1993).
60. Bernstein, J.B., "Improvements to the Electrically Stimulated Acoustic Wave method for analyzing bulk space charge," IEEE Transactions on Electrical Insulation, vol. 27, no.1, pp. 152-61 (1992).
61. Bernstein, J.B., Cohen, S.S., Wyatt, P.W., "Metal wire cutting by repeated application of low-power laser pulses," Review of Scientific Instruments, vol. 63, no. 6, pp. 3516-18 (1992).
62. Cohen, S.S., Bernstein, J.B., Wyatt, P.W., "The effect of multiple laser pulses on damage to thin metallic films," Journal of Applied Physics, vol. 71, no. 2, pp. 630-7 (1992).
63. Cohen, S.S., Bernstein, J.B., Wyatt, P.W., "Laser-induced line melting and cutting," IEEE Transactions on Electron Devices, vol. 39, no. 11, pp. 2480-5 (1992).
64. Bernstein, J.B., "Analysis of the electrically stimulated acoustic-wave method for observing space charge in semi-insulating films," Physical Review B (Condensed Matter), vol.44, no.19, pp. 10804-14 (1991).
65. Bernstein, J.B., Cooke, C.M., "Bulk space charge behavior in polymethylethacrylate under an imposed virtual cathode condition," IEEE Transactions on Electrical Insulation, vol. 26, no. 6, pp. 1080-6 (1991).
66. Bernstein, J.B., Cooke, C.M., "Electric poling behavior of polymethylmethacrylate," IEEE Transactions on Electrical Insulation, vol. 26, no. 6, pp. 1087-93 (1991).
67. Cohen, S.S., Wyatt, P.W., Bernstein, J.B., "Laser-induced melting of thin conducting films. II. Heat-dissipating substrates," IEEE Transactions on Electron Devices, vol.38, no.9 pp. 2051-7 (1991).
68. Cohen, S.S., Wyatt, P.W., Burns, J.A., Bernstein, J.B., "The mechanism of laser-induced vertical links," Journal of the Electrochemical Society, vol.138, no.10, pp. 3013-18 (1991).

Refereed Conference Proceedings

1. E Bender, JB Bernstein, DS Boning, "The Effects of Process Variations and BTI in Packaged FinFET Devices," IEEE International Reliability Physics Symposium (IRPS), 1-5 Monterey, CA (2023)
2. JB Bernstein, E Bender, A Bensoussan, "The Correct Hot Carrier Degradation Model," 2023 IEEE International Reliability Physics Symposium (IRPS), 1-5 Monterey, CA (2023)
3. E. Bender and J. B. Bernstein, "Self-heating Effects Measured in Fully Packaged FinFET Devices," 32ND INTERNATIONAL CONFERENCE ON MICROELECTRONICS, Serbia (2021)
4. I Aharn, Y Shalom, Y Dromi, A Shemaryahu, JB Bernstein, "GaN based Ring Oscillator PWM Generator," IEEE 12th Energy Conversion Congress & Exposition-Asia (ECCE-Asia 2021)
5. E Bender, JB Bernstein, A Bensoussan, "Reliability prediction of FinFET FPGAs by MTOL," Microelectronics Reliability, ESREF (2020)

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

6. I Aharon, M Sitbon, J Bernstein, “*Design Considerations for GaN Based Converters*,” 8th International Conference on Renewable Energy Research and Applications (ICRERA 2019)
7. G Golan, M Azoulay, J Bernstein, “*On the Ballistic Transport in Si Nano-Devices*,” *IEEE 31st International Conference on Microelectronics (MIEL)*, 55-58 (Sept. 2019)
8. M Musil, A Bensoussan, J Bernstein, F Coccetti, “Synopsis of Multiphysics Deep Sub-Micron Failure Rate Modeling Technique for CFR and EOL Prediction,” 2018 IEEE 13th Nanotechnology Materials and Devices Conference (NMDC) (Nov 2018)
9. G Golan, M Azoulay, S Shaheen, JB Bernstein, “A Novel Reliability Model For GaN Power FET,” 2018 IEEE International Conference on the Science of Electrical Engineering {Dec 2018}
10. J.B Bernstein, “Aerospace electronics reliability: Could it be predicted in a cost-effective fashion?,” IEEE Aerospace Conference, Colorado (Feb 2015)
11. J.B. Bernstein, O. Delly, M. Gabbay, “Combination of Multiple Mechanism for Post-Silicon Reliability Prediction,” ChipEx 2014, Tel Aviv (April 2014)
12. J.B. Bernstein, “Multiple Accelerated Test Matrix for Reliability Prediction,” SemIsrael Expo, Airport City, Israel (Nov 2013)
13. J.B. Bernstein and Y. Bot, “Physics Based Reliability Qualification,” IEEE-IRIC, (March 2013)
14. J.B. Bernstein, “Physics of Failure Based Reliability Qualification,” Proceedings of 19th International Conference of the Israel Society for Quality, pres. 7.1.4 Tel Aviv (October 2012).
15. Hava, F. Barmoav, C. Moulton, B. Kowalski, E. Ribak and J.B. Bernstein, “Prediction of Earpiece field failure rate based on accelerated Life test,” 2012 IEEE 27-th Convention, Eilat (2012).
16. J. Qin, M. White, J.B. Bernstein, “A Study of Scaling Effect on DRAM Reliability,” Annual Reliability and Maintainability Symposium (RAMS), Final Report, pp. 9C-4 (January 2011).
17. J. Qin, A. Hava, J.B. Bernstein, “FaRBS: a New PoF Based VLSI Reliability Prediction Method,” Annual Reliability and Maintainability Symposium (RAMS), pp. 9D-3 (January 2011).
18. M. Gurfinkel, P. Livshits, A. Rozen, Y. Fefer, J.B. Bernstein, Y. Shapira, “Supply signal fluctuations due to chip power grid resonance — a new reliability concern,” Proc. of the IEEE International Reliability Physics Symposium, (April-May 2008).
19. J. Qin, B. Yan, Y. Shoshany, R. Druker, H. Rahamim, H. Marom, J.B. Bernstein, “Study of Transistor and Product NBTI Lifetime Distributions (A),” International Integrated Reliability Workshop (IIRW) Final Report, pp. 1-16 (October 2008).
20. J. Qin, B. Yan, Y. Shoshany, R. Druker, H. Rahamim, H. Marom, J.B. Bernstein, “Study of Transistor and Product NBTI Lifetime Distributions (B),” International Integrated Reliability Workshop (IIRW) Final Report, pp. 64-67 (October 2008).
21. B. Yan, J. Qin, J. Dai, Q. Fan, J.B. Bernstein, “Reliability Simulation and Design Consideration of High Speed ADC Circuits.” International Integrated Reliability Workshop (IIRW) Final Report, pp. 125-128 (October 2008).
22. L. Condra, J. Qin and J.B. Bernstein, “State of the Art Semiconductor Devices in Future

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

Aerospace Systems,” Proceedings of the FAA/NASA/DoD Joint Council on Aging Aircraft Conference, Palm Springs, CA (April 2007).

23. M. Gurfinkel, J. Suehle, J.B. Bernstein, Yoram Shapira, A.J. Lelis, D. Habersat, N. Goldsman, “Ultra-fast Characterization of Transient Gate Oxide Trapping in SiC MOSFETs,” Proc. of the IEEE International Reliability Physics Symposium 2007.
24. J. Qin, X. Li, J.B. Bernstein, “SRAM Stability Analysis Considering Gate Oxide SBD, NBTI and HCI,” 2007 International Integrated Reliability Workshop (IIRW) Final Report, 2.2, (October 2007).
25. M. Gurfinkel, et. al., “Characterization of Interface and Bulk Oxide Traps in SiC MOSFETs with Epitaxially grown and implanted channels,” 2007 International Integrated Reliability Workshop (IIRW) Final Report, 8.3 (October 2007).
26. L. Yang, J.B. Bernstein, D. Gajewski and J. Walls, “Predictive Reliability Assessment and Failure Rate Modeling for Electronic Packages,” IMAPS 40th International Symposium on Microelectronics, Final Report, WA5 (November 2007).
27. M. Gurfinkel, J. Suehle, J.B. Bernstein, Y. Shapira, A.J. Lelis, D. Habersat, N. Goldsman, “Ultra-Fast Measurement of V_{th} Instability in SiC MOSFETs due to Positive and Negative Constant Bias Stress,” 2006 International Integrated Reliability Workshop (IIRW) Final Report, pp. 49-53 (October 2006).
28. M. White, C. Vu, C. Nguyen, R. Ruiz, Y. Chen, J.B. Bernstein, “Product Reliability Trends, Derating Considerations and Failure Mechanisms with Scaled CMOS,” 2006 International Integrated Reliability Workshop (IIRW) Final Report, pp. 156-159 (October 2006).
29. J. Qin, J.B. Bernstein, “Non-Arrhenius Temperature Acceleration and Stress-Dependent Voltage Acceleration for Semiconductor Devices Involving Multiple Failure Mechanisms,” 2006 International Integrated Reliability Workshop (IIRW) Final Report, pp. 93-97 (October 2006).
30. Bernstein, J. B., “Reliability Qualification at the Maryland-Israel Center for Product Realization,” Proceedings of 16th International Conference of the Israel Society for Quality, pp. 9.2.01 Tel Aviv (November 2006).
31. M. Gurfinkel, J. Suehle, J.B. Bernstein, Y. Shapira, “Enhanced Gate Induced Leakage Current in HfO₂ MOSFETs due to Remote Interface Trap-Assisted Tunneling,” 2006 International Electron Devices Meeting (IEDM) technical digest, pp. 755-758, (Dec 2006).
32. Xiaojun Li; Walter, J.D.; Bernstein, J.B.; “Simulating and Improving Microelectronic Device Reliability by Scaling Voltage and Temperature,” Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium, pp.496 - 502 (March 2005).
33. Xiaojun Li; Huang, B.; Qin, J.; Zhang, X.; Talmor, M.; Gur, Z.; Bernstein, J.B.; “Deep Submicron CMOS Integrated Circuit Reliability Simulation with SPICE,” Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on, pp. 382 - 389 (March 2005).
34. Zhu, B.; Suehle, I.S.; Vogel, E.; Bernstein, J.B.; “The contribution of HFO₂ bulk oxide traps to dynamic NBTI in pMOSFETs,” IEEE International Reliability Physics Symposium 2005 Proceedings, pp. 533 – 537 (April 2005).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

35. Kuan-Jung Chung; Bernstein, J.B.; Ji Luo; Tuchman, J.A.; Ma, Z.K.; "Experimental Study for Low Resistance Interline Connections Using Pulsed Laser Techniques," Quantum Electronics and Laser Science 2005, Conference Volume 3, pp.1564 - 1566 (May 2005).
36. Bing Huang; Xiaojun Li; Ming Li; Bernstein, J.; Smidts, "Study of the impact of hardware fault on software reliability," Proceedings. 16th IEEE International Symposium on Software Reliability Engineering. Chicago, IL, USA (Nov. 2005).
37. B. Zhu, J.S. Suehle, J.B. Bernstein, "Mechanism for reduced NBTI effect under pulsed bias stress conditions," Proceedings of Integrated Reliability Workshop, Phoenix (Arizona 2004).
38. J.S. Suehle, B. Zhu, Y. Chen, J.B. Bernstein, "Acceleration factors and mechanistic study of progressive breakdown in small area ultra-thin gate oxides," Proceedings of Integrated Reliability Workshop, Phoenix (Arizona 2004).
39. Ji Luo; Bernstein, J.B.; Tuchman, J.A.; Hu Huang; "A high performance radiation-hard field programmable analog array." Proceedings. 5th International Symposium on Quality Electronic Design. p. 522-7. (Los Alamitos, CA, 2004).
40. Hu Huang, Joseph B. Bernstein, Martin Peckerar, Ji Luo; "Combined Channel Segmentation and Buffer Insertion for Routability and Performance Improvement of Field Programmable Analog Arrays," Proceedings of the IEEE International Conference on Computer Design (October 2004).
41. X. Zhang, N. Goldsman, J.B. Bernstein, J.M. McGarrity, "Numerical and Experimental Characterization of 4H-SiC Schottky Diodes," Proceedings of IEEE International Semiconductor Device Research Symposium, p. 120-1 (2003).
42. M. White, M. Cooper, Y. Chen, J. Bernstein, "Impact of Junction Temperature on Microelectronic Device Reliability and Considerations for Space Applications," Proceedings of Integrated Reliability Workshop, p. 133-6 (Nevada 2003).
43. B. Zhu, J.B. Bernstein, J. Suehle, "Negative bias temperature instability of deep sub-micron p-MOSFETs under pulsed bias stress," Proceedings of Integrated Reliability Workshop, pp. 125-9 (Nevada 2003).
44. Y. Chen, D. Nguyen, S. Guertin, J.B. Bernstein, M. White, R. Menke, S. Kayali, "A Reliability Evaluation Methodology for Memory Chips for Space Applications when Sample Size is Small," Proceedings of Integrated Reliability Workshop, Lake Tahoe (Nevada 2003).
45. Ji Luo, Kuan-Jung Chung, Hu Huang, J.B. Bernstein, "Temperature Dependence of R(on,sp) in Silicon Carbide and GaAs Schottky diodes," Proceedings of IEEE International Reliability Physics Symposium, 40th annual (New Jersey 2002).
46. Zhuo Gao, Ji Luo, Hu Huang, Wei Zhang, J.B. Bernstein, "Reliable laser programmable gate array technology," Proceedings International Symposium on Quality Electronic Design, p. 252-6, Los Alamitos (California 2002).
47. D. Heh, J.B. Bernstein, E.M. Vogel, "Defect generation in ultra-thin oxide over large fluence ranges," Proceedings of Integrated Reliability Workshop, Lake Tahoe (Nevada 2002).
48. Z. Gao, J. Luo, Hu Huang, W. Zhang, J.B. Bernstein, "Reliable laser programmable gate array technology," Proceedings of International Symposium on Quality Electronic Design, pp. 252-256 (California 2002).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

49. J.S. Suehle, et.al ... J.B. Bernstein, "Challenges of high-k gate dielectrics for future MOS devices," 6th International Symposium on Plasma and Process Induced Damage, pp. 90-93 (California 2001).
50. B. Wang, J.B. Bernstein, "Latent Reliability Degradation of Ultra-Thin Oxides after Heavy Ion and Gamma Irradiation," Proceedings of Integrated Reliability Workshop (California 2001).
51. Bernstein, J.B. and Lee, J, "A Laser Formed MakeLink for Customization and Repair," Proceedings of IEEE International Symposium on Semiconductor Manufacturing, pp. 347-350 (California 2001).
52. Ji Luo, K. Chung, Hu Huang, J.B. Bernstein, "Comparison of Silicon Carbide Schottky diodes," Proceedings of 2001 GaAs Reliability Workshop (Virginia 2001).
53. Suehle, J.S., Vogel, E., Wang, B., Bernstein, J.B., "Temperature Dependence of Soft Breakdown and Wear-Out in Sub-3 nm SiO₂ Films," International Reliability Physics Symposium - Conference Proceedings, pp. 33-9 (California 2000).
54. E. M. Vogel, M. D. Edelstein, C. A. Richter, N. V. Nguyen, I. Levin, D. L. Kaiser, H. Wu, and J. Bernstein, "Issues in High- κ Gate Dielectrics for Future MOS Devices," Proceedings of IEEE Microelectronics Reliability Qualification Workshop (California 2000).
55. B. Wang, J. Suehle, E.M. Vogel, J.B. Bernstein, "The Effect of Stress Interruption and pulsed bias stress on Ultra-Thin Gate Dielectric Reliability," Proceedings of Integrated Reliability Workshop (California 2000).
56. J. Lee, G. Zhuo and J.B. Bernstein, "Laser Programmable Multichip Module using Vertical Make-link," Proceedings of the IEEE Electronic Components and Technology Conference, pp 932-936 (Nevada 2000).
57. Vogel, E., Suehle, J.S., Edelstein, M.D., Wang, B., Chen, Y., Bernstein, J.B., "Degradation of Ultra-thin SiO₂ Under Combined Substrate Hot Electron and Tunneling Stress," Semiconductor Interface Specialists Conference, (California 2000).
58. Shen, C.C., Kefner, A.R., Jr., Berning, D.W., Bernstein, J.B., "Failure dynamics of the IGBT during turn-off for unclamped inductive loading conditions," Conference Record of 1998 IEEE Industry Applications Conference, p. 3, vol. xxx+2410, 831-9, vol. 2 (New York 1999).
59. Zhang, W., Bernstein, J.B., "Electromigration simulation under DC/AC stresses considering microstructure," Proceedings of the IEEE 1999 International Interconnect Technology Conference, pp. 295, 41-3 (California 1999).
60. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., Chaparala, P., "The correlation of highly accelerated Q_{bd} tests to TDDB life tests for ultra-thin gate oxides," 1998 IEEE International Reliability Physics Symposium Proceedings. 36th Annual, pp. 87-91 (California 1998).
61. Bernstein, J.B., Zhang, W., Nicholas, C.H., "Laser formed connections for programmable wiring," Proceedings of the IEEE 1998 Custom Integrated Circuits Conference, pp. 608, 163-5 (California 1998).
62. Bernstein, J.B., Zhang, W., Nicholas, C.H., "Laser programmable metallic vias," Proceedings of the IEEE 1998 International Interconnect Technology Conference, pp. 304, 205-7 (New York 1998).
63. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., Chaparala, P., "The correlation of highly accelerated Q_{bd} tests to TDDB life tests for ultra-thin gate oxides," 1998 IEEE International Reliability Physics Symposium Proceedings. 36th Annual, pp. vii+421, 87-91 (Nevada 1998).

Joseph B. Bernstein, Ph.D.
Curriculum Vitae

Professor of Engineering
Dept. of Electrical Engineering
Ariel University, Israel
+972 (0)52-575-9301
joeybern@gmail.com

64. Chen, Y., Suehle, J.S., Shen, C.C., Bernstein, J.B., Messick, C., "A New Technique to Extract TDDDB Acceleration Parameters from Fast Qbd Tests," Proceedings of International Integrated Reliability Workshop, pp. 67-69, (Nevada 1997).
65. Bernstein, J.B., "Laser Formed Lateral Metallic Connections," Proceedings of the Second International Conference on Beam Processing of Advanced Materials, pp. 101-104 (Ohio 1995).
66. Bernstein, J.B., "Dielectric fracture leading to metallic connections employing a lateral link structure," Thin Films: Stresses and Mechanical Properties V. Symposium, MRS pp. 833-7 (Massachusetts 1994).
67. Bernstein, J.B., Ventura, T.M., Radomski, A.T., "Laser induced microfracture leading to high density metal-to-metal connections," Proceedings of the SPIE, The International Society for Optical Engineering, pp. 165-76 (Texas 1994).
68. Bernstein, J.B., Gleason, E.F., Wetsel, A.E., Liu, E.Z., Wyatt, P.W., "Anomalous Behavior of Semi-insulating Silicon Rich Amorphous Silicon Nitride," Amorphous Insulating Thin Films Symposium, MRS pp. 113-18 (Massachusetts 1993).
69. Bernstein, J.B., Gleason, E.F., Wyatt, P.W., "A thermally stable silicon rich amorphous silicon nitride alloy for electronic device applications," Amorphous Silicon Technology Symposium, MRS pp. 667-72 (California 1992).
70. Bernstein, J.B., Gleason, E.F., Wyatt, P.W., "High density metal cross-point laser linking," International Conference on Wafer Scale Integration Proceedings, pp. 176-81 (California 1992).
71. Bernstein, J.B., Cohen, S.S., Wyatt, P.W., "Fatigue of aluminum films leading to melting by multiple laser pulses," Phase Formation and Modification by Beam-Solid Interactions Symposium, MRS pp. 589-93 (Boston 1991).
72. Cooke, C.M., Wright, K.A., Takasu, N., Bernstein, J.B., Gollin, E., "Calibration of Volume Charge Measurements By Use of Electron Beam Implantation," 1989 Annual Report. Conference on Electrical Insulation and Dielectric Phenomena, pp. 508, 435-41 (Virginia 1989).
73. Bernstein, J.B., Bahl, S., Schlecht, M.F., "A Low Capacitance Power MOSFET with an Integral Gate Driver," Proceeding of the 18th Annual IEEE Power Electronics Specialists Conference, PESC vol. 87, pp. 704, 61-8 (Virginia 1987).