

EXHIBIT 17

EXHIBIT 17

**REPRESENTATIVE CLAIM CHART ILLUSTRATING INFRINGEMENT OF U.S. PATENT NO. 8,264,003
BY INNOSCIENCE'S ISG3201 DEVICE**

The following claim chart compares claims 1 and 10 of U.S. Patent No. 8,264,003 (“the ‘003 Patent”) to the ‘003 Patent Accused Products, e.g. Innoscience’s GaN power products that include a transistor circuit having a transistor in a merged cascode geometry and with a source-connected second gate that includes a field plate. Below, Innoscience’s ISG3201 is charted as a representative ‘003 Patent Accused Product.

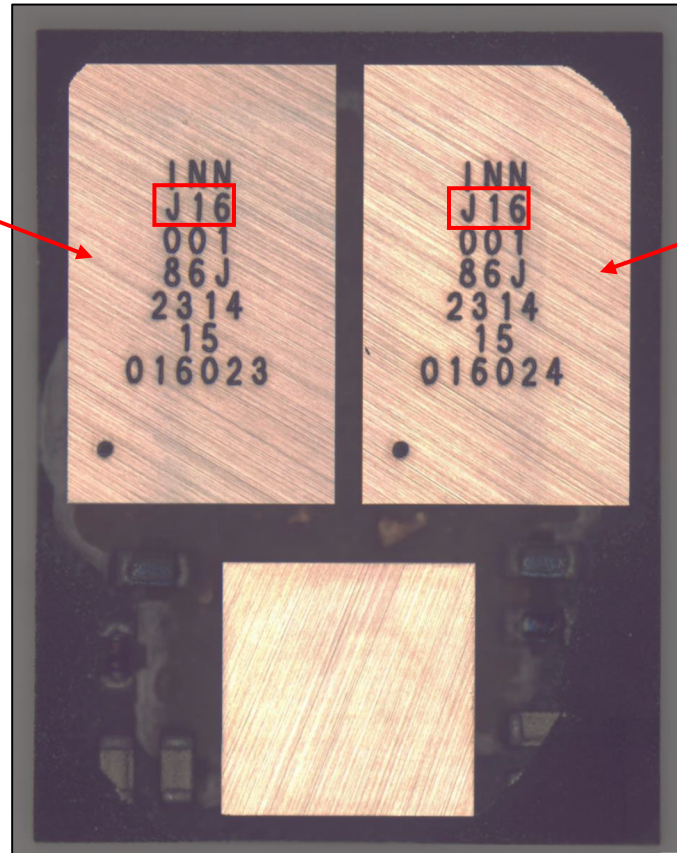
'003 Patent Claim 1	Innoscience’s GaN Power Products (e.g. ISG3201)
[1PRE] A merged cascode transistor circuit comprising:	To the extent the preamble is limiting, the preamble is met. Innoscience’s ISG3201 is a co-packaged product that integrates two 100V enhancement mode GaN devices with a half-bridge gate driver. 3. General description The ISG3201 is a 100V Copak product in Innoscience's SolidGaN family. It integrates <u>two 100V enhancement mode GaN devices</u> with a 100V half-bridge gate driver. ISG3201 employs bootstrap technique for high-side driver voltage and can operate up to 100V. The <i>See Ex. 31 at 1 (ISG3201 Datasheet, annotations added)</i>

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	(Photographs of top side (left panel) and bottom side (right panel) of ISG3201) In particular, the two 100V enhancement mode GaN devices included in ISG3201 are Innoscience's INN100W032A power transistors, as indicated by the code "J16" in their die markings, which is the product code for INN100W032A according to the INN100W032A datasheet.

'003 Patent Claim 1

Innoscience's GaN Power Products (e.g. ISG3201)

INN100W032A



INN100W032A

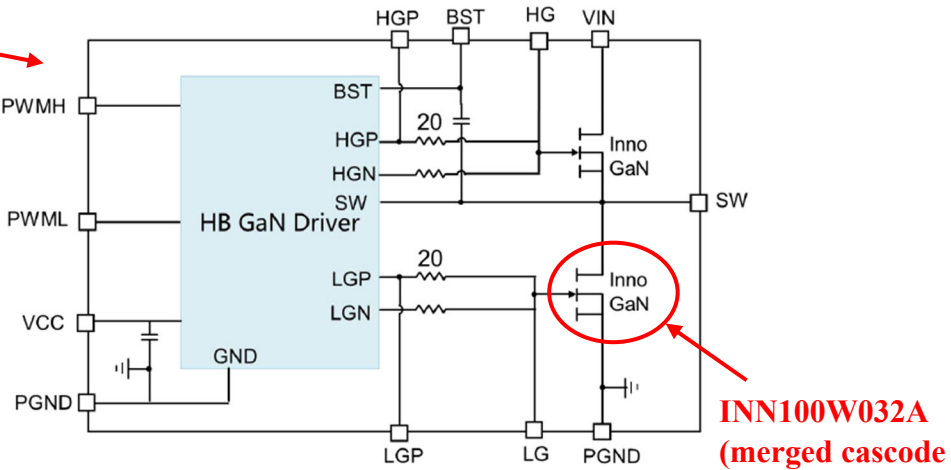
(Plan-view die photograph of a decapped ISG3201, annotations added)

Table 3 **Ordering information**

Type/Ordering Code	Package	Product Code
INN100W032A	WLCSP 3.5x2.13	J16

See Ex. 21 at 1 (INN100W032A Datasheet, annotation added)

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)																							
	Marking Reference: I N N X X X X X X X X X Y Y W W X X X X X Y Y Y Die Orientation Dot Gate Position <table><tr><th>Row</th><th>Description</th><th>Example</th></tr><tr><td>Row1</td><td>Company name</td><td>INN</td></tr><tr><td>Row2</td><td>Product code</td><td>XXX</td></tr><tr><td>Row3</td><td rowspan="2">Lot Code</td><td>XXX</td></tr><tr><td>Row4</td><td>XXX</td></tr><tr><td>Row5</td><td>Date code</td><td>YYWW</td></tr><tr><td>Row6</td><td>Wafer ID</td><td>XX</td></tr><tr><td>Row7</td><td>Location ID</td><td>XXXYYY</td></tr></table> See Ex. 21 at 12 (INN100W032A Datasheet, annotations added to illustrate the position of the product code in the die marking) As discussed below in limitation [1C], Innoscience's INN100W032A is a merged cascode transistor. Therefore ISG3201, which incorporates a merged cascode transistor, is a merged cascode transistor circuit.	Row	Description	Example	Row1	Company name	INN	Row2	Product code	XXX	Row3	Lot Code	XXX	Row4	XXX	Row5	Date code	YYWW	Row6	Wafer ID	XX	Row7	Location ID	XXXYYY
Row	Description	Example																						
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'003 Patent Claim 1	Innoscence's GaN Power Products (e.g. ISG3201)
	13. Block Diagram Block Diagram of ISG3201 is shown as Figure 1. A half-bridge GaN driver and two 100V GaN HEMTs are integrated. Besides, V_{cc} decoupling capacitor, Bootstrap capacitor, internal 20Ω turn-on resistor for both GaN HEMTs are also integrated. Turn-on speed can be adjusted by an optional resistor between HGP(LGP) pin and HG(LG) pin for top (bottom) GaN HEMT. Merged cascode transistor circuit  Figure 1. Block diagram of ISG3201 INN100W032A (merged cascode transistor) See Ex. 31 at 9 (ISG3201 Datasheet, annotations added)
[1A] an input voltage signal source having an input voltage signal;	Innoscence's ISG3201 meets this limitation. ISG3201 comprises a driver, which is an input voltage signal source having an input voltage signal V_{LG} that is applied at the low side gate terminal (LG) of the low side INN100W032A transistor.

13. Block Diagram

Block Diagram of ISG3201 is shown as Figure 1. A half-bridge GaN driver and two 100V GaN HEMTs are integrated. Besides, Vcc decoupling capacitor, Bootstrap capacitor, internal 20Ω turn-on resistor for both GaN HEMTs are also integrated. Turn-on speed can be adjusted by an optional resistor between HGP(LGP) pin and HG(LG) pin for top (bottom) GaN HEMT.

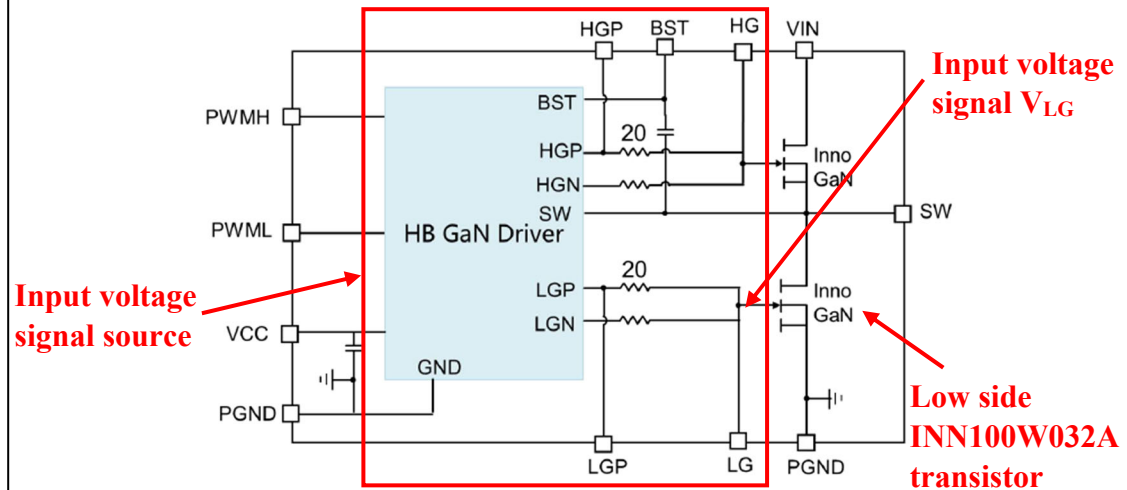


Figure 1. Block diagram of ISG3201

See Ex. 31 at 9 (ISG3201 Datasheet, annotations added)

5. Absolute maximum ratings

at $T_j = 25^\circ\text{C}$ unless otherwise specified.

All voltages are with respect to PGND pin.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscence sales office.

Table 1 Absolute maximum ratings at $T_j = 25^\circ\text{C}$

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
V_{in}	Input Voltage Supply, V_{in} to GND	100	V
I_D	Continuous current for internal GaN HEMT	60 (*)	A
	Pulsed (25°C , $T_{Pulse} = 100\ \mu\text{s}$)	230	A
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	$^\circ\text{C}$
$V_{CC(DC)}$	Supply Voltage (DC)	-0.3 to 6.0	V
$V_{CC(25ns)}$	Supply Voltage (25ns)	-0.3 to 8.0	V
$V_{BST-SW(DC)}$	BST to SW Voltage (DC)	-0.3 to 6.0	V
$V_{BST-SW(25ns)}$	BST to SW Voltage (25ns)	-0.3 to 8.0	V
$V_{SW(DC)}$	SW pin Voltage	-0.3 to 105	V
$V_{SW(25ns)}$	SW pin Voltage (25ns)	-5V to 108	V
$V_{BST-PGND}$	BST to PGND Voltage	-0.3 to $V_{SW}+6.0$	V
V_{HGP}, V_{HG}	HGP, HG pin Voltage	$V_{SW}-0.3$ to $V_{BST}+0.3$	V
V_{LGP}, V_{LG}	LGP, LG pin Voltage	-0.3 to 6.0	V
PWMH, PWML	PWMH, PWML pin Voltage	-0.3 to 6.0	V

Input
voltage
signal

See Ex. 31 at 2 (ISG3201 Datasheet, annotations added)

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[1B] a constant voltage source having a predetermined constant voltage;	Innoscience's ISG3201 meets this limitation. ISG3201 comprises a power ground (PGND), which is a constant voltage source having a voltage at a ground reference level (i.e. a predetermined constant voltage).																																				

13. Block Diagram

Block Diagram of ISG3201 is shown as Figure 1. A half-bridge GaN driver and two 100V GaN HEMTs are integrated. Besides, Vcc decoupling capacitor, Bootstrap capacitor, internal 20Ω turn-on resistor for both GaN HEMTs are also integrated. Turn-on speed can be adjusted by an optional resistor between HGP(LGP) pin and HG(LG) pin for top (bottom) GaN HEMT.

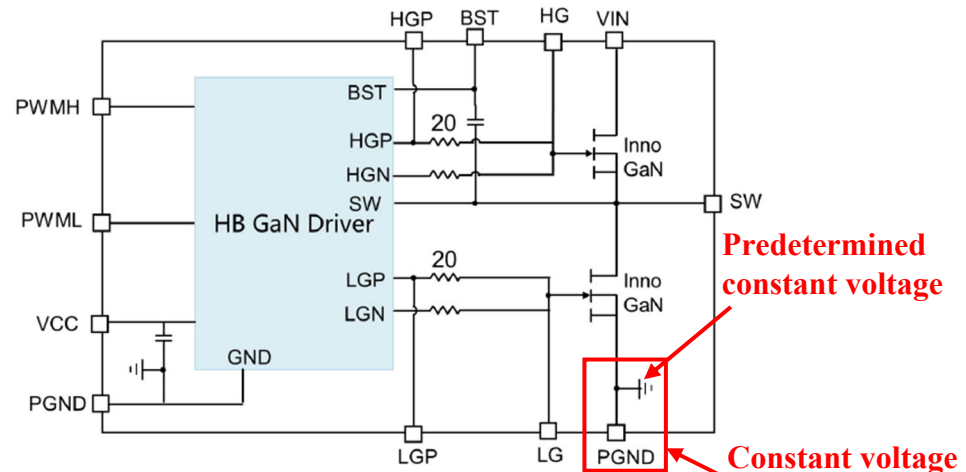


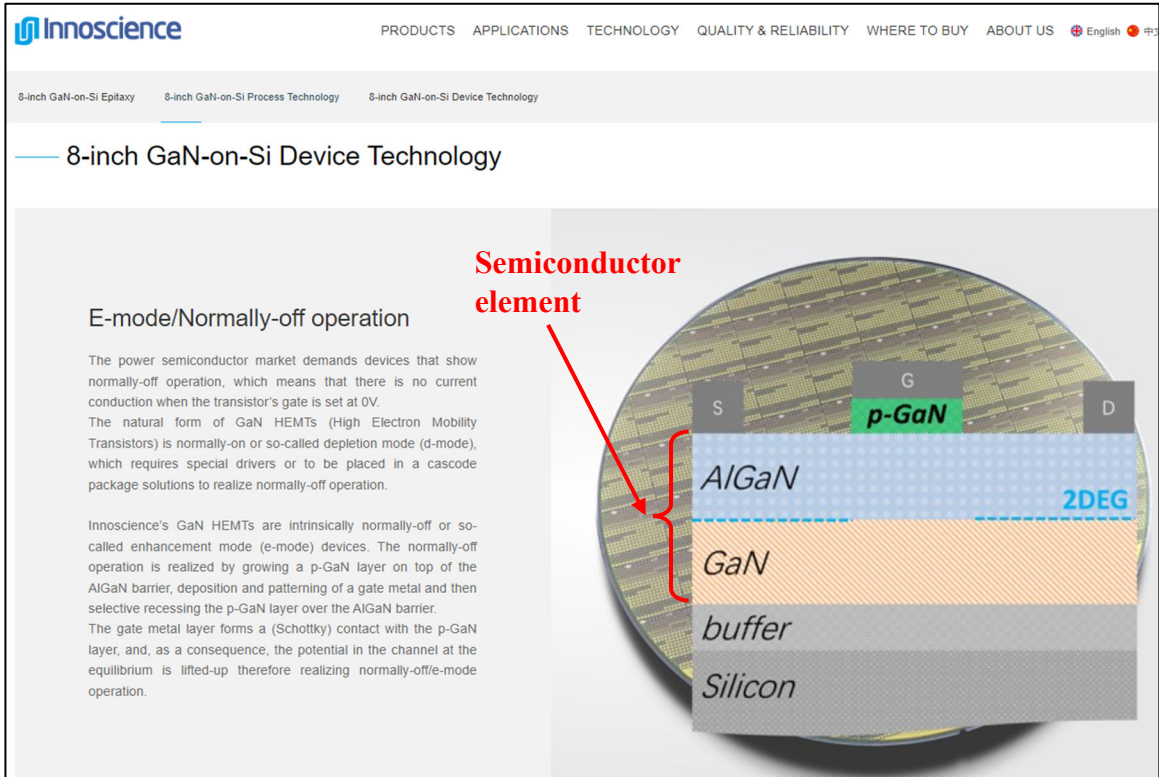
Figure 1. Block diagram of ISG3201

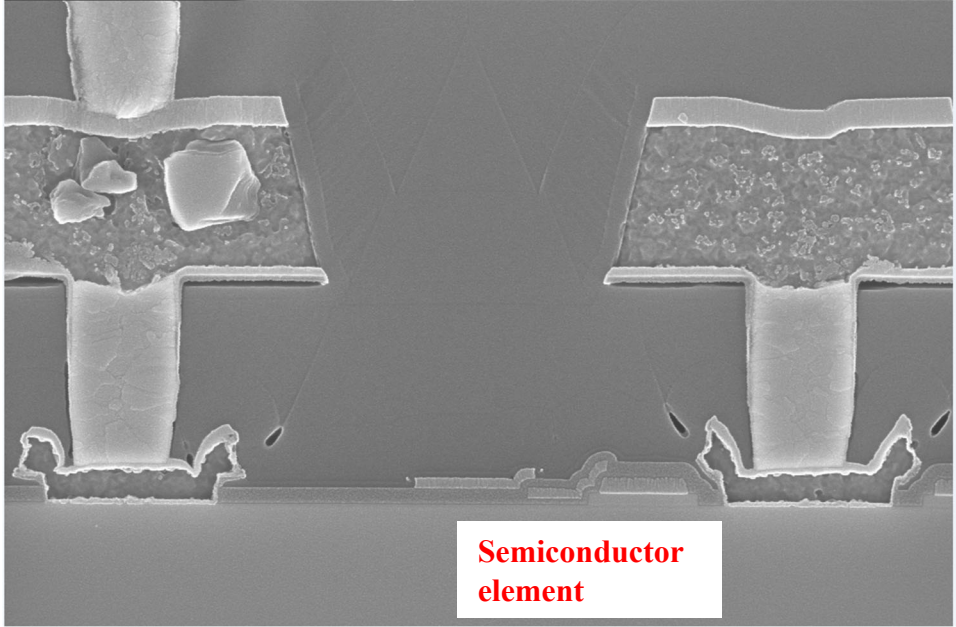
See Ex. 31 at 9 (ISG3201 Datasheet, annotations added)

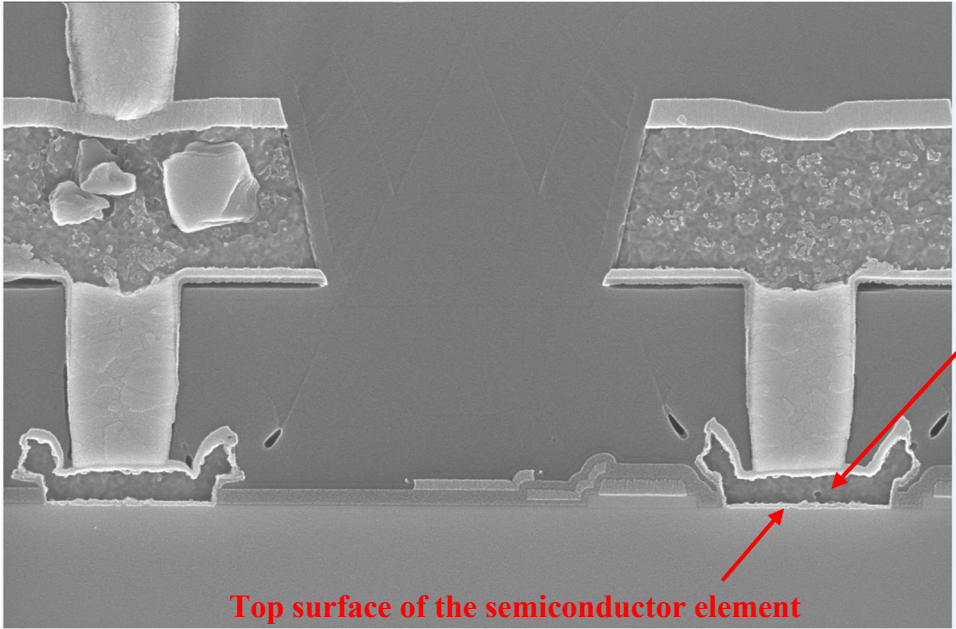
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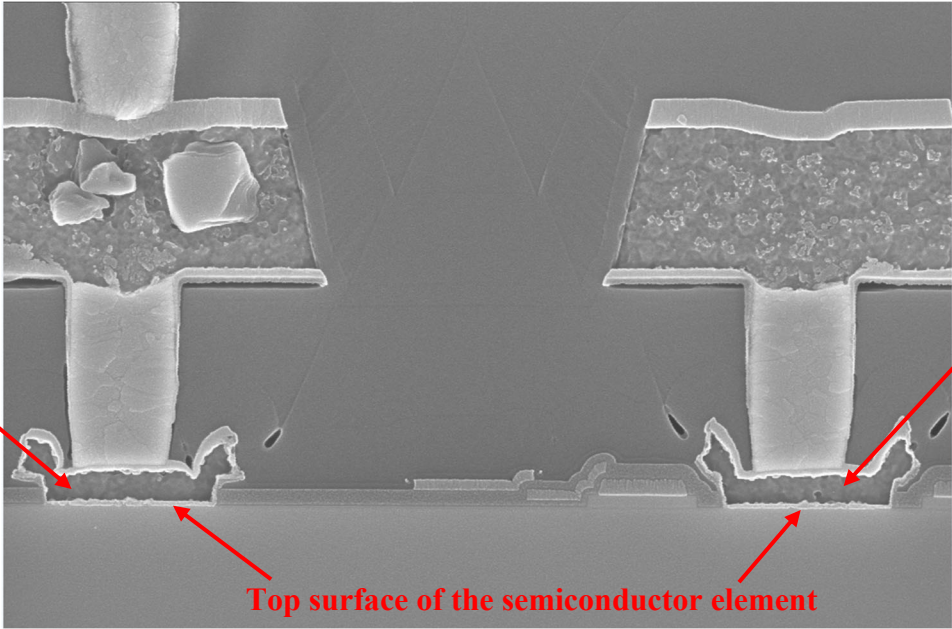
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[1C] a merged cascode transistor comprising:	The low side INN100W032A transistor in ISG3201 meets this limitation. The datasheet for Innoscience's INN100W032A product shows that it is an enhancement-mode GaN power transistor, which is a transistor.																																																																			

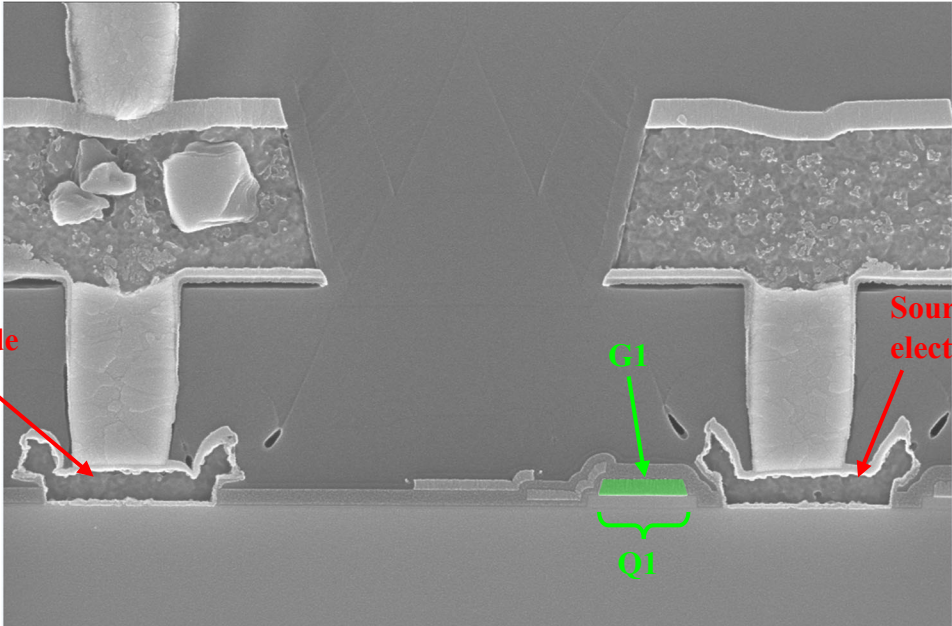
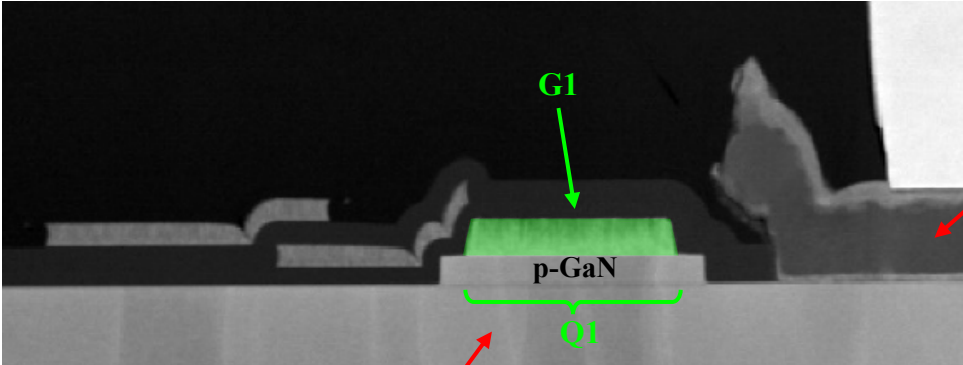
'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	The low side INN100W032A transistor is a merged cascode transistor at least because as discussed below in limitations [1C8] and [1C9], INN100W032A comprises an enhancement mode transistor and a depletion mode transistor, with a drain region of the enhancement mode transistor merged with a source region of the depletion mode transistor. See Ex. 21 at 1 (INN100W032A Datasheet, annotations added)
[1C1] a semiconductor element;	The low side INN100W032A transistor in ISG3201 meets this limitation.

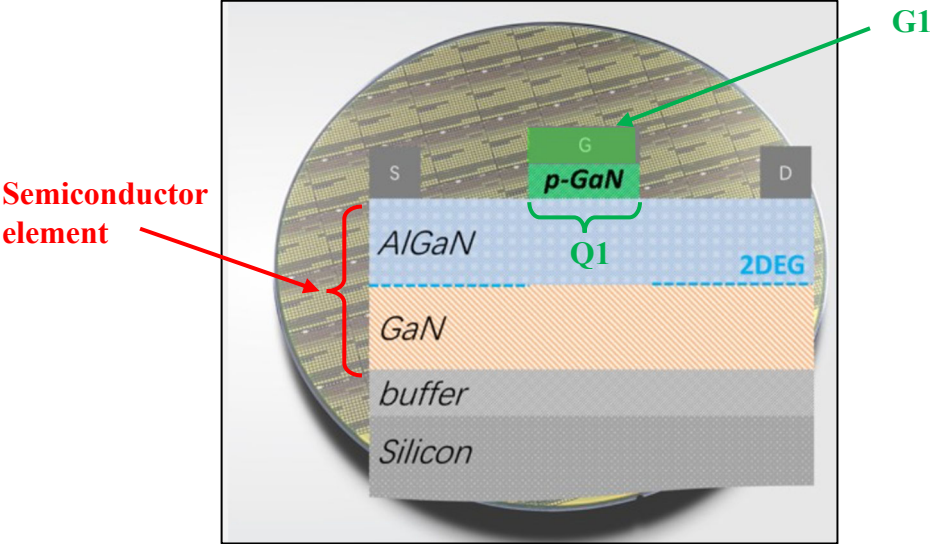
'003 Patent Claim 1	Innoscence's GaN Power Products (e.g. ISG3201)
	As illustrated on Innoscence's website, the INN100W032A transistor product is a GaN-on-Si device that includes an AlGaN layer and a GaN layer with a 2-dimensional electron gas (2DEG) at the interface between the AlGaN and GaN layers, which collectively constitute a semiconductor element.  E-mode/Normally-off operation The power semiconductor market demands devices that show normally-off operation, which means that there is no current conduction when the transistor's gate is set at 0V. The natural form of GaN HEMTs (High Electron Mobility Transistors) is normally-on or so-called depletion mode (d-mode), which requires special drivers or to be placed in a cascode package solutions to realize normally-off operation. Innoscence's GaN HEMTs are intrinsically normally-off or so-called enhancement mode (e-mode) devices. The normally-off operation is realized by growing a p-GaN layer on top of the AlGaN barrier, deposition and patterning of a gate metal and then selective recessing the p-GaN layer over the AlGaN barrier. The gate metal layer forms a (Schottky) contact with the p-GaN layer, and, as a consequence, the potential in the channel at the equilibrium is lifted-up therefore realizing normally-off/e-mode operation. See Ex. 19 at 4 (https://www.innoscence.com/site/technology, annotations added) The semiconductor element is also shown in a cross-sectional scanning electron microscopy (SEM) image of the INN100W032A product, as shown below.

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	 (Cross-sectional view SEM image of INN100W032A, annotations added)
[1C2] a source electrode electrically connected to a top surface of the semiconductor element;	The low side INN100W032A transistor in ISG3201 meets this limitation. As shown in the cross-sectional view SEM image, INN100W032A comprises a source electrode electrically connected to a top surface of the semiconductor element.

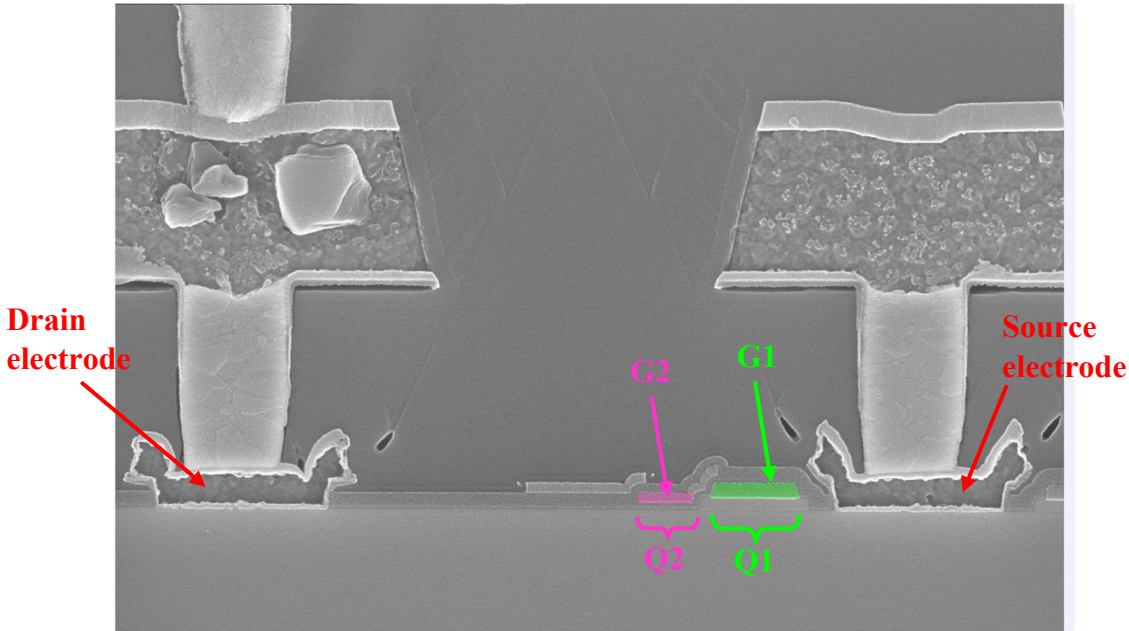
'003 Patent Claim 1	Innoscence's GaN Power Products (e.g. ISG3201)
	 (Cross-sectional view SEM image of INN100W032A, annotations added)
[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;	The low side INN100W032A transistor in ISG3201 meets this limitation. As shown in the cross-sectional view SEM image, INN100W032A comprises a drain electrode electrically connected to a top surface of the semiconductor element and spaced laterally away from the source electrode.

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	 (Cross-sectional view SEM image of INN100W032A, annotations added)
[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and	The low side INN100W032A transistor in ISG3201 meets this limitation. As shown in the cross-sectional view SEM image and cross-sectional view transmission electron microscopy (TEM) image, INN100W032A comprises a first gate (denoted by “G1”) positioned between the source electrode and the drain electrode. The first gate G1 is coupled to the semiconductor element via a p-GaN layer to form a first portion of the transistor (denoted by “Q1”).

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	 Drain electrode Source electrode G1 Q1 (Cross-sectional view SEM image of INN100W032A, annotations added)  Source electrode G1 p-GaN Q1 Semiconductor element

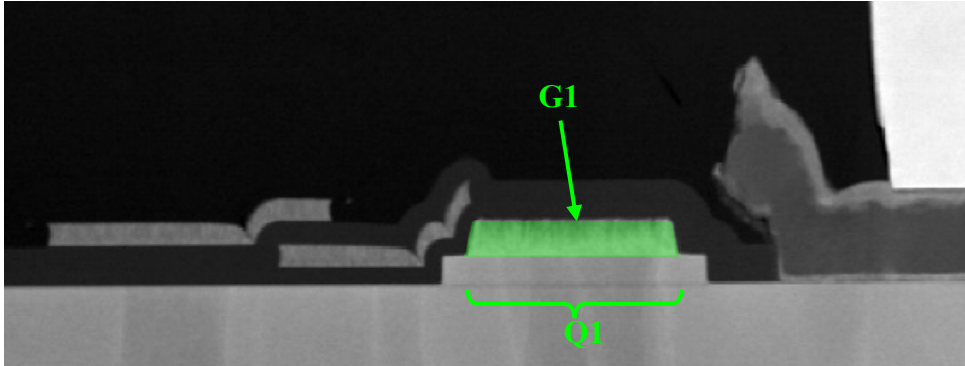
'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	(Cross-sectional view TEM image of INN100W032A, annotations added) Further, as shown in Innoscience datasheets and product materials, the first gate G1 in the INN100W032A transistor is coupled to the semiconductor element through a Schottky contact with a p-GaN layer to form a first portion of the transistor Q1. 

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	E-mode/Normally-off operation The power semiconductor market demands devices that show normally-off operation, which means that there is no current conduction when the transistor's gate is set at 0V. The natural form of GaN HEMTs (High Electron Mobility Transistors) is normally-on or so-called depletion mode (d-mode), which requires special drivers or to be placed in a cascode package solutions to realize normally-off operation. Innoscience's GaN HEMTs are intrinsically normally-off or so-called enhancement mode (e-mode) devices. The normally-off operation is realized by growing a p-GaN layer on top of the AlGaIn barrier, deposition and patterning of a gate metal and then selective recessing the p-GaN layer over the AlGaIn barrier. The gate metal layer forms a (Schottky) contact with the p-GaN layer, and, as a consequence, the potential in the channel at the equilibrium is lifted-up therefore realizing normally-off/e-mode operation. See Ex. 19 at 4 (https://www.innoscience.com/site/technology, annotations added)

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;	The low side INN100W032A transistor in ISG3201 meets this limitation. As shown in the cross-sectional view SEM image and cross-sectional view TEM image below, INN100W032A comprises a second gate (denoted by “G2”) positioned adjacent to the first gate G1, and between the source electrode and the drain electrode to form a second portion of the transistor (denoted by “Q2”).  (Cross-sectional view SEM image of INN100W032A, annotations added)

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	A cross-sectional TEM image of a GaN power device. The image shows two gate structures, G1 and G2, on a semiconductor substrate. Gate G1 is highlighted in green and is labeled with a green arrow. Gate G2 is highlighted in pink and is labeled with a pink arrow. A field plate is also indicated by a pink arrow. A source electrode is indicated by a red arrow. Brackets below the gates are labeled Q1 and Q2. (Cross-sectional view TEM image of INN100W032A, annotations added) The second gate G2 also includes a field plate, as shown in the annotated image above. Further, the second gate G2 in INN100W032A is coupled to the semiconductor element through an insulating layer as shown in the cross-sectional view TEM image. A cross-sectional TEM image of a GaN power device. The image shows gate G2, which is highlighted in pink and labeled with a pink arrow. An insulating layer is indicated by a red arrow, and a semiconductor element is indicated by a red arrow. Semiconductor element (Cross-sectional view TEM image of INN100W032A, annotations added)

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and	The low side INN100W032A transistor in ISG3201 meets this limitation. In the low side INN100W032A transistor, the first gate G1 is connected to the low side gate terminal LG of this INN100W032A transistor. Therefore, the first gate G1 is connected to the input voltage signal source in ISG3201 and has a voltage value of V_{LG}, i.e. the input voltage signal. <i>See</i> limitation [1A] above. 13. Block Diagram Block Diagram of ISG3201 is shown as Figure 1. A half-bridge GaN driver and two 100V GaN HEMTs are integrated. Besides, Vcc decoupling capacitor, Bootstrap capacitor, internal 20Ω turn-on resistor for both GaN HEMTs are also integrated. Turn-on speed can be adjusted by an optional resistor between HGP(LGP) pin and HG(LG) pin for top (bottom) GaN HEMT. Figure 1. Block diagram of ISG3201 <i>See</i> Ex. 31 at 9 (ISG3201 Datasheet, annotations added)

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	For a power transistor device, conduction of the device is based on a voltage applied to the gate. <i>See</i> Ex. 28 at 26-27. In the first portion of the transistor Q1 in the low side INN100W032A transistor, G1 is the gate. Therefore, conduction of Q1 is based on the voltage value V_{LG} applied to G1, i.e. the input voltage signal. Taken together, the first gate G1 is connected to the input voltage signal source such that conduction of the first portion of the transistor Q1 is based on a value of the input voltage signal.  (Cross-sectional view TEM image of INN100W032A, annotations added)
[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,	The low side INN100W032A transistor in ISG3201 meets this limitation. In the low side INN100W032A transistor, the source electrode (connected to the source terminal of this INN100W032A transistor) is connected to PGND of ISG3201 (i.e. constant voltage source).

13. Block Diagram

Block Diagram of ISG3201 is shown as Figure 1. A half-bridge GaN driver and two 100V GaN HEMTs are integrated. Besides, Vcc decoupling capacitor, Bootstrap capacitor, internal 20Ω turn-on resistor for both GaN HEMTs are also integrated. Turn-on speed can be adjusted by an optional resistor between HGP(LGP) pin and HG(LG) pin for top (bottom) GaN HEMT.

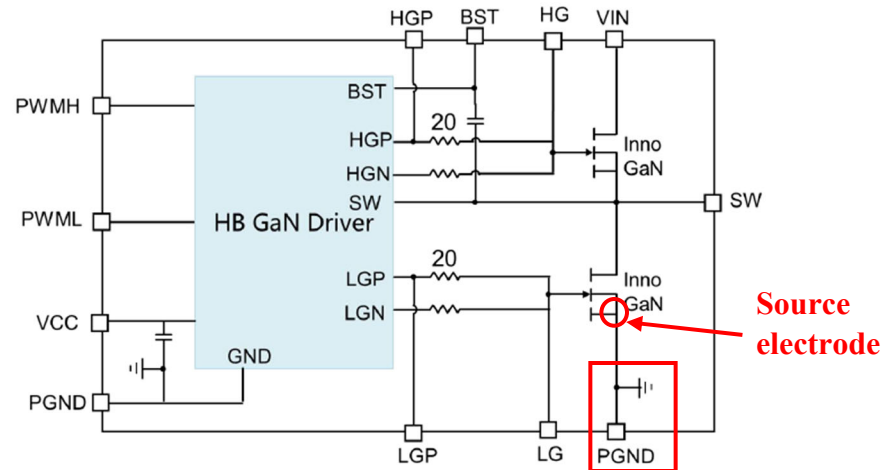
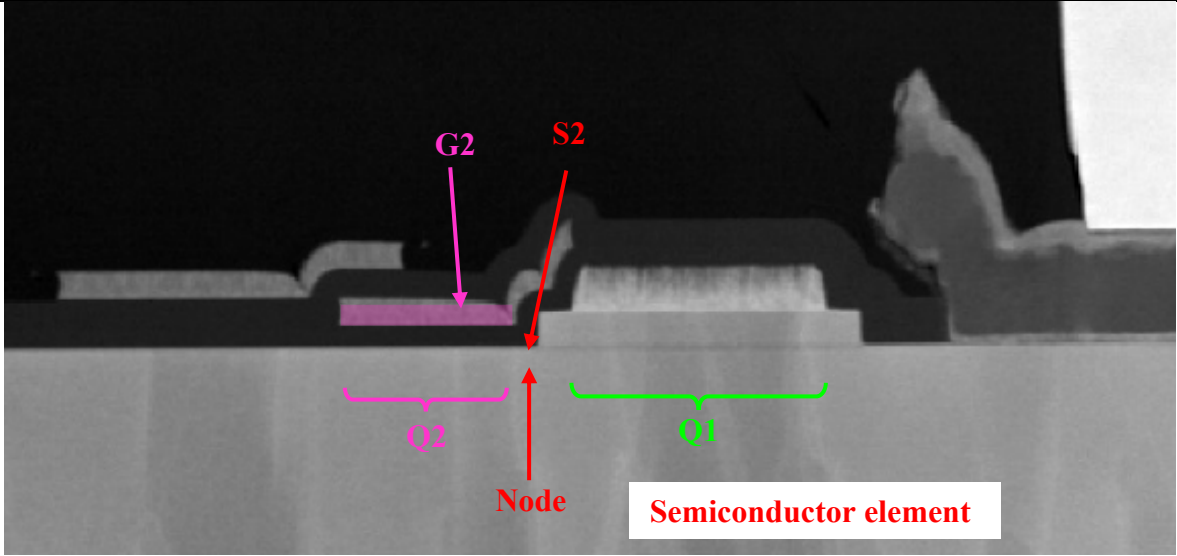


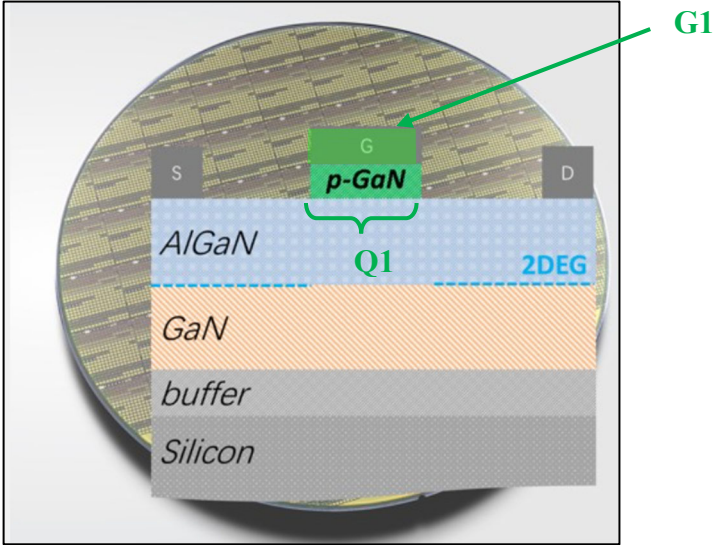
Figure 1. Block diagram of ISG3201

See Ex. 31 at 9 (ISG3201 Datasheet, annotations added)

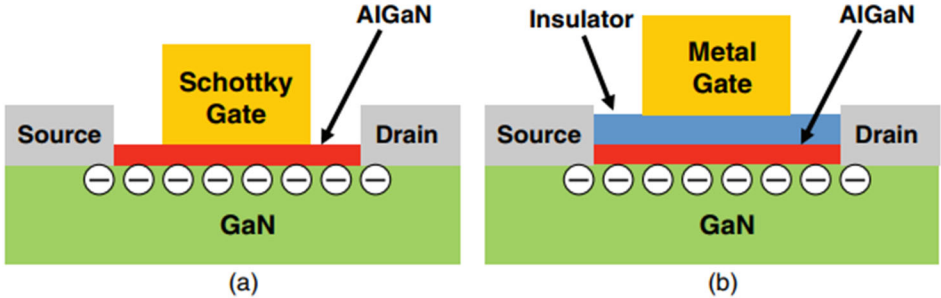
Plan-view photographs of a delayed INN100W032A illustrate that the second gate G2 in INN100W032A is connected to the source electrode through vertical vias and a common metal interconnect layer. Therefore, the second gate G2 is also connected to PGND (i.e. constant voltage source).

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	A plan-view photograph of a GaN power device (INN100W032A) showing a metal interconnect layer. The image displays several horizontal metal strips with vertical vias connecting them. Red arrows point to specific features: one arrow points to a vertical via labeled 'Vertical via contacting source electrode', another arrow points to a vertical via labeled 'Vertical via contacting second gate G2', and a third arrow points to the metal strips labeled 'Metal interconnect layer'. Vertical via contacting source electrode Vertical via contacting second gate G2 Metal interconnect layer (Plan-view photograph of a delayed INN100W032A, annotations added) As shown in the cross-sectional view TEM image of INN100W032A, the second gate G2 is the gate for the second portion of the transistor (Q2), and a node in the semiconductor element between Q1 and Q2 is a source (denoted by “S2”) of Q2. The gate-to-source voltage V_{GS} for Q2 equals a voltage difference between a voltage at G2 and a voltage at the source S2 (i.e. at the node). As discussed above, the second gate G2 is connected to PGND, and therefore has a voltage of the ground reference level (i.e. the predetermined constant voltage). As such, the gate-to-source voltage V_{GS} for Q2 equals a voltage difference between the predetermined constant voltage (at G2) and a voltage at a node (S2) in the semiconductor element between the first portion Q1 and the second portion Q2 of the transistor.

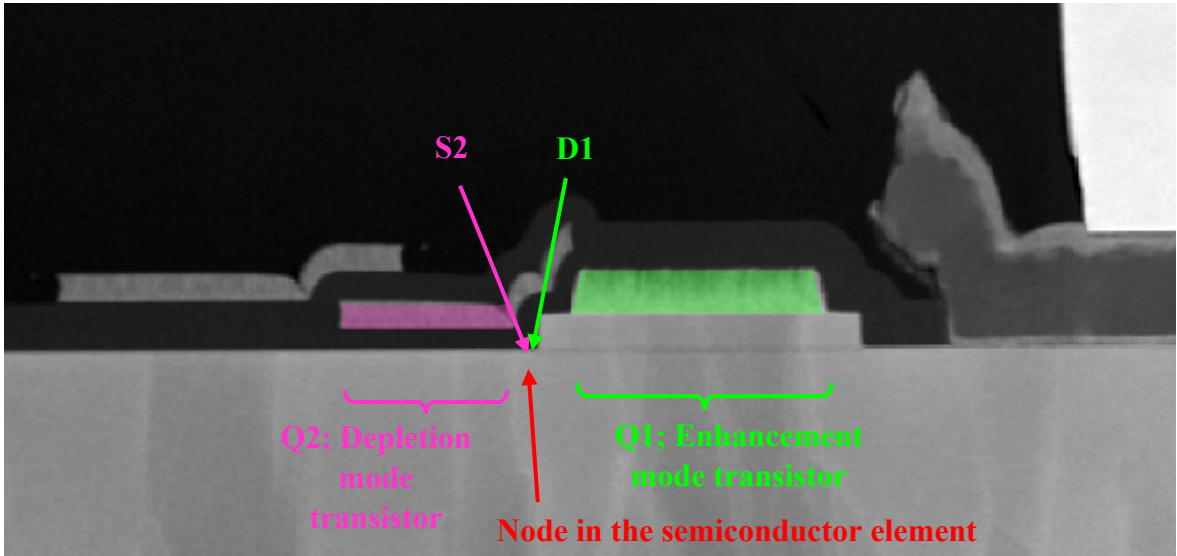
'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	 (Cross-sectional view TEM image of INN100W032A, annotations added) In a power transistor device, a threshold voltage (V_{th}) is a gate-to-source voltage (V_{GS}) below which the conduction of the device is off. <i>See</i> Ex. 28 at 26-27. Therefore, the second portion of the transistor Q2 conducts until its gate-to-source voltage V_{GS} (namely, a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor) reaches a threshold voltage V_{th} (i.e. reaches a predetermined level).
[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and	The low side INN100W032A transistor in ISG3201 meets this limitation. As discussed in limitation [1C4] above, in the first portion of the transistor Q1, the first gate G1 is coupled to the semiconductor element through a Schottky contact with a p-GaN layer. According to Innoscience's website, this realizes an enhancement mode device. Therefore, the first portion of the transistor Q1 is an enhancement mode transistor.

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	 The diagram illustrates a cross-section of a GaN power device. The layers from bottom to top are: Silicon, buffer, GaN, AlGaN, and p-GaN. The p-GaN layer is labeled 'Q1' and contains a 2DEG. A gate (G) is shown on top of the p-GaN layer, and a drain (D) is shown on the right. A source (S) is shown on the left. A green arrow labeled 'G1' points to the gate region.

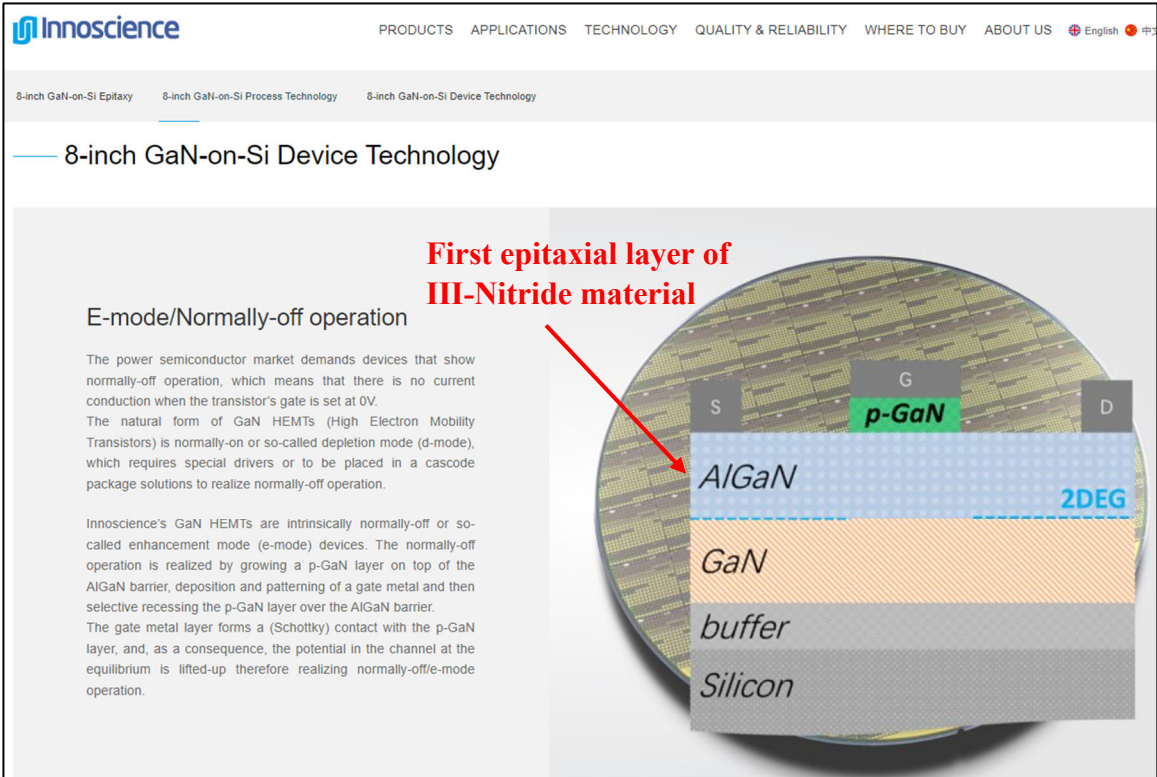
'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	E-mode/Normally-off operation The power semiconductor market demands devices that show normally-off operation, which means that there is no current conduction when the transistor's gate is set at 0V. The natural form of GaN HEMTs (High Electron Mobility Transistors) is normally-on or so-called depletion mode (d-mode), which requires special drivers or to be placed in a cascode package solutions to realize normally-off operation. Innoscience's GaN HEMTs are intrinsically normally-off or so-called enhancement mode (e-mode) devices. The normally-off operation is realized by growing a p-GaN layer on top of the AlGaIn barrier, deposition and patterning of a gate metal and then selective recessing the p-GaN layer over the AlGaIn barrier. The gate metal layer forms a (Schottky) contact with the p-GaN layer, and, as a consequence, the potential in the channel at the equilibrium is lifted-up therefore realizing normally-off/e-mode operation. See Ex. 19 at 4 (https://www.innoscience.com/site/technology, annotations added)

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	As discussed above in connection with limitation [1C5], the second gate G2 is coupled to the semiconductor element through an insulating layer, which is an insulated gate. Therefore, the second portion of the transistor (Q2) is an insulated gate transistor using an insulated gate G2, which according to the textbook “GaN Transistors for Efficient Power Conversion” is a common way to produce a depletion-mode transistor. There are two common ways to produce a d-mode HEMT device. The initial transistors introduced in 2004 had a Schottky gate electrode that was created by depositing a metal layer directly on top of the AlGaN. The Schottky barrier was formed using metals such as Ni-Au or Pt [9–11]. <u>Depletion-mode devices have also been made using an insulating layer and metal gate</u> similar to a MOSFET [12]. Both types are shown in Figure 1.6. GaN Technology Overview 7  Figure 1.6 Cross section of a basic depletion-mode GaN HEMT with (a) Schottky gate, or (b) <u>insulating gate</u> See Ex. 28 at 24-25 (GaN Transistors for Efficient Power Conversion, 2nd edition, annotations added) Furthermore, Innoscience's own website explains that without a Schottky contact on a p-GaN layer (such as the case with the insulated gate G2 on Q2), “the natural form of GaN HEMTs” is a depletion mode transistor.

'003 Patent Claim 1	Innoscience's GaN Power Products (e.g. ISG3201)
	E-mode/Normally-off operation The power semiconductor market demands devices that show normally-off operation, which means that there is no current conduction when the transistor's gate is set at 0V. The natural form of GaN HEMTs (High Electron Mobility Transistors) is normally-on or so-called depletion mode (d-mode), which requires special drivers or to be placed in a cascode package solutions to realize normally-off operation. Innoscience's GaN HEMTs are intrinsically normally-off or so-called enhancement mode (e-mode) devices. The normally-off operation is realized by growing a p-GaN layer on top of the AlGaIn barrier, deposition and patterning of a gate metal and then selective recessing the p-GaN layer over the AlGaIn barrier. The gate metal layer forms a (Schottky) contact with the p-GaN layer, and, as a consequence, the potential in the channel at the equilibrium is lifted-up therefore realizing normally-off/e-mode operation. See Ex. 19 at 4 (https://www.innoscience.com/site/technology, annotations added)

'003 Patent Claim 1	Innoscence's GaN Power Products (e.g. ISG3201)
[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.	The low side INN100W032A transistor in ISG3201 meets this limitation. As shown in the cross-sectional view TEM image of INN100W032A, a drain region (denoted by "D1") of the enhancement mode transistor Q1 is merged with a source region (denoted by "S2") of the depletion mode transistor Q2 at the node in the semiconductor element.  (Cross-sectional view TEM image of INN100W032A, annotations added)
'003 Patent Claim 10	Innoscence's GaN Power Products (e.g. ISG3201)
[10PRE] A merged cascode high electron mobility transistor circuit comprises:	To the extent the preamble is limiting, the preamble is met.

'003 Patent Claim 10	Innoscience's GaN Power Products (e.g. ISG3201)
	As discussed above in limitation [1PRE], Innoscience's ISG3201 is a co-packaged product that includes Innoscience's INN100W032A, which is a high-electron-mobility-transistor (HEMT). The image is a snippet from the INN100W032A datasheet. It features the Innoscience logo in the top right. The title 'INN100W032A' is prominently displayed, followed by the subtitle '100V Enhancement-mode GaN Power Transistor'. Below this, under the heading '1. General description', the text reads: 'GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in Solder Bar WLCSP with 3.5 mm x 2.13 mm package size.' The phrase 'high-electron-mobility-transistor (HEMT)' is enclosed in a red rectangular box. <i>See Ex. 21 at 1 (INN100W032A Datasheet, annotations added)</i> As discussed above in limitation [1C], INN100W032A is a merged cascode transistor. Therefore, INN100W032A is a merged cascode high electron mobility transistor. ISG3201, which incorporates a merged cascode high electron mobility transistor, is a merged cascode high electron mobility transistor circuit.
[10A] an input voltage signal source having an input voltage signal;	Innoscience's ISG3201 meets this limitation. ISG3201 comprises an input voltage signal source having an input voltage signal. <i>See</i> limitation [1A].
[10B] a constant voltage source having a predetermined constant voltage;	Innoscience's ISG3201 meets this limitation. ISG3201 comprises a constant voltage source having a predetermined constant voltage. <i>See</i> limitation [1B].
[10C] a merged cascode transistor comprising:	The low side INN100W032A transistor in ISG3201 meets this limitation.

'003 Patent Claim 10	Innoscience's GaN Power Products (e.g. ISG3201)
	ISG3201 comprises a low side INN100W032A transistor. <i>See</i> limitation [1A]. The low side INN100W032A transistor is a merged cascode transistor. <i>See</i> limitation [1C].
[10C1] a first epitaxial layer of III-Nitride material;	The low side INN100W032A transistor in ISG3201 meets this limitation. As illustrated on Innoscience's website, the INN100W032A transistor product is a GaN-on-Si device that includes an AlGaN layer and a GaN layer with a 2-dimensional electron gas (2DEG) at the interface between the AlGaN and GaN layers. The AlGaN layer is a first epitaxial layer of III-Nitride material.  The screenshot shows the Innoscience website's '8-inch GaN-on-Si Device Technology' page. On the left, there is text describing 'E-mode/Normally-off operation' and the structure of GaN HEMTs. On the right, a cross-sectional diagram of the device is shown, with layers labeled from top to bottom: Silicon, buffer, GaN, AlGaN, and p-GaN. A red arrow points from the text 'First epitaxial layer of III-Nitride material' to the AlGaN layer in the diagram. The diagram also shows a gate (G) and a drain (D) contact, and a 2DEG layer at the interface between the AlGaN and GaN layers.

'003 Patent Claim 10	Innoscience's GaN Power Products (e.g. ISG3201)
	Epitaxy Innoscience has been growing more than 10,000 wafers/month that have been successfully processed to produce HV and LV devices that were shipped and used by customers. Innoscience GaN-on-Si epitaxial process have been optimized to systematically obtain uniform and reproducible crack-free epi-wafers with low dislocations density and defects. See Ex. 19 at 4 (https://www.innoscience.com/site/technology, annotations added)
[10C2] a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;	The low side INN100W032A transistor in ISG3201 meets this limitation. In the INN100W032A transistor product, the GaN layer (i.e. second epitaxial layer of a III-Nitride material) is in contact with the AlGaN layer (i.e. first epitaxial layer) such that a 2DEG (i.e. a 2-dimensional electron gas conducting layer) is formed between the first and second epitaxial layers.

Innoscience PRODUCTS APPLICATIONS TECHNOLOGY QUALITY & RELIABILITY WHERE TO BUY ABOUT US English 中

8-inch GaN-on-Si Epitaxy 8-inch GaN-on-Si Process Technology 8-inch GaN-on-Si Device Technology

8-inch GaN-on-Si Device Technology

E-mode/Normally-off operation

The power semiconductor market demands devices that show normally-off operation, which means that there is no current conduction when the transistor's gate is set at 0V. The natural form of GaN HEMTs (High Electron Mobility Transistors) is normally-on or so-called depletion mode (d-mode), which requires special drivers or to be placed in a cascode package solutions to realize normally-off operation.

Innoscience's GaN HEMTs are intrinsically normally-off or so-called enhancement mode (e-mode) devices. The normally-off operation is realized by growing a p-GaN layer on top of the AlGaN barrier, deposition and patterning of a gate metal and then selective recessing the p-GaN layer over the AlGaN barrier. The gate metal layer forms a (Schottky) contact with the p-GaN layer, and, as a consequence, the potential in the channel at the equilibrium is lifted-up therefore realizing normally-off/e-mode operation.

First epitaxial layer of III-Nitride material

Second epitaxial layer of III-Nitride material

S G D

2DEG

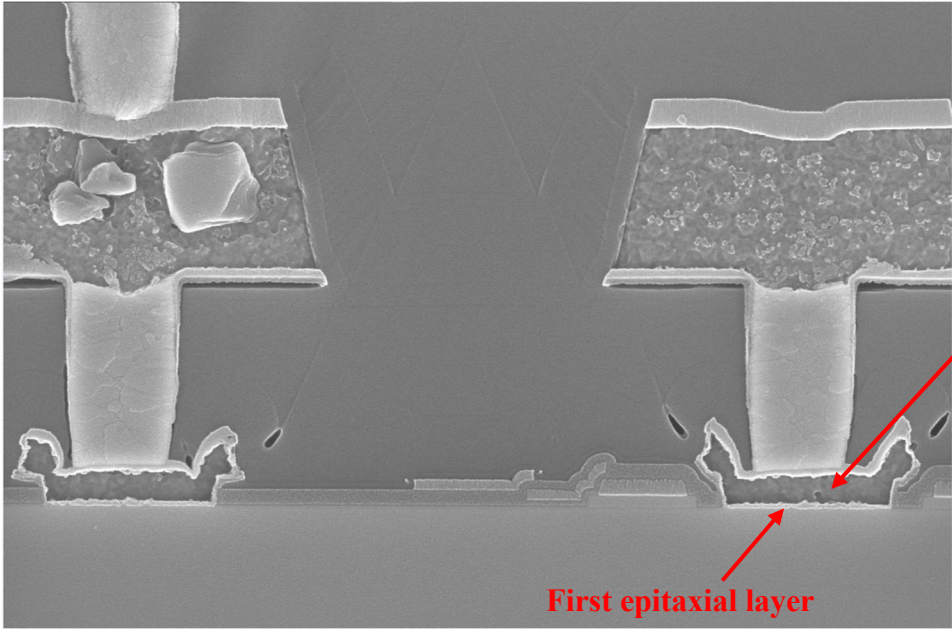
AlGaN

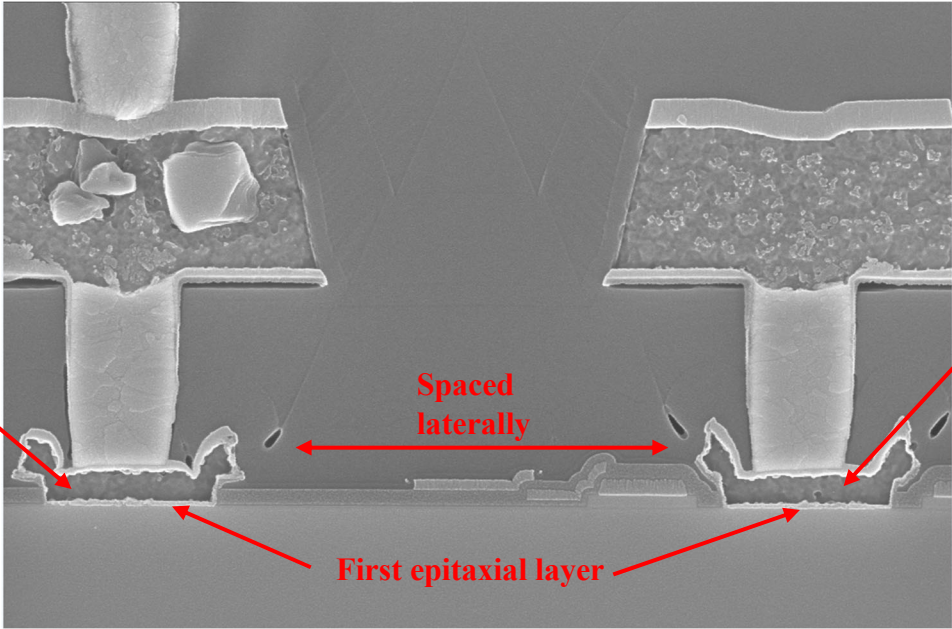
GaN

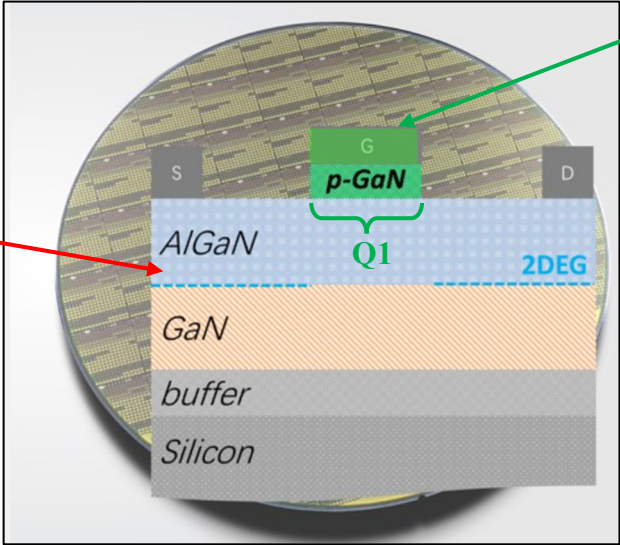
buffer

Silicon

'003 Patent Claim 10	Innoscience's GaN Power Products (e.g. ISG3201)
	Epitaxy Innoscience has been growing more than 10,000 wafers/month that have been successfully processed to produce HV and LV devices that were shipped and used by customers. Innoscience GaN-on-Si epitaxial process have been optimized to systematically obtain uniform and reproducible crack-free epi-wafers with low dislocations density and defects. See Ex. 19 at 4 (https://www.innoscience.com/site/technology, annotations added)
[10C3] a source electrode electrically connected to the first epitaxial layer;	The low side INN100W032A transistor in ISG3201 meets this limitation. As shown in a cross-sectional view SEM image, INN100W032A comprises a source electrode electrically connected to the first epitaxial layer.

'003 Patent Claim 10	Innoscience's GaN Power Products (e.g. ISG3201)
	 (Cross-sectional view SEM image of INN100W032A, annotations added)
[10C4] a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;	The low side INN100W032A transistor in ISG3201 meets this limitation. As shown in a cross-sectional view SEM image, INN100W032A comprises a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode.

'003 Patent Claim 10	Innoscience's GaN Power Products (e.g. ISG3201)
	 (Cross-sectional view SEM image of INN100W032A, annotations added)
[10C5] a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and	The low side INN100W032A transistor in ISG3201 meets this limitation. INN100W032A comprises a first gate (denoted by “G1”) positioned between the source electrode and the drain electrode to form a first portion of the transistor (denoted by “Q1”). <i>See</i> limitation [1C4]. G1 in INN100W032A is coupled to the first epitaxial layer through a Schottky contact to form Q1. <i>See also</i> limitation [1C4].

'003 Patent Claim 10	Innoscience's GaN Power Products (e.g. ISG3201)
	 The diagram shows a cross-section of a GaN power device. The layers from top to bottom are: <i>p-GaN</i> (green), <i>AlGaN</i> (blue), <i>GaN</i> (orange), <i>buffer</i> (grey), and <i>Silicon</i> (dark grey). A gate stack labeled 'G' is on top of the <i>p-GaN</i> layer. Source ('S') and drain ('D') electrodes are on the sides. A red arrow points to the <i>AlGaN</i> layer with the label 'First epitaxial layer'. A green arrow points to the <i>p-GaN</i> layer with the label 'G1'. A bracket labeled 'Q1' spans the <i>p-GaN</i> and <i>AlGaN</i> layers. The label '2DEG' is located in the <i>GaN</i> layer.

'003 Patent Claim 10	Innoscience's GaN Power Products (e.g. ISG3201)
	E-mode/Normally-off operation The power semiconductor market demands devices that show normally-off operation, which means that there is no current conduction when the transistor's gate is set at 0V. The natural form of GaN HEMTs (High Electron Mobility Transistors) is normally-on or so-called depletion mode (d-mode), which requires special drivers or to be placed in a cascode package solutions to realize normally-off operation. Innoscience's GaN HEMTs are intrinsically normally-off or so-called enhancement mode (e-mode) devices. The normally-off operation is realized by growing a p-GaN layer on top of the AlGaN barrier, deposition and patterning of a gate metal and then selective recessing the p-GaN layer over the AlGaN barrier. The gate metal layer forms a (Schottky) contact with the p-GaN layer, and, as a consequence, the potential in the channel at the equilibrium is lifted-up therefore realizing normally-off/e-mode operation. See Ex. 19 at 4 (https://www.innoscience.com/site/technology, annotations added)

'003 Patent Claim 10	Innoscience's GaN Power Products (e.g. ISG3201)
[10C6] a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;	The low side INN100W032A transistor in ISG3201 meets this limitation. INN100W032A comprises a second gate (denoted by "G2") positioned adjacent to the first gate G1, and between the source electrode and the drain electrode to form a second portion of the transistor (denoted by "Q2"). The second gate G2 also includes a field plate. <i>See</i> limitation [1C5].
[10C7] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and	The low side INN100W032A transistor in ISG3201 meets this limitation. In ISG3201, the first gate G1 of the low side INN100W032A transistor is connected to the input voltage signal source such that conduction of the first portion Q1 is based on a value of the input voltage signal V_{LG}. <i>See</i> limitation [1C6].
[10C8] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,	The low side INN100W032A transistor in ISG3201 meets this limitation. In ISG3201, the second gate G2 of the low side INN100W032A transistor is connected to the constant voltage source PGND such that the second portion of the transistor Q2 conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion Q1 and the second portion Q2 of the transistor reaches a predetermined level. <i>See</i> limitation [1C7].
[10C9] wherein the first portion of the transistor is an enhancement mode transistor and the second	The low side INN100W032A transistor in ISG3201 meets this limitation. In INN100W032A, the first portion Q1 of the transistor is an enhancement mode transistor and the second portion Q2 of the transistor is a depletion mode transistor. <i>See</i> limitation [1C8].

'003 Patent Claim 10	Innoscience's GaN Power Products (e.g. ISG3201)
portion of the transistor is a depletion mode transistor, and	
[10C10] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.	The low side INN100W032A transistor in ISG3201 meets this limitation. In INN100W032A, a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element. <i>See</i> limitation [1C9].