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(54) WIDE BANDGAP TRANSISTOR DEVICES WITH FIELD PLATES

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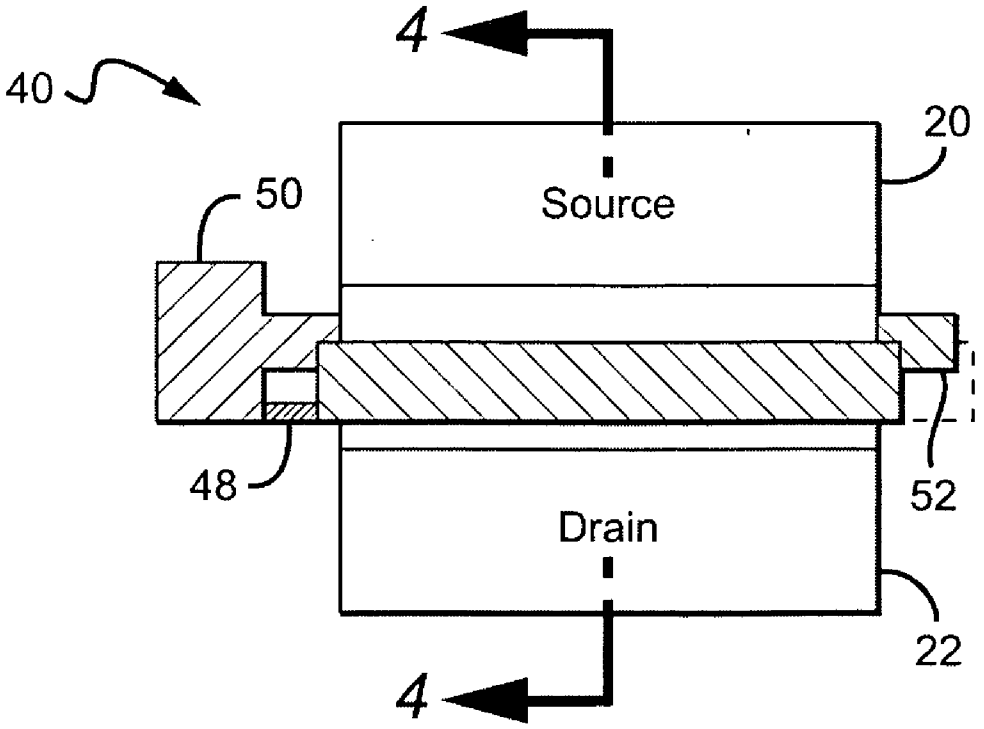
(57) ABSTRACT

A transistor structure comprising an active semiconductor layer with metal source and drain contacts formed in electrical contact with the active layer. A gate contact is formed between the source and drain contacts for modulating electric fields within the active layer. A spacer layer is formed above the active layer and a conductive field plate formed above the spacer layer, extending a distance L_f from the edge of the gate contact toward the drain contact. The field plate is electrically connected to the gate contact.



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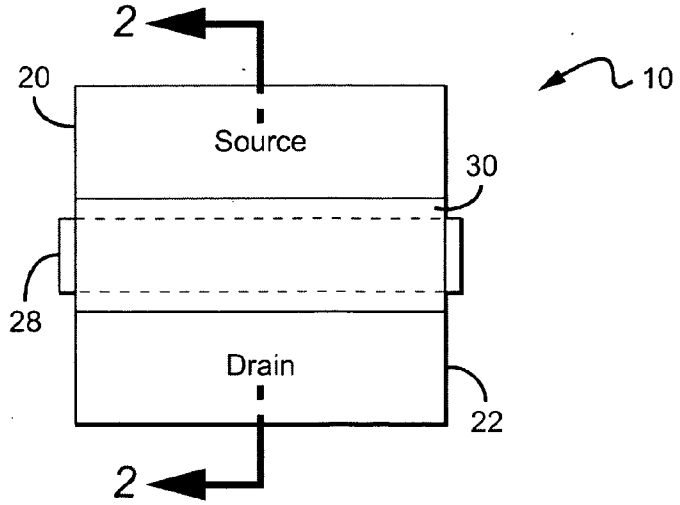

FIG. 1

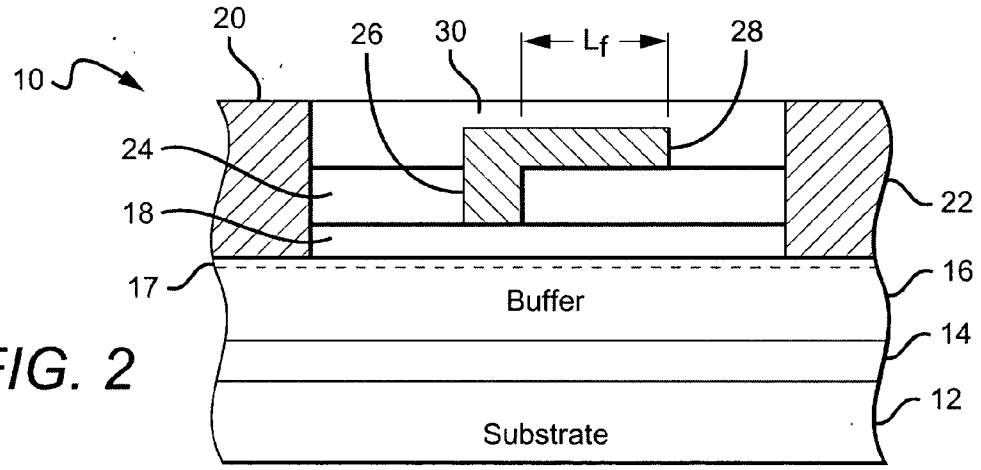

FIG. 2

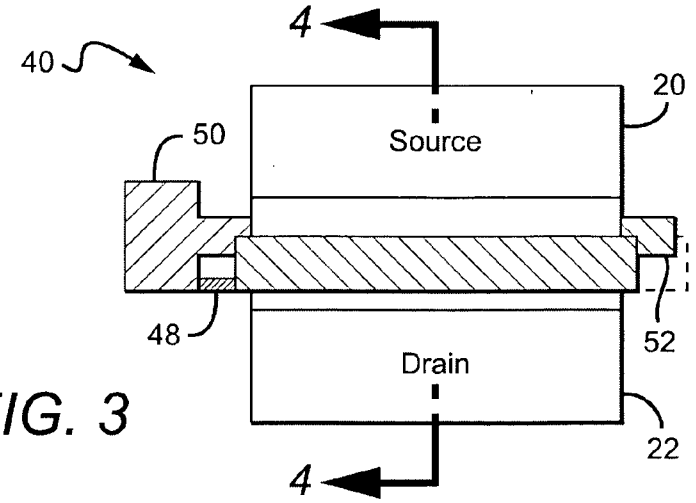

FIG. 3

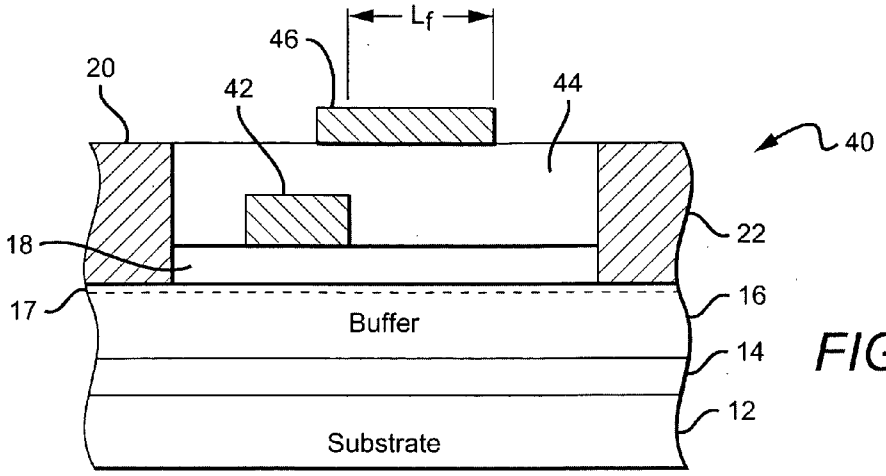

FIG. 4

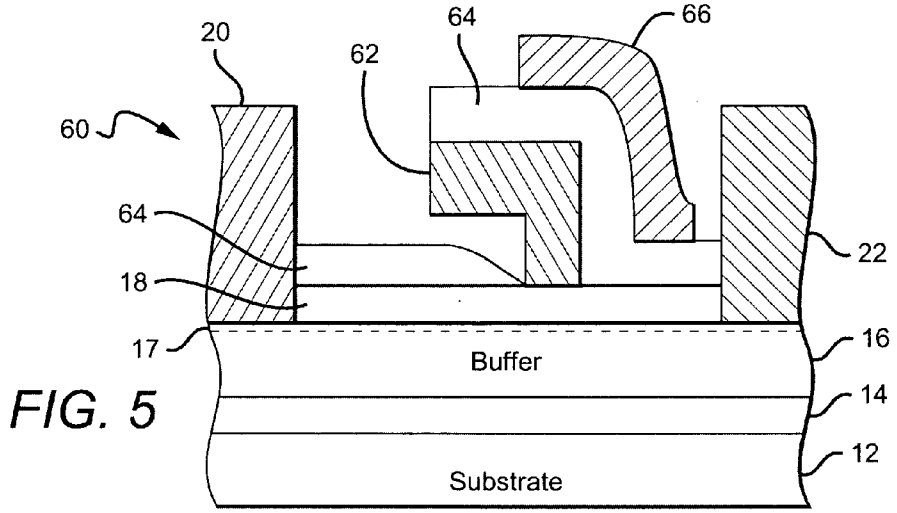

FIG. 5

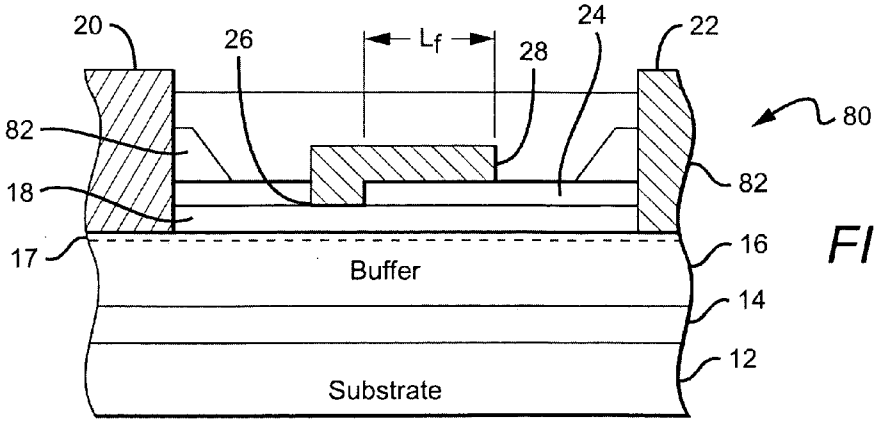

FIG. 6

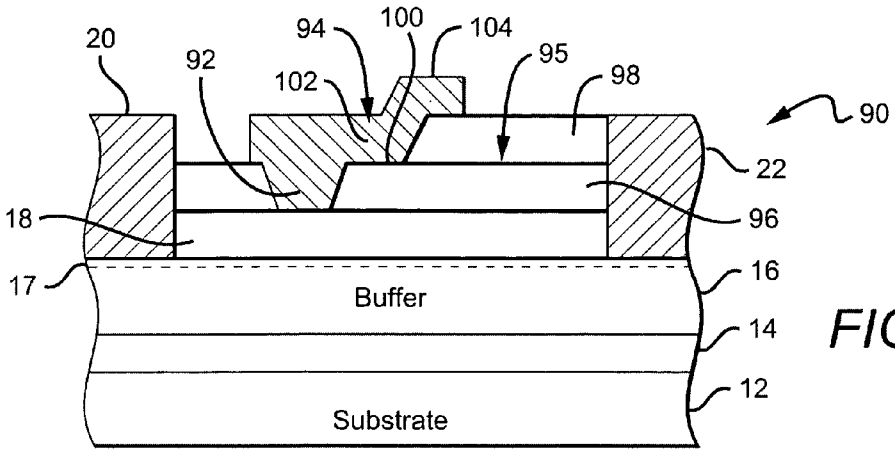

FIG. 7

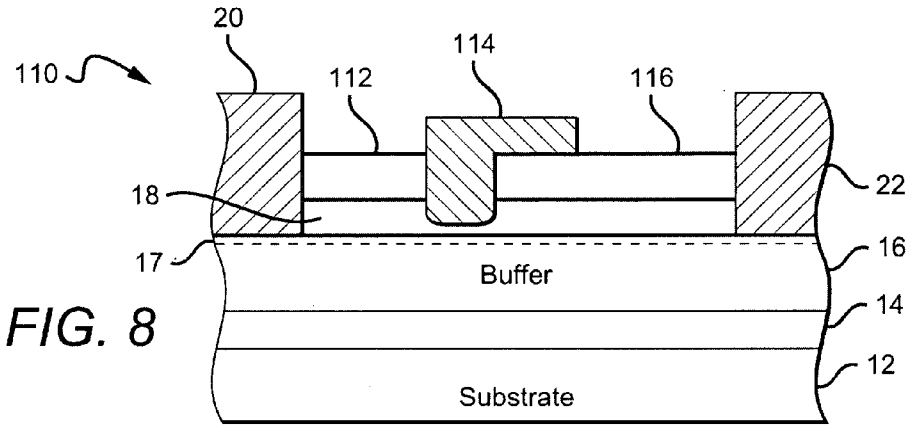

FIG. 8

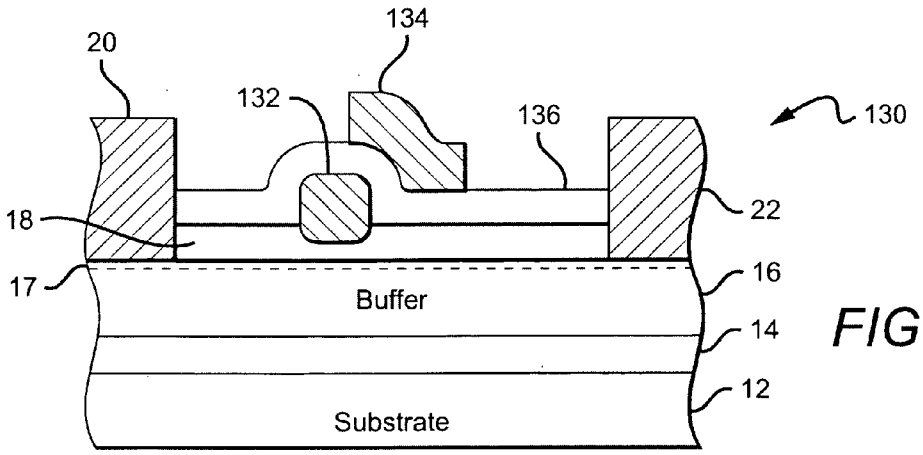

FIG. 9

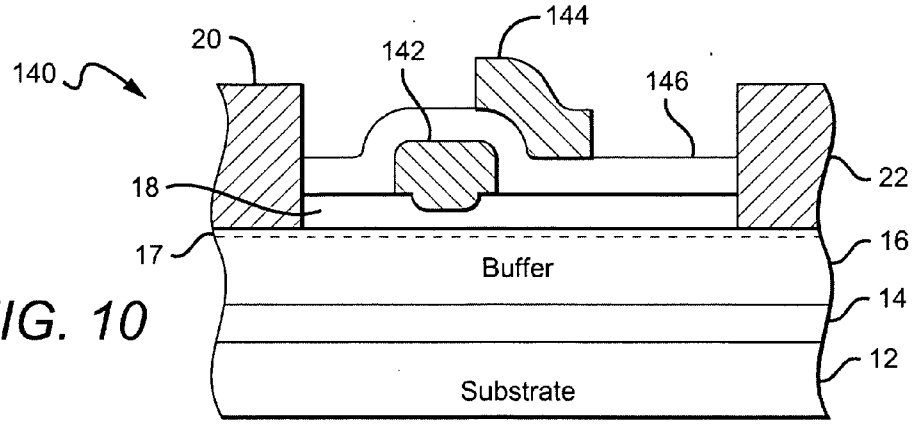

FIG. 10

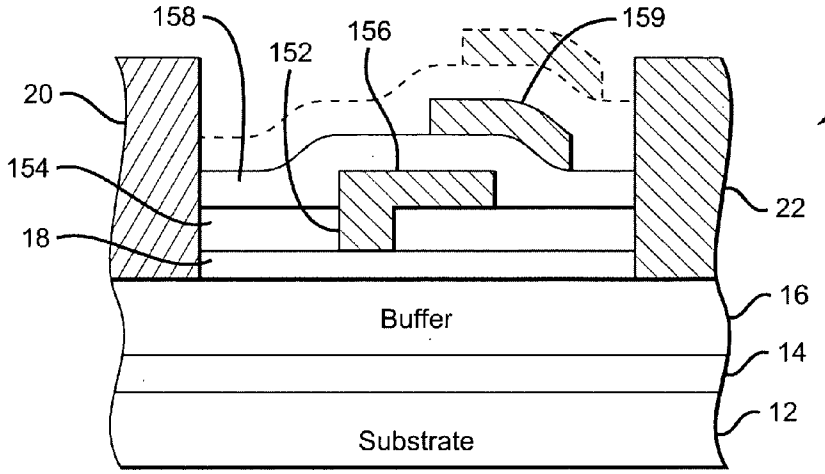

FIG. 11

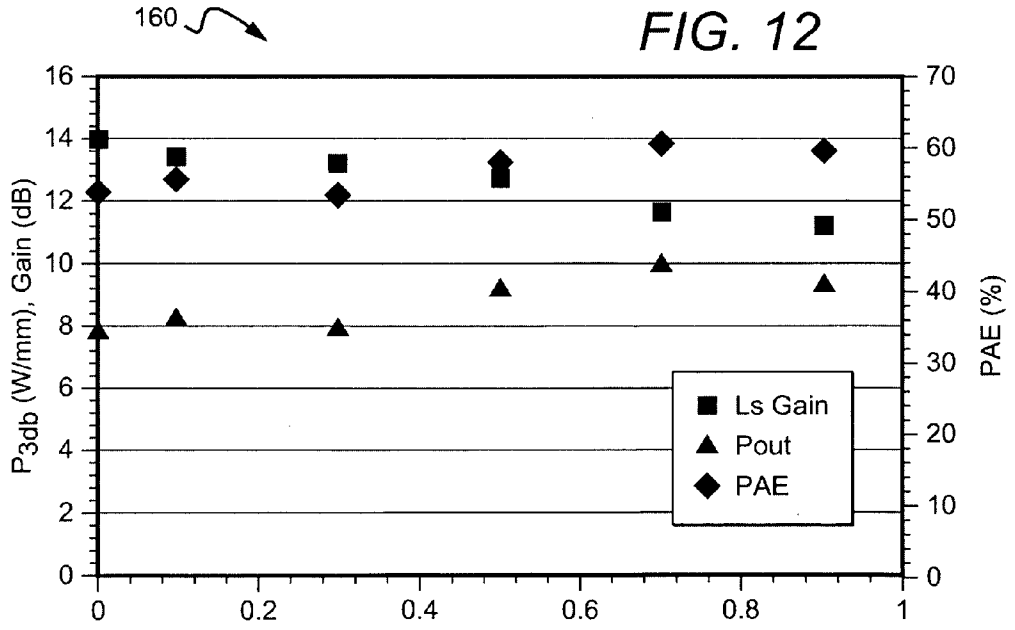

FIG. 12

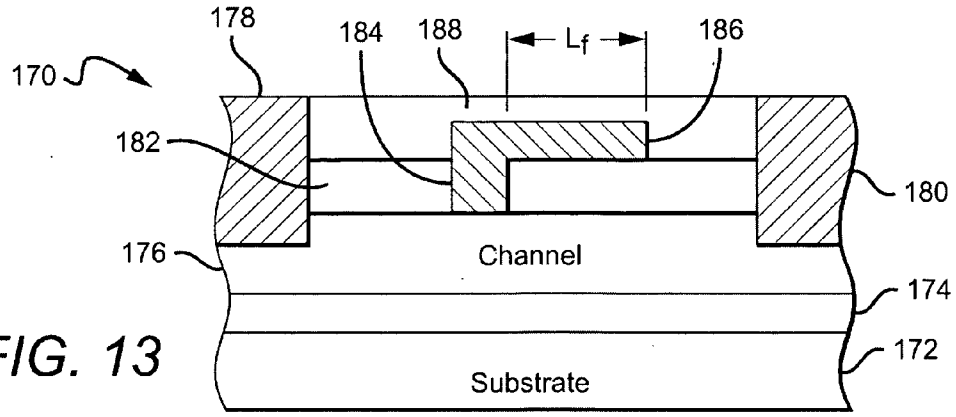

FIG. 13

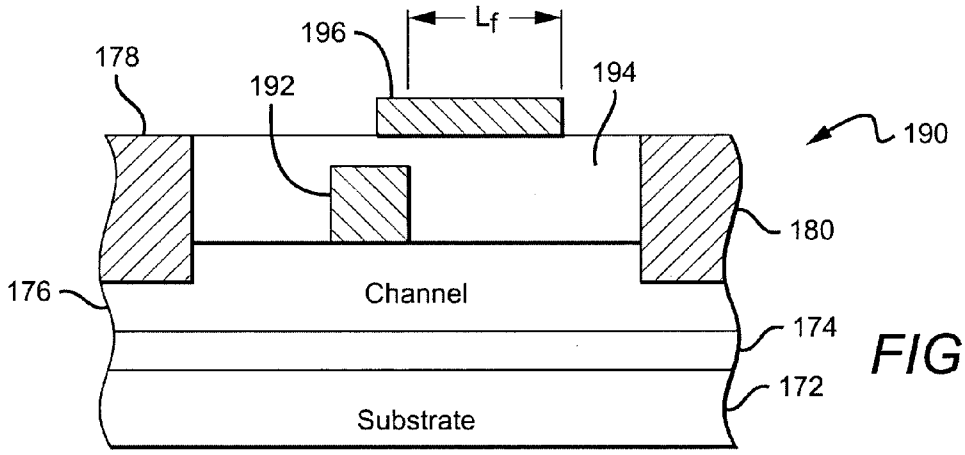

FIG. 14

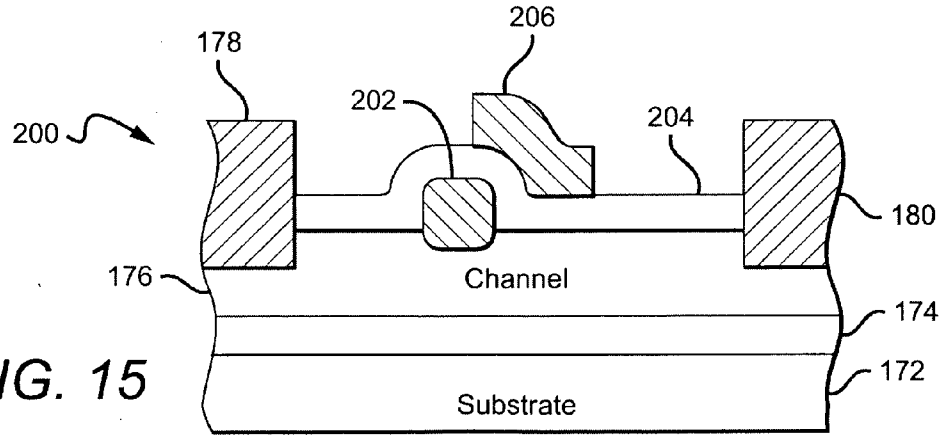

FIG. 15

WIDE BANDGAP TRANSISTOR DEVICES WITH FIELD PLATES

[0001] This application claims the benefit of provisional application Ser. No. 60/501,576 to Parikh et al., which was filed on Sep. 9, 2003.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to transistors and particularly to transistors utilizing field plates.

[0004] 2. Description of the Related Art

[0005] High electron mobility transistors (HEMTs) are a common type of solid state transistor that are regularly fabricated from semiconductor materials such as Silicon (Si) or Gallium Arsenide (GaAs). One disadvantage of Si is that it has low electron mobility (600-1450 $cm^2/V-s$), which produces a high source resistance. This resistance can degrade the Si based HEMT's high performance gain. [CRC Press, *The Electrical Engineering Handbook*, Second Edition, Dorf, p.994, (1997)]

[0006] GaAs based HEMTs have become the standard for signal amplification in civil and military radar, handset cellular, and satellite communications. GaAs has a higher electron mobility (approximately 6000 $cm^2/V-s$) and a lower source resistance than Si, which allows GaAs based devices to function at higher frequencies. However, GaAs has a relatively small bandgap (1.42 eV at room temperature) and relatively small breakdown voltage, which prevents GaAs based HEMTs from providing high power at high frequencies.

[0007] Improvements in the manufacturing of wide bandgap semiconductor materials such as AlGaN/GaN, has focused interest on the development of AlGaN/GaN HEMTs for high frequency, high temperature and high power applications. AlGaN/GaN has large bandgaps, as well as high peak and saturation electron velocity values [B. Belmont, K. Kim and M. Shur, *J.Appl.Phys.* 74, 1818 (1993)]. AlGaN/GaN HEMTs can also have two dimensional electron gas (2DEG) sheet densities in excess of $10^{13}/cm^2$ and relatively high electron mobility (up to 2019 cm^2/Vs) [R. Gaska, J. W. Yang, A. Osinsky, Q. Chen, M. A. Khan, A. O. Orlov, G. L. Snider and M. S. Shur, *Appl.Phys.Lett.,* 72, 707 (1998)]. These characteristics allow AlGaN/GaN HEMTs to provide very high voltage and high power operation at RF, microwave and millimeter wave frequencies.

[0008] AlGaN/GaN HEMTs have been grown on sapphire substrates and have shown a power density of 4.6 W/mm and a total power of 7.6 W [Y. F. Wu et al., *IEICE Trans.Electron.*, E-82-C, 1895 (1999)]. More recently, AlGaN/GaN HEMTs grown on SiC have shown a power density of 9.8 W/mm at 8 GHz [Y. F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller and U. K. Mishra, *IEEE Trans.Electron.Dev.,* 48, 586 (2001)] and a total output power of 22.9 at 9 GHz [M. Micovic, A Kurdoghlian, P. Janke, P. Hashimoto, D. W. S. Wong, J. S. Moon, L. McCray and C. Nguyen, *IEEE Trans.Electron.Dev.,* 48, 591 (2001)]. U.S. Pat. No. 5,192,987 to Khan et al. discloses GaN/AlGaN based HEMTs grown on a buffer and a substrate. Other AlGaN/GaN HEMTs and field effect transistors (FETs) have been described by Gaska et al., "High-Temperature Performance of AlGaN/GaN HFET's on SiC Substrates,"*IEEE Electron Device Letters,* Vol. 18, No. 10, October 1997, Page 492; and Ping et al., "DC and Microwave Performance of High Current AlGaN Heterostructure Field Effect Transistors Grown on P-type SiC Substrates,"*IEEE Electron Devices Letters,* Vol. 19, No. 2, February 1998, Page 54. Some of these devices have shown a gain-bandwidth product (f_T) as high as 67 gigahertz [K. Chu et al. WOCSEMMAD, Monterey, Calif. (February 1998)] and high power densities up to 2.84 W/mm at 10 GHz [G. Sullivan et al., "High Power 10-GHz Operation of AlGaN HFET's in Insulating SiC,"*IEEE Electron Device Letters*, Vol. 19, No. 6, Page 198 (June 1998); and Wu et al., *IEEE Electron Device Letters,* Volume 19, No. 2, Page 50 (February 1998)].

[0009] Electron trapping and the resulting difference between DC and RF characteristics have been a limiting factor in the performance of GaN based transistors, such as AlGaN/GaN HEMTS. Silicon Nitride (SiN) passivation has been successfully employed to alleviate this trapping problem, which has resulted in high performance devices with power densities over 10W/mm at 10 Ghz. U.S. Pat. No. 6,586,781 discloses methods and structures for reducing the trapping effect in GaN-based transistors. However, due to the high electric fields existing in these structures, charge trapping can still be an issue.

SUMMARY OF THE INVENTION

[0010] The present invention provides improved transistor structures utilizing gate connected field plates to improve operating characteristics. One transistor according to the present invention comprises a plurality of active semiconductor layers formed on a substrate. A source contact is formed in electrical contact with the plurality of active layers, and a drain contact is also formed in electrical contact with the plurality of active layers with space between the source and drain contacts on the topmost of the plurality of active layers. A gate is formed in electrical contact with the topmost of the plurality of active layers, between the source and drain contacts. A spacer layer of epitaxial material is formed on the surface of the topmost of the plurality of active layers, between the gate and the drain contact, wherein the gate is not covered by the spacer layer. A field plate is formed on the spacer layer integral to the gate.

[0011] Another embodiment of a transistor according to the present invention comprises a plurality of active semiconductor layers formed on a substrate. A source contact is formed in electrical contact with the plurality of active layers. A drain contact is also formed in electrical contact with the plurality of active layers with space between the source and drain contacts on the topmost of the plurality of active layers. A gate is formed in electrical contact with the topmost of the plurality of active layers, between the source and drain contacts. A spacer layer is formed on the surface of the topmost of the plurality of active layers, between the gate and the drain contact, and covering the gate contact. A field plate is formed on the spacer layer and is electrically connected to the gate.

[0012] Another embodiment of a transistor according to the present invention comprises a plurality of active semiconductor layers formed on a substrate. Source and drain contacts are formed in electrical contact with the plurality of active layers. A gate is formed in electrical contact with the

topmost of the plurality of active layers, between the source and drain contacts. A first spacer layer formed on the surface of the topmost of the plurality of active layers, between the gate and the drain contact, wherein the gate is not covered by the spacer layer. A first field plate formed on the spacer layer integral to the gate and extending toward the drain contact on the spacer layer. A second spacer layer covering the field plate and the surface of the spacer layer between the field plate and drain contact, and further comprising a second field plate on the second spacer layer and extending from the edge of the gate toward the drain contact.

[0013] These and other further features and advantages of the invention would be apparent to those skilled in the art from the following detailed description, taking together with the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] **FIG. 1** is a plan view of one embodiment of a HEMT according to the present invention;

[0015] **FIG. 2** is a sectional view of the HEMT in **FIG. 1**;

[0016] **FIG. 3** is a plan view of another embodiment of a HEMT according to the present invention;

[0017] **FIG. 4** is a sectional view of the HEMT in **FIG. 3**;

[0018] **FIG. 5** is a sectional view of another embodiment of a HEMT according to the present invention having a gamma shaped gate;

[0019] **FIG. 6** is a sectional view of another embodiment of a HEMT according to the present invention having an n+ doped contact layer;

[0020] **FIG. 7** is a sectional view of another embodiment of a HEMT according to the present invention having multiple spacer layers;

[0021] **FIG. 8** is a sectional view of another embodiment of a HEMT according to the present invention having a recessed gate;

[0022] **FIG. 9** is a sectional view of another embodiment of a HEMT according to the present invention having a recessed gate;

[0023] **FIG. 10** is a sectional view of still another embodiment of a HEMT according to the present invention having a recessed gate;

[0024] FIG; **11** is a graph showing the performance of certain HEMTs arranged according to the present invention;

[0025] **FIG. 12** is a sectional view of one embodiment of a MESFET according to the present invention;

[0026] **FIG. 13** is a sectional view of another embodiment of a MESFET according to the present invention; and

[0027] **FIG. 14** is still another embodiment of a MESFET according to the present invention having a recessed gate.

DETAILED DESCRIPTION OF THE INVENTION

[0028] The field plate arrangements according to the present invention can be used with many different transistor structures. Wide bandgap transistor structures generally include an active region, with metal source and drain contacts formed in electrical contact with the active region, and a gate contact formed between the source and drain contacts for modulating electric fields within the active region. A spacer layer is formed above the active region. The spacer layer can comprise a dielectric layer, a layer of epitaxial material such as an undoped or depleted wide bandgap epitaxial material, or a combination thereof. A conductive field plate is formed above the spacer layer and extends a distance L_f from the edge of the gate contact toward the drain contact. The field plate can be electrically connected to the gate contact. This field plate arrangement can reduce the peak electric field in the device, resulting in increased breakdown voltage and reduced trapping. The reduction of the electric field can also yield other benefits such as reduced leakage currents and enhanced reliability.

[0029] One type of transistor that can utilize the field plate arrangement according to the present invention is a high electron mobility transistor (HEMT), which typically includes a buffer layer and a barrier layer on the buffer layer. A two dimensional electron gas (2DEG) layer/channel is formed at the junction between the buffer layer and the barrier layer. A gate contact is formed on the barrier layer between the source and drain contacts and according to the present invention, a spacer layer is formed on the barrier layer at least between the gate and drain contact. It can also cover the barrier layer between the gate and source contact. The spacer layer can be formed before or after formation of the gate contact. The spacer layer can comprise a dielectric layer, a layer of undoped or depleted material Group III nitride material, or a combination thereof. Different Group III elements can be used in the spacer layer such as alloys of Al, Ga, or In, with a suitable spacer layer material being $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$). A conductive field plate is formed above the spacer layer and extends a distance L_f from the edge of the gate towards the drain contact. In some embodiments, the field plate is formed during the same deposition step as an extension of the gate contact. In other embodiments, the field plate and gate electrode are formed during separate deposition steps. The field plate can be electrically connected to the gate contact. In still other embodiments the field plate can be connected to the source contact.

[0030] Another type of transistor that can utilize a field plate arrangement according to the present invention is a metal semiconductor field effect transistor (MESFET), which typically comprises a buffer layer on a substrate and a channel layer on the buffer layer with the buffer layer between the substrate and channel layer. A source contact is included in ohmic contact with the channel layer and a drain contact is also included in ohmic contact with the channel layer. A space on the channel layer remains between the source and drain contacts with a gate included on the channel layer between the source and drain contacts. A spacer layer is included on the channel layer at least between the gate and drain contact. The spacer layer can also cover the space between the gate and source contact. A field plate is included on the spacer layer and in electrical contact with the gate.

[0031] This field plate arrangement for both the HEMT and MESFET can reduce the peak electric field in the device, compared to a device without a field plate, which can result in increased breakdown voltage and reduced trapping. The reduction of the electric field can also yield other benefits such as reduced leakage currents and enhanced reliability.

[0032] **FIGS. 1 and 2** show one embodiment of a nitride based HEMT **10** according to the present invention that comprises a substrate **12** which can be made of silicon carbide, sapphire, spinet, ZnO, silicon, gallium nitride, aluminum nitride, or any other material capable of supporting growth of a Group-III nitride material. In some embodiments, the substrate **12** can comprise semi-insulating 4H-SiC commercially available from Cree, Inc. of Durham, N.C.

[0033] A nucleation layer **14** can be formed on the substrate **12** to reduce the lattice mismatch between the substrate **12** and the next layer in the HEMT **10**. The nucleation layer **14** should be approximately 1000 angstroms (Å) thick, although other thicknesses can be used. The nucleation layer **14** can comprise many different materials, with a suitable material being $Al_zGa_{1-z}N$ (0<=z<=1). In one embodiment according to the present invention the nucleation layer comprises AlN ($Al_zGa_{1-z}N$,z=1). Nucleation layer **14** can be formed on the substrate **12** using known semiconductor growth techniques such as metal organic chemical vapor deposition (MOCVD), high vapor pressure epitaxy (HVPE) or molecular beam epitaxy (MBE). In still other embodiments, the nucleation layer can be formed as part of another layer in the HEMT **10**, such as the buffer layer (described in detail below).

[0034] The formation of a nucleation layer **14** can depend on the material used for the substrate **12**. For example, methods of forming a nucleation layer **14** on various substrates are taught in U.S. Pat. Nos. 5,290,393 and 5,686,738, each of which are incorporated by reference as if fully set forth herein. Methods of forming nucleation layers on silicon carbide substrates are disclosed in U.S. Pat. Nos. 5,393,993, 5,523,589, and 5,739,554 each of which is incorporated herein by reference as if fully set forth herein.

[0035] The HEMT **10** further comprises a high resistivity buffer layer **16** formed on the nucleation layer **14**, with a suitable buffer layer **16** made of a Group III-nitride material such as $Al_xGa_yIn_{(1-x-y)}N$ (0<=x<=1, 0<=y<=1, x+y<=1). In another embodiment according to the present invention the buffer layer **16** comprises a GaN layer that is approximately 2 μm thick, with part of the layer doped with Fe.

[0036] A barrier layer **18** is formed on the buffer layer **16** such that the buffer layer **16** is sandwiched between the barrier layer **18** and the nucleation layer **14**. Each of the buffer layer **16** and barrier layer **18** can comprise doped or undoped layers of Group III-nitride materials. The barrier layer **18** can comprise one of more layers of different materials such as InGaN, AlGaN, AlN, or combinations thereof. In one embodiment the barrier layer **18** comprises 0.8 nm of AlN and 22.5 nm of $Al_xGa_{1-x}N$ (x≈0.195, as measured by photo luminescence). Exemplary structures are illustrated in U.S. Pat. Nos. 6,316,793, 6,586,781, 6,548,333 and U.S. Published Patent Application Nos. 2002/0167023 and 2003/00020092 each of which is incorporated by reference as though fully set forth herein. Other nitride based HEMT structures are illustrated in U.S. Pat. Nos. 5,192,987 and 5,296,395 each of which is incorporated herein by reference as if fully set forth herein. The buffer and barrier layers **16**, **18** can be made using the same methods used to grow the nucleation layer **14**. A two dimensional electron gas (2DEG) layer/channel **17** is formed at the heterointerface between the buffer and barrier layer **16**, **18**. Electric isolation between the devices is done with mesa etch or ion implementation outside the active HEMT.

[0037] Metal source and drain contacts **20**, **22** are formed making ohmic contact through the barrier layer **18**. A spacer layer **24** can be formed on the surface of the barrier layer **18** between the source and drain contacts **20**, **22**. The spacer layer **24** can comprise a layer of non-conducting material such as a dielectric (SiN or SiO), or a number of different layers of non-conducting materials such as different dielectrics. In alternative embodiments the spacer layer can comprise one or more layers of epitaxial material alone or in combination with layers of dielectric material. The spacer layer can be many different thicknesses, with a suitable range of thicknesses being approximately 0.05 to 0.5 microns. The spacer layer **24** is primarily arranged to allow a field plate to be deposited on it, with the field plate extending from the gate **26** toward the drain contact **22**. Accordingly, in some embodiments according to the present invention the spacer layer **24** can be included only on the surface of the barrier layer **18** between the gate **26** and drain contact **22**.

[0038] In embodiments where the spacer layer **24** covers the barrier layer **18** between the source and drain contacts **20**, **22**, the spacer layer **24** can be etched to the barrier layer **18** and a gate electrode **26** deposited such that the bottom of the gate electrode **26** is on the surface of barrier layer **18**. In embodiments where the spacer layer **24** only covers a portion of the barrier layer **18**, the gate **26** can be deposited on the barrier layer **18** adjacent to the spacer layer **24**. In still other embodiments, the gate **26** can be deposited before the spacer layer **24**.

[0039] A field plate **28** can be formed integral to the gate by the metal forming the gate electrode being patterned to extend across spacer layer **24** so that the top of the gate **26** forms a field plate structure **28** extending a distance Lf away from the edge of gate **26** towards drain **22**. Stated differently, the part of the gate metal resting on the spacer layer **24** forms a field plate **28**. The structure can then be covered with a dielectric passivation layer **30** such as silicon nitride. Methods of forming the dielectric passivation **30** are described in detail in the patents and publications referenced above.

[0040] Electric current can flow between the source and drain contacts **20**, **22** through the 2DEG layer/channel **17** when the gate **26** is biased at the appropriate level. The source and drain contacts **20**, **22** can be made of different materials including but not limited to alloys of titanium, aluminum, gold or nickel. The gate **26** can also be made of different materials including but not limited to gold, nickel, platinum, palladium, iridium, titanium, chromium, alloys of titanium and tungsten, or platinum silicide. The gate **26** can have many different lengths, with a suitable range of gate lengths being 0.01 to 2 microns. In one embodiment according to the present invention a preferred gate length (L_g) is approximately 0.5 microns. In some embodiments, the field plate **28** is formed during the same deposition step as an extension of the gate **26**. In other embodiments, the field plate **28** and gate **26** are formed during separate deposition steps. The formation of source and drain contacts **20**, **22** is described in detail in the patents and publications referenced above.

[0041] The field plate **28** can extend different distances Lf over the barrier layer from the edge of the gate **26** with a

suitable range of distances being 0.1 to 1.5 μm, although other distances can also be used. The field plate **28** can comprise many different conductive materials with a suitable material being a metal, such as the same metal used for the gate **26**. The gate **26** and field plate **28** can be deposited using standard metallization methods.

[**0042**] **FIGS. 3 and 4** show another embodiment of a HEMT **40** according to the present invention that is similar to the HEMT **10** in **FIGS. 1 and 2**. For the same or similar features for the HEMT **40** in **FIG. 3** and **4**, and the figures that follow, the same reference numerals from **FIGS. 1 and 2** will be used. The HEMT **40** comprises a substrate **12**, nucleation layer **14**, buffer layer **16**, 2DEG **17**, barrier layer **18**, source contact **20**, and drain contact **22**. A gate **42** is formed after formation of the barrier layer **18**. A spacer/passivation layer **44** is formed on the device and particularly over the gate **42** and the surface of the barrier layer **18** between the gate **42** and the source and drain contacts **20**, **22**. In other embodiments the spacer/passivation layer can be included only over the gate **42** and the surface of the barrier layer **18** between the gate **42** and the drain contact **22**. A field plate **46** is then formed on the spacer/passivation layer **44** overlapping the gate **42** and extending a distance Lf in the gate-drain region. In the embodiment shown in **FIGS. 3 and 4**, the spacer/passivation layer **44** serves as a spacer layer for the field plate **46**. The overlap of the field plate **46** over the gate **42** and the distance Lf can be varied for optimum results.

[**0043**] The field plate **46** can be electrically connected to gate **42** and **FIG. 3** shows two alternative gate connection structures that can be used, although it is understood that other connection structures can also be used. The field plate **46** can be connected to the gate **42** through a first conductive path **48** running outside the active area of the HEMT **40** to a gate contact **50** that is used to make electrical contact to the gate **42**. A second conductive path **52** (shown in phantom) can also be used that runs outside of the active region of the HEMT **40** on the side opposite the gate contact **50**. The conductive path **52** is coupled between the gate **42** and the field plate **46**. Conductive vias (not shown) can also be used to connect the field plate **46** to the gate **42**, with each vias running between the two through the passivation layer **44**. The vias can be arranged periodically down the field plate **46** to provide for effective current spreading from the gate **42** to the field plate **46**.

[**0044**] As in HEMT **10** in **FIGS. 1 and 2**, the field plate **46** can extend different distances L_f over the barrier layer from the edge of the gate **42**, with a suitable range of distances being 0.1 to 1.5 μm, although other distances can also be used. In some embodiments, the field plate **46** can extend a distance Lf of 0.2 to 1 μm. In other embodiments, the field plate **46** can extend a distance Lf of 0.5 to 0.9 μm. In preferred embodiments, the field plate **46** can extend a distance L_f of approximately 0.7 μm.

[**0045**] **FIG. 5** shows another embodiment of a HEMT **60** according to the present invention that has many features similar to those in HEMTs **10** and **40**, including a substrate **12**, nucleation layer **14**, buffer layer **16**, 2DEG **17**, barrier layer **18**, source contact **20**, and drain contact **22**. HEMT **60**, however, has a gamma (Γ) shaped gate **62** that is particularly adapted to high frequency operation. The gate length is one of the important device dimensions in determining the speed of the device, and with higher frequency devices the gate length is shorter. Shorter gate contacts lead to high resistance that can negatively impact high frequency operation. T-gates are commonly used in high frequency operation, but it can be difficult to achieve a well-coupled placement of a field plate with a T-gate.

[**0046**] The gamma gate **62** provides for low gate resistance and allows for controlled definition of the gate footprint. A spacer/passivation layer **64** is included that covers the gamma gate **62** and the surface of barrier layer **18** between the gamma gate **62** and the source and drain contacts **20**, **22**. A space can remain between the horizontal portion of the gamma gate **62** and the top of the spacer layer. The HEMT **60** also includes a field plate **66** on the spacer layer **64** that overlaps that gamma gate **62**, with the field plate **66** preferably deposited on the side of the gamma gate not having a horizontal overhanging section. This arrangement allows for tight placement and effective coupling between the field plate and the active layers below it.

[**0047**] Like the field plate **46** shown in **FIGS. 3 and 4** and described above, the field plate **66** can be electrically connected to the gate **62** in many different ways. A first conductive path (not shown) can be included between the field plate **66** and the gate contact or a second conductive path (not shown) can be included between field plate **66** and the gate **62**, with both the conductive paths being outside the active area of the HEMT. Conductive vias can also be used between the field plate **66** and gate **62** that pass through the spacer layer **64**.

[**0048**] **FIG. 6** shows another embodiment of a HEMT **80** according to the present invention that is similar to HEMT **10** shown in **FIG. 1**, and also comprises a substrate **12**, nucleation layer **14**, buffer layer **16**, 2DEG **17**, barrier layer **18**, source contact **20**, drain contact **22**, spacer layer **24**, and gate **26** with a field plate structure **28**. The HEMT **80** also includes a doped n^+ contact layer **82** formed on the spacer layer **24**. Prior to formation of gate contact **26**, contact layer **82** is etched to reveal a portion of the surface of spacer layer **24**. A smaller portion of the spacer layer **24** can then be etched down to the barrier layer **18**. The contact layer **82**, spacer layer **24** and barrier layer can also be etched down to the buffer layer **16** so that source and drain contacts **20**, **22** can be deposited. Contact layer **82** facilitates formation of ohmic source and drain contacts **20**, **22** as well as providing low access region resistances.

[**0049**] **FIG. 7** shows another embodiment of a HEMT **90** according to the present invention having a substrate **12**, nucleation layer **14**, buffer layer **16**, 2DEG **17**, barrier layer **18**, source contact **20** and drain contact **22** similar to those in the HEMTs described above. The HEMT **90** also comprises a gate **92** and a field plate **94**. Instead of having a spacer layer, however, the HEMT **90** comprises multiple spacer layers **95**, in this case two, although it is understood that more spacer layers can be used. A first spacer layer **96** is formed on the barrier layer **18** at least between the gate **92** and the drain contact **22**, with a preferred spacer layer also on the barrier layer **18** between the gate **92** and source contact **20**. A second spacer layer **98** is formed on the first spacer layer **96** and can be arranged in many different ways. It preferably covers less than all of the top surface of the first spacer layer **96** to form a step **100**. The field plate **94** is formed on the spacer layers, and because of the step **100**, the

field plate **94** essentially comprises first and second field plates portions **102**, **104** each of which has a different spacing between it and the barrier layer **18**.

[**0050**] The first and second spacer layers **96**, **98** can comprise many different materials, with the layers typically comprising epitaxial materials or dielectric materials, such as SiN and SiO. In one embodiment according to the present invention, the first spacer layer **96** can be an epitaxial material and the second spacer layer **98** can be a dielectric material. In another embodiment the first spacer layer **96** can again be an epitaxial material, and the second spacer layer **98** can also be an epitaxial material of the same or different material as the first spacer layer **96**. It may also be possible to have the first spacer layer **96** comprise a dielectric material and the second spacer layer **98** comprise an epitaxial layer, although depending on the type of dielectric material used it can be difficult to form the second (epitaxial) layer **98** because of crystal structure loss. Better field plate coupling is typically provided using an epitaxial material, but the capacitance introduced by an epitaxial material can be higher than that of a dielectric material.

[**0051**] By having first and second field plates **102**, **104**, the HEMT **90** can exhibit its improved operating characteristics at two different voltages, with the first field plate **102** allowing improved operation of the HEMT **90** at one voltage and the second field plate **104** allowing improved operation at a higher second voltage. For example, in embodiments of the HEMT **90** wherein the first spacer layer **102** is epitaxial (typically AlGaN or similar material), the physical dimensions and dielectric constant of the layer **102** under the first field plate **102** is the same. The consistent dimensions and dielectric constant allow for the first field plate to provide improved HEMT **90** operating characteristics at a first voltage.

[**0052**] If the second layer **98** is made of a dielectric material it generally has a lower dielectric constant than the epitaxial material in the first layer **96**. As a result, the overall dielectric constant of the material under the second field plate **104** will be lower than the dielectric constant of the material under the first field plate **102**. This results in lower capacitance and reduced coupling. The greater distance between the second field plate **104** and the barrier layer **18** along with the lowered dielectric constant results in the second field plate **104** providing improved operating characteristics at a higher voltage.

[**0053**] In those embodiments of the HEMT **90** where the first and second layers **96**, **98** are epitaxial, the dielectric constant below the first and second field plates **102**, **104** remains the same, but the increased distance between the second field plate **104** and barrier layer **18** still provides improved operating characteristics at a higher voltage. The higher operating voltage, however, is typically different than it would be if the second spacer layer were a dielectric material.

[**0054**] The gate **92**, field plate **102**, **104**, and spacer layers **94**, **96** can be formed in many different ways, with one formation method being depositing the first (epitaxial) spacer layer **94** on the barrier layer **18** and then etching the barrier layer to provide a space for the gate **92**. The gate **92** can then be deposited and the second spacer layer **96** can be deposited on the first **96**. In other embodiments the second spacer layer **96** can be etched before deposition of the gate **92**. Alternatively, the first and second spacer layers **96**, **98** can be deposited on then etched in two etch steps; the first etch through both the layers **96**, **98** and the second through the second layer **98** to form the step **100**. The gate **92** can then be deposited and the field plates **102**, **104** can then be deposited over the first spacer and second spacer layers **96**, **98**. Alternatively, the first and second spacer layers **96**, **98** can be formed and then etched with the gate **92** and field plates formed in one or more formation steps. In still other embodiments a single spacer layer of epitaxial or dielectric material can be etched to provide a step such that the resulting field plate has first and second portions.

[**0055**] The gate and field plate structures according to the present invention can be used in many different ways beyond those shown in **FIGS. 1-7** above. **FIGS. 8, 9** and **10** show HEMTs **110**, **130** and **140**, respectively, with each HEMT having a substrate **12**, nucleation layer **14**, buffer layer **16**, 2DEG **17**, barrier layer **18**, source contact **20** and drain contact **22** similar to those in the HEMTs described above. The HEMT **110** (**FIG. 8**) is similar to the HEMT **10** in **FIGS. 1 and 2** except that its gate **112** is recessed in the barrier layer **18**. The HEMT's field plate **114** is deposited on a spacer layer **116** and extend from the gate **112** toward the drain contact **22**. The field plate **114** provides the same operating improvements as the field plate **28** in HEMT **10**. HEMT **130** (**FIG. 9**) is similar to HEMT **40** in **FIGS. 3 and 4** except that the gate **132** is recessed. The field plate **134** is deposited on a spacer layer **136** and provides the same operating benefits. The HEMTs described herein can also comprise gates that are only partially recessed. The HEMT **140** is similar to the HEMT **130** except that its gate **142** is partially recessed. Its field plate **144** is deposited on a spacer layer **146** and provides the same operating benefits.

[**0056**] **FIG. 11** shows still another embodiment of a HEMT **150** according to the present invention having a substrate **12**, nucleation layer **14**, buffer layer **16**, 2DEG **17**, barrier layer **18**, source contact **20** and drain contact **22**. The HEMT **150** also has a gate **152**, spacer layer **154**, and integral field plate **156**. The HEMT **150** further comprises a second spacer layer **158** covering the field plate **156**, spacer layer **154** and portion of the gate **152** above the spacer layer **154**. A second field plate **159** is on the second spacer layer **158** extending generally from the gate **152** toward the drain **22**, with the second field plate electrically coupled to the gate either by one or more vias (not shown) through the second spacer layer **158**, or by one or more conductive paths formed outside of the active region of the HEMT **150**. Other HEMTs according to the present invention can comprise additional spacer layer and field plate pairs, with one additional pair shown in phantom. The structure can also be covered by a dielectric passivation layer (not shown).

[**0057**] A GaN-based HEMT structure in accordance with the embodiment of **FIGS. 3 and 4** was constructed and tested, with the results of the testing shown in the graph **160** of **FIG. 12**. Initial testing showed a power density of 20.4 W/mm with 51% Power Added Efficiency (PAE) operating in class B at 82V and 4 GHz. More recent testing has achieved improved performance with a power density of 32W/mm with 55% PAE at 120V and 4 Ghz.

[**0058**] The effect of field plate distance (L_f) on device performance was tested. The field plate length L_f was varied from a distance of 0 to 0.9 μm and the PAE of the resulting

devices was then measured. As illustrated in **FIG. 12**, the PAE showed improvement once the field plate length was extended to 0.5 μm, with an optimum length of about 0.7 μm. However, the optimum length may depend on the specific device design as well as operating voltage and frequency.

[**0059**] The field plate arrangements described above can be used in other types of transistors. **FIG. 13** shows one embodiment of a metal semiconductor field effect transistor (MESFET) **170** according to the present invention that is preferably silicon carbide (SiC) based, although MESFETs of other material systems can also be used. MESFET **170** comprises a silicon carbide substrate **172** on which a silicon carbide buffer **174** and a silicon carbide channel layer **176** are formed with the buffer **174** sandwiched between the channel layer **176** and substrate **172**. Source and drain contacts **178**, **180** are formed in contact with the channel layer **176**.

[**0060**] A non-conducting spacer layer **182** is formed on the channel layer **176**, between the source and drain contacts **178**, **180**. Similar to the spacer layer **24** described above and shown in **FIGS. 1 and 2**, the spacer layer **182** can comprise a layer of non-conducting material such as a dielectric, or a number of different layers of non-conducting materials such as different dielectrics or epitaxial materials.

[**0061**] Also similar to the spacer layer **24** in **FIGS. 1 and 2**, the spacer layer **182** can be etched to the channel layer **176** and a gate **184** can be deposited such that the bottom of the gate **184** is on the surface of channel layer **176**. The metal forming the gate **184** can be patterned to extend across spacer layer **182** SO that the top of the gate **184** forms a field plate structure **186** extending a distance Lf away from the edge of gate **184** towards drain contact **180**. Finally, the structure can be covered with a dielectric passivation layer **188**, such as silicon nitride.

[**0062**] The fabrication of silicon carbide based MESFET devices is described in more detail in U.S. Pat. No. 5,686,737 and U.S. patent application Ser. No. 09/567,717 filed May 10, 2000 entitled "Silicon Carbide Metal-Semiconductor Field Effect Transistors and Methods of Fabricating Silicon Carbide Metal-Semiconductor Field Effect Transistors" each of which is incorporated herein by reference in its entirety.

[**0063**] **FIG. 14** shows another embodiment of a MESFET **190** according to the present invention that is similar to MESFET **170** in **FIG. 12**, but has a gate and field plate structure similar to that in the HEMT **40** shown in **FIGS. 3 and 4**. MESFET **190** comprises a silicon carbide substrate **172**, buffer **174**, and channel **176**. It also comprises a source contact **178**, drain contact **180**, and a gate **192** deposited on the channel **176**. A spacer layer **194** is deposited over the gate **192** and on the surface of the channel **176** between the gate **192** and the source and drain contacts **178**, **180**. A field plate **186** is deposited on the spacer layer **194** and overlaps the gate **192**. The field plate **196** is coupled to the gate **192** by a conductive path as described above in HEMT **40** of **FIGS. 3 and 4**. Many different conductive paths can be used including a first conductive path to the gate contact (not shown) or a second conductive path (not shown) to the gate **192**, both of which run outside of the MESFET active area. The field **196** can also be coupled to the gate **192** by conductive vias (not shown) through the spacer layer **194**.

[**0064**] Just as with the HEMTs above, different embodiments of MESFETs according to the present invention can comprise recessed gates. **FIG. 15** shows one embodiment of a MESFET **200** according to the present invention, with a recessed gate **202**. Similar to the MESFETs **170** and **190** shown in **FIGS. 12 and 13**, MESFET **200** also has a silicon carbide substrate **172**, buffer **174**, channel **176**, a source contact **178** and a drain contact **180**. The gate **202** deposited on the channel **176**. A spacer layer **204** is deposited over the gate **202** on the surface of the channel **176** between the gate **202** and the source and drain contacts **178**, **180**. The spacer layer **204** is thinner than the spacer layer **194** in **FIG. 14** such that it conforms more closely to the shape of the gate **202**. The gate **202** is partially recessed in the channel **176** and a field plate **206** is deposited on the spacer layer **204**, overlapping the gate **202**. The field plate **206** is coupled to the gate **202** by one or more conductive paths such as those described in HEMT **40** in **FIGS. 3 and 4**.

[**0065**] It is also understood that different embodiments of MESFETs according to the present invention can comprise multiple spacer layers as described HEMT **90** of **FIG. 7**. In some embodiments according to the present invention, the MESFETs can have two spacer layers in a stepped arrangement, although more than two spacer layers can be used. The layers can comprise epitaxial or dielectric materials as also described above, with the stepped arrangement effectively providing two field plates that provide improved operating characteristics at two voltages. It is also understood that MESFETs according to the present invention can also comprise multiple spacer layers and field plates similar to those on the HEMT **150** shown in **FIG. 11** and described above.

[**0066**] Although the present invention has been described in considerable detail with reference to certain preferred configurations thereof, other versions are possible. The field plate arrangement can be used in many different devices. The field plates can also have many different shapes and can be connected to the source contact in many different ways. Accordingly, the spirit and scope of the invention should not be limited to the preferred versions of the invention described above.

We claim:

1. A transistor, comprising:

a plurality of active semiconductor layers formed on a substrate;

a source contact formed in electrical contact with said plurality of active layers;

a drain contact also formed in electrical contact with said plurality of active layers with space between said source and drain contacts on the topmost of said plurality of active layers;

a gate formed in electrical contact with said topmost of said plurality of active layers, between said source and drain contacts;

a spacer layer of epitaxial material formed on the surface of the topmost of said plurality of active layers, between said gate and said drain contact, wherein said gate is not covered by said spacer layer; and

a field plate formed on said spacer layer integral to said gate.

2. The transistor of claim 1, wherein said field plate extends on said spacer layer a distance Lf from the edge of said gate toward said drain contact.

3. The transistor of claim 1, wherein said spacer layer comprises a plurality of spacer layers in a step arrangement between said gate and said drain contact.

4. The transistor of claim 3, wherein said field plate is formed on said spacer layer step arrangement forming a plurality of field plate portions, each of which has a different distance between it and the topmost of said plurality of active layers.

5. The transistor of claim 1, comprising a high electron mobility transistor (HEMT) and wherein said plurality of active layers comprises at least a buffer layer on said substrate and a barrier layer on said buffer layer with a two dimensional electron gas between said buffer and barrier layer, said barrier layer being the topmost of said plurality of active layers.

6. The transistor of claim 1, wherein said HEMT is gallium nitride based.

7. The transistor of claim 5, further comprising a nucleation layer between that said buffer layer and said substrate.

8. The transistor of claim 1, comprising a metal semiconductor field effect transistor (MESFET) wherein said plurality of active layers comprises at least a buffer layer on said substrate and a channel layer on said buffer layer, said channel layer being the topmost of said plurality of active layers.

9. The transistor of claim 8, wherein said MESFET is silicon carbide based.

10. The transistor of claim 1, wherein said gate is gamma shaped.

11. The transistor of claim 1, wherein said field plate provides a reduction in the peak operational electric field compared to a similar transistor without said field plate.

12. The transistor of claim 1, wherein said gate is at least partially recessed in said topmost of said plurality of active layers.

13. The transistor of claim 1, further comprising a passivation layer covering the at least some of the exposed surfaces of said transistor.

14. The transistor of claim 1, further comprising a second spacer layer covering said field plate and the surface of said spacer layer between said field plate and drain contact, and further comprising a second field plate on said second spacer layer and extending from the edge of said gate toward said drain contact.

15. The transistor of claim 1, further comprising at least one additional spacer layer and field plate pair over said spacer layer and field plate.

16. A transistor, comprising:

a plurality of active semiconductor layers formed on a substrate;

a source contact formed in electrical contact with said plurality of active layers;

a drain contact also formed in electrical contact with said plurality of active layers with space between said source and drain contacts on the topmost of said plurality of active layers;

a gate formed in electrical contact with said topmost of said plurality of active layers, between said source and drain contacts;

a spacer layer formed on the surface of the topmost of said plurality of active layers, between said gate and said drain contact and covering said gate contact; and

a field plate formed on said spacer layer and electrically connected to said gate.

17. The transistor of claim 16, wherein said field plate at least partially overlaps said gate and extends on said spacer layer toward said drain contact.

18. The transistor of claim 16, further comprising one or more conductive vias running between said gate and field plate through said through said spacer layer, said vias providing said field plate electrical connection with said gate.

19. The transistor of claim 16, further comprising one or more conductive paths between said field plate and gate, each said path running outside of said spacer layer and providing said field plate electrical connection with said gate.

20. The transistor of claim 16, wherein said spacer layer comprises a plurality of spacer layers in a step arrangement between said gate and said drain contact.

21. The transistor of claim 20, wherein said field plate is formed on said spacer layer step arrangement forming a plurality of field plate portions, each of which has a different distance between it and the topmost of said plurality of active layers.

22. The transistor of claim 16, comprising a high electron mobility transistor (HEMT) and wherein said plurality of active layers comprises at least a buffer layer on said substrate and a barrier layer on said buffer layer with a two dimensional electron gas between said buffer and barrier layer, said barrier layer being the topmost of said plurality of active layers.

23. The transistor of claim 22, wherein said HEMT is gallium nitride based.

24. The transistor of claim 22, further comprising a nucleation layer between that said buffer layer and said substrate.

25. The transistor of claim 16, comprising a metal semiconductor field effect transistor (MESFET) wherein said plurality of active layers comprises at least a buffer layer on said substrate and a channel layer on said buffer layer, said channel layer being the topmost of said plurality of active layers.

26. The transistor of claim 25, wherein said MESFET is silicon carbide based.

27. The transistor of claim 16, wherein said gate is gamma shaped.

28. The transistor of claim 16, wherein said field plate provides a reduction in the peak operational electric field compared to a similar transistor without said field plate.

29. The transistor of claim 16, wherein said gate is at least partially recessed in said topmost of said plurality of active layers.

30. The transistor of claim 16, further comprising a passivation layer covering the at least some of the exposed surfaces of said transistor.

31. A transistor structure, comprising:

an active semiconductor layer;

metal source and drain contacts formed in electrical contact with said active layer;

a gate contact formed between said source and drain contacts for modulating electric fields within said active layer;

a spacer layer is formed above the active layer; and

a conductive field plate formed above said spacer layer and extending a distance Lf from the edge of said gate contact toward said drain contact, said field plate electrically connected to said gate contact.

32. The transistor structure of claim 31, wherein said field plate provides a reduction in the peak operational electric field compared to a similar transistor structure without said field plate.

33. The transistor structure of claim 31, wherein said spacer layer comprises a dielectric layer, a layer of undoped or depleted with bandgap material, or a combination thereof.

34. A transistor, comprising:

an active semiconductor layer; metal source and drain contacts formed in electrical contact with said active layer;

a gate contact formed between said source and drain contacts for modulating electric fields within said active layer; and

a conductive field plate formed above said spaced above said active semiconductor layer and extending a distance L_f from the edge of said gate contact toward said drain contact, said field plate electrically connected to said gate contact and providing a reduction in the peak operational electric field is said transistor compared to a similar transistor without said field plate.

35. A transistor, comprising:

a plurality of active semiconductor layers formed on a substrate;

source and drain contacts formed in electrical contact with said plurality of active layers;

a gate formed in electrical contact with said topmost of said plurality of active layers, between said source and drain contacts;

a first spacer layer formed on the surface of the topmost of said plurality of active layers, between said gate and said drain contact, wherein said gate is not covered by said spacer layer;

a first field plate formed on said spacer layer integral to said gate and extending toward said drain contact on said spacer layer; and

a second spacer layer covering said field plate and the surface of said spacer layer between said field plate and drain contact, and further comprising a second field plate on said second spacer layer and extending from the edge of said gate toward said drain contact.

36. The transistor of claim 1, wherein said first and second field plates are electrically connected to said gate.

37. The transistor of claim 1, further comprising at least one additional spacer layer and field plate pair over said second spacer layer and second field plate, wherein each field plate in said pairs is electrically connected to said gate.

38. A metal semiconductor field effect transistor (MESFET), comprising:

a buffer layer on a substrate;

a channel layer on said buffer layer;

a source and drain contacts formed in electrical contact with said channel layer;

a gate formed in electrical contact with said channel layer, between said source and drain contacts;

a spacer layer formed on the surface of said channel layer at least between said gate and said drain contact; and

a field plate formed on the spacer layer in electrical contact with said gate.

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