

Wide-Band CMOS Cascode Low-Noise Amplifier Design Based on Source Degeneration Topology

Jongrit Lerdworatawee, *Student Member, IEEE*, and Won Namgoong, *Member, IEEE*

Abstract—A design methodology for a wide-band CMOS low noise amplifier (LNA) with source degeneration is presented. By allowing an arbitrary source degeneration and employing a general input matching network, the proposed wide-band CMOS LNA can be shown for any choice of transistor width to achieve the minimum noise figure at all frequencies of interest. The transistor width simply affects the gain of the LNA at the cost of power dissipation. These results apply uniquely to CMOS LNAs, as they are derived from a quasi-static MOSFET model. To validate these design concepts, a wide-band LNA was realized in 0.25- μm CMOS technology. The measured noise figure ranges from 2.7 to 3.7 dB over 3.2–4.8 GHz with power consumption of 20 mW. A close agreement with the theoretical results is observed.

Index Terms—Active circuits, broadband amplifier, CMOS analog integrated circuits, communication circuits, integrated circuit noise, low-noise design, receiver.

I. INTRODUCTION

THE primary objective in the design of the low-noise amplifier (LNA) is to achieve sufficiently large gain and low noise figure to suppress the additive noise at the subsequent stages. In most systems, this objective should be achieved while constraining the LNA input to provide an impedance of generally 50 Ω to avoid signal distortion caused by impedance mismatch. To provide a 50- Ω input termination, common wide-band LNAs use either a resistive termination by connecting a resistor in parallel at the input of the amplifier or employ a negative parallel resistive feedback. In both approaches, the presence of the resistor has a deleterious effect on the amplifier's noise figure. Furthermore, the latter architecture suffers from potential instability [1].

In narrow-band systems, low noise figure is achieved by employing an inductive source degeneration to present a 50- Ω input resistance without the resistive thermal noise. To satisfy the input power matching condition, another inductor is placed at the gate of the MOSFET to resonate at the desired frequency, which is typically at the carrier frequency [2], [3]. Although low noise figure can be achieved, this technique is only suitable for narrow-band applications.

This paper extends the design approach for narrow-band LNA with source degeneration to wide-band systems. The main dif-

ference is that in the proposed approach an arbitrary source degeneration and a general lossless matching network at the gate are employed. When the noise figure of the proposed LNA architecture is minimized constrained to input power matching condition, our analysis shows that the minimum noise figure can be made independent of the transistor width by properly choosing the source degeneration reactance. This result applies uniquely to CMOS LNA, since the analysis is based on the quasi-static MOSFET model. Our analysis result suggests that the proposed architecture is effective as a wide-band LNA, since the minimum noise figure can be achieved at all frequencies of interest using the same transistor. The transistor width simply affects the gain of the LNA at the cost of power dissipation. To validate this concept, a wide-band LNA has been designed in 0.25- μm CMOS at the target frequency range of 3.2–4.8 GHz.

The paper is organized as follows. Section II presents the fundamental noise theory for a common source MOSFET amplifier with source degeneration. Design considerations for the wide-band LNAs are presented in Section III. Section IV presents the LNA implementation issues and a detailed discussion of the experimental results. Conclusions are drawn in Section V.

II. NOISE THEORY FOR MOSFET AMPLIFIERS

A. Two-Port Circuit Model of Noisy MOSFET

The general block diagram of a LNA is shown in Fig. 1(a), where two identical MOSFETs M1 and M2 form a cascode amplifier and the input and output matching networks are assumed to be lossless. The advantage of this topology is that the Miller effect at the gate–drain capacitance in M1 is small, and M2 has a high output impedance at its drain, improving reverse isolation and, as a result, the stability of the LNA. In this paper, the quasi-static MOSFET model is employed to account for the high-field effects in short-channel devices [4]. The equation for the drain current is given by

$$I_d = \begin{cases} 2v_{\text{sat}}C_{\text{ox}}W \frac{(V_{\text{od}} - V_{\text{ds}}/2)V_{\text{ds}}}{(V_{\text{ds}} + L\varepsilon_{\text{sat}})}, & V_{\text{ds}} \leq V_{\text{dsat}} \\ v_{\text{sat}}C_{\text{ox}}W \frac{V_{\text{od}}^2}{V_{\text{od}} + L\varepsilon_{\text{sat}}}, & V_{\text{ds}} \geq V_{\text{dsat}} \end{cases} \quad (1)$$

where W and L are the gate width and length, C_{ox} is the gate oxide capacitance per unit area, and $v_{\text{sat}} (= \mu_{\text{eff}}\varepsilon_{\text{sat}}/2)$ is the saturation velocity with μ_{eff} and ε_{sat} denoting the effective electron mobility and the saturation electric field, respectively. In (1), $V_{\text{od}} (= V_{\text{gs}} - V_{\text{th}})$ is the gate overdrive voltage, V_{gs} is the gate–source voltage, V_{th} is the threshold voltage, V_{ds} is the drain–source voltage, and V_{dsat} is the drain–source saturation voltage, which is given by

$$V_{\text{dsat}} = \frac{V_{\text{od}}L\varepsilon_{\text{sat}}}{V_{\text{od}} + L\varepsilon_{\text{sat}}}. \quad (2)$$

Manuscript received June 8, 2004; revised November 1, 2004 and February 1, 2005. This work was supported in part by the Army Research Office under Contract DAAD19-01-1-0477, by the National Science Foundation under Grant ECS-0134629, and by the Semiconductor Research Corporation under Contract 2001-HJ-895. This paper was recommended by Associate Editor W. A. Serdijn.

The authors are with the Department of Electrical Engineering, University of Southern California, Los Angeles, CA 90089 USA (e-mail: lerdwora@usc.edu; namgoong@usc.edu).

Digital Object Identifier 10.1109/TCSI.2005.853585

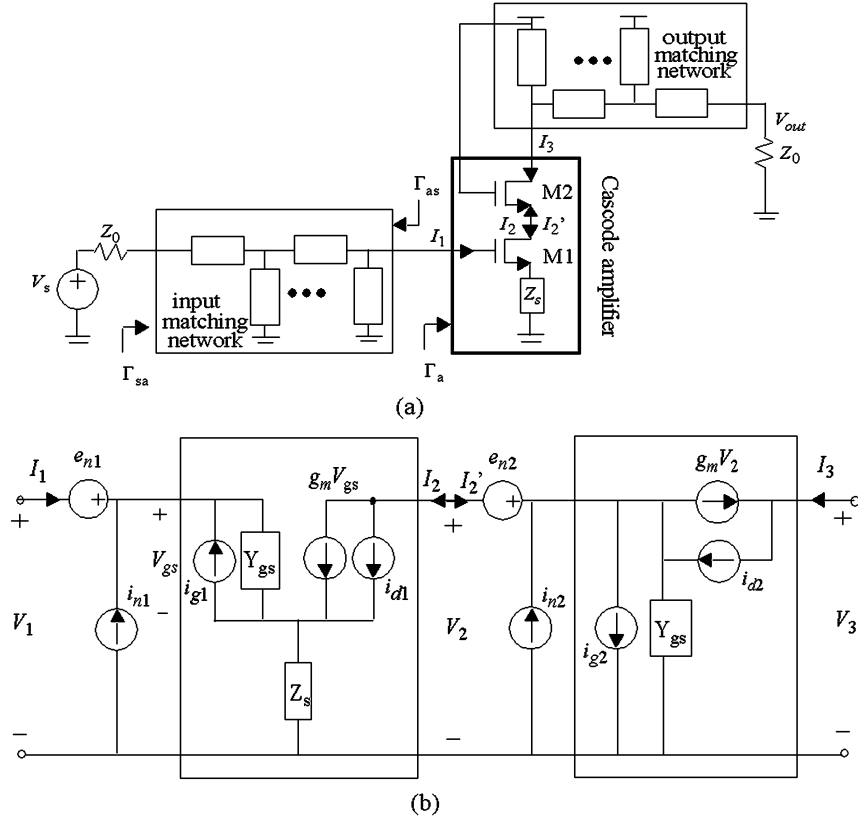


Fig. 1. LNA with reactive degeneration. (a) Block diagram. (b) Noisy small-signal model of the cascode amplifier.

Differentiating (1) in the saturation region with respect to V_{gs} and in the linear region with respect to V_{ds} when $V_{ds} = 0$ yields the ac characteristics of MOSFET, i.e., transconductance g_m and the zero-bias drain conductance g_{d0} ,

$$g_m = 2v_{sat}C_{ox}W \left[\frac{\rho(1 + \frac{\rho}{2})}{(1 + \rho)^2} \right] \quad (3)$$

$$g_{d0} = 2v_{sat}C_{ox}W\rho \quad (4)$$

where $\rho = (V_{gs} - V_{th})/L\varepsilon_{sat}$ is referred to as the normalized gate overdrive.

Fig. 1(b) presents the noisy small-signal model of the cascode amplifier block in Fig. 1(a), where the series feedback at the source of M1 is modeled as $Z_s = jX_s$ and the admittance between the gate and source of M1 is $Y_{gs} = jB_{gs}$ ($= j\omega C_{gs}$ where $C_{gs} = (2/3)C_{ox}WL$). In this paper, the noise of MOSFET consists of the induced gate noise i_g and the channel noise i_d [5]. These current noises are partially correlated because they share a common origin and possess the power spectral densities (PSD) as given by

$$S_{i_g}(\omega) = 4kT \frac{\delta\omega^2 C_{gs}^2}{5g_{d0}} \quad (5)$$

$$S_{i_d}(\omega) = 4kT\gamma g_{d0} \quad (6)$$

$$S_{i_g i_d}(\omega) = c\sqrt{S_{i_g}(\omega)S_{i_d}(\omega)} \quad (7)$$

where $k (= 1.38 \times 10^{-23} \text{ J/K})$ is the Boltzmann constant, T is the absolute temperature, δ and γ are the coefficients of the channel and gate noise, and c is referred to as the correlation

coefficient. In this paper, γ , δ , and c are assumed to be 2.5, 5 and $j0.395$, respectively [6].

To systematically analyze the signal and noise behavior of the cascode amplifier with source degeneration, the combined noisy two-port network model (defined according to [7]) for the two stages of the cascode amplifier can be shown to be

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} + \begin{bmatrix} e_n \\ i_n \end{bmatrix} = \begin{bmatrix} 0 & \left\{ -jX_s - \frac{(1-X_sB_{gs})}{g_m} \right\} \left(1 + \frac{jB_{gs}}{g_m} \right) \\ 0 & \frac{-jB_{gs}}{g_m} \left(1 + \frac{jB_{gs}}{g_m} \right) \end{bmatrix} \begin{bmatrix} V_3 \\ -I_3 \end{bmatrix} \quad (8)$$

where V_1 and V_3 (I_1 and I_3) are, respectively, the input and output voltages (currents) [see Fig. 1(b)]. In (8), e_n and i_n are the input-referred noise voltage and current of the cascode amplifier. Assuming that the transistors in the two stages of the cascode amplifier are of equal size so that they share the common ac characteristics and identical (but independent) noise statistics, e_n and i_n can be computed as given by

$$\begin{bmatrix} e_n \\ i_n \end{bmatrix} = \begin{bmatrix} jX_s & \frac{(1-X_sB_{gs})}{g_m} \\ 1 & \frac{jB_{gs}}{g_m} \end{bmatrix} \begin{bmatrix} i_{g1} \\ i_{d1} \end{bmatrix} + \begin{bmatrix} 0 & jX_s + \frac{(1-X_sB_{gs})}{g_m} \\ 0 & \frac{jB_{gs}}{g_m} \end{bmatrix} \begin{bmatrix} i_{g2} \\ i_{d2} \end{bmatrix} \quad (9)$$

where the subscripts gi and di refer to the gate and drain noise in the i th stage of the cascode amplifier.

Using the gate noise PSD, drain noise PSD, and their cross PSD [given in (5)–(7)], the noise correlation matrix (M) can be obtained by taking the expectation of the product of the input-referred noise vector [as given in (9)] and its Hermitian transpose, i.e.,

$$M = E \left\{ \begin{bmatrix} e_n \\ i_n \end{bmatrix} \begin{bmatrix} e_n \\ i_n \end{bmatrix}^H \right\} = S_{ig} \begin{bmatrix} m_{11} & m_{12} \\ m_{12}^* & m_{22} \end{bmatrix} \quad (10)$$

where m_{11} , m_{12} , and m_{22} are given by (11), shown at the bottom of the page. In (11), α and the angular cut-off frequency ω_T are

$$\alpha = \frac{g_m}{g_{d0}} = \frac{1 + \frac{\rho}{2}}{(1 + \rho)^2} \quad (12)$$

$$\omega_T = \frac{g_m}{C_{gs}} = \frac{3v_{sat}}{2L} \left[1 - \frac{1}{(1 + \rho)^2} \right] \quad (13)$$

where the second equality in (12) and (13) are obtained using (3) and (4). Note that both α and ω_T are dependent on ρ only for a given L .

B. Expressions for Four Noise Parameters

To derive the system noise figure, the noise parameters are first computed, i.e., the minimum noise figure F_{min} , the noise resistance R_n , and the optimum admittance Y_{opt} ($= G_{opt} + jB_{opt}$). With M specified in the preceding section, the noise parameters can be determined by [8]

$$F_{min} = 1 + \frac{S_{ig}}{2kT} \times \left(\Re e(m_{12}) + \sqrt{m_{11}m_{22} - (\Im m(m_{12}))^2} \right) \quad (14)$$

$$Y_{opt} = \frac{\sqrt{m_{11}m_{22} - (\Im m(m_{12}))^2} + j\Im m(m_{12})}{m_{11}} \quad (15)$$

$$R_n = \frac{S_{ig} m_{11}}{4kT}. \quad (16)$$

Substituting (11) into (14)–(16), the noise parameters can be obtained. For ease of analysis, a reasonable approximation is made by neglecting the high-order terms of ω/ω_T , since MOSFETs typically operate at frequencies well below the cutoff frequency (i.e., $\omega/\omega_T \ll 1$). As a result, terms involving $(\omega/\omega_T)^2$ in (11) can be neglected with little loss in accuracy. The noise parameters then become

$$F_{min} = 1 + \frac{2\omega}{\omega_T} \sqrt{\frac{\delta\gamma}{5}} (1 - |c|^2) \quad (17)$$

$$R_n = \frac{\gamma}{\alpha^2 g_{d0}} \times [1 - 2u_1(X_s B_{gs}) + (u_1^2 + u_2^2)(X_s B_{gs})^2] \quad (18)$$

$$Y_{pot} = B_{gs} \times \left\{ \frac{u_2 + j[(u_1^2 + u_2^2)(X_s B_{gs}) - u_1]}{1 - 2u_1(X_s B_{gs}) + (u_1^2 + u_2^2)(X_s B_{gs})^2} \right\} \quad (19)$$

where the coefficients u_1 and u_2 are given by

$$u_1 = 1 + \sqrt{\frac{\delta(\alpha|c|^2)^2}{5\gamma}} \quad (20)$$

$$u_2 = \sqrt{\frac{\delta\alpha^2}{5\gamma}} (1 - |c|^2).$$

It is worth noting that, as γ , δ , and c are constants (at least for the 0.25- μ m CMOS technology [9]), u_1 and u_2 are independent of W . Furthermore, since ω_T is dependent on ρ only [assuming minimum L ; see (13)], F_{min} is also independent of W . As explained shortly, this independence will become relevant in the design of wide-band CMOS LNAs.

C. Expression for Noise Figure Given a Perfect Power Match

Having computed the four noise parameters and denoting the admittance of the matching network as seen by the amplifier as Y_{as} [$= G_{as} + jB_{as}$, as shown in Fig. 1], the noise figure F can be obtained using the following equation:

$$F = F_{min} + \frac{R_n}{G_{as}} [(G_{as} - G_{opt})^2 + (B_{as} - B_{opt})^2]. \quad (21)$$

$$m_{11} = |c|^2 \left[X_s - \sqrt{\frac{5\gamma}{\delta(\alpha|c|^2)}} \frac{(1 - X_s B_{gs})}{B_{gs}} \right]^2 + (1 - |c|^2) X_s^2 + \left(1 + \sqrt{\frac{5\gamma}{\delta\alpha^2}} \right) \left(\frac{\omega}{\omega_T} \right)^2 \left[\left(X_s - \frac{1}{B_{gs}} \right)^2 + \left(\frac{g_m X_s}{B_{gs}} \right)^2 \right]$$

$$m_{12} = j|c|^2 \left(1 + \sqrt{\frac{5\gamma}{\delta(\alpha|c|^2)^2}} \right) \left[X_s - \sqrt{\frac{5\gamma}{\delta(\alpha|c|^2)}} \frac{(1 - X_s B_{gs})}{B_{gs}} \right] + j(1 - |c|^2) X_s$$

$$+ \left(1 + \sqrt{\frac{5\gamma}{\delta\alpha^2}} \right) \left(\frac{\omega}{\omega_T} \right)^2 \left[\frac{g_m X_s}{B_{gs}} + j \left(X_s - \frac{1}{B_{gs}} \right) \right]$$

$$m_{22} = |c|^2 \left(1 + \sqrt{\frac{5\gamma}{\delta(\alpha|c|^2)^2}} \right)^2 + (1 - |c|^2) + \left(1 + \sqrt{\frac{5\gamma}{\delta\alpha^2}} \right) \left(\frac{\omega}{\omega_T} \right)^2 \quad (11)$$

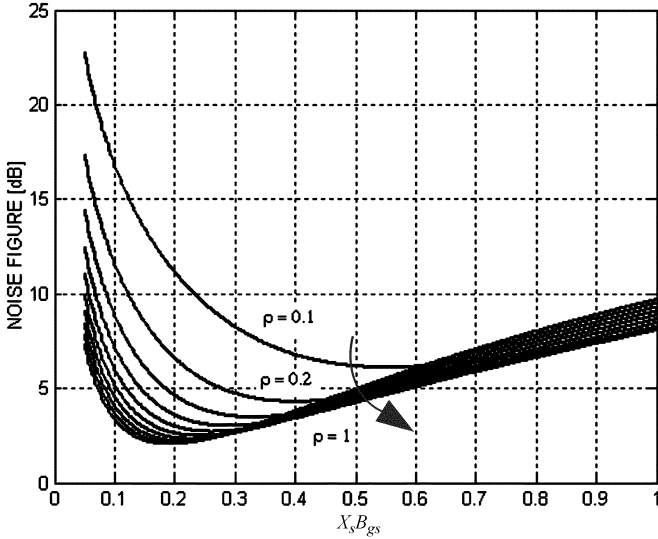


Fig. 2. Effect of $X_s B_{gs}$ on the noise performance for varying ρ values at 4 GHz.

Note that perfect power matching occurs when Y_{as} is the complex conjugate of the amplifier's input admittance Y_a , i.e.,

$$Y_a = \left(\frac{g_m X_s}{B_{gs}} + jX_s + \frac{1}{jB_{gs}} \right)^{-1} = B_{gs} \left\{ \frac{\frac{\omega_T}{\omega} (X_s B_{gs}) + j(1 - X_s B_{gs})}{1 - 2(X_s B_{gs}) + \left[1 + \left(\frac{\omega_T}{\omega} \right)^2 \right] (X_s B_{gs})^2} \right\}. \quad (22)$$

Substituting $Y_{as} [= Y_a^*]$, as given in (22) and the four noise parameters [as given in (17)–(19)] into (21) yields the noise figure of the LNA that achieves the input power match. After tedious but straightforward algebraic manipulations, the LNA noise figure given the input power match, which we denote as F_{match} , can be shown to be

$$F_{match} = F_{min} + \frac{\gamma}{\alpha} \left(\frac{\omega}{\omega_T} \right)^2 \frac{(U_1^2 + U_2^2)}{U_3 U_4 U_5} \quad (23)$$

where $\{U_i\}$ for $i \in \{1, \dots, 5\}$ are the polynomial of $X_s B_{gs}$ as given by

$$\begin{aligned} U_1 &= u_2 - \left(\frac{\omega_T}{\omega} + 2u_2 \right) (X_s B_{gs}) \\ &\quad + \left[2 \frac{\omega_T}{\omega} u_1 + u_2 \left(1 + \frac{\omega_T^2}{\omega^2} \right) \right] (X_s B_{gs})^2 \\ &\quad - \left(\frac{\omega_T}{\omega} \right) (u_1^2 + u_2^2) (X_s B_{gs})^3 \\ U_2 &= (1 - u_1) - [1 - (u_1^2 + u_2^2)] (X_s B_{gs}) \\ &\quad + \left[u_1 \left(1 - \frac{\omega_T^2}{\omega^2} \right) - (u_1^2 + u_2^2) \right] (X_s B_{gs})^2 \\ &\quad + \left(\frac{\omega_T}{\omega} \right)^2 (u_1^2 + u_2^2) (X_s B_{gs})^3 \\ U_3 &= (X_s B_{gs}) \\ U_4 &= 1 - 2(X_s B_{gs}) + \left[1 + \left(\frac{\omega_T}{\omega} \right)^2 \right] (X_s B_{gs})^2 \\ U_5 &= 1 - 2u_1(X_s B_{gs}) + (u_1^2 + u_2^2) (X_s B_{gs})^2. \end{aligned} \quad (24)$$

As F_{min} and $\{u_j\}$ (for $j \in \{1, 2\}$) are independent of W (as shown in the previous subsection), (23) suggests that F_{match}

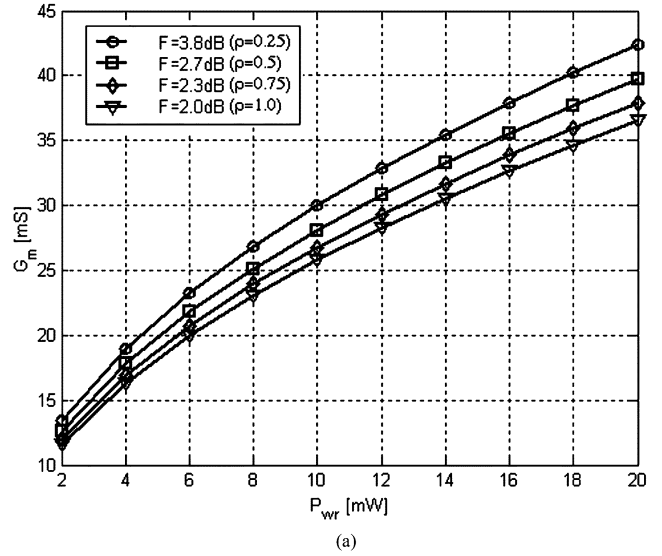
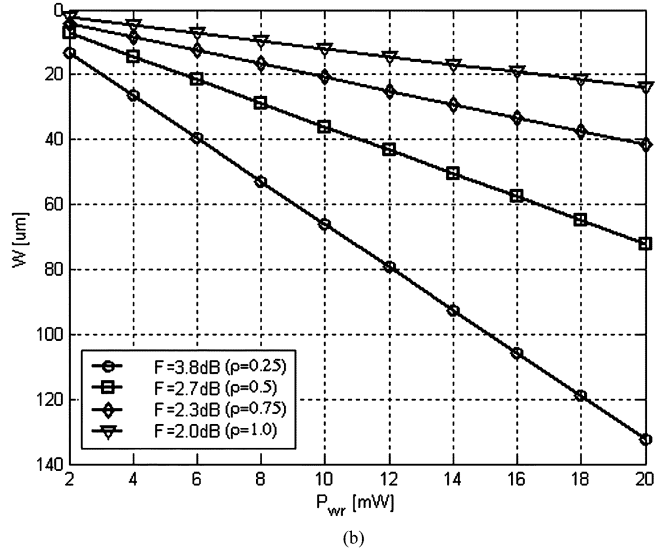
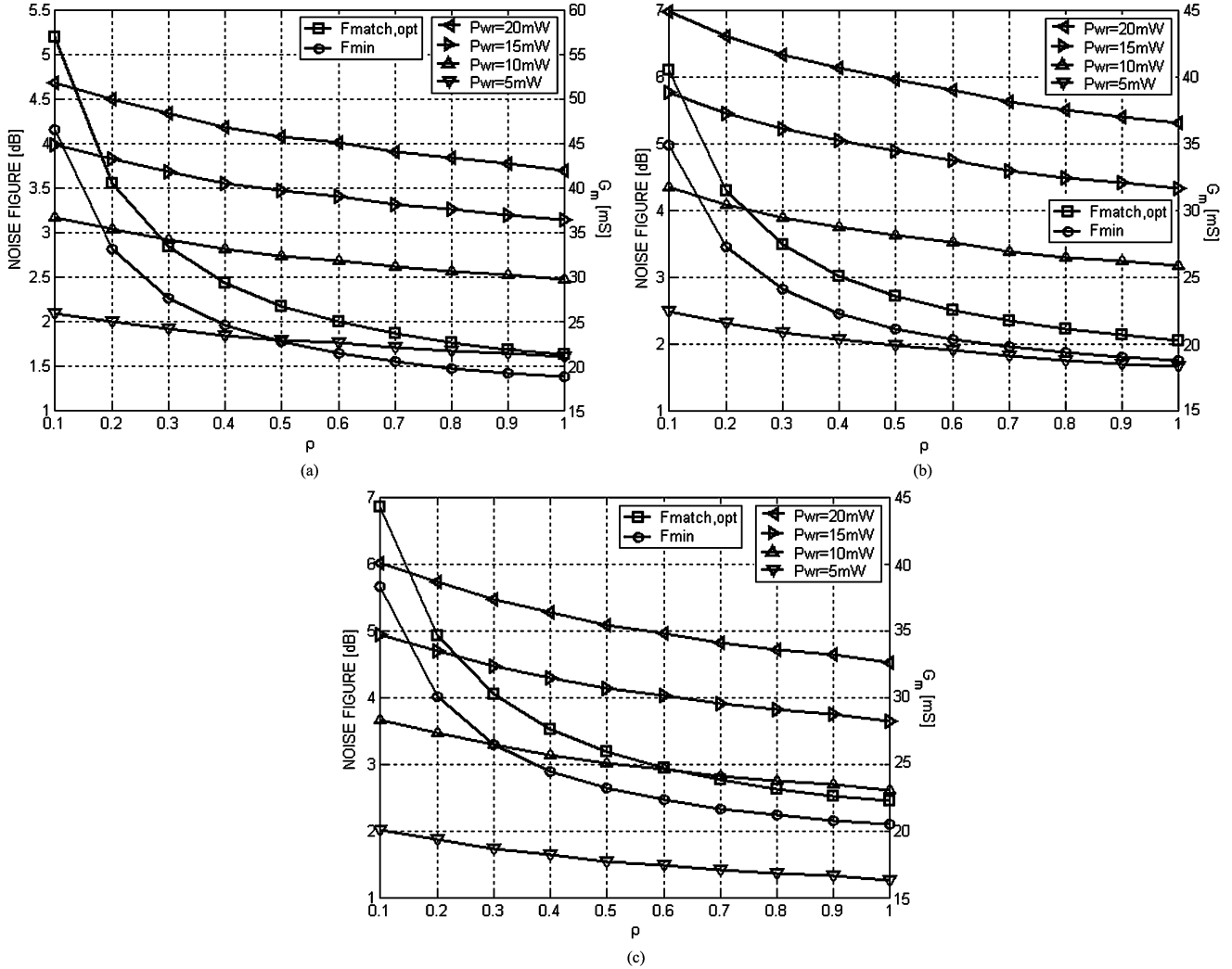


Fig. 3. Plots of (a) G_m versus P_{wrf} and (b) W versus P_{wrf} for different $F_{match,opt}$ (or ρ) values at 4 GHz.

becomes a function of the product $X_s B_{gs}$ only when the bias voltage ρ and the operating frequency ω are specified. This dependency of F_{match} on the product $X_s B_{gs}$ suggests that the LNA can be designed to satisfy the optimum $X_s B_{gs}$ that minimizes F_{match} regardless of W (which affects $B_{gs} = \omega C_{gs}$) by appropriately selecting X_s . This is an important result for wide-band CMOS LNA design because it means that, for any W chosen to satisfy a given power dissipation constraint, the LNA can achieve the minimum F_{match} over the frequency range of interest, since X_s can be adjusted to yield the optimum $X_s B_{gs}$ at each frequency. As this dependency of F_{match} on $X_s B_{gs}$ is derived for the quasi-static MOSFET model given in (1), the result that the minimum F_{match} can be achieved at all frequencies of interest is unique to a CMOS LNA.

III. DESIGN CONSIDERATIONS FOR WIDE-BAND LNAS

The wide-band LNA design objective is to choose the MOSFET parameters (i.e., size W and bias ρ) and the source


 Fig. 4. Plots of $F_{\text{match,opt}}$ and G_m subject to the power dissipation constraint at (a) 3, (b) 4, and (c) 5 GHz.

degeneration reactance X_s that minimize the noise figure over a frequency band of interest subject to power dissipation and input power matching constraints. The matching network at the gate is not a design parameter, since it is determined given X_s , W , and ρ . In this section, the role of each design parameter is described.

As discussed in the preceding section, F_{match} [as in (23) and (24)] is a function of $X_s B_{gs}$ only when ρ and ω are fixed. Fig. 2 plots F_{match} against $X_s B_{gs}$ for ρ ranging from 0.1 to 1 at 4 GHz. For a specific ρ , the minimum F_{match} (which we denote as $F_{\text{match,opt}}$) is achieved at the optimum $X_s B_{gs}$, as shown in Fig. 2, which the LNA can be designed to satisfy independent of W by appropriately selecting X_s . Furthermore, regardless of how the optimum $X_s B_{gs}$ varies with frequency, the LNA can achieve $F_{\text{match,opt}}$ at each frequency of interest by appropriately choosing X_s .

Although the proposed LNA is able to achieve $F_{\text{match,opt}}$ at all frequencies independent of W , the choice of W affects the LNA gain. From Fig. 1, the effective transconductance G_m given the input power match can be computed as

$$G_m = \frac{|I_3|}{|V_s|} = \frac{1}{2} \sqrt{\frac{\omega_T}{\omega Z_0 X_s}} = \frac{1}{2} \sqrt{\frac{2\omega_T C_{ox} L W}{3(X_s B_{gs}) Z_0}} \quad (25)$$

where Z_0 is the characteristic impedance (or 50 Ω). The last equality in (25) is obtained by multiplying B_{gs} both at the numerator and denominator. As is clear from (25), increasing W increases G_m . This increase in G_m , however, is at the expense of increasing power dissipation P_{wr} for a given ρ (or V_{od}), as can be seen from (1). Hence, the choice of W has no bearing on $F_{\text{match,opt}}$ but affects G_m and P_{wr} . The relation between G_m and P_{wr} is shown in Fig. 3(a) for different ρ (or $F_{\text{match,opt}}$) values at 4 GHz. In Fig. 3(b), the increase in W as a function of P_{wr} is also plotted for reference.

When P_{wr} is fixed, the role of ρ is to affect the tradeoff between $F_{\text{match,opt}}$ and G_m . As can be seen from Fig. 3, increasing ρ gradually decreases $F_{\text{match,opt}}$. However, G_m is also decreased, because as ρ increases, W must be reduced to keep the drain current (and as a result P_{wr}) constant [see (1)], which in turn reduces G_m according to (25). The dependency of $F_{\text{match,opt}}$ and G_m is illustrated in Fig. 4(a)–(c), which plot $F_{\text{match,opt}}$, F_{min} and G_m as a function of ρ at 3, 4, and 5 GHz.

As is clear from Fig. 4 as well as from (25), G_m decreases with increasing frequency. This suggests that adding an inductor at the drain of the transistor may be necessary to achieve an

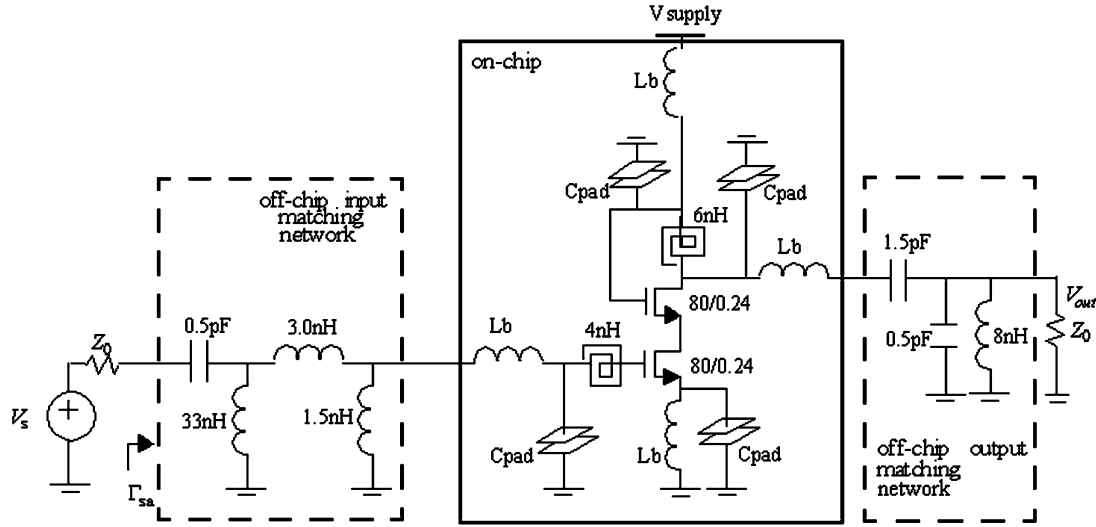


Fig. 5. Complete schematic of the LNA testing setup (biasing not shown).

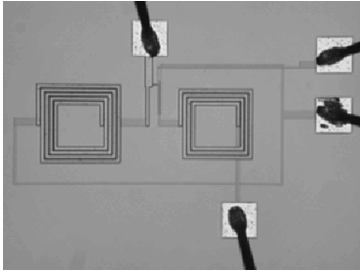


Fig. 6. Die photograph of the LNA IC.

approximately flat gain over the frequency band of interest. In fact, the LNA design described in the following section employs an inductor at the drain to compensate for the reduction in G_m with increasing frequency.

IV. MEASURED RESULTS

To validate the proposed wide-band CMOS LNA design concept, a 3.2–4.8-GHz LNA was implemented in TSMC 0.25- μm CMOS technology. This frequency band is selected, as it represents the likely operating band of the first generation ultra-wide-band (UWB) radio [10], [11]. A complete schematic of the test system is illustrated in Fig. 5 and the die photograph is shown in Fig. 6. The LNA was designed for a target power consumption of 20 mW. As a good compromise between $F_{\text{match,opt}}$ and G_m , ρ is selected to be 0.4 (or equivalently $V_{\text{gs}} = 1\text{ V}$), which represents the knee region of the noise figure curves in Fig. 4. The corresponding transistor size is $80\text{ }\mu\text{m}/0.24\text{ }\mu\text{m}$.

Having sized and biased the transistor, the next step is to design the source degeneration X_s that satisfies the optimum $X_s B_{\text{gs}}$ over the frequency range of interest. As shown in Fig. 7, the optimal X_s turns out to be relatively flat over 3–5 GHz. To reduce the complexity of the source degeneration, the optimal X_s was approximated with an inductor. The inductor size was chosen based on Fig. 8, which plots the noise figure as a function of the inductor size at 3, 4, and 5 GHz. The minimum in each of the three frequencies is relatively broad with a 1-nH in-

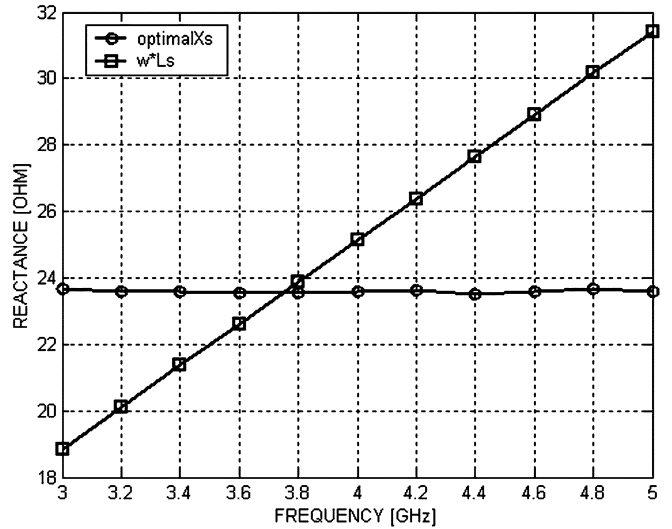


Fig. 7. Plots of the optimal source-degeneration reactance and a single inductor of 1 nH used to approximate the former.

ductor achieving a noise figure close to the minimum in all three frequencies. Hence, the LNA uses a 1-nH inductor, which was realized using a bonding wire. It is worth noting that the selection of a 1-nH inductor is for $W = 80\text{ }\mu\text{m}$, and a different inductance value may be needed for a different choice of W (or power dissipation requirement). After approximating the optimal X_s , the input matching network is designed to satisfy the input matching constraint. The input matching network is implemented partially off-chip to account for the bonding wire's inductance and the pad capacitance at the gate of M1 as shown in Fig. 5. The off-chip matching network consists of a series capacitor cascaded with an all-inductor pi-network, whereas the on-chip matching network is simply an inductor of 4 nH, which was realized with 3.5 turns, as shown by the spiral inductor on the right-hand side of Fig. 6.

Fig. 9 presents the simulated F_{min} , simulated $F_{\text{match,opt}}$ (assuming optimal X_s), and the measured noise figure with experimental setup as in Fig. 5. Even with the approximation of

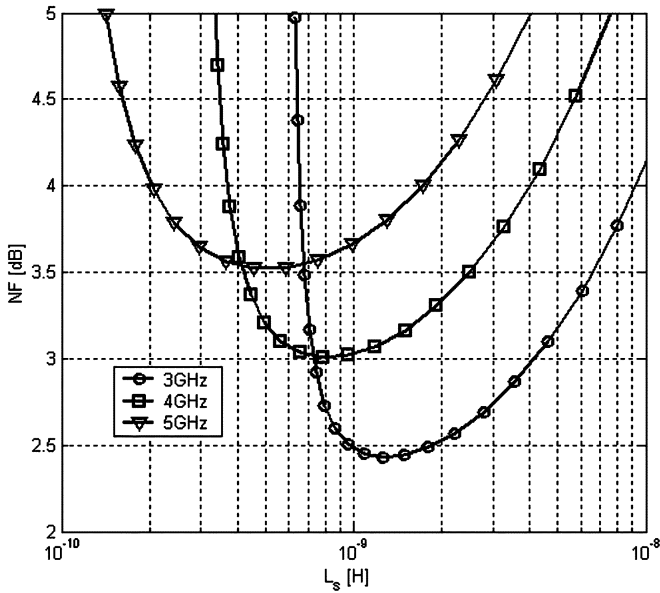


Fig. 8. Noise figure sensitivity analysis with respect to L_s at different frequencies.

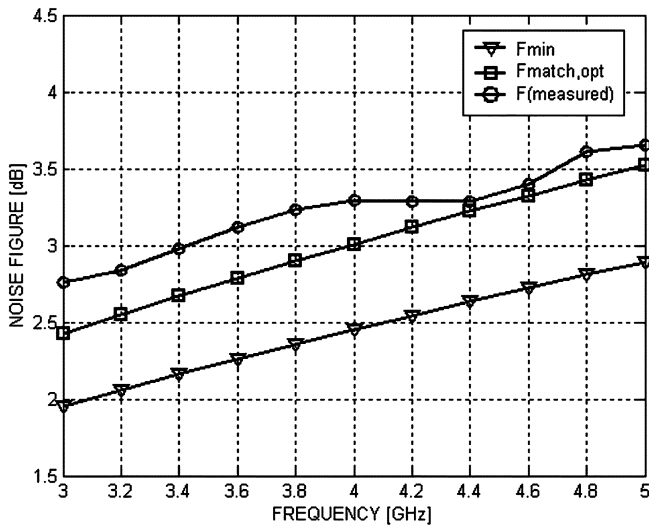


Fig. 9. Plot of the measured noise figure, as compared to the simulated $F_{\text{match,opt}}$ and F_{min} .

the optimal X_s using an inductor at the source degeneration, a close agreement between the measured noise figure and simulated $F_{\text{match,opt}}$ is observed. The measured magnitude of S11 and available gain are shown in Fig. 10, in which the measured return loss of greater than 9 dB is achieved. The measured available gain is approximately 7 dB with a 3-dB bandwidth between 3.2–4.8 GHz. Additional gain can be achieved by further optimizing the on-chip inductor and/or employing more advanced process technology (e.g., 0.18 μm). Fig. 11 shows the measured 1-dB compression point, IIP2, and IIP3 at 4 GHz. Summary of the performance results are given and compared with other published wide-band CMOS LNA work in Table I, which suggests that the LNA in this work outperforms other LNAs in terms of noise figure.

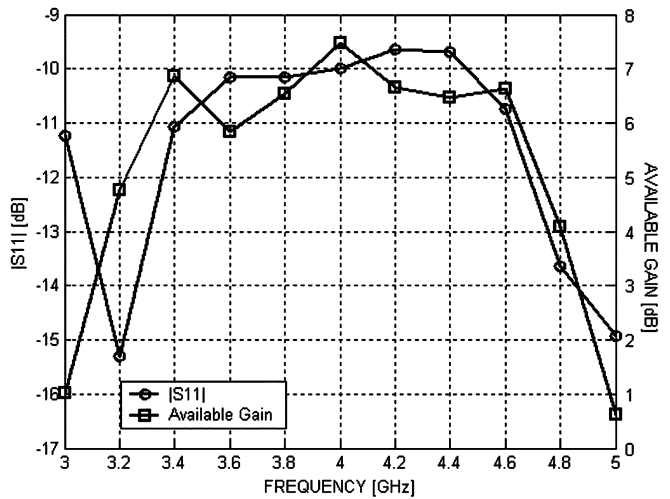


Fig. 10. Plots of the measured magnitude of S11 and available gain as a function of frequency.

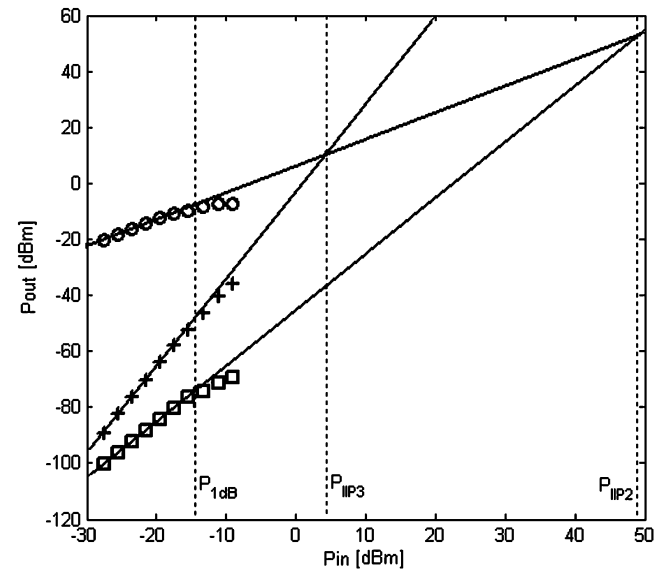


Fig. 11. Plots of the measured 1-dB compressed point, IIP2, and IIP3.

TABLE I
LNA PERFORMANCE SUMMARY AND COMPARISONS

	This work	[12]	[13]
Frequency (GHz)	3.2–4.8	3–5	3.1–10.6
Supply Voltage (V)	2.5	N/A	N/A
S11 (dB)	-9.5~15	-8~14	-10~37
CP1 (dBm@GHz)	-16@4	-15@2.5	-15@6
IIP2 (dBm@GHz)	49@4	N/A	N/A
IIP3 (dBm@GHz)	4@4	-4.7@2.5	-6.7@6
Noise Figure (dB)	2.7~3.7	4~5	4~9.6
Gain (dB)	7(Av)	13	9.2
Power (mW)	20	75	9
Technology	0.25 μm CMOS	0.18 μm CMOS	0.18 μm CMOS

V. CONCLUSION

This paper presents a design methodology for the wide-band CMOS LNA with source degeneration. Using the quasi-static MOSFET model, our analysis shows that the minimum noise figure can be made independent of the transistor width by

properly choosing the source degeneration reactance. This result shows that the proposed topology is effective as a wide-band LNA, since the same transistor can be used to achieve the minimum noise figure at all frequencies of interest. The transistor width simply affects the gain of the LNA at the cost of power dissipation. The transistor bias voltage affects the tradeoff between gain and the minimum noise figure. The results obtained in this paper apply uniquely to CMOS LNA, as the analysis are based on the quasi-static MOSFET model. To validate the proposed wide-band CMOS LNA design concepts, a wide-band LNA was implemented in 0.25- μm CMOS standard technology. A close agreement (< 0.3 dB) between measurement and analytical results were observed. The measured noise figure is 2.7–3.7 dB and the available gain is 7 dB while dissipating 20 mW.

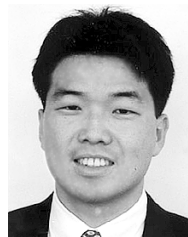
REFERENCES

- [1] J. Janssens, M. Steyaert, and H. Miyakawa, "A 2.7-V CMOS broadband low noise amplifier," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 1997, pp. 87–88.
- [2] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.
- [3] A. R. Shahani, D. K. Shaeffer, and T. H. Lee, "A 12-mW wide dynamic range CMOS front-end for a portable GPS receiver," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2061–2070, Dec. 1997.
- [4] K.-Y. Toh, P.-K. Ko, and R. G. Meyer, "An engineering model for short-channel mos devices," *IEEE J. Solid-State Circuits*, vol. 23, no. 8, pp. 950–958, Aug. 1988.
- [5] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.
- [6] N. G. Einspruch, *VLSI Electronics: Microstructure Science*. New York: Wiley, 1986.
- [7] H. Rothe and W. Dalke, "Theory of noise four poles," *Proc. IRE*, vol. 44-I, pp. 811–818, Jun. 1956.
- [8] H. Hillbrand and P. H. Russer, "An efficient method for compute aided noise analysis of linear amplifier network," *IEEE Trans. Circuits Syst.*, vol. CAS-23, no. 4, pp. 235–238, Apr. 1976.
- [9] J.-S. Goo, K.-H. Oh, C.-H. Choi, Z. Yu, T. H. Lee, and R. W. Dutton, "Guidelines for the power-constrained design of a CMOS tuned LNA," in *Proc. Int. Conf. Simulation of Semiconductor Processes and Devices (SISPAD)*, Sep. 2000, pp. 269–272.
- [10] *Multi-Band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a*, IEEE 802.15-03/268r2, 2003.
- [11] *XtremeSpectrum CFP Document*, IEEE 802.15-03/154r3, 2003.
- [12] S. Andersson, C. Svensson, and O. Drügge, "Wideband LNA for a multi-standard wireless receiver in 0.18 μm CMOS," in *Proc. Eur. Solid-State Circuit Conf.*, Sep. 2003, pp. 655–658.
- [13] A. Bevilacqua and A. M. Niknejad, "An ultra-wideband CMOS LNA for 3.1 to 10.6 GHz wireless receivers," in *Proc. IEEE Int. Solid-State Circuit Conf.*, Feb. 2004, pp. 382–383.



Jongrit Lerdworatawee (S'03) received the B.Eng. degree from Tsinghua University, Beijing, China, in 1998 and the M.Eng. degree from the National University of Singapore in 2000. He is currently working toward the Ph.D. degree at the University of Southern California, Los Angeles.

His current research interest are in RF/mixed signal communication circuits.



Won Namgoong (M'03) received the B.S. degree in electrical engineering and computer science from the University of California, Berkeley, in 1993, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1995 and 1999, respectively.

In 1999, he joined the faculty of the Electrical Engineering Systems Department, University of Southern California, Los Angeles, where he is an Assistant Professor. His current research activities include signal processing systems, wireless communication, and RF/mixed-signal circuits and systems.

Dr. Namgoong was the recipient of the National Science Foundation (NSF) CAREER Award in 2002. He is currently an Associate Editor for the IEEE TRANSACTION ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS.