

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AUSTRIA AG,
Patent Owner.

IPR2024-00094
U.S. Patent 8,264,003

DECLARATION OF JOSEPH B. BERNSTEIN, PH.D.

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I. INTRODUCTION

[001] I have been retained by Innoscience America, Inc. as an independent expert for the above-identified *inter partes* review proceeding involving U.S. Patent No. 8,264,003 (“the ’003 patent”).

[002] I am over 21 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

[003] Although I am being compensated for my time in connection with this proceeding at my standard hourly consulting rate and reimbursed for reasonable out-of-pocket expenses, no part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

[004] I have been asked to provide my opinion whether the claims of the ’003 patent would have been obvious to a person of ordinary skill in the art at the time of the earliest claimed priority date of the ’003 patent. In performing my analysis, I have been asked to assume that the priority date is March 20, 2006. My opinions are set forth below.

[005] Throughout this declaration, I refer to specific pages, figures, and/or line numbers of various exhibits. These citations are illustrative and are not intended to suggest that they are the only support for the propositions for which they are cited.

II. SUMMARY OF OPINIONS

[006] This declaration analyses claims 1-16 of the '003 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for my opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

[007] Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of March 20, 2006), it is my opinion that claims 1-16 of the '003 patent would have been obvious based on the asserted grounds discussed below.

III. QUALIFICATIONS AND BACKGROUND

[008] I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Ex-1004.

[009] I am competent to write this Declaration.

[010] This is a summary of my background and qualifications. I set forth my background in more detail in my Curriculum Vitae, which is attached as Exhibit A herewith.

[011] I graduated Summa Cum Laude from Union College in Schenectady, NY with a Bachelor of Science degree in Electrical Engineering in 1984.

Subsequently, I attended the Massachusetts Institute of Technology (MIT), where I earned a Master of Science degree in Electrical Engineering and Computer science in 1986, an Electrical Engineer degree in 1987, and a Doctor of Philosophy in Electrical Engineering and Computer Science in 1990.

[012] I performed research in semiconductor physics as an undergraduate student, and my bachelor's thesis related to Deal Surface States in silicon devices, which leads to degradation and failure in semiconductors to this day. The modern term for this failure mechanism is Negative Bias Temperature Instability (NBTI). This work formed my understanding through my doctoral studies and lead to my current work studying the physics of semiconductor devices, including wide bandgap (WBG) semiconductors for power device applications, such as gallium nitride (GaN) and silicon carbide (SiC) semiconductors.

[013] The topic of my Master of Science research work at MIT was on high-power semiconductor device physics, with the goal of optimizing Vertical MOSFETs for high frequency (10 MHz) switching operation. In pursuit of this goal, I designed and fabricated a power MOS transistor having an integrated turn-off driver. Hence, before beginning my Doctorate at MIT in 1990, I had already gained experience both in reliability physics and high voltage power electronic devices. Notably, my Master's work led to my second publication relating to

reducing (or eliminating) the Miller effect—a stated goal of the '003 patent— in power MOS devices by integrating a turn-off driver on the chip.

[014] My PhD research continued from my master's research relating high energy electrons charging insulating materials. For my PhD thesis, I analyzed the effects of high-energy electron injection of insulating materials by in-situ testing. My doctoral work as well as my MS project were very practical hands-on experimental experience, which has followed me for my research career. Also, my studies on reliability and specifically power devices continues to my current research programs relating to in-situ reliability studies of wide bandgap semiconductors as well as high voltage device gate drivers to eliminate miller effect in high frequency high power energy converters.

[015] After earning my Ph.D., I worked at MIT Lincoln Laboratory as a senior research staff member, during which time I taught at Boston University as an Adjunct Professor. My first position at Lincoln Lab was in the Wafer Scale Integration group. This group was responsible for developing and programming of wafer scale integrated circuits including wiring, routing, programming, packaging, and reliability for very large wafer scale integrated circuits. This is where I developed laser programmable interconnect technology which was my first set of patents and was the basis for my first start-up company.

[016] From 1995 to 2007, I was first an Assistant and then Associate Professor of Engineering at University of Maryland (UMD) while acting as co-founder and chief scientist of Lightspeed Semiconductor, a Silicon Valley company relating to high performance, metal-configurable gate arrays using laser anti-fuses. Some of those I worked with or taught during this time, including graduate students and former students, met the definition of a POSITA provided below as of March 20, 2006.

[017] Upon arriving at UMD as a professor of Microelectronics Reliability, I was soon invited by the head of CALCE, Professor Michael Pecht, to lead a group of industry packaging experts to investigate the emerging Korean electronics industry. This experience led to my complete immersion and familiarity with the development of commodity devices as emerging market opportunities spread across the globe. This led to my next book as a co-author, “Pecht, M., Bernstein, J.B., Searls, D., and Peckerar, M., The Korean Electronics Industry, CRC Press, 1997.”

[018] Thus, my background includes collaborations while at UMD and close association with industry. My research brought me close with many companies and government laboratories around the world looking into better, cheaper, and more reliable electronic devices and system. I have been sponsored by the Office of Naval Research to perform reliability evaluation of power devices. In fact, since

2003, I have had over 15 programs sponsored by US Government agencies evaluating power devices for Silicon IGBT's, SiC and most of my research today is focused on GaN. I lead an active research program in GaN device applications and reliability for power electronics using WBG semiconductors.

[019] While at the University of Maryland, I taught in the Reliability program as the specialist in microelectronics device reliability. In the summer of 1998, I joined the Jet Propulsion Laboratories as a NASA Summer Faculty Research Fellow where I taught short courses in reliability physics and practical solutions for assessing and improving reliability of electronic products. I was promoted from Assistant to Associate Professor with tenure in 2001. From 2003 to 2005, I was a Professor of Engineering at Tel-Aviv University on Sabbatical from the University of Maryland. During my tenure at Maryland, I had many programs also sponsored at the National Institute of Standards and Technology (NIST), where I worked directly with the semiconductor industry by means of the connection with NIST. This group acted as a government liaison with semiconductor manufacturing companies and often was the center for Joint Electron Device Engineering Council (JEDEC) round-robin testing and committee groups focused on reliability and standards for the semiconductor industry.

[020] I am currently employed as a full professor at Ariel University in Ariel, Israel. At Ariel, a focus of my research is on issues related to electronic

device reliability, including links between reliability, power, and thermal behavior. My current research focuses on packaged discrete GaN devices. My research looks at the functionality and performance of system-level reliability boards and packages, including high voltage transistors. My research looks at all the failure mechanisms that can affect the reliability of the circuits and systems and model these mechanisms to derive a complete reliability prediction methodology. I also have several consulting clients in the semiconductor field that apply my methodology, including Camtek, SanDisk and Maradin, as well as system level customers including Thales (France), EPC (California) and other smaller companies.

[021] In addition to a long list of publications, I have given numerous tutorials, talks, presentations, and lectures, in both academic and corporate settings, on semiconductor devices and reliability. For the past 5 years, at least, I have been the first or second most referenced author in the field of Microelectronics Reliability and in Physics of Failure as listed by Google Scholar. I lead the Laboratory for Reliable Electronics Systems at Ariel University. My laboratory is the premier center in Israel for reliability studies where we focus on power devices and evaluate failure mechanisms through failure analysis and modeling.

[022] I supervise four Ph.D. candidates at present and one post-Doctoral fellow. Three of these students are studying physics and circuit configurations to

test the reliability of GaN and SiC power devices while the fourth student is designing an integrated gate driver for MHz power conversion at kW of power. I have served as the advisor or co-advisor for 20 Ph.D. graduates in electrical and electronic engineering, many of whom graduated in the materials and mechanical engineering departments through the Reliability Program at the University of Maryland.

[023] I now teach classes at Ariel University that include undergraduate and graduate courses in Electrical Engineering. Some courses I have taught include VLSI Design, Reliability Engineering Fundamentals, Microelectronics Device Reliability, Advanced Reliability Engineering. I also developed coursework and curricula on Reliability Engineering and Electronic Device Reliability. I have authored numerous books, manuals, and teaching materials on reliability in electronics. Furthermore, I hold several patents related to GaN power device technology helping develop the elusive power system-on-a-chip.

[024] I have served as a testifying expert in litigation in several district court cases. I have also served as an expert in several matters at the Patent Trial and Appeal Board, including inter-partes reviews and patent reexaminations. I have also served as a technical consultant for electronics and computer systems companies on issues including testing and reliability. Some companies I have consulted on behalf of include SanDisk, Marvell Corp., Cypress Semiconductor,

Teradyne Corporation, and Freescale Semiconductor. A more complete listing is in my CV which is attached here as Exhibit A.

[025] A current copy of my curriculum vitae, Ex-1004 provides further information concerning my experience and qualifications and includes: a list of my patents, a list of the publications I have authored, and a list of the matters on which I have served as an expert witness.

IV. MATERIALS CONSIDERED

[026] In forming my opinions, I have read and considered the '003 patent and its prosecution history, the exhibits listed in the Exhibit List filed with the petition for inter partes review of the '003 patent, as well as any other materials referenced herein. I have reviewed the following at least the following documents:

Exhibit	Description
Ex-1001	U.S. Patent No. 8,264,003 (“the ’003 patent”)
Ex-1002	Prosecution History of the ’003 Patent (“Prosecution History”)
Ex-1005	U.S. Patent Publication No. 2005/0189561 to Kinzer et al (“Kinzer561”)
Ex-1006	U.S. Patent No. 6,160,280 to Bonn et al. (“Bonn”)
Ex-1007	U.S. Patent No. 6,483,135 to Mizuto et al. (“Mizuto”)
Ex-1008	U.S. Patent Publication No. 2004/0041169 to Ren et al. (“Ren”)
Ex-1009	U.S. Patent Publication No. 2005/0051800A1 to Mishra et al. (“Mishra”)

Ex-1010	Excerpts Of Public Verified Complaint of Infineon Technologies Austria AG and Infineon Technologies Americas Corp. Under Section 337, Inv. No. 337-TA-1414 (July 26, 2024).
Ex-1011	Exhibit 17 to Public Complaint in Inv. No. 337-TA-1414
Ex-1012	U.S. Patent Publication No. 2002/0171096A1 to Wakejima et al. (“Wakejima”)
Ex-1013	U.S. Patent Publication No. 2005/0051796 to Parikh et al. (“Parikh”)
Ex-1014	U.S. Patent No. 7,800,131 to Miyamoto et al. (“Miyamoto”)
Ex-1015	U.S. Patent No. 7,548,112 to Sheppard (“Sheppard”)
Ex-1016	U.S. Patent Publication No. US 2007/0170463 to Ueno et al (“Ueno”)
Ex-1017	U.S. Patent No. 7,408,399 to Salato et al. (“Salato”)
Ex-1018	U.S. Patent Publication No. 2006/0113593 A1 to Sankin et al. (“Sankin”)
Ex-1019	B. M. Green et al., “High-power broad-band AlGaIn/GaN HEMT MMICs on SiC substrates,” in <i>IEEE Transactions on Microwave Theory and Techniques</i> , vol. 49, no. 12, pp. 2486-2493, Dec. 2001, doi: 10.1109/22.971640 (“Green”)
Ex-1020	International Patent Publication No. WO 2005/070009 (“Beach”)
Ex-1021	U.S. Patent No. 6,586,781 to Wu et al. (“Wu”)
Ex-1022	U.S. Patent Publication No. 2002/0167023 to Chavarkar et al. (“Chavarkar”)
Ex-1023	Bernstein JB, Gleason EF, Wetsel AE, Liu EZ, Wyatt PW. “Anomalous Behavior of Semi-Insulating Silicon Rich Amorphous Silicon Nitride.” <i>MRS Proceedings</i> . 1992; 284:113. doi:10.1557/PROC-284-113 (“Bernstein-SiN”)

Ex-1024	Tessmann, A., Haydl, W. H., Hulsmann, A., & Schlechtweg, M. (1998). High-gain cascode MMICs in coplanar technology at W-band frequencies. <i>IEEE Microwave and Guided Wave Letters</i> , 8 (12), 430-431 (“Tessman”)
Ex-1025	Potirakis, S. M., and Alexakis, G. E. (2005). An accurate calculation of Miller effect on the frequency response and on the input and output impedances of feedback amplifiers. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 52(8), 491-495. (“Potirakis”)
Ex-1026	J. Lerdworatawee and Won Namgoong, "Wide-band CMOS cascode low-noise amplifier design based on source degeneration topology," in <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , vol. 52, no. 11, pp. 2327-2334, Nov. 2005, doi: 10.1109/TCSI.2005.853585. (“Lerdworatawee”)
Ex-1027	Ko, B. K., & Lee, K. (1996). A comparative study on the various monolithic low noise amplifier circuit topologies for RF and microwave applications. <i>IEEE Journal of Solid-State Circuits</i> , 31(8), 1220-1225 (“Ko”)
Ex-1029	LTspice cascode amplifier simulation
Ex-1030	LTspice cascode amplifier schematic
Ex-1031	LTspice cascode amplifier simulation data
Ex-1032	LTspice cascode amplifier graph

[032] I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

V. LEGAL STANDARDS

[033] I am not a lawyer. My understanding of the legal standards that apply in reaching the conclusions of this declaration are based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried faithfully to apply these legal standards to the challenged claims.

[034] I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

[035] I have been informed that a dependent claim is a patent claim that refers to a previous patent claim. I have been informed that a dependent claim includes all the limitations of the claim to which it refers.

[036] I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-16 of the '003 patent from the perspective of a person of ordinary skill in the art at the '003 patent's earliest claimed priority date of March 20, 2006, as described in more detail below.

[037] I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

[038] For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill in the Art

[039] I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

[040] I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Anticipation

[041] I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed

invention. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

C. Obviousness

[042] I have been informed that obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter, sought to be patented, and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made.

[043] I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available).

[044] I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to

assume that the date of invention for the challenged claims is March 20, 2006. My opinions would not change if I assumed a later date of invention.

[045] I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may consider the inferences and creative steps that a person of ordinary skill in the art would employ.

[046] I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

[047] In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a

“reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

[048] I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

[049] I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely

because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

[050] I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

[051] I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '003 patent.

[052] I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or

(2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. OVERVIEW OF THE '003 PATENT

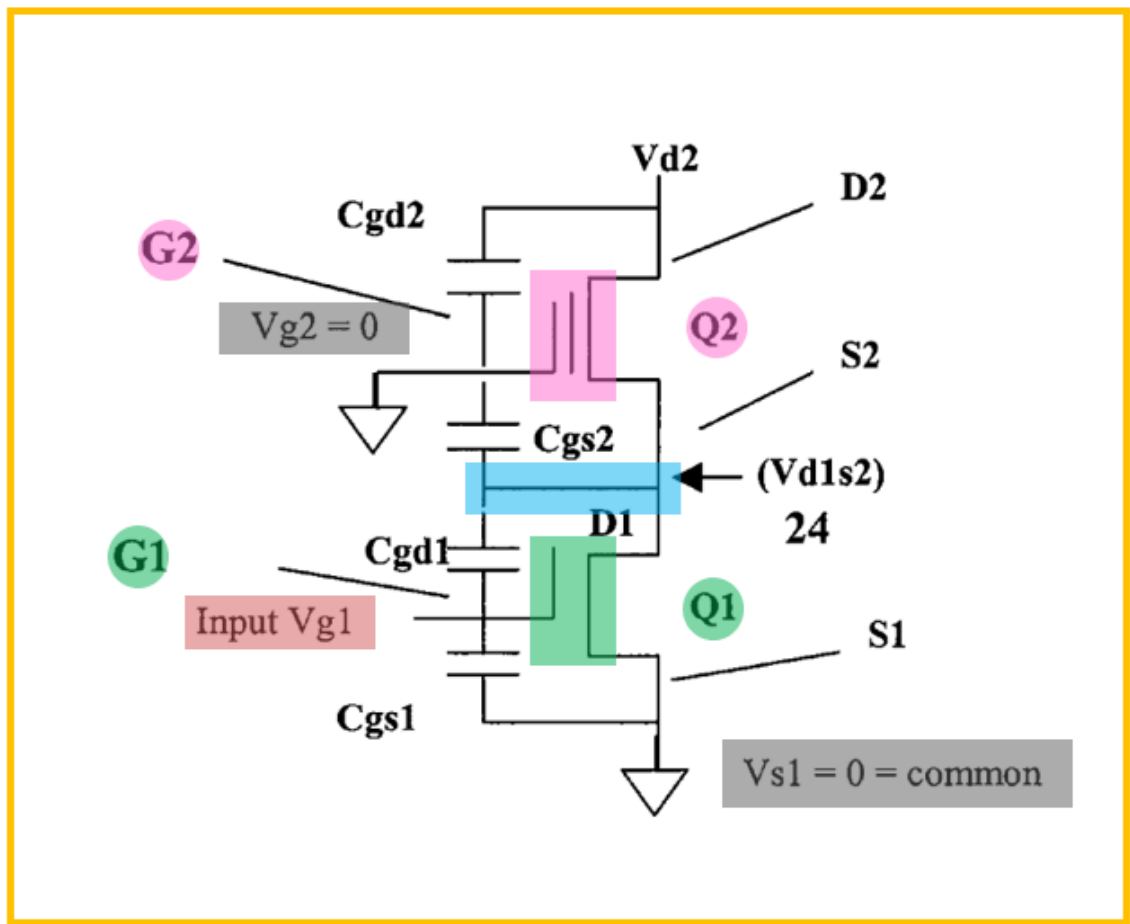
[053] The application that issued as the '003 patent was filed on March 20, 2007. '003 patent, Cover. It claims priority to U.S. Provisional Application Number 60/783,934, filed March 20, 2006. *Id.* The patent issued on September 11, 2012, with 16 claims, including independent claims 1 and 10. '003 patent, Cover, 5:25-8:10. The patent lists one inventor, Thomas Herman.

[054] The '003 patent claims a cascode with an enhancement mode first gate and a depletion mode second gate. '003 patent, claims 1, 10. The specification describes that prior art cascodes made from separate FETs suffered from “[l]arge drain-source Voltage (V_{ds}) swings during switching [that] create a large “Miller effect” and as a result, excessive switching losses.” Ex-1001, 1:36-38, 2:52-53. 3:29-31, Fig. 1. In addition, the patent describes that high dV/dt changes at the drain lead to transient voltages at the first gate, which turn this gate on when not desired and result in power and efficiency losses. Ex-1001, 1:39-47.

[055] The patent purports to solve this problem because its embodiments are made from a “single device and not two separate FETs.” Ex-1001, 2:48-52. The patent asserts that this arrangement reduces the Miller effect, reduces dV/dt , and

results in less power loss and higher efficiency. Ex-1001, 3:29-50. But as I will explain in greater detail below, it was long known in the art to create a cascode from a single device and not two separate FETs. Bonn (Ex. 1005), published in 1996, disclosed this arrangement over a decade before the '003 patent.

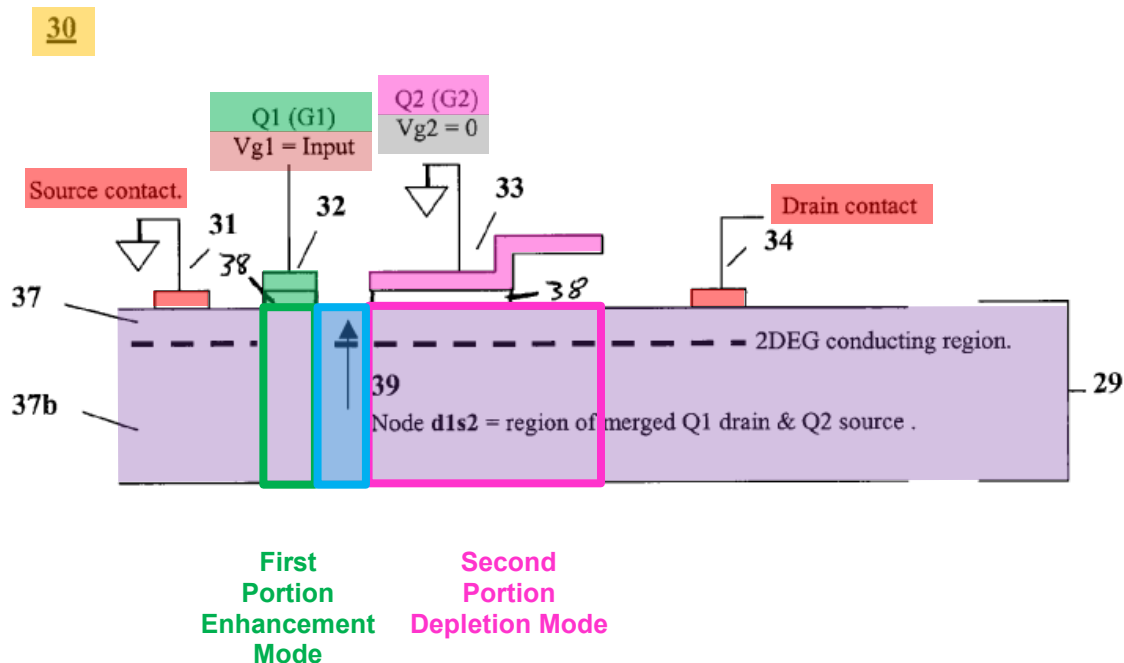
[056] Figure 2 (below) shows a circuit diagram of an embodiment of the '003 patent's **merged cascode** circuit with **first gate G1** and **second gate G2**. **Q1** is the **first portion** under **G1**, and it is in enhancement mode, which means it is normally off when the **input voltage** is at 0V and turns on only when the **input voltage** is above a positive threshold. Ex-1001, 2:54-3:23. **Q2** is the **second portion** under **G2**, and it is in depletion mode, normally on at 0V and above. Ex-1001, 2:54-3:23. **Q1** and **G2** connect to **ground** in some embodiments, as shown in Figures 2-4, and there is a **node** between the gates. Ex-1001, 2:54-3:23, Figs. 2-4.



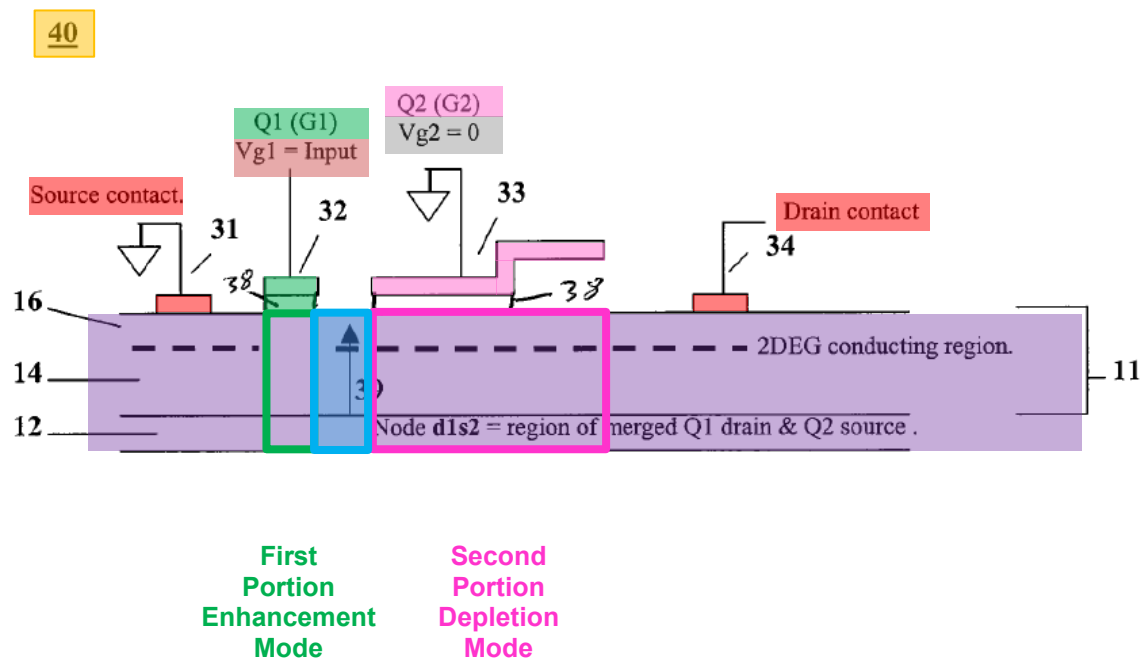
Ex-1001, Fig. 2 (annotated).

[057] The '003 patent claims, depicts, and describes the **node** as a region of the **semiconductor element** that laterally separates the **first portion** and the **second portion** of the transistor such as, for example, the color-coded **light blue** region or a region within the light **blue region** in Figure 2, above, and Figures 3-4, below. Ex-1001, Ex-1001, 4:4-8, Figs. 2-4, claim 1 (“a **node** in the **semiconductor element** between the **first portion** and the **second portion** of the transistor”), claim 10 (same). In Figure 3, the specification explains “**node 24** of FIG. 2 is

represented by the arrow 39 in the area of the merged Q1 drain and Q2 source. That is, on the drain side of the gate 32 (G1) of the first portion Q1 and on the source side of the gate 33 (Q2) of the second portion.” Ex-1001, 4:4-8. Both Figures 3 and 4 state “**node** d1s2 = region of merged Q1 drain and Q2 source,” where “d1” means the drain of **Q1** and “s2” means the source of **Q2**. Ex-1001, Figs. 3-4.



Ex-1001, Fig. 3 (annotated).



Ex-1001, Fig. 4 (annotated).

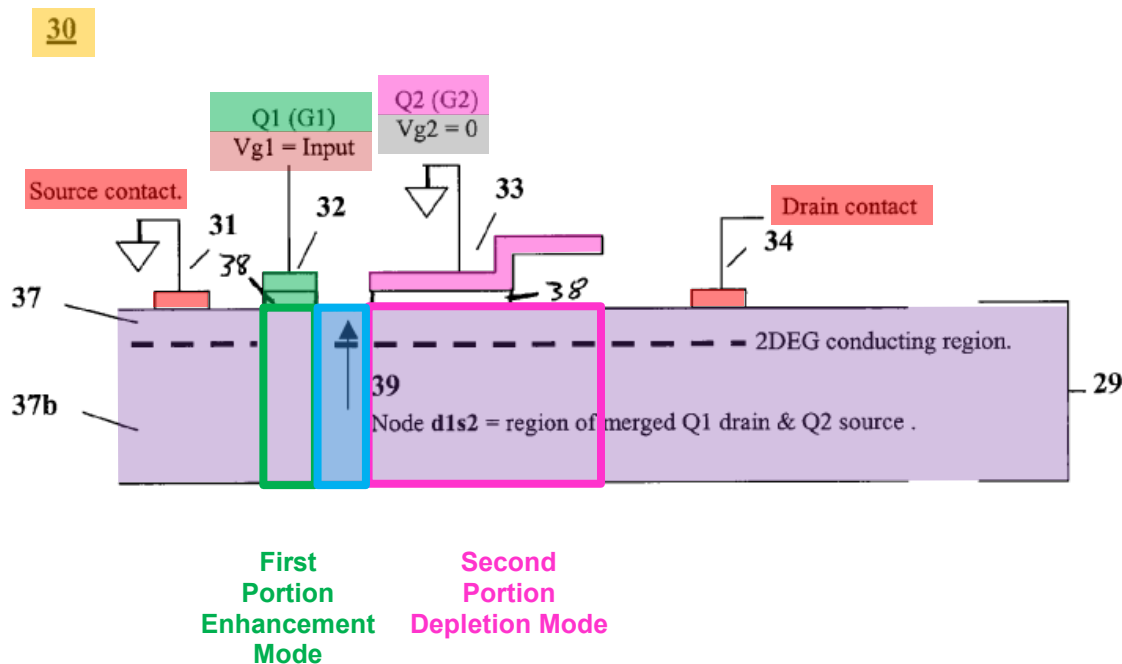
[058] Figures 3 and 4 (above) show a cascode made from a single device, with a **semiconductor element**, a **source** and **drain**, a **first gate** in enhancement mode, and a **second gate** in depletion mode. Ex-1001, 3:51-4:17 (Fig. 3), 4:23-43 (Fig. 4). Both gates connect to **ground**. **Q1** connects to **ground** via the 2DEG and **source** contact, while **Q2** connect to **ground** via a contact on the gate **G2**. As shown, both figures include a region of **merged Q1** drain and **Q2** source at a **node** between the enhancement mode gate **Q1** and depletion mode gate **Q2**, on the drain side of **Q1** and source side **Q2**. Ex-1001, 4:4-8 (discussing Figs. 2-3).

[059] Counsel informed me that the claims were only allowed after being amended to include the merged limitation and USPTO Examiner identified the

merged source and drain regions as the feature that led to allowance of the '003 patent. Ex-1002, 18 (Examiner's statement of reasons for allowance).

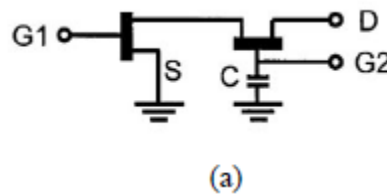
VII. TECHNOLOGICAL BACKGROUND

[060] The '003 patent purports to invent a cascode with a **first enhancement mode gate** and **second depletion mode gate** separated by a **node** in the underlying **semiconductor** that includes a **merged** drain region of the **first gate** and source region of the **second gate**. See § VI (OVERVIEW OF THE '003 PATENT), above. Claim 1 does not limit the semiconductors to any particular materials, while claims 2-16 require III-Nitride materials, and claims 3-9 and 11-16 require GaN materials. None of this was new at the time.



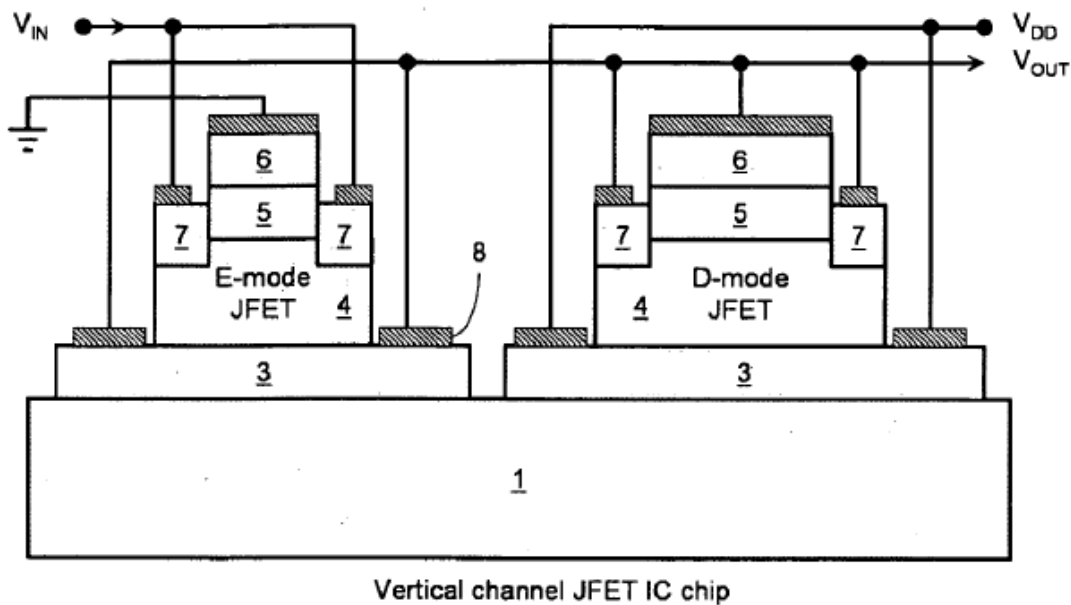
Ex-1001, Fig. 3 (annotated).

[061] Cascodes are two-stage amplifiers having a first, upper FET and second, lower FET that share a common source at the first FET, where the drain of the first gate connects in series to the source of the second gate. The source can be the ground, and the input to the second gate can also be grounded. Tessman (1998 publication date) illustrates this arrangement. Tessman (Ex-1024).



Tessman, Fig. 2(a).

In general, cascodes comprising a **first, enhancement mode gate** and **second, depletion mode gate** were common and recognized to be beneficial as of the priority date of the '003 patent. Bonn (1996 publication date) discloses this arrangement. Bonn, 8:67-9:4, Fig. 7. Salato (2005 priority date) discloses a “cascoded configuration of a normally ON depletion mode and a normally OFF [enhancement mode] semiconductor devices allows reliable and safe operation in switching mode power supply systems.” Salato (Ex-1017), 1:30-34. Sankin (2004 priority date) likewise disclose this arrangement. *E.g.*, Sankin (Ex-1018), ¶¶[0013], [0119], Fig. 1.

**FIG. 1**

Sankin, Fig. 1.

[062] Cascodes formed of two gates on a single semiconductor layer were known for many years before the '003 patent, whose earliest claimed priority date is March 20, 2006. For example, Green, published in 2001, discloses AlGaIn/GaN “monolithic” cascodes (i.e., dual gates over an AlGaIn layer). Green (Ex-1019), Abstract, § I, Fig 6. Bonn, published in 1996, discloses monolithic gallium-arsenide based cascodes with a **first enhancement mode gate** and **second depletion mode gate** separated by a **node** in the underlying **semiconductor** that includes a **merged** drain region of the **first gate** and source region of the **second gate**. As I will explain, while GaN was uncommon in 1996, it would have been obvious to form Bonn’s device from GaN materials by the time of the '003 patent

to realize the then-known benefits of these devices, including improved performance at high frequency, high temperature, and/or high power applications.

E.g., Ren, ¶¶[0012]-[0018], [0030], Figs. 1-2.

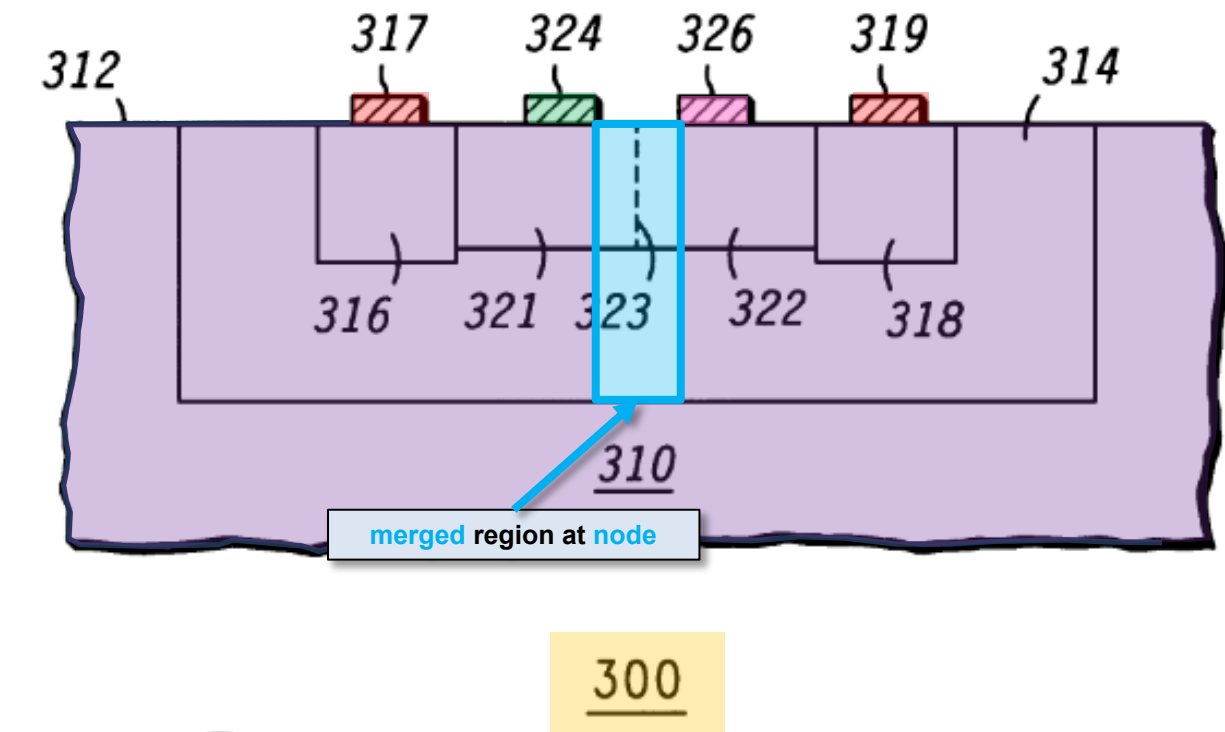
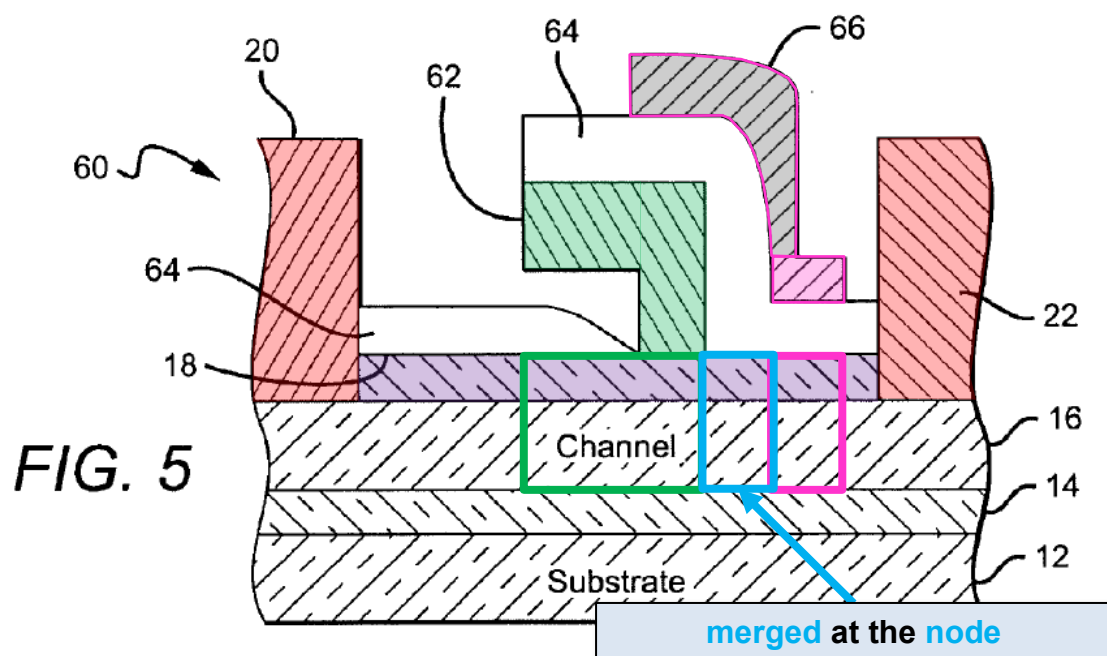


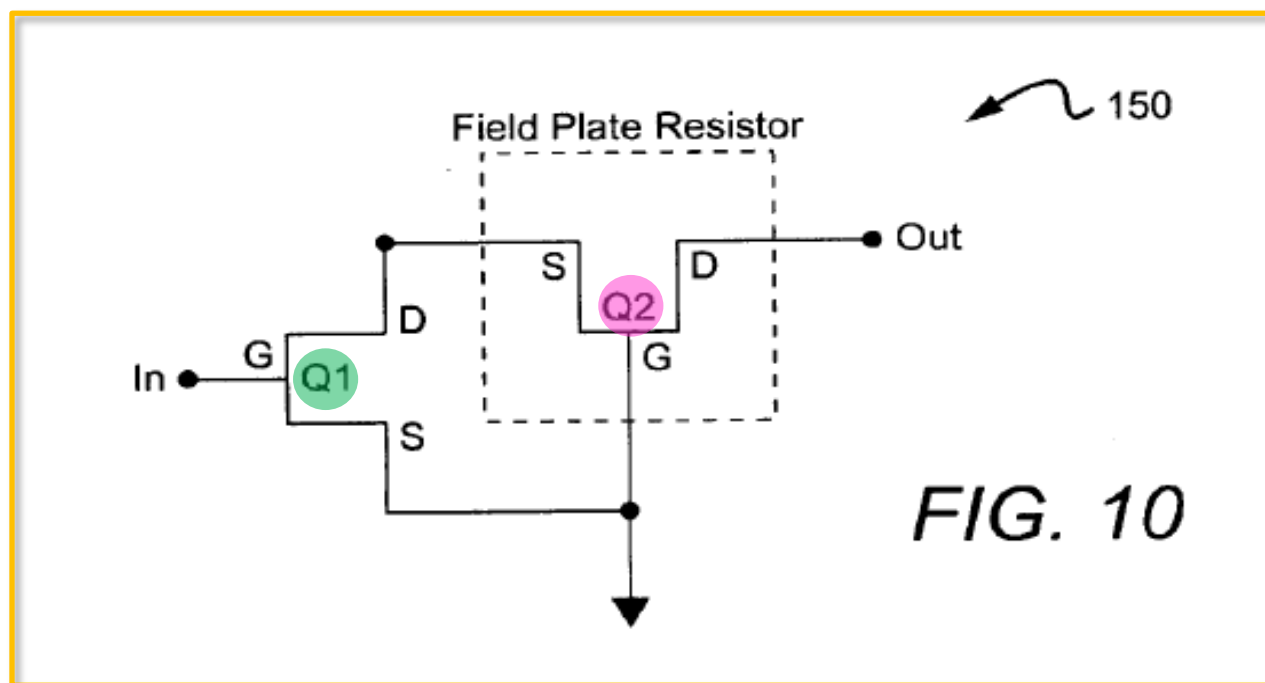
FIG. 7

Bonn, Fig. 7 (annotated)

[063] And as I will explain, Mishra also disclose cascodes with a **first gate** and **second gate** separated by a **node** in the underlying **semiconductor** that includes a **merged** drain region of the **first gate** and source region of the **second gate** under Infineon's apparent infringement theory (below).



Mishra, Fig. 5 (annotated).



Mishra, Fig. 10 (annotated).

[064] It is instructive to point out here that in a configuration like Mishra's or the '003 patent, where the gate of the second (upper) transistor **Q2** is electrically connected to the source of the first (lower) transistor **Q1**, and the source is set to ground (0V), then the upper transistor **Q2** would be a depletion mode device. This is because the only control of **Q2** is through the lower transistor **Q1**, which can only turn ON when the gate voltage on **Q1** is above its threshold (turn-on) voltage. **Q2** must be in the ON state when **Q1** turns on—that is the gate-to-source voltage of **Q2** must be above its threshold voltage. Hence, to achieve current flowing when the voltage at the first gate **G1** (V_{g1}) is above the threshold voltage, then voltage difference between the voltage applied to the second gate and the source of the second gate at the node (V_{gs2}) must be also above its threshold voltage (V_{th2}) when **Q1** turns on. The only way $V_{gs2} > V_{th2}$, when $V_{gs2} = 0$ (grounded) as shown in Figure 2 of the '003 patent, is if the **threshold voltage (V_{th2}) is negative**. That is because the source voltage $V_{s1} = 0 = \text{common}$, which is also at the same voltage as V_{g2} . Mishra, ¶¶[0055], [0058], Fig. 10. Hence, **Q2** must have a negative threshold voltage, which defines the upper device as a depletion mode transistor because it conducts with zero volts from the gate to source.

[065] For high power and high voltage operation, control signals are generally only positive voltages, requiring that **Q1** be an enhancement mode device so that it is normally off without any applied gate voltage, i.e., when

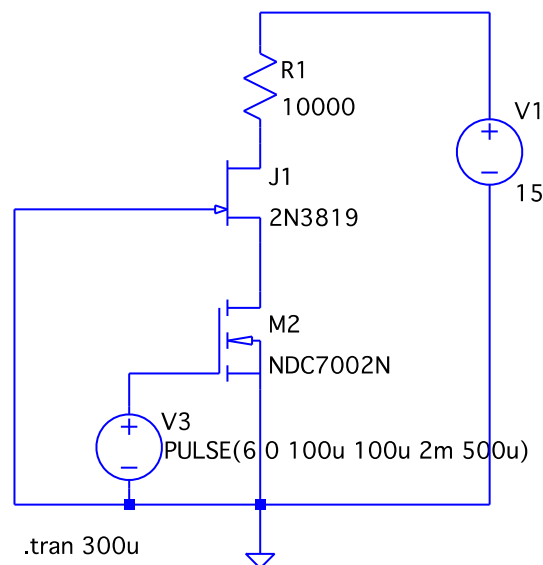
$V_{g1}=0$. *E.g., see* Salato (Ex-1017), 1:30-34. At the time of the '003 patent, such cascodes with a first stage enhancement and second stage depletion mode were known. This approach was implemented, for example, in Bonn. Bonn, 8:51-9:4. Sankin also used this approach. Sankin (Ex-1018), ¶¶[0013], [0119], Fig. 1. So does Salato, noting this configuration improves reliability and safety. Salato (Ex-1017), 1:30-34 (“cascoded configuration of a normally ON depletion mode and a normally OFF [enhancement mode] semiconductor devices allows reliable and safe operation in switching mode power supply system”).

[066] In a first stage enhancement and second stage depletion mode cascode, when V_{g1} becomes greater than the threshold voltage of the enhancement mode gate **G1**, then the two transistors will both be ON, allowing the current to flow through the combined cascode device. However, when V_{g1} is reduced to zero volts, below the threshold voltage such that **Q1** switches off, then the maximum voltage seen at the drain of **Q1** will be limited by the negative pinch-off or threshold voltage of the upper (**Q2**) depletion mode device. Although a POSITA at the time of the '003 patent would have readily understood these principles, to further illustrate this concept, I simulate the normal behavior of a cascode amplifier with a first enhancement mode gate and second depletion mode gate using the below example circuit in LTspice version 17.2.4 for Mac OS. Ex-1029. A POSITA

would have been able to generate a similar simulation at the time of the

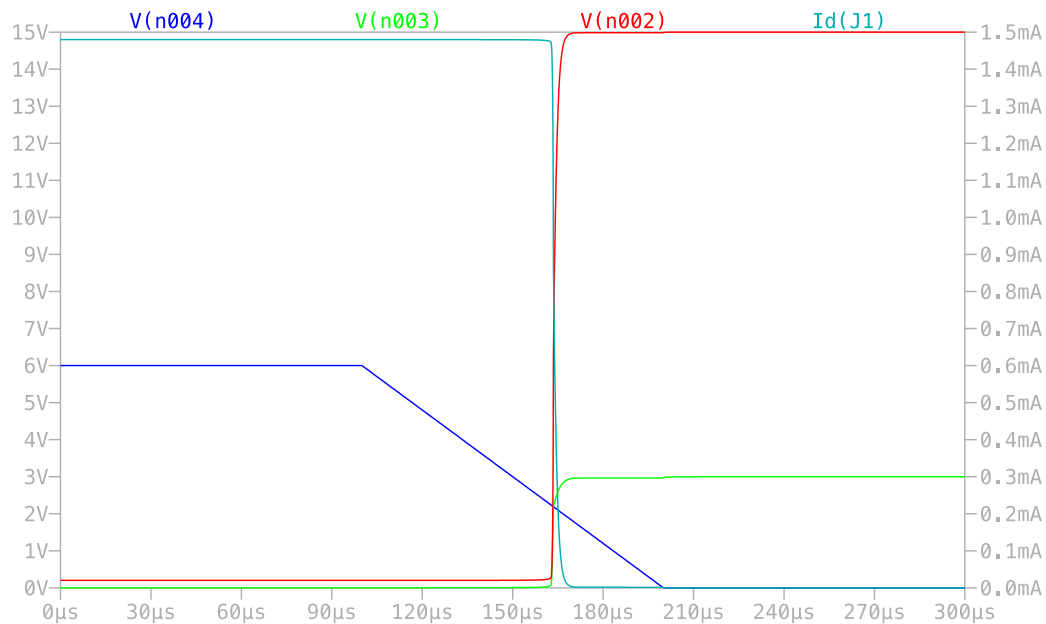
'003 patent. The SPICE parameters used for the two transistors are as follows:

- For Q1 (“M2 in Spice”): .model **NDC7002N** VDMOS(Rg=3 Vto=2.2 Rd=.8 Rs=.2 Rb=1 Kp=.4 lambda=.01 Cgdmax=.05n Cgdmin=.02n Cgs=.02n Cjo=.02n Is=2p ksubthres=.1 mfg=Fairchild Vds=50 Ron=2000m Qg=1n).
- For Q2 (“J1 in Spice”): .model **2N3819** NJF(Beta=1.304m Betatce=-.5 Rd=1 Rs=1 Lambda=2.25m Vto=-3 Vtotc=-2.5m Is=33.57f Isr=322.4f N=1 Nr=2 Xti=3 Alpha=311.7u Vk=243.6 Cgd=1.6p M=.3622 Pb=1 Fc=.5 Cgs=2.414p Kf=9.882E-18 Af=1 mfg=Vishay).



Ex-1030 (simulated circuit).

The circuit includes an NMOS transistor, NDC7002, as a representative enhancement mode transistor (“M2”), which simulates the role of Q1 in the ’003 patent. As I list above, this transistor has a turn on threshold voltage of 2.2V ($V_{to}=2.2$). For the depletion mode upper transistor J1, I used an N-type JFET 2N3819 that has a pinch-off voltage of -3V ($V_{to}=-3$) as I list above, which simulates the role of Q2 in the ’003 patent. The depletion mode gate J1 is connected to ground (Ex-1030), just as in the ’003 patent examples. *E.g.*, ’003 patent, Figs. 2-4. Also as shown above, the amplifier voltage is set with V1 at 15V. Ex-1029. For the simulation, I chose a resistance of 10,000 Ohms for resistor R1 because the simulated depletion mode device, J1, has an ON resistance of 133 Ohms. Ex-1029. This will be the resistance with zero volts at the gate M2, which is in series with the lower transistor. Next, I simulated the gate voltage at M2 with the PULSE command, shown as V3 in the schematic. Ex-1029; Ex-1030. The gate voltage starts at 6V (ON voltage) and remains ON for 100 μ s. Then, it ramps down to zero volts for the second 100 μ s of the simulation. Finally, the transient command (.tran) sets the simulation to last 300 μ s. I show the simulation results in the next figure. *See* Ex-1031 (simulation output data).



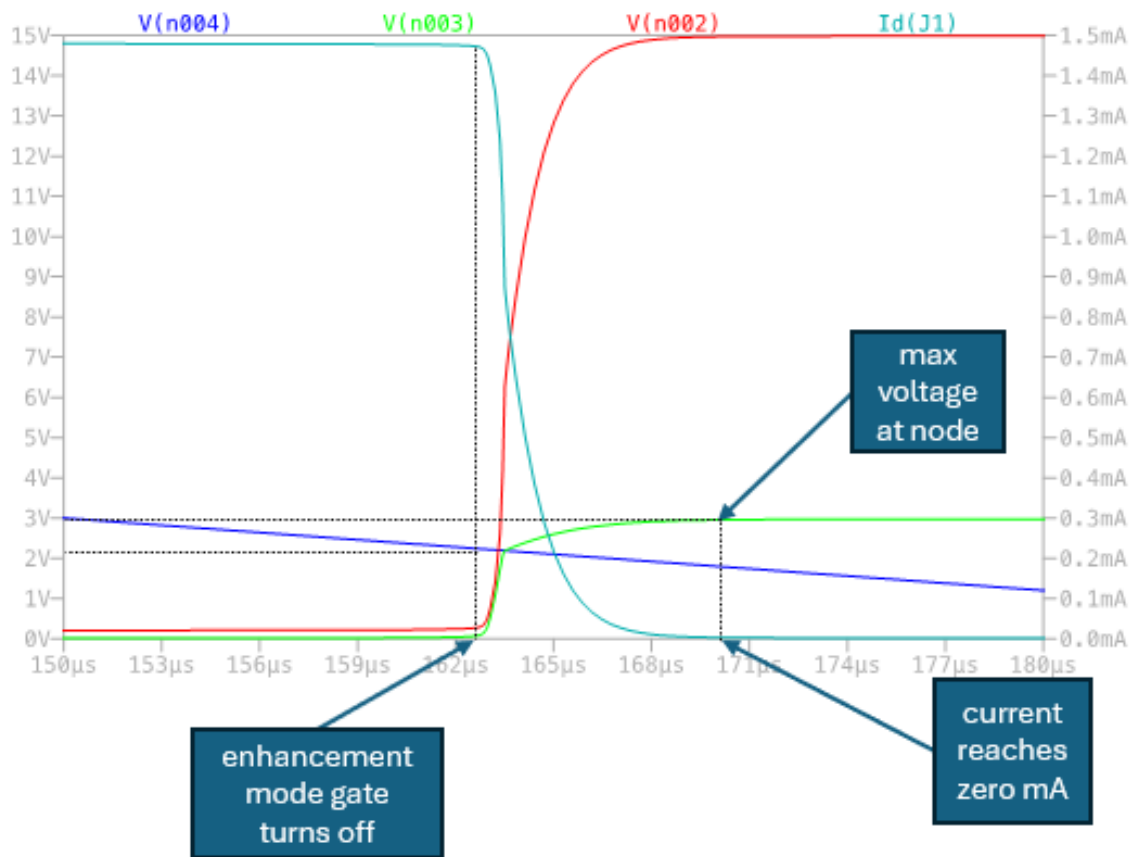
Ex-1032.

This figure shows this cascode works as an amplifier:

- In the first 100μs: V_{g1} , the input gate voltage at M2 (blue line, **V(n004)**) is high; the current in the device (cyan line, **Id(J1)**) is maximum; the drain voltage (red line, **Vn002**) is low; and the voltage at the middle node between the gates (green line, **V(n003)**) is zero. Ex-1032.
- From 100-200μs, the gate voltage at M2 (**V(n004)**) ramps down to zero, and the current (**Id(J1)**) begins to drop when V_{g1} crosses the threshold voltage and the first gate (M2) turns off. Ex-1032. But because the upper transistor is normally ON with zero volts input, the current continues to flow while the voltage at the middle node between the gates rises (green line, **V(n003)**). Ex-

1032. Once the drain voltage reaches the negative of the pinch-off voltage from the upper transistor (3V in this simulation), all remaining voltage is only across the upper transistor, as reflected in the red curve (**Vn002**). Ex-1032. Hence, the green curve (**V(n003)**) of voltage at the middle node between the gates (**V(n003)**) reaches a maximum at the pre-determined pinch-off, or negative threshold voltage of the upper transistor, J1 (Q2 of the '003 patent). Ex-1032. The current also reaches zero at when the maximum voltage is reached and the second gate is at pinch-off voltage. Ex-1032. **The current in the second portion of the transistor, J1, thus conducts until the voltage difference between ground (the input to J1) and a voltage at a node between the first and second gate (**V(n003)**) reaches the predetermined pinch-off voltage.** Ex-1032.

This transition is seen in close-up with the next figure, having the same color codes as the first figure, with annotations showing when the enhancement mode gate turns off, and when the maximum voltage at the node is reached and current reaches zero.



Ex-1032 (annotated)

This figure shows the middle 30μs of the same simulation, starting from time 150μs until 180μs, showing the transition from ON to OFF. Ex-1032. The lower, enhancement mode transistor M2 turns OFF when the gate voltage goes below the threshold voltage, at which point the upper transistor is still ON, and the voltage at the node (i.e., the drain of M2 (Q1 of the '003 patent) and source of J1 (Q2 of the '003 patent), rises with the voltage of the drain of the upper, depletion mode transistor, J1 (Q2 of the '003 patent). Ex-1032. When the gate to source voltage of the second transistor reaches the pinch-off voltage of -3V, then the upper transistor

turns off and the drain of the lower transistor can no longer rise. Ex-1032. I note that the foregoing results and description are exemplary only, and I observed similar results that support my opinion when varying the parameters of this simulation (e.g., when increasing or decreasing voltage V1).

VIII. LEVEL OF ORDINARY SKILL

[067] In rendering the opinions set forth in this declaration, I have been asked to consider the '003 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as “one skilled in the art,” “skilled artisan,” “POSITA,” “POSA” or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

[068] Taking the factors described in the Legal Standards – Level of Ordinary Skill in the Art section into consideration, it is my opinion that a person of ordinary skill in the art with respect to the '003 patent would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design. Additional education could substitute for professional experience and vice versa.

[069] Based on my educational background and experience, I was at least a person of ordinary skill in the art at the earliest priority date of the '003 patent.

IX. CLAIM CONSTRUCTION

[070] I am not an attorney. However, I have been informed by counsel of certain legal standards that apply with respect to claim construction and indefiniteness, and I have used those standards, described below in formulating my opinions.

[071] I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures (Ex-1001), and the patent’s prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent (Ex-1002). I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term’s plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent’s written description, the patent’s prosecution history, or both.

[072] I understand that claim interpretation may also be informed by “extrinsic evidence” (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the relevant time period.

[073] I was also informed by counsel that the applicant of the '003 patent can act as their own lexicographer, to set forth a definition of a claim term in the specification. The definition provided by the applicant can differ from the claim term's plain and ordinary meaning. I have also been informed by counsel that when a patent claim uses the term “comprises” as a transitional statement after the preamble, there is a presumption that the claim is open-ended and not limited to the recited elements.

[074] Based on my review of the materials cited herein and my personal knowledge and experience, I have considered the plain and ordinary meaning of each term of the '003 patent as it would have been understood by one skilled in the art at the earliest claimed priority date of the '003 patent of March 20, 2006. I apply the plain and ordinary meaning of each claim term throughout this declaration.

X. THE PRIOR ART

[075] In forming my opinions, I found the following prior art relevant when considering whether the claims of the '003 patent would have been obvious to a person of ordinary skill in the art:

- Ex-1006, U.S. Patent No. 6,160,280 to Bonn et al. (“Bonn”)
- Ex-1007, U.S. Patent No. 6,483,135 to Mizuto et al. (“Mizuto”)
- Ex-1008, U.S. Patent Publication No. 2004/0041169 to Ren et al. (“Ren”)
- Ex-1009, U.S. Patent Publication No. 2005/0051800A1 to Mishra et al. (“Mishra”)

[076] None of these references were cited during prosecution or considered by the Examiner. Ex-1002; Ex-1001, Cover. Based on my review, Bonn, Mizuto, Ren, and Mishra are not cumulative of the prior art considered during prosecution because the grounds presented herein teach the only claim feature the patent applicant argued was not disclosed by the prior art and which the Examiner identified in the statement of reasons for allowance— “wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion

mode transistor at the node in the semiconductor element.” Ex-1002, 18 (reasons for allowance).

A. Overview of Bonn (U.S. 6,160,280)

[077] Bonn is a U.S. patent issued December 12, 2000 directed to field effect transistors in a cascode arrangement for use as a downconverter. Bonn, Cover, 1:4-46. The corresponding application was filed March 4, 1996. I understand that Bonn is accordingly a prior art reference under 35 U.S.C. § 102(a).

[078] Like the '003 patent, Bonn discloses a field effect transistor in a **cascode** arrangement. Bonn, Abstract, 1:20-23, 2:66-3:22, 3:32-41, Fig. 1. Bonn describes “a **mixer 40** which comprises FETs 30 and 50 coupled in a **cascode** configuration.” Bonn, 2:66-3:6.

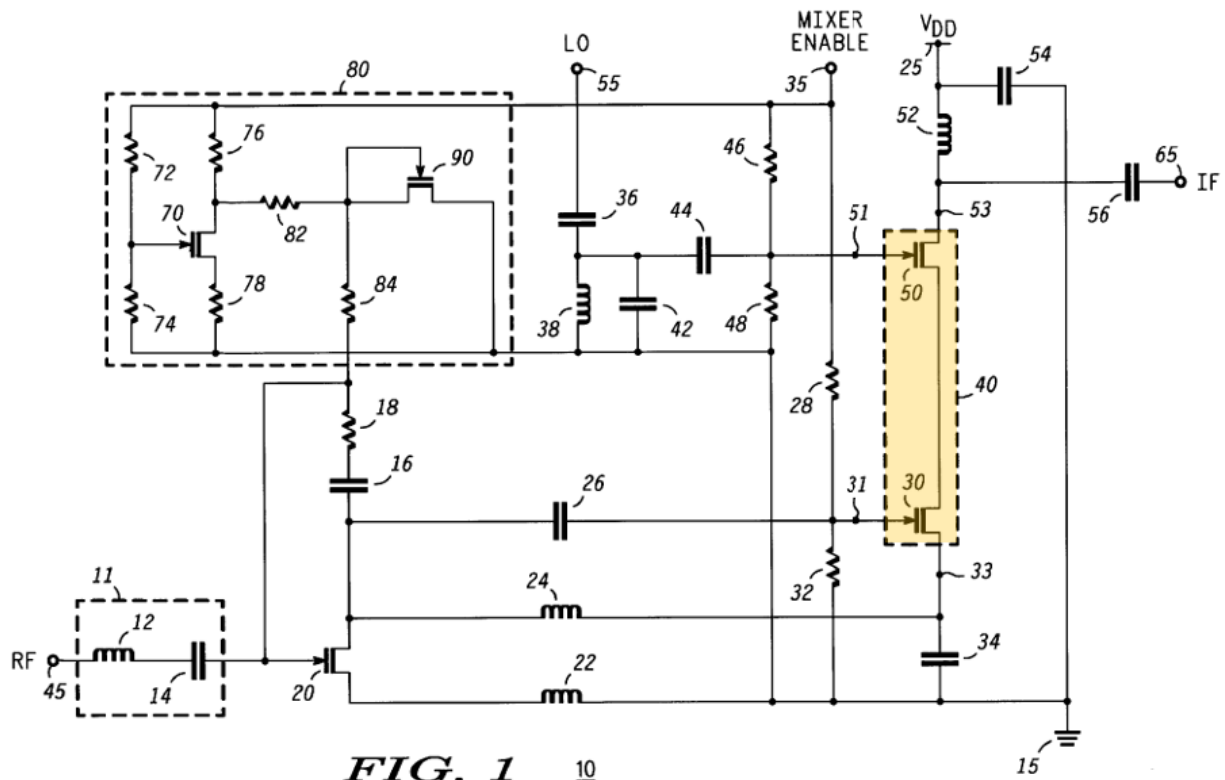


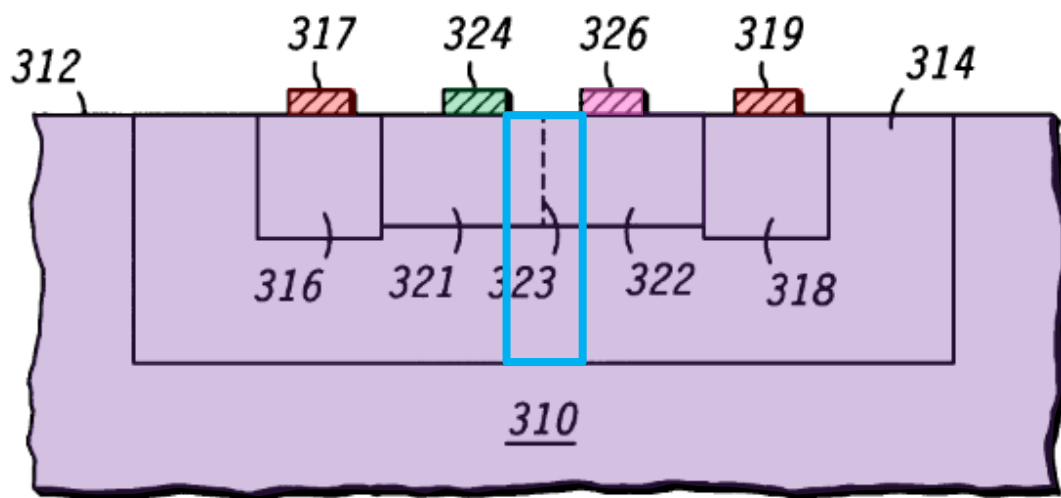
FIG. 1 10

Bonn, Fig. 1 (annotated)

[079] Also, like the '003 patent, Bonn's cascode is comprised of two gates formed on a single semiconductor structure. Bonn explains this arrangement uses minimal chip area. Bonn, 1:44-45, 5:42-43, 11:26-30.

[080] Figure 7 shows **structure 300**, an embodiment of **cascode mixer 40**, which includes "a body of semiconductor material or **substrate 310** having a **major surface 312**." Bonn, Fig. 7, 8:13-8:28; *see* Bonn, 8:13-9:27. The **substrate** may be gallium arsenide, with an impurity well 314 that enables different doping concentrations to form different types of gates. Bonn, 8:13-28.

[081] Bonn discloses the same arrangement as the '003 patent. Specifically, Bonn discloses “[a] **first gate structure 324** is formed on **major surface 312** above first gate region 321 and a **second gate structure 326** is formed on **major surface 312** above second gate region 322.” Bonn, 9:5-8. As shown in Fig. 7, the **first gate** is closer to **source electrode 317**, while the **second** is closer to **drain electrode 319**, and these gates are **separated by a region** of the **semiconductor**. Bonn, 8:33-35, Fig. 7. The **first gate** is in enhancement mode, and the **second gate** is in depletion mode. Bonn, 8:51-9:4. Bonn describes Figure 7’s dual gate FET as a “preferred embodiment” and discloses using it “in high frequency signal mixing,” such as the mixer of Figure 1, “as well as other applications such as high frequency signal amplification.” Bonn, 11:26-37.



300

FIG. 7

Bonn, Fig. 7 (annotated)

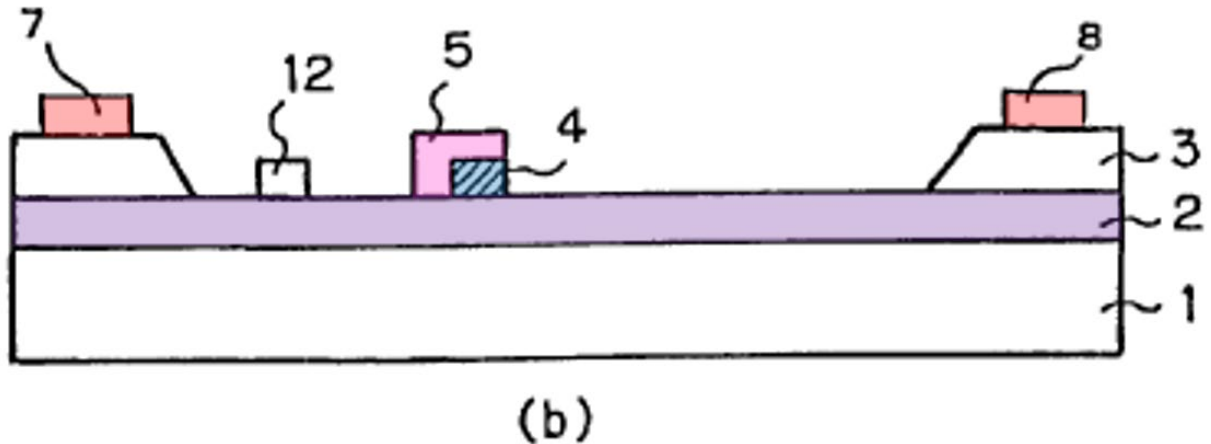
[082] Bonn's examples include gallium arsenide devices, which was a common semiconductor material when it was filed in 1996 (and remains common today). But Bonn teaches its structures are not limited to gallium arsenide and may include other types of FETs. Bonn, 11:11-22.

B. Overview of Mizuto (Ex-1007, U.S. 6,483,135)

[083] Mizuto is a U.S. Patent issued November 19, 2002. Mizuto, Cover. I understand that Mizuto is accordingly a prior art reference under 35 U.S.C. § 102(a).

[084] Mizuto discloses an overhanging drain-side field plate in gallium arsenide FETs and describes its benefits. Mizuto, 1:50-59, 2:12-45, 8:39-44, Figs. 2(g), 3(d), 5(e), 6(d), 7, 9(f), 10, 11(a)-(b), 12, 13, 16(g). Mizuto explains that overhanging field plate extensions assist with electrical field relaxation and improve breakdown voltage. Mizuto, 2:13-36. They further provide improved gain, especially at high frequency. Mizuto, 1:61-65. Mizuto shows and describes use of overhanging field plates over insulating dielectrics in a variety of configurations, including in eleven disclosed examples. Mizuto, 7:64-14:12, Figs. 2(g), 3(d), 5(e), 6(d), 7, 9(f), 10, 11(a)-(b), 12, 13, 16(g). Figure 11(b) shows one example overhanging field plate, which includes **source** and **drain** electrodes 7 and 8,

respectively, with **gate electrode 5** having a **field plate section** over **dielectric film 4** on **channel layer 2**. Mizuto, 12:30-47.

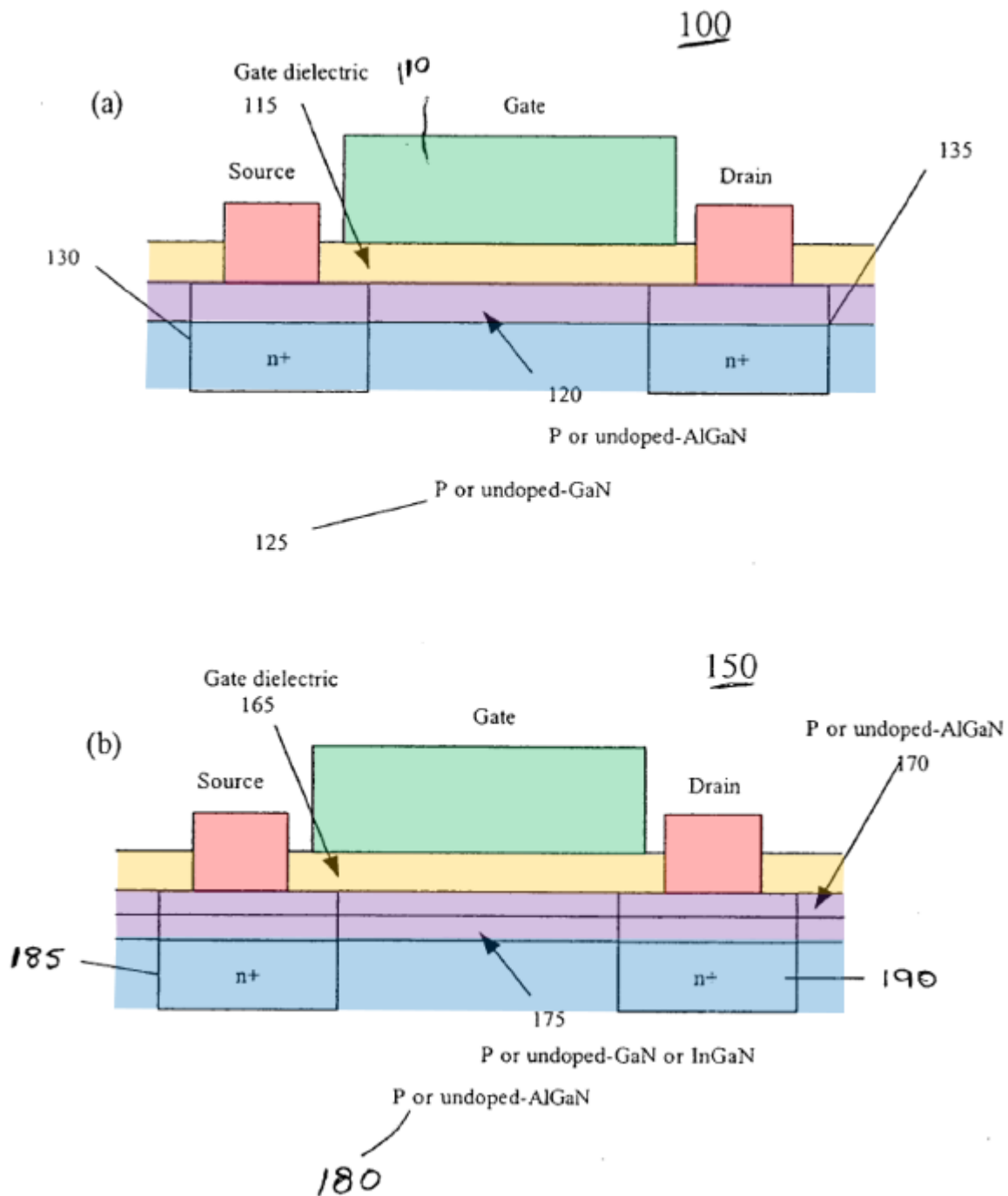


Mizuto, Fig. 11(b).

C. Overview of Ren (Ex-1007, U.S. 2004/0041169)

[085] Ren is a U.S. Patent Publication which published March 4, 2004. Ren, Cover. I understand that Ren is accordingly a prior art reference under 35 U.S.C. § 102(a).

[086] Ren describes a gallium nitride (GaN) MOSFET. Ren, Abstract, ¶¶[0003], [0013]-[0018]. Figs. 1-2. Ren's device includes a **gate electrode** between a **source** and **drain** electrode, over a **gate dielectric** and above an **AlGaN layer**, which may be doped p-type or undoped, which is over a **GaN or InGaN channel layer**. Ren, ¶¶[0035]-[0036], Figs. 1(a)-(b).



Ren, Figs. 1(a)-1(b) (annotated)

[087] Ren teaches the thickness of the **AlGaN layer** determines whether the device is in enhancement mode or depletion mode. Ren, ¶¶[0014], [0033]. A thin

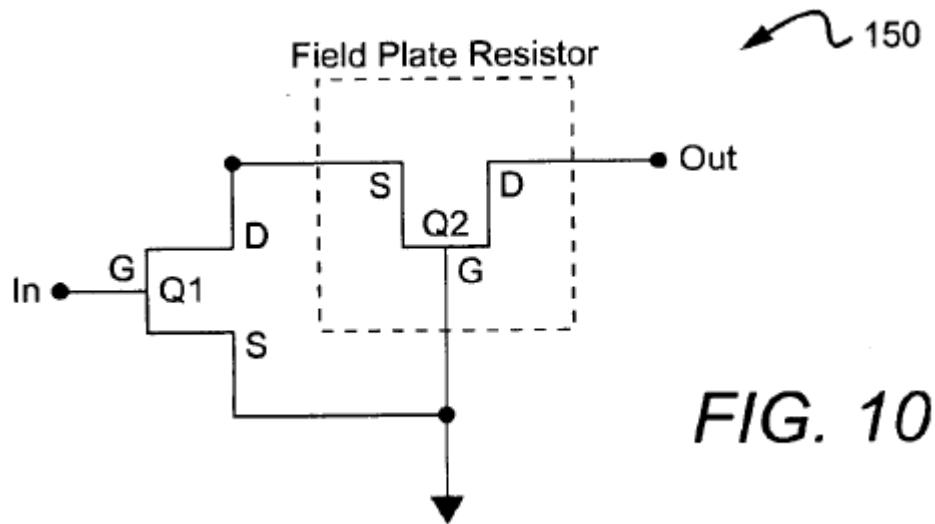
layer (e.g., less than 20 nm) permits enhancement mode operation, while a thick layer (e.g., above 20 nm) operates in depletion mode. Ren, ¶¶[0014], [0033].

[088] Ren discloses that enhancement mode devices consume no power “during stand-by mode,” can operate at high temperature, and have low switching losses. Ren, ¶[0040].

D. Overview of Mishra (Ex-1009, U.S. 2005/0051800A1)

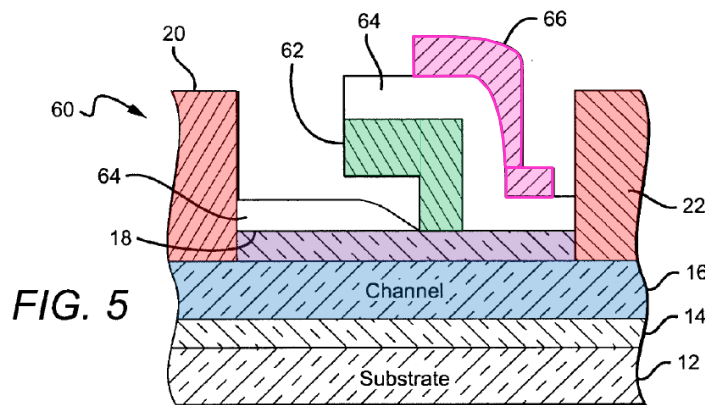
[089] Mishra is a U.S. Patent Publication which published March 10, 2005. Mishra, Cover. I understand that Mishra is accordingly a prior art reference under 35 U.S.C. § 102(a).

[090] Mishra discloses GaN HEMT cascode amplifiers with field plates. Mishra, Title, Abstract, [0002]-[0010]. Mishra teaches field plates in GaN transistors reduce peak electric field, increase breakdown voltage, and reduce electron trapping. Mishra, ¶¶[0029], [0054], [0060]. Figure 10 shows an example cascode transistor in which the drain side gate Q2 includes a field plate.



Mishra, Fig. 10.

[091] In one embodiment of the cascode, Mishra discloses a **gate electrode** between a **source** and **drain** electrode, and a **grounded field plate** over a dielectric and above an **AlGaIn layer**, which may be doped p-type or undoped, which is over a **GaN or InGaIn channel layer**. Mishra, ¶¶[0030]-[0035], [0042]-[0044], [0054]-[0062].



Mishra, Fig. 5 (annotated).

XI. OVERVIEW OF THE GROUNDS

Grounds		Challenged Claims	Basis	Prior Art
Bonn Grounds	1	1	§103	Bonn in view of Mizuto
	2	1-16	§103	Bonn in view of Ren and Mishra
Mishra Grounds	3	1-16	§103	Mishra in view of Ren

XII. GROUND 1: BONN AND MIZUTO (CLAIM 1)

[092] Claim 1 of the '003 patent is unpatentable in view of Bonn and Mizuto.

A. Motivation to Combine Bonn and Mizuto

[093] In my opinion, a person of ordinary skill would have found it obvious to use Bonn's cascode transistor for high frequency signal amplification and to further improve the cascode with Mizuto's teaching to use field plates to improve performance characteristics.

1. Motivation to Modify Bonn for High Frequency Signal Amplification

[094] Bonn discloses "[d]ownconverter 10 also includes a **mixer 40** which comprises **FETs** 30 and 50 coupled in a **cascode** configuration and serving as mixer transistors." 2:66-3:1. The downconverter "combines a radio frequency (RF)

signal and a local oscillator (LO) signal to provide an intermediate frequency (IF) signal.” Bonn, 2:8-12.

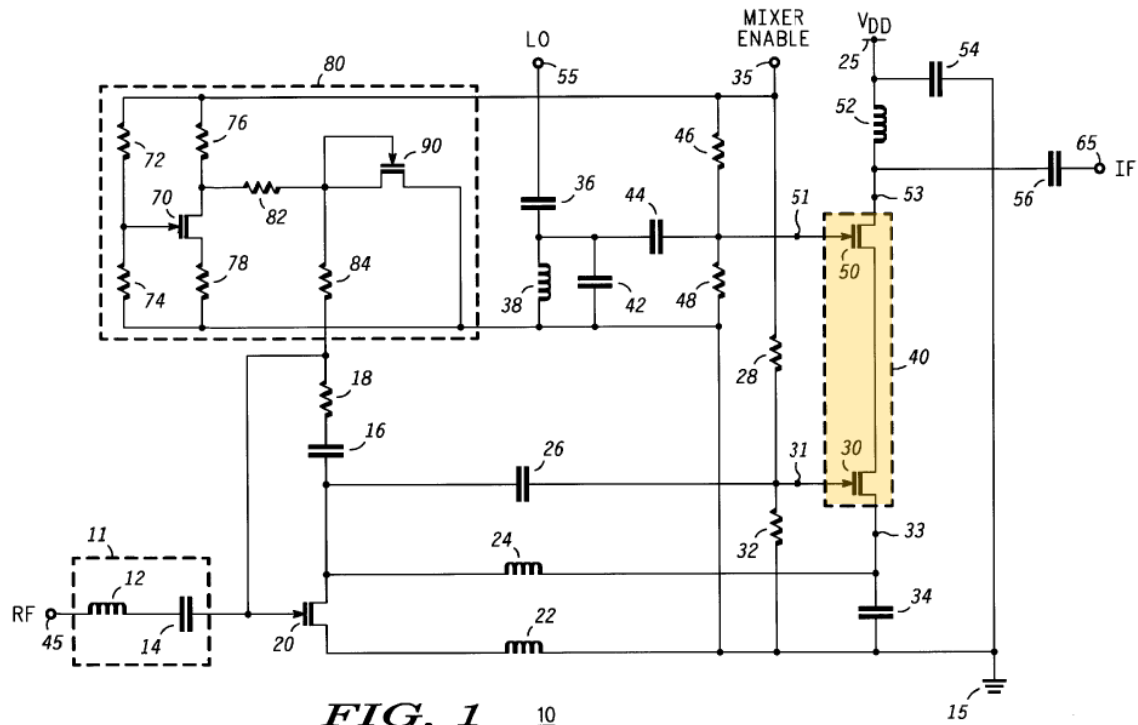


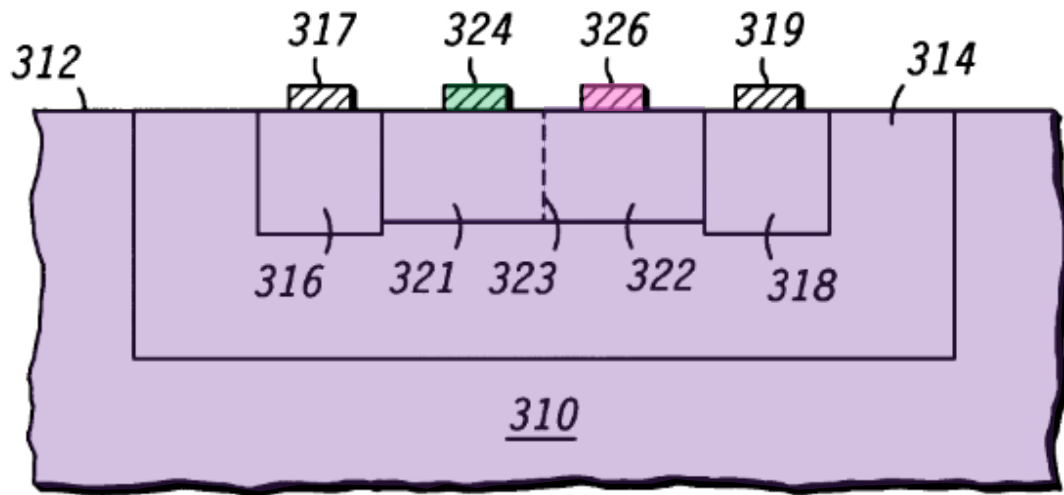
FIG. 1 10

Bonn Fig. 1 (annotated)

[095] Embodiments of mixer 40 of Figure 1 include a **dual gate FET**.

Bonn, 3:13-21, 5:57-67, 11:26-28, Fig. 7. Rather than using two distinct FETs for the mixer of Figure 1, Bonn discloses using a **dual gate FET 300** of Figure 7 over a **semiconductor 310** in an embodiment of **mixer 40** of Figure 1, as I illustrate below. Bonn, 8:13-9:28, 11:26-37, Fig. 7. Regarding Figure 7, Bonn states, “[a] **first gate structure 324** is formed on **major surface 312** above first gate region 321 a **second gate structure 326** is formed on **major surface 312** above second

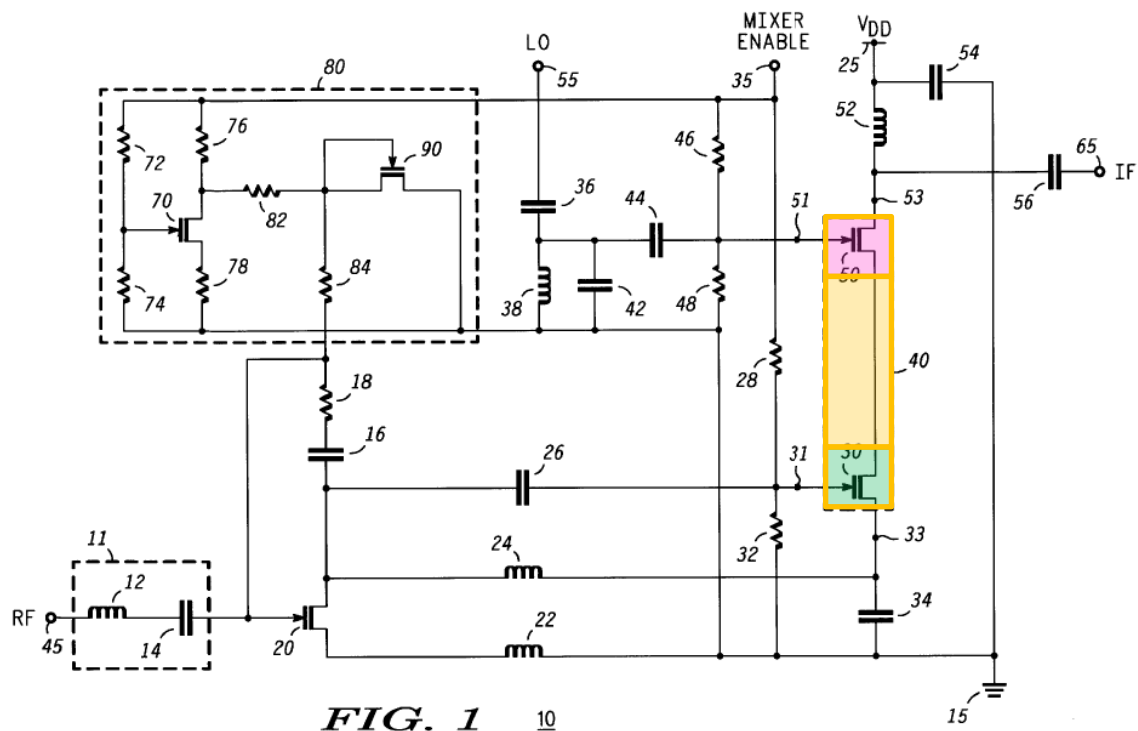
gate region 322.” Bonn, 9:5-8. The “first gate region 321 is in an enhancement mode and second gate region 322 is in a depletion mode.” Bonn, 8:51-9:4.



300

FIG. 7

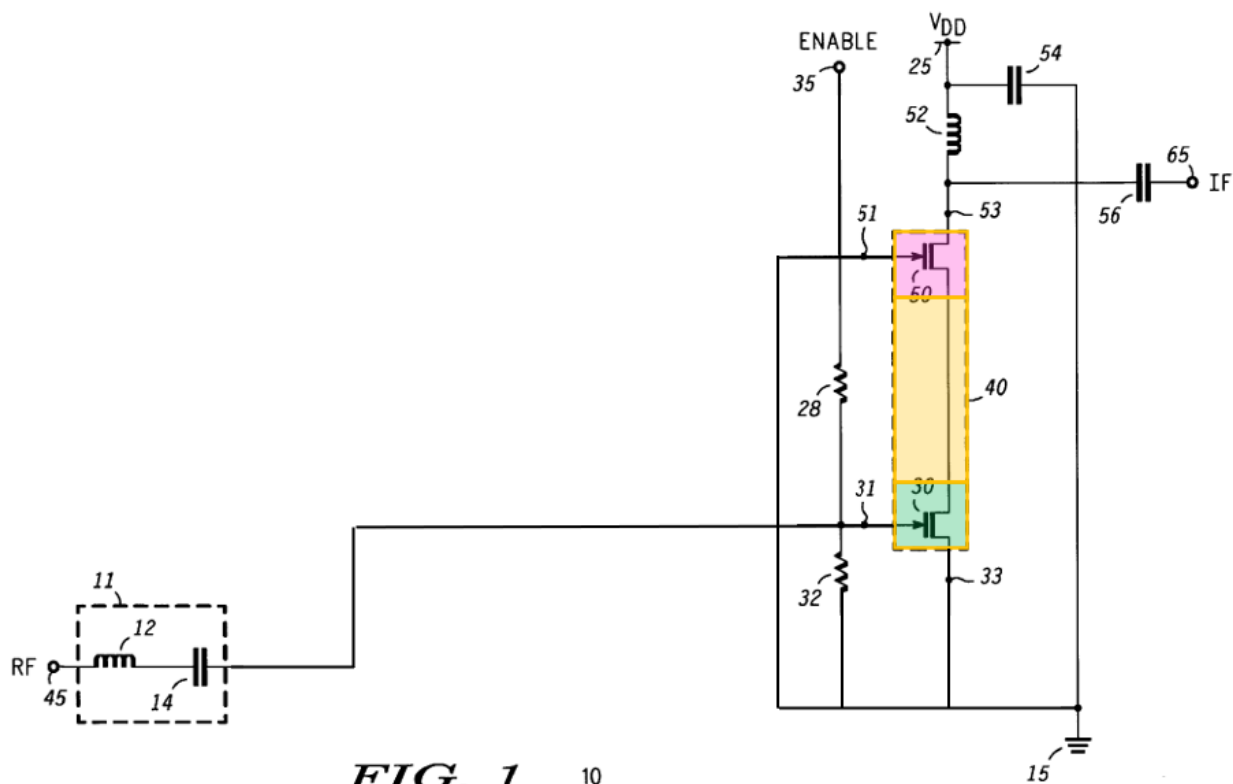
Bonn, Fig. 7 (annotated).



Bonn, Fig. 1 (annotated to show implementation of Figure 7's dual FET transistor)

[096] In addition to using Figure 7's "dual gate FET structure in high frequency signal mixing" applications as shown above in annotated Figure 1, Bonn discloses using this dual gate FET in "*other* applications such as high frequency signal amplification." Bonn, 11:26-37. Bonn thus teaches using its dual gate structures for signal amplification without signal mixing. Bonn explains signal amplification can be readily achieved because the gates of its dual gate FET have "individually adjusted" parameters "for optimum performance," such as "gate width, dopant concentration, and channel depth." Bonn, 5:60-65, 7:28-34, 9:18-21 11:26-37.

[097] Based on these teachings, a POSITA would have found it obvious to make simple modifications to the circuit of Figure 1 and use Figure 7's structure for high frequency signal amplification in place of **mixer 40**. Those modification are shown below.



Bonn, Figure. 1 (modified for high frequency signal amplification, annotated).

[098] As shown above, to achieve the “high frequency signal amplification” with Figure 7's dual gate FET structure as Bonn expressly teaches (Bonn, 11:26-37), a POSITA would have found it obvious to remove Figure 1's LO (local oscillator) port 55 and its associated impedance matching components because the LO signal is no longer being mixed. Bonn, 3:30-41 (“Capacitors 36, 42, and 44 and

inductor 38 cooperate to form an impedance matching element for providing a desired input impedance, e.g., 50 Ω , at LO port 55.”). Bonn emphasizes that the RF and LF circuitry are isolated from one another. Bonn, 1:20-23, 3:19-21 (“It should be noted that the cascode and dual gate embodiments of mixer 40 prevent the RF circuitry and the LO circuitry from interacting with each other.”). To achieve Bonn’s high frequency *signal amplification*, a POSITA would accordingly have removed Bonn’s LO circuitry with predictable success, i.e., without impacting the RF circuitry.

[099] Likewise, when implementing Bonn’s explicit teaching to use Figure 7’s dual gate FET structure for “high frequency signal amplification,” a POSITA would have found it obvious to remove FET 20 and associated circuitry. Bonn, 11:26-37. FET 20 is a low noise amplifier for receiving the RF signal that amplifies the signal prior to mixing at mixer 40. Bonn, 2:8-17. But Bonn also teaches using the dual gate FET 300 for the purpose of high frequency signal amplification, instead of FET 20, which greatly simplifies the circuitry, as shown above. Bonn, 11:26-37. A POSITA would have found it obvious to remove FET 20 and associated circuitry when using a dual gate FET for signal amplification over Bonn’s goal of designing circuits “with minimum chip area.” Bonn, 1:44-45, 5:42-43, 11:26-30.

[100] As shown, when removing FET 20 and using dual gate FET 300 for signal amplification, a POSITA would have found it obvious that this implementation does not require voltage source 80, because its function of biasing FET 20 to amplify the signal is not necessary, and would have found it obvious that capacitor 16 and resistor 18 are not needed because they are “optional” and serve to “establish a negative feedback loop for FET 20” between voltage source 80 and FET 20. Bonn, 2:27-65. Over Bonn’s teachings, a POSITA would also have removed: capacitor 26, which “functions as an impedance matching element between the drain of FET 20 and first gate terminal 31” (Bonn 3:23-29); inductor 24, which couples FET 20 to source terminal 33 (Bonn, 3:42-44); and inductor 22, which is “optional” and “provides a DC path from the source electrode of FET 20 and adjusts the noise characteristics of the LNA by altering its impedance”(Bonn, 2:34, 4:47-49). A person of ordinary skill would have found these modifications simple and obvious over Bonn’s teaching to use dual gate FET 300 for signal amplification and Bonn’s goal of designing for “minimum chip area.” Bonn, 1:44-45, 5:42-43, 11:26-37.

[101] In signal mixing embodiments, Bonn “shunts the AC signal from the source terminal 33 of mixer 40 to ground” via capacitor 34 so that FET 20 is not affected by feedback and noise. 5:9-14. Capacitor 34 and inductor 24 together “provide a low frequency path from the drain electrode of FET 20 to power supply

conductor 15 for the [intermediate frequency] IF noise components generated by FET 20,” i.e., they provide path from FET 20 to ground. Bonn, 4:14-15. In high frequency signal amplification embodiments without FET 20 and inductor 34, however, there would have been no such “IF noise components generated by FET 20” at source terminal 33, so a POSITA would have eliminated capacitor 34 and made a direct DC path from source terminal 33 of the dual gate FET to ground to form a common source amplifier, as shown above.

[102] Further, a POSITA would have removed capacitor 34 shorting first **gate structure 324** to increase the voltage difference between V_{DD} and the source terminal 33, which increases gain of the circuit. Increased gain increases signal amplification.

[103] In addition, a POSITA would have been further motivated to remove capacitor 34 because Bonn discloses first **gate structure 324** is in enhancement mode. If capacitor 34 was present between the source and ground, voltage would climb at the capacitor during operation, which reduces the gate-to-source voltage difference (voltage difference between first gate terminal 31 and source terminal 33). Accordingly, this unnecessarily increases the voltage required at first gate terminal 31 to turn on the enhancement mode device, while removing capacitor 34 lessens the voltage required at terminal 31 to turn on the gate, thereby motivating a POSITA to remove capacitor 34.

[104] In addition, because signals are not mixed in Bonn's high frequency signal amplification application and the second **gate structure 326** operates in depletion mode (ON at 0V), a POSITA would have understood the voltage divider at resistors 46 and 48 is not needed. Bonn explains the second gate FET 50 in mixing embodiments is enabled by setting the voltage at the voltage divider at resistors 46 and 48 (Bonn, 4:37-40) and disabled when that voltage is "near ground potential" (Bonn, 5:15-31). Without the LO signal in the signal amplification embodiment, those resistors would set the voltage at terminal 51 to a constant voltage at a value between V_{DD} and drain. But a POSITA would have understood that second **gate structure 326** allows channel conduction at ground potential (0V) because it is a depletion mode gate when using dual gate FET 300 for signal amplification. Bonn, 8:51-9:4. A POSITA would thus have been motivated to short terminal 51 to ground, as shown, to set the constant voltage at terminal 51 to zero volts.

[105] A POSITA would also have been motivated to remove resistors 46 and 48 and short terminal 51 to ground (power supply conductor 15) to reduce the Miller feedback noise at terminal 51 since this device is in depletion mode (i.e., ON at zero volts). Power supply conductor 15 operates at ground potential (zero volts). Bonn, 2:23-28, 3:65-67, 4:63-64, 5:1-8, Fig. 1. In general, a POSITA would have known the Miller effect is a negative feedback from the drain to the gate of a

transistor. *E.g.*, Potirakis (Ex-1025). A POSITA would have further understood a cascode avoids the Miller feedback by having a second, upper gate, providing a capacitively coupled direct pathway between it's the drain and ground. *See, e.g.*, Lerdworatawee (Ex-1026) at 1, 2, Fig. 1 (pathway via “output matching network”), Ko (Ex-1027) (discussing noise in various cascode topologies). Bonn's Figure 1 does the same by including a pathway from terminal 51 to ground via resistor 46. In the high frequency signal amplification embodiment, removing resistor 46 maintains a pathway from terminal 51 of the second transistor to ground, so feedback from the drain side cannot reach **gate structure 326**, which continues to allow channel conduction at zero volts (applied bias) because it is depletion mode.

[106] This is the way a cascode transistor works in a normal amplifier circuit. The Miller feedback from the dV/dt voltage rise of the drain of the upper transistor flows through the gate of Q2 and directly to ground, avoiding noise at the input to Q1, which is the RF input. Thus, a POSITA would have been motivated to short the second gate to ground to allow the drain side voltage to be raised higher and achieve high gain with less noise than a single transistor amplifier, thereby achieving Bonn's goal of high frequency signal amplification. Bonn, 11:26-37. This arrangement of enhancement mode and depletion mode transistors—with the source of the enhancement mode gate at ground potential and the input to the

depletion mode gate also connected to ground—was known in cascodes. *E.g.*, Mishra, ¶¶[0055]-[0056], [0058], Fig. 10; Sankin, ¶¶[0013], [0119], Fig. 1.

[107] A POSITA would have had predictable success when making this modification because the modification enables enhancement mode **gate structure 324** to control current in the dual gate FET 300 depletion mode **gate structure 326**. As explained above, a POSITA would have been familiar with this common arrangement and would have understood that the first, enhancement mode gate is OFF at 0V applied bias, and the voltage on the source side of the depletion mode gate will climb until it also turns off when that gate reaches the pinch-off voltage. *See* § VII (Technological Background), above.

[108] In the above modified Figure 1, I relabeled “mixing enable” at “voltage supply conductor 35” as “enable” because no signals are mixed in this implementation. For a high-frequency amplification application, “voltage supply conductor 35” controls conduction in the dual gate FET 300 by turning enhancement mode **gate structure 324** of Figure 7 on and off, as it would for a signal mixing embodiment. Bonn, 5:15-31.

[109] In the modified Figure 1, the remaining components serve the same functions in the signal amplification embodiment as with the signal mixing embodiments. For example, “[f]irst gate terminal 31 is coupled to power supply conductor 15 via a resistor 32 and to voltage supply conductor 35 via a

resistor 28.” Inductor 12 and capacitor 14 “form an impedance matching element 11 for providing a desired impedance, e.g., 50 ohms (Ω), at RF port 45.” Bonn, 2:18-20. The drain side capacitors 54 and 56 form an impedance transformer with inductor 52 at IF port 65, and capacitor 54 provides an AC current path from V_{DD} to ground. Bonn, 3:49-53. In this embodiment, IF port 65 serves as an output terminal of the circuit that provides a high frequency amplified signal.

2. Motivation to Combine Bonn’s High Frequency Signal Amplification Embodiment with Mizuto’s Field Plate

[110] Bonn’s drain voltage at drain terminal 53 (V_{DD} at power supply conductor 25 of Figure 1) is at a “high voltage level.” Bonn, 4:31-40. In my opinion, a POSITA would have been motivated to include Mizuto’s field plate over a dielectric in Bonn’s **second gate 326** for electric field relaxation, to improve gain at high frequency, and to improve characteristics to withstand these high voltages. Mizuto, 1:27-30, 1:61-65, 2:13-45.

[111] In Bonn’s high frequency signal amplification embodiment, **dual gate FET 300** of Figure 7 provides signal amplification. *See* § XII.A.1 (Motivation to Modify Bonn for High Frequency Signal Amplification), above. Bonn explains the drain voltage the drain terminal 53 (voltage supply V_{DD} of Figure 1) is at a “high voltage level” in signal mixing embodiments. Bonn, 4:31-40. A high voltage level V_{DD} is also consistent with Bonn’s goal of “high frequency signal amplification.”

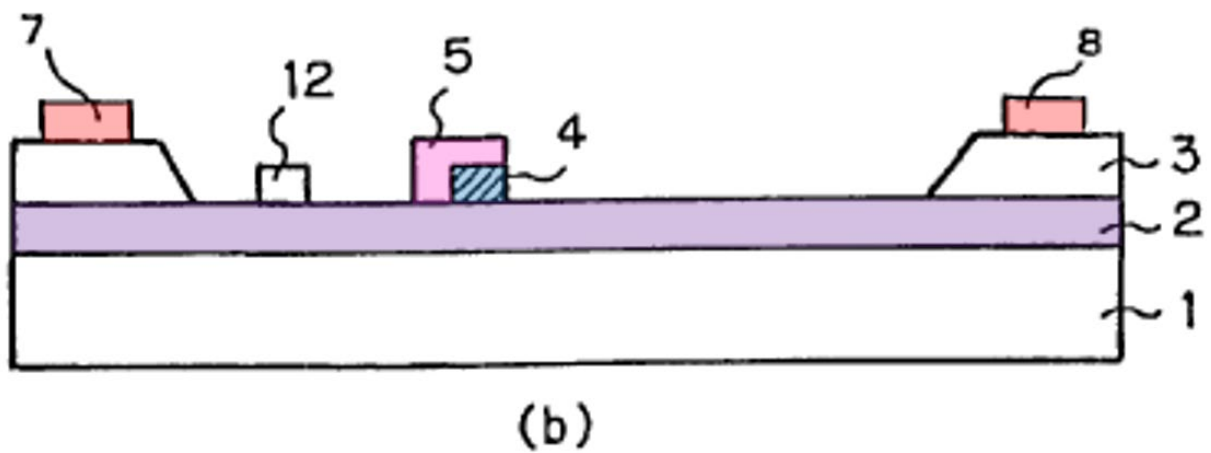
Bonn, 11:26-37. A POSITA would have applied high voltages at the drain of **second gate 326** (high voltage supply V_{DD} of Figure 1) in signal amplification embodiments. A POSITA would have understood a low voltage amplifier gets less gain, and the higher the voltage, the higher the gain (i.e., high voltages produce more signal amplification). This is a foundational principle in electrical engineering.

[112] In my opinion, a POSITA would have found it obvious to include Mizuto's field plate over a dielectric in Bonn's **second gate 326** for electric field relaxation, to improve gain at high frequency, and to "improve characteristics to withstand voltage." Mizuto, 1:27-30, 1:61-65, 2:13-45. Mizuto's overhanging field plate extensions improve electrical field relaxation and breakdown voltage. Mizuto, 2:13-36. And Mizuto's overhanging field plate provides improved gain, especially at high frequency. Mizuto, 1:61-65. Bonn seeks to improve performance in high frequency applications. Bonn, 1:8-23, 11:26-37. Mizuto discloses gate field plate extensions over insulating dielectrics in a variety of configurations for devices that improve device performance. Mizuto, 7:64-14:12, Figs. 2(g), 3(d), 5(e), 6(d), 7, 9(f), 10, 11(a)-(b), 12, 13, 16(g). These include a dual gate configuration. Mizuto, 12:30-47, Fig. 11(b).

[113] A POSITA would have been familiar with the many benefits of field plates in gallium arsenide devices that Mizuto teaches. It was well known at the

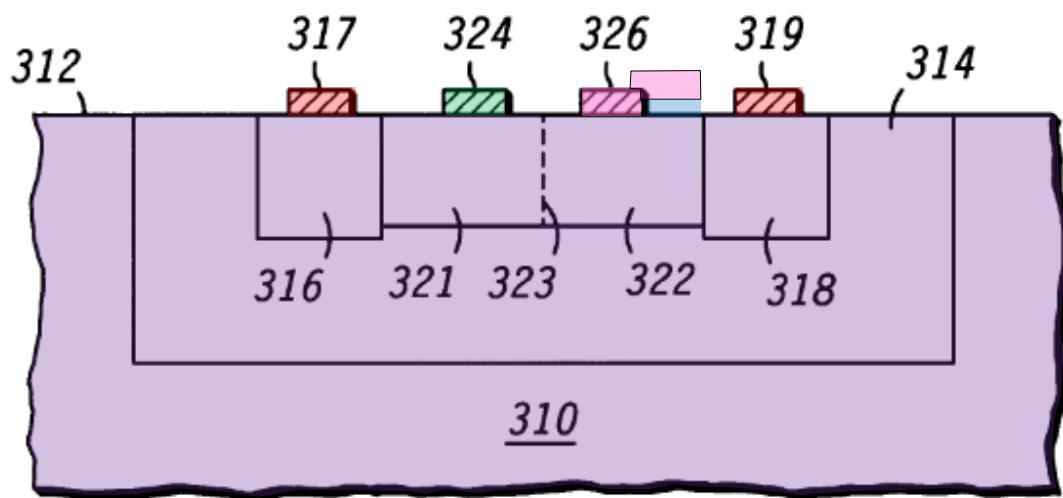
time of the '003 patent to use gate field plate extensions over a dielectric layer to control electric field and improve operating characteristics, including reduced peak electric field, increased breakdown voltage, reduced trapping, and reduced leakage, all with minimum impact on increased gate capacitance. Mizuto, 1:50-59, 2:12-45, 8:39-44; Mishra, ¶[0029]; Wakejima (Ex-1012), ¶¶[0053], [0064], [0219]-[0225], Figs. 23D-E, 24; Parikh (Ex-1013), ¶¶[0028], [0031]; Miyamoto (Ex-1014), 1:57-2:4, 3:11-26, 11:3-37; Sheppard (Ex-1015), 4:39-46. Further, field plates were used in dual gate cascodes like Bonn's structure 300 of Figure 7 before the '003 patent. Mishra, Abstract, ¶¶[0026]-[0030], [0048]-[0062], Figs. 5, 10.

[114] In view of this background knowledge and the teachings of Mizuto, a POSITA would have found it obvious to modify Bonn's **second gate structure 326** to include a **field plate extension** over a **dielectric** to achieve the many known benefits of field plates, including improved field relaxation, gain, and breakdown voltage. Mizuto, 1:61-65, 2:13-36.



Mizuto, Fig. 11(b).

[115] The resulting modified structure includes a field plate extension as shown in the modified Figure 7, below.



300

FIG. 7

Bonn, Fig.7 (modified to include a field plate extension on **second gate structure 326** over a **dielectric**)

B. Claim 1

[116] In my opinion, claim 1 is obvious over Bonn in view of Mizuto. As I will explain below, Bonn teaches every limitation of claim 1 except a field plate on the second gate structure. But the benefits of such field plates were well known, and it would have been obvious for a POSITA to include a field plate over the teachings of Mizuto. *See* § XII.A.2 (Motivation to Combine Bonn’s High Frequency Signal Amplification Embodiment with Mizuto’s Field Plate), above.

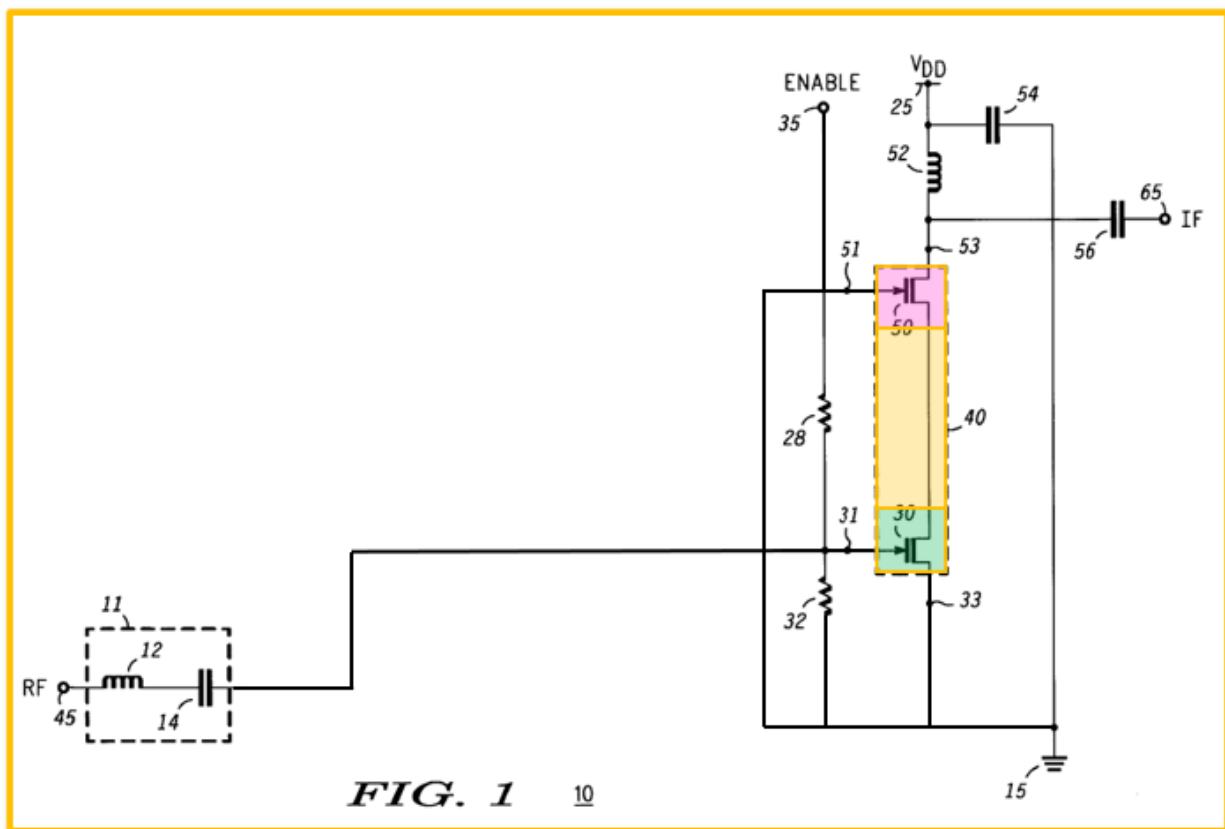
1. [1PRE] A merged cascode transistor circuit comprising:

[117] Bonn discloses or at least renders obvious [1PRE], a **merged cascode transistor** circuit. Bonn, 2:66-3:21, 5:32-56.

[118] Bonn states “[d]ownconverter 10 also includes a **mixer 40** which comprises **FETs** 30 and 50 coupled in a **cascode** configuration and serving as mixer transistors.” Bonn, 2:66-3:21. Downconverter 10 of Figure 1 is a **merged cascode transistor** circuit that includes cascode **mixer 40**.

[119] Further, as explained, Bonn discloses using its dual gate FETs for “high frequency amplification” without signal mixing. Bonn, 11:26-37. A POSITA would have been motivated to implement the dual gate FET of Bonn’s Figure 7, which has an enhancement mode **first gate** and depletion mode **second gate**, in a

modified version of the circuit of Figure 1. See § XII.A.1 (Motivation to Modify Bonn for High Frequency Signal Amplification), above. This modified circuit is also a **merged cascode transistor** circuit, as claimed, where the **first gate** and **second gate** share a common source the drain of the first gate is connected to the source of the second gate.

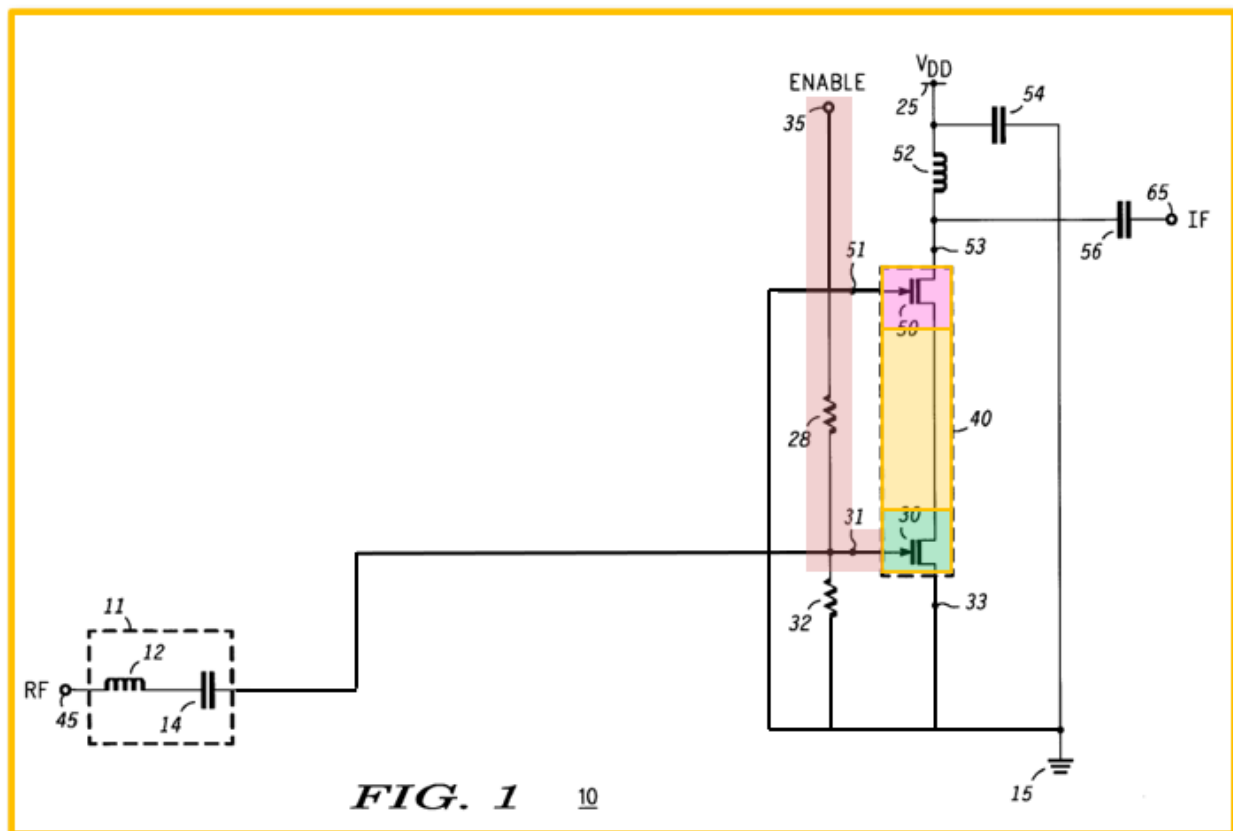


Bonn, Fig. 1 (modified for high frequency application, annotated)

2. [1A] an input voltage signal source having an input voltage signal;

[120] Bonn teaches [1A], an **input voltage signal source** having an input voltage signal. Bonn, 3:1-25.

[121] Bonn discloses a **voltage supply conductor 35** coupled to the first gate terminal 31 via resistor 28 that controls the potential of the first gate terminal 31. Bonn, 3:22-, 5:15-19, Fig. 1. First gate terminal 31 is coupled to enhancement mode **first gate 324** in the high frequency signal amplification embodiment. See § XII.A.1 (Motivation to Modify Bonn for High Frequency Signal Amplification), above. **Voltage supply conductor 35** is an **input voltage signal source** having an input voltage signal, as claimed.



Bonn, Fig. 1 (modified, annotated)

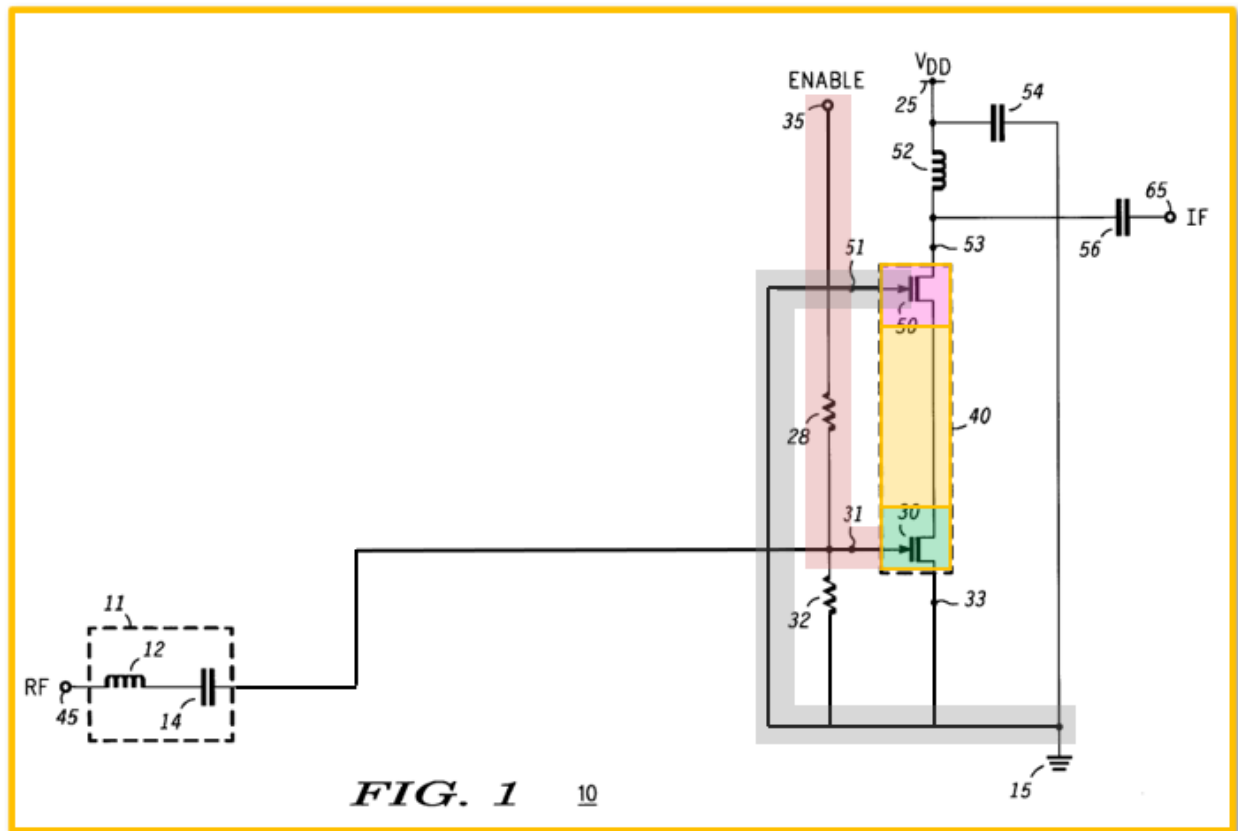
[122] Bonn thus teaches [1A].

3. [1B] a constant voltage source having a predetermined constant voltage;

[123] Bonn discloses or at least renders obvious [1B], a **constant voltage** source having a predetermined constant voltage.

[124] In signal mixing embodiments, Bonn discloses “second gate terminal 51 is coupled to power supply conductor 15 via a resistor 48 and to voltage supply conductor 35 via a resistor 46.” Bonn 3:30-32, Fig. 1. The voltage at the voltage divider of resistors 46 and 48 is a constant voltage source having a predetermined constant voltage, as claimed.

[125] In Bonn’s high frequency signal amplification embodiment with modified Figure 1, the depletion mode **second gate** is shorted to ground (**power supply conductor 15**) via terminal 51. *See* § XII.A.1 (Motivation to Modify Bonn for High Frequency Signal Amplification), above. **Power supply conductor 15** operates at ground. Bonn, 2:23-28, 3:65-67, 4:63-64, 5:1-8, Fig. 1. In this embodiment, **power supply conductor 15** is a **constant voltage** source having a predetermined constant voltage (i.e., 0V), as claimed.



Bonn, Fig. 1 (annotated)

[126] Like Bonn, the '003 patent describes the second gate is connected to ground—a **constant voltage** source. '003 patent, 3:42-46, Figs. 2-4.

4. [1C] a merged cascode transistor comprising:

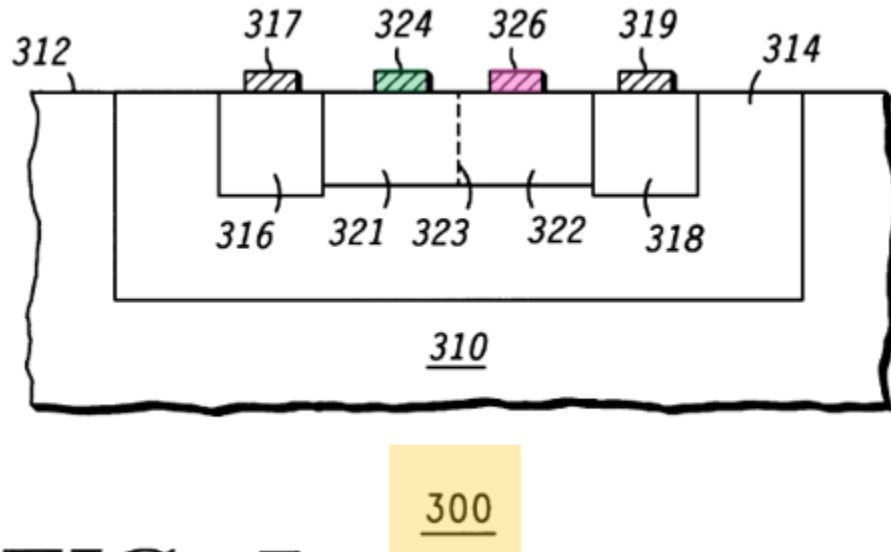
[127] Bonn discloses [1C], a **merged cascode transistor**.

[128] Embodiments of mixer 40 of Figure 1 include a “**dual gate FET**.”

Bonn, 3:13-21, 5:57-67, 11:26-37, Fig. 7. In these embodiments, rather than using two distinct FETs for the mixer of Figure 1, Bonn discloses “[a] **first gate** of the **dual gate FET** serves as first gate terminal 31 of **mixer 40** and a **second gate** of

the **dual gate FET** serves as second gate terminal 51 of **mixer 40**.” Bonn, 3:14-16 (referring to Fig. 1). Bonn explains the two gates the dual gate FET advantageously have “independently adjustable gate widths and channel properties,” including different “dopant concentration, channel depth, etc.” Bonn, 5:57-67, 8:51-9:4, 9:13-27, 11:22-37. It further teaches the dual gate approach “uses less chip area” than two separate FETs in cascode configuration. Bonn, 1:44-45, 11:22-37. Bonn teaches its dual gate FETs like the one in Figure 7 “can be tailored to provide superior performance over the prior art dual gate FET structures in ... high frequency signal amplification” applications. Bonn, 11:26-37. Thus, Bonn discloses configuring this cascode merged device as a single input, low-noise amplifier and not only as a mixer.

[129] Figure 7, below, depicts an example **dual gate FET 300** in **mixer 40** of Figure 1. Bonn, 8:13-9:28. Although Bonn does not expressly use the term “**merged cascode**,” this arrangement is the same as the “**merged cascode**” claimed and described in the '003 patent because it implements its cascode on a single semiconductor with two laterally spaced gates connected in series between a source and drain. *See* § VI (OVERVIEW OF THE '003 PATENT), above.

**FIG. 7**

Bonn, Fig. 7 (annotated).

5. [1C1] a semiconductor element; [1C2] a source electrode electrically connected to a top surface of the semiconductor element; and [1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;

[130] Bonn discloses [1C1]-[1C3], which are entirely conventional. Fig. 7.

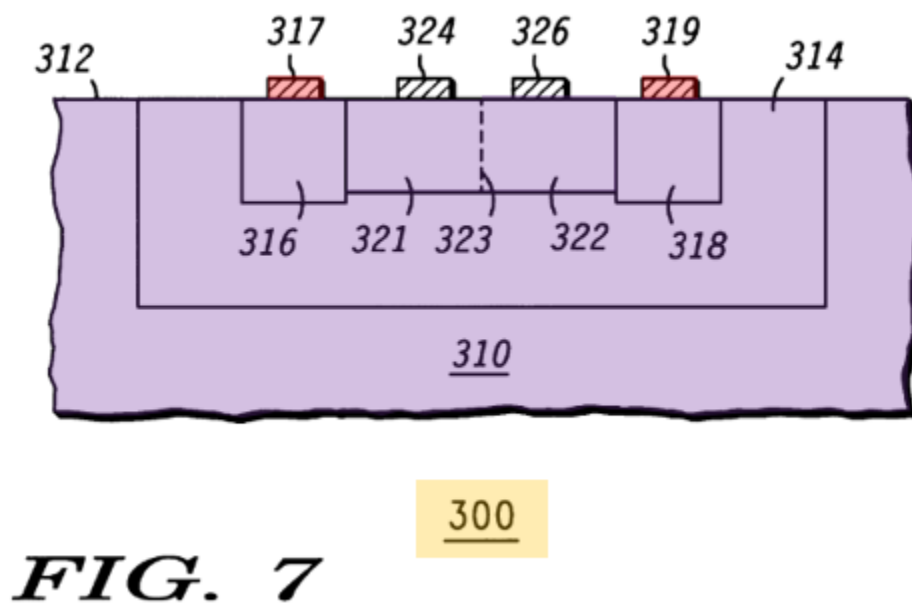
[131] Bonn discloses [1C1] because it discloses a semiconductor element.

Bonn discloses “**semiconductor material or substrate 310**,” which is the claimed **semiconductor element** because it comprises a semiconductor material. Bonn, 8:15-28. **Semiconductor 310** may be a GaAs material. Bonn, 8:15-28.

[132] Bonn discloses [1C2] and [1C3] because it discloses source and drain electrodes electrically connected to a top surface of the semiconductor element and spaced laterally across the surface of the semiconductor element. Bonn states, “[a]

source electrode 317 and a drain electrode 319 are on major surface 312 above source region 316 and drain region 318, respectively.” Bonn, 8:33-35, Fig. 7.

Bonn’s source and drain electrodes are thus electrically connected to major surface 312, which is the top surface of semiconductor 310. Bonn, 8:33-35, Fig. 7. The electrodes are laterally spaced, as claimed, across major surface 312 of semiconductor 310. Bonn, Fig. 7.

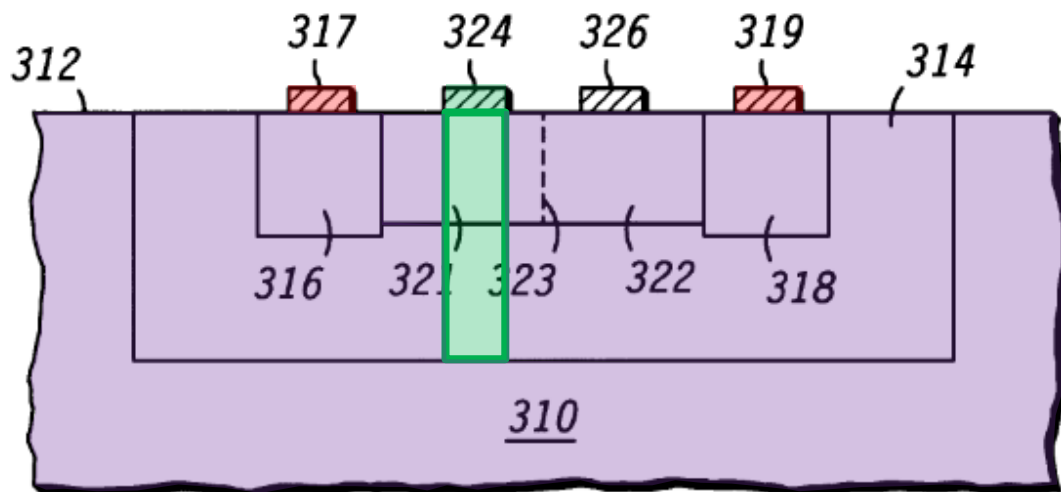


Bonn, Fig. 7 (annotated)

6. [1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

[133] Bonn discloses [1C4], a **first gate** positioned between the **source electrode** and the **drain electrode** and coupled to the **semiconductor element** to form a **first portion of the transistor**.

[134] Bonn states, “[a] **first gate structure 324** is formed on **major surface 312** above first gate region 321.” Bonn, 9:5-8. This **first gate** is thus coupled to **semiconductor 310** forming a **first portion** in first gate region 321 under the gate. It lies between **source electrode 317** and **drain electrode 319**, as shown in Figure 7.



300

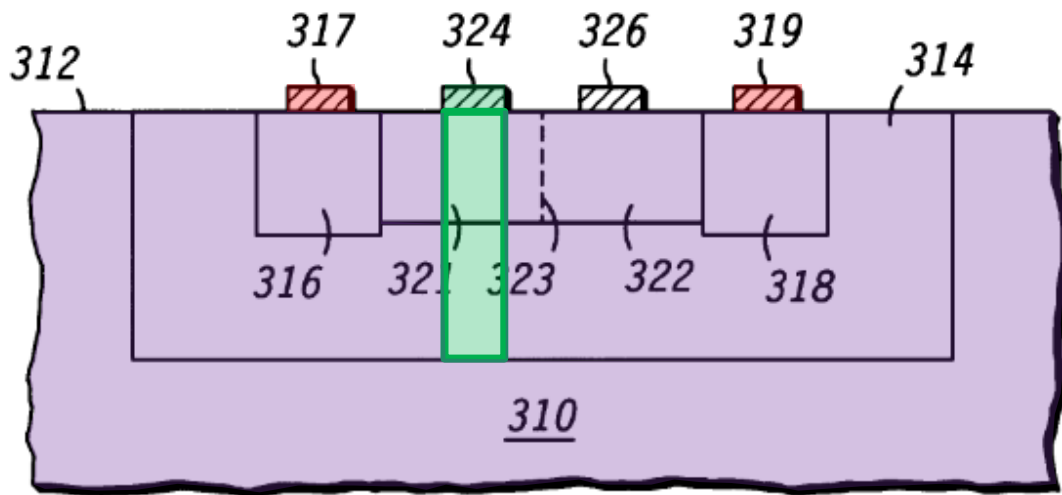
FIG. 7

Bonn, Fig. 7 (annotated)

-
7. [1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;

[135] Bonn renders obvious [1Cd5], a **second gate** positioned adjacent to the **first gate**, and between the **source electrode** and the **drain electrode** to form a **second portion of the transistor**, wherein the **second gate** includes a field plate and is also coupled to the **semiconductor element**.

[136] Bonn states “a **second gate structure 326** is formed on **major surface 312** above second gate region 322.” Bonn, 9:5-8. This **second gate** is positioned adjacent to the **first gate** between **source electrode 317** and **drain electrode 319**, as shown in Figure 7. The **second gate** is coupled to **semiconductor 310** because it is placed on **major surface 312**. Bonn, 9:5-8, Fig. 7.



300

FIG. 7

Bonn, Fig. 7 (annotated)

[137] Although Bonn does not disclose a field plate in the **second gate structure**, a POSITA would have found it obvious to include a field plate, as disclosed by Mizuto, to improve electrical performance characteristics, including improved field relaxation, voltage gain, and breakdown voltage. *See* § XII.A.2 (Motivation to Combine Bonn’s High Frequency Signal Amplification Embodiment with Mizuto’s Field Plate), above. When using this same dual gate cascode device in a high voltage application, a field plate would improve performance, as I explained in the motivation to combine section. When using the semiconductor of Figure 7 for a “high frequency signal amplification” as Bonn teaches (Bonn, 11:26-37), a field plate would have been obvious over Mizuto. *See*

§ XII.A.2 (Motivation to Combine Bonn's High Frequency Signal Amplification Embodiment with Mizuto's Field Plate), above. In that application, the drain voltage VDD would be high to achieve high gain (high signal amplification), and Mizuto's field plate over a dielectric in Bonn's **second gate 326** for electric field relaxation, to improve gain at high frequency, and to improve characteristics to withstand these high voltages. Mizuto, 1:27-30, 1:61-65, 2:13-45.

[138] Accordingly, the modified structure of Bonn's **dual gate FET 300** would have included a **field plate** on the **second gate structure**, over a **dielectric**, as shown below. **Gate 326** with its **field plate** forms a **second portion** of the transistor in the **semiconductor element**, as claimed.



300

FIG. 7

Bonn, Fig. 7 (annotated, modified by Mizuto to include field plate extension on

second gate structure 322 over a **dielectric**)

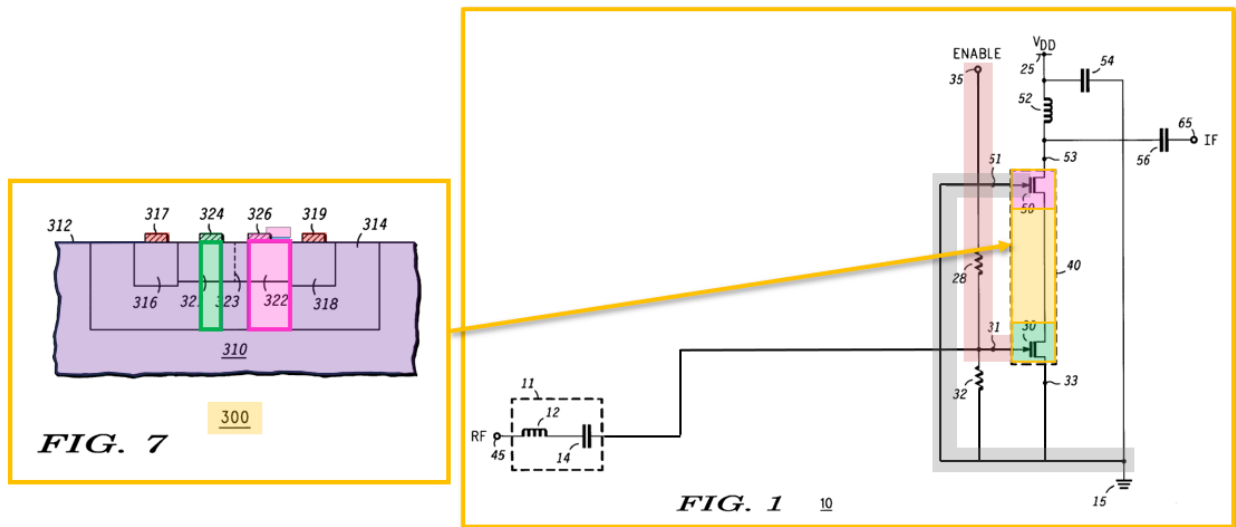
8. [1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and

[139] Bonn discloses [1C6], wherein the **first gate** is connected to the **input voltage signal source** such that conduction of **the first portion of the transistor** is based on a value of the **input voltage signal**.

[140] As explained, **voltage supply conductor 35** is an **input voltage signal**. See § XII.B.2 (Ground 1: [1A]), above. Further, shown below, in the proposed combination, terminal 31 of the **first gate structure 324** connects to a voltage divider formed by resistors 28 and 32, which is between ground (power supply conductor 15) and voltage supply conductor 35. Bonn, 3:23-25, Fig. 1. The voltage at terminal 31 delivered to the **first gate** is accordingly based on voltage supply conductor 35.

[141] Bonn discloses the “first gate region 321 is in an enhancement mode.” Bonn, 8:51-9:4. It is a foundational principle in semiconductor transistors that a two-dimensional electron gas (2DEG) forms at the heterojunction of a channel layer and a barrier layer, and in Bonn’s device, a 2DEG forms between the source and drain near the bottom of doped regions 321 and 323 at their interface with the underlying region of impurity well 314. Bonn, 8:13-9:27 (e.g., discussing “channel

region,” “first gate region 321,” “second gate region 323,” and “impurity well 314.”). By definition, enhancement mode transistors are off (non-conducting) at zero volts applied bias, having no 2DEG below the gate, but when the gate input voltage rises above a threshold value, a 2DEG forms below the gate and the channel begins to conduct. *See, e.g., Ren, Abstract, ¶[0030], Figs. 1-2.* The ’003 patent describes enhancement mode operations consistent with this understanding. ’003 patent, 2:59-3:9. Because Bonn’s first gate region 321 is in enhancement mode, its “conduction . . . is based on a value of the input voltage signal” received at terminal 31, as claimed: it only conducts when the received signal rises above a threshold value (a turn on voltage).



Bonn, Fig. 1 (modified for signal amplification, annotated), Fig. 7 (modified by Mizuto, annotated).

-
9. [1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,

[142] Bonn discloses [1C7], the **second gate** is connected to the **constant voltage source** such that the **second portion** of the transistor conducts until a voltage difference between the **predetermined constant voltage** and a voltage at a **node** in the **semiconductor element** between the **first portion** and the **second portion** of the transistor reaches a predetermined level.

[143] The **node** in the **semiconductor element** between the **first portion** and the **second portion** is a region of the semiconductor element that laterally separates the first portion and the second portion of the transistor such as, for example, the color-coded **light blue** region or a region within the **light blue** region, below. Bonn's depictions of this node are consistent with the node claimed and described in the '003 patent. *See* § VI (OVERVIEW OF THE '003 PATENT), above.



node



300

[144] Bonn discloses “second gate region 322 is in a depletion mode.”

Bonn, 8:51-9:4. By definition, depletion mode gates conduct at and above zero volts applied bias, which is how the '003 patent describes its depletion mode gate. *E.g.*, Ren, Abstract, ¶[0040], Figs. 1-2; '003 patent, 2:64-3:17.

[145] As I will explain, Bonn's **second gate region** “conducts until” a saturation voltage of the depletion mode **second gate** is reached that results in a pinch-off of the conduction layer (upper voltage limit). *See* § VII (Technological Background), above. The upper or lower voltage limit occur at a “predetermined level” of voltage difference between the **ground** and the **node**.

[146] Bonn's **second gate region 322** and **first gate region 321** are formed on the same **semiconductor 310**, so whether or not the **first gate** is ON determines whether the **second gate region 322** conducts. When the **input voltage** is above the turn on voltage threshold, the **first gate** is ON and a **2DEG** extends from **source** to **drain** below both gates, as shown below.

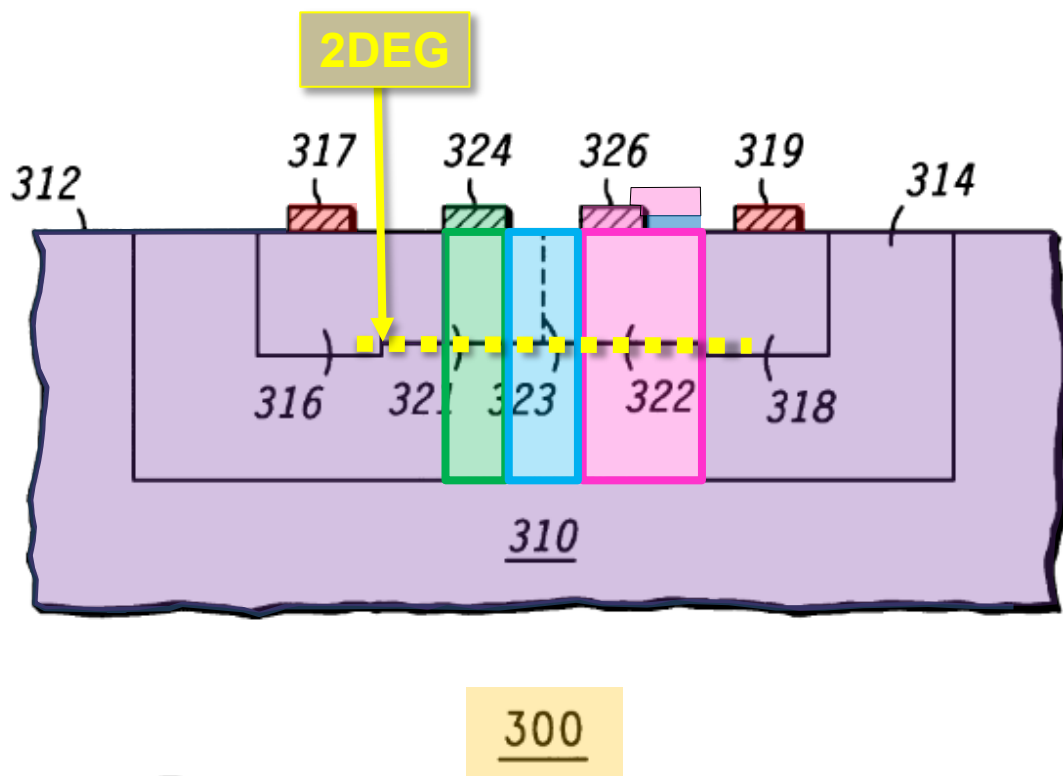
**FIG. 7**

Fig. 7 (annotated, modified by Mizuto).

When the input voltage falls below a threshold, the **first gate** will turn OFF, interrupting the **2DEG** in **first gate region 321**, as shown below.

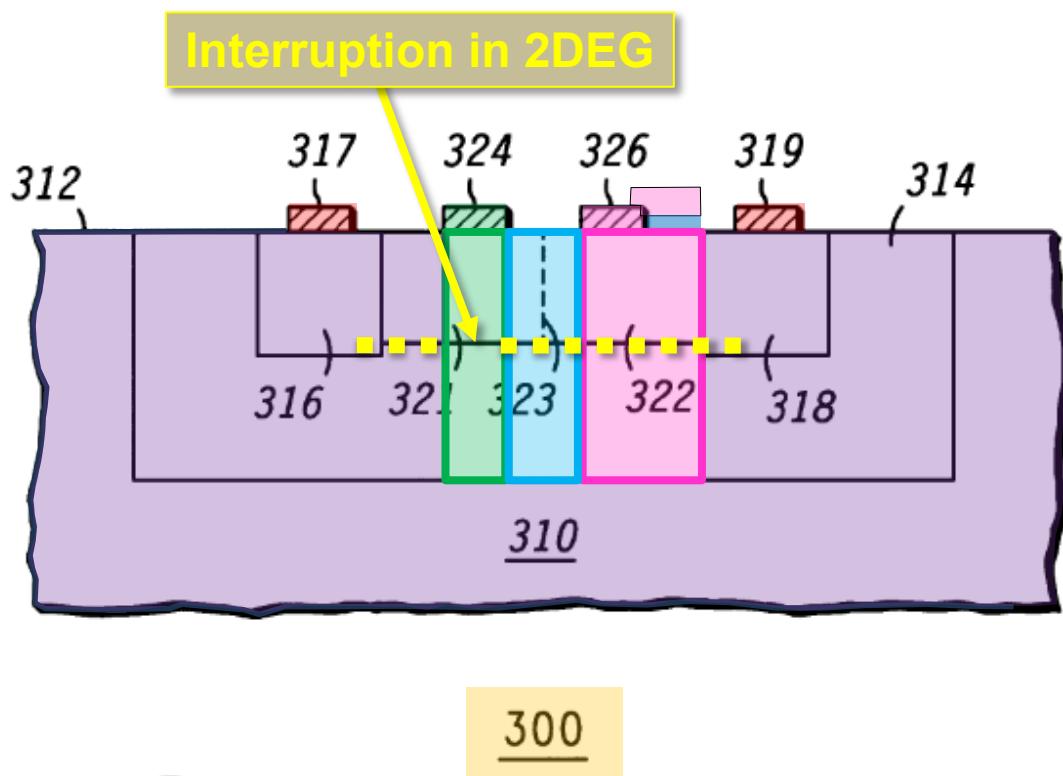
**FIG. 7**

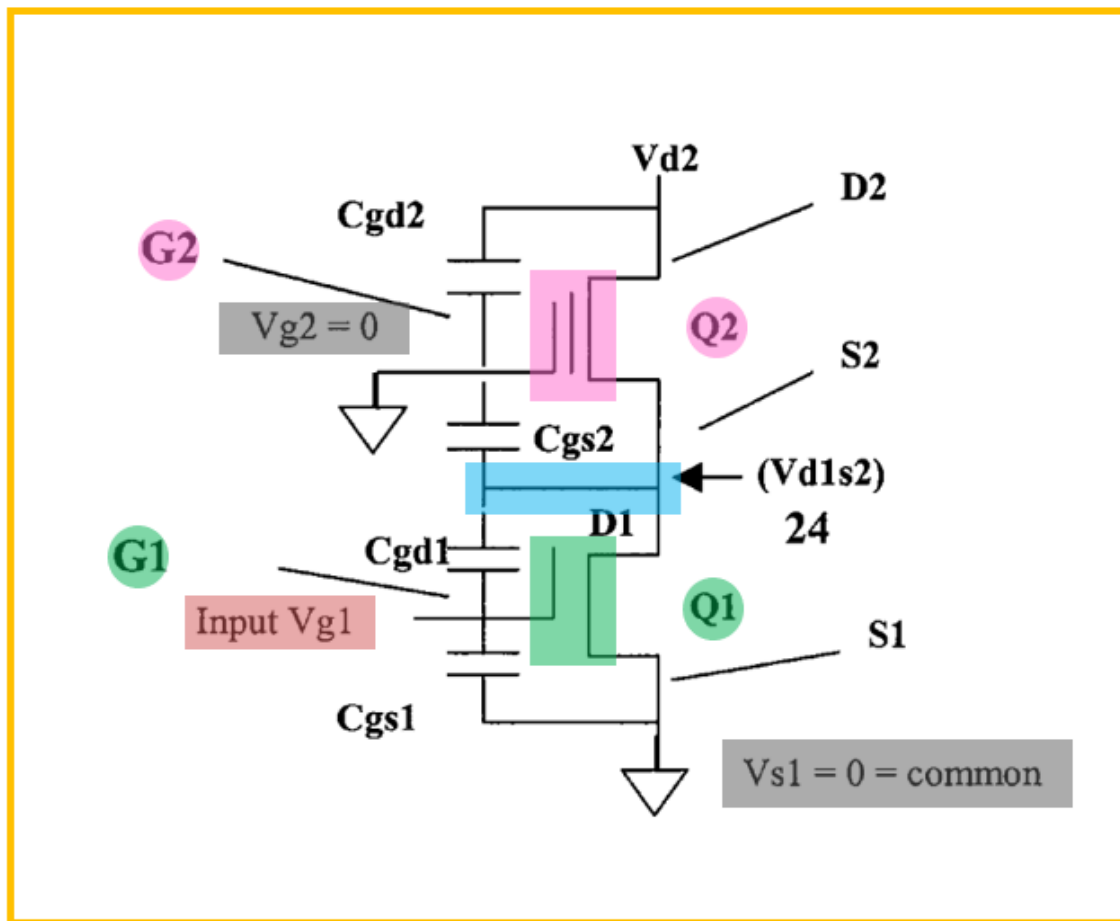
Fig. 7 (modified, annotated).

[147] When the **first gate** turns OFF, Bonn's **second gate 326** conducts until a saturation voltage of the depletion mode (second gate) is reached that results in a pinch-off of the conduction layer (upper voltage limit), which is how a depletion mode gate normally functions. *See* § VII (Technological Background) (e.g., describing pinch-off of cascodes with a first enhancement mode and second depletion mode gate, including simulation), above. The voltage at the **node** rises because it is connected to the **drain** via the 2DEG as shown above. As it rises, the voltage difference across the **second gate** between the **node** and the constant

voltage source becomes negative, until eventually it reaches a saturation voltage (i.e., a threshold voltage at a predetermined level) that results in a pinch-off of the conduction layer below the gate and conductivity ceases.

[148] Thereby, Bonn discloses conducting until a voltage difference between the **predetermined constant voltage** and a voltage at a **node** in the **semiconductor element** between the **first portion** and the **second portion** of the transistor reaches a predetermined level.

[149] Bonn's **second gate region 322** accordingly operates just like the **second portion Q2** of the '003 patent: "[w]hen the **input voltage at Vg1** and provided to the **gate 22** of the bottom portion **Q1** (Vg1) goes low, the bottom portion **Q1** turns OFF and the bottom portion **Q2** stops conducting" because a voltage difference between the **ground** and a voltage at a **node** has been reached. '003 patent, 2:64-3:17.



Ex-1001, Fig. 2 (annotated).

10. [1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and

[150] Bonn discloses [1C8], wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor.

[151] Bonn states “first gate region 321 is in an enhancement mode and second gate region 322 is in a depletion mode.” Bonn, 8:51-9:4.

**FIG. 7**

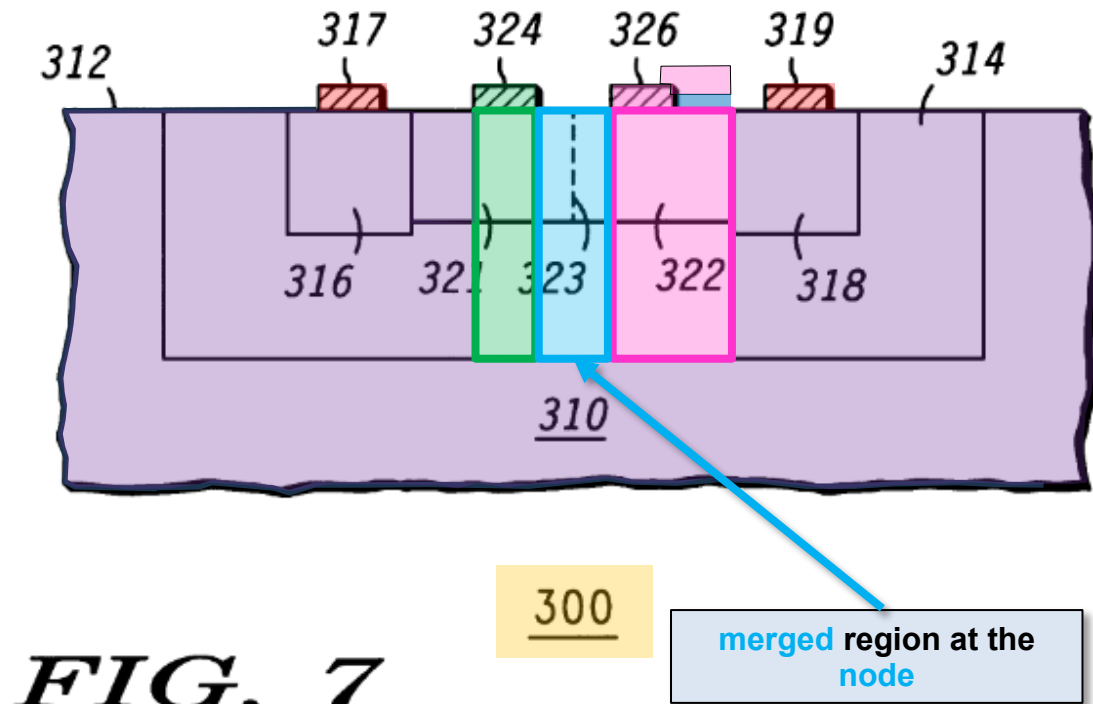
Bonn, Fig. 7 (modified, annotated)

11. [1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

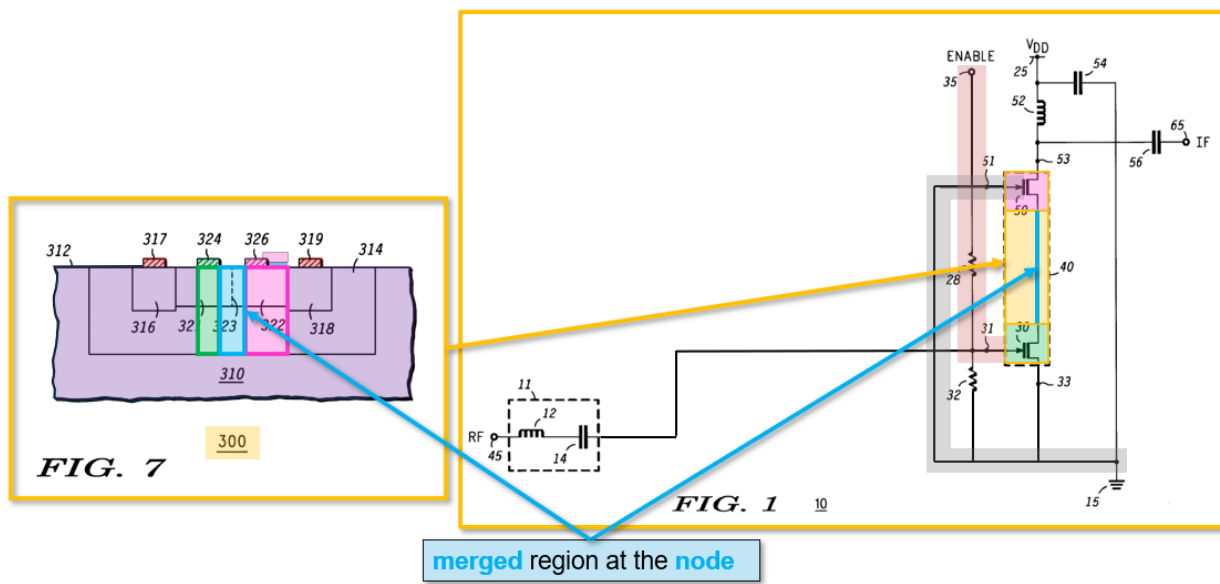
[152] Bonn discloses or at least renders obvious [1C9], wherein a drain region of the **enhancement mode transistor** is **merged** with a source region of the **depletion mode transistor** at the **node** in the **semiconductor element**.

[153] Figure 7 shows a separation between the **first gate 324** and **second gate 322**. Bonn, Fig., 7. That separation region is both a drain region of **first gate 324** (i.e., on the drain side of **first gate 324**) and a source region of **second gate 326** (on the source side of **second gate 326**). That is, the drain region of **first gate**

324 is merged with the source region of second gate 326 at a node. Bonn, 8:51-9:4.

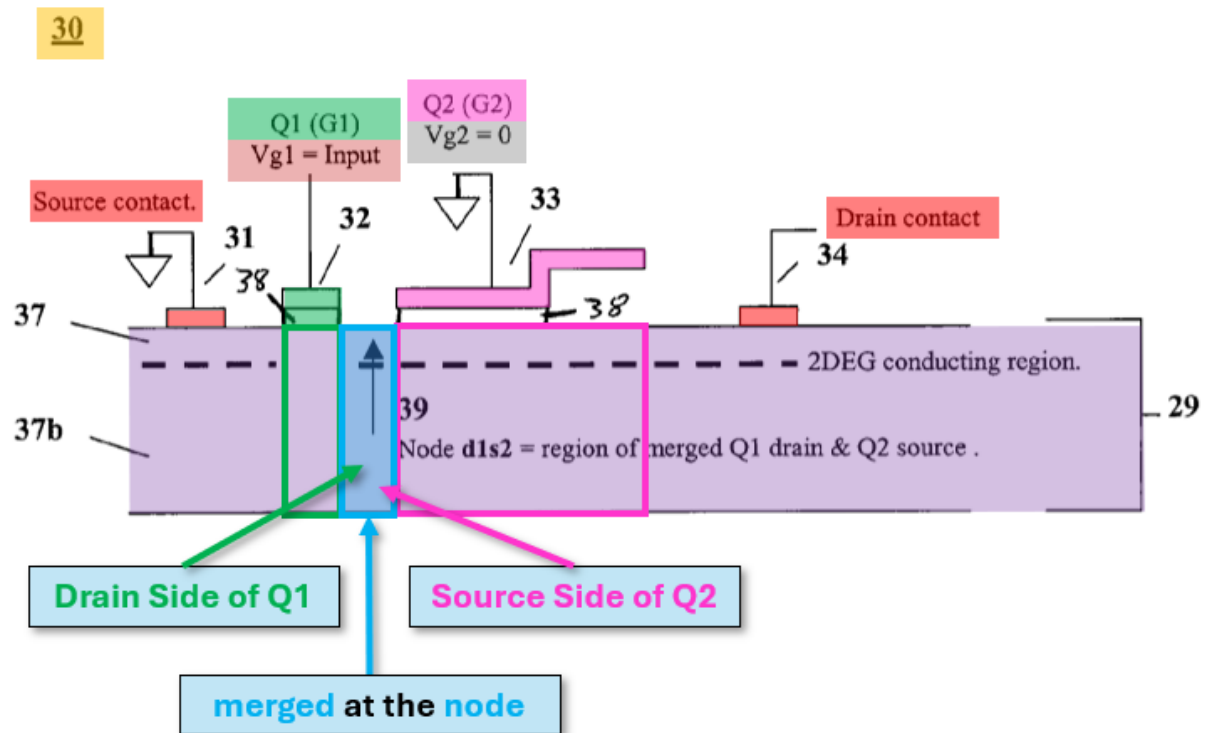


Bonn, Fig. 7 (annotated, modified)

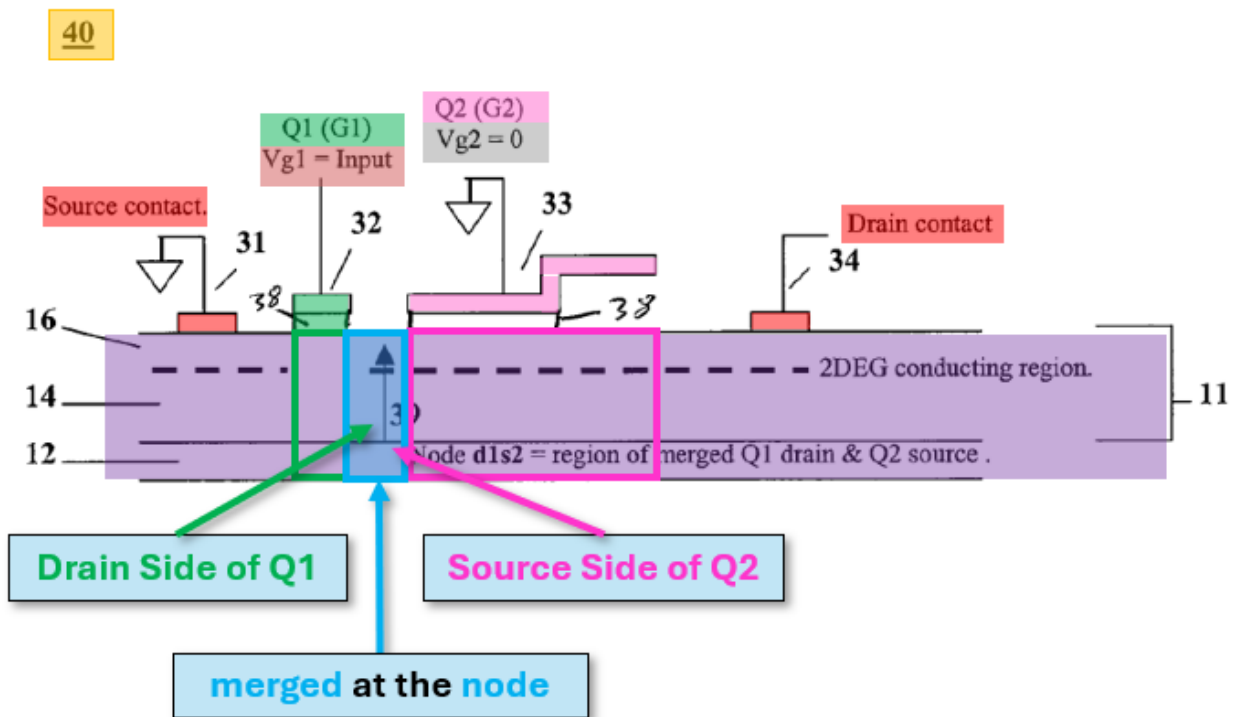


Bonn, Fig. 1 (modified for signal amplification, annotated), Fig. 7 (modified by Mizuto, annotated).

[154] I further illustrate Bonn's merged region in annotated Figure 7, above, in light blue. Bonn's disclosure of a merged region in Figure 7 is consistent with how the '003 patent describes and depicts the "region of merged Q1 drain & Q2 source" of Figs. 3 and 4. '003 patent, Figs. 3-4. The patent states "node 24 of FIG. 2 is represented by the arrow 39 in the area of the merged Q1 drain and Q2 source. That is, on the drain side of the gate 32 (G1) of the first portion Q1 and on the source side of the gate 33 (Q2) of the second portion." '003 patent, 4:4-8.



Ex-1001, Fig. 3 (annotated).



Ex-1001, Fig. 4 (annotated).

XIII. GROUND 2: BONN, REN, AND MISHRA (CLAIMS 1-16)

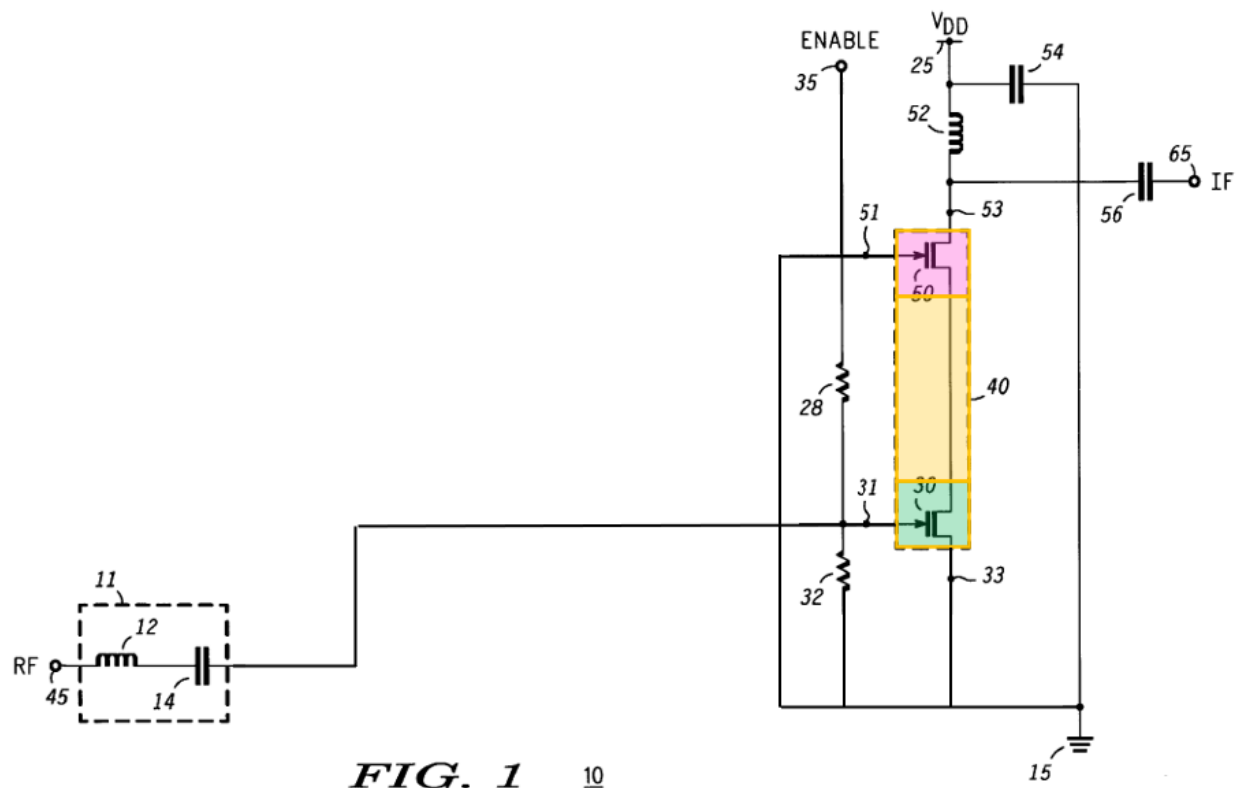
[155] Claims 2-16 of the '003 patent require the semiconductor element below the first and second gates to comprise two stacked III-nitride layers and claims 4-9 and 12-16 specifically require these III-nitride layers are AlGaN over GaN. Although Bonn and Mizuto render obvious claim 1 in my opinion, as I explain above for Ground 1, Bonn does not expressly disclose a device comprised of III-nitride semiconductor material; however, in my opinion, it would have been obvious to a POSITA to make Bonn's device out of GaN based semiconductor materials (since GaN technology largely developed between the time frame of

Bonn and of Ren) as Ren discloses, to achieve the benefits of GaN-based transistors. Further, when making Bonn's device with GaN materials, it would have been obvious to use field plate extension on Bonn's depletion mode gate, as Mishra discloses for GaN-based devices. Accordingly, Bonn in view of Ren and Mishra renders obvious claims 1-16 (Ground 2).

A. Motivation to Combine Bonn, Ren, and Mishra

1. Motivation to Modify Bonn for High Frequency Signal Amplification

[156] As I explained above, based on Bonn's express disclosures that its dual gate FETs "can be tailored to provide superior performance over the prior art dual gate FET structures in ... high frequency signal amplification" applications (Bonn, 11:26-37), Bonn's emphasis that its LO and RF circuitry are isolated (Bonn, 1:20-23, 3:19-21), and Bonn's goal of designing for "minimum chip area" (1:44-45, 5:42-43, 11:26-37), a POSITA would have been motivated to implement Bonn's dual gate FET 300 of Figure 7 in a modified circuit of Figure 1, below, with predictable success. *See* § XII.A.1 (Motivation to Modify Bonn for High Frequency Signal Amplification).



Bonn, Figure. 1 (modified for high frequency signal amplification, annotated).

2. Motivation to Combine Bonn's High Frequency Signal Amplification Embodiment with Ren

[157] In my opinion, it would have been obvious to a POSITA to make Bonn's device out of GaN based semiconductor materials, as Ren discloses, to achieve the benefits of GaN-based transistors, whose technology had improved during as of the time of the '003 patent.

[158] When Bonn was filed in 1996, GaN devices were in early development and uncommon. Bonn discloses forming its transistors from the more

commonly used material gallium arsenide and other “insulated gate FET (IFFET) structures” for its transistors. Bonn, 11:12-21. Bonn does not discuss GaN devices.

[159] But as of the earliest claimed priority date of the '003 patent, March 20, 2006, a POSITA would have been motivated to make Bonn's cascode using GaN materials as Ren discloses. The benefits of GaN devices were well known at the time, and improvements to GaN manufacturing techniques made these devices more common than they were previously. *E.g.*, Mishra, ¶[0007]. Ren describes the shortcomings of GaAs structures in semiconductor devices and how semiconductor devices are improved when using GaN instead of GaAs. Ren explains that GaN devices have a higher saturation velocity than other types of semiconductors, including GaAs devices. Ren, ¶[0005]. Ren notes that GaN devices' improved “physical characteristics [] are suitable for use in high-frequency, high-temperature, and high-power semiconductor devices.” Ren, ¶[0005].

[160] Further, Ren discloses GaN enhancement mode and depletion mode gates with an insulating “gate dielectric” layer between the gate metal contact and underlying AlGaN barrier layer. Ren, ¶¶[0012]-[0018], [0026], [0030], [0036], [0039], [0041], Figs. 1-2. Ren thus discloses the “insulated gate FET” structure that Bonn describes as a suitable option for its devices. Bonn, 11:12-22.

[161] A POSITA would have been familiar with using such insulating dielectrics to make GaN HEMTs, including in enhancement mode devices, as Ren

discloses. *E.g.*, Beach (Ex-1020), ¶¶[0033], [0047]-[0049], claim 5, Figs. 4-5. A POSITA would have known that gate insulating layers like those disclosed in Ren also reduce gate leakage. Beach, ¶¶[0005]-[0006]. Accordingly, a POSITA would have been motivated to use Ren's approach to reduce gate leakage and improve the switching characteristics of the device.

[162] Ren's solution includes an AlGaN over GaN epitaxial structure, where enhancement mode or depletion mode is enabled by varying the thickness of the AlGaN layer. Ren, ¶¶[0014], [0029], [0031]. A thinner layer leads to an enhancement mode device, while a thicker layer leads to a depletion mode device. Ren, ¶¶[0014], [0033]; *see* § X.C (Overview of Ren (Ex-1007, U.S. 2004/0041169)), above.

[163] A POSITA would have been motivated to combine Bonn and Ren to achieve the benefits of using GaN materials over GaAs materials, which were widely recognized at the time. Ren, ¶[0005]; Mishra, ¶[0020]. Ueno, for example, explains GaN is a suitable substitute for GaAs, stating "GaN-based compound semiconductor materials have been intensively studied as radiofrequency (RF) high-power devices," and GaN materials are "capable of forming heterojunctions in the same manner as conventionally used arsenic-based semiconductor materials containing gallium arsenide (GaAs) as a main component." Ueno (Ex-1016), ¶[0020]. Mishra further explains GaN leads to improvements over GaAs devices.

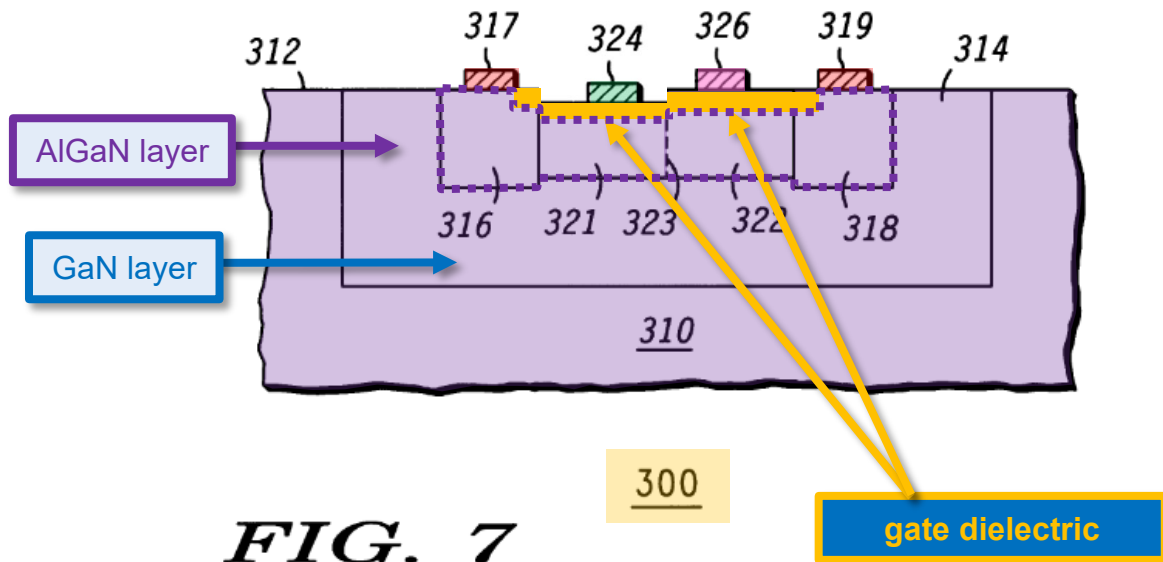
The “large bandgaps,” “high peak and saturation electron velocity values,” high 2DEG sheet densities, and “relatively high electron mobility” of GaN devices allows “AlGa_N/Ga_N HEMTs to provide very high voltage and high-power operation at RF, microwave and millimeter wave frequencies.” Mishra, ¶[0007] (citing papers).

[164] A POSITA would have found it obvious to make Bonn’s device using Ren’s Ga_N-based enhancement mode and depletion mode gates with an insulating “gate dielectric” layer between the gate metal contact and underlying AlGa_N barrier layer. Bonn expressly discloses substituting its GaAs FETs with such “insulated gate FET” structures, in which “the gate is separated from the major surface of the body of the semiconductor material by a gate dielectric layer.” Bonn, 11:12-21. A POSITA would have been motivated to make the combination in view of these teachings and Ren’s disclosure that Ga_N transistors are more suitable for high frequency, high temperature, and/or high-power applications. Ren, ¶¶[0012]-[0018], [0030], Figs. 1-2.

[165] The substitution of Bonn’s GaAs semiconductor materials in structure 300 of Figure 7 with Ren’s Ga_N materials would have predictably led to a cascode transistor with an enhancement mode Ga_N and a depletion mode Ga_N gate. Bonn’s dual gate FETs have “independently adjustable gate widths and channel properties,” including different “dopant concentration, channel depth, etc.” Bonn, 5:57-67, 8:51-

9:4, 9:13-27, 11:22-37. Bonn teaches its dual gate FETs like the one in Figure 7 “can be tailored to provide superior performance over the prior art dual gate FET structures in ... high frequency signal amplification” applications. Bonn, 11:26-37. Bonn discloses “[f]or epitaxial growth, different channel depths in different gate regions are achieved using selective etching.” Bonn, 10:50-52. This complements Ren’s teachings to adjust whether the gate is enhancement or depletion mode by varying the AlGa_N layer thickness. Ren, ¶¶[0014], [0029], [0031]. A POSITA would have selectively etched Ren’s AlGa_N layer and added Ren’s **dielectric** in a modified Bonn device to predictably create a first gate region 321 in enhancement mode (thinner AlGa_N layer) and second gate region 322 in depletion mode (thicker AlGa_N layer).

[166] Below, I include a schematic representation of the Bonn-Ren combination, in which the **AlGa_N layer** is thinner under enhancement mode **gate 324** and thicker under the depletion mode **gate 326**.

**FIG. 7**

Bonn, Fig. 7 (modified by Ren, annotated).

3. Bonn, Ren, and Mishra

[167] In my opinion, a person of ordinary skill would have found it obvious to further modify the Bonn cascode transistor used as a high-frequency signal amplifier as modified by Ren with Mishra's teaching to use field plates to improve performance characteristics.

[168] In my opinion, a POSITA would have found it obvious over Mishra to include a field plate in the Bonn-Ren **second gate 326**. Mishra's field plate extensions "reduce the peak electric field in the device that can result in increased breakdown voltage and reduced trapping" AlGaN/GaN semiconductor materials. Mishra, ¶[0029]. In some embodiments, the field plate is connected to source, just like the Bonn cascode. Mishra, ¶[0029]; Bonn, Figs. 1, 7. Mishra teaches

implementing its field plates in “[m]any different wide bandgap transistor structures [that] can be used in the cascode amplifier arrangement.” Mishra, ¶[0028], Fig. 10. The combination of Bonn and Ren is an AlGa_N/Ga_N cascode amplifier. *See* §§ XIII.A.1-XIII.A.2 (Motivation to Modify Bonn for High Frequency Signal Amplification)-(Motivation to Combine Bonn’s High Frequency Signal Amplification Embodiment with Ren), above.

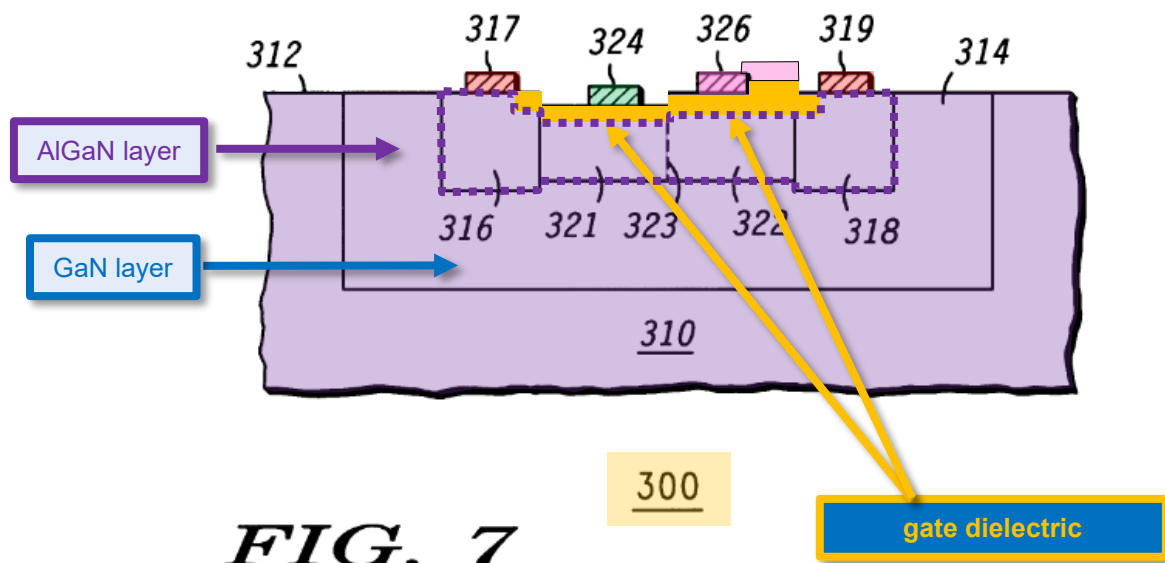
[169] In addition, the combination would have been obvious because Bonn seeks to improve performance in high frequency applications (Bonn, 1:8-23, 11:26-37), and Mishra teaches its field plated transistors “achieve efficient high power and high frequency signal amplification” and also result in “higher voltage and higher power operation” (Mishra, ¶¶[0011] [0062]). Mishra repeatedly teaches the high gain and high-power benefits of using field plates on its second stage transistor. Mishra, ¶¶[0012], [0027], [0056]-[0061]. For example, in cascode embodiments, Mishra teaches its “second stage transistor comprises a field plate to enable higher voltage and higher power operation.” Mishra, ¶[0061]. A POSITA would have included Mishra’s field plate extension to realize these benefits.

[170] A POSITA would have predictably included Mishra’s field plate extension on the depletion mode gate due to the many known benefits of a field plate in the AlGa_N/Ga_N device that Mishra teaches. It was well known at the time of the ’003 patent to use gate field plate extensions over a dielectric layer to control

electric field and improve operating characteristics, including reduced peak electric field, increased breakdown voltage, reduced trapping, and reduced leakage, all with minimum impact on increased gate capacitance. Mizuto, 1:50-59, 2:12-45, 8:39-44; Mishra, ¶¶[0029]; Wakejima (Ex-1012), ¶¶[0053], [0064], [0219]-[0225], Figs. 23D-E, 24; Parikh (Ex-1013), ¶¶[0028], [0031]; Miyamoto (Ex-1014), 1:57-2:4, 3:11-26, 11:3-37; Sheppard (Ex-1015), 4:39-46. Further, Mishra discloses field plates were used in dual gate cascodes like Bonn's structure 300 of Figure 7 as modified with Ren's AlGaN/GaN semiconductor materials. Mishra, Abstract, ¶¶[0026]-[0030], [0048]-[0062], Figs. 5, 10.

[171] In addition, Mishra teaches the benefits of a field plate extension above a “spacer layer”/“dielectric layer”/“passivation layer” between the field plate extension and the channel layer. Mishra, ¶¶[0028], [0035]-[0036], [0039], [0043], [0049]-[0050], Figs. 2 (spacer layer 24), 4 (passivation layer 44), 5 (spacer layer 64). A POSITA would have found it obvious to include a Mishra's field plate extension on top of the gate dielectric taught by Bonn and Ren.

[172] In view of Mishra and the background knowledge of a POSITA, a POSITA would have found it obvious to modify Bonn-Ren's **second gate structure 326** by including a **field plate extension** over a **dielectric** to achieve the above known benefits of field plate extensions. The resulting Bonn-Ren-Mishra transistor is shown below.



Bonn, Fig. 7 (modified by Ren and Mishra, annotated).

[173] The combination implements the combined Bonn-Ren-Mishra transistor in the circuit of Bonn's Figure 1.

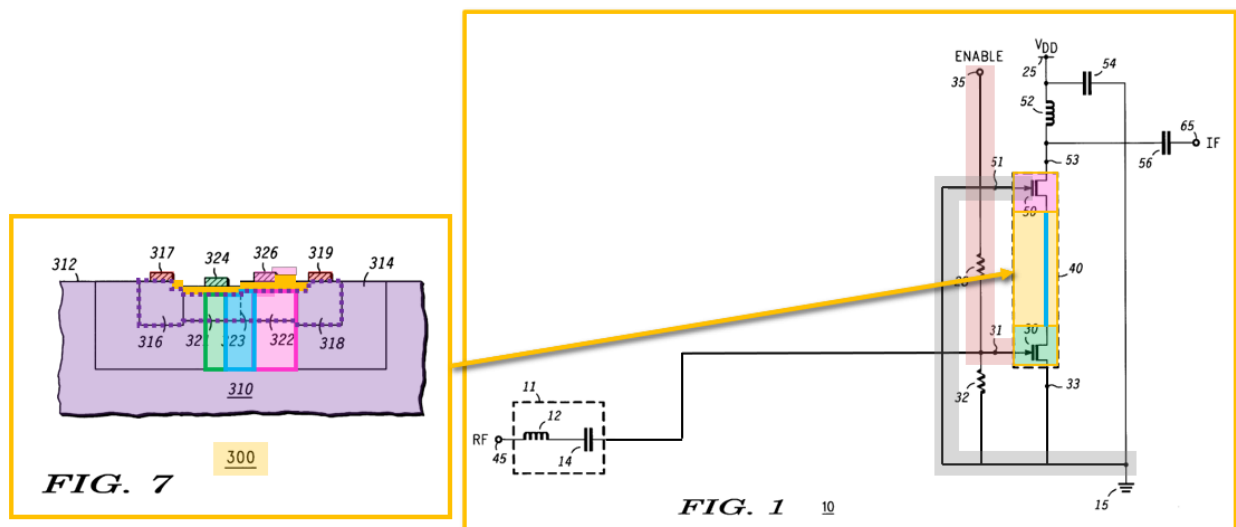


Fig. 1 (modified for signal amplification, annotated), Fig. 7 (modified by Ren and Mishra, annotated)

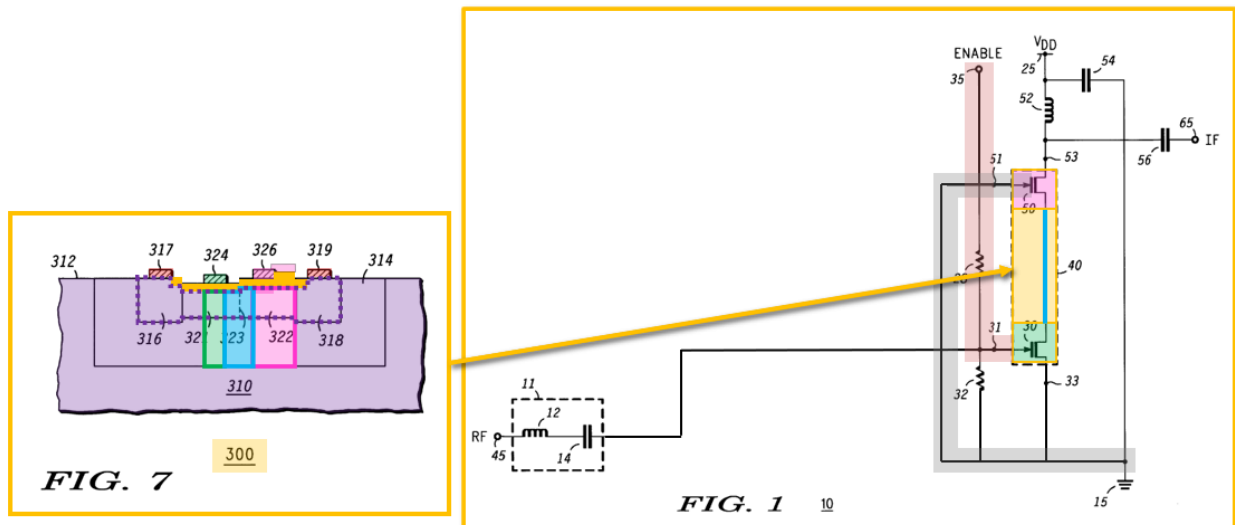
B. Claim 1

[174] Claim 1 is obvious over the combination of Bonn, Ren, and Mishra.

1. [1PRE] A merged cascode transistor circuit comprising:

[175] The combination of Bonn, Ren, and Mishra renders obvious [1PRE].

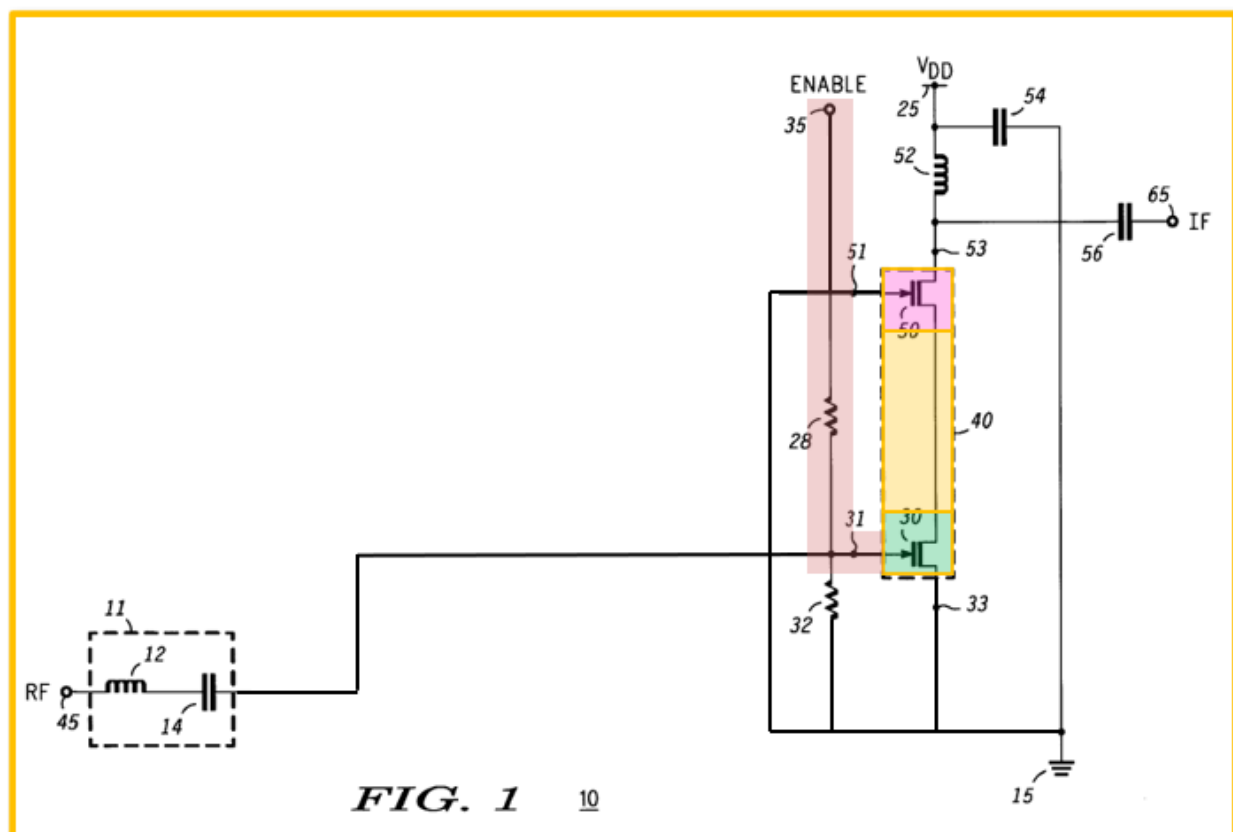
[176] Bonn discloses or at least renders obvious [1PRE], a **merged cascode transistor** circuit. *See* § XII.B.1 (Ground 1: [1PRE]), above. The Bonn-Ren-Mishra combination implements a **merged cascode transistor** circuit using Ren's AlGaN/GaN structures and Mishra's field plate extension. *See* § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above.



Bonn, Fig. 1 (modified for signal amplification, annotated), Fig. 7 (modified by Ren and Mishra, annotated)

2. [1A] an input voltage signal source having an input voltage signal;

[177] Bonn discloses [1A]. As explained, Bonn's **voltage supply conductor 35** is an **input voltage signal source** having an input voltage signal in Bonn's high frequency signal amplification embodiment, as claimed. *See* § XII.B.2 (Ground 1: [1A])



Bonn, Fig. 1 (modified, annotated)

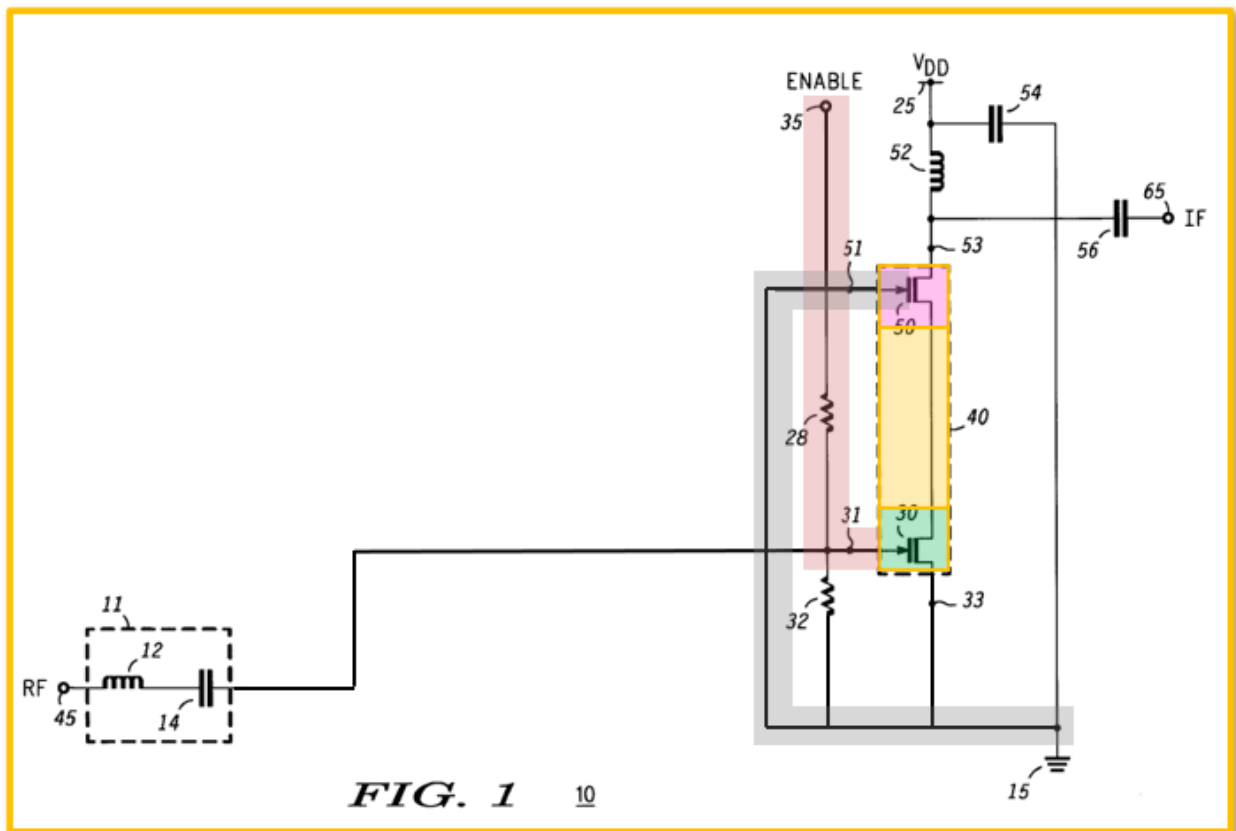
[178] The combination implements the combined Bonn-Ren-Mishra transistor in the modified Bonn Figure 1 circuit. *See* § XIII.A (Motivation to

Combine Bonn, Ren, and Mishra), above. **Voltage supply conductor 35** is an **input voltage signal source** having an input voltage signal in that combination.

3. [1B] a constant voltage source having a predetermined constant voltage;

[179] The combination of Bonn, Ren, and Mishra renders obvious [1B].

[180] In Bonn's high frequency signal amplification embodiment, **power supply conductor 15** is a **constant voltage** source having a predetermined constant voltage (i.e., 0V), as claimed. *See* § XII.B.3 (Ground 1: [1B]), above.



Bonn, Fig. 1 (modified, annotated)

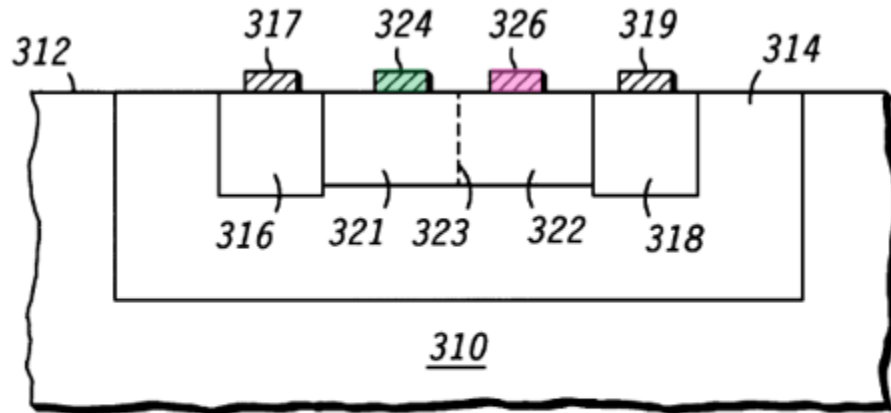
[181] The combination implements the combined Bonn-Ren-Mishra transistor in the modified Bonn Figure 1 circuit. *See* § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above.

4. [1C] a merged cascode transistor comprising:

[182] The combination of Bonn, Ren, and Mishra renders obvious [1C].

[183] Bonn discloses [1C], a **merged cascode transistor** in high frequency signal amplification embodiments. *See* § XII.B.4 (Ground 1: [1C]), above.

[184] Figure 7, below, depicts an example **dual gate FET 300** in **mixer 40** of Figure 1. Bonn, 8:13-9:28. Although Bonn does not expressly use the term “**merged cascode**,” this arrangement is the same as the “**merged cascode**” claimed and described in the '003 patent because it implements its cascode on a single semiconductor with two gates in between a source and drain. *See* §§ VI (OVERVIEW OF THE '003 PATENT), XII.B.4 (Ground 1: [1C]), above.



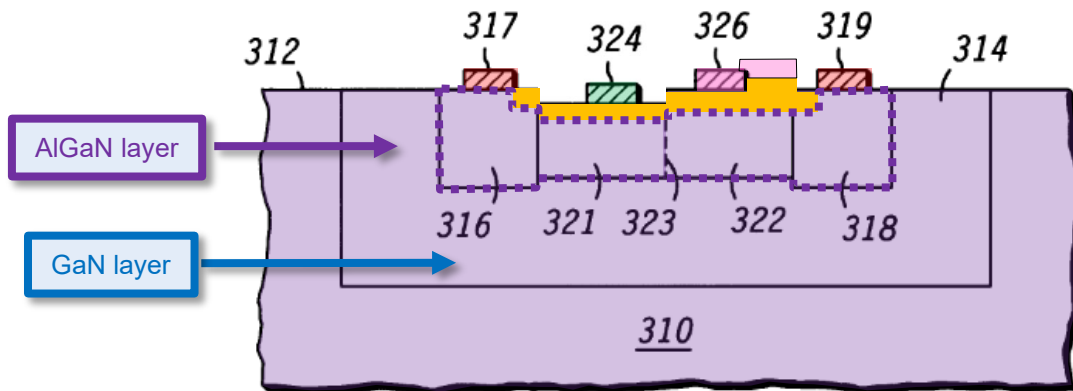
300

FIG. 7

Bonn, Fig. 7 (annotated).

[185] The Bonn-Ren-Mishra combination implements Bonn's same **merged cascode** using Ren's **AlGaN/GaN** structures and Mishra's **field plate extension**.

See § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above.



300

FIG. 7

Bonn, Fig. 7 (modified by Ren and Mishra, annotated)

5. [1C1] a semiconductor element;
[1C2] a source electrode electrically connected to a top surface of the semiconductor element; and
[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;

[186] The combination of Bonn, Ren, and Mishra renders obvious [1C1]-[1C3].

[187] Bonn discloses [1C1]-[1C3], which are entirely conventional. Fig. 7. *See* § XII.B.5 (Ground 1: [1C1]-[1C3]), above). The Bonn-Ren-Mishra combination discloses the same features using Ren's AlGa_N/Ga_N structures and Mishra's field plate extension. *See* § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above.

[188] The combination teaches [1C1] because it discloses a semiconductor element. The combination includes an AlGa_N layer below the gates, which is the claimed **semiconductor element** because it comprises a semiconductor material.

[189] The combination teaches [1C2] and [1C3] because it teaches source and drain electrodes electrically connected to a top surface of the semiconductor element and spaced laterally across the surface of the semiconductor element. The combination's AlGa_N layer semiconductor element is positioned below the “**source electrode 317**” and a “**drain electrode 319**.” Bonn, 8:33-35, Fig. 7; *see*

§ XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above. The **source** and **drain electrodes** are electrically connected to the **AlGaN** layer, and **electrodes** are laterally spaced, as claimed. Bonn, 8:33-35, Fig. 7; see § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above.

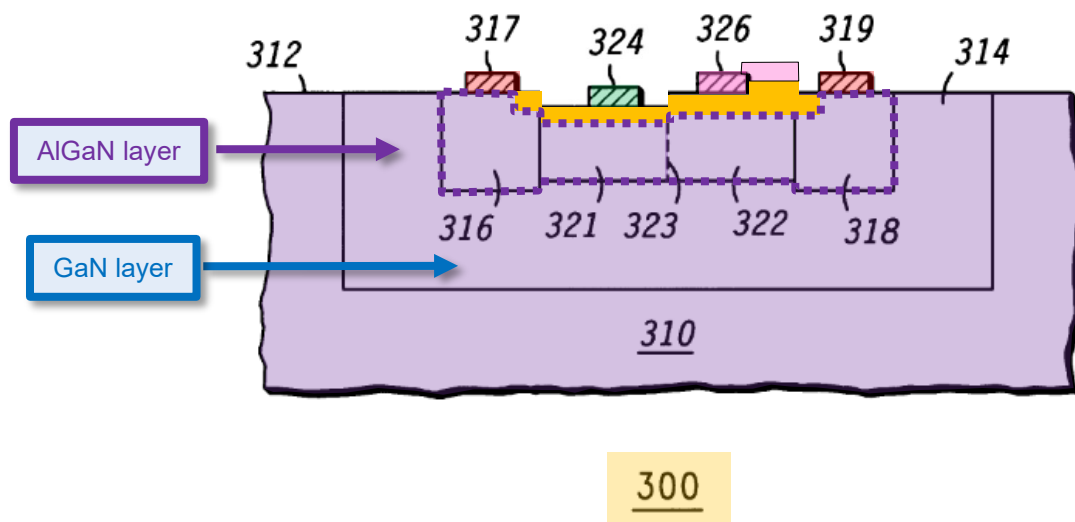


FIG. 7

Bonn, Fig. 7 (modified by Ren and Mishra, annotated)

6. [1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

[190] The combination of Bonn, Ren, and Mishra renders obvious [1C4].

[191] Bonn discloses [1C4], a **first gate** positioned between the **source electrode** and the **drain electrode** and coupled to the **semiconductor element** to form a **first portion of the transistor**. See § XII.B.6 (Ground 1: [1C4]), above.

[192] The Bonn-Ren-Mishra combination discloses the same features using Ren's AlGa_N/Ga_N structures and Mishra's **field plate extension**. See § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above. The **first gate** is coupled to **semiconductor 310** forming a **first portion** under the gate, and the **first gate** lies between **source electrode 317** and **drain electrode 319**, as shown in modified Figure 7.

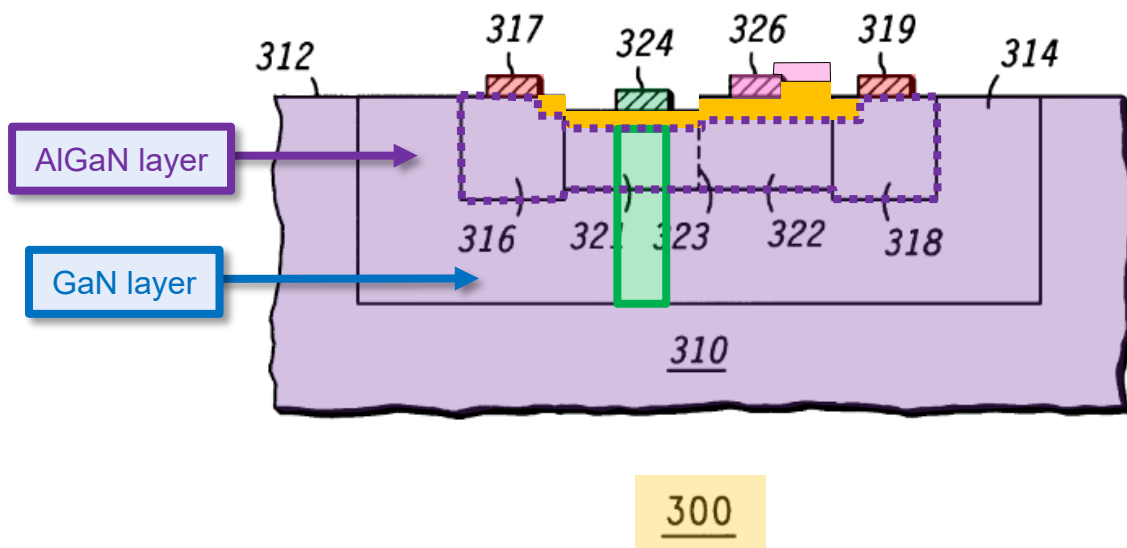


FIG. 7

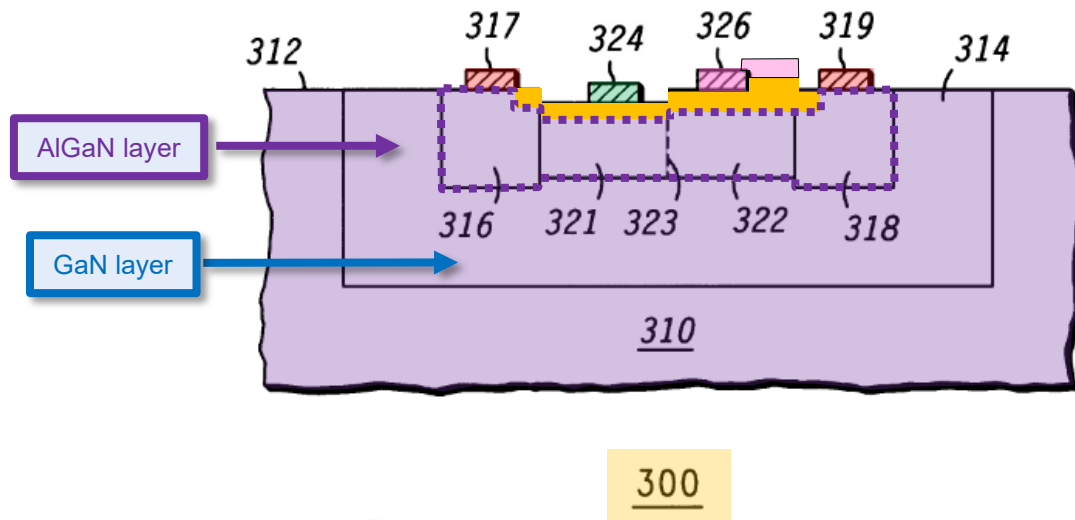
Bonn, Fig. 7 (modified by Ren and Mishra, annotated)

7. [1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;

[193] The combination of Bonn, Ren, and Mishra renders obvious [1C5].

[194] Bonn discloses a **second gate** positioned adjacent to the **first gate**, and between the **source electrode** and the **drain electrode** to form a **second portion of the transistor** ... and is also coupled to the **semiconductor element**.
See § XII.B.7 (Ground 1: [1C5]), above.

[195] The Bonn-Ren-Mishra combination discloses the same features using Ren's AlGaIn/GaN structures and discloses wherein the **second gate** includes a field plate. *See* § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above. For example, it would have been obvious to use a field plate on the depletion mode gate because Bonn seeks to improve performance in high frequency applications (Bonn, 1:8-23, 11:26-37), and Mishra teaches its field plated transistors "achieve efficient high power and high frequency signal amplification" and also result in "higher voltage and higher power operation" (Mishra, ¶¶[0011] [0062]). Mishra repeatedly teaches the high gain and high power benefits of using a field plate on its second stage transistor. Mishra, ¶¶[0012], [0027], [0056]-[0061]. For example, in cascode embodiments, Mishra teaches its "second stage transistor comprises a field plate to enable higher voltage and higher power operation." Mishra, ¶[0061]. A POSITA would have included Mishra's field plate extension to realize these benefits.



Bonn, Fig. 7 (modified by Ren and Mishra, annotated).

8. [1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and

[196] The combination of Bonn, Ren, and Mishra renders obvious [1C6].

[197] Bonn discloses [1C6], wherein the **first gate** is connected to the **input voltage signal source** such that conduction of **the first portion of the transistor** is based on a value of the **input voltage signal**. See § XII.B.8 (Ground 1: [1C6]), above.

[198] The Bonn-Ren-Mishra combination discloses the same features using Ren's AlGaN/GaN structures, as shown below. See § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above.

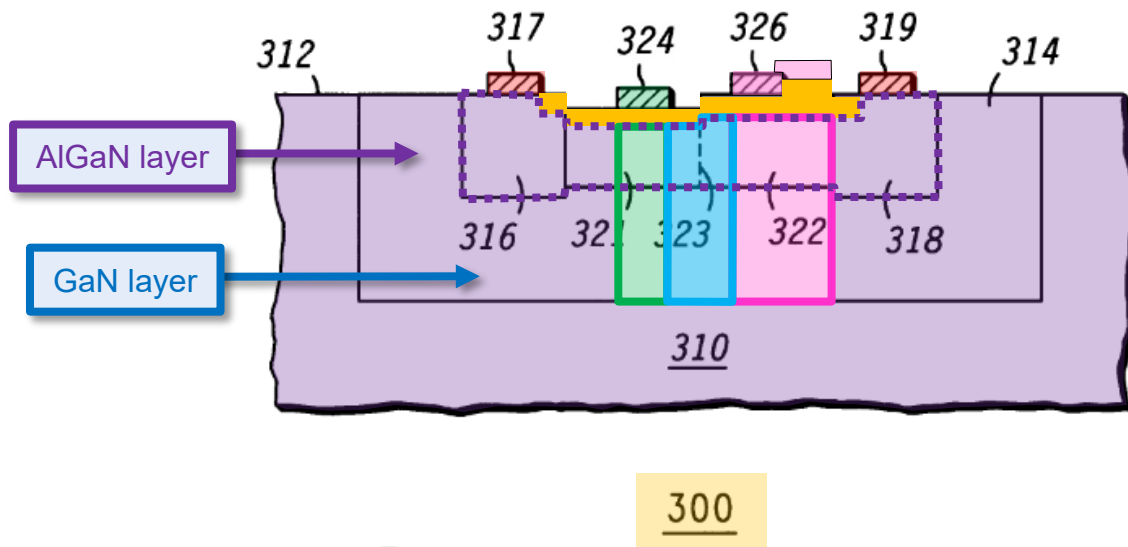


FIG. 7

Bonn, Fig. 7 (modified by Ren and Mishra, annotated).

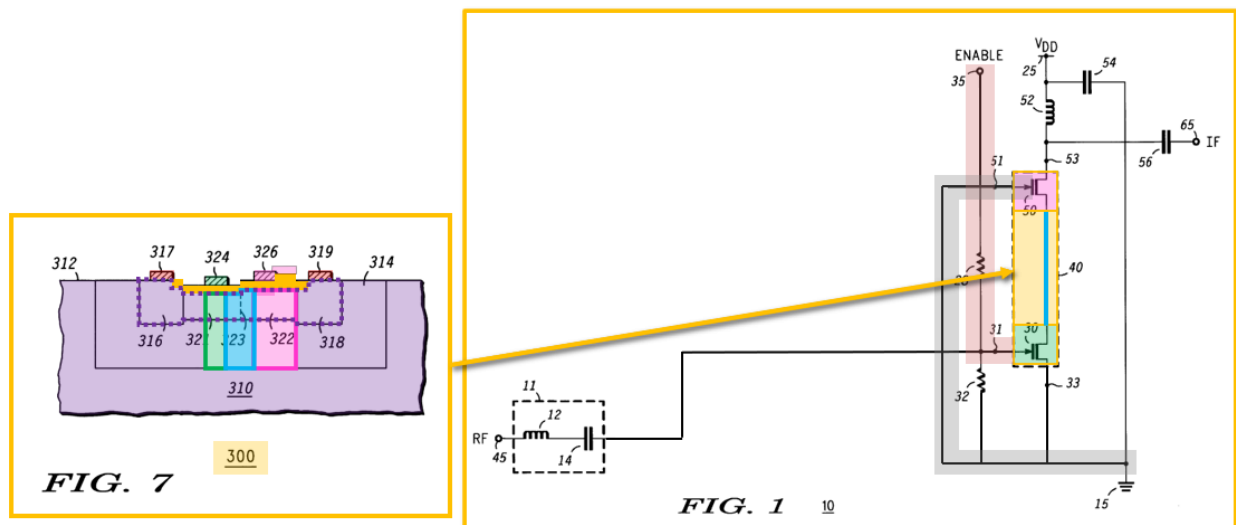


Fig. 1 (modified for signal amplification, annotated), Fig. 7 (modified by Ren and Mishra, annotated)

9. [1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor

element between the first portion and the second portion of the transistor reaches a predetermined level,

[199] The combination of Bonn, Ren, and Mishra renders obvious [1C7].

[200] Bonn discloses [1C7], the **second gate** is connected to the **constant voltage source** such that the **second portion** of the transistor conducts until a voltage difference between the **predetermined constant voltage** and a voltage at a **node** in the **semiconductor element** between the **first portion** and the **second portion** of the transistor reaches a predetermined level. *See* § XII.B.9 (Ground 1: [1C7]), above.

[201] The Bonn-Ren-Mishra combination discloses the same features using Ren's AlGa_N/Ga_N structures. *See* § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above. For the same reasons discussed in Ground 1, [1C7], the **second gate** “conducts until” either the turn on voltage of the enhancement mode first gate is reached (lower voltage limit) or a saturation voltage of the depletion mode second gate is reached that results in a pinch-off of the conduction layer (upper voltage limit) at which conductivity ceases. *See* §§ VII (Technological Background) (e.g., describing pinch-off of cascodes with a first enhancement mode and second depletion mode gate, including simulation), XII.B.9 (Ground 1: [1C7]), above. The upper or lower voltage limit occur at a “predetermined level” of voltage difference between the ground and the **node**.

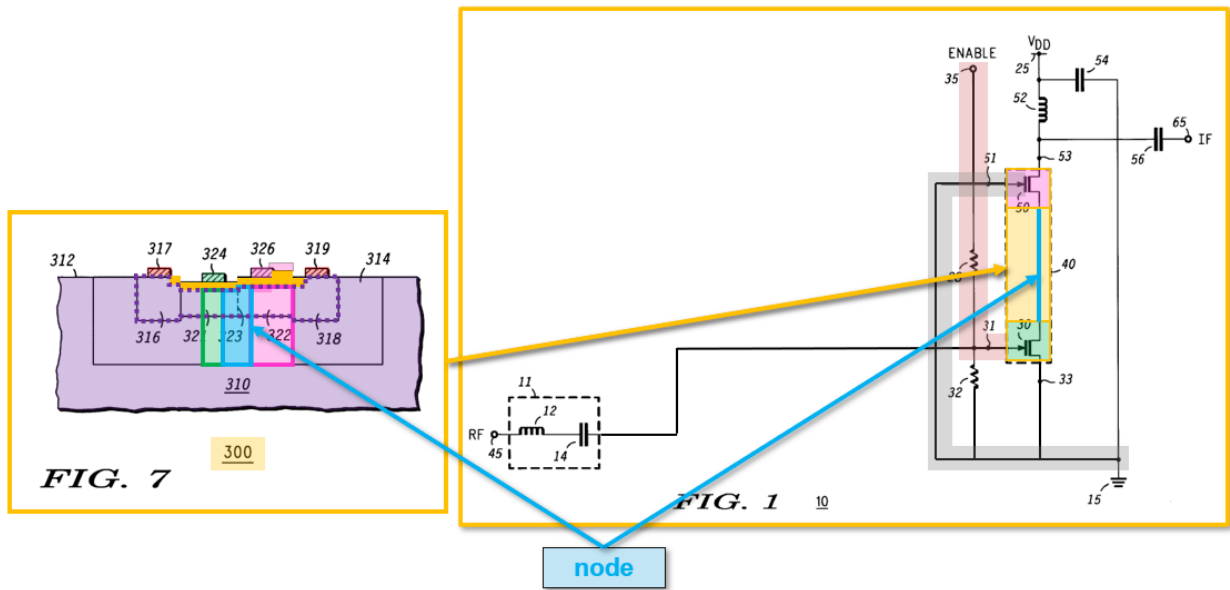
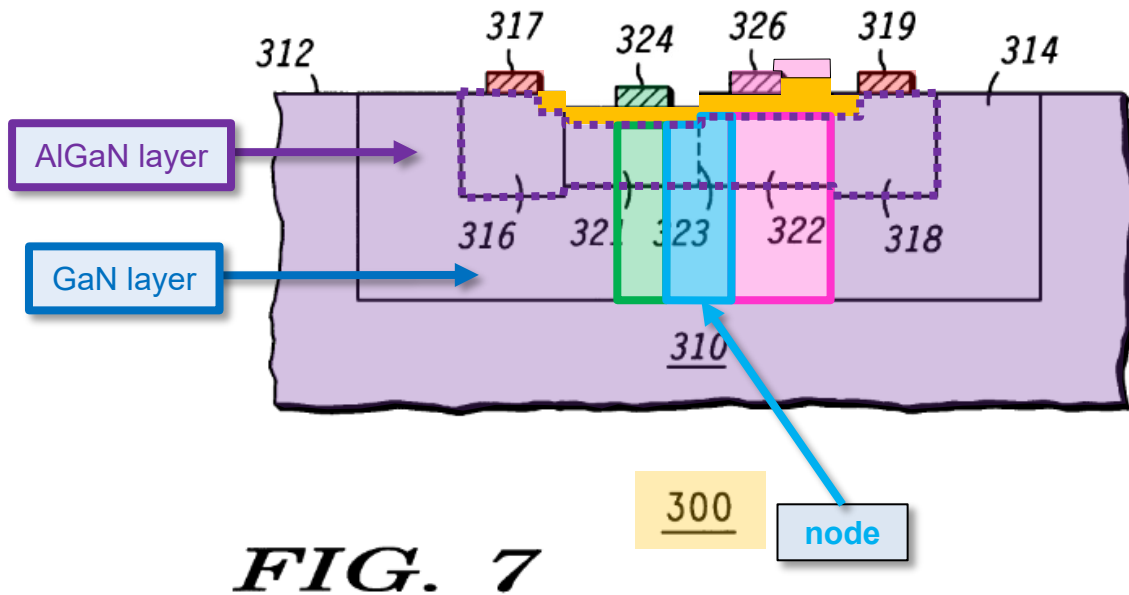


Fig. 1 (modified for signal amplification, annotated), Fig. 7 (modified by Ren and Mishra, annotated)



Bonn, Fig. 7 (modified by Ren and Mishra, annotated)

10. [1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and

[202] The combination of Bonn, Ren, and Mishra renders obvious [1C8].

[203] Bonn discloses [1C8], wherein the **first portion** of the transistor is an enhancement mode transistor and the **second portion** of the transistor is a depletion mode transistor. *See* § XII.B.10 (Ground 1: [1C8]), above.

[204] The Bonn-Ren-Mishra combination discloses the same features using Ren's AlGaIn/GaN structures. *See* § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above.

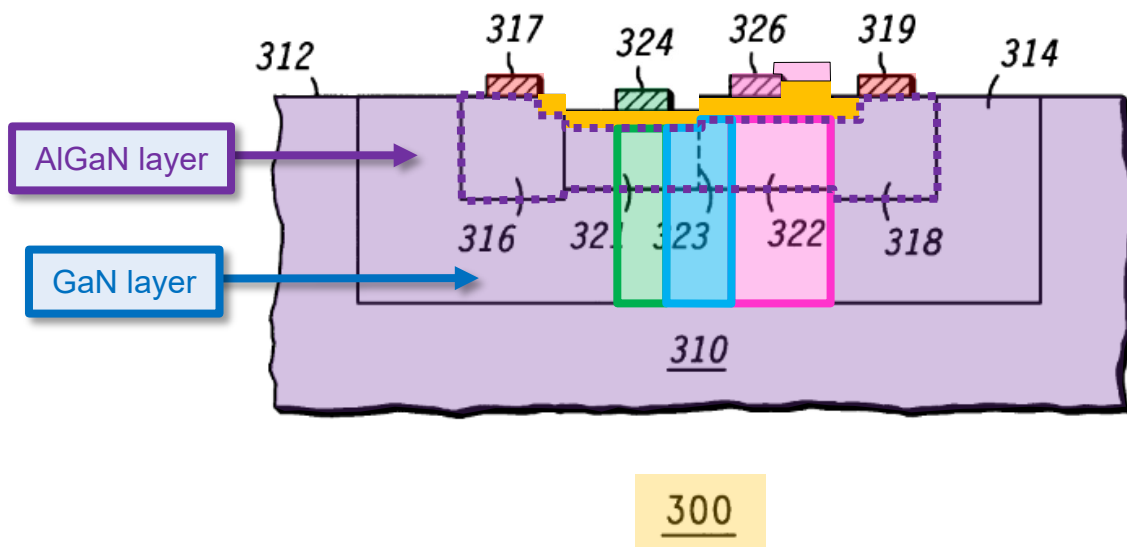


FIG. 7

Bonn, Fig. 7 (modified by Ren and Mishra, annotated)

11. [1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

[205] The combination of Bonn, Ren, and Mishra renders obvious [1C9].

[206] Bonn discloses or at least renders obvious [1C9], wherein a drain region of the **enhancement mode transistor** is merged with a source region of the **depletion mode transistor** at the **node** in the **semiconductor element**. See § XII.B.11 (Ground 1: [1C9]), above.

[207] The Bonn-Ren-Mishra combination discloses the same features using Ren's AlGaN/GaN structures. See § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above.

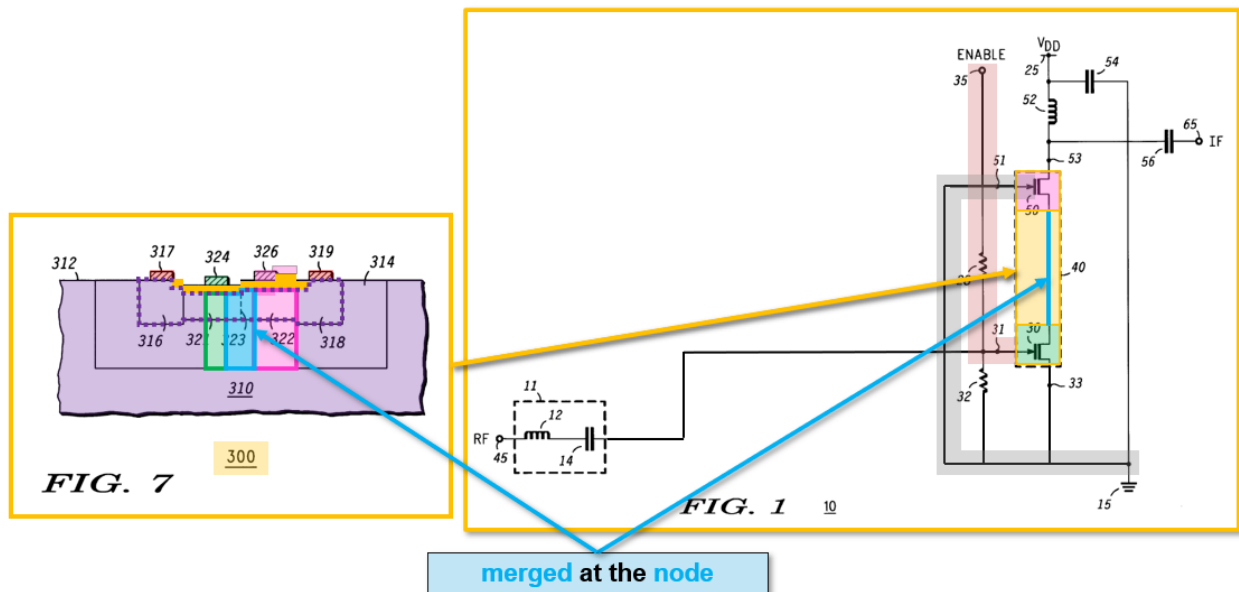


Fig. 1 (modified for signal amplification, annotated), Fig. 7 (modified by Ren and Mishra, annotated)

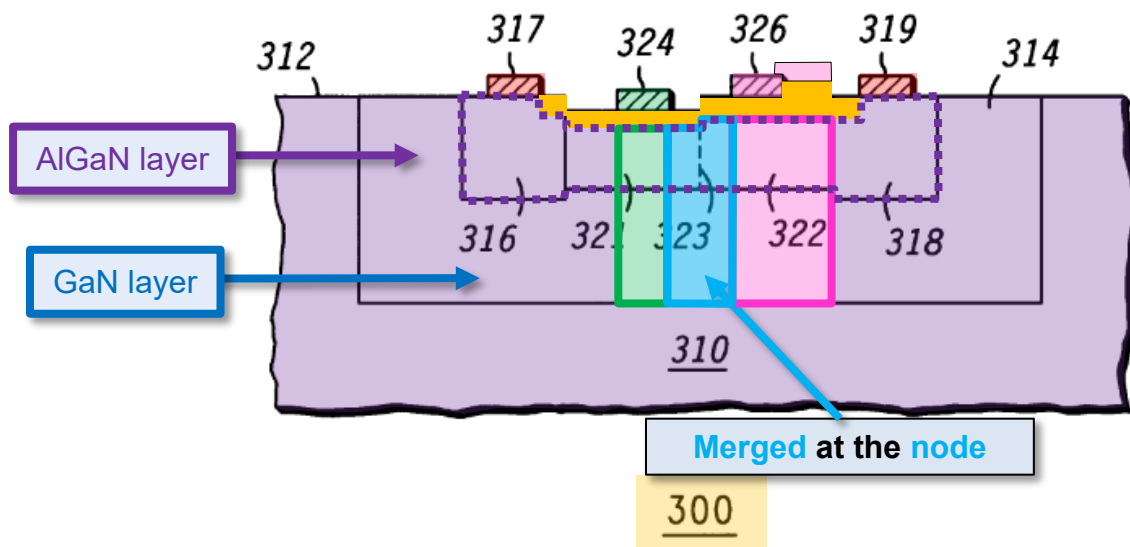


FIG. 7

Bonn, Fig. 7 (modified by Ren and Mishra, annotated)

C. Claim 2

[208] In my opinion, Bonn in view of Ren and Mishra renders claim 2.

1. [2PRE] The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:
[2A] a first III-Nitride layer; and

[209] Bonn in view of Ren and Mishra renders obvious [2PRE] and [2A],

“[t]he merged cascode transistor of claim 1, wherein the **semiconductor element** further comprises: **a first III-Nitride layer.**”

[210] The Bonn-Ren-Mishra combination includes an **AlGaIn layer** in the **semiconductor element**. Ren, ¶¶[0014], [0029], [0031]; *see* § XIII.A (Motivation

to Combine Bonn, Ren, and Mishra), above. AlGaN is a III-Nitride material. Ren, ¶¶[0003]-[0005], [0013]-[0014]; Mishra, ¶¶[0033]-[0034].

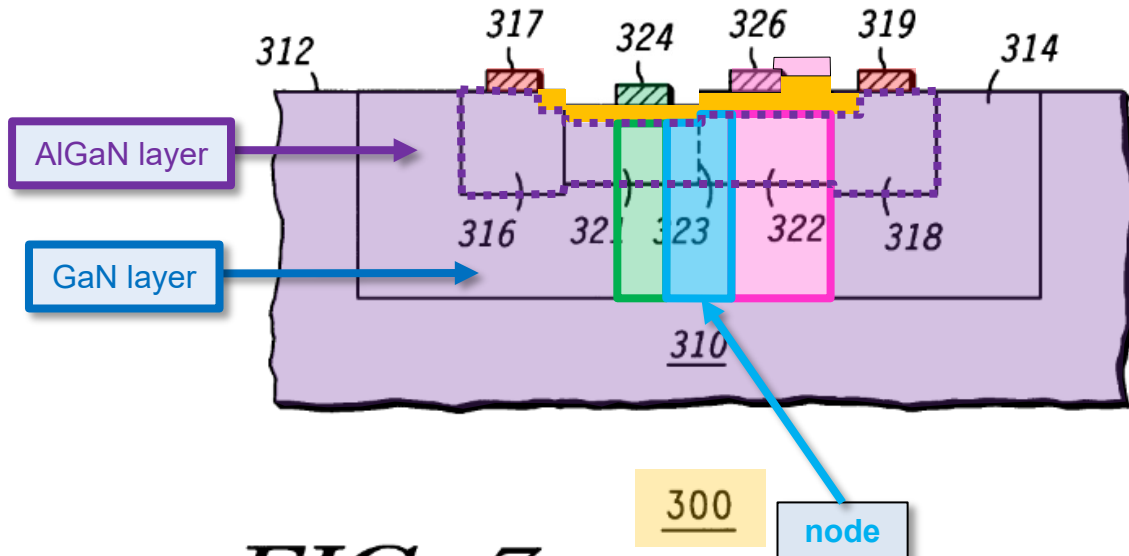


FIG. 7

Bonn, Fig. 7 (modified by Ren and Mishra, annotated)

2. [2B] a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.[2B] a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

[211] Bonn in view of Ren and Mishra renders obvious [2B], a **second III-Nitride** layer on which the first III-Nitride layer is positioned such that **a 2DEG conduction layer** forms between the **first** and **second III-Nitride** layers, wherein

the **source** electrode and the **drain** electrode are **ohmically connected** to the **first III-nitride layer**.

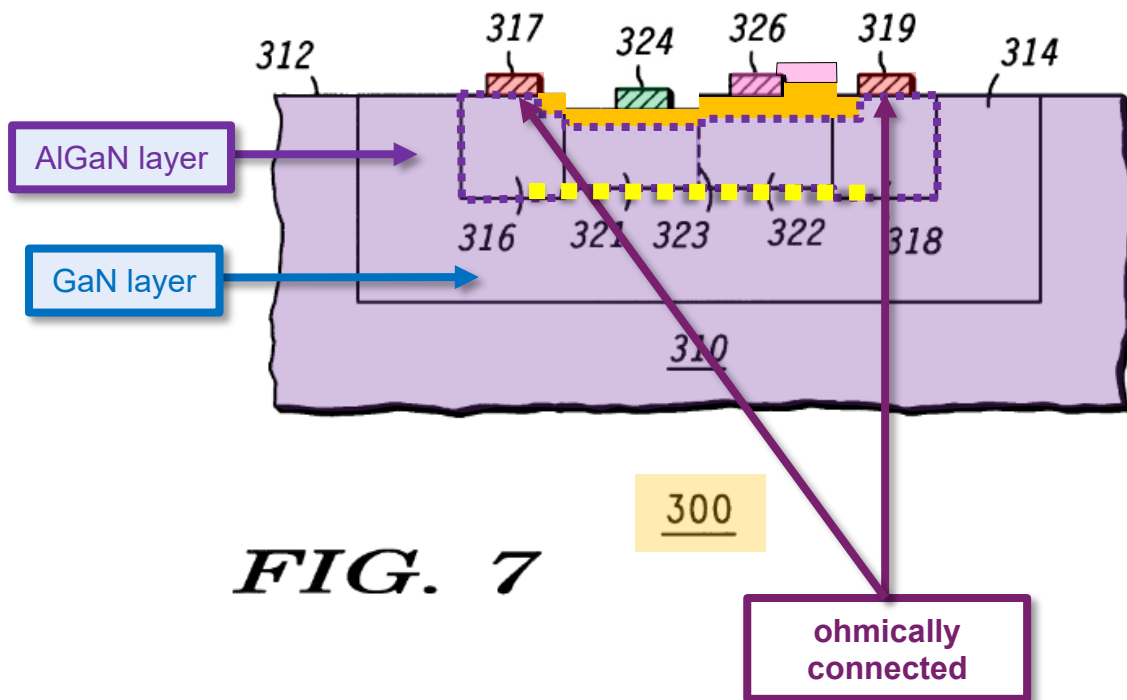
[212] The combination includes an **AlGa_N/Ga_N** stacked structure. Ren, ¶¶[0014], [0029], [0031]; *see* § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above. The combination's **GaN** layer is a **second III-Nitride** layer as claimed. Ren, ¶¶[0003], [0005]; Mishra, ¶¶[0033]-[0034].

[213] Although Ren does not use the term “2DEG conduction layer,” Ren discloses the “[t]he large interface charge can induce an electron sheet in the **GaN** near its interface with **AlGa_N**,” thereby disclosing that **a 2DEG conduction layer** forms between the **first** and **second III-Nitride** layers. Ren, ¶[0011]. For its transistors, Ren further states “the transistor structure forms a GaN quantum well at **AlGa_N/Ga_N** interface, which can provide better carrier confinement, improved carrier mobility and carrier concentration” i.e., it forms a 2DEG conduction layer between the **first** and **second III-Nitride** layers. Ren, ¶[0028]. A POSITA would have understood the “carrier” Ren describes refers to electrons, and “sheet carrier” at the **AlGa_N/Ga_N** interface refers to a 2DEG conduction layer. Ren, ¶¶[0025], [0028]. Ren further discusses and depicts inversion channels formed at the “heterojunction” at the **AlGa_N/Ga_N** interface and provides the energy band diagrams, and a POSITA would have understood a 2DEG at the heterojunction based on these disclosures. Ren, ¶¶[0035], [0039], [0023], Figs. 1a-1b, 2a-2b. Ren

states “[a]s a result of the band structure shown in FIG. 2(b), electrons can easily flow between the source and drain upon application of a voltage between the source and drain,” describing the well-understood physics of a 2DEG in semiconductor devices. Ren, ¶¶[0039].

[214] Mishra also describes that a 2DEG conduction layer forms between the AlGaN and GaN layers. Mishra, ¶¶[0007], [0037].

[215] Accordingly, in the combined Bonn-Ren-Mishra structure, a 2DEG conduction layer forms at the AlGaN/GaN interface, as illustrated in the dashed yellow line, below.



Bonn, Fig. 7 (modified, annotated).

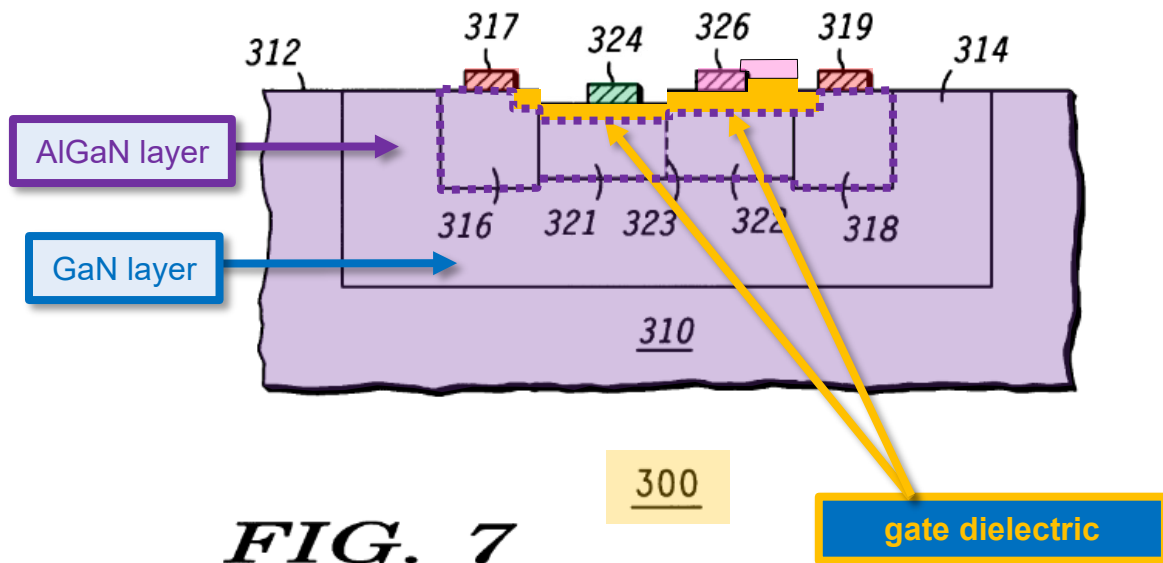
[216] Also as shown, in the combined Bonn-Ren-Mishra structure, the **source** and **drain** are electrodes that touch the **AlGa_N layer** and are **ohmically connected** to the **AlGa_N layer**. See § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above; Bonn, Fig. 7; Ren, Figs. 1a-1b. Bonn describes that source and drain electrodes are above source and drain regions of the semiconductor, which may be n-type doped. Bonn, 8:29-35. A POSITA would have understood this approach would lead to symmetrical, two-directional current flow that obey Ohm's law, i.e., the source and drain make ohmic contacts. Further, Mishra discloses its source and drain contacts are ohmic. Mishra, ¶¶[0035], [0037], [0045], Figs. 1-2, 6. Accordingly, in the Bonn-Ren-Mishra combination, source and drain contacts would have made ohmic contacts to the AlGa_N layer.

D. 3. The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

[217] Bonn in view of Ren and Mishra renders obvious claim 3, the merged cascode transistor of claim 2, further comprising **an insulating layer** positioned between the **first** and **second gates** and the **first III-Nitride** layer such that the **first** and **second gates** are capacitively coupled to the first **III-Nitride layer**.

[218] The combination includes an **insulating layer** below both gates. See § XIII.A (Motivation to Combine Bonn, Ren, and Mishra), above. Both Bonn and

Ren describe using a “gate dielectric,” which is an **insulating layer**, below the gate metal contact of its gates. Ren, ¶¶[0015], [0026], [0030], [0036], [0039], [0041], Figs. 1-2; Bonn, 11:12-2. A POSITA would have understood that this arrangement capacitively couples the gate to the underlying **AlGaN layer** because conductive materials are separated by an insulating gate dielectric layer such that there is capacitance between the gate and the AlGaN layer. This configuration is like well-known silicon MOS devices that have nearly zero gate leakage, reducing the energy needed to supply to the gate while keeping proper control of the channel conduction.

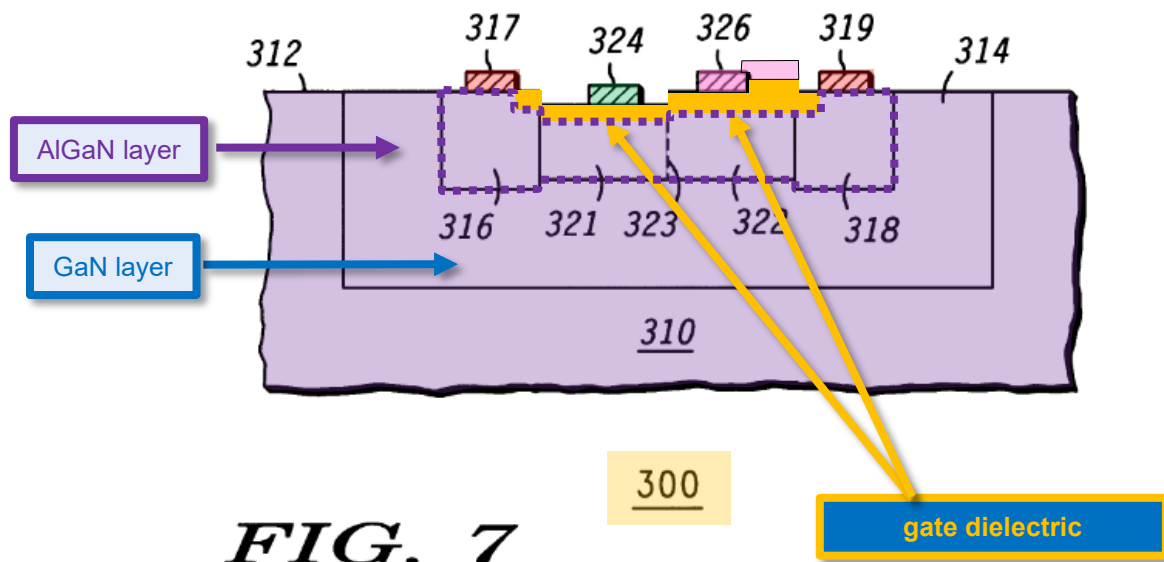


Bonn, Fig. 7 (modified by Ren and Mishra, annotated).

- E. 4. The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.**

[219] Bonn in view of Ren and Mishra renders obvious claim 4, the merged cascode transistor of claim 3, wherein the **first III-Nitride layer** comprises AlGaN material and the second **III-Nitride layer** comprises GaN material.

[220] The combination includes an **AlGaN/GaN** stacked structure as the **first III-Nitride layer** and **III-Nitride layer**. See §§ XIII.A (Motivation to Combine Bonn, Ren, and Mishra), XIII.C.1 (Ground 2: [2PRE], [2A]), XIII.C.2 (Ground 2: [2B]), above.



Bonn, Fig. 7 (modified by Ren and Mishra, annotated).

- F. 5. The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and**

the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

[221] Claim 5, which depends from claim 4 (which depends from claim 3), recites the same limitations as claim 3. Bonn in view of Ren and Mishra renders obvious claim 5 for the same reasons as for claim 3. *See* § XIII.D (Ground 2: claim 3), above.

G. 6. The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

[222] Bonn in view of Ren and Mishra renders obvious claim 6, the merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

[223] As explained, “first gate region 321 is in an enhancement mode.” Bonn, 8:51-9:4; *see* § XII.B.10 (Ground 1: [1C8]), above. The combination of Bonn, Ren, and Mishra uses Ren’s GaN enhancement mode transistor for first gate region 321. *See* §§ XIII.A (Motivation to Combine Bonn, Ren, and Mishra), XIII.B.10 (Ground 2: [1C8]), above. An enhancement mode transistor, by definition, is OFF at zero volts input voltage and conducts when an input voltage is above a predetermined threshold, as Ren discloses. Ren, ¶¶[0008] (enhancement mode “require[s] a positive voltage to turn on”), [0012] (an enhancement

MOSFET is characterized as a MOS device which forms a channel only when the gate to body (or source) voltage exceeds some threshold voltage”), [0038]-[0039].

Accordingly, the Bonn-Ren-Mishra combination renders obvious claim 6.

H. 7. The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.

[224] Bonn in view of Ren and Mishra renders obvious claim 7, the merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.

[225] As explained for limitation [1C7], the second gate region of the combination “conducts until” a saturation voltage of the depletion mode second gate is reached that results in a pinch-off voltage at which conductivity ceases in the conduction layer. *See* §§ VII (Technological Background) (e.g., describing pinch-off of cascodes with a first enhancement mode and second depletion mode gate, including simulation), XII.B.9 (Ground 1: [1C7]), XIII.B.9 (Ground 2: [1C7]), above.

I. 8. The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

[226] Bonn in view of Ren and Mishra renders obvious claim 8. Ren discloses using gate dielectric layers formed of silicon dioxide. Ren, ¶¶[0010], [0030].

J. 9. The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

[227] Bonn in view of Ren and Mishra renders obvious claim 9. Ren discloses “[g]ate dielectric layer 115 can be *any suitable dielectric*, such as SiO₂, SiN_x, MgO or SC₂O₃.” Ren, ¶[0030]. Thus, Ren discloses a gate dielectric formed of silicon dioxide (SiO₂) and a gate dielectric formed of silicon nitride (SiN_x), and a POSITA would have known that in combination they are also dielectric materials.

[228] A POSITA would have found it obvious that Ren’s “suitable dielectrics” include mixtures of materials Ren discloses, including a mixture of silicon dioxide and silicon nitride. A POSITA would have understood that such mixtures were common, especially for oxygen and nitrogen-based compounds, such that a mixture of SiN_x layer, which would have been silicon rich or mixed with oxides, such as SiO_xN_y (Silicon Oxy-Nitride), and silicon dioxide would have been obvious. Ren teaches such mixtures by including, for example, carbonated oxide (SiC₂O₃) as a suitable dielectric. Ren, ¶[0030]. As of the time of the ’003 patent, it was long known by a POSITA that these deposited insulators are often not stoichiometric, and it was routine to tailor mixtures of dielectrics for desired dielectric characteristics, including the permittivity, hardness, breakdown strength, conformal properties etc. *See* Bernstein-SiN (Ex-1023).

K. Claim 10

1. **[10PRE] 10. A merged cascode high electron mobility transistor circuit comprises:**

[229] The combination of Bonn, Ren, and Mishra renders obvious [10PRE].

As explained for [1PRE], the combination discloses a “merged cascode transistor circuit. *See* § XIII.B.1 (Ground 2: [1PRE]), above. Further, Ren discloses its devices are high electron mobility transistors (HEMTs). Ren, Abstract, ¶¶[0007]-[0014].

2. **[10A] an input voltage signal source having an input voltage signal;**

[230] The combination of Bonn, Ren, and Mishra renders obvious [10A] as explained for [1A]. *See* § XIII.B.2 (Ground 2: [1A]).

3. **[10B] a constant voltage source having a predetermined constant voltage;**

[231] The combination of Bonn, Ren, and Mishra renders obvious [10B] as explained for [1B]. *See* § XIII.B.3 (Ground 2: [1B]).

4. **[10C] a merged cascode transistor comprising:**

[232] The combination of Bonn, Ren, and Mishra renders obvious [10C] as explained for [1C]. *See* § XIII.B.4 (Ground 2: [1C]).

5. [10C1] a first epitaxial layer of III-Nitride material;

[233] The combination of Bonn, Ren, and Mishra renders obvious [10C1] as explained for [2PRE]-[2A]. *See* § XIII.C.1 (Ground 2: [2PRE]-[2A]). In addition to those reasons, Ren's AlGa_N layer is an "epitaxial" layer. Ren, ¶[0029] (purported invention includes "epitaxial stack" of AlGa_N and Ga_N layers).

6. [10C2] a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

[234] The combination of Bonn, Ren, and Mishra renders obvious [10C2] as explained for [2B]. *See* § XIII.C.2 (Ground 2: [2B]), above. In addition to those reasons, Ren's AlGa_N and Ga_N layers are "epitaxial" layers. Ren, ¶[0029] (purported invention includes "epitaxial stack" of AlGa_N and Ga_N layers).

7. [10C3] a source electrode electrically connected to the first epitaxial layer; [10C4] a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;

[235] The combination of Bonn, Ren, and Mishra renders obvious [10C3]-[10C4] as explained for [1C1]-[1C3]. *See* § XIII.B.5 (Ground 2: [1C1]-[1C3]), above.

8. **[10C5] a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and**

[236] The combination of Bonn, Ren, and Mishra renders obvious [10C5] as explained for [1C4]. *See* § XIII.B.6 (Ground 2: [1C4]), above.

9. **[10C6] a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;**

[237] The combination of Bonn, Ren, and Mishra renders obvious [10C6] as explained for [1C5]. *See* § XIII.B.7 (Ground 2: [1C5]), above.

10. **[10C7] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and**

[238] The combination of Bonn, Ren, and Mishra renders obvious [10C7] as explained for [1C6]. *See* § XIII.B.8 (Ground 2: [1C6]), above.

11. **[10C8] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,**

[239] The combination of Bonn, Ren, and Mishra renders obvious [10C8] as explained for [1C7]. *See* § XIII.B.9 (Ground 2: [1C7]), above.

- 12. [10C9] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and**

[240] The combination of Bonn, Ren, and Mishra renders obvious [10C9] as explained for [1C8]. *See* § XIII.B.10 (Ground 2: [1C8]), above.

- 13. [10C10] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.**

[241] The combination of Bonn, Ren, and Mishra renders obvious [10C10] as explained for [1C9]. *See* § XIII.B.11 (Ground 2: [1C9]), above.

- L. 11. The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.**

[242] The combination of Bonn, Ren, and Mishra renders obvious claim 11 as explained for claim 3. *See* § XIII.D (Ground 2: Claim 3), above.

- M. 12. The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGaN material and the second epitaxial layer comprises a GaN material.**

[243] The combination of Bonn, Ren, and Mishra renders obvious claim 12 as explained for claim 4. *See* § XIII.E (Ground 2: Claim 4), above.

- N. 13. The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input**

voltage signal provides an input voltage above a predetermined threshold voltage.

[244] The combination of Bonn, Ren, and Mishra renders obvious claim 13 as explained for claim 6. *See* § XIII.G (Ground 2: Claim 6), above.

O. 14. The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.

[245] The combination of Bonn, Ren, and Mishra renders obvious claim 13 as explained for claim 7. *See* § XIII.H (Ground 2: Claim 7), above.

P. 15. The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.

[246] The combination of Bonn, Ren, and Mishra renders obvious claim 14 as explained for claim 8. *See* § XIII.I (Ground 2: Claim 8), above.

Q. 16. The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.

[247] Bonn in view of Ren and Mishra renders obvious claim 16. Ren discloses “[g]ate dielectric layer 115 can be any suitable dielectric, such as SiO₂, SiN_x, MgO or SC₂O₃.” Ren, ¶[0030]. Thus, Ren discloses a gate dielectric formed of Silicon Nitride (SiN_x).

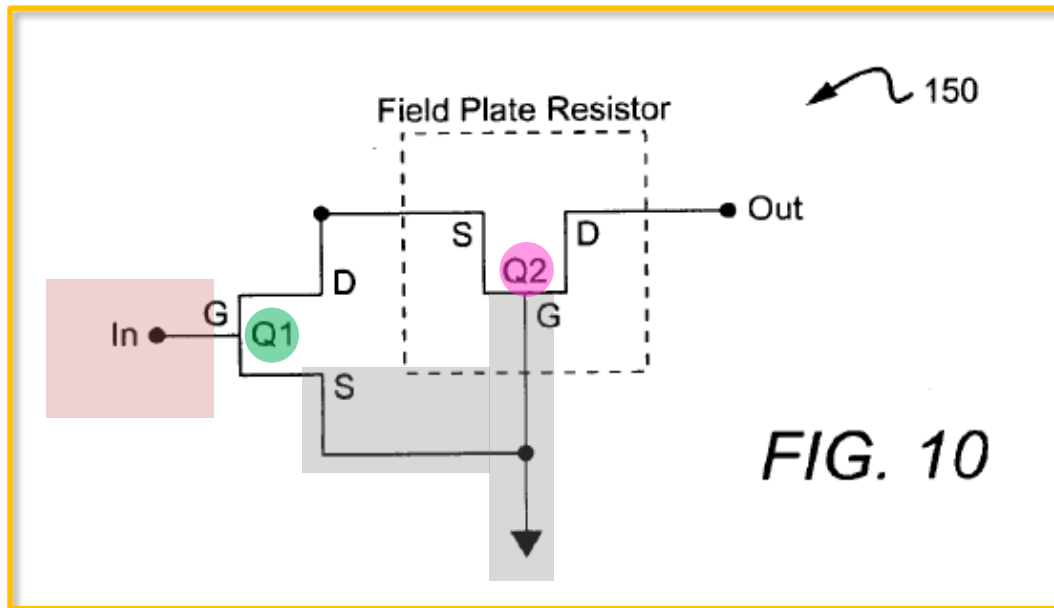
XIV. GROUND 3: MISHRA AND REN (CLAIMS 1-16)**A. Motivation to Combine Mishra and Ren**

[248] In my opinion, a POSITA would have found it obvious to combine Mishra and Ren.

[249] Mishra discloses implementing dual gate GaN HEMTs in cascode circuits. Mishra, Title, Abstract, ¶¶[0026]-[0028], [0030], [0042]-[0044], [0055]-[0060], Figs. 5, 10. Mishra describes a “2-stage cascode amplifier” with “a first stage transistor connected in common source configuration and a second stage field-plated transistor connected in common gate configuration,” where the “first stage is arranged to provide current gain and does not ‘see’ high voltages, while the second field-plated stage does see high voltages and is arranged to provide voltage gate.” Mishra, ¶[0056]. Mishra notes other cascode transistors consistent with its alleged invention are possible with different arrangements. Mishra, ¶[0057], [0062]-[0063]. Mishra flexibly describes its alleged invention as comprising “many different amplifier arrangements” with differently shaped field plates than those it expressly discloses. Mishra, ¶[0062]-[0063].

[250] The first and second stage transistors “can comprise a wide bandgap field effect transistor such as a GaN-based HEMT,” including those described in Mishra. Mishra, ¶[0057]. Mishra discloses biasing the source side gate (e.g., gate

62 of Figure 5) at low voltage, and the drain side gate (field plate 66 of Figure 5) at higher voltage. Mishra, ¶[0060]. Figure 10 shows an example cascode.



Mishra, Fig. 10 (annotated).

[251] Mishra does not explicitly comment on the mode in which **Q1** operates in cascode embodiments, but a POSITA would have found it obvious to use an enhancement mode device. As I will explain, a POSITA would have understood that Mishra’s low voltage bias of the source side transistor (**Q1**) includes low positive voltages—Mishra thus renders obvious using an enhancement mode gate as its source side gate. Mishra, ¶[0060].

[252] A POSITA would have found it obvious to use an enhancement mode device for **Q1**. Mishra notes “[t]he first stage is arranged to provide current gain and does not ‘see’ high voltages” and provides the example of **Q1** being “biased at

a low voltage.” Mishra, ¶¶[0055], [0060]. For high power and high voltage operation, the control signals are generally only positive voltages, requiring that **Q1** be an enhancement mode device so that it is normally off without any applied gate voltage, $V_{g1}=0$. At the time of the '003 patent, such cascodes with a first stage enhancement and second stage depletion mode were known. This approach was implemented, for example, in Bonn. Bonn, 8:51-9:4. Sankin also used this approach. Sankin (Ex-1018), ¶¶[0013], [0119], Fig. 1. So does Salato. Salato (Ex-1017), 1:30-34 (“cascoded configuration of a normally ON depletion mode and a normally OFF [enhancement mode] semiconductor devices allows reliable and safe operation in switching mode power supply system”).

[253] In a first stage enhancement and second stage depletion mode implementation of Mishra, when V_{g1} becomes greater than the threshold voltage of the enhancement mode gate **G1**, then the two transistors will both be ON, allowing the current to flow through the combined cascode device. However, when the V_g is reduced to zero volts, below the threshold voltage, then the maximum voltage seen at the drain of **Q1** will be limited by the negative pinch-off or threshold voltage of the upper (**Q2**) depletion mode device.

[254] Given the above, a POSITA would have found it obvious to make the first gate **G1** an enhancement mode gate. The cascode would be “off” (i.e., not

conducting) below the turn-on voltage of the enhancement mode gate, making it “normally off” at zero volts. A POSITA would have done so to achieve the benefits of a “normally off” device, including reduced power consumption and suitability for high voltage and high frequency operations. Ren, ¶¶[0005], [0040]. This arrangement also has the added known benefit of being safer to operate. Salato (2005 priority date) discloses a cascode with a “cascode configuration of a normally ON depletion mode and a normally OFF [enhancement mode] semiconductor devices allows reliable and safe operation in switching mode power supply systems.” Salato (Ex-1017), 1:30-34.

[255] Mishra expresses goals to “achieve efficient high power and high frequency signal amplification” and “reduce[d] leakage.” Mishra, ¶¶[0011], [0029]. To achieve these goals, in view of Mishra disclosures of: using many cascode arrangements and GaN-HEMT materials; using a first stage transistor to provide current gain; biasing the first gate at low voltage (e.g., at 0V); and operating at high frequency for maximum gain, a POSITA would have looked to disclosures of other GaN-based devices to form the first and second transistors, including Ren. Mishra, ¶¶[0011], [0029], [0055]-[0063]. Mishra discloses using a range of doped and undoped Group III-nitride material with various parameter values (e.g., thickness, doping concentration, etc.). Mishra, ¶[0034] (providing exemplary parameters and incorporating by reference patent publications to

disclose still other exemplary parameters). POSITA would have been capable of adjusting the threshold voltage of the input to operate in enhancement mode by adjusting the properties of semiconductor layers. As I will explain, it would have been obvious to do so over Ren.

[256] Ren discloses its devices have improved “physical characteristics that are suitable for use in high-frequency, high-temperature, and high-power semiconductor devices.” Ren, ¶[0005]. Ren further teaches the advantages of enhancement mode devices, noting they “use less power as compared to depletion mode devices because enhancement mode devices, unlike depletion mode devices, generally consume little or no power during stand-by mode.” Ren, ¶[0040]. Ren discloses making GaN enhancement mode (low voltage bias) or depletion mode gates (high voltage bias) with an insulating “gate dielectric” layer between the gate metal contact and underlying AlGaN barrier layer. Ren, ¶¶[0012]-[0018], [0026], [0030], [0036], [0039], [0041], Figs. 1-2.

[257] A POSITA would have found it obvious to use Ren’s simple techniques to make Mishra’s first gate enhancement mode and second gate depletion mode.

[258] A POSITA would also have been familiar with using insulating dielectrics to make GaN HEMTs, including in enhancement mode devices, as Ren discloses. *E.g.*, Beach (Ex-1020), ¶¶[0033], [0047]-[0049], claim 5, Figs. 4-5.

Mishra discloses a goal of “reduced leakage currents and enhanced reliability.

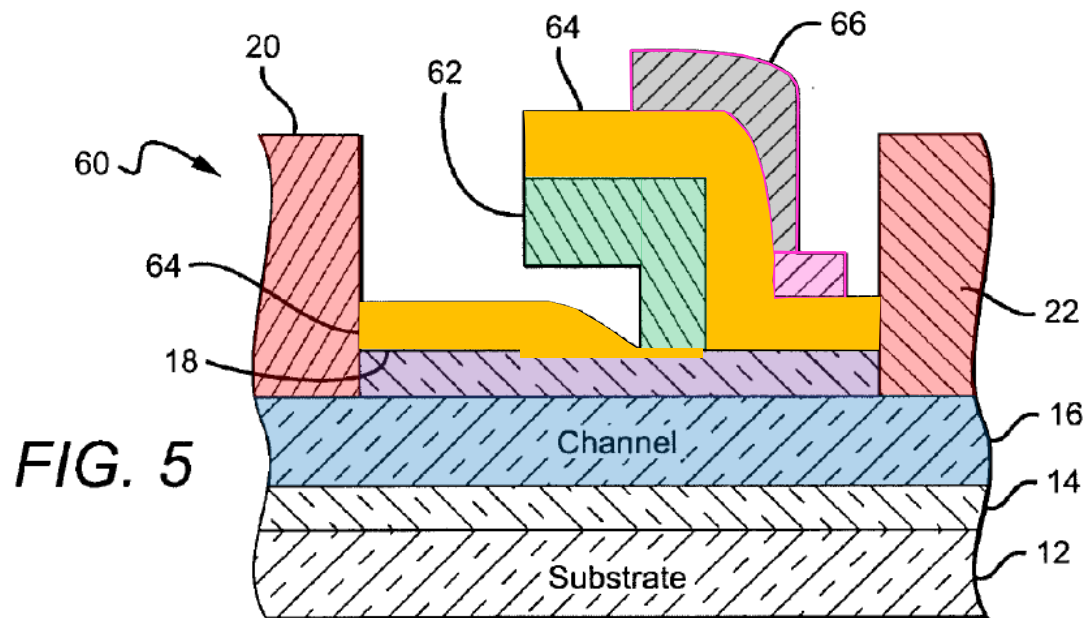
Mishra, ¶[0029]. A POSITA would have known that gate insulating layers like those disclosed in Ren also reduce gate leakage. Beach, ¶¶[0005]-[0006].

Accordingly, a POSITA would have been motivated to use Ren’s approach to reduce gate leakage.

[259] Ren’s solution includes an AlGa_N over Ga_N epitaxial structure, just like Mishra, and Ren teaches forming enhancement mode or depletion mode by varying the thickness of the AlGa_N layer. Ren, ¶¶[0014], [0029], [0031]. A thinner layer leads to an enhancement mode device, while a thicker layer leads to a depletion mode device. Ren, ¶¶[0014], [0033]; *see* § X.C (Overview of Ren (Ex-1007, U.S. 2004/0041169)), above.

[260] The combination would have been an implementation of Ren’s known option in Mishra’s device for predictable results. Mishra already discloses a “**spacer layer**”/“**dielectric layer**”/“**passivation layer**” above the channel layer that is under the **second gate** but not under the **first gate**. Mishra, ¶¶[0028], [0035]-[0036], [0039], [0043], [0049]-[0050], Figs. 2 (spacer layer 24), 4 (passivation layer 44), 5 (**spacer layer 64**). In the embodiment of Mishra’s Fig. 5, a POSITA would have extended **layer 64** under Mishra’s **gate 62** to realize the benefits of reduced gate leakage. *See* above (e.g., Beach, ¶¶[0005]-[0006]). When making this simple modification, a POSITA would have adjusted the doping

characteristics and **AlGaN** thickness, as Ren discloses, to predictably achieve an **enhancement mode** (thinner **AlGaN**) and **depletion mode** gates (thicker **AlGaN**) of the original Mishra device. *See* § XIV.K.12 (Ground 3: [10C9]), below; Ren, ¶¶[0014], [0029], [0031]. Mishra incorporates by reference Wu (Ex-1021) and Chavarkar (Ex-1022) for methods of forming gate contacts, which describes known methods of windowing and etching gates. Mishra, ¶¶[0034], [0037]; Wu, 7:19-26, Fig. 9 (window etching); Chavarkar, ¶¶[0023], [0040], Fig. 6 (gate recessed in AlGaN layer). Over the teachings of Mishra (including Wu and Chavarkar) and Ren, a POSITA would have found it obvious to etch under the **gate 62** to decrease **AlGaN** thickness and maintain enhancement mode in **gate 62** prior to depositing **passivation layer 64**. These modifications are illustrated in modified Figure 5, below.



Mishra, Fig. 5 (annotated, modified by Ren)

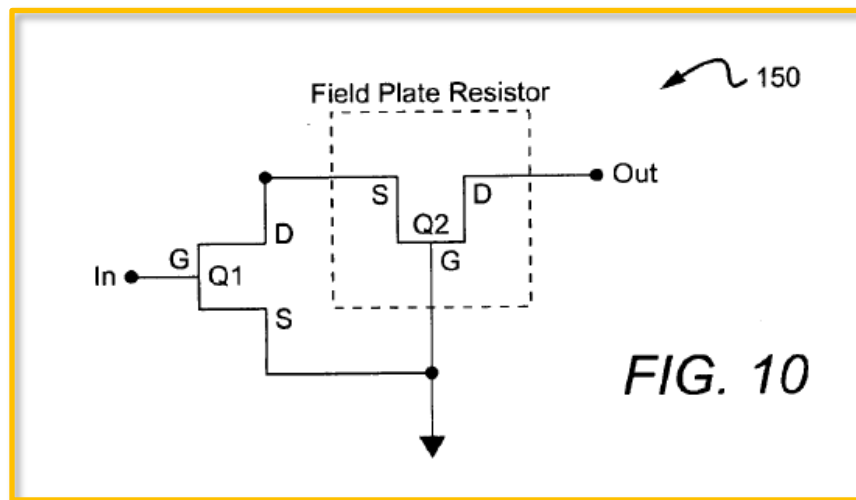
B. Claim 1

[261] Claim 1 is obvious over Mishra in view of Ren.

1. [1PRE] A merged cascode transistor circuit comprising:

[262] Mishra discloses [1PRE], a **merged cascode transistor** circuit.

Mishra discloses a cascode transistor circuit, as shown in Figure 10. Mishra, Title, Abstract, ¶¶[0026]-[0028], [0030], [0055]-[0060], Fig. 10.

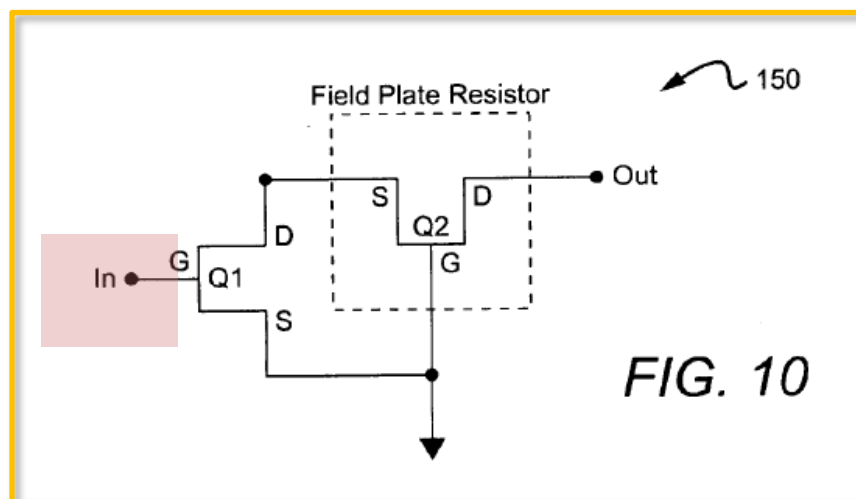


Mishra, Fig. 10 (annotated).

2. [1A] an input voltage signal source having an input voltage signal;

[263] Mishra discloses [1A], an input voltage signal source having **an input voltage signal**.

[264] Mishra's cascode has an **input voltage** at the first gate of Q1. Mishra, ¶¶[0055], [0058], Fig. 10.

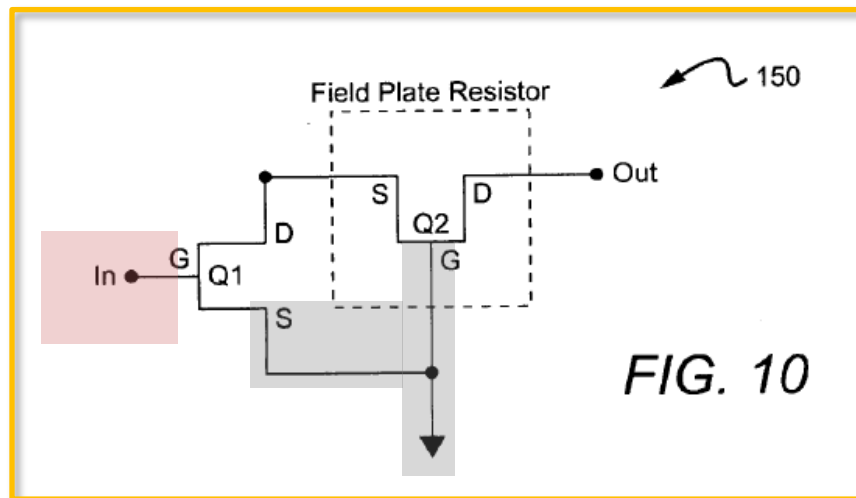


Mishra, Fig. 10 (annotated).

3. [1B] a constant voltage source having a predetermined constant voltage;

[265] Mishra discloses [1B], a **constant voltage** source having a predetermined constant voltage.

[266] Mishra's second gate, Q2 is connected to ground, a **constant voltage** source. Mishra, ¶¶[0055], [0058], Fig. 10.



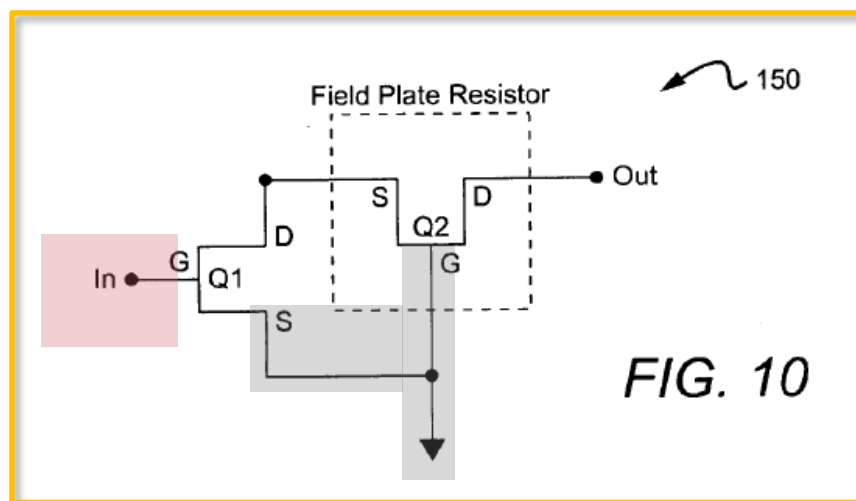
Mishra, Fig. 10 (annotated).

[267] The '003 patent also describes ground as a **constant voltage** source of the second gate. '003 patent, 3:42-46, Figs. 2-4.

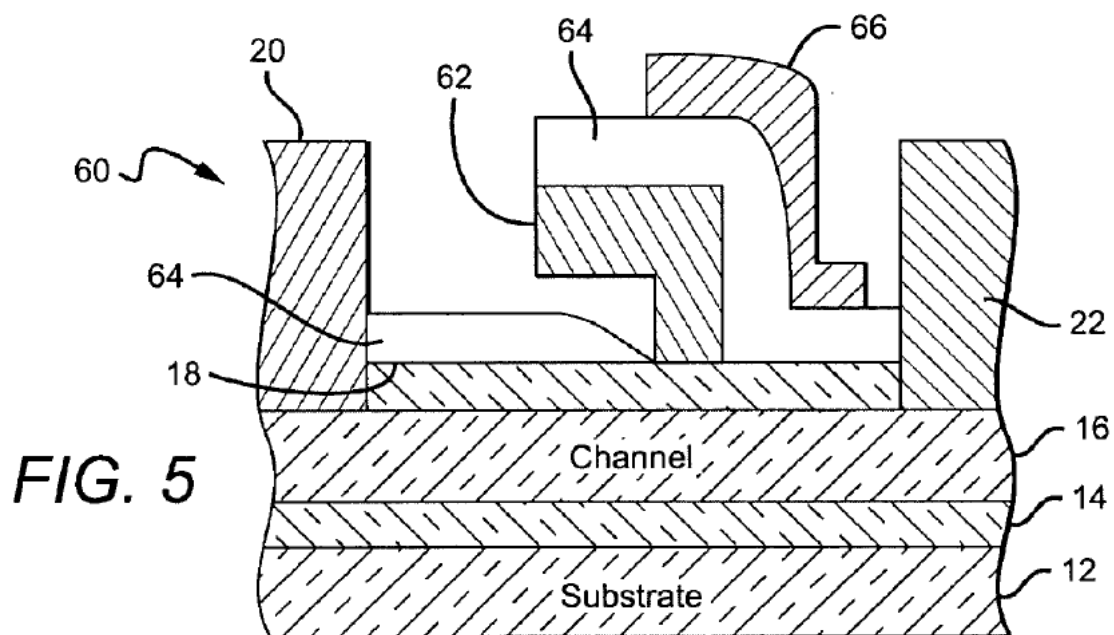
4. [1C] a merged cascode transistor comprising:

[268] Mishra discloses [1C], a **merged cascode transistor**.

[269] Mishra discloses a cascode transistor circuit, as shown in Figure 10. Mishra, Title, Abstract, ¶¶[0026]-[0028], [0030], [0055]-[0060], Fig. 10. Mishra describes implementing GaN HEMT transistors in cascode, including the FET of Figure 5. Mishra, ¶¶[0055]-[0060], Fig. 10.



Mishra, Fig. 10 (annotated).



Mishra, Fig. 5.

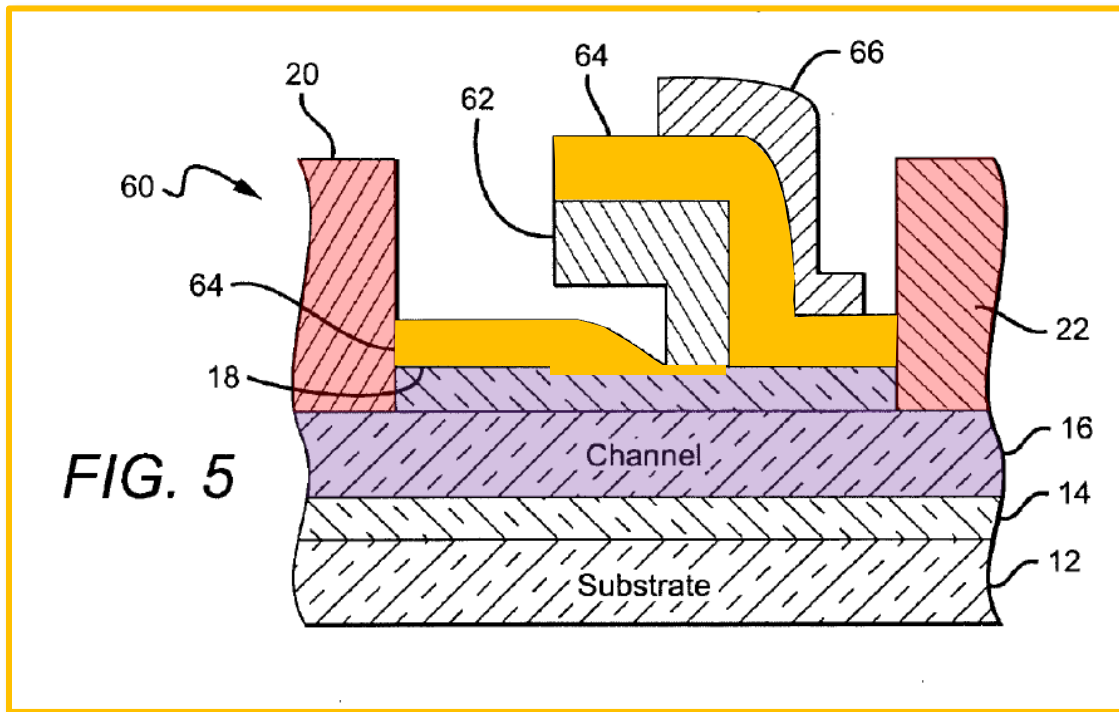
5. [1C1] a semiconductor element;
[1C2] a source electrode electrically connected to a top surface of the semiconductor element; and
[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;

[270] Mishra discloses [1C1]-[1C3], which are entirely conventional.

[271] Mishra discloses [1C1] because it discloses “**barrier layer 18**,” and “**channel 16**,” which form a **semiconductor element**, as claimed. Mishra, ¶¶[0034], [0042].

[272] Mishra discloses [1C2] and [1C3] because it discloses source and drain electrodes electrically connected to the semiconductor element and spaced laterally on either side of the semiconductor element, touching the top surface. Mishra’s “**source contact 20**” and “**drain contact 22**” are electrically connected to **barrier layer 18**, including its top surface, because “**source contact 20**” and “**drain contact 22**” contact **barrier layer 18**, including its top surface. Mishra, ¶[0042], Fig. 5. The “**source contact 20**” and “**drain contact 22**” are laterally spaced, as claimed. Mishra, Fig. 5.

[273] The Mishra-Ren combination includes the same features, as shown below. *See* § XIV.A (Motivation to Combine Mishra and Ren), above.



Mishra, Fig. 5 (annotated, modified by Ren).

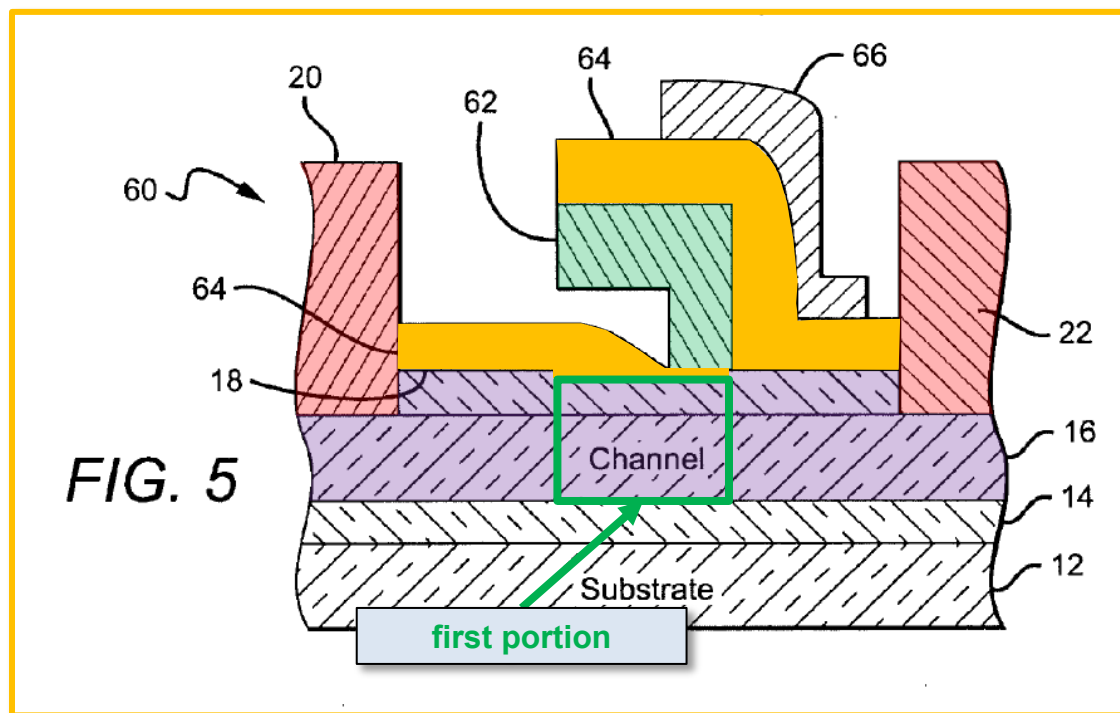
6. [1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

[274] Mishra in view of Ren renders obvious [1C4], a **first gate** positioned between the **source electrode** and the **drain electrode** and coupled to the **semiconductor element** to form a **first portion of the transistor**.

[275] Mishra's **gate 62** is a first gate between “**source contact 20**” and “**drain contact 22**.” Mishra, ¶¶[0042]-[0043], Fig. 5. **Barrier layer 18** and **channel 16** form a semiconductor element, as claimed. Further, **gate 62** is coupled to **barrier layer 18** because it is in contact with the top surface of **barrier layer 18**. Mishra, ¶¶[0042]-[0043], Fig. 5. The gate forms a **first portion of the**

transistor that includes the region of **barrier layer 18** and **channel 16** below the gate.

[276] The Mishra-Ren combination includes the same features, as shown below. *See* § XIV.A (Motivation to Combine Mishra and Ren), above.



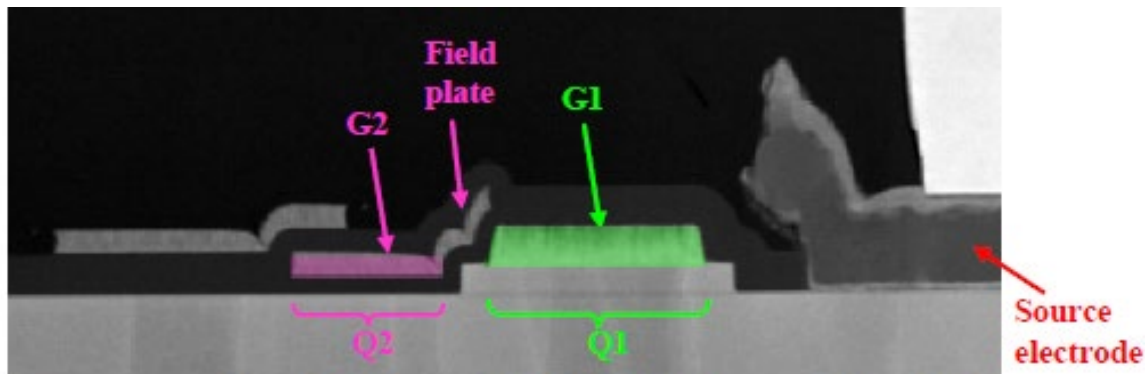
Mishra, Fig. 5 (annotated, modified by Ren)

7. [1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;

[277] Under Infineon's apparent infringement theory, Mishra in view of Ren renders obvious [1C5], a **second gate** positioned adjacent to the **first gate**, and between the **source electrode** and the **drain electrode** to form a **second portion of**

the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element.

[278] In a related proceeding, Infineon accuses certain Innoscience devices of infringement of the '003 patent. Ex-1010 at 11; Ex-1011. In a TEM image, Infineon identifies a first structure, G1, as the claimed first gate and a second structure, G2, as the second gate, and identifies a region of that same structure as a field plate. Ex-1011 at 21.



(Cross-sectional view TEM image of INN100W032A, annotations added)

Ex-1011 at 21.

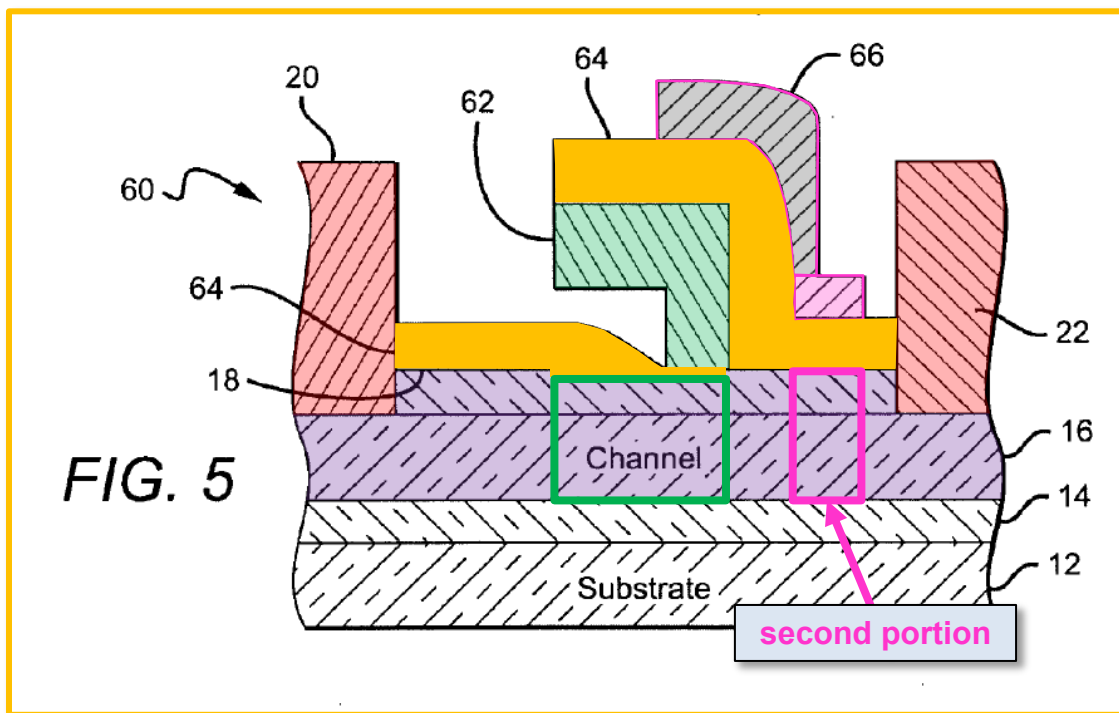
[279] Under Infineon's apparent infringement theory, Mishra discloses [1C5].

[280] Mishra's field plate 66 is positioned adjacent to the first gate, as shown in Figure 5. Mishra, ¶¶[0042]-[0045], Fig. 5. Field plate 66 is also between "source contact 20" and "drain contact 22." Mishra, ¶¶[0042]-[0045], Fig. 5.

Further, **field plate 66** is capacitively coupled to the **barrier layer 18** through the spacer layer 64. Mishra, ¶¶[0042]-[0045], [0060], Figs. 5.

[281] When implemented in a cascode, **field plate 66** is also coupled to ground and, consistent with Infineon's infringement theory, it forms a **second portion of the transistor** below its bottommost portion. Mishra, ¶¶[0042]-[0045], [0055]-[0061], Figs. 5, 10.

[282] The Mishra-Ren combination includes the same features, as shown below. *See* § XIV.A (Motivation to Combine Mishra and Ren), above.



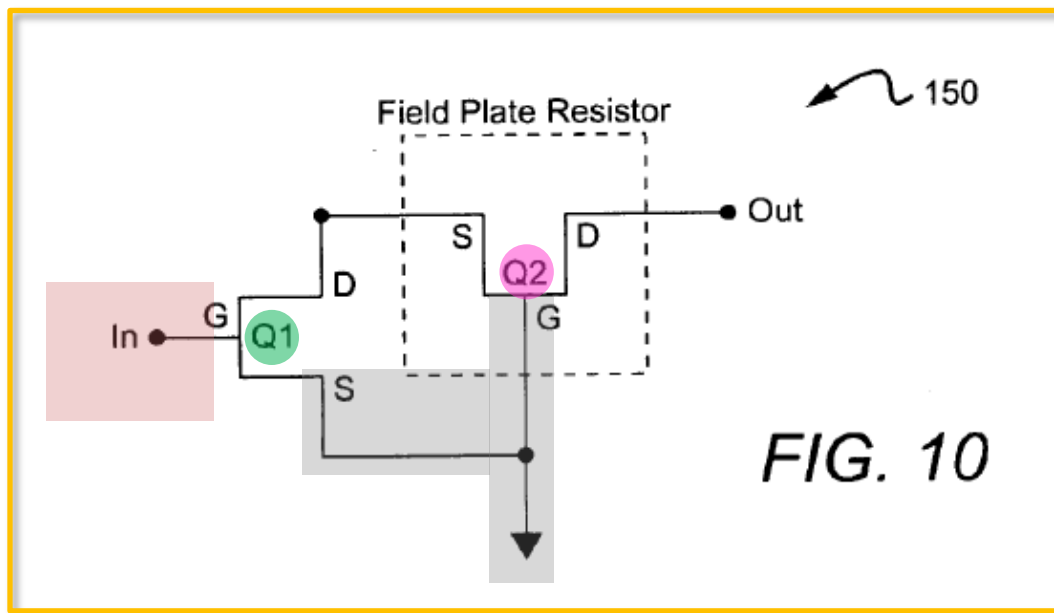
Mishra, Fig. 5 (annotated, modified by Ren).

8. [1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and

[283] Mishra in view of Ren renders obvious [1C6], wherein the **first gate** is connected to the **input voltage signal source** such that conduction of **the first portion of the transistor** is based on a value of the **input voltage signal**.

[284] Mishra's **gate 62** is connected to an **input** in cascode implementations that controls the conduction of **the first portion of the transistor** under the **gate 62**. Mishra, ¶¶[0042]-[0045], [0055]-[0061], Figs. 5, 10 (showing **input** to Q1). For example, Mishra teaches biasing the conduction of **gate 62** at low voltage, below which the gate would not conduct. Mishra, ¶[0060]. Describing a similar gate, Mishra teaches "[e]lectric current can flow between the source and drain contacts 20, 22 through a two-dimensional electron gas (2DEG) induced at the heterointerface between the channel layer 16 and the barrier layer 18 when the gate 26 is biased at the appropriate level." Mishra, ¶[0037]. Mishra thus discloses or at least renders obvious that conduction is based on an **input voltage signal**.

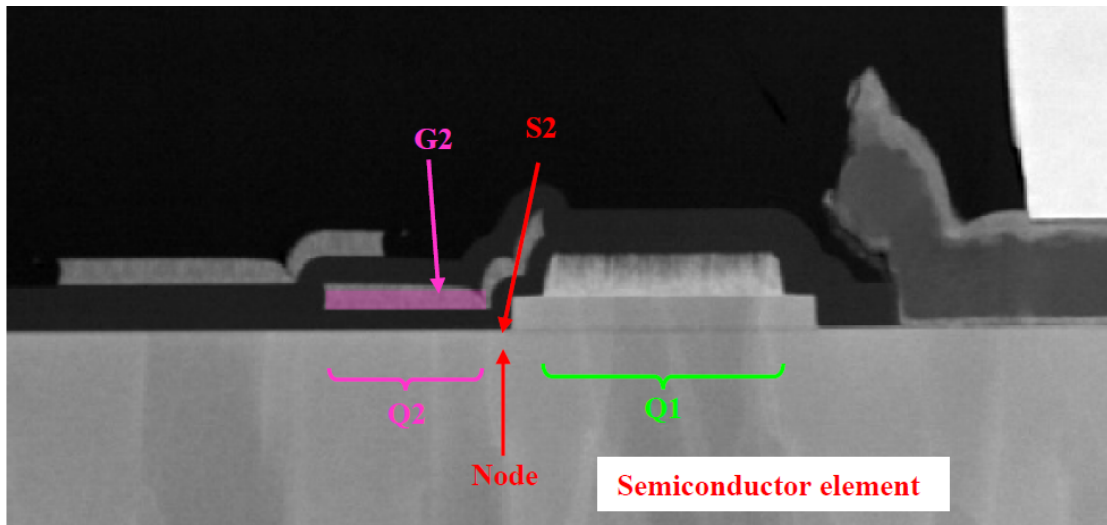
[285] Further, the Mishra-Ren combination includes the same features. *See* § XIV.A (Motivation to Combine Mishra and Ren), above.



Mishra, Fig. 10 (annotated)

9. [1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,

[286] Mishra in view of Ren renders obvious [1C7], the **second gate** is connected to the **constant voltage source** such that the **second portion** of the transistor conducts until a voltage difference between the **predetermined constant voltage** and a voltage at a **node** in the **semiconductor element** between the **first portion** and the **second portion** of the transistor reaches a predetermined level, under Infineon's apparent infringement theory. Ex-1011, 26.



(Cross-sectional view TEM image of INN100W032A, annotations added)

In a power transistor device, a threshold voltage (V_{th}) is a gate-to-source voltage (V_{GS}) below which the conduction of the device is off. *See* Ex. 28 at 26-27.

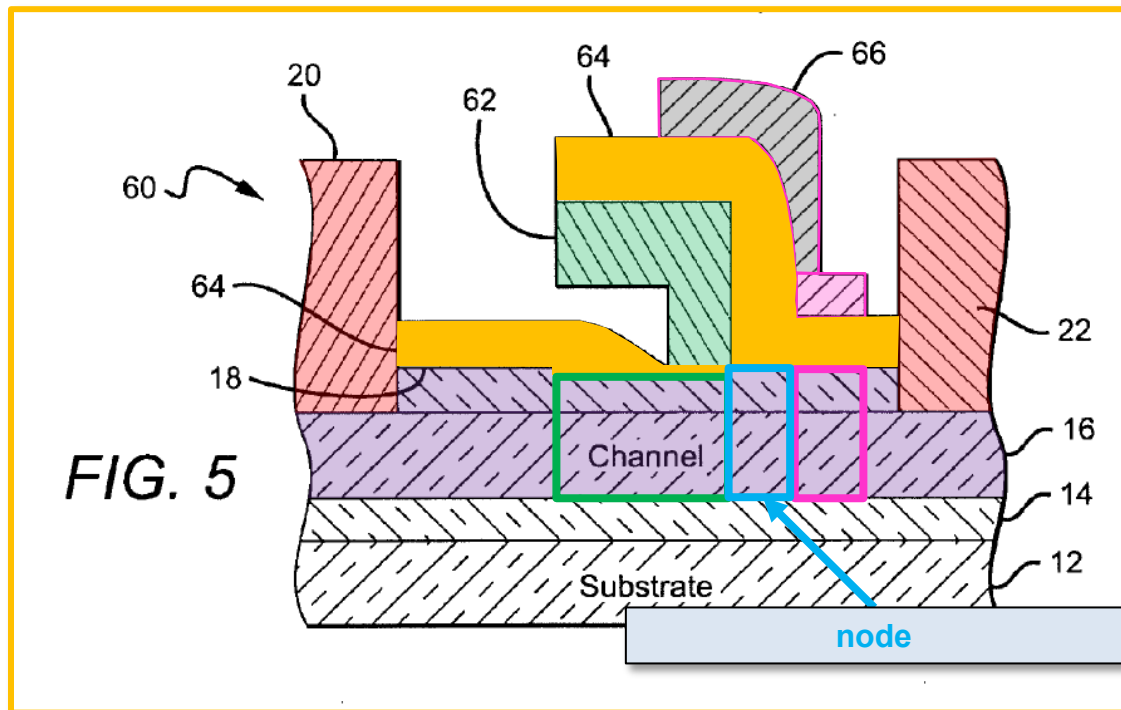
Therefore, the second portion of the transistor Q2 conducts until its gate-to-source voltage V_{GS} (namely, a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor) reaches a threshold voltage V_{th} (i.e. reaches a predetermined level).

Ex-1011, 26.

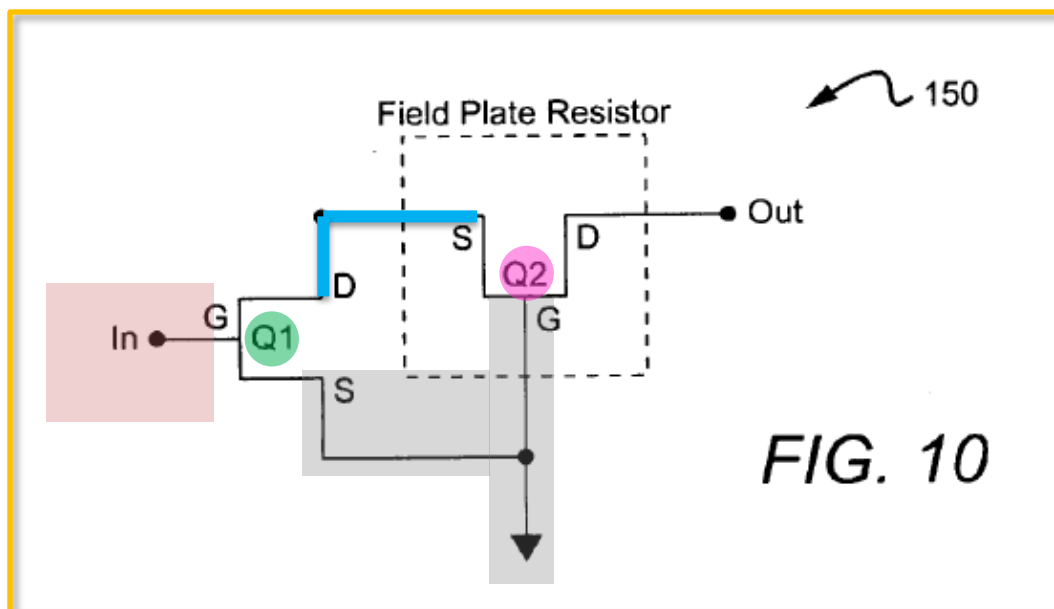
[287] Mishra's **field plate 66** and **gate 62** are formed on the same **barrier layer 18**, so whether the **second portion** conducts depends on an **input voltage** in cascode implementations that controls the conduction of **the first portion** under the **gate 62**. Mishra, ¶¶[0042]-[0045], [0055]-[0061], Figs. 5, 10 (showing **input** to Q1). In Mishra, "[e]lectric current can flow between the source and drain contacts 20, 22 through a two-dimensional electron gas (2DEG) induced at the heterointerface between the channel layer 16 and the barrier layer 18 when the gate 26 is biased at the appropriate level." Mishra, ¶[0037].

[288] In the Mishra-Ren combination, when the **first gate** is off, Mishra's **second portion** conducts until a saturation voltage of the depletion mode second gate is reached that results in a pinch-off of the conduction layer (upper voltage limit), which is how depletion mode gates normally function. *See* § VII (Technological Background) (e.g., describing pinch-off in cascodes with a first enhancement mode and second depletion mode gate, including simulation), above. When Mishra's **first gate** turns off (e.g., by reducing input voltage below the turn on voltage of the **first gate**), the 2DEG under the first gate disappears, but voltage at the **node** rises because it is connected to the **drain** via the 2DEG under the second transistor. As the **node** voltage rises, the voltage difference between the **second gate** (held to ground) and the increasing **node** voltage (which is the source voltage for the upper Q2) becomes negative (gate to source voltage will be negative when the source voltage rises above zero), until eventually it reaches a saturation voltage (i.e., a threshold voltage at a predetermined level) that results in a pinch-off of the conduction layer below the gate and conductivity ceases. Indeed, Mishra acknowledges this phenomenon, stating “the maximum voltage that can appear on the drain of the first stage transistor Q1 is the threshold voltage of the second stage transistor Q2.” Mishra, ¶[0059]. Pinch off thus occurs at a “predetermined level” of voltage difference between the **ground** and the **node**—Mishra's “threshold voltage.” Mishra, ¶[0059].

[289] The Mishra-Ren combination includes the same features, as shown below. *See* § XIV.A (Motivation to Combine Mishra and Ren), above.



Mishra, Fig. 5 (annotated, modified by Ren).



Mishra, Fig. 10 (annotated).

[290] The same occurs in the Mishra-Ren combination. As explained, a POSITA would have found it obvious to use Ren's simple techniques to make Mishra's **first gate** enhancement mode and **second gate** depletion mode. *See* § XIV.A (Motivation to Combine Mishra and Ren), above. The **first gate** is in enhancement mode and is off when V_{g1} is below its turn on (threshold) voltage.

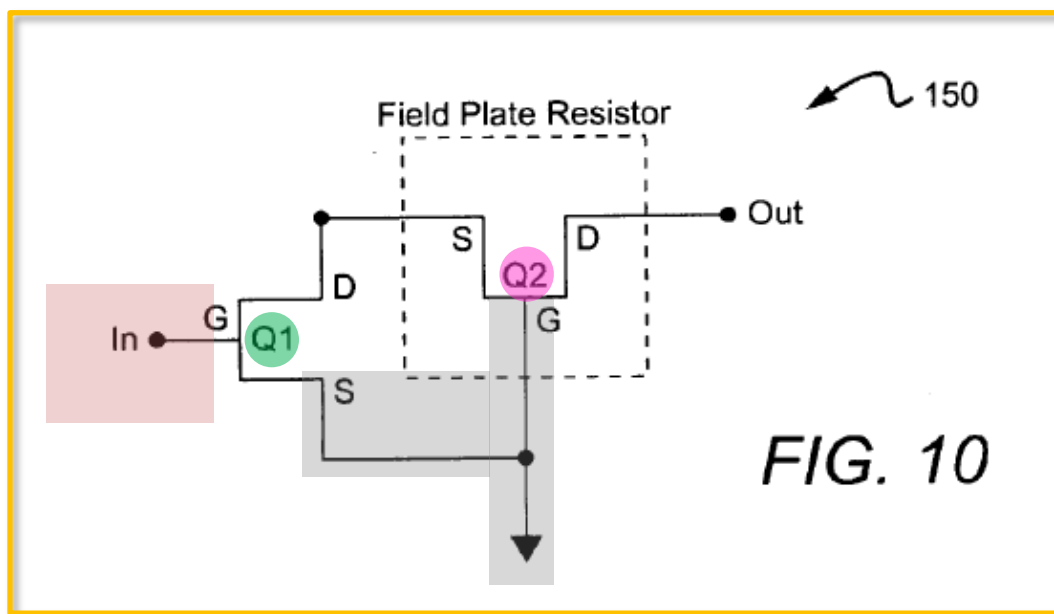
[291] Mishra-Ren's **second portion** identified above accordingly operates just like **second portion Q2** of the '003 patent: "[w]hen the **input voltage at V_{g1}** and provided to the **gate 22** of the bottom portion **Q1** (V_{g1}) goes low, the bottom portion **Q1** turns OFF and the bottom portion **Q2** stops conducting" because a voltage difference between the **ground** and a voltage at a **node** has been reached. '003 patent, 2:64-3:17.

10. [1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and

[292] Mishra in view of Ren renders obvious [1C8], wherein the **first portion** of the transistor is an enhancement mode transistor and the **second portion** of the transistor is a depletion mode transistor.

[293] A POSITA would have found it obvious to use Ren's simple techniques to make Mishra's first gate enhancement mode and second gate depletion mode. *See* § XIV.A (Motivation to Combine Mishra and Ren), above. As

I explained above, Mishra's **second gate** must be depletion mode because it is connected to ground and conducts. Mishra, ¶¶[0055]-[0056], [0058], Fig. 10; *see* § XIV.A (Motivation to Combine Mishra and Ren), above. In the Mishra-Ren combination, **Q2** remains in depletion mode. *See* § XIV.A (Motivation to Combine Mishra and Ren), above.



Mishra, Fig. 10 (annotated).

[294] In the Mishra-Ren combination, the first gate **Q1** in the cascode would be in enhancement mode, as Ren discloses. *See* § XIV.A (Motivation to Combine Mishra and Ren), above. A POSITA would have done so to achieve the benefits of “normally off” device, including reduced power consumption and suitability for high voltage and high frequency operations and to reduce gate leakage. *See*

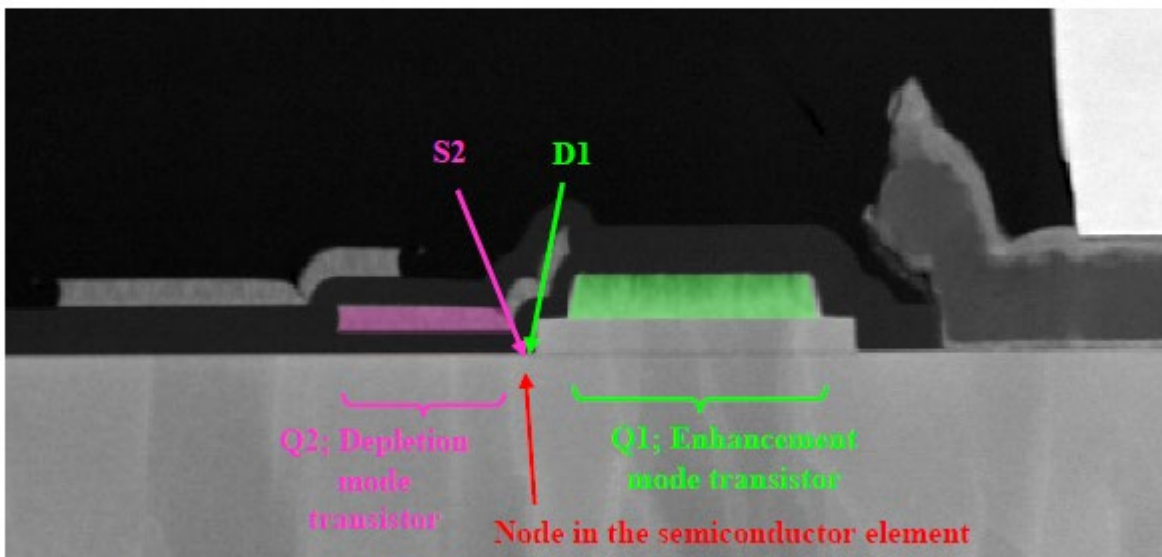
§ XIV.A (Motivation to Combine Mishra and Ren), above; Mishra, ¶¶[0011], [0055]-[0063], Ren, ¶¶[0005], [0040]; Beach, ¶¶[0005]-[0006].

11. [1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

[295] Mishra discloses [1C9], wherein a drain region of the **enhancement mode transistor** is **merged** with a source region of the **depletion mode transistor** at the **node** in the **semiconductor element**, under Infineon's apparent infringement theory. Ex-1011, 31.

The low side INN100W032A transistor in ISG3201 meets this limitation.

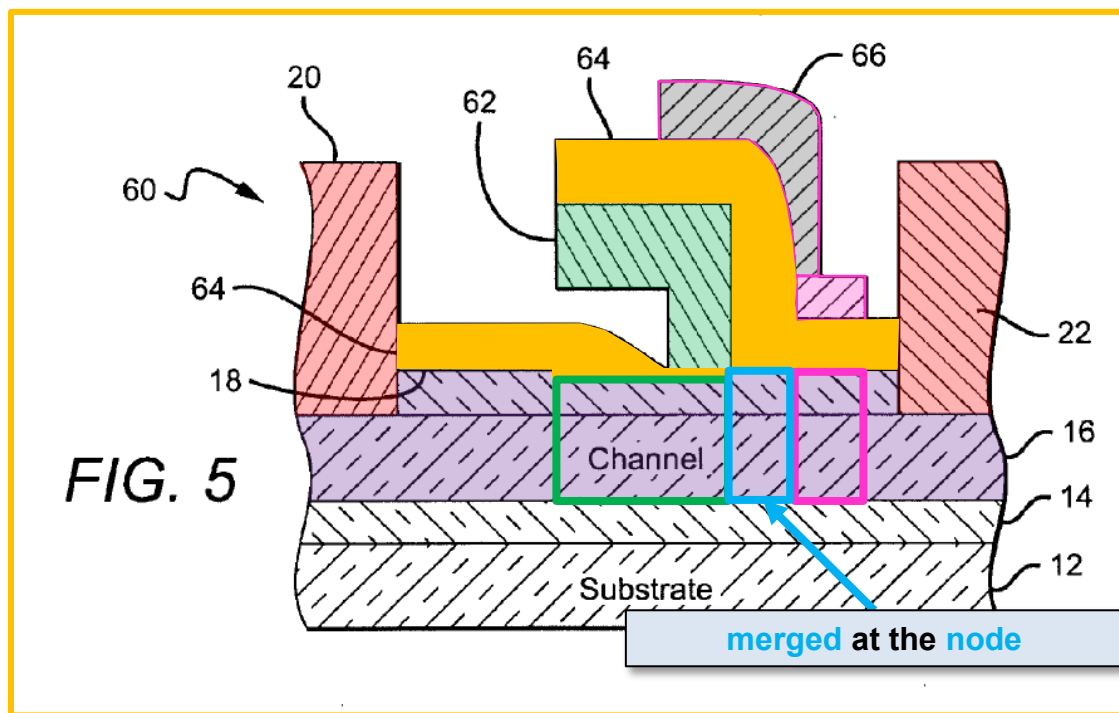
As shown in the cross-sectional view TEM image of INN100W032A, a drain region (denoted by "D1") of the enhancement mode transistor Q1 is merged with a source region (denoted by "S2") of the depletion mode transistor Q2 at the node in the semiconductor element.



(Cross-sectional view TEM image of INN100W032A, annotations added)

Ex-1011, 31.

[296] As shown below, Mishra includes a **merged** region on the drain side of **gate 62** and source side of **field plate 66**. Mishra, Fig. 5. The Mishra-Ren combination includes the same features, as shown below. *See* § XIV.A (Motivation to Combine Mishra and Ren), above.



Mishra, Fig. 5 (annotated, modified by Ren).

C. Claim 2

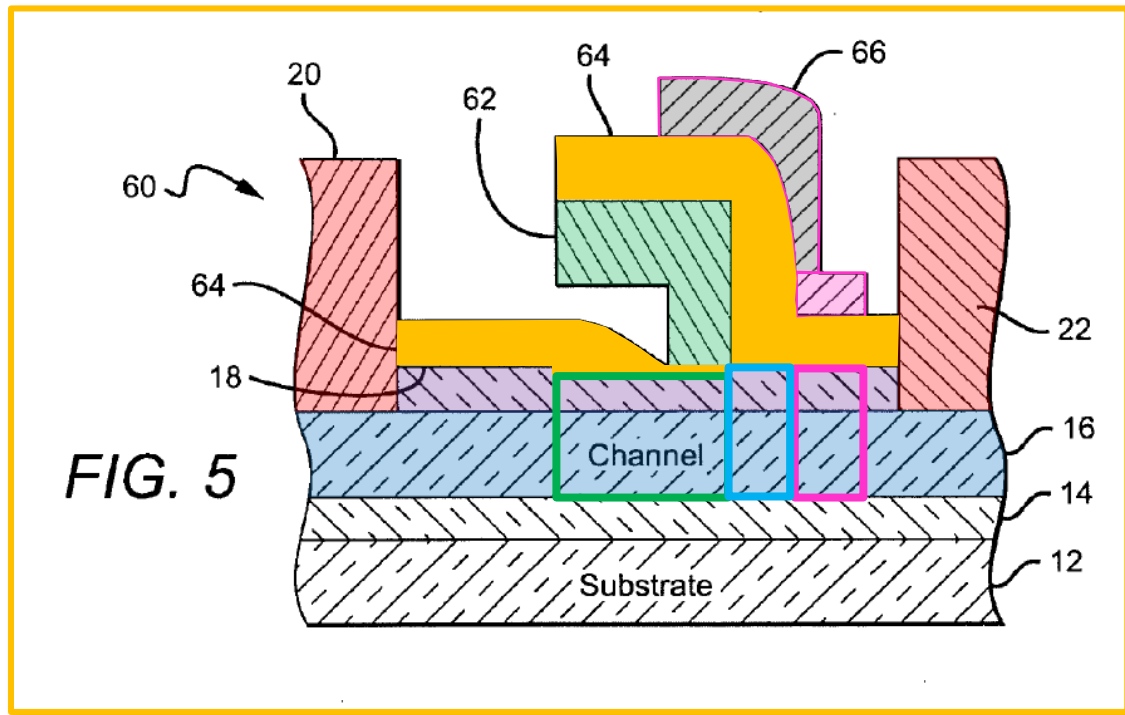
[297] Mishra in view of Ren renders obvious claim 2.

-
1. [2PRE] The merged cascode transistor of claim 1, wherein the semiconductor element further comprises: [2A] a first III-Nitride layer; and

[298] Mishra in view of Ren renders obvious [2PRE] and [2A], “[t]he merged cascode transistor of claim 1, wherein the semiconductor element further comprises: a first III-Nitride layer.”

[299] Mishra discloses barrier layer 18 in the semiconductor element, which is made from AlGa_N. Mishra, ¶¶[0033]-[0034]. Ren discloses the same. Ren, ¶¶[0003]-[0005], [0013]-[0014]. AlGa_N is a III-Nitride material. Mishra, ¶¶[0007]-[0010], [0033]-[0034], Fig. 5; Ren, ¶¶[0003]-[0005], [0013]-[0014]. The Mishra-Ren combination renders obvious a first III-Nitride layer in the semiconductor element.

[300] The Mishra-Ren combination includes the same features, as shown below. *See* § XIV.A (Motivation to Combine Mishra and Ren), above.



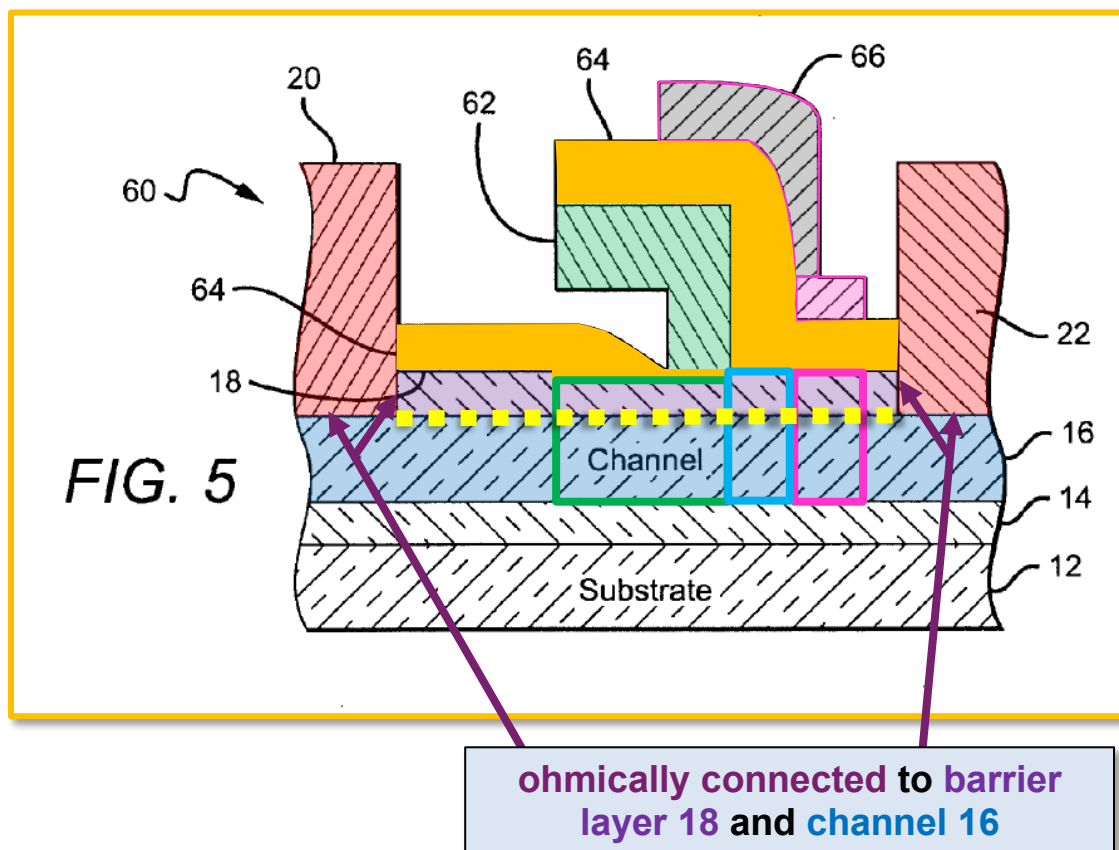
Mishra, Fig. 5 (annotated, modified by Ren).

2. [2B] a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

[301] Mishra in view of Ren renders obvious [2B], a **second III-Nitride** layer on which the first III-Nitride layer is positioned such that **a 2DEG conduction layer** forms between the **first** and **second III-Nitride** layers, wherein the **source** electrode and the **drain** electrode are **ohmically connected** to the **first III-nitride layer**.

[302] Mishra discloses an **GaN layer** below the **AlGaN layer**. Mishra, ¶¶[0007]-[0010], [0033]-[0034], Fig. 5. GaN is a III-Nitride material. Mishra,

¶¶[0007]-[0010], [0033]-[0034], Fig. 5; Ren, ¶¶[0003]-[0005], [0013]-[0014]. A **2DEG conduction layer** forms at the heterojunction of the **GaN layer** and **AlGaN layer**. Mishra, ¶[0037]. **Barrier layer 18** and the **channel 16** form the semiconductor element. The **source** electrode and the **drain** electrode are **ohmically connected** to **barrier layer 18** and the **channel** because they are in direct contact with those layers, and Mishra identifies the **source** and **drain** electrodes as **ohmic**. Mishra, ¶¶[0035], [0037], [0045].

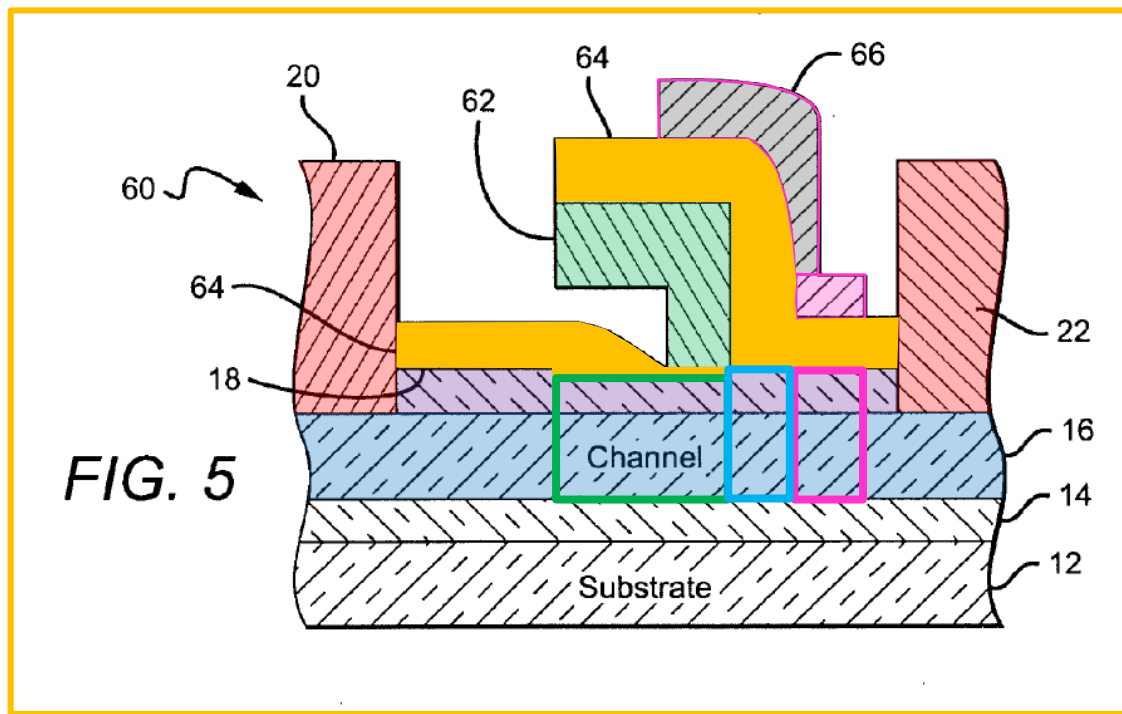


Mishra, Fig. 5 (annotated, modified by Ren).

- D. 3. The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.**

[303] Mishra in view of Ren renders obvious claim 3, the merged cascode transistor of claim 2, further comprising **an insulating layer** positioned between the **first** and **second gates** and the **first III-Nitride** layer such that the **first** and **second gates** are capacitively coupled to the first **III-Nitride layer**.

[304] The combination includes an **insulating layer** below both gates. *See* § XIV.A (Motivation to Combine Mishra and Ren), above. Ren describes using a “gate dielectric,” which is an **insulating layer**, below the gate metal contact of its gates. Ren, ¶¶[0015], [0026], [0030], [0036], [0039], [0041], Figs. 1-2. A POSITA would have understood this arrangement capacitively couples the gate to the underlying **AlGaN layer** because conductive materials are separated by an insulating gate dielectric layer such that there is capacitance between the gate and the AlGaN layer.



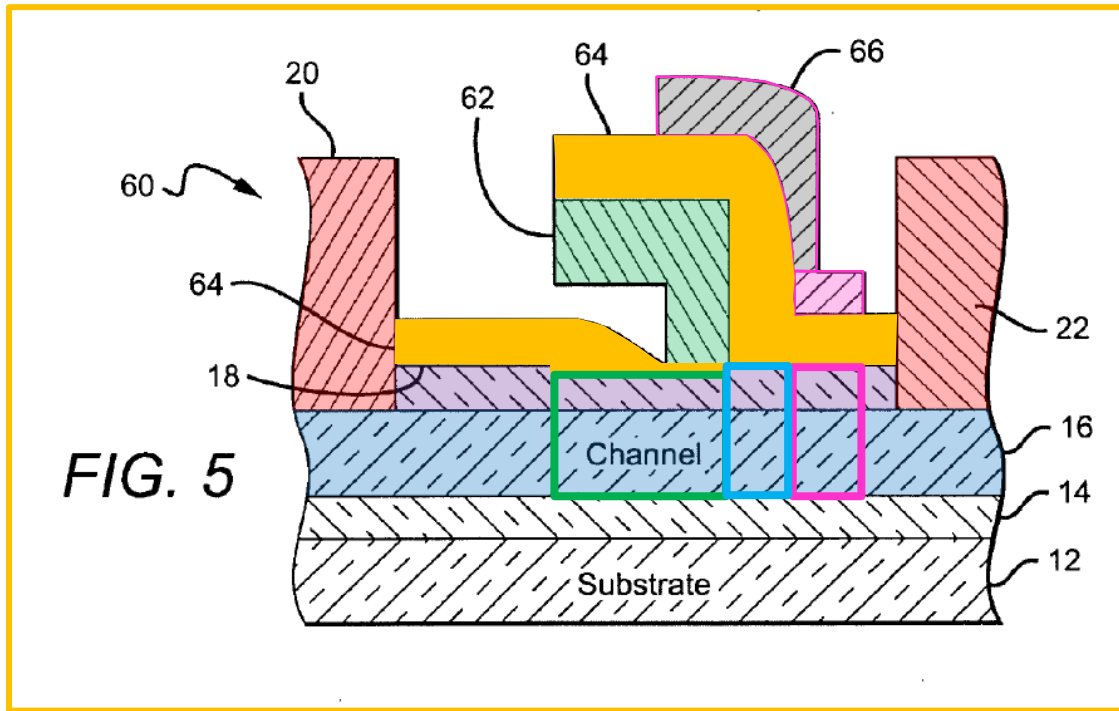
Mishra, Fig. 5 (annotated, modified by Ren).

E. 4. The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.

[305] Mishra in view of Ren renders obvious claim 4, the merged cascode transistor of claim 3, wherein the **first III-Nitride layer** comprises AlGaN material and the second **III-Nitride layer** comprises GaN material.

[306] Mishra discloses an **GaN layer** below the **AlGaN layer**. Mishra, ¶¶[0007]-[0010], [0033]-[0034], Fig. 5. AlGaN and GaN are III-Nitride materials. Mishra, ¶¶[0007]-[0010], [0033]-[0034], Fig. 5; Ren, ¶¶[0003]-[0005], [0013]-[0014].

[307] Ren also discloses an **AlGa**N over **GaN** epitaxial structure. Ren, ¶¶[0014], [0029], [0031].



Mishra, Fig. 5 (annotated, modified by Ren).

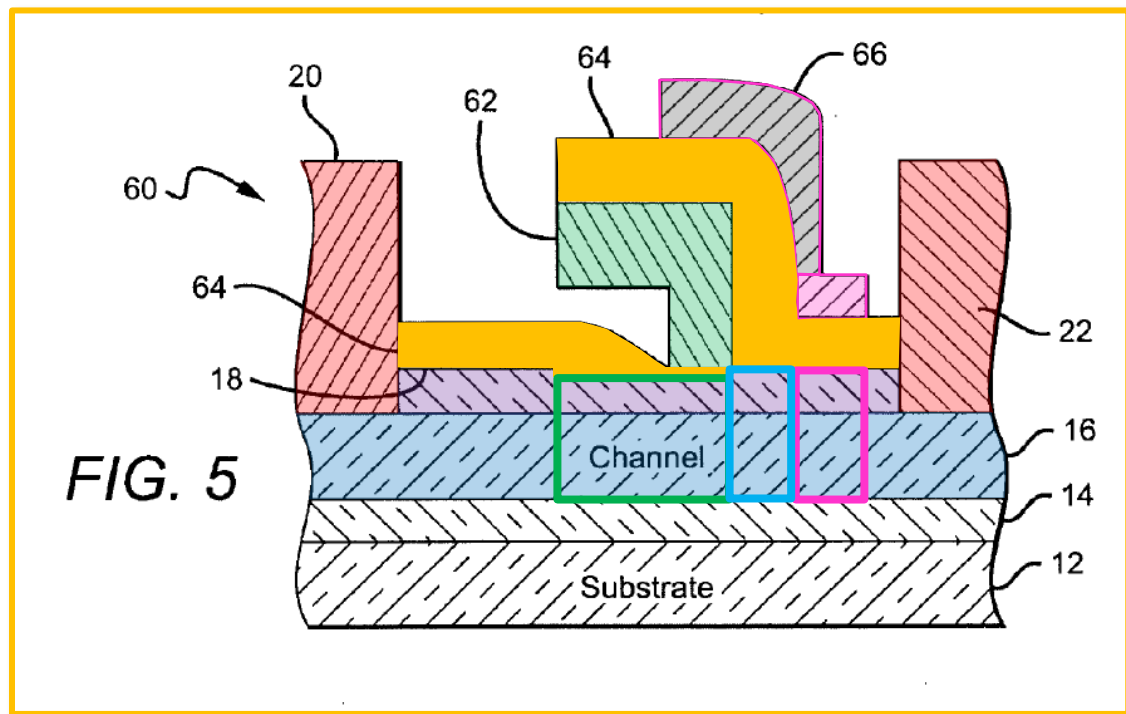
F. 5. The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.

[308] Claim 5, which depends from claim 4 (which depends from claim 3), recites the same limitations as claim 3. Mishra in view of Ren renders obvious claim 5 for the same reasons as for claim 3. *See* § XIV.D (Ground 3: claim 3), above.

G. 6. The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

[309] Mishra in view of Ren renders obvious claim 6, the merged cascode transistor of claim 5, wherein the **first portion** of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.

[310] As explained, the combination of Mishra and Ren uses Ren's GaN enhancement mode transistor for **gate 62**. See § XIV.A (Motivation to Combine Mishra and Ren), above. An enhancement mode transistor, by definition, is OFF at zero-volt input voltage and conducts (ON) when an input voltage is above a predetermined threshold, as Ren discloses. Ren, ¶¶[0008] (enhancement mode "require[s] a positive voltage to turn on"), [0012] (an enhancement MOSFET is characterized as a MOS device which forms a channel only when the gate to body (or source) voltage exceeds some threshold voltage"), [0038]-[0039]. Accordingly, the Mishra-Ren combination renders obvious claim 6.



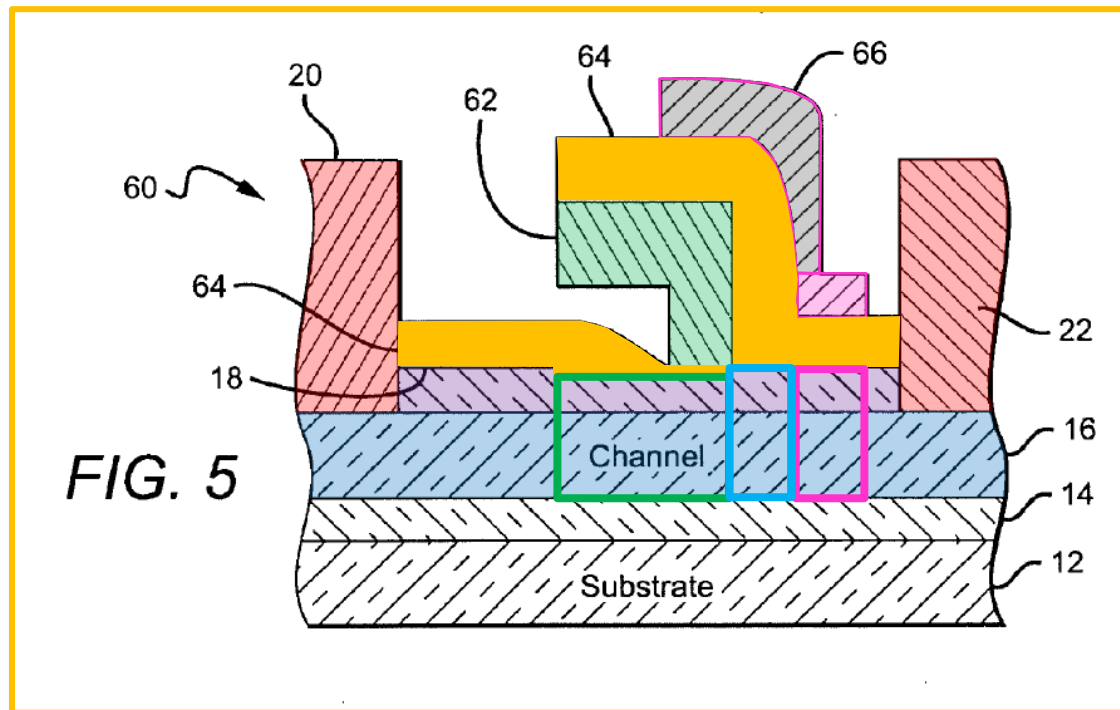
Mishra, Fig. 5 (annotated, modified by Ren).

H. 7. The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.

[311] Mishra in view of Ren renders obvious claim 7, the merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the **second portion of the transistor**.

[312] As explained for limitation [1C7], the **field plate 66** of the combination “conducts until” a saturation voltage of the depletion mode second gate is reached that results in a pinch-off of the conduction layer at which conductivity ceases. *See* §§ VII (Technological Background) (e.g., describing

pinch-off of cascodes with a first enhancement mode and second depletion mode gate, including simulation), above.XIV.B.9 (Ground 3: [1C7]),.



Mishra, Fig. 5 (annotated, modified by Ren).

I. 8. The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.

[313] Mishra in view of Ren renders obvious claim 8. Ren discloses using gate dielectric layers formed of silicon dioxide. Ren, ¶¶[0010], [0030].

J. 9. The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

[314] Mishra in view of Ren renders obvious claim 9. Ren discloses “[g]ate dielectric layer 115 can be *any suitable dielectric*, such as SiO₂, SiN_x, MgO or

SC₂O₃.” Ren, ¶[0030]. Thus, Ren discloses a gate dielectric formed of silicon dioxide (SiO₂) and a gate dielectric formed of silicon nitride (SiN_x), and a POSITA would have found it obvious that in combination they are also dielectric materials. A POSITA would have found it obvious that Ren’s “suitable dielectrics” include mixtures of materials Ren discloses, including a mixture of silicon dioxide and silicon nitride. A POSITA would have understood that such mixtures were common, especially for oxygen and nitrogen-based compounds, such that a mixture of SiN_x layer, which would have been silicon rich or mixed with oxides, such as SiO_xN_y (Silicon Oxy-Nitride), and silicon dioxide would have been obvious. Ren teaches such mixtures by including, for example, carbonated oxide (SiC₂O₃) as a suitable dielectric. Ren, ¶[0030]. As of the time of the ’003 patent, it was long known by a POSITA that these deposited insulators are often not stoichiometric, and it was routine to tailor mixtures of dielectrics for desired dielectric characteristics, including the permittivity, hardness, breakdown strength, conformal properties etc. *See* Bernstein-SiN (Ex-1023).

K. Claim 10

[315] Mishra in view of Ren renders obvious claim 10.

1. [10PRE] 10. A merged cascode high electron mobility transistor circuit comprises:

[316] Mishra discloses [10PRE]. As explained for [1PRE], the combination discloses a “merged cascode transistor circuit. *See* § XIV.B.1 (Ground 3: [1PRE]), above. Further, Mishra discloses its devices are high electron mobility transistors (HEMTs). Mishra, Abstract, ¶¶[0007]-[0010], [0027], [0042].

2. [10A] an input voltage signal source having an input voltage signal;

[317] Mishra discloses [10A] as explained for [1A]. *See* § XIV.B.2 (Ground 3: [1A]).

3. [10B] a constant voltage source having a predetermined constant voltage;

[318] Mishra discloses [10B] as explained for [1B]. *See* § XIV.B.3 (Ground 3: [1B]).

4. [10C] a merged cascode transistor comprising:

[319] Mishra discloses [10C] as explained for [1C]. *See* § XIV.B.4 (Ground 3: [1C]).

5. [10C1] a first epitaxial layer of III-Nitride material;

[320] Mishra renders obvious [10C1] as explained for [2PRE]-[2A]. *See* § XIV.C.1 (Ground 3: [2PRE]-[2A]). A POSITA would have understood Mishra’s

AlGa_N layer is an “epitaxial” layer. *See, e.g.*, Ren, ¶[0029] (describing “epitaxial stack” of AlGa_N and Ga_N layers).

6. **[10C2] a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;**

[321] Mishra discloses [10C2] as explained for [2B]. *See* § XIV.C.2

(Ground 3: [2B]), above. A POSITA would have understood Mishra’s Ga_N layer is an “epitaxial” layer. *See, e.g.*, Ren, ¶[0029] (describing “epitaxial stack” of AlGa_N and Ga_N layers).

7. **[10C3] a source electrode electrically connected to the first epitaxial layer; [10C4] a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;**

[322] Mishra discloses [10C3]-[10C4] as explained for [1C1]-[1C3]. *See*

§ XIV.B.5 (Ground 3: [1C1]-[1C3]), above.

8. **[10C5] a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and**

[323] Mishra discloses [10C5] as explained for [1C4]. *See* § XIV.B.6

(Ground 2: [1C4]), above.

9. **[10C6] a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode**

and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;

[324] Mishra discloses [10C6] under Infineon's apparent infringement theory, as explained for [1C5]. *See* § XIV.B.7 (Ground 3: [1C5]), above.

10. [10C7] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and

[325] Mishra renders obvious [10C7] as explained for [1C6]. *See* § XIV.B.8 (Ground 3: [1C6]), above.

11. [10C8] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,

[326] Mishra renders obvious [10C8] under Infineon's apparent infringement theory, as explained for [1C7]. *See* § XIV.B.9 (Ground 3: [1C7]), above.

12. [10C9] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and

[327] Mishra renders obvious [10C9] as explained for [1C8]. *See* § XIV.B.10 (Ground 3: [1C8]), above.

- 13. [10C10] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.**

[328] Mishra renders obvious [10C10] under Infineon's apparent infringement theory, as explained for [1C9]. *See* § XIV.B.11 (Ground 3: [1C9]), above.

- L. 11. The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.**

[329] Mishra in view of Ren renders obvious claim 11 as explained for claim 3. *See* § XIV.D (Ground 3: Claim 3), above.

- M. 12. The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGa_N material and the second epitaxial layer comprises a Ga_N material.**

[330] Mishra in view of Ren renders obvious claim 12 as explained for claim 4. *See* § XIV.E (Ground 3: Claim 4), above.

- N. 13. The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.**

[331] Mishra in view of Ren renders obvious claim 13 as explained for claim 6. *See* § XIV.G (Ground 3: Claim 6), above.

- O. 14. The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.**

[332] Mishra in view of Ren renders obvious claim 13 as explained for claim 7. *See* § XIV.H (Ground 3: Claim 7), above.

- P. 15. The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.**

[333] Mishra in view of Ren renders obvious claim 14 as explained for claim 8. *See* § XIV.I (Ground 3: Claim 8), above.

- Q. 16. The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.**

[334] Mishra in view of Ren obvious claim 16. Ren discloses “[g]ate dielectric layer 115 can be any suitable dielectric, such as SiO₂, SiN_x, MgO or SC₂O₃.” Ren, ¶[0030]. Thus, Ren discloses a gate dielectric formed of silicon nitride (SiN_x).

XV. CONCLUSION

[335] For the reasons set forth above, in my opinion, a person of ordinary skill in the art would have found claims 1-16 of the '003 patent obvious.

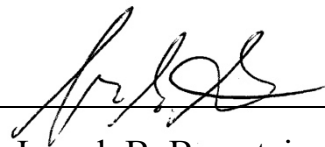
[336] In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be

subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

[337] I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: November 14, 2024

By: _____

A handwritten signature in black ink, appearing to read 'J.B. Bernstein', written over a horizontal line.

Joseph B. Bernstein, Ph.D.