

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

Case No. IPR2025-00094
Patent No. 8,264,003

PATENT OWNER'S PRELIMINARY RESPONSE

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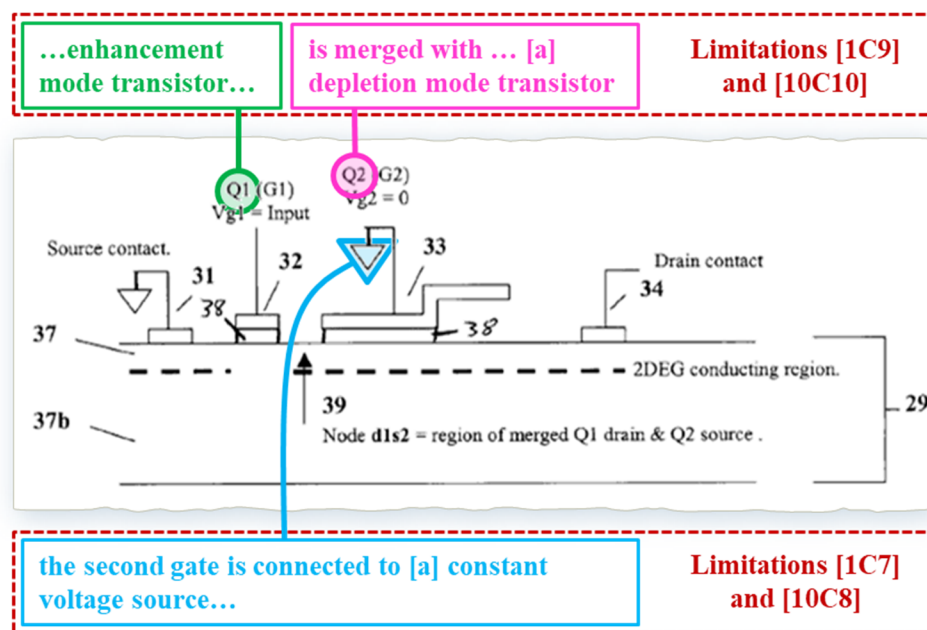
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Exhibit	Description
2001	Stewart, C.M., “Interim Processes for PTAB Workload Management,” Memorandum dated March 26, 2025
2002	Horowitz, P., & Hill, W. (1989). The Art of Electronics (2nd ed.). Cambridge University Press.
2003	Transcript Excerpt from Deposition of Thomas Herman dated January 17, 2025. <i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; ITC Inv. No. 337-TA-1414.

I. INTRODUCTION¹

The '003 patent is directed to a merged cascode transistor circuit that includes: (1) an enhancement mode transistor with a drain region that is merged with a source region of a depletion mode transistor (Limitations [1C9] and [10C10]); and (2) where the gate of the depletion mode transistor is connected to a constant voltage source (Limitations [1C7] and [10C8]), illustrated below.²

'003 Patent, Fig. 3 (annotated)



¹ PO will present its 314(a) positions supporting discretionary denial under separate cover to the Director pursuant to the *Interim Processes for PTAB Workload Management Memorandum* (“Memorandum”) issued on March 26, 2025. The deadline for filing that paper is April 26, 2025. Ex-2001.

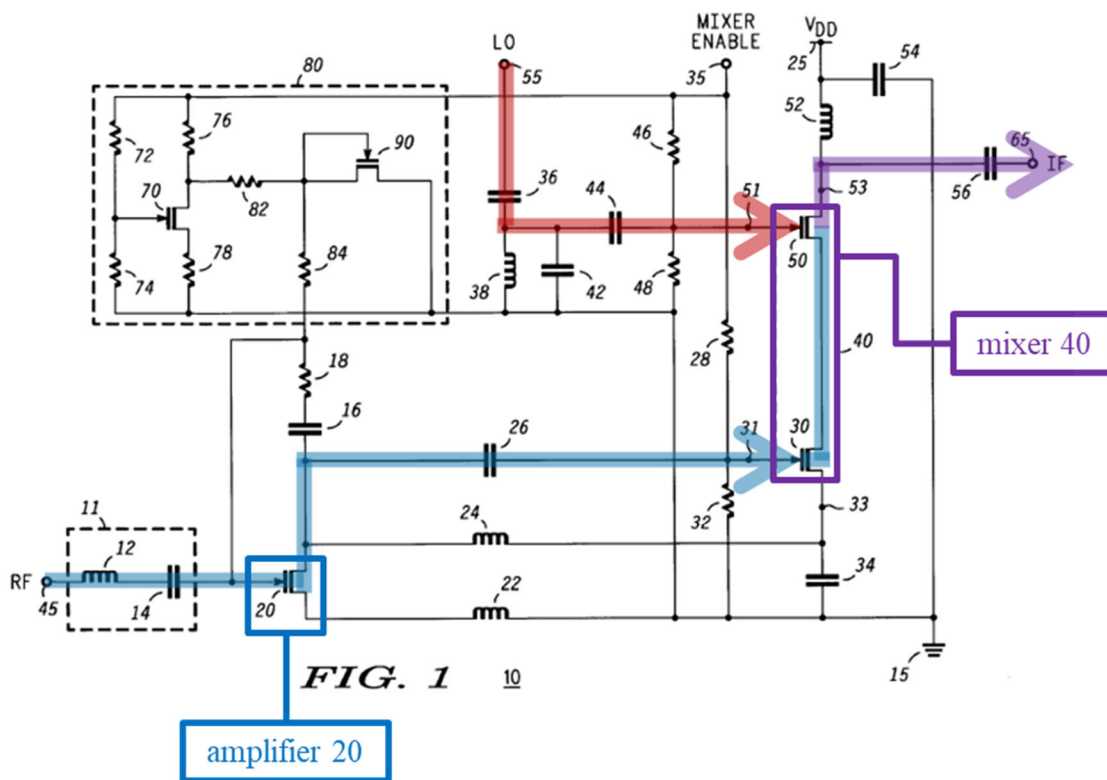
² Infineon adopts the Petition’s claim labels shown in the “Claim Appendix.”

The Petition's grounds fail to disclose or suggest at least one of those two limitations. The Petition alleges that the combination in each Ground would have nonetheless met the missing limitation(s), but the Petition fails.

A. Grounds 1 and 2 Fail Because Petitioner Proposes Rendering the Downconverter of Bonn Inoperable for its Intended Purpose

Ground 1 fails at least because neither Bonn, the primary reference, nor Mizuta, the secondary reference, discloses connecting the second gate of a dual-gate transistor to a constant voltage source as claimed by Limitation [1C7] (Ground 1 only challenges claim 1). Specifically, Bonn discloses a circuit 10 that comprises an amplifier 20 and a mixer 40. Bonn, Fig. 1 (below, annotated).

Bonn, Fig. 1 (Annotated)



While Bonn discloses that its mixer 40 can be a dual-gate transistor, both gates 30 and 50 are connected to *variable* voltage sources. Gate 30 is connected to an “**RF**” signal. Gate 50 is connected to an “**LO**” signal. The two signals are then mixed together to form an “**IF**” output signal. Bonn never discloses connecting either gate of its dual-gate transistor—let alone the second gate—to a *constant* voltage source as claimed in Limitation [1C7]. Indeed, this is for good reason as using a constant voltage source in Bonn (as proposed in the Petition) would defeat the purpose of mixing the **RF** and **LO** signals together in Bonn’s downconverter (Fig. 1, above).

While Bonn states that its dual-gate transistor can be “tailored” for use in “other applications such as high frequency signal amplification” (Bonn, 11:34-37), this sentence, in context, is referencing transistor properties (gate width, dopant concentration, etc.). *Id.*, 11:32-34. Bonn is not teaching “tailor[ing]” the circuit of Fig. 1 transform a downconverter into an amplifier, but that is exactly what Petitioner did.

The starting point of the Petition ground is Bonn’s Figure 1 (Petition, 22), which is a downconverter that already includes an amplifier. The Petition thus ignores the operation and stated goals of Bonn and argues—through the naked say-so of its expert—that POSAs would have stripped away (Petition, 23-25) most of the circuit including:

- Amplifier 20 (and associated circuitry)

- Voltage source 80 (and associated circuitry)
- Capacitors 16, 26, and 34
- Resistors 22, 24, 46 and 48
- LO Circuit port
- LO Circuit

In proposing this extensive “tailoring,” Petitioner plainly admits that the LO signal is no “longer needed” because mixing is removed from the modified circuit of Fig.1, but downconverting is the basic operating principle of the circuitry in Figure 1. *In re Ratti*, 270 F.2d 810, 813 (C.C.P.A. 1959) (finding a combination of art “not a proper ground for rejection of the claims” because it “would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as *a change in the basic principles under which the [the primary reference] construction was designed to operate.*”). As can be appreciated, Petitioner’s make-it-up-as-you-go “tailoring” is driven only by the goal of meeting the ’003 patent’s claims. No other rationale is offered for removing the overwhelming majority of circuit components of Fig. 1’s downconverter circuit, destroying its basic operating principle.

No articulable rationale is offered for removing the mixer and its necessary oscillator circuitry to create a newly configured amplifier. No articulable rationale is offered for configuring a new amplifier rather than modifying the existing

amplifier 20 of Fig. 1 (now removed). No articulable rationale is offered for changing the RF frequency and LO frequency input of Fig. 1 to a single high-frequency input—nothing but pure hindsight reconstruction. The proposed modification to the downconverter circuit of Fig. 1 is facially and technically absurd in all respects and does great violence to the circuit of Fig.1 in the name of “tailoring.” The law of obviousness does not support such hindsight “tailoring.”

Bonn’s mixer and amplifier serve critical roles in the design of the downconverter shown in Figure 1. The mixer combines two signals and the amplifier increases the strength of a single signal. Modifying Bonn’s Figure 1 downconverter to make it into an amplifier would have destroyed the downconverter’s operating principle, rendering it inoperable for its intended purpose.

The Federal Circuit has repeatedly held that a modification that would have rendered the primary reference “*inoperable for its intended purpose*” is not one a POSA would have made. *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984); *see also Trivasular v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (affirming the Board’s finding that a POSA would not have replaced barbs in a primary reference with gripping protuberances from a secondary reference because the modification “would *destroy the basic objective* of the barbs, which is to penetrate surrounding tissue”); *Medtronic v. Teleflex Innovations*, 69 F.4th 1341, 1349 (Fed. Cir. 2023)

(“[A] proposed modification’s *destruction of a device’s primary purpose is ... at odds with common sense and gives in to the very hindsight bias the obviousness inquiry is designed to avoid.*”); *In re Ratti*, 270 F.2d at 813 (a combination does not render a claim obvious when it would have changed the “basic principles” under which the primary reference “was designed to operate”). The Petition fails to establish that a POSA would have changed Bonn’s Fig. 1 circuitry so much as to destroy the operating principle of Bonn’s downconverter of Figure 1, not only rendering it inoperable for its intended purpose, but rendering it completely unrecognizable, and thus fails to establish that the Bonn-Mizuta Combination would have met Limitation [1C7].

Ground 2 relies on two different secondary references but the Petition cites neither in arguing that a POSA would have modified Bonn in the same way as alleged in Ground 1 (repurposing Bonn’s downconverter as an amplifier). Instead, the Petition merely cross-references its prior hindsight-biased analysis from Ground 1. Ground 2 thus fails for at least the same reasons as Ground 1.

B. Ground 3 Fails Because the Cited Art Fails to Disclose an Enhancement Mode Transistor Merged with a Depletion Mode Transistor—the Very Feature the Examiner Found Missing from the Art During Prosecution

Ground 3 fails because neither Mishra, the primary reference, nor Ren, the secondary reference, discloses an enhancement mode transistor with a drain region that is merged with a source region of a depletion mode transistor as claimed by

Limitations [1C9] and [10C10]. Ren lacks any disclosure of a dual-gate transistor and thus fails to disclose the claimed merged region for that reason. While Mishra discloses the notion of a hypothetical dual-gate structure, Mishra provides no details whatsoever of its structure or how it would operate. Even the Petition admits that “Mishra does not explicitly comment on the mode in which [Mishra’s first transistor] Q1 operates.” Petition, 83. Thus, neither Mishra nor Ren discloses Limitations [1C9] and [10C10]—the very limitation that the Petition admits the Examiner found lacking in the prior art during prosecution (*id.*, 11).

Without art that teaches all claimed limitations, the Petition instead relies on the say-so of Petitioner’s expert to supply the missing limitation through an obviousness combination. The Federal Circuit has repeatedly held that for expert testimony to supply a limitation missing from the prior art, “the limitation in question [must be] unusually simple and the technology particularly straightforward.” *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016). The Petition failed, however, to make either showing. The Board routinely denies institution under these circumstances and should do so here too.

II. GROUND 1 FAILS BECAUSE IT FAILS TO ESTABLISH THE BONN-MIZUTO COMBINATION WOULD MEET LIMITATION [1C7]

Ground 1 challenges only claim 1 as allegedly obvious over Bonn (Ex-1006) in view of Mizuto (Ex-1007).³ Petition, 6. But Ground 1 fails because the Petition fails to establish that the Bonn-Mizuto Combination would have met Limitation [1C7].

Claim 1 requires, in part, “the second gate is connected to the constant voltage source” (*see* Limitation [1C7]). The Petition cites only Bonn as allegedly disclosing this limitation (Petition, 40-45), but Bonn discloses connecting both gates of its dual-gate transistor to *variable* voltage sources. To account for this stark inconsistency, the Petition instead relies entirely on the testimony of its expert to supply this missing limitation through a series of modifications that strip out extensive and critical aspects of Bonn’s circuitry. But Bonn explains no such modifications. Petitioner’s modifications, unsupported by any objective evidence, is classic hindsight. The Board routinely denies institution under such circumstances.

³ The first-named inventor of U.S. Patent No. 6,483,135 is Mizuta^a, but this POPR will refer to it as “Mizuto^o” as the Petition does.

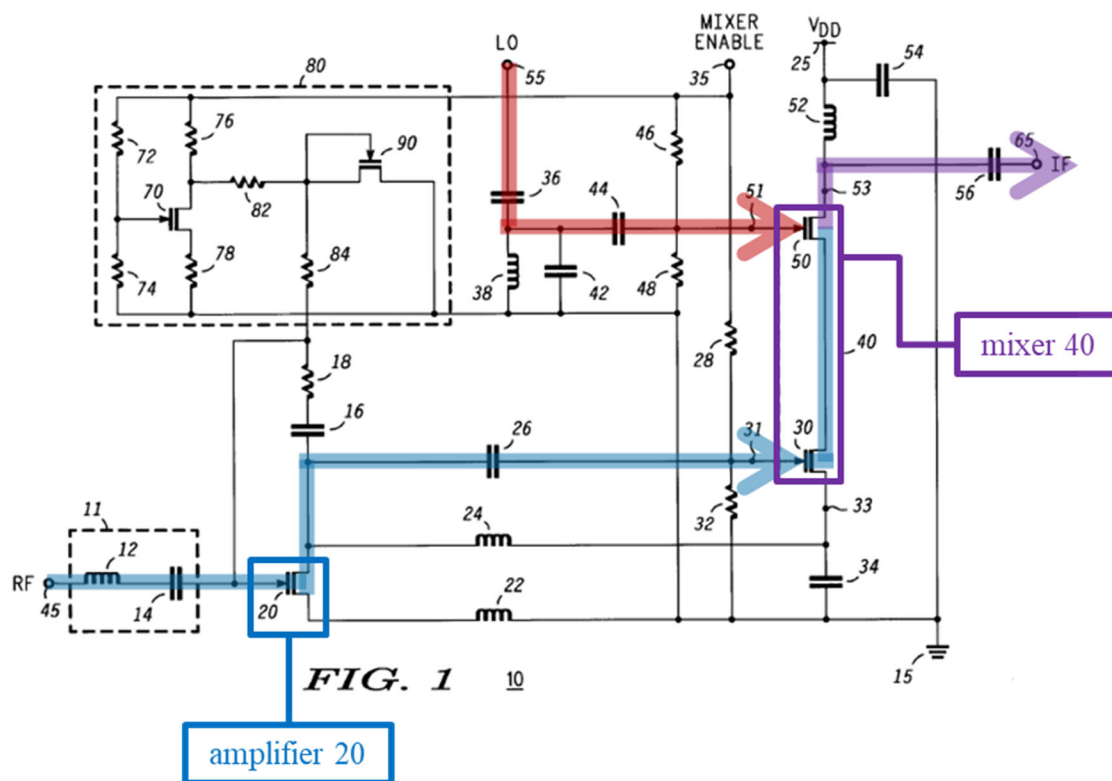
But even if Petitioner's expert testimony was considered, it would not establish that a POSA would have arrived at the missing limitation because the proposed modifications to Bonn's downconverter of Figure 1 would have destroyed its operating principle, rendering it inoperable for its intended purpose. The Federal Circuit has repeatedly held that a proposed modification that renders a primary reference inoperable for its intended purpose is not a modification that a POSA would have made. The Petition thus fails to establish that a POSA would have changed the operating principle of Bonn's downconverter circuitry, rendering it useless for its intended purpose for no apparent articulable rationale other than to meet the claims of the '003 patent.

A. Bonn Fails to Disclose a Second Gate Connected to a Constant Voltage Source (Limitation [1C7])

While the Petition alleges that Bonn discloses connecting the second gate of a dual-gate transistor to a constant voltage source as claimed by Limitation [1C7], the Petition cites no evidence to support that statement. Petition, 40-45. Indeed, Bonn does not disclose connecting the second gate of a dual-gate transistor to a constant voltage source as claimed by Limitation [1C7].

Bonn discloses a downconverter (10) with single-gate FET amplifier (20) connected to mixer (40), where mixer (40) is made up of two single-gate transistors. Bonn, 2:8-14, 2:66-3:12, Fig. 1 (annotated below).

Bonn, Fig. 1 (Annotated)



Bonn shows that the gate of amplifier 20 and the gates of both transistors in mixer 40 are driven gates—none of them are connected to a constant voltage source because doing so would have rendered mixer 40 inoperable (as explicitly proposed by Petitioner). As annotated in Bonn’s Fig. 1, above, the gate of amplifier FET 20 is connected to a variable voltage signal source (the RF signal on port 45) and a bias voltage supplied from power supply 80. *Id.*, 2:14-17 (“A gate electrode of FET 20 is coupled for receiving the RF signal at an RF port 45 via serially coupled inductor 12 and capacitor 14.”), 2:39-40 (“the gate electrode of FET 20 is [also] coupled to a voltage source 80”).

The gates in mixer 40 are also connected to variable voltage signal sources. The gate of FET 30 is connected to a variable voltage source (the amplified RF signal from amplifier FET 20) and biased through resistors 28 and 32. *Id.*, 3:22-29, Fig. 1. The gate of FET 50 is connected to a variable voltage source (the LO signal supplied through port 55) and biased through resistors 46 and 48. *Id.*, 3:31-40, Fig. 1. Bonn thus fails to disclose the claimed merged cascode transistor with the second gate connected to a constant voltage source.

While the Petition alleges that “Bonn discloses [1C7]” and “the second gate is connected to the constant voltage source,” the Petition cites nothing in Bonn that discloses that requirement. Petition, 40. The Petition cites its expert, Dr. Bernstein, [142]-[149] (*id.*), but those paragraphs of the Bernstein declaration cite nowhere in Bonn that discloses the second gate is connected to the constant voltage source either. Both the Petition’s and Dr. Bernstein’s conclusion that Bonn discloses the second gate is connected to the constant voltage source is simply unsupported. As explained above, Bonn provides no disclosure of connecting the second gate to a constant voltage source—both gates of mixer 40 are connected to variable voltage sources as such is necessary to enable mixing.

B. A POSA Looking to Modify Bonn Based on Mizuta Would Not Have Arrived at a Circuit Meeting Limitation [1C7]

The Petition alleges that a POSA would have modified Bonn by adding Mizuta’s field plate to Bonn’s second gate electrode. Petition, 26-28. But even if

Mizuta’s field plate were added to Bonn’s dual-gate transistor, that would still fail to disclose connecting the second gate of a merged cascode transistor to a constant voltage source as claimed—a feature absent from Bonn. Thus, the Petition’s proposed modification of Bonn based on Mizuta would fail to meet claim 1.

C. The Board Routinely Denies Institution when the Petition’s Grounds Rely on Prior Art with Missing Claimed Features

Unable to find a single prior art reference that connects the second gate of a dual-gate transistor to a constant voltage source, the Petition seeks to reconstruct that limitation in hindsight by using expert testimony to fill in the missing limitation. Petition, 22-25. Federal Circuit precedent, however, establishes that expert testimony can only be used to supply a limitation missing from the art if “the limitation in question [is] unusually simple and the technology particularly straightforward.” *Arendi*, 832 F.3d at 1362; *see also DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018) (“we have invoked common sense to fill in a *missing* limitation only when the limitation in question was unusually simple and the technology particularly straightforward.”) (internal quotes and citations omitted).

Petitioner did not even attempt to make that requisite showing. Petition, 22-25. The Board routinely denies institution where the petitioner seeks to meet a missing limitation based solely on expert testimony. *See e.g., Xerox* at 14-16 (precedential); *Apple v. Mullen Indus.*, IPR2023-00087, Paper 10, 19-20 (May 3,

2023) (“*Apple*”); *Microsoft Corp. et al. v. LiTL*, IPR2024-00458, Paper 17, 17-21 (Aug. 23, 2024).

1. Petitioner Relies on Expert Testimony to Supply a Missing Limitation

Petitioner alleges that POSAs would have modified Bonn’s downconverter in Figure 1 to “use Figure 7’s structure for high frequency signal amplification in place of mixer 40.” Petition, 22. The Petition then steps through a series of extensive modifications to Bonn’s downconverter in Figure 1 in order to reconfigure Bonn’s mixer 40 into an amplifier. *Id.* The Petition cites Bonn for its disclosure of the functions of the various components of its circuitry that the Petition removes, but, critically, Bonn nowhere suggests such modifications.

For example, the Petition alleges that “a POSITA would have removed Figure 1’s LO (local oscillator) port 55 and associated impedance matching components because the LO signal is no longer mixed.” Petition, 23, citing Bernstein, [098]; Bonn, 3:30-41. But the cited portion of Bonn (3:30-41) discloses how the “[s]econd gate terminal 51 is coupled to the power supply” and to a “second electrode capacitor 44,” which in turn, “is coupled to an LO port 55 ... for receiving an LO signal.” Bonn, 3:30-41. If that was removed, as the Petition suggests, then Bonn’s downconverter would become inoperable because it would no longer be able to mix the RF and LO signals together as Bonn discloses is the purpose of its downconverter.

Paragraph [098] of the Bernstein declaration cites the same portion of Bonn and thus fails to cite any objective evidence that a POSA would have ripped out Bonn's LO port and associated impedance matching components. Bernstein's unsupported conclusory testimony warrants no weight under the Board's precedential *Xerox* decision. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) ("*Xerox*") (presidential) ("the cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight. *See* 37 C.F.R. § 42.65(a) ('Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.')

Moreover, the Bernstein declaration is almost word-for-word the same as the Petition apart from Bernstein quoting Bonn whereas the Petition does not. *Compare* Petition, 23, *with* Bernstein, [098]. Not only does Bernstein's testimony have the same shortcomings as the Petition for the reasons explained above, but the Board routinely denies institution to petitions that are supported by little more than experts who merely repeat the conclusions articulated in the petition. *See e.g. Tesla v. Nikola*, IPR2019-01646, Paper 7, 19 (PTAB Mar. 27, 2020) (denying institution, holding "Mr. Baker's testimony simply repeats the conclusions articulated in the Petition" which "is entitled to little or no weight."); *One World Techs. v. Chervon*, IPR2020-00885, Paper 21, 29 (PTAB Nov. 6, 2020) (similar); *Fitbit v. Koninklijke*

Philips, IPR2020-00774, Paper 13, 25 (PTAB Oct. 16, 2020) (similar); *Micro-Tech (Nanjing) v. Bos. Sci. Scimed.*, IPR2020-00185, Paper 11, 19-20 (PTAB May 4, 2020) (similar); *Initiative for Med., Access & Knowledge (I-Mak) v. Gilead Pharmasset*, IPR2018-00122, Paper 10, 21 (PTAB May 21, 2018) (similar).

The Petition continues its piecewise “tailoring” of Bonn’s downconverter based on nothing more than Bonn’s disclosure of the function of the circuitry and then Bernstein’s testimony that a POSA would have removed it, without any citation to corroborating evidence. Petition, 23-25. This is a blatant hindsight reconstruction of the claims that attempts to meet a claim limitation missing from the art solely with expert testimony. As explained in the next section, the Federal Circuit has made clear that it is a rare case where a missing limitation can be met by expert testimony alone, and Petitioner failed to establish the factual predicate needed to do so.

2. Expert Testimony Can Supply a Missing Limitation Only in Rare Circumstances Not Present Here

The Federal Circuit has repeatedly held that for expert testimony to supply a limitation missing from the prior art, “the limitation in question [must be] unusually simple and the technology particularly straightforward.” *Arendi*, 832 F.3d at 1362; *see also DSS Tech.*, 885 F.3d at 1374 (“we have invoked common sense to fill in a *missing* limitation only when the limitation in question was

unusually simple and the technology particularly straightforward.”) (internal quotes and citations omitted).

In *Arendi*, the Federal Circuit reversed the Board’s finding of obviousness when not all limitations were disclosed by the prior art. 832 F.3d at 1366. The claimed technology related to a method of identifying duplicate entries in a database and the prior art disclosed a computerized address book. *Id.* at 1358-59. The Board reasoned that “it would have been obvious to ... search for duplicate telephone entries when entering a telephone number in an electronic address book.” *Id.* at 1360. The Federal Circuit disagreed, noting that the prior art reference did “not mention or imply that a search of any kind is involved with the ‘Add to address book’ function.” *Id.* at 1363. The “only documentary support the Board recited was the declaration of ... Appellees’ expert.” *Id.* at 1364. The Federal Circuit found that the Board erred by relying on “conclusory statements and unspecific expert testimony regarding searches in general,” which was “particularly problematic considering the fact that a key limitation of the [patent – identifying duplicate entries –] was missing from the prior art.” *Id.* at 1366.

In *DSS Tech.*, the Federal Circuit again reversed the Board’s finding of obviousness when not all limitations were disclosed by the prior art. 885 F.3d at 1375. The claimed technology related to a communication network with a single base station and multiple peripheral devices, where each was “energized in low

duty cycle RF bursts” intermittently. *Id.* at 1369-70. The prior art taught **peripheral devices** that operated in this manner, but **not the base station**. *Id.* at 1373. The Board found that it would have been obvious “to have the base station operate in an analogous manner” to the peripheral devices. *Id.* The Federal Circuit disagreed because the limitation at issue was “not ‘unusually simple,’ and the technology is not ‘particularly straightforward.’” *Id.* at 1375 (quoting *Arendi*).

The Federal Circuit has only sanctioned supplying a missing limitation through expert testimony in the rare circumstance where the prior art discloses every claimed element, but not the **repetition** of a known prior art element as required by a claim. For example, in *B/E Aerospace*, the Federal Circuit found that the claimed technology (“lavatory enclosures”) was not complex and that the claimed “second recess” simply involved “**repetition** of an existing element” (a disclosed first recess), and thus was obvious despite the prior art not having two recesses. *B/E Aerospace, Inc. v. C&D Zodiac, Inc.*, 962 F.3d 1373, 1380 (Fed. Cir. 2020). Another oft-cited example is *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324 (Fed. Cir. 2009). The Federal Circuit has characterized *Perfect Web* as a case where the patented invention related to a 3-step process of sending marketing emails where the “missing claim limitation” “was nothing more than an instruction to **repeat** [the three] steps A, B, and C until a particular quantity of email was sent in accordance with the claim.” *Arendi*, 832 F.3d at 1362. The Federal Circuit has

made clear that “the facts in *Perfect Web* ... *ought to be treated as the exception, rather than the rule.*” *Id.*

3. The Board Routinely Denies Institution Where Petitioner Fails to Justify Reliance on Expert Testimony to Supply a Missing Limitation

The Petition does not even attempt to establish that Petitioner’s reliance on expert testimony to supply a limitation missing from the cited prior art is consistent with Federal Circuit precedent. That is reason enough to deny institution.

Xerox involved a “mobile ticketing system for detecting fraudulent activity” and the claimed method required a step of “stor[ing] in a data record associated with the account a data value indicating the fraudulent activity.” *Xerox*, IPR2022-00624, Paper 9, 6. While the prior art (“Terrell”) taught that “the purchaser of the ticket could be blocked from further use of the system,” the petitioner did not allege that Terrell disclosed storing a data value indicating the fraudulent activity as claimed. *Id.*, 14. Instead, petitioner alleged that POSAs “‘would find it obvious’ that ‘blocking the account of the purchaser’ would includ[e] ‘storing a data value indicating the fraudulent activity in a data record associated with the user account.’” *Id.* But “[p]etitioner’s only evidence in support of its assertion ... [was] the opinion of its Declarant, Dr. Jones.” *Id.* at 15.

In denying institution, the Board not only found that Dr. Jones failed to adequately support his opinions, but that petitioner ran afoul of the principles

articulated in the Federal Circuit’s *Arendi* decision. *Id.* at 16. The Board noted that “[p]etitioner has not alleged” that “the limitation in question [is] unusually simple and the technology particularly straightforward,” “much less provided support for such an allegation.” *Id.* (quoting *Arendi*).

The Board reached a similar result in the more recent *Apple* decision. IPR2023-00087, Paper 10, 19-20. That case involved “systems and methods for determining a device’s location” (*id.*, 3) and the claims required the “device to display indicia of two locations other than its own” (*id.*, 15). The prior art (“Sheha”) disclosed “displaying the location of a caller and a called device on a screen, but [did] not disclose displaying multiple locations of other users.” *Id.*, 17. Petitioner alleged “it would have been obvious to display the locations of second and third devices simultaneously.” *Id.* Petitioner’s only evidence was “the opinion of its Declarant, Mr. Williams.” *Id.*, 17-18.

In addition to finding that Mr. Williams failed to adequately support his opinions (*id.*, 18), the Board found that petitioner ran afoul of the principles articulated in *Arendi*. *Id.*, 19. The Board noted that “[p]etitioner has not alleged” that “the limitation in question [is] unusually simple and the technology particularly straightforward,” “much less provided support for such an allegation” (*id.*, 19-20). The Board denied institution at least in part on that basis. *Id.* (quoting *Arendi*).

Just like the petitioners in *Xerox* and *Apple*, Petitioner did not even allege that the missing claimed limitation of connecting the second gate of a merged cascode transistor to a constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level is unusually simple or that the claimed technology is particularly straightforward. Neither is true.

Petitioner's failure to establish that this is one of the rare exceptions to the rule forbidding reliance on expert testimony alone to meet a claim limitation missing from the prior art is reason enough to deny institution.

D. The Petition Fails to Establish a POSA Would Have Modified Bonn's Downconverter to Configure a New Amplifier and Remove the Existing Amplifier

Even if Petitioner's hindsight reconstruction of the claimed requirement of connecting the second gate of a dual-gate transistor was considered, it would not establish that a POSA would have arrived at the missing limitation. Establishing obviousness over a combination of references requires establishing some non-hindsight *reason why* POSAs would have combined the teachings in the art in the manner claimed. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017). Petitioner's assertion that POSAs would have modified Bonn's

downconverter to turn it into an amplifier in a way that meets claim 1 is hindsight, unsupported by any credible evidence. First, the Petition fails to show that a POSA would have used Bonn's dual-gate transistor in Figure 7 as an amplifier in the first place because it was purpose-built as a mixer, not an amplifier. Second, the Petition fails to show that a POSA would have modified Bonn's circuitry in the way suggested by the Petition because it would have rendered Bonn's downconverter of Figure 1 inoperable for its intended purpose. Third, even if a POSA was motivated to use Bonn's dual-gate transistor as an amplifier, the Petition fails to show that a POSA would have connected its second gate to a constant voltage source as required by claim 1 of the '003 patent—Bonn discloses connecting both gates to variable voltage sources (*see* § II.A, *supra*).

1. The Petition Fails to Establish a POSA Would Have Used Bonn's Dual-Gate of Figure 7 as an Amplifier

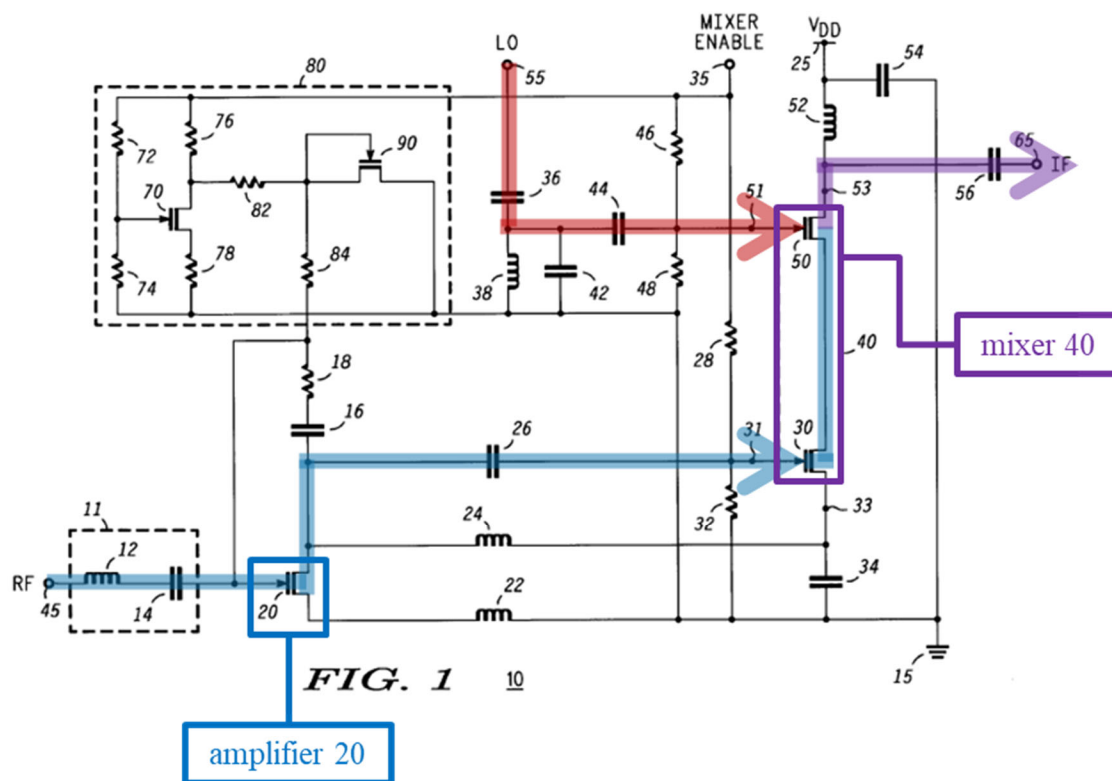
The Petition argues that “a POSA would have “use[d] Figure 7's structure for high frequency signal amplification in place of mixer 40.” Petition, 22. But the Petition cites no credible evidence to support that conclusion. In particular, the Petition fails to account for the fact that Bonn's transistor of Figure 7 is purpose-built as a mixer. Its unequal current carrying capacities ensure that the first signal applied to the first gate does not saturate (overload) the transistor when the second signal is applied to the second gate. While such a feature is beneficial to a mixer, it is detrimental for an amplifier, where the entire current from one signal must pass

beneath both gates. Bonn teaches that the structure of its dual-gate transistor “can be tailored” for other applications such as “high frequency amplification.” Bonn, 11:34-37. But the Petition fails to suggest any modifications to the transistor structure itself. Petition, 22. Instead, the Petition attempts to cite Bonn’s teaching of “tailoring” the *transistor* as a license to destroy the operating principle of Bonn’s *downconverter*. Regardless, the Petition’s asserted combination uses Bonn’s transistor unmodified and fails to address that a POSA would not have selected Bonn’s Figure 7 structure as an amplifier in the first place because it was tailor-made for use as a mixer.

a. Bonn’s Figure 7 Structure Has Unequal Current-Carrying Capacities Under Each Gate Purpose-Built for Mixing Applications

In Bonn’s downconverter 10, the mixer portion of the downconverter “combines a radio frequency (RF) signal” (shown in blue) “and a local oscillator (LO) signal” (shown in red) “to provide an intermediate frequency (IF) signal” (shown in purple). Bonn, 2:11-13, Fig. 1 (annotated, below). Bonn recognized that if the (blue) RF signal was too “strong,” that could drive the second transistor of the mixer (50) “into current saturation.” Bonn, 5:37-41; *see also id.*, 5:46-52.

Bonn, Fig. 1 (Annotated)

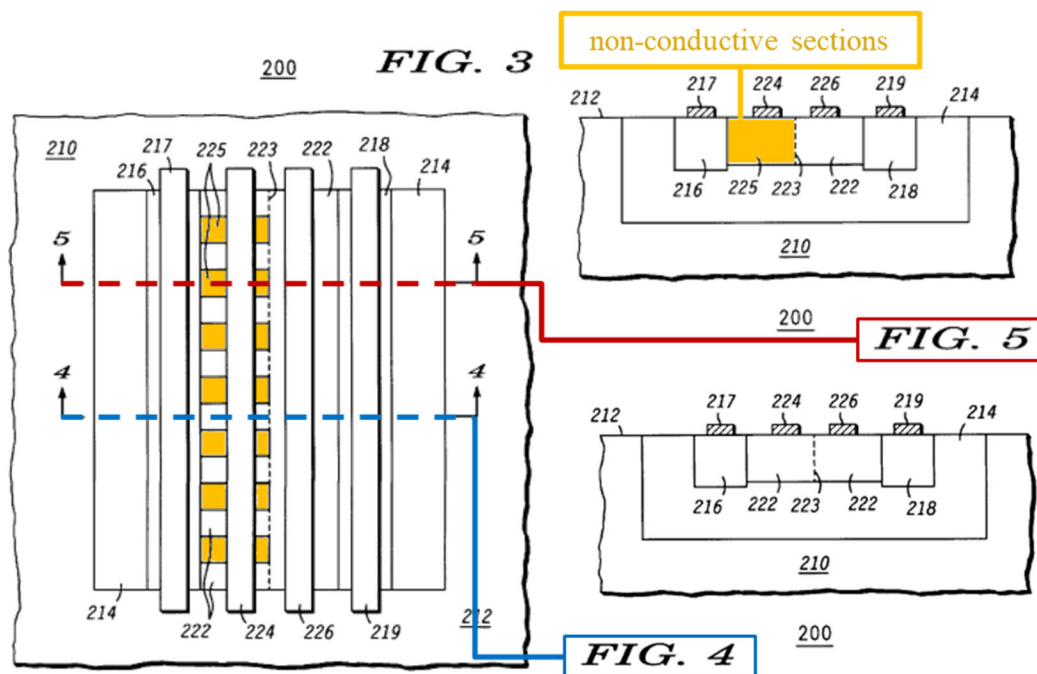


Bonn solved this problem by intentionally reducing the current-carrying capacity of the first FET (30) in comparison to the second FET (50). Specifically, Bonn discloses that “[i]n the cascode configuration, *FET 30 preferably has a smaller current conducting capacity than that of FET 50 to prevent FET 50 from being driven into current saturation by a strong RF signal* that may appear at the gate electrode of FET 30. *Id.*, 5:37-41; *see also id.*, 5:48-52.

Bonn achieves the reduction of current-carrying capacity including “[n]on-conductive sections 225” under the first gate to “reduce the effective channel width of the first gate region in structure 200.” *Id.*, 7:10-11, *see also id.*, 7:22-34,

7:59-64, Figs. 3, 4, and 5. Figure 3 (below) “is a top view of [Bonn’s] field effect transistor structure.” *Id.*, 1:54-56. Figure 4 “is a cross-sectional view along section line 4-4 of FIG. 3” and “FIG. 5 is a cross-sectional view along section line 5-5 of FIG. 3.” *Id.*, 1:57-61. As shown below, the transistor includes a number of non-conductive sections (in orange below) that act to reduce the current-carrying capacity of the first gate.

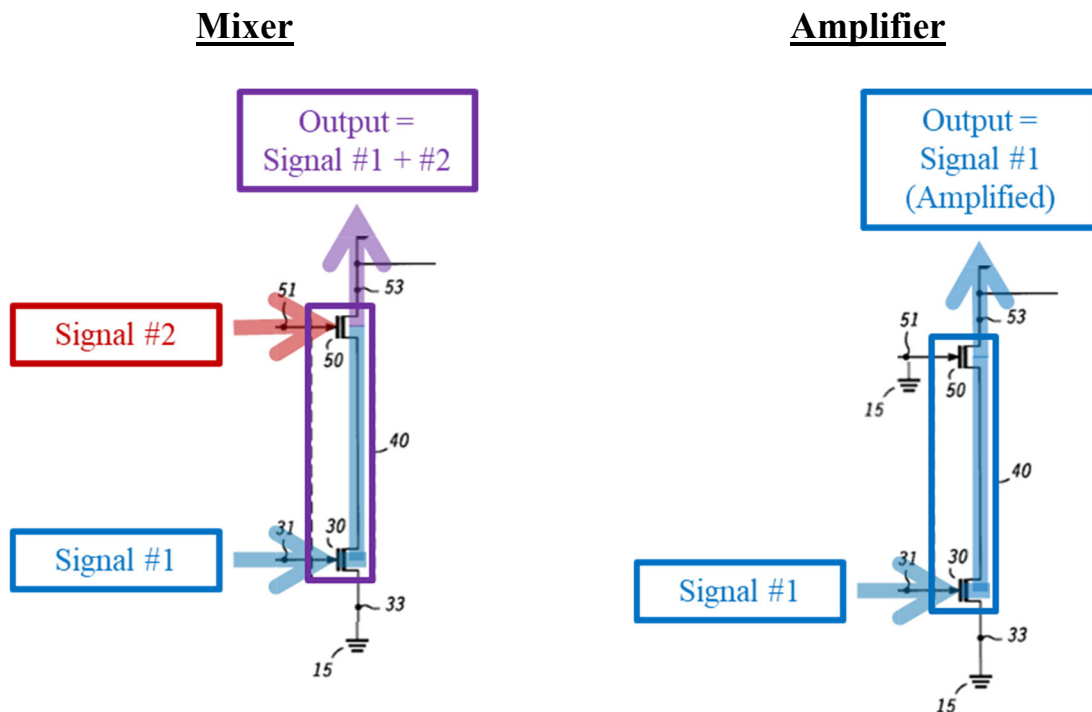
Bonn, Figs. 3-5 (Annotated)



The same is true for the structure of Figure 7, which the Petition alleges a POSA would have used as an amplifier. Petition, 22. Bonn discloses that the embodiment pictured in Figure 7 has “non-conductive sections 225 ... in first gate region 321 ... to individually adjust the gate width.” Bonn, 9:12-20.

b. Figure 7's Unequal Current-Carrying Capacities Under Each Gate Would Have Been Sub-Optimal for Use as an Amplifier

While such a transistor as Bonn's Figure 7 may be well suited as a mixer, it would have been sub-optimal for high-frequency signal amplification because of the imbalanced current-carrying capacity under the two gates. When a dual-gate transistor is used as a mixer, two signals are combined to form one output, which is why the imbalanced current-carrying capacity is desired. In an amplifier, only a single signal is amplified and so a transistor with equal current-carrying capacity would be better suited.



Neither the Petition nor the Bernstein declaration accounts for the imbalanced current-carrying capacity in Bonn's Figure 7 structure in each's argument that a

POSA would have used the Figure 7 structure as is, without modification, as an amplifier. Petition, 22; Bernstein, [097]. And the Petition proposes no modifications to Bonn's Figure 7 structure to make it suitable for use in an amplifier. The Petition's conclusion that a POSA would have used Bonn's Figure 7 structure as an amplifier is pure hindsight without any support by objective evidence. The Petition thus fails to establish that a POSA would have started with Bonn's Figure 7 structure for use as an amplifier in the first place.

2. The Petition Fails to Establish a POSA Would Have Rendered Bonn's Downconverter Inoperable for its Intended Purpose

While Bonn teaches that the structure of its dual-gate *transistor* "can be tailored" for other applications (Bonn, 11:34-37), the Petition misapplies that teaching as a license to destroy the basic operating principle of Bonn's *downconverter*, rendering it inoperable for its intended purpose. But the Federal Circuit has repeatedly held that a modification that would have rendered the primary reference "*inoperable for its intended purpose*" is not one a POSA would have made. *In re Gordon*, 733 F.2d at 902; *see also Trivasular*, 812 F.3d at 1068 (affirming the Board's finding that a POSA would not have replaced barbs in a primary reference with gripping protuberances from a secondary reference because the modification "would *destroy the basic objective* of the barbs, which is to penetrate surrounding tissue"); *Medtronic*, 69 F.4th at 1349 ("[A] proposed

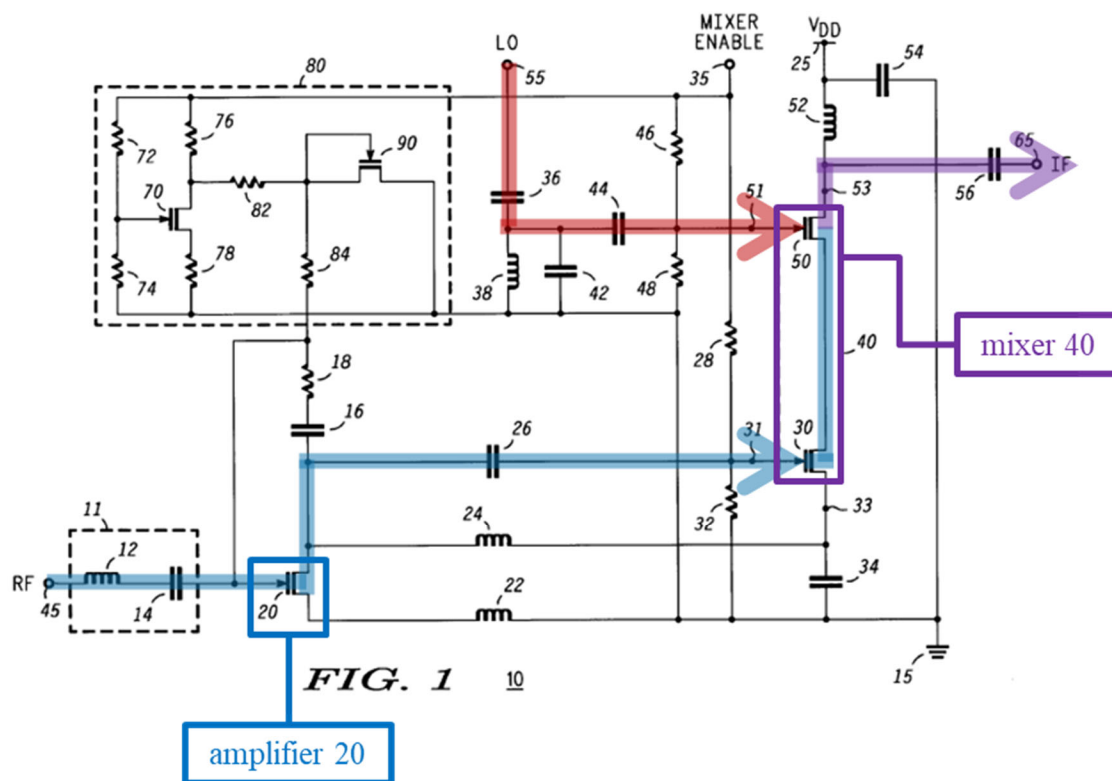
modification's *destruction of a device's primary purpose is ... at odds with common sense and gives in to the very hindsight bias the obviousness inquiry is designed to avoid.*"); *Henny Penny v. Frymaster*, 938 F.3d 1324, 1331-32 (Fed. Cir. 2019); *In re Ratti*, 270 F.2d at 813 (a combination does not render a claim obvious when it would have changed the "basic principles" under which the primary reference "was designed to operate").

Here, the Petition fails to establish that a POSA would have changed Bonn's downconverter circuitry so much as to change its basic operating principle, rendering it inoperable for its intended purpose. The Petition thus fails to establish that the Bonn-Mizuta Combination would have met Limitation [1C7].

3. The Petition Fails to Establish a POSA Would Have Connected the Second Gate of a Dual-Gate Device to a Constant Voltage Source as Claimed

Even if a POSA had been motivated to use the dual-gate transistor of Figure 7 as an amplifier and even if a POSA had been motivated to re-configure Bonn's downconverter to turn it into an amplifier, neither of which the Petition has established with objective non-hindsight driven evidence, the Petition still fails to show that a POSA would have been motivated to connect the gate terminal (51) to a constant voltage source as alleged. Petition, 22-25.

Bonn, Fig. 1 (Annotated)



As explained in more detail above (*see* § II.A, *supra*) Bonn only discloses applying a variable voltage source to **both** gates of its mixer 40. Mizuta does not disclose a dual-gate transistor at all. Thus, neither Bonn nor Mizuta provide any motivation to a POSA to connect a constant voltage source to the second gate of a dual-gate transistor.

E. The Expert Declaration Cannot Cure the Petition's Failures

1. The Evidence Relied Upon Needed to Be Cited and Explained in the Petition

The Petition's "Motivation to Modify Bonn for High Frequency Signal Amplification" section is eleven paragraphs spanning seven pages. Petition, 19-25.

It only cites to Bonn and to the Bernstein declaration. *Id.* As explained above, neither establishes that a POSA would have rewired Bonn's circuitry so significantly as to render Bonn's mixer inoperative for its intended purpose.

The Board has rules governing "Content" the Petition "must" have. 37 C.F.R. §42.22 and §42.104. Those rules make clear that the Petition "must" "includ[e] a detailed explanation of the significance of the evidence" (Rule 42.22(a)(2)) and "must" identify "the relevance of the evidence to the challenge raised, including identifying specific portions of the evidence that support the challenge" (Rule 42.104(b)(5)). The Petition violates these rules.

The cited portion of the Bernstein declaration ([094]-[109]) is sixteen paragraphs, spanning eleven pages, and cites five references that are **not** cited by nor explained in the Petition (Ex-1009, Ex-1018, Ex-1025, Ex-1026, and Ex-1027). Bernstein, [105]-[106]. None of that explanation and evidence cited only in the expert declaration can save the Petition because it cannot be incorporated by reference into the Petition.

"Arguments and information that are not presented and developed in the Petition, but instead are incorporated by reference, are not entitled to consideration, as it is improper to incorporate by reference arguments from one document into another document." *Instrumentation Lab. Co., v. Hemosonics LLC*, IPR2017-00855, Paper 55 (Feb. 13, 2019) (citing 37 C.F.R. § 42.6(a)(3); *see also*

Cook Grp. v. Boston Sci. Scimed, IPR2017-00131, Paper 13, 15 (May 15, 2017)

(“A *petition* must identify” “the relevance of the evidence to the challenge raised.

37 C.F.R. §42.104 (b). A string citation *purporting to incorporate arguments and evidence by reference is not a sufficient substitute for an explanation of the relevance of the asserted evidence.*”); 37 C.F.R. § 42.104(b)(5) (the *Petition* “must” identify “the *relevance* of the evidence to the challenge raised, including *identifying specific portions of the evidence* that support the challenge.”).

Thus, nothing in the expert declaration can save the Petition from its failure to show that a POSA would have rewired Bonn’s circuitry so significantly as to render Bonn’s mixer inoperative for its intended purpose.

2. The Expert Declaration Fails to Cure the Petition’s Deficiencies

Even if the Board were to wade through the Bernstein declaration, it does not remedy the Petition’s failures. The difference in length between the Petition (pages 19-25) and the Bernstein declaration’s corresponding paragraphs [094]-[109] are largely (1) the inclusion of quotations from Bonn omitted from the Petition, and (2) a discussion of the “background knowledge of a POSITA” in paragraphs [105]-[107], which is omitted from the Petition as well (Petition, 25). Neither cures the deficiencies of the Petition.

The quotes from Bonn do not cure the Petition’s deficiencies because Bonn only ever explains what the purpose of the various components of its circuitry are—Bonn does not suggest removing any of those components.⁴

Paragraphs [105]-[107] of the Bernstein declaration (the “background knowledge of a POSITA”) also do not cure the Petition’s deficiencies because they discuss a POSA’s knowledge of the “Miller effect” ([105]), “the way a cascode transistor works in a normal amplifier circuit” ([106]), and the familiarity a POSA would have had “with this common arrangement” of a cascode ([107])—none of which would have motivated a POSA to convert a mixer into an amplifier or connect the second gate of a dual-gate transistor to a constant voltage source as claimed. Specifically, Bonn’s dual-gate transistor is already in a cascode arrangement. Bonn, 1:21-23 (“[T]he mixer circuit may use a dual-gate field effect transistor or two field effect transistors in a cascode configuration to mix the RF and LO signals.”). Bernstein’s purported solution to reduce the Miller effect—using a cascode—is solving for a problem that does not exist in Bonn’s mixer because Bonn’s mixer is already in a cascode arrangement.

⁴ Bonn discloses that capacitor 16, resistor 18, and inductor 22 are “optional” (Bonn, 2:33-34), but removing those would not have changed the fundamental operation of Bonn’s downconverter 10 and mixer 40 as the Petition proposes.

Moreover, nothing in paragraphs [105]-[107] of the Bernstein declaration suggests a POSA would have been motivated to connect the second gate of a dual-gate transistor to ground. Bernstein cites Mishra (Bernstein, [106]), but Mishra only discloses connecting a constant voltage source to the second of two single-gate transistors, which are connected by wires to one another. *See* § IV.A.1, *infra*. Bernstein cites Sankin (Bernstein, [106]), but Sankin only discloses connecting a constant voltage source to the second of two single-gate transistors, which are connected by wires to one another too as shown below. Ex-1018, Fig. 2.

Prior Art: Sankin Fig. 2 (annotated)

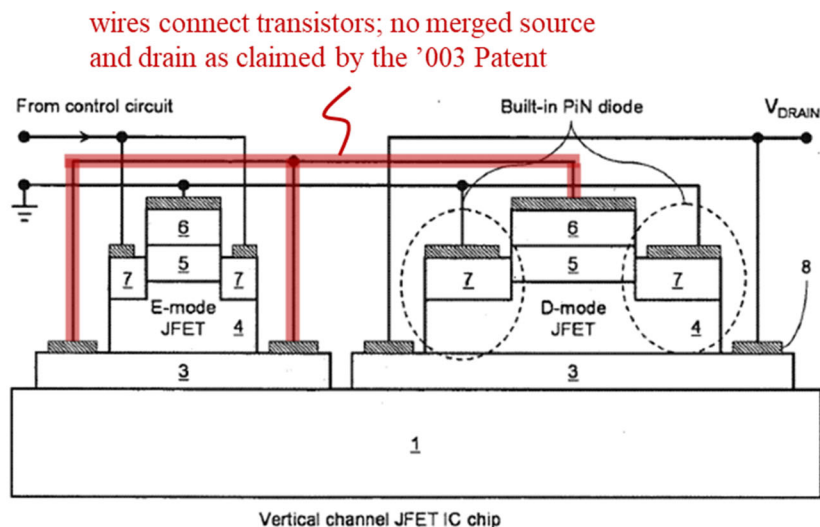


FIG. 2

Apart from the quotes from Bonn and citations to exhibits that are not cited in the Petition to show the background knowledge of a POSITA in paragraphs [105]-[107], the Bernstein declaration is largely word-for-word the same as the Petition. The Board routinely denies institution to petitions that are supported by

little more than experts who merely repeat the conclusions articulated in the petition. *See* § III.A.3, *supra* (citing authority).

In sum, even though the Bernstein declaration includes testimony, quotes from Bonn, and citations to exhibits that are not cited in the Petition and thus should not be considered, even if they were, they would not cure the Petition’s deficiencies.

* * *

In sum, Ground 1 fails because the Petition fails to establish that the Bonn-Mizuto Combination would have met Limitation [1C7].

III. GROUND 2 FAILS FOR THE SAME REASONS AS GROUND 1

Ground 2 challenges claims 1-16 as allegedly obvious over Bonn (Ex-1006) in view of Ren (Ex-1008) and Mishra (Ex-1009). Petition, 6. But Ground 2 fails for the same reasons Ground 1.

Ground 2 relies on two different secondary references (Ren and Mishra) but the Petition cites neither in arguing that a POSA would have modified Bonn in the same way as alleged in Ground 1 (repurposing Bonn’s mixer as an amplifier). Petition, 49. Instead, the Petition merely cross-references its prior hindsight-biased analysis from Ground 1 (citing Petition § VII.A.1) and cites “Bernstein, [156],” which itself merely cross-references Bernstein’s “§ XII.A.1 (Motivation to Modify Bonn for High Frequency Signal Amplification).”

The remaining proposed modifications based on Ren and Mishra only relate to “mak[ing] Bonn’s device out of GaN semiconductor materials, as Ren discloses” (Petition, 50) and “include[ing] a field plate” as Mishra discloses (*id.*, 54). None of the modifications from Ren and Mishra relate to connecting the second gate of a dual-gate transistor to a constant voltage source as required by Limitations [1C7] and [10C8]. The Petition *alleges* that Bonn discloses “the second gate is connected to the constant voltage source,” but only cross-references its Ground 1 analysis and the Bernstein declaration, [199]-[201]. Petition, 68. Bernstein [199]-[201] cites nothing in Bonn and merely cross-references Bernstein’s Ground 1 analysis. As explained above, Bonn has no disclosure of connecting the second gate to a constant voltage source—the two gates in Bonn’s mixer 40 are both connected to variable voltage sources. *See* § II.A, *supra*.

Ground 2 thus fails for at least the same reasons as Ground 1. *See* § II.A-E, *supra*.

IV. GROUND 3 FAILS FOR TWO INDEPENDENT REASONS

Ground 3 challenges claims 1-16 as allegedly obvious over Mishra (Ex-1009) and Ren (Ex-1008). Petition, 6. But Ground 3 fails because the Petition fails to establish that the Mishra-Ren Combination met Limitations [1C9] and [10C10] and failed to establish a POSA would have had at least a reasonable expectation of success.

A. The Petition Fails to Establish that the Mishra-Ren Combination Would Meet Limitations [1C9] and [10C10]

The Petition alleges that “Mishra discloses implementing dual gate GaN HEMTs in cascodes.” Petition, 82. While Mishra contains a single aspirational statement that “[o]ne alternative arrangement comprises a single transistor with a dual gate structure” (Mishra, [0062]), Mishra fails to disclose the structure of such a transistor. This lack of disclosure is fatal to Ground 3 because a transistor “with a dual gate structure” does not necessarily comprise a merged cascode transistor comprising a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor as required by Limitations [1C9] and [10C10]. In other words, just because Mishra happens to mention a generic concept, *i.e.* a dual gate structure, it does not mean that Mishra discloses the merged cascode transistor claimed by the ’003 patent.

The failure of Mishra to disclose a transistor with a merged source and drain region is fatal to Ground 3. Even the Petition admits that the requirement of merged source and drain regions of the enhancement mode and depletion mode transistors was the very limitation that the Examiner found missing from the prior art during prosecution. Petition, 11. Thus, the claimed feature missing from Ground 3 is the same feature missing from the art before the Examiner.

Faced with this critical missing limitation, the Petition uses the testimony of its expert alone to again tailor the missing limitation in a long series of

modifications starting from a single-gate transistor where, essentially, the only stated motivation is that the element was “known” or a similar conclusory statement that it would have been “obvious.” Petition, 82-88, citing Bernstein, [248]-[260]. As explained above, while there are some circumstances in which expert testimony alone can fill in a limitation missing from the prior art, that is only possible when there has been a showing that the limitation in question is unusually simple and the claimed technology is shown to be particularly straightforward. *See* § II.C, *supra*. The purpose of this requirement is to avoid the risk of hindsight bias, but the Petition fails to make either of those showings.

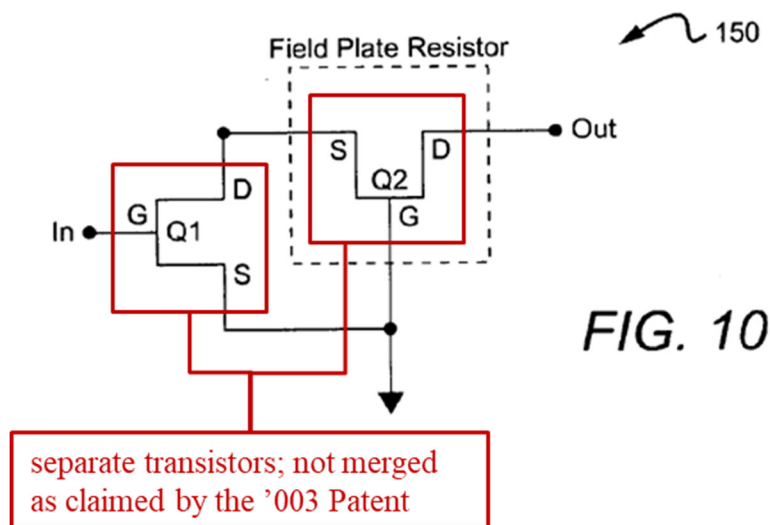
1. Mishra Fails to Disclose Limitations [1C9] and [10C10]

While the Petition alleges that Mishra discloses a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor as claimed by Limitations [1C9] and [10C10], the Petition cites no evidence to support that statement. Petition, 101-102. Indeed, Mishra never discloses a merged dual gate transistor of any type, let alone one with the drain region of an enhancement mode transistor merged with the source of a depletion mode transistor as required by Limitations [1C9] and [10C10].

Mishra discloses a “multi-stage amplifier” circuit but only discloses using two individual *single-gate* transistors coupled together as shown in Figure 10 (below, annotated). Mishra teaches that Fig. 10 shows “a multi-stage transistor

amplifier block” with “a first stage transistor Q1 and a second stage transistor Q2, each of which may comprise a wide-bandgap field effect transistor,” meaning that Fig. 10 discloses two separate transistors connected together, not a dual gate transistor. Mishra, [0058].

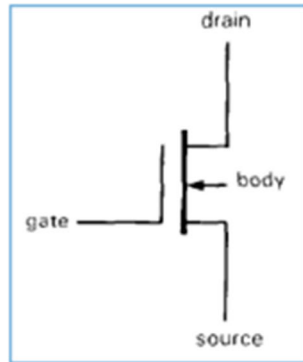
Mishra Fig. 10 (Annotated)



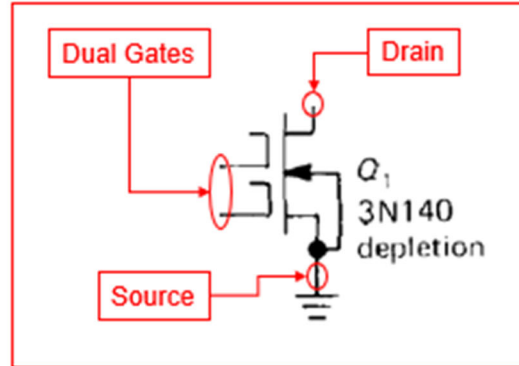
A POSA would have known that Mishra’s transistors are separate, ordinary, single-gate transistors as opposed to a dual-gate transistor for the additional reason that Mishra’s circuit diagram of Fig. 10 did not use the known symbol for a dual-gate transistor that was commonly used in the art (below).⁵

⁵ While Figure 2 of the '003 Patent does not use the dual-gate transistor symbol shown, the '003 Patent expressly states that “FIG. 2 illustrates a merged gate transistor.” Ex-1001, 2:36-37. Mishra has no such disclosure.

Comparison of Single-Gate and Dual-Gate Transistors



Ordinary (Single Gate)
Transistor

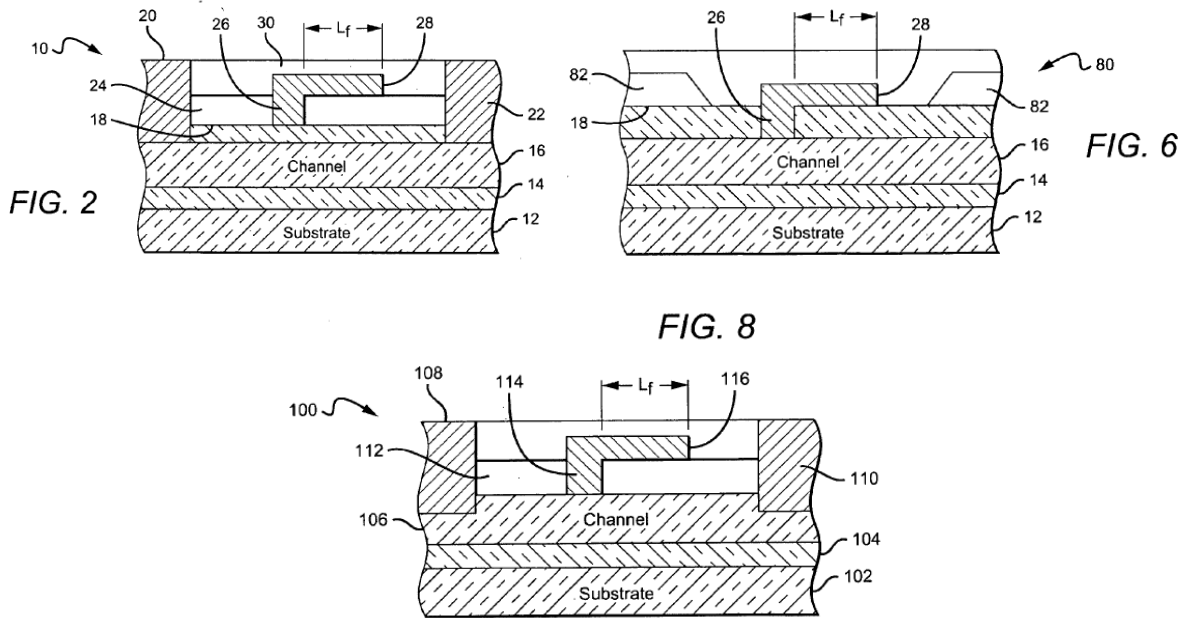


Dual Gate Transistor

Ex-2002, 114 (Figure 3.1), 883 (Figure 13.23, excerpted and annotated).

Moreover, all of Mishra's embodiments (Figs. 2, 4, 5, 6, 8, and 9) are of a single-gate transistor that includes a field plate connected to the gate. For example, the embodiments in Figures 2, 6, and 8 have the field plate connected to the gate in the cross section. Mishra, Figs. 2, 6, 8 (below).

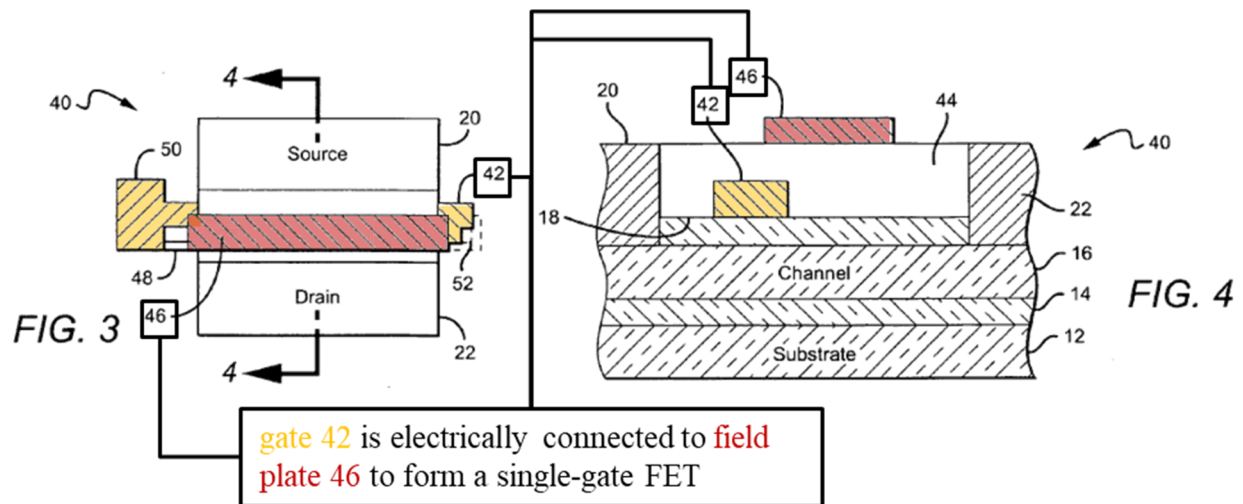
Mishra Figs. 2, 6, and 8



The embodiment in Figures 3 and 4 also are of a single-gate transistor.

Figures 3 (plan view) and 4 (cross-section) show that the field plate 46 is “electrically connected to gate 42.” Mishra, [0040]. Mishra discloses that “[t]he field plate 46 can be connected to the gate 42 through a first conductive path 48 running outside the active area of the HEMT 40 to a gate contact 50 that is used to make electrical contact to the gate 42” and that “[a] second conductive path 52 (shown in phantom) can also be used that runs outside of the active region of the HEMT 40 on the side opposite the gate contact 50.” *Id.*, [0040].

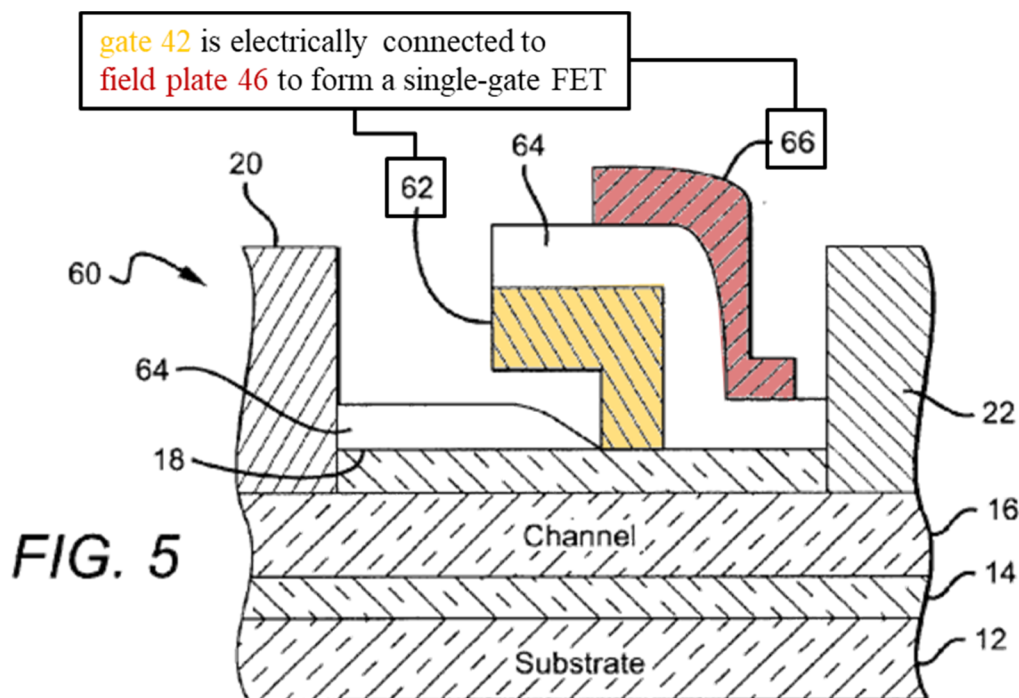
Mishra Figs. 3 and 4 (Annotated)



The embodiment of Figures 8 and 9 show a MESFET (as opposed to a HEMT) that “has a gate and field plate structure similar to that in the HEMT 40 shown in FIGS. 3 and 4.” *Id.*, [0052].

Mishra further discloses that “FIG. 5 shows another embodiment of a HEMT 60” that “also includes a field plate 66 on the spacer layer 64 that overlaps that gamma gate 62.” *Id.*, [0042]-[0043]. Mishra discloses that “[l]ike the field plate 46 shown in FIGS. 3 and 4 and described above, the field plate 66 can be connected to the gate 62 in many different ways.” *Id.*, [0044].

Mishra Fig. 5 (Annotated)

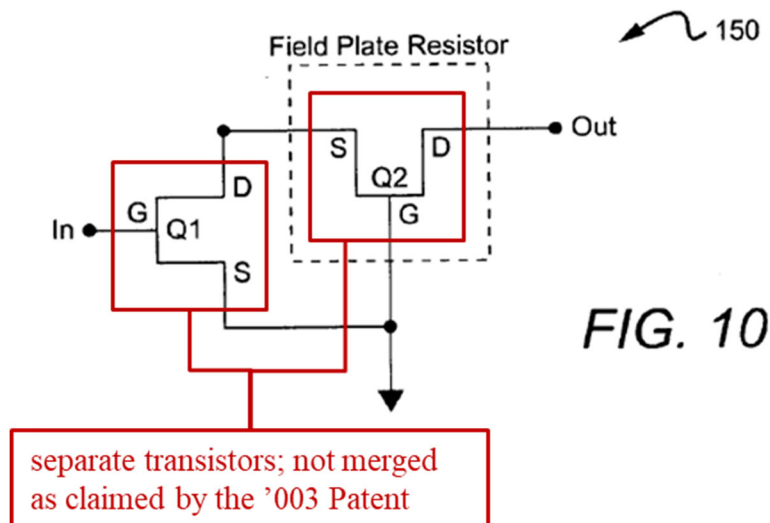


Thus, all of the embodiments of Figures 2, 4, 5, 6, 8, and 9 are single-gate transistors, not dual-gate transistors.

All of Mishra's single-gate transistors all depict the second stage of Mishra's 2-stage amplifier—none disclose the first stage. Mishra discloses that its single-gate transistors with field plates can be used in a "2-stage cascode amplifier structure." *Id.*, [0056]. Figure 10 (below) provides one such example of a "multi-stage transistor amplifier block." *Id.*, [0058]. But none of the embodiments of Figures 2, 4, 5, 6, 8, and 9 disclose Q1 in Figure 10 because they all have field plates and Mishra discloses that "Q1 does not include a field plate." *Id.*, [0059]. The embodiments of Figures 2, 4, 5, 6, 8, and 9 are all thus examples of Q2,

“which includes a field plate.” *Id.*, [0060]. Mishra thus discloses no structure for the first (Q1) of its two single-gate transistors.

Mishra Fig. 10 (Annotated)



While Mishra has a single generic statement in its penultimate paragraph that “[o]ne alternative arrangement comprises a single transistor with a dual gate structure” (*id.*, [0062]), Mishra does not disclose the structure of such a transistor. The Petition admits that “Mishra does not explicitly comment on the mode in which Q1 operates.” Petition, 83. Thus, Mishra does not disclose an enhancement mode transistor as part of the theoretical dual-gate structure.

Moreover, Mishra does not even disclose that its “dual gate structure” is of the type claimed by the '003 patent, having a drain region of the first transistor merged with the source region of the second transistor. For example, Petitioner’s own cited art, Sankin, discloses a transistor with two gates (*i.e.* a dual-gate

transistor) that does not have a drain region of the first transistor merged with the source region of the second transistor—the two transistors are connected by wires. Ex-1018 (below).

Prior Art: Sankin Fig. 2 (annotated)

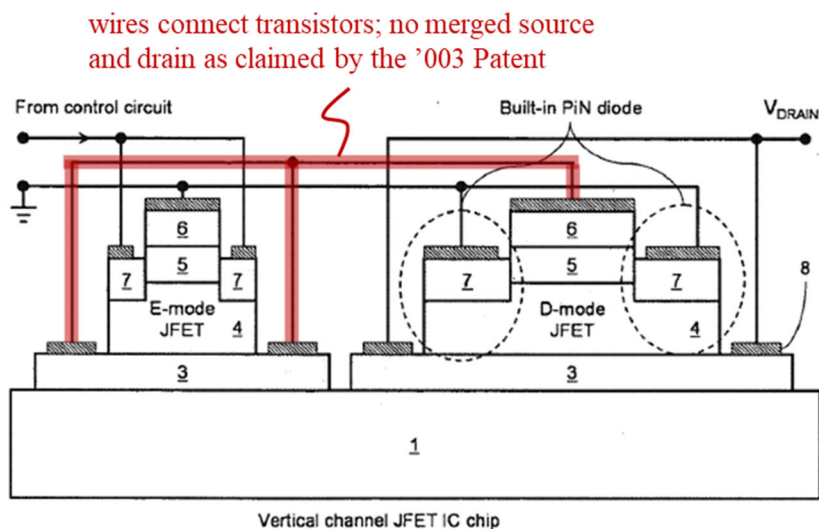


FIG. 2

The Petition offers no evidence that Mishra’s disclosure of a “dual gate structure” (Mishra, [0062]) was the merged type claimed by the '003 Patent and not the type connected by wires as disclosed by Sankin (above) or some other unclaimed type.

The Petition alleges that “Mishra discloses [1C9],” including “a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor,” but cites nowhere in Mishra that discloses that limitation.

Petition, 101. The Petition cites Ex-1011, but that is Infineon’s claim chart showing how Respondent’s products infringe the '003 patent—it provides no evidence as to the disclosure of Mishra. The Petition cites Figure 5 of Mishra, but

as explained above, Figure 5 shows a single-gate transistor with a field plate that is electrically connected to the gate, not a dual-gate transistor at all. The Petition cites Bernstein, [295]-[296], but those paragraphs are nearly word-for-word the same as the Petition—Bernstein does not cite anywhere in Mishra that discloses a dual-gate transistor with a drain region of the first transistor that is merged with a source region of the second transistor.

In sum, neither the Petition nor the Bernstein declaration cites any part of Mishra that discloses a drain region of the first transistor that is merged with a source region of the second transistor—let alone a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor as required by Limitations [1C9] and [10C10]. The Petition and Bernstein fail to cite any disclosure because, as explained above, Mishra has no such disclosure.

2. POSAs Motivated to Modify Mishra Based on Ren Would Not Have Arrived at a Circuit Meeting Any Challenged Claim

The Petition argues that modifying Mishra with Ren would have “added known benefit of being safer to operate” would have “achieve[d]” “‘efficient high power and high frequency signal amplification’ and ‘reduced leakage’” (Petition, 85), but the Petition fails to explain how Mishra was in any way deficient in these respects. The Petition fails to explain why such factors would have been a concern,

given the applications taught. The Petition’s alleged motivations are thus untethered to Mishra, which is what the Petition’s combination seeks to modify.

But even if it were accepted that a POSA would have been motivated to modify Mishra with Ren (which the Petition fails to prove), the Petition only alleges that a POSA would have modified Mishra “to make Mishra’s first gate enhancement mode and second gate depletion mode.” Petition, 86. Even if a POSA did make Mishra’s first transistor an enhancement mode transistor and Mishra’s second transistor a depletion mode transistor, that would still fail to disclose a merged transistor with the drain of the enhancement mode transistor merged with the source of the depletion mode transistor as required by Limitations [1C9] and [10C10].

3. The Board Routinely Denies Institution when the Petition’s Grounds Rely on Prior Art with Missing Claimed Features

Unable to find a single prior art reference that discloses a merged transistor with a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor as required by Limitations [1C9] and [10C10]—the very limitation that the Examiner found missing from the prior art as the Petition admits—the Petition seeks to reconstruct that limitation in hindsight by using expert testimony to fill in the missing limitation. Petition, 82-88. As explained more fully above in the Ground 1 analysis (*see* § II.C, *supra*), Federal Circuit precedent establishes that expert testimony can only be used to supply a

limitation missing from the art if “the limitation in question [is] unusually simple and the technology particularly straightforward.” *Arendi*, 832 F.3d at 1362; *see also DSS Tech.*, 885 F.3d at 1374 (“we have invoked common sense to fill in a *missing* limitation only when the limitation in question was unusually simple and the technology particularly straightforward.”) (internal quotes and citations omitted).

Petitioner does not even attempt to make that requisite showing. Petition, 82-88. As explained more fully above in the Ground 1 analysis (*see* § II.C, *supra*), the Board routinely denies institution where the petitioner seeks to meet a missing limitation based solely on expert testimony. *See e.g., Xerox* at 14-16 (precedential); *Apple* at 19-20; *Microsoft v. LiTL*, IPR2024-00458, Paper 17, 17-21.

Petitioner’s failure to establish that this is one of the rare exceptions to the rule forbidding reliance on expert testimony alone to meet a claim limitation missing from the prior art is reason enough to deny institution.

4. The Petition Fails to Establish a POSA Would Have Turned Mishra’s Single-Gate Transistor into a Dual-Gate Transistor

Establishing obviousness over a combination of references requires establishing some non-hindsight *reason why* POSAs would have combined the teachings in the art in the manner claimed. *Pers. Web Techs.*, 848 F.3d at 994. The Petition, however, identifies no reason why a POSA would have modified Mishra’s

single-gate transistor into a dual-gate transistor. Petition, 82-88. The Petition’s analysis begins with the false premise that Mishra’s Figure 5 shows a dual-gate transistor when it says, “Mishra discloses implementing dual gate GaN HEMTs in cascodes,” citing Figure 5 (*id.*, 82), and then later annotating Figure 5 as if it were a dual-gate transistor on page 88. But as explained above, Mishra’s Figure 5 shows a *single-gate* Q2 transistor—not a *dual-gate* transistor of any type. See § IV.A.1, *supra*.

Moreover, the Petition provides no objective reasoning why a POSA would have looked to convert Mishra’s Figure 5 single-gate transistor into a dual-gate transistor. Petition, 82-88. For example, the Petition alleges no benefit of a dual-gate transistor. The Petition alleges no drawback of the two single-gate transistors connected in series, as disclosed in Figure 10 of Mishra. And the Petition cites no evidence whatsoever of the alleged obviousness.

The Petition cites Bonn, Sankin, and Salato as disclosing “cascodes with first stage enhancement and second stage depletion mode gates.” Petition, 84. But none of those references are part of the combination of Ground 3, and the disclosure of a cascode with two single-gate transistors is different than the single device with merged transistors as claimed by the ’003 Patent. Moreover, Sankin discloses connecting its gates by wires; Sankin does not disclose a merged transistor as claimed by the ’003 patent. Ex-1018 (below).

Prior Art: Sankin Fig. 2 (annotated)

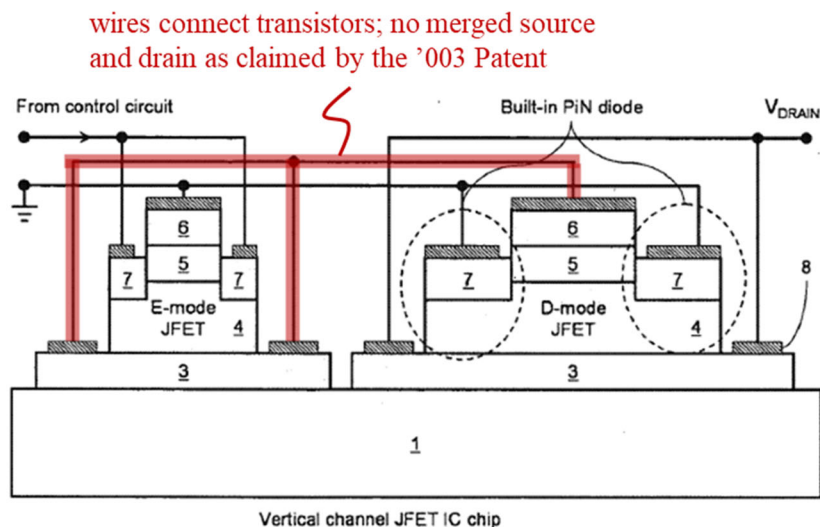


FIG. 2

And Salato issued on August 5, 2008, from an application filed on May 23, 2006—*after* March 20, 2006, which the Petition admits is the “earliest claimed priority of the '003 patent.” Petition, 2. The Petition does not even establish that Salato is prior art to the claims of the '003 patent. *See Penumbra, Inc. v. RapidPulse, Inc.*, IPR2021-01466, Paper 34, 29-35 (Mar. 10, 2023) (precedential); *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

The Petition cites “Bernstein, [248]-[260].” Petition, 82. But those paragraphs of Bernstein start with the same false assumption that Figure 5 shows a dual-gate transistor when Mishra discloses that it is a single-gate transistor. *See* § IV.A.1, *supra*. The Bernstein declaration equally lacks any objective reasoning why a POSA would have looked to convert Mishra’s Figure 5 single-gate transistor into a dual-gate transistor. Bernstein does not explain any benefit of a dual-gate

transistor or drawback of the two single-gate transistors connected in series. The Bernstein declaration thus does not cure the Petition's deficiency.

In sum, the Petition fails to articulate any reason why a POSA would have transformed Mishra's Figure 5 single-gate transistor into a dual-gate transistor, and certainly not into a dual-gate transistor having the drain of an enhancement mode transistor merged with the source of a depletion mode transistor as required by Limitations [1C9] and [10C10], particularly given that neither Mishra nor Ren disclose that limitation, which the Petition admits was missing from the art before the Examiner during prosecution as well. Petition, 11.

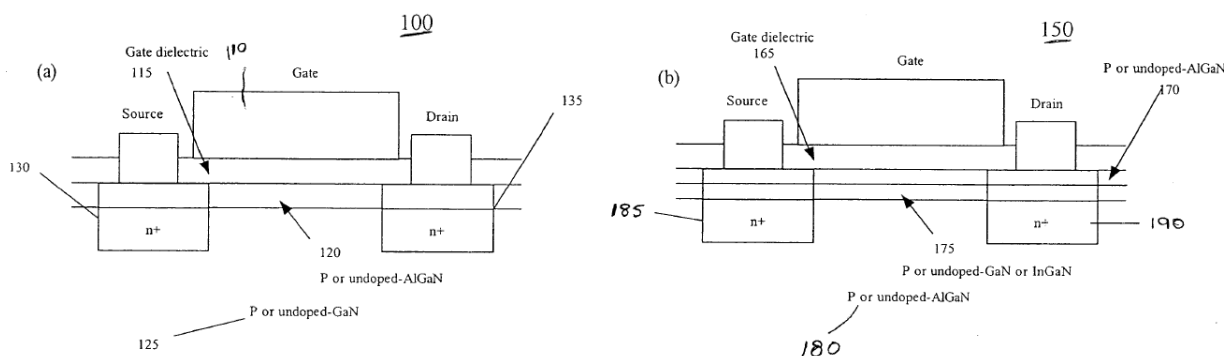
B. The Petition Fails to Establish at Least a Reasonable Expectation of Success for the Mishra-Ren Combination of Ground 3

The Petition also fails to establish that a POSA would have had at least a reasonable expectation of success in transforming Mishra's single-gate transistor into a dual-gate transistor with a drain region of an enhancement mode transistor merged with a source region of a depletion mode transistor as claimed by the '003 Patent. The Petition only alleges "predictable results" once in Ground 3, citing evidence that a POSA would have predictably been able to turn a depletion mode transistor into an enhancement mode transistor by changing the thickness of the dielectric layer between a gate electrode and the semiconductor surface and the AlGa_N thickness and doping. Petition, 86-87. While the cited evidence might show predictable success for making a *single-gate* AlGa_N/Ga_N enhancement mode

transistor and a *single-gate* AlGaN/GaN depletion mode transistor, none of the cited evidence discloses how to make a *dual-gate* transistor, let alone a dual-gate transistor having a drain region of an enhancement mode transistor merged with a source region of a depletion mode transistor.

The Petition cites Ren, but Ren does not disclose a dual-gate transistor of any type, let alone one with an enhancement mode GaN HEMT merged with a depletion mode GaN HEMT in the way claimed by the '003 Patent. Ren only discloses single-gate GaN transistors. *E.g.* Ren, Fig. 1(a)-(b) (below).

Ren's Single-Gate GaN Transistors (Figs. 1(a)-(b))



The Petition cites Wu (Ex-1021) and Chavarkar (Ex-1022), but neither discloses a dual-gate transistor of any kind. None of Ren, Wu, or Chavarkar thus can provide any evidence that a POSA would have had at least a reasonable expectation of success in making a merged dual-gate transistor as claimed.

The complete lack of disclosure of a merged dual-gate transistor is fatal to Ground 3 because even by March 20, 2026, GaN was still a relatively new

technology. As the Petition admits, “GaN was uncommon in 1996.” Petition, 2. While the Petition suggests that by 2006, “manufacturing improvements had made these devices more common” (*id.*, 51), this does not show that GaN semiconductor processing, much less GaN device and circuit engineering, was so well understood that a POSA would have expected to be able to successfully make a merged cascode transistor out of GaN, especially without undo experimentation.

For example, Thomas Herman, the sole named inventor of the '003 patent explained that making enhancement mode GaN transistors “was deemed a more difficult task.” Ex-2003, 30:2-15 (“**Q.** Did you design semiconductors with enhancement mode gates while you were at IR? **A.** The bulk of the effort at IR was depletion mode gates and transistors in GaN. **Q.** Did you also design enhancement mode transistors in GaN? **A.** There was interest in designing enhancement mode GaN transistors, but *that was deemed a more difficult task*. And I don’t believe there was any active effort to specifically fabricate enhancement mode GaN transistors, other than, you know, feasibility and discussions. But I don’t believe there was any effort to physically fabricate an enhancement mode GaN device.”). The Petition alleges that POSAs would have made a dual-gate GaN device with an enhancement mode transistor merged with a depletion mode transistor but fails to cite a single prior art reference that discloses how such a transistor could be made to work successfully.

In sum, even if a POSA were motivated to attempt a dual-gate GaN transistor with an enhancement mode transistor merged with a depletion mode transistor, the Petition cites no evidence whatsoever that would support the notion that a POSA would have had at least a reasonable expectation of success in making such a dual-gate GaN transistor without undue experimentation.

* * *

In sum, Ground 3 fails for the reasons explained above.

V. CONCLUSION

For the foregoing reasons, the Petition fails to carry its burden for any of Grounds 1-3. The Board should deny institution.

Respectfully submitted,
Infineon Technologies Americas Corp.

Date: April 11, 2025

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** contains 10,157 words excluding; a table of contents, a table of authorities, a certificate of service or word count, or appendix of exhibits or claim listing. Patent Owner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Date: April 11, 2025

/MacAulay Rush/
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Paralegal
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CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.6 (e)(4)

I certify that on April 11, 2025, a copy of the foregoing document, including any exhibits filed therewith, is being served via electronic mail, as previously consented to by Petitioner, upon the following:

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