

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

IPR2025-00094
Patent 8,264,003 B2

Before JO-ANNE M. KOKOSKI, CHRISTOPHER M. KAISER, and
LISA A. MURRAY, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

A. *Background and Summary*

Innoscence America, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–16 (“the challenged claims”) of U.S. Patent No. 8,264,003 B2 (Ex. 1001, “the ’003 patent”). Infineon Technologies Americas Corp. (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”). Patent Owner did not “file a brief requesting discretionary denial of institution,” so the case was referred to us “to consider the merits and non-discretionary considerations.” Paper 8, 1–2.

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). *Inter partes* review may not be instituted unless “the information presented in the petition filed under [35 U.S.C.] section 311 and any response filed under [35 U.S.C.] section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). “When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” 37 C.F.R. § 42.108(a) (2023). In other words, a decision to institute under § 314 may not institute on fewer than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 584 U.S. 357, 370–372 (2018). In addition, if the Board institutes trial, it will “institute . . . on all grounds in the petition.” PTAB Consolidated Trial Practice Guide, 5–6 (Nov. 2019)¹ (“CTPG”); *see also PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute to require “a simple yes-

¹ Available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

or-no institution choice respecting a petition, embracing all challenges included in the petition”).

For the reasons set forth below, upon considering the briefing and the evidence of record, we determine that the information presented in the Petition establishes a reasonable likelihood that Petitioner will prevail with respect to at least one of the challenged claims. Accordingly, we institute *inter partes* review of all challenged claims on all grounds asserted in the Petition.

B. Real Parties-in-Interest

Petitioner identifies itself, Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience (Suzhou) Technology Holding Company, Ltd. as real parties-in-interest. Pet. 116. Patent Owner identifies itself as the real party-in-interest. Paper 4, 1.

C. Related Matters

The parties identify the following related proceedings: *Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al.*, Case No. 4:24-cv-01553 (N.D. Cal.), and *In re Certain Semiconductor Devices and Products Containing the Same*, Inv. No. 337-TA-1414 (USITC). Pet. 116; Paper 4, 1.

D. The '003 Patent

The '003 patent, titled “Merged Cascode Transistor,” is directed to “[a] merged gate transistor” with two gates, each “capacitively coupled to the semiconductor element,” where “conduction of the first portion [of the transistor] is based on a value of the input voltage signal” supplied to the first gate, “and the second gate is connected to a predetermined constant voltage.” Ex. 1001, codes (54), (57). The application giving rise to the '003

patent was filed on March 20, 2007, and it claims priority to a provisional application filed on March 20, 2006. *Id.* at codes (21), (22), (60).

The '003 patent describes prior-art cascodes using separate field-effect transistors as suffering from “[l]arge drain-source voltage (V_{ds}) swings during switching [that] create a large ‘Miller effect’ and as a result, excessive switching losses.” *Id.* at 1:36–38, Fig. 1. “In addition, high dV/dt changes at the drain (D) may result in a voltage transient V_{G1} at the gate (G),” which “may turn the transistor 1 ON briefly when not desired.” *Id.* at 1:39–44. “This unwanted period of conduction may result in rather large power and efficiency losses.” *Id.* at 1:44–45.

The '003 patent describes solving these problems by using a “single device and not two separate FETs.” *Id.* at 2:48–52, Fig. 2. According to the '003 patent, this causes “the ‘Miller effect’ [to be] greatly reduced,” causing “power losses [to be] substantially reduced.” *Id.* at 3:29–31. Under this approach, “[t]he dV/dt at the drain (D1) of the bottom portion Q1 is also reduced,” and “will result in lower overall power losses and higher efficiency.” *Id.* at 3:29–50.

E. Illustrative Claim

Petitioner challenges claims 1–16 of the '003 patent. Claims 1 and 10 are independent. Claim 1 is illustrative; it is reproduced below.

1. A merged cascode transistor circuit comprising:
 - an input voltage signal source having an input voltage signal;
 - a constant voltage source having a predetermined constant voltage;
 - a merged cascode transistor comprising:
 - a semiconductor element;

- a source electrode electrically connected to a top surface of the semiconductor element;
 - a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
 - a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
 - a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
- wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level, wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

Ex. 1001, 5:25–61.

F. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 6, 19–114):

Claim(s) Challenged	35 U.S.C. § ²	Reference(s)/Basis
1	103	Bonn, ³ Mizuta ⁴
1–16	103	Bonn, Ren, ⁵ Mishra ⁶
1–16	103	Mishra, Ren

In support of its unpatentability arguments, Petitioner relies on the declaration of Joseph B. Bernstein, Ph.D. (Ex. 1003, “Bernstein Declaration”).

II. ANALYSIS

A. Legal Standards

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and “the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art;

² Amendments to 35 U.S.C. §§ 102 and 103 enacted by the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), took effect on March 16, 2013. The ’003 patent issued from an application filed on March 20, 2007, and it claims priority to a provisional application filed on March 20, 2006. *See* Ex. 1001, codes (22), (60). Therefore, we apply the pre-AIA versions of §§ 102 and 103. Neither party, however, argues that the outcome of this case would differ based on applying the pre-AIA or post-AIA versions of these laws.

³ US 6,160,280, issued Dec. 12, 2000 (Ex. 1006).

⁴ US 6,483,135 B1, issued Nov. 19, 2002 (Ex. 1007). Although Petitioner calls this reference “Mizuto,” we refer to it as “Mizuta” because that is the listed name of the first inventor. Ex. 1007, code (75).

⁵ US 2004/0041169 A1, published Mar. 4, 2004 (Ex. 1008).

⁶ US 2005/0051800 A1, published Mar. 10, 2005 (Ex. 1009).

(2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). “While the sequence of these questions might be reordered in any particular case,” *KSR*, 550 U.S. at 407, the U.S. Court of Appeals for the Federal Circuit has repeatedly emphasized that “it is error to reach a conclusion of obviousness until all those factors are considered,” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1328 (Fed. Cir. 2016). Because Patent Owner does not address objective evidence of non-obviousness, we focus solely on the first three *Graham* factors.

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in an *inter partes* review).

At this preliminary stage, we determine whether the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that at least one of the challenged claims would have been unpatentable over the proposed prior art. We analyze the asserted grounds with the above-noted principles in mind.

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the pertinent art at the time of the invention is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham*, 383 U.S. at 17–18.

Factors pertinent to a determination of the level of ordinary skill in the art include “(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.” *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). “Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case.” *Id.*

Petitioner contends that one of ordinary skill in the art “would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design.” Pet. 5 (citing Ex. 1003 ¶¶ 67–69). Petitioner also argues that “[a]dditional education could substitute for professional experience and vice versa.” *Id.* On the present record, Patent Owner does not dispute Petitioner’s proposed level of ordinary skill. Prelim. Resp. 1–52. Neither party explains why the outcome of this case would be affected by the adoption of any of the proffered definitions of a person of ordinary skill in the art.

For purposes of this Decision, we adopt Petitioner’s assessment of the level of ordinary skill in the art, as it appears to be consistent with the ’003 patent and the asserted prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Claim Construction

We apply the same claim-construction standard used in the federal courts—in other words, the claim-construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b), which is articulated in *Phillips*. *See* 37 C.F.R. § 42.100(b). Under the *Phillips* standard, the “words of a claim ‘are generally given their ordinary and customary meaning,’” which “is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1312–13.

Neither party proposes construing any claim terms. Pet. 6; Prelim. Resp. 1–52. On the present record, we agree. As discussed below, we are able to determine whether to institute *inter partes* review of the ’003 patent without expressly construing any terms. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Asserted Obviousness over Bonn and Mizuta

Petitioner argues that a person of ordinary skill in the art would have found claim 1 obvious in light of the combined teachings of Bonn and Mizuta. Pet. 19–48. Patent Owner disagrees. Prelim. Resp. 8–33.

1. Overview of Bonn

Bonn, titled “Field Effect Transistor,” relates “to semiconductor downconverters.” Ex. 1006, code (54), 1:4–6. Bonn depicts a downconverter in Figure 1, reproduced below:

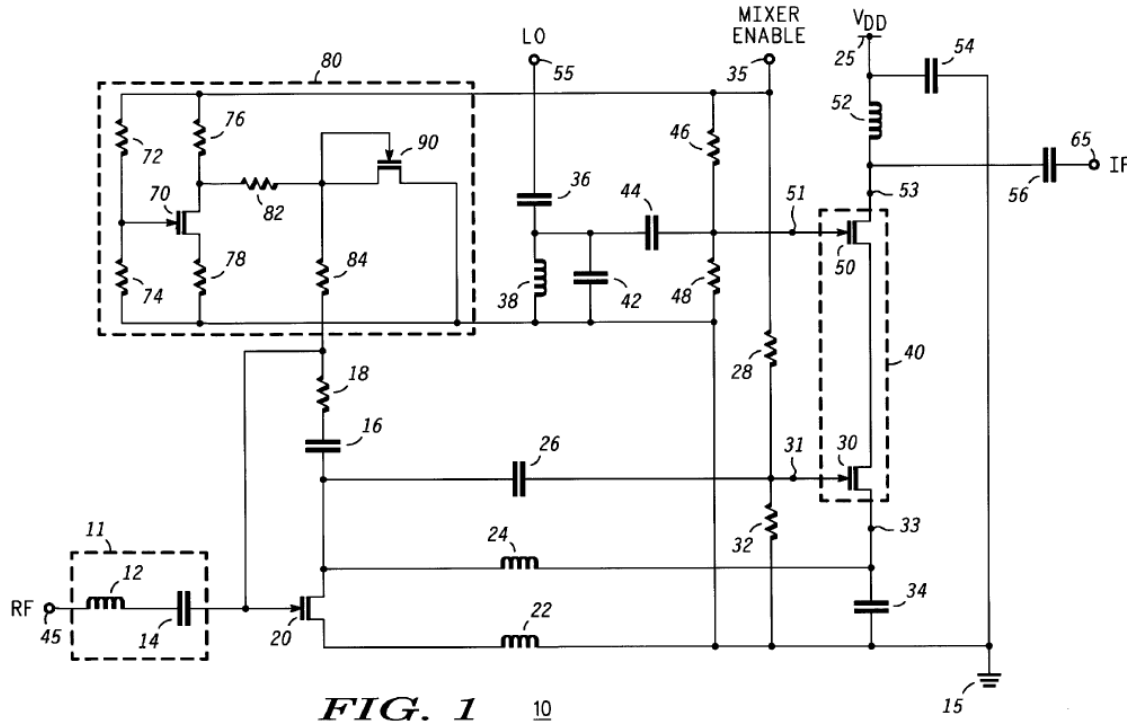


FIG. 1 10

Id. at 2:66–3:6, Fig. 1. Figure 1 of Bonn depicts “downconverter 10” in schematic form. *Id.* at 2:8. The downconverter of Figure 1 includes mixer 40 with field effect transistors 30 and 50 “coupled in a cascode configuration.” *Id.* at 2:66–3:6. Transistors 30 and 50 have gate terminals 31 and 51. *Id.* at 3:22, 3:30. “Second gate terminal 51 is coupled to power supply conductor 15 via a resistor 48 and to voltage supply conductor 35 via a resistor 46.” *Id.* at 3:30–32. “In addition, second gate terminal 51 is connected to a first electrode of capacitor 44. A second electrode of capacitor 44 is coupled to power supply conductor 15 via parallel connected capacitor 42 and inductor 38.” *Id.* at 3:32–36. “Further, the second electrode of capacitor 44 is coupled to [a local oscillator (‘LO’)]

port 55 via a capacitor 36 for receiving an LO signal. Capacitors 36, 42, and 44 and inductor 38 cooperate to form an impedance matching element for providing a desired input impedance, e.g., 50 Ω , at LO port 55.” *Id.* at 3:36–41.

2. Overview of Mizuta

Mizuta, titled “Field Effect Transistor,” relates to “[a] field effect transistor” that includes a “gate electrode [that] is provided with an overhanging field plate section.” Ex. 1007, codes (54), (57). Mizuta describes an overhanging, drain-side field plate section for gallium arsenide field-effect transistors. *Id.* at 12:30–47, Fig. 11(b). According to Mizuta, “the field centralization which develops on the edge section of the gate electrode on the drain side is made to relax and spread over, improving characteristics of withstand voltage.” *Id.* at 2:15–18. Field-effect transistors made using this method have “high withstand voltage characteristics and good gain characteristics, together with excellent high-frequency characteristics.” *Id.* at 1:61–65.

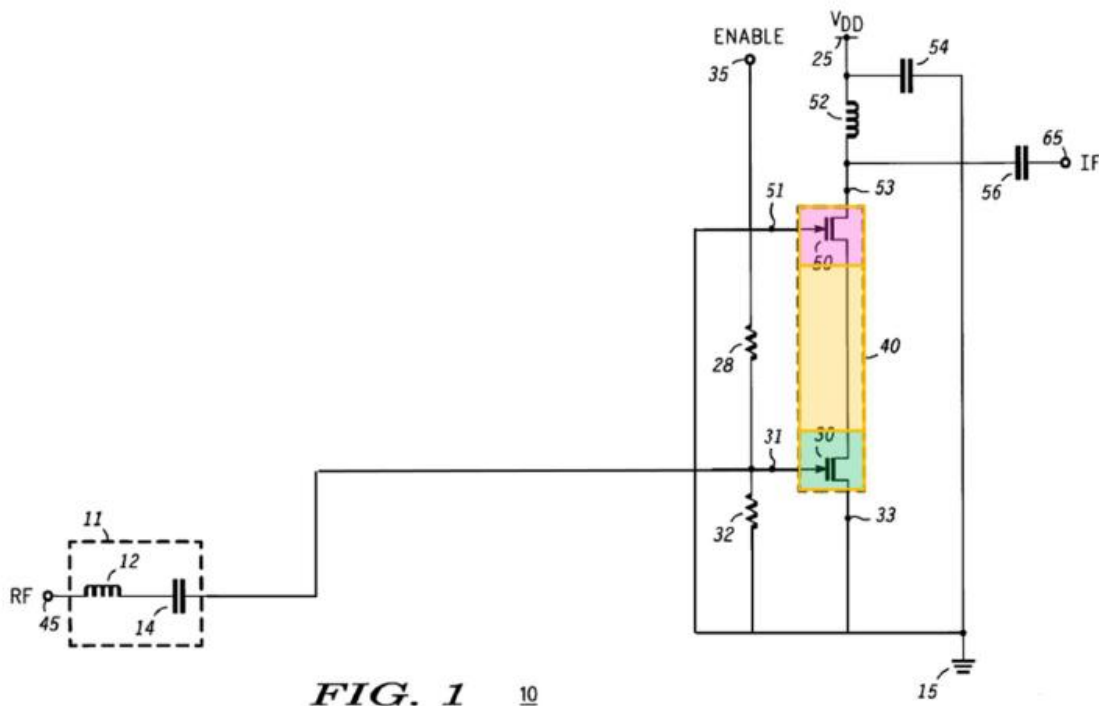
3. Analysis of Claim 1

- a) *Disputed Limitation*: “the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level”

Claim 1 recites “the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second

portion of the transistor reaches a predetermined level.” Ex. 1001, 15:53–56.

According to Petitioner, a person of ordinary skill in the art would have modified Bonn for signal amplification according to the teachings of Mizuta to arrive at the structure shown in the modified version of Figure 1 of Bonn, which is reproduced below:

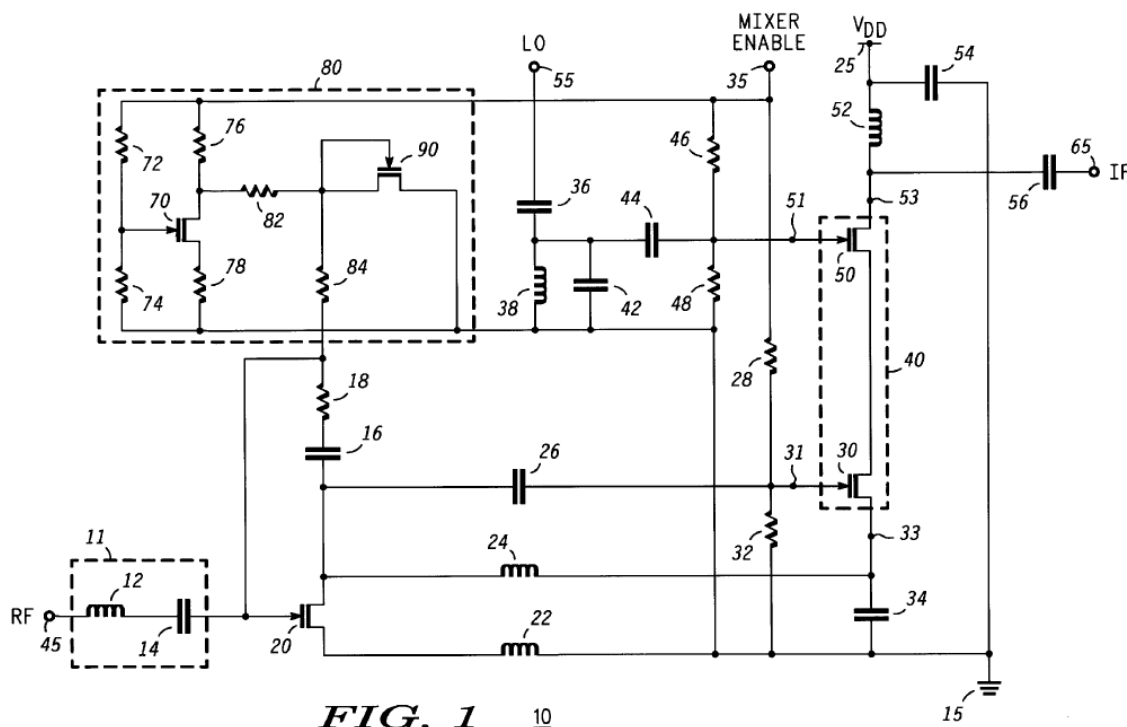


Pet. 40. According to Petitioner, modified Figure 1 depicts Bonn’s structure, “modified for signal amplification.” *Id.* Petitioner argues that, in the modified structure, the gate of second transistor 50 “is connected to the constant voltage source,” depicted in modified Figure 1 by the connection of second gate terminal 51 to power supply conductor 15. *Id.*

Patent Owner argues that Bonn teaches connecting the gate of the second transistor to a non-constant voltage source, that Petitioner fails to show sufficiently that a person of ordinary skill in the art would have modified Bonn to remove that connection, and that Petitioner’s proposed

modification would have rendered Bonn inoperable for its intended purpose. Prelim. Resp. 8–33. On the present record, we are persuaded that Petitioner has overcome these arguments sufficiently for purposes of the present Decision.

As Patent Owner argues, the unmodified teaching of Bonn includes a non-constant voltage source coupled to the gate of the second transistor. This is shown in Figure 1 of Bonn, reproduced below.



Ex. 1006, Fig. 1. In particular, Figure 1 of Bonn depicts local oscillator 55 coupled to the gate of second transistor 50. *Id.* Petitioner does not, however, rely on the unmodified structure of Bonn. Instead, Petitioner argues that a person of ordinary skill in the art would have modified Bonn's structure to conduct signal amplification instead of signal mixing. Pet. 19–25. Under this modification, as shown in Petitioner's modified version of Figure 1, Petitioner argues that a person of ordinary skill in the art would

have removed local oscillator 55 and its connection to the gate of second transistor 50. *Id.* at 19–25, 40–41.

Patent Owner argues that Petitioner does not show sufficiently that a person of ordinary skill in the art would have had a reason to modify Bonn to remove local oscillator 55. Prelim. Resp. 13–15. We disagree. Petitioner argues that, “[i]n addition to using Figure 7’s ‘dual gate FET structure in high frequency signal mixing’ applications . . . , Bonn discloses using this dual gate FET in ‘**other** applications such as high frequency signal amplification.’” Pet. 22 (quoting Ex. 1006, 11:26–37). Indeed, Bonn does suggest using its structure for signal amplification. Ex. 1006, 11:26–37 (“the dual gate FET structure of the present invention can be tailored to provide superior performance . . . in . . . other applications such as high frequency signal amplification”). On the present record, this appears to have provided the motivation for a person of ordinary skill in the art to use Bonn for amplification instead of for signal mixing. Petitioner relies on the testimony of Dr. Bernstein to show the modifications that a person of ordinary skill in the art would have considered necessary in order to convert Bonn’s structure for signal-amplification use. Pet. 23–25 (citing Ex. 1003 ¶¶ 98–109). In particular, Petitioner cites Dr. Bernstein’s testimony that a person of ordinary skill in the art “would have found it obvious to remove Figure 1’s LO (local oscillator) port 55 and its associated impedance matching components because the LO signal is no longer being mixed.” Ex. 1003 ¶ 98; see Pet. 23. Dr. Bernstein supports this testimony with citations to Bonn and with reasoning regarding why a person of ordinary skill in the art would have made this modification. Ex. 1003 ¶ 98 (citing Ex. 1006, 1:20–23, 3:19–21, 3:30–41). Accordingly, on the present record,

we are persuaded that Petitioner has shown sufficiently that a person of ordinary skill in the art would have had reason to modify Bonn's structure to remove the connection between a local oscillator and the gate of the second transistor.

Finally, Patent Owner argues that Petitioner's proposed modification would have rendered Bonn inoperable for its intended purpose because the modification would eliminate the ability of Bonn's structure to conduct high frequency signal mixing. Prelim. Resp. 26–27. As Patent Owner notes, one purpose of Bonn is to mix high-frequency signals. Ex. 1006, 11:33–36. But Bonn itself teaches using its structure for “other applications,” including “high frequency signal amplification.” *Id.* at 11:33–37. Thus, on the present record, we are persuaded that Petitioner's proposed modification does not render Bonn inoperable for its intended purpose so much as it acknowledges the modifications necessary to convert Bonn from one of its intended purposes to another.

Thus, Petitioner has shown sufficiently for the purpose of the present Decision that a person of ordinary skill in the art would have had reason to combine Bonn and Mizuta and that the combination of Bonn and Mizuta teaches or suggests the disputed limitation of claim 1. We encourage the parties to develop the arguments and the record surrounding this issue further during the trial.

b) Undisputed Limitations

Claim 1 also recites

1. A merged cascode transistor circuit comprising:
 - an input voltage signal source having an input voltage signal;
 - a constant voltage source having a predetermined constant voltage;

- a merged cascode transistor comprising:
 - a semiconductor element;
 - a source electrode electrically connected to a top surface of the semiconductor element;
 - a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
 - a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
 - a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
- wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and . . . , wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

Ex. 1001, 5:25–61. Petitioner argues that the combination of Bonn and Mizuta teaches or suggests these limitations. Pet. 29–40, 45–48.

After reviewing Petitioner’s arguments and information regarding the limitations identified immediately above, including the Bernstein Declaration, which are not addressed by Patent Owner at this stage (*see* Prelim. Resp. 8–33), we are persuaded that Petitioner sufficiently demonstrates, for purposes of deciding whether to institute trial, that the combination of Bonn and Mizuta teaches or suggests these limitations.

c) Conclusion Regarding Claim 1

Based on the current record, we determine that there is a reasonable likelihood that Petitioner will prevail in demonstrating that claim 1 is unpatentable as obvious over the combination of Bonn and Mizuta. Accordingly, we institute *inter partes* review with respect to all claims and all grounds asserted in the Petition.

E. Remaining Asserted Grounds

Petitioner argues that claims 1–16 of the '003 patent would have been obvious over the combination of Bonn, Ren, and Mishra. Pet. 48–82. Petitioner also argues that claims 1–16 would have been obvious over the combination of Mishra and Ren. *Id.* at 82–114.

Because Petitioner demonstrates a reasonable likelihood of success in proving that at least one claim of the '003 patent is unpatentable, we institute on all grounds and all claims raised in the Petition. See 37 C.F.R. § 42.108(a). Therefore, at this stage of the proceeding, it is not necessary for us to provide an assessment of every challenge raised by Petitioner. The remaining obviousness challenges, in our view, are best left for trial after full development of the record.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one challenged claim of the '003 patent. Accordingly, we institute *inter partes* review of all challenged claims on all grounds asserted in the Petition.

Our factual findings, conclusions of law, and determinations at this stage of the proceeding are preliminary and based on the evidentiary record developed thus far. This is not a final decision as to the patentability of

claims for which *inter partes* review is instituted. Our final decision will be based on the record as fully developed during trial.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted for claims 1–16 of the '003 patent on the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

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