

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

Case No. IPR2025-00094
Patent No. 8,264,003

DECLARATION OF DAVID K. CHOI, Ph.D.

Infineon Exhibit 2004 Innoscence v. Infineon IPR2025-00094
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I, David K. Choi, Ph.D., declare:

I. INTRODUCTION

1. I have been retained as an independent expert witness by Wolf, Greenfield & Sacks, P.C., counsel for Patent Owner Infineon Technologies Americas Corp. (“Infineon” or “Patent Owner”) to provide my opinions concerning a Petition for *inter partes* review (IPR) filed by Petitioner Innoscience America Inc. (“Innoscience” or “Petitioner”) challenging claims 1-16 (“Challenged Claims”) of U.S. Patent No. 8,264,003 (“the ’003 patent”). I am being compensated for my time at my standard rate plus actual expenses. My compensation is not dependent in any way upon the outcome of the *inter partes* review of the ’003 patent.

II. BACKGROUND AND QUALIFICATIONS

2. I received my B.S. degree in physics from the University of California, Berkeley, in 1993, my M.S. degree in Electrical and Computer Engineering from California State University, Fullerton, in 1996, and my Ph.D. degree in Electrical and Computer Engineering from the University of California, Santa Barbara, in 2001. By March 2006, I had earned a Ph.D. in Electrical and Computer Engineering and had over 12 years of professional and academic experience in research and product development in digital integrated circuit (IC)

design, analog circuit design, RF/Microwave circuit design, wireless communications, and semiconductor electronics.

3. From September 1993 to July 1994, I worked as a research assistant in the Department of Physics at the University of California, Irvine. In this role, I was responsible for the analysis and design of a cryogenic camera system for mid-Infrared imaging of deep space phenomenon using (at the time) the largest available (1 Megapixel, 1024x1024) Charge Coupled Device (CCD) and custom Fabry-Perot Interferometer.

4. From January 1995 to August 1996, I worked as a Digital Design Engineer at Western Digital Corporation in the ASIC design group (acquired by Adaptec Inc.). In this role, I used a number of industry-standard VLSI design tools from Cadence, Synopsis, Meta, etc. to perform static critical delay analysis, characterize and generate libraries for custom digital logic cells, and to analyze and design clock trees and custom ASIC pad driver cells. I received an award for outstanding achievement for developing a “no re-spin” solution to correct a design error preventing a new ASIC from being powered on, and was recognized for my analysis of circuit and system level meta-stable logic.

5. I worked at the Nokia Research Center as a Senior Research Engineer from April 2001 to March 2006. In that role, I designed, built, and tested RF circuits, RF systems, and power management systems. My work included

designing a novel LDMOS-based Chireix Outphasing (base station) transmitter for UMTS systems, development of an OFDM RF system simulator (with physical impairments and forward error correction (FEC)), development of baseband PAPR reduction techniques for OFDM radio systems, and development of a high power, high precision, 16-bit digitally-controlled (Half-bridge) switched-mode power supply.

6. From July 2006 to February 2007, I worked as a group leader and staff engineer in the Infrastructure Products Group at RF Micro Devices. In that role, I worked on advanced product development, including the development of a GaN HEMT dual carrier UMTS Doherty base station transmitter and a scalable GaN HEMT non-linear simulator model.

7. From March 2007 to July 2008, I worked as a Section Manager of the Technology Strategy Team in Technology Intelligence & Collaboration at Samsung Electronics. In that role, I worked on technical feasibility and business opportunity analysis of nanotechnology, and market and technical analysis of biomedical electronics and THz imaging.

8. From July 2008 to February 2011, I worked as a Technical Manager and Principal Engineer in the Advanced Development Group at Aethercomm, Inc. In that role, I worked on product development of pulsed/CW wideband, high power RF transmitters implemented in silicon LDMOS, GaAs FET and HBT, and

GaN HEMT device technologies. I also worked on the design of other RF/microwave components such as transformers, baluns, power detectors, switches, filters, magnetics (including inductors with and without ferrites), phase shifters, frequency control, signal processing elements and rectangular waveguides, microwave cavities, as well as, DC power management systems (including full and half-bridge converters), control logic, temperature compensation, fault protection, etc.

9. From May 2011 to December 2012, I worked as a Senior R&D RF Hardware Engineer in R&D Hardware Engineering at LGS Bell Labs Innovations. In that role, I developed high power, highly-linear, and efficient RF transmitter solutions for various wireless standards (including GSM/EDGE, CDMA, WCDMA, and LTE) using peak to average power reduction (PAPR) techniques, analog and digital (pre-distortion) linearization, and various high-Q (SAW, BAW, FBAR, ceramic, and cavity) filters.

10. From August 2013 to March 2014, I worked as a Technical Director in the RF/microwave Power Amplifier Business Unit at Mercury Systems, Inc. In that role, I directed and led all aspects of Mercury Systems' RF/microwave Power Amplifier Business Unit.

11. Since February 2012, I have been the Principal and Owner of RF Design Concepts, Ltd. In this role, I provide consulting services, including product

design and development related to RF/microwave circuits, power amplifiers, power management systems, semiconductor fabrication, advanced IC packaging, as well as for nascent scientific research/technologies.

12. In addition to my work experience in industry, I have also taught electrical engineering (Microelectronics, i.e., semiconductor circuits, diodes, transistors, and transistor circuits) at the university level. From March 2013 to March 2014 and from August 2015 to August 2016, I was an Adjunct Professor in the Department of Electrical, Computer, and Energy Engineering at the University of Colorado, Boulder. Also, from August 2004 to August 2008, I was a Visiting Scholar in the Department of Electrical & Computer Engineering at the University of California, San Diego. I have several published articles in the field of electrical engineering and power amplifier design, including adaptive impedance matching. A list of these publications can be found in my curriculum vitae, which is provided as Ex-2005.

13. I note that Dr. Bernstein candidly admitted several times at his deposition that he was “not an expert in RF circuits.” Ex-2009, 46:18-20, 60:20-21, 72:20-21. As explained above, unlike Dr. Bernstein, I am an expert in RF circuits and am very familiar with cascode circuits, the subject matter of the ’003 patent.

III. MATERIALS REVIEWED AND CONSIDERED

14. My findings, as explained below, are based on my years of education, research, experience, and background in the field of electrical engineering and power amplifier design, as well as my investigation and study of relevant materials for this declaration. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth in Section V below. In forming my opinions, I have studied and considered the Petition (Paper 1), the Board’s Institution Decision (Paper 9), and the materials listed in Appendix A.

IV. LEGAL PRINCIPLES

15. I am not an attorney. My role in this matter is primarily to explain technical information to assist a fact finder. I have therefore been advised by Infineon’s counsel of the relevant legal principles so that my testimony will be more helpful for the Board. Below is my understanding of those legal principles based on my communications with Infineon’s counsel and my prior experience with patent litigation matters. I applied the legal principles below, as necessary, in reaching my opinions.

A. IPR Proceedings & Burden of Proof

16. I understand that “*inter partes* review” (IPR) is a proceeding before the United States Patent & Trademark Office for evaluating the patentability of an issued patent’s claims based on prior-art patents and printed publications.

17. I understand that, in this proceeding, Petitioner has the burden of proving that the challenged claims of the '003 patent are unpatentable by a preponderance of the evidence. I understand that “preponderance of the evidence” means that a fact or conclusion is more likely true than not true.

B. Level of Skill in the Art

18. I understand that a person of ordinary skill in the art (“POSA”) provides a reference point from which the claimed invention(s) should be viewed. I understand that a POSA is a hypothetical person who is presumed to be one who thinks along the lines of conventional wisdom in the art and has ordinary creativity. I understand that a POSA is presumed to have knowledge of all the publications that are sufficiently related to the pertinent art (the “prior art”), and to have knowledge of all arts reasonably pertinent to the particular problem that the claimed invention addresses.

19. I understand that when assessing the level of ordinary skill for a given patent, relevant factors include (1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.

20. Taking the above factors into account, I provide my opinions regarding the level of ordinary skill for the '003 patent in Section V, below.

C. Claim Interpretation

21. I understand that, in IPR proceedings, claim terms in a patent are given their ordinary and customary meaning as understood by a POSA after reviewing the “intrinsic evidence,” which includes the language of the claims, the patent specification, the prosecution history (meaning the back and forth between the patent applicant and the examiner at the Patent Office), and documents cited on the face of the patent and/or during its prosecution history.

22. I understand that if the specification or prosecution history provides a special definition for a claim term that differs from the meaning the term would otherwise possess, that special definition applies. But I understand that it is otherwise normally improper to import limitations from the intrinsic evidence into the claims.

23. I understand that if the specification or prosecution history does not provide a special definition for a claim term, “extrinsic evidence” (i.e., evidence other than that included in the definition of intrinsic evidence) may also be relevant to assessing what the ordinary and customary meaning as understood by a POSA. Extrinsic evidence can include technical references not cited in the patent or its prosecution history, and statements by the patent owner and other experts in the field. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of skill in the art at the

time of the alleged invention. This can be useful for technical terms whose meaning may differ from their ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

24. I have applied these standards in preparing the opinions in this declaration.

D. Obviousness

25. I understand that for an invention claimed in a patent to be patentable, it must be, among other things, not obvious from the prior art. I understand that an invention is obvious if the differences between the patented subject matter and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made.

26. I understand that an invention is not rendered obvious simply on the basis of two or more different disclosures that collectively disclose all of the claimed elements. In other words, an invention is not obvious just because all of the elements that comprise the invention may have been known in the prior art. Instead, a person of ordinary skill in the art must have had a reasonable expectation of success in pursuing the possibility that turns out to succeed and is claimed.

In particular, I understand that knowledge of a goal does not itself render achievement of that goal obvious.

27. I also understand that determining whether or not a claimed invention would have been obvious requires assessing facts related to (1) the scope and content of the prior art, (2) the differences between the prior art and the claimed invention, (3) the level of ordinary skill in the art, and (4) any objective evidence of non-obviousness. I understand that this is known as consideration of the “*Graham* Factors.”

28. I further understand that an invention is not obvious just by demonstrating that each of its elements was, independently, known in the prior art. To prove that an invention is obvious, I understand that it can be important to point to a reason or reasons, such as a teaching, suggestion, or motivation, that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed invention does. I understand that this is because inventions in most (if not all) instances rely upon building blocks already known, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known; therefore, it can be important to point to such a reason or reasons. I understand that in identifying such a reason, the analysis need not require precise teachings in the prior art directed to the specific subject matter of the challenged claim.

29. I understand that while it is possible for expert testimony to supply a limitation missing from the prior art, the limitation in question must be shown to be unusually simple, and the claimed technology must be shown to be particularly straightforward.

30. I understand that it will often be necessary for a fact finder to look to interrelated teachings of multiple patents and the background knowledge possessed by a person having ordinary skill in the art in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. I understand that when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. I understand that the combination of familiar elements according to known methods may be obvious when it does no more than yield predictable results.

31. I also understand that a claim is not invalid as obvious if it is more than the predictable use of prior art elements according to their established functions.

32. Further, I understand that while predictability is a touchstone of obviousness, the concept of a “predictable result” under the law refers not only to

the expectation that prior art elements are capable of being physically combined, but also that the combination would have worked for its intended purpose.

33. I also understand that if the prior art teaches away from combining known elements in the manner claimed by the invention at issue, discovering a successful way to combine them is less likely to be obvious. In particular, I understand that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant, or would understand based on the reference that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant. Likewise, I understand that similar subject matter may not be sufficient motivation for a person of skill in the art to combine references if the references have conflicting elements.

34. Further, I understand that even if a reference does not necessarily "teach away," its statements regarding preferences are relevant to a finding regarding whether a person of ordinary skill would have had reason to combine that reference with another reference.

V. PERSON OF ORDINARY SKILL IN THE ART ("POSA")

35. I understand that a patent and prior-art references must be assessed from the perspective of a person having ordinary skill in the art ("POSA") to which

the patent is related, based on the understanding of that person at the time of the patent claim's priority date. I have been asked to provide my opinions as to the state of the art in the 2006 timeframe.

36. When I refer to a POSA, I am referring to one of ordinary skill in 2006, unless specified otherwise, even if I do not say so specifically in each case. I have applied this standard throughout my declaration.

37. I understand that Petitioner and Petitioner's expert, Dr. Joseph B. Bernstein, Ph.D. have proposed that a person of ordinary skill in the art (the Petition and Dr. Bernstein use the abbreviation "POSITA," but that is synonymous with POSA as I use) as of 2006 would be someone that would have had at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design and that additional education could substitute for professional experience and vice versa. Petition, 5; Bernstein, [067]-[069].

38. Taking the factors I describe in Section IV.B, above, into account, along with my personal experience working in the field and my knowledge of colleagues and others working in that field, I believe that a person of ordinary skill in the art of the '003 patent would be an individual who would have possessed at least a four-year degree in electrical engineering or a closely related field, and at

least two years of experience in semiconductor device design *and fabrication* and additional education could substitute for professional experience and vice versa.

39. While Dr. Bernstein's opinion and Petitioner's definition of a POSA differ slightly from my opinion, the difference is insignificant in the context of my opinions in this declaration. For the sake of simplicity, I have based my opinions on the level of skill as Dr. Bernstein and Petitioner define it, but my opinions would be the same if I applied my own definition. I have worked with many people who fit the characteristics of the POSA, and I am familiar with their level of skill. When developing the opinions set forth in this declaration, I assumed the perspective of a POSA as set forth above. My opinions are from that perspective even when I do not specifically say so.

40. As explained above in Section II, I possessed at least the above skill level as of 2006.

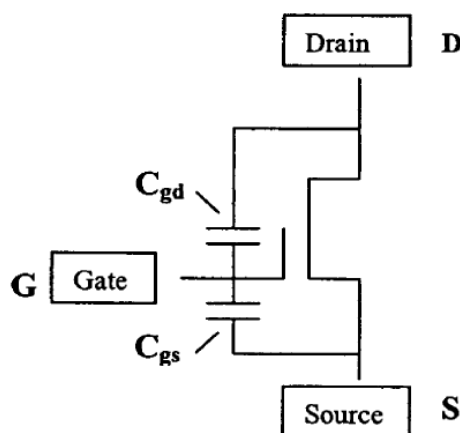
VI. '003 PATENT

A. Background

41. The '003 patent, titled "Merged Cascode Transistor," issued on September 11, 2012, from U.S. Application No. 11/688,338 (the "'338 Application"), which was filed on March 20, 2007, and claims priority to U.S. Provisional Application No. 60/783,934, which was filed on March 20, 2006. Ex-1001 ('003 patent) at face.

1. Field Effect Transistors

42. A “field effect transistor (FET)” is an electrically controlled switch that can permit or inhibit conduction between a “drain” and a “source” at a “gate” that “control[s] current flow between the drain and the source.” *Id.*¹, 1:29-31, Fig. 1 (reproduced below).



PRIOR ART

43. The transistor’s gate either permits or inhibits conduction between the source and drain by applying a voltage to the gate that exceeds a threshold. The application of the voltage at the gate changes the underlying semiconductor from a conductor to an insulator, or vice versa, depending on the transistor’s design.

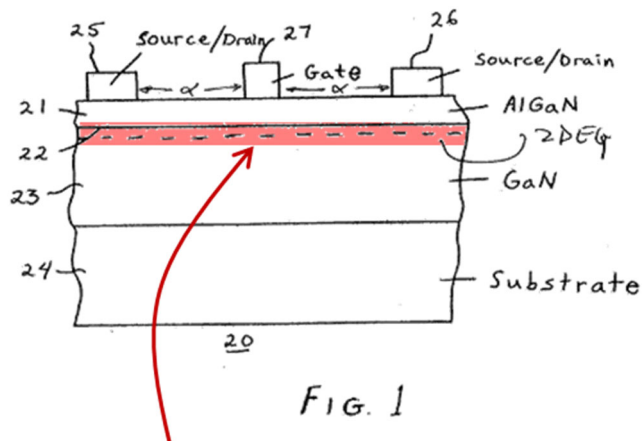
44. Transistors that are “normally ON” are also known as “depletion-mode” transistors, which means that a conductive “channel” exists between the

¹ “*Id.*” is an abbreviation for the Latin term “*idem*,” which means “the same,” and simply refers to the previously cited source.

drain and source even when a voltage is not applied to the gate. *Id.*, 2:54-55. In depletion-mode transistors, conduction between the drain and source is inhibited when the channel is removed by applying a voltage exceeding the threshold voltage between the gate and source. *Id.* Transistors that are “normally OFF” are known as “enhancement mode” transistors, which means that there is no conductive channel between the drain and source when no voltage, or a voltage not exceeding the threshold voltage is applied between the gate and source, while a conductive channel forms between the drain and source when a voltage exceeding the threshold voltage is applied between the gate and source. *Id.* at 2:59-61.

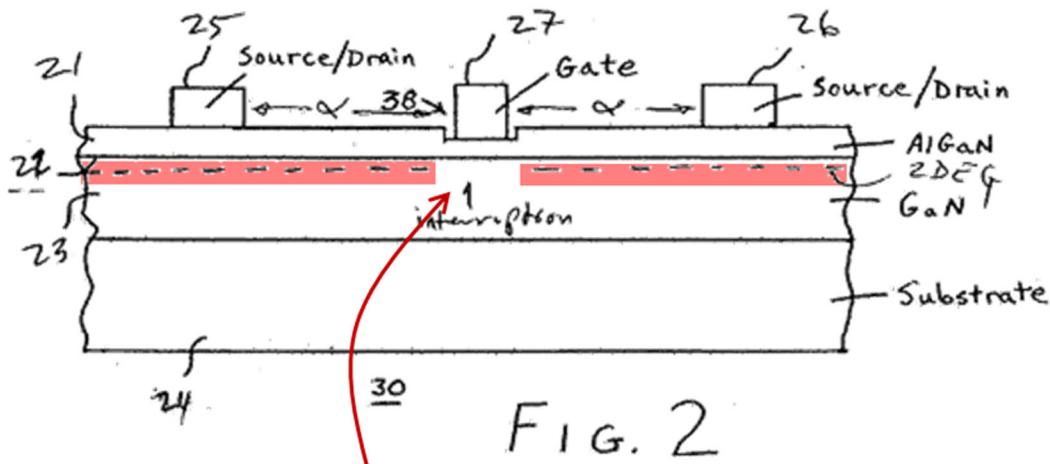
45. U.S. Patent Publication No. 2005/0189561 (Ex-1005, “Kinzer”), which is cited on the face of the ’003 patent, provides an example of both a depletion-mode transistor that is normally on and an enhancement mode transistor that is normally off. Ex-1005, [0013]-[0014], Figs. 1 and 2 (annotated below).

Depletion-Mode (Normally On) Transistor



Two-dimensional electron gas
("2DEG") permits conduction
between source and drain past gate

Enhancement Mode (Normally Off) Transistor



Break in 2DEG inhibits conduction
between source and drain at the gate

46. The '003 patent discloses that "FETs" are "used in large switching applications, for example, in DC-DC power converters." Ex-1001, 1:31-33. "Large drain-source voltage (V_{ds}) swings during switching create a large 'Miller effect' and, as a result, excessive switching losses." *Id.*, 1:31-33. "In addition, high dV/dt

changes” (dV/dt is the rate of change in voltage as a function of time), “at the drain (D) may result in a voltage transient VG1 at the gate (G),” which may turn the transistor [] ON briefly when not desired.” *Id.*, 1:39-44. “This unwanted period of conduction may result in rather large power and efficiency losses.” *Id.*, 1:44-45.

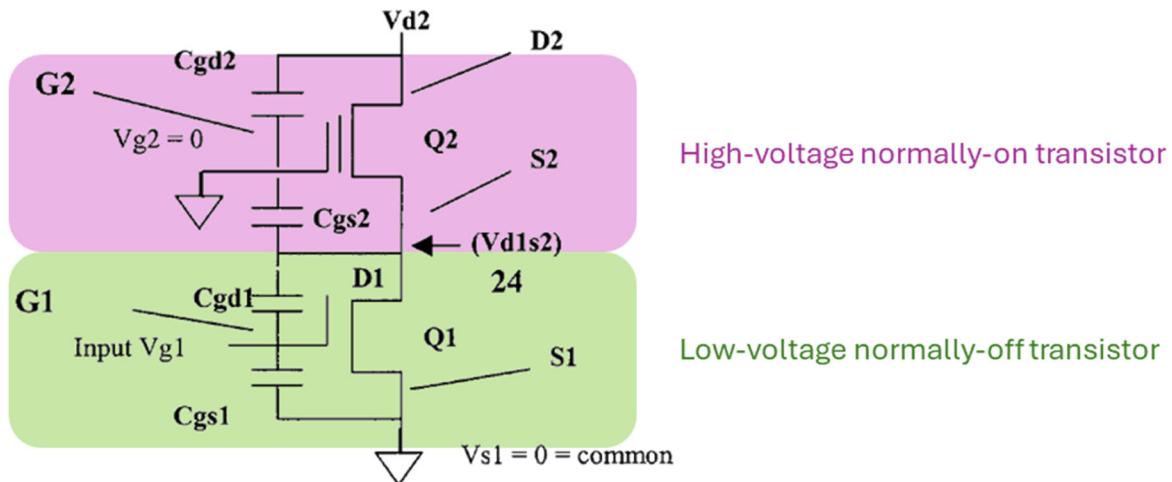
2. Cascode Circuit

47. The '003 patent discloses and claims a “merged cascode transistor” circuit. “Cascode” refers to a configuration of transistors, for example, “suitable for use in high voltage, high speed switching applications,” where the source of a high-voltage normally-on transistor (see below, purple) is connected to the drain of a low-voltage normally-off transistor (see below, green) and the gate of the high-voltage normally-on transistor is connected to the “common” return (usually 0 Volts). *Id.*, 2:48-3:50, Fig. 2 (annotated below). According to Dr. Bernstein, “to be a cascode, the only requirement is that the drain of we’ll call it the lower transistor is connected directly to the source of an upper transistor.”² Ex-2009, 13:7-11, but that is not the “only requirement.” While it is necessary for the drain of the lower

² At his deposition, Dr. Bernstein testified that a cascode is “not such a normal device.” Ex-2009, 188:7-17. He explained that “most people, especially who are not engineers, are not familiar with how a cascode works in general, even engineers.” *Id.* Dr. Bernstein continued that “[e]ven someone who can be an **electrical engineer, it’s not such a normal device.**” *Id.* While Dr. Bernstein may not be familiar with cascodes given that he candidly admitted that he was “not an expert in RF circuits” (Ex-2009, 46:18-20, 60:20-21, 72:20-21), I am an expert in RF circuits and am very familiar with cascode circuits.

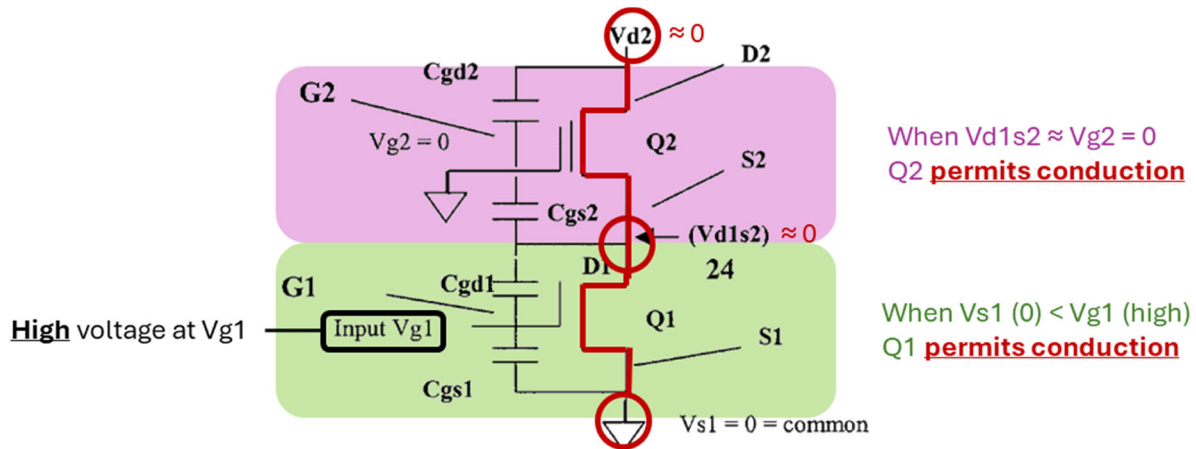
transistor to be directly connected to the source of the upper transistor, the upper transistor must also be biased such that it conducts when the lower transistor conducts, as discussed below.

Figure 2 (Annotated)



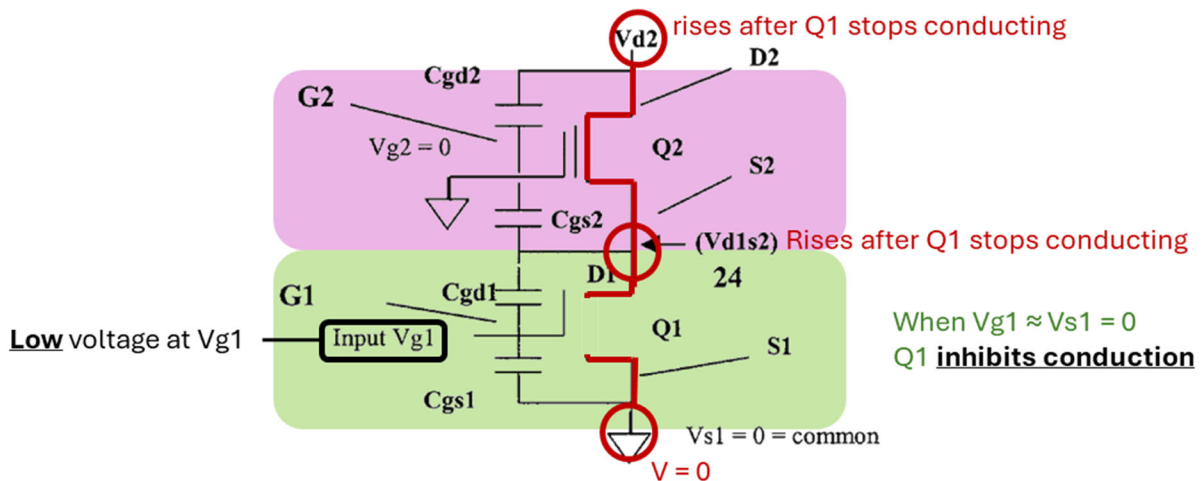
48. “In operation, when the input voltage signal provides a high voltage at Vg1,” the gate of the bottom transistor “Q1 is conducting.” Ex-1001, 2:64-65. Because the voltage at the bottom transistor’s source (“Vs1”) is always “0” (*id.*, Fig. 2), the “voltage at the node 24 (Vd1s2) at this time is low, substantially 0V” (*id.*, 3:31-34). On the top transistor, because the voltage at Vd1s2 (“substantially 0V”) is substantially the same as the voltage at Vg2, which “is set to 0,” the top transistor “is fully ON and is fully conducting” too. *Id.*, 3:2-6.

**When the Input Voltage is High,
Both Q1 and Q2 Transistors Permit Conduction**



49. “When the input voltage at V_{g1} ... goes low, the bottom portion Q1 turns OFF ... [and] stops conducting.” *Id.*, 3:10-12. “As a result, the voltage at the node 24 (V_{d1s2}) rises” because Q2 is still conducting. *Id.*, 3:12-13.

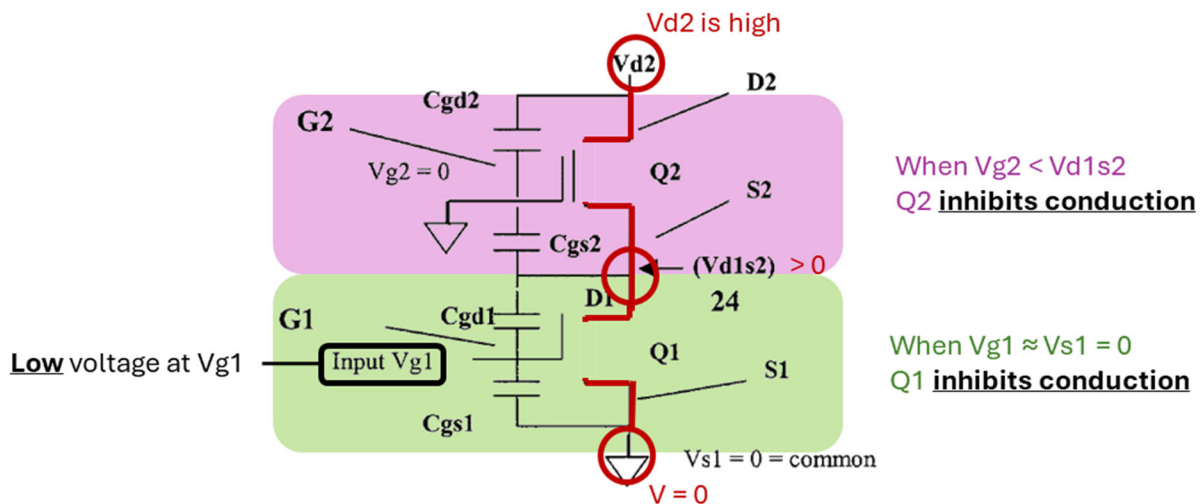
When the Input Voltage Goes Low, Q1 Stops Conducting and V_{d1s1} Rises



50. The voltage at V_{d1s1} continues to rise “until the gate-source voltage (V_{gs}) of the top portion Q2 reaches the pinch off voltage ... and the top portion Q2 turns OFF.” *Id.*, 3:14-15. “Thereafter, the drain voltage V_{d2} of the top portion Q1

risers to the full supply voltage.” *Id.*, 3:16-17. Thus, “the voltage at node 24 (V_{d1s2}) never rises above the magnitude of the pinchoff voltage,” which is “set low,” so that the voltage swing of the bottom portion q1 “is substantially reduced” and is “only a few volts.” *Id.*, 3:18-25. “This is a much smaller swing than would occur if a single FET were used alone as a switching device.” *Id.*, 3:25-27.

When the Input Voltage is Low and the Gate-Source Voltage of Q2 Reaches the Pinch-Off Voltage, Both Q1 and Q2 Transistors Inhibit Conduction



51. This cascode configuration reduces the “Miller effect” ... and thus power losses are also substantially reduced as well.” *Id.*, 3:30-31. “The dV/dt ,” or change in voltage as a function of time, “at the drain (D1) of the bottom portion Q1,” the low-voltage transistor, “is also reduced, thus, the capacitively coupled voltage transient V_{G1} is also reduced.” *Id.*, 3:31-34.

3. III-Nitride Transistors

52. Claims 2-16 all require that the semiconductor comprises two layers of a “III-Nitride” material. A “III-Nitride” material is one that includes nitrogen and at least one Group III element. Group III elements are those in the third column of the periodic table and include boron (B), aluminum (Al), gallium (Ga), indium (In), and thallium (Tl). GaN and AlGaN are examples of III-Nitride materials disclosed in the specification and which are expressly claimed (*see* claims 4-9 and 12-16).

53. By March 20, 2006, which the Petition identifies as the “earliest claimed priority of the ’003 patent” (Petition, 2, citing Ex-1003, [062]), GaN was still a relatively new technology. International Rectifier, the employer of Thomas Herman (the sole named inventor of the ’003 patent), had no active effort to specifically fabricate enhancement mode GaN transistors because that was deemed a “more difficult task,” according to Mr. Herman. Ex-2003, 30:2-15 (“**Q.** Did you design semiconductors with enhancement mode gates while you were at IR? **A.** The bulk of the effort at IR was depletion mode gates and transistors in GaN. **Q.** Did you also design enhancement mode transistors in GaN? **A.** There was interest in designing enhancement mode GaN transistors, but *that was deemed a more difficult task*. And I don’t believe there was any active effort to specifically fabricate enhancement mode GaN transistors, other than, you know, feasibility and

discussions. But I don't believe there was any effort to physically fabricate an enhancement mode GaN device.”).

54. The '003 patent expressly claims, not only a GaN enhancement mode transistor, but a GaN transistor that has at least two transistors merged together with a drain region of an enhancement mode transistor merged with the source region of a depletion mode transistor. This was a completely novel concept, as evidenced by the Petition relying entirely on obviousness combinations, finding no reference that disclosed the claimed invention. The novelty of the claimed invention of the '003 patent is all the more evident in that the Petition and the Bernstein Declaration fail to cite any prior art that discloses a GaN transistor comprising an enhancement mode transistor merged with a depletion mode transistor – the very limitation that the Bernstein Declaration acknowledges conferred the claims’ patentability during prosecution. Ex-1003, [076], citing Ex-1002, 18 (reasons for allowance).

B. Claimed Inventions

55. The Challenged Claims (claims 1-16, reproduced in Appendix B) are all directed to “***merged***” cascode transistor circuits that include a “***merged*** cascode transistor.” *Id.* at claims 1 and 10. One feature of a merged cascode transistor is that the “drain region of the enhancement mode transistor is merged with [the] source region of the depletion mode transistor.” *Id.* In other words, the transistor

claimed “is a single device and not two separate FETs.” *Id.*, 2:52-53. Examples of the claimed merged cascode transistors are shown in cross-section in Figures 3 and 4 (annotated below).

Figure 3 (Annotated)

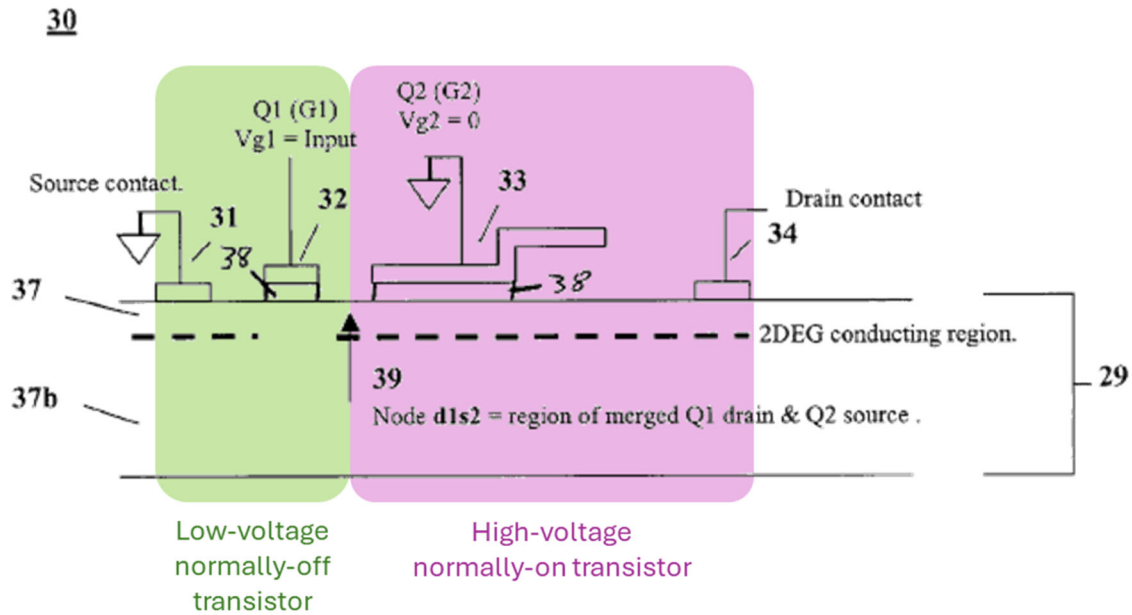
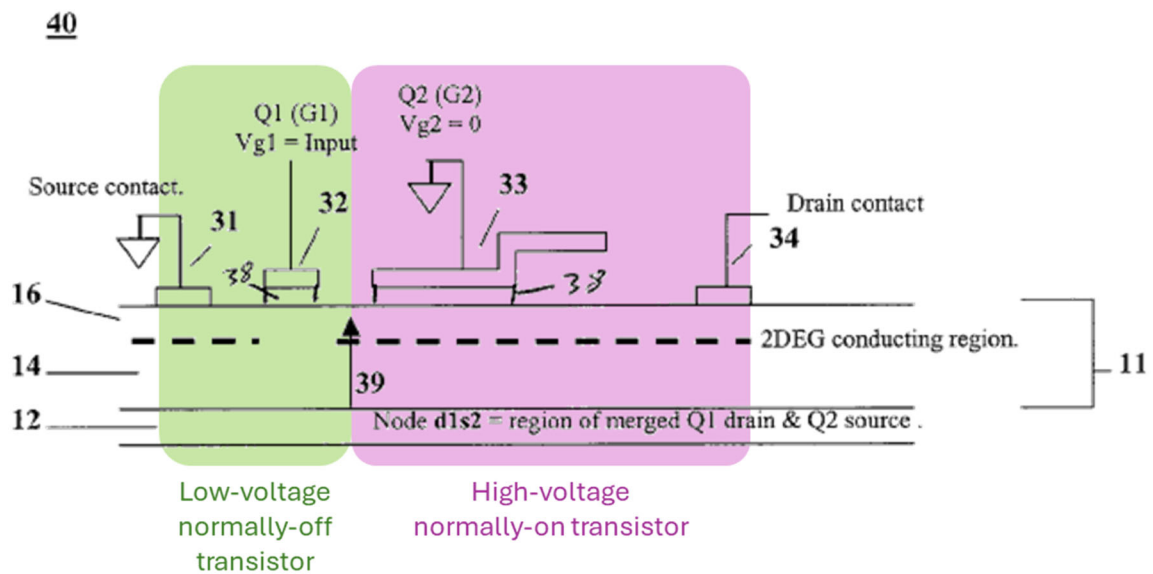


Figure 4 (Annotated)



56. In each of the above examples of a merged cascode transistor, there is “a source electrode [that is] electrically connected to a top surface of the semiconductor element” (*id.* at claims 1 and 10). The source electrode (also known as a contact, as indicated) is shown on the left side of Figs. 3 and 4 as reference numeral 31. *Id.*, 3:64-65, 4:31-32. “[A] drain electrode [is] electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode” (*id.* at claims 1 and 10), the drain electrode (also known as a contact, as indicated) is shown on the right side of the figures as reference numeral 34 (*id.*, 4:3-4, 4:33). “[A] first gate [is] positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor,” which “is an enhancement mode [(normally off)] transistor.” *Id.* at claims 1 and 10. “[A] second gate [is] positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, which “is a depletion mode [(normally on)] transistor.” *Id.*

57. Instead of the enhancement mode transistor, shown on the left side of the figures, above, having a its own drain electrode, the depletion mode transistor on the right side of the figures having its own source electrode, and an interconnection (e.g. a wire or conductor) between the respective drain and source electrodes, as would be needed for two completely separate, discrete, FETs in a

cascode configuration, the claimed *merged* cascode transistor has the “drain region of the enhancement mode transistor [] *merged* with [the] source region of the depletion mode transistor” *Id.* This results in the claimed *merged* cascode transistor “*a single device and not two separate FETs.*” *Id.*, 2:52-53. The drain region of the enhancement mode transistor is merged with the source region of the depletion mode transistor “at the node in the semiconductor element” (*id.* at claims 1 and 10), which is depicted in Figures 3 and 4 as the “arrow 39.” *Id.*, 4:4-8, Figs. 3 and 4.

VII. THE PETITION FAILS TO SHOW CLAIM 1 IS OBVIOUS OVER BONN IN VIEW OF MIZUTA (GROUND 1)

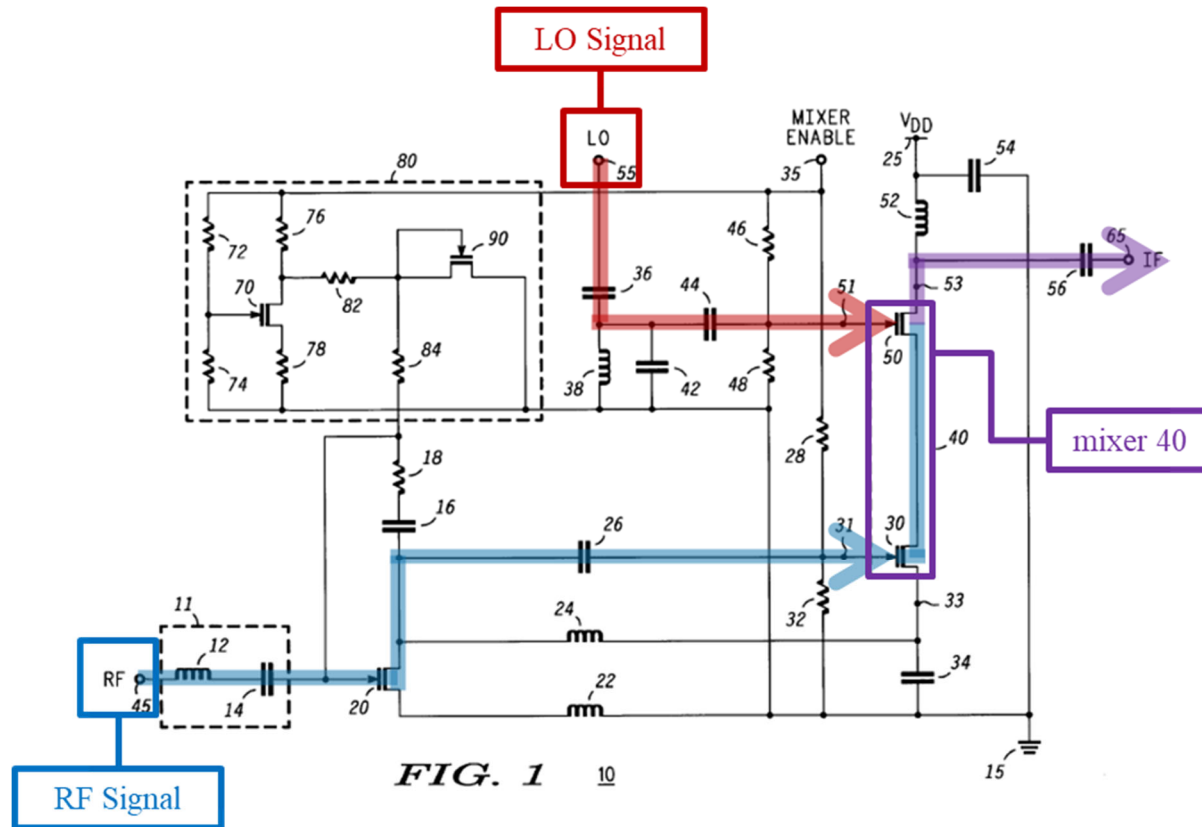
58. Ground 1 challenges only claim 1 as allegedly obvious over Bonn (Ex-1006) in view of Mizuta (Ex-1007).³ Petition, 6. Claim 1 requires, in part, “the second gate is connected to the constant voltage source” (*see* Limitation [1C7]). The Petition cites only Bonn as allegedly disclosing this limitation. Petition, 40-45. But Bonn discloses connecting both gates of its dual-gate transistor to *variable* voltage sources, **not** to a *constant* voltage source as claimed.

59. The only dual-gate transistor that Bonn discloses is purpose-built to be a mixer 40, not an amplifier. Bonn discloses that the gates 31 and 51 on its mixer 40 are each connected to variable voltage sources having “RF” (blue) and “LO”

³ See note 2, above.

(red) signals, respectively, to form an “IF” output signal (purple). Bonn at Fig. 1 (below, annotated).

Bonn, Figure 1 (Annotated)



Bonn never discloses connecting either gate of a dual-gate transistor to a constant voltage source as claimed by the '003 patent (Limitation [1C7]). *See also* Section VII.A, below.

60. Modifying Bonn based on Mizuta would not have resulted in a circuit meeting Limitation [1C7] because Mizuta fails to disclose dual-gate transistors at all. Thus, Mizuta does not teach connecting a second gate to a constant voltage

source. *See* Section VII.B, below. Ground 1 is thus based on two references, neither of which discloses Limitation [1C7].

61. Faced with two prior art references, neither of which disclose connecting the gate of a dual-gate transistor to a constant voltage source as required by the claims, the Petition, citing only the Bernstein Declaration, fabricates the claim limitation missing from the prior art using a series of assumptions and a long list of modifications to Bonn (*see* Petition, 19-25; Ex-1003 [094]-[109]) that are unsupported by Bonn (or Mizuta) and that a POSA would not have had reason to make. *See* Sections VII.C.1-5, below.

62. First, as explained in more depth in Section VII.C.1, below, making the modifications that the Petition and Bernstein Declaration argue a POSA would have transformed the basic principles of operation of Bonn's downconverter circuitry of Figure 1 to an amplifier. While Bonn discloses the hypothetical notion of using a dual-gate transistor for amplification, a POSA looking to implement Bonn's suggestion would have naturally started with circuitry that already was designed for amplification, such as the conventional, single-gate FET 20 and surrounding circuitry, which Bonn discloses is an amplifier. Ex-1006, 2:12-15. The Petition and the Bernstein Declaration provide no evidence to support the notion that a POSA would have started with Bonn's downconverter of Figure 1 and then changed its fundamental operating principle as proposed.

63. Second, as explained in more depth in Section VII.C.2, below, the Petition and Bernstein Declaration argue that a POSA would have used Bonn's dual-gate transistor shown in Figure 7 as part of an amplifier circuit. The Institution Decision largely bases its decision to institute a trial on the Petition's argument that, "[i]n addition to using *Figure 7's* 'dual gate FET structure in high frequency signal mixing' applications . . . , Bonn discloses using this dual gate FET in '*other applications* such as high frequency signal amplification.'" Paper 9, 14, quoting Petition, 22. But Bonn itself never teaches using the transistor of Figure 7 as an amplifier, as both the Petition and Institution Decision rely upon. Ex-1006, 11:33-37. While Bonn discloses the hypothetical notion of using a dual-gate transistor for amplification, Bonn never teaches using the FET of Figure 7 as the Petition suggests. *Id.* And the Petition and the Bernstein Declaration ignore the fact that Bonn's dual-gate transistor of Figure 7 was purpose-built as a mixer, and would not have been well suited to be used as an amplifier, something a POSA would have known. Specifically, the upper (second) transistor of Bonn's dual-gate mixer transistor was designed to have a current-carrying capacity greater than the lower (first) transistor so as not to cause the second transistor to saturate. While this transistor may have been well-suited as a mixer, a POSA would have known that such a transistor would not have been

optimal as an amplifier. Thus, a POSA would not have had reason to simply use Bonn's dual-gate mixer transistor as an amplifier transistor, as-is.

64. The Petition and the Bernstein Declaration, however, fail to even allege that a POSA would have modified Bonn's dual-gate mixer transistor to be used as an amplifier, let alone why a POSA would have had reason to do so, describe what modifications a POSA would have tried to make, whether a POSA would have had an expectation of success, or cite evidence in support of any such arguments. Thus, the Petition's argument that the Board based its institution on is predicated on the false presumption that a POSA would have used the dual-gate FET of Figure 7 as an amplifier, when in fact, a POSA would not have had reason to do so.

65. Third, as explained in further detail in Section VII.C.3, below, the Bernstein Declaration opines that POSAs would have made extensive modifications to the overall circuit shown in Figure 1 of Bonn (downconverter 10), to repurpose Bonn's mixer 40 as an amplifier. But the Bernstein Declaration seems to ignore the fact that Bonn's downconverter 10 already has an amplifier, FET 20, and fails to explain why a POSA would have had reason to make such extensive changes to re-purpose the overall circuit in Figure 1 (which includes both an amplifier, FET 20, and a mixer 40) so that it acts as an amplifier, much less, why a POSA would not have simply used the amplifier, FET 20, as Bonn purposefully

designed it in the first place. Obviously, using the much simpler, pre-existing amplifier, FET 20, would ***not*** have resulted in a circuit that meets claim 1. Absent any objective evidence as to why a POSA would have ignored the pre-existing amplifier, FET 20, in favor of making extensive (and ill-advised) modifications to Bonn's downconverter 10, the modifications suggested in the Petition and Bernstein Declaration amount to nothing more than impermissible hindsight.

66. Fourth, as explained in further detail in Section VII.C.4, below, Bonn discloses that both gates of its dual-gate transistor are individually driven with variable voltage signals. The Petition and Bernstein Declaration argue that POSAs would have instead connected the second gate to a constant voltage source, but again, fail to cite any objective evidence as to why a POSA would have had reason to make such a modification. Indeed, a prior art reference cited by Petitioner in its invalidity contentions for the '003 patent in connection with ITC Inv. No. 337-TA-1414, Mil'Shtein (Ex-2006), discloses that connecting the second gate of a two-gate FET to a constant voltage source as part of an amplifier "yield[ed] the worst results." Ex-2006, 302. The Petition and Bernstein Declaration fail to explain why a POSA would have reconfigured Bonn's circuitry in a way that the prior art disclosed resulted in the worst results. This again shows that the Petition and Bernstein Declaration are using nothing more than impermissible hindsight with their proposed modifications.

67. Fifth, as explained in further detail in Section VII.C.5, below, the Bernstein Declaration opines that a POSA would have stripped away Bonn's temperature compensation power supply without any explanation. This proposed modification further establishes the Petition's and the Bernstein Declaration's use of hindsight as the reason for the modification and not any reasoning based on evidence from the prior art.

68. Thus, the Petition and the Bernstein Declaration fail to show that claim 1 of the '003 patent is obvious.

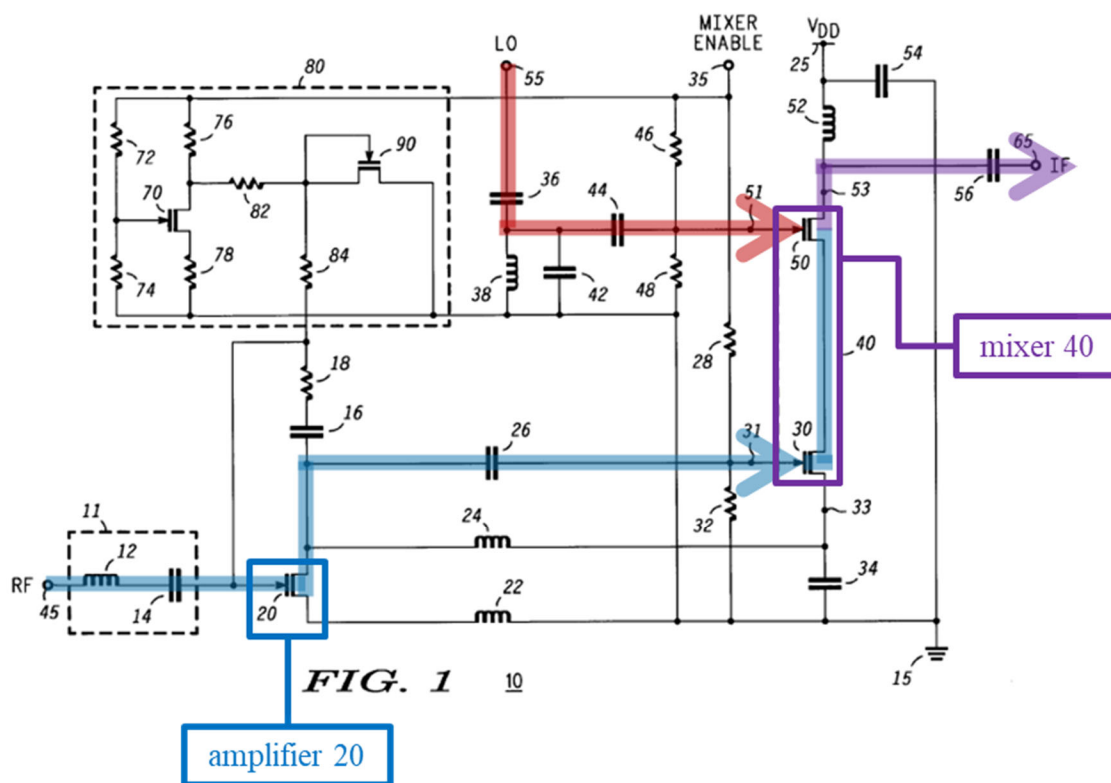
A. Neither Bonn nor Mizuta Disclose Connecting a Constant Voltage Source to the Second Gate of a Merged Cascode Transistor (Limitation [1C7])

69. Independent claim 1 requires that the “second gate [of a merged cascode transistor] is connected to the constant voltage source....” *See* Limitation [1C7]. While the Petition alleges that Bonn discloses connecting the second gate of a dual-gate transistor to a constant voltage source as claimed by Limitation [1C7], the Petition cites no evidence to support that statement. Petition, 40-45. Indeed, Bonn does not disclose connecting the second gate of a dual-gate transistor to a constant voltage source as claimed by Limitation [1C7]. Mizuta has no such disclosure either.

1. Bonn (Ex-1006) Discloses Connecting Both Gates of Its Dual-Gate Mixer 40 to Variable Voltage Signal Sources

70. Bonn discloses a downconverter (10) with single-gate FET amplifier (20) connected to mixer (40), where mixer (40) is made up of two single-gate transistors. *E.g.*, Ex-1006, 2:8-14, 2:66-3:12, Fig. 1 (annotated below).

Bonn, Figure 1 (Annotated)



71. Bonn shows that the gate of amplifier 20 and the gates of both transistors in mixer 40 are driven gates—none of them are connected to a constant voltage source.

72. As annotated in Bonn's Figure 1, above, the gate of amplifier FET 20 is connected to a variable voltage signal source (the RF signal on port 45) and a

bias voltage supplied from power supply 80. *Id.* at 2:14-17 (“A gate electrode of FET 20 is coupled for receiving the RF signal at an RF port 45 via serially coupled inductor 12 and capacitor 14.”), 2:39-40 (“the gate electrode of FET 20 is [also] coupled to a voltage source 80”); *see also* Ex-2009, 58:8-59:15, 64:18-21.

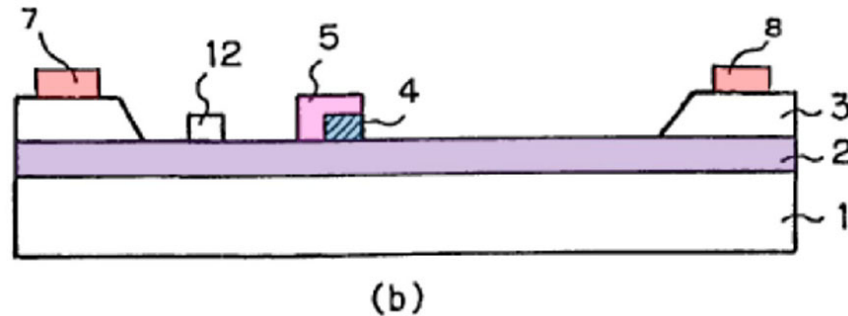
73. The gate of each transistor in the mixer 40 are also connected to variable voltage signal sources. The gate of FET 30 is connected to a variable voltage source (the amplified RF signal from amplifier FET 20) and biased through resistors 28 and 32. Ex-1006, 3:22-29, Fig. 1; Ex-2009, 68:22-69:6 (“Q. But in Figure 1 of Bonn gate 30 is connected to the amplified RF signal; is that right? A. It is, yes....”). The gate of FET 50 is connected to a variable voltage source (the LO signal supplied through port 55) and biased through resistors 46 and 48. Ex-1006, 3:31-40, Fig. 1; Ex-2009, 69:7-15. Bonn thus fails to disclose the claimed merged cascode transistor with the second gate connected to a constant voltage source.

2. Mizuta (Ex-1007) Fails to Disclose a Cascode Transistor of Any Type

74. Mizuta fails to disclose a cascode transistor of any type (in fact, Mizuta never even uses the word cascode and fails to otherwise disclose a cascode circuit), much less the claimed merged cascode transistor. *See generally*, Mizuta (Ex-1007). For example, Figure 11(b), the Figure that the Bernstein Declaration

reproduces, shows only a single gate (5) between electrodes (7) and (8) (Mizuta describes structure 12 as a “sub electrode,” *see id.*, 12:30-32).

Mizuta Figure 11(b) (Annotated by Dr. Bernstein)



Ex-1003, [084]. While Dr. Bernstein testified that the “sub electrode” under some circumstances might function as a gate, he admitted that he does not rely on Mizuta for disclosing a dual-gate structure. Ex-2009, 111:20-112:3 (“Q. ... you’re not relying on Mizuta for the disclosure of the dual-gate structure; is that right? A. Right.”). In my opinion, a POSA would not have understood Mizuta as disclosing the second gate of a merged cascode being connected to a constant voltage source as claimed.

3. Conclusion: Neither Bonn nor Mizuta Disclose Limitation [1C7]

75. While the Petition alleges that “Bonn discloses [1C7]” and “the second gate is connected to the constant voltage source,” the Petition cites nothing in Bonn that discloses that requirement. Petition, 40. The Petition cites its expert, Dr. Bernstein, [142]-[149] (*id.*), but those paragraphs of the Bernstein declaration

cite nowhere in Bonn that discloses the second gate is connected to the constant voltage source either. Both the Petition's and Dr. Bernstein's conclusion that Bonn discloses the second gate is connected to the constant voltage source is simply unsupported. As explained above, Bonn provides no disclosure of connecting the second gate to a constant voltage source—both gates of mixer 40 are connected to variable voltage sources, as it is necessary to enable mixing.

76. The Institution Decision acknowledges that Bonn does not disclose connecting the second gate of a dual-gate transistor to a constant voltage source as claimed by Limitation [1C7]. Paper 9, 13 (“Figure 1 of Bonn depicts local oscillator 55 coupled to the gate of second transistor 50. Petitioner does not, however, rely on the unmodified structure of Bonn.”). While the Institution credited the Petition's reliance on a heavily modified version of Bonn, as I explain below in Sections VII.C.1-5, those modifications are based on hindsight, not on those that a POSA would have had reason to make.

77. Thus, limitation [1C7] (the “second gate [of a merged cascode transistor] is connected to the constant voltage source....”) is absent from the cited prior art of Ground 1.

B. A POSA Motivated to Modify Bonn Based on Mizuta Would Not Have Arrived at a Circuit Meeting Limitation [1C7]

78. The Petition and the Bernstein Declaration allege that a POSA would have modified Bonn by adding Mizuta's field plate to Bonn's second gate electrode. Petition, 26-28; Ex-1003, [110]-[115]. But even if Mizuta's field plate were added to Bonn's dual-gate transistor, that would still fail to disclose connecting the second gate of a merged cascode transistor to a constant voltage source, as claimed, which is a feature absent from both Bonn and Mizuta. Adding Mizuta's field plate does not change the voltages applied to the gates of the transistors in Bonn's mixer 40. Bonn never suggests any of the string of modifications that the Bernstein Declaration imposes on Bonn's circuitry—Bonn discloses the *purpose* of the circuitry, it never suggests *removing* any of it, much less modifying it in the ways suggested in the Bernstein Declaration. Thus, even if a POSA were motivated to modify Bonn based on Mizuta, Bonn in combination with Mizuta would not have disclosed a cascode transistor circuit that connects the second gate of a merged cascode transistor to a constant voltage source as claimed.

C. The Petition and Bernstein Declaration Fail to Show a POSA Would Have Had a Reason to Modify Bonn to Meet the Missing Limitation [1C7]

79. The Institution Decision acknowledged the fact that Bonn did not disclose connecting a constant voltage source to the second gate of Bonn's dual-

gate transistor, instead basing its decision to institute a trial on Petitioner's arguments that a POSA would have arrived at a "modified version of Figure 1" that "removed local oscillator 55 and its connection to the gate of second transistor 50." Paper 9, 13-14. But the Petition and Bernstein Declaration failed to show that a POSA would have arrived at the modified version of Figure 1 (Petition, 19-25; Ex-1003, [097]-[109]) for several reasons explained below.

1. Changing Bonn's Downconverter into an Amplifier Would Have Rendered It Unsatisfactory for Its Intended Purpose

80. Making the modifications proposed by the Petition (at 19-25) and the Bernstein Declaration ([097]-[109]) would have turned Bonn's downconverter circuitry of Figure 1 into an amplifier, rendering Bonn's downconverter circuitry unsatisfactory for its intended purpose as a downconverter. But the Petition and Bernstein Declaration cite no prior-art-based evidence that a POSA would have sought to change the operating principle of Bonn's downconverter circuitry. While Bonn states that its dual-gate transistor can be "tailored" for use in "other applications such as high frequency signal amplification" (*id.*, 11:34-37), this sentence, in context, is referencing transistor properties (gate width, dopant concentration, etc.). Bonn is not teaching "tailor[ing]" the circuit of Fig. 1 to transform a downconverter into an amplifier. A POSA would not have made the proposed modifications because doing so would have rendered Bonn's

downconverter useless for its intended purpose for no apparent articulable rationale other than to meet the claims of the '003 patent.

81. Specifically, Petitioner alleges that POSAs would have modified Bonn's downconverter in Figure 1 to "use Figure 7's structure for high frequency signal amplification in place of mixer 40." Petition, 22. The Petition then steps through a series of extensive modifications to Bonn's downconverter in Figure 1 in order to reconfigure Bonn's mixer 40 into an amplifier by stripping away most of Bonn's downconverter circuit, including:

- Amplifier 20 (and associated circuitry)
- Voltage source 80 (and associated circuitry)
- Capacitors 16, 26, and 34
- Resistors 22, 24, 46 and 48
- LO Circuit port
- LO Circuit

Id., 23-25. The Petition cites Bonn for its disclosure of the functions of the various components of its circuitry that the Petition removes, but, critically, Bonn nowhere suggests such modifications to remove that circuitry. No articulable rationale is offered for removing the mixer and its necessary oscillator circuitry to create a newly configured amplifier.

82. For example, the Petition alleges that “a POSITA would have removed Figure 1’s LO (local oscillator) port 55 and associated impedance matching components because the LO signal is no longer mixed.” Petition, 23, citing Bernstein, [098]; Ex-1006, 3:30-41. But the cited portion of Bonn (3:30-41) discloses how the “[s]econd gate terminal 51 is coupled to the power supply” and to a “second electrode capacitor 44,” which in turn, “is coupled to an LO port 55 ... for receiving an LO signal.” Ex-1006, 3:30-41. If those portions were removed, as the Petition suggests, then Bonn’s downconverter would become inoperable because it would no longer be able to mix the RF and LO signals together as Bonn discloses is the purpose of its downconverter. Paragraph [098] of the Bernstein Declaration cites the same portion of Bonn and thus fails to cite any objective evidence that a POSA would have ripped out Bonn’s LO port and associated impedance matching components. In short, while Dr. Bernstein opines that a POSA would have made the proffered modification, his opinion is not supported by any objective evidence.

83. The Petition continues its piecewise “tailoring” of Bonn’s downconverter based on nothing more than Bonn’s disclosure of the function of the circuitry and then Bernstein’s testimony that a POSA would have removed it, without any citation to corroborating prior art evidence that a POSA would have removed that circuitry. Petition, 23-25. This is a blatant hindsight reconstruction of

the claims that attempts to meet a claim limitation missing from the art solely with expert testimony.

84. On the contrary, a POSA would **not** have looked to change the fundamental operating principle of Bonn's downconverter to repurpose it as an amplifier. A downconverter and an amplifier are two different types of devices with different purposes. An amplifier takes a *single input signal* and (ideally) produces a *single* higher voltage/current/power *output signal* at the same frequency as the input signal⁴. Ex-2009:52:19-53:2 (For an amplifier, "there is no change in the frequency."). In the case of an LNA, the LNA must also provide an output with as little added noise as possible. On the other hand, a downconverter takes *two input signals* (an RF signal and an LO signal) and produces *two output signals, of which, one, the IF signal* (at a frequency lower than the RF signal, in the case of a downconverter), *is retained* and the other, the "image signal," is typically filtered out. Moreover, it is often not necessary for a mixer to have gain. Bonn explains that "[t]he mixing process provides a mixed signal, which has a spectrum comprised of the sum and difference of the frequencies of the RF and LO signals" and that "[t]he higher frequency [image] components in the mixed signal are filtered out leaving an intermediate frequency (IF) component which serves as

⁴ The ratio of the amplitude of the output to the input signal is known as gain.

the output signal of the downconverter.” Ex-1006, 1:14-20; *see also* Ex-2009, 47:11-13.

85. The heart of Bonn’s downconverter of Figure 1 is mixer 40. It is the mixer that performs the essential function of a downconverter *i.e.* frequency conversion, without which a downconverter could not perform its most essential function. “Downconverters are used in radio applications to convert a[n RF] signal of one frequency to a[n IF] signal of another frequency.” Ex-1006, 1:8-9. The modifications to Bonn’s downconverter in Figure 1 that the Petition and Bernstein Declaration allege that a POSA would have had reason to make would strip out the essential function of Bonn’s downconverter in Figure 1.⁵ Ex-2009, 73:12-20 (“Q. So your modified circuitry would eliminate the down-converter function of Figure 1 of Bonn; is that right? A. My figure is purely as an amplifier ... I’m not using my circuit for a down-converter....”), 75:7-16.

⁵ Incidentally, the one thing that Bonn might suggest is to strip out the amplifier. As a POSA would have known, an LNA stage, like in Bonn’s downconverter of Fig. 1, is not always needed or used and there are applications where a first stage LNA could actually hurt, for instance, by desensitizing the downconverter, or as Bonn discloses, consuming too much current. Bonn in fact states that a “common problem with a downconverter is the need to individually supply the low noise amplifier and the mixing transistor with sufficient current for operation” and that “the low noise amplifier and mixing transistor may each require two to three milli-amps of operating current.” Ex-1006, 1:24-28.

86. Even Dr. Bernstein admitted at his deposition that Bonn's downconverter has special and unique properties. Dr. Bernstein explained that "you almost never see a circuit diagram on a device patent," "[s]o there's something very interesting in Bonn, and he's teaching something in a particular application." *Id.*, 53:7-10. "[A] POSITA would understand that this [downconverter] is a very sort of special application" and that Bonn "spends a lot of time explaining this RF application [] because it's not a usual application." *Id.*, 44:18-20, 45:2-3. It is safe to say that a POSA would not have looked to strip away the very functionality that made Bonn's downconverter so unique.

87. Dr. Bernstein's modification is motivated, not by what a POSA would have done, but by his own personal inexperience with downconverters and mixers. At Deposition, Dr. Bernstein candidly admitted that "I'm not an RF circuit expert, so I have very little experience with down-converters and mixers, to be honest." Ex-2009-46:18-20. Dr. Bernstein repeated that he was "not an expert in RF circuits" two times, emphasizing the fact. *Id.*, 60:20-21, 72:20-21. He admitted that "I generally am not familiar with down-converters," "I have no experience making down-converters," and "I don't know what Dr. Bonn or Mr. Bonn was thinking." *Id.*, 44:16-17, 44:22-45:1, 77:15-17. And Dr. Bernstein admitted that he had no experience with mixers either. *Id.*, 75:7-16 ("[H]onestly, I don't know how to make a mixer. I've never designed a mixer in my life."). Dr. Bernstein thus

modifies Bonn's Figure 1 circuitry not because a POSA would have done so, but because, by his own admission, he does not understand how downconverters and mixers work.

88. Unlike Dr. Bernstein, I am an expert in RF circuits, and I am familiar with both downconverters and mixers. In my expert opinion, I think it is safe to say that a POSA would not have had reason to modify a downconverter so that it no longer performs its most essential function, as the Petition and Bernstein Declaration contend.

2. The Petition and Bernstein Declaration Fail to Show Bonn's Dual-Gate Transistor Would Be Suitable as an Amplifier and Fails to Show a POSA Would Have Modified it to Make it Suitable

89. Bonn states that "the dual gate FET structure of the present invention can be *tailored* [(i.e modified)] to provide superior performance over the prior art dual gate FET structures in ... *other applications* such as high frequency signal amplification" (Ex-1006, 11:33-37), but Bonn never discloses an actual dual-gate FET specifically tailored for high frequency signal amplification or, for that matter, how Bonn's dual-gate FET structure would be used to design an amplifier. The Bernstein Declaration opines that the same passage from Bonn "teaches using its dual gate structures for signal amplification without signal mixing" and that *a POSA would have "use[d] Figure 7's structure for high frequency signal*

amplification in place of mixer 40.” Ex-1003, [096]-[097]; *see also* Petition, 22.

But the Bernstein Declaration is wrong.

90. A POSA would not have looked to the structure in Bonn’s Figure 7 for use in a high frequency signal amplifier because “[i]n the cascode configuration, FET 30 preferably has a smaller current conducting capacity than that of FET 50 to prevent FET 50 from being driven into current saturation by a strong RF signal that may appear at the gate electrode of FET 30.” Ex-1006, 5:37-41. As a POSA would have known that, when used in a high frequency LNA (Low Noise Amplifier) application, FET 50 and FET 30 would be operated with mismatched current densities, resulting in suboptimal operation, and a POSA, therefore, would not have had reason to use such a transistor in this application.

91. Moreover, all the “modifications” that the Bernstein Declaration describes are to the circuitry of Figure 1. Ex-1003, [097]-[109]. The Bernstein Declaration never suggests any modification to the structure in Bonn’s Figure 7 to make it suitable for high frequency signal amplification. *Id.* Absent such modifications, which the Bernstein Declaration does not describe or cite evidence to support, a POSA would not have had reason to embark upon the extensive modifications of Bonn’s downconverter circuitry, because a POSA would have known that the structure in Bonn’s Figure 7 would not have been desirable for use in a high frequency amplifier.

a. Bonn's Dual-Gate Mixer FET of Figure 7 Would Have Been Unsuitable for High Frequency Signal Amplification

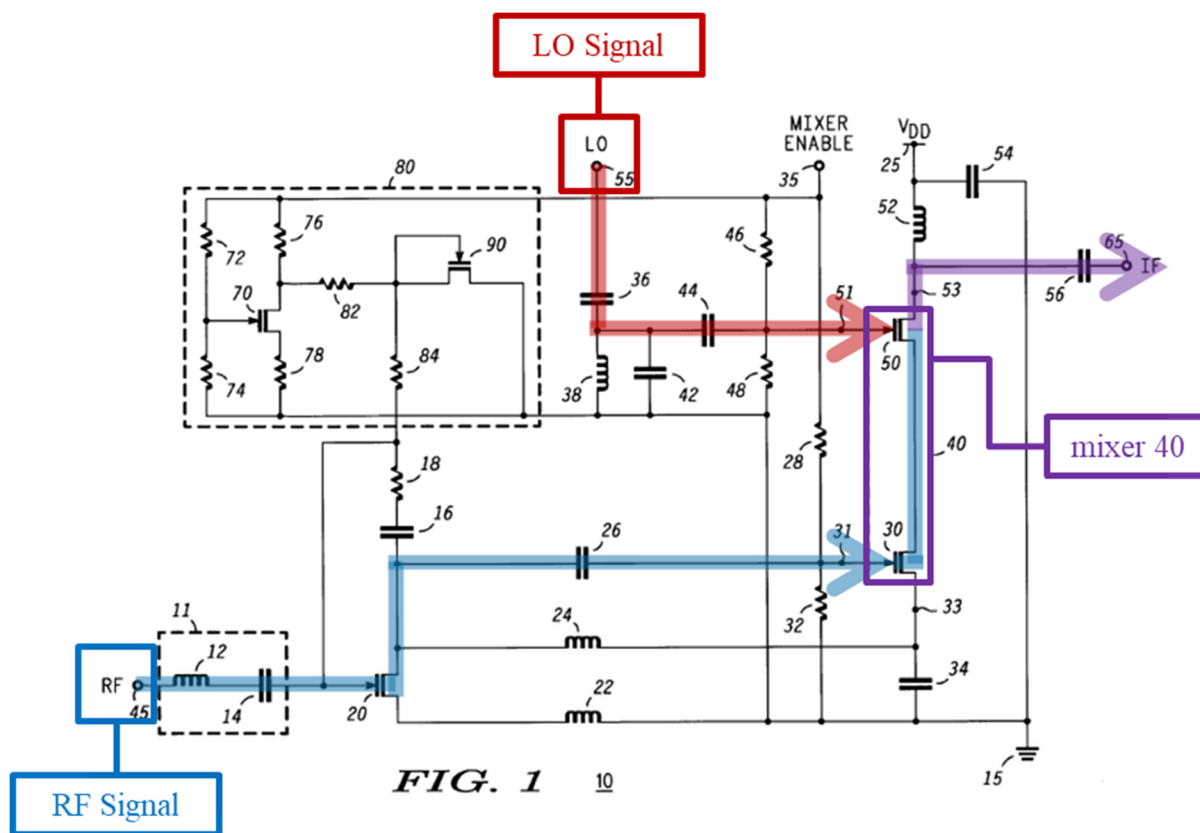
92. Bonn discloses field effect transistors (FETs) to be used in a downconverter. Ex-1006, 2:9-10 (“FIG. 1 is a schematic diagram of a downconverter 10 in accordance with an embodiment of the present invention.”). “A downconverter typically includes a low noise amplifier (LNA), an image filter, and a mixer circuit.” *Id.*, 1:10-11. As the Bernstein Declaration admits, “Bonn discloses using a dual gate FET 300 of Figure 7 ... in an embodiment of mixer 40 of Figure 1.” Ex-1003, [095]. Thus, the dual-gate transistor of Figure 7 is used as a *mixer* in Bonn’s downconverter.

93. In Bonn’s downconverter, the mixer takes two high frequency input signals (one at the RF frequency (containing the desired information signal) and the other at the LO (Local Oscillator) frequency) and outputs a desired IF (Intermediate Frequency) signal⁶ at a lower frequency, which is shown in Figure 1 of Bonn (below). As Bonn discloses, the mixer portion of the downconverter “combines a radio frequency (RF) signal” (shown in blue) “and a local oscillator

⁶ Except in the special case of an “Image rejection mixer,” a mixer generally produces two IF signals, the purpose of the “image (rejection) filter” in Bonn’s Fig. 1 is to remove the second, unwanted IF signal, which is called the “image” signal.

(LO) signal” (shown in red) “to provide an intermediate frequency (IF) signal” (shown in purple). Ex-1006, 2:11-13.

Bonn, Figure 1 (Annotated)

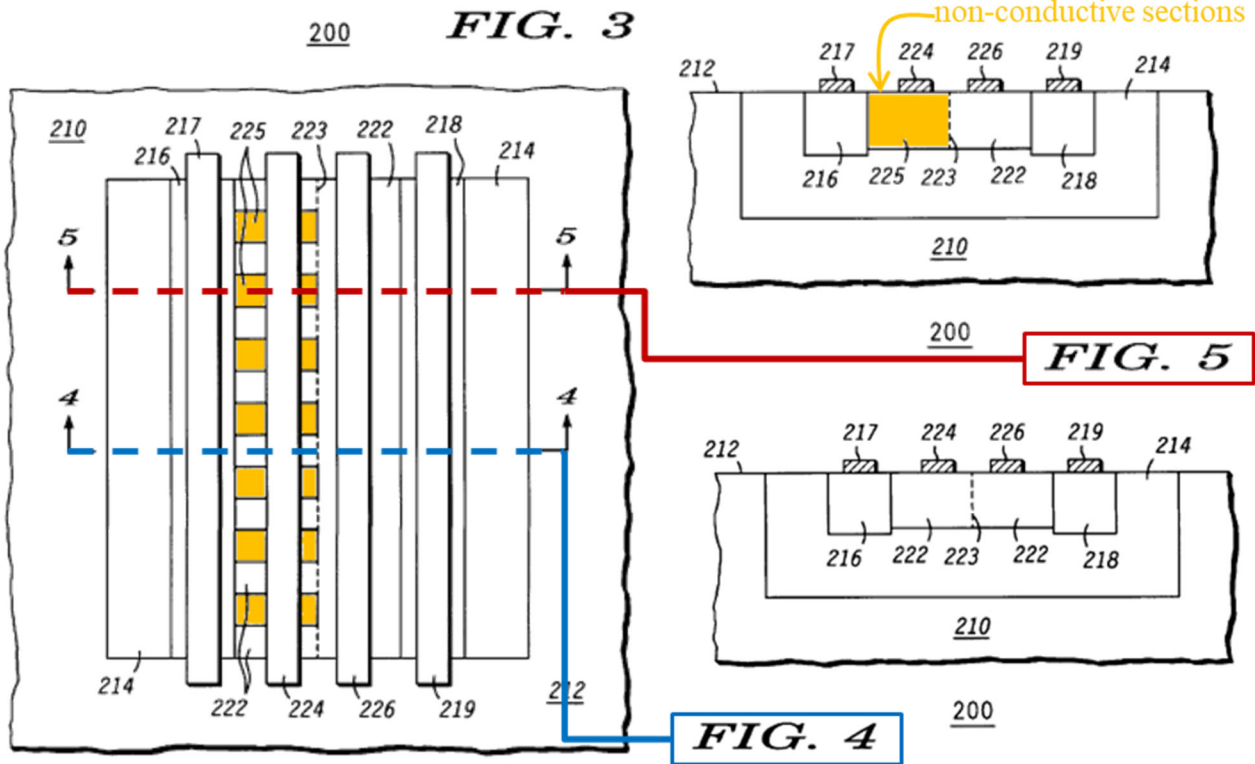


Bonn recognized, however, that if the (blue) RF signal was too “strong,” that could drive the second transistor of the mixer (50) “into current saturation,” meaning that the second transistor (50) could be pushed into an unintentional operating region. *Id.*, 5:37-41, *see also id.* at 5:46-52 (describing ways “to prevent mixer 40 from being driven into current saturation by a strong RF signal that may appear at first gate terminal 31 of mixer 40”).

94. Bonn solved the problem of the second transistor being driven into saturation by intentionally reducing the current-carrying capacity of the first FET (30) in comparison to the second FET (50). Specifically, Bonn discloses that “[i]n the cascode configuration, *FET 30 preferably has a smaller current conducting capacity than that of FET 50 to prevent FET 50 from being driven into current saturation by a strong RF signal* that may appear at the gate electrode of FET 30. *Id.*, 5:37-41; *see also id.*, 5:48-52.

95. Bonn achieves the reduction of current-carrying capacity of the first FET (30) in comparison to the second FET (50) by including “[n]on-conductive sections 225” to “reduce the effective channel width of the first gate region in structure 200.” *Id.*, 7:10-11, *see also id.*, 7:22-34, 7:59-64, Figs. 3, 4, and 5. Fig. 3 (below) “is a top view of [Bonn’s] field effect transistor structure.” *Id.*, 1:54-56. Figure 4 “is a cross-sectional view along section line 4-4 of FIG. 3” and “FIG. 5 is a cross-sectional view along section line 5-5 of FIG. 3.” *Id.*, 1:57-61. As shown below, the transistor includes a number of non-conductive sections (in orange below) that act to reduce the current-carrying capacity of the first gate.

Bonn, Figs. 3-5 (Annotated)



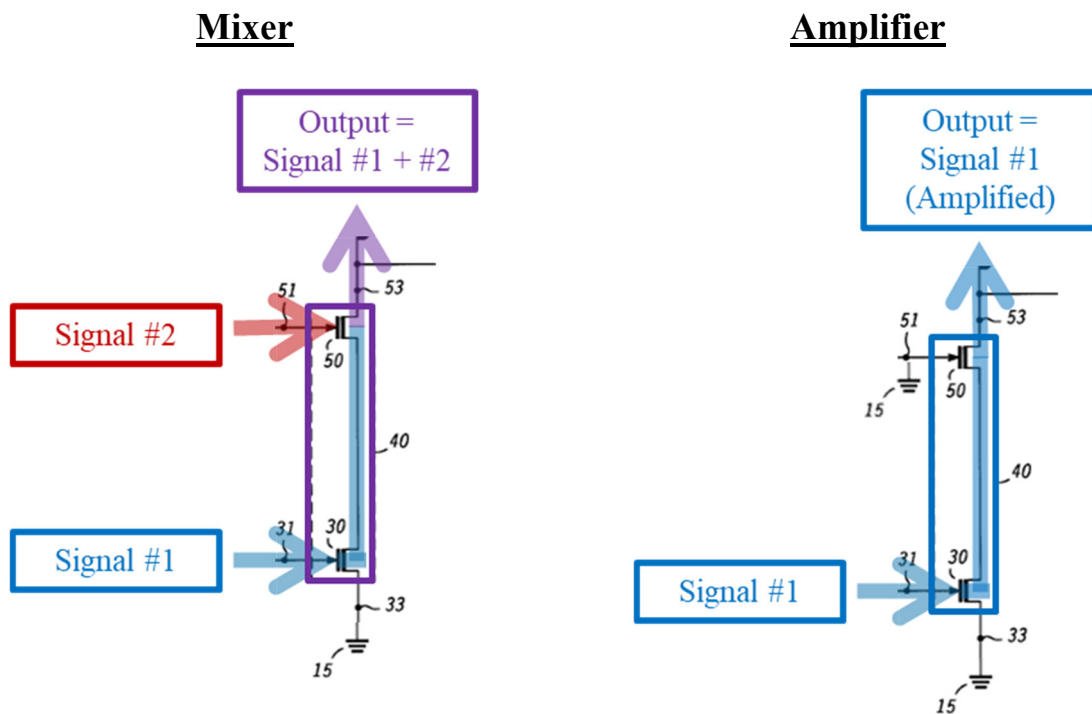
96. The same is true for the structure of Figure 7, which the Bernstein Declaration argues a POSA would use as an amplifier. Bonn discloses that the embodiment pictured in Figure 7 has “non-conductive sections 225 ... in first gate region 321 ... to individually adjust the gate width.” *Id.*, 9:12-20. These non-conductive sections 225 are not shown in Figure 7, but neither are they shown in Figure 4 because the presence or absence of the non-conductive sections 225 is dependent on where the cross-section is taken (as shown above with respect to the embodiment of Figures 3-5, shown above). Dr. Bernstein also admitted that Bonn applied the non-conducting sections shown in Figures 3-5 in the structure of Figure

7 as well. Ex-2009, 98:19-99:12 (Q. And *that applies to figure 7*, correct? A. He [Bonn] gave two cross-sections earlier to somehow differentiate between non-conducting and conducting, but *he said it's the same idea* [for Figure 7].”).

97. While Bonn uses the permissive word “can” in describing the presence of the non-conductive sections in Figure 7 (Ex-1006, 9:12-20 (“non-conductive sections ... *can* be formed”)), a POSA would have understood Bonn meant that such non-conductive sections are formed in the structure of Figure 7 because Bonn states that it is the “preferable” configuration. *Id.*, 5:37-41 (“In the cascode configuration, *FET 30 preferably has a smaller current conducting capacity than that of FET 50 to prevent FET 50 from being driven into current saturation by a strong RF signal* that may appear at the gate electrode of FET 30.”); *see also id.*, 5:48-52. While Dr. Bernstein argued at his deposition that the non-conductive sections are “completely optional” (Ex-2009, 99:7-17), that is not how a POSA would have understood Bonn’s description of the Figure 7 structure. A POSA would have understood Bonn to be describing that the non-conductive sections are indeed present in the Figure 7 structure intentionally to achieve the “preferable” smaller current-carrying capacity of FET 30 in relation to FET 50. Ex-1006, 5:37-41, 5:48-52.

98. While such a transistor may be well suited as a mixer, a POSA would not have had reason to use it for a high frequency signal amplification because of

the imbalanced current-carrying capacity under the two gates. When a dual-gate transistor is used as a mixer, two signals are combined to form one (desired) output. The imbalanced current-carrying capacity is desired to mitigate the undesirable effects (harmonic distortion, lower conversion gain, spurious mixing products, etc.) associated with transistor saturation. In an amplifier, only a single signal is amplified, and so a transistor with equal current-carrying capacity is more suitable and provides better performance because that same signal must be carried through both top and bottom transistors.



99. When asked about whether the structure of Figure 7 would have been suitable as an amplifier given the presence of non-conductive sections 225 to reduce the current-carrying capacity of the first gate, Dr. Bernstein initially

testified, “to be honest, just to finish your question, *I don’t honestly understand what he means when he says current carrying capacity...*” Ex-2009, 95:4-6; *see also id.*, 99:22-101:17 (“If *he’s restricting the flow* by reducing the width of one or the other, that will only mean there will be a higher resistance or a higher voltage drop across that part.... *I don’t know why* you would do it, ... again, *I don’t understand enough about RF circuits.*”).

100. Dr. Bernstein later admitted that Bonn’s design is optimized for the downconverter application, not as an amplifier. Ex-2009, 99:22-101:17 (“If he’s restricting the flow by reducing the width of one or the other, ... *He’s doing it for a very specific reason in his down-converters*, and I do not know his reason.... But it is not something you’ll see in most normal transistors because normally you would like to get as much current -- you want to get the lowest possible on resistance.”), 102:6-10 (“by intentionally restricting the gain by lowering the current flow between devices, you’re not getting your maximum current through, which means you’re going to have a higher voltage drop.”). As explained earlier, when used in a high frequency LNA (Low Noise Amplifier) application, FET 50 and FET 30 would be operated with mismatched current densities, resulting in suboptimal operation, and a POSA, therefore, would not have had reason to use such a transistor in this application.

101. In sum, a POSA would not have had reason to “use Figure 7’s structure for high frequency signal amplification” as the Bernstein Declaration alleges. Ex-1003, [096]-[097].

b. The Petition and Bernstein Declaration Propose No Modification to Figure 7’s Structure to Make it Suitable for High Frequency Signal Amplification

102. The Petition and Bernstein Declaration argue that a POSA would have “use[d] Figure 7’s structure for high frequency signal amplification.” Ex-1003, [097]; *see also* Petition, 22. While the Bernstein Declaration proposed “modifications,” those modifications are only with respect to the overall downconverter circuitry in Figure 1. *Id.*, [097]-[109]. The Bernstein Declaration never suggests any modification to the structure in Bonn’s Figure 7 to make it more suitable for a high frequency signal amplifier application. *Id.* Specifically, the Bernstein Declaration cites Bonn’s disclosure that parameters of Bonn’s dual-gate transistor could have been “individually adjusted” ““for optimum performance,’ such as ‘gate width, dopant concentration, and channel depth.’” Ex-1003, [096]. But the Bernstein Declaration never proposes any specific modification to the structure in Bonn’s Figure 7 to make it more suitable for use as an amplifier, how such modifications would be made, or their likelihood of success. As explained above, without modification (which the Bernstein Declaration does not propose,

describe, or cite evidence to support), a POSA would not have had reason to use the structure in Figure 7 for a high frequency signal amplifier.

103. Dr. Bernstein ignores the non-conductive sections of Figure 7 through hindsight analysis. When asked whether he commented on the non-conductive sections of Bonn's Figure 7 in his declaration, Dr. Bernstein defended his choice not to do so, arguing that "[t]here is no non-conductive sections in the '003 patent or in Mishra or in anybody else," which was why "I didn't feel it was anything that I needed to analyze." Ex-2009, 101:18-102:18. But a POSA would not have had the '003 patent to use as a roadmap as Dr. Bernstein uses in classic hindsight fashion.

104. At his deposition, Dr. Bernstein suggested that the structure of Figure 8 had "exactly the same current carrying capacity" for each gate. Ex-2009, 93:10-14. But Dr. Bernstein was mistaken. Bonn states that, with respect to Figure 8, "[i]t should be understood that non-conductive sections like non-conductive sections 225 in structure 200 if FIG. 3 can be formed in first gate regions 421A-421D...." Ex-1006, 10:66-11:3. While Bonn uses the permissive word "can" in describing the presence of the non-conductive sections in Figure 8 (and Figure 7), a POSA would have understood Bonn meant that such non-conductive sections are formed in the structures of Figures 7 and 8 because Bonn states that it is the "preferable" configuration. *Id.*, 5:37-41, 5:48-52. A POSA would thus understand Figure 8 to

have such non-conductive sections, just as Bonn's other embodiments do.

Regardless, Dr. Bernstein confirmed that the structure of Figure 8 did not form a part of his opinions as stated in his declaration. Ex-2009, 96:4-6 ("Q. Now, you don't rely on figure 8 specifically in your expert declaration, do you? A. I do not.").

105. Consequently, a POSA would not have embarked upon the extensive modifications to the overall downconverter circuitry of Figure 1 as proposed by the Bernstein Declaration to use the dual-gate FET of Figure 7 (purpose built for use in a mixer) as an amplifier because a POSA would have known that the dual-gate FET of Figure 7 was optimized for use as a mixer, as opposed to a high frequency signal amplifier.

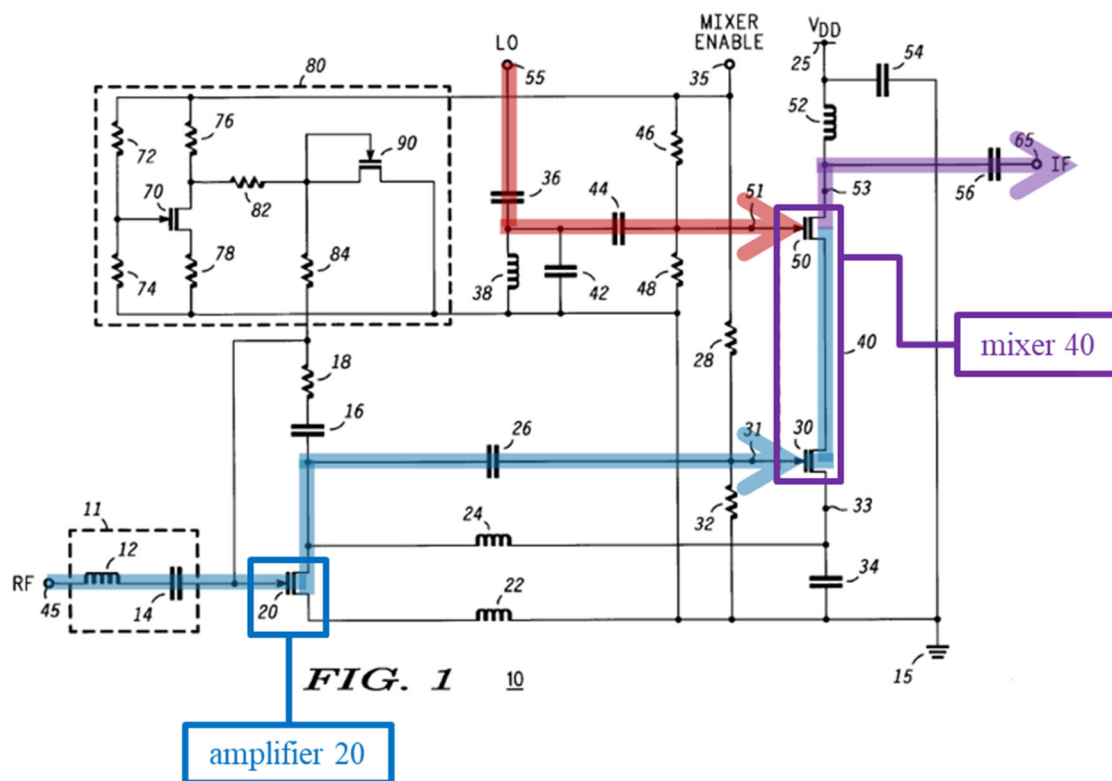
3. The Petition and Bernstein Declaration Fail to Show that a POSA Would Have Re-Wired Bonn's Circuitry to Re-Purpose a Mixer as an Amplifier When the Circuitry Already Contained an Amplifier

106. As explained above, Bonn discloses a downconverter with a single-gate FET amplifier (20) connected to a mixer (40). The Bernstein Declaration opines that "a POSITA would have found it obvious to make simple modifications to the circuit of Figure 1" to use the dual-gate mixer FET of Figure 7 as a "high frequency signal amplification in place of mixer 40." Ex-1003, [097]. However, the Bernstein Declaration cites no evidence and provides no explanation why a POSA would have extensively modified the circuitry in Figure 1 to re-purpose

mixer 40 as an amplifier, especially when the downconverter in Figure 1 already has an amplifier at FET 20.

107. Bonn discloses that FET 20 in Figure 1 (below, annotated) is an amplifier. Ex-1006, 2:12-14 (“Downconverter 10 includes a field effect transistor (FET) 20 which serves as a low noise amplifier (LNA) for amplifying the RF signal.”). Likewise, the Bernstein Declaration admits FET 20 is a “low noise amplifier for receiving the RF signal that amplifies the signal prior to mixing at mixer 40.” Ex-1003, [099]. Bonn explains that the gate of the amplifier FET 20 is capacitively coupled to the RF signal port 45 and powered by a voltage source 80. Ex-1006, 2:14-17 (“A gate electrode of FET 20 is coupled for receiving the RF signal at an RF port 45 via serially coupled inductor 12 and capacitor 14.”), 2:39-40 (“Still referring to FIG. 1, the gate electrode of FET 20 is coupled to a voltage source 80.”). Accordingly, the voltage source 80 provides a voltage bias to the gate of FET 20, and the RF signal modulates the conductivity of FET 20. Bonn explains that the conductivity is modulated between “a source electrode of FET 20,” which “is coupled to a power supply conductor 15 via an inductor 22” (*id.*, 2:21-22), and a drain electrode, which carries the amplified signal to gate terminal 31 of the mixer 40 (*id.*, 3:24-25). *See also id.*, Fig. 1.

Bonn, Figure 1 (Annotated)



108. The Bernstein Declaration cites no evidence and provides no objective reasoning as to why a POSA would have had reason to re-purpose mixer 40 as an amplifier in place of the LNA FET 20 in Bonn's downconverter in Figure 1. Ex-1003, [099]. Such an unsupported opinion is the hallmark of hindsight bias, which I understand is improper in an obvious analysis.

4. The Petition and Bernstein Declaration Fail to Show that POSAs Would Have Connected the Depletion Mode Gate of Bonn's Dual-Gate Transistor to a Constant Voltage Source as Claimed

109. Even if a POSA had had reason to use the dual-gate transistor of Figure 7 as an amplifier and even if a POSA had had reason to re-configure Bonn's

mixer (40) to turn it into an amplifier, neither of which a POSA would have had reason to do, the Bernstein Declaration would still fail to show that, in Bonn's Figure 1, a POSA would have had reason to connect the gate terminal (51) to a constant voltage source, such as ground, as the Bernstein Declaration argues. Ex-1003, [097], [104]-[105].

a. Mil'Shtein (Ex-2006) Disclosed Connecting the Second Gate to a Constant Voltage Produced the "Worst" Results

110. Indeed, a prior art reference cited by Petitioner in its invalidity contentions for the '003 patent in connection with ITC Inv. No. 337-TA-1414, Mil'Shtein (Ex-2006), discloses a dual-gate structure for a HEMT configured in the way the Petition proposes, which produced the "worst results." Ex-2006, 302. Dr. Bernstein testified at deposition that "that's my good friend Mil'Shtein" and that he "looked at this [Ex-2006] in my own background research," "[i]t's very familiar to me," and that "I don't remember exactly when I saw it, but fairly recently." Ex-2009, 173:16-175:7.

111. Mil'Shtein compared the performance of its dual-gate transistor using different gate bias and driving conditions against a conventional "single gate pHEMT of the same dimensions," and reported the following four results of that testing. Ex-2006, 302; Ex-2009, 176, 9-11 ("Q. And so figure 1 shows a dual-gate

transistor; is that right? A. That is right.”), 180:2-11 (“he’s using these two gates together as a single gate”).

112. **First**, for a conventional single-gate pHEMT, Mil’Shtein disclosed a “current gain of nearly 16 GHz for the normal HEMT.” Ex-2006, 302. The frequency refers to the frequency at which the circuit stops acting as an amplifier—meaning a unity gain of one, which Dr. Bernstein acknowledged is a “standard thing.” Ex-2009, 185:6-11. The higher the frequency of the unity gain, the better the amplifier’s performance, which Dr. Bernstein also acknowledged. *Id.* (testifying that “16 gigahertz is higher so it’s better, let’s say, more higher bandwidth than the unity gain of 9 gigahertz”). The 16 GHz measured for the single-gate pHEMT was thus the benchmark that Mil’Shtein used for comparing a dual-gate pHEMT under three different biasing conditions, described below.

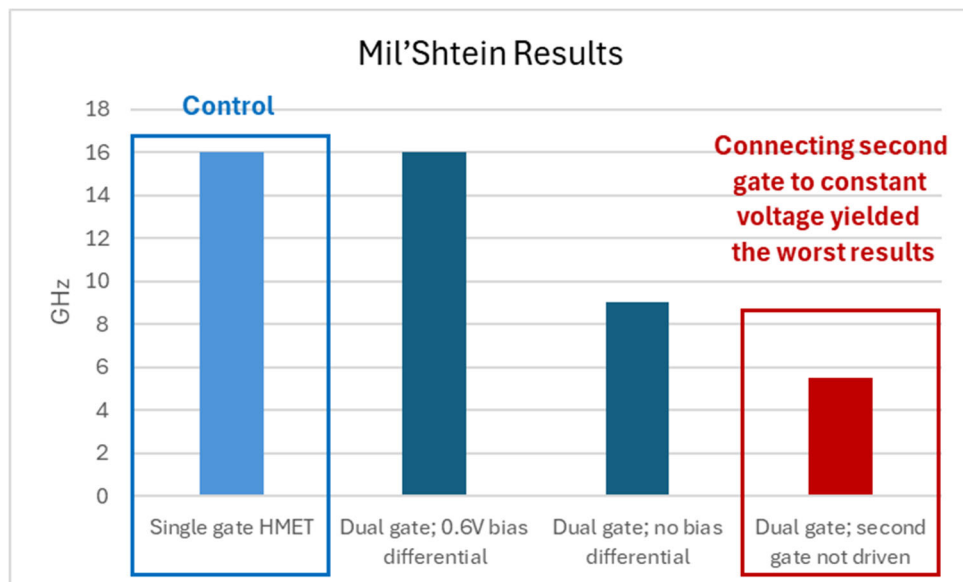
113. **Second**, for Mil’Shtein’s dual-gate pHEMT “with the 0.6 V bias differential and the RF input injected into both gates” *i.e.* with both gates actively with the same RF signal but with different gate bias voltages, it “[t]rack[ed] the results of the regular HEMT device closely.” Ex-2006, 302. Therefore, the “0.6 V bias differential and the RF input injected into both gates” performed similarly to a conventional single-gate pHEMT.

114. **Third**, with “no bias differential,” *i.e.*, the same bias voltage applied to both gates and “the RF [signal] injected into both gates,” a “unity gain limit of

about 9 GHz” was measured, underperforming the single-gate HEMT device’s 16 GHz. *Id.*; see also Ex-2009, 185:6-11 (testifying that “16 gigahertz is higher so it’s better, let’s say, more higher bandwidth than the unity gain of 9 gigahertz”).

Therefore, the dual-gate pHEMT with the same bias voltage applied to both gates and “the RF [signal] injected into both gates” performed worse than the conventional single-gate pHEMT.

115. **Fourth**, when “the RF [was] injected into only the Schottky gate,” meaning the second gate was held at a constant voltage as proposed by the Petition and then Bernstein Declaration, that “*yield[ed] the worst results* with a unity limit of about 5.5 GHz.” Ex-2006, 302.



As “higher [is] better” (Ex-2009, 185:6-11), the dual-gate pHEMT with the second gate set at a constant voltage yielded the worst results.

116. **Conclusion:** Mil'Shtein thus teaches that driving both gates of a dual-gate transistor in an amplification application resulted in better results than when only one gate was actively driven, which would have motivated a POSA to consider driving both gates of a dual-gate transistor, rather than connecting its upper (second) gate to a constant voltage source, as claimed in the '003 patent.

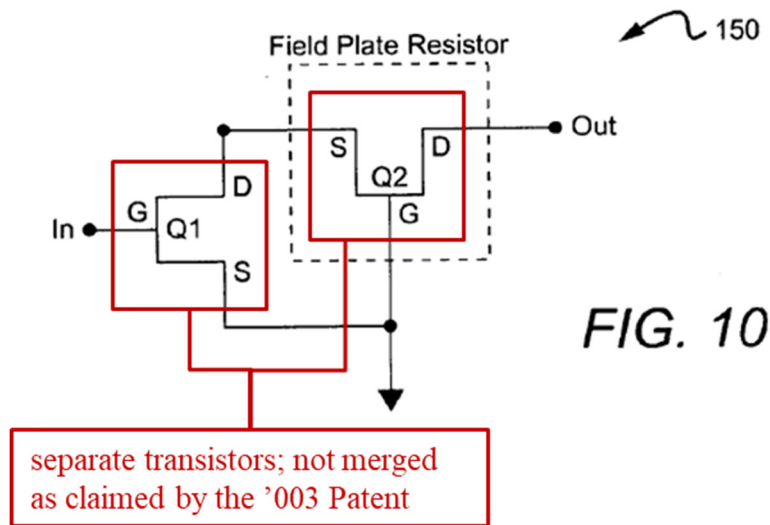
b. Mishra and Sankin Disclose Individual Transistors Connected by Wires, Not a Merged Transistor as Claimed

117. The Bernstein Declaration cites Mishra and Sankin as allegedly disclosing “the way a cascode transistor works in a normal amplifier circuit,” but that misrepresents the disclosures of Mishra and Sankin, which disclose two single-gate transistors (plural) connected together by wires, not a merged cascode transistor as claimed. Ex-1003, [106].

118. As I explain in more detail, below, in Section VIII.D.2.a, below, Mishra discloses a multi-stage amplifier circuit, but only discloses two individual *single-gate* transistors coupled together by wires as shown in Figure 10 (below), not a merged cascode transistor as claimed. Ex-1009, [0058] (stating that Figure 10 discloses “a multi-stage transistor amplifier block” with “a first stage transistor Q1 and a second stage transistor Q2, each of which may comprise a wide-bandgap field effect transistor,” meaning that Figure 10 discloses two separate transistors connected together, not a dual-gate transistor). The '003 patent does not purport to

have invented typical cascode circuits comprised of separate single-gate transistors, which is what Mishra discloses. Ex-1001, 2:52-53 (“the FET 20 of Fig. 2 is a single device and not two separate FETs”). Moreover, while the Bernstein Declaration alleges that Mishra discloses the “arrangement of enhancement mode and depletion mode transistors” (Ex-1003, [106]), there is no such disclosure in Mishra. The Bernstein Declaration later admits that “Mishra does not explicitly comment on the mode in which Q1 operates.” Ex-1003, [251]; *see also* Ex-2009 (“Q. In paragraph 251 you state: ‘Mishra does not explicitly comment on the mode in which Q1 operates in cascode embodiments’; is that right? A. I believe that’s exactly what I said before the break. Yes, he does not comment on whether it is -- what mode it is.”). Mishra thus does not disclose the operation of an enhancement mode transistor merged with a depletion mode transistor as one single FET. And Mishra does not provide any evidence of how a merged cascode transistor, as claimed, would work.

Mishra, Figure 10 (Annotated)



119. Another reference that the Bernstein Declaration cites as allegedly disclosing “the way a cascode transistor works in a normal amplifier circuit” is Sankin. Ex-1003, [106]. While Sankin discloses an enhancement mode transistor connected with a depletion mode transistor, Sankin connects the drain of the enhancement mode transistor to the source of the depletion mode transistor **with wires or interconnections** as opposed to having a drain region of the enhancement mode transistor that is merged with a source region of the depletion mode transistor at a node in the semiconductor element as claimed by the '003 Patent. Ex-2009, 32:18-22 (“Q. ... in figure 2 of Sankin the drain of the E-mode JFET is connected to the source of the D-mode JFET **by wires**; is that right? A. **That is correct.**”). Sankin’s transistor of Figure 2 would not have met Limitations [1C9]

and [10C10] because the drain (3) of Sankin's E-mode JFET is not "merged" with the source (6) of the D-mode JFET, being connected by wires.

Sankin Figure 2 (Annotated)

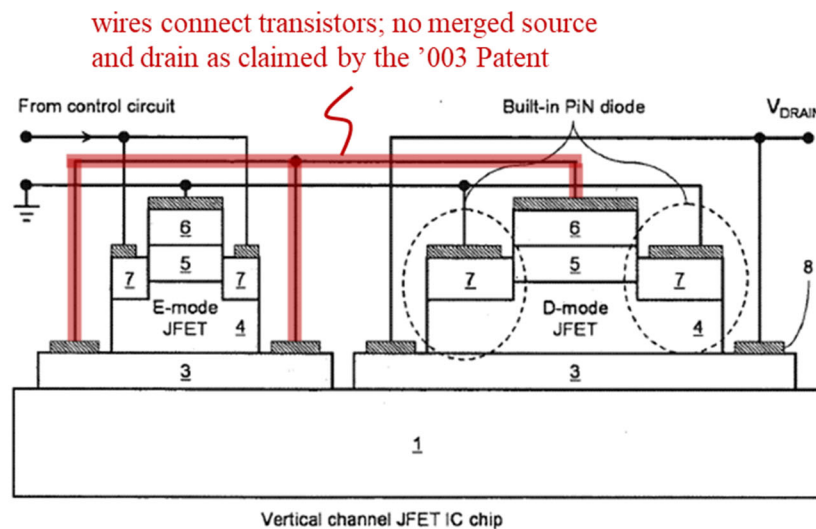


FIG. 2

Ex-1018, Fig. 2.

120. The Bernstein Declaration cites Figure 1 (Ex-1003, [106]), but that figure shows that the ground is only connected to the source (6) of the enhancement mode JEFT, not the gate (7) of the depletion mode JFET, as would be required by limitation [1C7]. Ex-1018, [0147]. The two transistors are also connected by wires, unlike the merged cascode transistor claimed by the '003 patent. Ex-2009, 31:5-10 ("Q. So my question was specifically: There's no depiction of the drain region of the enhancement mode transistor that merged with the source region depletion mode transistor, correct? A. It's depicted here as connections probably *with wires or metal.*"). Sankin's transistor of Figure 1 would

not have met Limitations [1C9] and [10C10] because the drain (3) of Sankin's E-mode JFET is not "merged" with the source (6) of the D-mode JFET, being connected by wires.

Sankin Figure 1 (Annotated)

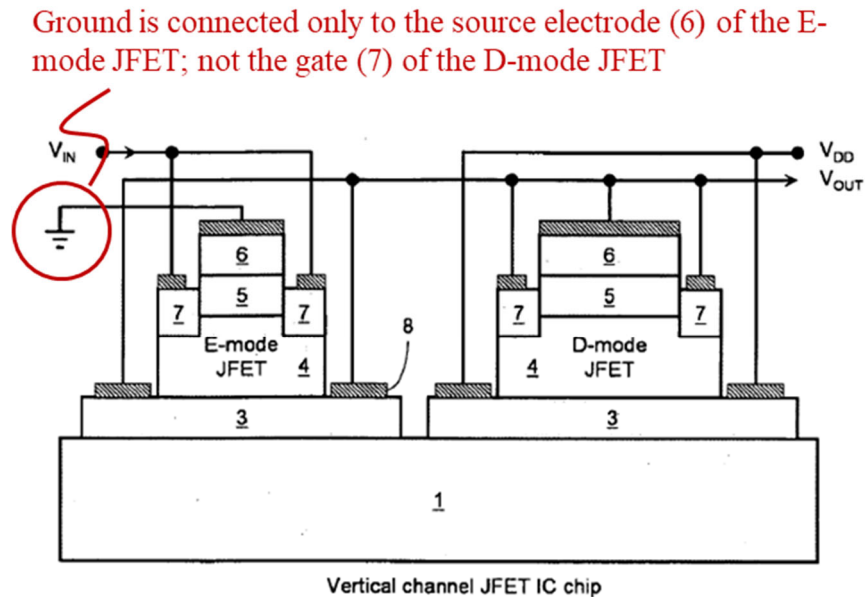


FIG. 1

121. Thus, both Sankin and Mishra disclose separate, individual transistors connected by wires, not a merged cascode transistor. Sankin and Mishra also do not disclose a merged cascode transistor circuit where the gate of the depletion mode transistor is connected to a constant voltage source.

122. Since neither Mishra nor Sankin discloses a merged cascode transistor in a cascode transistor circuit where the gate of the depletion mode transistor is connected to a constant voltage source, neither reference would have motivated a POSA to connect the second gate of Bonn's dual-gate mixer FET to a constant

voltage source (instead of Bonn's disclosure of each gate driven by separate variable voltage signals).

c. Conclusion: The Petition and the Bernstein Declaration Fail to Show a POSA Would Have Connected Bonn's Second Gate to a Constant Voltage Source as Claimed by the '003 Patent

123. In sum, the Petition and the Bernstein Declaration cite no evidence in the prior art that a POSA would have had reason to connect the second gate of a dual-gate transistor to a constant voltage source without the benefit of impermissible hindsight bias. The Petition and the Bernstein Declaration, therefore, fail to show a second gate connected to a constant voltage source and thus fail to show that limitation [1C7] was disclosed in the prior art, much less that it was obvious.

5. The Petition and Bernstein Declaration Fail to Show that POSAs Would Have Removed Bonn's Temperature Compensation Power Supply

124. The Petition and the Bernstein Declaration argue that a POSA would have removed voltage source 80 (along with amplifier FET 20). Petition, 23-24; Ex-1003, [100]. Voltage source 80 not only biases amplifier FET 20, but it also serves to "compensate[] for voltage variations that may be caused by temperature and transistor threshold voltage variations." Ex-1006, 2:59-65. As I explained above, a POSA would not have had reason to remove amplifier FET 20 (and voltage source 80, for that matter) and convert mixer 40 into an amplifier in

Bonn's Figure 1, but a POSA would have known that essentially any amplifier circuit would benefit from a temperature compensated bias voltage as Bonn discloses.

125. At deposition, when asked what the purpose of voltage source 80 was, Dr. Bernstein admitted that he did not know. Ex-2009, 59:17-60:22 (“Q. And you mentioned the biasing circuitry 80. What’s the purpose of that? A. ... as I said, I’m not an expert in RF circuits, but there's obviously some reason why he’s fixing this voltage....”).

126. The Petition’s and Bernstein Declaration’s removal of the amplifier temperature compensation disclosed by Bonn in their remaking of Bonn’s downconverter further suggests hindsight bias in the Petition’s and Bernstein Declaration’s proposed modifications in Ground 1.

VIII. THE PETITION FAILS TO SHOW CLAIMS 1-16 ARE OBVIOUS OVER BONN IN VIEW OF REN AND MISHRA (GROUND 2)

127. Ground 2 (Bonn in view of Ren and Mishra) fails to show that claims 1-16 of the ’003 patent are obvious.

128. The Petition and the Bernstein Declaration both rely entirely upon the reasoning used in Ground 1 in arguing that a POSA would have (1) used Bonn’s Figure 7 dual-gate mixer transistor as an amplifier and (2) modified the circuitry shown in Bonn’s Figure 1 to re-purpose Bonn’s downconverter as an amplifier. Petition, 49-50 (citing Ex-1003, [156] and cross-referencing “§ VII.A.1.”); Ex-

1003, [156] (cross-referencing “§ XII.A.1 (Motivation to Modify Bonn for High Frequency Signal Amplification)”).

129. The Petition and Bernstein Declaration then propose further modifications, such as making the Bonn transistor “using GaN instead of GaAs” based on Ren (Petition, 50-54; Ex-1003, [157]-[165]) and then adding a field plate to the second gate electrode based on Mishra’s teachings (Petition, 54-57; Ex-1003, [167]-[173]).

130. Notably, the Petition and Bernstein Declaration do not allege that Ren or Mishra discloses connecting the second gate of a merged cascode transistor to a constant voltage source, perhaps because neither Ren nor Mishra discloses that claimed limitation.

131. Even if a POSA had reason to combine Bonn’s dual-gate transistor with Ren’s disclosure of a GaN transistor (which would have been a *profound* modification that a POSA would not have had reason to make, as I explain below) and Mishra’s disclosure of adding a field plate to the second gate, that combination would not have resulted in a circuit that meets Limitations [1C7] and [10C8]. In short, Ground 2 suffers from the same missing limitation as Ground 1, and neither Ren nor Mishra fills in the gap.

A. None of Bonn, Ren, and Mishra Disclose Connecting a Constant Voltage Source to the Second Gate of a Merged Cascode Transistor (Limitations [1C7] and [10C8])

132. Independent claims 1 and 10 both require that the “second gate [of a merged cascode transistor] is connected to the constant voltage source....” *See* Limitations [1C7] and [10C8]. The Petition and Bernstein Declaration identify no disclosure in either Bonn, Ren, or Mishra that discloses this limitation. Petition, 67-69 (Limitation [1C7] analysis), 80 (Limitation [10C8] analysis merely cross-referencing the earlier [1C7] analysis); Ex-1003, [199]-[201] (Limitation [1C7]), [239] (Limitation [10C8] analysis merely cross-referencing the earlier [1C7] analysis). The Petition and Bernstein Declaration fail to identify any disclosure of this limitation because Bonn, Ren, and Mishra lack any disclosure of a second gate of a merged cascode transistor connected to the constant voltage source as claimed.

1. Bonn (Ex-1006) Discloses Connecting Both Gates of Its Dual-Gate Mixer 40 to Variable Voltage Signal Sources

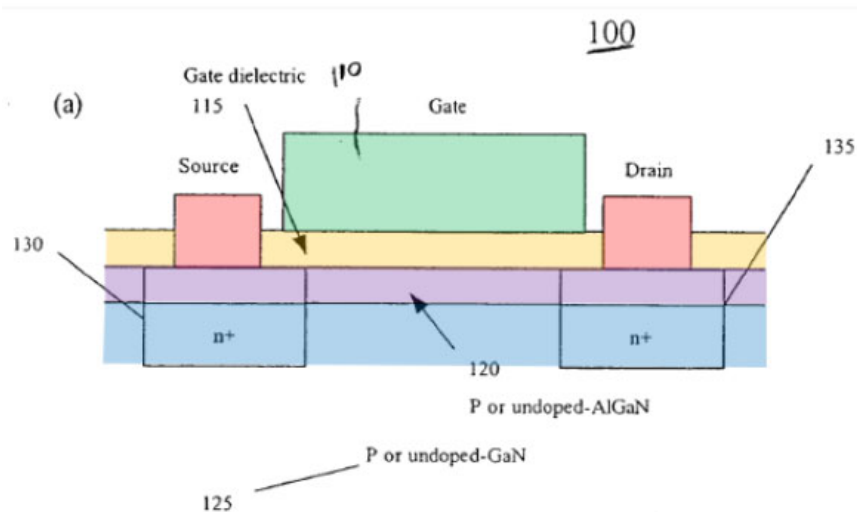
133. As I explained in Section VII.A.1, above, Bonn only discloses applying a variable voltage signal to the gate of its amplifier FET 20, separate variable voltage signals to each gate of mixer 40 (see my discussion of Ground 1). Even the Institution Decision acknowledges that Bonn does not disclose connecting the second gate of a dual-gate transistor to a constant voltage source as claimed by Limitation [1C7]. Paper 9, 13 (“Figure 1 of Bonn depicts local oscillator 55 coupled to the gate of second transistor 50. Petitioner does not,

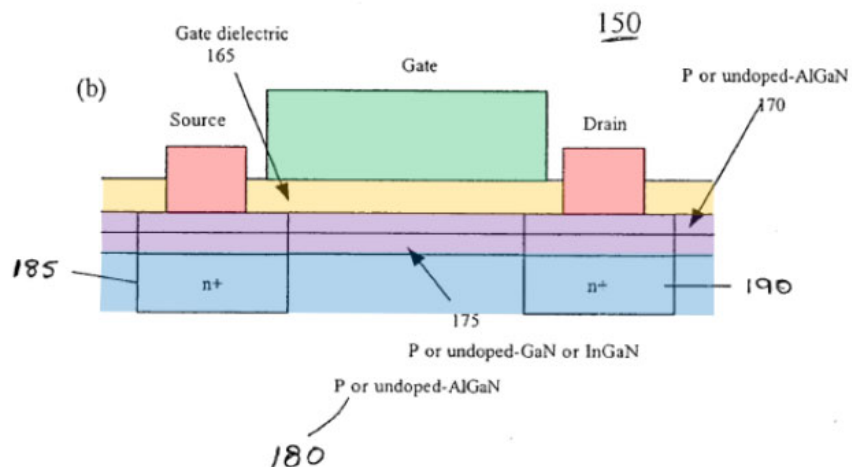
however, rely on the unmodified structure of Bonn.”). Bonn thus never discloses connecting the second gate of a merged cascode transistor to a constant voltage source as claimed. *Id.*

2. Ren (Ex-1008) Fails to Disclose a Cascode Transistor of Any Type

134. Ren fails to disclose a merged cascode transistor of any type (Ren never even uses the word cascode and fails to otherwise disclose a cascode circuit) and thus could not possibly disclose a second gate connected to a constant voltage source as claimed. *See generally*, Ex-1008; *see also* Ex-2009, 123:6-18 (“Well, everything in Ren is really just about the gate, and he doesn’t show any dual-gate of any transistor.”). For example, Figures 1(a) and 1(b), the Figures that the Bernstein Declaration reproduces, show only a single gate (in green) between source and gate electrodes (in red).

Ren Figures 1(a) and 1(b) (Annotated by Dr. Bernstein)



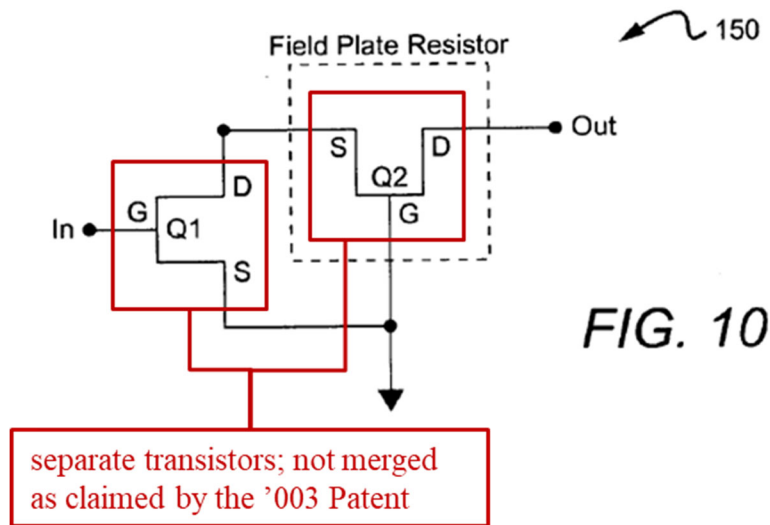


Ex-1003, [086]. Ren thus does not disclose the second gate of a merged cascode being connected to a constant voltage source as claimed.

3. Mishra (Ex-1009) Discloses a Multi-Stage Amplifier Circuit with Two Single-Gate Transistors Coupled Together by Wires

135. As explained further below in Section VIII.D.2.a, Mishra discloses a multi-stage amplifier circuit with two single-gate transistors coupled together in Figure 10 (below), but does not disclose a dual-gate transistor that would satisfy the claims of the '003 patent. *See also* Ex-1009, [0058] (stating that Figure 10 discloses “a multi-stage transistor amplifier block” with “a first stage transistor Q1 and a second stage transistor Q2, each of which may comprise a wide-bandgap field effect transistor,” meaning that Figure 10 discloses two separate transistors, not a dual-gate transistor).

Mishra, Figure 10 (Annotated)



136. While Mishra has a throw-away statement in its penultimate paragraph that “[o]ne alternative arrangement comprises a single transistor with a dual gate structure” (Ex-1009, [0062]), Mishra does not disclose the structure of such a transistor and does not disclose how such a transistor would have operated. Consequently, a POSA would not have understood Mishra disclosing connecting a constant voltage source to the second gate of a merged cascode transistor as required by limitations [1C7] and [10C8].

4. Conclusion: None of Bonn, Ren, and Mishra Disclose Limitations [1C7] and [10C8]

137. Thus, limitations [1C7] and [10C8] (the “second gate [of a merged cascode transistor] is connected to the constant voltage source....”) are missing from the cited prior art of Ground 2.

B. A POSA Motivated to Modify Bonn Based on Ren and Mishra Would Not Have Arrived at a Circuit Meeting Limitations [1C7] and [10C8]

138. The Petition and the Bernstein Declaration allege that a POSA would have modified Bonn by “using GaN instead of GaAs” based on the disclosures of Ren (Petition, 50-54; Ex-1003, [157]-[165]) and adding a field plate to the second gate electrode based on Mishra’s teachings (Petition, 54-57; Ex-1003, [167]-[173]). But as I explain below (*see* Section VIII.C), a POSA would not have been motivated to make such modifications. But for the sake of argument, even if Bonn’s transistor were made of GaN and Mishra’s field plate were added to Bonn’s dual-gate transistor, that still would not disclose connecting the second gate of a merged cascode transistor to a constant voltage source, as claimed, a feature absent from Bonn, Ren, and Mishra.

139. Changing the semiconductor material and adding a field plate would not necessarily change how Bonn’s transistor is configured or connected to surrounding circuitry. And Bonn never suggests any of the series of modifications that the Bernstein Declaration proposes to Bonn’s circuitry of Figure 1—Bonn discloses the *purpose* of the circuitry, it never suggests *removing* any of it, and particularly not in ways that fundamentally change the circuitry’s purpose, as the Bernstein Declaration does.

140. Thus, a POSA would not have been motivated to modify Bonn based on Ren and Mishra the way the Petition and the Bernstein Declaration allege, and would not have arrived at a cascode transistor circuit that connects the second gate of a merged cascode transistor to a constant voltage source as claimed.

C. The Petition and Bernstein Declaration Fail to Show a POSA Would Have Had a Reason to Modify Bonn to Meet the Missing Limitations [1C7] and [10C8] in Ground 2 For the Same Reasons Described for Ground 1

141. Even though Ground 2 cites Ren and Mishra as secondary references, where Ground 1 did not, the Petition and Bernstein Declaration never rely on Ren or Mishra to inform the proposed modifications to Bonn's Figure 1 circuitry to transform Bonn's downconverter into an amplifier. Petition, 49-50 (describing the alleged motivation to modify Bonn, cross referencing "§ VII.A.1," which was the earlier Ground 1 analysis, and citing "Bernstein, [156]"); Ex-1003, [156] (describing the alleged motivation to modify Bonn, cross referencing "§ XII.A.1," which was the earlier Ground 1 analysis). Dr. Bernstein admitted at deposition that he relied on his Ground 1 analysis for the alleged modifications to Bonn's Figure 1 circuitry in Ground 2. Ex-2009, 114:21-115:7.

142. Thus, there is nothing new in Ground 2 regarding repurposing Bonn's downconverter circuitry of Figure 1 into an amplifier that I have not already analyzed in my analysis of Ground 1. *See* Section VII.C, above. The Petition's and Bernstein Declaration's analysis from Ground 1 is wrong for the reasons I

previously described above in discussing Ground 1. *See* Section VII.C, above. The analysis in Ground 2 is thus wrong for the same reasons.

D. The Petition and Bernstein Declaration Fail to Show a POSA Would Have Had a Reasonable Expectation of Success for its Bonn-Ren-Mishra Combination

143. The Petition and the Bernstein Declaration Fail to Show a POSA would have had a reasonable expectation of success for the Bonn-Ren-Mishra Combination because neither one cites a single prior art reference that discloses the structure or how to make a merged cascode transistor out of GaN, despite arguing that a POSA would have sought to modify Bonn’s dual-gate mixer FET to make it “using GaN instead of GaAs.” Ex-1003, [157]-[166]; *see also* Petition, 50-54. The Petition only cites the Bernstein Declaration as evidence of alleged predictability. Petition, 52, citing only Ex-1003, [165]. The Bernstein Declaration, however, cites no prior art evidence to show that a POSA would have had at least a reasonable expectation of successfully making a merged cascode transistor out of GaN. Ex-1003, [165].

1. In 2006, GaN Was Still a New Technology

144. While I explain why the references that the Petition and Bernstein Declaration do cite are not in fact evidence of a reasonable expectation of success in the following sub-section, this failure of proof is critical because claims 2-16 all require a “III-Nitride layer” (Limitations [2A] and [2B]) or a “III-Nitride material”

(Limitations [10C1] and [10C2]). A “III-Nitride” material is one that includes nitrogen and at least one Group III element. Group III elements are those in the third column of the periodic table and include boron (B), aluminum (Al), gallium (Ga), indium (In), and thallium (Tl). GaN and AlGaN are examples of III-Nitride materials disclosed in the specification and which are expressly required by claims 4-9 and 12-16.

145. Not only did Dr. Bernstein testify that a cascode is “not such a normal device” (Ex-2009, 188:7-17), but as the Bernstein Declaration further admits, in the late 1990s, “GaN devices were in early development and uncommon” (Ex-1003, [158]). While the Bernstein Declaration (and the Petition) suggests that by 2006 “improvements to GaN manufacturing techniques made these devices more common than they were previously” (*id.*, [195]; *see also* Petition, 51), this does not show that GaN semiconductor processing, much less GaN device and circuit engineering, was so well understood that a POSA would have expected to be able to successfully make a merged cascode transistor out of GaN, especially without undue experimentation.

146. The complete lack of disclosure that would have taught a POSA how to make a dual-gate GaN FET with an enhancement mode transistor merged with a depletion mode transistor in the prior art cited by the Bernstein Declaration is fatal to Ground 2 (and to Ground 3 as discussed below) because even by March 20,

2006, GaN was still a relatively new technology. For example, Thomas Herman, inventor of the '003 patent, explained that making enhancement mode GaN transistors “was deemed a more difficult task.” Ex-2003, 30:2-15 (“Q. Did you design semiconductors with enhancement mode gates while you were at IR? A. The bulk of the effort at IR was depletion mode gates and transistors in GaN. Q. Did you also design enhancement mode transistors in GaN? A. There was interest in designing enhancement mode GaN transistors, but *that was deemed a more difficult task*. And I don't believe there was any active effort to specifically fabricate enhancement mode GaN transistors, other than, you know, feasibility and discussions. But I don't believe there was any effort to physically fabricate an enhancement mode GaN device.”).

147. Mr. Herman’s recount of the state of the art is consistent with my own recollection from the time. Even today, I am not aware of any disclosure of a merged cascode transistor made from GaN as of 2006.

148. As discussed previously in Section VIII.A.2, above, Ren may have disclosed single-gate GaN enhancement and depletion mode transistors, but does not disclose how to merge the two together. And as discussed in Section VIII.D.2.c, below, Beach may disclose a dual-gate transistor, but only one where the two gates operated the same way (either in enhancement mode or depletion mode, not a combination of one of each). As a POSA would have known, there

would have been nothing simple about creating a merged cascode transistor from GaN, much less would it have been likely to yield predictable results.

149. A POSA would have known that “*innovation in semiconductor manufacturing processes*, particularly the development and introduction of new process technology in this industry, *retains a strong element of trial and error.*”

Ex-2008, 1414-EXPERT-0002267-268 (native pages 69-70). Ex-2008 is a true and accurate copy of a 2002 Workshop Report published by the National Academies of Science and Medicine that chronicled the challenges Intel faced when trying to duplicate a semiconductor fabrication line. In fact, the risks and unpredictable consequences (like in the proverbial “Butterfly Effect”) of changing a known semiconductor process are so great that even Intel Corporation uses the so-called “copy exactly” philosophy:

A good example of this approach to process innovation is the so-called “copy exactly” philosophy that the Intel Corporation relies on in transferring process technologies among manufacturing plants. This approach to managing the development and transfer of process technologies concedes that *in the absence of a complete understanding of the process technology it is necessary to copy the entire system—the length of pipes, the placement of equipment—exactly, rather than in a way that is based on engineering or scientific knowledge.* This is a remarkable example of pre-scientific problem solving and trial-and-error experimentation in this industry.

Id. at 1414-EXPERT-0002268 (native page 70). I had first heard of Intel’s need to make an “exact copy” as early as 1995 from my Master’s advisor, who mentioned it as an anecdote from his days in industry, and heard of it subsequently in later

years throughout my tenure as a PhD student studying semiconductor devices, and while working in industry. A POSA would have thus known that semiconductor processing steps cannot be mixed and matched.

150. Changing the core semiconductor technology, which is what a switch from GaAs to GaN would entail, is a profound change that a POSA would not have expected to be successful, especially not without undue experimentation. A POSA would thus not have had a reasonable expectation of successfully modifying Bonn's dual-gate transistor to make it out of GaN, as the Petition and Bernstein Declaration propose for Ground 2.

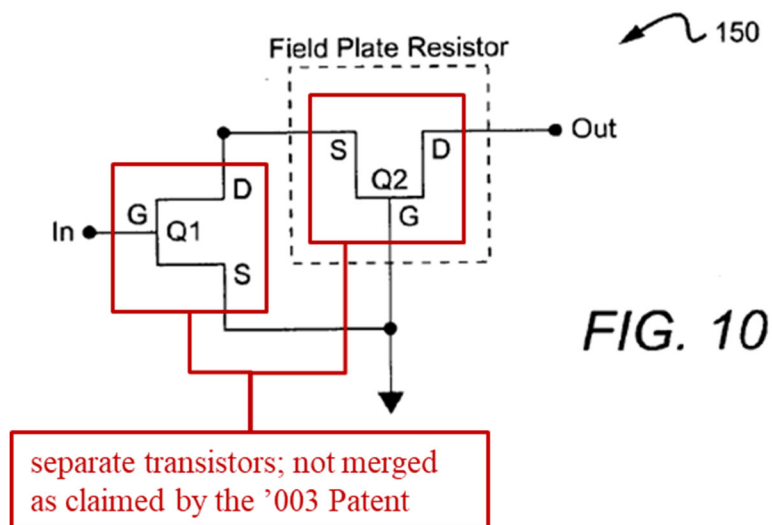
2. None of the Cited Art Discloses How to Make a Merged Cascode Transistor from GaN

a. Mishra Does Not Disclose How to Make a Dual-Gate GaN Transistor or What the Structure of One Would Look Like

151. The Petition and the Bernstein Declaration cite Mishra as disclosing the alleged "improvements to GaN manufacturing techniques" (Petition, 51, citing Ex-1003, [159]), but Mishra does not disclose how to make a dual-gate transistor or even what the structure of one would look like. Mishra discloses a multi-stage amplifier circuit, but only discloses two *individual transistors* coupled together in Figure 10 (below), not a dual-gate transistor as claimed. Ex-1009, [0058] (stating that Figure 10 discloses "a multi-stage transistor amplifier block" with "a first stage transistor Q1 and a second stage transistor Q2, each of which may comprise a

wide-bandgap field effect transistor,” meaning that Figure 10 discloses two separate transistors connected in series, not a dual-gate transistor).

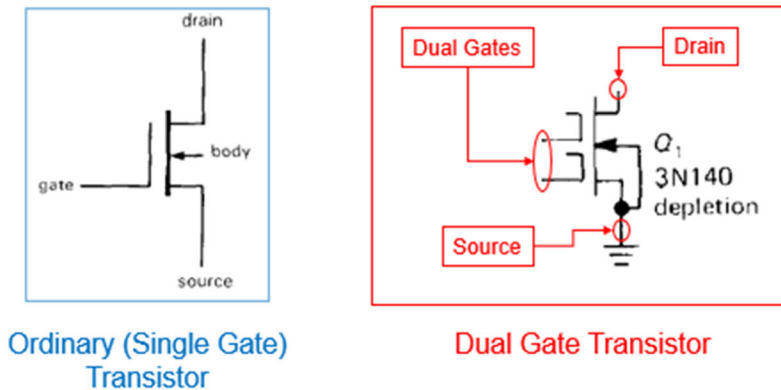
Mishra, Figure 10 (Annotated)



152. As a POSA would have known, Mishra’s transistors are separate, ordinary, single-gate transistors (annotated in blue, below), as opposed to a dual-gate transistor. A dual-gate transistor would have two gates belonging to the same device (not two separate devices), as shown in its circuit symbol (annotated in red, below), which a POSA would have readily recognized as a dual-gate transistor.⁷

⁷ I note that Figure 2 of the '003 patent does not use the dual-gate transistor symbol shown below but the '003 patent expressly states that “FIG. 2 illustrates a merged gate transistor.” Ex-1001, 2:36-37. Mishra has no such disclosure, which is why a POSA would understand Mishra’s Figure 10 to disclose two separate transistors and not one dual-gate transistor.

Comparison of Single-Gate and Dual-Gate Transistors



Ex-2002, 114, 883.

153. The above symbols of a single-gate and dual-gate transistor come from a 1994 reprinting of a textbook entitled “The Art of Electronics,” 2nd Edition, by Paul Horowitz and Winfield Hill. *Id.*, 2-3. This is an authoritative textbook that I have in my own collection.

154. All of Mishra’s FET embodiments (Figs. 2, 4, 5, 6, 8, and 9) are of a single-gate transistor that includes a field plate electrically connected to that gate. For example, for the embodiments shown in Figures 2, 6, and 8, the field plate is electrically connected to the gate in the cross-section itself. Ex-1009 at Figs. 2, 6, 8 (below). *See also* Ex-2009, 124:12-125:1 (Dr. Bernstein testifying that Figures 1, 2, 6, and 8 all show single-gate transistors).

Mishra Figs. 2, 6, and 8

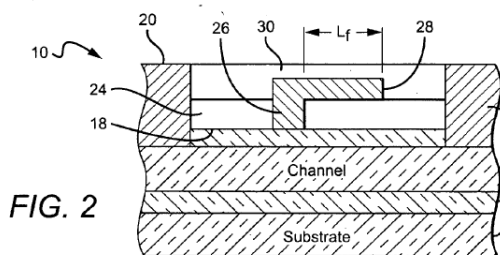


FIG. 2

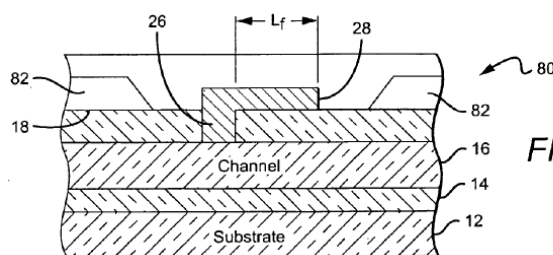


FIG. 6

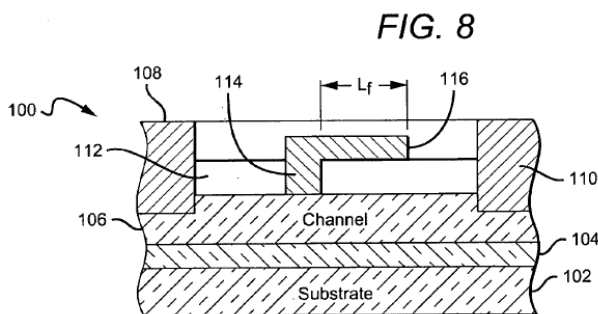
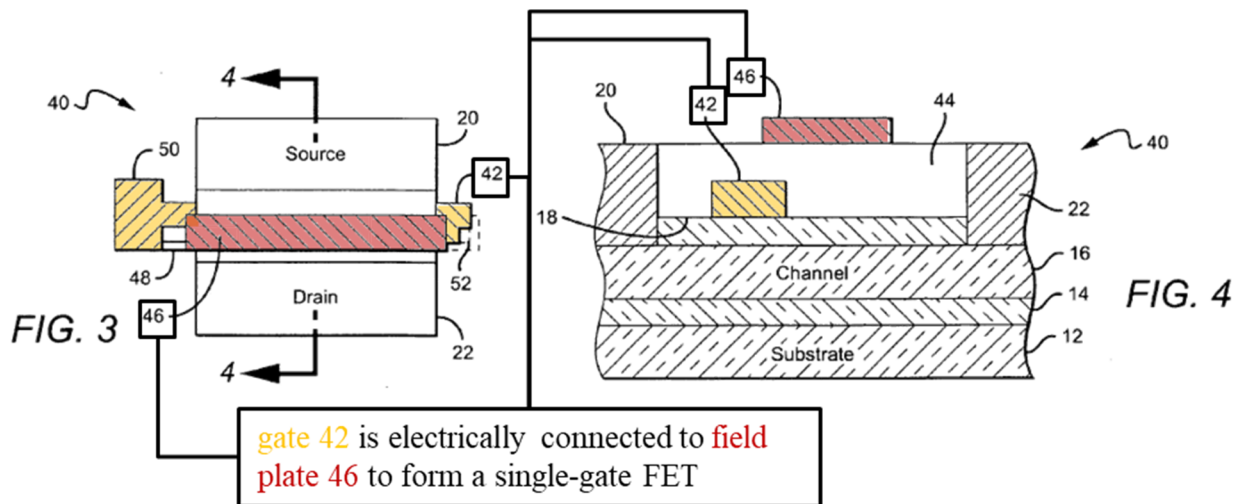


FIG. 8

155. Figures 3 and 4 show an embodiment where the field plate 46 is separated from the gate 42 by a dielectric in cross-section (Figure 4) but is “electrically connected to gate 42” as shown by FIG. 3, which “shows two alternative gate connection structures that can be used.” Ex-1009, [0040]; *see also* Ex-2009, 125:20-127:3 (Dr. Bernstein testifying that Figures 3 and 4 “looks” to be the same embodiment and that “46 can be connected to 42.”).

Mishra Figs. 3 and 4

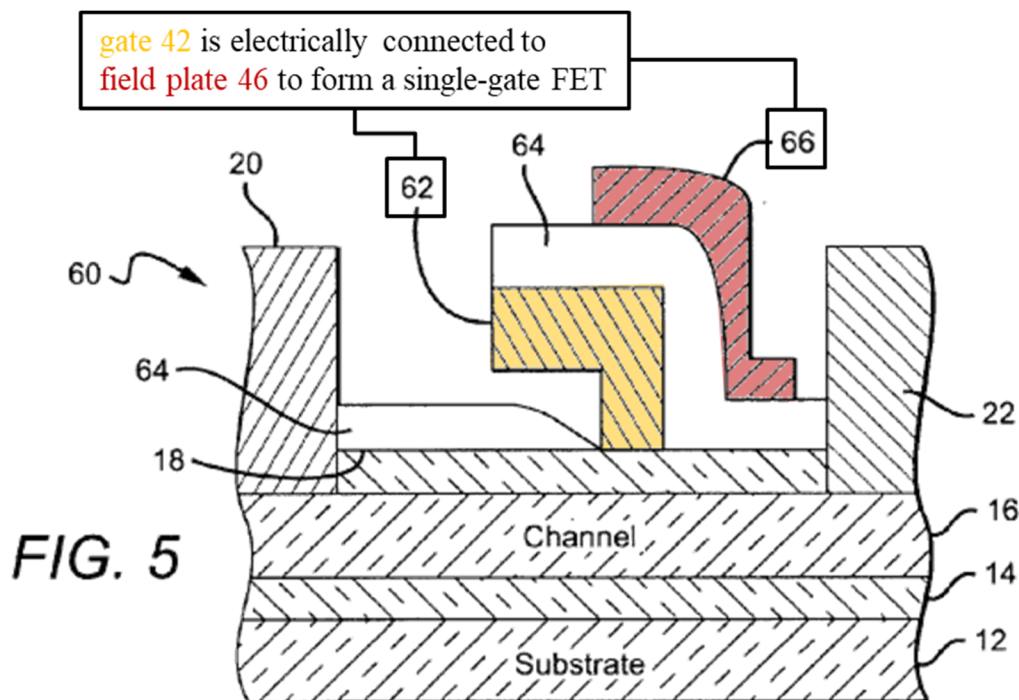


Mishra discloses that “[t]he field plate 46 can be connected to the gate 42 through a first conductive path 48 running outside the active area of the HEMT 40 to a gate contact 50 that is used to make electrical contact to the gate 42” and that “[a] second conductive path 52 (shown in phantom) can also be used that runs outside of the active region of the HEMT 40 on the side opposite the gate contact 50.” Ex-1009, [0040]. The embodiment of Figure 9 shows a MESFET (as opposed to a HEMT in the prior embodiments) that “has a gate and field plate structure similar to that in the HEMT 40 shown in FIGS. 3 and 4.” *Id.*, [0052]; Ex-2009, 128:20-129:2 (testifying the field plate structure of Figure 9 is similar to that of Figures 3 and 4).

156. Mishra further discloses that “FIG. 5 shows another embodiment of a HEMT 60” that “also includes a field plate 66 on the spacer layer 64 that overlaps that gamma gate 62.” Ex-1009, [0042]-[0043]. Mishra discloses that “[l]ike the

field plate 46 shown in FIGS. 3 and 4 and described above, the field plate 66 can be connected to the gate 62 in many different ways.” *Id.*, [0044].

Mishra Figure 5 (Annotated)



157. The Bernstein Declaration in some portions contends that “Mishra discloses a gate electrode between a source and drain electrode, and a *grounded field plate* over a dielectric and above an AlGa_N layer.” Ex-1003, [091]. The Bernstein Declaration highlights the phrase “grounded field plate” in pink and then shows an annotated image of Mishra’s Figure 5, with field plate 66 in pink, implying that Mishra discloses that field plate 66 is grounded. *Id.* While Mishra does mention the field plate may be connected to the source (Ex-1009, [0029], [0062]), Mishra never describes Figure 5 as having such a connection, rather,

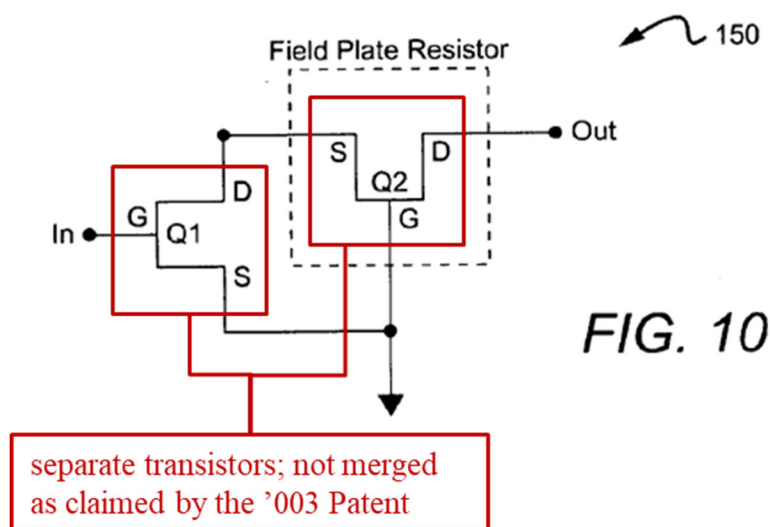
describing that field plate 66 connects to the gate 62 (*id.*, [0044]). The Bernstein declaration thus mistakenly alleges that “Mishra discloses biasing the source side gate (e.g., gate 62 of Figure 5) at low voltage, and the drain side *gate* (field plate 66 *of Figure 5*) at higher voltage.” Ex-1003, [250]. The Bernstein Declaration invokes that misrepresentation about Figure 5 when describing the Figure 10 circuitry in Ground 3. *Id.* (referencing the “field plate 66 of Figure 5” when describing Figure 10). None of the Bernstein Declaration’s citations, “Mishra, ¶¶[0030]-[0035], [0042]-[0044], [0054]-[0062], Fig. 5” or “[0060]” support its mistaken contention. Ex-1003, [091], [250].

158. At his deposition, Dr. Bernstein confirmed that Figure 5 depicts a single-gate transistor. Ex-2009, 153:2-14 (“Q. So for the unmodified figure 5 of Mishra, Mishra itself does not disclose that figure 5 is a dual-gate structure; is that correct? A. He calls 66 -- as I recall, he calls it a field plate.... So this [66] is between the gate and the drain, so it’s a field plate and -- as disclosed in Mishra, which is why Mishra by itself, we’re not only holding -- we’re not only saying Mishra anticipates.”), 150:16-20 (“[Mishra is] not telling us that that [sic] field plate is also a gate.”). Thus, all of the embodiments of Figures 2, 4, 5, 6, 8, and 9 are single-gate transistors, not dual-gate transistors, which Dr. Bernstein admitted to be true. *Id.*, 154:8-155:2 (“Q. Before the break we were talking about ... whether or not Mishra itself provided a figure that showed a single transistor with a

dual-gate structure. And I think the answer was no.... Do I have that right? A. You have that basically right....”).

159. Mishra discloses that its single-gate transistors with field plates can be used in a “2-stage cascode amplifier structure.” Ex-1009, [0056]. Figure 10 (below) provides one such example of a “multi-stage transistor amplifier block.” *Id.*, [0058]. But none of the embodiments of Figures 2, 4, 5, 6, 8, and 9 disclose Q1 in Figure 10 because they all have field plates and Mishra discloses that “Q1 does not include a field plate.” *Id.*, [0059]. The embodiments of Figures 2, 4, 5, 6, 8, and 9 are all thus examples of Q2, “which includes a field plate.” *Id.*, [0060]. Mishra thus discloses no structure for the first (Q1) of its two single-gate transistors. Indeed, Mishra undoubtedly put a dashed box around Q2 in Figure 10, denoting that was Mishra’s invention and where it should be used in the circuit.

Mishra, Figure 10 (Annotated)



160. When asked about whether Mishra in fact discloses a Q1 transistor based on Mishra's disclosure that "Q1 does not include a field plate," and yet all of Mishra's figures show a transistor with a field plate, Dr. Bernstein suggested that was a "logical conclusion which is not true," and then argued that a transistor with a field plate could be used as a Q1 transistor. Ex-2009, 147:19-149:10. Regardless of whether that is true or not is beside the point because Mishra discloses no transistor without a field plate and states the Q1 transistor in his device did not have one. A POSA would have understood that to mean that Mishra discloses no structure for the first (Q1) of its two single-gate transistors.

161. The mode of operation (enhancement or depletion mode) of Q1 is not disclosed either, but given that the transistor symbols are the same for both in Figure 10, a POSA would have understood Q1 and Q2 to be of the same type, either enhancement mode or depletion mode.

162. The mode of operation for the Q2 transistors is depletion mode in each of the embodiments of Figs. 2, 4, and 6, which show the gate contact on the buffer layer 18, or channel layer 16. Similarly, Mishra shows only depletion mode MESFETs in Figs. 8 and 9, as evidenced by the gate contact on the channel layer 106.

163. A POSA would, therefore, have no reason to think Q1 and Q2 would be enhancement mode (and especially not that Q1 would be enhancement mode

and Q2 would be depletion mode, or vice versa), especially since, nowhere in Mishra is enhancement mode even mentioned and all the more so because depletion mode GaN and GaAs FETs are, and were, far more commonly used.

164. While Mishra has a throw-away statement in its penultimate paragraph that “[o]ne alternative arrangement comprises a single transistor with a dual gate structure” (Ex-1009, [0062]), Mishra does not disclose the structure of such a transistor, does not disclose how such a transistor would have been manufactured, and does not disclose how such a transistor would have operated. Ex-2009, 154:8-155:2 (“Q. Before the break we were talking about ... whether or not Mishra itself provided a figure that showed a single transistor with a dual-gate structure. And I think the answer was no.... Do I have that right? A. You have that basically right....”).

165. Mishra also discloses the hypothetical notion that “[i]n still other embodiments the field gate can be connected to the source contact.” Ex-1009, [0029]; *see also id.*, [0062] (stating the field plate “can be connected to the source contact”). But again, Mishra does not disclose the structure of such a transistor, does not disclose how such a transistor would have been manufactured, and does not disclose how such a transistor would have operated. As explained above, Mishra’s figures and the accompanying descriptions always show or describe the field plate connected to the gate or physically a part of it. While Mishra uses the

phrase “field *gate*” as opposed to “field *plate*” in paragraph [0029], given that Mishra consistently describes the structure as a field plate (not a second gate), a POSA would not have understood paragraph [0029] as disclosing a second gate. Even Dr. Bernstein candidly admitted that “a POSITA would overlook the word ‘gate’ or ‘plate’ as I did.” Ex-2009, 197:16-198:8.

166. Thus, Mishra provides no enabling disclosure of a dual-gate transistor, which is to say it provides no disclosure sufficient for a POSA to make or use a dual-gate transistor without undue experimentation. Mishra, therefore, is not evidence that a POSA would have had a reasonable expectation of success in making the combination set forth in Ground 2.

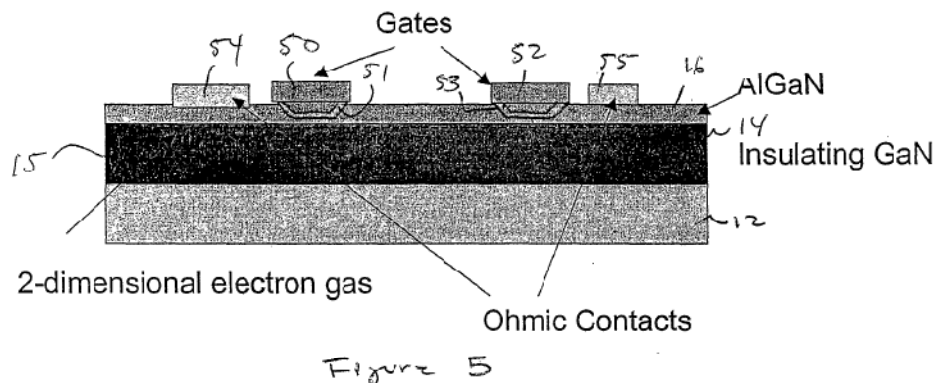
b. Ren Has No Disclosure of a Dual-Gate GaN Transistor at All

167. The Petition and Bernstein Declaration also cite Ren (Petition, 51; Ex-1003, [159]), but as I explain in Section VIII.A.2, above, Ren has no disclosure of a dual-gate GaN transistor. Ren does not disclose the structure of a dual-gate GaN transistor, does not disclose the operation of a dual-gate GaN transistor, and does not disclose how a dual-gate GaN transistor would be made. Ex-2009, 123:6-18 (“Well, everything in Ren is really just about the gate, and he doesn’t show any dual-gate of any transistor.”). Thus, Ren provides no enabling disclosure of a dual-gate transistor either and is, therefore, not evidence that a POSA would have had a reasonable expectation of success in making the combination set forth in Ground 2.

c. Beach's Dual-Gate Transistor Has the Same Mode of Operation for Each Gate; Beach Fails to Disclose an Enhancement Mode Transistor Merged with a Depletion Mode Transistor as Claimed

168. The Petition and the Bernstein Declaration cite International Patent Publication No. WO 2005/070009 (Ex-1020, "Beach"). *See* Petition 51, citing Ex-1003, [161]. While Beach discloses a dual-gate transistor (e.g., Fig. 5, below), both gates have the same mode of operation, not an enhancement mode transistor merged with a depletion mode transistor as claimed by the '003 patent. Ex-1020, [0048] ("gate electrodes 50, 52 each locally interrupt the 2DEG under the gate contact to interrupt the conduction channel provided at interface 15."), [0051] ("Gate contacts 50, 52 are both activated to permit current to flow to/from electrode 54, 55."); Ex-2009, 159:9-160:19 (testifying that Beach's "intention is to have two enhancement modes," and "it looks like those [gates] both have to be enhancement modes because they were above zero"), 161:1-4 ("Q. And you're not relying on Beach as disclosing an enhancement mode gate next to a depletion mode gate in your report, correct? A. Right. I do not.").

Beach, Figure 5



169. Beach further explains that “[i]f one or both of gate contacts 50, 52 are not activated, no current flows between electrodes 54, 55,” “[a]ccordingly, bi-directional device 56 acts as a logic power AND gate, where the switch is active only when both ‘inputs’ are active, meaning gate contacts 50 and 52 are active.”). Ex-1020, [0051]. Since Beach’s device 56 is disclosed as an AND logic gate, a POSA would have known that the two inputs (in this case, gate contacts) would generally be connected to separate variable voltage sources, not a constant voltage source as required by the claims of the ’003 patent.

170. Beach thus does not disclose the structure of a dual-gate GaN transistor with an enhancement mode transistor merged with a depletion mode transistor, does not disclose the operation of such a dual-gate GaN transistor, and does not disclose how such a dual-gate GaN transistor would be made. Beach thus provides no enabling disclosure of the type of dual-gate transistor claimed by the

'003 patent and is, therefore, not evidence that a POSA would have had a reasonable expectation of success in making the combination set forth in Ground 2.

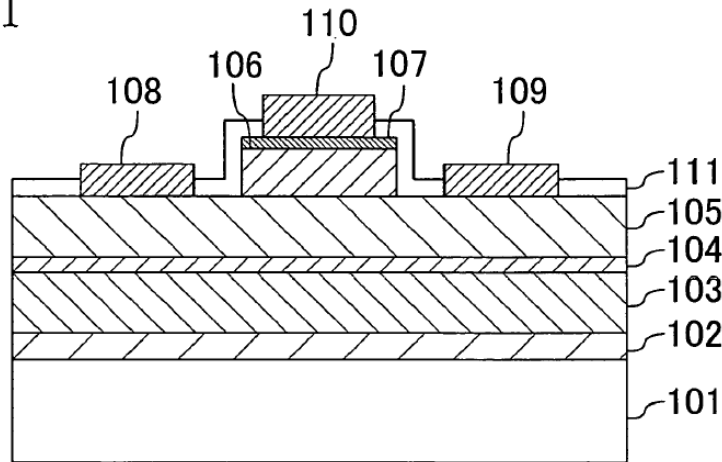
d. Ueno Does Not Disclose a Dual-Gate Transistor, and the Petition and the Bernstein Declaration Do Not Establish That It Is Even Prior Art

171. The Petition and the Bernstein Declaration cite U.S. Patent Publication No. 2007/0170463 (Ex-1016, “Ueno”) (*see* Petition, 52, citing Ex-1003, [163]), but Ueno was not published until July 26, 2007, from an application that was filed on December 29, 2006—*after* the March 20, 2006, priority date that the Bernstein Declaration has assumed for the '003 patent (Ex-1003, [004], [007], [036], [062], [074], [159]). The Bernstein Declaration does not even explain how Ueno is prior art to the '003 patent, or what significance it would have to the validity analysis, as it is not prior art.

172. Ueno also does not disclose a dual-gate GaN transistor. *See generally* Ex-1016. Figure 1, for example, shows only a single-gate transistor.

Ueno, Figure 1

FIG. 1



Ueno does not disclose the structure of a dual-gate GaN transistor, does not disclose the operation of a dual-gate GaN transistor, and does not disclose how a dual-gate GaN transistor would be made. *Id.* Ueno thus provides no enabling disclosure of a dual-gate transistor and is, therefore, not evidence that a POSA would have had a reasonable expectation of success in making the combination set forth in Ground 2.

3. Conclusion: Petition and Bernstein Declaration Fail to Establish a Reasonable Expectation of Success for Ground 2

173. This complete lack of disclosure of a dual-gate GaN FET with an enhancement mode transistor merged with a depletion mode transistor in the prior art cited by the Bernstein Declaration is fatal because even by March 20, 2006, GaN was still new technology. The inventor of the '003 patent explained at

deposition that making enhancement mode GaN transistors “was deemed a more difficult task.” Ex-2003, 30:2-15.

174. The Petition and Bernstein Declaration allege that POSAs would have made a dual-gate GaN device with an enhancement mode transistor merged with a depletion mode transistor, but fail to cite a single prior art reference that discloses how such a transistor could be made to work successfully. Without prior art disclosure of the structure of a dual-gate GaN device, as claimed by the '003 patent, or how to make one, a POSA would not have had a reasonable expectation of success in doing so. The Bernstein Declaration thus fails to establish that a POSA would have had at least a reasonable expectation of success.

IX. THE PETITION FAILS TO SHOW CLAIMS 1-16 ARE OBVIOUS OVER MISHRA IN VIEW OF REN (GROUND 3)

175. Ground 3 (Mishra in view of Ren) fails to show that claims 1-16 of the '003 patent are obvious.

176. The Petition and the Bernstein Declaration allege that “Mishra discloses implementing dual gate GaN HEMTs in cascode[]” circuits. Petition, 82, citing Ex-1003, [249]. While there is one place in Mishra containing a throw-away statement that “[o]ne alternative arrangement comprises a single transistor with a dual gate structure” (Ex-1009, [0062]), Mishra fails to disclose the structure of such a transistor or how to make one.

177. This lack of disclosure is fatal to Ground 3 because a transistor “with a dual gate structure” does not necessarily comprise a merged cascode transistor comprising a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor as claimed by the ’003 patent (“Limitations[1C9] and [10C10]). In other words, just because Mishra happens to mention an ordinary, known concept, *i.e.*, a dual-gate structure, it does not mean that Mishra discloses the merged cascode transistor claimed by the ’003 patent. The secondary reference, Ren, fails to disclose a dual-gate transistor at all and, thus, does not fill the gap in Mishra’s disclosure.

178. The failure of Mishra and Ren to disclose a transistor with a merged source and drain region is fatal to Ground 3. Even the Bernstein Declaration admits that the requirement of merged source and drain regions of Limitations [1C9] and [10C10] was the very limitation that was added to the claims during prosecution before the claims were allowed. Ex-1003, [059] (“the claims were only allowed after being amended to include the merged limitation and USPTO Examiner identified the merged source and drain regions as the feature that led to allowance of the ’003 patent.”). And yet, this is the very claimed feature missing from the cited prior art of Ground 3.

179. Faced with this limitation absent from the prior art, the Petition and the Bernstein Declaration try to cobble together the missing limitation in a long

series of modifications starting from a single-gate transistor where, essentially, the only stated motivation is that the element to be added was “known” or a similar conclusory statement that it would have been “obvious.” As I explained above, I understand that while there are some circumstances in which expert testimony alone can fill in a limitation missing from the prior art, that is only possible when there has been a showing that the limitation in question is unusually simple and the claimed technology is shown to be particularly straightforward. I understand that the purpose of this requirement is to avoid the risk of hindsight bias. The Petition and Bernstein Declaration fail to make either of these showings.

180. Moreover, even by March 20, 2006, GaN HEMTs were still a new technology. Mishra discloses only depletion-mode GaN HEMTs. This is shown in each of the embodiments of Figs. 2, 4, and 6, which show the gate contact on the buffer layer 18, or channel layer 16. Similarly, Mishra shows only depletion mode MESFETs in Figs. 8 and 9, as evidenced by the gate contact on the channel layer 106. Mishra does not disclose an enhancement mode GaN HEMT, let alone a dual-gate transistor with an enhancement mode GaN HEMT merged with a depletion mode GaN HEMT in the way claimed by the '003 patent. Ren discloses an enhancement mode GaN HEMT but not a dual-gate GaN transistor, let alone one with an enhancement mode GaN HEMT merged with a depletion mode GaN HEMT in the way claimed by the '003 patent. Thus, even if a POSA were

motivated (which a POSA would not have been) to embark on the long journey of modifications that the Petition and Bernstein Declaration chronicles a POSA would have been allegedly motivated to make, the Petition and Bernstein Declaration cite no evidence whatsoever that would support the notion that a POSA would have had at least a reasonable expectation of success in making a dual-gate GaN transistor with an enhancement mode GaN HEMT merged with a depletion mode GaN HEMT in the way the Petition and Bernstein Declaration allege.

181. The Petition thus fails to show that claims 1-16 of the '003 patent are obvious.

A. Neither Mishra nor Ren Disclose a Dual-Gate Transistor with the Drain Region of an Enhancement Mode Transistor Merged with the Source of a Depletion Mode Transistor (Limitations [1C9] and [10C10])

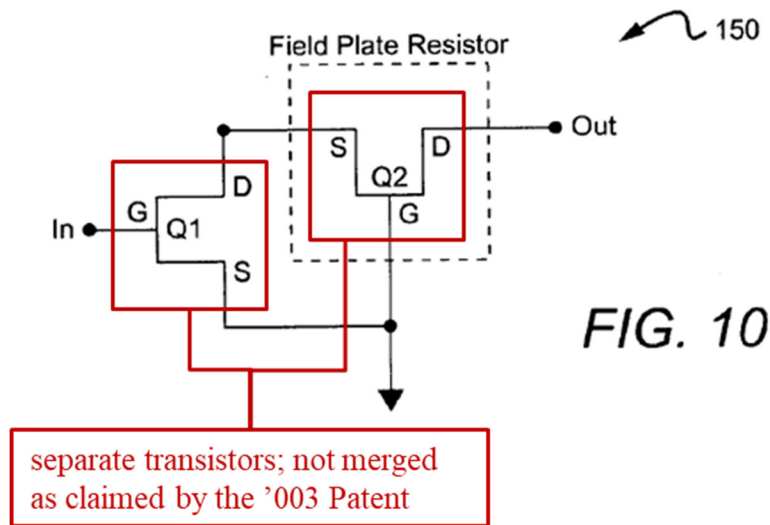
182. Independent claims 1 and 10 both require that “a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor....” *See* Limitations [1C9] and [10C10]. The Petition and the Bernstein Declaration fail to identify any disclosure in either Mishra or Ren that discloses this limitation. Petition, 101-103 (Limitation [1C9] analysis), 113 (Limitation [10C10] analysis cross-referencing the earlier Limitation [1C9] analysis); Ex-1003, [295]-[296] (Limitation [1C9] analysis), [328] (Limitation [10C10] analysis cross-referencing the earlier Limitation [1C9] analysis). This is because Mishra and Ren

lack any disclosure of a drain region of the enhancement mode transistor that is merged with a source region of the depletion mode transistor, as claimed.

1. Mishra's (Ex-1009) Disclosure of an Ordinary "Dual Gate" Transistor Does Not Disclose to a POSA a Transistor with the Drain Region of an Enhancement Mode Transistor Merged with the Source of a Depletion Mode Transistor as Claimed

183. As explained in depth in Section VIII.D.2.a, above, with respect to Ground 2, Mishra discloses a "multi-stage amplifier" circuit but only discloses two individual *single-gate* transistors coupled together with wires or interconnects as shown in Figure 10 (shown annotated, below), and not a dual-gate transistor. Ex-1009, [0058] (stating that Figure 10 discloses "a multi-stage transistor amplifier block" with "a first stage transistor Q1 and a second stage transistor Q2, each of which may comprise a wide-bandgap field effect transistor," meaning that Figure 10 discloses two separate transistors connected together, not a dual-gate transistor); Ex-2009, 154:8-155:2 ("Q. Before the break we were talking about ... whether or not Mishra itself provided a figure that showed a single transistor with a dual-gate structure. And I think the answer was no.... Do I have that right? A. You have that basically right....").

Mishra, Figure 10 (Annotated)



184. As explained in depth in Section VIII.D.2.a, above, all of Mishra's embodiments (Figs. 2, 4, 5, 6, 8, and 9) are of a single-gate transistor that includes a field plate connected to the gate.

185. Mishra does have a throw-away statement in its penultimate paragraph that "[o]ne alternative arrangement comprises a single transistor with a dual gate structure." Ex-1009, [0062]. But Mishra does not disclose the structure of such a transistor. This lack of disclosure is fatal to Ground 3 because the disclosure of the ordinary, known concept, of a dual-gate structure would not be enough to amount to a disclosure, in the eyes of a POSA, of a dual-gate transistor of the type claimed by the '003 patent that comprises a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor.

186. As explained in Section VIII.D.2.a, above, all the embodiments shown in Mishra's figures are depletion mode, so a POSA would have no reason to think Q1 and Q2 would be enhancement mode (and especially not that Q1 would be enhancement mode and Q2 would be depletion mode, or vice versa), especially since, nowhere in Mishra is enhancement mode even mentioned. Indeed, Dr. Bernstein admits that "Mishra does not explicitly comment on the mode in which Q1 operates," *i.e.*, Mishra does not disclose an enhancement mode transistor as claimed by the '003 patent. Ex-1003, [251]; *see also* Ex-2009 ("Q. In paragraph 251 you state: 'Mishra does not explicitly comment on the mode in which Q1 operates in cascode embodiments'; is that right? A. I believe that's exactly what I said before the break. Yes, he does not comment on whether it is -- what mode it is.").

187. Not only does Mishra not disclose the structure or operation of its hypothetical dual-gate transistor, but it also does not disclose that the drain of one gate is merged with the source of the second gate. A POSA would not have understood Mishra to be making such a disclosure, either. For example, the Petition and the Bernstein Declaration cite Sankin (Ex-1003), which discloses dual-gate transistors, but only ones where the drain of the first transistor and the source of the second transistor are connected by wires. *E.g.*, Ex-1008, Figure 2 (annotated below); Ex-2009, 32:18-22 ("Q. ... in figure 2 of Sankin the drain of

the E-mode JFET is connected to the source of the D-mode JFET *by wires*; is that right? A. *That is correct.*”).

Sankin Figure 2 (Annotated)

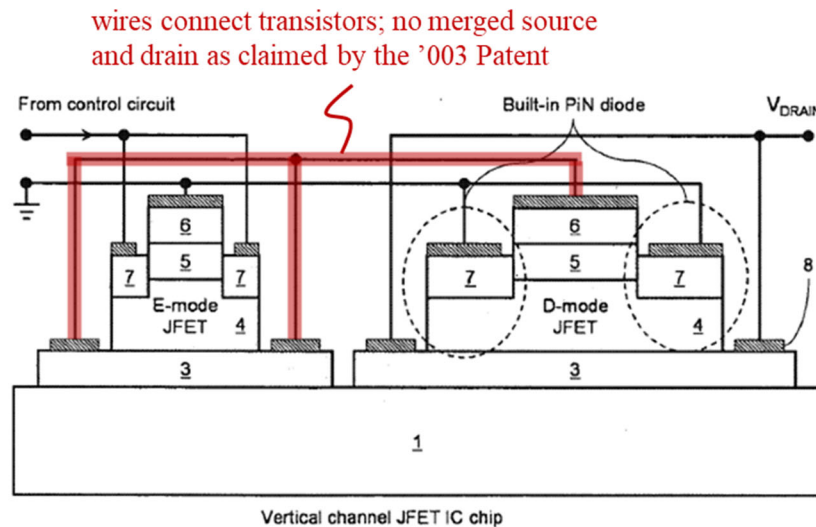


FIG. 2

Ex-1018, Fig. 2.

188. While other art, such as Beach, discloses dual-gate transistors that are not connected by wires, Beach only discloses a dual-gate transistor where both gates have the same mode of operation, and thus does not disclose a transistor with the drain region of an enhancement mode transistor merged with the source of a depletion mode transistor as claimed. Ex-1020, [0048] (“gate electrodes 50, 52 each locally interrupt the 2DEG under the gate contact to interrupt the conduction channel provided at interface 15.”), [0051] (“Gate contacts 50, 52 are both activated to permit current to flow to/from electrode 54, 55.”); Ex-2009, 159:9-160:19 (testifying that Beach’s “intention is to have two enhancement modes,” and

“it looks like those [gates] both have to be enhancement modes because they were above zero”), 161:1-4 (“Q. And you’re not relying on Beach as disclosing an enhancement mode gate next to a depletion mode gate in your report, correct? A. Right. I do not.”).

Beach, Figure 5

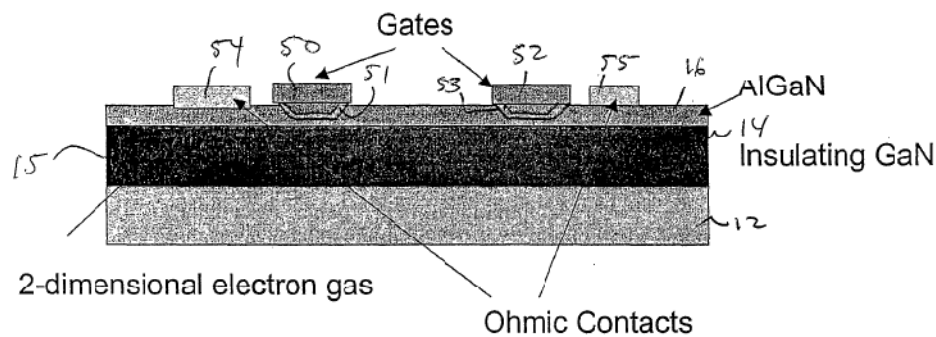


Figure 5

189. Beach further explains that “[i]f one or both of gate contacts 50, 52 are not activated, no current flows between electrodes 54, 55,” “[a]ccordingly, bi-directional device 56 acts as a logic power AND gate, where the switch is active only when both “inputs” are active, meaning gate contacts 50 and 52 are active.”). Ex-1020, [0051]. Since Beach’s device 56 is disclosed as an AND logic gate, a POSA would have known that the two inputs (in this case, gate contacts) would generally be connected to separate variable voltage sources. As even Dr. Bernstein admits, “Mishra does not explicitly comment on the mode in which Q1 operates” (Ex-1003, [251]), which is why a POSA would not have understood Mishra as

disclosing a dual-gate transistor with the drain region of an enhancement mode transistor merged with the source of a depletion mode transistor as claimed.

190. Given the numerous different types of dual-gate transistors that were known, a POSA would not have understood Mishra's disclosure of a generic dual-gate structure to be disclosing the very specific merged cascode structure disclosed and claimed by the '003 patent, with "a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor...." as required by limitations [1C9] and [10C10]).

2. Ren (Ex-1008) Fails to Disclose a Cascode Transistor of Any Type

191. As explained in Section VIII.A.2, Ren does not disclose a cascode configuration or a dual-gate transistor of any type and thus cannot possibly disclose a cascode or dual-gate transistor with a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor as claimed. *See also generally*, Ex-1008. Ren thus does not disclose a cascode or dual-gate transistor with a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor as claimed.

3. Conclusion: Neither Mishra nor Ren Disclose Limitations [1C9] and [10C10]

192. Thus, Limitations [1C9] and [10C10] (“a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor...”) are missing from the cited prior art of Ground 3.

B. Modifying Mishra Based on Ren Would Not Have Arrived at a Transistor Meeting Limitations [1C9] and [10C10]

193. A POSA would not have had reason to combine the teachings of Mishra and Ren, but for the sake of argument, even if one of Ren’s teachings of an enhancement mode transistor were incorporated as Q1 in Mishra’s Figure 10, there would be, at best, Ren’s separate GaN enhancement mode transistor, with its own gate, connected by wires with Mishra’s separate depletion mode transistor, with its own gate.

194. Again, neither Mishra nor Ren discloses the structure of a dual-gate transistor, or how to make one, and neither reference would have given a POSA any reason to transform Mishra’s or Ren’s single-gate transistors into a dual-gate transistor, much less the claimed transistor of the ’003 patent. And given that neither Mishra nor Ren discloses a merged cascode transistor specifically, a POSA would not have arrived at anything resembling the claimed merged cascode transistor of the ’003 patent without the benefit of hindsight.

C. The Petition and the Bernstein Declaration Fail to Even Allege that the Missing Limitation Was Unusually Simple or Particularly Straightforward

195. Unable to find a single prior art reference that discloses a dual-gate transistor with a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor as required by limitations [1C9] and [10C10], the Petition and Bernstein Declaration seek to reconstruct that limitation in hindsight by using expert testimony alone to fill in the missing limitation. Petition, 82-88; Ex-1003, [249]-[260].

196. As I explained above, I understand that while there are some circumstances in which expert testimony alone can fill in a limitation missing from the prior art, that is only possible when there has been a showing that the limitation in question is unusually simple and the claimed technology is shown to be particularly straightforward. I understand that the purpose of this requirement is to avoid the risk of hindsight bias.

197. The Petition and Bernstein Declaration fail to even allege, let alone establish with objective evidence, that the missing limitation is unusually simple or particularly straightforward. Petition, 82-88; Ex-1003, [249]-[260].

198. On the contrary, the missing limitation of a dual-gate transistor with a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor, as required by limitations [1C9] and [10C10], is not

unusually simple. As I explained in detail in Section VIII.D.2.a-d, above, none of the cited art in Ground 3 (which is also cited in Ground 2) discloses a dual-gate transistor with a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor or how to make one. And semiconductor manufacturing continues to involve significant “*trial and error*.” Ex-2008, 1414-EXPERT-0002267-268 (native pages 69-70).

199. The Petition and the Bernstein Declaration thus fail to establish obviousness for this reason alone.

D. The Petition and the Bernstein Declaration Fail to Show a POSA Would Have Had a Reason to Modify Mishra to Meet the Missing Limitations [1C9] and [10C10]

200. Absent disclosure of limitations [1C9] and [10C10], the Petition and the Bernstein Declaration propose modifications to Mishra’s single-gate transistor but do so without providing any plausible reasons why a POSA would have been so motivated to make the modification. Petition, 82-88; Ex-1003, [249]-[260].

1. Using Enhancement Mode for Q1 Would Not Have Been “Obvious” as Alleged

201. The Petition admits that “Mishra does not explicitly comment on the mode in which Q1 operates,” but argues that enhancement mode would have been “obvious” because “[a] POSITA would have understood Mishra’s low voltage bias of source side transistor (Q1) includes low *positive* voltages.” Petition, 83-84, citing Ex-1003, [251]-[252] and Ex-1009, [0060]. The Bernstein Declaration goes

further, alleging that Mishra’s high frequency devices are intended for some vague “high power and high voltage [application], [where] the control signals are generally ***only positive voltages***, requiring that Q1 be an enhancement mode device.” Ex-1003, [252]. But the premise that a POSA would have understood Mishra’s Q1 to be using “only” positive voltages, and thus Q1 must be enhancement mode, is entirely unsupported.

202. First, as the Petition admits, “Mishra does not explicitly comment on the mode in which Q1 operates.” Petition, 83-84. Mishra never discloses an enhancement mode transistor. Mishra does disclose that the Q2 transistors are depletion mode transistors. This is shown in each of the embodiments of Figs. 2, 4, and 6, which show the gate contact on the buffer layer 18, or channel layer 16. Similarly, Mishra shows only depletion mode MESFETs in Figs. 8 and 9, as evidenced by the gate contact on the channel layer 106. Given that the transistor symbols are the same for both in Figure 10, a POSA would have understood Q1 and Q2 to be of the same type (*see* Section VIII.D.2.a, above), a POSA would have understood Q1 to be depletion mode too.

203. Second, Mishra itself never discloses using positive voltages, as both the Petition and Bernstein Declaration allege. Petition, 83-84; Ex-1003, [252]. Paragraph [0060] of Mishra discloses using a negative (“-6V”) voltage, not a positive voltage. Ex-1009, [0060].

204. Third, Mishra discloses that its high frequency devices are actually intended for applications at frequencies up to 10 GHz for signal amplification in civil and military radar, handset cellular, and satellite communications (Ex-1009, [0006], [0009]-[0010]), where “only positive voltages” (as the Bernstein Declaration alleges) are **not** used. In my own industrial experience working with GaN HEMT devices in this time frame, the first viable applications were in signal amplification for civil radio communications, broadband military (electronic warfare), and commercial cellular communications. In these systems, ***positive and negative*** supply voltages were readily available, and often were provided in customers’ SCD (Source Control Document), *i.e.*, the specifications of the overall system, which had both positive and negative supply voltages available in the customer’s system. Even for many years after Mishra and the ’003 patent were disclosed, it was essentially a given that both positive and negative supply voltages were readily available for use in GaN HEMT applications such as those envisioned by Mishra.

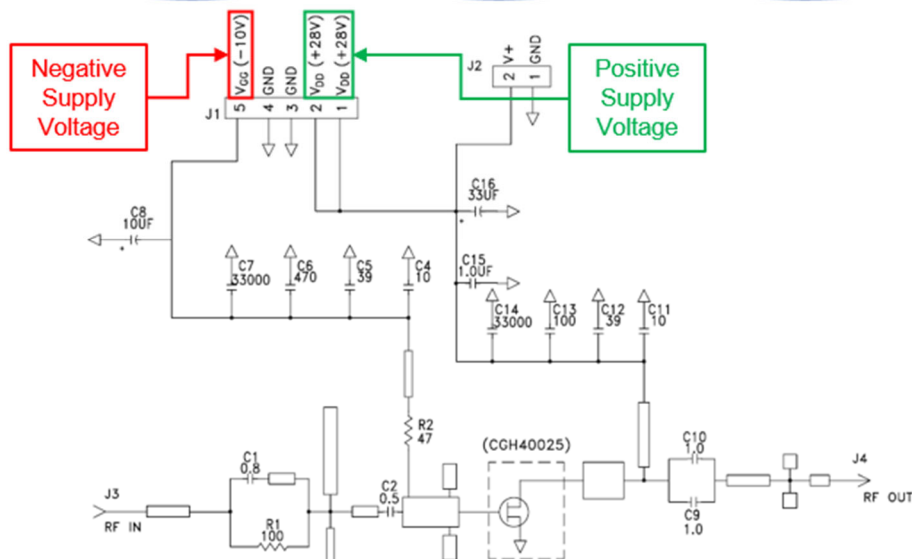
205. For example, Ex-2007 is a true and accurate copy of a preliminary datasheet for the Cree⁸ CGH40025F GaN HEMT that shows a copyright date of 2007. I have intimate knowledge of the CGH40025F GaN HEMT device and have

⁸ Note that Cree (now Wolfspeed) is the designated assignee of Mishra.

used it in a number of my own RF power amplifier designs. The datasheet discloses a “25 W, RF Power GaN HEMT” device with applications in “2-Way Private Radio,” “Broadband Amplifiers,” “Cellular Infrastructure,” “Test Instrumentation,” and “Class A, AB, Linear Amplifiers suitable for OFDM, W-CMDA, EDGE, CDMA waveforms” (*id.*, 1414-EXPERT-0002134) and shows an example application circuit with **both positive** (+28V) (green) **and negative** (-10V) (red) supply voltages, reproduced and annotated below (*id.*, 1414-EXPERT-0002139). Note that the negative supply voltage, “ V_{GG} ,” is used to bias the gate of the CGH40025F, which is a depletion-mode GaN HEMT device.

Cree CGH40025F Data Sheet (Annotated)

CGH40025F-TB Demonstration Amplifier Circuit Schematic



206. Thus, the Petition’s Bernstein Declaration’s proposed reasoning to modify Mishra to make Q1 an enhancement mode transistor is unsupported by any

prior art evidence, and in fact contradicted by the evidence from 2007 that I cite above.

2. Bonn, Sankin, and Salato's Different Applications Would Not Have Motivated a POSA to Modify Mishra

207. The Petition and Bernstein Declaration also cite Bonn, Sankin, and Salato⁹ to show that using an enhancement mode transistor as the first transistor was “known,” but each of Bonn, Sankin, and Salato disclose very different applications than Mishra, so it is not plausible that a POSA would have had reason to use the approach disclosed by those references. Petition, 84; Ex-1003, [252].

208. Mishra discloses that the circuit of Figure 10 is used for signal amplification. Ex-1009, [0006], [0009]-[0010].

209. Bonn discloses using an enhancement mode transistor in a cascode configuration as a mixer. Ex-1006, 2:66-3:1 (“Downconverter 10 also includes a mixer 40 which comprises FETs 30 and 50 coupled in a cascode configuration and serving as *mixer* transistors.”). But an amplifier and a mixer perform two fundamentally different functions. An amplifier takes a *single input signal* and (ideally) produces a *single* higher voltage/current/power *output signal* at the same

⁹ The Petition and Bernstein Declaration fail establish that Salato is prior art. See Section VII, above.

frequency as the input signal.¹⁰ On the other hand, a mixer takes *two input signals* (an RF signal and an LO signal) and produces *two output signals, of which, one, the IF signal* (at a frequency lower than the RF signal, in the case of a downconverter), *is retained* and the other, the “image signal,” is typically filtered out. Moreover, it is often not necessary for a mixer to have gain. A POSA would not have had any reason to have applied Bonn’s teaching about its mixer to Mishra’s amplifier.

210. Sankin and Salato both disclose power supply systems. Ex-1017, 1:31-34 (“cascode configuration of a normally ON depletion mode and a normally OFF [enhancement mode] semiconductor devices allows reliable and safe operation in switching mode *power supply system*.”); Ex-1018, Abstract (“*power switches* are described”). Power supply systems, again, perform different functions than signal amplification for civil and military radar, handset cellular, and satellite communications, as disclosed by Mishra. Ex-1009, [0006], [0009]-[0010].

211. Thus, while the Bernstein Declaration’s citations to Bonn, Sankin, and Salato (*see* Ex-1003, [252]) may very well apply, respectively, to Bonn, Sankin and Salato, a POSA would not have had reason (nor does the Bernstein Declaration supply any) to abandon the applications well-suited to Mishra in favor of those

¹⁰ The ratio of the amplitude of the output to the input signal is known as gain.

suiting to Bonn, Sankin or Salato. Thus, those references' different applications would not have provided a reason for a POSA to have modified Mishra.

3. Adjusting the Threshold Voltage Does Not Change the Mode of Operation of a Transistor

212. The Petition and Bernstein Declaration allege that a POSA would have looked to Ren to adjust the threshold voltage of Mishra's GaN-based transistor (Petition, 85, citing Ex-1003, [255]), but that does not change the mode of operation from depletion mode to enhancement mode, as will be discussed further below. The Bernstein Declaration alleges that because "Mishra discloses using a range of doped and undoped Group III-nitride material with various parameter values," a "POSITA would have been capable of adjusting the threshold voltage of the input to operate in enhancement mode by adjusting the properties of semiconductor layers" and "[a]s I will explain, it would have been obvious to do so over Ren." Ex-1003, [255].

213. However, nothing about Mishra's use of "a range of doped and undoped Group III-nitride material with various parameter values" would have motivated a POSA to look to Ren, specifically. A POSA would have known, and as Mishra explains, using "a range of doped and undoped Group III-nitride material with various parameter values" describes, generally, how the conducting channel in a HEMT is formed. Ex-1009, [0034]. But the mere knowledge of the effect of semiconductor doping does not serve as motivation for a POSA to further

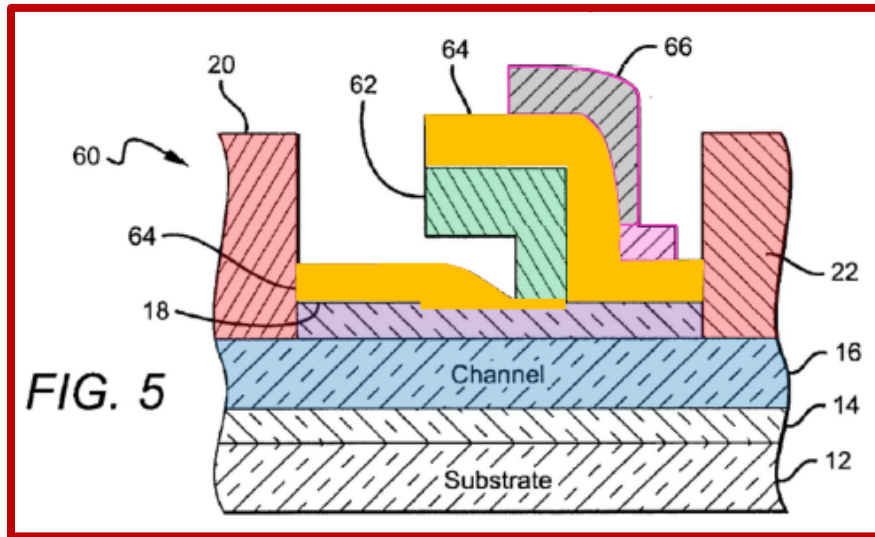
modify a known device (which was, ostensibly, designed with such knowledge in the first place).

214. The Bernstein Declaration’s comment about “adjusting the threshold voltage of the input to operate in enhancement mode by adjusting the properties of semiconductor layers” conflates adjusting threshold voltage with changing a mode of operation from depletion mode (ostensibly, in Mishra’s HEMT devices) to enhancement mode (in Ren’s MOSFET devices). Bernstein’s comment ignores that Ren expressly states that it is a “gate dielectric [] disposed over the channel region [and a] gate electrode [] disposed on the gate dielectric [that results in] a true enhancement MOSFET” (Ex-1008, [0026]), not by “adjusting the properties of [the underlying] semiconductor layers,” as the Bernstein Declaration and the Petition alleges. Petition, 85; Ex-1003, [255].

4. It Would Not Have Been “Obvious” to a POSA to Arrive at the Modified Version of Mishra

215. The Petition alleges a “POSITA would have used Ren’s simple techniques to make Mishra’s first gate enhancement mode and second gate depletion mode,” providing a “Modified Figure 5” that “shows these modifications,” which I will refer to as the Mishra-Ren Combination. Petition, 86-88, citing Ex-1003, [257]-[260].

Alleged Mishra-Ren Combination



But neither the Petition nor the Bernstein Declaration cites objective evidence to establish this alleged obviousness.

216. I understand that obviousness is a legal conclusion based on a framework as described above in Section IV.D and that an expert should have to explain the reasons why a modification would have been made, citing evidence in support. The Bernstein Declaration fails to explain why the modification would have been “obvious” and the report fails to cite evidence substantiating that conclusion. Ex-1003, [257]-[260]. For example, the Bernstein Declaration provides no reason why a POSA would have modified Mishra’s single-gate transistor into a dual-gate transistor. The Bernstein Declaration alleges no benefit of a dual-gate transistor. The Bernstein Declaration alleges no drawback of the two single-gate transistors connected in series, as disclosed in Figure 10 of Mishra. And the

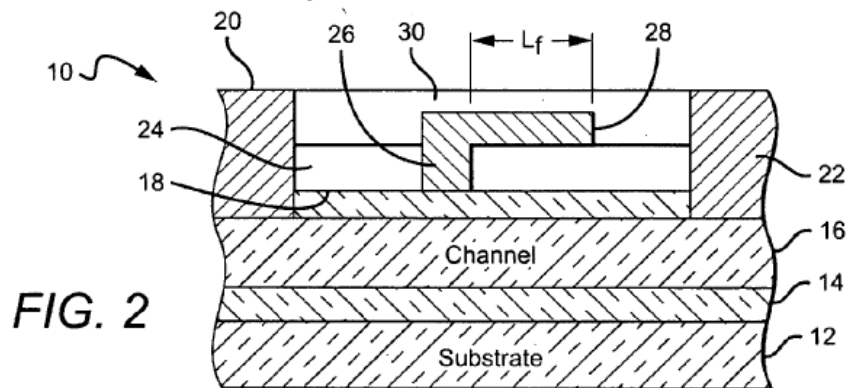
Bernstein Declaration cites no evidence whatsoever of the alleged obviousness.

Absent such analysis and evidence, one can only conclude that hindsight bias is the reason for the proposed modifications, which (as I understand it) is impermissible in an obviousness analysis.

217. The Bernstein Declaration states that “A POSITA would have found it obvious to use Ren’s simple techniques to make Mishra’s first gate enhancement mode and second gate depletion mode” Ex-1003, [257]. But as I explained in Section VIII.D.2.a, Mishra does not disclose the structure of a dual-gate transistor—Mishra discloses the embodiment shown in Figure 5 is a single-gate transistor with a field plate that is connected to that single gate. Moreover, the Bernstein Declaration’s rationale for combining Mishra and Ren fails to show that a POSA would have had reason to make such a combination.

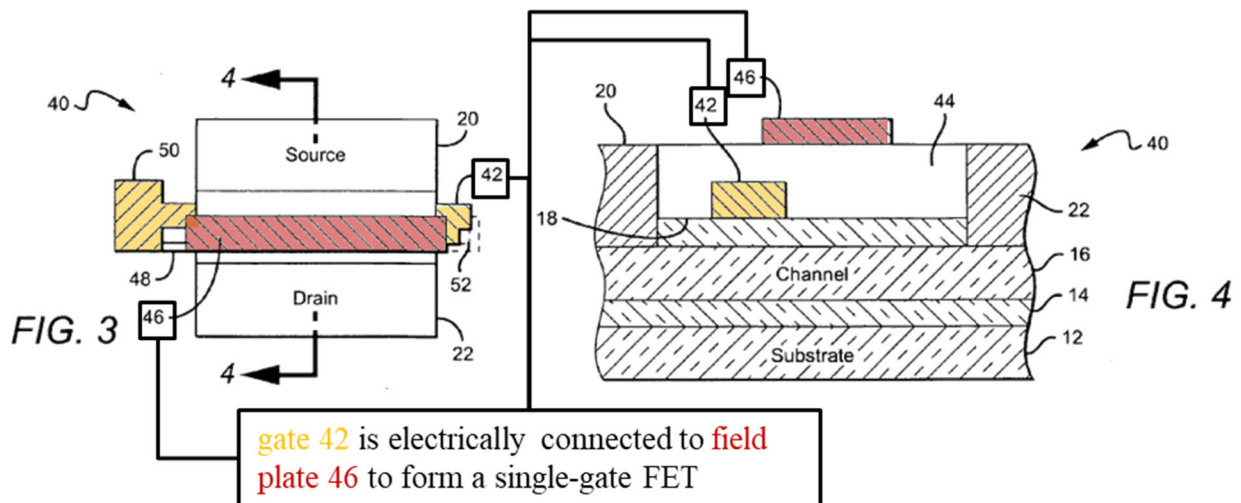
218. For example, the Petition argues that “Mishra already discloses a spacer, dielectric, or passivation layer above the channel that is under the second gate but not under the first gate” and cites “Figs. 2, 4, 5.” Petition, 87. But the Petition provides no reason for selecting Figure 5 and not Figures 2 or 4. Mishra’s Figure 2 would not have met the claims of the ‘003 patent because it only depicts a single gate under any possible interpretation.

Mishra Fig. 2



219. Mishra's Figure 4 would not have met the claims of the '003 patent because its field plate 46, which the Petition argues is a second gate with respect to Figure 5, does not have a field plate as required by Limitations [1C5] and [10C6].

Mishra Figs. 3 and 4



220. Paragraph [258] of the Bernstein Declaration states that an insulated gate would have advantages over a non-insulated gate, as allegedly disclosed by

Ren and Beach, but it is unclear how that would inform or motivate a POSA to try turning a single-gate transistor into a dual-gate transistor.

221. Paragraph [259] of the Bernstein Declaration alleges that Ren discloses an enhancement mode and depletion mode transistor “by varying the thickness of the AlGa_N layer.” But Ren’s teachings involve a “true enhancement MOSFET,” which, unlike Mishra, has a “gate dielectric [] disposed over the channel region [and a] gate electrode [] disposed on the gate dielectric.” Ex-1008, [0026]. Ren does not provide any motivation for creating a dual-gate structure because Ren does not disclose any dual-gate structures of any kind.

222. Paragraph [260] of the Bernstein Declaration alleges predictable results, but attempting to make the alleged Mishra-Ren Combination would have led to anything but predictable results. First, the Bernstein Declaration alleges that a POSA would have “extended layer 64 under Mishra’s gate 62 to realize the benefits of reduced gate leakage.” Ex-1003, [260]. But a POSA would have known that doing so would have required changing and adding to several of Mishra’s processing steps, such as depositing resist, curing the resist, etching/patterning the resist, depositing a new layer, depositing resist, curing the resist, etching/patterning the resist, and etching/patterning the new layer for each new added layer. As a POSA would have known, not only is each processing step comprised of several sub-processes, but depending on the materials and methods required, the

semiconductor wafers would need to be transported from one set of apparatuses to another set of apparatuses, which carries its own inherent risks. All of this would have had to be done without disrupting the flow of all of the other processing steps.

223. Moreover, as a POSA would have known, each process step, and its constituent sub-processes, are performed under different environmental conditions (temperatures, pressures, humidities, etc.) and involve different materials and chemical processes that can create incompatibilities and require that one process step/steps occur before/after another process step/steps. Similar to baking a cake (but obviously far, far more complicated and tedious), one process step usually cannot simply be swapped in or out with another. Adding the wrong amounts (of yeast, flour, water, etc.) or at the wrong time, heating the oven to the wrong temperature, not allowing the oven to pre-heat to a prescribed temperature, not allowing the dough to rise/rise high enough, and so on and so forth, are not likely to yield predictable results. In semiconductor processing, the odds of success when making such unknown/untested changes go down at least a million-fold.

224. Specifically, in Mishra's process, gate 62 is formed *before* a "*spacer/passivation layer 64 is included that covers the gamma gate 62* and the surface of the barrier layer 18 between the gamma gate 62 and the source and drain contacts 20, 22." Ex-1009, [0043]. A POSA would have known that the extensive sub-processes associated with each layer fabrication described above would have

to be repeated several times to move Mishra's gate 62 on top of the passivation layer 64. For example, the Bernstein Declaration says a POSA would have "etch[ed] under the gate 62 to decrease AlGa_N thickness and maintain enhancement mode in gate 62." Ex-1003, [260].

225. But as a POSA would have known, additional process steps would likely be needed after etching, such as thermally annealing the etched semiconductor surface to later deposit a new passivation layer between the Bernstein Declaration's new gate 62 and field plate 66. Moreover, the Bernstein Declaration says nothing about the material composition, thickness, deposition method, etc. that would need to be carefully considered to make a high-quality and reliable new passivation layer between the new gate 62 and field plate 66. Of course, even after all of this, Dr. Bernstein's "simple modification" (Ex-1003, [260]) would additionally require "adjust[ing] the doping characteristics and AlGa_N thickness, as Ren discloses to *predictably* achieve an enhancement mode (thinner AlGa_N) and depletion mode gates (thicker AlGa_N) of the original Mishra's device." *Id.* As a POSA would have known, there would have been nothing simple about this, much less would it have been likely to yield predictable results.

226. A POSA would have also known that changing and adding process steps to an existing process is not only costly but carries an inherent risk of

negatively impacting the desired performance of the device, both in ways that are predictable and in ways that are not or could not be foreseen. As a practitioner of semiconductor processing, a POSA would have known that “***innovation in semiconductor manufacturing processes***, particularly the development and introduction of new process technology in this industry, ***retains a strong element of trial and error.***” Ex-2008, 1414-EXPERT-0002267-268 (native pages 69-70). Ex-2008 chronicled the challenges Intel faced when trying to duplicate a semiconductor fabrication line. In fact, the risks and unpredictable consequences (like in the proverbial “Butterfly Effect”) of changing a known semiconductor process are so great that even Intel Corporation uses the so-called “copy exactly” philosophy:

A good example of this approach to process innovation is the so-called “copy exactly” philosophy that the Intel Corporation relies on in transferring process technologies among manufacturing plants. This approach to managing the development and transfer of process technologies concedes that ***in the absence of a complete understanding of the process technology it is necessary to copy the entire system—the length of pipes, the placement of equipment—exactly, rather than in a way that is based on engineering or scientific knowledge.*** This is a remarkable example of pre-scientific problem solving and trial-and-error experimentation in this industry.

Id. at 1414-EXPERT-0002268 (native page 70).

227. It is thus extremely unlikely that a POSA would have had reason to make the Mishra-Ren Combination, which would require multiple different process changes, as the Bernstein Declaration alleges. On the contrary, a POSA

would **not** have had reason to brazenly and cavalierly change a known process, much less to import untested process steps from some outside process as the Bernstein Declaration alleges.

228. In sum, the Bernstein Declaration fails to articulate any reason why a POSA would have transformed Mishra's single-gate transistor into a dual-gate transistor, let alone the Mishra-Ren Combination. None of the reasons stated in the Bernstein Declaration is sufficient to show obviousness based on my understanding of the legal framework (*see* Section IV.D, above).

E. The Petition and the Bernstein Declaration Fail to Show a POSA Would Have a Reasonable Expectation of Success

229. The Petition and the Bernstein Declaration fail to establish that a POSA would have had at least a reasonable expectation of success in transforming Mishra's single-gate transistor into a dual-gate transistor with a drain region of an enhancement mode transistor merged with a source region of a depletion mode transistor, as claimed by the '003 patent. The Petition only ever alleges success or predictability twice in Ground 3, in a single paragraph spanning pages 86-87, citing only the Bernstein Declaration at paragraph [260]. But Dr. Bernstein's opinion of predictability is not supported by the prior art, especially in view of the inherent risks and unintended consequences I explained in Section IX.D.4, above.

1. None of the Cited Art Shows How to Make a Dual-Gate Transistor with the Drain Region of an Enhancement Mode Transistor Merged with the Source of a Depletion Mode Transistor

230. Paragraph [260] of the Bernstein Declaration (and the corresponding portion of the Petition at pages 86-87) describes why a POSA might have known how to make a single-gate AlGaIn/GaN enhancement mode transistor and a single-gate AlGaIn/GaN depletion mode transistor based on the teachings of Ren, but Ren does not disclose a dual-gate transistor, let alone a dual-gate transistor having a drain region of an enhancement mode transistor merged with a source region of a depletion mode transistor. *See generally* Ex-1008. As such, Ren cannot possibly provide any evidence that a POSA would have had at least a reasonable expectation that such a dual-gate transistor would be made successfully or that one could be made with the same techniques used to make single-gate transistors.

231. The same is true of U.S. Patent No. 6,586,781 (Ex-1021, “Wu”) and U.S. Patent Publication No. 2002/0167023 (Ex-1022, “Chavarkar”), which are cited in paragraph [260] of the Bernstein Declaration and the corresponding portion of the Petition at pages 86-87. Neither Wu nor Chavarkar discloses a dual-gate transistor of any kind, let alone a dual-gate transistor having a drain region of an enhancement mode transistor merged with a source region of a depletion mode transistor. Wu and Chavarkar thus provide no evidence that a POSA would have

had at least a reasonable expectation of success in making such a dual-gate transistor as the one claimed by the '003 patent.

232. The Bernstein Declaration additionally cites Beach (Ex-1020) (*see* Ex-1003, [260]), which the Petition does not cite. But as explained in Section VIII.D.2.c, while Beach discloses a dual-gate transistor (e.g., Fig. 5, below), both gates have the same mode of operation, not an enhancement mode transistor merged with a depletion mode transistor as claimed by the '003 patent. *See also* Ex-1020, [0048] (“gate electrodes 50, 52 each locally interrupt the 2DEG under the gate contact to interrupt the conduction channel provided at interface 15.”), [0051] (“Gate contacts 50, 52 are both activated to permit current to flow to/from electrode 54, 55.”).

Beach, Figure 5

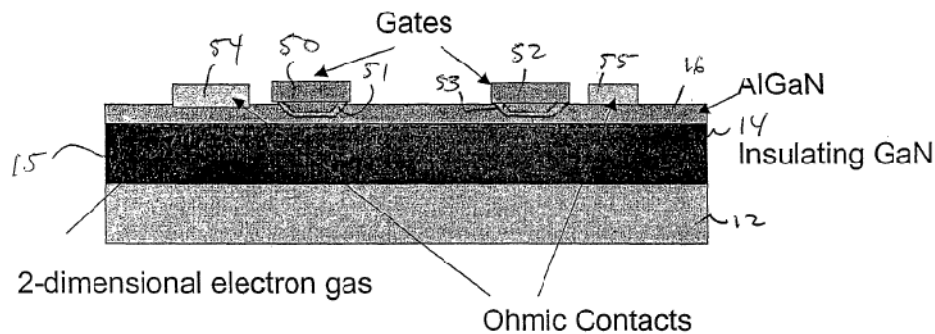


Figure 5

Beach thus does not disclose the structure of a dual-gate GaN transistor with an enhancement mode transistor merged with a depletion mode transistor, does not disclose the operation of such a dual-gate GaN transistor, and does not disclose

how such a dual-gate GaN transistor would be made. Beach thus provides no enabling disclosure of the type of dual-gate transistor claimed by the '003 patent and thus provides no evidence of predictably making one.

2. The Failure to Cite Any Art Disclosing a Dual-Gate Transistor as Claimed is Fatal Because GaN Technology Was Still New

233. As I explained above in Section VIII.D.1, in my analysis for Ground 2, the complete lack of disclosure that would have taught a POSA how to make a dual-gate GaN FET with an enhancement mode transistor merged with a depletion mode transistor in the prior art cited by the Bernstein Declaration is fatal to Ground 3 because there is, therefore, no evidence to show a POSA would have had a reasonable expectation of success in making the Mishra-Ren Combination.

234. As the Bernstein Declaration admits, in the late 1990s, “GaN devices were in early development and uncommon.” Ex-1003, [158]. While the Bernstein Declaration (and the Petition) suggests that by 2006 “improvements to GaN manufacturing techniques made these devices more common than they were previously” (*id.*, [195]; *see also* Petition, 51), this does not show that GaN semiconductor processing, much less GaN device and circuit engineering, was so well understood that a POSA would have expected to be able to successfully make a merged cascode transistor out of GaN, especially without undue experimentation.

235. Even by March 20, 2006, GaN was still a relatively new technology. For example, Thomas Herman, inventor of the '003 patent, explained that making enhancement mode GaN transistors “was deemed a more difficult task.” Ex-2003, 30:2-15 (“Q. Did you design semiconductors with enhancement mode gates while you were at IR? A. The bulk of the effort at IR was depletion mode gates and transistors in GaN. Q. Did you also design enhancement mode transistors in GaN? A. There was interest in designing enhancement mode GaN transistors, but *that was deemed a more difficult task*. And I don't believe there was any active effort to specifically fabricate enhancement mode GaN transistors, other than, you know, feasibility and discussions. But I don't believe there was any effort to physically fabricate an enhancement mode GaN device.”).

236. Mr. Herman’s recount of the state of the art is consistent with my own recollection from the time. Even today, I am not aware of any disclosure of a merged cascode transistor made from GaN as of 2006.

237. And a POSA would have known that “*innovation in semiconductor manufacturing processes*, particularly the development and introduction of new process technology in this industry, *retains a strong element of trial and error*.” Ex-2008, 1414-EXPERT-0002267-268 (native pages 69-70).

In sum, the Bernstein Declaration does not cite any plausible reasons why a POSA would have had at least a reasonable expectation of successfully designing and

making a dual-gate GaN device as the Bernstein Declaration proposes. The Bernstein Declaration cites no disclosure of any prior art that taught the structure of a dual-gate GaN device as claimed by the '003 patent or how one would be successfully made. Additionally, Mr. Herman's testimony demonstrates the fact that GaN was still a relatively new technology to work in as of the mid-2000s. Without prior art disclosure of the structure of a dual-gate GaN FET or how to successfully make one, a POSA would not have had a reasonable expectation of doing so. The Bernstein Declaration thus fails to establish that a POSA would have had at least a reasonable expectation of success.

X. CONCLUSION

238. I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

239. I declare under penalty of perjury that the foregoing is true and correct.

Dated: September 30, 2025

By: 

David K. Choi, Ph.D.

APPENDIX A: MATERIALS CONSIDERED

Document	Description
Paper 1	Petition for Inter Partes Review of U.S. Patent No. 8,264,003
Paper 9	Institution Decision
Ex-1001	U.S. Patent No. 8,264,003 (“the ’003 patent”)
Ex-1002	Prosecution History of the ’003 Patent (“Prosecution History”)
Ex-1003	Declaration of Joseph B. Bernstein, Ph.D. (“Bernstein”)
Ex-1004	Curriculum Vitae of Joseph B. Berstein, Ph.D.
Ex-1005	U.S. Patent Publication No. 2005/0189561 to Kinzer et al. (“Kinzer561”)
Ex-1006	U.S. Patent No. 6,160,280 to Bonn et al. (“Bonn”)
Ex-1007	U.S. Patent No. 6,483,135 to Mizuta et al. (“Mizuta”)
Ex-1008	U.S. Patent Publication No. 2004/0041169 to Ren et al. (“Ren”)
Ex-1009	U.S. Patent Publication No. 2005/0051800A1 to Mishra et al. (“Mishra”)
Ex-1010	Excerpts Of Public Verified Complaint of Infineon Technologies Austria AG and Infineon Technologies Americas Corp. Under Section 337, Inv. No. 337-TA-1414 (July 26, 2024).
Ex-1011	Exhibit 17 to Public Complaint in Inv. No. 337-TA-1414
Ex-1012	U.S. Patent Publication No. 2002/0171096A1 to Wakejima et al. (“Wakejima”)
Ex-1013	U.S. Patent Publication No. 2005/0051796 to Parikh et al. (“Parikh”)
Ex-1014	U.S. Patent No. 7,800,131 to Miyamoto et al. (“Miyamoto”)
Ex-1015	U.S. Patent No. 7,548,112 to Sheppard (“Sheppard”)
Ex-1016	U.S. Patent Publication No. US 2007/0170463 to Ueno et al. (“Ueno”)

Document	Description
Ex-1017	U.S. Patent No. 7,408,399 to Salato et al. (“Salato”)
Ex-1018	U.S. Patent Publication No. 2006/0113593 A1 to Sanking et al. (“Sankin”)
Ex-1019	B. M. Green et al., “High-power broad-band AlGa _N /Ga _N HEMT MMICs on SiC substrates,” in <i>IEEE Transactions on Microwave Theory and Techniques</i> , vol. 49, no. 12, pp. 2486-2493, Dec. 2001, doi: 10.1109/22.971640 (“Green”)
Ex-1020	International Patent Publication Number WO 2005/070009 (“Beach”)
Ex-1021	U.S. Patent No. 6,586,781 to Wu et al. (“Wu”)
Ex-1022	U.S. Patent Publication No. 2002/0167023 to Chavarkar et al. (“Chavarkar”)
Ex-1023	Bernstein JB, Gleason EF, Wetsel AE, Liu EZ, Wyatt PW. “Anomalous Behavior of Semi-Insulating Silicon Rich Amorphous Silicon Nitride.” <i>MRS Proceedings</i> . 1992; 284:113. doi:10.1557/PROC-284-113 (“Bernstein-SiN”)
Ex-1024	Tessmann, A., Haydl, W. H., Hulsman, A., & Schlechtweg, M. (1998). High-gain cascode MMICs in coplanar technology at Wband frequencies. <i>IEEE Microwave and Guided Wave Letters</i> , 8 (12), 430-431 (“Tessman”)
Ex-1025	Potirakis, S. M., and Alexakis, G. E. (2005). An accurate calculation of Miller effect on the frequency response and on the input and output impedances of feedback amplifiers. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 52(8), 491-495. (“Potirakis”)
Ex-1026	J. Lerdworatawee and Won Namgoong, "Wide-band CMOS cascode low-noise amplifier design based on source degeneration topology," in <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , vol. 52, no. 11, pp. 2327-2334, Nov. 2005, doi: 10.1109/TCSI.2005.853585. (“Lerdworatawee”)

Document	Description
Ex-1027	Ko, B. K., & Lee, K. (1996). A comparative study on the various monolithic low noise amplifier circuit topologies for RF and microwave applications. <i>IEEE Journal of Solid-State Circuits</i> , 31(8), 1220-1225 (“Ko”)
Ex-1028	Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al., No. 3:24-cv-01553-SK, Dkt. No. 56, Order Staying and Conditionally Closing Case for Statistical Purposes (N.D. Cal. Aug. 27, 2024)
Ex-1029	LTspice cascode amplifier simulation
Ex-1030	LTspice cascode amplifier schematic
Ex-1031	LTspice cascode amplifier simulation data
Ex-1032	LTspice cascode amplifier graph
Ex-2002	Horowitz, P., & Hill, W. (1989). <i>The Art of Electronics</i> (2nd ed.). Cambridge University Press.
Ex-2003	Transcript Excerpt from Deposition of Thomas Herman dated January 17, 2025. <i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; ITC Inv. No. 337-TA-1414.
Ex-2006	Mil’Shtein, S., et al., Heterostructure transistor with tunable gate bias, <i>Microelectronics Journal</i> 36 (2005) 301-303.
Ex-2007	Preliminary Cree CGH40025F Datasheet, May 2007.
Ex-2008	Jorgenson, Dale W., et al. eds., <i>Measuring and Sustaining the New Economy: Report of a Workshop</i> (National Academy Press, 2002).
Ex-2009	Transcript of Deposition of Joseph B. Bernstein dated August 27, 2025. <i>Innoscience America, Inc. v. Infineon Technologies Americas Corp.</i> , IPR2025-00094.
Ex-2010	Errata to the Deposition of Joseph B. Bernstein dated September 27, 2025

APPENDIX B: CLAIM LISTING¹¹

Claim Element	Claim Language
[1PRE]	A merged cascode transistor circuit comprising:
[1A]	an input voltage signal source having an input voltage signal;
[1B]	a constant voltage source having a predetermined constant voltage;
[1C]	a merged cascode transistor comprising:
[1C1]	a semiconductor element;
[1C2]	a source electrode electrically connected to a top surface of the semiconductor element;
[1C3]	a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
[1C4]	a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
[1C5]	a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
[1C6]	wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
[1C7]	the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,

¹¹ These claim element labels correspond to those applied by the Petition. *See* Paper 1, “Claim Appendix.”

Claim Element	Claim Language
[1C8]	wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
[1C-9]	wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.
[2PRE]	The merged cascode transistor of claim 1, wherein the semiconductor element further comprises:
[2A]	a first III-Nitride layer; and
[2B]	a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.
3	The merged cascode transistor of claim 2, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.
4	The merged cascode transistor of claim 3, wherein the first III-Nitride layer comprises AlGaN material and the second III-Nitride layer comprises GaN material.
5	The merged cascode transistor of claim 4, further comprising an insulating layer positioned between the first and second gates and the first III-Nitride layer such that the first and second gates are capacitively coupled to the first III-Nitride layer.
6	The merged cascode transistor of claim 5, wherein the first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.
7	The merged cascode transistor of claim 6, where in the predetermined level is a pinch off voltage of the second portion of the transistor.
8	The merged cascode transistor of claim 7, wherein the insulation layer is comprised of silicon dioxide.
9	The merged cascode transistor of claim 8, wherein the insulation layer is comprised of silicon nitride.

Claim Element	Claim Language
[10PRE]	A merged cascode high electron mobility transistor circuit comprises:
[10A]	an input voltage signal source having an input voltage signal;
[10B]	a constant voltage source having a predetermined constant voltage;
[10C]	a merged cascode transistor comprising:
[10C1]	a first epitaxial layer of III-Nitride material;
[10C2]	a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;
[10C3]	a source electrode electrically connected to the first epitaxial layer;
[10C4]	a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;
[10C5]	a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and
[10C6]	a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;
[10C7]	wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and
[10C8]	the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
[10C9]	wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
[10C10]	wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

Claim Element	Claim Language
11	The merged cascode high electron mobility transistor of claim 10, further comprising an insulating layer positioned between the first and second gates and the first epitaxial layer.
12	The merged cascode high electron mobility transistor of claim 11, wherein the first epitaxial layer comprises an AlGa _N material and the second epitaxial layer comprises a Ga _N material.
13	The merged cascode high electron mobility transistor of claim 12, wherein first portion of the transistor conducts when the input voltage signal provides an input voltage above a predetermined threshold voltage.
14	The merged cascode high electron mobility transistor of claim 13, wherein the predetermined level is a pinch off voltage of the second portion of the transistor.
15	The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon dioxide.
16	The merged cascode high electron mobility transistor of claim 14, wherein the insulating layer is comprised of silicon nitride.