

**In the Matter of:**

*Innoscence America, Inc. vs  
Infineon Technologies Americas Corp.*

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*Joseph B. Bernstein*

*August 27, 2025*

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1 UNITED STATES PATENT AND TRADEMARK OFFICE

2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3  
4 INNOSCIENCE AMERICA, INC., :

5 Petitioner, : Case No.:

6 VS. : IPR 2025-00094

7 INFINEON TECHNOLOGIES AMERICAS: Patent No.

8 CORP., : 8,264,003

9 Patent Owner. : Pages 1-202

10  
11 - - -  
wednesday August 27, 2025  
12 - - -

13 Deposition of JOSEPH B. BERNSTEIN,  
14 PH.D., taken by patent owner at Finnegan Henderson  
15 Farabow Garrett & Dunner, LLP, 1875 Explorer Street,  
16 Suite 890, Reston, VA 20190 commencing at 9:28 a.m.,  
17 before Sherry L. Brooks, Certified LiveNote Reporter  
18 and Notary Public, in and for the Commonwealth of  
19 Virginia.

20 - - -  
21 MAGNA LEGAL SERVICES

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A P P E A R A N C E S :

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(Via Zoom)

I N D E X

- - -

TESTIMONY OF: JOSEPH B. BERNSTEIN, PH.D.

By Mr. Balich 6, 195

By Mr. MacDonald 187

P R E V I O U S L Y M A R K E D E X H I B I T S

| EXHIBIT NUMBER | DESCRIPTION | PAGE MARKED |
|----------------|-------------|-------------|
|----------------|-------------|-------------|

|              |                                                  |   |
|--------------|--------------------------------------------------|---|
| Exhibit 1003 | Expert Declaration of Joseph B. Bernstein, PH.D. | 8 |
|--------------|--------------------------------------------------|---|

|              |                                                             |    |
|--------------|-------------------------------------------------------------|----|
| Exhibit 1006 | United States Patent 6,160,280<br>Bonn, et al. - 12/12/2000 | 45 |
|--------------|-------------------------------------------------------------|----|

|              |                                                                  |     |
|--------------|------------------------------------------------------------------|-----|
| Exhibit 1007 | United States Patent 6,483,135<br>B1 - Mizuta, et al. - 11/19/02 | 103 |
|--------------|------------------------------------------------------------------|-----|

|              |                                                                                                           |     |
|--------------|-----------------------------------------------------------------------------------------------------------|-----|
| Exhibit 1009 | United States Patent<br>Application Publication,<br>Mishra, et al. - 3/10/05<br>Pub. No.: 2005/0051800 A1 | 123 |
|--------------|-----------------------------------------------------------------------------------------------------------|-----|

EXHIBITS CONTINUED:

P R E V I O U S L Y   M A R K E D   E X H I B I T S

| EXHIBIT NUMBER | DESCRIPTION | PAGE MARKED |
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|              |                      |    |
|--------------|----------------------|----|
| Exhibit 1018 | United States Patent | 26 |
|--------------|----------------------|----|

Application Publication

Sankin, et al. - 6/1/06

Pub. No.: 2006/0113593 A1

|              |                             |    |
|--------------|-----------------------------|----|
| Exhibit 1019 | High-Power Broad-Band AlGaN | 23 |
|--------------|-----------------------------|----|

HEMT MMICs on SiC Substrates

Bruce M. Green, et al.

|              |                           |     |
|--------------|---------------------------|-----|
| Exhibit 1020 | International Application | 156 |
|--------------|---------------------------|-----|

Published Under the Patent

Cooperation Treaty (PCT)

WO 2005/07009 A2 - 8/4/05

EXHIBITS CONTINUED:

NEWLY MARKED EXHIBIT

|              |                            |     |
|--------------|----------------------------|-----|
| Exhibit 2006 | Heterostructure Transistor | 174 |
|              | with Tunable Gate Bias -   |     |
|              | S. Mil'shtein, J. Palma -  |     |
|              | Dated 4/19/05              |     |
|              | Journal from 2005          |     |

(Exhibit 2006 retained by Counsel - Agile Law.)  
(Exhibits 1003, 1006, 1007, 1009,  
1018-1020 attached to transcript.)

- - -

P R O C E E D I N G S

- - -

WHEREUPON,

JOSEPH B. BERNSTEIN, PH.D.

after having been first duly sworn, was  
examined and testified as follows:

- - -

EXAMINATION BY COUNSEL FOR PATENT OWNER  
BY MR. BALICH:

Q. Good morning, Mr. Bernstein. Could you  
state your name and business address for the record?

A. Joseph Bernstein, and my address is 48  
Meshech Chochmah, M-E-S-H-E-C-H, C-H-O-C-H-M-A (sic),  
in Modi'in Illit -- is the name of the city,  
I-L-L-I-T, in Israel.

Q. My name is Jason Balich and I represent  
the patent owner, Infineon. And you've been deposed  
several times before; is that correct?

A. That is correct.

Q. So I'm just going to remind you of some of  
the ground rules. I'm going to be asking questions  
today, and if at any time you don't understand a

1 question, could you please let me know?

2 A. Yes.

3 Q. And if you don't ask me to clarify a  
4 question, can we assume that you understood what my  
5 question was?

6 A. Yes.

7 Q. And if at any time you need a break,  
8 please let me know.

9 All right?

10 A. Okay.

11 Q. The only thing that I ask is that if  
12 there's a pending question that you answer the  
13 pending question before the break.

14 Is that fair?

15 A. That is fair.

16 Q. Is there any reason that you wouldn't be  
17 able to testify truthfully and completely to the  
18 questions I ask today?

19 A. I don't believe so.

20 Q. Okay. So as I mentioned off the record  
21 beforehand we have two different ways of looking at  
22 exhibits. We've got an iPad with Agile Law and

1 you've brought a copy of the exhibits. Feel free to  
2 use whichever copy is most comfortable to you.

3 And if we could start with Exhibit 1003,  
4 which is your declaration?

5 A. Yes.

6 Q. Do you recognize Exhibit 1003 as the  
7 expert declaration that you submitted in connection  
8 with this matter?

9 A. Yes.

10 Q. And so if I refer to your declaration,  
11 you'll understand that I'm referring to Exhibit 1003,  
12 correct?

13 A. Yes, I will understand that.

14 Q. Okay. If you could turn to the last page,  
15 do you see that there's two page numbers at the  
16 bottom?

17 A. Yes.

18 Q. So one page number is in the middle,  
19 right? Correct?

20 A. Yes, 169.

21 Q. Yep. And then there's another page number  
22 on the bottom left?

1           A.     182 of 182.

2           Q.     Can we agree that during this deposition  
3 that I'm going to refer to the page numbers on the  
4 bottom left?

5           A.     That's fine.

6           Q.     Okay. So looking at page 182 of your  
7 declaration, is that your signature?

8           A.     That is my signature, yes.

9           Q.     And you signed your declaration on  
10 November 14, 2024; is that correct?

11          A.     That's what it says. So it's correct.

12          Q.     Okay. Since then have you found anything  
13 in your declaration that you need to correct?

14          A.     Going through it I have noticed some  
15 grammatical minor changes. I noticed -- and I can't  
16 even find them. Like it would say CB-7 or something,  
17 but they're just minor and I don't think there's  
18 anything that needs to be corrected that's not  
19 obviously just a typo or something.

20          Q.     Got it. I understand. Have you ever  
21 previously provided expert testimony for Innoscience  
22 before?

1 A. No, this is my first time.

2 Q. And have you ever provided expert  
3 testimony for Infineon before?

4 A. I don't believe I ever have given  
5 testimony for Infineon.

6 Q. And have you ever worked for Innoscience  
7 before this present engagement?

8 A. No, I did not.

9 Q. And have you ever worked for Infineon?

10 A. As I'm thinking, I think I gave a remote  
11 lecture. I'm pretty sure I did give a lecture on  
12 reliability, which is my expertise, and I think there  
13 was an engagement with Infineon a number of years  
14 ago. It's very hard to recall even if I have any  
15 records of it.

16 Q. And have you ever worked with the Finnegan  
17 law firm before your present engagement?

18 A. No. This is my first time working for  
19 Finnegan.

20 Q. So if you turn to page 14 of your  
21 declaration, paragraph 3, you state you are being  
22 compensated for your time at your standard hourly

1 consulting rate; is that right?

2 A. That's right.

3 Q. what is your standard hourly consulting  
4 rate?

5 A. My consulting rate is \$600 per hour.

6 Q. And how many hours did you spend from the  
7 time you were engaged by Innoscience until the time  
8 that you signed your declaration?

9 A. I know they always ask that, but I don't  
10 really keep good track. It was several weeks, I  
11 guess. Maybe about -- let's see. well, let's say  
12 all together it may be \$30,000. So divide that by  
13 \$600, whatever it is.

14 Q. Okay. And then how many hours have you  
15 spent since signing your declaration?

16 A. working on this particular project?

17 Q. Yes.

18 A. Not so much. Just preparation since I've  
19 been -- paid for my plane fare and a few days that  
20 I've been here, so however many hours there are in a  
21 day. I'm here full-time for them these last few  
22 days.

1 Q. Okay. So you were preparing for your  
2 deposition for two days?

3 A. Yes.

4 Q. If you could turn to page 38 of your  
5 declaration, paragraph 61. Let me know when you're  
6 there.

7 A. Yes.

8 Q. Okay. You state that cascodes are  
9 two-stage amplifiers having a first upper FET and a  
10 second lower FET that share a common source at the  
11 first FET; is that right?

12 A. That is what it says.

13 Q. Okay. What does having a common source  
14 mean?

15 A. Common usually means ground. The common  
16 node is the ground node in general. Although for  
17 instance, I do experiments where there can be two  
18 sort of commons (sic) depending if you have an  
19 interface someplace else.

20 But, generally, the common node is where  
21 you would reference all other voltages to the common  
22 node. That's why it's generally ground zero. So a

1 voltage is positive if it's above the ground  
2 potential; negative if it's below the ground  
3 potential.

4 Q. So with a cascode, does the ground have to  
5 be connected to particular parts of the first and the  
6 second FET?

7 A. Well, to be a cascode the only requirement  
8 is that the drain of we'll call it the lower  
9 transistor is connected directly to the source of an  
10 upper transistor. Pretty much that's the definition  
11 of cascode.

12 Q. So other than the drain of the lower  
13 transistor being connected to the source of the upper  
14 transistor, there's no other requirement for it to be  
15 a cascode?

16 MR. MACDONALD: Objection. Form.

17 A. Well, I have seen people referring to the  
18 what we'll call the gate. It's generally in the FET  
19 mode that -- we'll call the upper transistor the  
20 higher voltage transistor on the drain side.

21 It's usually -- and I think what I've  
22 seen, you know, I'd say almost always -- but not

1 always because I know that sometimes it's not, but  
2 generally that would be grounded.

3 so there would be a common gate that would  
4 generally be a cascode, depending on how the  
5 transistors are configured.

6 so the cascode has sort of two properties  
7 to be really called cascode. Although, again, these  
8 kinds of definitions in engineering are sometimes a  
9 little bit loose depending on how the designer means  
10 it, but generally the source is grounded and you  
11 would have a common gate, as they call it.

12 BY MR. BALICH:

13 Q. Okay. But the common gate is not required  
14 to meet the definition of a cascode, strictly  
15 speaking?

16 MR. MACDONALD: Objection to form.

17 A. I have seen -- actually, it was brought up  
18 to my attention that even wikipedia defines that the  
19 gate would be grounded in a -- and, again, I -- you  
20 know, in my experience, as I said, I didn't look  
21 through engineering dictionaries.

22 But I understand that commonly, most

1 commonly -- and I'm saying this because I know that  
2 even in Bonn, for instance, he would call it a  
3 cascode, and it's not -- if you want to use this  
4 example.

5 But overwhelmingly other places you do see  
6 that it would be considered grounded and that would  
7 be considered a requirement of what they want to  
8 define as cascode. But this is sort of on the edge  
9 because definitions sometimes are used in different  
10 context in different ways when it comes to  
11 transistors.

12 BY MR. BALICH:

13 Q. Okay. So on that page 38 of your  
14 declaration you show figure 2(a) from Tessman; is  
15 that right?

16 A. Yes.

17 Q. And Tessman figure 2(a) shows two FETs  
18 that are connected in the series; is that right?

19 A. Yes, it does.

20 Q. The source of the FET on the left is  
21 connected to the ground, correct?

22 A. Yes.

1 Q. And the drain of the FET on the left is  
2 connected to the source of the FET on the right,  
3 correct?

4 A. That's correct.

5 Q. And so conduction of the FET on the left  
6 is controlled by the voltage at terminal 1G (sic),  
7 correct?

8 A. It says G1, but --

9 Q. Okay. G1 -- sorry.

10 MR. MACDONALD: I don't mean to interrupt,  
11 but the real time is frozen. Do we want to go off  
12 the record?

13 MR. BALICH: Let's go off the record.

14 (A break was taken.)

15 BY MR. BALICH:

16 Q. Dr. Bernstein, welcome back from our break  
17 to resolve some technical issues.

18 I see that you've got page 38 of your  
19 declaration open, correct? And I wanted to ask you  
20 some more questions about Tessman figure 2(a) which  
21 you've reproduced on that page.

22 So the drain of the FET on the left is

1 connected to the source of the FET on the right; is  
2 that right? Is that correct?

3 A. The drain on the FET on the left, yep, is  
4 connected to the source of the device on the right.  
5 That is correct.

6 Q. Yep. All right. And so then conduction  
7 of the FET on the left is controlled by the voltage  
8 at terminal G1, correct?

9 A. Well, to be technically correct, it  
10 depends on the circuit that it's in to say that --  
11 what the voltage is at the drain. Of course, if the  
12 drain is at zero voltage, nothing will conduct. So  
13 it's -- it also depends on the circuit that it's in.

14 Q. Sure. So I guess based on the circuit  
15 that Tessman discloses, how does Tessman intend to  
16 enable or disable conduction at the FET on the left?

17 A. Well, this is a transistor, and every  
18 POSITA knows how to use transistors in various  
19 circuits to perform various functions; for instance,  
20 if it's going to be an amplifier or if it's going to  
21 be a mixer.

22 So, generally, if you were to have, let's

1 say, a resistor connected to the drain which would be  
2 connected to a voltage source, and if there's going  
3 to be some threshold voltage or a subthreshold  
4 current, the current that flows is going to be --  
5 we'll call it the Kirchhoff current law, which is a  
6 continuous current -- the current flow all depends on  
7 the circuit that it's connected to.

8           So it's a transistor. So assuming that  
9 the second transistor is conducting, that is to say  
10 it is biased such that it is in a conducting mode,  
11 then the current in the first transistor will be the  
12 same as the current in the second, which will always  
13 be the case because, as I said, Kirchhoff's current  
14 law, KCL, tells you that the current in any series  
15 connection is going to be the same in all the parts  
16 of that series.

17       Q.     And so then how does Tessman control  
18 whether the FET on the left is conducting or not?

19       A.     Well, again, it's a transistor. The  
20 voltage between the gate and the source is what  
21 determines based on the threshold voltage of that  
22 transistor if it is, we'll say, in a conducting mode.

1 It doesn't necessarily mean it is conducting unless  
2 there's current, obviously.

3 Q. Right. So then Tessman connects the  
4 source of the FET on the left to ground, right?

5 A. That's correct.

6 Q. And so then how would the FET on the left  
7 be controlled to be in either a conducting mode or  
8 not a conducting mode?

9 A. Well, this all depends in our definition  
10 of insulating gate transistors.

11 As I said, the source can be -- yeah, the  
12 source -- or excuse me again. Right. The source can  
13 be the ground -- I'm reading my document -- and the  
14 input to the second gate can also be grounded, as we  
15 said of Tessman.

16 But in general, cascode is comprising a  
17 first enhancement mode gate which would be the case,  
18 meaning it has a positive threshold voltage, which  
19 means if the gate voltage is below the threshold  
20 voltage it is generally not conducting. And when the  
21 gate voltage is above the threshold it will be in a  
22 conducting mode.

1           And I called it -- it's called an  
2 enhancement mode transistor, but it's not limited to  
3 being in an enhancement mode transistor. But Tessman  
4 -- I don't recall the exact source, if his is defined  
5 as enhancement or conducting.

6           But any FET can be enhancement mode, which  
7 means it's off when the voltage is below the  
8 threshold. And the second in -- I described it as a  
9 depletion mode, which means it is normally in a  
10 conducting state, that is to say it has a channel  
11 available for conductivity and -- which would mean  
12 that when the voltage is below -- when the threshold  
13 voltage -- excuse me.

14           When the gate voltage is at zero it is  
15 conducting. Enhancement mode means at zero voltage  
16 it's not conducting. Enhancement mode means by  
17 definition you enhance to make it channel, so you  
18 have to put a voltage at the gate to source. It has  
19 to be above a threshold voltage.

20           And a depletion mode you -- it is  
21 conducting with zero volts at the gate. So it will  
22 be in a conducting mode at zero volts, but to turn it

1 off you would have to go below the threshold voltage,  
2 assuming it's an N-type.

3 It would be opposite for P-types, but in  
4 our case most -- all of our gallium nitride and  
5 gallium arsenide, all the wide band gaps --

6 (Whereupon, Madam Reporter asked for  
7 clarification from the witness.)

8 A. The gallium nitride and gallium arsenide  
9 devices require that the voltage be below threshold  
10 voltage in order to stop conducting or above the  
11 threshold voltage to start conducting.

12 That's because they're N-type devices, but  
13 you can have P-type devices. It's a long lesson.  
14 So, anyway, I hope I answered your question in there.

15 MR. MACDONALD: Dr. Bernstein, just to  
16 clarify, during the deposition today the court  
17 reporter will interject for a spelling and, you know,  
18 when she doesn't hear a word, but you're answering  
19 the questions from counsel and not any questions from  
20 her.

21 THE WITNESS: Okay.

22 BY MR. BALICH:

1 Q. So just so I perhaps can distill that  
2 down, so Tessman can control the FET on the left  
3 through controlling the voltage at G1; is that right?

4 A. Relative to ground, yes.

5 Q. Relative to ground. Thank you. And  
6 Tessman controls whether the FET on the right is  
7 conducting by controlling the voltage at G2 relative  
8 to the voltage at the drain -- strike that.

9 I said that wrong. Tessman controls  
10 whether the FET on the right is conducting by  
11 controlling the voltage at G2 relative to the source  
12 of the FET on the right, correct?

13 A. It is correct to say the -- we refer to  
14 the threshold as being the gate of the volt -- excuse  
15 me -- the voltage from the gate to source is how we  
16 generally refer to a threshold voltage.

17 Q. Right. So Tessman controls whether the  
18 FET on the right is conducting by controlling the  
19 voltage at G2 relative to the source; is that  
20 correct?

21 A. That is correct.

22 Q. Okay. And the gate of the FET on the

1 right is capacitively coupled to ground, correct?

2 A. That's what that C stands for, yes.

3 Q. Okay. So the FET on the right is not  
4 conductively coupled to ground, correct?

5 A. Right. It is capacitively coupled to  
6 ground and the G2 node is -- right, is accessible.

7 Q. Okay. If you could open Exhibit 1019 to  
8 Green?

9 A. Green?

10 Q. 1019.

11 A. I have Mishra.

12 Q. And if you don't have that --

13 A. Oh, 1019?

14 Q. Correct. If it's not in there, I  
15 definitely have it on the iPad. It's on the iPad if  
16 that would be more convenient?

17 A. Okay. 1019?

18 Q. Do you see 1019 on the list?

19 A. Okay. Yes.

20 Q. Okay. And just by way of explanation, so  
21 we're using the electronic exhibit and you can scroll  
22 -- I believe you can make that bigger because that

1 looks tiny. And the way that you can make it bigger  
2 is there's a plus and a minus button, zoom in, zoom  
3 out at the top left.

4 A. Oh, here.

5 MR. MACDONALD: Is this Exhibit 1019? We  
6 have a paper copy. That's tiny on that screen.

7 A. Green, okay.

8 BY MR. BALICH:

9 Q. So Exhibit 1019 is an article authored by  
10 Bruce Green; is that right?

11 A. That's what it says, Bruce M. Green.

12 Q. Okay. So if I refer to this document as  
13 Green, will you understand that I'm referring to  
14 Exhibit 1019?

15 A. Yes, I'll understand that.

16 Q. So if you could turn to page 2 of Green  
17 and look at figure 2(a). Let me know when you're  
18 there,

19 A. Okay. Yes, I'm here.

20 Q. Figure 2(a) of Green shows the same  
21 circuit as figure 2(a) of Tessman; is that right?

22 MR. MACDONALD: Objection. Form.

1           A.     It's generally the same. He indicates  
2 here a resistor between, which is probably  
3 technically more accurate because there's always some  
4 resistance in wires. So the VG -- he calls it VG1  
5 and VG2. So it looks very similar to Tessman.

6                     BY MR. BALICH:

7           Q.     Okay. And so figure 2(a) of Green shows  
8 the gate of the FET on the right is capacitively  
9 coupled to ground, correct?

10          A.     Yes. That is correct.

11          Q.     And the gate of the FET on the right is  
12 not conductively connected to ground, correct?

13          A.     The way it is written, yes. It's just the  
14 capacitor.

15          Q.     Okay. So figure 2(a) of Green just by  
16 looking at the figure doesn't show connecting  
17 terminal G2 to a constant voltage source, correct?

18          A.     We don't know what it's connected to.  
19 It's just the transistor.

20          Q.     Right. Okay. If you could turn to page 4  
21 of Green and take a look at figure 6(a).

22          A.     6(a), yes.

1 Q. Okay. Figure 6(a) of Green shows a FET on  
2 the top left where the gate is capacitively coupled  
3 to ground; is that right?

4 A. Well, you're in a circuit. So there's --  
5 capacitance is connecting everything to -- it's a  
6 mimic. It is a -- there's always -- right, there's  
7 always some capacitance on every wire. So he's  
8 describing the capacitance. There is a capacitance  
9 connected to ground through a capacitor.

10 Q. And figure 6(a) of Green does not show  
11 that the gate of the FET on the top left is  
12 conductively coupled to ground; is that right?

13 A. That is correct. VG2 is whatever VG2 is.

14 Q. Okay. Figure 6(a) of Green does not show  
15 connecting the terminal G2 to a constant voltage  
16 source; is that right?

17 A. It doesn't show what it's connected to.

18 Q. Okay. If you could open Exhibit 1018.  
19 That's Sankin. It might be the one right before  
20 Green.

21 A. Oh, right here, yes.

22 Q. So Exhibit 1018 is patent publication

1 number US 2006/0113593.

2 Did I read that correctly?

3 A. I wasn't paying attention to your reading  
4 the number, but I'll assume you did.

5 Q. Okay. The first named inventor is Igor  
6 Sankin; is that correct?

7 A. Yes.

8 Q. So if I refer to this document as Sankin,  
9 will you understand that I'm referring to Exhibit  
10 1018?

11 A. That's reasonable.

12 Q. Okay. If you could take a look at Figure  
13 1 of Sankin, that shows 2 JFETs next to each other;  
14 is that right?

15 A. That is right, yes.

16 Q. And the JFET on the left is an E-mode  
17 JFET; is that correct?

18 A. That's correct.

19 Q. E-mode refers to enhancement mode,  
20 correct?

21 A. That's probably what it does.

22 Q. And enhancement mode transistors are

1 normally off; is that right?

2 A. That's what I said, yes.

3 Q. Okay. And the JFET on the right is a  
4 D-mode JFET, correct?

5 A. Correct.

6 Q. A D-mode refers to depletion mode, right?

7 A. That is correct.

8 Q. And depletion mode transistors are  
9 normally off; is that right?

10 A. That's what it means here.

11 Q. So, again, looking at Figure 1 of Sankin,  
12 reference Number 6 refers to the source; is that  
13 right?

14 A. Number 6?

15 Q. So do you see the numbers?

16 A. Are you referring to the number here? 6  
17 looks like a gate, doesn't it?

18 Q. So let's take a look at a different part  
19 of Sankin. If you could flip to paragraph 147, and  
20 let me know when you're there.

21 A. 147.

22 Q. Okay. And in the middle, roughly middle

1 of paragraph 147, Sankin states, "As shown in Figure  
2 1, the devices comprise drain (3), drift" --

3 A. Just a minute. I'm not there yet. Oh,  
4 where you're reading again -- I can just read it to  
5 myself.

6 Q. Go ahead. Read it to yourself and let me  
7 know when you're ready.

8 A. Okay. Where you're saying, "As shown in  
9 Figure 1, the devices comprise drain (3), drift (4),  
10 channel (5), and source (6) epitaxially grown n-type  
11 layers, and P-type implanted gate regions (7)."

12 Q. So if we go back to Figure 1 with that in  
13 mind, so reference Number 6 refers to the source; is  
14 that right?

15 A. He refers to 6 as the source.

16 Q. And reference Number 7 refers to the two  
17 gate regions; is that right?

18 A. That's what it says, yes.

19 Q. And reference Number 3 refers to the  
20 drain; is that correct?

21 A. Drain 3, yes.

22 Q. Okay. And then there's a bunch of boxes

1 with diagonal shading. Do you see those boxes?

2 A. Yes.

3 Q. Those are all contacts; is that right?

4 A. That's what it probably represents, yes.

5 Q. So in Figure 1 of the drain of the E-mode  
6 JFET is connected to the source of the D-mode JFET by  
7 wires, right?

8 A. The drain is the bottom. We have wires  
9 connecting the -- yes, wires connecting the drain of  
10 the E-mode through the wires to the source of the  
11 D-mode.

12 Q. And so Figure 1 of Sankin does not show a  
13 drain region of the enhancement mode transistor  
14 merged with a source region of the depletion mode  
15 transistor, right?

16 A. Let me look at it straight here. What are  
17 you asking me again?

18 Q. Sure. Figure 1 of Sankin does not show a  
19 drain region of the enhancement mode transistor  
20 merged with a source region of the depletion mode  
21 transistor; is that correct?

22 A. E-mode is enhancement mode, which means it

1 is normally off, and the drain of that is connected  
2 to the source with wires to the D-mode, which at zero  
3 voltage we said is normally conducting. Okay.  
4 That's correct.

5 Q. So my question was specifically: There's  
6 no depiction of the drain region of the enhancement  
7 mode transistor that merged with the source region  
8 depletion mode transistor, correct?

9 A. It's depicted here as connections probably  
10 with wires or metal.

11 Q. Okay. And Figure 1 of Sankin shows the  
12 source of the E-mode JFET connected to ground,  
13 correct?

14 A. The source of the E-mode is connected to  
15 ground, yes. It has a nice picture on figure 3 if  
16 it's the same.

17 Q. And figure 1 of Sankin shows the gate of  
18 the E-mode JFET is connected to a signal, correct?

19 A. Well, whatever voltage VGS is. So if it's  
20 a signal or a voltage, it's -- whatever voltage VGS  
21 is, depending on the circuit that it's in.

22 Q. Okay. And that's the VIN, correct?

1           A.     Yes. VIN on the Figure 1, yes.

2           Q.     Figure 1 of Sankin shows that the gate of  
3 the E-mode JFET -- strike that.

4                   Figure 1 of Sankin shows that the gate of  
5 the D-mode JFET on the right is not connected to a  
6 constant voltage source, correct?

7           A.     The gate of the D-mode, which is 7 at  
8 gate?

9           Q.     Correct.

10          A.     7 is connected to 8, which is 3, which is  
11 the drain. So it looks like we have the gate of the  
12 D-mode device connected to what is the drain portion  
13 of the E-mode device. Okay.

14          Q.     So, for instance, the gate of the D-mode  
15 device is not connected to ground, correct?

16          A.     Right. It is depicted here that it's  
17 connected to the drain, which is interesting.

18          Q.     And then if you could scroll down and take  
19 a look at figure 2 of Sankin, in figure 2 of Sankin  
20 the drain of the E-mode JFET is connected to the  
21 source of the D-mode JFET by wires; is that right?

22          A.     That is correct.

1 Q. Okay. Let's go back to your declaration  
2 at Exhibit 1003, and if you could turn to page 43.

3 A. Yes.

4 Q. And on page 43 is paragraph 66 or at least  
5 the start of paragraph 66; is that right?

6 A. Yes.

7 Q. And you mention a software called LTspice;  
8 is that right?

9 A. That is right.

10 Q. And on the bottom of the page you  
11 reference a specific version 17.2.4, correct?

12 A. That is correct.

13 Q. Do you know when that version was  
14 released?

15 A. Oh, version 17, that's probably -- I  
16 update my LTspice regularly. So it's probably pretty  
17 recent.

18 Q. Okay. So, for instance, version 17 was  
19 not available in 2006, right?

20 A. That's correct. Probably. I don't know  
21 when 17 came out.

22 Q. Okay. Now, if you turn to page 44, so the

1 next page, you state that you used a particular model  
2 for Q1; is that right?

3 A. That's right.

4 Q. what model is that?

5 A. well, I -- model -- spice has a library of  
6 commercially available devices, and I wanted to make  
7 a simulation of -- we made a simulation just so we  
8 could demonstrate the way a D-mode and an E-mode  
9 device would work in a cascode operation.

10 So this was only to just show what we  
11 already knew is the -- you know, the way devices  
12 work.

13 Any POSITA would know if you put a --  
14 (Whereupon, Madam Reporter asked for  
15 clarification from the witness.)

16 A. However you say that, POSITA, POSA,  
17 however you want to -- whatever language -- person  
18 of skill of ordinary art (sic).

19 So I chose standard MOS devices. For  
20 instance, NDC7002N, which has a VDMOS, as it says.  
21 And those are the parameters from the LTspice model  
22 that go into the model.

1           Each of these letters mean something. Rg  
2 is gate resistance. And then it says Vto, which is  
3 the turn on voltage, is 2.2 volts. And I put that in  
4 black so we know that we have -- it indicates that  
5 it's an enhancement mode device.

6           And then R is drain resistance, Rd source  
7 resistance, and Rb is the typical resistance. So  
8 that was the main issue. I wanted to find a device  
9 that had something like a matched pair where you had  
10 Rb is one for the lower device.

11           And similarly, for the Q2 I used another  
12 JFET, the 2N3819 NJF, and there it had a threshold  
13 voltage of minus 3.

14           So I was just doing a simulation to show  
15 how a standard enhancement mode/depletion mode device  
16 would work in a -- in normal operation in a standard  
17 circuit in a very common circuit.

18           So I made my own circuit with a resistor  
19 of 10,000 ohms and a voltage source --

20           (Whereupon, Madam Reporter asked for  
21 clarification from the witness.)

22           A.     Made my own circuit with a 10,000 ohm

1 resistor and a 15-volt supply, but the key -- the two  
2 key things are the Vto was 2.2 volts and the  
3 depletion mode has a threshold voltage of minus 3  
4 volts and the Rs is 1 ohm.

5 BY MR. BALICH:

6 Q. Thanks. That saved me a few questions.

7 A. Okay.

8 Q. what type of transistor does the NDC7002N  
9 describe?

10 A. well, it says VDMOS, which means a  
11 vertical DMOS. So it's a fairly standard power  
12 transistor which has low resistance of one when it's  
13 on. And it's, I'll say, something in my mind typical  
14 -- has parameters that are very typical. I use that  
15 transistor model for most of my circuit work, just a  
16 very nice generic MOSFET.

17 Q. Does that model simulate a type 3 nitride  
18 device?

19 A. No. I said these are both silicon  
20 devices. It's just to show what does a cascode do  
21 when you have a depletion mode and an enhancement  
22 mode together.

1           Q.     So just for the record, the model you used  
2 for Q2, N -- sorry -- 2N3819 also simulates a silicon  
3 device; is that right?

4           A.     Yes. These are standard spice model and  
5 have probably been around for many years. Old, old  
6 devices.

7           Q.     And did your simulation simulate these two  
8 transistors connected by wires?

9           A.     This -- what I have here is the whole  
10 simulation. So other than the Rd for the drain  
11 resistance, there's no extra parasitic devices. I  
12 didn't include any extra resistors.

13                   So I just took the sample models and  
14 connected them together, which means the simulation  
15 would assume that this drain of the M2 is connected  
16 to the source of the J1.

17           Q.     Okay. But the simulation didn't  
18 specifically attempt to simulate a single transistor  
19 with an E-mode gate merged with a D-mode gate?

20           A.     It was just the circuit simulation. So it  
21 doesn't distinguish about merged or not merged.

22           Q.     Okay. Now, you didn't try to simulate a

1 single transistor with the two gates as part of the  
2 same transistor; is that right?

3 A. well, I made a very simple simulation in  
4 spice. If you were to use a more complicated -- if I  
5 wanted to simulate the device, spice is a circuit  
6 simulator, not a device simulator.

7 Q. Okay. In your own personal experience  
8 have you ever used a GaN dual-gate cascode  
9 transistor?

10 A. A GaN dual-gate cascode transistor? I use  
11 lots of GaN transistors. I don't know that I've ever  
12 used one where there's a specifically extra pin. But  
13 I think most GaN transistors will have field plates,  
14 but I -- and they just are what they are. There's  
15 usually three terminals.

16 There's the source and sometimes on the  
17 devices there's -- it's -- there's a fourth pin to  
18 the substrate, but generally there's no -- I don't --  
19 I don't have any experience with a single device  
20 having two gates where I can connect the two gates.

21 Q. what about a device that has two gates but  
22 where the gate of the depletion mode gate is

1 connected to the source of the enhancement mode gate?

2 A. Right. Well, I know that Infineon has a  
3 principle where they have said that -- I put it in my  
4 report where there's a theory of a floating -- of a  
5 field plate which would be source connected.

6 There is a theory that I worked on and I  
7 put that in my document where that could be  
8 considered a gate. And I know that we do have Ren,  
9 which I referred to, who can tell you you can make a  
10 gate by knowing the -- insulating -- you can make an  
11 insulated gate.

12 But in all the transistors I've used  
13 they're all automatically connected and I have no way  
14 of disconnecting it from the source.

15 Q. So apart from Infineon's theory of the  
16 case, based on your own personal experience and  
17 knowledge, do you know if you've ever worked with a  
18 GaN transistor that had an enhancement mode gate and  
19 a depletion mode gate where the depletion mode gate  
20 was connected to the source terminal of the  
21 transistor?

22 A. Until this case I never considered the

1 field plate which has to be there because whenever  
2 you want to go to voltages above, you know, even 100  
3 volts or even less sometimes, any power transistor,  
4 even silicon when I worked on my master's in the  
5 '80s, would have field plates.

6           And the field plates are there because you  
7 don't want to ruin the gate and you want to maintain  
8 nice property. So all the GaN devices I have used  
9 have within them except -- you know, when you have  
10 just three terminals you don't ever consider that as  
11 a -- until this case I never considered them as a  
12 field plate until I saw this theory.

13           However, you can make -- as I said, Ren  
14 teaches us very nicely. If I make my oxide thin  
15 enough so there's good capacitive coupling into the  
16 gate, I can, if I wanted to make a device,  
17 intentionally make a depletion mode, which is what I  
18 use -- you know, I -- as long as we're back here,  
19 this is how I describe Mishra, which is the  
20 capacitively coupled Mishra figure 5 I hold as that  
21 device.

22           But I would never consider that as a

1 device, only if you need to. I would never consider  
2 that as a gate. I would have considered it only as a  
3 field plate. That's the way I would normally use  
4 that in my lab.

5 Q. Got it. And what page on your report are  
6 you referring to?

7 A. Now I'm on page 162.

8 Q. 162, okay. So have you ever used the  
9 device that had the similar principles as the  
10 modified Mishra figure 5 that you have on page 162?

11 A. I have used devices similar to the  
12 Innoscience device -- they're very common -- but I  
13 never used one as a cascode. That was not ever my  
14 intention. I used it only as a single transistor,  
15 and I never considered the gate as -- the field plate  
16 as a gate. A field plate is just there to protect  
17 the first device. So I, in my experience, never  
18 considered that as a second gate.

19 Q. Okay.

20 MR. BALICH: I'm going to switch topics.  
21 I don't know if you need to take a break; would like  
22 to take a break.

1 MADAM REPORTER: I'd like a break.

2 MR. BALICH: Okay. Let's go off the  
3 record.

4 (A break was taken.)

5 BY MR. BALICH:

6 Q. welcome back, Dr. Bernstein, from the  
7 break, if you could turn to page 61 of your  
8 declaration. And this is the start of the section  
9 Ground 1: Bonn and Mizuta; is that correct?

10 A. That's what it is.

11 Q. And if you turn the page to page 62,  
12 you've reproduced with some annotations Figure 1 of  
13 Bonn; is that right?

14 A. That is right.

15 Q. what type of device is depicted by the  
16 circuit diagram of Figure 1?

17 A. well, this is the device that Bonn  
18 teaches, and as you see from figure 7 next door  
19 that's the device.

20 Q. what does Figure 1 do? Yeah. what's the  
21 purpose of Figure 1?

22 A. well, Figure 1 as a circuit -- see now we

1 have a whole circuit we can talk about.

2 This circuit is a mixer circuit where we  
3 have a mixer enable that enables this mixer device,  
4 which as depicted here could be -- and he described  
5 it as being two devices, but his invention allows  
6 this to be in one device with a smaller area.

7 And you can see the biasing,  
8 B-I-A-S-I-N-G, resistors. And it's described well in  
9 his patent 46 and 48 for the upper transistor and 28  
10 and 32 for the lower transistor.

11 It's capacitively coupled to the ground,  
12 you see, because there's an oscillator circuit from  
13 what he defines as a low-noise amplifier 20. So it  
14 mixes the RF signal with the local oscillator LO in a  
15 way that you can get an IF at the output.

16 Q. And Bonn describes this as a  
17 down-converter; is that right?

18 A. Yes.

19 Q. And, generally speaking, what would a  
20 POSITA understand a down-converter to do?

21 A. It's actually very interesting because  
22 Bonn's invention really is a semiconductor

1 transistor. If you actually look at the -- the name  
2 of the invention, I think it's -- if you look at  
3 Bonn, he says that it's a field-effect transistor.

4 And nowhere in his abstract does he  
5 describe anything but a field-effect transistor which  
6 can serve as a low-noise amplifier. And then he  
7 gives this figure and spends a lot of time describing  
8 a down-converter.

9 So I think the simple answer is that he  
10 understood that for the low-noise amplifier -- it  
11 says right at the beginning, a down-converto  
12 typically includes a low-noise amplifier, an image  
13 filter, and a mixer circuit.

14 And I think it's not normal in the state  
15 in the art depending on if you're in an RF -- if  
16 you're an RF engineer. I generally am not so  
17 familiar with down-converters, so I think that's why  
18 he spends a lot of time explaining it so that a  
19 POSITA would understand that this is a very sort of  
20 special application. Whereas, the normal application  
21 would be an amplifier.

22 So he doesn't -- the reason I believe -- I

1 don't know what Dr. Bonn or Mr. Bonn was thinking,  
2 but it seems the reason he spends a lot of time  
3 explaining this RF application is because it's not a  
4 usual application.

5           So this circuit is a very complicated  
6 circuit and it's not clear -- since it's not  
7 connected to ground, I don't know who --

8           (Whereupon, Madam Reporter asked for  
9 clarification from the witness.)

10       A.     The source is not connected to the ground.  
11 So it is not an amplifier, but he describes this as a  
12 cascode configuration of two transistors and many  
13 other things in my report.

14           BY MR. BALICH:

15       Q.     Sure. While we have Bonn open, let me ask  
16 you a few questions about that. So you currently  
17 have Exhibit 1006 open; is that correct?

18       A.     That is correct.

19       Q.     And Exhibit 1006 -- I'm going to read off  
20 the patent number if you want to look at that -- is  
21 patent Number 6,160,280; is that right?

22       A.     That is right.

1 Q. And the first named inventor is Fred Bonn?

2 A. That is correct.

3 Q. And so if I refer to this document as  
4 Bonn, you're going to understand that I'm referring  
5 to Exhibit 1006; is that right?

6 A. That is right.

7 Q. If you could turn to column 1 of Bonn,  
8 starting at line 8, Bonn states that,  
9 "Down-converters are used in radio applications to  
10 convert a signal of one frequency to a signal of  
11 another frequency."

12 Did I read that correctly?

13 A. You read that correctly.

14 Q. Okay. Would you agree with Bonn's  
15 description of a down-converter as converting a  
16 signal of one frequency to a signal of another  
17 frequency?

18 A. As I said, I'm not an RF circuit expert,  
19 so I have very little experience with down-converters  
20 and mixers, to be honest. So I could rely on Bonn to  
21 assume that he is teaching us correctly the  
22 application of a down-converter.

1 Q. Got it. And in that same paragraph of  
2 Bonn, Bonn -- starting at line 14 Bonn states, "The  
3 mixing process provides a mixed signal, which has a  
4 spectrum comprised of the sum and difference of the  
5 frequencies of the RF and LO signals."

6 Did I read that correctly?

7 A. You did read that correctly.

8 Q. Okay. So as part of Bonn's down-converter  
9 he has a mixer, correct?

10 A. Yes.

11 Q. And it's the mixer that mixes the RF and  
12 the LO frequencies, correct?

13 A. That is correct.

14 Q. And the output of that is the intermediate  
15 frequency or the IF; is that right?

16 A. Again, the circuit that Bonn drew is --  
17 the problem that he's trying to solve is the  
18 down-converter, which is why I immediately in my -- I  
19 am not analyzing that device at all as a  
20 down-converter because that's not the application.

21 I believe -- really, I think that's not  
22 even his primary application. I think the secondary

1 application, that needs explanation.

2 I simplified it to what any POSITA would  
3 do to understand how to use a cascode device in a  
4 simple amplifier application. He obviously didn't  
5 have to explain it because any POSITA knows this.

6 He does have to explain the down-converter  
7 because I think a simple POSITA would not know how to  
8 use it in this application, but my analysis was not  
9 at all based on the converter application.

10 Q. Got it. But I do have some more questions  
11 about Figure 1 of Bonn, and you can either take a  
12 look at that figure in Bonn or in your report, either  
13 one.

14 In Figure 1 of Bonn what is depicted by  
15 reference Number 20?

16 A. That is -- I believe he calls that the  
17 low-noise amplifier.

18 Q. And what's the purpose of a low-noise  
19 amplifier?

20 A. To amplify a signal with low noise.

21 Q. So trying not to use the word "amplified"  
22 in the definition that one is trying to define, would

1 you agree that an amplifier takes an input signal of  
2 a particular frequency and produces a signal of a  
3 higher power output of the same frequency?

4 A. well, it all depends on what kind of  
5 amplifier. I think in his application his could have  
6 been even a unity gain amplifier. I don't know that  
7 there's an amplification, but that doesn't mean it's  
8 not an amplifier.

9 An amplifier can have gain of greater than  
10 one or even less than one. So the gain of the  
11 amplifier all depends on the rest of the circuitry,  
12 but it is connected to the ground on the bottom. So  
13 it's a source connected.

14 I don't know if the 22 is a -- is a  
15 parasitic conductor, but probably. And if it's not,  
16 then it could be a low-gain low-noise amplifier if  
17 you have inductors so that the source would not be  
18 constant.

19 Generally, loads on the source will reduce  
20 the gain. So we don't know anything about the gain  
21 of this transistor.

22 Q. But, generally speaking, what is an

1 amplifier without using the word "amplifier" or  
2 "amplification"?

3 A. well, an amplifier is the generic use of a  
4 -- basically, a transistor is used as an amplifier,  
5 but an amplifier has many, many functions and  
6 transistors have many functions.

7 You can make a source follower amplifier  
8 which you would put a resistor intentionally to make  
9 the gain low so that you can mix signals. You can  
10 make a signal transistor into a mixer, a standard  
11 two-input or comparator. There are many, many uses  
12 for this transistor.

13 And if you notice on all the other patents  
14 we have, even on Herman himself, there's no circuits  
15 because it's obvious to any POSITA how you would use  
16 it.

17 The first semester electrical engineering  
18 student knows how to take a transistor and make an  
19 amplifier, how to make a high-gain amplifier, a  
20 low-gain amplifier, to make a mixer.

21 You know, we teach our students -- and I  
22 remember learning, you know, the first laboratory is

1 how to connect a transistor to make it work.

2 Again, generally the high gain one has the  
3 source grounded, which is what I -- which is how I  
4 depicted it. Of course, these transistors can be  
5 used in any way, and a POSITA would have obviously  
6 been able to take that transistor and use it how he  
7 wants.

8 In fact, it's not clear what the gain is  
9 because we have inductor as the load, which is very  
10 interesting, which is more or less how we would use  
11 it in a power device application.

12 For instance, the Infineon or the  
13 Innoscence product would be used more or less in  
14 exactly this configuration, and you would have a  
15 diode at the output unless you want to have the AC.

16 So if it's an RF AC amplifier or it could  
17 be a switch; it could be a mixer. I don't think that  
18 these patents can have any need to describe other  
19 uses.

20 Q. So for an amplifier is the frequency of  
21 the input the same as the frequency of the output?

22 MR. MACDONALD: Objection. Form.

1           A.     If you're making an RF amplifier, say  
2 class A -- they call it a class A amplifier -- you  
3 can configure the device. It's not necessarily --  
4 I'm not so sure here if it's figured to be a gain --  
5 how much gain is in this amplifier.

6                     But the gain is always the output power,  
7 let's say, versus the input power. So you'd put a  
8 small RF signal on the input and the transistor  
9 causes much higher voltage, which would then give  
10 more power on the output if you're going to configure  
11 it as a high-gain amplifier.

12                    It says low noise, so it's not clear that  
13 you're going to want necessarily high gain.  
14 Sometimes it's a trade-off of noise and gain.  
15 Usually, that's a trade-off with noise and gain. So  
16 usually that's a trade-off. That's, again,  
17 second-year electrical engineering students.

18                    BY MR. BALICH:

19           Q.     Got it. And other than changing the gain  
20 of the signal, does an amplifier change the frequency  
21 of the signal?

22           A.     A simple transistor, as in this

1 configuration and in my Figure 1, there is no change  
2 in the frequency.

3           You'd have to -- that's where the mixer  
4 comes in. That's why he had to explain this very,  
5 I'll say, more complicated circuit. That's why he  
6 explained with a lot of words and a figure.

7           It's very interesting because you almost  
8 never see a circuit diagram on a device patent. So  
9 there's something very interesting in Bonn, and he's  
10 teaching something in a particular application.

11           But he says -- because nowhere in his  
12 abstract does he even mention the word down-converter  
13 -- it's very interesting -- although in his  
14 background he talks about it.

15           And the claims themselves are all on the  
16 device itself. So it's interesting that he spends --  
17 he felt this was a very important innovation for the  
18 down-converter, but it looks like he's making a  
19 typical amplifier, just a simple amplifier.

20       Q.     Okay. And specifically for amplifier 20  
21 in Figure 1 its purpose is to change the gain of the  
22 RF signal without changing its frequency; is that

1 right?

2 MR. MACDONALD: Objection. Form.

3 A. You said gain. No. It would give gain --  
4 if you configured this -- I don't know what the gain  
5 is because we have resistors and we have inductors.  
6 So in this circuit you can have a gain of 1.

7 You can make a low-noise filter. In fact,  
8 you can use a transistor to filter so you get lower  
9 noise. So he calls it a low-noise amplifier. It  
10 doesn't necessarily mean it has much gain. It's just  
11 an amplifier.

12 BY MR. BALICH:

13 Q. Right. And I'm trying to understand the  
14 purpose of the low-noise amplifier 20 in Figure 1.

15 MR. MACDONALD: Objection. Form.

16 A. Okay. Let's see where he describes it  
17 because I did not analyze his circuit to any great  
18 extent.

19 why he puts that there, that's -- I -- I  
20 -- I cut it out from my modification because I'm now  
21 making the -- what he called the mixer 40 into the  
22 high-gate amplifier which he himself says -- Bonn

1 says very clearly it can be used as a high-gain  
2 amplifier or a high-frequency amplifier.

3 BY MR. BALICH:

4 Q. Okay. Take a look at --

5 MR. MACDONALD: I'm sorry, Jason. Please  
6 allow the witness to finish answering.

7 MR. BALICH: Sure.

8 MR. MACDONALD: Go ahead, Dr. Bernstein.  
9 I don't think you were finished.

10 A. I was saying Bonn tells us -- he says over  
11 here, "The dual-gate FET structure of the present  
12 invention can be tailored to provide superior  
13 performance over the prior art dual-gate FET  
14 structure in high frequency signal mixing, as well as  
15 other applications such as high frequency signal  
16 amplification."

17 And as I said in his abstract, Bonn tells  
18 us that a field-effect transistor structure can serve  
19 as a low-noise amplifier.

20 Now, in his Figure 1, he has what he  
21 describes as an amplifier. It looks like it is not  
22 his invention as an amplifier, but in principle he

1 could have, which would look an awful lot like my  
2 depiction over here.

3 But I don't think he needs to because any  
4 POSITA would understand right away the simplest, most  
5 normal application for a transistor is an amplifier.  
6 Transistors have many functions. They can be mixers,  
7 as I said. They can be -- they can be -- what did I  
8 call it? -- well, they could be filters.

9 Transistors have many, many functions, and  
10 a POSITA would know in his particular application  
11 what to use it for.

12 And that's my depiction and the way I  
13 understood this device. And he says itself -- he  
14 tells you to use it as a high-frequency amplifier,  
15 which any POSITA would know, and that's exactly the  
16 -- that is the device that I analyzed.

17 BY MR. BALICH:

18 Q. Okay. If you could turn to column 2 of  
19 Bonn starting at about line 8, the paragraph starts,  
20 "Figure 1 is the schematic diagram of the  
21 down-converter 10."

22 Do you see that?

1           A.     I see that.

2           Q.     And if you look a few lines down to line  
3 -- about 13, there's another sentence,  
4 "Down-converter 10 includes field-effect transistor  
5 (FET) 20 which serves as a low-noise amplifier (LNA)  
6 for amplifying the RF signal."

7                     Did I read that correctly?

8           A.     You read that correctly.

9           Q.     So Bonn's FET 20 amplifies the RF signal;  
10 is that correct?

11          A.     It says it's amplifying, but it's also a  
12 low-noise amplifier. So there's filtering involved  
13 as well. It's a filtered amplifier.

14                     But we don't know anything about, you  
15 know, as I say -- generally when we're referring to  
16 amplifiers, we refer to property such as gain,  
17 bandwidth, et cetera, et cetera. And he's not  
18 telling us any details of what this amplifier is.

19                     Again, he's assuming when it comes to the  
20 amplifier a POSITA knows how to make an amplifier.

21          Q.     Right. So a low-noise amplifier is a  
22 known thing that a POSITA would have known what that

1 is?

2 A. A POSITA knows what is a low-noise  
3 amplifier and he would know how to wire it up, yes.

4 Q. Okay. Taking a look at Figure 1 of Bonn  
5 again, amplifier 20 has one gate; is that correct?

6 A. It is depicted here as having only one  
7 gate.

8 Q. And the single gate that is depicted of  
9 amplifier 20 is connected to the RF signal; is that  
10 right?

11 MR. MACDONALD: Objection. Form.

12 A. Yes. The RF signal goes in through a  
13 filter. As I -- again, I'd like to take my  
14 depiction. I believe he could have substituted his  
15 device over there completely even without showing the  
16 second gate and it would work also as a low-noise  
17 amplifier so -- considering he himself tells us that  
18 his device is a low-noise amplifier.

19 That's how he describes it in the  
20 abstract. Okay. But what's your question exactly?

21 BY MR. BALICH:

22 Q. So the -- as depicted in figure 1, the

1 single gate of amplifier 20 is connected to the RF  
2 signal; is that correct?

3 MR. MACDONALD: Objection. Form.

4 A. well, through the filter, yes. There's an  
5 RF signal through a filter into the gate of signal  
6 20. And what's interesting also is it's connected to  
7 -- do you see there's a connection between those two  
8 resistors and the biasing circuit 80?

9 And so it's interesting that -- as I say,  
10 that's why I'm not convinced that it has very much  
11 gain because it looks like he does several things to  
12 hurt the gain, but amplification doesn't necessarily  
13 mean gain. You can have an amplifier with a gain of  
14 one and there's no amplification at all, but it's  
15 still called an amplifier.

16 BY MR. BALICH:

17 Q. And you mentioned the biasing circuitry  
18 80. What's the purpose of that?

19 A. well, it's very clear when you see the  
20 circuit it's connected to what they call the mix and  
21 able -- mixer enable (sic). Okay?

22 And he has a very interesting transistor

1 90 and that interesting transistor 90 looks like it  
2 has a drain connected to the gate, which would tell  
3 me that that's going to be fixed when it's on at a  
4 threshold voltage.

5           So it's fixing the node that's connected  
6 to resistors 84 and 18 to be some voltage above zero  
7 because you see transistor 90 goes to the ground --  
8 directly to the ground.

9           So there's some threshold voltage above  
10 zero which is probably a small voltage because it's  
11 never going to go more than that considering -- 90  
12 would have to be a drain connected gate because when  
13 you see something connected to the ground it must be  
14 the source.

15           And so that means this voltage at 84 is a  
16 very small voltage. It's no more than the threshold  
17 voltage. So that's what this balancing circuit looks  
18 to do, and through those two resistors somehow he's  
19 shunting the output.

20           And, as I said, I'm not an expert in RF  
21 circuits, but there's obviously some reason why he's  
22 fixing this voltage.

1           It's capacitively coupled, which means in  
2 the DC this whole node is sitting there biasing that  
3 threshold voltage 20 -- oh, okay, now that I'm  
4 speaking it out I see that 20 is now biased to the  
5 same voltage as 90.

6           Do you see that?

7       Q.     Yep.

8       A.     Okay. which means that this -- they call  
9 it the voltage balancing circuit is telling me that  
10 he's fixing that voltage here to be at -- to be at  
11 the threshold voltage.

12           So he's biasing that gate so that when you  
13 put in the RF signal it's a -- again, this is a nice  
14 trick. In fact, I have something that I thought was  
15 an invention of my own doing this with gallium  
16 nitride, but in gallium nitride devices today the  
17 threshold voltage vary a little too much. So you  
18 can't do this reliably.

19           But now -- you know, now I see. It's very  
20 simple. He's keeping that -- because 90 -- the drain  
21 of 90 is fixed at the threshold voltage above ground,  
22 he's keeping the node at 20 above ground.

1           You need to have resistors so if the RF  
2 signal comes in you want it to turn on and off to 20.  
3 So 20 is at the threshold voltage, which hopefully is  
4 the same threshold voltage as 90, and the RF signal  
5 going in there will turn that transistor on and off.  
6 So you'll get an amplifier.

7           So it's a very nice way of figuring out  
8 the Q-point. You know, I said that's the  
9 second-degree (sic) electrical engineer job  
10 challenge, is to find the Q-point of your amplifier.

11         Q.     And you just said will turn that  
12 transistor on and off. That transistor is transistor  
13 20 that you're referring to?

14         A.     Transistor 20 will be sitting at the  
15 threshold voltage. So it looks like he's trying to  
16 -- in the linear region. He's not turning on and  
17 off. He's actually amplifying the RF signal.

18           So it may be even a class A amplifier  
19 where the output has kind of the same characteristic  
20 as the input. It looks like that's what -- this is a  
21 biased -- I think he called it a biasing circuit, if  
22 I recall. So he's clearly biasing 20 to be at the

1 same voltage at the threshold from 90.

2           So he's assuming 90 and 20 have the same  
3 threshold voltage. And when you're at the threshold  
4 voltage a little higher is conducting, a little bit  
5 lower is insulating. There's always a range. So  
6 it's called a subthreshold current. So you're going  
7 to get an amplification at the threshold voltage.  
8 That's how he's getting an amplifier.

9           Q.     Okay. So the voltage at the gate of 20  
10 would be a variable voltage; is that right?

11           A.     Well, it's -- it's -- the input of the RF  
12 through the capacitor. So that would be the filtered  
13 RF say combined with what would be the DC voltage  
14 between 18 and 14. So that is the biased point, is  
15 the voltage between 84 and 18.

16                   (Whereupon, Madam Reporter asked for  
17 clarification from the witness.)

18           A.     Resistor is 18 and resistor 84, which is  
19 where that same input voltage is going. However,  
20 there's a capacitor. So my guess is that's supposed  
21 to be pretty much a DC set point otherwise known as  
22 the Q-point, the quiescent point.

1                   And so the RF signal would be -- if you  
2 want to say -- you're defining obviously it's -- in  
3 DC it would be -- it would be a constant voltage.  
4 But in the AC while RF is on there would be a  
5 variable voltage, I guess.

6                   BY MR. BALICH:

7           Q.       So there's a variable voltage going to the  
8 gate of FET 20?

9           A.       Well, as I said, you have to be very  
10 careful with definitions. Let's call it an RF signal  
11 that is around the quiescent point. So how -- do you  
12 want to define that as variable?

13                   These are the kind of definitions we have  
14 to get right away, right? I think of it as an RF  
15 signal around a particular DC voltage. Is it DC  
16 voltage without RF? Without RF it's going to be a  
17 signal that's amplified.

18           Q.       So the RF signal transforms the DC voltage  
19 into an alternating voltage?

20           A.       I guess that's probably a good way to  
21 describe it.

22           Q.       Okay. So now Bonn's Figure 1 also

1 includes a mixer 40; is that right?

2 A. That is right.

3 Q. And both gates of mixer 40 are connected  
4 to signals as well, correct?

5 A. The way we told it here -- as I said, my  
6 analysis was not on the mixer part because I was  
7 trying to use this to show the transistor he had,  
8 which Bonn tells us is a low-noise amplifier or a  
9 high-gain, high-frequency amplifier.

10 If you take away capacitor 40 such that  
11 it's not connected, then that would be a DC voltage  
12 on the bias of the second transistor.

13 what -- Bonn is teaching us how -- by  
14 having a cascode, and here he doesn't say they have  
15 to be one device. He doesn't say this is  
16 necessarily, although he's exciting (sic) about his  
17 invention, is that instead of having two devices  
18 hooked together the way we saw before with Sankin he  
19 says I can save space by putting it in one device  
20 because space is very important.

21 And that's the excitement, his excitement.  
22 So he is exploiting those two -- these two gates

1 which are coming out. So he shows that they're  
2 isolated since you have a -- the local oscillator  
3 circuit fed through we'll say capacitor 4 into 51,  
4 similarly the output of our low-noise amplifier going  
5 through 26.

6 And these two transistors are working  
7 together. And if you see by the biasing, it looks  
8 like they're both biased above zero. So we don't  
9 know even in this configuration he would want  
10 necessarily -- although he tells us you can make the  
11 upper transistor a depletion mode and the lower one  
12 enhancement mode.

13 But when I would look at this I would say  
14 these could both be enhancement modes because it  
15 would work the same function, how you bias it. You  
16 can't bias either of these negatively by the way he  
17 has it here.

18 So the mixing happens because you have the  
19 RF -- from the RF going through 26 into 31 and you  
20 have the local oscillator going through 44 into 51.  
21 And the signals are then mixed at the output from the  
22 drain 53 giving you an IF output through the

1 capacitor 56.

2 Q. Okay. I just want to break that down a  
3 little bit. You mentioned that as depicted in Figure  
4 1 both gate 30 and 50 would be enhancement mode  
5 gates; is that right?

6 MR. MACDONALD: Objection. Form.

7 A. I said if you look at the voltages applied  
8 -- and these would have to be quiescent voltages, as  
9 we said before. Because we see transistor 20 has a  
10 very careful biasing circuit, we notice the same  
11 thing on 31 with the transistor 32 to 28.

12 Now, unless the mixer enable is a negative  
13 voltage, which I think couldn't be for the sake of --  
14 I think we would have to say -- and I'm just doing  
15 this now. So I did not analyze this completely.

16 But it looks to me like the mixer enable  
17 is at a positive voltage. And I believe he does make  
18 reference -- and, again, it's only just from my  
19 memory.

20 He does make a reference about the enable  
21 -- it is positive, then it turns on. If he says  
22 that, then we know they're both likely enhancement

1 mode because, again, to be an amplifier even in a  
2 mixer you have to be above or at the threshold  
3 voltage. So the threshold voltage is very important.

4 That's why he goes through this whole  
5 circuit that shows how carefully you have to balance  
6 these voltages. So they're all sitting right at the  
7 threshold, and then we -- only then can it amplify or  
8 mix or do what else it wants to do. So that's why  
9 the biasing is very important, which is why I didn't  
10 want to analyze this.

11 I just wanted to analyze it in a normal  
12 way because that's the whole case over here, is that  
13 we're looking at a normal device, a standard  
14 amplifier that any POSITA would be able to build.

15 And I -- nowhere else in my entire  
16 document do I refer to Figure 1 other than what I  
17 called modified Figure 1 because it's a nice starting  
18 point. I could have just written it on my own. Any  
19 POSITA would no how to bias a normal cascode in a  
20 normal situation.

21 BY MR. BALICH:

22 Q. But in Figure 1 of Bonn gate 30 is

1 connected to the amplified RF signal; is that right?

2 A. It is, yes. We're hopefully biased  
3 properly such that the RF signal that comes in from  
4 the low-noise amplifier will trigger that transistor  
5 to operate on and off or, you know, amplify that  
6 signal.

7 Q. And gate 50 is connected to the LO signal;  
8 is that right?

9 A. It is connected through the capacitor in  
10 this circuit to -- biased at -- right, it has to be  
11 carefully biased, again, and assuming everything is  
12 correct, through the capacitor 44, assuming LO is an  
13 AC signal which I think is described as an oscillator  
14 -- so it probably is -- filtered with all those  
15 capacitors. And that's where 40 serves as a mixer.

16 Q. So then both gate 30 and 50 would be  
17 connecting to -- connected to alternating voltages?

18 MR. MACDONALD: Objection. Form.

19 A. Well, before you put -- before you turn on  
20 the oscillators, DC, that's the hardest part is  
21 making it to the quiescent point. I believe that's  
22 why he gave us these circuits, how they mix.

1           I think he gives us a lot of details. You  
2 may want to be careful about the current carrying  
3 capacity, blah, blah, blah. And, of course, he tells  
4 us that we can make either gate enhancement mode or  
5 depletion mode.

6           And he said preferably -- and I think his  
7 preferable -- in an amplifier you would make the  
8 enhancements mode the lower transistor 30 and the  
9 depletion mode 50, but I believe in this circuit this  
10 is not the case because they would have to be  
11 positive voltages.

12           And if you have a depletion mode biased  
13 positively, then you're not going to have any  
14 control. So there's -- that AC signal is going do  
15 nothing.

16           In fact, if we say that it is like one of  
17 the depictions that we put it in and that were  
18 depletion mode, I don't think that this will work as  
19 a mixer because, you know, it's way above threshold.  
20 It's not going to do anything.

21           So even if you have an AC signal going in  
22 and if it were in depletion mode biased above zero,

1 you're not going to get any mixing. So it would not  
2 work as a mixer if that were the way people are  
3 putting it out.

4 That's why you have to very carefully take  
5 it out of that and put it into a circuit that would  
6 work.

7 BY MR. BALICH:

8 Q. Okay. But Bonn's Figure 1 shows an AC  
9 signal going to both gate 30 and 50?

10 A. It shows the AC signal, but we have to  
11 assume that it's all biased properly because I said  
12 it can't be in this circuit the way it's biased that  
13 that second one would be in depletion mode.

14 Q. Okay. So now Figure 1 of Bonn does not  
15 disclose connecting a constant voltage source to  
16 either gate 30 or 50, right?

17 A. Okay. Again, the fact that he has RF  
18 signals going through as an amplifier, and if you  
19 want to define constant as being like some Q-point  
20 where there's always a DC, before you put on any AC  
21 there's always a constant voltage.

22 I would look at that biasing circuit --

1 and he's careful about the biasing circuit -- as a  
2 DC. It is a constant voltage. On top of the  
3 constant voltage he puts in a small signal which,  
4 hopefully, is around the threshold voltage if it's  
5 biased properly.

6 But, again, this is a secondary  
7 application. The primary application is as I've  
8 drawn. I'd rather -- you know, I don't think it  
9 matters how he configures it in Figure 1 because  
10 that's not the analysis that I did.

11 Q. So your analysis -- strike that.

12 In your analysis now you've proposed  
13 taking the Figure 1 circuitry and then converting it  
14 into an amplifier; is that right?

15 A. I'm proposing showing -- I'm not -- I'm  
16 not depending on his Figure 1. I did that as a way  
17 to illustrate. In fact, as we saw before the node 33  
18 of the source is not even connected to ground.  
19 Again, it's going through a special loop.

20 As I said, I'm not an expert in RF  
21 circuits, but it is not what we were defining before  
22 as a normal cascode at all. Although, I think he may

1 have described it as cascode-like, but it's not being  
2 used as an amplifier certainly.

3 My circuit I'm saying, okay, let's call it  
4 an amplifier. He called it an amplifier. He very  
5 clearly says it's an amplifier. In the abstract he  
6 says at the very end -- because that -- it's a device  
7 -- it's a device.

8 So let's connect it as an amplifier that  
9 has gain. So my amplifier I know has gain, and you  
10 put in an RF signal and you will get out an RF  
11 signal.

12 Q. So your modified circuitry would eliminate  
13 the down-converter function of Figure 1 of Bonn; is  
14 that right?

15 A. My figure is purely as an amplifier and  
16 I'm saying -- I'm not -- I'm not using my circuit for  
17 a down-converter. The same way Bonn -- when he says  
18 you can use it as an amplifier, he's also doing the  
19 same thing because, you know, he's using it as an  
20 amplifier not as a converter -- as a mixer.

21 So -- but a transistor has many functions,  
22 right? A transistor can be used as a mixer. It can

1 be used as an amplifier. As I say, it could be lots  
2 of other things, used as filters.

3 People use transistors all the time. It's  
4 the first most basic thing that you learn in  
5 engineering school. I try to teach our students that  
6 they know how to use transistors properly, and  
7 certainly any POSITA would not need to be shown this  
8 circuit in their head.

9 Mishra doesn't teach the circuit. Herman  
10 doesn't teach the circuit. None of these references  
11 I have I believe -- Mizuta doesn't teach the circuit.  
12 So they all assume you know how to use the circuit.  
13 So I'm just taking his device which is really his  
14 invention, his device, and putting it in a low-noise,  
15 high-frequency amplifier.

16 So the fact that he had a circuit was a  
17 nice thing to work with I thought or with counsel --  
18 with the counsel we decided that, you know, this is a  
19 nice starting place to explain the operation.

20 Q. And your circuit you're referring to your  
21 modified Bonn Figure 1 on page 65 of your  
22 declaration; is that right?

1           A.     Yes. I only refer to the rest of my  
2     declaration -- as I recall, I only referred to the  
3     modified -- my modified declaration -- my modified  
4     Figure 1 that I'm calling because that is what a  
5     POSITA would normally understand to be a  
6     high-frequency amplifier.

7           Q.     Okay. And so your modified of Figure 1  
8     would not function as a mixer, correct?

9           A.     As I said, honestly, I don't know how to  
10    make a mixer. I've never designed a mixer in my  
11    life. I don't know what would function or not  
12    function as a mixer.

13          Q.     And for fear of getting the same answer,  
14    your modified Figure 1 wouldn't function as a  
15    down-converter, correct?

16          A.     I don't know. Maybe it would.

17          Q.     But you're not aware that it would  
18    function as a down-converter, correct?

19                 MR. MACDONALD: Objection. Form.

20          A.     All I did -- what I did was I took the  
21    gate 51 of what is not necessarily in Bonn but what  
22    Bonn tells us we can do. Remember, all of his gates

1 are completely flexible. He can make it enhancement  
2 mode, depletion mode.

3 He can change the current carrying  
4 capacity of this one or that. He can make them  
5 match. He can make them unmatch. He can do whatever  
6 he wants with this to provide whatever function he  
7 wants, and he gives instructions so any POSITA would  
8 be able to build his transistor for their needs.

9 Now, I took 51 in Bonn. He has it biased  
10 with these resistors. If I took away capacitor 44,  
11 it would be no different than mine except he has it  
12 biased positively.

13 So if I had, for instance, an enhancement  
14 mode transistor for that second one, I could have put  
15 it to a constant bias, maybe more like Tessman like  
16 we talked about before or Sankin. I could bias that.

17 If I have the ability to get in there, if  
18 I have another terminal, I can bias it as I like. If  
19 they're the same transistor, which seems to be the  
20 way Bonn is explaining it, I can bias the voltage at  
21 a certain point, anything I like.

22 I can certainly make resistor 48 zero and

1 then I have exactly my circuit. Take resistor 48 and  
2 make it very, very small, just a solder joint. I  
3 could make resistor 48 a short-circuit and 46 to be  
4 an open circuit, and I have exactly my configuration  
5 of 51 going to ground.

6 I also have to remove capacitor 34 in  
7 order to make it a common source. So it would be an  
8 amplifier as any POSITA would know how to do.

9 BY MR. BALICH:

10 Q. So that's a great answer, but it didn't  
11 answer my question. Your modified figure on page 65  
12 of your declaration, to your knowledge, that would  
13 not work as a down-converter; is that correct?

14 MR. MACDONALD: Objection to form.

15 A. As I said, I have no experience making  
16 down-converters and I don't know that you cannot make  
17 a down-converter with a single transistor. Maybe  
18 that you could.

19 I think, in fact, Bonn says he knows you  
20 can, but he likes the idea about having them not  
21 interact with each other for some noise effects, but  
22 I do believe you can make a down-converter with even

1 a single transistor.

2 BY MR. BALICH:

3 Q. So in your declaration you opine that a  
4 POSITA would have found it obvious to use figure 7  
5 structure for high frequency signal amplification in  
6 place of mixer 40; is that right?

7 A. Bonn tells you explicitly this device,  
8 figure 7 -- I'll read it again if you like, column 11  
9 if I recall. Okay.

10 He says: "Therefore, the dual-gate FET  
11 structure of the present invention can be tailored to  
12 provide superior performance over the prior art  
13 dual-gate FET structures in high frequency signal  
14 mixing as well as other applications" -- because we  
15 know there are many.

16 You could probably make a mixer. I don't  
17 know. I know in -- you can make a comparator with a  
18 single transistor. So you can make a comparator with  
19 a signal transistor. That's sort of like a mixer.  
20 You can have the same function. You probably could  
21 use it as a cascode transistor, also other  
22 applications.

1           It could be maybe a different kind of  
2 converter, but I don't know enough about converters  
3 -- "such as high frequency signal amplification."  
4 And that's really all he needs to say to tell a  
5 POSITA how to make what I call the modified Figure 1.

6           Q.     Okay. In that passage you just read does  
7 Bonn specifically say to use the structure of figure  
8 7?

9           MR. MACDONALD: Objection. Form.

10          A.     well, the paragraph before says, "It  
11 should be noted that the FET structures described  
12 with reference to figures 3, 7, and 8."

13                 And I think if we go to figures 3, 7, and  
14 8 -- it's really 7 is the one -- 3 -- oh, so 3 is the  
15 vertical layout, 7 is the horizontal layout. So it's  
16 the same device. And 8 is the same device without  
17 any non-conducting regions as he calls them.

18                 So he's talking about this exact device.  
19 He's talking about specifically figure 7 as the only  
20 one describing the cross-section of what the  
21 transistor looks like.

22                 BY MR. BALICH:

1           Q.     So in that paragraph you just read, Bonn  
2     says: "It should be noted that the FET structures  
3     described with reference to figures 3, 7, and 8 are  
4     not limited to gallium arsenide FET structures"; is  
5     that correct?

6           A.     That is correct. They're equally  
7     applicable to arsenide -- they're equally applicable  
8     to insulated gate FETs; that is, IG FET structures.

9                     And -- well, that's why -- as we said,  
10    that's -- that, for me, says, oh, if I have a GaN  
11    device like Ren -- that is an insulated gate  
12    structure in GaN as opposed to gallium arsenide --  
13    then he's referring also to not only gallium arsenide  
14    here but also to GaN over here because Ren tells you  
15    this insulated gate gallium nitride device has  
16    enhancement mode or depletion mode just like he has  
17    enhancement mode and depletion mode.

18                    So it seems like he's describing how in  
19    the future when -- by 2006 when people were to come  
20    along and make GaN based insulated gate transistors,  
21    then, voila, Bonn is also describing that his -- his  
22    circuit, his semiconductor, figure 7, can be applied

1 to that technology as well.

2 And I think that's a very, very simple  
3 straightforward combination and that's what I did.

4 Q. So the paragraph that you read earlier,  
5 column 11, lines 23 through 37, does that paragraph  
6 mention figure 7?

7 A. well, paragraph -- figure 7 mentions --  
8 this is the finale of his patent. It should be noted  
9 the J -- you have to start with this paragraph.

10 And by now after you've read the previous  
11 paragraph, by now it should be appreciated that a  
12 down-converter and a method of generating RF signals  
13 have been provided, okay, which I would not have  
14 known if Bonn didn't show me this whole circuit.

15 But the transistor is just a simple  
16 transistor. So he's very happy to have taught how to  
17 make a down-converter out of this interesting circuit  
18 where you have access to both the gates of the upper  
19 transistor and lower transistor.

20 But in his descriptions of figure 7 he  
21 says you can have depletion modes, enhancement modes  
22 which you can do in gallium arsenide and they were

1 not at the time able to do it in gallium nitride.

2 Of course, the advantages of gallium  
3 nitride became very clear later on, and that's what  
4 our patent, the Herman patent at issue, is, is the  
5 gallium nitride. And it's obvious, you know, to  
6 anyone reading his documents that since he said it  
7 can be applied to any IGFET and figures 3, 7, and 8,  
8 he's telling you how to make a power circuit.

9 That's exactly how you would lay out a  
10 power transistor. He's doing it in GaN, in gallium  
11 arsenide, and Ren comes along and does exactly the  
12 same thing in GaN with an insulator.

13 So he easily has -- he can accomplish --  
14 everything that -- that Bonn was teaching here I can  
15 accomplish ten years later in -- not ten years later  
16 -- this is 2003, so we'll give it eight or nine years  
17 later. You're able to accomplish in Ren -- with Ren  
18 combined with Bonn.

19 Q. Okay. Turning back to your expert  
20 declaration at page 65, which I think you're already  
21 at --

22 A. Yes.

1           Q.     -- again, we've gone over -- you proposed  
2 modifications to Bonn's circuitry of Figure 1; is  
3 that right?

4           A.     well, when you use the word  
5 "modification," we have to be careful here because  
6 really I was trying to build an amplifier because  
7 that's what Bonn says to do. The fact that he has  
8 his transistor in here as a mixer is nice because he  
9 taught how to make a mixer.

10                   I don't use it. I have no interest in  
11 making a mixer, and I think for the case of the -- I  
12 should say the issues in this -- in our case, in our  
13 -- in the lawsuit, whatever it is, don't relate to a  
14 mixer.

15                   But he tells us all he has to do is -- he  
16 tells us in the abstract and he tells us at the end  
17 of the document, really I made a cascode transistor.  
18 And everyone knows 99 percent of power devices are  
19 used as, you know, either an amplifier or as a  
20 switching circuit the way power switches would use.

21                   There is a niche application, although I  
22 guess probably people in RF use these kinds of things

1 all the time. Again, I'm not an RF engineer. I  
2 don't pretend to be. I don't think I need to be to  
3 be able to opine on semiconductor devices.

4 So it's the devices that I'm focusing on,  
5 and that's why I wouldn't call it a modification.  
6 Really, I'm just building a circuit around that so we  
7 can see. It's nice that this is the only reference  
8 that I've seen actually where the circuit is in there  
9 because he's trying to teach us something special  
10 about the circuit.

11 We didn't need that circuit. None of the  
12 other patents have circuits. Herman doesn't have a  
13 circuit. No one has a circuit because it's obvious  
14 any POSITA would know how to take a transistor and  
15 stick it to ground.

16 Q. So on the caption below the figure on page  
17 65 you have a parenthetical, and you say modified,  
18 right?

19 A. Right. Maybe -- I could maybe -- maybe --  
20 maybe this was an error. Of course, when we make a  
21 declaration there's a lot of back-and-forth with  
22 counsel. And I don't remember why the decision was

1 to modify one into what we would say -- and not just  
2 from the beginning.

3 Certainly, I did with my simulation. I  
4 just made up my own circuit. So I could have just  
5 made up my own circuit and put it in there. But it  
6 was, we thought, a convenient thing because it's up,  
7 it's using one of the patents that we're referring  
8 to.

9 So it's -- yeah, we probably did not have  
10 to say modified. I would have just said build a high  
11 gate amplifier, design an amplifier.

12 Q. Okay. In your declaration you don't  
13 propose any modifications to the dual-gate FET  
14 structure of figure 7 of Bonn; is that right?

15 A. Well, Bonn describes figure 7 in many,  
16 many different ways. There's two gates. They're  
17 both fully adjustable. You can change the doping  
18 profile. You can do -- you can use even different  
19 gate structures.

20 In fact, I believe he says at the end how  
21 flexible he says it is, and he gives very good  
22 directions for any POSITA to be able to design a

1 depletion mode and an enhancement mode.

2           So he can make 23 in enhancement mode  
3 according to the way he teaches it. You can make 326  
4 a depletion mode the way he handles it.

5           And that's why I added Mizuta just to show  
6 that you could put a field plate, which would allow  
7 you to go to higher voltages which would be obvious  
8 for someone who wants to make a device that can  
9 handle higher voltages. Maybe more than 20 or 30  
10 volts you'll start needing field plates.

11           Certainly by 100 volts or 200 volts you  
12 need to have field plates, just the nature of the  
13 world.

14           So Bonn tells us exactly from figure 7  
15 with the ability to be able to make a depletion mode  
16 and an enhancement mode as the lower transistor, a  
17 depletion on the upper transistor, and he says that  
18 would be as a cascode and -- which would have the  
19 same channel and have all the characteristics we  
20 need.

21           So any POSITA would then design his  
22 circuit. And then, of course, he says even figures 3

1 and 8 -- really 3 is less important because not too  
2 many people, as far as I know, are going to put  
3 non-insulating -- we're not worried so much about the  
4 current carrying capacity.

5 He's worried about that in the mixer  
6 application maybe, but I think a normal person -- a  
7 normal device I would buy from Infineon, for  
8 instance, would look more like figure 8 in terms of  
9 the source and the drain.

10 They would have field plates on them  
11 connected to ground, which is what we did here. So  
12 there would be source connected field plates. If you  
13 want it intentionally as a cascode, then you'd have  
14 to know exactly what -- the diffusion you need and  
15 that's why we have Ren to teach us how to make the  
16 insulated gate D-mode.

17 But I would use exactly figure 7 as  
18 described by Bonn to make this transistor or any  
19 POSITA would be able to.

20 Q. So other than adding the field plate to  
21 gate 326, do you propose any other modifications to  
22 Bonn's figure 7 structure?

1 MR. MACDONALD: Objection. Form.

2 A. Okay. Within Bonn -- and this is just a  
3 layout figure -- Bonn describes what are these layers  
4 321 and 322. They're different dopings (sic). Okay?

5 And assuming the first one within Bonn --  
6 again, it's within Bonn. Bonn is very broad. Bonn  
7 teaches -- my full flexibility, I can make whatever  
8 current carrying capacity I want for one or the  
9 other.

10 And so within Bonn I could make the oxides  
11 thicker or thinner and I can make the AlGaN thinner  
12 and thinner (sic). In fact, Ren tells me by changing  
13 the thickness of the AlGaN I can easily make one  
14 enhancement mode and one depletion mode.

15 So I don't know if it's really a  
16 modification or just using the teaching of Ren in  
17 this figure from Bonn. I can make the full power  
18 device.

19 BY MR. BALICH:

20 Q. In your declaration, you don't propose a  
21 specific modification other than the field plate to  
22 figure 7; is that right?

1 MR. MACDONALD: Objection. Asked and  
2 answered.

3 A. I'll answer it again, if you'd like.  
4 within 7 describe the way Bonn describes it and  
5 assuming he sets it up in the way that the POSITA  
6 would want to to make the enhancement mode and  
7 depletion mode in the right way, without a field  
8 plate this device is probably not going to get to the  
9 kind of voltages someone who wants to get higher  
10 voltage or higher gain amplifier.

11 So simply adding a field plate, which  
12 Mizuta does very nicely because he shows even  
13 different ways of dielectrics, different ways of  
14 making that field plate. It doubles to a two-tiered  
15 field plate.

16 Now his field plate is attached to the  
17 gate, as is the way I depicted it is attached to the  
18 gate. You can attach the gate to the field plate or  
19 we can do as Mishra tells us. And he tells us that I  
20 can make a -- paragraph 62 -- oh, paragraph 62 and -3  
21 it is understood that we can -- that one alternative,  
22 we can comprise a single transistor with two gates.

1           So Mishra has a dual-gate structure which  
2 I pointed out from figure 5 of Mishra where it is not  
3 a gate-connected field plate but rather a  
4 source-connected field plate.

5           And that's where I said, according to the  
6 theory of Infineon, any source-connected field plate  
7 may be good gate. I don't know about that.

8           Mishra doesn't comment on it, other than  
9 being a source-connected field plate, he says over  
10 here, "although the present invention has been  
11 described in considerable detail with references,  
12 certain preferred configurations thereof."

13           Other versions are possible. So he says,  
14 "The field plate can be used in many different  
15 devices. A field plate can also have many different  
16 shapes and can be connected to the source contact in  
17 many different ways."

18           So Mishra tells us how to make a  
19 source-connected field plate. Ren tells us if that  
20 oxide was thin enough so there's capacitive coupling  
21 to the AlGaN layer. I would have a -- let me get  
22 this right -- depletion mode device which would be

1 directly connected to the enhancement mode device,  
2 and it would look an awful lot like Herman.

3 BY MR. BALICH:

4 Q. Dr. Bernstein, I appreciate that. I've  
5 got limited time here. And I asked you specifically  
6 about Bonn, and you went on for a few minutes about  
7 Mishra and Ren that are not part of your ground 1  
8 combination.

9 And so I would appreciate that going  
10 forward you could answer my questions. And if your  
11 counsel has further explanation that he wants to come  
12 out, then your counsel can ask follow-up questions.

13 MR. MACDONALD: I mean, just to be clear,  
14 when we're talking about Bonn and figure 7, it's not  
15 just ground 1, and that's why he's speaking about  
16 Ren. I think that the question while I was objecting  
17 should be a little more focused to help focus the  
18 discussion.

19 MR. BALICH: Sure. I appreciate that.

20 BY MR. BALICH:

21 Q. So as it applies to ground 1, you've  
22 proposed adding a field plate to one of Bonn's gates

1 in figure 7?

2 A. Right.

3 Q. In your declaration, do you propose making  
4 any other modifications to figure 7?

5 A. well, as I said, when you say  
6 modifications, it's so broadly described, assuming  
7 I'm using it, as we said, making a device much like I  
8 depicted in my -- in my modified figure 1 where you  
9 would have an enhancement mode, which would see the  
10 low voltage, and as I showed in my simulation, if you  
11 make a depletion mode which has a threshold voltage  
12 connected to ground which could be a source-connected  
13 field plate.

14 I have illustrated it here as a  
15 gate-connected field plate. You would need some sort  
16 of field plate where the voltage is held at a  
17 constant voltage low enough so that a drain which  
18 would allow to go to a higher voltage but which would  
19 not short out the gate.

20 That is a very, very -- it's the  
21 reliability -- this is what I study all the time.  
22 That is the most common failure mechanism, is that

1 there will be too much voltage that will get toward  
2 the gate.

3 The gates are very sensitive, so you have  
4 to keep the voltage away from the gate in a GaN  
5 device or -- and also gallium arsenide as well.

6 Q. So Bonn's dual-gate FET as shown in figure  
7 7 has a first gate with a smaller current carrying  
8 capacity than the second gate; is that right?

9 MR. MACDONALD: Objection. Form.

10 A. I think Bonn says they're completely  
11 flexible. In fact, if you look at figure 8 they both  
12 look like they're exactly the same current carrying  
13 capacity. So I don't know where you said -- get that  
14 from.

15 Do you have a source where you think that  
16 he says that?

17 BY MR. BALICH:

18 Q. Sure. If you take a look at Bonn, column  
19 5, starting at line 37. And let me know when you're  
20 there.

21 A. Prior art down-converters, is that where  
22 you're reading from? From where?

1           Q.     Column 5 of line -- I got the line -- 37.  
2     So it says, "FET 30 preferably has a smaller current  
3     conducting capacity than that of FET 50 to prevent  
4     FET 50 from being driven into current saturation by a  
5     strong RF signal that may appear at the gate  
6     electrode of FET 30."

7                     Did I read that correctly?

8           A.     You read that correctly, but I'm not  
9     opining on it as a mixer, I said before. He's  
10    talking about it in a very specific case of a mixer  
11    where he's making intentionally -- in fact, he shows  
12    in figure -- the one that said for figure 3 how he's  
13    intentionally making non-conducting regions.

14                    But he also says the non-conducting  
15    regions are completely flexible. You can put them on  
16    the upper transistor or the lower transistor. I  
17    cannot have them at all like he shows in figure 8.

18                    He can do anything he wants to make the  
19    current carrying capacity either more or less on  
20    either one of those devices, but it's certainly  
21    flexible. And a POSITA would want to make a normal  
22    high-gain amplifier, as I've depicted, and would more

1 likely use the figure 8 without any non-conducting  
2 servers (sic), in which case, the current carrying  
3 capacity would be the same.

4 And I really -- to be honest, just to  
5 finish your question, I don't honestly understand  
6 what he means when he says current carrying capacity,  
7 other than the on state resistance, RDS, because by  
8 making the width narrower he's only making the  
9 resistance higher.

10 So if he wants to balance the on state  
11 resistance, which is the way I'll say a normal POSITA  
12 that I understand -- a non-RF engineer would  
13 understand this transistor.

14 A current carrying capacitor generally  
15 means either -- well, it's not really an art term  
16 when you're describing transistors. You'll see RDS  
17 on. You'll see maximum voltage. You'll see maximum  
18 current.

19 If they mean by maximum current -- these  
20 two transistors are in series, which means  
21 Kirchhoff's current law, the same current. One may  
22 have more resistance than the other. It may blow up,

1 may get too hot. I don't know what he means, but  
2 either way Bonn does not commit to one or the other  
3 being higher or lower current carrying capacity.

4 Q. Now, you don't rely on figure 8  
5 specifically in your expert declaration, do you?

6 A. I do not.

7 Q. And then if you could turn to column 7 of  
8 Bonn, beginning at line 10. Let me know when you're  
9 there. Bonn states, "Non-conductive sections 225  
10 reduce the effective channel width of the first gate  
11 region in structure 200."

12 Did I read that correctly?

13 A. You did.

14 Q. So Bonn is intentionally introducing  
15 non-conductive sections to reduce the effective  
16 channel width; is that right?

17 MR. MACDONALD: Objection. Form.

18 A. As we said, he is specifically designing a  
19 transistor as a mixer. So -- which means he wants to  
20 tune the resistance, the onset resistance of the  
21 upper or the lower device so that they're tuned to  
22 each other so they're tuned to the circuit.

1           That's not my application. He also says I  
2 could if I want to put non-conducting sections on the  
3 other transistor. He also says I can put it on  
4 neither transistor. And, as I said, I didn't bring  
5 up figure 8, but I looked at figure 8 and you don't  
6 see any non-conducting regions.

7           So he doesn't require non-conducting  
8 regions anywhere. And he says in all of this in  
9 column 11 when he talks about the down-converter,  
10 "equally applicable to any insulated gate  
11 transistor."

12           Or is it in column 9? He does -- I'll  
13 just say it -- outside and I'm sure we can find it if  
14 we look. He does say that those non-conducting  
15 structures are not limited, are not -- are not  
16 required on any -- in either of the gates.

17           So, you know, if he wants to design one  
18 where it's restricted in one on (sic) the other,  
19 that's fine. But he also gives you the flexibility  
20 of figure 7, which has no non-conducting area.

21           The non-conducting areas are from the  
22 other two figures, I think, 225 -- figures 4 and 5

1 show you where you can have a section where there's  
2 non-conducting and conducting areas.

3 But the normal application for a normal  
4 amplifier would not have these, and he's open for  
5 that. He says you don't have to have the  
6 non-conducting regions.

7 BY MR. BALICH:

8 Q. If you turn to Bonn, column 8, starting at  
9 line 13 Bonn begins describing figure 7; is that  
10 right?

11 A. Yes, "Figure 7 is a cross-sectional view  
12 of a field-effect transistor structure in accordance  
13 with yet another embodiment of the present  
14 invention."

15 Q. And Bonn continues describing figure 7  
16 until column 9, line 28 when Bonn starts describing  
17 figure 8; is that right?

18 A. That's fair.

19 Q. So in the preceding paragraph, column 9  
20 that begins line -- well, 12 --

21 A. 12, it should be understood.

22 Q. -- that "non-conducting (sic) sections

1 like non-conductive sections 225 in structure 200 of  
2 figure 3 can be formed in the first gate region 321,  
3 second gate region 322, or both, to individually  
4 adjust the gate width of each gate"; is that right?

5 Did I read that correctly?

6 A. You read that correctly.

7 Q. And that applies to figure 7, correct?

8 A. well, it's a cross-sectional view. Figure  
9 7 is a cross-section. He gave two cross-sections  
10 earlier to somehow differentiate between  
11 non-conducting and conducting, but he said it's the  
12 same idea.

13 This is a conducting, but I could easily  
14 make some of it non-conducting. But it's not  
15 required on any of them as well. He does say either  
16 the upper or the lower or both, but they're optional  
17 completely. In figure 8 he shows none.

18 Q. So the non-conducting sections would mean  
19 that if such a fact (sic) were used as an amplifier  
20 it would operate with mismatched current densities;  
21 is that right?

22 A. If you -- the properties of a channel are

1 -- the resistance is really the most important  
2 aspect. when you turn it on there's a certain  
3 resistance of the channel.

4           The width -- if you make it wider, there's  
5 more current or to say a lower resistance. If you  
6 make them narrower, there's more resistance. So he's  
7 really describing the variability if you want for  
8 some reason. Usually, in power devices you want it  
9 all just current.

10           But there's no discontinuity in current.  
11 Kirchhoff's current law always applies. So it means  
12 whatever current is in the first (unintelligible), it  
13 will automatically be in the second region.

14           If he's restricting the flow by reducing  
15 the width of one or the other, that will only mean  
16 there will be a higher resistance or a higher voltage  
17 drop across that part. It will always work, and of  
18 course it will work because it's just making one  
19 width smaller than the other.

20           I don't know why you would do it, and  
21 that's why he has a nice figure 8 where none of it's  
22 -- he's doing it -- again, I don't understand enough

1 about RF circuits. He's doing it for a very specific  
2 reason in his down-converters, and I do not know his  
3 reason.

4 I did not analyze his reason, and I  
5 honestly think it makes no difference in our  
6 proceedings whether -- what his intention was by  
7 adding non-conducting regions.

8 But it is not something you'll see in most  
9 normal transistors because normally you would like to  
10 get as much current -- you want to get the lowest  
11 possible on resistance. That's how you make your  
12 transistors better.

13 But to restrict the flow to make your  
14 resistance higher in a certain part or the other, the  
15 current is going to flow. It's going to work. It  
16 just may be a little bit more power dissipated than  
17 you would like.

18 Q. And you didn't specifically comment in  
19 your declaration on the non-conductive sections in  
20 Bonn's figure 7, correct?

21 MR. MACDONALD: Objection. Form.

22 A. I'm using figure 7 to show us the teaching

1 of Bonn, how it applies to the '003 patent. There is  
2 no non-conductive sections in the '003 patent or in  
3 Mishra or in anybody else. Most people are designing  
4 these devices for high power.

5           They want to get as much transconductance  
6 as possible. They want to get high gain. And by  
7 intentionally restricting the gain by lowering the  
8 current flow between devices, you're not getting your  
9 maximum current through, which means you're going to  
10 have a higher voltage drop.

11           It will certainly work, and I didn't --  
12 it's immaterial because that's not what the  
13 proceeding here is about. Nobody cares about these  
14 non-conducting sections. And you don't need it, even  
15 according to Bonn, only if you're trying to do some  
16 balance with these RF signals, which I don't know the  
17 details of, and I didn't feel it was anything that I  
18 needed to analyze.

19           BY MR. BALICH:

20           Q.     If you could turn to page 56 of your  
21 declaration --

22           MR. MACDONALD: And I think it might be

1 almost time for a break. I think lunch may be here.

2 THE WITNESS: I don't mind answering this  
3 last question.

4 MR. BALICH: Let's go ahead and take a  
5 break. Let's go off the record.

6 (Whereupon, at 12:17 p.m., a  
7 luncheon recess was taken.)

8 - - -

9 A F T E R N O O N S E S S I O N

10 (12:58 p.m.)

11 Whereupon,

12 JOSEPH B. BERNSTEIN, PH.D.

13 was called for continued examination, and having been  
14 previously duly sworn was examined and testified  
15 further as follows:

16 EXAMINATION BY COUNSEL FOR PATENT OWNER  
17 CONTINUED

18 BY MR. BALICH:

19 Q. welcome back from lunch.

20 A. Thank you.

21 Q. If you could turn to Exhibit 1007, so this  
22 is Mizuta.

1           A.     Yes, I have it here.

2           Q.     So Exhibit 1007 -- and I'm going to read  
3 the patent number -- is U.S. Patent Number 6,483,135;  
4 is that right?

5           A.     That's the number. You read it correctly.

6           Q.     And the first named inventor is Masashi  
7 Mizuta; is that correct?

8           A.     I don't know how to pronounce Japanese,  
9 but I'm assuming so.

10          Q.     I just want to clarify one thing. In your  
11 declaration you refer to Exhibit 1007 as Mizuto (sic)  
12 and --

13          A.     I saw that. He wrote Mizuto even, you see  
14 that?

15          Q.     Got it. So if I refer to this document as  
16 Mizuta, with an A, you'll understand I'm referring to  
17 Exhibit 1007; is that correct?

18          A.     That is perfectly fair.

19          Q.     Okay. So now if you could turn back to  
20 your report, page 56 you should see paragraph 83 and  
21 that begins your overview of Mizuta, right?

22          A.     That is correct.

1 Q. Okay. You don't allege that Mizuta  
2 discloses a dual-gate transistor; is that right?

3 A. I have in the next picture, figure 11(b),  
4 which I would say is a dual-gate transistor and by  
5 description it is, but I use this really only for the  
6 -- for the field plate.

7 Q. Okay. So let's -- let's turn back to  
8 Mizuta.

9 A. Okay.

10 Q. If you could turn to column 12, and then I  
11 think line 33, do you see the paragraph that begins,  
12 "This FET can be produced"?

13 A. Yes.

14 Q. And Mizuta says that, "This FET can be  
15 produced by forming a subelectrode 12 after a gate  
16 electrode 5"; is that correct?

17 A. That's exactly what it says.

18 Q. And that's referring to figure 11(b),  
19 correct?

20 A. That is correct, yes, 11(b).

21 Q. And you reproduced figure 11(b) in your  
22 report at page 57?

1           A.     I did.

2           Q.     And so reference numeral 12 is a  
3 subelectrode. It's not a gate; is that right?

4                   MR. MACDONALD: Objection. Form.

5           A.     well, he describes what it is. "The  
6 subelectrode 12 is connected, for example, with a  
7 drain electrode, to which a positive voltage is  
8 applied. This lowers the resistance of the region  
9 directly under the subelectrode 12 and eases the  
10 current flow so the higher efficiency of the element  
11 can be attained," is what he says.

12                   If it changes in any way the current flow  
13 by definition, a field gate that is above the  
14 channel, even if it increases or decreases the  
15 resistance, would be a gate by most definitions of  
16 what a gate is, but I didn't rely on this as a  
17 certain gate.

18                   It looks pretty similar to the -- to a  
19 dual-gate, but it is. He describes it as you would  
20 describe a gate, a field-effect transistor is where  
21 the voltage that is separated by an insulator will  
22 affect the field, is what affects the on resistance

1 or the conductivity.

2 BY MR. BALICH:

3 Q. Just so I understand, your understanding  
4 of a gate is anything that affects the conductivity  
5 of semiconductor under it?

6 A. Well, anything actually. It's with a  
7 field -- it's called a field-effect transistor. That  
8 means by putting a voltage that creates an electric  
9 field across an insulator and there is a conductive  
10 flow.

11 If you put it on with a thick insulator  
12 like we do with a field plate, it will -- there's a  
13 point there because it does affect the fields. It is  
14 always a field-effect if you have metal next to a  
15 semiconductor. There's some field effect.

16 That's why you need -- closer has more  
17 capacitive coupling. Farther away it has less  
18 capacitive coupling, but he's calling it a  
19 subelectrode. I don't think he really defines what  
20 he means by subelectrode.

21 But he wants to actually connect that to  
22 the drain if this is in what we said was a -- I don't

1 want to opine on what he was thinking with this  
2 subelectrode, but he describes it in that paragraph  
3 over there as something that does affect the current  
4 flow.

5 But he wants to put a positive voltage,  
6 which means if it's completion mode somehow it can  
7 turn the transistor on more. So he obviously meant  
8 that it's close enough that there's some effect of a  
9 voltage on the channel.

10 He said it lowers the resistance of the  
11 region. well, a resistor that's controlled by a gate  
12 is by definition a transistor.

13 Q. And I know you just said it, but it has  
14 now escaped my brain. what is the subelectrode 12  
15 connected to?

16 A. For example, to the drain electrode. So  
17 he's having it to -- somehow adding field on the  
18 source site. I don't know that anyone does this in  
19 practice other than making that a separate gate, but  
20 it looks like it's a depletion mode as if because  
21 he's adding more voltage while somehow making it more  
22 conductive.

1 But generally you wouldn't connect -- I  
2 mean, it's funny, though, because he's adding a field  
3 plate, which is why it's a very strange configuration  
4 by his own description because with a field plate you  
5 want to shield the gate from the drain side.

6 To then have the drain connect back over  
7 to the source side seems odd unless he has some other  
8 distances and he's not showing why he's doing this,  
9 but he's showing that there is a gate there.

10 And it obviously has an effect on the  
11 resistance, so if you change the resistance by  
12 putting voltage on a gate, that means this  
13 subelectrode is a gate. You know, it's like if it  
14 quacks like a duck --

15 Q. Sure. So would the subelectrode act as a  
16 depletion mode gate or an enhancement mode gate?

17 A. Well that, would all depend on the barrier  
18 levels and the material underneath it.

19 Like, for instance, if it's AlGa<sub>N</sub> that's  
20 of a certain thickness -- what we learn from Ren,  
21 where if it's a thin gate and it's a thin dielectric  
22 and a thin AlGa<sub>N</sub>, then it would be -- you know, he's

1 -- it looks like it's still on even with zero voltage  
2 because it said it could be connected, for instance,  
3 to the drain.

4 But either way it's an N channel, but  
5 let's -- I think he's neutral. Right now you can say  
6 if it's a thick enough gate it would be let's say,  
7 depletion mode and this would just -- raising it up  
8 would somehow lower the resistance of the channel.

9 It would be giving it more carriers, which  
10 it would do. It would give more carriers -- Ren  
11 actually has beautiful pictures of the channel --  
12 carrier channel. But you could have also made the  
13 AlGaN thinner and the oxide thinner, in which case,  
14 it could be designed -- if we use the teaching of Ren  
15 there, we could easily put Ren's enhancement mode  
16 gate in that position. There's no reason not to.

17 BY MR. BALICH:

18 Q. Okay. So getting back, though, to figure  
19 11(b) of Mizuta, so if the subelectrode 12 acts as a  
20 gate, would there then be two depletion mode gates,  
21 12 and 5 next to each other; is that right?

22 A. I don't think he defines 5 necessarily as

1 being depletion mode. You can make it anything you  
2 want. It's just a field-effect transistor. You  
3 could just as easily make -- just as we learned in  
4 Bonn, have flexibility. We learned from Ren exactly  
5 how to be flexible.

6 I just change the thicknesses in my  
7 aluminum nitride and my gate oxide and I can make  
8 either one depletion or enhancement mode. There's  
9 only two choices, either enhancement or depletion.

10 Q. And Mizuta does not disclose which one  
11 referenced numeral 12 in reference to numeral 5; is  
12 that right?

13 A. I would have to read the whole thing over  
14 again. I don't recall if he commits to any of them  
15 being enhancement or depletion mode. It may be if  
16 you want to tell me a particular place in there that  
17 you're referring to.

18 Q. No. I must have misunderstood what you  
19 were telling me earlier. That's okay.

20 In any event, you're not relying on Mizuta  
21 for the disclosure of the dual-gauge structure; is  
22 that right?

1           A.     Right. I mean, I put it in my report  
2 here, it looks awfully close, but I'm relying on  
3 Mizuta for the field plate --

4           Q.     Okay.

5           A.     -- especially because I bring Ren up in  
6 the next section.

7           Q.     Then if you'd take a look at column --  
8 still in Mizuta -- column 11, line 42.

9           A.     Let me change my glasses -- oh, that's  
10 okay. I'm okay. Column 11, line 42. The FET or the  
11 present example?

12          Q.     Hold on. Hold on -- strike that. If  
13 you'll look at column 12, line 42 where we were. So  
14 Mizuta states that "The subelectrode 12 is connected,  
15 for example, with a drain electrode, to which a  
16 positive voltage is applied."

17                   Did I read that correctly?

18          A.     Yes, that's what it says.

19          Q.     Does the mention of a positive voltage  
20 tell us what type of gate subelectrode 12 would form  
21 or does it not?

22          A.     It doesn't teach us that, because whenever

1 you go above the -- even if the threshold is  
2 negative, you could still put a more positive voltage  
3 and it would make the resistor go down because it  
4 fills up the channel.

5 Q. Okay. Let's go back to your declaration,  
6 page 102. And this is the start of the section on  
7 ground 2 Bonn, Ren, and Mishra; is that right?

8 A. Somewhere near the start, yes. Well, it's  
9 Number 4 to 1 -- claim 1 -- is in claim 1 and this I  
10 believe is a combination of Bonn, Ren, and Mishra.  
11 So that's ground 2. I forget what my grounds are.

12 Q. So you're on page 102 --

13 A. I'm going back to page 102 where it says,  
14 "Motivation to Combine Bonn, Ren, and Mishra."

15 Q. Correct. Exactly. So in paragraph 156  
16 you opine that a POSITA would have modified Bonn to  
17 make it into an amplifier; is that right?

18 A. I explained that before. Where are you  
19 reading?

20 Q. Paragraph 156.

21 A. Yes. It expressed disclosure in the  
22 dual-gate FETs. (Reading unintelligibly). That was

1 -- right.

2 Q. And in paragraph 156 you cross-reference  
3 your prior analysis from ground 1 that explains this  
4 "Motivation to Modify Bonn for High Frequency Signal  
5 Amplification," right?

6 A. That's well, you said modify. I would say  
7 I'm using Bonn, using Bonn within the specification  
8 of Bonn. So I don't think of myself as modifying  
9 figure 7, if that's what you're saying.

10 Q. well, the section heading says, Motivation  
11 to Modify Bonn," right?

12 A. Right. Fine. well, I was thinking more  
13 modifying like my circuit, how I'm putting it in.  
14 But figure 7 is describing the transistor. So I'm  
15 not -- Bonn's transistor can be any shape and form  
16 that I want. So I don't know if that's a  
17 modification. Maybe, I don't know.

18 Q. Okay.

19 A. This are words. This is language. This  
20 is not the engineering.

21 Q. Sure. Sure. And my question is that you  
22 -- you're relying on your analysis from ground 1 in

1 terms of the modifications you make to Bonn for  
2 ground 2?

3 A. I believe I'm referring back to the  
4 analysis I did in 1(b) I think it was -- or what I  
5 did before in my -- oh, right, ground 1. I believe,  
6 yes. I believe it was all explained in ground 1.  
7 Yes, okay.

8 Q. Okay. And in paragraph 156 you don't cite  
9 Ren as contributing to any reason to modify Bonn's  
10 circuitry; is that right?

11 A. well, for the sake of the field gate, the  
12 field gate doesn't require me to be in gallium  
13 nitride. I mean, I use Ren really just to show that  
14 I'm going to go from gallium arsenide to gallium  
15 nitride.

16 I believe Mishra or Mishro (sic) or  
17 whatever his name is -- oh, Mishra. Mishra is the  
18 other guy. Mishra is the professor -- excuse me,  
19 Professor Mishra. Mishra is the one with the field  
20 plate over the separate field plate, not the one  
21 attached to the gate.

22 So this is Bonn, Ren, and Mishra. I was

1 confused because I thought we were talking about  
2 Mizuto (sic). So I don't have Mizuto here. So maybe  
3 I was -- I was in the wrong mindset.

4 Can you please ask the question again?

5 Q. Sure. In paragraph 156 that you've got at  
6 page 102, you don't cite Ren as contributing to any  
7 reason to modify Bonn's circuitry; is that right?

8 A. Okay. That's a good question. I mean, I  
9 use Ren to tell us that I can take the teachings of  
10 Bonn and use it for gallium nitride. I use Mishra or  
11 the other one -- but in this case we're using Mishra  
12 to tell us about the field plate.

13 Q. Let me ask it a different way. In the  
14 section "Motivation to Combine Bonn, Ren, and  
15 Mishra," you've got three subsections.

16 A. A.

17 Q. A is the motivation to combine and then  
18 you've got a subsection 1 on page 102.

19 A. I'm just going back. This is section  
20 Roman numeral 8, ground 2, Bonn, Ren, and Mishra.  
21 And you're saying section A, which is motivation to  
22 combine?

1 Q. Right. And then there's a subsection 1.  
2 On that same page, "Motivation to Modify Bonn,"  
3 right?

4 A. Um-hum.

5 Q. Don't flip the page yet. On page 103  
6 there's a subsection 2, "Motivation to Combine Bonn's  
7 High Frequency Signal Amplification Embodiment with  
8 Ren"; correct?

9 A. Yes.

10 Q. And then if you turn to page 108, you've  
11 got a third subsection "Bonn, Ren, and Mishra."  
12 Do you see that?

13 A. Yes, I do.

14 Q. So each subsection, one, two, and three,  
15 describes a different modification; is that right?

16 A. A different modification or a different  
17 way of looking at it.

18 Q. Okay. And so starting with the last one,  
19 Number 3, that's where you describe the addition of a  
20 field plate; is that right?

21 A. I believe that's why we added Mishra here.  
22 Do we have Mishra otherwise? Mishra here is to teach

1 us the field plate that's not connected to the gate.

2 Q. Correct. And then the second subsection  
3 that began on page 103, this was the subsection about  
4 making Bonn's transistor out of gallium nitride; is  
5 that right?

6 A. That sounds correct. My motivation to  
7 combine Bonn's high frequency signal with Ren to make  
8 gallium nitride, yes.

9 Q. And so then the first subsection, the  
10 "Motivation to Modify Bonn for High Frequency Signal  
11 Amplification," that describes the modifications  
12 needed to make Bonn circuitry into an amplifier; is  
13 that right?

14 A. The modification -- only that modification  
15 of figure 1, right. Maybe that was a poor choice of  
16 words, but that's -- right. I didn't have to say  
17 that, as we say, but that's what I did.

18 Q. And instead of copying and pasting  
19 everything that you had in ground 1 you simply  
20 cross-reference your prior analysis in ground 1 in  
21 paragraph 156; is that right?

22 A. If I make a reference C section, yes,

1 7(a)(1), yes.

2 Q. Okay. And so in that analysis in that  
3 cross-reference in paragraph 156 -- in that paragraph  
4 you're not relying on Ren to modify Bonn, correct?

5 MR. MACDONALD: Objection. Form.

6 A. Well, I bring Ren -- Ren coming up in the  
7 next section too, so we're seeing --

8 BY MR. BALICH:

9 Q. Right. So in Section 1 --

10 A. I'm just simply stating what we had  
11 already learned from Section 1.

12 Q. Okay. And I think that's what I'm trying  
13 to drive at, is that Ren and Mishra don't form any  
14 reason to modify Bonn's circuitry beyond what you had  
15 previously described in ground 1?

16 A. Well, I described certainly in ground 1  
17 Bonn by telling us that it's in IGT -- IG transistor  
18 integrating into transistor, as I said, and the  
19 capacitors and the channel characteristics are fully  
20 flexible.

21 And he said -- I think he gives the  
22 motivation himself. I think he says, if I'm not

1 mistaken, it should be noted in column 10, a line  
2 around 12 -- it should be noted that the FET  
3 structures described in reference to figure 3, 7, and  
4 8 are not limited to gallium arsenide FET structures.  
5 They are equally applicable to insulated gate FETs,  
6 and Ren is an insulated gate FET.

7 Ah, ten years later on GaN, but I think  
8 the motivation to combine is very clear that any  
9 POSITA would say if I had a Ren I could use that for  
10 his insulated gate FET.

11 Q. Right. But that has to do with changing  
12 of the technology of the transistor, right?

13 A. That's what he's teaching. He's teaching,  
14 as I said, a field effect transistor.

15 Q. Right. I'm just asking about the  
16 circuitry, taking the circuitry and transforming it  
17 into the modified circuitry that you provide in your  
18 declaration.

19 A. Right. I -- maybe -- the way you're  
20 bringing it up here sounds like modified maybe was  
21 not the right word. I'm just making an amplifier, a  
22 simple amplifier.

1           So that's what I'm saying. The only  
2 modification is I'm just using his circuit as a  
3 representation for what any POSITA would know how to  
4 put a transistor into an amplifier.

5           Q.     Okay. So in making the amplifier you're  
6 not relying on the teachings of Ren and Mishra?

7           A.     Okay. An amplifier has a box where the  
8 transistor goes. That transistor can be a silicon  
9 transistor. It can be anything I want. It's still  
10 an amplifier.

11                 My analysis describes very clearly when  
12 I'm talking about GaN versus gallium arsenide and how  
13 a POSITA would be able to modify from the gallium  
14 arsenide of Bonn to a gallium nitride of Ren, and  
15 either way the transistor will have whatever  
16 characteristic that transistor has and will work in  
17 this amplifier.

18           Q.     Okay. My question doesn't have to do with  
19 the transistor. It just has to do with the  
20 circuitry, just the circuitry.

21           A.     And I don't understand your question.

22           Q.     Okay. In making the circuitry of an

1 amplifier you are relying exclusively on Bonn.

2 You're not relying on Ren and Mishra in ground 2?

3 A. Okay. I said before I'm not relying on  
4 Bonn for that circuit. I even made my own circuit  
5 for the simulation. I'm relying on the fact that I  
6 know what a circuit looks like.

7 The reason I'm using the modification of  
8 figure 1 is only for convenience. Since we have a  
9 circuit that has it in there, we figure -- I don't  
10 know -- I could have just said, well, I'm just going  
11 to build an amplifier and that's what it would look  
12 like.

13 So I'm just taking out from Bonn, his  
14 circuit, and taking out the amplifier part and  
15 hooking it up to be an amplifier so that we're all on  
16 the same page, and we know that that's really what  
17 we're dealing with.

18 Q. Okay. You're not relying on Ren and  
19 Mishra for the amplifier circuitry on page 103?

20 A. I'm relying on just the fact that that's  
21 how you build an amplifier with a transistor, any  
22 field effect transistor from anybody's patent from

1 any company.

2 Q. Okay. If you could turn back in your  
3 expert declaration to page 57, this is a start of the  
4 summary that you provide on the disclosure of Ren?

5 A. Overview of Ren, yes.

6 Q. And you don't allege that Ren discloses a  
7 dual-gate transistor; is that right?

8 A. Well, everything in Ren is really just  
9 about the gate, and he doesn't show any dual-gate of  
10 any transistor.

11 So he teaches how you can make an  
12 enhancement mode or a depletion mode from the same --  
13 in the same process, which is -- technologically,  
14 that's the breakthrough, you need to make it, you  
15 know, something like silicon where you have PMOS and  
16 NMOS. There's no PMOS equivalent in gallium nitride  
17 or gallium arsenide. So that's why this is  
18 important.

19 Q. If you could turn to Exhibit 1009 --

20 A. Mishra.

21 Q. -- Mishra. Do you recognize Exhibit 1009  
22 -- and I'm going to read the patent application

1 number -- as US patent publication number  
2 2005/0051800?

3 A. That's correct.

4 Q. And the first named inventor is Umesh  
5 Mishra; is that correct?

6 A. I don't know if it's Umesh (phonetic) or  
7 Umesh, but yes.

8 Q. And if I refer to this document as Mishra,  
9 you'll understand that I'm referring to Exhibit 1009,  
10 correct?

11 A. Yes, correct.

12 Q. Figures 1 and 2 of Mishra show a single  
13 gate transistor; is that right?

14 A. Yes, it does.

15 Q. And if you turn the page to figure 6, that  
16 shows a single gate transistor as well, correct?

17 A. well, Mishra is making a big deal about  
18 the field plate on the gate, which is similar, but  
19 illustrated here is a single-gate transistor.

20 Q. Figure 8 shows a single-gate transistor;  
21 is that right?

22 MR. MACDONALD: Objection. Form.

1           A.     Figure 8 does also. But if I can point to  
2 what I think I pointed to before, paragraph 62,  
3 wherein all of these transistors -- "It is understood  
4 that many different amplifier arrangements can be  
5 used according to the present invention. One  
6 alternative arrangement comprises a single transistor  
7 with a dual-gate structure."

8                     So he certainly allows us to make any one  
9 of his into a dual-gate structure regardless of which  
10 number is printed with or without a dual-gate.

11                    And as I said before, we saw in 63 he  
12 tells us that on -- well, you didn't get to it yet,  
13 but figure 5 is what I used before for -- element 66  
14 is certainly connected to the source, and then we can  
15 decide if that's a field plate or if it's a gate.

16                    BY MR. BALICH:

17           Q.     We'll get there.

18           A.     You're getting there. All right. I'm  
19 ready to go.

20           Q.     So now, looking at figures 3 and 4 of  
21 Mishra, those disclose the same embodiment, one from  
22 the top view and one a cross-section; is that right?

1           A.     It looks that way. I didn't read it in  
2 detail. Again, I have to remind myself, but it looks  
3 like that's a field plate. Element 46 is the same as  
4 element 46 on figure 4. So, yes, it looks like it's  
5 a cross-section versus a top view.

6           Q.     And Mishra discloses that field plate 46  
7 is connected to the gate 42 in figures 3 and 4,  
8 correct?

9                   MR. MACDONALD: Objection. Form.

10          A.     He tells us that 46 can be connected to  
11 42. Similarly, he tells us it can be connected to  
12 20, the source. Right now it's a separate device.  
13 Maybe he would want to put it into a mixer circuit  
14 for all I know, but I don't know. I don't think he  
15 requires it to be connected to the gate.

16                   BY MR. BALICH:

17          Q.     But figure 3 shows that it's connected?

18                   MR. MACDONALD: Objection. Form.

19          A.     Well, I turn to paragraph 40. It says,  
20 "The field plate 46 can be electrically connected to  
21 the gate 42 and figure 3 shows two alternative gate  
22 connection structures that can be used, although it

1 is understood that other connection structures can be  
2 used," for instance, we said before, even to the  
3 source, which --

4 BY MR. BALICH:

5 Q. Okay. Mishra doesn't disclose connecting  
6 the field plate to the source, does Mishra?

7 A. What do you mean? He does. I read that  
8 to you -- oh, I didn't read it to you. Paragraph 29,  
9 if I recall, I think he clearly says it.

10 He says, "The field plate can be  
11 electrically connected to the gate contact and in  
12 some embodiments the field plate is formed as an  
13 extension of the gate contact" -- see -- "while in  
14 other embodiments the field plate and gate electrode  
15 are formed during separate deposition steps. In  
16 still other embodiments the field plate can be  
17 connected to the source contact."

18 So that's pretty clear. And 63 he says:  
19 "Although the present invention has been described in  
20 considerable detail with reference to certain  
21 configurations thereof, other versions are possible.

22 "The field plate arrangement can be used

1 in many different devices. The field plates can also  
2 have many different shapes and can be connected to  
3 the source contact in many different ways."

4 Yes -- sorry. I'm happy I remembered  
5 where it was. Okay.

6 Q. If you could turn to paragraph 52 of  
7 Mishra. Paragraph 252 discloses that the embodiment  
8 of figure 9 shows an MESFET.

9 A. You can call it a MESFET.

10 Q. So paragraph 52 of Mishra discloses that  
11 figure 9 shows a MESFET; is that right?

12 A. Yes. Let me look at figure 9, please.  
13 Yes.

14 Q. And paragraph 52 also states that figure 9  
15 "has a gate and a field plate structure similar to  
16 that of the HEMT 40 shown in figures 3 and 4"; is  
17 that right?

18 A. Oh, high-electron mobility transistor.  
19 They call it a HEMT, H-E-M-T.

20 Q. So let me restate the question. Mishra 52  
21 -- paragraph 52 states that the gate in the field  
22 plate structure of figure 9 are similar to that of

1 figures 3 and 4; is that right?

2 A. That's correct.

3 Q. Let's turn to paragraph 42. Paragraph 42  
4 talks about figure 5; is that right?

5 A. Yes.

6 Q. And Mishra discloses that figure 5  
7 "includes a field plate 66 on the spacer layer 64  
8 that overlaps the gamma gate 62."

9 A. Where are you reading again, please?

10 Q. Sure.

11 A. Paragraph 42 I don't see any 66.

12 Q. Actually, let's take a look at paragraph  
13 43.

14 A. He's talking about figure 5, which is our  
15 gamma gate. Okay.

16 Q. So at the top of page 4 with the  
17 continuation of paragraph 43, Mishra says that "HEMT  
18 60 also includes a field plate 66 on the spacer layer  
19 64 that overlaps the gamma gate 62."

20 Did I read that correctly?

21 A. Yes, you did, with the field plate 66  
22 preferably deposited on the side of the gamma gate

1 not having a horizontal overhanging section. That's  
2 his distinction between figures 4 and 5.

3 Q. Okay. And then in the next paragraph,  
4 paragraph 44, Mishra discloses that "like the field  
5 plate 46 shown in figures 3 and 4" --

6 A. Yes. That's the one you showed before.

7 Q. -- "the field plate 66 can be connected to  
8 the gate 62 in many different ways"; is that right?

9 A. Field plate 66 -- which paragraph are you  
10 reading?

11 Q. Paragraph 44, the first sentence.

12 A. Oh, "Like the field plate 46 shown in  
13 figures 3 and 4, the field plate 66 be connected to  
14 the gate 62 in many different ways," yes.

15 Q. Okay.

16 A. And he says before not necessarily because  
17 -- we saw that we do allow it to be connected to a  
18 source, but -- and then we go back to the same  
19 argument about the source connected field plate.

20 But in many different ways he's saying, as  
21 he said before, it means with vias -- I think he  
22 described it very clearly with vias -- it can be

1 connected with vias.

2 Q. what's the purpose of field plate 66 in  
3 figure 5?

4 MR. MACDONALD: Objection. Form.

5 A. First of all, he does make some  
6 distinctions between a HEMT and a MESFET, which there  
7 are subtle differences between the two.

8 HEMT is the kind that we're talking about.  
9 Generally, gallium nitride is -- we used today -- are  
10 in the high-electron mobility transistor mode.

11 A MESFET is a metal semiconductor contact  
12 where it looks more like a JFET where, again, you  
13 turn off what he calls the channel.

14 It's interesting in his figures they're  
15 both labeled very much the same -- I just noticed  
16 this now -- and he calls the channel this whole area.

17 But in a HEMT the channel area would be  
18 the small amount, and in a MESFET it would be  
19 underneath but structurally it's very similar.

20 And the field plate, to answer your  
21 question, on number 66 is -- as we said, it's a field  
22 plate generally to protect the gate. And you can

1 connect it to the gate. And as we learned from many  
2 operations, you don't really want to increase the  
3 capacitings (sic).

4 So generally nowadays we put the field  
5 plate which is on the drain side of the gate  
6 connected to the source to protect the field from  
7 farming the gate. It's a reliability issue, which is  
8 how I'm so familiar with this area.

9 BY MR. BALICH:

10 Q. Okay. Does the field plate 66 at all act  
11 as a gate?

12 A. Well, it all depends on the thicknesses.  
13 I think I mentioned that if the oxide -- or the  
14 insulating thickness Number 64 is thin enough such as  
15 there's capacitive coupling to the -- what could be  
16 the AlGa<sub>N</sub> region -- I think in his case that probably  
17 would be AlGa<sub>N</sub> -- then we have Ren who tells us by  
18 controlling these amounts it would obviously be a  
19 gate.

20 In fact, I can even make it an enhancement  
21 mode gate if I wanted, or if it's thicker, a less  
22 connection where the aluminum AlGa<sub>N</sub> layer is thicker

1 and oxide is thinner, it can be like a depletion mode  
2 gate.

3 And, of course, if it's very thick like  
4 sort of depicted in figure 4 where it may not have  
5 any influence at all, it may only prevent the fields  
6 from coming in and it may not act like a gate at all.

7 So it all depends on the relative terms  
8 and thicknesses -- not terms -- excuse me -- the  
9 relative thicknesses and dielectric constants, et  
10 cetera.

11 Q. If you turn to paragraph 59 of Mishra,  
12 Mishra is talking about the first stage transistor  
13 Q1; is that right?

14 A. Well, here he's referring to figure 10.  
15 He's referring to our dual-gate configuration.

16 Q. So in paragraph 59 the last sentence that  
17 begins with Moreover -- do you see Moreover? --

18 A. Yes.

19 Q. -- Mishra says: "Since the first stage  
20 amplifier Q1 does not include a field plate" -- do  
21 you see that?

22 A. Yes, yes.

1 Q. So all of the figures that we just looked  
2 at, 1, 3, 4, 5, those all have field plates, right?

3 A. Well, he's describing a very special case  
4 here. The idea is that if we were to make like, you  
5 know, the combined gate, which it sounds like he's  
6 implying, and certainly the way I read in my article  
7 where you could make this an actual Q2.

8 The distinction is very -- not -- how it  
9 affected your designing is such that there is a field  
10 plate such that this would be, let's say, a depletion  
11 mode transistor.

12 The idea is that the cutoff of that  
13 depletion mode will stop any more fields, so you  
14 don't need -- that's the whole point. You don't need  
15 a field plate on the gate if you have a field plate  
16 that's hanging -- overhanging.

17 Again, you could connect it just as easily  
18 to the gate because it will keep the same voltage,  
19 but you could reduce the capacitance by connecting 66  
20 to the source.

21 Q. In figure 5 that you're looking at right  
22 now, gate 62 itself has its own field plate; is that

1 right?

2 A. He's calling this -- this is the gamma  
3 configuration as they called it, and the field plate  
4 is pointing to the source side.

5 Q. Correct.

6 A. So it's not going to have the same effect  
7 for the high voltage, but he's introducing this here  
8 -- usually, we try to make a very, very small  
9 connection as possible and you need some room, but  
10 there is still voltage on the gate.

11 So I don't honestly know what it's from  
12 because the gate voltage is not much higher than the  
13 source voltage, so we're not worried about a  
14 breakdown on this side.

15 So I guess he can extend it over if he  
16 wants, but I believe the only reason he makes it  
17 skinny over here is because he wants to narrow that  
18 as much as possible to reduce the capacitance to the  
19 substrate.

20 Q. And so what we're describing is element 62  
21 has a small portion that's in contact with 18; is  
22 that correct?

1           A.     Right. Again, in this configuration it's  
2 in contact. Of course, I modified it to be  
3 insulating gate like Ren. His is not like Ren. His  
4 is a MESFET. MESFET would mean metal. You use the  
5 ME for metal, the metal semiconductor. When the  
6 metal directly touched the semiconductor, that's a  
7 MESFET.

8                     If it's an insulator, it could be an  
9 insulated gate MESFET or it could be a high-electron  
10 mobility transistor and HEMT.

11                    (Whereupon, Madam Reporter asked for  
12 clarification from the witness.)

13           A.     There could be an insulator there, which  
14 would make it an insulated gate HEMT, but if it's  
15 directly conducting the silicon, it could be a  
16 MESFET.

17                    BY MR. BALICH:

18           Q.     And again, looking at figure 5, there's a  
19 portion of gate 62 that is not in direct contact with  
20 18; is that right?

21           A.     That is correct.

22           Q.     And so the portion of 62 that's not in

1 direct contact with 18 that's what a POSITA would  
2 understand is a field plate, right?

3 A. well, it certainly acts like a field plate  
4 like he's showing below. I don't recall why exactly  
5 he wants that gamma gate. I thought it might have to  
6 do with processing, and I'd have to read again to --  
7 I don't know that I commented on that. Because it's  
8 on the source side it certainly is not a protection  
9 issue.

10 Q. Right. And then looking at the structure  
11 labeled 66 in figure 5, the portion that goes up and  
12 overlaps gate 62, that would be a field plate; is  
13 that right?

14 A. Yes. He describes the whole thing as a  
15 field plate, and I was only showing how it can be  
16 easily interpreted to be his dual-gate as he says you  
17 can implement a dual-gate in figure 10, assuming that  
18 that oxide thickness 64 is thin enough such that it  
19 will be an effective depletion mode transistor and  
20 then it would have a field plate, of course, going  
21 sort of in the wrong direction.

22 But it's -- for manufacturing purposes you

1 need to have -- you need to have some leeway in how  
2 you deposit the metals.

3 Q. So if both 62 and 66 were used as gates,  
4 they would both have field plates?

5 A. Usually, the -- okay. The field plate is  
6 only there to protect from high fields from damaging  
7 the gate.

8 So if the -- if it's arranged in such a  
9 way, for instance, like this where 66 is connected to  
10 the source, there's no worry that the field by the  
11 gate region which is only going to go to some 5 volts  
12 and small voltage because it's turning on and off the  
13 gate, but the drain can be at 100 volts.

14 An electric field goes from the positive  
15 to the negative and it goes basically in lines, and  
16 if there's a conductor, the lines will move around.

17 So anything near the 100 volts is going to  
18 be closer to 100 volts. If you're halfway between  
19 zero and 100 volts, you're up to 50 volts and that's  
20 the voltage at that point.

21 A field plate as -- a field plate is there  
22 to protect what's underneath it in general. So this

1 62 having the field plate to the left, I don't really  
2 know what it's protecting from what, but 66 is  
3 certainly protecting what would be the high voltage  
4 at drain number 22, that voltage, from effecting the  
5 gate.

6 Q. I want to circle back to that concept of  
7 protecting the high voltage. I appreciate that  
8 Mishra calls element 66 the field plate. But would a  
9 POSA understand it to be a field plate?

10 A. That's bread and butter for another  
11 engineer working in these fields. Field plates are  
12 essential.

13 I mean, when I was working in the '80s,  
14 you know, even with silicon devices, international  
15 rectifiers, original MOSFETs, they had field plates.  
16 Everything needs a field plate if your voltages are  
17 above 20 and 30 volts just because you don't want --  
18 working with very big voltage you don't want  
19 breakdowns.

20 You have to be very, very careful with  
21 field plates always when you're working with voltages  
22 above, you know, something that could be dangerous.

1           Q.     Let me rephrase the question a little bit.  
2     You had mentioned something that field plates  
3     typically are intended to protect against the high  
4     voltages and they're typically positioned such that  
5     they go in the direction of the drain.

6                     And I'm sure I'm not accurately describing  
7     what you told me. But my question is: Given the  
8     purpose of a field plate, would a POA just looking  
9     at figure 5 of Mishra not have understood those  
10    structures to be field plates because of the  
11    traditional purpose of a field plate?

12          A.     well, in my own report on page 144 and 143  
13    you can see on the same opening the -- we'll say the  
14    accused product -- whatever you want to call it --  
15    and Mishra. And by the Infineon theory, the G2,  
16    they're calling it a second gate. Whereas, in Mishra  
17    he calls it a field plate.

18                    But you can see it's really only dependent  
19    on the thickness whether or not it is a gate that is  
20    a Ren depletion mode transistor, which is, I believe,  
21    what in Mishra it means when he says you can have  
22    this.

1           And it's not purely as a field plate  
2 because it works also to turn off -- once this  
3 transistor turns on, then there's no more field. All  
4 the field will be between the field plate and the  
5 drain, which is exactly the intention here.

6           The drain is way over here and this is  
7 meant to be a 600-volt device, it looks like, because  
8 there will be one gate turned off when this will get  
9 to, let's say, 200 volts and then here this will be  
10 maybe 100 volts.

11           And so all the higher fields -- that's why  
12 there has to be a higher -- there may be a third one.  
13 You can do as many as you want as a field plate to  
14 protect this delicate gate which is only being turned  
15 on at like 5 volts. If more than 10 volts gets  
16 across the gate, it's dead. It's very strong  
17 reliability problems.

18           So these are very, very important to have  
19 field plates on transistors. And if you look at the  
20 structure of the field plate and, as I said, if I  
21 make the oxide thin enough, I can make an actual and  
22 effective gate that can turn on in something like 3

1 or 4 volts and not, you know, have to withstand 100  
2 volts.

3 MR. MACDONALD: Sorry, just to clarify for  
4 the record, Dr. Bernstein was pointing at the center  
5 numbered pages 143 and 144.

6 THE WITNESS: Oh, I'm sorry. Pages 156 of  
7 my -- and 157.

8 BY MR. BALICH:

9 Q. So then is your interpretation of the --  
10 you're in ground 3?

11 A. I don't know where I am. Maybe it's  
12 ground 3. It's the end of the book. You're asking  
13 me the same question, so --

14 Q. Sure. It doesn't matter. So is your  
15 interpretation of the figure on page 182 of your  
16 report --

17 A. 157 --

18 Q. -- sorry -- 157. Is your interpretation  
19 of the image on page 157 of your report based on how  
20 a POSA would have understood it or is it based on  
21 Infineon's infringement theories?

22 A. No, no, no. This is not based on

1 Infineon's infringement theory. I'm basing this on  
2 Ren who -- so a POSITA who knows or a POSA who knows  
3 Ren and understands that metal on top of an insulator  
4 on top of a GaN device can make a depletion mode  
5 transistor with the proper thickness of GaN and  
6 within a proper amount of capacitive coupling.

7           So he would probably have it thinner, but  
8 these are all diagrams. I can make it -- a POSA  
9 would know how to make that oxide thinner so that you  
10 can get the capacitive coupling and you can turn this  
11 on at whatever voltage you want, 5 volts, and it  
12 won't necessarily act as a field plate which is  
13 designed for much higher voltage.

14       Q.     So getting back to the unmodified version  
15 of Mishra figure 5 --

16       A.     Oh, it's -- the only modification here is  
17 the oxide that I put under the gate. This is exactly  
18 5.

19       Q.     Okay. Both structures 62 and 66 have  
20 field plates; is that right?

21       A.     66 -- there's no second field plate shown  
22 over what would be 66. But if 66 were like Mishra

1 says, if 66 were, in fact, a gate and you wanted to  
2 set -- any of his structures can be used in a  
3 dual-gate system. I could make any one of his  
4 transistors also. I can make another one in -- as  
5 many as I want at whatever threshold voltage I'd like  
6 to choose.

7 Q. Right. But it's your opinion that if  
8 structure 66 was a gate it would include as shown in  
9 figure 5 a field plate?

10 A. What's interesting about the field plate  
11 is that it's pointing in the south direction.

12 Q. Right.

13 A. But you could call that a field plate, but  
14 it's not a very effective field plate. It's just the  
15 way it deposits it.

16 You could put like we did over here a  
17 second field plate and this would be a field plate at  
18 second gate as the way -- and the theory of Infineon  
19 where they want to say any source connected field  
20 plate is a gate.

21 I'm not so sure because it's a field plate  
22 because the voltage is much higher. So here it's a

1 gate if you make the oxide thinner. That's all that  
2 I'm saying. Ren teaches us how to make a transistor  
3 in exactly that configuration.

4 Q. So let's go back to Ren paragraph 59. Let  
5 me know when you're there.

6 A. Ren?

7 Q. I misspoke. Mishra.

8 A. Oh, okay.

9 Q. Mishra paragraph 59.

10 A. Okay.

11 Q. And so this is the one with the sentence  
12 moreover, Q1 does not include a field plate.

13 A. Well, first of all, you have to see he's  
14 referring to figure 10. So we don't know how these  
15 are configurative.

16 I guess he said either the alternative  
17 arrangement is a single transistor with a dual-gate,  
18 which is how we're looking at it, or if he's talking  
19 about two separate transistors, which I think is one  
20 of the cases you were saying.

21 It could be either of those, but -- so  
22 let's understand that he's talking about the circuit

1 figure right now without interpretation of field  
2 plates or anything.

3 Q. Sure. So in figure 10 Q1 does not include  
4 a field plate?

5 A. I don't know. Maybe it does. He doesn't  
6 commit himself.

7 Q. well, Mishra says in paragraph 59 --

8 A. "Since the maximum voltage that can appear  
9 on the drain of the first stage transistor Q1 is the  
10 threshold voltage of the second stage transistor Q2,  
11 the first stage transistor Q1 does not 'see' high  
12 fields (sic) or high electric fields and hence would  
13 not benefit from a field plate."

14 whether it has one or not, I don't know,  
15 but it won't necessarily benefit because the voltage  
16 is guaranteed to be low enough, which is telling me  
17 that he's saying the threshold voltage of this one  
18 has to be low enough to not affect the gate in this  
19 configuration, which is why it really much depends on  
20 -- what do you call it? -- how thick that oxide is,  
21 as we said before.

22 Q. Okay. But then in the next sentence,

1 "Moreover" --

2 A. Moreover, since the first stage Q1 does  
3 not include a field plate -- oh, so he's now assuming  
4 it doesn't in this arrangement. First he said it  
5 won't need to if -- that's what he said, if the field  
6 plate is -- you know, if the second one turns on at a  
7 low enough voltage, that's fine.

8 And since this stage does not in his  
9 example include a field plate it does not experience  
10 the increased capacitance associated with a field  
11 plate, thereby permitting higher gain at its  
12 operating frequency.

13 This is the advantage of the cascode. I  
14 think I've spoke about this certainly at length.  
15 That's why we want to use this because you don't have  
16 the extra capacitance of the field plate because you  
17 have the Q2 which will shut off before the voltage  
18 goes -- my simulations show this, you know, right.

19 Q. So then if Mishra tells us that amplifier  
20 Q1 does not include a field plate, any structure that  
21 has a field plate must not be Q1; is that right?

22 MR. MACDONALD: Objection to form.

1           A.     You're making a logical conclusion which  
2 is not true. I could -- if I were to take two  
3 transistors and it happens to have a field plate,  
4 even if I only use it to vi (sic) volt and it might  
5 not have needed it doesn't mean I can't use it with a  
6 field plate.

7                   BY MR. BALICH:

8           Q.     So I'm more asking about Mishra's  
9 disclosure than what could be done.

10          A.     Mishra -- if he's disclosing this as a  
11 field plate -- and, as we said, he can include two.  
12 And we know from -- well, certainly from Bonn -- but  
13 we know from Ren how I can make one in depletion mode  
14 and one in enhancement mode, which I've shown very  
15 clearly.

16                   You would not need this field plate that's  
17 going to the 6, and that's what he says. That's  
18 right. That would only --

19                   (Whereupon, Madam Reporter asked for  
20 clarification from the witness.)

21          A.     Element 66 would not need to be a field  
22 plate for that gate because it's not protecting from

1 -- we are protecting it from the drain voltage, which  
2 is very high 22. So probably element 66 would need  
3 another field plate on top of it to get to higher  
4 voltage.

5 But, again, it all depends on what voltage  
6 you're designing for. If you're designing for a  
7 20-volt circuit, you might not need any field plates  
8 and this would just be a gate. So everything is all  
9 very flexible and it all depends on the application  
10 of the engineer who wants to design his circuit.

11 BY MR. BALICH:

12 Q. Okay. Let's turn to paragraph 62 of  
13 Mishra. And Mishra says: "It is understood that  
14 many different amplifier arrangements can be used  
15 according to the present invention. One alternative  
16 arrangement comprises a single transistor with a  
17 dual-gate structure."

18 Did I read that correctly?

19 A. Yes, and I think I said that a few times.

20 Q. Sure. So Mishra describes the dual-gate  
21 structure as an alternative arrangement, right?

22 A. Well, you understand that he's -- he's

1 teaching us how to make a gate. And we know that if  
2 you want to put two, three, or four -- I think  
3 somewhere else we discussed or if not -- in the old  
4 days of vacuum tubes they always had many gates, but  
5 there would be a reason to even if nothing else to  
6 have either floating or connected field plates so  
7 that the main -- I'll say the main gate which turns  
8 on and off -- all you're doing is controlling the  
9 channel current, right?

10           So when you turn off that channel current,  
11 it doesn't matter what's out there. The current  
12 doesn't flow. So you can use two or three gates, but  
13 he's describing the gate junction itself, and in this  
14 case he's showing something with some internal field  
15 plate for the gate.

16           But he obviously is showing you I can make  
17 this for many, many more gates. He did not suggest  
18 necessarily -- that's why I had to include the Ren  
19 combination. He's not telling us that that field  
20 plate is also a gate.

21           I'm saying within him he can -- within  
22 Mishra we can certainly call this a gate if that

1 oxide is thin enough and it has the interaction to  
2 make it like a second gate in a dual-gate structure.

3           So he is describing a dual-gate structure,  
4 and I'm showing how we can in a sense either modify  
5 -- if not modification, just play with the  
6 thicknesses of the oxide and the AlGaN to make it a  
7 second gate, and then we have his -- his cascode  
8 figure 10.

9           Q.     Okay. Just -- just to be clear, figure 5  
10 without modification does not show a dual-gate  
11 structure; is that correct?

12           A.     Well, the way I see it, if -- again, it's  
13 either a gate or it's -- it's -- it's either a gate  
14 and that's why he used the Infineon theory because  
15 that's not a standard theory to say that any plate --  
16 any -- what do you call it? -- a field plate -- any  
17 source connected field plate is a gate.

18                   I understand that's the theory that you're  
19 using. I'm not opining on that because I don't think  
20 that's a standard art term or understanding. Whether  
21 something is a field plate or a gate depends on the  
22 threshold voltage that it causes.

1           So you can make with Ren, his teaching --  
2 I can choose to make the oxide and the AlGaN  
3 thickness proper such that I can make it a gate and I  
4 can probably control the threshold voltage to  
5 whatever I want it to be, even 5 volts so it's a low  
6 enough voltage so that the lower gate doesn't see  
7 voltage above that 5 volts.

8           Mishra says very clearly that whatever  
9 threshold volt that that turns on it's got to be a  
10 negative threshold -- it's a depletion mode. The  
11 enhancement mode will not see beyond that because  
12 obviously the field has stopped there and everything  
13 is going to go from the field plate and up.

14         Q.     So now you've been pointing to the picture  
15 on page 157 of your report?

16         A.     Oh, yes, I'm sorry. I could have just  
17 been using figure 5. I just picked figure 5. It  
18 made nice colors here. So that's why I --

19         Q.     And for the picture on page 157 you  
20 explained that you modified figure 5 of Mishra with  
21 Ren; is that right?

22         A.     Right. I made this to be consistent with

1 Ren.

2 Q. So for the unmodified figure 5 of Mishra,  
3 Mishra itself does not disclose that figure 5 is a  
4 dual-gate structure; is that correct?

5 A. He calls 66 -- as I recall, he calls it a  
6 field plate and I don't think he commits himself to  
7 if it's enhancement mode, depletion mode. I think  
8 he's completely silent about that. He's just talking  
9 about the effect of the field plate in relation to  
10 the drain.

11 So this is between the gate and the drain,  
12 so it's a field plate and -- as disclosed in Mishra,  
13 which is why Mishra by itself, we're not only holding  
14 -- we're not only saying Mishra anticipates or --

15 Q. I appreciate that, and that's what I was  
16 asking.

17 A. I thought that you were asking --

18 Q. I only ask simple questions.

19 A. Okay.

20 Q. So --

21 A. But it looks awful similar, doesn't it?

22 MR. MACDONALD: Sorry. It looks like I

1 just lost the real time. It just suddenly crashed.

2 MR. BALICH: Let's go off the record and  
3 take a break.

4 (A break was taken.)

5 BY MR. BALICH:

6 Q. welcome back, Dr. Bernstein.

7 A. Thank you.

8 Q. Before the break we were talking about  
9 paragraph 62 of Mishra and whether or not Mishra  
10 itself provided a figure that showed a single  
11 transistor with a dual-gate structure.

12 And I think the answer was no, that one  
13 would have to take one of the structures that Mishra  
14 discloses and modify it in order to get the dual-gate  
15 structure that Mishra suggests in paragraph 62.

16 Do I have that right?

17 A. You have that basically right. We still  
18 have looming the -- what I pointed here, the Infineon  
19 theory about any field plate that is connected to the  
20 source. I did not take that position.

21 I'm just saying that this is a position,  
22 in which case, it might read on this. However, I was

1 taking the position to combine it with Ren to get to  
2 that conclusion.

3 Q. Right. And, obviously, you understand  
4 that in the context of an IPR one must look at the  
5 prior art based on the eyes of a person of ordinary  
6 skill at the time of the invention; is that correct?

7 A. Can you say that again?

8 Q. Sure. In the context of an IPR where --  
9 the law instructs us to read the prior art through  
10 the eyes of a person of ordinary skill, correct?

11 A. Correct. That's the way I understand it.

12 Q. And, certainly, Infineon's infringement  
13 contentions did not exist back in 2006; is that  
14 right?

15 A. Okay. Yes. That is correct that there  
16 was no intention -- contentions ten years ago, 20  
17 years ago.

18 Q. Okay. And I just want to -- if you'd take  
19 a look at your report, which you're on -- if you  
20 would go to page 143 --

21 A. My 143 or your 143?

22 Q. The 143 in the bottom left corner.

1 A. Okay, yes.

2 Q. In paragraph 251 you state: "Mishra does  
3 not explicitly comment on the mode in which Q1  
4 operates in cascode embodiments"; is that right?

5 A. I believe that's exactly what I said  
6 before the break. Yes, he does not comment on  
7 whether it is -- what mode it is.

8 Q. Okay. Let's turn to a different exhibit,  
9 Exhibit 1020. That's probably in the binder --

10 A. It's not in my binder here -- oh, okay.

11 Q. Exhibit 1020 is a copy of -- and I'll read  
12 the publication number -- WO 2005/070009, correct?

13 A. That's what it says.

14 Q. And the first named inventor is Robert  
15 Beach, correct?

16 A. Where is Beach named? -- oh, Weiner -- oh,  
17 Robert Beach and Sam Weiner, yes.

18 Q. Okay. And you pointed out that the  
19 applicant is listed as International Rectifier  
20 Corporation, correct?

21 A. That's correct.

22 Q. And that's the same company that is the --

1 that's listed on the face of the '003 patent as the  
2 assignee, correct?

3 A. Yes.

4 Q. So if I refer to this document as Beach,  
5 will you understand that I'm referring to Exhibit  
6 1020?

7 A. I can do that.

8 Q. Okay. If you turn to page 25 of Beach  
9 you'll get to figure 5. Do you see figure 5?

10 A. Figure 5, yes.

11 Q. Figure 5 of Beach shows the dual-gate  
12 transistor, correct?

13 A. I didn't read the specification, but  
14 assuming 54 is, let's say, the source and 55 would be  
15 a gate since they -- ohmic contacts, it is labeled.  
16 They're both labeled ohmic contacts, O-H-M-I-C --  
17 would suggest that the two gates are labeled as --  
18 gates are in between. So it looks like two gates  
19 between what could be a source and a drain.

20 Q. And, in fact, in figure 5 there's the word  
21 "gates" with two arrows up pointing to 50 and 52,  
22 correct?

1           A.     I think I said that, yes.

2           Q.     Oh, sorry. And both gates 50 and 52 are  
3 enhancement mode gates; is that right?

4           A.     Oh, I'm not going to commit to what -- if  
5 they're both enhancement mode -- I didn't -- that  
6 you'd have to read in the specification based on how  
7 it's, you know, laid out.

8                   Can you point to me in the text where he  
9 tells you that?

10          Q.     Hold on. Let's just still take a look at  
11 figure 5.

12          A.     Okay.

13          Q.     The structure of both gates in figure 5  
14 look to be the same, correct?

15          A.     Well, from the size. But if these are  
16 gallium nitride -- oh, gallium nitride. So generally  
17 gallium nitride are not doped (sic). So if they're  
18 the same thickness -- that's AlGa<sub>N</sub> -- AlGa<sub>N</sub>  
19 thicknesses and they were cut down.

20                   So -- okay. It's not clear if they --  
21 whether it's enhancement or depletion mode. You'd  
22 have to measure it basically or it has to be

1 specified somewhere, but generally it could be either  
2 or depending on the thicknesses, as we said.

3 Q. And if you go to page 1 of Beach -- sorry  
4 -- page 2 -- the title of Beach is Enhancement Mode  
5 III-Nitride FET, correct?

6 A. Okay. That's what it sounds like.

7 Q. And if you go to paragraph 46 --

8 A. Okay.

9 Q. -- the second sentence of paragraph 46  
10 says: "By providing a recessed gate contact on AlGaN  
11 layer 16, the current voltage characteristics of  
12 device 31 are modified to obtain a normally (sic) off  
13 device rather than a normally (sic) on device"; is  
14 that right?

15 A. That's what it says. That's actually very  
16 consistent with Beach -- I mean, with Ren as we  
17 pointed out. He says a thinner aluminum nitride will  
18 make it enhancement mode and thicker will make it  
19 depletion mode.

20 So he says you're making it thinner to  
21 make it -- so he's consistent with Ren.

22 Q. Okay. So figure 5 shows two enhancement

1 mode gates next to each other, correct?

2 A. I -- again, if the specification tells you  
3 that their intention is to have two enhancement modes  
4 -- much like as we said before, Bonn in his circuit  
5 with the mixers -- it looks like those both have to  
6 be enhancement modes because they were above zero.

7 Q. And you're not aware of any disclosure in  
8 Beach that shows an enhancement mode gate next to a  
9 depletion mode gate, right?

10 A. Again, it's been a long time since I went  
11 over these, and I did not review this before the  
12 deposition. So I can't say under oath what I know is  
13 to be written here or not written -- sorry.

14 Q. Sitting here right now with your memory as  
15 it is, you don't recall Beach disclosing a dual-gate  
16 transistor with an enhancement mode gate next to a  
17 depletion mode gate, do you?

18 A. I don't. I mean, if you want me to read  
19 through it a little --

20 Q. No. No. That's okay.

21 A. I'll have to rely on you. That's all that  
22 I can say. I do feel like I have an oath that --

1 Q. And you're not relying on Beach as  
2 disclosing an enhancement mode gate next to a  
3 depletion mode gate in your report, correct?

4 A. Right. I do not.

5 Q. Okay. Let's go back to your declaration.

6 A. Okay.

7 Q. Page 157.

8 A. Okay.

9 Q. And on page 157 this shows the Mishra/Ren  
10 combination; is that right?

11 A. Yes. I, in fact, said modified by Ren,  
12 yes.

13 Q. Okay. And you drew the claimed first  
14 portion of the transistor as a green box; is that  
15 correct?

16 A. A green box, yes. The green box is --  
17 surrounds channel. That is what I said is the --  
18 what did I call it? -- the enhancement mode.

19 Q. Um-hum.

20 A. Yes.

21 Q. In the green box of the first portion is  
22 under the green gate 62, correct?

1           A.     That's correct.

2           Q.     And gate 62, I think we discussed earlier,  
3 has a field plate, right?

4           A.     If it's described -- he describes the  
5 gamma gate, again, because it's a low voltage. I  
6 don't recall exactly why, but it's a field plate just  
7 that it's going in the wrong direction if you want to  
8 say it's a field plate. It's an overlap, but there's  
9 always overlaps when you put metal on material.  
10 There's always overlaps.

11          Q.     So would a POSA understand the overlapping  
12 portion as a field plate or would a POSA not  
13 understand the overlapping portion as a field plate?

14          A.     A POSA would understand a floating or  
15 connected structure between the source -- between the  
16 drain and the gate as a field plate. I don't know if  
17 we would necessarily call that a field plate facing  
18 the source because the voltage is much smaller.

19          Q.     Do you take a position one way or the  
20 other as part of your declaration as to whether  
21 that's a field plate?

22          A.     You know, I don't really. Again, I'd have

1 to read Ren again as to why he described the gate  
2 because here on figure 2, for instance, where  
3 definitely he described it as a field plate because  
4 it's in the right direction. And 46 is a field  
5 plate. It's on the right side.

6 He described that as a gamma -- I don't  
7 recall if there's a reason why he said it had to be  
8 -- I just know from manufacturing it's very hard to  
9 put metal without there being some overlap on the  
10 insulating (sic). So I don't know what that's  
11 representing to be honest.

12 Q. Okay. So is the portion of 62 that  
13 overlaps but does not touch the dielectric 64 -- does  
14 that have a specific purpose?

15 MR. MACDONALD: Objection. Form.

16 A. Do you mean -- well, the part directly  
17 under what is the gate we have the recessed aluminum  
18 nitride, as we described, which is the same as your  
19 Beach. He recessed the nitride to illustrate that  
20 it's an enhancement mode.

21 The fact that I drew channel which would  
22 be underneath what could be the field, I guess I

1 probably could have been more accurate on what would  
2 have been that small amount, but there is some  
3 fields, though, from that gate. So there would be  
4 some influence.

5 I guess it would act as a field plate in  
6 the fact that there would be some -- some of the  
7 voltage at that surface would affect channel  
8 underneath it, but most of the effect is going to be,  
9 obviously, right where the oxide is thin and the  
10 AlGa<sub>N</sub> is thinner.

11 The way HEMT channels work is the channel  
12 is usually there and you have to try to shut it off.  
13 You want to shut it off at the smallest point as  
14 possible so then the current doesn't flow. That's  
15 how you get the most efficiency in a HEMT by making  
16 the gate as thin as possible.

17 BY MR. BALICH:

18 Q. One question on how HEMT -- GaN HEMTs  
19 work. Is the channel only on or only off or is there  
20 partially on and partially off as well?

21 A. We saw actually in Bonn as an amplifier.  
22 It can work as an linear amplifier. Again, this is

1 just from my own experience, and I don't believe I  
2 put this in my report, but that's one of the  
3 properties of all transistors.

4 And there is we're able to say a  
5 subthreshold. Around the threshold region there's  
6 always some -- what can we call it? -- the  
7 conductivity is somewhat variable. I can increase  
8 the conductivity or decrease the conductivity linear.  
9 It's not exact on and off.

10 Q. It's like the simulation. There's a small  
11 region where it's partially conductive, but --

12 A. Exactly.

13 Q. -- but away from that region it's either  
14 conductive or not?

15 A. Right. In general it's -- I can show you.  
16 If you understand that -- in Ren there's a beautiful  
17 diagram from a physics point of view. I don't know  
18 what your background is.

19 But you can see there's a well that's  
20 labeled 250 and the goal when you change the voltage  
21 on the gate you increase or decrease the occupancy,  
22 how many electrons are in that well. So there's a

1 small number of electrons. It is high resistance,  
2 low conductive, and you get more and more electrons.

3 so you affect how many electrons feel or  
4 (inaudible). And that's how it works in a HEMT. In  
5 fact, that's why I think it was the -- what was the  
6 other reference? -- the Mizuta, whatever his name  
7 was.

8 Q. Mizuta.

9 A. Mizuta, and he was saying that you could  
10 in principle -- if I put the opposite voltage, I can  
11 even make it stronger on. So that's what he put it  
12 as a gate on the other side.

13 But, obviously, if he put the voltage on  
14 the other way, he couldn't turn it off. If you can  
15 modulate that amount of electrons, you're modulating  
16 the conductivity. There's a -- it's called a  
17 conductivity modulated transistor.

18 Generally, it's used in -- again, it's  
19 used as an amplifier. Then you want that linearity.  
20 If you're losing it as a switch like an on-off  
21 switch, then you want to go beyond. And we use all  
22 kinds of circuits like that.

1           Q.     Getting back to your report at page 157,  
2 you drew the second portion as a pink box; is that  
3 right?

4           A.     Yes, the second portion is the pink box.

5           Q.     And the pink box of the second portion is  
6 under what you've annotated as a second pink gate; is  
7 that right?

8           A.     I believe that's true. This is my  
9 Mishra/Ren combination. I'm now looking at that  
10 structure as Ren would as a single gate in the Ren --  
11 in the Ren configuration.

12          Q.     Right. And the structure that you've  
13 labeled as the second gate, that has itself a field  
14 plate; is that correct?

15          A.     Oh, if you want to say similarly to the --  
16 to that gamma plate. Again, it's in the wrong  
17 direction. So it's not really acting effectively as  
18 what you would like to see for a field plate.

19                 In principle, I think I called it a field  
20 plate in my -- field plate 66. He calls it the field  
21 plate. When implemented in a cascode, the question  
22 is, Did I call it a field plate attached to that

1 gate?

2 I don't remember if I committed to calling that a  
3 field plate.

4 we called it the field plate because  
5 that's the Mishra -- the whole thing is the Mishra  
6 field plate.

7 Q. So I guess my question is: How would a  
8 POSA understand that? would a POSA understand the  
9 portion of 66 that overlaps towards the source as a  
10 field plate or would a POSA not?

11 A. I think because it's facing toward the low  
12 voltage side a POSA can see this is a way for me to  
13 be able to connection (sic) to that so I can make a  
14 connection with vias -- I can use vias and I can  
15 connect to that piece of metal from another place.

16 So there would be good reason to have  
17 metal there. As a field plate it would really only  
18 be effective if it's on the drain side.

19 Q. And so is that why the pink box is sort of  
20 narrow because the gamma portion of 66 is not really  
21 influencing the field in the channel?

22 MR. MACDONALD: Objection. Form.

1           A.       The way I drew it over here, I separated  
2 out what could be the field plate or the wire from  
3 what is the gate, which is the part that would  
4 influence the channel.

5                   Similarly, I'm not sure about what the use  
6 of that gamma on the left side is, other than it  
7 obviously has some effect on the channel. It would  
8 be the same thing here except there's no channel.

9                   It's just something that would add  
10 capacitance perhaps, but it's not protecting anything  
11 because the voltage here, as Mishra pointed out, is  
12 going to be limited to the threshold voltage of that  
13 second transistor in my Ren reading.

14                   BY MR. BALICH:

15           Q.       Got it. Why did you show the first  
16 portion and the second portion different with respect  
17 to that overhanging portion towards the source side?

18           A.       You know, I don't think I meant anything  
19 more than that, then just saying that that was the  
20 channel because there is some influence.

21                   I'm making the gate thinner, but obviously  
22 where the direct connection is over that thin oxide

1 in that portion there would be a thick oxide and  
2 whatever is separating it. So it's not going to be  
3 nearly as effective as here, but it could be some  
4 influence depending on the gate.

5 I don't know why -- to be honest, it's --  
6 I don't know. It's all a cartoon anyway.

7 Q. You mentioned that whether something acts  
8 as a gate or not in part depends on the thickness of  
9 the oxide layer underneath it; is that right?

10 A. I did mention -- come to think of it,  
11 depending on the conductivity of the AlGaN layer, you  
12 know, because I see that I did notch it down earlier  
13 -- so we'll call that whole thing a channel. There  
14 will be some influence even if it's not from this  
15 gamma, but there will be still some influence of what  
16 the voltages are.

17 It's going to be a -- you know, field  
18 lines are always very -- you know, you have to  
19 predict those and whatever, but it's not meant to be  
20 taken too literally.

21 Q. Okay.

22 A. So what was your question again? I'm

1   sorry.

2           Q.     Let me ask a different question.  Other  
3   than the notch in the AlGaN layer, I don't -- have  
4   you -- strike that.

5                   Have you modified Mishra's figure 5 in any  
6   other way other than the notch in the AlGaN layer?

7                   MR. MACDONALD:  Objection to form.

8           A.     well, if you notice there's a little  
9   yellow, so we did add a little insulator to make it  
10  like Ren's insulating gate AlGaN.

11                   And the idea is we have a thin oxide under  
12  the green gate and a thicker oxide under the other  
13  gate -- thicker AlGaN and a thinner AlGaN to show one  
14  in depletion mode and one in enhancement mode.

15                   BY MR. BALICH:

16           Q.     Did you modify at all the spacing between  
17  the structure labeled 66 and the AlGaN layer?

18           A.     I believe this is just exactly from figure  
19  5.  So I didn't try to make any other distinctions.  
20  I'm not making any commitments to how thick that is.

21           Q.     Sure.  How did you know that the pink  
22  structure would act as a gate?

1           A.     well, that's part of a motivation to  
2 combine with Ren because Ren shows us very nicely  
3 that exact structure.

4                     And I just think it's obvious to combine a  
5 simple -- if you see that structure and you want to  
6 make that into a gate -- and the same POSA would look  
7 at Ren and says, hum, I have metal, I have an  
8 insulator, a gate dielectric, and then I have my  
9 AlGaN and then my GaN. So that's exactly what you  
10 have.

11                    So it seems to me he's exactly drawing for  
12 us what Ren shows, and Ren's pictures are certainly  
13 out of proportion just as these pictures are. His  
14 looks like a very thick dielectric. So it looks  
15 almost identical. I look only at that pink region  
16 and I look at Ren. So I said, oh, it's a beautiful  
17 combination.

18           Q.     would POSAs have done modeling in order to  
19 design the thicknesses of the insulating layers with  
20 respect to the other components of the transistor?

21           A.     Again, this is outside of my report.  
22 You're asking me to opine on what people do. I can

1 certainly say that in the academic world where we do  
2 lots of modeling because we don't have much to  
3 manufacturer, you know, modeling is a critical part  
4 of any kind of design but especially when it comes to  
5 these kinds of transistors.

6 Q. Let's -- we're going to try to use our  
7 iPad for this next one. If you could scroll down to  
8 the last document on the left-hand side. So it  
9 should be 2006 --

10 A. I think I have 2006.

11 Q. I can't imagine that you do.

12 MR. MACDONALD: No. 2006 would be not  
13 something you would have. I don't know what that is.

14 A. Okay.

15 BY MR. BALICH:

16 Q. So click on that. And so then you can use  
17 the arrow to hide, and then there's zooming in and  
18 zooming out. There's -- it doesn't work that way,  
19 unfortunately, but next to the -- near the top  
20 there's plus and minus buttons.

21 A. Okay. Oh, yeah, that's my good friend  
22 Mil'shtein. He's a big Israeli.

1 Q. And we're going to do our best to use the  
2 iPad, but let me know if you have any trouble because  
3 I appreciate it's very small.

4 THE WITNESS: He'll be very happy to have  
5 people reading his papers.

6 MR. MACDONALD: Are we entering this as an  
7 exhibit?

8 THE WITNESS: I have seen this before.  
9 I'm pretty sure I've seen this before. It's one of  
10 our exhibits. I know that I've seen this --

11 MR. MACDONALD: Okay.

12 THE WITNESS: -- because I looked at this  
13 in my own background research.

14 MR. BALICH: And so, Luke, this is on  
15 Agile Law for you, and so this will be an exhibit to  
16 this deposition, 2006.

17 (Exhibit Number 2006 was marked for  
18 identification and was retained by counsel.)

19 BY MR. BALICH:

20 Q. All right. Dr. Bernstein, you mentioned  
21 that you're familiar with Dr. Mil'shtein, right?

22 A. I'm familiar with him and his work and we

1 actually made him an associate faculty (sic) in our  
2 department.

3 Q. And you mentioned that you've, in fact,  
4 seen this particular article before; is that correct?

5 A. That is correct. It's very familiar to  
6 me. I don't remember exactly when I saw it, but  
7 fairly recently in my own --

8 Q. Okay.

9 A. Yeah.

10 Q. And just to identify it, if you look on  
11 the first page, Exhibit 2006, there's a publication  
12 from the Microelectronic Journal from 2005; is that  
13 right?

14 A. That's correct.

15 Q. And the first named author is S.  
16 Mil'shtein, correct?

17 A. Samuel.

18 Q. And if I refer to the document as  
19 Mil'shtein, you'll understand that I'm referring to  
20 Exhibit 2006, correct?

21 A. Yes. You don't often get your friends'  
22 papers. Okay.

1 Q. Okay. So now appreciating that it might  
2 have been some time since you've seen this last,  
3 always feel free if you need to read it, read it.  
4 But I'm going to direct your attention to the second  
5 of the three pages to the figure, figure 1. And  
6 figure 1 has a label. It says tuned gate bias pHEMT,  
7 correct?

8 A. That's correct.

9 Q. And so figure 1 shows a dual-gate  
10 transistor; is that right?

11 A. That is right. As I recall, he was  
12 worrying about the -- how -- what's the optimal field  
13 plate to put on this.

14 Q. Yep. And --

15 A. The other thing is I know he only works in  
16 gallium arsenide. I see that this is all gas --

17 Q. And then on page 302, that's the second of  
18 three pages, there's a paragraph near the end of the  
19 column. It starts, "we designed and modeled."

20 Do you see that paragraph?

21 A. Yes.

22 Q. And it states, "we designed and modeled

1 [11] a novel TGB pHEMT using" --

2 A. Silvaco.

3 Q. -- "Silvaco ATLAS finite-point simulation  
4 software."

5 Did I read that correctly?

6 A. You did.

7 Q. Thank you for that assistance. Is the  
8 Silvaco ATLAS software one that you're familiar with?

9 A. I've never used these myself, but those  
10 are well-known device simulation software.

11 Q. Okay. And then if you look at the top of  
12 the next column on the same page --

13 A. Excuse me. Can we just look to where he  
14 defined TGB?

15 Q. Sure.

16 A. What is TGB gate? Tunable gate -- oh,  
17 that must be tunable gate bias, TGB. There you go.

18 Q. That makes sense actually because that's  
19 what I'm going to ask you about.

20 A. Okay. I think he was presenting. He had  
21 an invention here, I guess, for a tunable gate bias.

22 Q. Yep. So at the right column on page 302

1 -- that's the middle of the three pages -- you see  
2 the paragraph that starts, "The proper biasing  
3 condition"?

4 A. Yes.

5 Q. And Mil'shtein states, "The proper biasing  
6 condition at the second gate was determined through  
7 trial and error"; is that right?

8 A. That's right.

9 Q. And we've discussed biasing before with  
10 respect to Bonn, I think, right?

11 A. Um-hum. Biasing simply means putting a  
12 voltage.

13 Q. Perfect. And it's putting a voltage with  
14 a -- an RF signal, right?

15 A. Usually, a bias means a DC signal. It  
16 just means a voltage.

17 Q. No, no, no. The bias is a DC signal, but  
18 you're using the bias to increase the voltage of an  
19 RF signal; is that right?

20 A. I think what he's showing here is he's  
21 putting a bias on the second gate which would be the  
22 field plate and the voltage is the -- the RF is

1 coming in on the first gate.

2 So he's showing the field plate how it  
3 affects the gain of that transistor and the operation  
4 of that transistor by properly biasing condition. So  
5 you put the -- the AC signal is coming on gate 1 and  
6 the DC signal is on gate 2.

7 Q. Let's go to the -- the last page, 303, and  
8 I want to direct you to the paragraph that says  
9 "Current iteration."

10 Do you see that?

11 A. Yes. "Current iteration of the design,"  
12 yeah.

13 Q. And so in the middle of that paragraph  
14 there's a sentence that says, "In addition, pumping  
15 the input signal."

16 Do you see that?

17 A. Yes.

18 Q. And that sentence reads, "In addition,  
19 pumping the input signal to both gates will, in our  
20 opinion, reduce the equivalent RF capacitance of the  
21 gate."

22 Do you see that?

1           A.     Yes.

2           Q.     So does that suggest that Mil'shtein is  
3 putting the input signal with both gates with just  
4 different biasing on the second?

5           A.     That's a good question. Is he answering  
6 just through his simulations? well, they do trial  
7 and error in simulations. He's a very big simulation  
8 guy. Let me read this again, "In addition, pumping  
9 the input signal to both gates."

10                   It sounds like he's putting -- he's using  
11 these two gates together as a single gate.

12           Q.     Right.

13           A.     So to reduce the capacitance between the  
14 gates. That's what it looks like.

15           Q.     Right. So with that in mind, let's go  
16 back to 302.

17           A.     And I don't know if that's with or without  
18 a bias. That's interesting, that he's biasing and  
19 putting a signal on. That's what I don't know. Did  
20 he say here?

21           Q.     Yeah, I think so. Let me ask you some  
22 questions that might go through that.

1           A.     Well, again, I may be familiar with this  
2 and familiar with him, but it doesn't mean I read it  
3 in detail here.

4           Q.     Okay. So if you go to the second page  
5 there's a -- on the right-hand column there's a  
6 paragraph that says, "Figure 3 compares the I-V  
7 curves" --

8                     Do you see that?

9           A.     Yes.

10          Q.     -- "for the TGB or tunable gate bias  
11 pHEMT" and then comparing that with a single gate  
12 pHEMT of the same dimensions.

13                     Now, obviously, I didn't read that  
14 verbatim.

15          A.     You read it pretty right.

16          Q.     Okay.

17          A.     Do you want to look at figure 3?

18          Q.     Yes.

19          A.     Okay. So these are the I-V  
20 characteristics, the drain current versus the drain  
21 bias voltage. So this is -- and they call this I-V  
22 characteristics.

1           And just to answer your previous question,  
2 the curves in the beginning, that's as you turn on.  
3 That's the threshold. That's why you can get like a  
4 linear signal by going up and down on the --

5           Q.     Close to that threshold?

6           A.     Right. Close to that threshold you'll get  
7 just the resistor.

8           Q.     Okay.

9           A.     They call it transconductance, is the  
10 official term.

11          Q.     So Mil'shtein is comparing his TGB pHEMT  
12 with a single gate pHEMT of the same dimension,  
13 right?

14          A.     That's what it looks like he's doing.

15          Q.     Okay.

16          A.     And the dots are -- oh, standard HEMT is  
17 with the dots without his second gate and the solid  
18 lines are TGB HEMT. So he's showing in general you  
19 get more transconductance on the standard HEMT.  
20 okay?

21                 MR. MACDONALD: Counsel, I'll let this go  
22 on for a bit, but the witness already indicated he

1 hasn't read this carefully, not in a while. And so I  
2 just don't see the relevance here.

3 MR. BALICH: well, he said he was familiar  
4 with Mil'shtein and his work.

5 MR. MACDONALD: Right, but we're here to  
6 talk about his declaration. So let's just try get to  
7 that, please.

8 MR. BALICH: Sure. Sure.

9 BY MR. BALICH:

10 Q. So in that paragraph that starts off with  
11 figure 3, Mil'shtein discloses a current gain of  
12 nearly 16 gigahertz for the normal HEMT.

13 Do you see that?

14 A. Okay. Generally, we don't talk about gain  
15 in terms of hertz. Let me see this again. "Figure 3  
16 compares the I-V curves to the TGB pHEMT with a  
17 single gate pHEMT of the same dimension."

18 Curves correspond to gate voltage biases  
19 of 0.2, 0.4, 0.6. These are biases on the gate.

20 "Compared with the regular HEMT the TGB  
21 transistor carries more evenly spaced and better  
22 saturated curves, which corresponds to improved early

1 voltage" -- oops.

2           So he was trying to say that the early  
3 voltage is the -- when you draw a line from the drain  
4 down to here and he's saying that it's straighter.  
5 So that's his goal. It may be less gain, but it  
6 gives a straighter characteristic. That's what he's  
7 optimizing here.

8           So -- so what -- what are we getting at  
9 here?

10       Q.     So Mil'shtein says, "Unity current gain of  
11 16 gigahertz for the normal HEMT"; is that right?

12       A.     It's strange because gain is not mentioned  
13 in hertz, right? That's why it's interesting.

14           "Modeling of S-parameters defined the  
15 magnitude of the S21" -- that's the parameter of the 4  
16 -- whatever. That's the S-parameter as they call it  
17 -- "as a unity current gain of nearly 16 gigahertz  
18 for the normal HEMT."

19           That's very interesting. What do they  
20 mean a unity current gain of -- unity means one, a  
21 current gain of one. Unity means a current gain of  
22 one. Does he mean at 16 gigahertz? I think that may

1 be an awkward sentence.

2 "Modeling of S-parameters defined the  
3 magnitude of the S21 as unity current gain of nearly  
4 16" -- why did he use "of"? I don't understand what  
5 he means by that. I'm sorry.

6 Q. well, let's maybe read the rest of that  
7 paragraph and --

8 A. "TGB device with no bias differential and  
9 the RF input injected into" -- differential meaning  
10 the difference between that and the bias, I guess --  
11 "both gates results in a unity gain limit of about 9  
12 gigahertz."

13 Oh, I understand. That's the cutoff  
14 frequency. So he's talking about usually what time  
15 he goes to gain. There's a certain gain. Like we  
16 see there's a higher gain and at what frequency does  
17 the gain cut off to be a unity gain. That's the  
18 standard thing.

19 when it's a unity gain it's basically not  
20 an amplifier, as we were saying before. Unity gain  
21 means no amplification. More than one is good. So a  
22 higher frequency means the higher frequency for the

1 unity gain.

2 16 gigahertz is higher so it's better,  
3 let's say, more higher bandwidth than the unity gain  
4 of 9 gigahertz. That's the bandwidth. Now I  
5 understand.

6 So the TGB device with the bias  
7 differential and RF injected into the Schottky gate  
8 yields the worst results with the unity gain limit of  
9 only about 5.5 gigahertz. He didn't say only, but --  
10 so, yeah. He's showing his invention gets a better,  
11 higher bandwidth.

12 Q. So would you interpret that as when you  
13 put the RF into just the first gate and not the  
14 second one, that's the worst results?

15 MR. MACDONALD: Objection. Relevance.  
16 Foundation. He's not looking at this reference.  
17 It's not in his report, Jason. This is going on a  
18 long time.

19 A. I think before he gets to the conclusion  
20 my feeling is he's putting DC voltage on gate 2 and  
21 showing how the DC voltage on gate 2 affects the  
22 transconductance. More than that, I don't know what

1 we're getting at.

2 MR. BALICH: Okay. I'll pass the witness  
3 for any questioning you might have.

4 MR. MACDONALD: Okay. I'll take a break.  
5 (A break was taken.)

6 EXAMINATION BY COUNSEL FOR THE PETITIONER  
7 BY MR. MACDONALD:

8 Q. Dr. Bernstein, do you recall discussing  
9 with counsel the simulations you prepared for your  
10 declaration?

11 A. Yes, I recall.

12 Q. And let's go to paragraph 66 of your  
13 declaration.

14 A. Yes.

15 Q. And this paragraph describes those  
16 simulations, correct?

17 A. It looks like it. I don't know where we  
18 start, but it looks like I'm talking about my  
19 simulations, yes.

20 Q. Do you see it says about five lines up  
21 from the bottom of page 43, "Although a POSITA at the  
22 time of the '003 patent would have readily understood

1 these principles, to further illustrate this concept,  
2 I simulated the normal behavior of a cascode  
3 amplifier with a first enhancement mode gate and  
4 second depletion mode gate using the below example  
5 circuit in LTspice version 17.2.4 for MacOS"?

6 A. Yes.

7 Q. Dr. Bernstein, what is the purpose of the  
8 simulations that you developed for your declaration?

9 A. As I said, just to simulate the normal  
10 behavior. When we're talking about cascodes, most  
11 people, especially who are not engineers, are not  
12 familiar with how a cascode works in general, even  
13 engineers.

14 Even someone who can be an electrical  
15 engineer, it's not such a normal device. So it's  
16 good to simulate it so we all understand how a  
17 cascode system works.

18 Q. And do you recall you told Mr. Balich that  
19 the transistors you included in your simulation were  
20 not three nitride transistors?

21 A. That's correct. They were both silicon  
22 devices.

1 Q. Was it important to the purpose of your  
2 simulation whether or not those transistors were or  
3 were not three nitride transistors?

4 A. For the purpose of showing how a cascode  
5 works, it makes no difference, just to see how the  
6 principle of the cascode -- the I-V -- the I-V  
7 characteristic of a typical cascode configuration.

8 Q. And do you recall, Dr. Bernstein, that you  
9 discussed whether or not the transistors you included  
10 in your simulation were wired?

11 A. He asked me if they were -- if I -- I  
12 don't remember exactly what he asked, but I just put  
13 them in a simulation. I didn't make any -- I didn't  
14 put any other parasitic -- that's what I assume he  
15 meant.

16 I didn't put any parasitic elements other  
17 than what comes with the normal simulation. So I  
18 just connected them together.

19 Q. You connected them together with wires.  
20 Is that what you mean?

21 A. Well, it's a simulation. Simulation just  
22 is one node connected to the other node. So the

1 drain of the J1 would be connected to the source of  
2 the M2 with no intermediary inductances --

3 (Whereupon, Madam Reporter asked for  
4 clarification from the witness.)

5 A. So the drain of the M2 is connected to the  
6 source of the J1 with no intermediary elements.

7 BY MR. MACDONALD:

8 Q. And that connection is a wired connection?  
9 I'm just trying to clarify.

10 A. Well, it's a simulation. So it's all  
11 electronic, but it would be as if completely wired  
12 with zero resistance, as if.

13 Q. Okay. And you testified that that  
14 connection was not a merged transistor, correct?

15 A. I testified that they were tested as if  
16 two separate elements -- so, again, it's a  
17 simulation.

18 So since they're both -- I don't think I  
19 commented if they were merged -- or maybe he asked if  
20 they were merged, but they certainly -- I don't know.  
21 I mean, they could be on the same piece of silicon  
22 since they're both silicon devices.

1 I didn't comment on -- I said I -- I just  
2 put them together in a simulation. I don't know that  
3 there would be any difference in behavior if they  
4 were merged or not merged as far as the simulation is  
5 concerned. So if I used the word "wired" -- it means  
6 connected -- it is a simulation.

7 Q. In your view is there a difference in  
8 behavior if the connections between the two  
9 transistors were wired versus if they were merged?

10 A. By the way I did my simulations, it  
11 wouldn't make any difference. I'm pretty sure even  
12 in the -- in Bonn he says they could be wired, but it  
13 takes up less area.

14 So I'd have to think about that more if  
15 there is an actual difference practically from how  
16 the behavior would work, but off the top of my head I  
17 think the electrical characteristics don't care if  
18 they're wired or if they're on the same piece of  
19 material.

20 Q. Okay. Dr. Bernstein, do you remember  
21 talking about figure 5 of Mishra?

22 A. Yes.

1 Q. Okay. And let's look at figure 5, please.

2 A. Okay. I have it in my report here.

3 Q. Okay. Do you see structure 66 in figure  
4 5?

5 A. Yes.

6 Q. And you referred to structure 66 as a  
7 source connected field plate today?

8 A. Yes.

9 Q. Let's please look at paragraph 29.

10 A. Yes.

11 Q. Do you see it says, "In still other  
12 embodiments the field gate can be connected to the  
13 source contact"?

14 Do you see that?

15 A. Yes.

16 Q. And do you see in paragraph 63 --

17 A. There they call it a field gate. Here  
18 they call it a field plate.

19 Q. Dr. Bernstein, I haven't asked a question  
20 yet.

21 A. Sorry.

22 Q. In paragraph 63 it says, "The field plates

1 can also have many different shapes and can be  
2 connected to the source contact in many different  
3 ways."

4 Do you see that?

5 A. Yes.

6 Q. And you mentioned paragraphs 29 and 63  
7 today, right?

8 A. I believe I did.

9 Q. And above in paragraph 62 do you see that  
10 it says, "One alternative arrangement comprises a  
11 single transistor with a dual-gate structure"?

12 A. Yes.

13 Q. Now, turning to figure 5 of Mishra again,  
14 how do paragraphs 29, 62, and 63 affect your  
15 understanding of how a POSITA would view structure 66  
16 in figure 5?

17 MR. BALICH: Objection to form.

18 A. Okay. Well, I think I stated and I made  
19 it very clear in my declaration that 66 is written  
20 here as a field plate.

21 But if you connect this to the source as  
22 it said in the many number of ways based on paragraph

1 63 I can -- with vias or some other way of getting a  
2 metal, I can make it a source connected field plate.

3 It's interesting. I just -- it just  
4 occurred to me on paragraph 29 he refers to it as a  
5 field gate, so in a sense there is a hint that it  
6 could be a gate. But there it would work.

7 And if I combine this with Ren, as I said,  
8 we have the structure exactly as Ren shows where you  
9 have a metal and insulator and AlGaN layer and then a  
10 GaN layer.

11 So that would be obvious to combine. I  
12 believe that's the approach I took in my declaration.  
13 So that field plate can also act at that gate as a  
14 second gate.

15 BY MR. MACDONALD:

16 Q. Now, moving on, Dr. Bernstein, to the  
17 Motivation to Combine Mishra and Ren on ground 3 of  
18 your declaration -- that begins on page 142 at  
19 paragraph 248 and the motivation ends on page 148 --  
20 actually, 149 of figures, but the paragraph on page  
21 134 begins paragraph 260.

22 And that is the end of your Motivation to

1 Combine Mishra and Ren analysis, correct?

2 A. Right. Before I get to claim 1, yes.

3 Q. And you remember talking about the  
4 combination of Mishra and Ren today?

5 A. Yes.

6 Q. Do you recall telling counsel that in the  
7 context of an IPR obviousness is from the viewpoint  
8 of a POSITA?

9 A. Yes.

10 Q. Is that the viewpoint you applied in your  
11 Motivation to Combine Mishra and Ren?

12 A. Certainly, I tried very hard to keep in  
13 mind that my whole report was based on how a POSITA  
14 would see these. That's why I have to make sure that  
15 it's a combination that is obviously easy to combine  
16 in the eyes of a POSITA -- POSA.

17 MR. MACDONALD: Okay. No further  
18 questions.

19 EXAMINATION BY COUNSEL FOR PATENT OWNER  
20 BY MR. BALICH:

21 Q. Just one question about paragraph 29 in  
22 Mishra, if you want to go there. So paragraph 29

1 begins with, "The field plate can be electrically  
2 connected to the gate contact and in some embodiments  
3 the field plate is formed as an extension of the gate  
4 contact while in other embodiments the field plate  
5 and gate electrode are formed during separate  
6 deposition steps."

7 And then in the next sentence Mishra  
8 mentions the field gate?

9 A. That's interesting, right?

10 Q. Do you think that's a typo? Do you think  
11 he just meant field plate?

12 A. I think the fact that I didn't even pick  
13 it up until this very moment probably suggests he  
14 sees field plate and gate the way sort of that I did.  
15 It's -- he's referring to -- he's referring to it as  
16 a field plate.

17 You know, again, these are words of art  
18 that are somewhat loose. And it does look like a  
19 gate in the way I showed figure 5, but that's why,  
20 again, I needed -- I did not say it was anticipatory  
21 by itself. I'm not saying it is, but it can be seen  
22 and modified with Ren to make a gate.

1           He probably saw is somewhat that way, too.  
2 He probably typed gate, plate. You know, all these  
3 words go back to vacuum tubes, believe it or not.  
4 They go back to the vacuum tubes. There was a plate.  
5 They called that a plate and the gate, so they just  
6 transferred language.

7           Q.     So do you think Mishra just made a mistake  
8 when typing field plate versus field gate?

9           A.     Had he said field gate in the first place  
10 instead of gate (sic) I think he probably would not  
11 have -- it wouldn't really change the meaning.

12                 And I think in his mind as -- you know,  
13 it's interesting he does use the word gate here as  
14 we're using it, but it might be -- I don't know. I  
15 don't know what was in his mind when he wrote this.

16           Q.     And what about a POSITA reading that? You  
17 mentioned that you hadn't picked up on that until  
18 now. Do you think a POSITA would have understood  
19 that as the field plate structure that he  
20 consistently describes?

21           A.     what languages is used for that piece of  
22 metal I don't think would make a difference in the

1 mind of a POSITA because it is what it is. You know,  
2 it's a piece of metal that goes over the conformal  
3 coating of the insulator.

4 I think a POSITA would see that this  
5 insulator is conformal. It's pretty much continuous  
6 and that's just the metal that goes on top of it.  
7 Probably a POSITA would overlook that word "gate" or  
8 "plate" as I did.

9 MR. BALICH: Okay. No other questions.  
10 We're done.

11 MR. MACDONALD: Okay. No further  
12 questions. Now we're off the record.

13 MADAM REPORTER: Mr. MacDonald, reading  
14 and signing?

15 MR. MACDONALD: Yes, he'll review.

16 MADAM REPORTER: would you like a copy,  
17 sir?

18 MR. MACDONALD: we'll wait for Jason to  
19 order it. He can review.

20 MADAM REPORTER: would you like a rough,  
21 Mr. MacDonald?

22 MR. MACDONALD: No, thanks.

(Signature having not been waived, the  
deposition of Joseph B. Bernstein, Ph.D. was  
concluded at 3:29 p.m.)

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C E R T I F I C A T E

I do hereby certify that I am a Notary Public in good standing, that the aforesaid testimony was taken before me, pursuant to notice, at the time and place indicated; that said deponent was by me duly sworn to tell the truth, the whole truth, and nothing but the truth; that the testimony of said deponent was correctly recorded in machine shorthand by me and thereafter transcribed under my supervision with computer-aided transcription; that the deposition is a true and correct record of the testimony given by the witness; and that I am neither of counsel nor kin to any party in said action, nor interested in the outcome thereof.

WITNESS my hand and official seal this

\_\_\_\_\_ day of \_\_\_\_\_, 2025.

Sherry L. Brooks

Notary Public

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|----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Exhibits</b>                                    | <b>0.4</b><br>183:19                                                                                                                                                                                               | <b>1019</b><br>23:7,10,13,17,18<br>24:5,9,14                                                  | 119:3 142:6                                                                                                                                      |
| <b>Exhibit 1003</b><br>3:10 8:3,6,11 33:2          | <b>0.6</b><br>183:19                                                                                                                                                                                               | <b>102</b><br>113:6,12,13 116:6,<br>18                                                        | <b>157</b><br>142:7,17,18,19<br>152:15,19 161:7,9<br>167:1                                                                                       |
| <b>Exhibit 1006</b><br>3:12 45:17,19 46:5          | <b>003</b><br>102:1,2 157:1<br>187:22                                                                                                                                                                              | <b>1020</b><br>156:9,11 157:6                                                                 | <b>16</b><br>159:11 183:12<br>184:11,17,22 185:4<br>186:2                                                                                        |
| <b>Exhibit 1007</b><br>3:14 103:21 104:2,<br>11,17 | <b>1</b>                                                                                                                                                                                                           | <b>103</b><br>117:5 118:3 122:19                                                              | <b>162</b><br>41:7,8,10                                                                                                                          |
| <b>Exhibit 1008</b>                                | <b>1</b>                                                                                                                                                                                                           | <b>108</b><br>117:10                                                                          | <b>169</b><br>8:20                                                                                                                               |
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| <b>Exhibit 1018</b><br>4:5 26:18,22 27:9,10        | 42:9,12,16,20,21,22<br>46:7 48:11,14 53:1,<br>21 54:6,14 55:20                                                                                                                                                     | <b>11(b)</b><br>105:3,18,20,21<br>110:19                                                      | <b>17.2.4</b><br>33:11 188:5                                                                                                                     |
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| <b>Exhibit 1020</b><br>4:12 156:9,11 157:5,<br>6   | 71:8,14 72:9,13,16<br>73:13 74:21 75:4,7,<br>14 79:5 83:2 91:7,<br>15,21 92:8 113:9<br>114:3,22 115:5,6<br>116:18 117:1<br>118:15,19,20 119:9,<br>11,15,16 122:8<br>124:12 134:2 159:3<br>176:5,6,9 179:5<br>195:2 | <b>12:17</b><br>103:6                                                                         | <b>182</b><br>9:1,6 142:15                                                                                                                       |
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| <b>0</b>                                           |                                                                                                                                                                                                                    |                                                                                               |                                                                                                                                                  |
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