

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AUSTRIA AG,
Patent Owner.

Case IPR2025-00094
U.S. Patent 8,264,003

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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Exhibit	Description
Ex-1001	U.S. Patent No. 8,264,003 (“the ’003 patent”)
Ex-1002	Prosecution History of the ’003 Patent (“Prosecution History”)
Ex-1003	Declaration of Joseph B. Bernstein, Ph.D. (“Bernstein”)
Ex-1004	Curriculum Vitae of Joseph B. Berstein, Ph.D.
Ex-1005	U.S. Patent Publication No. 2005/0189561 to Kinzer et al (“Kinzer561”)
Ex-1006	U.S. Patent No. 6,160,280 to Bonn et al. (“Bonn”)
Ex-1007	U.S. Patent No. 6,483,135 to Mizuto et al. (“Mizuto”)
Ex-1008	U.S. Patent Publication No. 2004/0041169 to Ren et al. (“Ren”)
Ex-1009	U.S. Patent Publication No. 2005/0051800A1 to Mishra et al. (“Mishra”)
Ex-1010	Excerpts Of Public Verified Complaint of Infineon Technologies Austria AG and Infineon Technologies Americas Corp. Under Section 337, Inv. No. 337-TA-1414 (July 26, 2024).
Ex-1011	Exhibit 17 to Public Complaint in Inv. No. 337-TA-1414
Ex-1012	U.S. Patent Publication No. 2002/0171096A1 to Wakejima et al. (“Wakejima”)
Ex-1013	U.S. Patent Publication No. 2005/0051796 to Parikh et al. (“Parikh”)
Ex-1014	U.S. Patent No. 7,800,131 to Miyamoto et al. (“Miyamoto”)
Ex-1015	U.S. Patent No. 7,548,112 to Sheppard (“Sheppard”)
Ex-1016	U.S. Patent Publication No. US 2007/0170463 to Ueno et al (“Ueno”)

Ex-1017	U.S. Patent No. 7,408,399 to Salato et al. (“Salato”)
Ex-1018	U.S. Patent Publication No. 2006/0113593 A1 to Sanking et al. (“Sankin”)
Ex-1019	B. M. Green et al., “High-power broad-band AlGa _N /Ga _N HEMT MMICs on SiC substrates,” in <i>IEEE Transactions on Microwave Theory and Techniques</i> , vol. 49, no. 12, pp. 2486-2493, Dec. 2001, doi: 10.1109/22.971640 (“Green”)
Ex-1020	International Patent Publication Number WO 2005/070009 (“Beach”)
Ex-1021	U.S. Patent No. 6,586,781 to Wu et al. (“Wu”)
Ex-1022	U.S. Patent Publication No. 2002/0167023 to Chavarkar et al. (“Chavarkar”)
Ex-1023	Bernstein JB, Gleason EF, Wetsel AE, Liu EZ, Wyatt PW. “Anomalous Behavior of Semi-Insulating Silicon Rich Amorphous Silicon Nitride.” <i>MRS Proceedings</i> . 1992; 284:113. doi:10.1557/PROC-284-113 (“Bernstein-SiN”)
Ex-1024	Tessmann, A., Haydl, W. H., Hulsmann, A., & Schlechtweg, M. (1998). High-gain cascode MMICs in coplanar technology at W-band frequencies. <i>IEEE Microwave and Guided Wave Letters</i> , 8 (12), 430-431 (“Tessman”)
Ex-1025	Potirakis, S. M., and Alexakis, G. E. (2005). An accurate calculation of Miller effect on the frequency response and on the input and output impedances of feedback amplifiers. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 52(8), 491-495. (“Potirakis”)
Ex-1026	J. Lerdworatawee and Won Namgoong, "Wide-band CMOS cascode low-noise amplifier design based on source degeneration topology," in <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , vol. 52, no. 11, pp. 2327-2334, Nov. 2005, doi: 10.1109/TCSI.2005.853585. (“Lerdworatawee”)

Ex-1027	Ko, B. K., & Lee, K. (1996). A comparative study on the various monolithic low noise amplifier circuit topologies for RF and microwave applications. <i>IEEE Journal of Solid-State Circuits</i> , 31(8), 1220-1225 (“Ko”)
Ex-1028	Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al., No. 3:24-cv-01553-SK, Dkt. No. 56, Order Staying and Conditionally Closing Case for Statistical Purposes (N.D. Cal. Aug. 27, 2024)
Ex-1029	LTspice cascode amplifier simulation
Ex-1030	LTspice cascode amplifier schematic
Ex-1031	LTspice cascode amplifier simulation data
Ex-1032	LTspice cascode amplifier graph

I. Introduction

Patent Owner repeatedly ignores the express teachings of prior art references Bonn (Ex-1006) and Mishra (Ex-1009). For Bonn, it contends “no credible evidence” supports Bonn’s dual gate transistor as a signal amplifier even though Bonn says to do exactly that: “the dual gate FET structure of the present invention can be tailored to provide superior performance . . . [for] high frequency signal amplification.” Paper 14 (POR), 17-19; Bonn, 11:26-37.

For Mishra, Patent Owner argues its “alternative [amplifier] arrangement compris[ing] a single transistor with a dual gate structure” has no effect because a POSITA would not have known how to implement this teaching. POR, 35-42; Mishra, [0062]. This fails on the facts and the law, because Mishra discloses more detail than the ’003 patent. *See Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 1471 (Fed. Cir. 1997) (prior art that provided “a level of detail similar to” the patent was enabling); *King Pharms., Inc. v. Eon Labs., Inc.*, 616 F.3d 1267, 1276 (Fed. Cir. 2010) (prior art need only disclose a limitation to the degree of specificity found in the patent to anticipate).

Patent Owner also repeatedly attacks positions the Petition did not take. Although Ground 2 implements Ren’s GaN approach for each gate of Bonn’s adjustable, dual gate transistor, Patent Owner illogically argues this fails because Ren lacks a dual gate. POR, 30-32. That was not the asserted ground. Patent Owner

then attacks the addition of Mishra to Ground 2 for the same reason—an allegedly missing dual gate amplifier—even though Ground 2 only relies on Mishra for its field plate. POR, 35-43.

Patent Owner makes vague assertions untethered to the claims that it was “difficult” to make GaN devices and the field retained a “strong element of trial and error.” POR, 32-35. This does not show nonobviousness. See *Volvo Penta of the Ams. v. Brunswick Corp.*, 81 F.4th 1202, 1212 (Fed. Cir. 2023) (rejecting unexplained assertion commercial success was tied to the claims). Moreover, a “strong element of trial and error” supports the Petition, not Patent Owner, because “it is not inventive to discover the optimum or workable ranges by routine experimentation.” *In re Applied Materials, Inc.*, 692 F.3d 1289, 1295 (Fed. Cir. 2012).

For these and other reasons, the Patent Owner Response fails, and the claims are obvious over the asserted grounds.

II. Level of Skill in Art

Petitioner and Patent Owner apply the same definition of a POSITA. Paper 1 (“Petition”), 5; Ex-2004, ¶39.

III. Bonn Expressly Teaches to Implement its Dual gate Transistor as an Amplifier, Which Would Have Made Modified Figure 1 Obvious (Grounds 1-2)

Bonn teaches to use its dual gate transistor for “high frequency signal amplification.” Bonn, 11:26-37; Petition, 22-38, 49-50; Ex-1003, [094]-[109], [156]. Patent Owner has no basis to disregard this. POR, 10-13, 17-19. The proposed modifications of Figure 1 do not make Bonn’s device “inoperable for its intended purpose.” *See* POR, 3-4, 15-18. Rather, the Petition proposes a simple circuit that implements Bonn’s explicit intent—high frequency signal amplification. Petition, 22-38, 49-50; Ex-1003, [094]-[109], [156].

This readily distinguishes the Petition from Patent Owner’s caselaw. *See* POR, 4, 15-16 (citing *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984); *Medtronic, Inc. v. Teleflex Innovations S.a.r.l.*, 69 F.4th 1341 (Fed. Cir. 2023); *In re Ratti*, 270 F.2d 810 (C.C.P.A. 1959); *Henny Penny Corp. v. Frymaster*, 938 F.3d 1324, 1331-32 (Fed. Cir. 2019)). *In re Gordon* found the asserted reference “teaches away” from the modification. 733 F.2d at 902. *Medtronic* held the same. F.4th at 1349. *In re Ratti* found a reference “points away” from a combination that altered “basic principles.” 270 F.2d at 813. And *Henny Penny* held a reference did “not contemplate” the proposed modification. 938 F.3d at 1331-32. Unlike those references, Bonn teaches *towards* the proposed high-frequency amplification. Bonn, 11:26-37.

The law has long recognized an express teaching, suggestion, or motivation can establish obviousness while avoiding hindsight. *In re Kahn*, 441 F.3d 977, 987-88 (Fed. Cir. 2006). Although the Supreme Court rejected a rigid teaching-suggestion-motivation test as the only way to establish obviousness, it found that test “helpful” as one way to do so. *KSR Intn’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 401-402, 415-418 (2007). The MPEP continues to endorse this approach. MPEP § 2143.01 (citing *In re Kahn*).

Patent Owner does not dispute that Bonn teaches to use its dual-gate transistor for high-frequency signal amplification. POR, 18. Patent Owner instead criticizes the Petition for following that teaching to propose changes that alter the downconverter circuitry of Figure 1. POR, 15-18. But each modification merely implements Bonn’s instructions, resulting in a simpler circuit. Petition, 22-38, 49-50; Ex-1003, [094]-[109], [156].

A. The Petition implements Bonn’s signal amplifier and simplifies its circuit by removing components related to signal mixing (Grounds 1-2)

The Petition implements Bonn’s dual-gate, high frequency amplification embodiment within the context of the circuit of Figure 1. Petition, 22; Ex-1003, [096]-[097]. Every change simplifies Figure 1 by removing components that support signal mixing but which are unnecessary for dual gate amplification. Petition, 22-25; Ex-1003, [097]-[108]. That is the “articulable rationale” the Petition offers. *See*

POR, 10-13. Patent Owner hyperbolically characterizes these changes as “absurd” and doing “great violence” to Figure 1. POR, 13. Far from it. The result is a basic circuit that a POSITA would have encountered as an undergraduate. *See* Ex-2009, 73:12-74:21.

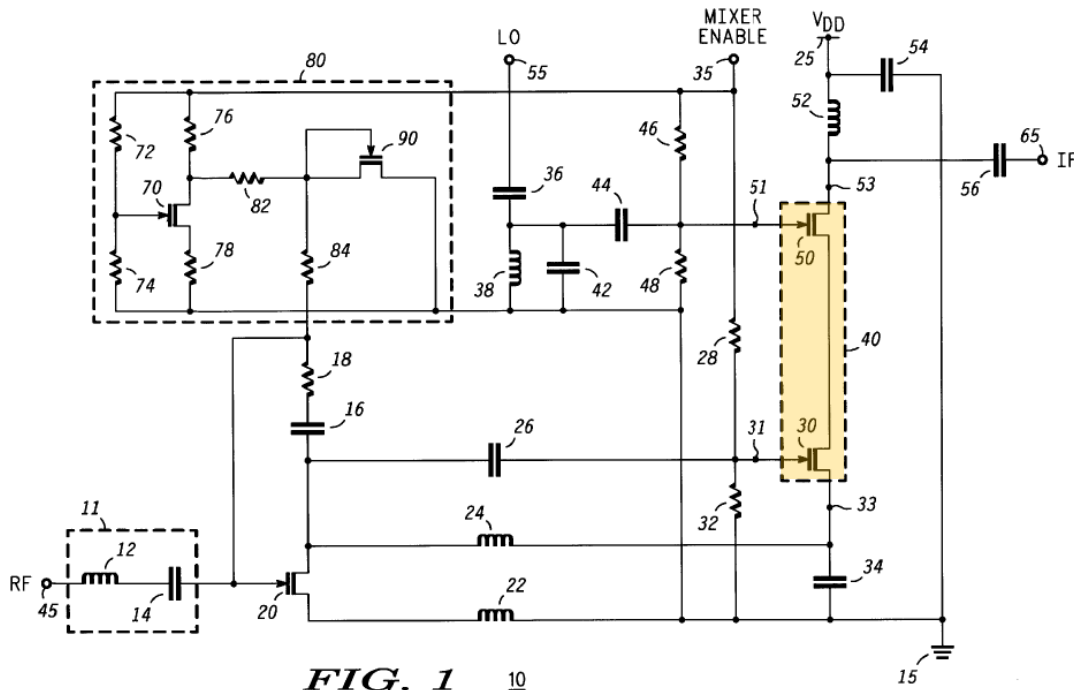


FIG. 1 10

Bonn Fig. 1 (annotated)

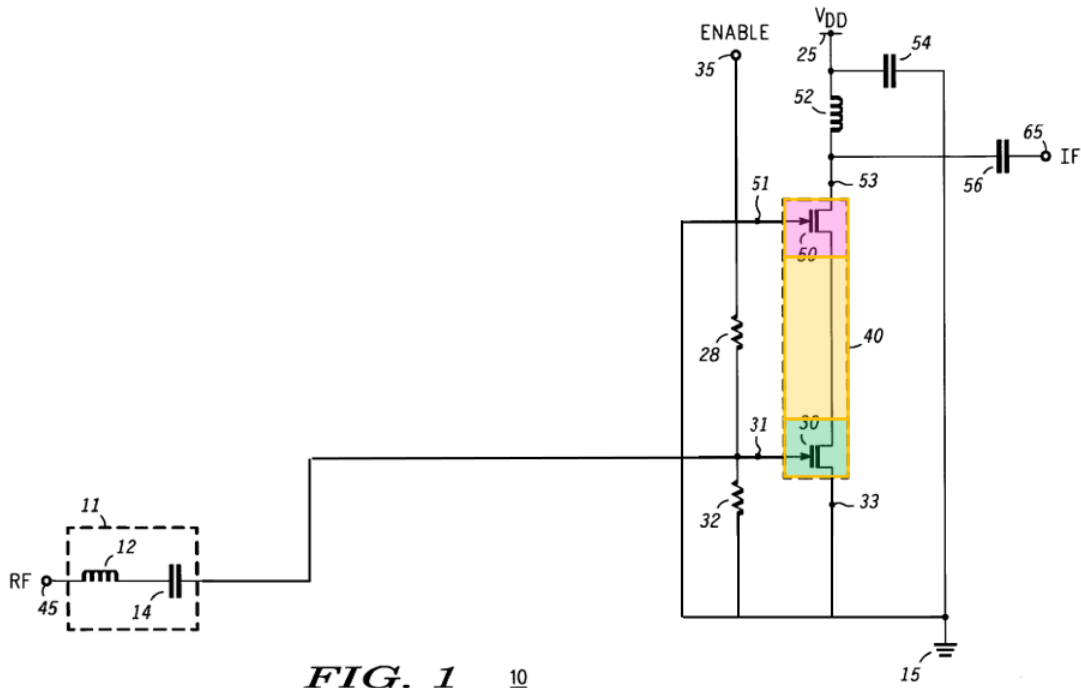


FIG. 1 10

Bonn, Figure. 1 (modified)

Bonn's downconverter mixes two signals, while amplification involves only one. Petition, 23; Ex-1003, [098]; Ex-2009, 73:12-74:21. The straightforward implementation of Bonn's teaching to use its dual-gate transistor for amplification removes the variable LO signal circuitry from Bonn's downconverter. Petition, 22-38, 49-50; Ex-1003, [094]-[109], [156]. Without a LO signal, the voltage divider at resistors 46 and 48 sets the second gate terminal to "a constant voltage at a value between V_{DD} and drain." Ex-1003, [104]. Bonn thus renders obvious the supposedly missing limitation—a constant voltage input—by teaching to amplify one signal, not two. See POR, 2-3, 11, 26-27. A POSITA would have then removed those resistors and set this voltage to zero because Bonn's second gate is in depletion mode, and

because it would have improved Miller feedback, amplification, and noise. Petition, 24-25; Ex-1003, [102]-[107]; Ex-2009, 85:12-91:2.

Bonn unmistakably teaches to use its dual-gate transistors, such as the transistor of Figure 7, as an amplifier. Bonn, 11:26-37; Ex-2009, 78:3-79:21. The fact that Bonn also discloses a single-gate amplifier, FET 20, does not negate this teaching. Patent Owner's contrary assertions fail. POR, 11-13, 24-25.

B. The Petition's proposed modifications would have increased signal amplification, reduced Miller feedback, and lowered noise, advantages which Patent Owner does not dispute (Grounds 1-2)

Shorting the second gate of Bonn's dual-gate amplifier to ground would have provided advantages over a single-gate amplifier, including increased amplification, reduced feedback, and lower noise. Petition, 24-25; Ex-1003, [102]-[107]. This would have been obvious because the second gate is in depletion mode. Ex-1003, [104]; Bonn, 8:51-9:4 Patent Owner never disputes those benefits. *See generally* POR; Ex-2004.

Patent Owner instead irrelevantly alleges that a different reference, Mil'Shtein (Ex-2006) teaches away from a constant voltage source in Bonn's modified Figure 1. POR, 27-29; Ex-2004, ¶¶110-116; see Ex-2009 at 185:13-186:1. But the doctrine of teaching away does not apply to Mil'Shtein, it only applies to the asserted references. *Tec Air, Inc. v. Denso Mfg. Michigan Inc.*, 192 F.3d 1353, 1360 (Fed. Cir. 1999); *In re Beattie*, 974 F.2d 1309, 1313 (Fed. Cir. 1992) (declarations opining on teaching

away irrelevant because they did not address the asserted art). Mil'Shtein fails to mention Bonn's circuit or transistor Bonn. Ex-2006. It presents a software model of a different circuit and different transistor. Ex-2006, 301-302. And the Petition did not even discuss Mil'Shtein, which was introduced by Patent Owner. Mil'Shtein is thus not probative. *Tec Air* 192 F.3d at 1360; *In re Beattie*, 974 F.2d at 1313.

Regardless, nothing in Mil'Shtein constitutes a teaching away from modified Figure 1. A reference does not teach away “if it merely expresses a general preference for an alternative invention but does not ‘criticize, discredit, or otherwise discourage’ investigation into the invention claimed.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.23d 1314, 1327 (Fed. Cir. 2009) (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed.Cir.2004)). That is the case here.

Mil'Shtein assessed one parameter, the unity limit, in four modeled amplifiers—single gate, dual gate with bias, dual gate without bias, and dual gate with the second gate connected to constant voltage. Ex-2006, 302; *see* Ex-2004, ¶116. The unity limit is a cutoff frequency above which there is no gain. Ex-2009, 185:13-186:1. Mil'Shtein found a constant voltage second gate produced “the worst” result on this specific outcome among those four models. Ex-2006, 303. Yet even that configuration amplified signals below 5.5 GHz. Ex-2006, 303. Mil'Shtein thus only expresses a preference for the other three approaches when evaluating one parameter—cutoff frequency. Ex-2006, 302. That is no teaching away.

Mil'Shtein does not address the benefits described in the Petition: increased signal amplification (e.g., below the cutoff), reduced Miller feedback, and lower noise. Ex-2006, 302; Petition, 24-25. Neither does Patent Owner. POR, 27-29. Those benefits stand un rebutted.

C. Bonn teaches to use Figure 7's dual gate as a signal amplifier (Grounds 1-2)

Bonn explains “the dual gate FET structure of the present invention can be tailored to provide superior performance . . . [for] high frequency signal amplification.” Bonn, 11:26-37. This discloses using Figure 7 for signal amplification. *Id.*; *see id.* 8:13-9:27. Bonn teaches individually adjusting “width, dopant concentration, and channel depth, under each gate of the dual gate FET” for different applications. *Id.* at 11:30-33. Bonn’s flexible disclosure contradicts Patent Owner’s assertion that Bonn’s Figure 7 is “tailor-made for use as a mixer.” POR, 18-19; Petition, 33, 53.

The Petition does not need to propose more specific modifications to Figure 7 to render signal amplification obvious. Bonn already discloses how to adjust gate parameters to achieve desired outcomes, and a POSITA would have had success doing so. Bonn, 8:13-9:27; Petition, 23, 33, 49, 53; Ex-1003, [098], [128]-[129], [156]. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *Applied Materials*, 692 F.3d at 1295 (quoting *In re Aller*, 220 F.2d

454, 456 (C.C.P.A. 1955)); *Pfizer Inc. v. Sanofi Pasteur Inc.*, 94 F.4th 1341, 1347-49 (Fed. Cir. 2024) (same).

Patent Owner misunderstands Bonn by contending Figure 7 has unequal current-capacity, which allegedly renders it unsuitable for amplification. POR, 19-24. Patent Owner relies on a preferred embodiment that configures the first gate with a lower current carrying capacity than the second. POR, 20-21. But obviousness is not limited to Bonn's preferred embodiment. *Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1372 (Fed. Cir. 2005) (error to limit prior art to a preferred embodiment); *FMC Corp. v. Sharda USA, LLC*, 145 F.4th 1326, 1334 (Fed. Cir. 2025) (anticipating embodiment need not be preferred). Instead, Bonn is applicable for all it teaches. *See AliveCor, Inc. v. Apple Inc.*, 130 F.4th 1006, 1015 (Fed. Cir. 2025); *In re Mouttet*, 686 F.3d 1322, 1331 (Fed. Cir. 2012); *Beckman Instruments, Inc. v. LKB Produkter AB*, 892 F.2d 1547, 1551 (Fed. Cir. 1989).

Bonn's non-conductive sections may alter current carrying capacity, but they are optional and "not intended as a limitation of the present invention." Bonn, 7:18-28, 9:12-27; Ex-2009, 96:7-98:6. They are individually adjustable under both gates, so some embodiments would not have had smaller current carrying capacity in the first gate. Bonn, 9:12-27, 11:26-37; Ex-2009, 96:7-98:6. Bonn even teaches embodiments with a *larger* current capacity in the first gate, the opposite of the preferred embodiment. Bonn, 7:23-28. For Figure 7, non-conductive sections "can

be formed” under either gate, both gates, or none, because they “can be individually adjusted.” Bonn, 9:12-27; Ex-2009, 96:7-98:6. Patent Owner cites no authority to disregard “the permissive word ‘can’ in describing the presence of the nonconductive sections” and limit Bonn to a preferred configuration. POR, 22. The law does not support that position. *Arthrocare*, 406 F.3d at 1372; *FMC Corp.*, 145 F.4th at 1334.

Bonn’s signal amplification embodiment applies to Figure 7. Bonn discloses just three dual gate structures. Bonn, 1:54-61 (Figs. 3-5, a first transistor), 1:65-67 (Fig. 7, a second transistor), 2:1-5 (Figs. 8-9 ,a third transistor). All three have adjustable non-conductive portions under both gates. Bonn, 7:18-28 (Fig. 3), 9:12-20 (Fig. 7), 10:66-11:7 (Fig. 8). While the current carrying capacity of the first gate may be smaller than the second in some embodiments of Figs. 3-5, it may also be larger. Bonn, 5:37-40 (smaller), 7:10-17 (smaller), 7:22-28 (larger). And Bonn never discusses the current carrying capacity of the gates of Figures 7 or 8-9. Bonn, 8:13-11:10. Thus, Bonn’s dual gate signal amplifier plainly includes Figure 7 and does not exclude it due to unequal current carrying capacity, as Patent Owner contends. POR, 19-22.

Patent Owner makes another error when contending Figure 7 is not obvious for signal amplification because it is suboptimal due to supposedly unequal current carrying capacity. POR, 22-24. Even if true (it is not), this is immaterial.

Obviousness does not require the best option, only a suitable one. *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197-98 (Fed. Cir. 2014); *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021); *Intel Corp. v. PACT XPP Schwiez AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023); *see In re Fulton*, 391 F.3d at 1200 (combination need not be the most preferred).

**D. Patent Owner’s attempts to discredit Dr. Bernstein fail
(Grounds 1-2)**

Dr. Bernstein possesses relevant expertise to the ’003 patent, which “relates to a transistor for use in high voltage, high speed switching applications” of power converters, including GaN devices, and purports to reduce the “Miller effect.” Ex-1001, 1:24-50, 3:28-30; Ex-1003, [008]-[025]; Ex-1004. He holds graduate degrees in Electrical Engineering from MIT. Ex-1004, [011]. His PhD in Electrical Engineering and Computer Science involved “high voltage device gate drivers to eliminate miller effect in high frequency high power energy converters.” Ex-1004, [015]. He is a university professor, “leads[s] an active research program in GaN device applications,” and holds “several patents related to GaN power device technology.” Ex-1004, [018], [023]

As of the earliest claimed priority of 2006, Dr. Bernstein far exceeded the parties’ definition of a POSITA: “a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design.” Ex-1003, [068]. Dr. Bernstein received his electrical engineering bachelor’s

degree in 1984 and his PhD in 1990. Ex-1003, [008]-[025]. He has designed semiconductor devices and taught their principles to students for more than thirty-five years. *Id.* He thus qualifies to testify as an expert here. *Kyocera Senco Indus. Tools Inc. v. Int’l Trade Comm.*, 22 F.4th 1369, 1376-78 (expert “must at least have ordinary skill”).

Although Dr. Bernstein honestly remarked he lacked extensive firsthand experience with downconverters and RF signal mixing applications, these statements enhance his credibility and are of no moment. Ex-2009, 44:16-17, 60:20-21, 72:20-21, 77:15-17. He does not need such expertise. The ’003 patent specification and claims never mention signal mixing. Ex-1001. And he does not base his opinion on Bonn’s signal mixing application.

Instead, Dr. Bernstein based his grounds on Bonn’s signal amplification embodiments. Ex-1003, [094]-[115]. He explained how to simplify Bonn’s signal mixing circuit by removing components that support mixing the LO signal, many of which Bonn explicitly identifies as relating to LO mixing. Ex-1003, [098]-[110]. And Dr. Bernstein proposed to remove single-gate amplifier FET 20 and associated components because it would not have been necessary in Bonn’s dual-gate amplifier embodiments. *Id.* His analysis does not require deep understanding of signal mixing, which is not part of his obviousness challenge.

Patent Owner gives no legally sufficient argument to give Dr. Bernstein's testimony "no weight." See POR, 14-15 (citing *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356 (Fed. Cir. 2008)). *Sundance* excluded a patent attorney who had no training or experience in the relevant technology from serving as technical expert. *Sundance*, 550 F.3d at 1361-64. That is far removed from the circumstances here. Dr. Bernstein's four decades of training and experience makes him "qualified in the pertinent art." *Id.* at 1363-64.

IV. It would have been obvious to implement Bonn's dual-gate transistor in GaN (Ground 2)

A. Patent Owner attacks positions the Petition did not take for Ground 2

Patent Owner misses the mark by repeatedly attacking positions the Petition did not take on the Bonn-Ren-Mishra combination. POR, 5-6, 30-46. This combination calls for modifying Bonn's individually adjustable GaAs dual gates in cascode, which have an enhancement mode first stage and depletion mode second stage. Petition, 48-57. It follows Ren's teachings to make enhancement and depletion mode GaN transistors because Ren explains that GaN performs better than GaAs, especially for high-frequency, high-temperature, and high-power applications. Petition, 50-54.

Patent Owner does not dispute those benefits. POR, 31-32 It instead argues "Ren has no disclosure of how to make a *dual-gate* GaN transistor" POR, 31

(emphasis original). That was never the combination. Bonn teaches individually adjusting the properties of each gate, and a POSITA would have made those individual gate adjustments using Ren's GaN techniques. Petition, 50-54. Patent Owner's critique fails to rebut the Petition. POR, 30-32. Ren's single-gate teachings apply to each gate in Bonn's individually adjustable dual gate transistor. Petition, 50-54.

Patent Owner fails to address that the combination adds Mishra's field plate to the Bonn-Ren gate to improve performance. Petition, 54-57. Patent Owner instead launches an eight-page attack alleging Mishra does not disclose a dual gate transistor. POR, 35-43. While that is wrong (*infra* Section V), it is immaterial to Ground 2. Patent Owner does not dispute the actual combination of Ground 2, which involved only Mishra's field plate. Petition, 54-57; POR, 35-43.

Patent Owner launches similarly misplaced critiques of Beach, Ueno, and Sankin (for all grounds) for not teaching a dual gate merged cascode with a first enhancement mode and second depletion mode stage. POR, 43-46; *see* POR, 7, 9, 29-30, 34, 43-45, 52, 55-57, 59, 66, 68-69, 70. Those references are not asserted in the combination. They illustrate background knowledge. Ueno, like Mishra, shows

GaN was known as a desirable GaAs substitute. Petition, 52.¹ Beach demonstrates that insulating dielectrics in enhancement mode GaN HEMTs were known, controlled leakage, and could be in dual gate devices. Petition, 51, 86, 101; Ex-1003, [228]. Sankin implemented known cascodes with first enhancement and second depletion mode stages, as did Salato (Ex-1017), and Bonn. Petition, 2, 5, 84. Those points remain unrefuted.

B. Patent Owner’s vague discussion of the state of the art fails to defeat Ground 2

Patent Owner asserts that GaN was an emerging technology in 2006 so the specific teachings of Ren and Mishra can be discounted as too difficult to implement. POR, 32-35. There are two problems with this analysis. First, it falls far short of the legal requirement for secondary consideration of nonobviousness, which must be tied to the claims. See *Volvo*, 81 F.4th at 1212; *Medtronic*, 70 F.4th at 1337-39. Second, Patent Owner’s concurrent assertions that the field of semiconductor technology “retains a strong element of trial and error” supports the grounds in the Petition, not Patent Owner. POR, 34 (quoting Ex-2008, 69-70).

¹ Patent Owner alleges Ueno is not prior art. POR, 45. But Dr. Bernstein relies on its teaching the GaN as a GaAs substitute was intensely studied prior to 2006. Ex-1003, ¶153. This is proper evidence for expert opinion. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281 (Fed. Cir. 1985)

Patent Owner suggests secondary considerations of nonobviousness by relying on a vague comment by the inventor Thomas Herman from a deposition in another proceeding. POR, 33 (citing Ex-2003, 30:2-15). He stated the original applicant, International Rectifier, “deemed [it] a more difficult task” to design GaN enhancement mode transistors. *Id.* Mr. Herman does not explain whether it was “more difficult” for business, cost, logistical, technical or other reasons. Ex-2003, 30:2-15. Regardless, his comments are untethered to the claims and shows the patent never fulfilled any need or achieved success— International Rectifier did not make Mr. Herman’s device. *Id.* Nothing here outweighs Ren’s prior art GaN enhancement mode transistor. *See Dow Chem. Co. v. Halliburton Oil Well Cementing Co.*, 324 U.S. 32, 330 (1945) (secondary considerations do not outweigh clear obviousness); *Genentech, Inc. v. Sandoz Inc.*, 55 F.4th 1368, 1378 (Fed. Cir. 2022) (“weak secondary considerations” do not overcome “strong” obviousness grounds (quoting *W. Union Co. v. MoneyGram Payment Sys., Inc.*, 626 F.3d 1361, 1371 (Fed. Cir. 2010))).

If, as Patent Owner asserts, semiconductor technology “retains a strong element of trial and error,” then this only proves a POSITA would have followed Bonn, Ren, and Mishra to arrive at the combination of Ground 2. *See* POR, 34. A POSITA habituated to “trial and error” would not have found it “inventive to discover the optimum or workable ranges by routine experimentation” in view of

Bonn, Ren, and Mishra. *See Applied Materials*, 692 F.3d at 1295; *In re Aller*, 220 F.2d at 456; *Pfizer*, 94 F.4th at 1347-49.

V. Mishra Discloses a Dual-Gate Transistor in Cascode Arrangement, Which Renders the Claims Obvious (Ground 3)

Mishra discloses “different amplifier arrangements” for its GaN transistors, including “a single transistor with a dual gate structure.” Mishra, [0062]. In context, this passage implements a dual gate in Figure 10, which is a two-stage cascode amplifier with first stage transistor (Q1) followed by second stage transistor (Q2) in cascode. Mishra, [0052]-[0063]; Ex-2009, 145:11-146:6, 191:20-194:14. There are just two choices for each transistor—enhancement or depletion mode. Ex-2009, 111:8-9 (discussing Mizuta (Ex-1007)). An enhancement mode first stage followed by a depletion mode second stage was common and obvious over Mishra’s disclosure to use “low voltages” and because it would have reduced power consumption, rendered the cascode suitable for high voltage and frequency, and enhanced safety. Petition, 83-88, 100; Ex-1003, [251]-[255]. Ren also describes the benefits of enhancement mode in GaN transistors, and it would have been obvious to make an enhancement mode first stage transistor using Ren’s techniques. *Id.* Patent Owner does not defeat these motivations. POR, 6-10, 46-75.

A. Mishra provides more information on how to implement its embodiments than the '003 patent

Patent Owner cannot ignore Mishra's teaching to use a dual gate transistor in cascode. A reference should be read for all it teaches. *See AliveCor*, 130 F.4th at 1015; *In re Mouttet*, 686 F.3d at 1331; *Beckman Instruments*, 892 F.2d at 1551. The law shows Mishra sufficiently discloses how to implement its teachings on dual gates. *KSR* rejected Patent Owner's rigid demand for anything more than Mishra's already-detailed disclosure. *KSR Intn'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418, 422 (2007) (obviousness accounts for "inferences and creative steps" and a POSITA "is also a person of ordinary creativity, not an automaton."). But Patent owner nevertheless attempts to disregard Mishra's dual gate as a "throw-away." POR, 42, 62.

Patent Owner's attacks carry little weight because Mishra discloses more detail than the '003 patent. POR, 35-42; *see Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461 (Fed. Cir. 1997) (prior art that provided "a level of detail similar to" the patent was enabling). Even under stringent anticipation standards, the prior art need only disclose a limitation to the degree of specificity found in the patent, not more. *See, e.g., King*, 616 F.3d at 1276. For example, in *King*, the relevant limitation required "increasing the oral bioavailability" of a drug. *Id.* at 1270-71. For this, the patent "disclose[d] no more than taking [the drug] with food," which the prior art also disclosed. *Id.* at 1276. Accordingly, the Court found the patent invalid,

concluding “the prior art need only give the same results as the patent, not better.” *Id.* (internal quotations omitted); *see also Arbutus Biopharma Corp. v. Modernatx, Inc.*, 65 F.4th 656, 661, 663 (Fed. Cir. 2023) (patent claims invalid where the prior art “specificity” was “the same as in the [asserted patent]”).

Mishra describes multiple transistor structures and explains how to make and operate them. Mishra, [0030]-[0063], Figs. 1-10; *see* Petition, 82-88. Mishra provides manufacturing methods, including deposition, contact formation, etching, passivation, and nucleation, and it cites other references for further details. Mishra, [0029]-[0036]. Mishra enumerates physical characteristics, including layer composition, doping concentrations, and layer thickness. *E.g.*, Mishra, [0030]-[0035]. And it extensively discusses the length, placement, and other features of its field plate, including that it may be source connected. Mishra, [0026]-[0029], [0036]-[0063], Fig. 7; Petition, 82-83, 94-96, 98. Mishra even includes experimental performance data. Mishra, Fig. 7. It details a two-stage cascode amplifier circuit, providing a circuit diagram that mirrors the '003 patent. Mishra, [0056]-[0063]; Petition, 82-88; *compare* Mishra, Fig. 10 (cascode circuit) *with* Ex-1001, Fig. 2 (same). Mishra then teaches to implement its amplifiers with two gates side-by-side on one semiconductor substrate, which was known. Mishra, [0062]; Petition, 82-83. A POSITA needed no more detail to expect success. Petition, 82-88.

The '003 patent, in contrast, provides far less, implicitly assuming a POSITA would have understood how to make its device. It nowhere discusses any manufacturing methods beside using the term “epitaxial layer[s]” without giving any methods. *E.g.*, Ex-1001, 2:7-31. The patent is silent as to physical transistor characteristics. Instead of giving specific thickness or doping ranges, like Mishra, the patent provides a high-level list of materials. Ex-1001, 4:43-54 (mentioning III-nitrides, GaN, InAlGaN, and AlGaN layers), 4:55-63 (SiC buffer) 4:63-67 (AlN buffer), 5:6-17 (certain metals and insulators). It provides no details of its field plate other than that it is “adjacent” to the gate. Ex-1001, 3:38-42, claims 1, 10, Figs. 3-4. It includes no experimental data.

If, as Patent Owner contends, a POSITA would not have succeeded implementing Mishra’s dual gate, then a POSITA would not have been able to make the '003 patent’s device either.

B. Mishra discloses a source connected field plate

Mishra repeatedly discloses a source connected field plate, explaining it “reduce[s] the peak electric field” and improves breakdown voltage, trapping, leakage, and reliability. *Mishra*, [0029], [0053], [0063]; *Petition*, 27, 82-83. Field plates can “be connected to the source contact in many different ways.” *Mishra*, [0063]. For example, conductive vias connect field plates to other structures. *Mishra*, [0040], [0044], [0052]. *Mishra* has a “second stage field-plated transistor connected

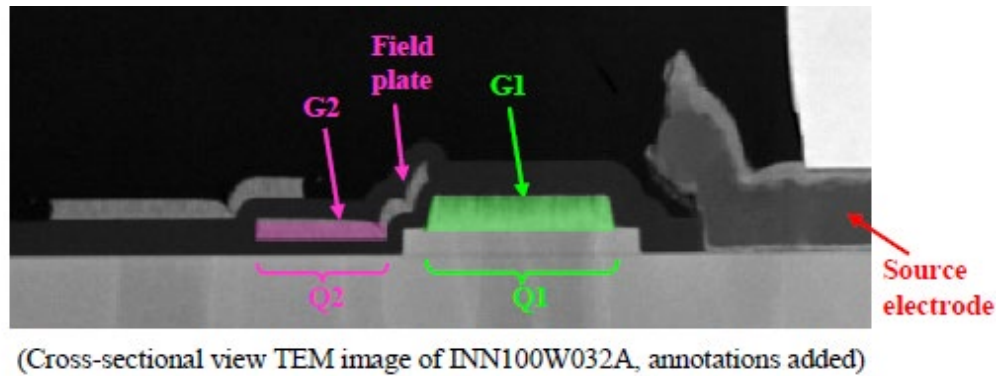
in common gate configuration,” i.e. connected to source, which is the norm for cascodes. Mishra, [0056], Fig. 10; Petition, 82-83; Ex-2009, 13:12-14:11. Mishra extensively discusses the characteristics of its field plate. Mishra, [0026]-[0029], [0036]-[0063], Fig. 7. Patent Owner improperly disregards these disclosures as if they did not exist. POR 42-43; *see AliveCor*, 130 F.4th at 1015; *In re Mouttet*, 686 F.3d at 1331; *Beckman Instruments*, 892 F.2d at 1551.

Patent Owner’s allegations that Mishra does not explain how to implement a source-connect field plate fails as a matter of law because Mishra provides more detail than the ’003 patent. POR, 35-43; *see Motorola*, 121 F.3d at 1471; *King*, 616 F.3d at 1276; *Arbutus Biopharma Corp. v. Modernatx, Inc.*, 65 F.4th 656, 661 & 663 (Fed. Cir. 2023). The ’003 patent itself never explains how its field-plated gate connects to ground and provides no details of its manufacture, composition, or dimensions. Ex-1001, 3:38-42, claims 1, 10, Figs. 3-4. Mishra thus discloses the field plate at a higher specificity than the patent. *See King*, 616 F.3d at 1276.

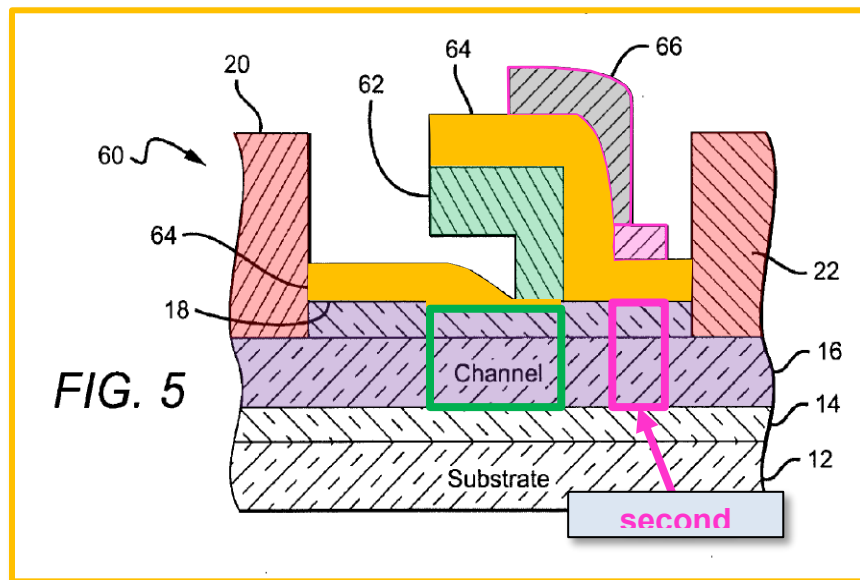
C. Mishra’s dual gate transistor teaching applies to Figure 5, and a source connected field plate in Figure 5 is the claimed second gate under Patent Owner’s infringement theories

Figure 5 depicts a single transistor amplifier with one gate. Mishra, [0042]-[0043]; Ex-2009, 153:2-14, 150:16-20. But it expressly states that each of its amplifiers could be arranged as “a single transistor with a dual gate structure.” Mishra, [0062]; Petition, 82-83. By connecting Mishra’s field plate to source, which

Mishra teaches, makes a dual gate device that has the claimed second gate under Patent Owner's infringement theories. Petition, 94-95; Ex-2009, 144:7-145:3, 191:20-194:14; Ex-1011, 21.²



Ex-1011, 21.



Mishra, Fig. 5 (annotated, modified by Ren).

² Mishra's Figure 5 orients source on the left while Infineon's image orients it on the right.

Patent Owner does not dispute that a source connected field plate overlapping another gate is itself a gate. POR, 47-52. Patent Owner thus concedes that, if Mishra teaches a source-connected field plate for Figure 5, it renders obvious the field plated second gate of [1C5]. *Id.*; Petition, 94-95, 97-98, 101-102.

That is exactly what Mishra teaches. Mishra's unqualified alternative to implement dual gate structures applies to all embodiments. *Id.*; *see* Petition, 82-88; Ex-2009, 124:20-125:17, 191:20-194:14. No "reason" is needed for specifically "selecting" Figure 5. *See* POR, 62-65. According to Patent Owner, one way to make a dual gate structure is to connect a field plate to the source. Petition, 94-95; Ex-2011, 21. This renders obvious [1C5].

D. It would have been obvious to implement Mishra's first stage transistor as enhancement in the dual gate cascode embodiment

It would have been obvious to implement Mishra's first stage transistor as enhancement in the dual gate cascode embodiment with a second stage transistor as depletion mode. Petition, 83-84; Ex-1003, [251]-[252]. The parties agree that Mishra's second stage transistor Q2 is in depletion mode. Petition, 100; POR, 53. Regarding Q1, the Petition provides two motivations to use enhancement mode. Neither invoke "common sense," as Patent Owner alleges. POR, 71-74.

First, the Petition reasoned Mishra's "low voltages" at first stage transistor Q1 included low positive voltages and thereby rendered enhancement mode obvious,

citing Dr. Bernstein’s analysis that low positive voltages are *required*. Petition, 83-85; Ex-1003, [251]-[252]; Mishra, [0060]. The Petition showed a dual cascode with a first stage enhancement mode device was known, as were enhancement mode GaN transistors, making the choice of Q1 as enhancement mode obvious. Petition, 83-88, 100-101. In response, while Patent Owner disputes positive was *required*, it fails to show that positive voltage was not obvious. POR, 53-54.

In fact, Patent Owner acknowledges positive voltages were common in such devices. POR, 54. All agree Mishra does not specify the mode of Q1 and only mentions “low voltages.” Petition, 83-84; POR, 53-54. But there are only two choices of low voltage (positive or negative), and two choices of gate (enhancement or depletion). Ex-2009, 111:8-9. And Patent Owner explains that “positive and negative supply voltages were readily available” in systems like Mishra’s. POR, 54 (citing Ex-2004, ¶204). That analysis shows the Petition was correct, which reasoned low positive voltage and the corresponding enhancement mode gate would have been an obvious choice among this limited set of options. Petition, 83-84; *see Kennematal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1384-85 (Fed. Cir. 2015) (an option among a limited set is obvious); *In re Geave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009) (when a genus “is so limited that a [POSITA] can ‘at once envisage each member of this limited class,’” the species is disclosed) (quoting *Eli Lilly & Co. v. Zenith Goldline Pharms., Inc.*, 471 F.3d 1369, 1376 (Fed.Cir.2006)); *see also*

KSR, 550 U.S. at 421 (person of skill would pursue a finite number of predictable solutions).

Second, the Petition explained Ren also motivates an enhancement mode Q1 for its power-saving benefits and reduced gate leakage, and it would have allowed high-voltage, high-frequency applications. Petition, 86-88, 100-101; Ex-1003, [255-260] [292]-[294]. Ren provides a simple mechanism for making enhancement or depletion mode gates—controlling the dielectric layer thickness. Petition, 85-88. Mishra already uses dielectrics in its gates. *Id.*

Patent Owner thus lodges an inapt criticism that Ren discloses just one gate, not two. POR, 59-60. That misunderstands the combination, which is to implement Ren’s method of controlling the properties of a GaN transistor on Q1 in Mishra’s dual gate cascode. Petition, 82-88.

Patent Owner’s veiled analogous art attack also fails. It contends a POSITA would not have been “specifically” motivated to combine Mishra and Ren because Mishra adjusts its GaN gate properties within a doping range while Ren teaches to also adjust the dielectric thickness. POR, 57. But Mishra and Ren are analogous to the ’003 patent under both tests: “(1) whether the art is from the same field of endeavor, regardless of the problem addressed and, (2) if the reference is not within the field of the inventor’s endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved.” *In re Bigio*,

381 F.3d 1320, 1325 (Fed. Cir. 2004). The references and the '003 patent all describe GaN power transistors, so they clearly fall within the same field of endeavor, and they all address problems in high power, high frequency applications, including noise (e.g., Miller effect). Mishra, [0010]; Ren, [0004]-[0005]; Ex-1001, 1:24-50; Petition, 82-88.

It would have been obvious to follow Mishra's teaching to control the properties of its materials with Ren's straightforward method of altering dielectric thickness. Petition, 82-88. These teachings conflict do not conflict. POR, 57-59. Patent Owner invents obstacles that a POSITA would have known how to overcome. *Id.* Afterall, Mishra (and Ren) gives more information on its device than the '003 patent provides. Sections. V.A-B; *C.f. King*, 616 F.3d at 1276.

VI. Conclusion

For the foregoing reasons and as explained in the Petition, the Board should find all claims of unpatentable.

Dated: December 24, 2025

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37 C.F.R. § 42.24(D) CERTIFICATION

Under the provisions of 37 CFR § 42.24(d), Petitioner certifies that the word count under §42.24(c)(1) for the foregoing Petitioner's Reply to Patent Owner's Response totals 5,546 words, as measured by the word-processing system used to prepare this paper.

Dated: December 24, 2025

By: Lionel M. Lavenue/

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing **Petitioner's Reply to Patent Owner's Response** was served on December 24, 2025, via email directed to counsel of record for the Patent Owner at the following:

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