

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

Case No. IPR2025-00094
Patent No. 8,264,003

PATENT OWNER'S SUR-REPLY

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LISTING OF EXHIBITS

Exhibit	Description
2001	Stewart, C.M., “Interim Processes for PTAB Workload Management,” Memorandum dated March 26, 2025
2002	Horowitz, P., & Hill, W. (1989). The Art of Electronics (2nd ed.). Cambridge University Press.
2003	Transcript Excerpt from Deposition of Thomas Herman dated January 17, 2025. <i>In the matter of Certain Semiconductor Devices and Products Containing the Same</i> ; ITC Inv. No. 337-TA-1414.
2004	Declaration of David K. Choi Ph.D.
2005	CV of David K. Choi Ph.D.
2006	Mil’Shtein, S., et al., Heterostructure transistor with tunable gate bias, Microelectronics Journal 36 (2005) 301-303.
2007	Preliminary Cree CGH40025F Datasheet, May 2007.
2008	Jorgenson, Dale W., et al. eds., Measuring and Sustaining the New Economy: Report of a Workshop (National Academy Press, 2002).
2009	Deposition of Joseph B. Bernstein (August 27, 2025).
2010	Errata to Deposition of Joseph B. Bernstein (September 27, 2025).

I. INTRODUCTION

The Petitioner Reply concedes that its expert, Dr. Bernstein, “*lacked*” “*experience with downconverters and RF signal mixing applications.*”¹ Reply, 13. That concession is fatal to Grounds 1 and 2. In essence, Petitioner argues that even though Dr. Bernstein did not understand the operation of the downconverter circuit that he set out to completely redesign—to the point of inoperability, that at least he understood the technology of the patent claims he was trying to match. There could not be a more compelling admission of hindsight reconstruction.

Petitioner insists that Dr. Bernstein “does not need such expertise” in the art applied in the petition grounds because he “proposed to remove” the components that made Bonn’s Figure 1 circuit a downconverter. Reply, 13. But that skips over the foundational issue of why a POSA would have had a motivation to remove those components in the first place. Dr. Choi, who is an expert on downconverters and RF circuit design, testified that “*a POSA would not have looked to strip away the very functionality that made Bonn’s downconverter so unique.*” Ex-2004 ¶¶86-88; POR, 15-18. Dr. Choi’s testimony stands unrebutted as Petitioner did not cross-examine him nor dispute his qualifications as an expert on RF circuit design. Indeed, Petitioner does not challenge Dr. Choi’s testimony in any regard. Dr. Choi’s testimony that a POSA would not have modified Bonn’s downconverter as

¹ Emphasis added unless otherwise noted.

proposed is thus the only competent evidence. Grounds 1 and 2 thus fail for this reason alone.

Ground 2 fails for the additional reason that the Petition failed to establish at least a reasonable expectation of success in making Bonn's dual-gate transistor out of GaN. The Reply now pivots, arguing that "a *dual-gate* GaN transistor" "was never the combination." Reply, 14-15. But Ground 2 plainly states that a POSA would "implement Bonn's *dual gate* FET 300 of Figure 7" and "*make [it] out of GaN.*" Petition, 49-50. Indeed, the claims require a dual-gate transistor comprising an enhancement mode transistor *merged* with a depletion mode transistor. *See* Limitations [1C9] and [10C10]. But the Petition and Reply fail to cite any evidence on an expectation of success in such a modification. The Reply concedes that Ren had only "single-gate teachings." Reply, 15. Petitioner cites no evidence that Ren's "single-gate teachings" provided the information needed to make the claimed dual-gate GaN transistor. Dr. Choi testified that making Bonn's dual-gate transistor out of GaN "would have been a *profound* modification" that a POSA would not have expected to be successful. Ex-2004 ¶¶131, 143-150 (emphasis original); POR, 31-46. The Reply does not contest Dr. Choi's testimony. Without any prior art evidence showing that a POSA would have reasonably expected success in making the claimed merged cascode transistor from GaN, Ground 2 fails for this additional reason.

Ground 3 fails because the Petition failed to establish that a POSA would have understood Mishra as disclosing a *merged* cascode transistor or rendering such a transistor obvious. POR, 46-52; Ex-2004 ¶¶152-165, 182-184. The Reply fails to address this foundational issue. For example, the Reply points out that Mishra discloses a “dual gate transistor in cascode.” Reply, 19. But disclosing the genus of dual-gate transistors does not amount to disclosing the specific claimed species of *merged* cascode transistor. Numerous types of dual-gate transistors were known, different from the one claimed. POR, 67-70, citing Ex-2004 ¶¶119-121, 177, 183-190, 232. Sankin, for example, disclosed a dual-gate transistor connected by wires, not a merged transistor as claimed. POR, 68-69; Ex-2004 ¶¶119-121; Ex-2009, 32:18-22. Petitioner offers no explanation why Mishra discloses (or renders obvious) a *merged* cascode transistor, as opposed to a different type of dual-gate transistor like Sankin’s.

The Reply’s other arguments never address Mishra’s failure to disclose a merged cascode transistor. For example, the Reply argues that “Mishra describes multiple transistor structures” and “Mishra sufficiently discloses how to implement its teachings.” Reply, 19-20. But Petitioner does not dispute that every single one of Mishra’s transistor structures was a single-gate transistor—not a dual-gate transistor. POR, 35-43. The Petition had argued that Mishra’s Figure 5 embodiment had a “second gate” (Petition, 86-88), but Dr. Bernstein admitted that

it did not. Ex-2009, 153:2-14, 150:16-20 (“[Mishra is] *not telling us that that* [sic] *field plate is also a gate.*”); POR, 39-40. The Reply now concedes, “Figure 5 depicts a *single transistor* amplifier *with one gate.*” Reply, 22. Petitioner’s failure to dispute that Mishra does not disclose a *merged* cascode transistor is fatal to Ground 3.

II. GROUNDS 1 & 2 FAILED TO ESTABLISH A POSA WOULD HAVE SCRAPPED BONN’S DOWNCONVERTER

Dr. Bernstein testified that Bonn’s “circuit is a *very complicated* circuit” and that “*I don’t understand enough about RF circuits*” to understand how Bonn’s downconverter worked. Ex-2009, 45:5-6, 99:22-101:17; *see also id.*, 44:16-17 (“I generally am *not so familiar with down-converters*”), 77:15-17 (“I have *no experience making down-converters.*”). Petitioner now concedes that Dr. Bernstein “*lacked*” “*experience with downconverters and RF signal mixing applications.*” Reply, 13. Given that Dr. Bernstein admits to having no understanding of how the Bonn circuit operates, his testimony on obvious modifications to the very same cannot be accorded weight.

Infineon’s Dr. Choi, in contrast, is an expert in RF circuit design and downconverters. Ex-2004 ¶¶88; POR, 18. He testified that:

- A. A POSA would not have used Bonn’s Figure 7 transistor for high-frequency signal amplification as Dr. Bernstein proposed because of its unequal current-carrying capacity. Ex-2004 ¶¶92-101; POR, 19-24.

- B.** A POSA would not have remade Bonn’s downconverter into an amplifier as Dr. Bernstein proposed, thereby “strip[ping] away the very functionality that made Bonn’s downconverter so unique.” Ex-2004 ¶¶86-88; POR, 15-18.
- C.** The Petition failed to show that a POSA would have repurposed Bonn’s mixer as an amplifier when the downconverter in Figure 1 already has an amplifier at FET 20. Ex-2004 ¶¶106-107; POR, 24-25.
- D.** The Petition failed to show that a POSA would have connected the second gate of a dual-gate transistor to a constant voltage source as claimed, since Mil’Shtein disclosed that doing so “*yield[ed] the worst results.*” POR, 28-29; Ex-2006, 302; Ex-2004 ¶115.

Petitioner did not depose Dr. Choi, did not dispute his qualifications as an expert on RF circuit design, and did not challenge his testimony in any way. Dr. Choi’s testimony is thus uncontested and should be dispositive that Petitioner failed to meet its burden for Grounds 1 and 2.

The Reply tries to patch up its “blatant hindsight reconstruction of the claims” (Ex-2004 ¶83; POR, 15), but fails to show that the Petition met its burden.

A. Petitioner Failed to Show a POSA Would Have Started with Bonn's Figure 7 Structure for Use as an Amplifier Absent Hindsight

Petitioner argued that a POSA would have “use[d] Figure 7’s structure for high frequency signal amplification in place of mixer 40.” Petition, 22. But Figure 7’s structure has “*non-conductive sections* 225 ... in first gate region 321 ... to individually adjust the gate width.” Ex-1006, 9:12-20; *see also* Ex-2004 ¶¶96; Ex-2009, 98:19-99:12; POR, 20-22. These non-conductive sections would have resulted in unequal current-carrying capacities across the gates, rendering the transistor suboptimal for high-frequency signal amplification. POR, 22; Ex-2004 ¶¶98. The Petition proposed no modifications to Bonn’s Figure 7 structure to make it suitable for use in an amplifier. Dr. Choi explained that a POSA would have had no reason to modify the transistor structure in Figure 7 for high-frequency signal amplification as the Petition proposed. POR, 23-24; Ex-2004 ¶¶102-105. The Reply does not dispute Dr. Choi’s testimony.

The Reply argues that Bonn has a “flexible disclosure,” and “discloses how to adjust gate parameters to achieve desired outcomes,” that its non-conductive sections were “optional” and could be arranged differently, so the Petition did “not need to propose” modifications to Figure 7. Reply, 9-11. That is wrong as a matter of law. Petitioner must make its case “with particularity” *in the Petition*. 35 U.S.C. § 312; 37 C.F.R. § 42.22 (requiring a “detailed explanation”). It cannot handwave

later by adding new theories that appear nowhere in the Petition. It was Petitioner's choice to "use Figure 7's structure for high frequency signal amplification in place of mixer 40" ***unmodified***. Petition, 22. Petitioner also chose not to rebut Dr. Choi's now uncontested testimony that a POSA would not have picked Bonn's Figure 7's structure as the Petition proposed. "I might have come up with a better rationale had I bothered" is not an argument that the PTAB should endorse.

Petitioner likely picked such an unsuitable transistor because Dr. Bernstein did not understand Bonn's disclosure. POR, 23-24; Ex-2009, 95:4-6 ("***I don't honestly understand what he means when he says current carrying capacity....***"), 99:22-101:1 ("***I don't know why*** you would do it, ... again, ***I don't understand enough about RF circuits.***"). But it is not the Board's role to fix problems with the Petition or its expert's lack of understanding and address arguments Petitioner could have made but did not—the Board's role is to address the arguments the Petition did make. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (The Board does not "enjoy[] a license to depart from the petition and institute a different inter partes review of [its] own design.") (emphasis omitted); *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (The Board must "base its decision on arguments that were advanced by a party" and has no power to "raise, address, and decide unpatentability theories never presented by the petitioner."); *Nautilus Hyosung v. Diebold*, IPR2016-00580, Paper 15, 7 (Jan. 31,

2017) (“[t]he Board must base its analysis on the arguments and evidence presented in the petition and not upon what the petitioner *could have* argued.”) (emphasis original); *Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, 925 F.3d 1373, 1383 (Fed. Cir. 2019) (“We will not fault the Board for analyzing Petitioners’ obviousness grounds in the way presented in the Petition.”).

The Reply also argues that the Petition was not required to select the best option, only a suitable one. Reply, 11-12. But Dr. Choi testified that a POSA would not have viewed Bonn’s Figure 7 structure as being suitable for high-frequency signal amplification. POR, 23-24; Ex-2004 ¶¶102-105. Petitioner does not dispute Dr. Choi’s testimony, thus conceding that Figure 7’s structure was not suitable and not one a POSA would have picked.

In sum, the uncontested expert testimony is that Figure 7’s structure is not suitable for the purpose the Petition proposed, and a POSA would not have used it in the first place. POR, 24; Ex-2004 ¶105.

B. Petitioner’s Proposed Ground Would Have Rendered Bonn’s Downconverter Inoperable for Its Intended Purpose

1. Scrapping Bonn’s Downconverter Would Render Fig. 1 Inoperable for Its Intended Purpose

Bonn teaches that its dual-gate transistor can be “tailored” for use in “other applications such as high frequency signal amplification.” Ex-1006, 11:34-37.

Bonn’s suggestion to “tailor[.]” refers to transistor properties (gate width, dopant

concentration, etc.); it is **not** a license to reinvent the downconverter of Figure 1 to the point that it is unrecognizable. POR, 11-12; Ex-2004 ¶¶80. Petitioner does not dispute this fact, pointing to no disclosure in Bonn that suggests the drastic dismantling of its operational purpose and function to reinvent it into an amplifier.

In Reply, Petitioner rehashes all the components that the Petition alleged POSAs would have stripped away from Bonn's downconverter to change its basic operating principle. Reply, 3-7. In doing so, Petitioner cites nothing more than the naked say-so of its admittedly unqualified expert. *Id.* The Reply argues that the transformation of Bonn's downconverter into an amplifier merely "implements Bonn's explicit intent" and that "each modification merely implements Bonn's instructions." *Id.*, 3. But the Reply fails to dispute that Bonn's Fig. 1 is not an amplifier, but a downconverter, and only teaches the functions of the components in its downconverter, never suggesting stripping them all away. POR, 10-13; Ex-2004 ¶¶80-83. Petitioner thus failed to establish that a POSA would have destroyed Bonn's downconverter to change its basic operating principle. POR, 15-18; Ex-2004 ¶¶84-88.

2. Petitioner Concedes Dr. Bernstein "Lacked" "Experience with Downconverters and RF Signal Mixing Applications"

Petitioner's proposed dismantling of Bonn's downconverter is based exclusively on the naked say-so of Dr. Bernstein. Petition, 23-25; POR, 12-13; Reply, 4-7. But Dr. Bernstein admitted that he was not an RF circuit expert and

was unfamiliar with Bonn's downconverter. POR, 14-15; Ex-2009, 44:16-17, 46:18-20 ("*I'm not an RF circuit expert*, so I have *very little experience with down-converters and mixers, to be honest.*"), 60:20-21, 72:20-21, 77:15-17.

Petitioner now concedes that Dr. Bernstein "*lacked*" "*experience with downconverters and RF signal mixing applications.*" Reply, 13.

The Reply argues that Dr. Bernstein's testimony is sound because he "far exceeded the parties' definition of a POSITA." Reply, 12. But even if Dr. Bernstein was qualified to offer opinions on the technology of the '003 patent, it does not mean he can offer expert opinions on other topics on which he admits he lacks specialized expertise. *Lebron v. Sec'y of Fla. Dep't of Child. & Fams.*, 772 F.3d 1352, 1368 (11th Cir. 2014). "Testimony on subject matters unrelated to the witness's area of expertise is prohibited by Rule 702." *Louis Vuitton Malletier v. Dooney & Bourke*, 525 F. Supp. 2d 558, 642 (S.D.N.Y. 2007) (citing *Seatrax v. Sonbeck Int'l*, 200 F.3d 358 (5th Cir. 2000)). Expert testimony "beyond [the witness'] expertise and knowledge" is "in the realm of speculation." *XpertUniverse v. Cisco Sys.*, No. 09-cv-157, 2013 WL 865974, 10 at *3 (D. Del. Mar. 7, 2013). Dr. Bernstein is not qualified to opine on modifying the RF circuitry of Bonn's downconverter because both he and Petitioner concede that he lacks the necessary expertise for that specific topic.

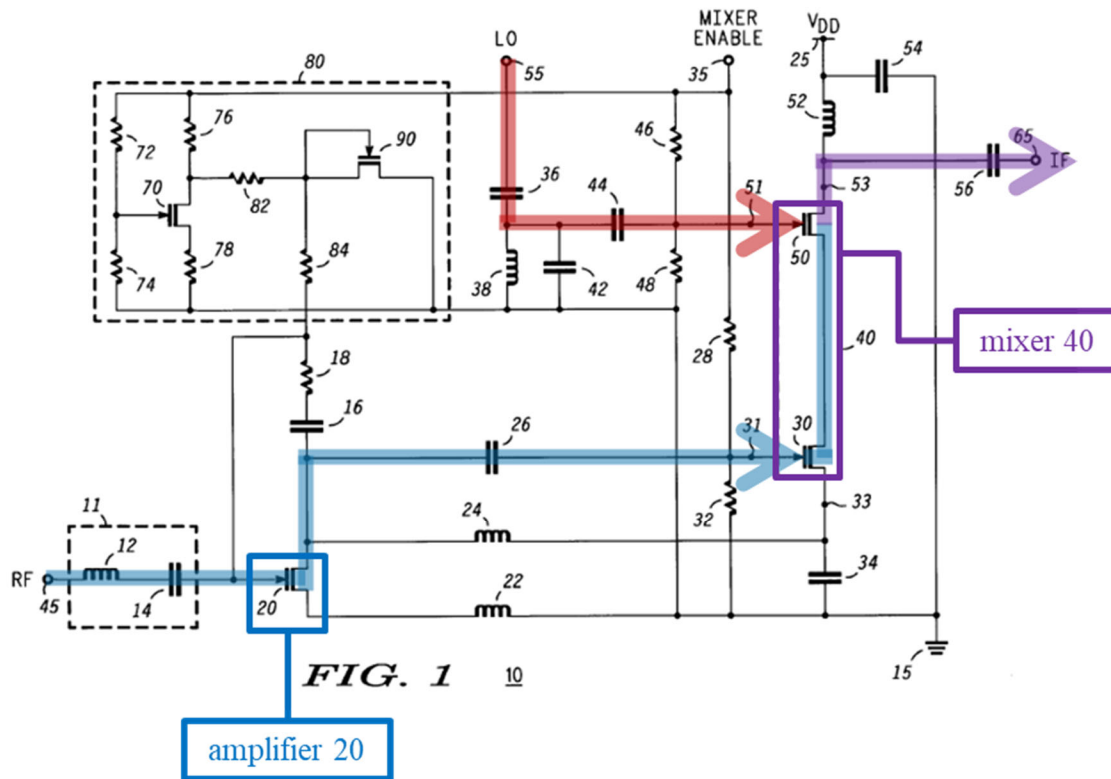
The Reply also argues that Dr. Bernstein “does not need such expertise” because he “proposed to remove” the components that made Bonn’s Figure 1 circuit a downconverter. Reply, 13. But that skips over the foundational issue of whether a POSA would have made such a proposal in the first place, let alone provide an articulable rationale necessary to render the removal of a laundry list of specific components obvious. Dr. Bernstein’s reason is not a technical one. Indeed, it cannot be, given that he admits he does not understand the component’s operation or the circuit’s functionality. Dr. Bernstein destroyed the Bonn circuit to match the claims. This textbook hindsight reconstruction must be rejected.

On the other hand, Dr. Choi, who is an expert on downconverters and RF circuit design, testified that “*a POSA would not have looked to strip away the very functionality that made Bonn’s downconverter so unique.*” Ex-2004 ¶¶86-88; POR, 15-18. Petitioner did not challenge Dr. Choi’s testimony in any way. Dr. Choi’s testimony that a POSA would *not* have modified Bonn’s downconverter in the way proposed by the Petition is thus uncontested.

C. Petitioner Failed to Show that a POSA Would Have Reconstructed Bonn’s Circuitry When it Already Contained an Amplifier

Bonn discloses a downconverter with a single-gate FET amplifier (20) connected to a mixer (40). Ex-2004 ¶¶106-107; POR, 24-25.

Bonn, Figure 1 (Annotated)



The Petition failed to explain why a POSA would have extensively modified the circuitry in Figure 1 to repurpose mixer 40 as an amplifier when the downconverter in Figure 1 already has an amplifier at FET 20. POR, 25; Ex-2004 ¶108.

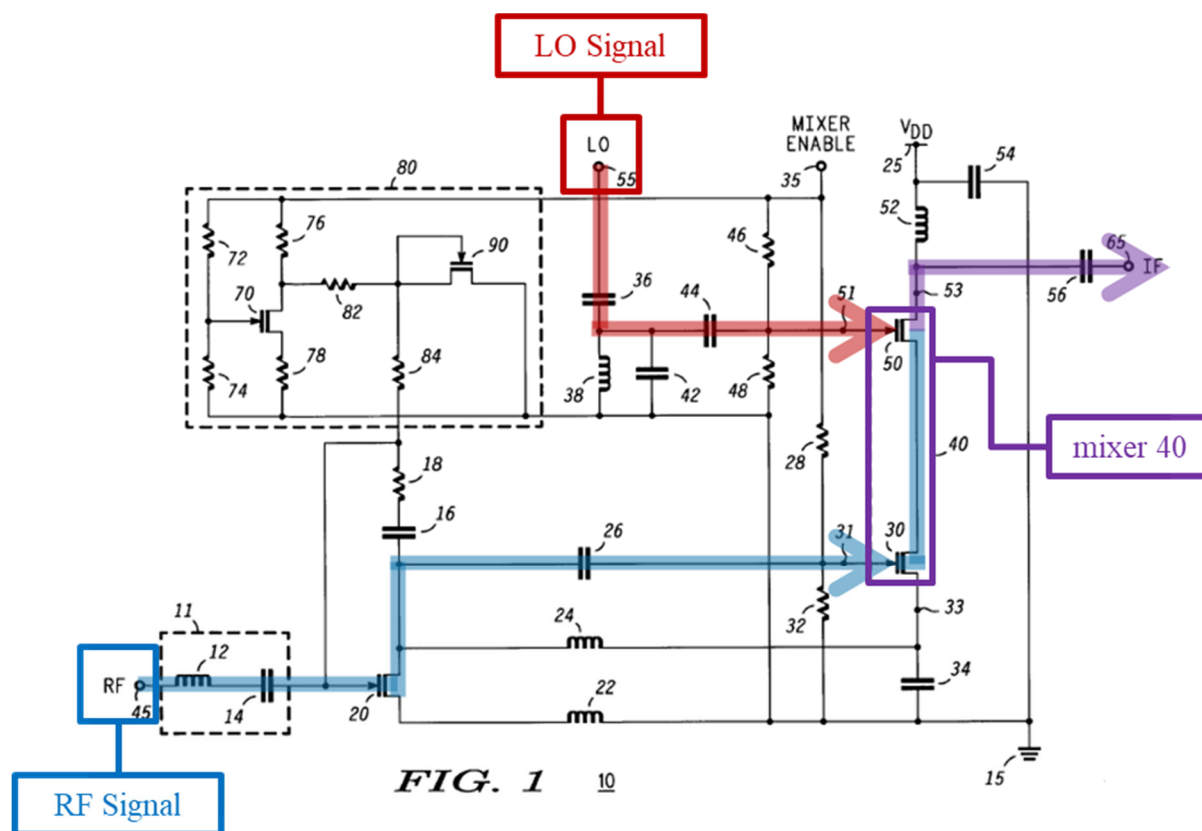
The Reply has no answer. The Reply argues that Bonn's disclosure of the single-gate FET 20 does not negate its teaching that a dual-gate transistor could be used as an amplifier. Reply, 7. "Could be" is not the standard for obviousness. The required logic must explain *why* a POSA would have used a dual-gate transistor in place of the single-gate FET 20. POR, 25. That answer is provided nowhere in the Petition because there is no logical answer. The only rationale here is the hindsight

reconstruction of a circuit by an alleged “expert” that could not understand the circuit he was modifying, based upon the roadmap provided to him in the form of the claims of the ’003 patent. *Id.*

D. Mil’Shtein Disclosed Connecting the Second Gate to a Constant Voltage Produced the “Worst” Results

Bonn’s downconverter (10) only ever connects a transistor’s gate to a *variable* voltage source, never disclosing connecting the second gate of a merged cascode transistor to a *constant* voltage source as required by Limitations [1C7] and [10C8]. POR, 10-11; Ex-1006, 2:8-14, 2:66-3:12, Fig. 1 (annotated below); Ex-2004 ¶¶58-59, 70-73. Indeed, the Board acknowledged that Bonn failed to disclose connecting either gate of mixer 40 to a *constant* voltage source as claimed. Paper 9, 13.

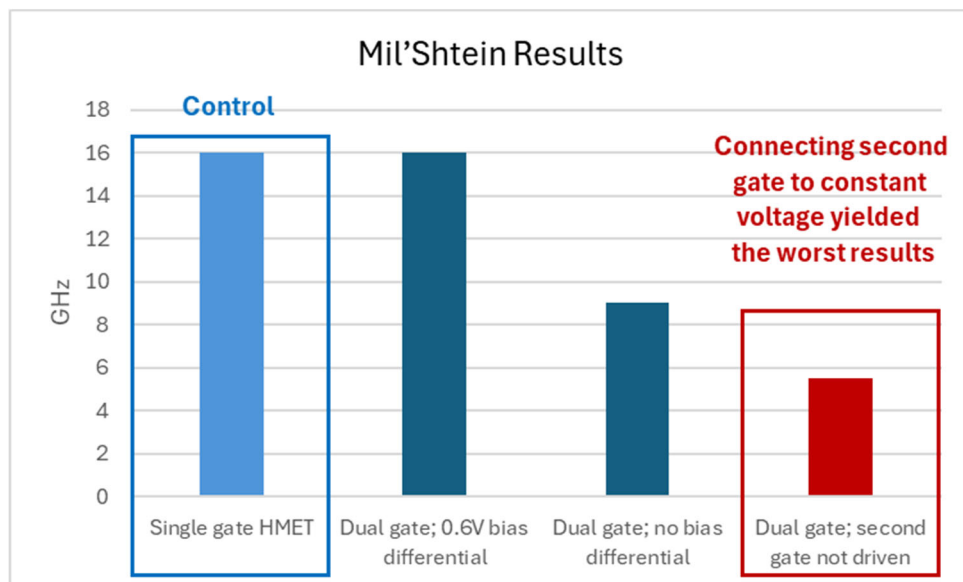
Bonn, Fig. 1 (Annotated)



Dr. Choi testified, “[e]ven if a POSA had had reason to use the dual-gate transistor of Figure 7 as an amplifier and even if a POSA had had reason to re-configure Bonn’s mixer (40) to turn it into an amplifier,” Petitioner still failed to show that “a POSA would have had reason to connect the gate terminal (51) to a constant voltage source, such as ground.” Ex-2004 ¶¶109-115; POR, 26-30. Again, Petitioner failed to contest Dr. Choi’s testimony.

Dr. Choi’s testimony is supported by Bonn, which discloses applying a *variable* voltage source to *both* gates of its dual-gate transistor. POR, 26-27; Ex-2004 ¶¶69-73, 80-88. And Dr. Choi’s testimony is supported by Mil’Shtein, which

disclosed connecting the second gate of a dual-gate transistor to a constant voltage source “*yield[ed] the worst results.*” POR, 28-29; Ex-2006, 302; Ex-2004 ¶115.



The Reply argues that connecting the second gate of Bonn’s dual-gate transistor to ground would have “provided advantages over a single-gate amplifier, including increased amplification, reduced feedback, and lower noise” that “Patent Owner never disputes.” Reply, 7-9. But Infineon had no reason to dispute that a dual-gate transistor had benefits “over a single-gate amplifier.” The transistor of Figure 7 that Petitioner proposed was already a dual-gate structure. Moreover, the Petition never alleged that connecting the second gate of a dual-gate transistor to ground would have reduced feedback or lowered noise, as the Reply claims. The Petition alleges those benefits were achieved through “remov[ing] resistors 46 and

48,” which the Petition never alleges relates to connecting the second gate to ground.² Petition, 25. Infineon cannot dispute what the Petition failed to present.

The Reply argues that connecting the second gate to ground still “amplified signals below 5.5 GHz.” Reply, 8. But Petitioner failed to explain why that matters. The Petition argued that Bonn disclosed the use of its dual-gate transistor for “high frequency signal amplification.” Petition, 24, citing Ex-1006, 11:26-37. High frequency amplification is intended for frequencies of “**10 GHz.**” POR, 54; Ex-1009, [0006], [0009]-[0010]; Ex-2004 ¶¶204. At 10 GHz, Mil’Shtein shows that connecting the second gate to a constant voltage source produced no amplification because the transistor stopped amplifying at **5.5 GHz.** POR, 28; Ex-2004 ¶¶112-115. That a grounded second gate amplified at frequencies below 5.5 GHz is thus immaterial to whether it would amplify at the targeted frequency range—the use case the Petition proposes. Petitioner can’t seem to keep its story straight.

The Reply argues that Mil’Shtein only “assessed one parameter.” Reply, 8-9. But Petitioner does not dispute Dr. Choi’s conclusion from Mil’Shtein’s

² The Petition argued that “remov[ing] capacitor 34 to short gate structure 324 to ground” increases “signal amplification” (Petition, 24) but the Petition and Dr. Bernstein never compared that configuration to a dual-gate amplifier where both gates are driven as Mil’Shtein did.

assessment of that one parameter that “driving both gates ... resulted in better results than when only one gate was actively driven, which would have motivated a POSA to consider driving both gates ..., rather than connecting its upper (second) gate to a constant voltage source, as claimed in the ’003 patent.” Ex-2004 ¶116; POR, 29.

The Reply argues that Mil’Shtein does not “teach away” from connecting Bonn’s second gate to a constant voltage source. Reply, 7-8. But Infineon never argued that it did. POR, 27-29. Infineon only explained that Mil’Shtein prefers driving both gates, rather than connecting the second gate to a constant-voltage source as claimed (POR, 29; Ex-2004 ¶116), a point Petitioner now concedes. Reply, 8 (Mil’Shtein “expresses a preference for the other three approaches,” not the claimed approach).

The Reply argues that “Mil’Shtein is [] not probative” because Infineon, not Petitioner, introduced it. Reply, 7-8, citing *Tec Air v. Denso Mfg. Michigan*, 192 F.3d 1353 (Fed. Cir. 1999) and *In re Beattie*, 974 F.2d 1309 (Fed. Cir. 1992). But neither of those cases stands for the proposition that a prior art reference cannot disprove an obviousness rationale just because the patent owner cited it rather than Petitioner. Moreover, Dr. Bernstein testified that Mil’Shtein was his “good friend,” that he was “very familiar” with the article, and that ***Dr. Bernstein reviewed it as part of “my own background research.”*** Ex-2009, 173:16-175:7; POR, 27 n.4. Dr.

Bernstein thus knew of Mil'Shtein, knew that it taught a preference for driving a dual-gate transistor in ways contrary to the one he proposed, and Petitioner chose to conceal that teaching by failing to file it with the Board despite obligations to do so. 37 C.F.R. § 42.51(b)(1)(iii).

In sum, Mil'Shtein teaches that connecting a dual-gate transistor in the manner proposed by the Petition “*yield[ed] the worst results*” and is thus further evidence that a POSA would not have connected a dual-gate transistor in the manner proposed by the Petition. POR, 27-29.

III. GROUND 2 FAILED TO ESTABLISH THAT A POSA WOULD HAVE HAD A REASONABLE EXPECTATION OF REMAKING BONN'S TRANSISTOR FROM GAN

As an initial matter, the Reply argues that “a *dual-gate* GaN transistor” “was never the combination.” Reply, 14-15. But that’s contrary to the record here. Ground 2 argued a POSA would “implement Bonn’s *dual gate* FET 300 of Figure 7” and “*make [it] out of GaN.*” Petition, 49-50. Indeed, all the claims require a dual-gate transistor comprising an enhancement mode transistor *merged* with a depletion mode transistor. *See* Limitations [1C9] and [10C10]. And claims 2-16 all require a “III-Nitride layer” (Limitations [2A] and [2B]) or a “III-Nitride material” (Limitations [10C1] and [10C2]), of which GaN is an example, and the one the Petition picked for its Ground 2 combination. Petition, 49-50. If making “a *dual-gate* GaN transistor” was not the combination of Ground 2 as the Reply alleges,

then the Petition either failed to show the combination met the claims or failed to make its case “with particularity,” either of which is fatal to Ground 2. 35 U.S.C. § 312; 37 C.F.R. § 42.22 (requiring a “detailed explanation”).

Ground 2 failed for the additional reason that the Petition failed to establish at least a reasonable expectation of success in making Bonn’s dual-gate transistor out of GaN. POR, 31-46. Specifically, the Petition failed to cite any prior art reference disclosing that a POSA would have known how to make a merged cascode transistor out of GaN. *Id.* The Reply has no answer—never arguing that the Petition met its burden in establishing a reasonable expectation of success.³ Reply, 14-18.

If anything, the Reply confirms the Petition’s failure. The Reply concedes that Ren had only “single-gate teachings.” Reply, 15. Petitioner cites no evidence that Ren’s “single-gate teachings” provided the information needed to make the claimed dual-gate GaN transistor. The Reply concedes that whether Mishra discloses a dual-gate transistor “is immaterial to Ground 2.” *Id.* And the Reply does not dispute that Beach, Ueno, and Sankin each fail to disclose a dual-gate merged cascode transistor. *Id.*, 15-16. The Reply argues that Infineon’s discussion

³ The Reply’s arguments about “secondary considerations” (Reply, 16-17) are strawman arguments. Infineon’s POR never mentions secondary considerations.

of the state of the art is “vague” (Reply, 16-17), but does not dispute Dr. Choi’s conclusion that “a switch from GaAs to GaN ... is a profound change that a POSA would not have expected to be successful.” Ex-2004 ¶150; POR, 35.

IV. GROUND 3 FAILED TO ESTABLISH THAT MISHRA DISCLOSED OR RENDERED OBVIOUS A MERGED CASCODE TRANSISTOR

Ground 3 fails because the Petition failed to establish that a POSA would have understood Mishra as disclosing a *merged* cascode transistor or rendering such a transistor obvious. POR, 46-52, 67-70; Ex-2004 ¶¶152-165, 182-190. Numerous types of dual-gate transistors were known, different from the one claimed. POR, 67-70, citing Ex-2004 ¶¶119-121, 177, 183-190, 232. Sankin, for example, disclosed a dual-gate transistor connected by wires, not a merged transistor as claimed. POR, 68-69; Ex-2004 ¶¶119-121; Ex-2009, 32:18-22. While Mishra discloses a “dual gate transistor in cascode” (Reply, 19), disclosing the genus of dual-gate transistors does not amount to disclosing the specific claimed species of *merged* cascode transistor. POR, 46-52, 67-70; Ex-2004 ¶¶152-165, 182-190. To this, the Reply has no answer, silently conceding that Mishra does not disclose a merged cascode transistor as claimed.

Without any prior art that discloses a merged cascode transistor, Petitioner and its declarant cannot now rely on common sense alone to fill in the missing limitation. POR, 71-74. The Reply argues that the Petition does not invoke common sense (Reply, 24), but that relates to picking an enhancement mode for

the first gate. The Reply's disavowal of using common sense does not address the lack of disclosure of a *merged* cascode transistor in any of the prior art cited in Ground 3.

Finally, Ground 3 fails because the Petition failed to establish that a POSA would have had at least a reasonable expectation of success in transforming Mishra's single-gate transistor into a dual-gate transistor with a drain region of an enhancement mode transistor merged with a source region of a depletion mode transistor. POR, 75-76; Ex-2004 ¶¶229-237. The Reply has no answer to this either, never once mentioning an expectation of success.

The arguments that the Reply does make never address the above foundational issues, silently conceding that Mishra does not disclose or render obvious a merged cascode transistor, as opposed to a different type of dual-gate transistor, such as Sankin's.

A. The Degree of Mishra's Disclosure of How to Implement Its Embodiments Is Immaterial Because Petitioner Does Not Dispute Every One of Those Embodiments Was a Single-Gate Structure

The Reply argues that "Mishra describes multiple transistor structures" and "Mishra sufficiently discloses how to implement its teachings." Reply, 19-21. But Petitioner does not dispute that every single one of Mishra's transistor structures was a single-gate transistor—not a dual-gate transistor. POR, 35-43. The Petition had argued that Mishra's Figure 5 embodiment had a "second gate" (Petition, 86-

88), but Dr. Bernstein admitted that it did not. Ex-2009, 153:2-14, 150:16-20 (“[Mishra is] *not telling us that that* [sic] *field plate is also a gate.*”); POR, 39-40. The Reply now concedes that “Figure 5 depicts a *single transistor* amplifier *with one gate.*” Reply, 22. It thus does not matter how well Mishra describes its single-gate transistors or how to make them, because, as Petitioner concedes, every one of those structures was a single-gate structure, not a dual-gate structure as claimed.

B. Mishra’s Disclosure of a Source Connected Field Plate Is Immaterial Because Petitioner’s Expert Admitted Mishra’s Field Plate Is Not a Second Gate

The Reply argues that “Mishra repeatedly discloses a source connected field plate” (Reply, 21-22) but fails to explain the relevance of that disclosure. To the extent Petitioner intended to imply that Mishra’s source connected field plate is a second gate, Petitioner’s own expert flatly contradicted that contention. Ex-2009, 153:2-14, 150:16-20 (“[Mishra is] *not telling us that that* [sic] *field plate is also a gate.*”); POR, 39-40. It thus does not matter whether Mishra discloses a source connected field plate as part of its single-gate transistors, because the challenged claims require a merged cascode transistor with two gates, not just one, as disclosed by Mishra’s transistor structures. POR, 47-52, citing Ex-2004 ¶¶152-153, 156-166, 182-184; Ex-2009, 154:8-155:2 (“Q. Before the break we were talking about ... *whether or not Mishra itself provided a figure that showed a* single

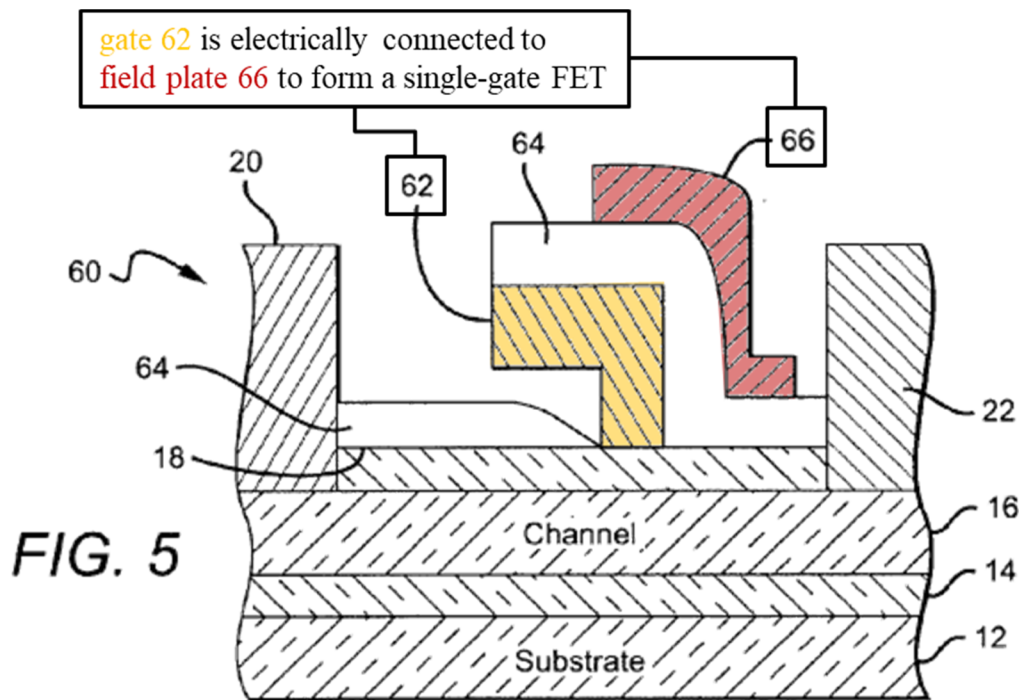
transistor with a *dual-gate structure*. And *I think the answer was no....* Do I have that right? A. *You have that basically right....*”).

C. Infineon’s Infringement Contentions Do Not Establish Mishra’s Figure 5 Structure Has Two Gates

The Reply argues that “Mishra’s dual gate transistor teaching applies to Figure 5 and a source connected field plate in Figure 5 is the claimed second gate under Patent Owner’s infringement theories.” Reply, 22-24. This argument is wrong for multiple independent reasons.

First, Mishra does not disclose that the field plate in Figure 5 is connected to the source—Mishra discloses that it is connected to the gate. POR, 39-40. Specifically, Mishra discloses that “[l]ike the field plate 46 shown in FIGS. 3 and 4 and described above, the *field plate 66* can be *connected to the gate 62 in many different ways*.” Ex-1009, [0044]; Ex-2004 ¶¶156-158.

Mishra Figure 5 (Annotated)



Dr. Choi explained that “[w]hile Mishra does mention the field plate may be connected to the source (Ex-1009, [0029], [0062]), *Mishra never describes Figure 5 as having such a connection*, rather, describing that field plate 66 connects to the gate 62 (*id.*, [0044]).” Ex-2004, ¶157; POR, 39-40. Petitioner does not dispute Dr. Choi’s testimony. Even Dr. Bernstein confirmed that Figure 5 depicts a single-gate transistor at his deposition. Ex-2009, 153:2-14, 150:16-20 (“[Mishra is] *not telling us that that* [sic] *field plate is also a gate.*”); POR, 39-40. Petitioner’s contention that Figure 5 shows a source-connected field plate is thus unsupported by Mishra. Reply, 22 (“Figure 5 depicts a *single transistor* amplifier *with one gate.*”).

Second, Petitioner provides no reason why Mishra’s source-connected field plate or why “Mishra’s dual gate transistor teaching applies *to Figure 5*.” Reply, 22-24. The Reply argues “[n]o reason is needed for specifically selecting Figure 5,” (*id.*, 24), but that is not an accurate statement of the law. POR, 62-66. Just because a dual gate transistor and source-connected field plate “*could be combined*” with Figure 5, that “is not enough.” *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017) (emphasis original). “Obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Id.*, quoting *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (emphasis original). Petitioner’s argument lacks any reason why a POSA *would have made* the combinations with Figure 5 specifically. POR, 62-66. Had Petitioner picked any of the other embodiments of Mishra, that combination would not have met the claims—something Petitioner does not dispute in Reply. *Id.*, 63-64. The Petition plainly picks Figure 5 out of hindsight rather than any objective reason, which is improper. *Pers. Web Techs.*, 848 F.3d at 994.

Third, Infineon’s infringement contentions show why Petitioner’s infringing product meets the claims. Ex-1011. The contentions never discuss Mishra or its Figure 5 transistor. *Id.* Infineon’s infringement contentions, therefore, cannot

establish that Mishra's Figure 5 has two gates. In other words, just because Petitioner's infringing product has a second gate that comprises a field plate does not mean that Mishra Figure 5's field plate acts as a gate, even if it were connected to the source, and not connected to the gate 62 as Mishra teaches. Ex-2009, 153:2-14, 150:16-20 ("[Mishra is] *not telling us that that* [sic] *field plate is also a gate.*"); POR, 39-40.

D. Whether It Would Have Been Obvious to Implement Mishra's First Gate in Enhancement Mode Is Immaterial to Whether Mishra Discloses a Merged Cascode Transistor

Petitioner admitted that "Mishra does not explicitly comment on the mode in which [Mishra's first transistor] Q1 operates" (Petition, 83) but argued that it would have been obvious to implement the first stage transistor as enhancement mode (*id.*, 84). Infineon explained why the Petition failed to establish that a POSA would have selected an enhancement mode followed by a depletion mode. POR, 52-62.

The Reply addresses some but not all of those explanations. Reply, 24-27. For example, the Reply argues about Mishra's alleged disclosure of "low positive voltages" as "making the choice of Q1 as enhancement mode obvious." Reply, 24-25. But the Reply fails to dispute that Mishra discloses using a negative ("-6V") voltage rather than a positive voltage, as alleged. Ex-1009, [0060]; Ex-2004 ¶203; POR, 54. The Reply argues that other references, such as Ren, achieved benefits

using an enhancement-mode transistor. Reply, 26-27. But Ren discloses its transistors are used for “inverter systems” for “high power electronics.” Ex-1008, [0040]. And the Reply fails to dispute that the Petition failed to establish that the benefit Ren (and others) achieved for applications different than Mishra’s signal amplification would not have been realized by Mishra’s use of an enhancement mode transistor. POR, 55-57; Ex-2004 ¶¶207-211 (“Power supply systems, again, perform different functions than signal amplification ... as disclosed by Mishra.”). The Reply’s failure to dispute these facts demonstrates that the Petition failed to show that a POSA would have selected an enhancement mode followed by a depletion mode gate as claimed.

Regardless of whether a POSA would have chosen an enhancement mode first stage transistor or not, the Reply’s arguments fail to address the foundational issue that Mishra does not disclose or render obvious a *merged* cascode transistor, as opposed to a different type of dual-gate transistor like Sankin’s. The Board thus need not reach the issue of whether an enhancement mode first stage transistor would have been obvious.

Respectfully submitted,
Infineon Technologies Americas Corp.

Date: February 4, 2026

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing **PATENT OWNER's SUR-REPLY** contains 5,566 words excluding; a table of contents, a table of authorities, a certificate of service or word count, or appendix of exhibits or claim listing. Patent Owner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Date: February 4, 2026

/MacAulay Rush/
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Paralegal
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CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.6 (e)(4)

I certify that on February 4, 2026, a copy of the foregoing document, including any exhibits filed therewith, is being served via electronic mail, as previously consented to by Petitioner, upon the following:

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