United States Patent and Trademark Office

Before the Patent Trial and Appeal Board

Innoscience America, Inc.

(Petitioner)

v.

Infineon Technologies Americas Corp.

(Patent Owner)

IPR2025-00094 | **U.S. Patent No. 8,264,003**

Infineon Exhibit 2011
Innoscience v. Infineon
IPR2025-00094

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Three Grounds, Multiple Overlapping Failures

Grounds 1 & 2	**Multiple Reasons a POSA Would Not Have Modified Bonn as Petition Proposes:** • **Dr. Bernstein admitted "I am not an RF circuit expert" three times and that he had "very little experience with down-converters" such as Bonn's** • Mil'Shtein taught the proffered configuration "yield[ed] the worst results"

POR at 10-13; PO Reply at 4-18

Grounds 2 & 3	**Failure to Establish a Reasonable Expectation of Success:** • In 2006, GaN was still an emerging and unpredictable technology • Petitioner failed to show a POSA could have predictably remade Bonn's transistor from GaN or Mishra's single-gate transistor into a merged dual-gate GaN transistor

POR at 30-46, 75-76; PO Reply at 18-21

Ground 3	**Missing Disclosure of a Merged Dual-Gate Transistor:** • Mishra's disclosure of the *genus* of dual gate transistors fails to disclose the specific *species* of merged dual gate transistor claimed • Petitioner identifies no other prior art evidence to fill this evidentiary gap

POR at 46-52, 62-74; PO Reply at 20-27

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

GROUNDS 1 & 2

BONN-BASED GROUNDS FAIL BECAUSE DR. BERNSTEIN DID NOT UNDERSTAND BONN

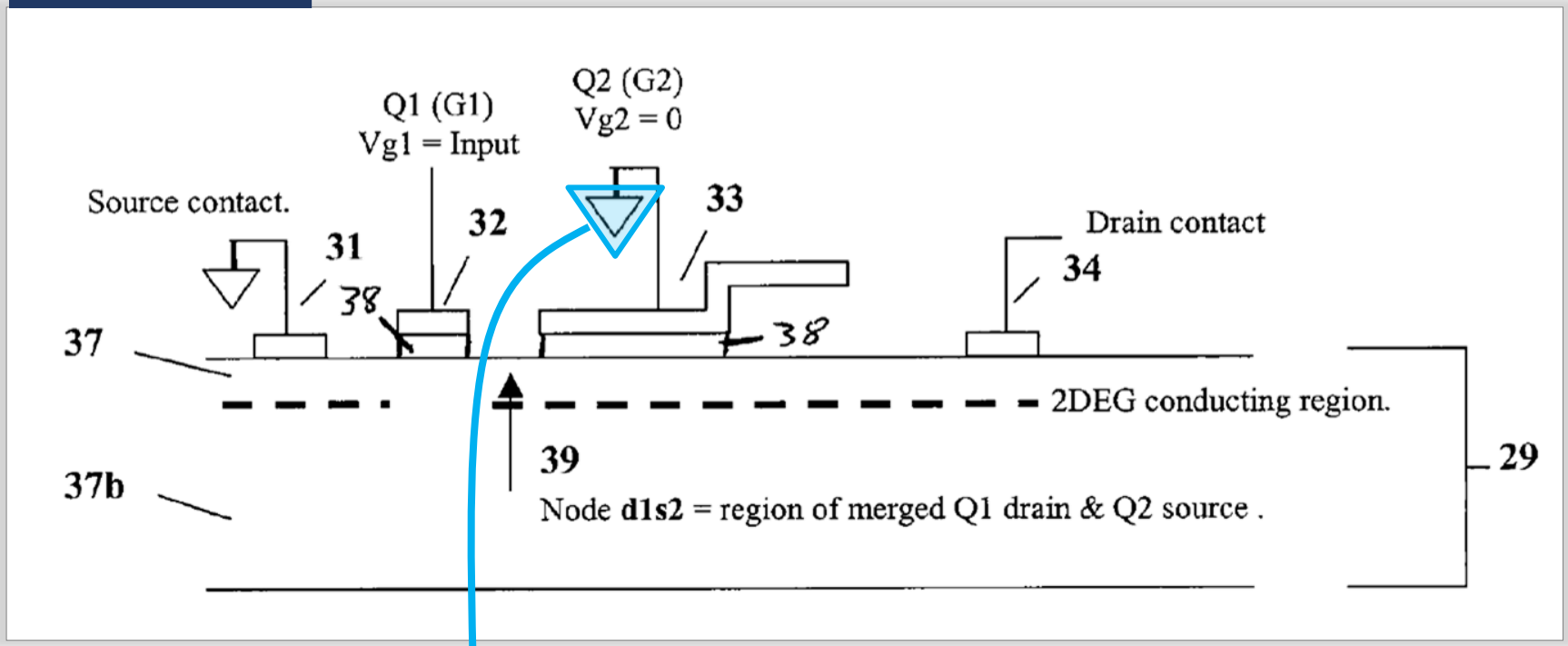
Dr. Bernstein: "I'm not an RF circuit expert, so I have very little experience with down-converters and mixers."

Ex-2009, 46:18-22, 60:20-22, 72:20-22; POR at 10-30; PO Reply at 4-18

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’003 Patent Claims Connecting the Second Gate to a Constant Voltage Source

’003 Patent



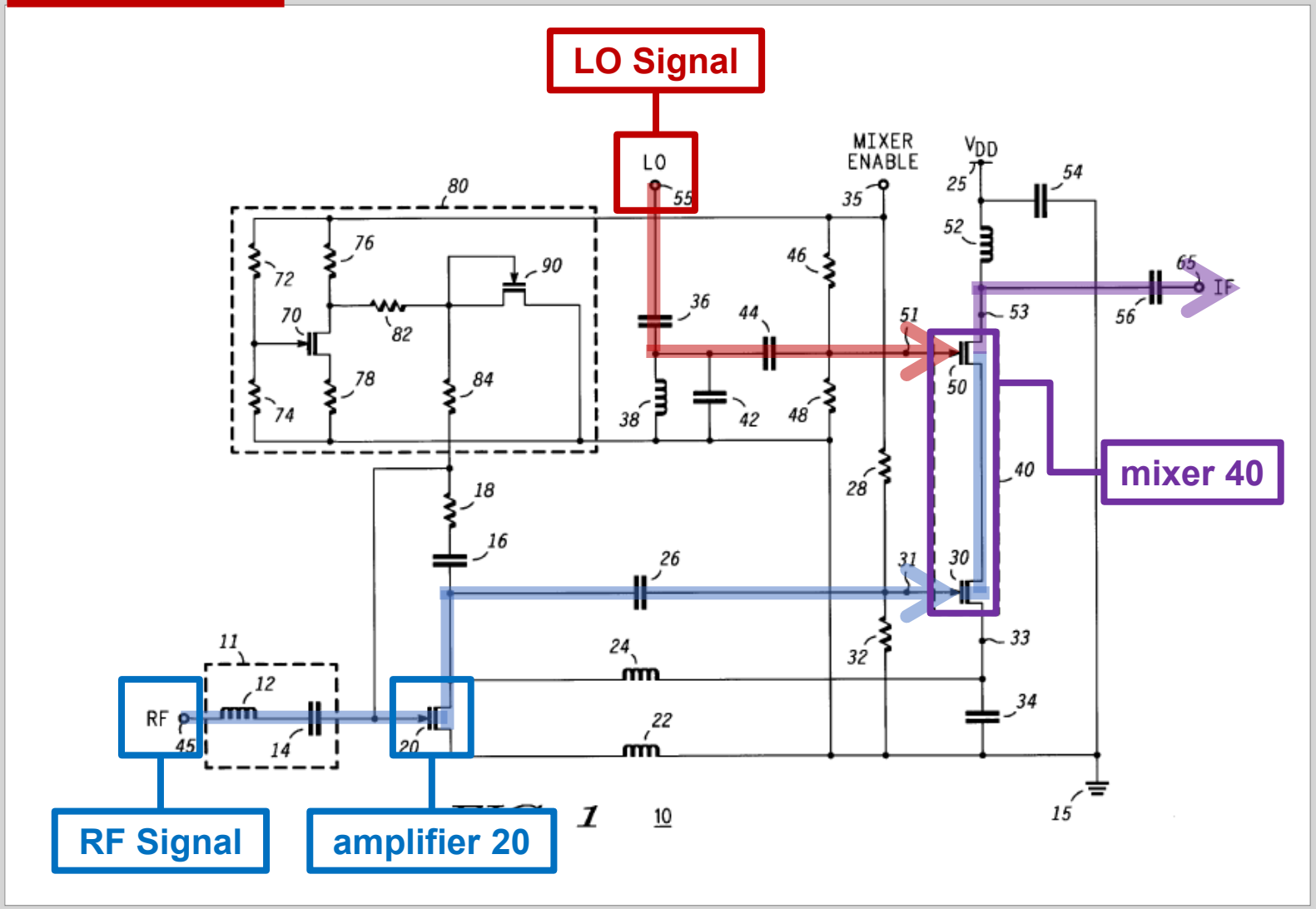
the second gate is connected to [a] constant voltage source…

Limitations [1C7] and [10C8]

POR at 1

Bonn's Figure 1 Is a Downconverter – Not an Amplifier – All Gates Are Connected to Variable Voltage Sources

Bonn



Ex-1006, Fig. 1; Ex-2004 at ¶¶ 70, 73, 93; POR, 2, 10-11, 20; PO Reply at 11-18

Petitioner Stripped Away Most of Bonn's Downconverter, Making it Inoperable for its Intended Purpose

Stripped Away

- **Amplifier 20**
  (and associated circuitry)
- **Voltage source 80**
  (and associated circuitry)
- **Capacitors**
  16, 26, and 34
- **Resistors**
  22, 24, 26 and 48
- **The LO Circuit port**
- **The LO Circuit**

Petition, 23-25; POR, 12-13

Petition

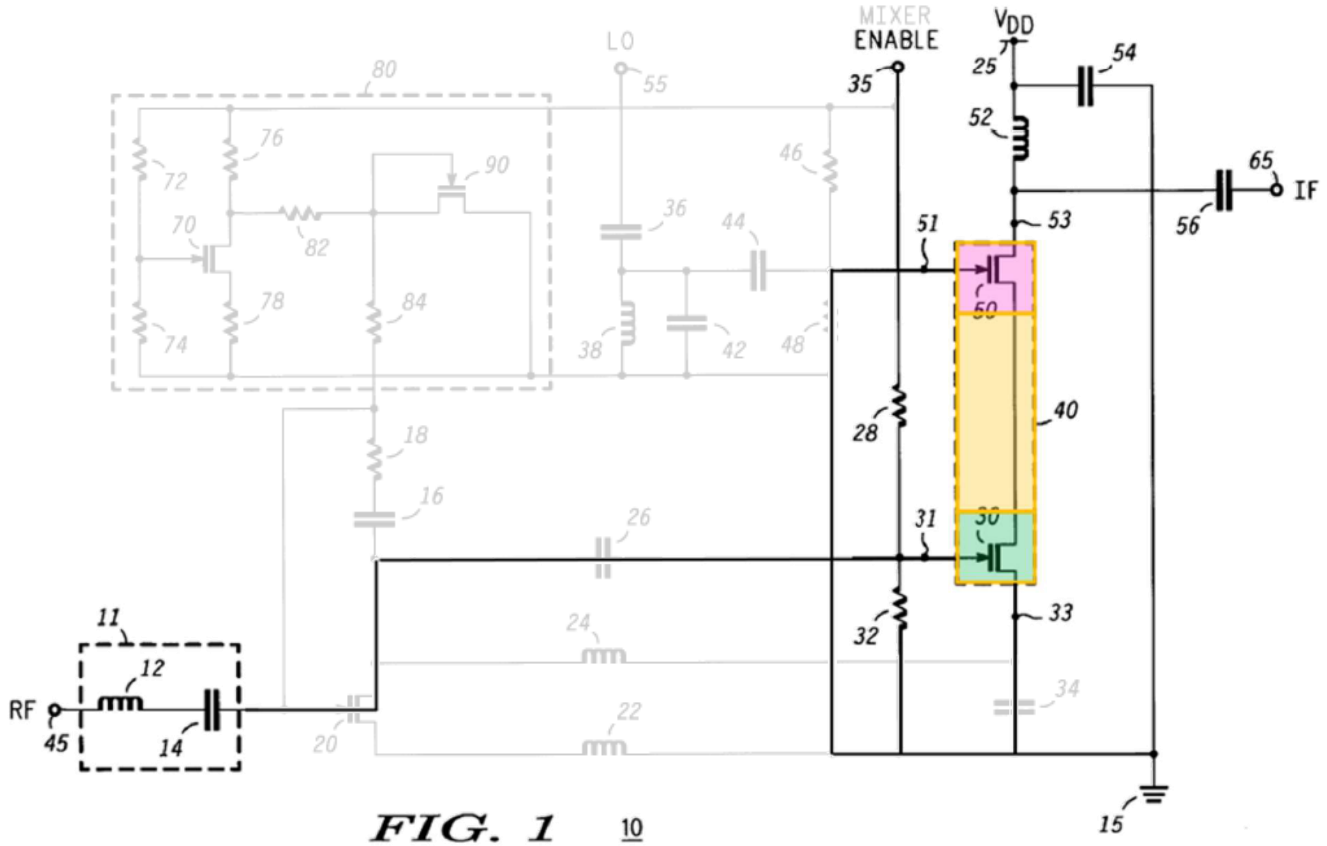


FIG. 1 10

Overlay of Bonn's Fig. 1 and the modified version in the Petition at 23; Ex-2004 ¶¶86-88; POR at 14-18; PO Reply at 8-9;

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Dr. Bernstein Testified that Bonn's Downconverter Was "Special" and "Complicated"

Dr. Bernstein

> And I think it's not normal in the state in the art depending on if you're in an RF -- if you're an RF engineer. I generally am not so familiar with down-converters, so I think that's why he spends a lot of time explaining it so that a POSITA would understand that this is a very sort of special application. Whereas, the normal application would be an amplifier.
>
> So he doesn't -- the reason I believe -- I don't know what Dr. Bonn or Mr. Bonn was thinking, but it seems the reason he spends a lot of time explaining this RF application is because it's not a usual application.
>
> So this circuit is a very complicated circuit and it's not clear -- since it's not connected to ground, I don't know who --

Ex-2009 at 44-45; POR at 14-15

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Bernstein Admitted that He Lacked Experience with RF Circuits and Downconverters

Dr. Bernstein

And I think it's not normal in the state in the art depending on if you're in an RF -- if you're an RF engineer. I generally am not so familiar with down-converters, so I think that's why he spends a lot of time explaining it so that a POSITA would understand that this is a very sort of special application. Whereas, the normal application would be an amplifier.

Q. So that's a great answer, but it didn't answer my question. Your modified figure on page 65 of your declaration, to your knowledge, that would not work as a down-converter; is that correct?

MR. MACDONALD: Objection to form.

A. As I said, I have no experience making down-converters and I don't know that you cannot make a down-converter with a single transistor. Maybe that you could.

Q. Okay. Would you agree with Bonn's description of a down-converter as converting a signal of one frequency to a signal of another frequency?

A. As I said, I'm not an RF circuit expert, so I have very little experience with down-converters and mixers, to be honest. So I could rely on Bonn to assume that he is teaching us correctly the application of a down-converter.

Admitted this 3x (Ex-2009, 46:18-22, 60:20-22, 72:20-22)

Ex-2009 at 44-46; 60:20-21, 72:20-21, 75:7-16, 77:15-17, ; POR at 14-15

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Petitioner Conceded that Dr. Bernstein "Lacked" "Experience with Downconverters and RF Signal Mixing Applications"

Petitioner's Reply

Although Dr. Bernstein honestly remarked he lacked extensive firsthand experience with downconverters and RF signal mixing applications, these statements enhance his credibility and are of no moment. Ex-2009, 44:16-17, 60:20-21, 72:20-21, 77:15-17. He does not need such expertise. The '003 patent specification and claims never mention signal mixing. Ex-1001. And he does not base his opinion on Bonn's signal mixing application.

Reply at 13

Just because Dr. Bernstein understood the technology he was looking to reconstruct through hindsight does not mean he can offer expert opinions on other topics on which he admits he lacks specialized expertise.

PO Reply at 9-11

Louis Vuitton Malletier v. Dooney & Bourke

"Testimony on ***subject matters unrelated to the witness's area of expertise is prohibited*** by Rule 702."

Louis Vuitton Malletier v. Dooney & Bourke, 525 F. Supp. 2d 558, 642 (S.D.N.Y. 2007) (citing *Seatrax v. Sonbeck Int'l*, 200 F.3d 358 (5th Cir. 2000))

XpertUniverse v. Cisco Sys.

Expert testimony "beyond [the witness'] expertise and knowledge" is "in the ***realm of speculation***."

XpertUniverse v. Cisco Sys., No. 09-cv-157, 2013 WL 865974, 10 at *3 (D. Del. Mar. 7, 2013)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Dr. Choi Testified that a POSA Would Not Have Scrapped Bonn's Downconverter

Dr. Choi

88. Unlike Dr. Bernstein, I am an expert in RF circuits, and I am familiar with both downconverters and mixers. In my expert opinion, I think it is safe to say that a POSA would not have had reason to modify a downconverter so that it no longer performs its most essential function, as the Petition and Bernstein Declaration contend.

Ex-2004 at ¶ 88

- **Petitioner did not depose Dr. Choi**
- **Petitioner did not challenge Dr. Choi's testimony in any way**

PO Reply at 11

Dr. Choi's Testimony is *Uncontested*

The Petition Picked Figure 7 Because Dr. Bernstein Did Not Understand Bonn

Petition

Based on these teachings, a POSITA would have found it obvious to modify the circuit of Figure 1 and use Figure 7's structure for high frequency signal amplification in place of mixer 40. Bernstein, [097].

Petition at 22

Dr. Bernstein

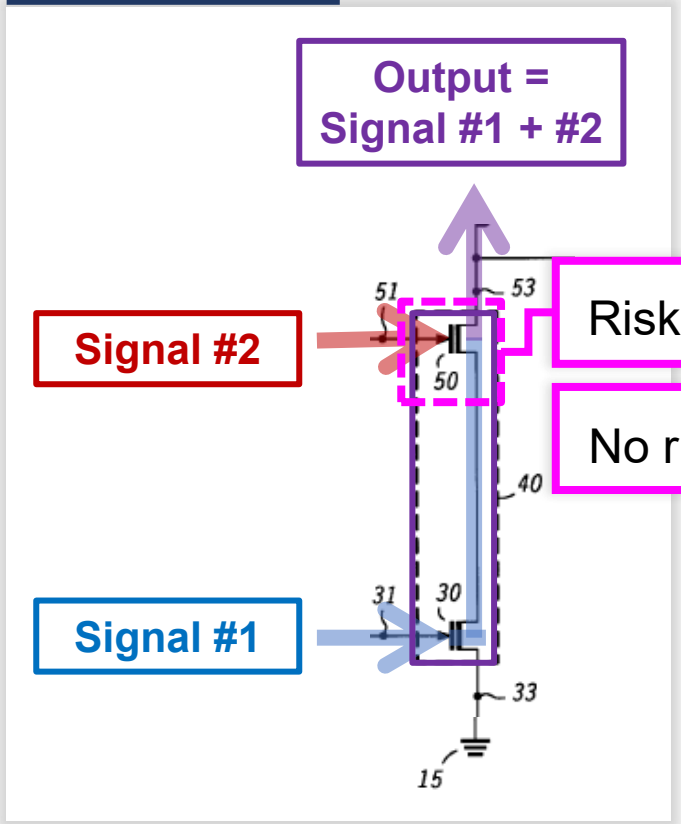
And I really -- to be honest, just to finish your question, I don't honestly understand what he means when he says current carrying capacity, other than the on state resistance, RDS, because by making the width narrower he's only making the resistance higher.

I don't know why you would do it, and that's why he has a nice figure 8 where none of it's -- he's doing it -- again, I don't understand enough about RF circuits. He's doing it for a very specific reason in his down-converters, and I do not know his reason.

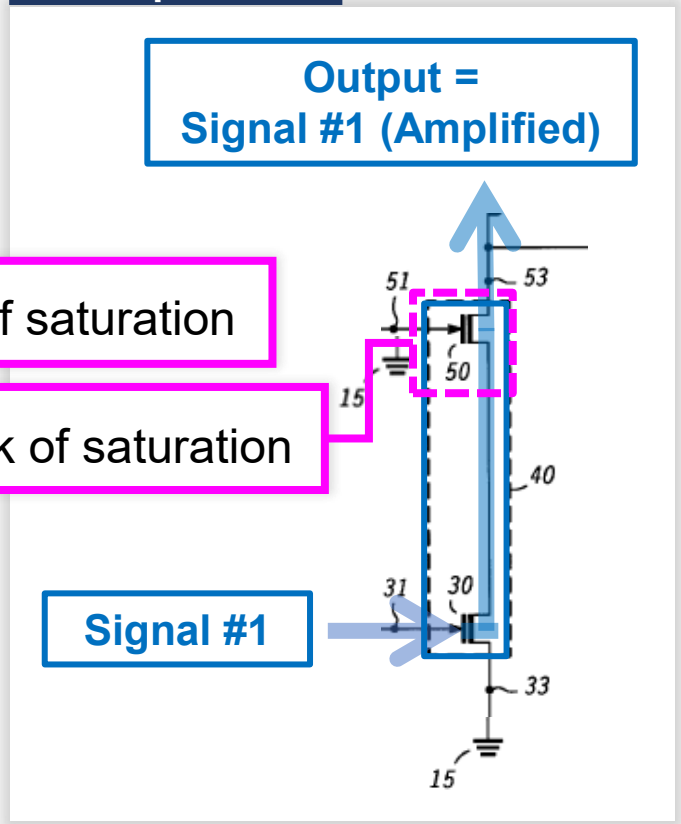
Ex-2009, 95:4-6, 99:22-101:1; POR, 23-24; PO Reply at 6-8

The Non-Conductive Sections Make Fig. 7's Structure Unsuitable as an Amplifier

Mixer



Amplifier



Dr. Choi

98. While such a transistor may be well suited as a mixer, a POSA would not have had reason to use it for a high frequency signal amplification because of the imbalanced current-carrying capacity under the two gates. When a dual-gate transistor is used as a mixer, two signals are combined to form one (desired) output. The imbalanced current-carrying capacity is desired to mitigate the undesirable effects (harmonic distortion, lower conversion gain, spurious mixing products, etc.)_associated with transistor saturation. In an amplifier, only a single signal is amplified, and so a transistor with equal current-carrying capacity is more suitable and provides better performance because that same signal must be carried through both top and bottom transistors.

105. Consequently, a POSA would not have embarked upon the extensive modifications to the overall downconverter circuitry of Figure 1 as proposed by the Bernstein Declaration to use the dual-gate FET of Figure 7 (purpose built for use in a mixer) as an amplifier because a POSA would have known that the dual-gate FET of Figure 7 was optimized for use as a mixer, as opposed to a high frequency signal amplifier.

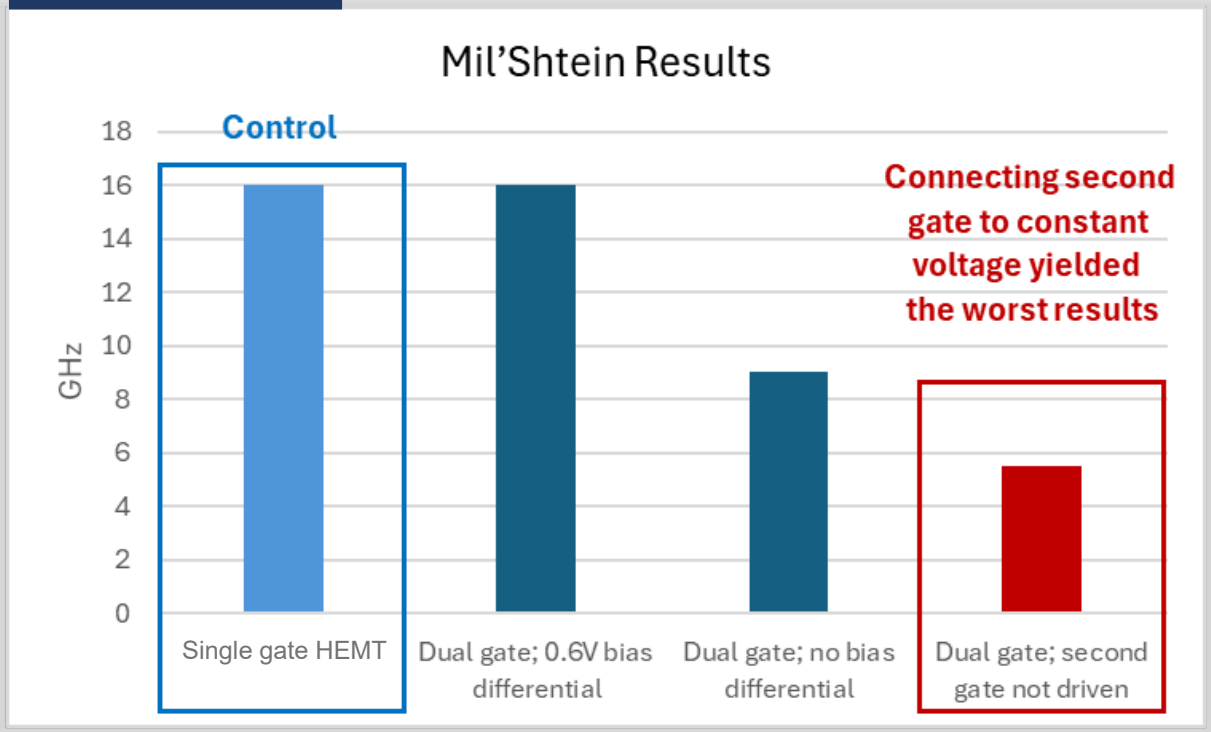
Ex-2004 at ¶¶ 98, 105; POR, 19-24; PO Reply at 6-8

Dr. Choi's Testimony is *Uncontested*

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Mil'Shtein Taught Connecting the Second Gate to a Constant Voltage Source, as Proposed by the Petition, Yielded the "Worst Results"

Dr. Choi



115. **Fourth,** when "the RF [was] injected into only the Schottky gate," meaning the second gate was held at a constant voltage as proposed by the Petition and then Bernstein Declaration, that "***yield[ed] the worst results*** with a unity limit of about 5.5 GHz." Ex-2006, 302.

Ex-2004 at ¶115;

Mil'Shtein

Modeling of *S*-parameters defined the magnitude of the S_{21} as a unity current gain of nearly 16 GHz for the normal HEMT. Tracking the results of the regular HEMT device closely is the TGB HEMT with the 0.6 V bias differential and the RF input injected into both gates. The TGB device with no bias differential and the RF injected into both gates results in a unity gain limit of about 9 GHz. The TGB device with the bias differential and the RF injected into only the Schottky gate yields the worst results with a unity limit of about 5.5 GHz.

Ex-2006 at 302

116. **Conclusion**: Mil'Shtein thus teaches that driving both gates of a dual-gate transistor in an amplification application resulted in better results than when only one gate was actively driven, which would have motivated a POSA to consider driving both gates of a dual-gate transistor, rather than connecting its upper (second) gate to a constant voltage source, as claimed in the '003 patent.

POR at 27-29; Ex-2004 at ¶¶ 110-116; Ex-2006 at 302; PO Reply at 13-18

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1 and 2 – Both Based on Bonn – Fail Because the Petition's Modifications to Bonn Are a Blatant Hindsight Reconstruction of the Claims

1

- Petitioner's modifications to Bonn's downconverter are supported only by the naked say-so of Dr. Bernstein, who "lacked" "experience with downconverters"
- Dr. Choi testified a POSA would not render Bonn's downconverter inoperable

POR at 14-15; Reply at 13; PO Reply at 9-11

2

- Bonn designed Fig. 7 as a mixer; a POSA would not have used it as an amplifier
- Petitioner failed to show a POSA would have used Fig. 7's structure to begin with

POR at 18-24; PO Reply at 6-8

3

- Bonn's downconverter already had an amplifier at FET 20
- The Petition failed to explain why a POSA would have scrapped it

POR at 24-25; PO Reply at 11-13

4

- Bonn never discloses connecting a second gate to a constant voltage source
- A 2005 article by Mil'Shtein discloses that doing so "yield[ed] the worst results"

POR at 26-30; PO Reply at 13-18

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

GROUNDS 2 & 3

NO REASONABLE EXPECTATION OF SUCCESS FOR MAKING A MERGED GaN TRANSISTOR

Dr. Choi: "Changing the core semiconductor technology ... is a profound change that a POSA would not have expected to be successful."

Ex-2004 at ¶150; POR at 30-46, 75-76; PO Reply at 18-21

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

In 2006, Making Silicon Transistors Was Unpredictable; GaN Even More So

Ex-2008

The "Copy Exactly" Process Technology

In recent research with colleagues at the University of California, Berkeley, and Georgetown University, Dr. Mowery and his group[13] found that innovation in semiconductor manufacturing processes, particularly the development and introduction of new process technology in this industry, retains a strong element of trial and error. It relies to a remarkably small extent on simulations or reliable, robust, predictive models.

A good example of this approach to process innovation is the so-called "copy exactly" philosophy that the Intel Corporation relies on in transferring process technologies among manufacturing plants. This approach to managing the development and transfer of process technologies concedes that in the absence of a complete understanding of the process technology it is necessary to copy the entire system—the length of pipes, the placement of equipment—exactly, rather than in a way that is based on engineering or scientific knowledge. This is a remarkable example of pre-scientific problem solving and trial-and-error experimentation in this industry. At the same time, however, semiconductor manufacturing process technology and manufacturing performance have benefited enormously from the application of computing technology to manufacturing process control, data capture, and analysis.

Ex-2008, 1414-EXPERT-0002277-788 (native page 69-70)

Dr. Choi

mode, not a combination of one of each). As a POSA would have known, there would have been nothing simple about creating a merged cascode transistor from GaN, much less would it have been likely to yield predictable results.

150. Changing the core semiconductor technology, which is what a switch from GaAs to GaN would entail, is a profound change that a POSA would not have expected to be successful, especially not without undue experimentation. A POSA would thus not have had a reasonable expectation of successfully modifying Bonn's dual-gate transistor to make it out of GaN, as the Petition and Bernstein Declaration propose for Ground 2.

Ex-2004 ¶¶ 149-150

Dr. Choi's Testimony is *Uncontested*

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

POR at 30-46, 75-76; PO Reply at 18-20

Ground 2: Petition's Alleged Predictability of a Dual-Gate GaN FET Is Unsupported

Petition

> The substitution of GaAs in Bonn's structure 300 with Ren's GaN materials would have predictably led to a cascode transistor with an enhancement mode GaN and a depletion mode GaN gate. Bernstein, [165]. Bonn's dual gate FETs have

Petition at 52

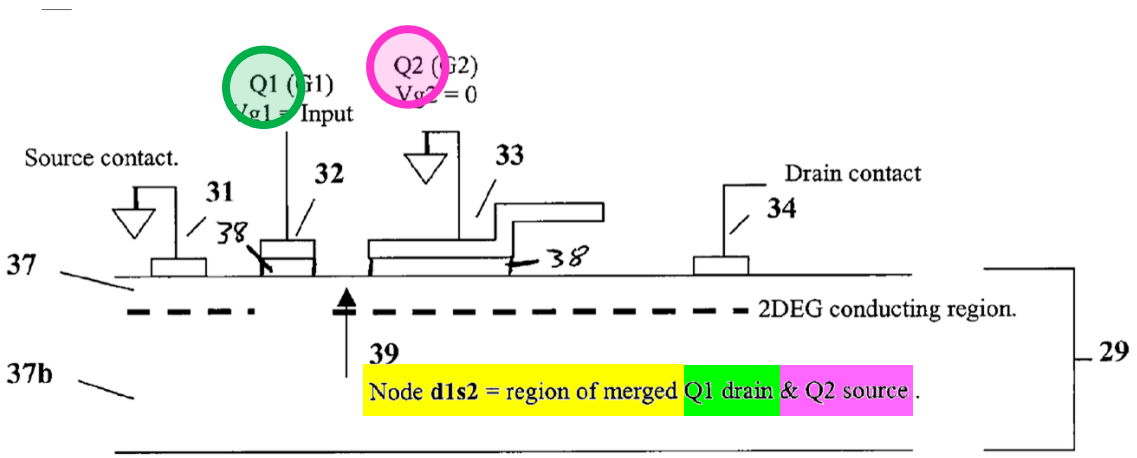
- **No prior-art support for Petition's allegations of predictability**
- **Predictability alone insufficient to establish a reasonable expectation of success**

POR at 30-46; PO Reply at 18-20

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’003 Patent Claims a *Merged* Dual Gate Transistor – Different than the Ordinary Prior Art Dual-Gate Transistors Connected by Wires

’003 Patent



tion mode transistor, and wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

Ex-1001 at Fig. 3, claim1

Sankin

wires connect transistors; no merged drain and source as claimed by the ’003 Patent

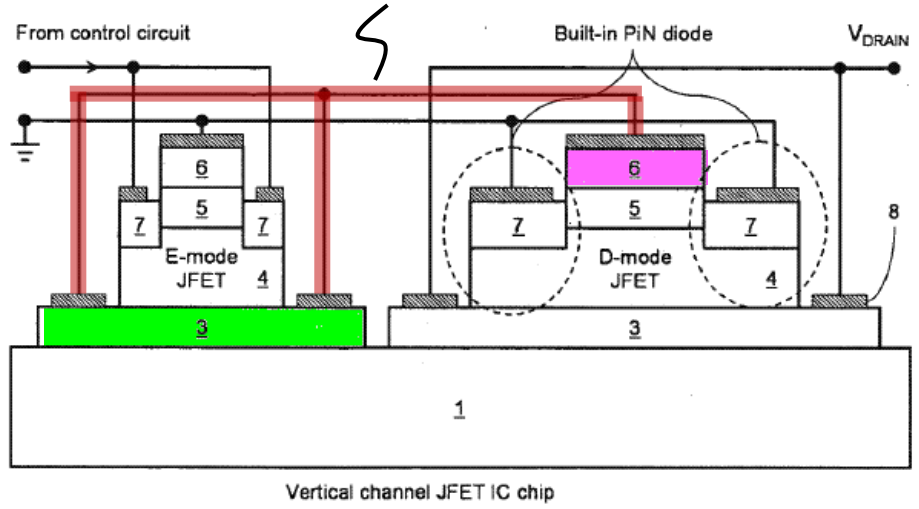


FIG. 2

Ex-2004 at ¶¶ 119-121,187; Ex-1018 at Fig. 2; Ex-2009 at 32:18-22

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 3: Predictably Turning a Single-Gate Depletion Mode Transistor Into an Enhancement Mode Transistor Is Irrelevant to Making a Merged Dual-Gate Transistor

Petition

Ren discloses an AlGaN over GaN structure, like Mishra, and Ren teaches forming enhancement mode or depletion mode by varying AlGaN thickness. Bernstein, [259]; Ren, ¶¶[0014], [0029], [0031]. A thinner layer leads to enhancement mode, while a thicker layer leads to depletion mode. Ren, ¶¶[0014], [0033]; § VI.C.

The combination would have implemented Ren's known option in Mishra's device for predictable results. Bernstein, [260]. Mishra already discloses a spacer,

Petition at 86

Dr. Bernstein

Q. And you don't allege that Ren discloses a dual-gate transistor; is that right?

A. Well, everything in Ren is really just about the gate, and he doesn't show any dual-gate of any transistor.

Ex-2009 at 123:6-10

Dr. Choi

230. Paragraph [260] of the Bernstein Declaration (and the corresponding portion of the Petition at pages 86-87) describes why a POSA might have known how to make a single-gate AlGaN/GaN enhancement mode transistor and a single-gate AlGaN/GaN depletion mode transistor based on the teachings of Ren, but Ren does not disclose a dual-gate transistor, let alone a dual-gate transistor having a drain region of an enhancement mode transistor merged with a source region of a depletion mode transistor. *See generally* Ex-1008. As such, Ren cannot possibly provide any evidence that a POSA would have had at least a reasonable expectation that such a dual-gate transistor would be made successfully or that one could be made with the same techniques used to make single-gate transistors.

Ex-2004 at ¶ 230

The Reply Has No Answer, Conceding the Point

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

POR at 75-76; PO Reply at 21

GROUND 3

MISHRA FAILS TO DISCLOSE OR RENDER OBVIOUS A MERGED DUAL-GATE TRANSISTOR

Dr. Choi: "a transistor 'with a dual gate structure' does not necessarily comprise a merged cascode transistor ... as claimed by the '003 patent."

Ex-2004 at ¶177; POR at 46-52, 62-74; PO Reply at 20-27

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Petitioner's Reply Changes Ground 3

Petition

The first and second stage transistors "can comprise a wide bandgap field effect transistor such as a GaN-based HEMT." Mishra, ¶[0057]; Bernstein, [250]. Mishra discloses biasing the cascode's source side gate (e.g., gate 62, Figure 5) at lower voltage and the drain side gate (e.g., field plate 66, Figure 5) at higher voltage. Mishra, ¶[0060]. Figure 10 shows an example.

The combination would have implemented Ren's known option in Mishra's device for predictable results. Bernstein, [260]. Mishra already discloses a spacer, dielectric, or passivation layer above the channel that is under the second gate but not under the first gate. *Id.*; Mishra, ¶¶[0028], [0035]-[0036], [0039], [0043].

Petition at 83, 86-87

Reply

Figure 5 depicts a single transistor amplifier with one gate.

Reply at 22

PO Reply at 21-22

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

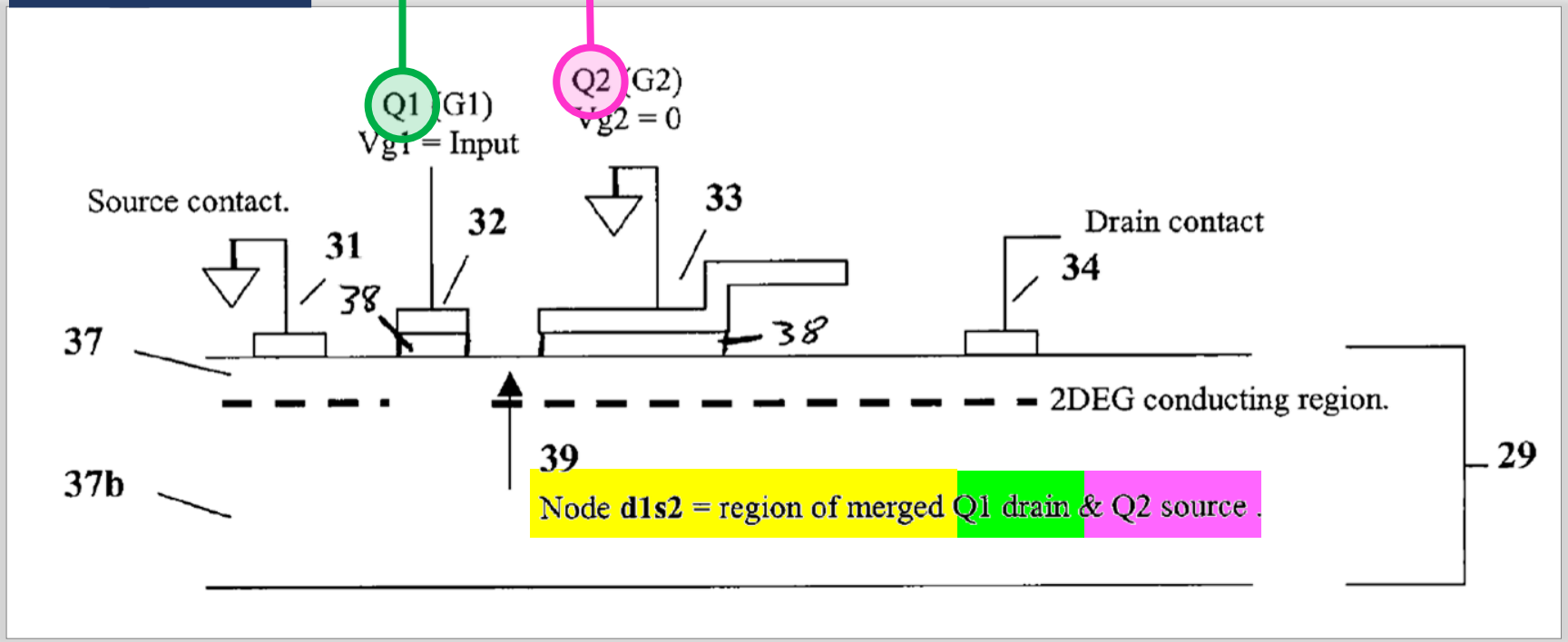
’003 Patent’s Merged Cascode Transistor

…enhancement mode transistor…

is merged with … [a] depletion mode transistor

Limitations [1C9] and [10C10]

’003 Patent



DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Mishra's Disclosure of a Dual-Gate Transistor Does Not Disclose a *Merged* Transistor

Mishra

[0062] It is understood that many different amplifier arrangements can be used according to the present invention. One alternative arrangement comprises a single transistor with a dual gate structure.

Sankin

Wires connect Q1 drain and Q2 source; they are not "merged" as claimed

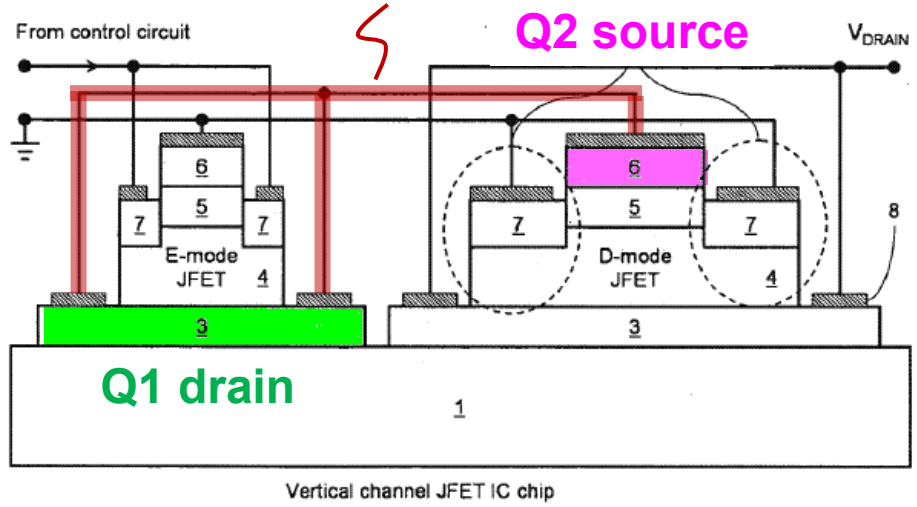


FIG. 2

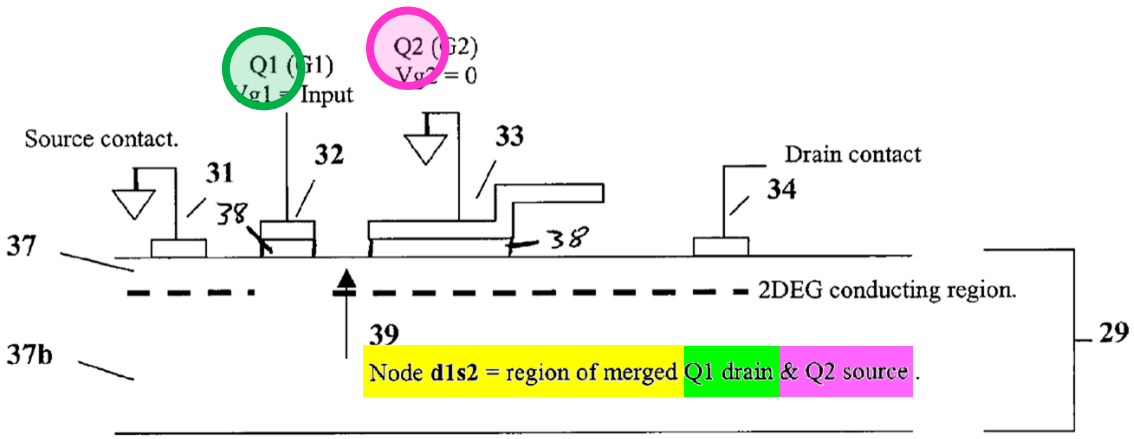
Ex-2004 at ¶¶ 119-121,187; Ex-1018 at Fig. 2; Ex-2009 at 32:18-22; POR at 62-70

Dr. Choi

[T]he disclosure of the ordinary, known concept, of a dual-gate structure would not be enough to amount to a disclosure, in the eyes of a POSA, of a dual-gate transistor of the type claimed by the '003 patent that comprises a drain region of an enhancement mode transistor that is merged with a source region of a depletion mode transistor.

Ex-2004 at ¶185

'003 Patent



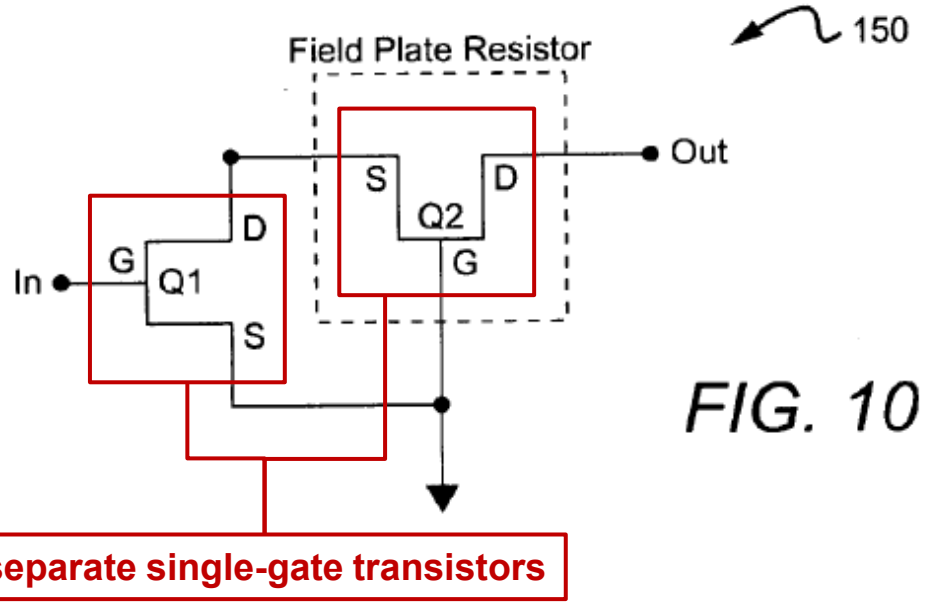
Ex-1001 at Fig. 3

Dr. Choi's Testimony is *Uncontested*

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

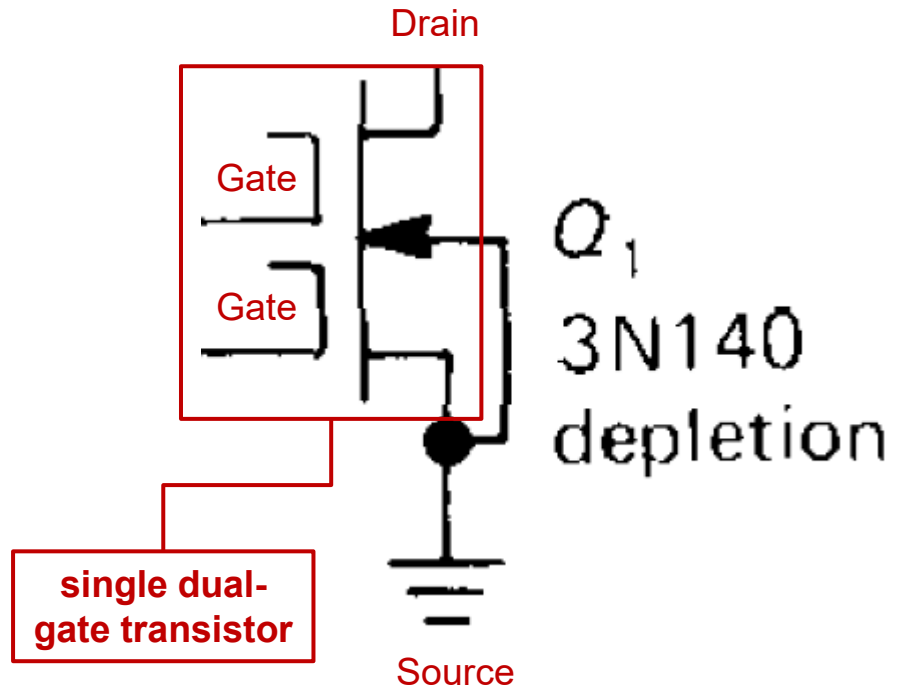
Mishra Fig. 10 Shows Two Single-Gate Transistors – Not a Dual Gate Transistor

Mishra



Ex-1009 at Fig. 10, [0058] ; Ex-2004 at ¶151

Horowitz



Ex-2002 at 883; Ex-2004 at ¶¶152-153; POR at 35-37

Dr. Choi

152. As a POSA would have known, Mishra's transistors are separate, ordinary, single-gate transistors ..., as opposed to a dual-gate transistor. A dual-gate transistor would have two gates belonging to the same device (not two separate devices), as shown in its circuit symbol ..., which a POSA would have readily recognized as a dual-gate transistor.

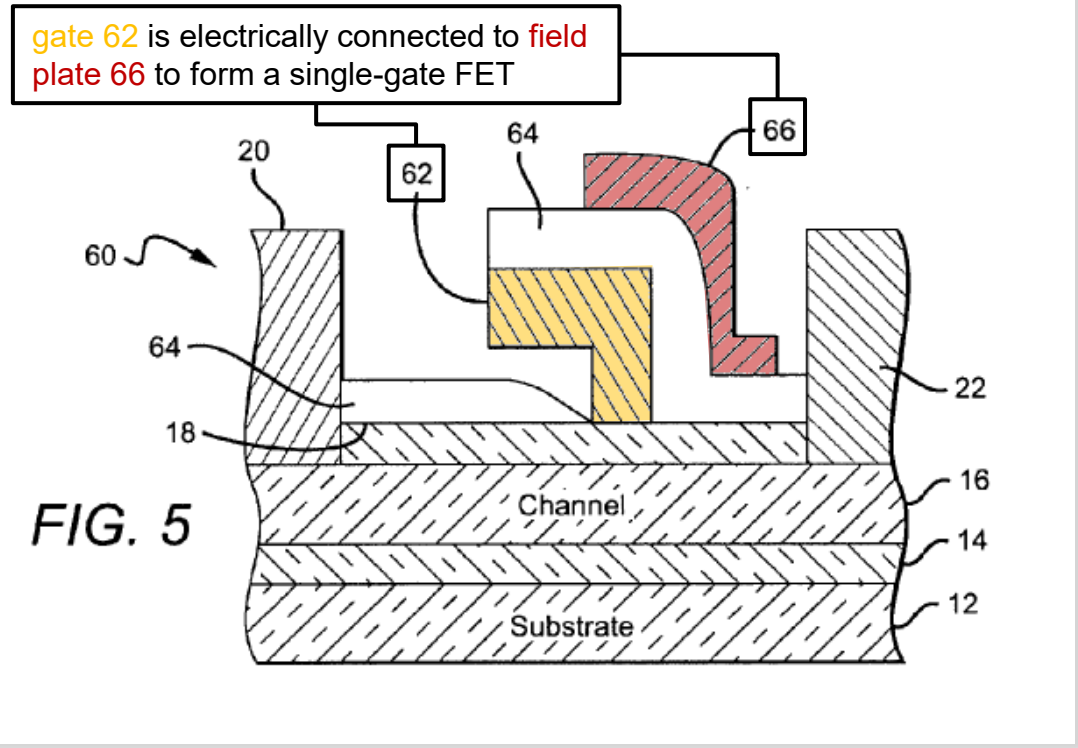
Uncontested

Ex-2004 at ¶152

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Dr. Bernstein Testified Fig. 5's Field Plate 66 Is Not a Gate

Mishra



Ex-1009 at Fig. 5, [0042]-[0043]; Ex-2004 at ¶¶ 156-158; POR, 39-40, 67-70

Dr. Bernstein

Q. So for the unmodified figure 5 of Mishra, Mishra itself does not disclose that figure 5 is a dual-gate structure; is that correct?

A. He calls 66 -- as I recall, he calls it a field plate and I don't think he commits himself to if it's enhancement mode, depletion mode. I think he's completely silent about that. He's just talking about the effect of the field plate in relation to the drain.

So this is between the gate and the drain, so it's a field plate and -- as disclosed in Mishra, which is why Mishra by itself, we're not only holding -- we're not only saying Mishra anticipates or --

Q. I appreciate that, and that's what I was asking.

But he obviously is showing you I can make this for many, many more gates. He did not suggest necessarily -- that's why I had to include the Ren combination. He's not telling us that that field plate is also a gate.

Ex-2009 at 153:2-16, 150:16-20

Petitioner Failed to Address Mishra's Missing Limitation

- The degree of Mishra's disclosure of how to implement its embodiments is immaterial because Petitioner does not dispute every one of Mishra's embodiments was a single-gate structure. Reply at 19-21; PO Reply at 21-22
- Mishra's disclosure of a source connected field plate is immaterial because Dr. Bernstein testified Mishra's field plate is not a second gate. Reply at 21-22; Ex-2009 at 153:2-14, 150:16-20 ("[Mishra is] not telling us that that [sic] field plate is also a gate."); POR, 39-40.PO Reply at 22-23.
- Whether it would have been obvious to implement Mishra's first gate in enhancement mode is immaterial to whether Mishra discloses a merged cascode transistor. Reply at 24-27; PO Reply at 26-27.

PO Reply at 20-27

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Conclusion: All Three Grounds Fail; All Claims Should Be Confirmed Patentable

Grounds 1 & 2	**Multiple Reasons a POSA Would Not Have Modified Bonn as Petition Proposes:** • **Dr. Bernstein admitted "I am not an RF circuit expert" three times and that he had "very little experience with down-converters" such as Bonn's** • Mil'Shtein taught the proffered configuration "yield[ed] the worst results"

POR at 10-13; PO Reply at 4-18

Grounds 2 & 3	**Failure to Establish a Reasonable Expectation of Success:** • In 2006, GaN was still an emerging and unpredictable technology • Petitioner failed to show a POSA could have predictably remade Bonn's transistor from GaN or Mishra's single-gate transistor into a merged dual-gate GaN transistor

POR at 30-46, 75-76; PO Reply at 18-20

Ground 3	**Missing Disclosure of a Merged Dual-Gate Transistor:** • Mishra's disclosure of the *genus* of dual gate transistors fails to disclose the specific *species* of merged dual gate transistor claimed • Petitioner identifies no other prior art evidence to fill this evidentiary gap

POR at 46-52, 62-74; PO Reply at 20-27

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Additional Slides

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Claimed Merged Cascode Transistor Circuit

'003 Patent

All claims require:

1. An enhancement mode transistor *merged with* a depletion mode transistor

2. A second gate that is connected to a constant voltage source

Claims 2-16 require:

3. III-Nitride layers or materials, of which GaN and AlGaN are examples

POR at 1, 32-33

1. A merged cascode transistor circuit comprising:
an input voltage signal source having an input voltage signal;
a constant voltage source having a predetermined constant voltage;
a merged cascode transistor comprising:
a semiconductor element;
a source electrode electrically connected to a top surface of the semiconductor element;
a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level, wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

2. The merged cascode transistor of claim **1**, wherein the semiconductor element further comprises:
a first III-Nitride layer; and
a second III-Nitride layer on which the first III-Nitride layer is positioned such that a 2DEG conduction layer forms between the first and second III-Nitride layers, wherein the source electrode and the drain electrode are ohmically connected to the first III-Nitride layer.

10. A merged cascode high electron mobility transistor circuit comprises:
an input voltage signal source having an input voltage signal;
a constant voltage source having a predetermined constant voltage;
a merged cascode transistor comprising:
a first epitaxial layer of III-Nitride material;
a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;
a source electrode electrically connected to the first epitaxial layer;
a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;
a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and
a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;
wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level, wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

EX1001 at Claims 1, 2, 10

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

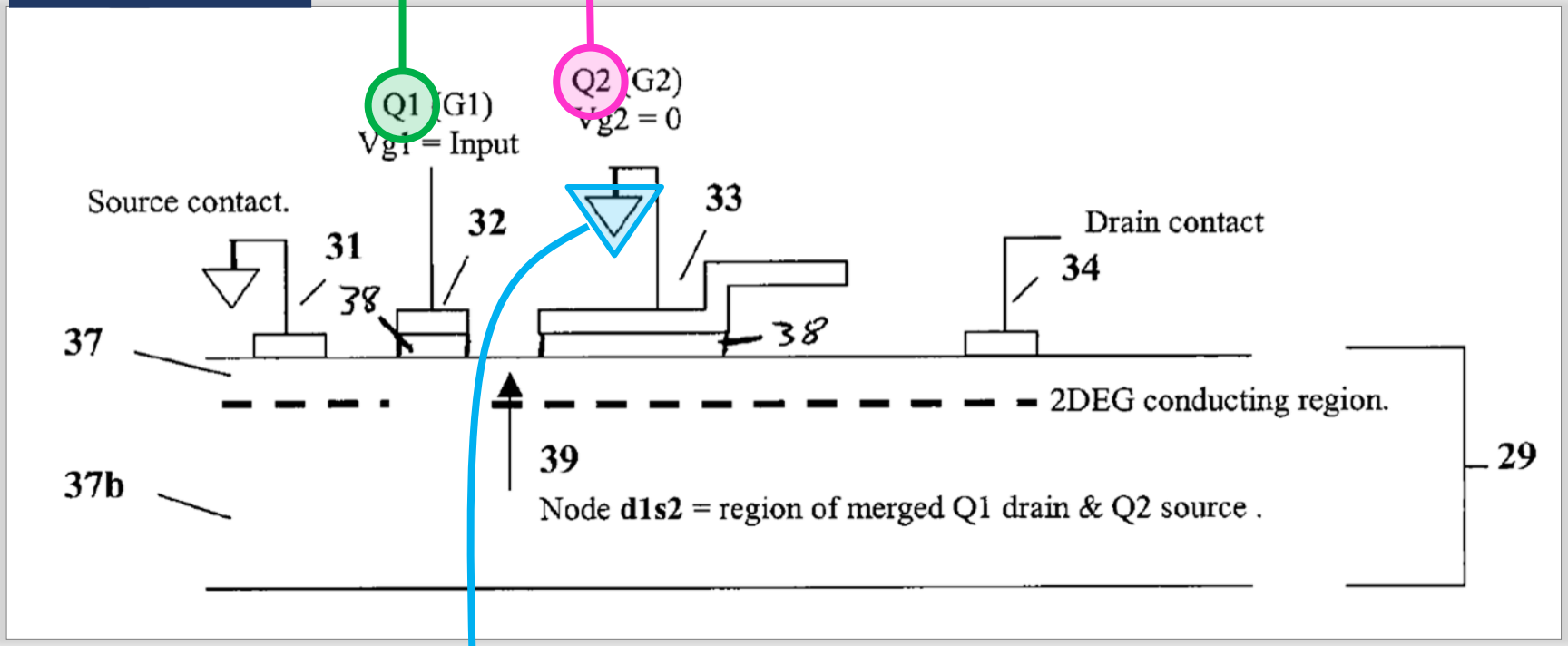
Figure 3: Merged Cascode Transistor Circuit

…enhancement mode transistor…

is merged with … [a] depletion mode transistor

Limitations [1C9] and [10C10]

’003 Patent



the second gate is connected to [a] constant voltage source…

Limitations [1C7] and [10C8]

POR at 1

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Bonn's Suggestion to Tailor its Transistor Was Not an Invitation to Destroy its Downconverter

Bonn

By now it should be appreciated that a downconverter and a method for generating an IF signal have been provided. The LNA and the mixer in the downconverter of the present invention are coupled in a single DC path, thereby reducing the power consumption. In a preferred embodiment of the present invention, the mixer is a dual gate FET with independently adjustable gate width and channel properties. The dual gate FET uses less chip area than two FETs in a cascode configuration. Furthermore, the parameters such as gate width, dopant concentration, and channel depth, under each gate of the dual gate FET are individually adjusted for optimum performance. Therefore, the dual gate FET structure of the present invention can be tailored to provide superior performance over the prior art dual gate FET structures in high frequency signal mixing as well as other applications such as high frequency signal amplification.

Ex-1006 at 11:22-37

Dr. Choi

sought to change the operating principle of Bonn's downconverter circuitry. While Bonn states that its dual-gate transistor can be "tailored" for use in "other applications such as high frequency signal amplification" (*id.*, 11:34-37), this sentence, in context, is referencing transistor properties (gate width, dopant concentration, etc.). Bonn is not teaching "tailor[ing]" the circuit of Fig. 1 to transform a downconverter into an amplifier. A POSA would not have made the

Ex-2004 at ¶80

Dr. Choi's Testimony is *Uncontested*

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

POR at 11-12

Modifications that Render a Reference Inoperable Are Not Ones a POSA Would Make

In re Gordon

A modification that would have rendered the primary reference "inoperable for its intended purpose" is not one a POSA would have made

In re Gordon, 733 F.2d 900, 902 (Fed. Cir. 1984)

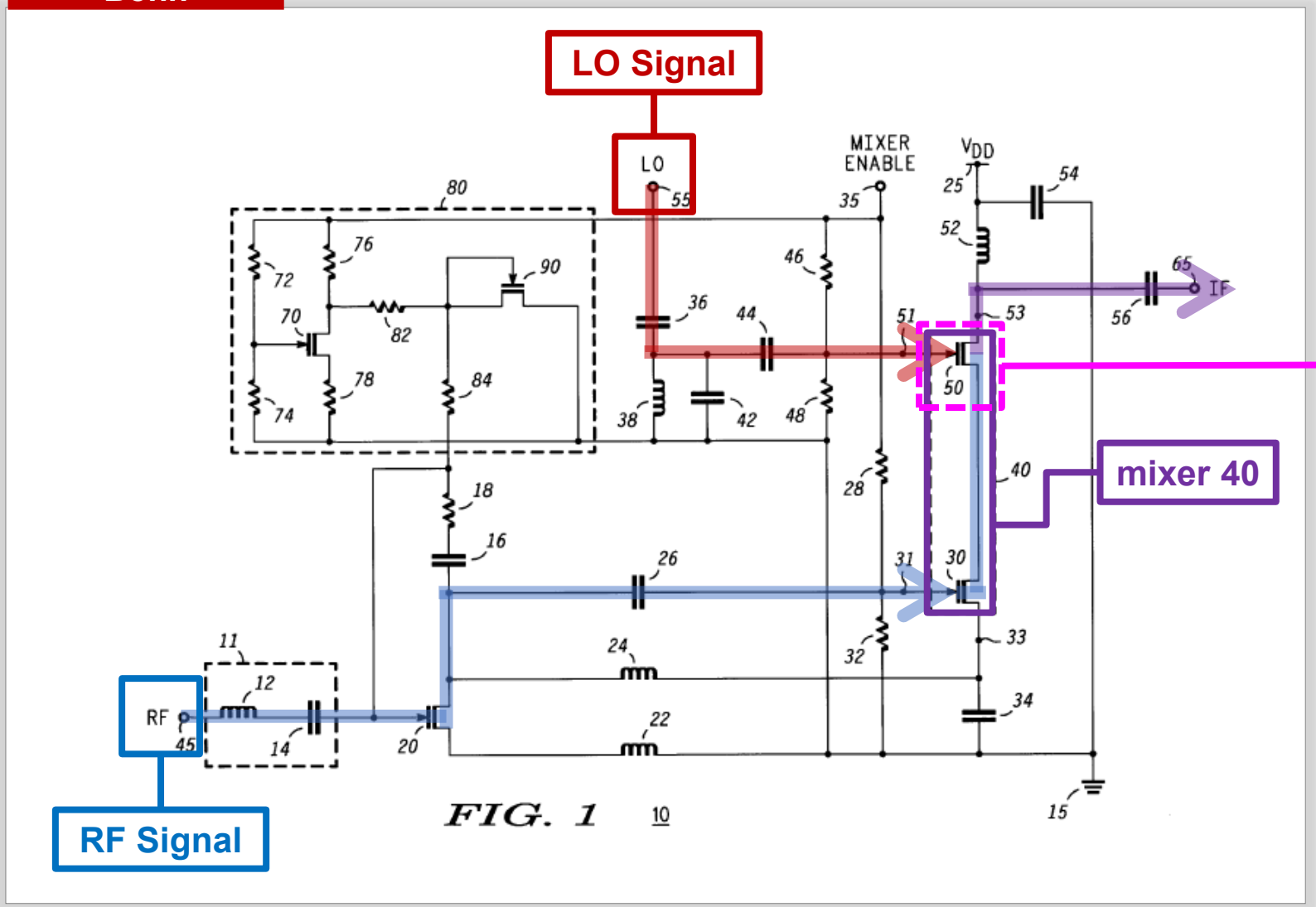
In re Ratti

A combination does not render a claim obvious when it would have changed the "basic principles" under which the primary reference "was designed to operate"

In re Ratti, 270 F.2d 810, 813 (C.C.P.A. 1959)

Bonn's Downconverter Combines Two Signals, Risking Current Saturation

Bonn



Bonn recognized that if the **RF signal** was too "strong," that could drive the second transistor of the mixer (50) "***into current saturation***."

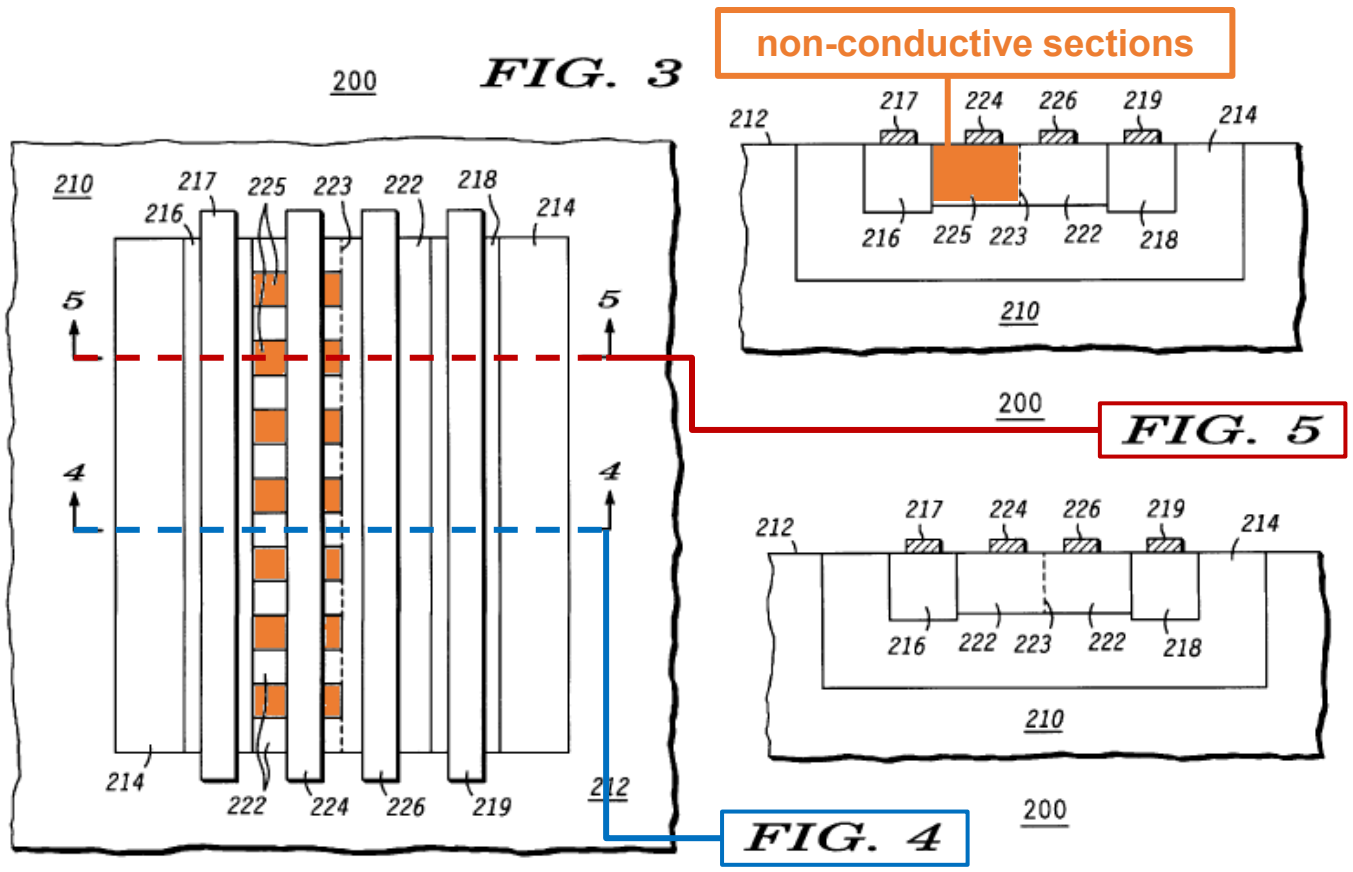
Ex-1006, 5:37-41, 5:46-52; Ex-2004 ¶93.; POR, 19

Ex-1006 at 2:11-13 , Fig. 1; Ex-2004 at ¶¶ 89-105; POR, 19-24; PO Reply at 6-8

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Bonn's Dual-Gate Transistor Had Non-Conductive Sections to Avoid Saturation

Bonn



Figs. 3-5 show **non-conductive sections** in the first gate region, **not** the second:

> Non-conductive sections **225** reduce the effective channel width of the first gate region in structure **200**. Therefore the current conducting capacity of the first gate region is smaller than that of the second gate region. By adjusting the number of non-conductive sections **225** and the width of each non-conductive section **225**, the gate width of first gate structure **224** is adjusted independently of the gate width of second gate structure **226**.

Ex-1006 at 7:10-17

Bonn teaches **Fig. 7 has the same structure as Figs. 3-5**:

> It should be understood that non-conductive sections like non-conductive sections **225** in structure **200** of FIG. **3** can be formed in first gate region **321**, second gate region **322**, or both, to individually adjust the gate width of each gate. It should also be understood that the channel depth of first gate

Ex-1006 at 9:12-15

Ex-1006 at 7:10-11, 7:22-34, 7:59-64, Figs. 3, 4, and 5, 9:12-19; Ex-2004 at ¶¶ 89-105; POR, 19-24; PO Reply at 6-8

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Reply's Invitation to Consider Bonn's "Flexible Disclosure" Should Be Declined

- The Reply argues that Bonn has a "flexible disclosure," that its non-conductive sections were "optional" and could be arranged differently, so the Petition did "not need to propose" modifications to Figure 7. Reply, 9-11
- Petitioner must make its case "with particularity" ***in the Petition***
  35 U.S.C. § 312; 37 C.F.R. § 42.22 (requiring a "detailed explanation")
- Petition chose to use Fig. 7's structure as-is, without modification

"I might have come up with a better rationale had I bothered" is not an argument that the PTAB should endorse

PO Reply at 6-7

The Board's Role Is Not to Fix the Petition or Petitioner's Expert's Problems

SAS Inst., Inc. v. Iancu

The Board does not "enjoy[] a license to depart from the petition and institute a different *inter partes* review of [its] own design."

SAS Inst., Inc. v. Iancu, 138 S. Ct. 1348, 1356 (2018)

In re Magnum Oil Tools Int'l, Ltd.

The Board must "base its decision on arguments that were advanced by a party" and has no power to "raise, address, and decide unpatentability theories never presented by the petitioner."

In re Magnum Oil Tools Int'l, Ltd., 829 F.3d 1364, 1381 (Fed. Cir. 2016)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

The Petition Fails to Explain Why a POSA Would Not Have Used Amplifier 20

- The Petition failed to explain why a POSA would have extensively modified Figure 1 to repurpose mixer 40 as an amplifier when the downconverter in Figure 1 already has an amplifier at FET 20 POR, 25
- The Reply argues that Bonn's disclosure of FET 20 does not "negate" its teaching that a dual-gate transistor could be used as an amplifier Reply, 7
- Must be some articulable reason other than hindsight

PO Reply at 11-13

Pers. Web Techs., LLC v. Apple, Inc.

Just because prior art elements "could be combined" "is not enough."

Pers. Web Techs., LLC v. Apple, Inc., 848 F.3d 987, 994 (Fed. Cir. 2017).

Belden Inc. v. Berk–Tek LLC

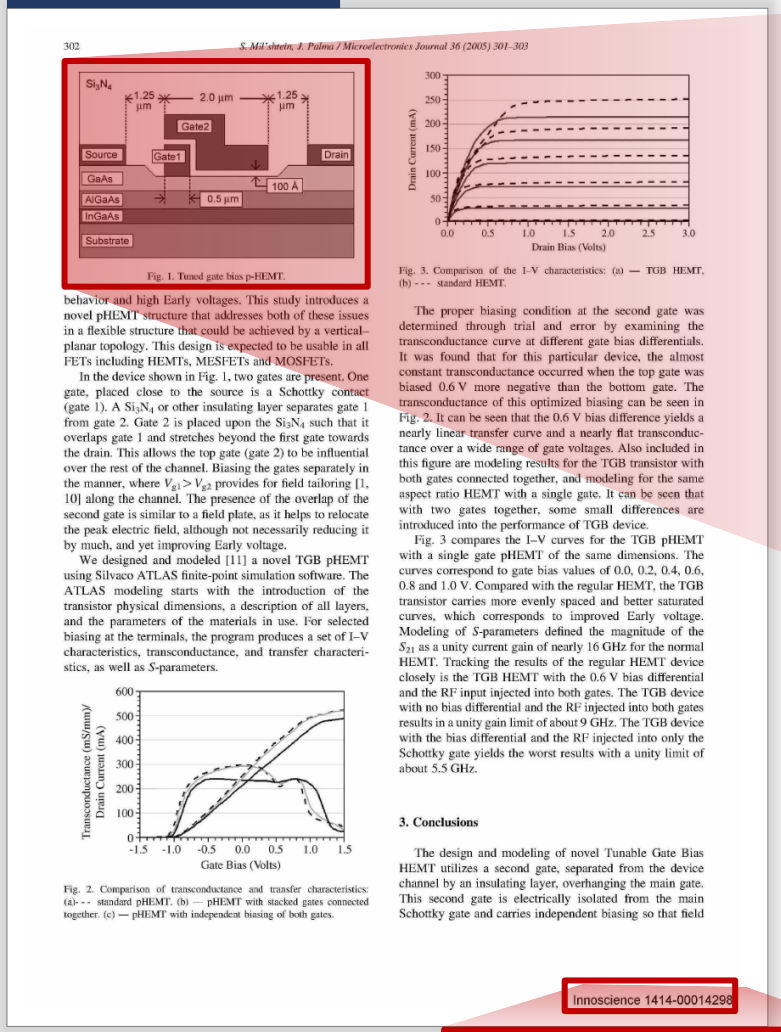
"Obviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention."

Belden Inc. v. Berk–Tek LLC, 805 F.3d 1064, 1073 (Fed. Cir. 2015)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Mil'Shtein Compared the Performance of a Dual-Gate Transistor Using Different Gate Bias and Driving Conditions

Mil'Shtein



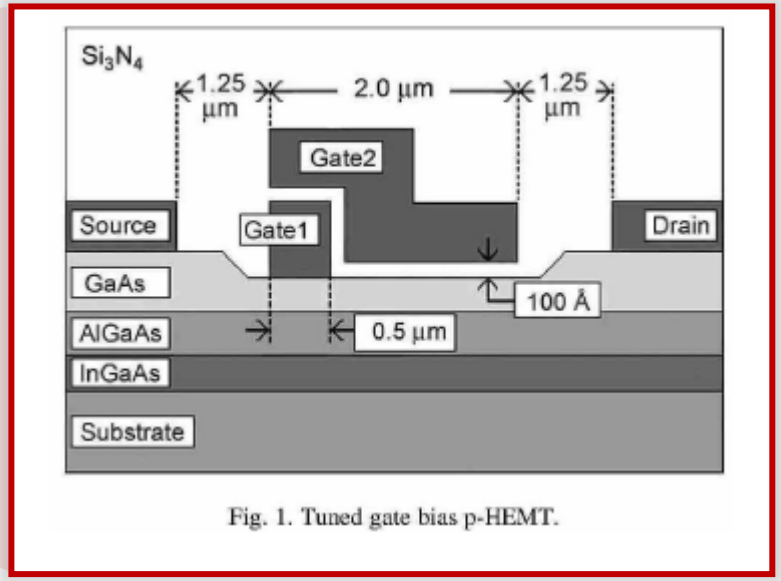


Fig. 1. Tuned gate bias p-HEMT.

Ex-2006 at 302

Dr. Bernstein was "very familiar" with the Mil'Shtein article because he "looked at [it] in [his] own background research."

Innoscience 1414-00014298

Innoscience 1414-00014298 **Petitioner produced Mil'Shtein in the co-pending ITC Investigation**

Dr. Bernstein

A. Okay. Oh, yeah, that's my good friend Mil'shtein. He's a big Israeli.

THE WITNESS: He'll be very happy to have people reading his papers.

MR. MACDONALD: Are we entering this as an exhibit?

THE WITNESS: I have seen this before. I'm pretty sure I've seen this before. It's one of our exhibits. I know that I've seen this --

MR. MACDONALD: Okay.

THE WITNESS: -- because I looked at this in my own background research.

Q. And you mentioned that you've, in fact, seen this particular article before; is that correct?

A. That is correct. It's very familiar to me. I don't remember exactly when I saw it, but fairly recently in my own --

Ex-2009 at 173:16-175:7

POR at 27-29; Ex-2004 at ¶¶ 110-116; PO Reply at 13-18

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

The Reply's Arguments Miss Their Marks

- Any advantages a dual-gate transistor had over a single-gate transistor are irrelevant because Bonn's transistor was already a dual-gate transistor. PO Reply at 15-16; Reply at 7-9.
- That connecting the second gate to ground still "amplified signals below 5.5 GHz" is irrelevant because the Petition proposed using the transistor for "high frequency amplification," or frequencies of "10 GHz." PO Reply at 16; Reply at 8; POR at 54; Ex-2004 ¶204.
- Mil'Shtein may have only "assessed one parameter," but Petitioner does not contest Dr. Choi's testimony that parameter was enough to dissuade a POSA from using the proposed approach given that it "yield[ed] the worst results." Reply at 8-9; Ex-2004 at ¶116; POR at 29; PO Reply at 16-17.
- Infineon never argued "teaching away." Reply at 7-8; POR at 27-29; PO Reply at 17.
- Infineon was forced to introduce Mil'Shtein because Petitioner concealed it; Dr. Bernstein admitted he reviewed Mil'Shtein as part of his background research. Reply at 7-8; Ex-2009, 173:16-175:7; POR, 27 n.4; PO Reply at 17-18.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Reply's Argument on the Ground 2 Combination Is Contrary to the Petition

Reply

Patent Owner does not dispute those benefits. POR, 31-32 It instead argues "Ren has no disclosure of how to make a ***dual-gate*** GaN ~~transistor~~" POR, 31 (emphasis original). That was never the combination. Bonn teaches individually

Reply at 14-15

Petition

A POSITA would have been motivated to implement Bonn's dual gate FET 300 of Figure 7 in a modified Figure 1 circuit, below, with predictable success

It would have been obvious to make Bonn's device out of GaN ~~semiconductor~~ materials, as Ren discloses, to achieve the benefits of GaN-based transistors, whose technology had improved by the time of the '003 patent. Bernstein, [157]-[165].

Petition at 49-50

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

PO Reply at 18

No Dispute Mishra's Figs. 2, 3, 4, 6, and 8 Are Single-Gate Transistors

Mishra

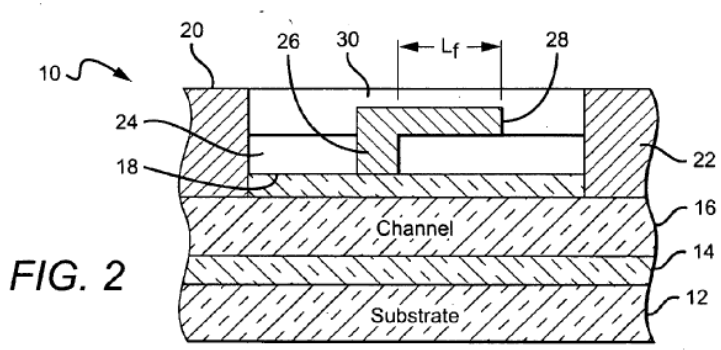


FIG. 2

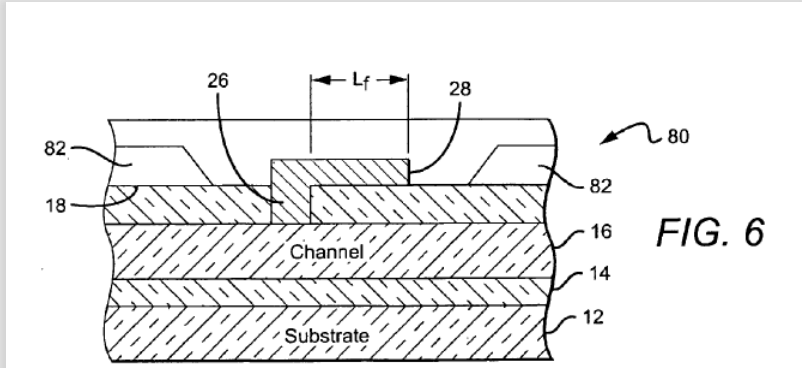
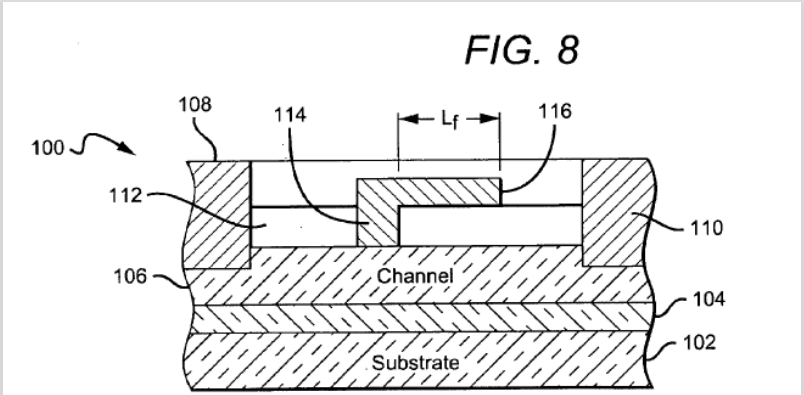


FIG. 6



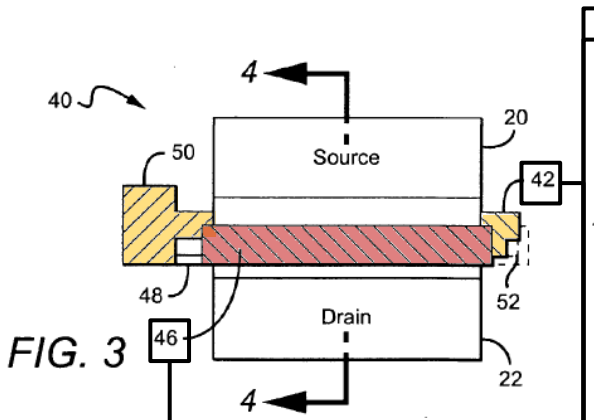


FIG. 3

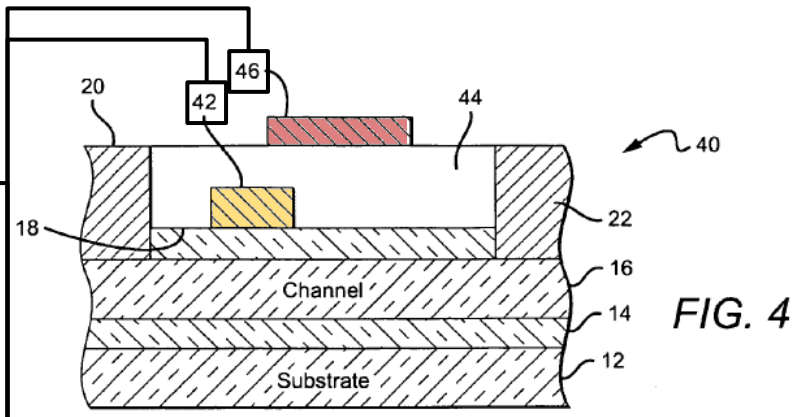


FIG. 4

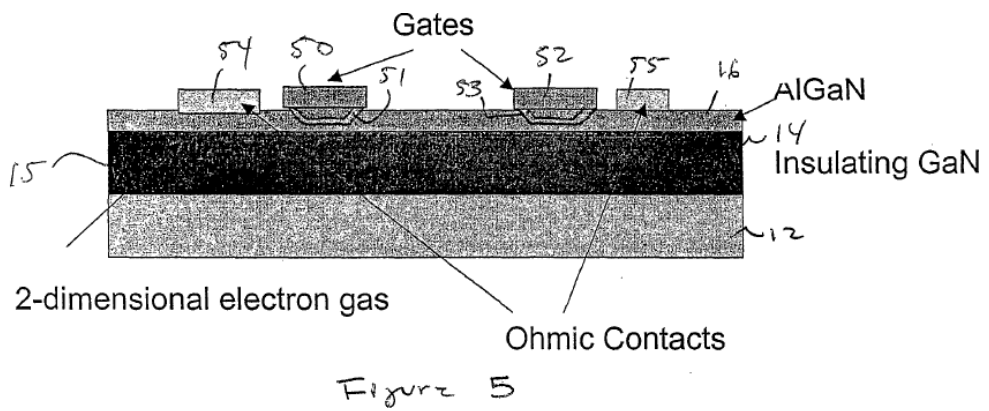
gate 42 is electrically connected to field plate 46 to form a single-gate FET

Ex-1009 at Figs. 2-4, 6, 8; Ex-2004 ¶¶ 154-155; Ex-2009, 124:12-125:1, 125:20-127:3; POR at 37-39

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Beach's Dual Gate Transistor Had the Same Mode For Both Gates

Beach



Ex-1020 at Fig. 5, [0048], [0051]

Dr. Choi

170. Beach thus does not disclose the structure of a dual-gate GaN transistor with an enhancement mode transistor merged with a depletion mode transistor, does not disclose the operation of such a dual-gate GaN transistor, and does not disclose how such a dual-gate GaN transistor would be made. Beach thus provides no enabling disclosure of the type of dual-gate transistor claimed by the '003 patent and is, therefore, not evidence that a POSA would have had a reasonable expectation of success in making the combination set forth in Ground 2.

Ex-2004 at ¶170

Dr. Bernstein

Q. Okay. So figure 5 shows two enhancement mode gates next to each other, correct?

A. I -- again, if the specification tells you that their intention is to have two enhancement modes -- much like as we said before, Bonn in his circuit with the mixers -- it looks like those both have to be enhancement modes because they were above zero.

Q. And you're not relying on Beach as disclosing an enhancement mode gate next to a depletion mode gate in your report, correct?

A. Right. I do not.

Ex-2009 at 159:22-160:6, 161:1-4

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

POR at 43-45

Petitioner Cannot Fill In Mishra's Missing Limitation Without Prior Art Evidence

Arendi S.A.R.L. v. Apple Inc.

Missing limitations can only be supplied through common sense if "the limitation in question [is] unusually simple and the technology particularly straightforward."

Arendi S.A.R.L. v. Apple Inc., 832 F.3d 1355, 1362 (Fed. Cir. 2016)

DSS Tech. Mgmt., Inc. v. Apple Inc.

"we have invoked common sense to fill in a missing limitation only when the limitation in question was unusually simple and the technology particularly straightforward."

DSS Tech. Mgmt., Inc. v. Apple Inc., 885 F.3d 1367, 1374 (Fed. Cir. 2018)
(quoting *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016))

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

POR at 71-73

A POSA Would Have Overlooked Mishra's Reference to a "Field Gate"

Dr. Bernstein

Q. So do you think Mishra just made a mistake when typing field plate versus field gate?

A. Had he said field gate in the first place instead of gate (sic) I think he probably would not have -- it wouldn't really change the meaning.

And I think in his mind as -- you know, it's interesting he does use the word gate here as we're using it, but it might be -- I don't know. I don't know what was in his mind when he wrote this.

Q. And what about a POSITA reading that? You mentioned that you hadn't picked up on that until now. Do you think a POSITA would have understood that as the field plate structure that he consistently describes?

A. What languages is used for that piece of metal I don't think would make a difference in the mind of a POSITA because it is what it is. You know, it's a piece of metal that goes over the conformal coating of the insulator.

I think a POSITA would see that this insulator is conformal. It's pretty much continuous and that's just the metal that goes on top of it. Probably a POSITA would overlook that word "gate" or "plate" as I did.

Ex-2009 at 197:16-198:8

Dr. Choi

field plate connected to the gate or physically a part of it. While Mishra uses the phrase "field ***gate***" as opposed to "field ***plate***" in paragraph [0029], given that Mishra consistently describes the structure as a field plate (not a second gate), a POSA would not have understood paragraph [0029] as disclosing a second gate.

Ex-2004 at ¶165; POR at 43

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Petition Provides No Reason to Select Figure 5 to Implement the Dual Gate Transistor

Mishra

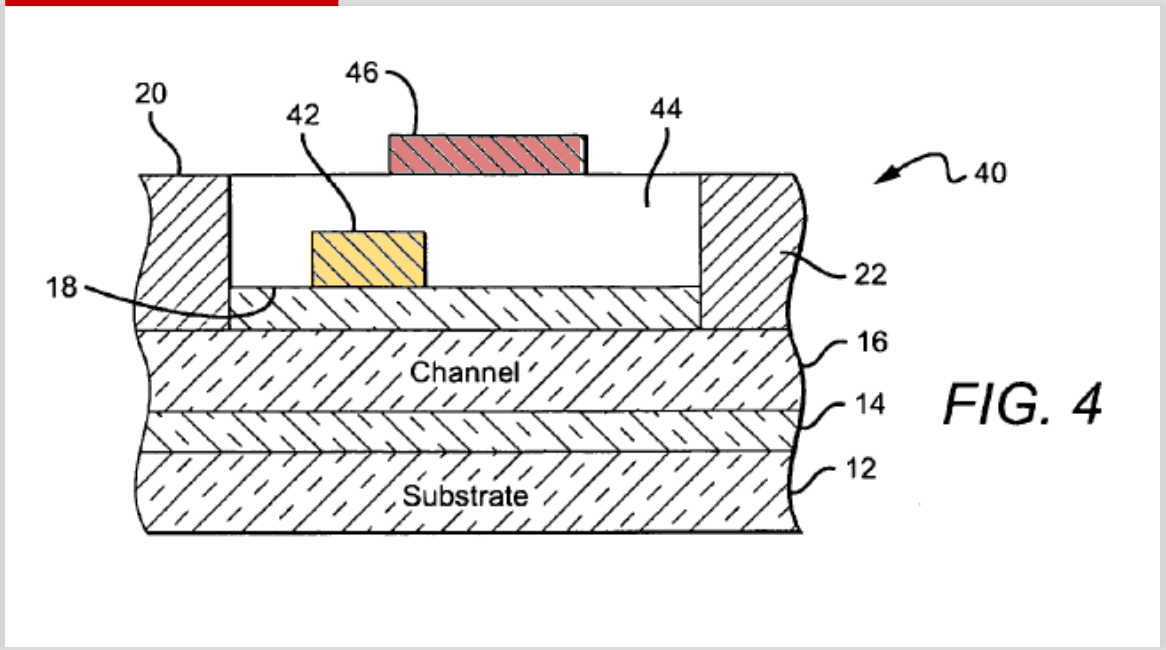


FIG. 4

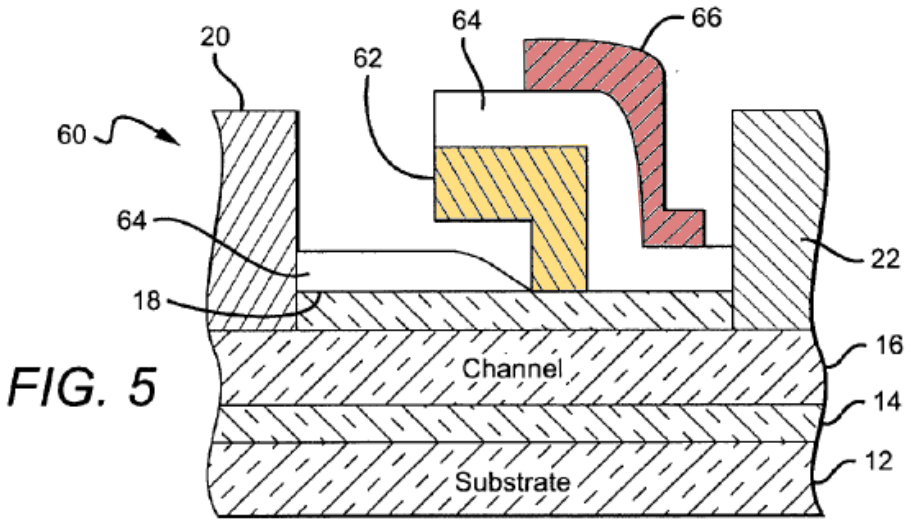


FIG. 5

Ex-1009 at Figs. 3-5; Ex-2004 ¶¶ 215-228; POR at 62-66; PO Reply at 25

Pers. Web Techs., LLC v. Apple, Inc.

Just because prior art elements "could be combined" "is not enough."

Pers. Web Techs., LLC v. Apple, Inc., 848 F.3d 987, 994-94 (Fed. Cir. 2017).

Belden Inc. v. Berk–Tek LLC

"Obviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention."

Belden Inc. v. Berk–Tek LLC, 805 F.3d 1064, 1073 (Fed. Cir. 2015)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Petition Provides No Reason to Connect Fig. 5's Field Plate to the Source

Mishra

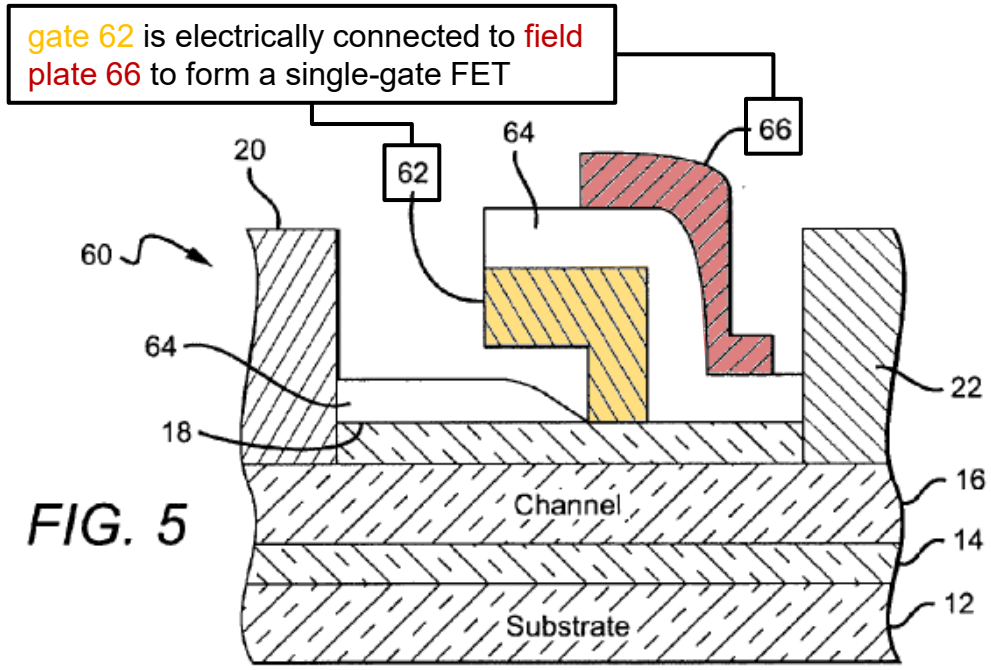


FIG. 5

[0044] Like the field plate **46** shown in **FIGS. 3 and 4** and described above, the field plate **66** can be connected to the gate **62** in many different ways. A first conductive path (not

Ex-1009 at Fig. 5, [0044]

Dr. Bernstein

But he obviously is showing you I can make this for many, many more gates. He did not suggest necessarily -- that's why I had to include the Ren combination. He's not telling us that that field plate is also a gate.

Ex-2009 at 150:16-20, 153:2-14

Dr. Choi

implying that Mishra discloses that field plate 66 is grounded. *Id.* While Mishra does mention the field plate may be connected to the source (Ex-1009, [0029], [0062]), Mishra never describes Figure 5 as having such a connection, rather, describing that field plate 66 connects to the grate 62 (*id.*, [0044]). The Bernstein

Ex-2004 at ¶157

Dr. Choi's Testimony is *Uncontested*

PO Reply at 23-26

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Petition's Reason For Selecting an Enhancement Mode Followed by a Depletion Mode Is Unsupported

Petition

Mishra does not explicitly comment on the mode in which Q1 operates, but a POSITA would have found enhancement mode obvious. Bernstein, [251]-[252]. A POSITA would have understood Mishra's low voltage bias of source side transistor (Q1) includes low positive voltages—Mishra thus renders obvious using an enhancement mode source side gate. *Id.*; Mishra, ¶[0060]. At the time of the '003 patent, cascodes with first stage enhancement and second stage depletion mode gates were known. Bernstein, [252]. This approach was implemented, for example, in Bonn, Sankin, and Salato *Id.*; Bonn, 8:51-9:4; Sankin (Ex-1018), ¶¶[0013], [0119], Fig. 1; Salato (Ex-1017), 1:30-34.

Petition at 83-84

Mishra

[0060] Higher breakdown voltage and higher power operation is enabled by the second stage transistor **Q2** (or subsequent stages) which includes a field plate to reduce the electric field within the device. Hence the multi-stage amplification block **100** obtains the benefits of the field plate without detrimental impact on the overall gain of the amplifier block. Stated differently, any field plate capacitance shows up at output capacitance in the second stage instead of feedback capacitance, which can significantly improve gain. **Q1** can be biased at a low voltage (−6V) and provides current gain, while **Q2** is biased at a high voltage and generates voltage gain. Non-field-plate devices are more suited to lower voltage operation (where dispersion is not a problem), while field plated devices are more suited to high bias operation. Multi-stage amplifier blocks according to the present invention combine the strengths of both these devices.

Ex-1009 at [0060]

- **Mishra's circuit is for signal amplification**
- **Bonn's circuit is a mixer/downconverter**
- **Sankin and Salato are power supplies**
- **Ren is an inverter system**

Dr. Choi's *uncontested* testimony is that different applications than Mishra's would not motivate a POSA

Ex-1009, [0006], [0009]-[0010]; Ex-1006, 2:66-3:1; Ex-1017, 1:31-34; Ex-1018, Abstract ; Ex-2004 at ¶ 203, 207-211; POR at 53-57; PO Reply at 26-27

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE