

Petitioner's Demonstrative Exhibits

Case No: IPR2025-00094
Patent No. 8,264,003

Innoscence America, Inc.
v. Infineon Technologies Austria AG

April 8, 2026

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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**All claims
unpatentable**

Overview of the '003 Patent

The '003 Patent: Merged Cascode

'003 Patent claims merged cascode with single FET, the first enhancement mode gate and the second depletion mode gate are separated by a node, which forms a merged region

Merged Cascode Transistor

(12) **United States Patent**
Herman

(10) **Patent No.:** US 8,264,003 B2
(45) **Date of Patent:** Sep. 11, 2012

(54) **MERGED CASCODE TRANSISTOR**

(75) **Inventor:** Thomas Herman, Manhattan Beach, CA (US)

(73) **Assignee:** International Rectifier Corporation, El Segundo, CA (US)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 9 days.

(21) **Appl. No.:** 11/848,338

(22) **Filed:** Mar. 28, 2007

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(60) Provisional application No. 60/783,934, filed on Mar. 20, 2006.

(51) **Int. Cl.** (2006.01)
H01L 29/66

(52) **U.S. Cl.** 357/194; 257/229; 246

(58) **Field of Classification Search** 257/192; 257/194; 195; 129/14; 129/144; 129/246; 257/120; 249

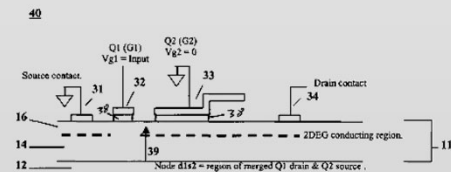
See application file for complete search history.

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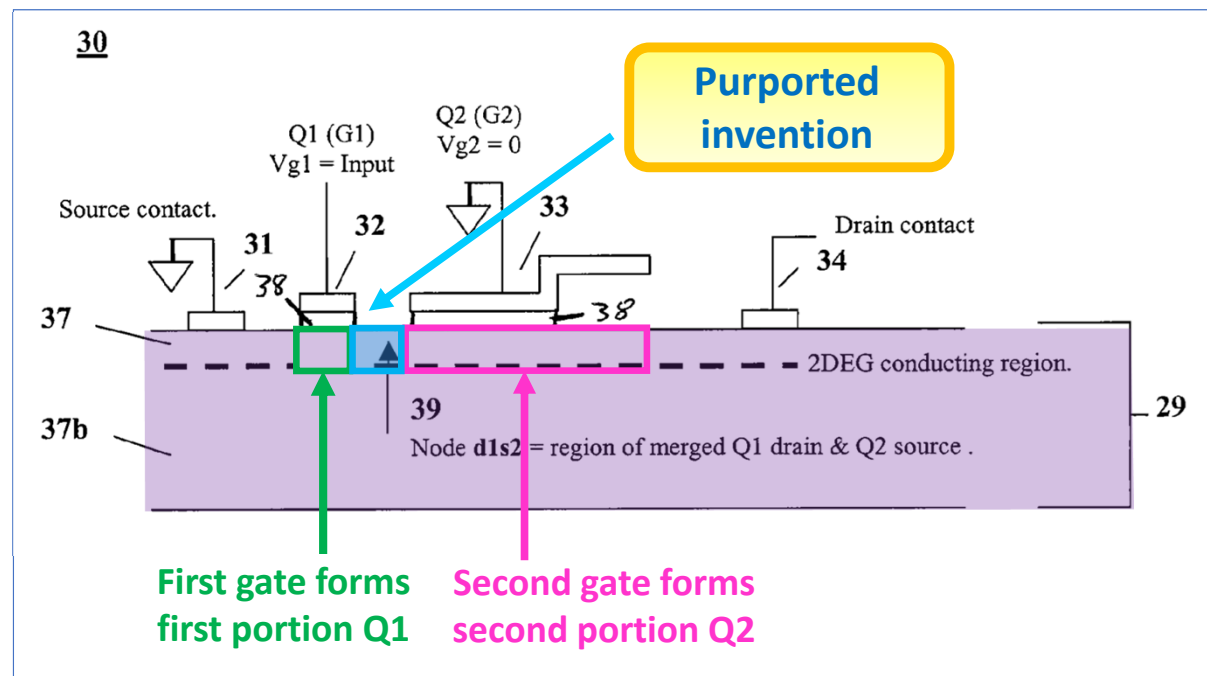
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16 Claims, 4 Drawing Sheets



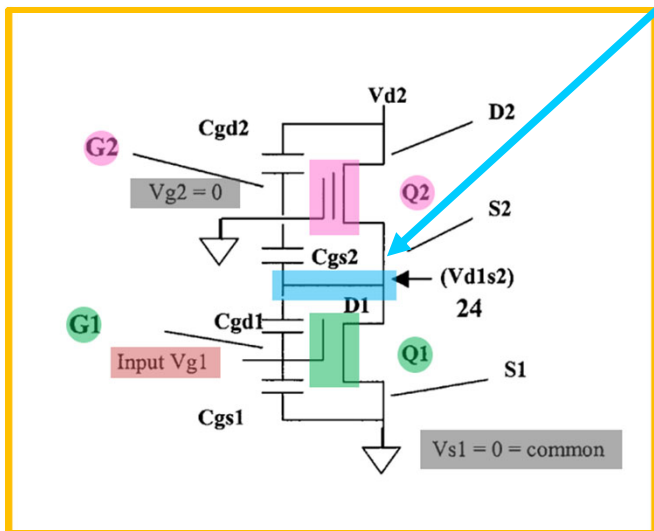
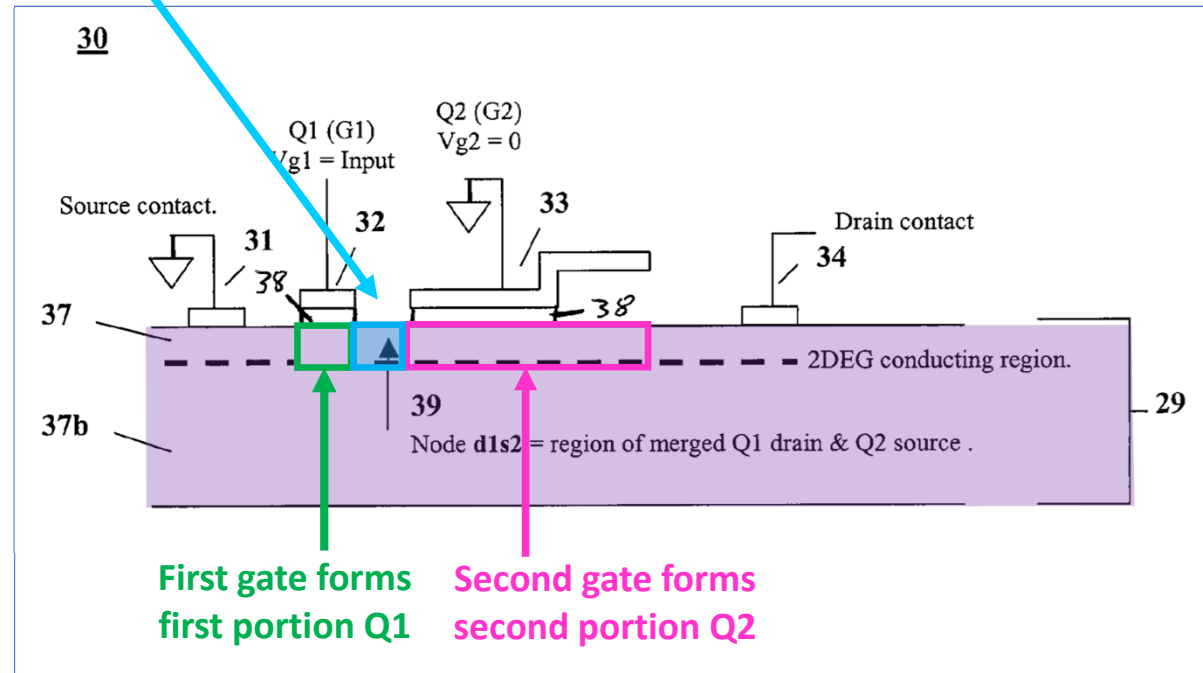
'003 Patent, cover.



'003 Patent, Fig. 3 (annotated).

The '003 Patent: Merged Cascode

'003 Patent purports to invent:
A merged region between
e-mode and d-mode transistors

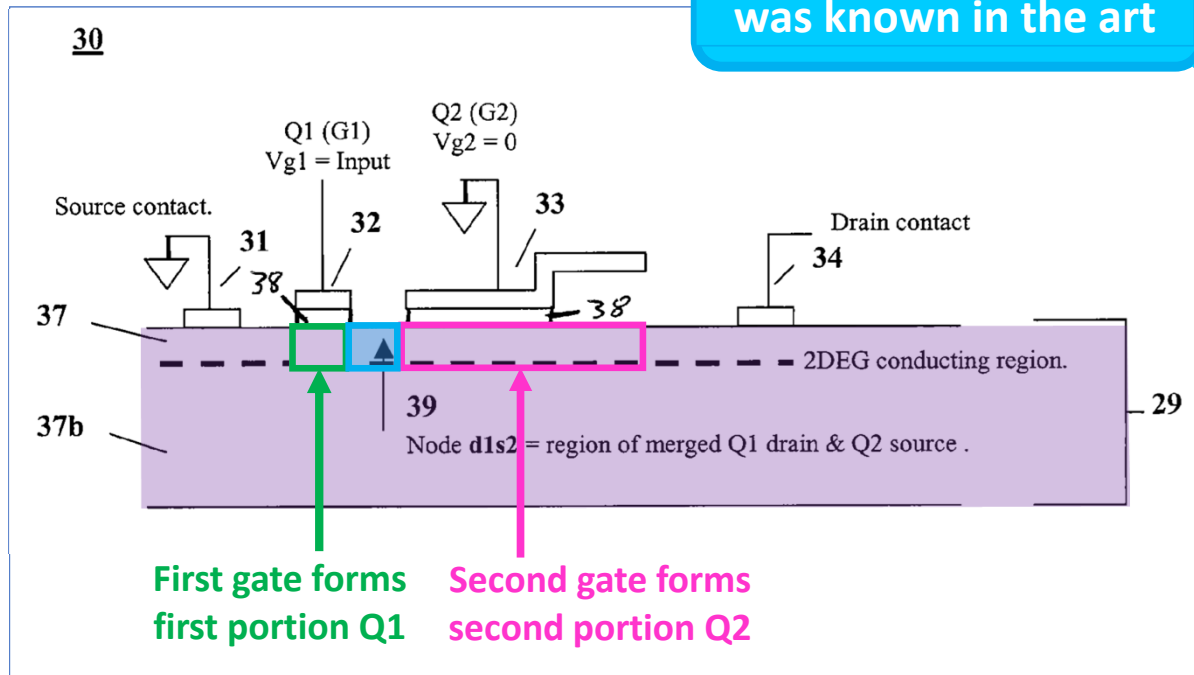


'003 Patent, Figs. 2, 3 (annotated).

The '003 Patent: Merged Cascode

'003 Patent claims to reduce Miller effect, reduce dV/dt , reduce power loss, and increase efficiency through the use of a single FET with merged region

But the merged region was known in the art



'003 Patent, Fig. 3 (annotated); Paper No. 1 at 2-4.

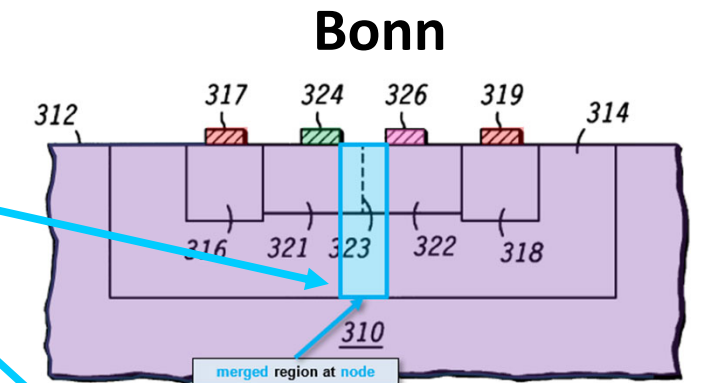
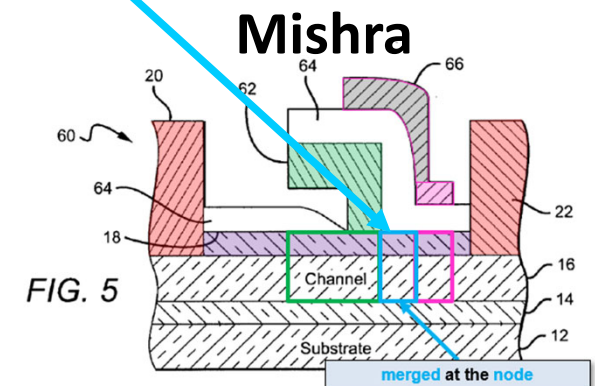


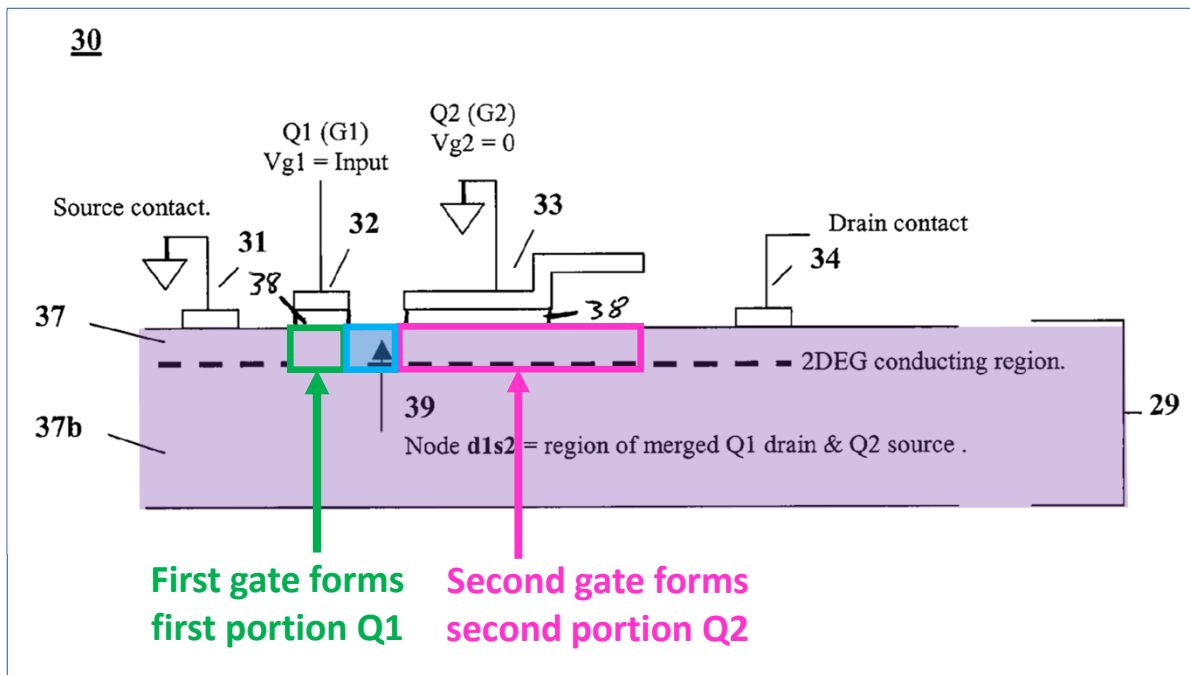
FIG 7 Bonn (Ex. 1006), Fig. 7 (annotated).



Mishra (Ex. 1009), Fig. 5 (annotated).

The '003 Patent: Merged Cascode

Merged region with e-mode and d-mode known in the art



Bonn

Bonn discloses a dual gate FET with a merged region with e-mode and d-mode

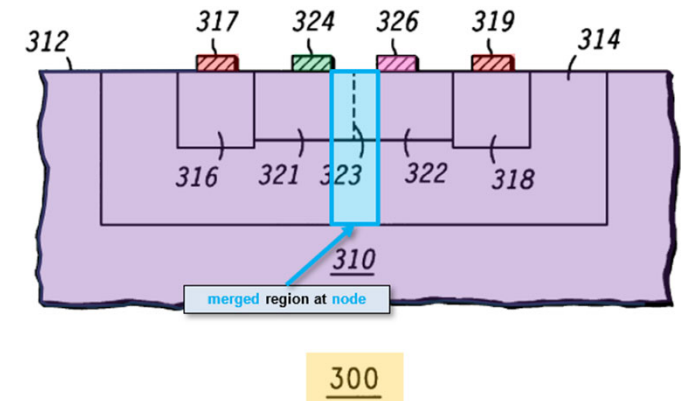


FIG. 7

Paper No. 1 at 5, 84-88; Paper No. 15 at 24-27.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

The '003 patent

Claim 1: merged cascode transistor circuit

[1PRE] A merged cascode transistor circuit comprising:

[1A] an input voltage signal source having an input voltage signal;

[1B] a constant voltage source having a predetermined constant voltage;

[1C] a merged cascode transistor comprising:

[1C1] a semiconductor element;

[1C2] a source electrode electrically connected to a top surface of the semiconductor element;

[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;

[1C4] first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and

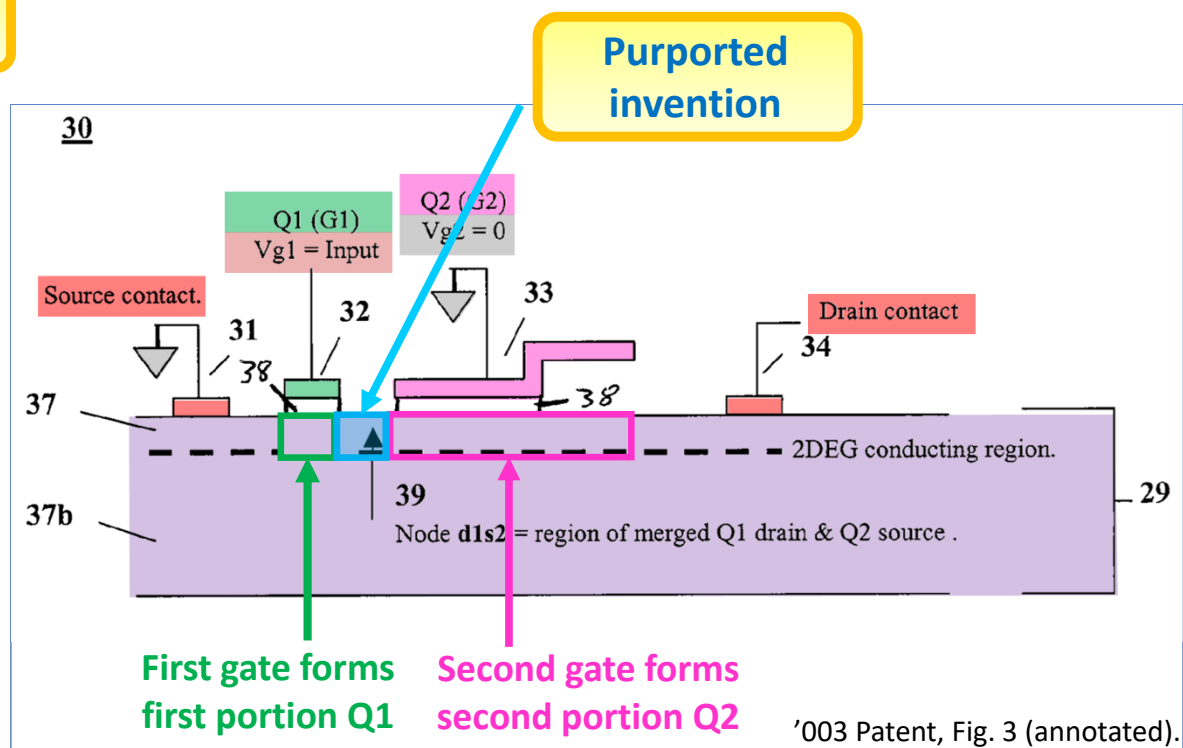
[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;

[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and

[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,

[1C8] wherein the **first portion of the transistor is an enhancement mode transistor** and the **second portion of the transistor is a depletion mode transistor**, and

[1C9] wherein **a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node** in the semiconductor element.



'003 patent claim 1

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

The '003 patent

Claim 10: specifies the semiconductor material as GaN

[10PRE] A merged cascode high electron mobility transistor circuit comprises:

[10A] an input voltage signal source having an input voltage signal;

[10B] a constant voltage source having a predetermined constant voltage;

[10C] a merged cascode transistor comprising:

[10C1] a first epitaxial layer of III-Nitride material;

[10C2] a second epitaxial layer of a III-Nitride material in contact with the first epitaxial layer such that a 2-dimensional electron gas conducting layer is formed between the first and second epitaxial layers;

[10C3] a source electrode electrically connected to the first epitaxial layer;

[10C4] a drain electrode electrically connected to the first epitaxial layer and spaced laterally from the source electrode;

[10C5] a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor; and

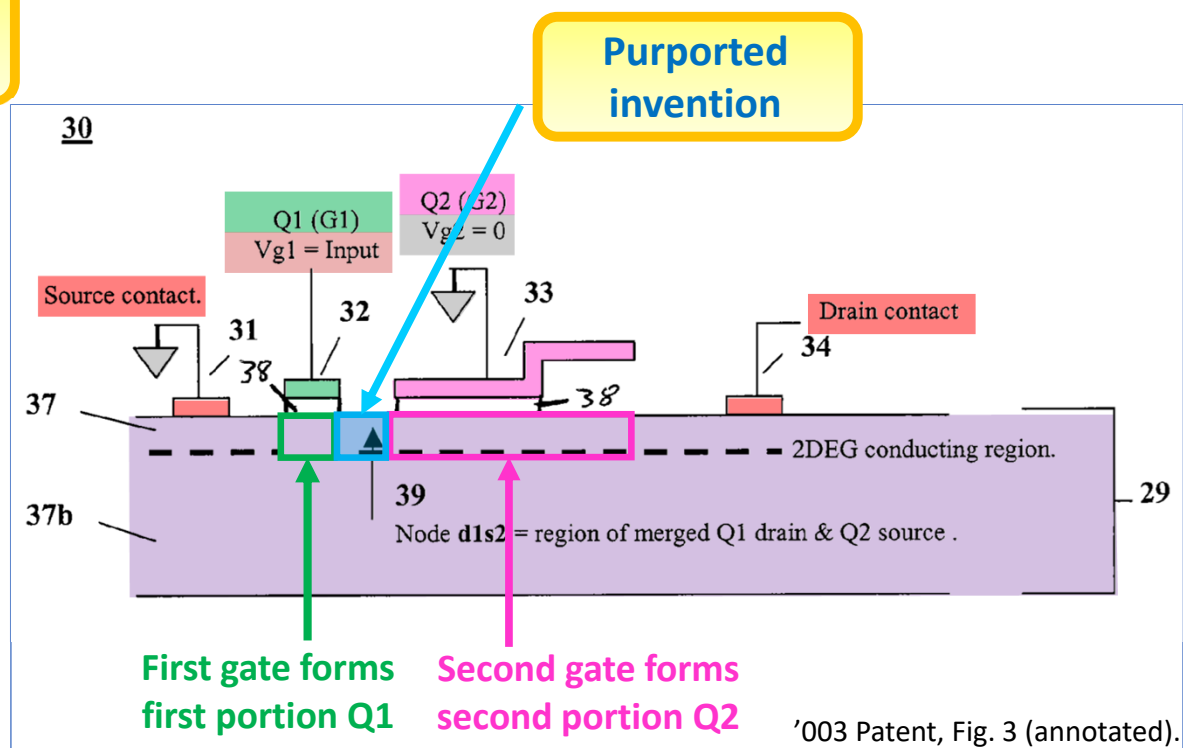
[10C6] a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor;

[10C7] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion is based on a value of the input voltage signal and

[10C8] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,

[10C9] wherein the **first portion of the transistor is an enhancement mode transistor** and the **second portion of the transistor is a depletion mode transistor**, and

[10C10] wherein a **drain region of the enhancement mode transistor is merged** with a **source region of the depletion mode transistor at the node** in the semiconductor element.



'003 Patent, Fig. 3 (annotated).

'003 patent claim 10

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Invalidity Grounds

	Ground	Challenged Claims	Basis	Prior Art
Bonn Grounds	1	1	§ 103	Bonn and Mizuta
	2	1-16	§ 103	Bonn , Ren, and Mishra
Mishra Ground	3	1-16	§ 103	Mishra and Ren

Ground 1: Bonn-Mizuto renders obvious claim 1

	Ground	Challenged Claims	Basis	Prior Art
Bonn Grounds	1	1	§ 103	Bonn and Mizuta
	2	1-16	§ 103	Bonn , Ren, and Mishra
Mishra Ground	3	1-16	§ 103	Mishra and Ren

To find claim 1 invalid over Bonn and Mizuta (Ground 1), the Board need only:

- ✓ Agree that Bonn teaches that its “dual gate FET structure . . . can be tailored to provide superior performance . . . [for] high frequency signal amplification.”

'003 Patent Ground 1: Bonn-Mizuta renders obvious claim 1

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
✓	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
✓	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
✓	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

Infineon does not dispute it would have been obvious to use Mizuta's field plate

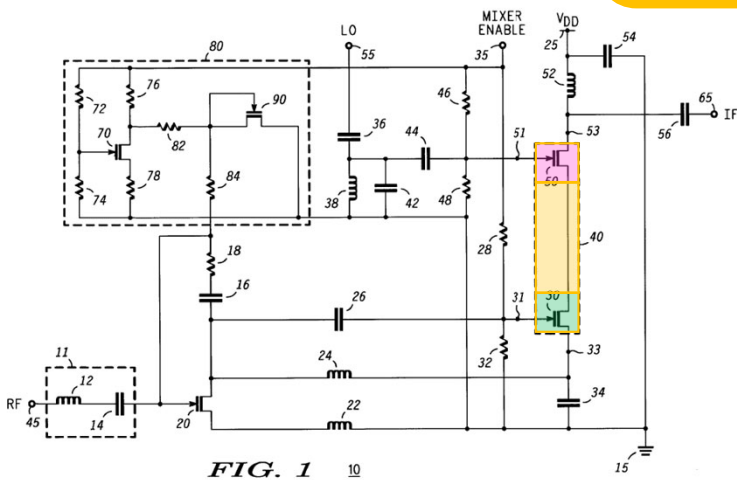
Mizuta discloses a field plate

Infineon disputes [1C7] and the motivation to modify Bonn's device for signal amplification



Paper No. 1 at 19-48.

Bonn motivates the modification: it tells a POSITA to use its dual gate FET for high frequency signal amplification

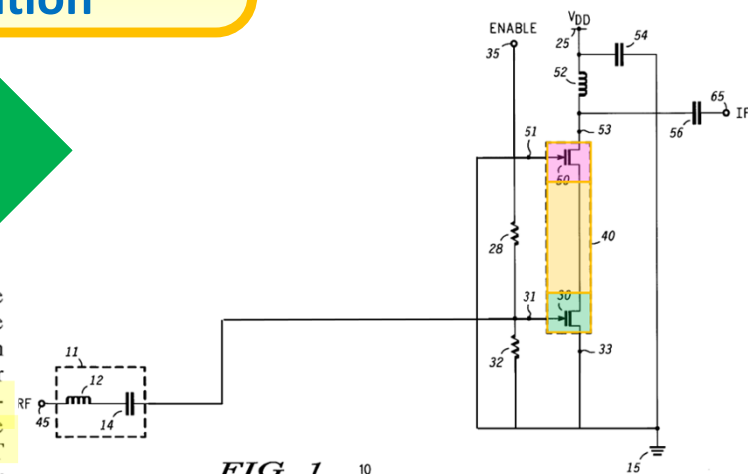


Bonn (Ex. 1006), Fig. 1 (annotated)



dual gate FET uses less chip area than two FETs in a cascode configuration. Furthermore, the parameters such as gate width, dopant concentration, and channel depth, under each gate of the dual gate FET are individually adjusted for optimum performance. Therefore, the dual gate FET structure of the present invention can be tailored to provide superior performance over the prior art dual gate FET structures in high frequency signal mixing as well as other applications such as high frequency signal amplification.

Bonn (Ex. 1006), 11:26-37



Bonn (Ex. 1006), Fig. 1 (annotated)

Bonn supports every change to Figure 1:
it explains the role of all components of Figure 1

Dr. Bernstein is an Expert in the Field of Power Converters

Infineon's ad hominem attack on Dr. Bernstein fails to show the modifications are not obvious

II. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art ("POSITA") would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design. Additional education could substitute for professional experience and vice versa. Bernstein, [067]-[069].

Paper No. 1 at 5.

Bonn itself teaches the modification proposed by Dr. Bernstein, who provided his honest expert opinion.



Dr. Bernstein is an expert:

- ✓ Graduate degree in Electrical Engineering
- ✓ PhD in Electrical Engineering and Computer Science
- ✓ Leads a research program in GaN device applications
- ✓ Holds patents related to GaN power devices
- ✓ Exceeds the agreed-on definition of a POSITA

Paper No. 15 at 12-14.

Dr. Bernstein is an Expert in the Field of Power Converters



And I think it's not normal in the state depending on if you're in an RF -- if you're an RF engineer. I generally am not so familiar with down-converters, so I think that's why he spends a lot of time explaining it so that a POSITA would understand that this is a very sort of special application. whereas, the normal application would be an amplifier.

Dr. Bernstein's honesty adds credibility, and Bonn explains its device in great detail, so a POSITA would have understood how to convert it to an amplifier

Although Dr. Bernstein honestly remarked he lacked extensive firsthand experience with downconverters and RF signal mixing applications, these statements enhance his credibility and are of no moment. Ex-2009, 44:16-17, 60:20-21, 72:20-21, 77:15-17. He does not need such expertise. The '003 patent specification and claims never mention signal mixing. Ex-1001. And he does not base his opinion on Bonn's signal mixing application.

Paper No. 15 at 13.

Ex. 2009, 44:14-21.



3 But I don't think he needs to because any
4 POSITA would understand right away the simplest, most
5 normal application for a transistor is an amplifier.
6 Transistors have many functions. They can be mixers,
7 as I said. They can be -- they can be -- what did I
8 call it? -- well, they could be filters.
9 Transistors have many, many functions, and
10 a POSITA would know in his particular application
11 what to use it for.
12 And that's my depiction and the way I
13 understood this device. And he says itself -- he
14 tells you to use it as a high-frequency amplifier,
15 which any POSITA would know, and that's exactly the
16 -- that is the device that I analyzed.

Ex. 2009, 57:3-16

**Dr. Bernstein followed Bonn's instructions to make
"the simplest, most normal application for a
transistor," which "is an amplifier."**

Bonn gives explicit instructions

By now it should be appreciated that a downconverter and a method for generating an IF signal have been provided. The LNA and the mixer in the downconverter of the present invention are coupled in a single DC path, thereby reducing the power consumption. In a preferred embodiment of the present invention, the mixer is a dual gate FET with independently adjustable gate width and channel properties. The dual gate FET uses less chip area than two FETs in a cascode configuration. Furthermore, the parameters such as gate width, dopant concentration, and channel depth, under each gate of the dual gate FET are individually adjusted for optimum performance. Therefore, the dual gate FET structure of the present invention can be tailored to provide superior performance over the prior art dual gate FET structures in high frequency signal mixing as well as other applications such as high frequency signal amplification.

Bonn (Ex. 1006), 11:26-37.

Paper No. 15, 13.

Purported novelty of patent

Bonn (Ex. 1006), Fig. 7 (annotated).

The fact that Bonn discloses another amplifier, FET 20, is irrelevant. Bonn tells its reader to use the dual gate FET for high frequency signal amplification.

300

Paper No. 15 at 3-12.

'003 Patent Ground 1: Infineon's 3 Arguments Are Based on Bonn's Modification

	Infineon's Arguments:	Innoscence's Arguments
#1	1. Bonn's modification is hindsight	1. Bonn's <u>modifications are not hindsight</u> because Bonn discloses tailoring its device to amplification
#2	2. Bonn does not each connecting second gate to constant voltage	2. By teaching to remove signal mixing amplification, Bonn teaches connecting its second gate to constant voltage which provides <u>advantages over a single-gate amplifier</u>
#3	3. Bonn's modification to achieve signal amplification is unsatisfactory for intended purpose	3. Bonn's intended purpose is signal amplification

By now it should be appreciated that a downconverter and a method for generating an IF signal have been provided. The LNA and the mixer in the downconverter of the present invention are coupled in a single DC path, thereby reducing the power consumption. In a preferred embodiment of the present invention, the mixer is a dual gate FET with independently adjustable gate width and channel properties. The dual gate FET uses less chip area than two FETs in a cascode configuration. Furthermore, the parameters such as gate width, dopant concentration, and channel depth, under each gate of the dual gate FET are individually adjusted for optimum performance. Therefore, the dual gate FET structure of the present invention can be tailored to provide superior performance over the prior art dual gate FET structures in high frequency signal mixing as well as other applications such as high frequency signal amplification.

Bonn (Ex. 1006), 11:26-37.

Paper No. 14 at 10-30; Paper No. 15 at 3-14.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 1: Modifying Bonn's Downconverter Is Not Hindsight

#1

1. Infineon argues modifying Bonn for amplification is hindsight

Modifying Bonn is not hindsight because Bonn discloses “tailor[ing]” the dual gate FET structure

The proposed modifications would have increased signal amplification, reduced Miller feedback, and lowered noise, advantages which Patent Owner does not dispute

By now it should be appreciated that a downconverter and a method for generating an IF signal have been provided. The LNA and the mixer in the downconverter of the present invention are coupled in a single DC path, thereby reducing the power consumption. In a preferred embodiment of the present invention, the mixer is a dual gate FET with independently adjustable gate width and channel properties. The dual gate FET uses less chip area than two FETs in a cascode configuration. Furthermore, the parameters such as gate width, dopant concentration, and channel depth, under each gate of the dual gate FET are individually adjusted for optimum performance. Therefore, the dual gate FET structure of the present invention can be tailored to provide superior performance over the prior art dual gate FET structures in high frequency signal mixing as well as other applications such as high frequency signal amplification.

Explicit disclosure for modification to amplifier

Bonn (Ex. 1006), 11:26-37.

Paper No. 15, 3-4, 9-12.

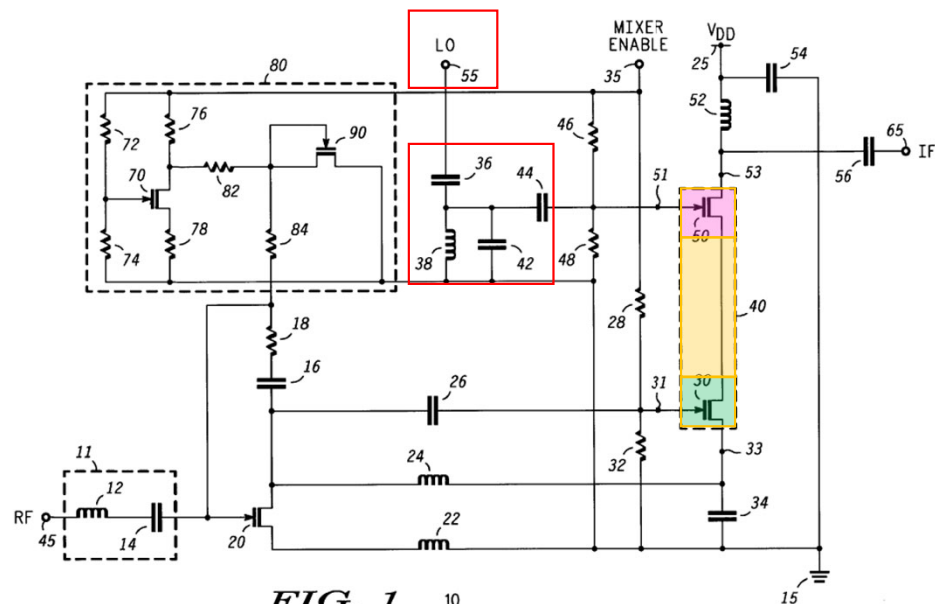
Ground 1: Modifying Bonn's Downconverter Is Not Hindsight

#1

1. Infineon argues modifying Bonn for amplification is hindsight

Every modification comes from Bonn itself: signal amplification only requires one signal

To achieve “high frequency signal amplification” with Figure 7’s dual gate FET structure (Bonn, 11:26-37), a POSITA would have removed Figure 1’s LO (local oscillator) port 55 and associated impedance matching components because the LO signal is no longer mixed. Bernstein, [098]; Bonn, 3:30-41. Bonn isolates RF and LF circuitry. Bonn, 1:20-23, 3:19-21. For Bonn’s high frequency signal amplification, a POSITA would have removed Bonn’s LO circuitry with predictable success, i.e., without impacting RF circuitry. Bernstein, [098].



Bonn (Ex. 1006), Fig. 1 (annotated).

Paper No. 1 at 23; Ex. 1003 at ¶[098].

Step 1

Remove LO circuitry (port 55 and impedance matching components 36, 42, 44, 38) because amplification only requires one signal

Ground 1: Modifying Bonn's Downconverter Is Not Hindsight

#1

1. Infineon argues modifying Bonn for amplification is hindsight

Not hindsight

Every modification comes from Bonn itself: signal amplification only requires one signal

Likewise, when using a dual gate FET for “high frequency signal amplification,” a POSITA would have removed FET 20 (amplifier when mixing) and associated circuitry, which would no longer be needed. Bernstein, [099]-[103]; Bonn, 2:8-17, 11:26-37. When removing FET 20, a POSITA would have removed: voltage source 80; capacitors 16, 26, and 34; resistor 18; and inductors 22 and 24. Bernstein, [099]-[101]. These modifications would have been obvious over Bonn’s teachings to use dual gate FETs for high frequency signal amplification and goal of designing for “minimum chip area.” Bernstein, [099]-[103]; Bonn, 1:44-45, 5:42-43, 11:26-37.

Paper No. 1 at 23-24; Ex. 1003 at ¶¶[099]-[100].

Step 2

Remove FET 20 and associated circuitry (16, 18, 80, 26, 24, 22) because Bonn instructs using dual-gate for amplification

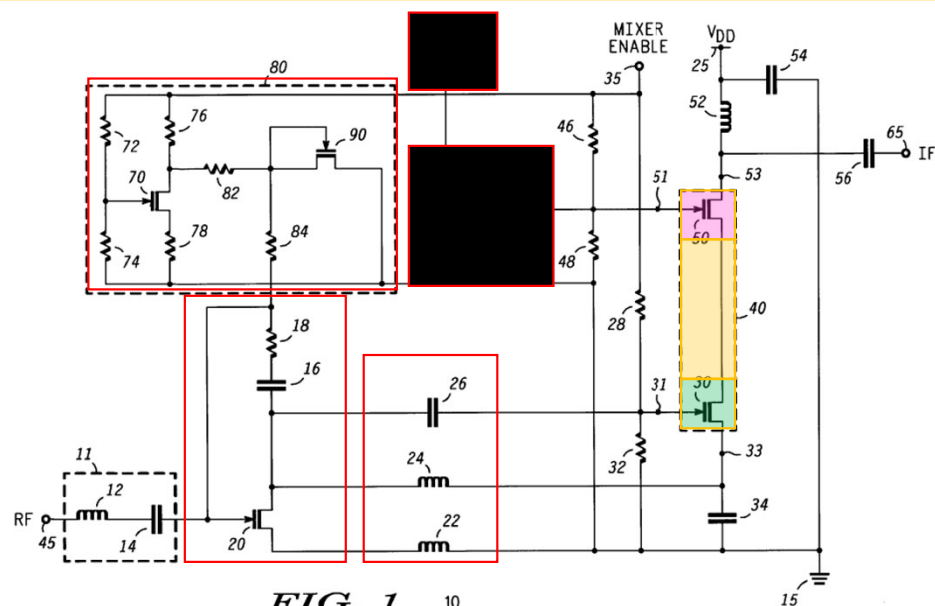


FIG. 1 10

Bonn (Ex. 1006), Fig. 1 (annotated).

Ground 1: Modifying Bonn's Downconverter Is Not Hindsight

#1

1. Infineon argues modifying Bonn for amplification is hindsight

Not hindsight

Every modification comes from Bonn itself: signal amplification only requires one signal

A POSITA would have been additionally motivated to remove capacitor 34 to short gate structure 324 to ground. Bernstein, [102]-[103]. This would increase voltage difference between V_{DD} and source terminal 33, which increases gain, thereby increasing signal amplification. *Id.* Further, Bonn discloses gate structure 324 is enhancement mode, and a POSITA would have removed capacitor 34 to decrease voltage at terminal 31 and thereby lower the gate turn-off voltage. Bernstein, [103].

Paper No. 1 at 24; Ex. 1003 at ¶¶[101]-[103].

Step 3

Remove capacitor 34 to increase gain

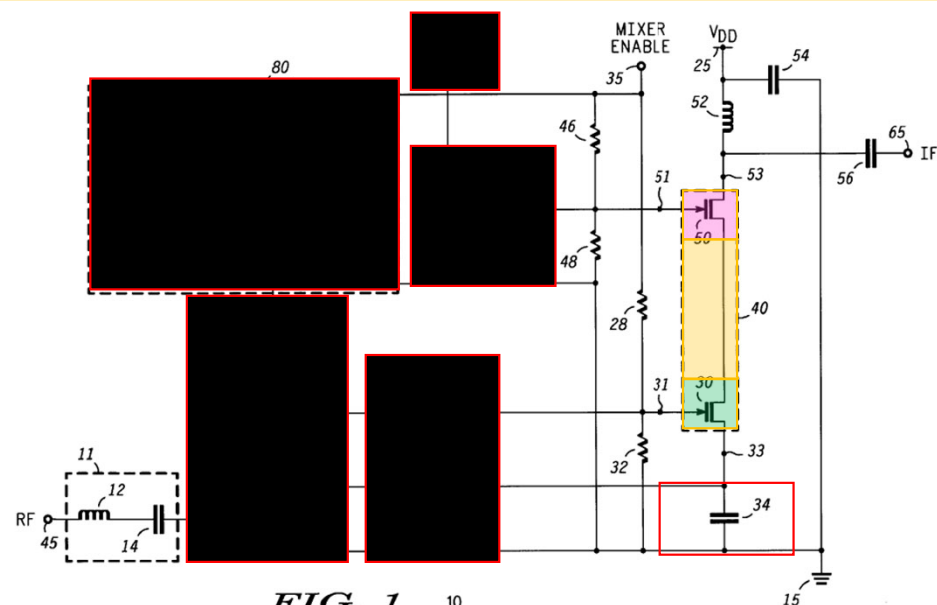


FIG. 1 10

Bonn (Ex. 1006), Fig. 1 (annotated).

Ground 1: Modifying Bonn's Downconverter Is Not Hindsight

#1

1. Infineon argues modifying Bonn for amplification is hindsight

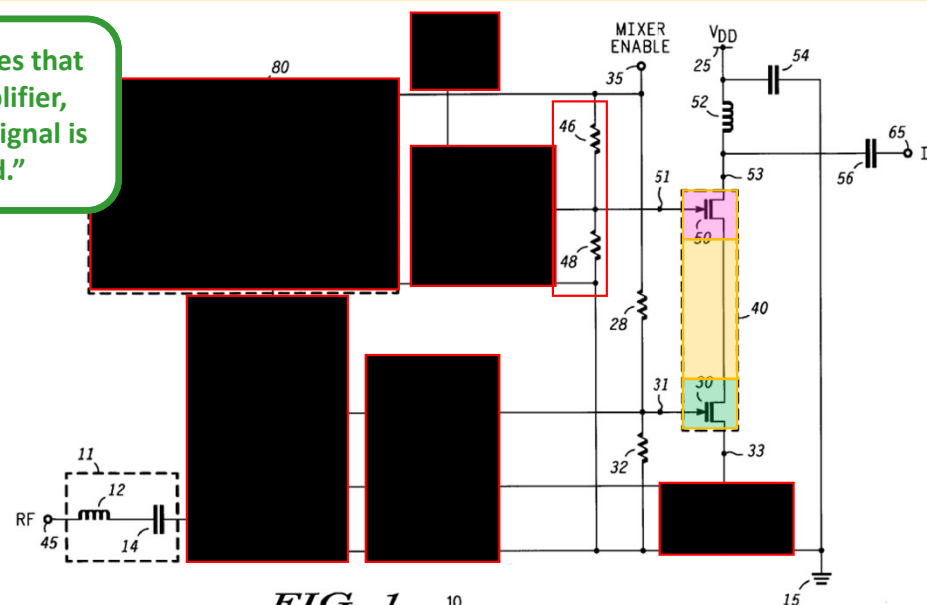
Not hindsight

Every modification comes from Bonn itself: signal amplification only requires one signal

Infineon agrees that "[i]n an amplifier, only a single signal is amplified."

In addition, a POSITA would have removed resistors 46 and 48 to reduce Miller feedback at terminal 51, which would allow drain side voltage to increase and achieve high gain with less noise than a single transistor amplifier, thereby achieving Bonn's goal of high frequency signal amplification. Bernstein, [105]-[107] (discussing Bonn and background knowledge of a POSITA); Bonn, 2:23-28, 3:65-67, 4:63-64, 5:1-8, 11:26-37. Fig. 1.

Paper No. 1 at 25; Ex. 1003 at ¶¶[104]-[107]; Paper No. 14 at 22.



Bonn (Ex. 1006), Fig. 1 (annotated).

Step 4

Remove 46 and 48 to set terminal 51 to ground to control current in depletion mode

Ground 1: Modifying Bonn's Downconverter Is Not Hindsight

#1

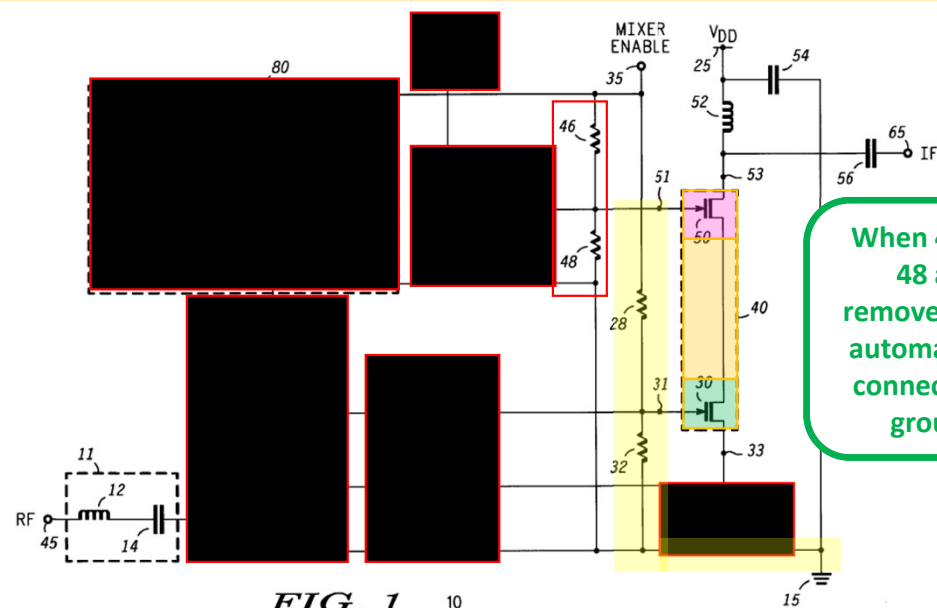
1. Infineon argues modifying Bonn for amplification is hindsight

Not hindsight

Every modification comes from Bonn itself: signal amplification only requires one signal

In addition, a POSITA would have been motivated to remove resistors 46 and 48 and short terminal 51 to ground, as shown above. Bernstein, [104]-[107]. The modification enables enhancement mode gate structure 324 to control current in the depletion mode gate structure 326, and a POSITA would have had predictable success when making this modification. *Id.* A POSITA would have understood second gate structure 326 allows channel conduction at ground potential (0V) because it is in depletion mode, and a voltage divider at resistors 46 and 48 would have been unnecessary. Bernstein, [104]; Bonn, 4:37-40, 5:15-31, 8:51-9:4. A POSITA would have known this common arrangement and understood the first, enhancement mode gate is off at 0V applied bias, so voltage on the source side of the depletion mode gate will climb toward V_{DD} until the second gate reaches pinch-off voltage. Bernstein, [107].

Paper No. 1 at 24-25; Ex. 1003 at ¶¶[104]-[107].



Bonn (Ex. 1006), Fig. 1 (annotated).

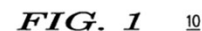
Step 4

Remove 46 and 48 to set terminal 51 to ground to control current in depletion mode

1. Infineon argues modifying Bonn for amplification is hindsight

**Every modification comes from Bonn itself:
signal amplification only requires one signal**

Paper No. 1 at 25; Ex. 1003 at ¶¶[104]-[109].



Bonn (Ex. 1006), Fig. 1 (annotated).

Final structure is the standard cascode wiring, modified from Bonn's original circuitry and tailored to high frequency signal amplification, as taught by Bonn

Ground 1: Modifying Bonn's Downconverter Is Not Hindsight

#2

2. Infineon argues a POSITA would not have connected Bonn's second gate to constant voltage

Shorting the second gate of Bonn's dual-gate amplifier to ground would have provided advantages over a single-gate amplifier, including increased amplification, reduced feedback, and lower noise

...because signals are not mixed in Bonn's

signal amplification application and the second gate structure 326 operates in depletion mode (ON at 0V), a POSITA would have understood the voltage divider at resistors 46 and 48 is not needed. Bonn explains the second gate FET 50 in mixing embodiments is enabled by setting the voltage at the voltage divider at resistors 46 and 48 (Bonn, 4:37-40) and disabled when that voltage is "near ground potential" (Bonn, 5:15-31). Without the LO signal in the signal amplification embodiment, those resistors would set the voltage at terminal 51 to a constant voltage at a value between V_{DD} and drain. But a POSITA would have understood that second gate structure 326 allows channel conduction at ground potential (0V) because it is a depletion mode gate when using dual gate FET 300 for signal amplification. Bonn, 8:51-9:4. A POSITA would thus have been motivated to short terminal 51 to ground, as shown, to set the constant voltage at terminal 51 to zero volts.

Paper No. 1 at 25; Ex. 1003 at ¶[104].

Removing LO signal circuitry sets the second gate terminal to "a constant voltage at a value between V_{dd} and a drain." Dr. Bernstein, ¶[104]

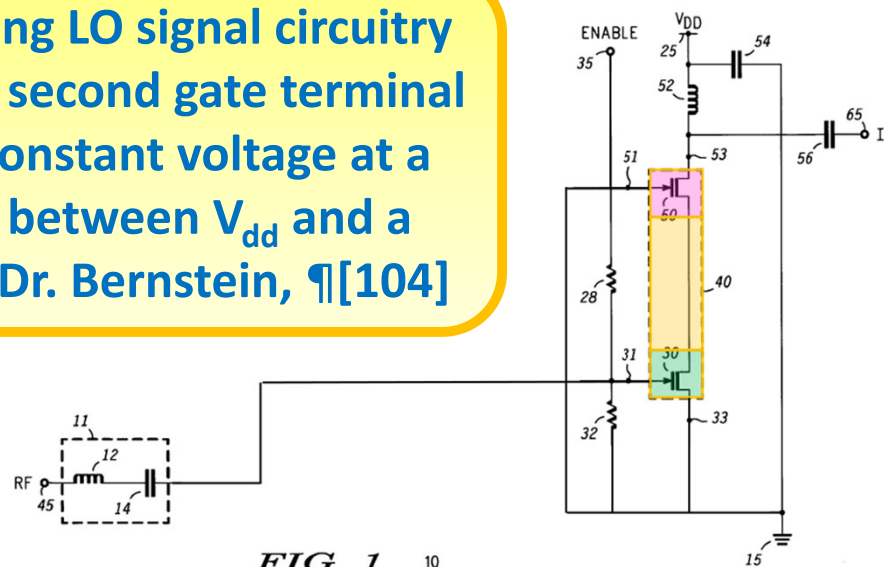


FIG. 1 10

Bonn (Ex. 1006), Fig. 1 (annotated).

#2

2. Infineon argues a POSITA would not have connected Bonn's second gate to constant voltage

Shorting the second gate of Bonn's dual-gate amplifier to ground would have provided advantages over a single-gate amplifier, including increased amplification, reduced feedback, and lower noise. Petition, 24-25; Ex-1003, [102]-[107]. This would have been obvious because the second gate is in depletion mode. Ex-1003, [104]; Bonn, 8:51-9:4 Patent Owner never disputes those benefits. See generally POR; Ex-2004.

Paper No. 15 at 7-9

Infineon's reference Mil'Shtein is irrelevant and does not teach away

- Mil'Shtein assessed the unity limit: the cutoff frequency above which there is no gain. Ex-2009, 185:13-186:1.
- A constant-voltage second gate amplified signals below 5.5 GHz. Ex-2006, 303.
- Mil'Shtein only expresses a preference for the other three approaches when evaluating one parameter—cutoff frequency. Ex-2006, 302.

Ground 1: Bonn's Figure 7 Would Function As an Amplifier

#3

3. Infineon argues Bonn's modification to achieve signal amplification is unsatisfactory for intended purpose

Bonn discloses using Figure 7 for signal amplification including adjusting parameters for different applications

By now it should be appreciated that a downconverter and a method for generating an IF signal have been provided. The LNA and the mixer in the downconverter of the present invention are coupled in a single DC path, thereby reducing the power consumption. In a preferred embodiment of the present invention, the mixer is a dual gate FET with independently adjustable gate width and channel properties. The dual gate FET uses less chip area than two FETs in a cascode configuration. Furthermore, the parameters such as gate width, dopant concentration, and channel depth, under each gate of the dual gate FET are individually adjusted for optimum performance. Therefore, the dual gate FET structure of the present invention can be tailored to provide superior performance over the prior art dual gate FET structures in high frequency signal mixing as well as other applications such as high frequency signal amplification.

Explicit disclosure for adjusting parameters for amplification

Bonn (Ex. 1006), 11:26-37

Paper No. 14 at 10-30; Paper No. 15 at 3-14.

Ground 1: Bonn's Figure 7 Would Function As an Amplifier

#3

3. Infineon argues Bonn's modification to achieve signal amplification is unsatisfactory for intended purpose

Infineon alleges Bonn's Fig. 7 has unequal current-capacity due to non-conductive sections under the gates, making it unsuitable for amplification

It should be understood that non-conductive sections like non-conductive sections 225 in structure 200 of FIG. 3 can be formed in first gate region 321, second gate region 322, or both, to individually adjust the gate width of each gate. It should also be understood that the channel depth of first gate region 321 can be different from the channel depth of second gate region 322. Therefore, the gate width and channel properties under each gate can be individually adjusted. Furthermore, structure 300 is not limited to including two gate structures as shown in FIG. 7. Structure 300 may be a multi-gate FET that includes more than two gate structures. In addition, structure 300 is not limited to having a single-fingered configuration. A multi-fingered multi-gate FET structure having individually adjustable channel properties under each gate can be developed from structure 300 of FIG. 7.

Bonn (Ex. 1006), 9:12-27

Infineon is wrong because Bonn is not limited to a preferred embodiment

- Patent Owner incorrectly relies on preferred embodiment
- Bonn's non-conductive sections are optional and individually adjustable under both gates when present
- Some embodiments would not have had smaller current carrying capacity in the first gate
- Bonn teaches embodiments with larger current capacity in the first gate

Patent Owner cites no authority to disregard "the permissive word 'can' in describing the presence of the nonconductive sections" and limit Bonn to a preferred configuration. See Paper No. 14 at 22.

Paper No. 14 at 19-24; Paper No. 15 at 10-12; Ex-2009, 96:7-98:6.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

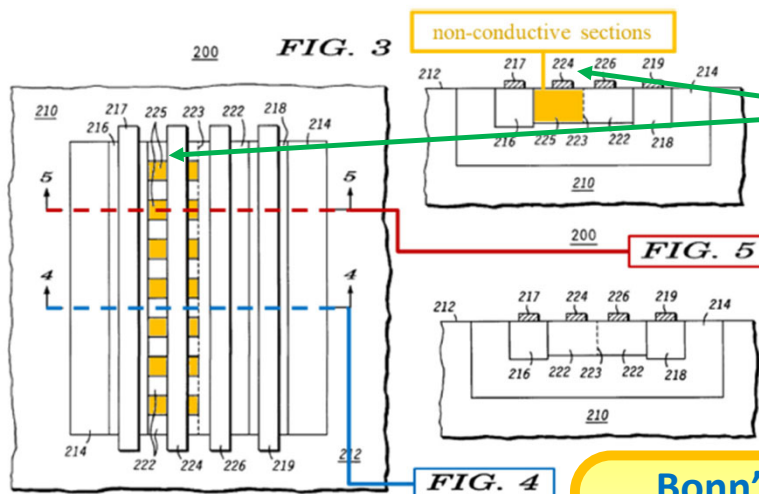
Ground 1: Bonn's Figure 7 Would Function As an Amplifier

#3

3. Infineon argues Bonn's modification to achieve signal amplification is unsatisfactory for intended purpose

Bonn discloses that the current carrying capacity of the first gate may be smaller or larger than the second gate

Bonn, Figs. 3-5 (Annotated)



Paper No. 14, 21.

SMALLER
under first gate

Optional and fully
configurable

LARGER
under first gate

Bonn's dual gate signal amplifier plainly includes Figure 7 and does not exclude it due to unequal current carrying capacity

circuitry. In the cascode configuration, FET 30 preferably has a smaller current conducting capacity than that of FET 50 to prevent FET 50 from being driven into current saturation by a strong RF signal that may appear at the gate electrode of FET 30.

Bonn (Ex. 1006), 5:37-40

225 in the first gate region. It should be understood that non-conductive sections 225 are not limited to being formed under first gate structure 224. For example, a dual gate FET may have nonconductive sections under its second gate, which results in the current conducting capacity of the first gate region of the dual gate FET being larger than the current conducting capacity of the second gate region. It should also

Bonn (Ex. 1006), 7:22-28

Bonn *never* discusses current carrying capacity of the gates of Figure 7

'003 Patent Ground 1: Infineon's 3 Arguments Are Based on Bonn's Modification

	Infineon's Arguments:	Innoscence's Arguments
#1	1. Bonn's modification is hindsight 	1. Bonn's <u>modifications</u> are <u>not hindsight</u> because Bonn discloses tailoring its device to amplification 
#2	2. Bonn does not each connecting second gate to constant voltage 	2. By teaching to remove signal mixing amplification, Bonn teaches connecting its second gate to constant voltage which provides <u>advantages</u> over a single-gate amplifier 
#3	3. Bonn's modification to achieve signal amplification is unsatisfactory for intended purpose 	3. Bonn's intended purpose is signal amplification 

Bonn teaches that its "dual gate FET structure . . . can be tailored to provide superior performance . . . [for] high frequency signal amplification."

Paper No. 14 at 10-30; Paper No. 15 at 3-14.

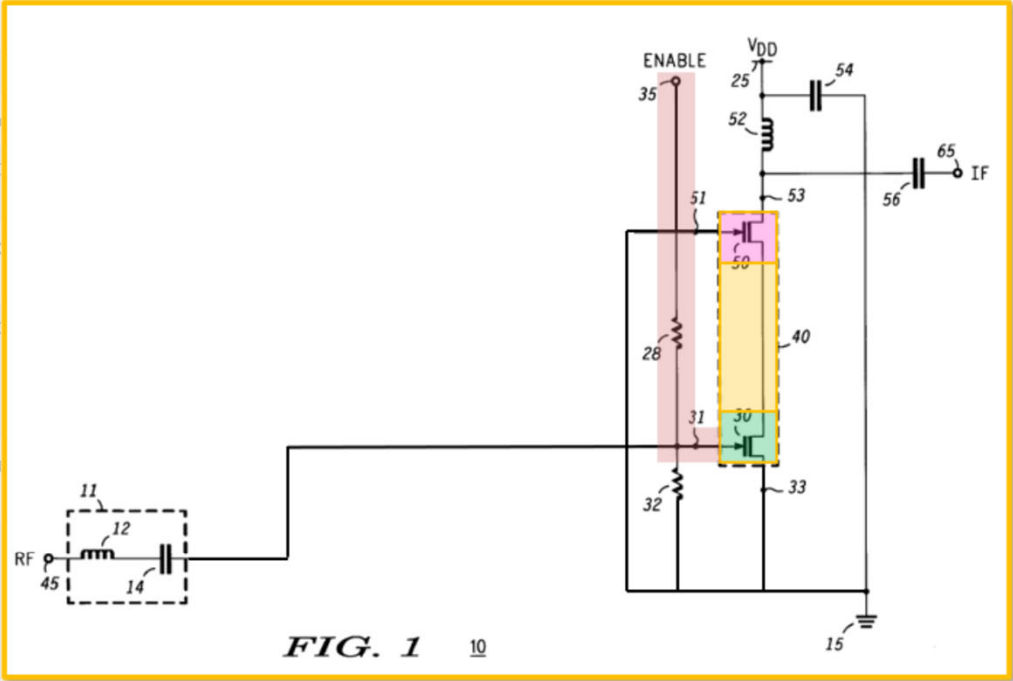
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Bonn (Ex. 1006), Fig. 1 (annotated).

Ground 1: Bonn in view of Mizuta

Paper No. 1 at 30-31.

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
	[1B] a constant voltage source having a predetermined constant voltage;
	[1C] a merged cascode transistor comprising:
	[1C1] a semiconductor element;
	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode of the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode of the semiconductor element to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the constant voltage source;
	[1C6] wherein the first gate is connected to the input voltage signal source such that the first portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

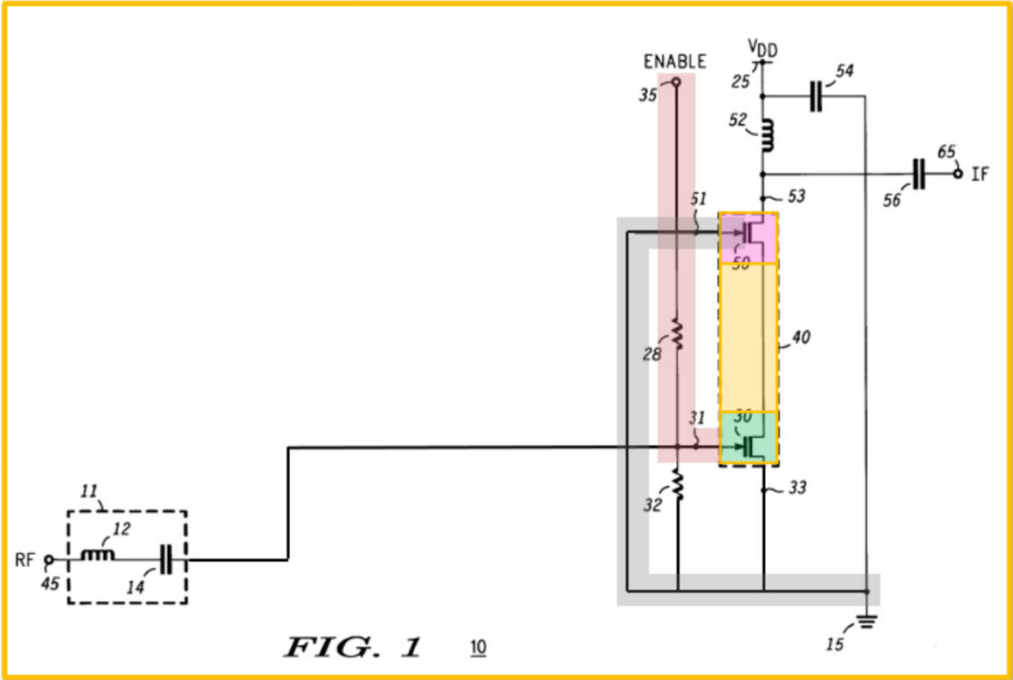


Bonn (Ex. 1006), Fig. 1 (annotated).

Ground 1: Bonn in view of Mizuta

Paper No. 1 at 31-32.

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
	[1C] a merged cascode transistor comprising:
	[1C1] a semiconductor element;
	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode of the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode of the semiconductor element to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the constant voltage source;
	[1C6] wherein the first gate is connected to the input voltage signal source such that the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

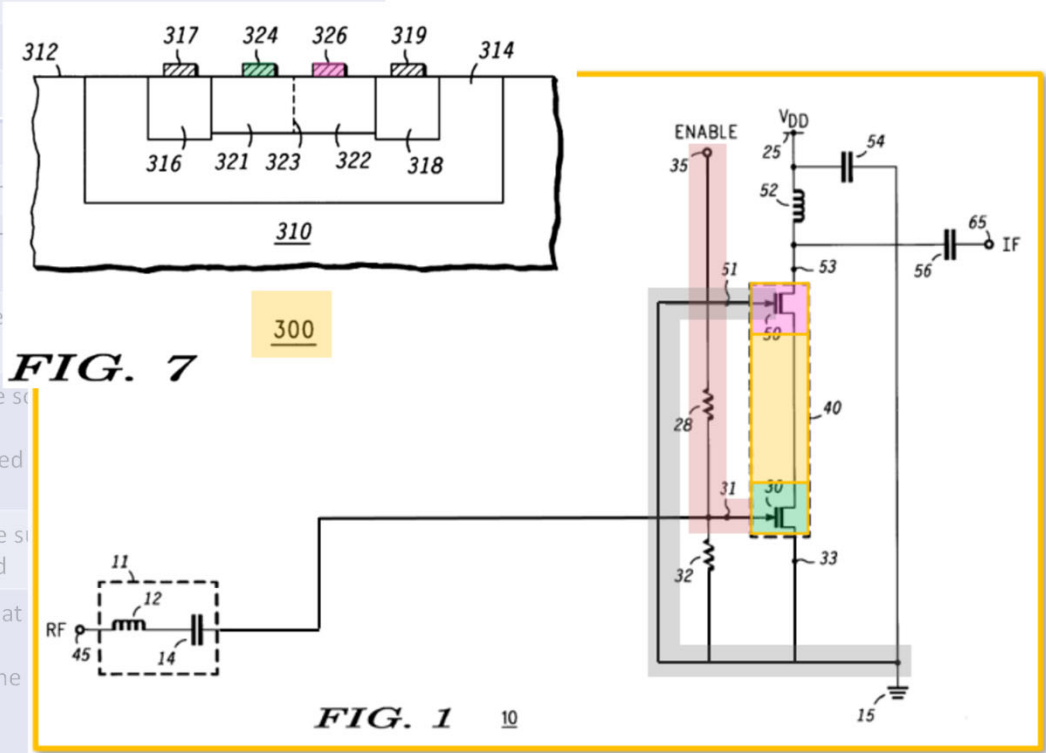


Bonn (Ex. 1006), Fig. 1 (annotated).

Ground 1: Bonn in view of Mizuta

Paper No. 1 at 33-34.

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
	[1C1] a semiconductor element;
	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the input voltage signal source;
	[1C6] wherein the first gate is connected to the input voltage signal source such that the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



Bonn (Ex. 1006), Figs. 1, 7 (annotated).

Ground 1: Bonn in view of Mizuta

Paper No. 1 at 34-35.

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode on the top surface of the semiconductor element to form a first portion of the transistor;
	[1C5] a second gate positioned adjacent to the first gate, an electrode to form a second portion of the transistor, wherein the second gate includes a field plate and an electrode;
	[1C6] wherein the first gate is connected to the input voltage signal source and the second gate is connected to the constant voltage source, and the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage difference between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C7] the second gate is connected to the constant voltage source and the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage difference between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is electrically connected to the drain electrode and a source region of the depletion mode transistor is electrically connected to the source electrode at the node in the semiconductor element;

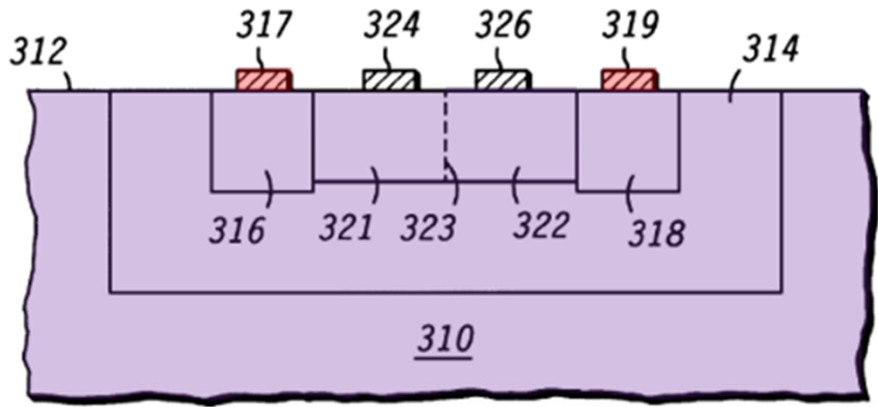


FIG. 7

Bonn (Ex. 1006), Fig. 7 (annotated).

300

Bonn (Ex. 1006), Fig. 7 (annotated).

Ground 1: Bonn in view of Mizuta

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element laterally away from the source electrode;
✓	[1C4] a first gate positioned between the source electrode and the drain electrode and electrically connected to the input voltage signal source to form a first portion of the transistor; and
✓	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

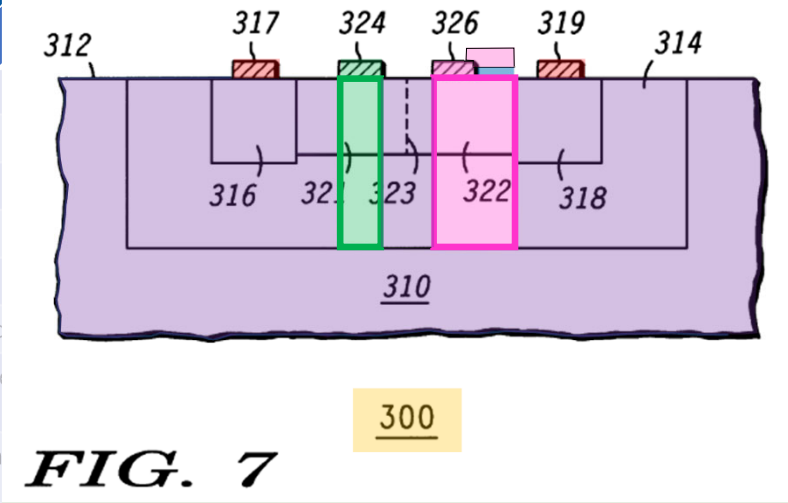


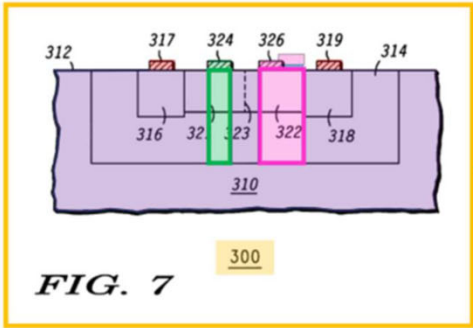
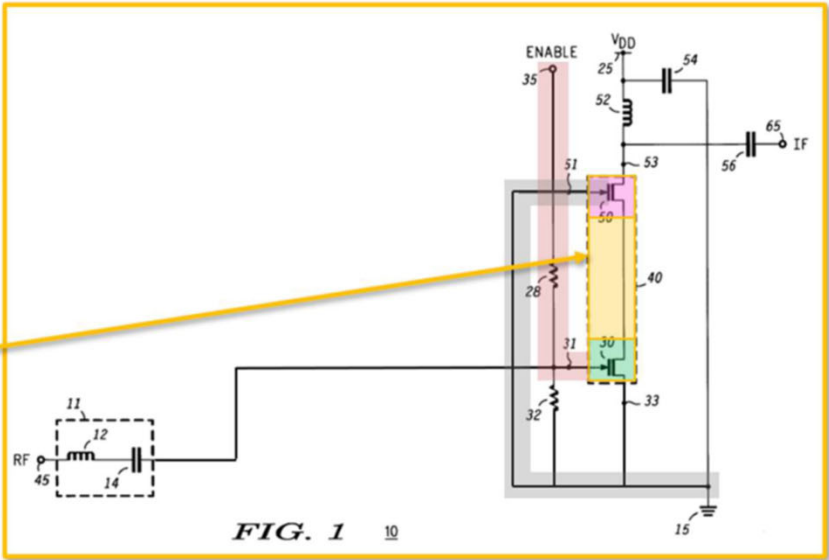
FIG. 7

Bonn (Ex. 1006), Fig. 7 (annotated).

Infineon does not dispute it would have been obvious to use Mizuta's field plate

Ground 1: Bonn in view of Mizuta

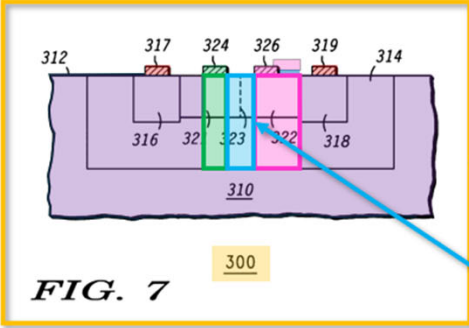
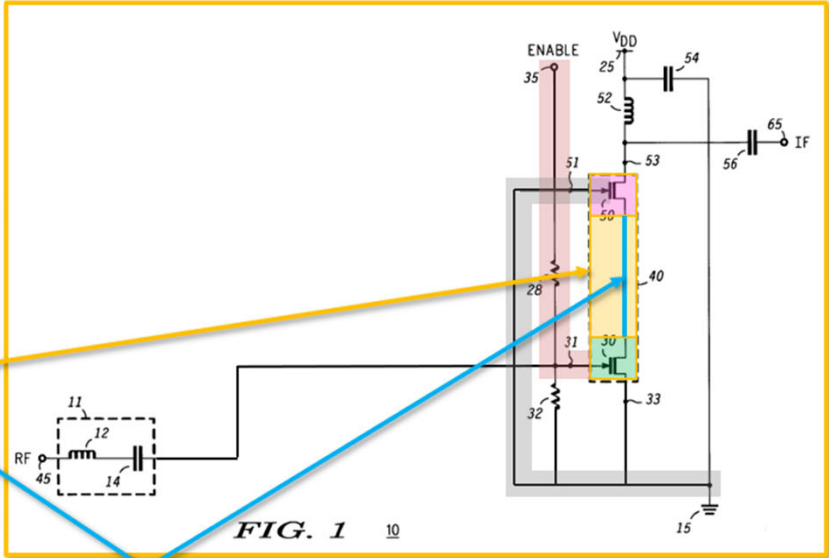
Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the semiconductor element and laterally away from the source electrode;
✓	[1C4] a first gate positioned between the source electrode and the drain electrode to form a first portion of the transistor;
✓	[1C5] a second gate positioned adjacent to the first gate and the drain electrode to form a second portion of the transistor, the second gate also coupled to the semiconductor element;
✓	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



Bonn (Ex. 1006), Figs. 1, 7 (annotated).

Ground 1: Bonn in view of Mizuta

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the semiconductor element and laterally away from the source electrode;
✓	[1C4] a first gate positioned between the source electrode and the drain electrode to form a first portion of the transistor;
✓	[1C5] a second gate positioned adjacent to the drain electrode to form a second portion of the transistor, wherein the second gate includes a first gate region and a second gate region;
✓	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
✓	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



node

Bonn (Ex. 1006), Figs. 1, 7 (annotated).

FIG. 7

300

FIG. 7

300

Paper No. 1 at 46-48.

Ground 2: Bonn-Ren-Mishra renders obvious claims 1-16

	Ground	Challenged Claims	Basis	Prior Art
Bonn Grounds	1	1	§ 103	Bonn and Mizuta
	2	1-16	§ 103	Bonn, Ren, and Mishra
Mishra Ground	3	1-16	§ 103	Mishra and Ren

To find claims 1-16 invalid over Bonn, Ren, and Mishra (Ground 2), the Board need only:

- ✓ Agree that Bonn teaches that its “dual gate FET structure . . . can be tailored to provide superior performance . . . [for] high frequency signal amplification.”
- ✓ Agree Bonn’s dual-gate transistor would have been made out of GaN for benefits that both parties agree would be better to make out GaN GaAs

'003 Patent Ground 2: Bonn-Ren-Mishra renders obvious claims 1-16

	Bonn + Ren + Mishra	Limitation
Ren discloses using GaN	✓	[1PRE] A merged cascode transistor circuit comprising:
	✓	[1A] an input voltage signal source having an input voltage signal;
	✓	[1B] a constant voltage source having a predetermined constant voltage;
	✓	[1C] a merged cascode transistor comprising:
	✓	[1C1] a semiconductor element;
	✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
	✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
	✓	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
Mishra discloses a field plate	✓	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
	✓	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
	✓	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	✓	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	✓	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

Paper No. 1 at 6, 48-82.

	Infineon's Arguments:	Innoscence's Arguments
#1	1. Bonn's express teaching of signal amplification should be ignored (from Ground 1)	1. Bonn instructs a POSITA to use its dual-gate structure for signal amplification for the reasons explained in Ground 1
#2	2. Ren only discloses one gate, so a POSITA would not have made Bonn's dual gate transistor out of GaN	2. POSITA would have applied state of the art of GaN technology in 2006 to Bonn's 1996 device

Paper No. 14 at 30-46; Paper No. 15 at 14-18.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

	Infineon's Arguments:	Innoscence's Arguments
#1	1. Bonn's express teaching of signal amplification should be ignored (from Ground 1)	1. Bonn instructs a POSITA to use its dual-gate structure for signal amplification for the reasons explained in Ground 1
#2	2. Ren only discloses one gate, so a POSITA would not have made Bonn's dual gate transistor out of GaN	2. POSITA would have applied state of the art of GaN technology in 2006 to Bonn's 1996 device

Ground 1 arguments addressed above, focusing on Ren-specific arguments for Ground 2

#2

2. Infineon argues Ren only discloses one gate, so a POSITA would not have made Bonn's dual gate transistor out of GaN

Ren describes benefits of GaN, which are the same benefits Bonn calls for

Benefits of GaN are undisputed

Bonn strives for reduced power consumption and high frequency signal amplification

Ren presents a solution to Bonn's problems:

- Reduce gate leakage
- Higher saturation velocity
- Higher breakdown voltage
- Suitable for high-frequency, high-temperature, high-power

By now it should be appreciated that various methods for generating an IF signal have been proposed. The LNA and the mixer in the downconverter of the present invention are coupled in a single DC path, thereby reducing the power consumption. In a preferred embodiment of the present invention, the mixer is a dual gate FET with independently adjustable gate width and channel properties. The dual gate FET uses less chip area than two FETs in a cascode configuration. Furthermore, the parameters such as gate width, dopant concentration, and channel depth, under each gate of the dual gate FET are individually adjusted for optimum performance. Therefore, the dual gate FET structure of the present invention can be tailored to provide superior performance over the prior art dual gate FET structures in high frequency signal mixing as well as other applications such as high frequency signal amplification.

'003 Patent Ground 2: Bonn-Ren-Mishra renders obvious claims 1-16

#2

2. Infineon argues Ren only discloses one gate, so a POSITA would not have made Bonn's dual gate transistor out of GaN

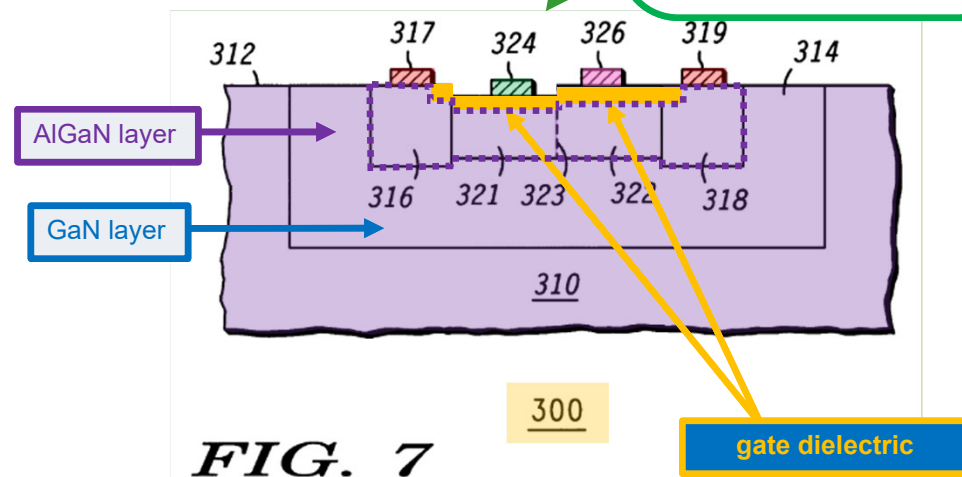
Ren describes how to make GaN e-mode and d-mode gates, allowing for easy implementation of Bonn's Figure 7

Ren teaches to adjust thickness of AlGa_xN layer to make it e-mode or d-mode

Bonn's device contains individually adjustable e-mode and d-mode

[0014] The thickness of the Al_xGa_{1-x}N layer is less than 20 nm. This provides negligible sheet carrier concentration in the GaN layer at its interface with Al_xGa_{1-x}N to permit enhancement mode operation. Typically, at some Al_xGa_{1-x}N thickness value from 10 to about 20 nm, the device will become a depletion mode device for any thickness above this value.

Ren (Ex. 1008) at ¶[0014].



Bonn (Ex. 1006), Fig. 7 (annotated).

Paper No. 1 at 50-54; Paper No. 15 at 14-16.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

'003 Patent Ground 2: Bonn-Ren Mishra renders obvious claims 1-16

#2

2. Infineon argues Ren only discloses one gate, so a POSITA would not have made Bonn's dual gate transistor out of GaN

Motivation for making Bonn's device GaN

A POSITA would have been motivated to make individual gate adjustments to Bonn's dual-gate using Ren's GaN techniques

Bonn and Ren both disclose using insulated gate FET (IGFET) structures

It should be noted that the FET structures described with reference to FIGS. 3, 7, and 8 are not limited to gallium arsenide FET structures. They are equally applicable to insulated gate FET (IGFET) structures. For an IGFET, the gate is separated from the major surface of the body of semiconductor material by a gate dielectric layer. In addition, for an n-channel IGFET, the source and drain regions have an n-type conductivity and the channel region has a p-type conductivity; and for a p-channel IGFET, the source and drain regions have a p-type conductivity and the channel region has an n-type conductivity.

Bonn (Ex. 1006), 11:12-22.

[0014] The thickness of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer is less than 20 nm. This provides negligible sheet carrier concentration in the GaN layer at its interface with $\text{Al}_x\text{Ga}_{1-x}\text{N}$ to permit enhancement mode operation. Typically, at some $\text{Al}_x\text{Ga}_{1-x}\text{N}$ thickness value from 10 to about 20 nm, the device will become a depletion mode device for any thickness above this value.

Ren's simple approach:
Thin = enhancement mode
Thick = depletion mode

14].

#2

2. Infineon argues Ren only discloses one gate, so a POSITA would not have made Bonn's dual gate transistor out of GaN

Bonn discloses varying depth, thickness, composition of both gates and Ren provides simple method of varying dielectric thickness to achieve e-mode, d-mode

By now it should be appreciated that a downconverter and a method for generating an IF signal have been provided. The LNA and the mixer in the downconverter of the present invention are coupled in a single DC path, thereby reducing the power consumption. In a preferred embodiment of the present invention, the mixer is a dual gate FET with independently adjustable gate width and channel properties. The dual gate FET uses less chip area than two FETs in a cascode configuration. Furthermore, the parameters such as gate width, dopant concentration, and channel depth, under each gate of the dual gate FET are individually adjusted for optimum performance. Therefore, the dual gate FET structure of the present invention can be tailored to provide superior performance over the prior art dual gate FET structures in high frequency signal mixing as well as other applications such as high frequency signal amplification.

Bonn (Ex. 1006), 11:12-22.

[0014] The thickness of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer is less than 20 nm. This provides negligible sheet carrier concentration in the GaN layer at its interface with $\text{Al}_x\text{Ga}_{1-x}\text{N}$ to permit enhancement mode operation. Typically, at some $\text{Al}_x\text{Ga}_{1-x}\text{N}$ thickness value from 10 to about 20 nm, the device will become a depletion mode device for any thickness above this value.

Ren (Ex. 1008) at ¶[0014].

A POSITA would have adjusted the individual properties of each of Bonn's gates using Ren's GaN techniques

#2

2. Infineon argues Ren only discloses one gate, so a POSITA would not have made Bonn's dual gate transistor out of GaN

It can be noted that the FET structures described with reference to FIGS. 3, 7, and 8 are not limited to gallium arsenide FET structures. They are equally applicable to insulated gate FET (IGFET) structures. For an IGFET, the gate is separated from the major surface of the body of semiconductor material by a gate dielectric layer. In addition, for an n-channel IGFET, the source and drain regions have an n-type conductivity and the channel region has a p-type conductivity; and for a p-channel IGFET, the source and drain regions have a p-type conductivity and the channel region has an n-type conductivity.

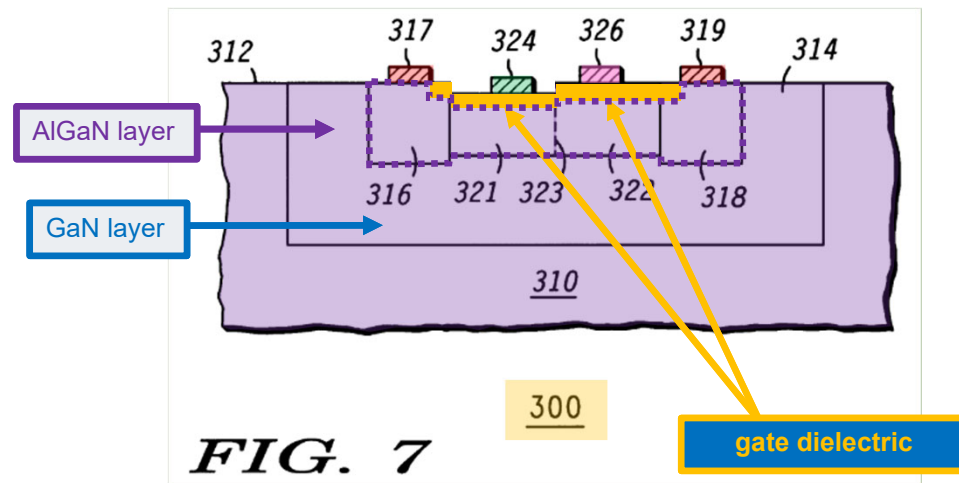
Bonn (Ex. 1006), 11:12-22.

[0014] The thickness of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer is less than 20 nm. This provides negligible sheet carrier concentration in the GaN layer at its interface with $\text{Al}_x\text{Ga}_{1-x}\text{N}$ to permit enhancement mode operation. Typically, at some $\text{Al}_x\text{Ga}_{1-x}\text{N}$ thickness value from 10 to about 20 nm, the device will become a depletion mode device for any thickness above this value.

Paper No. 1 at 50-54; Paper No. 15 at 14-16.

Ren (Ex. 1008) at ¶[0012].

Bonn and Ren both contain a gate dielectric layer



Bonn (Ex. 1006), Fig. 7 (annotated).

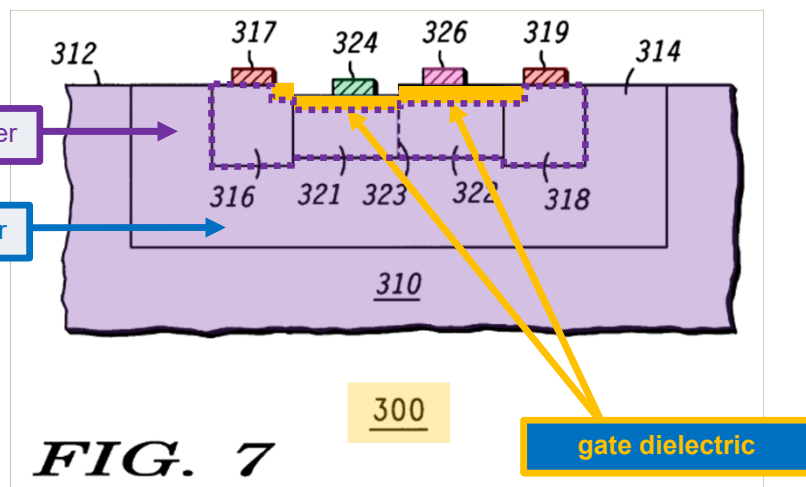
Ren discloses adjusting thickness of this layer to make the transistor either e-mode or d-mode

#2

2. Infineon argues Ren only discloses one gate, so a POSITA would not have made Bonn's dual gate transistor out of GaN

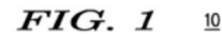
Infineon's vague discussions on the state of the art fails to defeat Ground 2

- Infineon's assertions that the field of semiconductor technology "retains a strong element of trial and error" shows a POSITA would have used routine experimentation to combine Bonn, Ren, and Mishra.
- The inventor's statement that International Rectifier "deemed" making GaN e-mode transistors "a more difficult task" does not explain whether it was "more difficult" for business, cost, logistical, technical or other reasons, and does not support non-obviousness.



	Infineon's Arguments:	Innoscence's Arguments
#1	1. Bonn cannot be modified for the reasons outlined in Ground 1 	1. Bonn instructs a POSITA to use its dual-gate structure for signal amplification for the reasons explained in Ground 1 
#2	2. No reasonable expectation of success in remaking Bonn's transistor out of GaN 	2. POSITA would have applied state of the art of GaN technology in 2006 to Bonn's 1996 device 

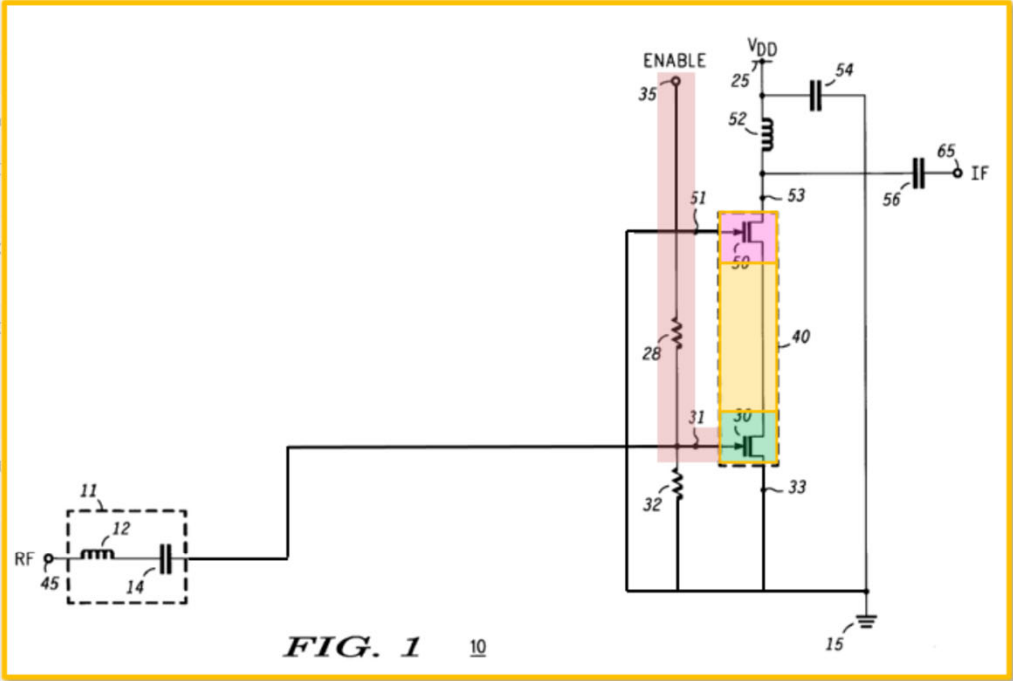
Bonn's dual-gate transistor can be modified to an amplifier and used with GaN, as taught by Ren



DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 2: Bonn-Ren-Mishra

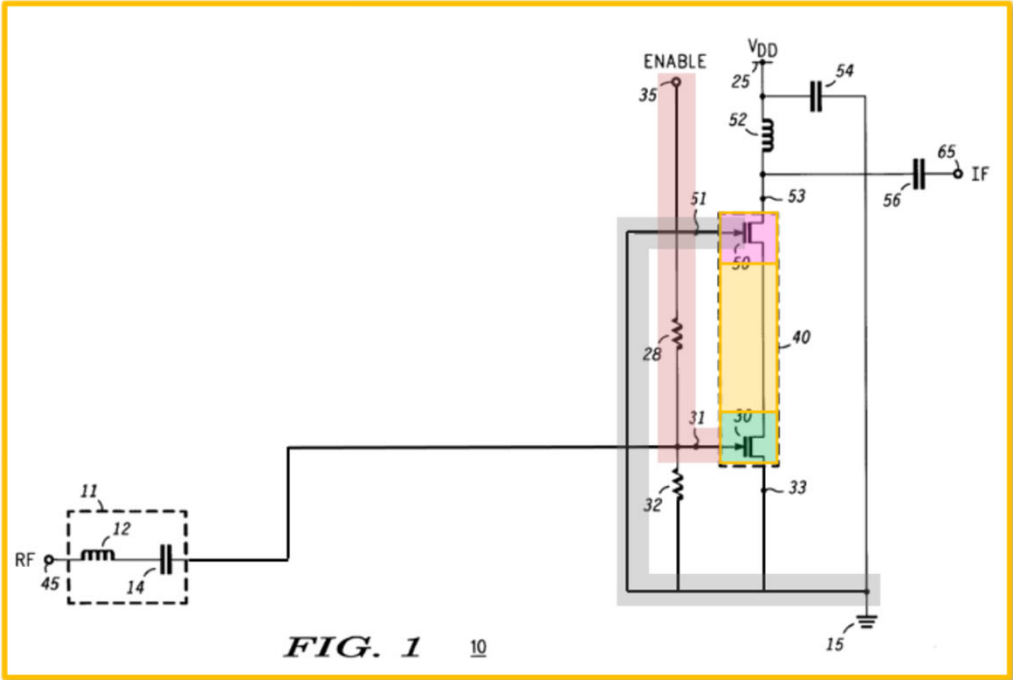
Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
	[1B] a constant voltage source having a predetermined constant voltage;
	[1C] a merged cascode transistor comprising:
	[1C1] a semiconductor element;
	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode of the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode of the semiconductor element to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the constant voltage source;
	[1C6] wherein the first gate is connected to the input voltage signal source such that the first portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



Bonn (Ex. 1006), Fig. 1 (annotated).

Ground 2: Bonn-Ren-Mishra

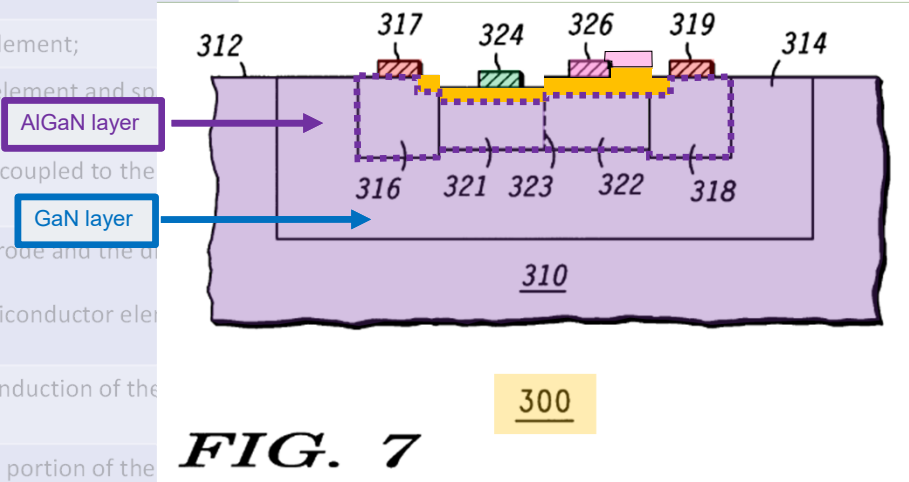
Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
	[1C] a merged cascode transistor comprising:
	[1C1] a semiconductor element;
	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode of the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode of the semiconductor element to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the constant voltage source;
	[1C6] wherein the first gate is connected to the input voltage signal source such that the first portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



Bonn (Ex. 1006), Fig. 1 (annotated).

Ground 2: Bonn-Ren-Mishra

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
	[1C1] a semiconductor element;
	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



Bonn (Ex. 1006), Fig. 7 (annotated).

Ground 2: Bonn-Ren-Mishra

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

AlGaN layer

GaN layer

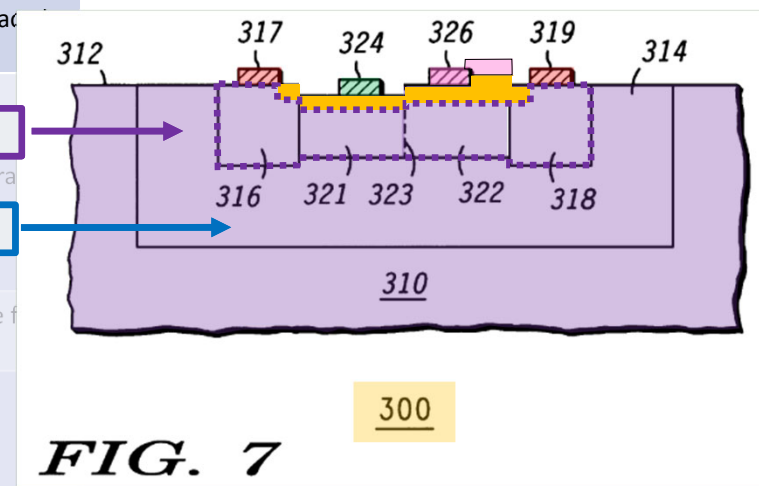


FIG. 7

Bonn (Ex. 1006), Fig. 7 (annotated).

Ground 2: Bonn-Ren-Mishra

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
✓	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate
	[1C6] wherein the first gate is connected to the input voltage signal source and the second portion of the transistor is based on a value of the input voltage signal;
	[1C7] the second gate is connected to the constant voltage source and the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage difference between the first portion and the second portion of the transistor reaches a predetermined level
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is a depletion mode transistor at the node in the semiconductor element

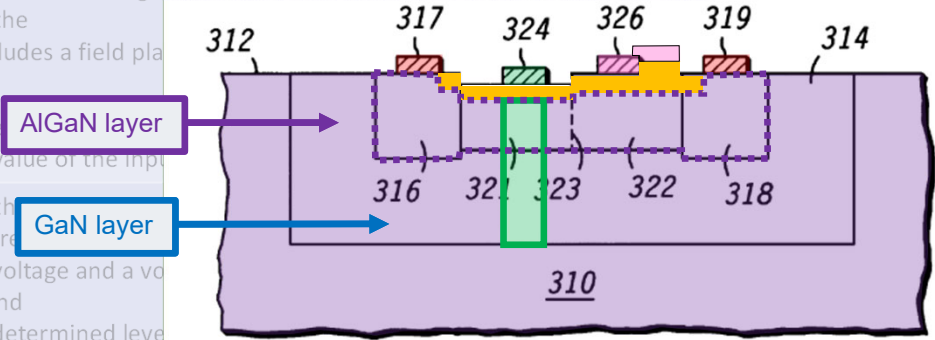


FIG. 7

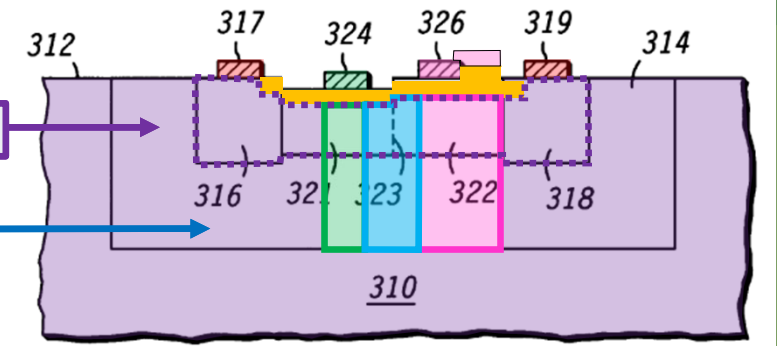
Bonn (Ex. 1006), Fig. 7 (annotated).

Ground 2: Bonn-Ren-Mishra

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and laterally away from the source electrode;
✓	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
✓	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

AlGaIn layer

GaN layer



300

FIG. 7

Bonn (Ex. 1006), Fig. 7 (annotated).

Ground 2: Bonn-Ren-Mishra

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and laterally away from the source electrode;
✓	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
✓	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
✓	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

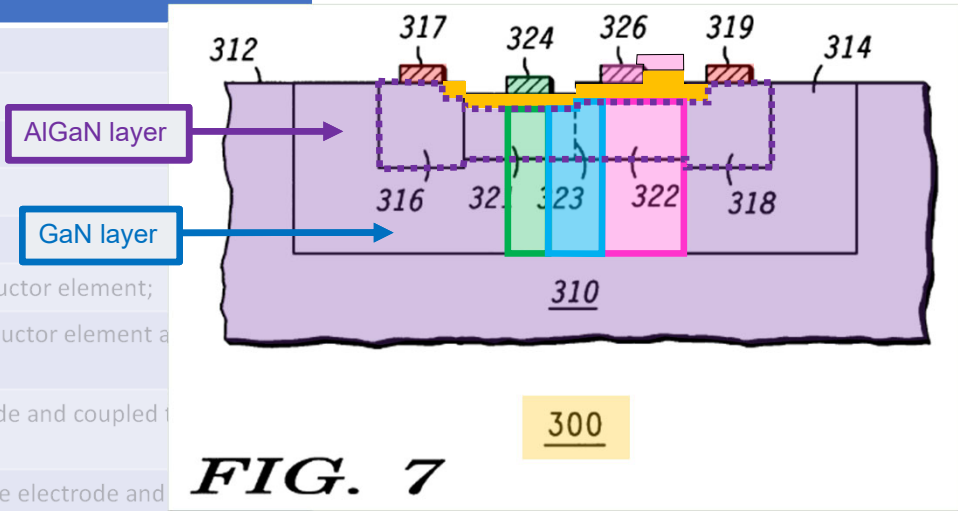


FIG. 7

Bonn (Ex. 1006), Fig. 7 (annotated).

Ground 2: Bonn-Ren-Mishra

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit
✓	[1A] an input voltage signal source having
✓	[1B] a constant voltage source having a p
✓	[1C] a merged cascode transistor compris
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically conn
✓	[1C3] a drain electrode electrically conne
✓	[1C4] a first gate positioned between the
✓	[1C5] a second gate positioned adjacent t
✓	[1C6] wherein the first gate is connected
✓	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

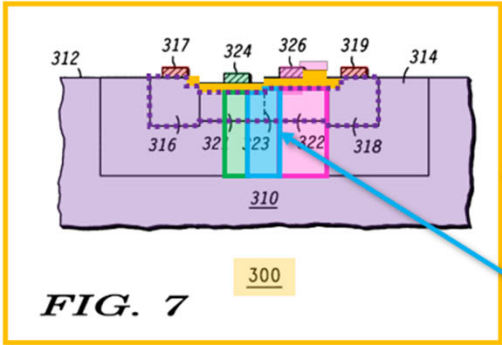


FIG. 7

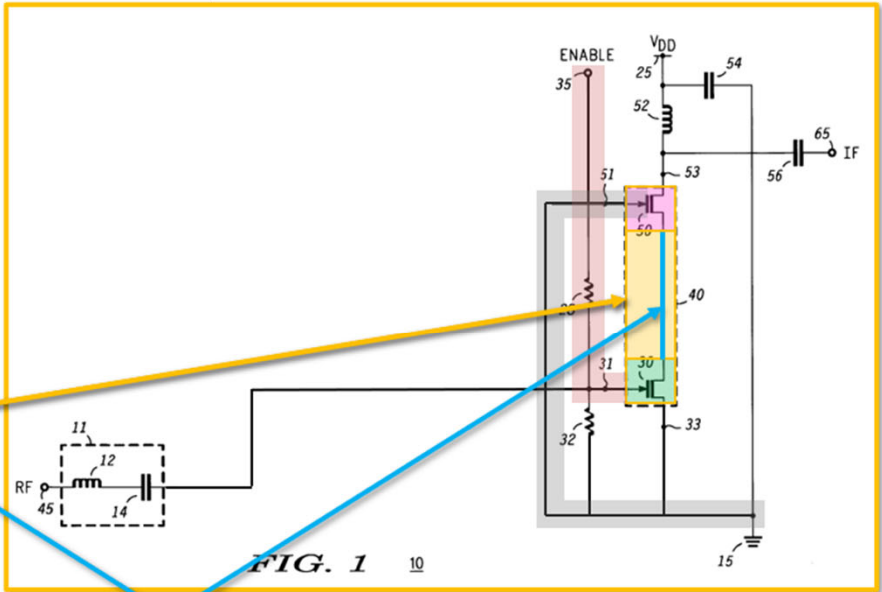


FIG. 1

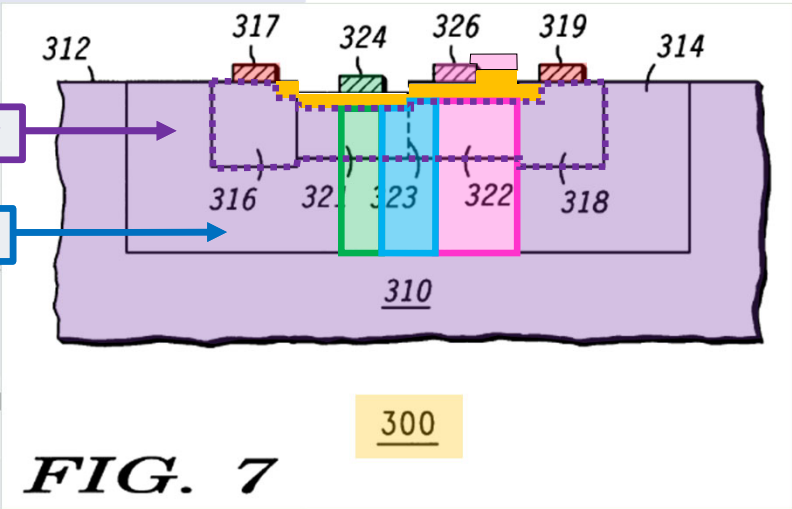
node

Bonn (Ex. 1006), Figs. 1, 7 (annotated).

Paper No. 1 at 67-69.

Ground 2: Bonn-Ren-Mishra

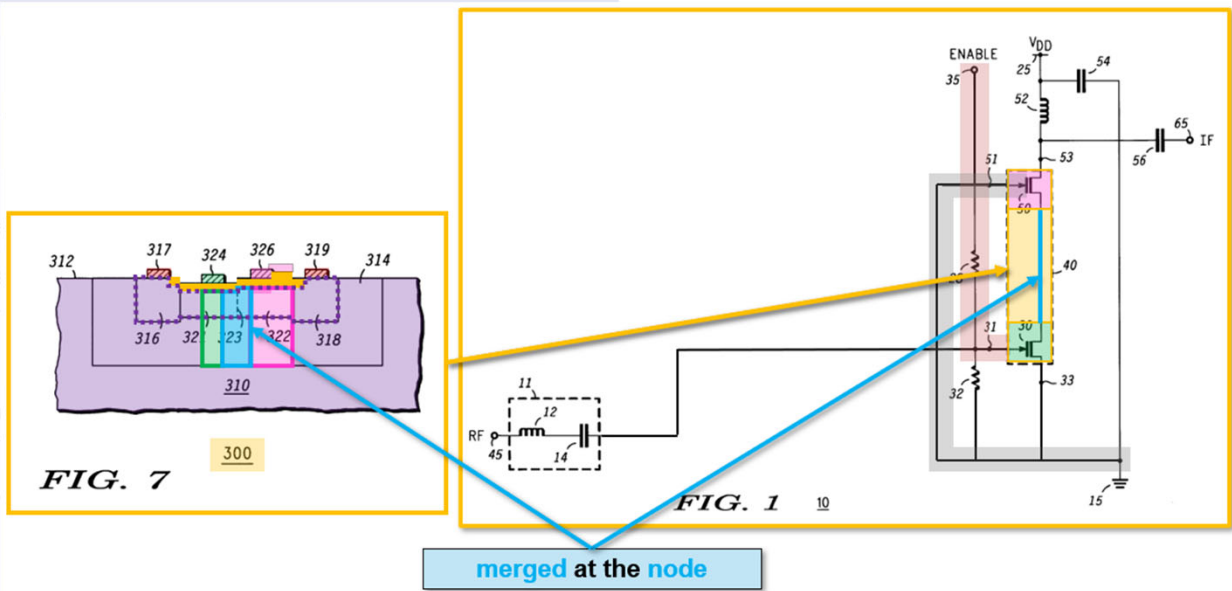
Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element laterally away from the source electrode;
✓	[1C4] a first gate positioned between the source electrode and the drain electrode on the top surface of the semiconductor element to form a first portion of the transistor; and
✓	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode on the top surface of the semiconductor element to form a second portion of the transistor, wherein the second gate is also coupled to the semiconductor element;
✓	[1C6] wherein the first gate is connected to the input voltage signal source such that the first portion of the transistor is based on a value of the input voltage signal and
✓	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
✓	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



Bonn (Ex. 1006), Fig. 7 (annotated).

Ground 2: Bonn-Ren-Mishra

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a
✓	[1C3] a drain electrode electrically connected to the
✓	laterally away from the source electrode;
✓	[1C4] a first gate positioned between the source ele
✓	semiconductor element to form a first portion of the
✓	[1C5] a second gate positioned adjacent to the first
✓	electrode to form a second portion of the transistor,
✓	also coupled to the semiconductor element;
✓	[1C6] wherein the first gate is connected to the input
✓	portion of the transistor is based on a value of the in
✓	[1C7] the second gate is connected to the constant v
✓	transistor conducts until a voltage difference
✓	between the predetermined constant voltage and a
✓	between the first portion and the second
✓	portion of the transistor reaches a predetermined level,
✓	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion
✓	of the transistor is a depletion mode transistor, and
✓	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the
✓	depletion mode transistor at the node in the semiconductor element.



Bonn (Ex. 1006), Figs. 1, 7 (annotated).

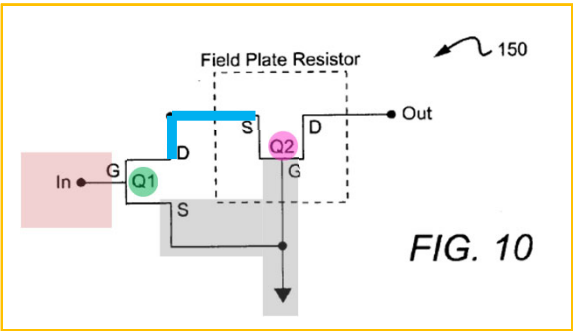
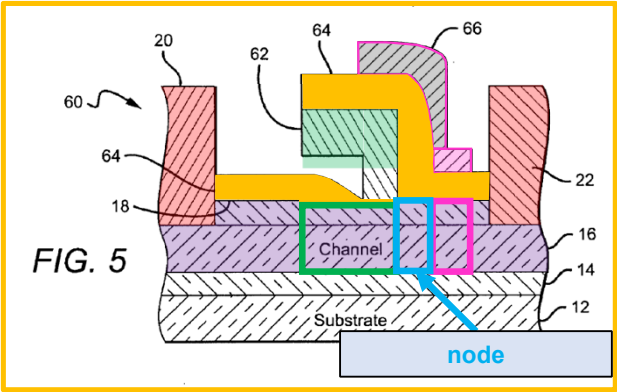
Paper No. 1 at 70-71.

Ground 3: Mishra-Ren renders obvious claims 1-16

	Ground	Challenged Claims	Basis	Prior Art
Bonn Grounds	1	1	§ 103	Bonn and Mizuta
	2	1-16	§ 103	Bonn, Ren, and Mishra
Mishra Ground	3	1-16	§ 103	Mishra and Ren

To find claims 1-16 invalid over Mishra and Ren (Ground 3), the Board need only:

- ✓ Agree that Mishra discloses a dual-gate transistor in a cascode arrangement
- ✓ Agree that it would have been obvious to select the first stage as enhancement mode



Paper No. 1 at 82-114; Mishra (Ex. 1009), Figs. 5, 10.

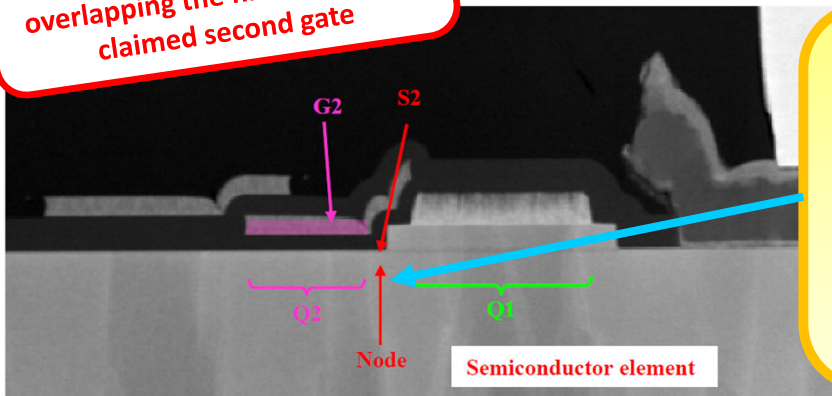
Ground 3: Mishra-Ren renders obvious claims 1-16

Mishra discloses an arrangement with “a single transistor with a dual gate structure”

[0062] It is understood that many different amplifier arrangements can be used according to the present invention. One alternative arrangement comprises a single transistor with a dual gate structure.

Infinion alleges a source-connected field plate overlapping the first gate is the claimed second gate

Mishra (Ex. 1009) at ¶ [0062].



Accused device and Mishra have the same overlapping, source-connected field plate and node

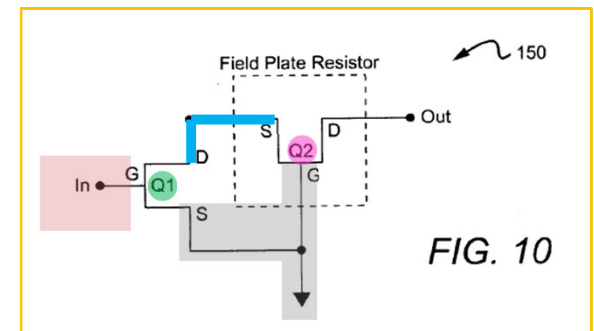
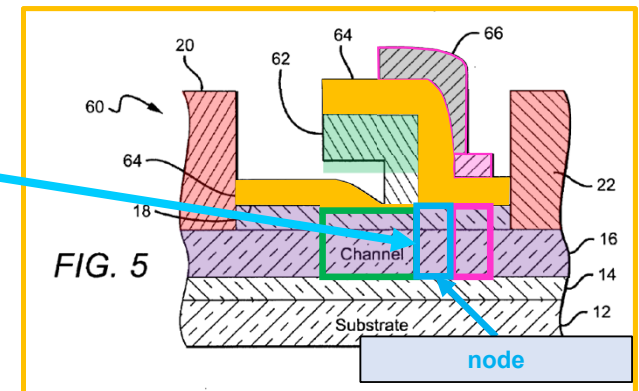


FIG. 10



Mishra (Ex. 1009), Figs. 5, 10.

Paper No. 1 at 82-114; Paper No. 15 at 18-23.

Ground 3: Mishra-Ren renders obvious claims 1-16

Bonn + Ren + Mishra	Limitation
Ren discloses using GaN ✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
Mishra discloses a dual gate transistor in cascode arrangement ✓	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
✓	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
✓	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
✓	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
✓	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
✓	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

Paper No. 1 at 82-114.

Infineon's Arguments:	Innoscence's Arguments:
<div>#1</div> <div>1. Mishra [0062] has no effect, it does not disclose a dual-gate structure</div>	1. Mishra discloses “a single transistor with a dual gate structure.” Mishra, [0062].
<div>#2</div> <div>2. POSITA would not have selected an e-mode first stage transistor</div>	2. There are only two choices, e-mode or d-mode, and a POSITA would have found it obvious to choose e-mode because it improves safety and performance at high frequency amplification

[0062] It is understood that many different amplifier arrangements can be used according to the present invention. One alternative arrangement comprises a single transistor with a dual gate structure.

Ex. 1009 at ¶ [0062].

either one depletion or enhancement mode. There's only two choices, either enhancement or depletion.

Ex. 2009 (Berstein deposition), 11:8-9.

Paper No. 14 at 46-76; Paper No. 15 at 18-23.

Ground 3: Mishra-Ren renders obvious claims 1-16

#1

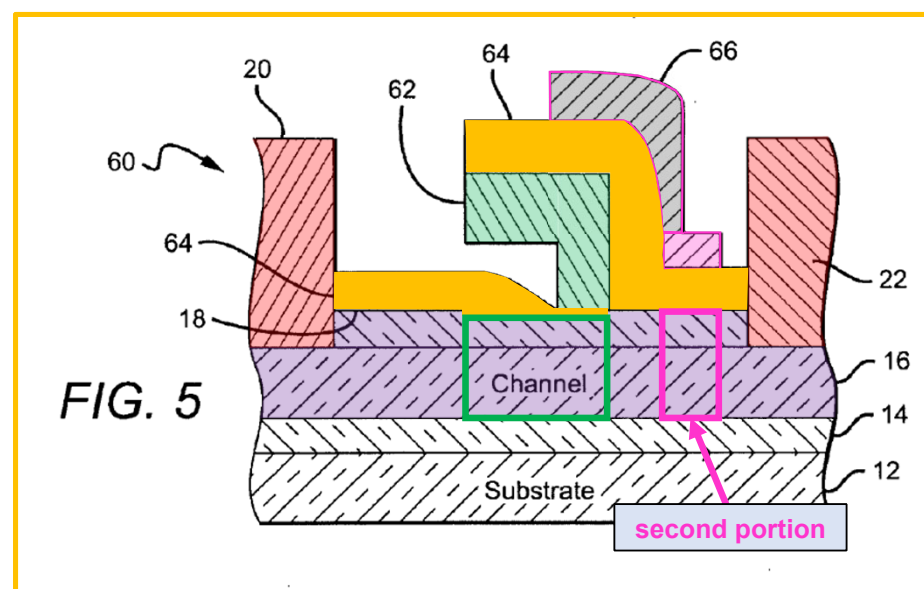
1. Infineon argues
Mishra does not
disclose a dual gate
structure

Mishra's dual gate transistor teaching applies to Figure 5

[0044] Like the field plate 46 shown in FIGS. 3 and 4 and described above, the field plate 66 can be connected to the gate 62 in many different ways. A first conductive path (not shown) can be included between the field plate 66 and the gate contact or a second conductive path (not shown) can be included between field plate 66 and the gate 62, with both the conductive paths being outside the active area of the HEMT. Conductive vias can also be used between the field plate 66 and gate 62 that pass through the spacer layer 64.

Mishra (Ex. 1009) at ¶ [0044]

Mishra teaches connecting its field plate to source, which makes a dual gate device with claimed second gate



Mishra (Ex. 1009), Fig. 5 (annotated).

Ground 3: Mishra-Ren renders obvious claims 1-16

#1

1. Infineon argues Mishra does not disclose a dual gate structure

Mishra discloses more detail than the '003 patent, including transistor structure and how to make and operate transistors



Prior art that provided a “level of detail similar to” the patent was enabling. *Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461 (Fed. Cir. 1997)

[0036] The spacer layer 24 can be etched to the barrier layer 18 and a gate electrode 26 deposited such that the bottom of the gate electrode 26 is on the surface of barrier layer 18. The metal forming the gate electrode may be patterned to extend across spacer layer 24 so that the top of the gate 26 forms a field plate structure 28 extending a distance L_f away from the edge of gate 26 towards drain 22. Stated differently, the part of the gate metal resting on the spacer layer 24 forms a field plate 28. Finally, the structure can be covered with a dielectric passivation layer 30 such as silicon nitride. Methods of forming the dielectric passivation 30 are described in detail in the patents and publications referenced above.

[0029] The field plate can be electrically connected to the gate contact and in some embodiments the field plate is formed as an extension of the gate contact while in other embodiments the field plate and gate electrode are formed during separate deposition steps. In still other embodiments the field gate can be connected to the source contact. This field plate arrangement can reduce the peak electric field in the device that can result in increased breakdown voltage and reduced trapping. The reduction of the electric field can also yield other benefits such as reduced leakage currents and enhanced reliability.

Mishra (Ex. 1009) at ¶ [0029].

Mishra discloses many details on how to implement its gates

Paper No. 15 at 19-21.

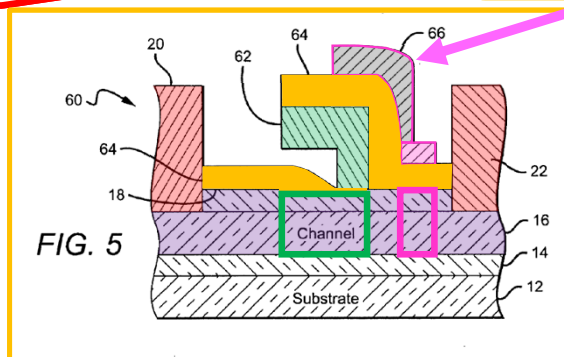
Mishra (Ex. 1009) at ¶ [0036].

Ground 3: Mishra-Ren renders obvious claims 1-16

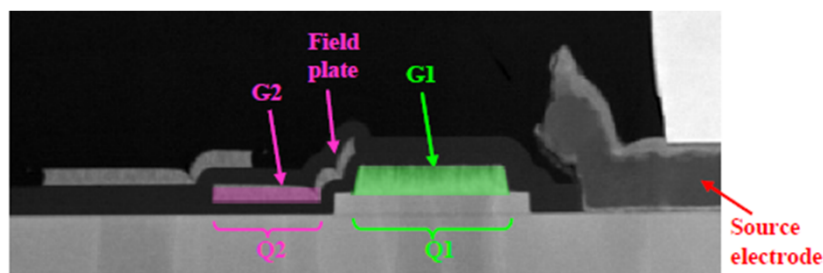
#1

1. Infineon argues
Mishra does not
disclose a dual gate
structure

Mishra discloses a **source connected field plate**, which is
the second gate under Infineon's theories



Mishra (Ex. 1009) at ¶ [0036].



(Cross-sectional view TEM image of INN100W032A, annotations added)

Ex-1001, 21

- Field plates can “be connected to the source contact in many different ways.” Mishra, [0063].
- Mishra discloses that conductive vias connect field plates to other structures. Mishra, [0040], [0044], [0052].
- Mishra has a “second stage field-plated transistor connected in common gate configuration,” i.e. connected to source, which is the norm for cascodes. Mishra, [0056], Fig. 10; Paper No. 1, 82-83; Ex-2009, 13:12-14:11.
- Mishra extensively discusses the characteristics of its field plate. Mishra, [0026]-[0029], [0036]-[0063], Fig. 7.

Paper No. 1 at 27, 82-83; Paper No. 15 at 21-24; Mishra at [0029], [0053], [0063]

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 3: Mishra-Ren renders obvious claims 1-16

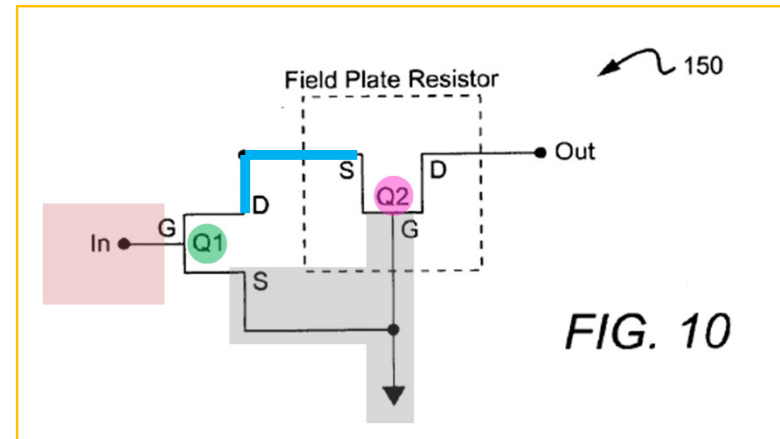
#2

2. Infineon argues a POSITA would not have selected an e-mode first stage transistor

There are only two transistor options: enhancement mode or depletion mode

either one depletion or enhancement mode. There's only two choices, either enhancement or depletion.

Ex. 2009, 11:8-9.



Mishra (Ex. 1009), Fig. 10 (annotated).

The Parties dispute whether Mishra's first transistor is in enhancement mode

Ground 3: Mishra-Ren renders obvious claims 1-16

#2

2. Infineon argues a POSITA would not have selected an e-mode first stage transistor

Each transistor is either E-Mode or D-Mode, there are only two options

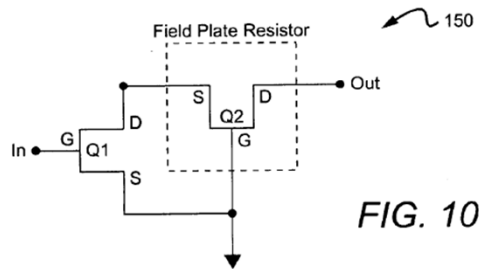


FIG. 10

Mishra (Ex. 1009), Figure 10

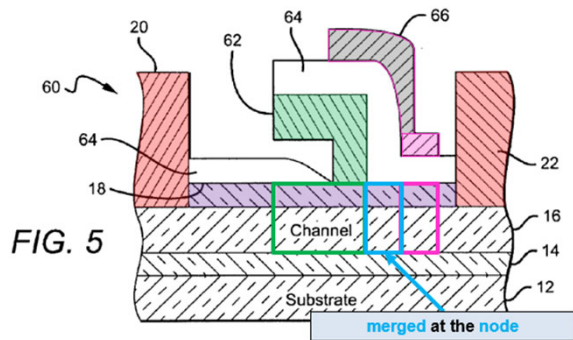


FIG. 5

either one depletion or enhancement mode. There's only two choices, either enhancement or depletion.

Ex. 2009, 11:8-9.

Four options

First Transistor	Second Transistor
E-Mode	D-Mode
E-Mode	E-Mode
D-Mode	E-Mode
D-Mode	D-Mode

E-Mode followed by D-Mode would have been obvious:

- Limited options: e-mode or d-mode
- Mishra discloses low control voltages
- Reduced power consumption
- Suitable for high-voltage, high-frequency applications

Paper No. 1 at 5, 84-88; Paper No. 15 at 24-27.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

75

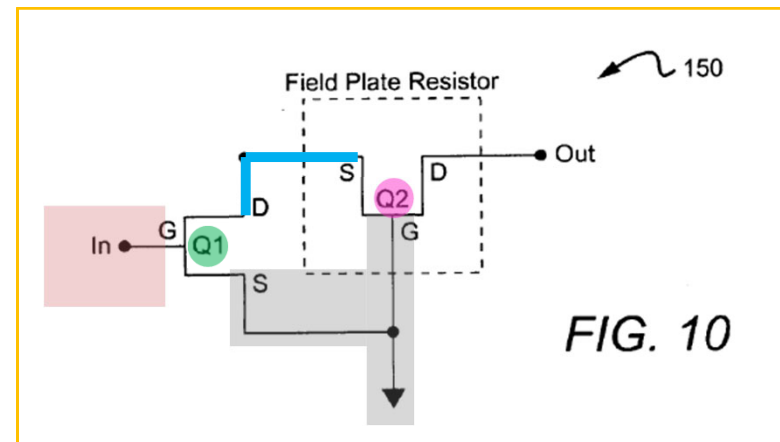
Ground 3: Mishra-Ren renders obvious claims 1-16

#2

2. Infineon argues a POSITA would not have selected an e-mode first stage transistor

It would have been obvious to a POSITA to implement Mishra's first stage transistor as enhancement in the dual gate cascode embodiment with a second stage transistor as depletion mode

Parties agree that Mishra's second stage transistor **Q2** is in depletion mode



Mishra (Ex. 1009), Fig. 10 (annotated).

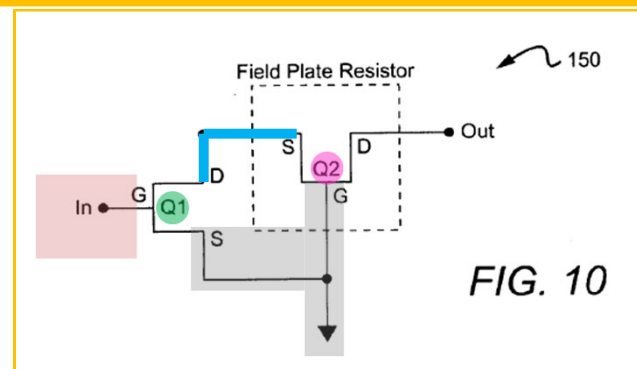
Ground 3: Mishra-Ren renders obvious claims 1-16

#2

2. Infineon argues a POSITA would not have selected an e-mode first stage transistor

It would have been obvious to a POSITA to implement Mishra's first stage transistor as enhancement in the dual gate cascode embodiment with a second stage transistor as depletion mode

[0060] Higher breakdown voltage and higher power operation is enabled by the second stage transistor Q2 (or subsequent stages) which includes a field plate to reduce the electric field within the device. Hence the multi-stage amplification block 100 obtains the benefits of the field plate without detrimental impact on the overall gain of the amplifier block. Stated differently, any field plate capacitance shows up at output capacitance in the second stage instead of feedback capacitance, which can significantly improve gain. Q1 can be biased at a low voltage ($-6V$) and provides current gain, while Q2 is biased at a high voltage and generates voltage gain. Non-field-plate devices are more suited to lower voltage operation (where dispersion is not a problem), while field plated devices are more suited to high bias operation. Multi-stage amplifier blocks according to the present invention combine the strengths of both these devices.



Mishra (Ex. 1009), Fig. 10 (annotated).

Low voltages at first stage transistor Q1 include low positive voltages, making enhancement mode obvious

Infineon never explains why Mishra's low voltage excludes low positive voltage

Mishra (Ex. 1009) at ¶ [0060].

Paper No. 15 at 24-27.

Ground 3: Mishra-Ren renders obvious claims 1-16

#2

2. Infineon argues a POSITA would not have selected an e-mode first stage transistor

It would have been obvious to a POSITA to implement Mishra's first stage transistor as enhancement in the dual gate cascode embodiment with a second stage transistor as depletion mode

[0005] One area that still has not been fully exploited is the engineering of substrates to achieve higher carrier mobility. Gallium nitride (GaN), which is a Group-III nitride compound semiconductor, has a large forbidden band gap, equal to about 3.4 eV. The indirect transition conduction band is positioned at a level higher than the forbidden band by more than 1.5 eV. The saturation velocity of GaN is approximately 2.5×10^7 cm/s, which is higher than other types of semiconductors, such as silicon (Si), gallium arsenide (GaAs), and silicon carbide (SiC). Further, the breakdown electric field of GaN is approximately 5×10^6 V/cm, which is greater than SiC, and greater than Si and GaAs by more than one order of magnitude. Thus, GaN has physical characteristics that are suitable for use in high-frequency, high-temperature, and high-power semiconductor devices.

Ren (Ex. 1008) at ¶ [0005].

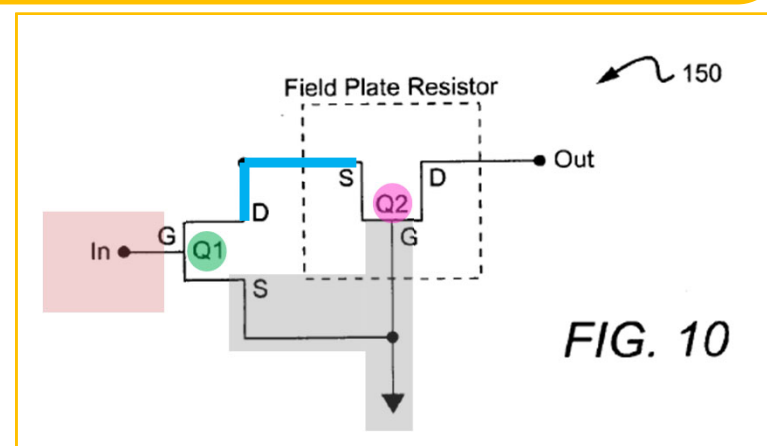


FIG. 10

Mishra (Ex. 1009), Fig. 10 (annotated).

Ren motivates enhancement mode Q1 for power-saving benefits and reduced gate leakage

Ground 3: Mishra-Ren renders obvious claims 1-16

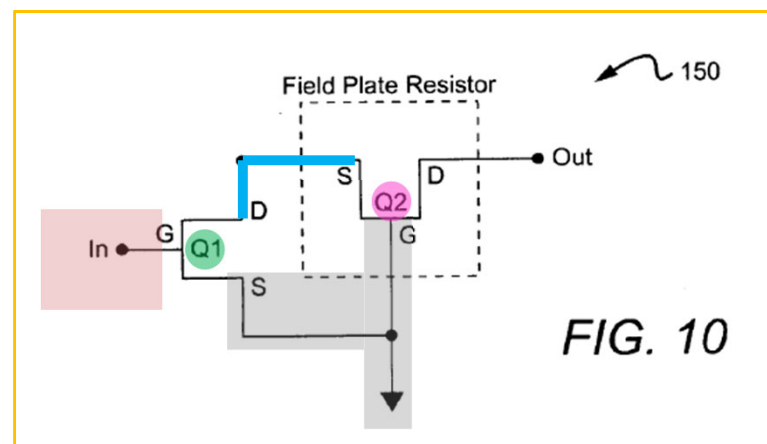
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2. Infineon argues a POSITA would not have selected an e-mode first stage transistor

It would have been obvious to a POSITA to implement Mishra's first stage transistor as enhancement in the dual gate cascode embodiment with a second stage transistor as depletion mode

[0056] A 2-stage cascode amplifier structure (or amplification block) in accordance with embodiments of the invention includes a first stage transistor connected in common source configuration and a second stage field-plated transistor connected in common gate configuration. The first stage is arranged to provide current gain and does not "see" high voltages, while the second field plated stage does see high voltages and is arranged to provide voltage gain.

Mishra (Ex. 1009) at ¶ [0056].



Mishra (Ex. 1009), Fig. 10 (annotated).

Mishra discloses second stage as depletion mode, and it would have been obvious to implement first stage as enhancement

Ground 3: Mishra-Ren renders obvious claims 1-16

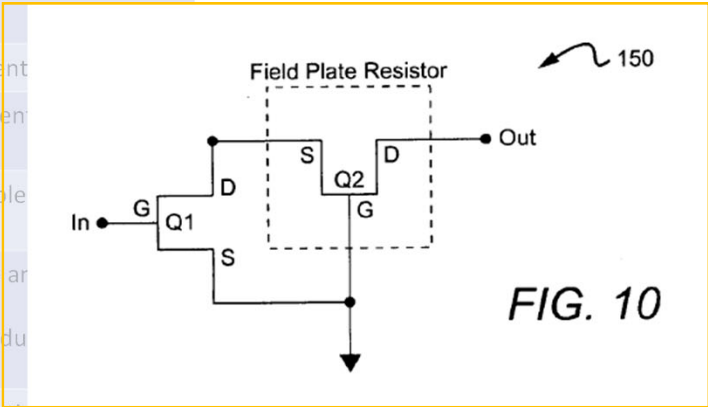
	Infineon's Arguments:	Innoscence's Arguments
#1	1. Mishra [0062] has no effect, it does not disclose a dual-gate structure	1. Mishra discloses "a single transistor with a dual gate structure." Mishra, [0062].
#2	2. A POSITA would not have selected an e-mode first stage transistor	2. There are only two choices, e-mode or d-mode, and a POSITA would have found it obvious to choose e-mode because it improves safety and performance at high frequency amplification

Mishra discloses a dual-gate structure and a POSITA would have found it obvious to choose a first stage enhancement mode transistor

Paper No. 14 at 46-76; Paper No. 15 at 18-23.

Ground 3: Mishra-Ren

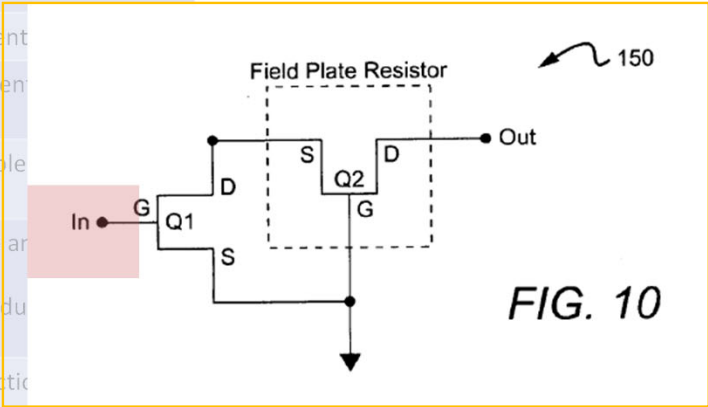
Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
	[1A] an input voltage signal source having an input voltage signal;
	[1B] a constant voltage source having a predetermined constant voltage;
	[1C] a merged cascode transistor comprising:
	[1C1] a semiconductor element;
	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



Mishra (Ex. 1009), Fig. 10.

Ground 3: Mishra-Ren

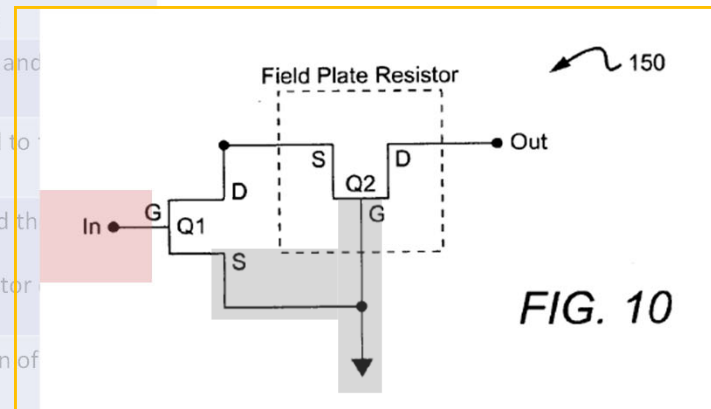
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	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
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	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



Mishra (Ex. 1009), Fig. 10 (annotated).

Ground 3: Mishra-Ren

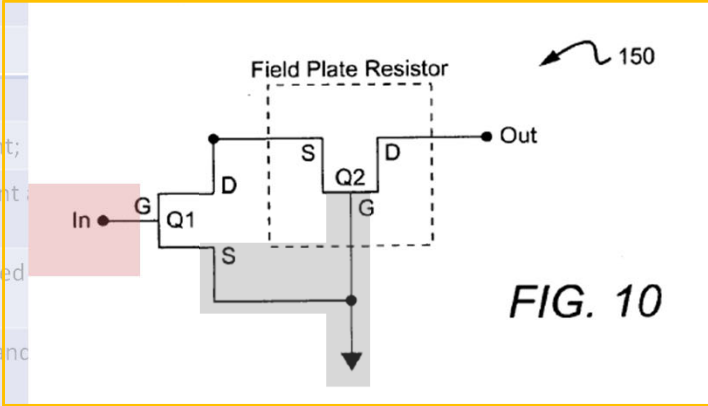
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	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
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Mishra (Ex. 1009), Fig. 10 (annotated).

Ground 3: Mishra-Ren

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	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
	[1C5] a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
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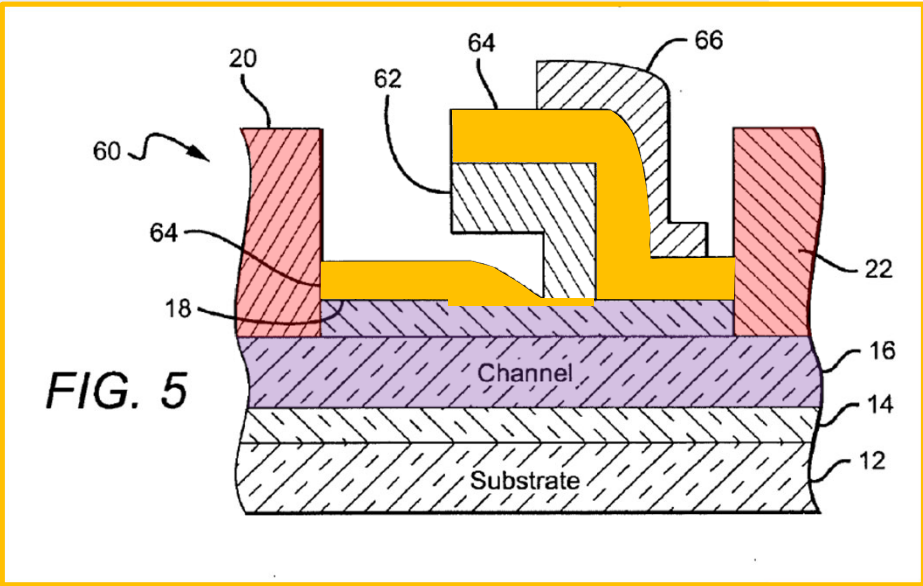


Mishra (Ex. 1009), Fig. 10 (annotated).

Ground 3: Mishra-Ren

Paper No. 1 at 92-93.

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✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
	[1C4] a first gate positioned between the source electrode and the drain electrode on the top surface of the semiconductor element to form a first portion of the transistor;
	[1C5] a second gate positioned adjacent the drain electrode to form a second portion of the transistor, wherein the second gate in the second portion of the transistor is positioned laterally away from the first gate;
	[1C6] wherein the first gate is connected to a first terminal of the input voltage signal source and the second gate is connected to a second terminal of the input voltage signal source;
	[1C7] the second gate is connected to the constant voltage source until a voltage difference between the predetermined constant voltage and the input voltage signal reaches a predetermined threshold voltage;
	[1C8] wherein the first portion of the transistor is a depletion mode transistor;
	[1C9] wherein a drain region of the depletion mode transistor is at the node in the semiconductor element.

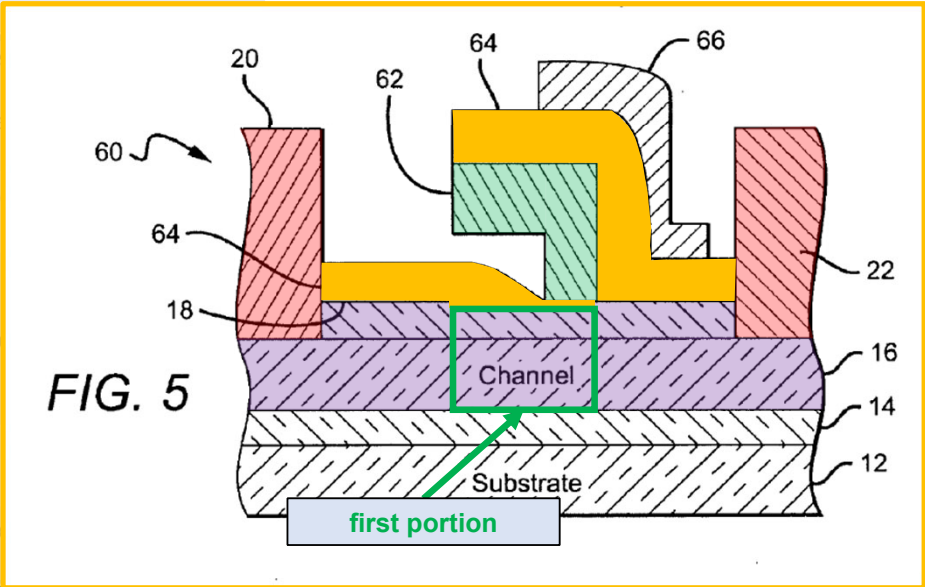


Mishra (Ex. 1009), Fig. 5 (annotated).

Ground 3: Mishra-Ren

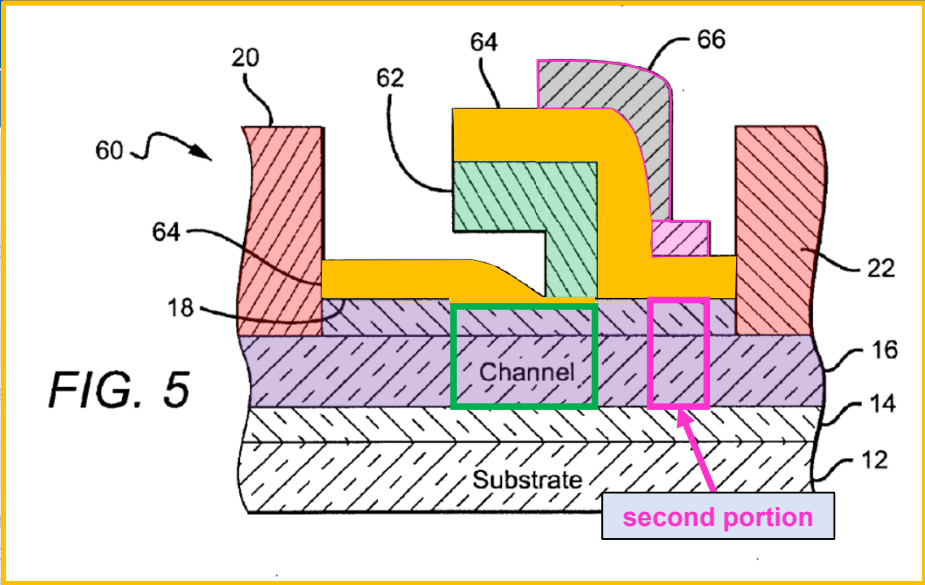
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	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a drain region of the depletion mode transistor at the node in the semiconductor element.

Mishra (Ex. 1009), Fig. 5 (annotated).



Ground 3: Mishra-Ren

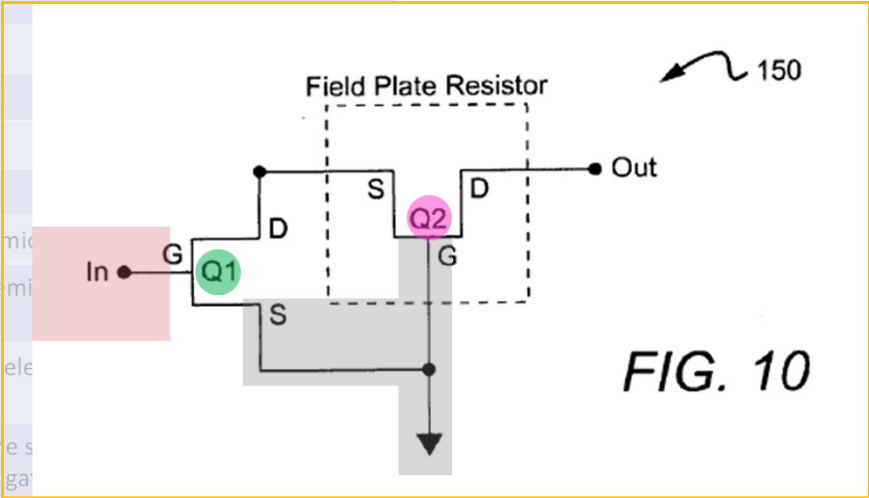
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Mishra (Ex. 1009), Fig. 5 (annotated).

Ground 3: Mishra-Ren

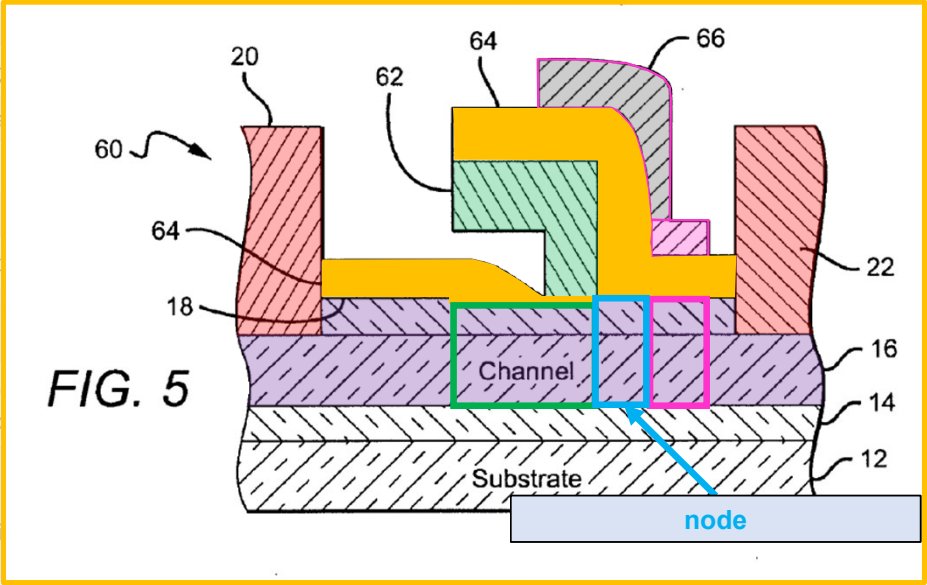
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	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
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Mishra (Ex. 1009), Fig. 10 (annotated).

Ground 3: Mishra-Ren

Bonn + Mizuta	Limitation
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✓	[1C4] a first gate positioned between the source electrode and the drain electrode to form a first portion of the transistor;
✓	[1C5] a second gate positioned adjacent to the first gate, and a second electrode to form a second portion of the transistor, wherein the second gate includes a field plate and a second electrode;
✓	[1C6] wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and
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Mishra (Ex. 1009), Fig. 5 (annotated).

Ground 3: Mishra-Ren

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an output voltage;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to the semiconductor element;
✓	[1C3] a drain electrode electrically connected to the semiconductor element laterally away from the source electrode;
✓	[1C4] a first gate positioned between the source electrode and the drain electrode to form a first portion of the transistor;
✓	[1C5] a second gate positioned adjacent to the drain electrode to form a second portion of the transistor, the second gate also coupled to the semiconductor element;
✓	[1C6] wherein the first gate is connected to the input voltage signal source and the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
✓	[1C7] the second gate is connected to the constant voltage source such that the second portion of the transistor conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level,
✓	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

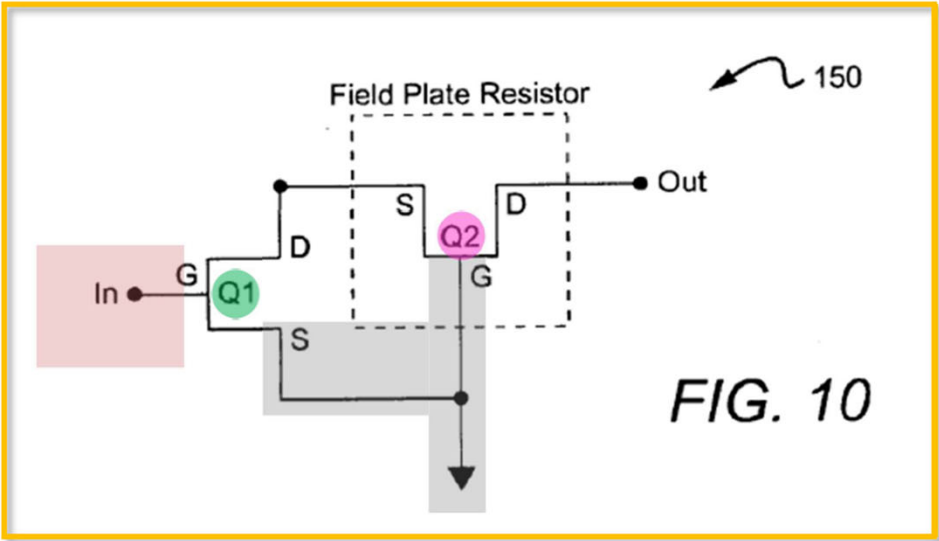


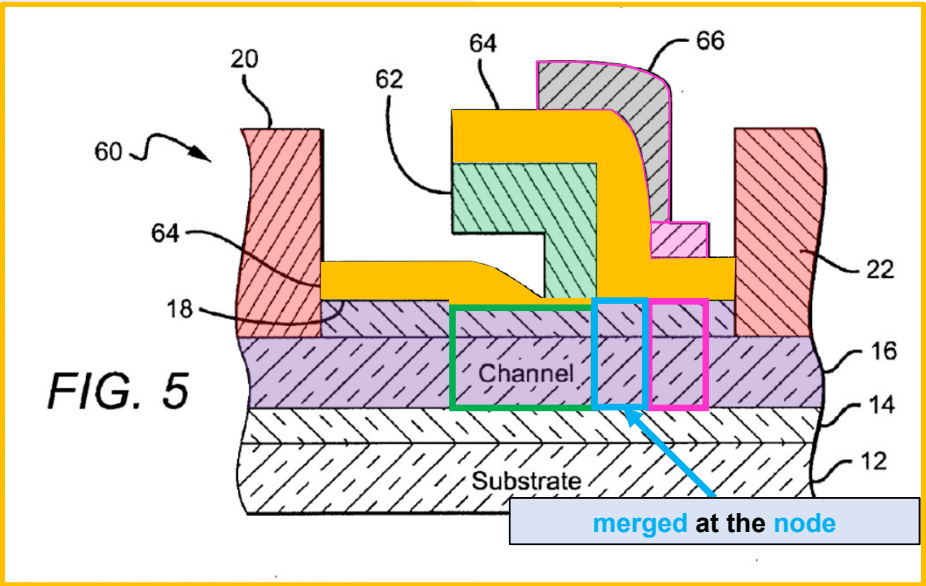
FIG. 10

Mishra (Ex. 1009), Fig. 5 (annotated).

Paper No. 1 at 100-101.

Ground 3: Mishra-Ren

Bonn + Mizuta	Limitation
✓	[1PRE] A merged cascode transistor circuit comprising:
✓	[1A] an input voltage signal source having an input voltage signal;
✓	[1B] a constant voltage source having a predetermined constant voltage;
✓	[1C] a merged cascode transistor comprising:
✓	[1C1] a semiconductor element;
✓	[1C2] a source electrode electrically connected to a top surface of
✓	[1C3] a drain electrode electrically connected to the top surface of
✓	[1C4] a first gate positioned between the source electrode and the
✓	[1C5] a second gate positioned adjacent to the first gate, and betw
✓	[1C6] wherein the first gate is connected to the input voltage sign
✓	[1C7] the second gate is connected to the constant voltage source
✓	[1C8] wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and
✓	[1C9] wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.



Mishra (Ex. 1009), Fig. 5 (annotated).

Paper No. 1 at 101-103.

All claims of the '003 patent are unpatentable

Questions ?



Thank you