

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

IPR2025-00094
Patent 8,264,003 B2

Record of Oral Hearing
Held: April 8, 2026

Before: JO-ANNE M. KOKOSKI, CHRISTOPHER M. KAISER, and
LISA A. MURRAY, *Administrative Patent Judges*.

APPEARANCES:

ON BEHALF OF THE PETITIONER:

LUKE H. MACDONALD, ESQ.
LIONEL M. LAVENUE, ESQ.
DEANNA C. SMILEY, ESQ.
Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
901 New York Ave NW
Washington, D.C. 20001
(202) 408-4000
luke.macdonald@finnegan.com
lionel.lavenue@finnegan.com
deanna.smiley@finnegan.com

ON BEHALF OF THE PATENT OWNER:

SCOTT A. MCKEOWN, ESQ.
JASON W. BALICH, ESQ.
Wolf Greenfield & Sacks, P.C.
600 Atlantic Ave. Fl. 23
Boston, MA 02210
(617) 646-8000
smckeown-ptab@wolfgreenfield.com
jbalich-ptab@wolfgreenfield.com

The above-entitled matter came on for hearing on April 8, 2026,
commencing at 12:58 p.m., via video teleconference.

P R O C E E D I N G S

- - - - -

JUDGE KAISER: Okay. Good afternoon, everyone. This is a hearing in IPR2025-00094, caption, Innoscience America, Incorporated versus Infineon Technologies Americas Corporation challenging patent 8,264,003. I'm Judge Kaiser. And the panel also includes Judge Murray, who's in the hearing room in Alexandria, and Judge Kokoski, who is appearing remotely. Let's please start with appearances. And we'll start with anyone here on behalf of Petitioner.

MR. MACDONALD: Thank you, Your Honor. This is Luke MacDonald on behalf of the Petitioner from the law firm, Finnegan. I'm joined today with my colleagues, Mr. Lionel Lavenue and Ms. Deanna Smiley, also from Finnegan.

JUDGE KAISER: Okay. Welcome to all of you. And anyone here on behalf of Patent Owner?

MR. BALICH: Yes, Your Honors. My name is Jason Balich from Wolf Greenfield. I'll be arguing today for Patent Owner Infineon. Also here with me today are my colleagues, lead counselor for Patent Owner, Scott McKeown and Greg Corbett, both of Wolf Greenfield.

JUDGE KAISER: Okay. Thank you. Welcome to all of you as well. All right. So each side is going to have 60 minutes total to present its arguments. Petitioner has the burden of proof and will present first and may reserve some of its 60 minutes for rebuttal. Patent Owner will present its arguments after Petitioner's initial presentation, and Patent Owner can reserve some of its time for surrebuttal.

1 Just a couple of reminders before we start. First, as noted in the
2 hearing order, this hearing is open to the public and there may be members
3 of the public present in the room or listening or viewing on the public line.
4 As far as I'm aware, there isn't any confidential material on the record in this
5 proceeding, so I don't really anticipate any problems there.

6 The panel has access to the demonstrative exhibits and all of the
7 papers and exhibits that have been filed. If you'd be so kind, in order to keep
8 a clear record, when you refer to a demonstrative exhibit or anything in the
9 record, please give us the number of the demonstrative exhibit or the slide or
10 the exhibit number that you're referring to along with a page number or
11 something to point us in the right direction. And just to help those of us who
12 are attending remotely, please make sure when you are speaking today that
13 you speak into a microphone so that we can hear you.

14 So I think with those preliminaries out of the way, we're ready to
15 get started. I'll ask Petitioner's counsel, how much time would you like to
16 reserve for rebuttal?

17 MR. MACDONALD: Thank you, Your Honor. Five minutes for
18 rebuttal, please.

19 JUDGE KAISER: Okay. So we'll give you 55 minutes. And I
20 think you can start whenever you're ready.

21 MR. MACDONALD: Thank you, Your Honors. Again, this is
22 Luke MacDonald for the Petitioner. Today we're going to talk, as we just
23 spoke, about the '003 Patent. We'll begin with an overview of the prior art
24 and then get into the invalidity grounds. Now, we've included this Slide 2
25 here, shown on our screen as a table of contents, in case Your Honors have

1 any questions or want to jump to any particular section. This is a handy
2 guide.

3 And as we will see, all claims are unpatentable. I'm looking now
4 at Slide 4 of the Petitioner's demonstratives. And one thing to keep in mind
5 is that the only thing in the '003 Patent that led to allowance after seven
6 rejections is this tiny blue square shown here on the screen. This is simply a
7 region that is between two transistors on a dual-gate transistor structure.

8 Now, the particular structure described in the '003 Patent is to have
9 a first gate that is in enhancement mode. It's the green gate here on this slide
10 with -- and it -- a second gate, which is in depletion mode that has a field
11 plate. And the second gate is in pink here on this slide. And so the only
12 thing that led to allowance, the purported point of novelty, is that blue
13 square, which resides between the portion under the first gate and the portion
14 under the second gate. Once that was described in words, after seven
15 rejections, the patent office allowed it.

16 Now, moving on to Slide 5. We do see here the same schematic
17 we were just looking at, plus the circuit diagram. The circuit diagram on the
18 left simply shows that this transistor is wired in the standard cascode
19 arrangement, namely, common source, common gate, where the input to the
20 second gate is connected to ground and the source side of the first gate is
21 also connected to ground. So this is the normal cascode arrangement.

22 And before we proceed any further with the demonstratives, I just
23 wanted to peruse the patent itself. So I'm going to switch my screen over to
24 the '003 Patent which I'm showing here on the screen, this is Exhibit 1001 to
25 the proceeding. Now, one thing to keep in mind about this patent is it's only

1 nine pages long. It only has four figures. Let's look through them briefly.

2 So Figure 1 is prior art. Figure 2 is this cascode circuit. Figure 3
3 is a very basic diagram showing this dual-gate structure drawn in a rough
4 fashion. And Figure 4 is the almost the exact same figure with very few
5 difference, only described in the body of the specification as being a GaN
6 device.

7 Now, if we look at the specification for the '003 Patent, we see it
8 only has four and a half columns. Let's take a look at that. So the first
9 column, we have the background section. Second column, we begin to
10 describe some of the detailed embodiments. When you get to the dual-gate
11 structure -- we're in column 3 now -- of the '003 Patent, the description
12 begins around line 51 and it continues to column 4 and ends around lines 22.
13 So that is the entirety of how the -- this patent describes making its device.

14 Similarly, column 4 continues the description with Figure 4. And
15 it begins there, right around line 24 and continues halfway down column 5 to
16 about line 23. So it's just a few paragraphs for each figure. And when the
17 patent tells us to make its device, it simply refers to the rough location of
18 these different features of the patent, and it lists some materials. It says, you
19 know, a POSITA, go ahead and make my device.

20 I'll give you some example materials. But you know how to
21 implement this. You know how to make an enhancement mode, I'm not
22 going to bother to tell you. You know how to make a depletion mode, I'm
23 not going to bother to tell you. None of those details are in the patent. So I
24 think that's important to keep in mind as we go through Petitioner's
25 presentation.

1 I'm looking now at Slide 6 of the demonstratives. We'll see that
2 this merged region, the sole point of alleged inventiveness was known in the
3 prior art. Bonn is shown on the top right, that's one of the asserted
4 references. Bonn has a dual-gate structure. Bonn has a first gate which is in
5 enhancement mode and a second gate which is in depletion mode. And
6 there's a region between those two gates which is necessary in a dual-gate
7 structure. That's just the space between them. And we've shaded it here in
8 blue to show that this is the claimed merged region. It's the same space. It's
9 on the drain side of one gate and the source side of the second gate.

10 Now, when Bonn describes its device, it's a much longer
11 disclosure. It describes a lot of details about how to make its device, how to
12 dope its device, the channel depth, the channel width, the thickness of
13 various layers. All those details are found in Bonn. Likewise, we see a
14 merged region in the Mishra reference also in the asserted grounds. And in
15 the Mishra reference, we have a lot of disclosure about its source-connected
16 fuel plate, that is the pink structure on the right, and a lot of disclosure about
17 other features of its device, which is the first gate shown in green here on the
18 right.

19 And now, the Mishra reference discloses to connect that pink
20 structure, which is a source-connected fuel plate to the source. It says you
21 can do it in a lot of ways -- that's in paragraph 63 of Mishra -- without regard
22 to any figure. It just tells a POSITA, you know, you can go and to connect
23 this field plate to source. Now, under Infineon's theory, that little flat, planar
24 region that's shaded in pink is a gate. And that squiggly portion that
25 overlaps the first gate is a field plate.

1 And when you connect that structure to source, you have a source-
2 connected field plate, which under Infineon's theory is a second gate,
3 according to the patent. So this is what they've alleged infringes the device.
4 When you do that, you'll see Mishra has that exact blue region, which is that
5 spacing between the two gates.

6 Moving on to Slide 7. We see here again, Bonn's disclosure. And
7 we just wanted to emphasize that Bonn has a dual gate FET, that's a field
8 effect transistor. It has the merged region. It has enhancement mode. And
9 it has depletion mode. So these are the main features of the patent that
10 purportedly led, you know, to its novelty over the prior art.

11 Looking at Slide 8, we see a reproduction of Claim 1 and different
12 portions of the figure are color coded and mapped to features of the claims,
13 so namely, that first gate, the second gate, the merged region. Most of our
14 discussion today is going to be on those claim features. And Claim 1,
15 importantly, does not require gallium nitride materials.

16 So that's something that the patent reserves for dependent claims
17 that depend from Claim 1 or the second independent claim, which is Claim
18 10. So anything that might be special about gallium nitride -- and which the
19 Patent Owner alleges is inventive -- or the prior art doesn't apply to Claim 1.
20 It only applies to those other claims.

21 So let's get into the invalidity grounds. I'm looking at Slide 11
22 right now. Our invalidity grounds fall into two main buckets. The first two
23 grounds rely on Bonn as a primary reference. And the second bucket is the
24 Mishra ground, which is Ground 3, where Mishra is the primary reference.

25 So as we will discuss today, the Bonn primary reference has all the

1 features of the claimed transistor and the features of the circuit. And we're
2 relying on Mizuta in that first round, just for the field plate. And Patent
3 Owner never alleges that it wouldn't have been obvious to use a field plate in
4 Bonn's device.

5 Secondly, we have Ground 2. This is the combination of Bonn,
6 Ren, and Mishra, where we're relying on Ren and Mishra for their gallium
7 nitride disclosures. Ren tells us how to adjust both gates of Bonn's dual-gate
8 structure to make one enhancement mode and the other depletion mode.

9 And finally, the Mishra and Ren grounds, where we're just relying
10 on Ren for the same teachings to explain how to make an enhancement
11 mode or depletion mode. None of those teachings are included in the
12 specification of the '003 Patent because '003 Patent assumes a POSITA
13 knows how to do all those modifications.

14 In order to find Claim 1 invalid over the prior art, the Board only
15 needs to agree with Petitioner that Bonn teaches using the dual gate FET
16 structure for signal amplification. And from that, all the modifications we
17 propose flow naturally. And all the modifications we propose are supported
18 by Bonn itself, explaining, you know, what its different circuit components
19 do as well as the testimony of Dr. Bernstein.

20 Looking at Slide 13, we've summarized here that there are no
21 particular disputes with respect to the claim limitations checked off in green,
22 including using Mizuta field plates. So most of the argument today focuses
23 on these motivation to combine, motivation to modify. And there's a dispute
24 about whether or not a POSITA would have connected that second gate to
25 the source. But as we will see, that flows directly from Bonn as well as

1 Bonn's teaching of using a cascode, which is, you know, of course, common
2 source, common gate, that's the natural way to do a cascode.

3 Looking at Slide 14, we are now showing the modifications that
4 are sort of the central dispute between the parties. On the left, we see Figure
5 1 of Bonn only modified to shade the dual-gate structure, where the first gate
6 is shaded in green and the second transistor structure is shaded in pink. And
7 Bonn has an important teaching found in column 11, where it tells a person
8 of skill to use its dual-gate structure for high frequency signal amplification.

9 And from that teaching, we have shown that a POSITA would
10 have made this very simple signal amplifier, which is found on the right.
11 And the reason why this is an obvious transformation is that Bonn's dual-
12 gate structure on the left is being used for signal mixing. Signal mixing
13 involves two signals. Once you strip out everything associated with that
14 second signal, you arrive at a much simpler circuit, for example, the one
15 here on the right.

16 You'll hear a lot from Patent Owner, as shown on Slide 15, that Dr.
17 Bernstein is somehow not qualified to opine in this matter. And none of that
18 is true. The agreed upon definition of a person of ordinary skill is someone
19 who possess at least a four-year degree in electrical engineering or closely
20 related field and at least two years of experience in semiconductor device
21 design. So that's shown here on Slide 15, with the usual caveats for
22 swapping education and professional experience.

23 Now, Dr. Bernstein received his bachelor's degree in 1984. He got
24 a master's from MIT in 1986. He has -- he got his PhD in 1990, also from
25 MIT. And he is a professor of electrical engineering. He has been leading a

1 research group in GaN device applications for decades, and he holds patents
2 related to GaN devices. He absolutely meets the definition of a POSITA,
3 and he has the expertise described right here and then some.

4 And the reason why his testimony is reliable is that he's a very
5 honest, incredible expert who followed the teachings right in Bonn to
6 explain what a POSITA would have done to arrive at -- as he described -- a
7 transistor that they would have encountered in their first year of electrical
8 engineering undergraduate school, namely, a signal amplifier.

9 So right here, we see on Slide 16, some of the dispute regarding
10 Dr. Bernstein. And he's explaining that Bonn provides a lot of detail about
11 its circuit. It explains how all of its components work. And so when a
12 person of skill wants to implement that teaching to do a high frequency
13 signal amplification with the dual gate device, Bonn gives all the
14 information a POSITA might need to know to make those changes.

15 And as a result, a POSITA arrives at a circuit which is, according
16 to Dr. Bernstein, the simplest, most normal application for transistor, which
17 is an amplifier. And just, you know, to give you a few citations from his
18 deposition, he says on page 50 of his deposition, which is Exhibit 2009, that
19 he simplified this device to what any POSITA would do to understand how
20 to use a cascode device in a simple amplifier application.

21 And so the fact that he gave some testimony regarding his
22 expertise on RF is irrelevant because the reference is not relied on for signal
23 mixing or down converters or RF applications. He's simply following its
24 teaching to use a signal amplifier.

25 Moving on to Slide 18, we can see readily that Bonn discloses the

1 exact arrangement that the patent purports to have invented. Namely, it says
2 right here from column 8 and column 9, that the first gate region 321 is in
3 enhancement mode and the second gate region 322 is in depletion mode.
4 And so we put little color coded boxes corresponding to that statement into
5 Figure 7 on Slide 18, where you can see that there is indeed a space between
6 the regions under the gates. That is the merged region. It is just what flows
7 naturally from having a dual gate, with one gate being in enhancement mode
8 and the other in depletion mode.

9 And you'll also hear from Patent Owner some arguments with
10 respect to a different amplifier that Bonn discloses. Now, Bonn discloses it
11 has FET 20, that's Field Effect Transistor 20, and it uses it for signal
12 amplification. That's all well and good. Nothing about that disclosure
13 undermines Bonn's other teaching to use its dual-gate transistor for signal
14 amplification. It says it right here in column 11, as we've shown on Slide
15 19.

16 Generally, as shown on Slide 20, Infineon uses three different
17 types of arguments to attack this modification. First, they'll argue that
18 Bonn's -- the modifications are hindsight. But of course, this is not hindsight
19 because the reference itself tells you to use the dual gate device for signal
20 amplification.

21 Second, Infineon will allege that the reference doesn't teach
22 connecting the second gate to constant voltage. But again, signal mixing
23 involves two signals. When we remove one of those signals, that gate is
24 immediately connected to a constant voltage and a POSITA would have
25 even went further by connecting it to ground to make that common cascode

1 arrangement and to do -- to realize greater gain and greater performance, as
2 we explained in the petition.

3 Third, Infineon is alleging that Bonn's modification to achieve
4 signal amplification is somehow unsatisfactory for its intended purpose. But
5 Bonn gives you the purpose. Bonn tells us one of its purposes is signal
6 amplification. And so all the modifications that we propose are just
7 following Bonn's explicit instruction. It is not contrary to any purpose in
8 Bonn.

9 Let's address their first argument here, shown on Slide 21.
10 Infineon argues that this is all hindsight. But Infineon does not dispute that
11 these modifications increase signal amplification. They reduce Miller
12 feedback, that's a noise problem. And they lead to lower noise. All these
13 advantages are not in dispute. And these advantages are realized when one
14 follows Bonn's teaching to use its dual gate device for signal amplification.
15 So it's not hindsight.

16 In addition, the petition very carefully laid out all of the changes
17 that are proposed to Figure 1 of Bonn. It laid it out step by step and referred
18 to each portion of the circuit as Bonn explained it and what it was doing and
19 why it was unnecessary for this second purpose of Bonn, which is signal
20 amplification. Every modification comes from Bonn itself.

21 Shown on Slide 22, we see the first step when signal mixing,
22 which involves two signals, is changed to be signal amplification, which
23 involves one signal. We're going to remove one of those two signals. In the
24 bottom portion of Figure 1 shown on Slide 22, you'll see that the one signal
25 is being fed to the green gate. And it's being mixed with a second signal, the

1 low signal, which is being fed to the pink gate.

2 And once you remove all the circuitry associated with that low
3 signal and this impedance matching components that are associated with that
4 low signal, they're highlighted here in the box in red, then you no longer
5 have a variable input voltage to that second gate. Right now, we have a
6 constant voltage at that second gate.

7 Now, as a second step, because Bonn tells us that you should use
8 its dual gate FET for amplification, we're going to remove the redundant
9 FET 20. A POSITA would understand that this is not needed. And so all
10 the components that Bonn describes as being associated with that second
11 -- with that single gate field effect transistor, FET 20, for signal
12 amplification are no longer needed. They're highlighted here on Slide 23 in
13 red.

14 Once those are removed, a POSITA would understand that the goal
15 is to increase gain. And this capacitor 34, right down here, is no longer
16 needed for its signal amplification embodiment because a POSITA would
17 realize further gain that the voltage difference between VDD, that's at the
18 top on the output of the second gate and the source of the first gate. So that
19 too, as shown on Slide 24, is highlighted in red, and it is blacked out for
20 Slide 25.

21 And finally, we'll consider the voltage divider, which is resistors
22 46 and 48 that operate to split the voltage signal which is received at that
23 pink gate. Now, with one signal being involved in the signal amplification
24 embodiment, we don't need that voltage divider anymore. Moreover, a
25 POSITA would know that because that gate is that depletion gate -- is a

1 depletion mode gate, one of skill would know not to leave that resistor in
2 and require positive voltage to control it. We could just set that right to
3 ground by removing those resistors. So all that is in the petition. That's step
4 4, and we black that out.

5 When you do that, this is automatically connected to ground that's
6 already baked into the wiring of Bonn, as shown on Slide 26. And the result
7 is shown on Slide 27. So this is a basic signal amplifier, as Dr. Bernstein
8 said in his deposition and page 50, it is the first semester electrical
9 engineering student knows how to make -- take a transistor and make an
10 amplifier, how to make a high gain amplifier, a low gain amplifier, and to
11 make a mixer.

12 And that's what we have right here is a very simple amplifier
13 flowing naturally from all of Bonn's teachings. This is the standard cascode
14 wiring that's also found in the '003 Patent. Bonn describes the transistor as a
15 cascode, which is, of course, the common source, common gate, that's on
16 Slide 27 in the modified figure.

17 Moving to Slide 28. We'll next address Infineon on second point
18 about not connecting that second gate to constant voltage. But as we just
19 discussed, as soon as that low signal is removed, the second gate, the pink
20 gate, is already at constant voltage.

21 Moreover, then a POSITA removes the voltage divider, as we've
22 already discussed, to realize the additional gain and make that -- and meet
23 that goal, accomplish the goal of signal amplification. Infineon attacks this
24 idea about this connecting the second gate to constant voltage by introducing
25 an irrelevant reference, which is Mil'Shtein.

1 Okay. Infineon tries to argue that Mil'Shtein somehow counsels
2 against this combination. It teaches away. But Mil'Shtein is not relevant
3 here. It is not one of the asserted references. And it only expresses a
4 general preference for using other approaches besides the constant voltage at
5 the second gate. It only describes that general preference for one parameter,
6 which is the unity limit.

7 So Mil'Shtein considered four setups. And it found that the
8 constant voltage at the second gate had the lowest unity limit. This is the
9 frequency above which no gain is realized. So there's amplification below
10 5.5 gigahertz, but not above. And Mil'Shtein expressed his general
11 preference. That is not a teaching away.

12 Moreover, Patent Owner will tell you today that somehow Dr.
13 Bernstein concealed this reference. Nothing could be further from the truth.
14 In his deposition, Dr. Bernstein mentioned that he had seen this reference
15 before -- recently. His deposition occurred months after he filed his
16 declaration.

17 Moreover, it would not be unusual that Dr. Bernstein, who is a
18 professor in Israel, who is an expert in the narrow field of semiconductors,
19 was familiar with Dr. Mil'Shtein, who was also taught at Israeli universities
20 and who was also working in the same field. So there's nothing here,
21 although Patent Owner thinks they have something special, which shows
22 that the combinations was not obvious. All the combinations that we'll talk
23 about today flow directly from the references themselves and have nothing
24 to do with Mil'Shtein's analysis of optimizing performance around that one
25 parameter, which is the unity limit.

1 Moving on to Slide 30, we will address now Infineon's argument
2 that somehow signal amplification is unsatisfactory for Bonn's purpose.
3 And that is simply not true. So shown here on Slide 30 is another quote
4 from column 11, showing again that Bonn tells us to use the dual gate for
5 high frequency signal amplification. There's nothing here that shows that
6 this would be contrary to Bonn's purpose.

7 In making this argument, as shown on Slide 31, Infineon alleges a
8 very complicated technical defense in which they say that Figure 7 has
9 unequal current carrying capacity. And because of this, somehow you
10 would never use the transistor of Figure 7 for signal amplification. But that
11 is not true. So Bonn tells us that the features which control current carrying
12 capacity are optional.

13 And Bonn tells us that in some embodiments, the first gate will
14 have a smaller current carrying capacity than the second gate. It also tells us
15 that in other embodiments, the first gate will have a larger current carrying
16 capacity than the other gate. These current carrying capacity modifications
17 are completely optional and fully configurable.

18 So let's turn now to Slide 32. We see here a figure from the Patent
19 Owner response. And here, the Patent Owner has highlighted in yellow
20 these nonconductive regions. And again, Bonn says those regions are
21 optional, those regions are fully configurable. Here is the embodiment
22 shown in the top right of Slide 32 where we see Bonn describing a dual gate
23 cascode transistor with a smaller current carrying capacity under the first
24 gate. That's column 5, lines 37 to 40.

25 Another embodiment shown on Slide 32 shows a larger current

1 carrying capacity under the second gate. And when Bonn describes Figure
2 7, it never mentions the current carrying capacity under either gate. It's not
3 something that it considers. So all of Dr. Choi's analysis regarding unequal
4 current carrying capacity is simply not applicable. The law of obviousness
5 doesn't say you even have to use the best option, just one of the options.
6 This is a suitable option. And Bonn describes doing its transistor in many
7 different ways. Infineon will tell you that we didn't rebut Dr. Choi's
8 testimony. But this is our rebuttal right here. It's simply not true.

9 Looking on Slide 33, we have now shown that each of Infineon's
10 attacks to the modifications does not succeed. So Bonn's modifications are
11 not hindsight because Bonn tells us to tailor its device to signal
12 amplification. And by teaching that, Bonn teaches to connect that second
13 gate to constant voltage. And a POSITA would have done that for various
14 reasons, as described in the petition, for all the benefits that are undisputed.

15 Bonn also tells us that its intended purpose is signal amplification.
16 So there's nothing about the modification which is hindsight here or
17 unsatisfactory for its intended purpose. So with that, I'm going to jump now
18 to the second ground.

19 JUDGE KAISER: All right. Before you do that, can I interrupt
20 you for just a minute?

21 MR. MACDONALD: Yes, absolutely, Your Honor.

22 JUDGE KAISER: I'd like to focus on the language at column 11
23 of Bonn that you've been talking about as sort of Bonn disclosing a -- I guess
24 maybe I'll call it a secondary purpose for signal amplification, in addition to
25 down conversion and signal mixing. That paragraph strikes me as at least

1 potentially ambiguous. That last sentence, certainly, I agree with you it can
2 be read as, hey, here's a great device for down converting signals that can
3 also be adapted to do other things, including signal mixing and high
4 frequency signal amplification.

5 But I wonder if that sentence could also be read as sort of the
6 parameters of this down converting device are such -- are adjustable in such
7 a way that you can accomplish down conversion in a way that allows you to
8 optimize the mixing and amplification results within the down converting
9 function. And if that's a possible reading, then why is that reading wrong
10 and your reading right, I guess, is my question?

11 MR. MACDONALD: Yeah. I understand the question. When we
12 parse that last sentence, I don't think that it contemplates an embodiment in
13 which there is both down conversion and amplification. And the reason why
14 I think it's that's somewhat straightforward from the sentence is it uses the
15 term "as well as other applications." So it says Bonn can be used for a first
16 thing as well as a second thing. And so that's a disjointed presentation of
17 two options that are not overlapping. Did I understand the question
18 correctly?

19 JUDGE KAISER: Yeah. I think you did. Is there any other
20 evidence in the record that supports that reading or are we just sort of trying
21 to parse the language there?

22 MR. MACDONALD: So that is the place where Bonn tells us to
23 use its dual gate FET structure for a high frequency signal amplification.
24 And then in addition, Bonn is referring here to the tailoring of its dual gate
25 device. And it uses this term as well as describes the individually adjusted

1 -- it's kind of highlighted here on the screen -- features of that device.

2 And so as Dr. Bernstein pointed out -- I mean, the most normal
3 application of a transistor is signal amplification. This is something that
4 everybody knows a transistor would be used for. They have many purposes.
5 And so it's just this disclosure alone, as well as this detailed discussion of
6 how to make its device which is more detailed than the patent, that allows us
7 to know that, okay, a POSITA reading this would be able to very quickly
8 make a signal amplifier out of Bonn's transistor.

9 JUDGE KAISER: Okay.

10 MR. MACDONALD: Okay.

11 JUDGE KAISER: Thank you.

12 MR. MACDONALD: Yeah, thank you. Moving on to Ground 2.
13 So now, we'll get into Ground 2, which involves the combination of Bonn,
14 Ren, and Mishra. And so we're using the same modified version of Bonn's
15 circuit diagram to support this ground as well as the additional teachings of
16 Ren and Mishra to support modifying Bonn's gallium arsenide device into
17 the more superior gallium nitride device.

18 And so, as shown on Slide 46, the combination addresses each
19 limitation of Claim 1. We're relying on Ren because it teaches the superior
20 performance of gallium nitride technology. That superiority is not in
21 dispute. And we're relying on Mishra for disclosure of a field plate.

22 Now, Mishra is a gallium nitride device. And it teaches the
23 advantage of that and also gives a lot of disclosure on its field plates. Just
24 like with Ground 1, there's no separate attack about the field plate aspect of
25 Limitation 1C5. That combination aspect of it is not disputed.

1 So moving on to Slide 47. Infineon launches two main arguments.
2 The first is to repeat its points from Ground 1, which we've already
3 addressed, namely the argument that we should ignore the teaching. We
4 were just looking at that disclosure in column 11. And the second argument
5 Infineon launches is that Ren only discloses one gate. And so a POSITA
6 couldn't have made Bonn's dual-gate transistor out of GaN because Ren
7 doesn't have two gates.

8 But as we will see, a POSITA would absolutely have been
9 motivated to use GaN. GaN was, in 2006, known to have a lot of
10 advantages over gallium arsenide. So it's important to remember that Bonn
11 was published in 1996 at a time when gallium nitride devices were
12 uncommon. It was in its infancy. And so Bonn used the standard
13 technology of that time, which was gallium arsenide. By 2006, which is the
14 relevant date here, a POSITA would have known the advantage of GaN and
15 had a lot of success using references like Ren or Mishra, which are gallium
16 nitride references, that teach all the aspects of a gate -- all the aspects of a
17 gallium nitride transistor.

18 Moving to Slide 49. We see that Ren presents solutions to
19 problems that Bonn poses. So Bonn, shown here in column 11, again,
20 describes reducing power consumption. And it describes the high frequency
21 signal amplification embodiment. And Ren gives solutions to that. It tells
22 us that gallium nitride improves gate leakage, it improves the saturation
23 velocity, the breakdown voltage, and it's good for high frequency, high
24 temperature, high power applications.

25 And so a POSITA would have combined those teachings with

1 Bonn's teaching that each of its two transistors in its dual-gate structure
2 could be individually adjusted. That is the combination. Ren teaches a
3 simple way to make each of those two structures either enhancement mode
4 or depletion mode. And so if you recall when the '003 Patent says to make
5 an enhancement mode device, it never tells us how to do that, but Ren does.
6 Ren gives us a very simple way to do it, which is namely, to take this thin
7 dielectric layer under the gate.

8 And if you make it very thin, the gate will be in enhancement
9 mode. If you make it thicker, the gate will be in depletion mode. And so
10 that teaching is readily combinable with Bonn's teaching to individually
11 adjust the channel width, dopant concentration, the channel depth under each
12 of its two gates.

13 Now, moving to Slide 51. We see again, here's where Ren
14 describes part of its very simple approach. It says that the AlGaN,
15 aluminum gallium nitride layer, can have a thickness value of between 10
16 and 20 nanometers. And if it's above a certain value in that range, it will be
17 in depletion mode. If it's below a certain value in that range, it will be in
18 enhancement mode. So Ren provides all these details about those aspects of
19 its disclosure.

20 And this fits very naturally with Bonn's disclosure. So Bonn tells
21 us here in column 11, lines 12 to 22, that the devices which are depicted in
22 Figures 3, 7, and 8, including the one that we've been discussing today, can
23 be insulated gate FETs. So that's a structure which has a dielectric layer
24 under the gate, just like Ren. And so it was natural and obvious for a
25 POSITA to take Ren's teaching to individually adjust one gate and apply to

1 each of Bonn's individually adjustable gates to make them either
2 enhancement mode, which is Bonn's direct teaching, or depletion mode,
3 which is Bonn's direct teaching.

4 Now, Infineon will tell us today that somehow -- we didn't argue
5 this -- we don't respond to their argument that Ren doesn't have two gates,
6 but this is our response. The combination has always been Bonn's two gates,
7 which both can be adjusted, as Bonn describes with Ren's teaching, to make
8 one of them enhancement mode, following Bonn's teaching and Ren's
9 teaching. And one of them depletion mode, following the teachings of both
10 references.

11 Moving to Slide 52. We'll address Infineon's arguments. Well, I
12 guess this is just further evidence regarding the references and their
13 combinability. Bonn here on the left is showing the gate width, the dopant
14 concentration, the channel depth can be adjusted. Ren is describing specific
15 adjustments that achieve Bonn's configuration of enhancement mode,
16 depletion mode, cascode.

17 And so as we just discussed, both of these devices have the gate
18 dielectric layer beneath them, as shown on Slide 53. One of the arguments
19 that Infineon makes against this combination is to get -- present sort of a
20 vague discussion on the state of the art. And in both cases, the main
21 arguments that Infineon advances works against them.

22 So in the first case, Infineon alleges that the field of semiconductor
23 technology, "Retains a strong element of trial and error." And they say that
24 this makes the combination somehow not obvious. But it's completely the
25 opposite. A POSITA who is habituated to trial and error would have

1 absolutely taken Bonn's very detailed teachings with Ren's very detailed
2 teachings and figured out through trial and error how to make the
3 combination function as an integrated device.

4 And it's very important to note that the '003 Patent doesn't tell us
5 how to make its device. It just lists some materials, gives us the basic
6 outline, and says, go ahead and make it. And so a POSITA in possession of
7 Bonn's very detailed disclosure and Ren's very detailed disclosure would
8 absolutely have been able, through trial and error, to make the proposed
9 combination because it would have led to superior performance.

10 Now, the other thing Infineon mentions is a deposition statement
11 from the inventor of the '003 Patent, Mr. Thomas Herman. Now, Mr.
12 Herman was being deposed in the parallel ITC investigation. And the '003
13 Patent was dropped from that investigation. And Mr. Herman says in that
14 deposition that his employer, International Rectifier, who was the applicant
15 of the '003 Patent, deemed it a more difficult task to make an enhancement
16 mode device. But he never explains why.

17 He doesn't tell us was that business reasons, was it cost reasons,
18 was it logistical reasons, was it technical reasons? And so Infineon's
19 argument that it was too difficult to make enhancement mode actually runs
20 contrary to the oath that Mr. Herman signed when he filed his application
21 and said it was enabled because the level of detail in the '003 Patent is very,
22 very bare bones when it comes to enhancement mode. You won't find it in
23 those four and a half columns how to make a device. And in contrast, of
24 course, Bonn and Ren describe a lot of details about how to make their
25 devices.

1 So moving to Slide 55, we see that those two arguments which
2 Infineon has launched against this combination also both fail. So all the
3 modifications we've discussed for Ground 1 would have been obvious, and
4 the -- a POSITA would have used the gallium arsenide -- I'm sorry, the
5 gallium nitride technology in 2006 to improve Bonn's devices and would
6 have known how to do so.

7 And so with that, I think I will move to Ground 3. Okay. Looking
8 now on Slide 67, we see an overview of the Mishra Grounds. And so this
9 addresses all claims in the '003 patent, just like Ground 2. So the
10 combination of Mishra and Ren has just two main disputes. And so if the
11 Board agrees that Mishra discloses a dual-gate transistor in cascode
12 arrangement and if the Board agrees that would have been obvious that the
13 first stage would have been in enhancement mode, according to the
14 combination, then Mishra and Ren render obvious all claims.

15 It's important to note that the reading of Mishra, as shown here on
16 Slide 68 in the bottom right, where the source-connected field plate is a
17 second gate, it's identical to Infineon's allegations regarding infringement.
18 So this is their theory of what a second gate is. Now if we look on the left,
19 it's a TEM image from the complaint in the ITC investigation. And that flat
20 planar region, which is shaded in pink, is part of the field plate. And that
21 squiggly upper portion -- I can highlight it here on the screen, although I
22 don't know -- it doesn't show on the screen, the laser. That squiggly upper
23 portion, which overlaps the first transistor, which is Q1, is the field plate
24 under Infineon's read.

25 Looking at Mishra, we see the same arrangement. It's flipped left

1 to right because the source and drain are flipped from the TEM image versus
2 the figure in Mishra. Now we see that flat, pink planar portion, which is the
3 second gate, and its squiggly portion which overlaps the first gate, that
4 structure 66 highlighted in pink. And under Infineon's read that is a second
5 gate, and it has that merged region right there between those two gates.

6 And Mishra tells us over and over many details about its field
7 plates. It provides a lot of detail about how to connect its field plates in
8 various ways. And in paragraph 63, for example -- not shown here on this
9 slide -- it simply tells us that it can be connected to the source in many ways
10 because a POSITA would know how to do that. That's very similar to the
11 level of detail in the '003 Patent where it just says that the field plate is there,
12 without describing how it's wired or anything that Patent Owner now
13 contends would not have been obvious.

14 Now, paragraph 62 of Mishra is shown on this slide, and Mishra
15 here unambiguously says one alternative arrangement -- it's referring to its
16 amplifier arrangements -- comprises a single transistor with a dual-gate
17 structure. And so all one of skill would need to do to make this combination
18 obvious would be to take this teaching here and also Mishra's teaching to
19 make its field plate source connected and we have a dual-gate transistor
20 under Infineon's read. And we could plug it into this cascode circuit, which
21 is Figure 10, where there's a long description of the cascode circuit
22 -- beginning around paragraph 55 and ending around paragraph 63
23 -- including this disclosure to use dual gate and just combine those elements
24 to arrive at the claimed invention. It was straightforward and obvious.

25 Moving to Slide 69, we see here that the combination addresses all

1 limitations of Claim 1. Again, we're relying on Ren for its GaN teachings,
2 for its teachings to make enhancement mode with that very simple approach
3 versus depletion mode, and to rely on Mishra's cascode disclosure and its
4 dual gate disclosure.

5 Infineon launches two attacks against Ground 3. So the first is that
6 we should ignore paragraph 62. According to Infineon, that paragraph has
7 no effect. But that is not the law, obviousness does not allow us to ignore
8 this explicit teaching to make its devices from a single gate into a dual gate.
9 Moreover, Mishra provides all the mechanisms that one of skill would need
10 to do that under Infineon's theory, just wire that second field plate to source
11 and now you have a second gate.

12 Infineon's second argument is that a POSITA would not have
13 selected enhancement mode as a first stage. But of course, as we pointed
14 out, there are only two choices. The gate is either enhancement mode or
15 depletion mode, and this is fully consistent with Mishra's disclosure to use
16 low-control voltages, which would have included low positive control
17 voltages for its first gate. It was known to do cascodes in enhancement
18 mode first stage and depletion mode second stage. That's what Bonn
19 describes. That's what some of the other supporting background references
20 also describe.

21 Moving to Slide 71, we'll address the first argument that Mishra
22 does not disclose a dual-gate structure. But as we just said, the only
23 modification needed to make this structure of Figure 5 a dual gate, according
24 to Infineon, is to make that pink structure a gate by wiring it to source. And
25 Mishra tells us to do that. Mishra describes many details of its device, as

1 summarized here on Slide 72.

2 The Federal Circuit has long told us that prior art, which provides a
3 level of detail similar to the patent, was enabling. This is from a Motorola
4 decision in 1997. And so Mishra provides us with everything we would
5 need to know in order to simply wire that second gate -- a tiny, little change
6 -- to the source in order to make it a gate under Infineon's theory.

7 So here are some of the places -- shown on 73 -- where Mishra
8 tells us to do that. Mishra, in paragraph 63, speaking about all of its
9 embodiments, said field plates can be connected to the source contact in
10 many different ways. Paragraphs 40, 44, and 52 tell us to use conductive
11 vias to connect field plates. Paragraph 56, Mishra describes a second stage
12 field-plated transistor connected in common gates configuration.

13 And so common, of course, refers to ground. So this is a second
14 stage of a cascode which is directly wired to ground. And that's what we see
15 in the left on paragraph 73 is a source connected second stage, just like
16 Infineon alleges in the bottom left of Slide 73 would be the claim's second
17 gate.

18 Moving to Slide 74, we see the parties dispute whether Mishra's
19 first transistor is in enhancement mode. But we just wanted to point out this
20 is a very limited set of options, just two, every gate is either in enhancement
21 mode or in depletion mode. And that's something that we pointed out before
22 in the Patent Owner response on questioning from Infineon.

23 Here we have Figure 10 of Mishra, which just shows the basic
24 layout for a cascode. And so when Mishra tells us to make a cascode, a
25 person of skill would have understood that Q1, that's the first stage, could

1 have been -- would have been in enhancement mode in some embodiments.

2 Looking at Slide 75, we play out those two options among the two
3 stages and see that that creates four options for the cascode, enhancement
4 mode followed by depletion mode, which is the claimed arrangement, would
5 have been an obvious choice among these limited options. Mishra does
6 describe low-control voltages. It doesn't say they have to be negative.
7 There's never a reason that Patent Owner provides to exclude low positive
8 voltages when it tells you to use low-control voltages.

9 Moreover, Mishra talks about reduced power consumption. This is
10 a very common problem in transistor technology. So of course, a person of
11 skill would look to enhancement mode, well-known devices to solve that
12 problem. Enhancement mode devices are off at zero volts control. So
13 there's no current flowing through the channel at zero volts, it solves that
14 power consumption problem.

15 Secondly, it's well-known that enhancement modes are suitable for
16 high voltage, high frequency applications. So POSITA, among these -- all
17 these limited options, would have found the enhancement with choice
18 perfectly obvious and natural.

19 Moving to Slide 76, I just wanted to point out that the parties agree
20 that Mishra's second stage is in depletion mode. So that's not on the table.
21 So it's just this one gate where Infineon contends that it wouldn't be in
22 enhancement mode. But of course, that contradicts Mishra itself.

23 Looking at Slide 77, this is a quote from paragraph 60 of Mishra.
24 It tells us here Q1 can be biased at a low voltage. It doesn't say it has to be
25 negative. And then in parentheses, it gives us an example, negative 6 volts.

1 But this does not exclude other examples. There's no express disclaimer
2 here in the reference that tells us you would never use low positive voltage,
3 especially considering that Mishra talks about reduced power consumption
4 and those other benefits we just described.

5 A POSITA would understand that of course there is a second
6 option, instead of depletion mode you could use enhancement mode. And
7 Infineon never explains why that would be excluded. Is there any reason
8 you wouldn't use enhancement mode? Mishra doesn't tell us and neither
9 does Infineon.

10 Moving on to Slide 78, we see a quote from Ren which talks about
11 the benefits of gallium nitride technology. And in particular, it talks about
12 the benefits of enhancement mode in gallium nitride technology. It tells us
13 that, you know, GaN motivates enhancement mode Q1 to -- for its power
14 saving benefits and for reduced gate leakage.

15 Moving to Slide 79, we see that it's not in dispute that Mishra
16 discloses the second stage as depletion mode. So it would have been
17 obvious to just choose one of the two options, enhancement mode for its first
18 stage, especially in light of all the teachings we just discussed.

19 So on Slide 80, we see a summary of the main attacks that Infineon
20 launches against Ground 3. They want us to ignore paragraph 62 -- but
21 that's contrary to law -- and they want to tell us that a POSITA would never
22 use an enhancement mode first-stage transistor. But of course, the petition
23 provides a lot of reasons why that would have been obvious. It improves
24 safety, it improves performance at high frequency, it reduces power
25 consumption. And there are just two choices. It would have been obvious

1 to use enhancement mode.

2 And so before I turn it over to the Patent Owner, I wanted to
3 address some of the arguments that they are making that we hear today. So
4 I'm going to switch now to -- on my screen just some of the slides. So these
5 slides come from the Patent Owner's demonstratives. We're looking at the
6 cover slide now. And you'll hear from Infineon many times that there's all
7 these arguments and all this evidence that we didn't rebut. And we just want
8 to set the record straight that we absolutely rebut those arguments in
9 evidence.

10 On the next slide here, I'm looking at Slide 12 from Patent Owner's
11 demonstratives, here's one of the more egregious examples. It says here Dr.
12 Choi's testimony is uncontested. And this slide talks about Dr. Choi's very
13 complicated analysis of why the current carrying capacity of Bonn's dual-
14 gate structure would never be used for signal amplification. So just to be
15 clear, we absolutely do rebut that.

16 Here's our rebuttal shown on the screen now. This is Slide 31 from
17 the Petitioner's demonstratives, we're summarizing the points we just
18 discussed. Bonn's embodiment with smaller current carrying capacity onto
19 the first gate is just one option. And we've discussed that at length in the
20 reply. We rebutted Dr. Choi's testimony. The signal amplification
21 modifications and embodiments do not need to be the best option. They just
22 need to be a suitable one.

23 And here, Bonn has described many different ways of making its
24 current carrying capacity under the two different gates either smaller or
25 larger under one; or no difference at all, they could have the same current

1 carrying capacity, because those sections are fully optional.

2 On the next screen, I'm going to show you another of their more
3 egregious examples. So this is Slide 19 from Patent Owner's presentation.
4 Dr. Choi here is making the argument that Ren does not disclose a dual-gate
5 transistor, so it can't provide any evidence that a person of skill would have
6 combined it with Bonn. But we do respond to this point. We absolutely
7 address his argument because we tell Infineon that they got the combination
8 backwards.

9 So Bonn has the dual gate. Bonn has individually adjustable
10 transistors for both of its two gates. And a person of skill would have
11 applied Ren's teachings to each of those individually adjustable gates. That's
12 our response. We absolutely respond to their point. We have conceded
13 nothing here. This is Slide 50 from Petitioner's demonstratives.

14 Okay. Here's one last example. This is from Slide 23 of Patent
15 Owner's response. Again, they're telling us Dr. Choi's testimony is
16 uncontested. I just wanted to read Dr. Choi's testimony here. So in the top
17 right of Slide 23, we see Dr. Choi says "the disclosure of the ordinary,
18 known concept of a dual-gate structure."

19 And just as an aside, here he's admitting that dual-gate structures
20 are ordinary, they're conventional, they're well-known. But anyways, he
21 goes on to say this would not be enough to amount to a disclosure in the
22 eyes of a POSA of a dual-gate transistor of the type claimed by the '003
23 Patent.

24 And so, of course, we rebut this. We go on at great length to talk
25 about how Bonn's transistors and Mishra's transistors are described in great

1 detail. And so shown here on Slide 71 is our rebuttal. We talk about the
2 very simple change that would be required to make Mishra's device a dual-
3 gate transistor under their theory. That's in the reply at pages 18 to 23. All
4 we need to do is connect that pink structure to the source. That's our
5 rebuttal. And of course, Mishra describes this at a much higher level of
6 detail than the '003 Patent does. It doesn't tell us anything about how its
7 field plate is connected to source.

8 And so finally, I also wanted to point out that many of Patent
9 Owner's responses either mislead or mistake the things that we have said.
10 So I just wanted to set the record straight on a couple of points. So this is
11 the cover of Patent Owner's sur-reply. I'm going to move now to page 2 of
12 the sur-reply. It says here - I'm reading from the first full paragraph. I think
13 I can highlight this on my screen. The reply now pivots, arguing that quote,
14 "a dual-gate transistor" -- and then there's another, quote, "was never the
15 combination."

16 Okay. So I don't know where they're getting this from. We're
17 going to go to our reply. Because there is no pivoting here. Let's take a look
18 at what we actually said. So let's go to the reply here. So this is Petitioner's
19 reply to Patent Owner's response, that's Paper 15. I'm going to go to the part
20 they just quoted. Here is page 14. I'm looking at the bottom of page 14, it
21 says right here talking about Patent Owner. It -- Patent Owner instead
22 argues, quote, "Ren has no disclosure of how to make a dual gate GaN
23 transistor," citing the Patent Owner response at page 31 with emphasis added
24 -- emphasis original rather.

25 And here we say that was never the combination. And so there's

1 no pivoting here, right? We're just addressing their point. And if Patent
2 Owner read on, they would see that there's no pivoting because we explain
3 the combination that I've been talking about during today's presentation. So
4 here we say at the top of page 15, Bonn teaches individually adjusting the
5 properties of each gate, and a POSITA would have made those individual
6 gate adjustments using Ren's GaN techniques, petition -- said in the petition
7 50 to 54.

8 So that's always been the combination, Bonn's two gates with
9 Ren's teachings. We don't know where we're getting -- they're getting that
10 pivoting concept from. That's simply not our argument. That's not our
11 position. And that's not -- those quotes are pulled out of context and very
12 misleading.

13 Let's move now to one of Petitioner's -- Patent Owner's Slides. I'm
14 looking at Slide 39. I just want to be very careful with the quotes that Patent
15 Owner is using. So let's look at the second bullet. It says here, talking about
16 the connecting the second gate to ground, that the petition proposed using
17 the transistor for blah-blah-blah-blah 10 gigahertz, frequencies of "10
18 gigahertz." And that's in quotes, okay?

19 The petition made no such proposition. It never said anything
20 about 10 gigahertz. That's their argument. That's not our argument. So I
21 just want us to be very careful with their use of quotes, which is very
22 misleading in this particular bullet.

23 And finally, now moving to Slide 35, we see a quote at the bottom,
24 which Patent Owner seems to suggest Dr. Bernstein said. But he never said
25 anything like this. It says, quote, "I might have come up with a better

1 rationale had I bothered," end quote. And this is also very misleading. Dr.
2 Bernstein never said that. We just wanted to make sure that the record was
3 clear on this point.

4 And with that, we'll take questions, Your Honor.

5 JUDGE MURRAY: Counsel, this is Judge Murray. I want to
6 return to column 11 of Bonn -- to the paragraph that you discussed at some
7 length -- that ends with "as well as other applications such as high frequency
8 signal amplification." And my question is, what does this sentence mean
9 exactly? Is Bonn saying that down converters can be used for signal
10 amplification, or is it saying that Bonn encompasses circuits that are not
11 down converters?

12 MR. MACDONALD: So it begins with talking about the dual gate
13 FET structure, Your Honor. It says, therefore the dual gate FET structure of
14 the present invention can be tailored to provide superior performance over
15 the prior art dual gate FET structures. Okay. So that's the context. It's
16 addressing that structure, which is Figure 7, not the down converter which is
17 Figure 1. And it tells us that one of those applications is high frequency
18 signal amplification.

19 So as Dr. Bernstein said, this is the most normal way to use a
20 transistor as a signal amplifier. And an amplifier is not a down converter.
21 They're two different things. The down converter aspect is about the wiring.

22 JUDGE MURRAY: Thank you.

23 MR. MACDONALD: Yeah, thank you. Okay. If there are no
24 further questions, Your Honors, I can turn over the lectern. Thank you.

25 JUDGE KAISER: Okay. Thank you very much. So we'll hear

1 from Patent Owner next. And whenever you get a chance to get set up there,
2 please let us know how much time you'd like to reserve. And then I think
3 start when you're ready.

4 MR. BALICH: Thank you, Your Honors. I'd like to reserve 10
5 minutes for rebuttal. Again, my name is Jason Balich, representing Patent
6 Owner Infineon. Your Honor, Slide 2 shows a summary of why Petitioner's
7 three obviousness grounds all fail. As you heard from Petitioner, Grounds 1
8 and 2 are based on Bonn, which discloses a down converter that Petitioner
9 discarded to use as a parts list.

10 But Petitioner's declarant Dr. Bernstein was incompetent when it
11 came to Bonn's down converter, and he admitted it. Dr. Bernstein discarded
12 the parts he didn't understand and kept the parts that he knew would map to
13 the claims of the challenged patent. But just because Dr. Bernstein
14 understood the technology that he was trying to reconstruct doesn't mean he
15 can credibly say that a POSA would have used Bonn's down converter for
16 nothing more than a parts list.

17 Moreover, even if a POSA would have used Bonn's dual-gate
18 transistor as an amplifier, Mil'Shtein shows that a POSA would not have
19 connected the second gate to a constant voltage source as claimed. And
20 that's because Mil'Shtein taught that doing so yields the worst results.

21 Ground 3 fails for an easier reason. Petitioner relied on Mishra's
22 Figure 5 as disclosing a dual-gate transistor. But Petitioner conceded in its
23 reply brief that Figure 5 has only one gate, not two. And Dr. Bernstein
24 testified that Figure 5 has only one gate, not two. That alone is fatal to
25 Ground 3.

1 So let's look at these overlapping failures one by one. Slide 4
2 shows the limitation that even the institution decision acknowledged was
3 missing from Bonn, specifically, every challenged claim requires a second
4 gate of a dual-gate transistor that's connected to a constant voltage source.

5 Slide 5 shows Bonn's down converter. It's complicated, but Bonn
6 teaches how every part works. The whole point of the circuit is combining
7 two signals to form a single one from two different variable voltage sources.
8 The RF signal in blue is combined with the yellow signal in red to form the
9 combined purple signal. Notably, no gate of any transistor is connected to a
10 constant voltage source as the challenged claims require. Petitioner in its
11 presentation mentioned cascode and Bonn's disclosure of it several times.
12 But Bonn uses cascode simply to describe two transistors connected in
13 series, like in mixture -- in mixer 40.

14 Now, Petitioner argues that a POSA would have looked to make an
15 amplifier. But notably, the down converter already has an amplifier,
16 transistor 20. Petitioner removes it. But why? What was wrong with the
17 existing amplifier? And if a POSA wanted to use a dual-gate structure, why
18 not substitute it there? Petition does not say.

19 Slide 6 shows an overlay of Petitioner's modified circuit over
20 Bonn's original down converter. Petitioner viewed Bonn as a pile of parts
21 that Petitioner stripped away to map the challenged claims. We already
22 covered Bonn's amplifier 20. Why did Petitioner strip it away? What was
23 wrong with it? Why remove an amplifier when the stated goal of the
24 petition was amplification? Petition doesn't say.

25 Petitioner stripped away voltage source 80. Again, why? What

1 was wrong with the existing voltage source? Petitioner stripped away
2 capacitors, resistors, inductors, and the entire LO port in the circuit. But
3 where does Bonn say to do that? Petition doesn't say. Sure, Bonn tells us
4 the function of those parts, but Bonn never once suggests removing any of
5 them. The resulting circuit is not a modified down converter. It's an entirely
6 different circuit, one that renders Bonn's down converter inoperable.

7 Turning to Slide 7, Petitioner's Dr. Bernstein admitted that Bonn's
8 down converter was a very -- sort of a special application that was very
9 complicated. In other words, this was a circuit that Bonn took great care to
10 design. Dr. Bernstein found Bonn's down converter was so complicated that
11 he simply scrapped every component that he didn't understand. That's easy
12 to do when you know what the end goal is, using the challenged claims as a
13 roadmap.

14 As shown on Slide 8, Dr. Bernstein may have understood the
15 technology that he was looking to reconstruct, but he didn't understand how
16 Bonn's down converter worked. He admitted at his deposition, I generally
17 am not so familiar with down converters, and I have no experience making
18 down converters. And he admitted three times that he is not an RF circuit
19 expert. As Petitioner mentioned, Dr. Bernstein's expertise is in GaN
20 transistors. To him, everything looks like a GaN transistor, but he is not
21 familiar with circuits. In short, Dr. Bernstein didn't know what he was
22 talking about regarding Bonn's down converter, and he admitted it.

23 Skipping ahead to Slide 10, while Dr. Bernstein didn't understand
24 how Bonn worked, Patent Owner's declarant did. Dr. Choi testified that a
25 POSA would not have modified Bonn's down converter as the petition

1 proposed. Petitioner didn't depose Dr. Choi, didn't challenge his
2 qualifications, and didn't challenge his testimony in any way. Dr. Choi's
3 testimony is thus the only competent evidence on the issue that a POSA
4 would not have scrapped Bonn's down converter. That should be dispositive
5 of the failure of Grounds 1 and 2, which are both based on these
6 Frankenstein modifications to Bonn.

7 I'd like to touch briefly on Petitioner's Slide 14. So I'm jumping
8 from Patent Owner slides to Petitioner's Slides. And on Petitioner Slide 14,
9 at the bottom, Petitioner argues that Bonn supports every change to Figure 1
10 because it explains the role of all of the components of Figure 1. But that's
11 nonsense. Any patent with a circuit will explain how it works.

12 Never once does Bonn suggest removing any of those components
13 that Bonn painstakingly put together to make, according to Dr. Bernstein,
14 this very special down converter. Petitioner argues that Bonn's suggestion to
15 tailor its transistor to scrap down converter is provided in column 11. But
16 that's not what Bonn teaches, and Your Honors picked up on that.

17 So I'm going to switch back to Patent Owner's slide deck. I'm
18 going to go to Patent Owner's Slide 31. So if you look at Patent Owner's
19 Slide 31, you can see that Bonn teaches the dual gate FET structure of the
20 present invention can be tailored. Dr. Choi took a look at this, and he
21 testified that a POSA reading this would understand that this means that
22 Bonn is inviting tailoring the transistor. Bonn never teaches tailoring or
23 scrapping the down converter. As Dr. Choi testified, a POSA would not
24 have looked to destroy Bonn's down converter based on the teaching that the
25 transistor can be tailored.

1 So now, turning back to Slide 11, Petitioner spent considerable
2 time arguing about the flexibility of Bonn's disclosure. But notably, none of
3 that's in the petition. Page 22 of the petition states a POSITA would have
4 found it obvious to modify the circuit of Figure 1 and use Figure 7's
5 structure for the transistor. I'm paraphrasing a little bit. But as you can see,
6 petition never suggests any modification to Figure 7's structure. This is
7 going to be a theme because Petitioner makes a number of arguments now in
8 its presentation for the first time that Your Honors will see was not in the
9 petition.

10 Turning to Slide 12, even if you agree with Petitioner that a POSA
11 would have used Bonn's down converter as a bag of parts and reassembled it
12 into an amplifier, Petitioner still provides no reason why a POSA would
13 have picked Bonn's Figure 7 transistor structure when the evidence is that it
14 would have been unsuitable as an amplifier. You see a mixer combines two
15 signals. And because of that, there's a risk of current saturation at the second
16 gate.

17 Bonn also recognized this and intentionally added nonconductive
18 sections to Figure 7's structure, resulting in unequal current carrying
19 capacities to prevent current saturation at that second gate. But an amplifier
20 boosts just one signal, not two. There is no risk of current saturation at the
21 second gate. But as Dr. Choi testified, that same feature that made Figure 7
22 work so well as a mixer made it unsuitable as an amplifier. He testified that
23 a POSA would have used -- would not have used Bonn's Figure 7 structure
24 as an amplifier. And in this regard, Dr. Choi's testimony is uncontested.

25 Petitioner, in their presentation, kept on saying this is our response.

1 But it's too late. As Your Honor saw, the petition never made any
2 modification to Bonn's Figure 7 structure, so trying to make modifications
3 now at the oral argument is just too late. Petitioner also argued that the
4 nonconductive sections in Figure 7's transistor were not there. It was a
5 figment of their imagination. That's not what Dr. Choi testified. Bonn states
6 on column 9, lines 12 through 20, that the same nonconductive sections that
7 Bonn describes throughout its specification also applies to Figure 7.

8 Turning to Slide 13, I'd like to touch on Mil'Shtein. Mil'Shtein is
9 not on the ground, its Patent Owner's evidence. But nonetheless, Petitioner
10 knew of Mil'Shtein because Dr. Bernstein testified that he reviewed it as part
11 of his background research. Mil'Shtein shows that even if a POSA were to
12 use Bonn's Figure 7 transistor as an amplifier, a POSA would not have
13 connected the second gate to a constant voltage source as claimed.

14 Now remember, this is the limitation that even the institution
15 decision acknowledged Bonn does not disclose. Mil'Shtein compared the
16 performance of a dual-gate transistor under three different vias conditions in
17 comparison to a single-gate transistor used as a control. The single-gate
18 transistor had a unity current gain of 16 gigahertz. And as even Dr.
19 Bernstein admitted, higher is better.

20 Mil'Shtein then tested a dual-gate transistor with three different
21 vias conditions and found that when the second gate was connected to a
22 constant voltage source, that yielded the worst results. Even the reply at
23 page 8 concedes that Mil'Shtein -- and I quote -- "expresses a preference for
24 the other three approaches." So this is not a case where POSA had several
25 equal options, but one where the prior art expressed a preference for the

1 configuration different than the one Petitioner proposed. It was therefore
2 incumbent on the petition to explain why a POSA would not have picked the
3 better options in favor of the one that yielded the worst results. Petition
4 doesn't do this.

5 Slide 14 summarizes a ground of why both -- summarizes why
6 both Grounds 1 and 2 fail. And unless Your Honors have any questions
7 about Grounds 1 and 2, I'll move to Ground 3.

8 Turning to Slide 21 of Patent Owner's slide deck, deciding Ground
9 3 should be straightforward. The petition's primary basis for its contention
10 that Mishra disclosed a merged transistor was its argument that Figure 5 has
11 a second gate in the form of field plate 66. You can see this in the petition at
12 pages 83 and the paragraph spanning pages 86 and 87. Petitioner's entire
13 presentation that we just heard right now was predicated on Figure 5 having
14 two gates.

15 But Petitioner conceded in its reply brief that Figure 5 depicts a
16 single-transistor amplifier with one gate. That's dispositive of Ground 3.
17 The petition built its entire argument of Figure 5 being a dual-gate structure.
18 And with that foundation gone, there's nothing left.

19 Now, Petitioner seems to argue in its presentation that Infineon
20 -- something about Infineon's theory, Infineon's infringement contentions.
21 But the director made it very clear in the precedential decision, Revo
22 Technologies, that Petitioners can't simply adopt a Patent Owner's District
23 Court constructions at the PTAB without some explanation. Here, the
24 petition said that every single claimed term should be construed by its plain
25 meaning. I have no idea what Petitioner means by Infineon's theory of the

1 case and how that applies to Mishra. And I don't understand that because
2 the petition never explained it.

3 As shown on Slide 22, all of the challenged claims require that the
4 drain of the enhancement mode transistor shown in green be merged with
5 the source of the depletion mode transistor shown in pink. You can see this
6 in Figure 3 of the challenged patent, the drain of Q1 is merged with the
7 source of Q2 at the node identified by the arrow 39.

8 Turning to Slide 23, Mishra does have a reference to a dual-gate
9 structure. But as Dr. Choi explained, the disclosure of the ordinary, known
10 concept of a dual-gate structure would not have amounted to the disclosure
11 in the eyes of a POSA of a dual-gate transistor of the type claimed by the
12 '003 Patent. And that's because, as you can see on Slide 23, not all dual-gate
13 transistors have merged sources and drains.

14 For example, one of Petitioner's own references, Sankin, which is
15 Exhibit 1018, discloses a dual-gate transistor. But the drain on Sankin's first
16 transistor in green is connected to the source of Sankin's second transistor in
17 pink by wires. They're not merged. That's why Mishra's one-sentence
18 disclosure of a dual-gate structure doesn't disclose to a POSA the specific
19 structure of a merged transistor is claimed. Now, notably, this is the very
20 limitation that the examiner found lacking from the prior art during the
21 original prosecution. Mishra doesn't disclose the limitation either.

22 Shown on Slide 24, Mishra's Figure 10 shows two ordinary, single-
23 gate transistors electrically connected by wires. This is confirmed by the
24 Horowitz and Hill textbook, which is Exhibit 2002, which shows that the
25 standard circuit symbol for a dual-gate transistor has two gates belonging to

1 the same device, a symbol Mishra never uses. Instead, Mishra shows two
2 separate single-gate devices connected externally. Dr. Choi testified that a
3 POSA would have known Mishra's transistors are separate, ordinary single-
4 gate transistors as opposed to a dual-gate transistor. And again, Dr. Choi's
5 testimony is uncontested.

6 Turning to Slide 25, even Petitioner's own declarant, Dr. Bernstein,
7 admits that Figure 5 only has one gate, not two, as the petition alleged. I
8 asked Dr. Bernstein if Mishra's unmodified Figure 5 was of a dual-gate
9 structure. And he admitted that reference number 66 was a field plate and
10 that a field plate is not a gate. Literally, he says, Mishra -- he's, Mishra -- is
11 not telling us that the field plate is not a gate. This admission is fail -- is
12 fatal to Ground 3, which relies on Figure 5 as disclosing a dual-gate
13 structure, which according to Petitioner's own declarant, it does not.

14 Now I'd like to address a few of Petitioner's slides. So if you could
15 turn to Petitioner's Slide 67. So on Petitioner's Slide 67, there Petitioner
16 argues that to find the claims invalid over Ground 3, the Board need only
17 agree that Mishra discloses a dual-gate transistor. But that's wrong. As
18 we've been discussing, the Board would also need to find that Mishra
19 discloses a merged dual-gate transistor, not just any old dual-gate transistor.
20 And that Figure 5 is an example of one because that's the embodiment that
21 the petition relies on. Remember, the dual-gate transistor is the key
22 limitation that the examiner found missing from the prior art during the
23 original prosecution.

24 Next, I'd like to address Slide 70 -- Petitioner's Slide 71. In
25 Petitioner's Slide 71, Petitioner argues that Mishra teaches connecting its

1 field plate to the source. But you can see that's plainly wrong based on this
2 slide. In Petitioner's own highlighted portion in paragraph 44, Mishra tells
3 us that the field plate 66 is connected to the gate, not the source. This
4 reinforces that Figure 5 is of a single transistor with one gate, just as
5 Petitioner's reply brief concedes.

6 On Petitioner's Slide 73, Petitioner argues that Mishra discloses
7 that field plates can be connected to the source contact. But as we just saw
8 in the last slide, field plate 66 and Figure 5 is connected to the gate 62, not
9 the source. The petition never argues that a POSA would have modified
10 Figure 5 to disconnect the field plate from the gate and then to reconnect it
11 from -- to the source.

12 The argument is entirely missing from the petition, and therefore
13 improper to be making now. Moreover, that a field plate can be connected
14 to the source is not the standard for obviousness. Petition would have
15 needed to provide some reason, but it didn't because it never made the
16 argument in the first place. And indeed, Dr. Bernstein admitted that Mishra
17 is not telling us that the field plate is also a gate. That's at his deposition
18 transcript, Exhibit 2009, page 150, at lines 16 through 20.

19 Finally, I'd like to go back to Petitioner's Slide 72. Petitioner
20 argues that Mishra discloses more detail than the '003 Patent. But the degree
21 of detail that Mishra discloses is simply not relevant. Because as we have
22 just seen, Mishra only discloses a single gate, not a merged dual-gate
23 transistor. That's the disclosure that the '003 Patent has but that Mishra
24 lacks.

25 I'm going to go back to Patent Owner's slide deck right now. And

1 I'm going to go to Patent Owner's Slide 47. On Patent Owner's Slide 47,
2 Petitioners spent a lot of time arguing that it would have been obvious to
3 select an enhancement mode gate followed by a depletion mode gate. But
4 while that is a great argument that there's only two choices, that argument is
5 unsupported.

6 As Dr. Choi explained, Mishra discloses that the Q2 transistor is a
7 depletion mode transistor; Petitioner agrees. Because the transistor symbols
8 are the same for both transistors in Figure 10, Dr. Choi explained that a
9 POSA would have understood Q1 and Q2 to be the same type of transistors,
10 both depletion mode. The petition argues that the enhancement mode for Q1
11 would have been obvious because Mishra uses low positive voltages.

12 And the petition cites Mishra at paragraph 60. But that paragraph
13 discloses Mishra using negative voltages, not positive voltages. The reply
14 had no answer. Petitioner's presentation just now tries to flip the script and
15 says that Mishra does not exclude positive voltages. But again, Petitioner
16 never made that argument in the petition. And it's too late to be making that
17 argument now.

18 Petition cites Bonn, Sankin, and Salato to show using an
19 enhancement mode transistor as the first transistor was known. But just
20 because something is known, it is legally insufficient for it to be obvious.
21 And while the petition alleges that each reference discloses a set of benefits
22 for their own application, Petitioner fails to make that connection that those
23 benefits for those other applications would have been transferable to
24 Mishra's different application.

25 You see, Mishra discloses that its circuit 10 -- Figure 10 is used for

1 signal amplification. But Bonn discloses using it as a mixer. Sankin and
2 Salato both disclose using it for power supply systems. And Ren, mentioned
3 for the first time in a reply, discloses an inverter system. But an amplifier,
4 mixer, an inverter system, and power supply all perform fundamentally
5 different functions. As Dr. Choi testified, a POSA would not have had any
6 reason to have applied those other references' teachings to Mishra's
7 amplifier. And again, Dr. Choi's testimony is uncontested.

8 Your Honors, do you have any questions for me on Ground 3?
9 Otherwise, I want to touch briefly on reasonable expectations of success.

10 So if we turn to Patent Owner's Slide 16, the reason Petitioner
11 needed to establish a reasonable expectation of success -- of course, beyond
12 the fact that it's required in order to make that a prima facie case of
13 obviousness -- is because of as of 2006 GaN was still a new technology. Dr.
14 Bernstein admitted that GaN devices were in early development and
15 uncommon in the '90s. And Thomas Herman, the inventor of the patent
16 itself, the '003 Patent, explained that designing enhancement mode GaN
17 transistors was of interest but not done because it was deemed more difficult.

18 Finally, Intel's Copy Exactly philosophy demonstrates how
19 unpredictable semiconductor processing was and still is. The Copy Exactly
20 philosophy recognized that POSAs did not have a complete understanding of
21 the semiconductor processing and that it was inherently unpredictable.
22 That's not to say that it couldn't be done. Once you figure out what it was,
23 you copy exactly and you can do it again.

24 But as Dr. Choi testified, if silicone conductor -- semiconductor
25 manufacturing was so inherently unpredictable, it would have been an even

1 more profound switch to switch from Bonn's transistor technology to GaN,
2 and a POSA would not have expected it to be successful.

3 Turning to Slide 17, this shows the sum total of the petition's
4 argument on predictability for Ground 2. Petition argues that making Bonn's
5 transistor from GaN would have predictably led to a cascode transistor made
6 out of GaN. But that skips over the fundamental step as to whether making
7 Bonn's transistor from GaN in the first place a POSA would have had a
8 reasonable expectation of success. Petitioner cites no prior art evidence in
9 support of this.

10 Petitioner cites Dr. Bernstein's paragraph 165, but he has the
11 identical conclusory remark and cites nothing in support. It was Petitioner's
12 burden to establish a reasonable expectation of success. And the single
13 conclusory sentence is unsupported by any prior art evidence and it's
14 therefore insufficient. Making a silicon transistor was so unpredictable with
15 decades of experience, making a GaN transistor was even more so.

16 And again, this was one of many times when Petitioner remarked
17 -- this is our response to this slide. But this presentation, this oral argument,
18 is the first time we're hearing of their response. It's not in the briefs. It's too
19 late now.

20 Turning to Slide 18, as a reminder, the claims require the drain
21 region of enhancement mode transistor in green to be merged with the
22 source region of a depletion mode transistor in purple. But again, not all
23 dual-gate transistors are merged to dual-gate transistors.

24 Slide 19 shows the sum total of Ground 3's argument regarding
25 predictability. As you can see, Ground 3 lacks any evidence of a reasonable

1 expectation of success in turning Mishra's single-gate transistor into a dual
2 gate, merged transistor made from GaN. Petition argues it would have been
3 predictable to use Ren's known option, but that refers to Ren's teaching of
4 how to make either a single gate enhancement mode or a single gate
5 depletion mode transistor.

6 Predictability, changing the mode of a single gate transistor is
7 entirely different from whether a POSA would have had a reasonable
8 expectation of success in making a merged dual-gate transistor from GaN.
9 Petitioner never alleged predictability in making specifically a merged dual-
10 gate transistor from GaN, and it needed to have done so in order to satisfy its
11 prima facie obviousness case.

12 Once again, Petitioner seems to think that the oral argument is a
13 time to respond to these comments, but the time has passed. If you search
14 the petition for expectation of success and you search its reply brief, you're
15 not going to find it.

16 I'll just end with the Petitioner made a number of allegations about
17 somehow Infineon was being misleading, one of them being how Dr. Choi's
18 testimony was uncontested. And that's true, Petitioner did not depose Dr.
19 Choi. If you look in Petitioner's reply brief, Petitioner never mentions Dr.
20 Choi, never mentions his qualifications, never disputes his testimony in any
21 way. And so it's very much accurate to say that his testimony is
22 uncontested.

23 The last one I'll touch upon is in Patent Owner's Slide 35. There's
24 a quote at the bottom. "I might have come up with a better rationale had I
25 bothered." That is in Petitioner's sur-reply, pages 6 to 7. Patent Owner

1 never implied that Dr. Bernstein had that quote.

2 So Your Honors, turning to Slide 27 in sum, all of Petitioner's
3 three grounds fail for multiple overlapping reasons. The Board should
4 confirm all challenged claims as being patentable. If you don't have any
5 questions, I'll reserve the rest of my time for surrebuttal.

6 JUDGE KAISER: Can I ask you a question on Ground 1?

7 MR. BALICH: Sure.

8 JUDGE KAISER: So I asked a similar question, I guess, to
9 Petitioner's counsel, the language that's there and sort of the -- at the end of
10 claim 11 -- or end of column 11 before it goes on to the claims in Bonn.
11 Petitioner has suggested that that last sentence or maybe the whole
12 paragraph should be read in a way to suggest that Bonn is saying, you know,
13 hey, I know I've disclosed a down converter, that down converter can work
14 for other reasons as well or for other applications as well, which I guess is
15 actually the language that Bonn uses. And among those is amplification.
16 And so that's an invitation to go do lots of things to Bonn to make Bonn a
17 new and better amplifier.

18 I know you disagree with that. And you've said -- I think if we
19 bring your presentation today, at best that's an invitation to play around with
20 how the merged dual-transistor structure is put together rather than the entire
21 circuit. But can you point to, you know, what evidence there is to suggest
22 that Petitioner's reading is wrong or yours is right or both? That would be
23 helpful.

24 MR. BALICH: Sure. I'll point to two things. The first is literally
25 the words of Bonn in that -- that sentence says the dual gate FET structure of

1 the present invention can be tailored and that tailoring can be used as a high
2 frequency signal amplification. So Bonn is very clear that this sentence is
3 about the dual gate FET structure.

4 The second piece of evidence that I can point to is Dr. Choi's
5 testimony about how a POSA would have read this paragraph in Bonn and
6 would have read it in the same way that I described. And so this is not me
7 speaking as an attorney, as attorney argument. This is me conveying to you
8 what a POSA -- how a POSA would have understood that through the eyes
9 of Dr. Choi.

10 And certainly, you know, we don't dispute that a dual-gate FET
11 could have been used for amplification. But for the reasons we provided by
12 Dr. Choi, the Figure 7 structure specifically was unsuitable for that
13 application. And of course, there is no mention of modifying it in the
14 petition itself.

15 JUDGE KAISER: Okay. I understand. Thank you.

16 MR. BALICH: Do Your Honors have any other questions?

17 JUDGE MURRAY: Yes. Counsel, is Dr. Choi's testimony
18 uncontested or is it unrebutted? Uncontested suggests that the parties are in
19 agreement, whereas unrebutted suggests that you believe that the counter
20 argument was not persuasive.

21 MR. BALICH: Your Honor, so the facts, however you wish you
22 wanted to find the word uncontested, was Petitioner had the opportunity to
23 depose Dr. Choi. They chose not to take it. And they failed to explain why
24 his testimony was somehow incorrect in their reply brief. So I'm not
25 suggesting that they have signed up and agreed with Dr. Choi, but they have

1 not explained why, to the extent that they disagree why they would disagree.

2 JUDGE MURRAY: Okay. Thank you.

3 MR. BALICH: Any other questions? Well, then I'll reserve the
4 rest of my time for surrebuttal. Thanks.

5 MR. MACDONALD: Thank you, Your Honors.

6 JUDGE KAISER: Okay. Thank you. Yeah, we'll hear from
7 Petitioner's counsel.

8 MR. MACDONALD: Okay. Let me get my AV set up, please.
9 Okay. So thank you, Your Honors. I just wanted to make a couple of quick
10 points. You know, as we sort of predicted, Patent Owner has a few points
11 where they're arguing a gotcha. You know, Dr. Choi's testimony is
12 uncontested, however we want to define it. But I just want to be clear that,
13 you know, under the rules 37 CFR 42.65, the Board is not required to credit
14 expert testimony just because they're not subject to cross examination. I
15 think that we're on the same page here as far as that goes.

16 So in terms of the discussion on Bonn that Patent Owner just
17 presented, Patent Owner's counsel admitted -- I'm quoting him -- "Sure,
18 Bonn tells us the function of those parts." So in other words, Bonn tells us
19 what all those parts do. So that's not contested. And Bonn tells us to use the
20 dual-gate transistor as a signal amplifier. They ask, but why? It's because
21 Bonn tells us to do that.

22 When you do that, Bonn also tells us, as shown here on my screen
23 on Slide 14, that the amplifier can be used and would be used, where we've
24 shaded it in Figure 1. So that's kind of the starting point of Bonn is I have a
25 dual gate, I'm putting it in that place, and I'm going to tell you to use it for a

1 single amplification. And because Bonn tells us what all of these parts do, a
2 POSITA would have made these very simple modifications to arrive at a
3 standard amplifier.

4 So Dr. Bernstein testified about this at length. And Dr. Choi has
5 never said that the modified figure on the right is not an amplifier or it's
6 something that a POSITA would not have understood. Everybody knows
7 that that is an amplifier. And in fact, it's also the standard cascode wiring.
8 That's the wiring in the '003 Patent, the cascode common source, common
9 gate. It's also the wiring in Mishra's cascode of Figure 10, common source,
10 common gate. So Bonn says use a cascode. Bonn says use it for signal
11 amplification. It's all very straightforward from there.

12 Let's move now to the discussion involving Mishra's field plate.
13 So right here in the petition, we say the motivation and combination that
14 we're talking about for Mishra and Ren. This is Ground 3. And the petition
15 says very straightforwardly that when implemented in cascode -- I'm reading
16 in the bottom paragraph -- field plate 66 is coupled to ground. So in other
17 words, it's Mishra's teaching to use a dual gate device in cascode.

18 Let's look at Mishra. Okay. So here's Mishra in Figure 10, I'm
19 showing that on my screen. And of course, this is the standard cascode
20 wiring with, you know, the ground connected both to the gate, Q2, and to the
21 source. So when Mishra says, hey, let's wire this up in cascode, that's what
22 it's talking about. I'm going to flip to - just so we see this in context today
23 -- paragraph 62 and 63, Mishra is giving us alternative embodiments. It says
24 one alternative comprises a single transistor with a dual-gate structure.

25 I mean, there's nothing else it can mean other than when, say,

1 Figure 10, which has two separate transistors, could be implemented as one.
2 That's exactly what it's talking about. If you look at this entire page, starting
3 back on the previous page with paragraph 55, all this describes that cascode
4 arrangement. And it concludes by saying, you could do this with two gates.
5 So it's pretty straightforward just from that.

6 Moreover, when the petition talked about wiring the second gate to
7 ground, just like Mishra teaches with the source, Patent Owner came back
8 on response and said, oh, but you don't explain how to do that. And of
9 course, you know, the patent doesn't either. It just says, wire it to ground.
10 And then we pointed out all of the places where Mishra says that. One of
11 them is right here on this screen. That's paragraph 63.

12 And it describes all the different shapes of the field plates. And it
13 says, preferred configuration the field plate can use in many different shapes
14 and can be connected to the source contact in many different ways. I mean,
15 that's all the disclosure a POSITA needs to make that simple change.

16 So the question before Your Honors regarding the Mishra
17 reference is whether or not when you connect Mishra's dual-gate cascode
18 -- which I'll put on the screen in just a moment. This is Bonn. Okay. Here's
19 an example. So I'm looking at Slide 68. The question for Your Honors is, is
20 a source-connected field plate a gate? Infineon says it is. If it's not, then
21 Your Honors should clarify that point. But under their theory that that little
22 planar portion is capacitively coupled to the semiconductor, it's right there in
23 that image.

24 I don't know why Counsel is pretending to be confused on this
25 point. This is an image from their complaint. It's right there in the public.

1 And you see that pink structure, it's a field plate. It's connected to source,
2 and they allege that's a gate. So if that's true, then Mishra discloses that
3 second gate. There's no confusion there. That they do have that same
4 structure. And we just saw in paragraph 63, Mishra tells us to do that.

5 And so finally, I think I just wanted to conclude with some of
6 Patent Owner's comments about the expectation of success. Obviousness
7 doesn't require a use of a magic phrase. We have explained in great detail
8 all of these different embodiments and why a POSITA would do it and how
9 the references support those changes.

10 You know, whether we use the magic word or not, all that
11 combination is explained, and a POSITA would have enjoyed success for all
12 the reasons that we provided in the petition and in response to their
13 arguments. And so with that, we rest, except for further questions, Your
14 Honor. I can see the clock is running out.

15 JUDGE MURRAY: No questions from me.

16 JUDGE KAISER: I have no questions either. Thank you very
17 much.

18 MR. MACDONALD: Thank you.

19 MR. BALICH: Your Honors, I just want to address a few points.
20 I've got Patent Owner's Slide 5 up on the screen. And the first point I want
21 to make is that Petitioner chose to start with Bonn's down converter. We
22 didn't somehow force them to pick such a complex and highly specialized
23 circuit. Remember, the claims of the '003 Patent do claim a circuit. They
24 also claim a particular type of transistor in the circuit, but they claim a
25 circuit. And this was the circuit that Petitioner chose, and they saw a parts

1 list. And they decided to destroy it and make it inoperable for its intended
2 purpose. As Dr. Choi explained, no POSA would have done that.

3 Petitioner also said that Bonn clearly says that even if a POSA
4 were to use a dual-gate transistor as an amplifier, they would stick it where
5 the mixer is. That's not in Bonn. Petitioner's counsel just made that up right
6 now. If anything, they would have put it where the existing amplifier was.
7 At the very least, it was Petitioner's obligation to explain why a POSA
8 would not have put it where the existing amplifier is. So Your Honors,
9 simply put, column 11's invitation to modify the transistor is no invitation to
10 destroy the down converter, which was a very special application.

11 The other thing that I want to touch upon is this repeated notion
12 that Mishra Figure 5 discloses a dual-gate transistor; it doesn't. Petitioner
13 concedes it in its reply brief that Figure 5 depicts a single transistor with one
14 gate. Petitioner is declaring Dr. Bernstein admitted in his deposition that
15 Figure 5 was a single transistor with one gate.

16 And when you look in the petition, Petitioner never proposes
17 modifying Figure 5 to disconnect the field plate from the gate, which is what
18 Mishra tells us in paragraph 44, and reconnect it to the source. That is
19 entirely missing from the petition. It is new argument made right now and is
20 why Ground 3 fails. Your Honors, do you have any questions?

21 JUDGE KAISER: I don't have any questions. Thank you.

22 JUDGE MURRAY: None from me. Thanks.

23 MR. BALICH: Thank you very much.

24 JUDGE KAISER: Okay. Thank you to both of the counsel who
25 argued today. And I hope you will express my -- and I think the -- and I

1 think I speak for the entire panel in fact -- express our admiration for the
2 way your teams have argued this case, both in writing and today at the
3 hearing, all those folks who helped you prepare for this, put together and
4 filed your papers and exhibits, and your support staff. This has been
5 extremely helpful, and the panel really appreciates everyone's efforts. So I
6 think with that, the case is submitted.

7 (Whereupon, the above-entitled matter went off the record at 2:44
8 p.m.)

PETITIONER:

Lionel Lavenue
Kara Specht
Cory Bell
Umber Aggarwal
Deanna Smiley
Shannon Yi
Luke MacDonald
Carlos Duarte-Guevara
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, LLP
lionel.lavenue@finnegan.com
kara.specht@finnegan.com
cory.bell@finnegan.com
umber.aggarwal@finnegan.com
deanna.smiley@finnegan.com
shannon.yi@finnegan.com
luke.macdonald@finnegan.com
carlos.duarte-guevara@finnegan.com

PATENT OWNER:

Scott McKeown
Jason Balich
WOLF GREENFIELD & SACKS, P.C.
smckeown-ptab@wolfgreenfield.com
jbalich-ptab@wolfgreenfield.com