

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AMERICAS CORP.,
Patent Owner.

IPR2025-00094
Patent 8,264,003 B2

Before JO-ANNE M. KOKOSKI, CHRISTOPHER M. KAISER, and
LISA A. MURRAY, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Innoscence America, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–16 (“the challenged claims”) of U.S. Patent No. 8,264,003 B2 (Ex. 1001, “the ’003 patent”). Infineon Technologies Americas Corp. (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”). Patent Owner did not “file a brief requesting discretionary denial of institution,” so the case was referred to us “to consider the merits and non-discretionary considerations.” Paper 8, 1–2.

On July 9, 2025, we instituted *inter partes* review of the challenged claims on all grounds set forth in the Petition. Paper 9 (“Inst. Dec.”). Patent Owner filed a Response (Paper 14, “PO Resp.”), Petitioner filed a Reply (Paper 15), and Patent Owner filed a Sur-reply (Paper 16). At the request of both parties, we held an oral hearing, the transcript of which has been entered into the record. Paper 22 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the challenged claims of the ’003 patent. For the reasons discussed below, we determine Petitioner has not established by a preponderance of the evidence that any of the challenged claims are unpatentable.

B. Real Parties-in-Interest

Petitioner identifies itself, Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience (Suzhou) Technology Holding Company, Ltd. as real parties-in-interest. Pet. 116. Patent Owner identifies itself as the real party-in-interest. Paper 4, 1.

C. Related Matters

The parties identify the following related proceedings: *Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al.*, Case No. 4:24-cv-01553 (N.D. Cal.), and *In re Certain Semiconductor Devices and Products Containing the Same*, Inv. No. 337-TA-1414 (USITC). Pet. 116; Paper 4, 1.

D. The '003 Patent

The '003 patent, titled “Merged Cascode Transistor,” is directed to “[a] merged gate transistor” with two gates, each “capacitively coupled to the semiconductor element,” where “conduction of the first portion [of the transistor] is based on a value of the input voltage signal” supplied to the first gate, “and the second gate is connected to a predetermined constant voltage.” Ex. 1001, codes (54), (57). The application giving rise to the '003 patent was filed on March 20, 2007, and it claims priority to a provisional application filed on March 20, 2006. *Id.* at codes (21), (22), (60).

The '003 patent describes prior-art cascodes using separate field-effect transistors as suffering from “[l]arge drain-source voltage (V_{ds}) swings during switching [that] create a large ‘Miller effect’ and as a result, excessive switching losses.” *Id.* at 1:36–38, Fig. 1. “In addition, high dV/dt changes at the drain (D) may result in a voltage transient V_{G1} at the gate (G),” which “may turn the transistor 1 ON briefly when not desired.” *Id.* at 1:39–44. “This unwanted period of conduction may result in rather large power and efficiency losses.” *Id.* at 1:44–45.

The '003 patent describes solving these problems by using a “single device and not two separate FETs.” *Id.* at 2:52–53, Fig. 2. According to the '003 patent, this causes “the ‘Miller effect’ [to be] greatly reduced,” causing

“power losses [to be] substantially reduced.” *Id.* at 3:31. Under this approach, “[t]he dV/dt at the drain (D1) of the bottom portion Q1 is also reduced,” and “will result in lower overall power losses and higher efficiency.” *Id.* at 3:31–50.

E. Illustrative Claim

Petitioner challenges claims 1–16 of the ’003 patent. Claims 1 and 10 are independent. Claim 1 is illustrative; it is reproduced below.

1. A merged cascode transistor circuit comprising:
 - an input voltage signal source having an input voltage signal;
 - a constant voltage source having a predetermined constant voltage;
 - a merged cascode transistor comprising:
 - a semiconductor element;
 - a source electrode electrically connected to a top surface of the semiconductor element;
 - a drain electrode electrically connected to the top surface of the semiconductor element and spaced laterally away from the source electrode;
 - a first gate positioned between the source electrode and the drain electrode and coupled to the semiconductor element to form a first portion of the transistor; and
 - a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor, wherein the second gate includes a field plate and is also coupled to the semiconductor element;
- wherein the first gate is connected to the input voltage signal source such that conduction of the first portion of the transistor is based on a value of the input voltage signal and the second gate is connected to the constant voltage source such that the second portion of the transistor

conducts until a voltage difference between the predetermined constant voltage and a voltage at a node in the semiconductor element between the first portion and the second portion of the transistor reaches a predetermined level, wherein the first portion of the transistor is an enhancement mode transistor and the second portion of the transistor is a depletion mode transistor, and wherein a drain region of the enhancement mode transistor is merged with a source region of the depletion mode transistor at the node in the semiconductor element.

Ex. 1001, 5:25–61.

F. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 6, 19–114):

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)/Basis
1	103(a)	Bonn, ² Mizuta ³
1–16	103(a)	Bonn, Ren, ⁴ Mishra ⁵
1–16	103(a)	Mishra, Ren

¹ Amendments to 35 U.S.C. §§ 102 and 103 enacted by the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), took effect on March 16, 2013. The ’003 patent issued from an application filed on March 20, 2007, and it claims priority to a provisional application filed on March 20, 2006. *See* Ex. 1001, codes (22), (60). Therefore, we apply the pre-AIA versions of §§ 102 and 103. Neither party, however, argues that the outcome of this case would differ based on applying the pre-AIA or post-AIA versions of these laws.

² US 6,160,280, issued Dec. 12, 2000 (Ex. 1006).

³ US 6,483,135 B1, issued Nov. 19, 2002 (Ex. 1007). Although Petitioner calls this reference “Mizuto,” we refer to it as “Mizuta” because that is the listed name of the first inventor. Ex. 1007, code (75).

⁴ US 2004/0041169 A1, published Mar. 4, 2004 (Ex. 1008).

⁵ US 2005/0051800 A1, published Mar. 10, 2005 (Ex. 1009).

In support of its unpatentability arguments, Petitioner relies on the Declaration of Joseph B. Bernstein, Ph.D. Ex. 1003. Patent Owner relies on the Declaration of David K. Choi, Ph.D. Ex. 2004.

II. ANALYSIS

A. *Legal Standards*

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and “the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). “While the sequence of these questions might be reordered in any particular case,” *KSR*, 550 U.S. at 407, the U.S. Court of Appeals for the Federal Circuit has repeatedly emphasized that “it is error to reach a conclusion of obviousness until all those factors are considered,” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1328 (Fed. Cir. 2016). Because Patent Owner does not address objective evidence of non-obviousness, we focus solely on the first three *Graham* factors.

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review

petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in an *inter partes* review).

We analyze the asserted grounds with the above-noted principles in mind.

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the pertinent art at the time of the invention is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham*, 383 U.S. at 17–18.

Factors pertinent to a determination of the level of ordinary skill in the art include “(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.” *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). “Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case.” *Id.*

Petitioner contends that one of ordinary skill in the art “would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device

design.” Pet. 5 (citing Ex. 1003 ¶¶ 67–69). Petitioner also argues that “[a]dditional education could substitute for professional experience and vice versa.” *Id.* Patent Owner does not dispute Petitioner’s proposed level of ordinary skill. PO Resp. 1–76. Neither party explains why the outcome of this case would be affected by the adoption of the proffered definition of a person of ordinary skill in the art. Accordingly, and because it appears to be consistent with the ’003 patent and the asserted prior art, we adopt Petitioner’s assessment of the level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Claim Construction

We apply the same claim-construction standard used in the federal courts—in other words, the claim-construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b), which is articulated in *Phillips*. *See* 37 C.F.R. § 42.100(b). Under the *Phillips* standard, the “words of a claim ‘are generally given their ordinary and customary meaning,’” which “is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1312–13.

Neither party proposes construing any claim terms. Pet. 6; Prelim. Resp. 1–76. In addition, as discussed below, we are able to determine the outcome of this proceeding without expressly construing any terms. Thus, we do not construe any terms for the purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy,

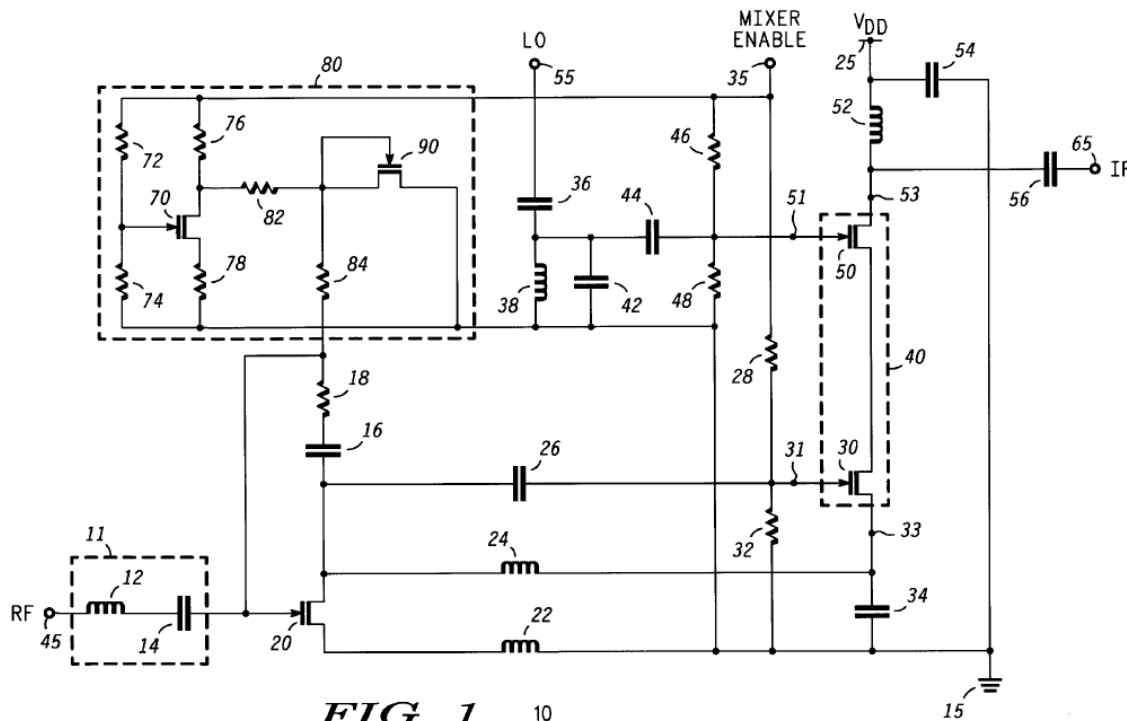
and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Asserted Obviousness over Bonn and Mizuta

Petitioner argues that a person of ordinary skill in the art would have found claim 1 obvious in light of the combined teachings of Bonn and Mizuta. Pet. 19–48; Reply 3–14. Patent Owner disagrees. PO Resp. 10–30; Sur-reply 4–18.

1. Overview of Bonn

Bonn, titled “Field Effect Transistor,” relates “to semiconductor downconverters.” Ex. 1006, code (54), 1:4–6. Bonn depicts a downconverter in Figure 1, reproduced below:



Id. at 2:66–3:6, Fig. 1. Figure 1 of Bonn depicts “downconverter 10” in schematic form. *Id.* at 2:8. The downconverter of Figure 1 includes mixer 40 with field effect transistors 30 and 50 “coupled in a cascode configuration.” *Id.* at 2:67. Transistors 30 and 50 have gate terminals 31

and 51. *Id.* at 3:22, 3:30. “Second gate terminal 51 is coupled to power supply conductor 15 via a resistor 48 and to voltage supply conductor 35 via a resistor 46.” *Id.* at 3:30–32. “In addition, second gate terminal 51 is connected to a first electrode of capacitor 44. A second electrode of capacitor 44 is coupled to power supply conductor 15 via parallel connected capacitor 42 and inductor 38.” *Id.* at 3:32–36. “Further, the second electrode of capacitor 44 is coupled to [a local oscillator (‘LO’)] port 55 via a capacitor 36 for receiving an LO signal. Capacitors 36, 42, and 44 and inductor 38 cooperate to form an impedance matching element for providing a desired input impedance, e.g., 50 Ω , at LO port 55.” *Id.* at 3:36–41.

2. *Overview of Mizuta*

Mizuta, titled “Field Effect Transistor,” relates to “[a] field effect transistor” that includes a “gate electrode [that] is provided with an overhanging field plate section.” Ex. 1007, codes (54), (57). Mizuta describes an overhanging, drain-side field plate section for gallium arsenide field-effect transistors. *Id.* at 12:30–47, Fig. 11(b). According to Mizuta, “the field centralization which develops on the edge section of the gate electrode on the drain side is made to relax and spread over, improving characteristics of withstand voltage.” *Id.* at 2:15–18. Field-effect transistors made using this method have “high withstand voltage characteristics and good gain characteristics, together with excellent high-frequency characteristics.” *Id.* at 1:63–65.

3. *Analysis of Claim 1*

To show obviousness, it is not enough to merely show that the prior art includes separate references covering each separate limitation in a

challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). “This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *KSR*, 550 U.S. at 418–419. On the other hand, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *Id.* at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). However, a petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, a petitioner must articulate a reason why a person of ordinary skill in the art would have combined or modified the prior art references. *In re NuVasive, Inc.*, 842 F.3d 1376, 1382 (Fed. Cir. 2016); *see also Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1366 (Fed. Cir. 2017) (“In determining whether there would have been a motivation to combine prior art references to arrive at the claimed invention, it is insufficient to simply conclude the combination would have been obvious without identifying any reason why a person of skill in the art would have made the combination.”); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.”) (citing *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014)).

In arguing for the obviousness of claim 1 over the combination of Bonn and Mizuta, Petitioner argues that a person of ordinary skill in the art would have modified Bonn to perform high-frequency signal amplification. Pet. 19–25. In particular, Petitioner argues that a person of ordinary skill in the art “would have found it obvious to modify the circuit of Figure 1 [of Bonn] and use Figure 7’s structure for high frequency signal amplification in place of mixer 40,” followed by additional modifications to the circuit of Figure 1. *Id.* at 22–25. These additional modifications include removing LO port 55, removing FET 20 (along with voltage source 80, capacitors 16, 26, and 34, resistor 18, and inductors 22 and 24), removing capacitor 34 and shorting gate structure 324 to ground, and removing resistors 46 and 48 and shorting terminal 51 to ground. *Id.*

According to Petitioner, the motivation for these modifications was that “Bonn . . . teaches using its dual gate structures for signal amplification without signal mixing.” *Id.* at 22 (citing Ex. 1006, 11:26–37). On the record developed at trial, we disagree. Bonn does, as Petitioner argues, teach that “the dual gate FET structure of the present invention can be tailored to provide superior performance over the prior art dual gate FET structures in high frequency signal mixing as well as other applications such as high frequency signal amplification.” Ex. 1006, 11:33–37. But the tailoring that Bonn refers to relates to changes to the structure of the field-effect transistor itself, not to the circuitry surrounding that transistor. *Id.* (teaching that the reason that “the dual gate FET structure of the present invention can be tailored” is that “the parameters such as gate width, dopant concentration, and channel depth, under each gate of the dual gate FET are individually adjusted for optimum performance”). Thus, although Bonn might have

motivated a person of ordinary skill in the art to have made changes to the dual-gate FET itself, we are not persuaded that it would have motivated the additional changes to the circuit of Bonn's Figure 1.

Petitioner also argues that some (but not all) of its proposed changes to Bonn's Figure 1 would have produced benefits that would have motivated those changes. In particular, Petitioner argues that "[s]horting the second gate of Bonn's dual-gate amplifier to ground would have provided advantages over a single-gate amplifier, including increased amplification, reduced feedback, and lower noise." Reply 7 (citing Pet. 24–25). The modifications included within the phrase "[s]horting the second gate of Bonn's dual-gate amplifier to ground" appear to include those highlighted on pages 24 and 25 of the Petition and for which Petitioner argues that the changes would increase amplification, reduce feedback, or lower noise, including both (1) removing capacitor 34 and shorting gate structure 324 to ground, and (2) removing resistors 46 and 48 and shorting terminal 51 to ground. *See* Pet. 24–25.

These advantages fail to provide a motivation to make the changes Petitioner suggests for two reasons. First, these advantages stem from making only some of Petitioner's suggested changes. They do not motivate either removing LO port 55 or removing FET 20 (along with voltage source 80, capacitors 16, 26, and 34, resistor 18, and inductors 22 and 24). Second, and more importantly, Petitioner does not even allege—let alone show by a preponderance of the evidence—that these are advantages of Bonn's as-modified structure over Bonn's unmodified structure. Instead, they are "advantages over a single-gate amplifier." Reply 7. Thus, they cannot provide a motivation to make any modification to Bonn's Figure 1.

Bonn suggests that “the parameters such as gate width, dopant concentration, and channel depth, under each gate of the dual gate FET are individually adjusted for optimum performance,” permitting the dual-gate FET to be tailored for use in high-frequency signal amplification. Ex. 1006, 11:26–37. But, on the record developed at trial, Petitioner does not show that a person of ordinary skill in the art would have been motivated to start with Bonn’s downconverter circuit and to have modified it into an amplifier circuit. Because proving this motivation is necessary for Petitioner to prove its obviousness case, Petitioner has not shown by a preponderance of the evidence that claim 1 would have been obvious over the combination of Bonn and Mizuta.

E. Asserted Obviousness over Bonn, Ren, and Mishra

Petitioner argues that claims 1–16 of the ’003 patent would have been obvious over the combination of Bonn, Ren, and Mishra. Pet. 48–82; Reply 3–18. Patent Owner disagrees. PO Resp. 30–46; Sur-reply 4–20.

1. Overview of Ren

Ren, titled “GaN-Type Enhancement MOSFET Using Hetero Structure,” “relates to an enhancement mode metal oxide semiconductor field effect transistor (MOSFET) formed from a Group-III nitride compound Semiconductor.” Ex. 1008, code (54), ¶ 3. In Figure 1, reproduced below, Ren depicts “n-channel GaN based enhancement mode MOSFET[s] according to [two separate] embodiment[s] of the invention”:

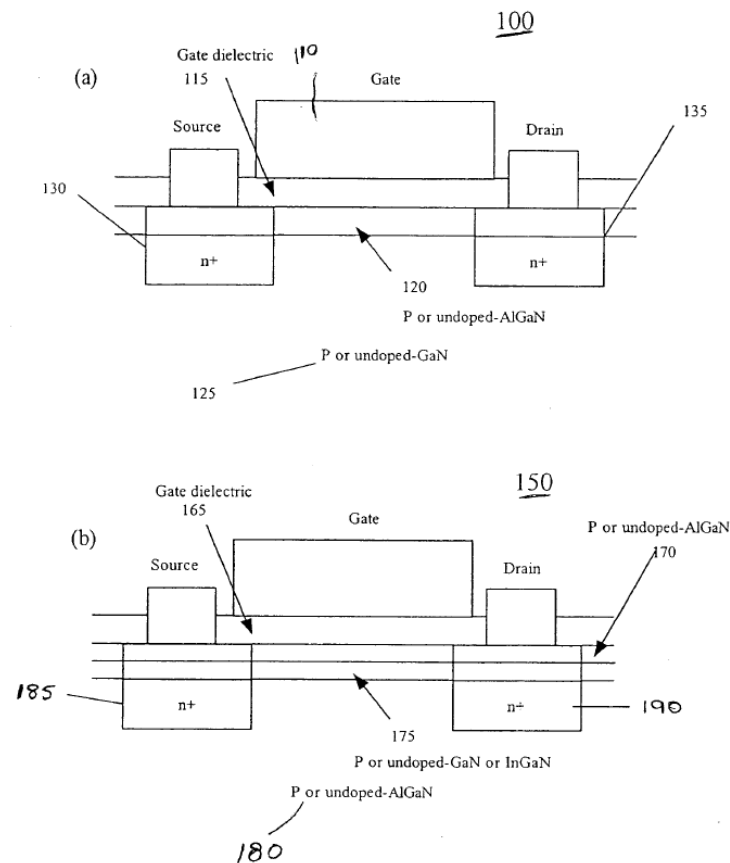


FIG. 1

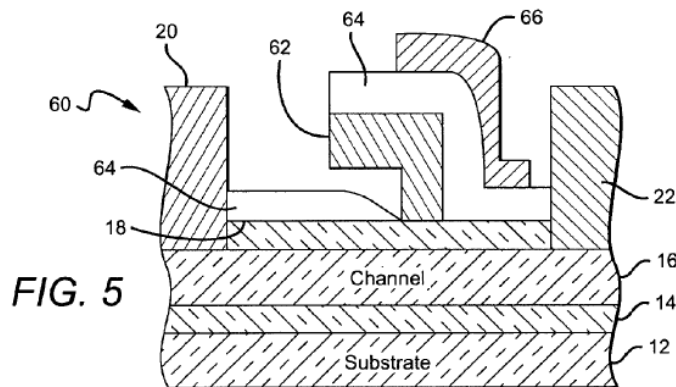
Ex. 1008 ¶¶ 20–21, Fig. 1. Each of the MOSFETs illustrated in Figure 1 includes a gate electrode located between a source electrode and a drain electrode and above a gate dielectric. *Id.* at Fig. 1. Below the gate dielectric, Figure 1(a) depicts a p-doped or undoped AlGaN layer, with a p-doped or undoped GaN channel layer below that. *Id.* ¶¶ 30–31, Fig. 1(a). Below the gate dielectric, Figure 1(b) depicts a p-doped or undoped AlGaN layer, with a p-doped or undoped GaN or InGaN layer below that, and a p-doped or undoped AlGaN layer farther below that. *Id.* ¶ 36, Fig. 1(b).

According to Ren, the operating mode of its device can be controlled by changing the thickness of the AlGaN layer, with a thin layer leading to a device operating in enhancement mode and a thick layer leading to a device

operating in depletion mode. *Id.* ¶¶ 14, 33. Ren teaches that the dividing line between enhancement mode and depletion mode is at a thickness of about 20 nanometers. *Id.* Ren discloses that enhancement mode devices “use less power as compared to depletion mode devices because enhancement mode devices, unlike depletion mode devices, generally consume little or no power during stand-by mode. Thus, the invention can reduce switching loss.” *Id.* ¶ 40.

2. Overview of Mishra

Mishra, titled “Cascode Amplifier Structures Including Wide Bandgap Field Effect Transistor with Field Plates,” “relates to transistors and particularly to amplifier circuits utilizing field plated transistors.” Ex. 1009, code (54), ¶ 3. Figure 5 of Mishra, reproduced below, depicts one of Mishra’s multiple embodiments of a high electron mobility transistor (HEMT):



Id. ¶ 42, Fig. 5. From the bottom of Figure 5 up, the figure depicts substrate layer 12, nucleation layer 14, and channel layer 16. *Id.* Atop the channel layer are source contact 20, drain contact 22, and barrier layer 18. *Id.* Between the source and drain contacts and on top of the barrier layer is “gamma(Γ) shaped gate 62 that is particularly adapted to high frequency

operation.” *Id.* “A spacer/passivation layer 64 is included that covers the gamma gate 62 and the surface of barrier layer 18 between the gamma gate 62 and the source and drain contacts 20, 22.” *Id.* ¶ 43. “The HEMT 60 also includes a field plate 66 on the spacer layer 64 that overlaps that gamma gate 62, with the field plate 66 preferably deposited on the side of the gamma gate not having a horizontal overhanging section.” *Id.* According to Mishra, “field plate 66 can be connected to the gate 62 in many different ways.” *Id.* ¶ 44.

3. *Analysis of Claims 1–16*

In arguing for the obviousness of claim 1 over the combination of Bonn, Ren, and Mishra, Petitioner argues that a person of ordinary skill in the art would have modified the circuit of Bonn’s Figure 1 to perform high-frequency signal amplification. Pet. 49–50 (citing Pet. 19–25). Petitioner relies on the same arguments for those modifications in this ground that it relies on in its Bonn/Mizuta ground. *Id.* We find those arguments unpersuasive here for the same reasons discussed above. Accordingly, Petitioner has not shown by a preponderance of the evidence that claims 1–16 would have been obvious over the combination of Bonn, Ren, and Mishra.

F. Asserted Obviousness over Mishra and Ren

Petitioner also argues that claims 1–16 would have been obvious over the combination of Mishra and Ren. Pet. 82–114; Reply 18–27. Patent Owner disagrees. PO Resp. 46–76; Sur-reply 20–27.

1. *Analysis of Claim 1*

Among other limitations, claim 1 recites both “a first gate positioned between the source electrode and the drain electrode and coupled to the

semiconductor element to form a first portion of the transistor” and “a second gate positioned adjacent to the first gate, and between the source electrode and the drain electrode to form a second portion of the transistor.” Ex. 1001, 5:25–61. Petitioner argues that “Mishra’s gate 62 is a first gate between ‘source contact 20’ and ‘drain contact 22’” and that “Mishra’s field plate 66 is” the recited second gate, “positioned adjacent to the first gate” and “between ‘source contact 20’ and ‘drain contact 22.’” Pet. 93–95 (citing Ex. 1009 ¶¶ 42–45, 55–61, Figs. 5, 10). Petitioner also argues that “Mishra includes a merged region on the drain side of gate 62 and source side of field plate 66,” where field plate 66 acts as the gate of the depletion mode transistor. *Id.* at 102 (citing Ex. 1009, Fig. 5); *see also id.* at 86–88 (identifying field plate 66 as a “second gate”).

Patent Owner argues that Mishra does not teach or suggest that field plate 66 in its Figure 5 is a second gate. PO Resp. 62–66. Petitioner replies that Mishra teaches “connecting Mishra’s field plate to source,” which turns that field plate into a second gate, and that Mishra teaches connecting the field plate of Figure 5 to the source. Reply 22–24. Patent Owner counters that Mishra does not teach connecting the field plate to the source. Sur-reply 23–26. On the record developed at trial, we agree with Patent Owner.

As it is disclosed in Mishra, field plate 66 in Figure 5 is connected to the gate, not to the source, and it is therefore not a second gate. Reply 22 (“Figure 5 depicts a single transistor with one gate.”); Ex. 1009 ¶ 44 (“field plate 66 can be connected to the gate 62 in many different ways”); *see* Ex. 2004 ¶ 157 (“Mishra never describes Figure 5 as having . . . a connection” between field plate 66 and the source); Ex. 2009, 150:16–20 (Mishra is “not telling us that the field plate is also a gate”), 154:8–155:2 (referring to idea

“that one would have to take one of the structures that Mishra discloses and modify it in order to get the dual-gate structure” as “basically right”). Mishra states that a field plate may be electrically connected to the source, but it does not state that this teaching applies to the embodiment of Figure 5. Ex. 1009 ¶¶ 29, 53, 63. Thus, the preponderance of the evidence does not support the field plate of Mishra’s Figure 5 being a second gate, as Petitioner argues in the Petition.

In the Reply, Petitioner abandons its argument that the field plate of Mishra’s Figure 5 is a second gate in favor of a new position. Petitioner’s new argument is that a person of ordinary skill in the art would have found it obvious to connect the field plate of Mishra’s Figure 5 to the source instead of the gate, converting the field plate into a second gate. *Compare* Pet. 83 (equating “drain side gate” with “field plate 66, Figure 5”), 86–88 (identifying field plate 66 as a “second gate”), *with* Reply 21–22 (identifying only the embodiment of Mishra’s Figure 10 as a source-connected field plate), 22–23 (arguing that Mishra teaches that the Figure 5 embodiment “could be arranged as ‘a single transistor with a dual gate structure’”). Although “the introduction of new evidence in the course of the trial is to be expected in *inter partes* review trial proceedings,” *Genzyme Therapeutic Prods. LP v. Biomarin Pharm. Inc.*, 825 F.3d 1360, 1366 (Fed. Cir. 2016), the shifting of arguments is not, *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1286 (Fed. Cir. 2017). Accordingly, Petitioner’s change of arguments here is inappropriate.

Moreover, even if we were to consider Petitioner’s inappropriate new argument, we would conclude that Petitioner does not support the argument with sufficient evidence. “Whether [an obviousness ground] is based on

combining disclosures from multiple references, combining multiple embodiments from a single reference, or selecting from large lists of elements in a single reference, there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination.” *In re Stepan*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017). Petitioner’s new argument relies on a person of ordinary skill in the art modifying the Figure 5 embodiment of Mishra to connect the field plate to the source rather than the gate. Reply 21–24. Petitioner does not, however, show that a person of ordinary skill in the art would have had a motivation to make this modification or a reasonable expectation that this combination would be successful. *Id.* Petitioner argues instead that “[n]o ‘reason’ is needed.” *Id.* at 24. Thus, Petitioner does not show by a preponderance of the evidence that claim 1 would have been obvious over the combination of Mishra and Ren.

2. *Analysis of Claim 10*

Similar to the “first gate” and “second gate” limitations of claim 1, claim 10 recites both “a first gate positioned between the source electrode and the drain electrode and coupled to the first epitaxial layer to form a first portion of the transistor” and “a second gate, including a field plate, positioned adjacent to the first gate, and between the drain electrode and source electrode and coupled to the first epitaxial layer to form a second portion of the transistor.” Ex. 1001, 6:28–67. Petitioner relies on its claim 1 arguments for these limitations. Pet. 112 (citing Pet. 93–96). Accordingly, Petitioner’s argument for the obviousness of claim 10 fails for the same reasons as its argument for the obviousness of claim 1.

3. *Analysis of Remaining Claims*

Claims 2–9 and 11–16 depend, directly or indirectly, from claims 1 and 10. Ex. 1001, 5:62–8:9. Because, as discussed above, Petitioner has not shown the obviousness of claims 1 and 10, Petitioner has not shown the obviousness of claims 2–9 and 11–16.

III. CONCLUSION⁶

After considering the briefs, evidence, and oral arguments in this case, we determine that Petitioner has not proven by a preponderance of the evidence that any claim of the '003 patent is unpatentable.

The following table summarizes the outcome for the challenged claims of this Final Written Decision:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1	103(a)	Bonn, Mizuta		1
1–16	103(a)	Bonn, Ren, Mishra		1–16
1–16	103(a)	Mishra, Ren		1–16
Overall Outcome				1–16

⁶ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not demonstrated by a preponderance of the evidence that any of the challenged claims of the '003 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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