

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Title Stack Of Horizontally Extending And Vertically Overlapping
Features, Methods Of Forming Circuitry Components, And Methods Of
Forming An Array Of Memory Cells

PRELIMINARY AMENDMENT

To: Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

From: Mark Matkin
Wells St. John P.S.
601 West First Avenue, Suite 1300
Spokane, WA 99201-3828
(Tel. 509-624-4276; Fax 509-838-3424)

Please enter the following amendments prior to examining the above-identified application.

AMENDMENTS

Amendments to the Claims

1. (Original): A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion; and

removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing.

2. (Original): The method of claim 1 wherein the operative and dummy structures comprise the same material.

3. (Original): The method of claim 2 wherein the operative and dummy structures comprise a plurality of the same materials.

4. (Original): The method of claim 3 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

5. (Original): The method of claim 2 wherein the operative and dummy structures consist essentially of the same material.

6. (Original): The method of claim 1 wherein the features comprise plates.

7. (Original): The method of claim 1 wherein the operative and dummy structures comprise programmable material.

8. (Original): The method of claim 1 wherein the operative and dummy structures comprise semiconductive material.

9. (Original): The method of claim 8 wherein the semiconductive material of the operative structures comprises interconnected channels of a plurality of vertically oriented transistors.

10. (Original): The method of claim 9 wherein interconnected channels are of vertically oriented charge storage transistors.

11. (Original): The method of claim 1 wherein the operative and dummy structures comprise conductive material.

12. (Original): A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the plates in the end portion;

forming horizontally elongated openings through the structures to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures; and

removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings.

13. (Original): The method of claim 12 wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures.

14. (Original): The method of claim 12 wherein the operative and dummy structures comprise hollow cylinders.

15. (Original): The method of claim 12 wherein the operative and dummy structures comprise laterally solid pillars.

16. (Original): The method of claim 12 wherein the features comprise plates.

17. (Original): A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming primary portion openings through the features in the primary portion and forming end portion openings through the features in the in the end portion;

forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the end portion openings and forming operative structures therewith within the primary portion openings and forming dummy structures therewith within the end portion openings;

forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures; and

removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.

18. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings at the same time.

19. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings at different times.

20. (Original): The method of claim 17 comprising forming at least some of the end portion openings horizontally overlap ends of individual ones of the features.

21. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings to have the same horizontal and vertical cross sections.

22. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings to have at least one of different horizontal cross sections or different vertical cross sections.

23. (Original): The method of claim 17 wherein said at least one of conductive material, semiconductive material, and programmable material is deposited simultaneously into the primary portion openings and the end portion openings.

24. (Original): The method of claim 17 wherein the features comprise plates.

25. (Original): A method of forming an array of memory cells, comprising:

forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion, the end portion having sacrificial material-comprising stairs;

forming a plurality of first openings into the primary portion of the stack;

forming a plurality of second openings into the end portion of the stack;

simultaneously forming at least one of conductive material, semiconductive material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and forming dummy structures therewith within the second openings in the end portion;

forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings;

removing at least a portion of the sacrificial material that is laterally between the horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material;

after the removing, forming conductive material into the horizontally elongated openings and the void spaces;

removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure; and

forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion.

26. (Original): The method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel regions of a NAND string.

27. (Original): The method of claim 25 wherein the memory cells comprise cross-point memory cells and the at least one formed material comprises programmable material.

28. (Original): The method of claim 25 comprising forming the first and second openings using the same masking step.

29. (Original): The method of claim 25 comprising forming the first and second openings using different masking steps.

30. (Original): The method of claim 25 wherein the sacrificial material is dielectric.

31. (Original): The method of claim 25 wherein the sacrificial material is at least one of semiconductive and conductive.

32. (Original): The method of claim 25 wherein the features comprise plates.

33. (Original): A method of forming an array of cross-point memory cells, comprising:

forming a stack of horizontally extending and vertically overlapping dielectric features, the stack comprising a primary portion and an end portion, at least some of the dielectric features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming openings through the dielectric features in the primary portion and in the end portion;

lining the openings with first material;

lining the first material-lined openings with programmable material;

filling remaining volume of the first and programmable material-lined openings with conductive material;

forming horizontally elongated trenches through the dielectric features to form horizontally elongated and vertically overlapping dielectric lines from dielectric material of the dielectric features, the dielectric lines individually extending from the primary portion into the end portion and individually laterally about sides of both the openings in the primary and end portions;

removing at least some of sacrificial material that is elevationally between the dielectric lines in the primary and end portions laterally between the trenches selectively relative to the dielectric lines and the first material lining in the openings;

after removing at least a portion of the sacrificial material, removing at

least a portion of the first material that is elevationally between the dielectric lines to expose laterally outer sidewalls of the programmable material that is elevationally between the dielectric lines; and

replacing at least a portion of the sacrificial material with conductor material that is in electrical connection with the laterally outer sidewalls of the programmable material and to comprise vertically spaced horizontal conductive lines; individual ones of the cross-point memory cells comprising crossing ones of the horizontal conductive lines in the primary portion and conductive material in the openings in the primary portion having the programmable material there-between.

Claims 34-38 (Canceled).

39. (Original): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion; and

dummy structures extending vertically through the features in the end portion.

Claims 40 and 41 (Canceled).

REMARKS

Claims 34-38, 40, and 41 are canceled. Claims 1-33 and 39 are in the application for consideration.

Claims are canceled herein without prejudice and solely to reduce filing fees. Applicant reserves the right to submit the subject matter of such claims back into this application or into an application that claims priority to this application.

Examination on the merits is requested.

Respectfully submitted,

Dated: 4-12-11

By:


Mark S. Matkin
Reg. No. 32,268

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Stack Of Horizontally Extending And Vertically Overlapping Features,
Methods Of Forming Circuitry Components, And Methods Of Forming
An Array Of Memory Cells

* * * * *

INVENTORS:

Sanh D. Tang
Roger W. Lindsay
Krishna K. Parat

ATTORNEY'S DOCKET NO. MI22-4725

STACK OF HORIZONTALLY EXTENDING AND VERTICALLY OVERLAPPING FEATURES, METHODS OF FORMING CIRCUITRY COMPONENTS, AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS

TECHNICAL FIELD

[0001] Embodiments disclosed herein pertain to stacks of horizontally extending and vertically overlapping features, and to methods of forming circuitry components and to methods of forming an array of memory cells.

BACKGROUND

[0002] Integrated circuits are often formed on a semiconductor substrate such as a silicon wafer or other semiconductive material. In general, layers of various materials which are semiconductive, conductive, or electrically insulative are utilized to form the integrated circuits. By way of examples, the various materials may be doped, ion implanted, deposited, etched, grown, etc. using various processes. A continuing goal in semiconductive processing is to strive to reduce the size of individual circuitry components, thereby enabling smaller and denser integrated circuitry.

[0003] Memory is one type of integrated circuitry, and is used in computer systems for storing data. Such is usually fabricated in one or more arrays of individual memory cells. The memory cells might be volatile, semi-volatile, or nonvolatile. Nonvolatile memory cells can store data for extended periods of time, in many instances including when the computer is turned off. Volatile memory dissipates and therefore requires being refreshed/rewritten, in many instances multiple times per second. Regardless, the smallest unit in each array is termed as a memory cell and is configured to store data as one of at least two different selectable states. In a binary system, the states are considered as either a “0” or a “1”. In other systems, at least some individual memory cells may be configured to store data as one of more than two selectable states.

[0004] Integrated circuitry fabrication continues to strive to produce smaller and denser integrated circuits. Accordingly, the fewer components an individual circuit device has, the smaller the construction of the finished device can be. A simple memory cell will be comprised of two conductive electrodes having a programmable material there-between. The programmable material is selected or designed to be configured in a selected one of at least two different physical memory states to enable storing of information by an individual memory cell. The reading of the cell comprises determination of which of the states the programmable material is in, and the writing of information to the cell comprises placing the programmable material in a target memory state. Some programmable materials retain a memory state in the absence of refresh, and thus may be incorporated into nonvolatile memory cells.

[0005] Some programmable materials may contain mobile charge carriers larger than electrons and holes, for example ions in some example applications. Regardless, the programmable materials may be converted from one memory state to another by moving the mobile charge carriers to alter a distribution of charge density within the programmable materials. Some example memory devices that utilize ions as mobile charge carriers are resistive RAM (RRAM) cells, which can include classes of memory cells containing multivalent oxides, and which can include memristors in some specific applications. Other example memory devices that utilize ions as charge carriers are programmable metallization cells (PMCs); which may be alternatively referred to as a conductive bridging RAM (CBRAM), nanobridge memory, or electrolyte memory.

[0006] The RRAM cells may contain programmable material sandwiched between a pair of electrodes. The programming of the RRAM cells may comprise transitioning the programmable material between first a memory state in which charge density is relatively uniformly dispersed throughout the material and a second memory state in which the charge density is concentrated in a specific region of the material (for instance, a region closer to one electrode than the other).

[0007] A PMC may similarly have programmable material sandwiched between a pair of current conductive electrodes. The PMC programmable material comprises ion conductive material, for example a suitable chalcogenide or any of various suitable oxides. A suitable voltage applied across the electrodes generates current conductive super-ionic clusters or filaments. Such result from ion transport through the ion conductive material which grows the clusters/filaments from one of the electrodes (the cathode), through the ion conductive material, and toward the other electrode (the anode). The clusters or filaments create current conductive paths between the electrodes. An opposite voltage applied across the electrodes essentially reverses the process and thus removes the current conductive paths. A PMC thus comprises a high resistance state (corresponding to the state lacking a current conductive filament or clusters between the electrodes) and a low resistance state (corresponding to the state having a current conductive filament or clusters between the electrodes), with such states being reversibly interchangeable with one another.

[0008] Another type of nonvolatile memory is known as flash memory, a type of EEPROM (electrically-erasable programmable read-only memory) that may be erased and reprogrammed in groups. A typical flash memory array includes a large number of nonvolatile memory cells usually grouped into blocks. Each of the cells within a block may be electrically programmed by charging its programmable gate material. The charge may be removed from the programmable gate material by a block erase operation. NAND is a basic architecture of flash memory. A NAND architecture comprises at least one select gate coupled in series to a serial combination of memory cells (with the serial combination being commonly referred to as a NAND string).

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Fig. 1 is a diagrammatic oblique view of a semiconductor substrate fragment in process in accordance with an embodiment of the invention.

[0010] Fig. 2 is a view of the Fig. 1 substrate at a processing step subsequent to that shown by Fig. 1.

[0011] Fig. 3 is a view of the Fig. 2 substrate at a processing step subsequent to that shown by Fig. 2.

[0012] Fig. 4 is a view of the Fig. 3 substrate at a processing step subsequent to that shown by Fig. 3.

[0013] Fig. 5 is a view of the Fig. 4 substrate at a processing step subsequent to that shown by Fig. 4.

[0014] Fig. 6 is an end view of Fig. 5 relative to line 6-6 in Fig. 5.

[0015] Fig. 7 is a view of the Fig. 5 substrate wherein certain material in Fig. 5 is not shown in Fig. 7 solely for clarity.

[0016] Fig. 8 is an end view of Fig. 7 relative to line 8-8 in Fig. 7.

[0017] Fig. 9 is a view of the Fig. 7 substrate at a processing step subsequent to that shown by Fig. 7.

[0018] Figs. 10 is a view of the Fig. 9 substrate wherein certain material in Fig. 9 is not shown in Fig. 10 solely for clarity.

[0019] Fig. 11 is a view of the Fig. 9 substrate at a processing step subsequent to that shown by Fig. 9.

[0020] Fig. 11A is an enlarged view of a portion of Fig. 11.

[0021] Fig. 12 is view of the Fig. 11 substrate wherein certain material in Fig. 11 is not shown in Fig. 12 solely for clarity.

[0022] Fig. 13 is a view of the Fig. 12 substrate at a processing step subsequent to that shown by Fig. 12.

[0023] Fig. 14 is a diagrammatic perspective view of a semiconductor substrate fragment in process in accordance with an embodiment of the invention.

[0024] Fig. 15 is a view of the Fig. 14 substrate at a processing step subsequent to that shown by Fig. 14.

[0025] Fig. 16 is a view of the Fig. 15 substrate at a processing step subsequent to that shown by Fig. 15.

[0026] Fig. 17 is a view of the Fig. 16 substrate at a processing step subsequent to that shown by Fig. 16.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0027] Example embodiments in accordance with the invention of methods of forming circuitry components are initially described with reference to Figs. 1-10. In some embodiments, an array of memory cells may be fabricated, for example as described with reference to Figs. 1-13 and with reference to Figs. 14-17. In one embodiment, such may comprise cross-point memory cells (e.g., as shown in Fig. 17), and in one embodiment may comprise NAND circuitry (e.g., as shown in Figs. 11, 11A, 12, and 13).

[0028] Referring to Fig. 1, a substrate fragment 10 comprises a suitable base substrate 13 over which various materials have been provided. Base substrate 13 may be homogenous or non-homogenous, for example comprising multiple different composition materials and/or layers. As examples, such may comprise bulk monocrystalline silicon and/or a semiconductor-on-insulator substrate. As an additional example, such may comprise dielectric material having contacts (e.g., conductive vias) formed therein which extend vertically or otherwise into communicative contact (e.g., current conductive electrical connection) with device components, regions, or material that is elevationally inward of the dielectric material. In this document, vertical is a direction generally orthogonal to a primary surface relative to which the substrate is processed during fabrication and which may be considered to define a generally horizontal direction. Further, “vertical” and “horizontal” as used herein are generally perpendicular directions relative one another independent of orientation of the substrate in three-dimensional space. Further in this document, “elevational” and “elevationally” are with reference to the vertical direction from a base substrate upon which the circuitry is fabricated.

[0029] The base substrate may or may not be a semiconductor substrate. In the context of this document, the term “semiconductor substrate” or “semiconductive substrate” is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in

assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0030] In one embodiment, substrate 10 comprises a stack of alternating sacrificial material 12 and dielectric material 14 formed over base substrate 13. Each material 12 and 14 may be homogenous or non-homogenous. In one embodiment, the respective sacrificial materials 12 are of the same composition relative one another. In one embodiment, the respective dielectric materials 14 are of the same composition relative one another. Regardless, sacrificial material 12 may be selectively etchable, in one embodiment highly selectively etchable, relative to dielectric material 14. In the context of this document, a "selective" etch requires removal of the stated one material relative to another at a rate of at least 1.5:1, and a highly selective etch at a rate of at least about 10:1. Sacrificial material 12 may be any one or more of conductive (e.g., current conductive), dielectric, or semiconductive. By way of an example only, dielectric material 14 may comprise silicon dioxide (whether doped or un-doped), and an example sacrificial material is a conductive or insulative nitride, for example titanium nitride or silicon nitride, respectively. A dielectric material 16 and a hardmask 18 have been provided outwardly of alternating materials 12, 14. Each material 16 and 18 may be homogenous or non-homogenous. Dielectric material 16 may be of the same composition as dielectric material 14, and hardmask material 18 may be of the same composition as sacrificial material 12. Fig. 1 depicts vertical tiers of three sacrificial materials 12 with two alternating dielectric materials 14. Additional alternating pairs of sacrificial and dielectric materials may be provided elevationally inward of innermost sacrificial material 12 or elevationally outward of outermost sacrificial material 12.

[0031] Stack of alternating materials 12, 14 may be considered as comprising a primary portion 18 and an end portion 20. The end portion in the depicted embodiment has been patterned to form a stair step-like construction. Such may be formed to provide horizontal area for later forming contacts to components,

regions, or material in end portion 20 as will be apparent in the continuing discussion. In one embodiment and as shown, end portion 20 comprises individual stairs 21 which at least include sacrificial material 12.

[0032] In one embodiment, materials 12 and 14 may be features (e.g., plates), such as plates or features that are plate-like, whether continuously and/or discontinuously formed. In one embodiment, a method of forming circuitry components comprises forming a stack of horizontally extending and vertically overlapping plates at least some of which increase in horizontal extent in the vertical inward direction in the end portion of the stack (i.e., at least some of which extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion). Either of collective materials 12 or 14 may be considered in such example embodiment as comprising such plates, or materials 12 and 14 in combination in the depicted embodiment may be considered as such plates. In one embodiment, the horizontally extending and vertically overlapping plates are dielectric, for example plates 14 regardless of the composition of sacrificial material 12. In one embodiment, all of the plates increase in horizontal extent in the vertical inward direction in the end portion of the stack. For example in the embodiment of Fig. 1, either of collective plates 12 or collective plates 14 may be considered as plates all of which increase in horizontal extent progressing vertically inward in the end portion of the stack. Alternately, a composite of each immediately adjacent plate pairs 12, 14 may be considered as respective plates which increase in horizontal extent in the vertical inward direction in end portion 20 of the stack.

[0033] In one embodiment, primary portion 18 and end portion 20 comprise a portion of an array area 22 within which a plurality of memory cells will be fabricated. Logic circuitry (not shown) may be fabricated outside of the array area. Control and/or other peripheral circuitry (not shown) for operating the memory array may or may not fully or partially be within the array area, with an example array area as a minimum encompassing all of the memory cells of the given array/sub-array. Further, multiple sub-arrays might also be fabricated and operated

independently, in tandem, or otherwise relative one another. As used in this document, a “sub-array” may also be considered as an array.

[0034] Referring to Fig. 2, dielectric material has been formed over substrate 10 and planarized at least to the outermost surface of hardmask 18. The dielectric material may be homogenous or non-homogenous and, in one embodiment, may be of the same composition as that of material 14 and is so shown and designated in the figures.

[0035] Referring to Fig. 3, first openings 25 have been formed into primary portion 18 of the stack and second openings 27 have been formed into end portion 20 of the stack. Any openings which overlap the primary and end portions may be such first or second openings (i.e., as primary portion openings or end portion openings), with example such openings being shown in Fig. 3 and designated as second openings 27. Openings 25, 27 may be formed through each plate 12, 14. An example technique for forming openings 25, 27 is by photolithographic patterning followed by subtractive anisotropic etching. First openings 25 need not be of the same shape and/or density relative one another. Second openings 27 need not be of the same shape and/or density relative one another, or relative to any one or more of first openings 25. As examples, openings 25 and 27 may be formed to have the same horizontal and vertical cross sections (not shown). Alternately, openings 25 and 27 may be formed to have at least one of different horizontal cross sections (as shown) or different vertical cross sections (as shown). Further and regardless, openings 25 and 27 may be formed at the same time or at different times, and/or may use the same masking step or different masking steps where, for example, photolithographic or other masking is used. In one embodiment and as shown, at least some of openings 27 in end portion 20 are formed to horizontally overlap ends of individual plates 12 and/or 14.

[0036] At least one of conductive material, semiconductive material, and programmable material is/are deposited into the openings. In one embodiment where conductive material is deposited into the openings, such may comprise

current conductive material. In the context of this document, current conductive material can include a composition where electric current flow may inherently occur therein predominantly by movement of subatomic positive and/or negative charges when such are generated as opposed to predominantly by movement of ions. Example current conductive materials are elemental metals, alloys of elemental metals, current conductive metal compounds, and conductively doped semiconductive material, including any combinations thereof.

[0037] In one embodiment, the depositing of the conductive material, semiconductive material and/or programmable material occurs simultaneously into all of the openings in the primary portion. In one embodiment, the depositing of such material occurs simultaneously into all of the openings in the end portion. In one embodiment, the depositing of such material occurs simultaneously into all of the openings in both of the primary and end portions. Operative structures (e.g., circuit components, such as local vertical extensions) are formed therewith within the openings in the primary portion, and dummy structures (e.g. dummy vertical extensions) are formed therewith within the openings in the end portion. In the context of this document, a “dummy” structure is a structure which is used to mimic a physical property of another structure (e.g., load carrying ability of an operative structure) and which may comprise a circuit inoperable electrical dead end (e.g., is not part of a current flow path of a circuit even if conductive). Openings in which dummy structures are formed may be considered as “dummy openings”.

[0038] For example referring to Fig. 4, a material 30 has been deposited within openings 25, 27, and then planarized back through hardmask material 18 (not shown). An example thickness for material 30 is from about 100 to about 150 Angstroms. Material 30 may be homogenous or non-homogenous, and may comprise one or more of conductive material (e.g., current conductive material), semiconductive material, and programmable material. In one embodiment, material 30 comprises semiconductive material. Further in such embodiment, the semiconductive material may comprise interconnected channels of a plurality of

vertically oriented transistors, and in one embodiment comprises interconnected channels of vertically oriented charge storage transistors as will be apparent from the continuing discussion. Regardless, in one embodiment, material 30 may form operative structures 31 (e.g., operative circuit components 31) within primary portion openings 25 and form dummy structures 32 (e.g., dummy circuit components) within end portion openings 27. In one embodiment and as shown, such operative structures 31 and dummy structures 32 are in the form of hollow cylinders. Alternately by way of example, such may be in the form of laterally solid pillars (not shown in Fig. 4). Regardless, the above processing describes but examples of forming operative structures 31 vertically through plates 12 and/or 14 in primary portion 18 and forming dummy structures 32 vertically through plates 12 and/or 14 in end portion 20. In one embodiment, the operative and dummy structures may comprise the same material (as shown). In one embodiment, the operative and dummy structures may comprise a plurality of the same materials (not shown in Fig. 4), and in one such embodiment be arranged in the same lateral order relative one another in the operative and dummy structures. In one embodiment, the operative and dummy structures may consist essentially of the same material.

[0039] Referring to Figs. 5-8, horizontally elongated openings 34 (e.g., trenches) have been formed through plates 12 and/or 14, and laterally between material 30, to form horizontally elongated and vertically overlapping lines 36 from material of the plates. Lines 36 individually extend from primary portion 18 into end portion 20 and individually laterally about sides of vertically extending portions of both operative structures 31 and dummy structures 32. Figs. 7 and 8 are views of Figs. 5 and 6, respectively, wherein dielectric material 14 added in Fig. 2 is removed solely for clarity in such drawings. Where either of operative structures 31 or dummy structures 32 are upwardly open (e.g., as shown), such may be partially or wholly filled (not shown) with dielectric and/or other material prior to the forming of horizontally elongated openings 34.

[0040] Referring to Figs. 9 and 10, at least some of sacrificial material 12 that is elevationally between lines 36 within primary portion 18 and end portion 20 has been removed from being laterally between horizontally elongated openings 34. Such thereby, in one embodiment, forms void spaces 29 elevationally between vertically spaced horizontal dielectric lines 36. An example technique includes etching, for example isotropic dry and/or wet etching. Etching may be conducted selectively (ideally, highly selectively) relative to lines 36, operative structures 31, and dummy structures 32. Fig. 10 is a view of the Fig. 9 substrate wherein dielectric material 14 added in Fig. 2 is removed solely for clarity in such drawing.

[0041] The above processing discloses but example embodiments of forming circuitry components in accordance with some aspects of the invention. In one embodiment, a method of forming circuitry components comprises forming a stack of horizontally extending and vertically overlapping features. By way of example only, such features may comprise plates, with the example depicted structure of plates 14 comprising but one example of such plates. Regardless, in such embodiment, the stack comprises a primary portion and an end portion wherein at least some of the features increase in horizontal extent in the vertical inward direction in the end portion of the stack (i.e., at least some of which extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion). Operative structures 31 (e.g., circuit components) are formed vertically through the features in the primary portion and dummy structures 32 (e.g., dummy circuit components) are formed vertically through the features in the end portion. The processing depicted through Fig. 4, or through Figs. 5-8, are examples. The operative and dummy structures may comprise the same material, and in one embodiment may consist essentially of the same material. The dummy structures may support material of the features from vertical movement in the end portion while at least some of sacrificial material that is elevationally between the material of the features in the primary and end portions is removed. The processing depicted in going from that of Figs. 5-8 to that of Figs. 9 and 10 is but one such example processing. With respect to a prior art problem, dummy structures heretofore have not been provided in a stair-like end portion of an array.

Accordingly, the floors/ceilings that are vertically between the respective void spaces 29 in Figs. 9 and 10 may be sagged, bent, or broken during processing due to lack of support. In accordance with one embodiment of the invention, dummy structures in the end portion support the features (e.g., the respective ceilings and floors, or plates) from vertical movement, for example by laterally engaging side portions of such floors/ceilings that were created where such dummy structures extend there-through. Regardless, other attributes as described may be employed.

[0042] Additional processing may occur in fabricating integrated circuitry, for example in fabricating an array of memory cells as next described with reference to Figs. 11-13. Referring to Figs. 11 and 11A, material 40 has been isotropically deposited within horizontally elongated openings 34, former void spaces 29 (not shown in Figs. 11, 11A), and any remaining volume of openings 25, 27. Material 40 has subsequently been removed from horizontally elongated openings 34 to form vertically spaced horizontal conductive lines 42 within the void spaces elevationally between horizontal lines 36 of dielectric material 14. In one embodiment, conductive lines 42 collectively cross a row of the operative and dummy structures at different respective elevations. In one embodiment, individual structures 31, 32 cross different conductive lines at different respective elevations. In the depicted example, conductive lines 42 extend longitudinally straight linear. Alternately by way of example, some or all of lines 42 may not be straight linear, for example being longitudinally curvilinear (not shown). Material 40 may also be removed from the remaining internal volume of openings 25, 27 as shown. Fig. 12 depicts the circuitry of Fig. 11 wherein the dielectric material that is shown as being deposited in Fig. 2 is removed solely for clarity.

[0043] Figs. 11, 11A, and 12 depict but one example embodiment comprising NAND circuitry wherein operative structures 31 comprise interconnected channel regions of a NAND string. In such example embodiment, material 40 comprises a composite of a suitable tunnel dielectric 49 (Fig. 11A), floating gate/charge trapping material 48, dielectric 50, and conductive control gate material 52.

Thereby, conductive material 52 provides but an example conductive portion of conductive lines 42 that is within the void spaces between the horizontal lines of dielectric material, and which collectively cross a row of the operative and dummy structures at different respective elevations. Individual ones of the memory cells of the example circuitry of Figs. 11 and 11A comprise an intersection of an individual horizontal conductive line and an individual operative structure (e.g., in the form of a string of channels of NAND), and some of which are indicated with reference numeral 55.

[0044] In one embodiment, a respective contact may be formed to a stair extension of individual ones of horizontal conductive lines 42 in end portion 20 for making communicative connection to circuitry. One such example is diagrammatically shown in Fig. 13. The dielectric material 14 of Fig. 2 is again showed removed solely for clarity in depicting certain components. Specifically, Fig. 13 shows example individual contacts 60 (e.g, current conductive contacts) which may be formed through the dielectric material 14 (not shown) of Fig. 2 for making communicative connection to circuitry, such as that elevationally outward of that depicted by Fig. 13 with respect to each conductive line 42.

[0045] Circuitry components other than or in addition to components of memory cells may be fabricated in accordance with embodiments of the invention.

[0046] An example embodiment of a method of forming an array of cross-point memory cells is next described with reference to Figs. 14-17. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix “a” or with different numerals. Fig. 14 depicts an alternate embodiment substrate fragment 10a to that depicted by Fig. 4. In Fig. 14, openings 25, 27 have been lined with a first material 62. In one embodiment, such material is dielectric (i.e., a 15 to 30 Angstroms thick layer of undoped silicon dioxide). Thereafter, a programmable material 30 was deposited to line over first material 62 within openings 25, 27. Then, remaining volume of openings 25, 27 has been filled with conductive material 64, and materials 62, 30, and 64 planarized back to materials 14 and 16.

Horizontally elongated openings (not shown in Fig. 14) may then be formed analogous to the processing depicted by Figs. 5-8.

[0047] Programmable material 30 may be solid, gel, amorphous, crystalline, or any other suitable phase. Any existing or yet-to-be developed programmable material may be used, with only some examples being provided below.

[0048] One example programmable material is ion conductive material. Example suitable such materials comprise chalcogenide-type (for instance, materials comprising one or more of germanium, selenium, antimony, tellurium, sulfur, copper, etc.; with example chalcogenide-type materials being $\text{Ge}_2\text{Sb}_2\text{Te}_5$, GeS_2 , GeSe_2 , CuS_2 , and CuTe) and/or oxides such as zirconium oxide, hafnium oxide, tungsten oxide, copper oxide, niobium oxide, iron oxide, silicon oxide (specifically, silicon dioxide), gadolinium oxide, etc. capable of inherently (or with additive) supporting electrolyte behavior. Such may have silver, copper, cobalt, and/or nickel ions, and/or other suitable ions, diffused therein for ionic conduction, analogously to structures disclosed in U.S. Patent No. 7,405,967 and U.S. Patent Publication Number 2010/0193758.

[0049] Additional example programmable materials include multi-resistive state metal oxide-comprising material. Such may comprise, for example, at least two different layers or regions generally regarded as or understood to be active or passive regions, although not necessarily. Alternately, such may only comprise active material. Example active cell region compositions which comprise metal oxide and can be configured in multi-resistive states include one or a combination of $\text{Sr}_x\text{Ru}_y\text{O}_z$, Ru_xO_y , and $\text{In}_x\text{Sn}_y\text{O}_z$. Other examples include MgO , Ta_2O_5 , SrTiO_3 , SrZrO_3 , BaTiO_3 , $\text{Ba}_{(1-x)}\text{Sr}_x\text{TiO}_3$, ZrO_x (perhaps doped with La), and CaMnO_3 (doped with one or more of Pr, La, Sr, or Sm). Example passive cell region compositions include one or a combination of Al_2O_3 , TiO_2 , and HfO_2 . Regardless, a programmable material composite might comprise additional metal oxide or other materials not comprising metal oxide. Example materials and constructions for a multi-resistive state region comprising one or more layers including a programmable metal oxide-comprising material are described and disclosed in U.S.

Patent Nos. 6,753,561; 7,149,108; 7,067,862; and 7,187,201, as well as in U.S. Patent Application Publication Nos. 2006/0171200 and 2007/0173019. Further as is conventional, multi-resistive state metal oxide-comprising materials encompass filament-type metal oxides, ferroelectric metal oxides and others, and whether existing or yet-to-be developed, as long as resistance of the metal oxide-comprising material can be selectively changed.

[0050] The programmable material may comprise memristive material. As an example, such material may be statically programmable semiconductive material which comprises mobile dopants that are received within a dielectric such that the material is statically programmable between at least two different resistance states. At least one of the states includes localization or gathering of the mobile dopants such that a dielectric region is formed and thereby provides a higher resistance state. Further, more than two programmable resistance states may be used. In the context of this document, a “mobile dopant” is a component (other than a free electron) of the semiconductive material that is movable to different locations within said dielectric during normal device operation of repeatedly programming the device between at least two different static states by application of voltage differential to the pair of electrodes. Examples include atom vacancies in an otherwise stoichiometric material, and atom interstitials. Specific example mobile dopants include oxygen atom vacancies in amorphous or crystalline oxides or other oxygen-containing material, nitrogen atom vacancies in amorphous or crystalline nitrides or other nitrogen-containing material, fluorine atom vacancies in amorphous or crystalline fluorides or other fluorine-containing material, and interstitial metal atoms in amorphous or crystalline oxides. More than one type of mobile dopant may be used. Example dielectrics in which the mobile dopants are received include suitable oxides, nitrides, and/or fluorides that are capable of localized electrical conductivity based upon sufficiently high quantity and concentration of the mobile dopants. The dielectric within which the mobile dopants are received may or may not be homogenous independent of consideration of the mobile dopants. Specific example dielectrics include TiO_2 , AlN , and/or MgF_2 . Example programmable materials that comprise oxygen vacancies as mobile

dopants may comprise a combination of TiO_2 and TiO_{2-x} in at least one programmed resistance state depending on location of the oxygen vacancies and the quantity of the oxygen vacancies in the locations where such are received. An example programmable material that comprises nitrogen vacancies as mobile dopants is a combination of AlN and AlN_{1-x} in at least one programmed state depending on location of the nitrogen vacancies and the quantity of the nitrogen vacancies in the locations where such are received. An example programmable material that comprises fluorine vacancies as mobile dopants may be a combination of MgF_2 and MgF_{2-x} in at least one programmed resistance state depending on location of the fluorine vacancies and the quantity of the fluorine vacancies in the locations where such are received. As another example, the mobile dopants may comprise aluminum atom interstitials in a nitrogen-containing material.

[0051] Still other example programmable materials include polymer materials such as Bengala Rose, AlQ_3Ag , Cu-TCNQ, DDQ, TAPA, and fluorescein-based polymers.

[0052] Referring to Fig. 15, such corresponds in processing sequence to that of Fig. 9 of the above-described embodiments. Sacrificial material 12 (not shown) has been at least partially removed (e.g., by etching) between dielectric lines 36 in primary portion 18 and end portion 20 laterally between horizontally elongated openings 34. Material 12 may be etched selectively (ideally, highly selectively) relative to dielectric lines 36, first material lining 62, and conductive material 64 in openings 25, 27. Figs. 14 and 15 depict an example embodiment wherein the operative and dummy structures comprise a plurality of the same materials, and in such embodiment arranged in the same lateral order relative one another in the operative and dummy structures. Regardless, in one embodiment, first material lining 62 may serve as a protecting barrier from adverse exposure of programmable material 30 to the etching chemistry which etches the sacrificial material.

[0053] Referring to Fig. 16, at least a portion of first material 62 has been removed elevationally between dielectric lines 36 to expose laterally outer sidewalls of programmable material 30 that is elevationally between dielectric

lines 36. An example technique for doing so where material 62 comprises silicon dioxide includes etching with a dilute HF solution.

[0054] Referring to Fig. 17, at least a portion of sacrificial material 12 (not shown) of Fig. 14 has been replaced with conductor material 52 (e.g., current conductive material) that is in electrical connection with the laterally outer sidewalls of programmable material 30 and to comprise vertically spaced horizontal conductive lines 42a. Materials 64 and 52 may be of the same composition or of different compositions. Further and regardless, conductive material 64 within remaining volumes of openings 25, 27 alternately may be provided subsequent to the etching depicted by Fig. 15. Regardless, Fig. 17 also depicts conductor material 52 as having been at least partially removed from horizontally elongated openings 34 to form such vertically spaced horizontal conductive lines 42a.

[0055] Individual ones of the cross-point memory cells comprise crossing ones of the horizontal conductive lines in the primary portion and conductive material in the openings in the primary portion having the programmable material there-between, with some of such example memory cells being indicated with reference numeral 55 in the Fig. 17 example embodiment.

[0056] An embodiment of the invention includes a stack of horizontally extending and vertically overlapping features. The stack comprises a primary portion and an end portion. At least some of the features extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion. Operative structures extend vertically through the features in the primary portion. Dummy structures extend vertically through the features in the end portion. In one embodiment, the features may be horizontally extending lines, for example formed of any one or combination of conductive (e.g., current conductive), semiconductive, and/or dielectric material(s). In one embodiment, the features comprise a combination of horizontally extending conductive and dielectric lines (e.g., overlapping and alternating such lines). In one embodiment, contacts may be in the end portion, for example extending vertically to the lines.

Any other attribute as described above may be used, for example as shown and described with respect to Figs. 1-13 and with respect to Figs. 14-17.

[0057] In compliance with the statute, the subject matter disclosed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method of forming circuitry components, comprising:
forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;
forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion; and
removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing.
2. The method of claim 1 wherein the operative and dummy structures comprise the same material.
3. The method of claim 2 wherein the operative and dummy structures comprise a plurality of the same materials.
4. The method of claim 3 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.
5. The method of claim 2 wherein the operative and dummy structures consist essentially of the same material.
6. The method of claim 1 wherein the features comprise plates.

7. The method of claim 1 wherein the operative and dummy structures comprise programmable material.

8. The method of claim 1 wherein the operative and dummy structures comprise semiconductive material.

9. The method of claim 8 wherein the semiconductive material of the operative structures comprises interconnected channels of a plurality of vertically oriented transistors.

10. The method of claim 9 wherein interconnected channels are of vertically oriented charge storage transistors.

11. The method of claim 1 wherein the operative and dummy structures comprise conductive material.

12. A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the plates in the end portion;

forming horizontally elongated openings through the structures to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures; and

removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings.

13. The method of claim 12 wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures.

14. The method of claim 12 wherein the operative and dummy structures comprise hollow cylinders.

15. The method of claim 12 wherein the operative and dummy structures comprise laterally solid pillars.

16. The method of claim 12 wherein the features comprise plates.

17. A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming primary portion openings through the features in the primary portion and forming end portion openings through the features in the in the end portion;

forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the end portion openings and forming operative structures therewith within the primary portion openings and forming dummy structures therewith within the end portion openings;

forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures; and

removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.

18. The method of claim 17 comprising forming the primary portion openings and the end portion openings at the same time.

19. The method of claim 17 comprising forming the primary portion openings and the end portion openings at different times.

20. The method of claim 17 comprising forming at least some of the end portion openings horizontally overlap ends of individual ones of the features.

21. The method of claim 17 comprising forming the primary portion openings and the end portion openings to have the same horizontal and vertical cross sections.

22. The method of claim 17 comprising forming the primary portion openings and the end portion openings to have at least one of different horizontal cross sections or different vertical cross sections.

23. The method of claim 17 wherein said at least one of conductive material, semiconductive material, and programmable material is deposited simultaneously into the primary portion openings and the end portion openings.

24. The method of claim 17 wherein the features comprise plates.

25. A method of forming an array of memory cells, comprising:

- forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion, the end portion having sacrificial material-comprising stairs;
- forming a plurality of first openings into the primary portion of the stack;
- forming a plurality of second openings into the end portion of the stack;
- simultaneously forming at least one of conductive material, semiconductive material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and forming dummy structures therewith within the second openings in the end portion;
- forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings;
- removing at least a portion of the sacrificial material that is laterally between the horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material;
- after the removing, forming conductive material into the horizontally elongated openings and the void spaces;
- removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure; and
- forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion.

26. The method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel regions of a NAND string.

27. The method of claim 25 wherein the memory cells comprise cross-point memory cells and the at least one formed material comprises programmable material.

28. The method of claim 25 comprising forming the first and second openings using the same masking step.

29. The method of claim 25 comprising forming the first and second openings using different masking steps.

30. The method of claim 25 wherein the sacrificial material is dielectric.

31. The method of claim 25 wherein the sacrificial material is at least one of semiconductive and conductive.

32. The method of claim 25 wherein the features comprise plates.

33. A method of forming an array of cross-point memory cells, comprising:

forming a stack of horizontally extending and vertically overlapping dielectric features, the stack comprising a primary portion and an end portion, at least some of the dielectric features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming openings through the dielectric features in the primary portion and in the end portion;

lining the openings with first material;

lining the first material-lined openings with programmable material;

filling remaining volume of the first and programmable material-lined openings with conductive material;

forming horizontally elongated trenches through the dielectric features to form horizontally elongated and vertically overlapping dielectric lines from dielectric material of the dielectric features, the dielectric lines individually extending from the primary portion into the end portion and individually laterally about sides of both the openings in the primary and end portions;

removing at least some of sacrificial material that is elevationally between the dielectric lines in the primary and end portions laterally between the trenches selectively relative to the dielectric lines and the first material lining in the openings;

after removing at least a portion of the sacrificial material, removing at least a portion of the first material that is elevationally between the dielectric lines to expose laterally outer sidewalls of the programmable material that is elevationally between the dielectric lines; and

replacing at least a portion of the sacrificial material with conductor material that is in electrical connection with the laterally outer sidewalls of the programmable material and to comprise vertically spaced horizontal conductive lines; individual ones of the cross-point memory cells comprising crossing ones of the horizontal conductive lines in the primary portion and conductive material in

the openings in the primary portion having the programmable material there-between.

34. The method of claim 33 comprising forming the trenches after the filling.

35. The method of claim 33 wherein the conductive material and the conductor material are of the same composition.

36. The method of claim 33 wherein the conductive material and the conductor material are of different compositions.

37. The method of claim 33 wherein the first material is dielectric.

38. The method of claim 33 wherein the features comprise plates.

39. A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion; and

dummy structures extending vertically through the features in the end portion.

40. The stack of claim 39 further comprising contacts in the end portion.

41. The stack of claim 39 wherein the features comprise horizontally extending conductive lines.

ABSTRACT OF THE DISCLOSURE

A method of forming circuitry components includes forming a stack of horizontally extending and vertically overlapping features. The stack has a primary portion and an end portion. At least some of the features extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion. Operative structures are formed vertically through the features in the primary portion and dummy structures are formed vertically through the features in the end portion. Horizontally elongated openings are formed through the features to form horizontally elongated and vertically overlapping lines from material of the features. The lines individually extend from the primary portion into the end portion, and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures. Sacrificial material that is elevationally between the lines is at least partially removed in the primary and end portions laterally between the horizontally elongated openings. Other aspects and implementations are disclosed.

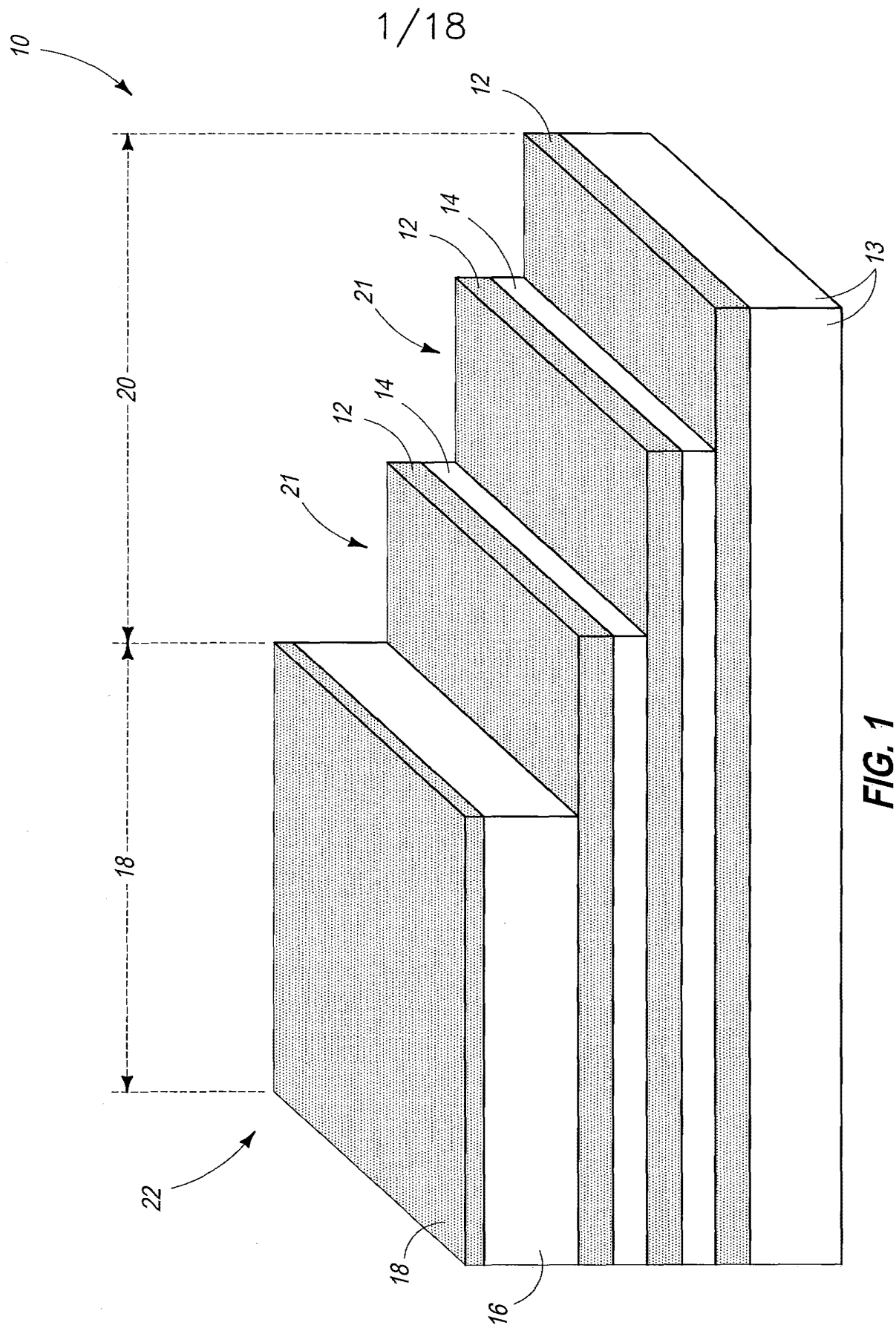


FIG. 1

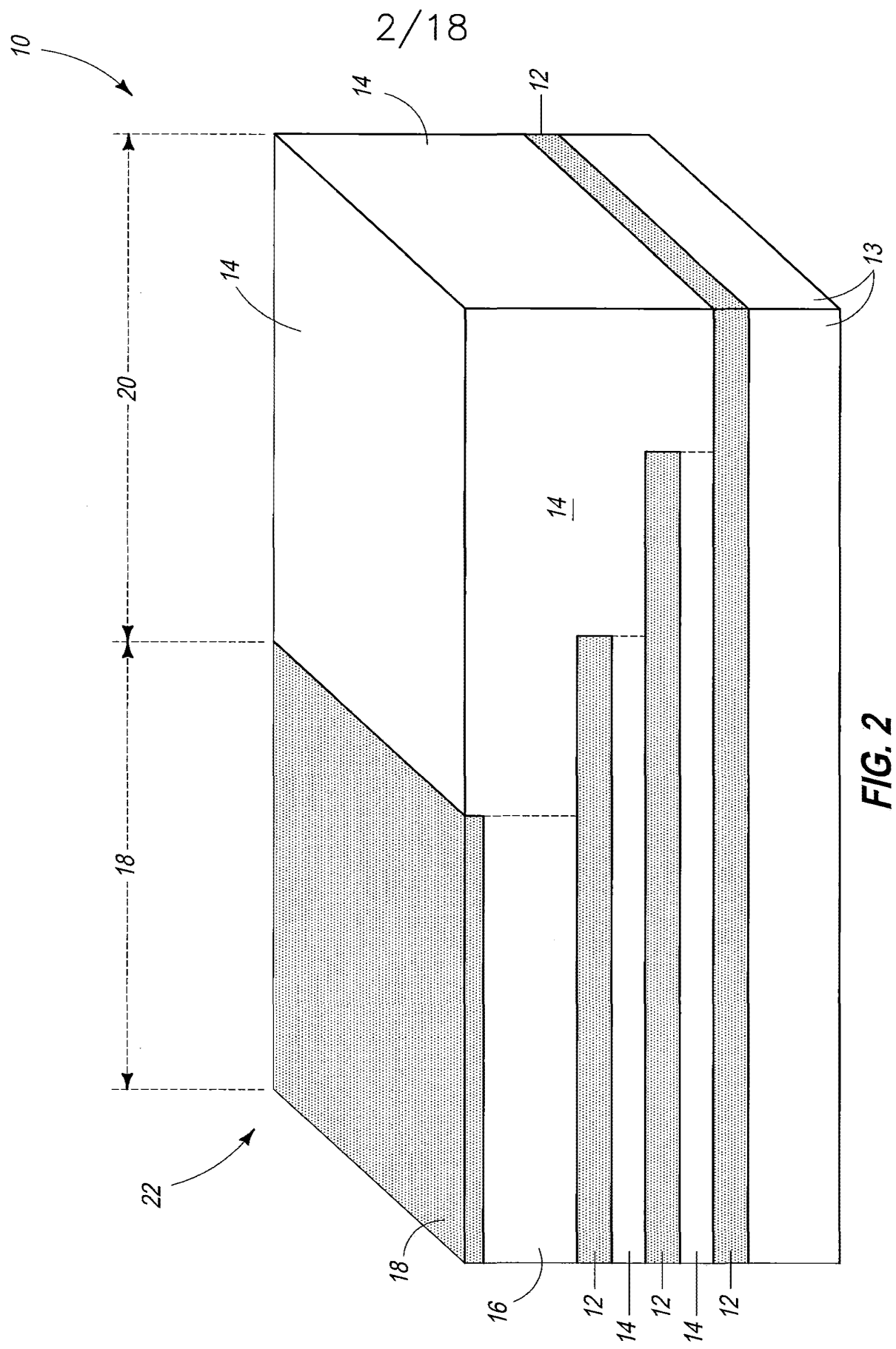


FIG. 2



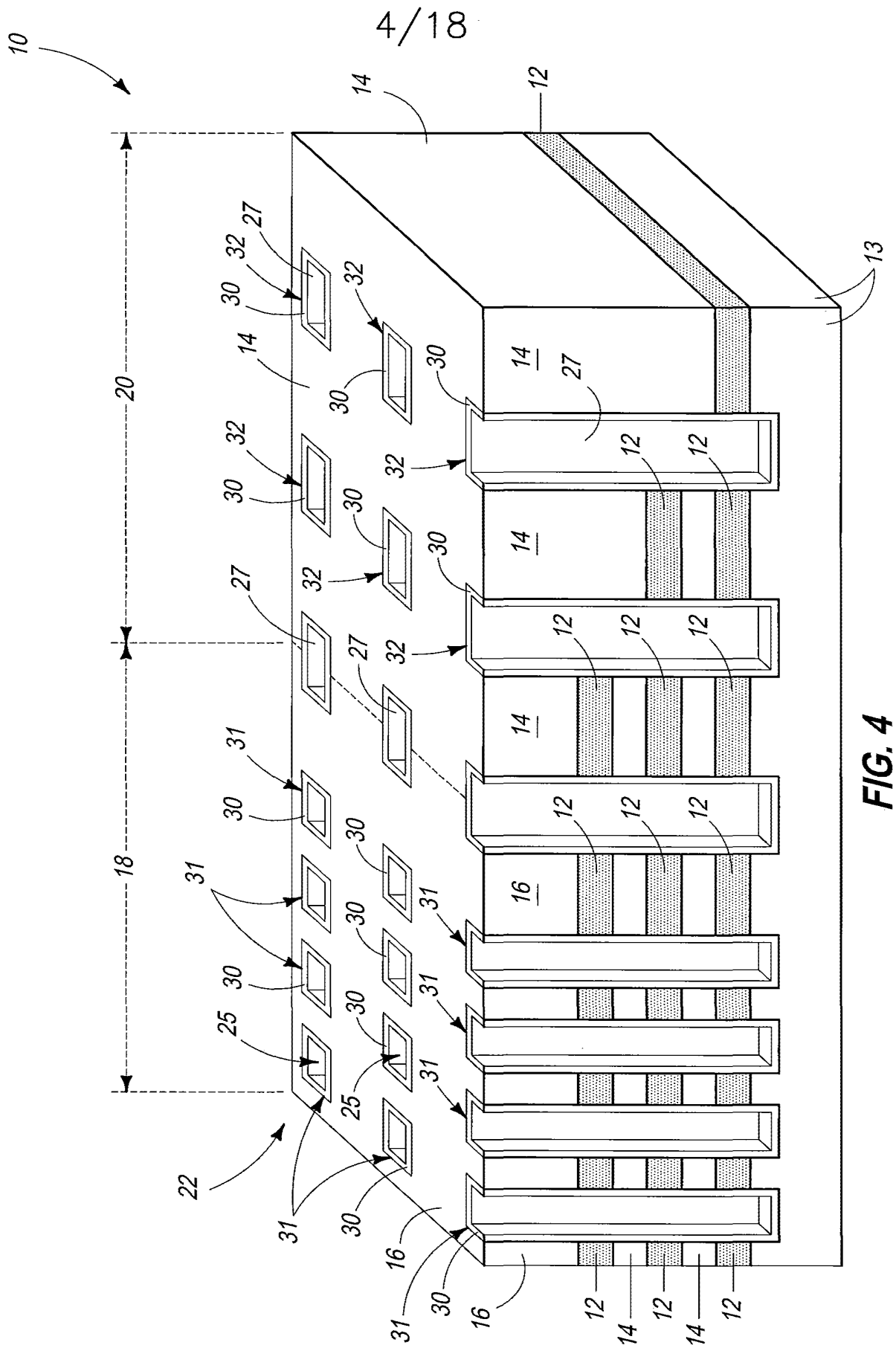


FIG. 4

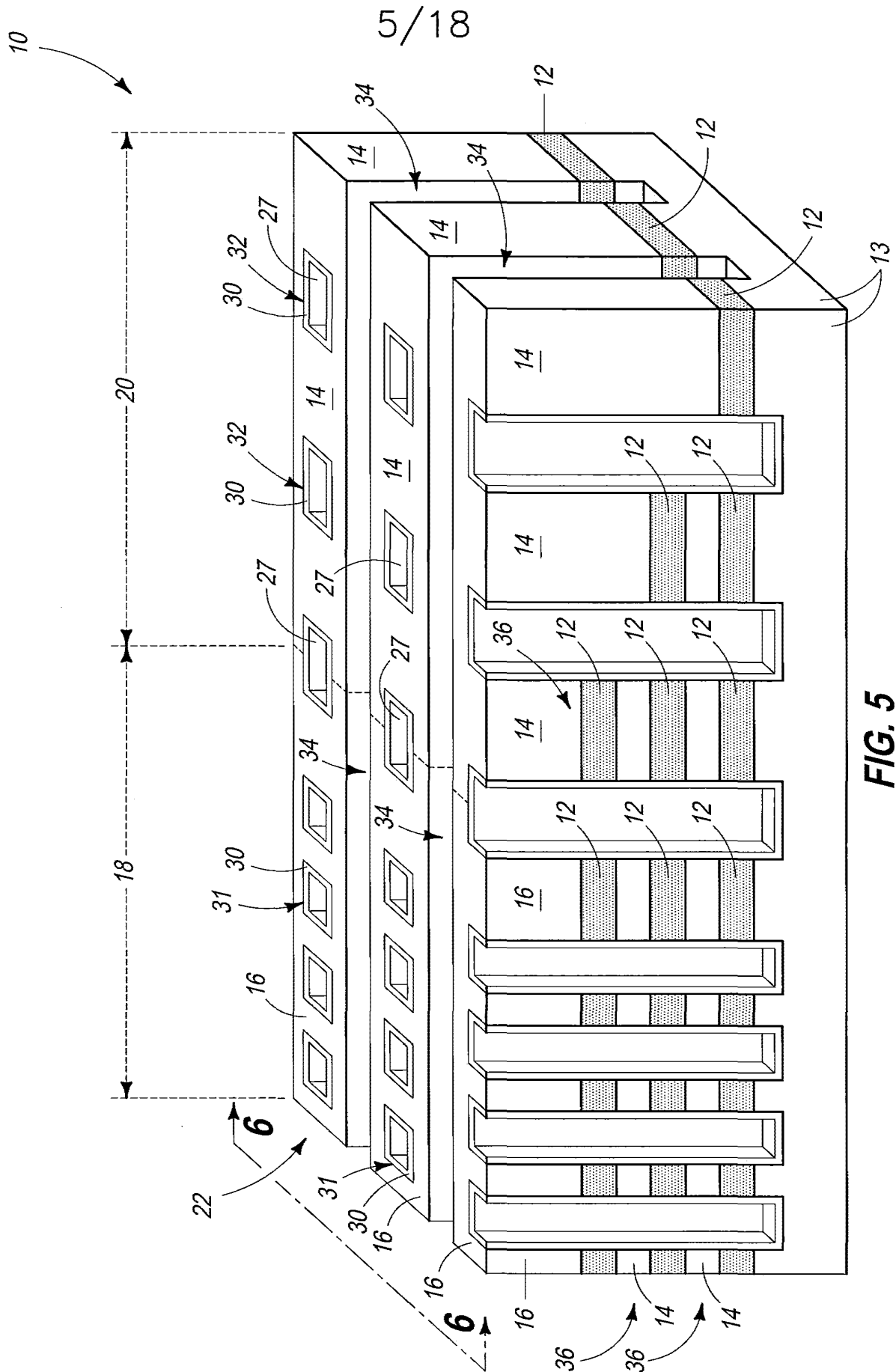


FIG. 5

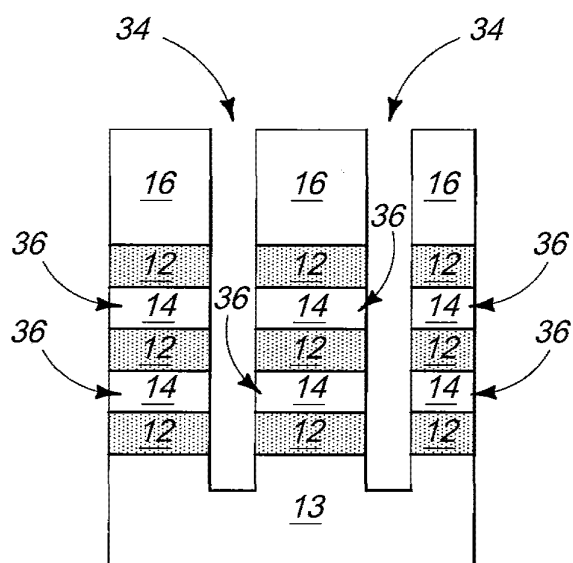
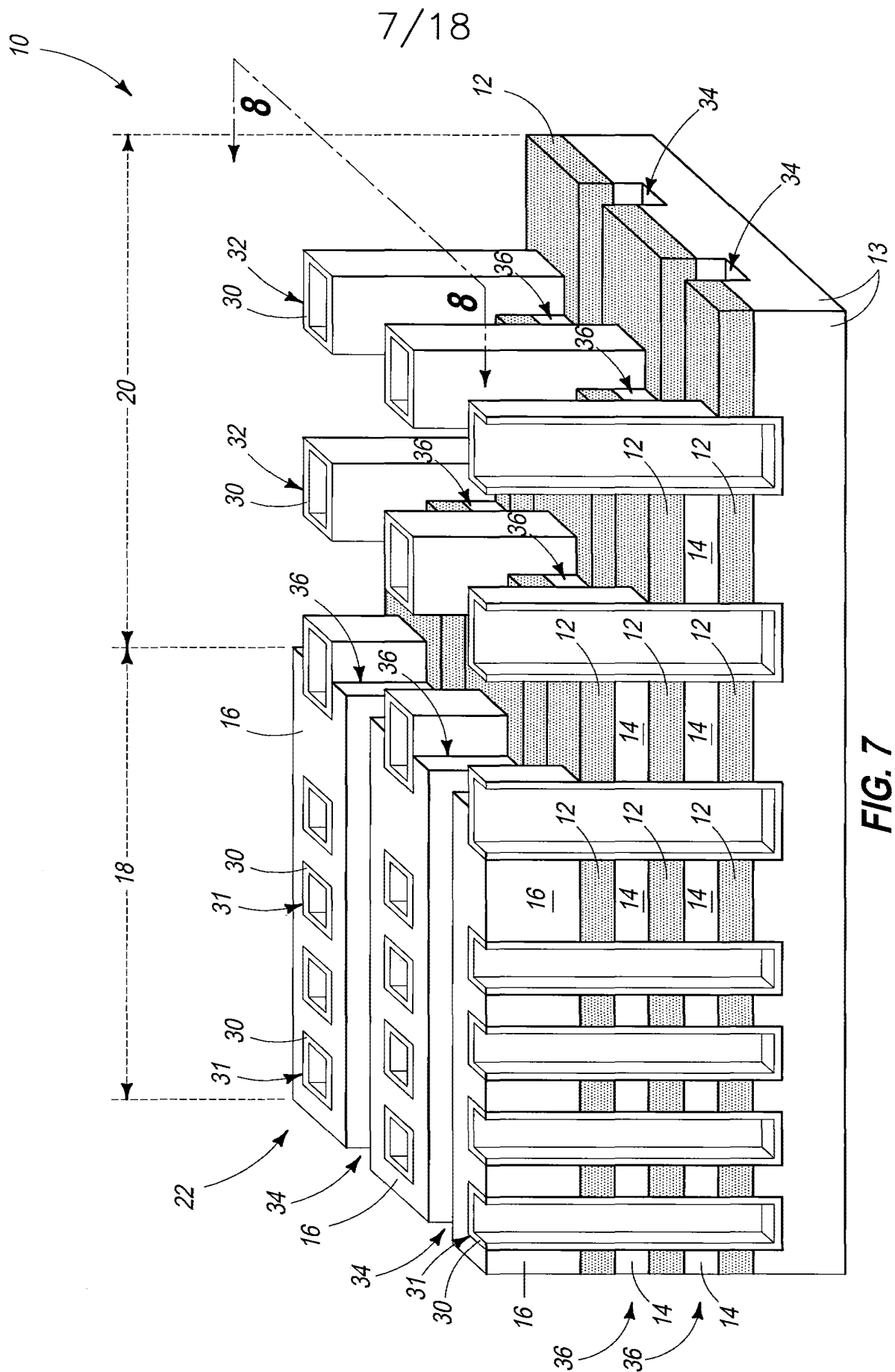


FIG. 6



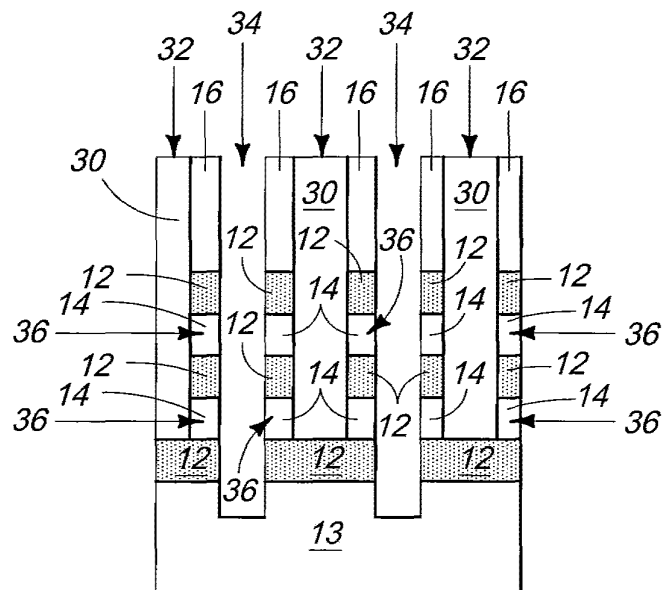


FIG. 8

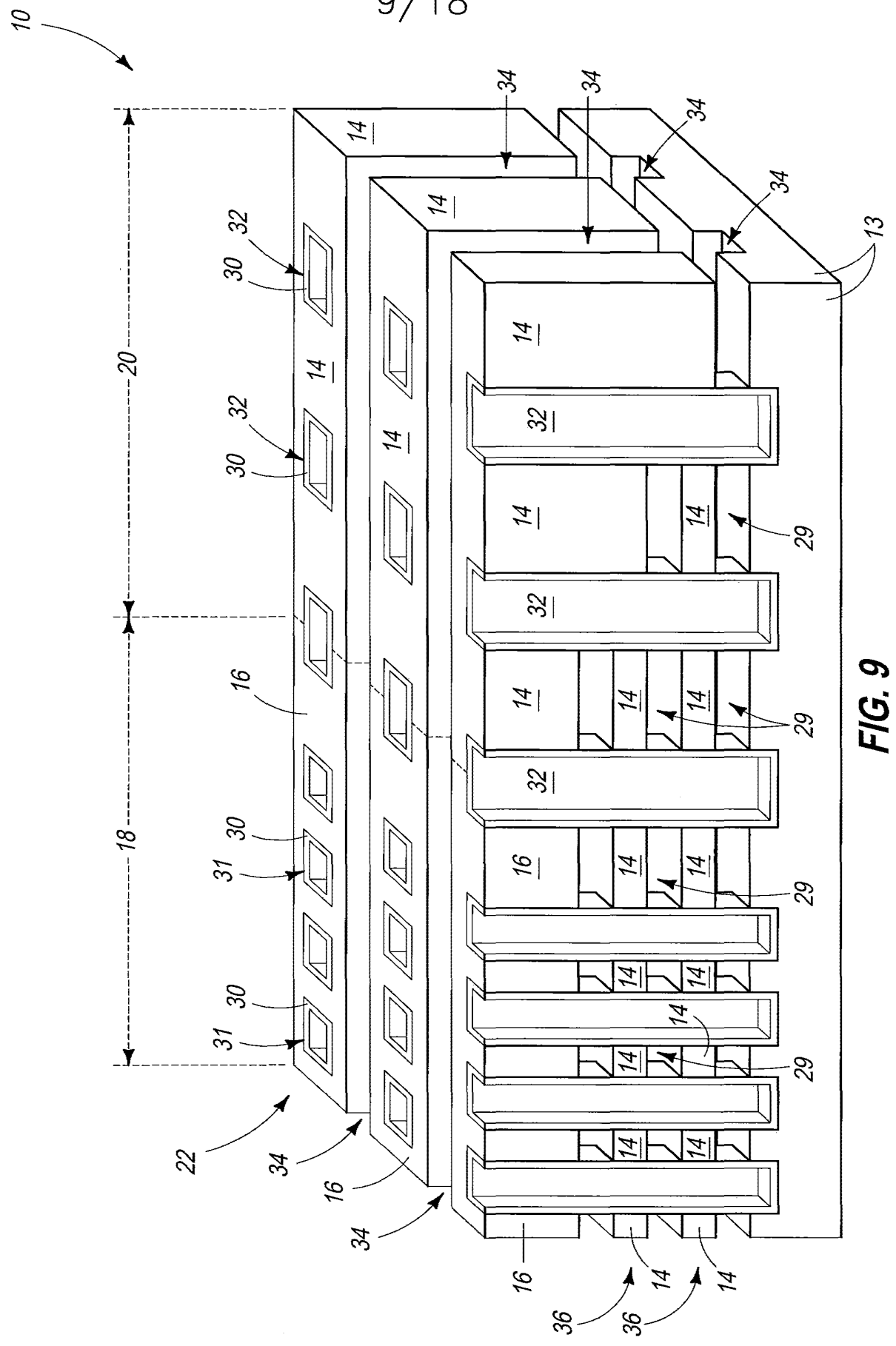
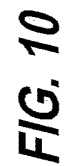


FIG. 9

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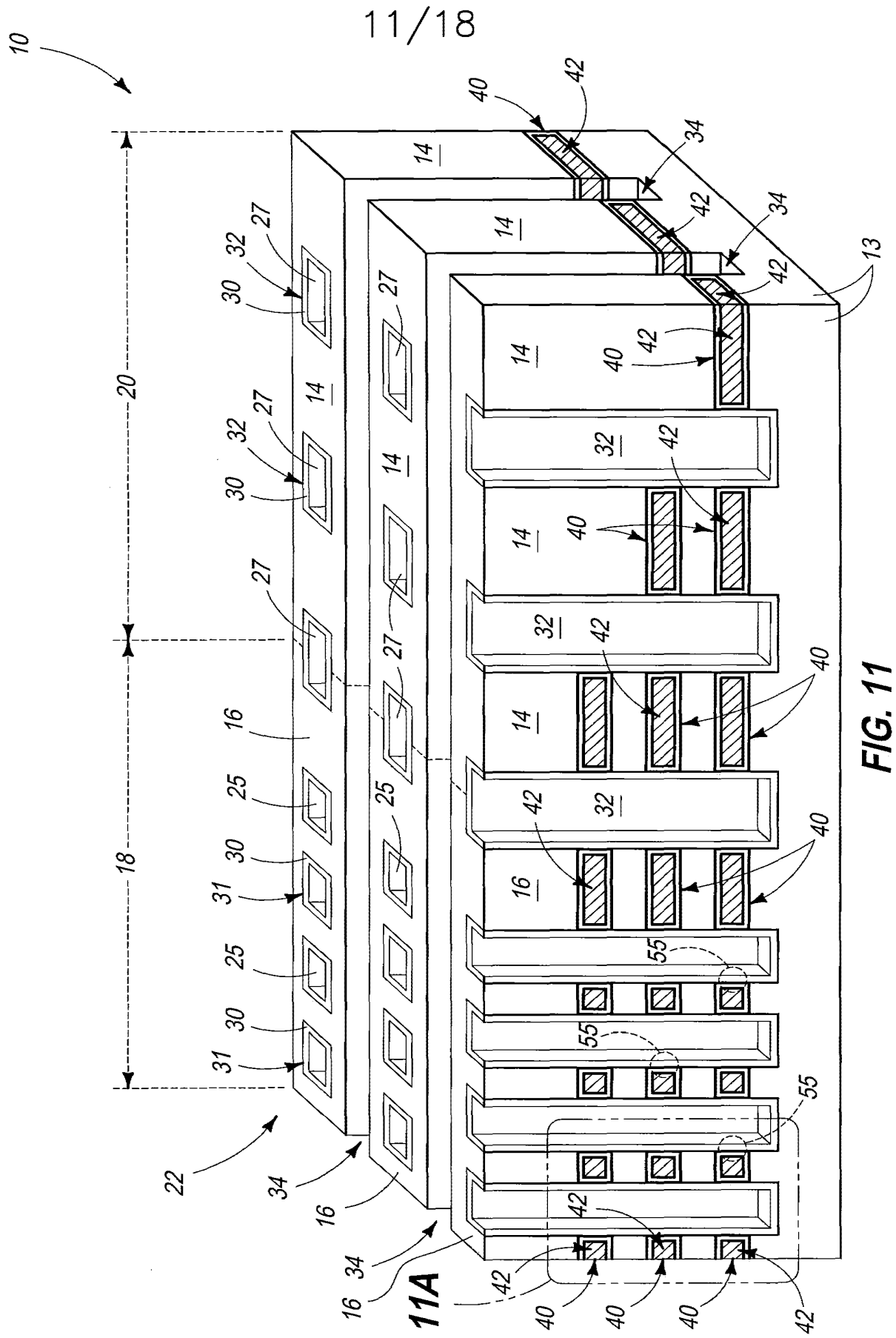


FIG. 11

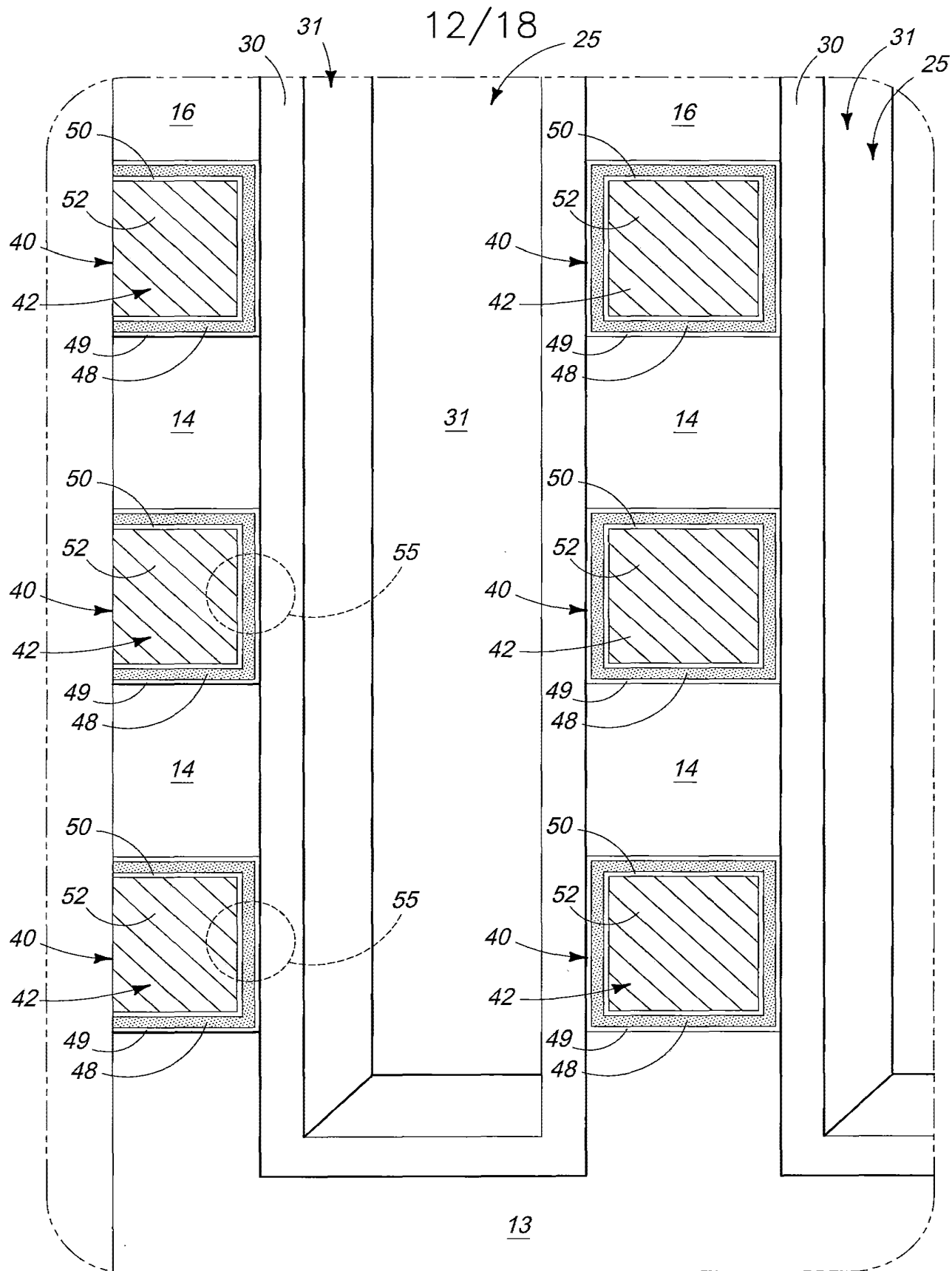
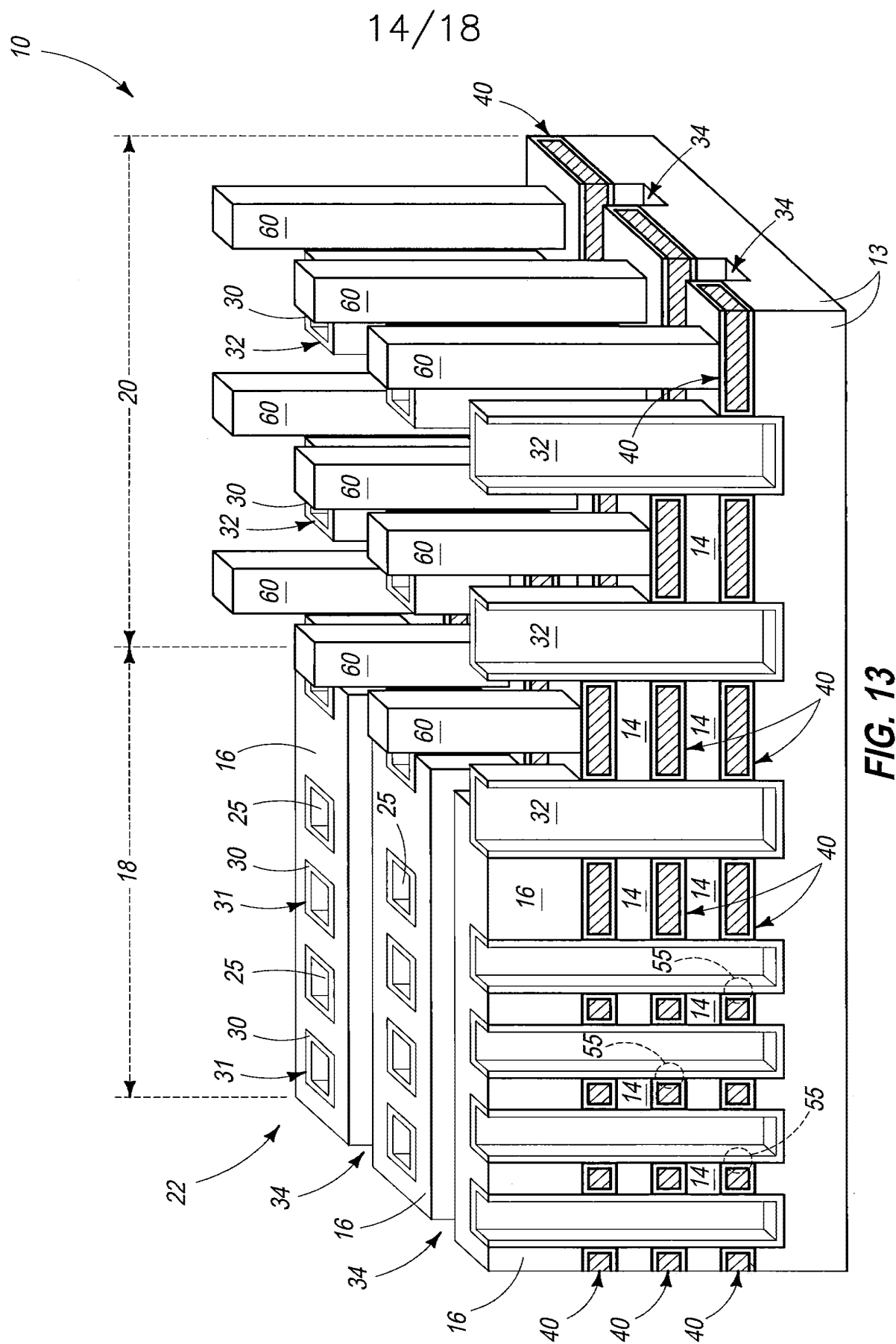


FIG. 11A





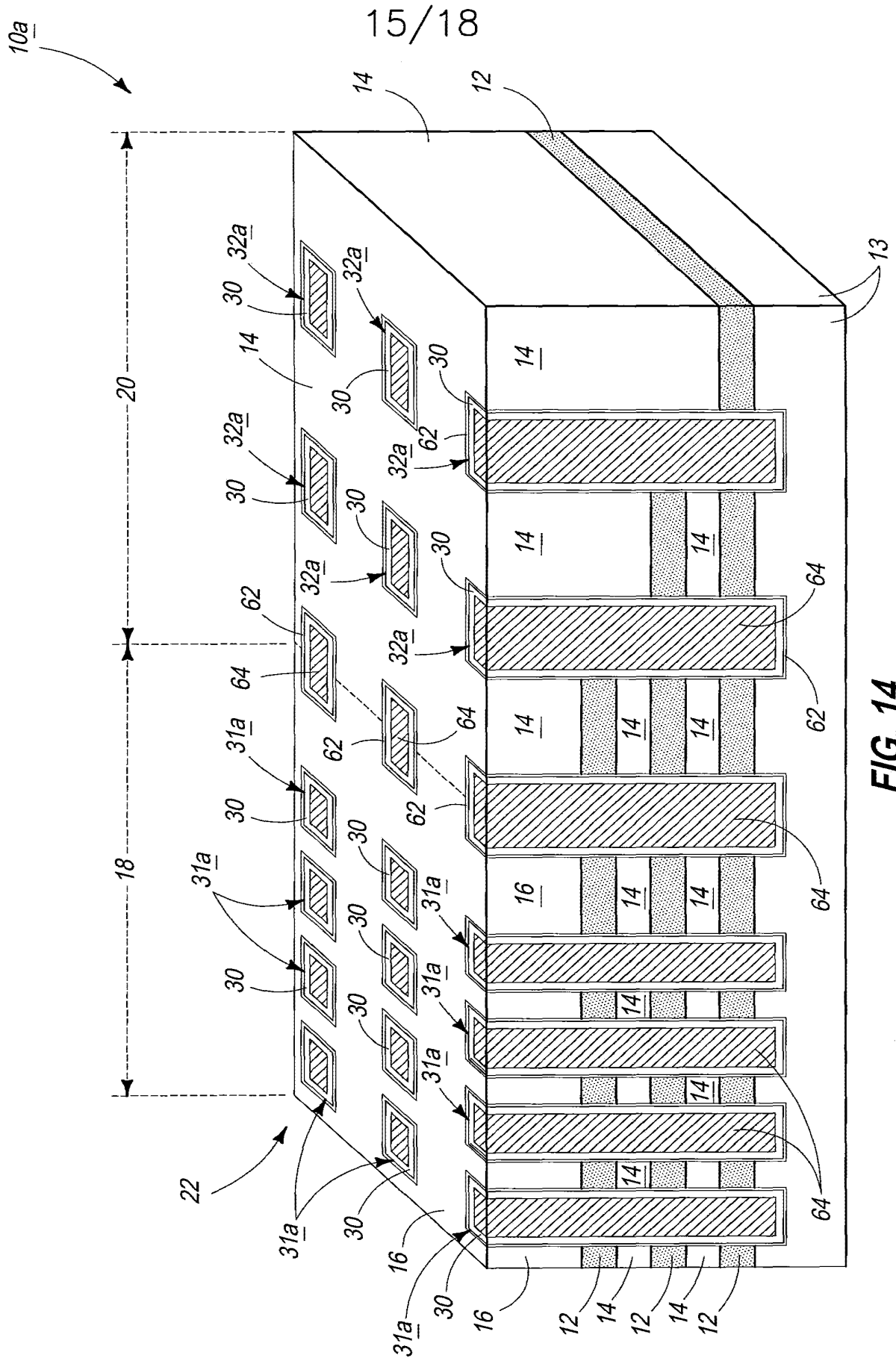
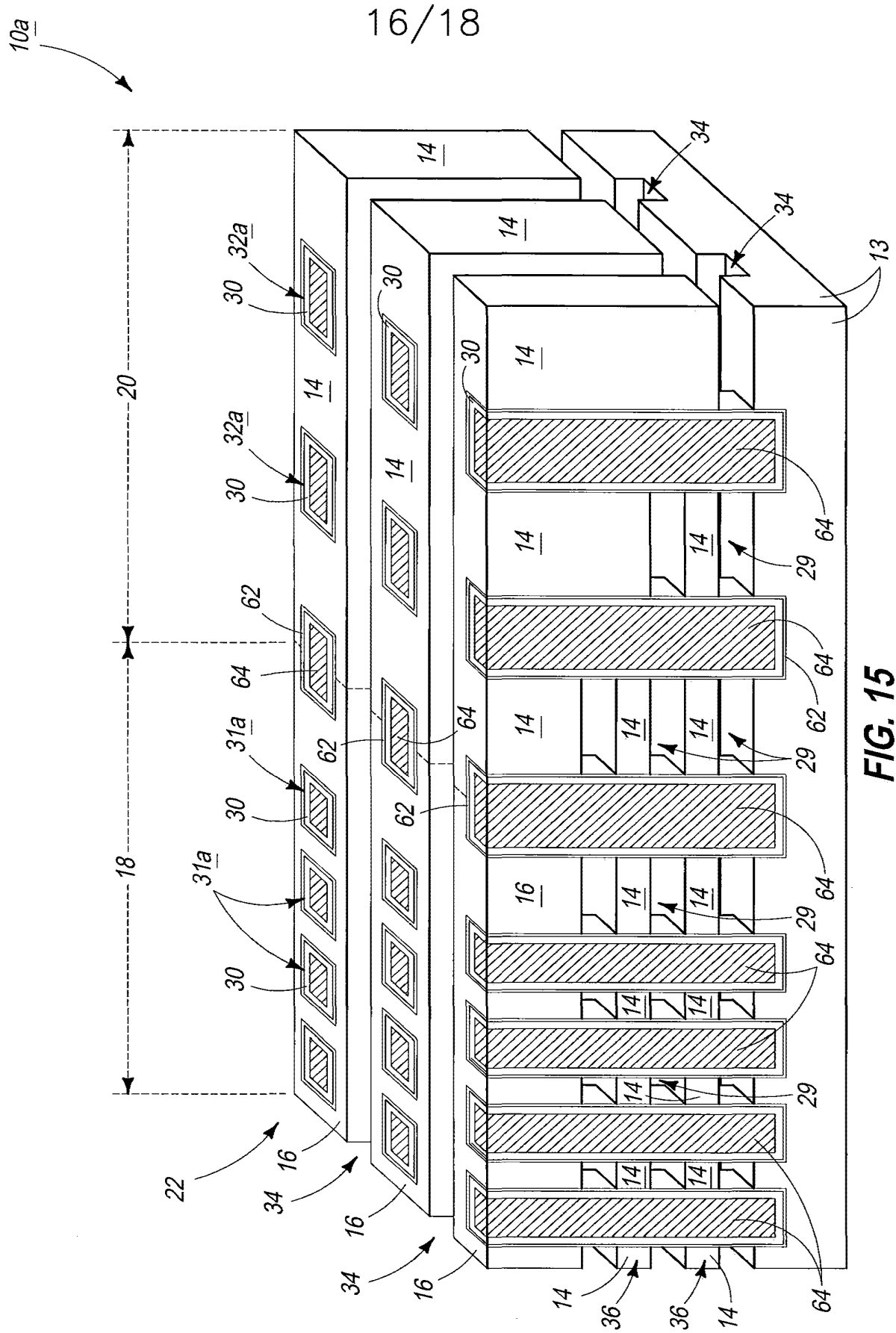


FIG. 14



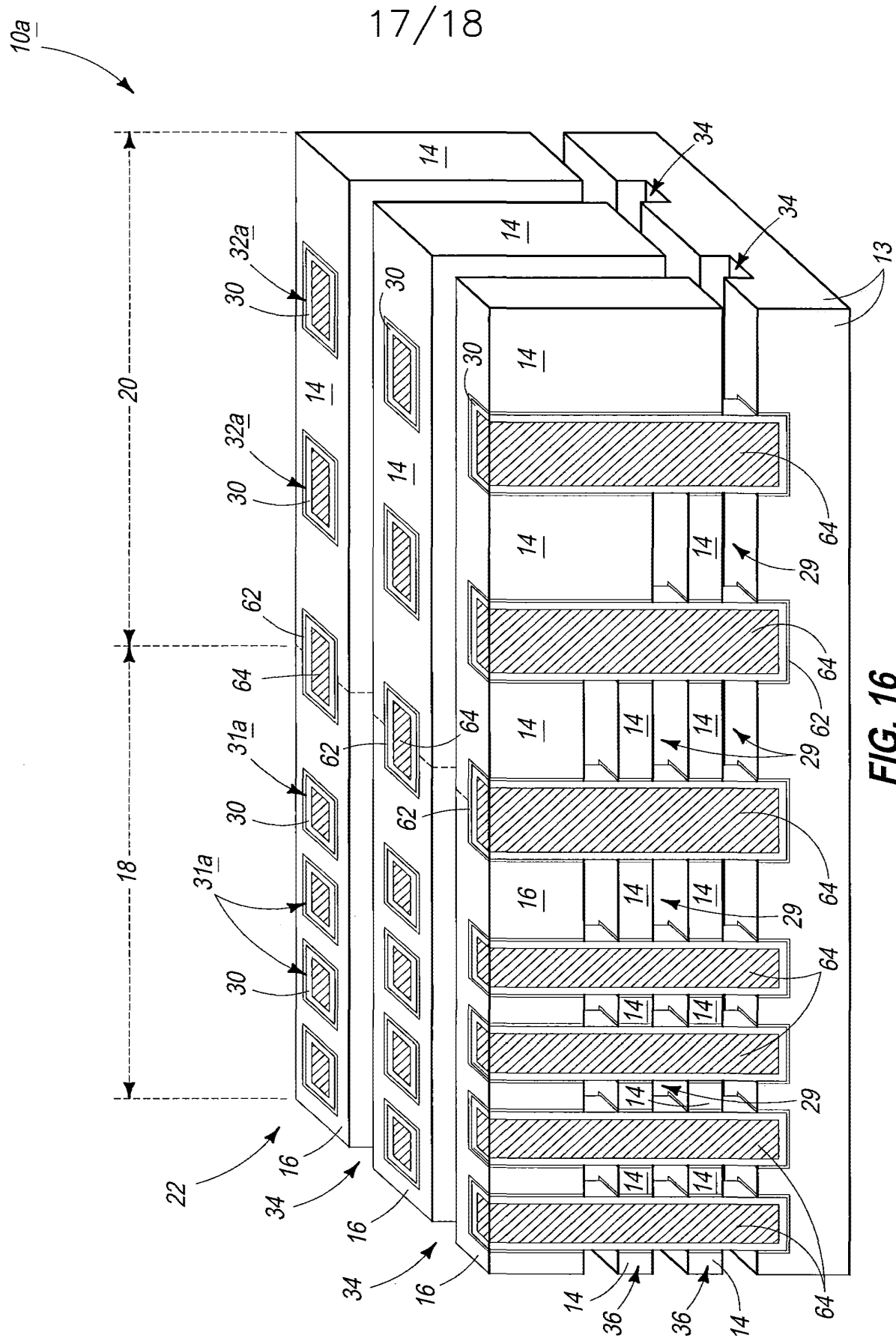


FIG. 16

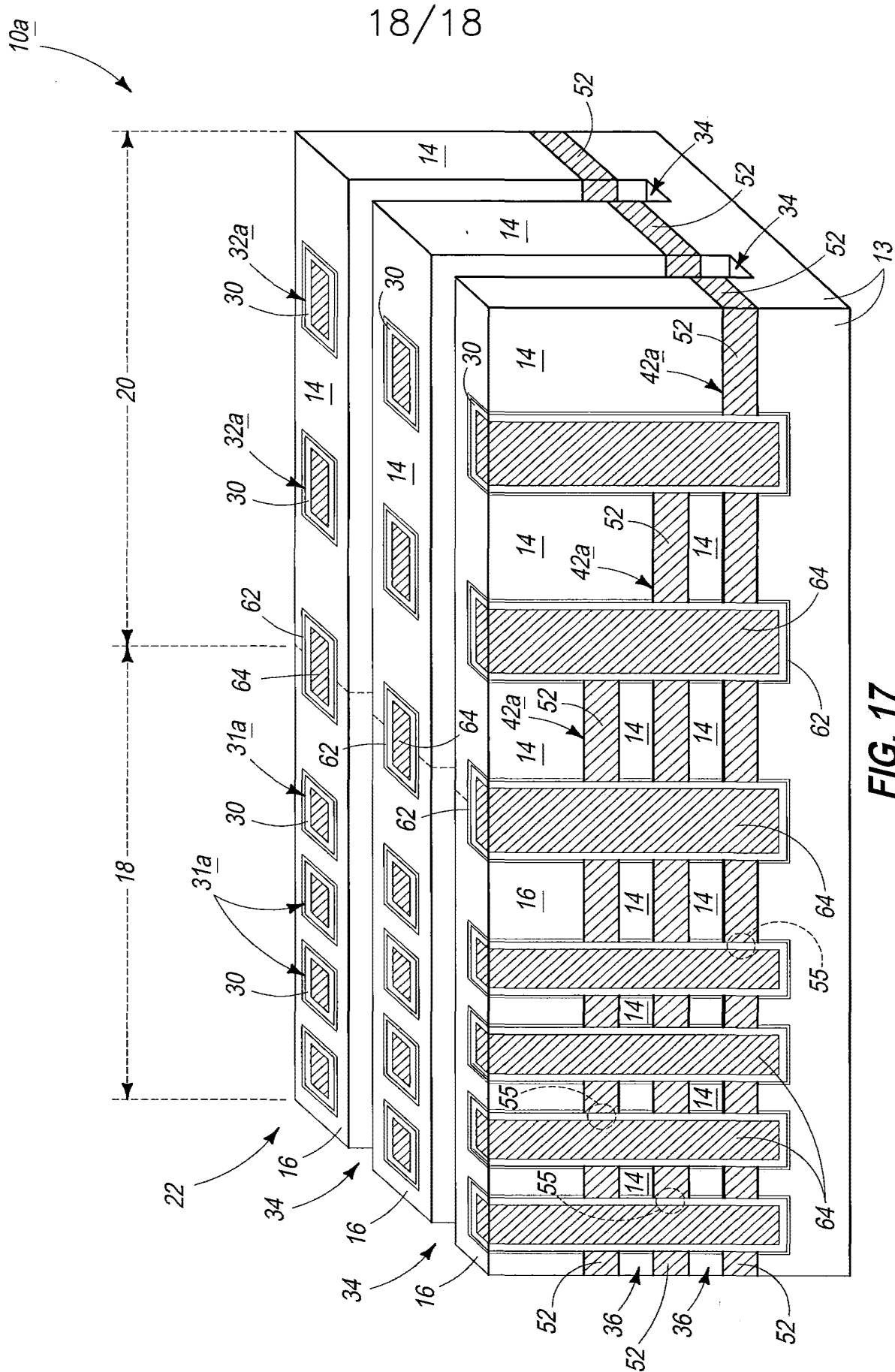


FIG. 17

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. Filed Herewith
Filing Date Filed Herewith
Confirmation No. Unassigned
Inventor Sanh D. Tang et al.
Assignee Micron Technology, Inc.
Group Art Unit..... Unknown
Examiner Unknown
Attorney's Docket No. MI22-4725
Title: Stack of Horizontally Extending And Vertically Overlapping Features,
Methods Of Forming Circuitry Components, And Methods Of Forming An
Array Of Memory Cells

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE
UNDER 37 CFR § 3.73(b)

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

MICRON TECHNOLOGY, INC., the Assignee of the entire right, title and interest in the above-identified patent application by an Assignment, a copy of which is provided herewith, hereby appoints, for purposes of the identified patent application including any divisional and any continuation thereof, the practitioners associated with:

Customer Number 021567

and Russ Slifer, Registration No. 39,838, as its attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

The Assignee certifies that the documentary evidence of the chain of title to the Assignee which is in the above-identified Assignment has been

reviewed and to the best of Assignee's knowledge and belief, title is in the Assignee, and that the above-identified Assignment was previously filed for recordation pursuant to 37 CFR § 3.11 or will be so-filed herewith.

Please direct all correspondence regarding this application to:

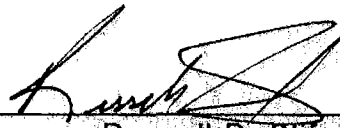
Customer No. 021567
Wells St. John P.S.
Attn: Mark S. Matkin
601 West First Avenue, Suite 1300
Spokane, WA 99201-3828
Telephone: (509) 624-4276
Facsimile: (509) 838-3424

MICRON TECHNOLOGY, INC.

Dated: _____

4/11/11

By: _____



Name: Russell D. Slifer
Title: Chief Patent Counsel

Attachments: Copy of Assignment;
Assignee Certificate of Assistant Corporate Secretary.

MICRON TECHNOLOGY, INC.
CERTIFICATE OF ASSISTANT CORPORATE SECRETARY

I, the undersigned, Jan R. Reimer, certify that I am the Assistant Corporate Secretary of Micron Technology, Inc., a Delaware corporation (the "Company"), and that I have been duly elected and am presently serving in such capacity in accordance with the Bylaws of the Company. I hereby further certify on behalf of the Company that the following resolutions are a true and correct copy of the resolutions adopted by the Company's Board of Directors at a meeting duly held on February 8, 2006, a quorum being present, and have been entered into the minutes of said meeting; that I am the keeper of the corporate seal and of the minutes and records of this Company; and that the said resolutions have not been rescinded or modified.

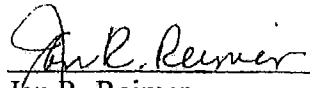
Such resolutions are in conformity with the Restated Certificate of Incorporation and Bylaws of the Company and are now in full force and effect.

WHEREAS, certain key employees require the authority to execute certain documents on behalf of the Company in order to enable them to effectively and efficiently carry out their responsibilities and duties to the Company.

NOW THEREFORE BE IT RESOLVED, that the Board hereby approves and authorizes Mr. Russell D. Slifer, Chief Patent Counsel, to execute on behalf of the Company, documents pertaining to the Company's patent prosecution matters, including but not limited to documents relating to representation before a patent examining authority, patent terms and other patent prosecution procedures, both in the United States and other countries, upon such terms and conditions as the General Counsel of the Company shall deem necessary or appropriate.

IN WITNESS WHEREOF, I have hereunto subscribed my name and affixed the seal of the said Company, as of the 17th day of February, 2006.




Jan R. Reimer
Assistant Corporate Secretary

ASSIGNMENT

PARTIES TO THE ASSIGNMENT:

INVENTORS:

Sanh D. Tang
1273 N. Jullion Ave.
Boise, ID 83704
United States

Roger W. Lindsay
4376 Falconcrest Way
Boise, ID 83716
United States

Krishna K. Parat
4177 Hubbart Drive
Palo Alto, CA 94306
United States

ASSIGNEE:

Micron Technology, Inc.
MS 1-525
8000 South Federal Way
Boise, ID 83716
United States

BACKGROUND OF THIS ASSIGNMENT:

Inventors have conceived certain new and useful inventions disclosed in a United States patent application titled Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells.

Micron Technology, Inc. (hereinafter referred to as "ASSIGNEE") desires to acquire the entire right, title and interest in said inventions and with respect to any Letters Patent that may be granted with respect to the inventions in both the United States and in all foreign countries.

THE PARTIES AGREE AS FOLLOWS:

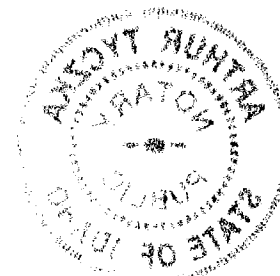
In consideration of good and valuable consideration, the receipt, sufficiency and adequacy of which is hereby acknowledged, INVENTORS have sold, assigned and transferred, and by these present do hereby sell, assign and transfer to ASSIGNEE the entire right, title and interest in the above-identified inventions and application and to any reissues, renewals, divisions or continuations of the application thereof, and hereby authorizes the Commissioner of Patents and Trademarks to issue such Letters Patent to ASSIGNEE for the sole use of ASSIGNEE, its successors or assigns.

INVENTORS further agree to execute, at the request and expense of ASSIGNEE, such other formal documents as may be required to fully convey the interest transferred herein and will similarly execute any patent application papers (foreign or domestic) required for the filing of any divisional, continuation, renewal or reissue of the patent application or resulting Letters Patent; and will generally do everything necessary or desirable to obtain and enforce proper protection for the inventions assigned hereby.

INVENTORS further assign to ASSIGNEE the whole right, title and interest in the inventions disclosed in the application throughout all

countries foreign to the United States. ASSIGNEE is hereby authorized to apply for patents relating to the inventions in its own name in countries where such procedure is proper; to claim the benefit of the International Convention; to file and prosecute International Applications relating to the inventions under the Patent Cooperation Treaty; and to file and prosecute applications relating to the inventions under the European Patent Convention. INVENTORS agree to execute applications relating to the inventions in those countries and under those conventions where it is necessary that the same be executed by the inventor, and to execute assignments of such applications and the resulting Letters Patent to ASSIGNEE as well as all other necessary papers in relation to such applications and Letters Patent. INVENTORS hereby consent that a copy of this assignment shall be deemed a full legal and formal equivalent of any document which may be required in any country as proof of the right of ASSIGNEE to apply for patent and other form of protection for said inventions and to claim the aforesaid benefit of the right of priority.

To be binding on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.



Dated: 04-08-11

Signature: Sanh D. Tang
Sanh D. Tang

State of Idaho)

County of Ada) ss.

On this 8th day of April, 2011, before me, Art Tyczka - Public Notary (name and title of Notary Official), personally appeared Sanh D. Tang, known or identified to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed within the Assignment, and acknowledged to me that he/she executed the Assignment in his/her authorized capacity, and that by his/her signature on the Assignment, the person executed the Assignment.



Arthur Tyczka
My Commission Expires: 3-15-12

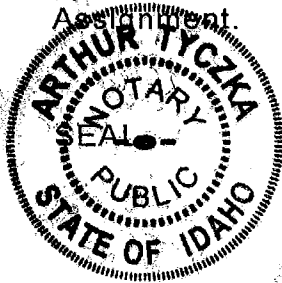
Dated: 4-11-2011

Signature: Roger W. Lindsay
Roger W. Lindsay

State of Idaho)

County of Ada) ss.

On this 11th day of April, 2011, before me, Art Tyczka - Public Notary (name and title of Notary Official), personally appeared Roger W. Lindsay, known or identified to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed within the Assignment, and acknowledged to me that he/she executed the Assignment in his/her authorized capacity, and that by his/her signature on the Assignment, the person executed the Assignment.



Arthur Tyczka
My Commission Expires: 3-15-12

Dated: 4/5/2011

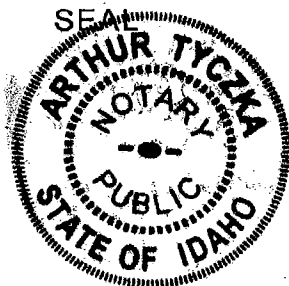
Signature: Krishna K. Parat
Krishna K. Parat

State of Idaho

County of Ada

)
) ss.
)

On this 5th day of April, 20 11, before me, Arthur Tycka - Public Asst (name and title of Notary Official), personally appeared Krishna K. Parat, known or identified to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed within the Assignment, and acknowledged to me that he/she executed the Assignment in his/her authorized capacity, and that by his/her signature on the Assignment, the person executed the Assignment.



Arthur Tycka
My Commission Expires: 3-15-12

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Stack of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to in this declaration.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * *

Full name of inventor: Sam D. Tang
Inventor's Signature: Sam D. Tang
Date: 04-08-2011
Residence: Boise, ID
Citizenship: United States
Post Office Address: 1273 N. Jullion Ave.
Boise, ID 83704
United States

* * * * *

Full name of inventor: Roger W. Lindsay
Inventor's Signature: Roger W. Lindsay
Date: 4-11-2011
Residence: Boise, ID
Citizenship: United States
Post Office Address: 4376 Falconcrest Way
Boise, ID 83716
United States

* * * * *

Full name of inventor: Krishna K. Parat
Inventor's Signature: Krishna K. Parat
Date: 4/5/2011
Residence: Palo Alto, CA
Citizenship: United States
Post Office Address: 4177 Hubbart Drive
Palo Alto, CA 94306
United States

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells		
First Named Inventor/Applicant Name:		Sanh D. Tang		
Filer:		Mark S. Matkin/Lori Tetrault		
Attorney Docket Number:		MI22-4725		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	14	52	728
Independent claims in excess of 3	1201	3	220	660
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2478

Electronic Acknowledgement Receipt

EFS ID:	9861505
Application Number:	13085083
International Application Number:	
Confirmation Number:	1403
Title of Invention:	Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	21567
Filer:	Mark S. Matkin/Lori Tetrault
Filer Authorized By:	Mark S. Matkin
Attorney Docket Number:	MI22-4725
Receipt Date:	12-APR-2011
Filing Date:	
Time Stamp:	16:22:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 2478
RAM confirmation Number	3286
Deposit Account	230925
Authorized User	MATKIN,MARK S.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		PreliminaryAmendment.pdf	327523	yes	15
			285e88778610e79621677346ed678c945810bcd		

Multipart Description/PDF files in .zip description

	Document Description	Start	End
	Preliminary Amendment	1	1
	Claims	2	14
	Applicant Arguments/Remarks Made in an Amendment	15	15

Warnings:

Information:

2		Specification.pdf	1228523	yes	30
			abc0167e651b69f9b031d2a39866e70abc53f9bd		

Multipart Description/PDF files in .zip description

	Document Description	Start	End
	Specification	1	20
	Claims	21	29
	Abstract	30	30

Warnings:

Information:

3	Drawings-only black and white line drawings	Drawings.pdf	715139	no	18
			18eeab0f69258b03a8f8e3e1ded657dae02e6a72		

Warnings:

Information:

4	Power of Attorney	PowerofAttorney.pdf	306654	no	8
			44e08b468b9407e7f34b66130cf085e884724f1d		

Warnings:

Information:

5	Oath or Declaration filed	Declaration.pdf	63227 67e9477dbd9547315e2eaa834aea6887fba b8f24	no	2
Warnings:					
Information:					
6	Fee Worksheet (PTO-875)	fee-info.pdf	37842 dd17c3c5b788919dbefdee480a54bbc4280 0042e	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2678908		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/085,083		Filing Date 04/12/2011		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$	=		X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	04/12/2011	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(i))	*	34	Minus	** 34	=	0		X \$52=	0	
Independent (37 CFR 1.16(h))	*	6	Minus	***6	=	0		X \$220=	0	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE			TOTAL ADD'L FEE	0	
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(i))	*		Minus	**	=			X \$	=	
Independent (37 CFR 1.16(h))	*		Minus	***	=			X \$	=	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE			TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/RAMONA WILSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/085,083	04/12/2011	2827	2478	MI22-4725	34	6

CONFIRMATION NO. 1403

21567

Wells St. John P.S.
601 W. 1st Street #1300
Spokane, WA 99201

FILING RECEIPT



OC000000047304471

Date Mailed: 04/25/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Sanh D. Tang, Boise, ID;
Roger W. Lindsay, Boise, ID;
Krishna K. Parat, Palo Alto, CA;

Power of Attorney: The patent practitioners associated with Customer Number 021567

Domestic Priority data as claimed by applicant

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

If Required, Foreign Filing License Granted: 04/20/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/085,083**

Projected Publication Date: 10/18/2012

Non-Publication Request: No

Early Publication Request: No

Title

Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/085,083	04/12/2011	Sanh D. Tang	MI22-4725

21567
Wells St. John P.S.
601 W. 1st Street #1300
Spokane, WA 99201

CONFIRMATION NO. 1403
POA ACCEPTANCE LETTER



Date Mailed: 04/25/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/12/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/ebekele/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/085,083			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	540		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220		
TOTAL CLAIMS (37 CFR 1.16(j))	34	minus 20 = *	14			x 52 =	728		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	6	minus 3 = *	3			x 220 =	660		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	2478		
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		x =	
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
TOTAL ADD'L FEE								TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		x =	
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
TOTAL ADD'L FEE								TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									

Substitute for form 1449A/PTO

(Use as many sheets as necessary)

Complete if Known

Application Number	13085083
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Filing Date	04-12-11
-------------	----------

First Named Inventor	Sanh D. Tang
----------------------	--------------

Art Unit	2827
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Examiner Name	Unknown
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Attorney Docket Number	MI22-4725
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Sheet	1	of	2
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[illegible][illegible]

Date	
Considered	

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786.9199) and select option 2.

Under the Paperwork reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	13085083
				Filing Date	04-12-11
				First Named Inventor	Sanh D. Tang
				Art Unit	2827
				Examiner Name	Unknown
Sheet	2	of	2	Attorney Docket Number	MI22-4725

NON PATENT LITERATURE DOCUMENTS			
Examiner initial *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	7	Katsumata et al., "Pipe-shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Cooperation for Ultra High Density Storage Devices", Toshiba Corporation, 2009 Symposium on VLSI Technology Digest of Technical Papers, pp. 136-137.	☐
	8	Komori et al., "Disturbless Flash Memory due to High Boost Efficiency on BiCS Structure and Optimal Memory Film Stack for Ultra High Density Storage Device", Center for Semiconductor Research & Development, Toshiba Corporation, IEEE, 2008, pp. 851-854.	☐
	9	Niklaus et al., "Wafer-Level 3D Integration Technology Platforms for ICs and MEMS", Research Paper, Center for Integrated Institute, Rennsselaer Polytechnic Institute (RPI).	☐
			☐
			☐
			☐
			☐
			☐
			☐
			☐
			☐

Examiner Signature		Date Considered	
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* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1. Applicants unique citation designation number. (optional) 2. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	10018248
Application Number:	13085083
International Application Number:	
Confirmation Number:	1403
Title of Invention:	Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	21567
Filer:	Mark S. Matkin/Cheryl Thompson
Filer Authorized By:	Mark S. Matkin
Attorney Docket Number:	MI22-4725
Receipt Date:	04-MAY-2011
Filing Date:	12-APR-2011
Time Stamp:	13:45:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		ids4-30-11.pdf	135908 2b832a95d24d0343fe0a497d4f49999f1ae81174	yes	4

	Multipart Description/PDF files in .zip description								
	Document Description		Start	End					
	Transmittal Letter		1	2					
	Information Disclosure Statement (IDS) Filed (SB/08)		3	4					
Warnings:									
Information:									
2	NPL Documents	niklaus.pdf	742894	no	8				
			780b2f5bbb4b9970c0180707e4716329c11f06d4						
Warnings:									
Information:									
3	NPL Documents	katsumata.pdf	199713	no	2				
			e57fc3d91230d63f62ca9c53099fdda88aa1df3b						
Warnings:									
Information:									
4	NPL Documents	komori.pdf	282664	no	4				
			3eb9f871a23ea49345aa31e3b50d13c67ed9ad2a						
Warnings:									
Information:									
Total Files Size (in bytes):			1361179						
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.									

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 13/085,083
Filing Date April 12, 2011
Confirmation No. 1403
Inventor Sanh D. Tang
Assignee Micron Technology, Inc.
Group Art Unit 2827
Examiner Unknown
Attorney's Docket No. MI22-4725
Title: ... Stack Of Horizontally Extending And Vertically Overlapping Features,
Methods Of Forming Circuitry Components, And Methods Of Forming An
Array Of Memory Cells

INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO/SB/08

The attached Form PTO/SB/08 is submitted in compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, and your attention is directed to the references listed on the attached Form PTO/SB/08. No copies of any cited U.S. patents or U.S. published applications are included herewith. Copies of all other cited art are attached. No admission is made regarding whether the submitted references are prior art.

This Information Disclosure Statement is being filed within three months of the filing date of the application or before the mailing date of a first Office Action, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 4-30-11

By: 
Mark S. Matkin
Reg. No. 32,268



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/085,083	04/12/2011	Sanh D. Tang	MI22-4725

CONFIRMATION NO. 1403

PUBLICATION NOTICE



OC000000057150413

21567
Wells St. John P.S.
601 West First Avenue
Suite 1300
Spokane, WA 99201-3828

Title:Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

Publication No.US-2012-0261722-A1

Publication Date:10/18/2012

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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13/085,083

04/12/2011

Sanh D. Tang

MI22-4725

1403

21567

7590

05/07/2014

Wells St. John P.S.

601 West First Avenue

Suite 1300

Spokane, WA 99201-3828

EXAMINER

NGUYEN, CUONG QUANG

ART UNIT

PAPER NUMBER

2811

MAIL DATE

DELIVERY MODE

05/07/2014

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/085,083	Applicant(s) TANG ET AL.	
	Examiner CUONG Q. NGUYEN	Art Unit 2811	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-41 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☐ Claim(s) _____ is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☒ Claim(s) 1-41 are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date _____ | 4) ☐ Other: _____ |

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 39-41, drawn to a semiconductor device, classified in class 257, subclass 202.
- II. Claims 1-38, drawn to a method of making a semiconductor device, classified in class 438, subclass 100+.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case unpatentability of the group I invention would not necessarily imply unpatentability of the group II invention, since the device of the group I invention could be made by processes materially different from those of group II invention, for example, forming the dummy structure the device as claimed in device claim 39 without using the sacrificial material as required in method claim 1.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

This application further contains claims directed to the following patentably distinct species as following:

Embodiment 1 described in Fig.1-10 (comprising only memory cells).

Embodiment 2 described in Fig.11-13 (comprising NAND circuitry).

Embodiment 3 described in Fig.14-17 (comprising cross-point memory cell).

The species are independent or distinct because as disclosed the different species have mutually exclusive characteristics for each identified species. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or a grouping of patentably indistinct species to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election

Art Unit: 2811

shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong Nguyen whose telephone number is (571) 272-1661. The examiner can normally be reached on 8:00 am to 5:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Lynne Gurley who can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-irect.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Cuong Q Nguyen/

Primary Examiner, Art Unit 2811

Application/Control Number: 13/085,083

Page 6

Art Unit: 2811

5/5/2014

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 13/085083
Filing Date April 12, 2011
Confirmation No. 1403
Inventor..... Sanh D. Tang
Assignee Micron Technology, Inc.
Group Art Unit 2811
Examiner Cuong Quang Nguyen
Attorney's Docket No. MI22-4725
Title:..... Stack Of Horizontally Extending And Vertically Overlapping
Features, Methods Of Forming Circuitry Components, And Methods Of
Forming An Array Of Memory Cells

RESPONSE TO MAY 7, 2014 OFFICE ACTION

To: Mail Stop Amendment
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

From: Mark S. Matkin (Tel. 509-624-4276; Fax 509-838-3424)
 Wells St. John P.S.
 601 W. First Avenue, Suite 1300
 Spokane, WA 99201-3828

AMENDMENTS

Responsive to the Office Action dated May 7, 2014, Applicant amends
and remarks as follows:

Amendments to the Claims:

1. (Original): A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion; and

removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing.

2. (Original): The method of claim 1 wherein the operative and dummy structures comprise the same material.

3. (Currently Amended): The method of claim 2 wherein the operative and dummy ~~structures~~ structures comprise a plurality of the same materials.

4. (Original): The method of claim 3 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

5. (Original): The method of claim 2 wherein the operative and dummy structures consist essentially of the same material.

6. (Original): The method of claim 1 wherein the features comprise plates.

7. (Original): The method of claim 1 wherein the operative and dummy structures comprise programmable material.

8. (Original): The method of claim 1 wherein the operative and dummy structures comprise semiconductive material.

9. (Original): The method of claim 8 wherein the semiconductive material of the operative structures comprises interconnected channels of a plurality of vertically oriented transistors.

10. (Original): The method of claim 9 wherein interconnected channels are of vertically oriented charge storage transistors.

11. (Original): The method of claim 1 wherein the operative and dummy structures comprise conductive material.

12. (Original): A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the plates in the end portion;

forming horizontally elongated openings through the structures to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures; and

removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings.

13. (Original): The method of claim 12 wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures.

14. (Original): The method of claim 12 wherein the operative and dummy structures comprise hollow cylinders.

15. (Original): The method of claim 12 wherein the operative and dummy structures comprise laterally solid pillars.

16. (Original): The method of claim 12 wherein the features comprise plates.

17. (Original): A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming primary portion openings through the features in the primary portion and forming end portion openings through the features in the in the end portion;

forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the end portion openings and forming operative structures therewith within the primary portion openings and forming dummy structures therewith within the end portion openings;

forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures; and

removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.

18. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings at the same time.

19. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings at different times.

20. (Original): The method of claim 17 comprising forming at least some of the end portion openings horizontally overlap ends of individual ones of the features.

21. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings to have the same horizontal and vertical cross sections.

22. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings to have at least one of different horizontal cross sections or different vertical cross sections.

23. (Original): The method of claim 17 wherein said at least one of conductive material, semiconductive material, and programmable material is deposited simultaneously into the primary portion openings and the end portion openings.

24. (Original): The method of claim 17 wherein the features comprise plates.

25. (Original): A method of forming an array of memory cells, comprising:

forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion, the end portion having sacrificial material-comprising stairs;

forming a plurality of first openings into the primary portion of the stack;

forming a plurality of second openings into the end portion of the stack;

simultaneously forming at least one of conductive material, semiconductive material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and forming dummy structures therewith within the second openings in the end portion;

forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings;

removing at least a portion of the sacrificial material that is laterally between the horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material;

after the removing, forming conductive material into the horizontally elongated openings and the void spaces;

removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure; and

forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion.

26. (Withdrawn): The method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel regions of a NAND string.

27. (Withdrawn): The method of claim 25 wherein the memory cells comprise cross-point memory cells and the at least one formed material comprises programmable material.

28. (Original): The method of claim 25 comprising forming the first and second openings using the same masking step.

29. (Original): The method of claim 25 comprising forming the first and second openings using different masking steps.

30. (Original): The method of claim 25 wherein the sacrificial material is dielectric.

31. (Original): The method of claim 25 wherein the sacrificial material is at least one of semiconductive and conductive.

32. (Original): The method of claim 25 wherein the features comprise plates.

33. (Withdrawn): A method of forming an array of cross-point memory cells, comprising:

forming a stack of horizontally extending and vertically overlapping dielectric features, the stack comprising a primary portion and an end portion, at least some of the dielectric features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming openings through the dielectric features in the primary portion and in the end portion;

lining the openings with first material;

lining the first material-lined openings with programmable material;

filling remaining volume of the first and programmable material-lined openings with conductive material;

forming horizontally elongated trenches through the dielectric features to form horizontally elongated and vertically overlapping dielectric lines from dielectric material of the dielectric features, the dielectric lines individually extending from the primary portion into the end portion and individually laterally about sides of both the openings in the primary and end portions;

removing at least some of sacrificial material that is elevationally between the dielectric lines in the primary and end portions laterally between the trenches selectively relative to the dielectric lines and the first material lining in the openings;

after removing at least a portion of the sacrificial material, removing at least a portion of the first material that is elevationally between the dielectric lines to expose laterally outer sidewalls of the programmable material that is elevationally between the dielectric lines; and

replacing at least a portion of the sacrificial material with conductor material that is in electrical connection with the laterally outer sidewalls of the programmable material and to comprise vertically spaced horizontal conductive lines; individual ones of the cross-point memory cells comprising crossing ones of the horizontal conductive lines in the primary portion and

conductive material in the openings in the primary portion having the programmable material there-between.

Claims 34-38 (Canceled).

39. (Withdrawn): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion; and

dummy structures extending vertically through the features in the end portion.

Claims 40 and 41 (Canceled).

REMARKS

Claim 3 is amended. Claims 1-33 and 39 are in the application for consideration.

The Examiner alleges claims 34-38, 40, and 41 are in the application. They are not.

The Examiner has required restriction under 35 U.S.C. §121 between Claims 39-41 (Group I), drawn to a semiconductor device allegedly classified in class 257, subclass 202 and Claims 1-38 (Group II), drawn to a method of making a semiconductor device allegedly classified in class 438, subclass 100+. Additionally, the Examiner identifies patentably distinct species of an Embodiment 1, Embodiment 2, and Embodiment 3. The undersigned objects to the species as either not being inclusive of all of the subject matter of Applicant's claims and/or as being directed to subject matter not claimed by Applicant. As examples, the Examiner identifies Embodiment 1 as comprising "only" memory cells whereas Applicant never uses the word "only" in a claim. Further, none of claims 1-24 is limited to memory cells.

Applicant hereby elects Group II, Embodiment 1. Claims 1-25 and 28-32 are readable thereon or are generic to multiple of the Examiner's species that include the elected species.

Examination on the merits is requested.

Respectfully submitted,

Dated: July 1, 2014

By: /Mark S. Matkin/
Mark S. Matkin
Reg. No. 32,268

Electronic Acknowledgement Receipt

EFS ID:	19478643
Application Number:	13085083
International Application Number:	
Confirmation Number:	1403
Title of Invention:	Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	21567
Filer:	Mark S. Matkin/natale king
Filer Authorized By:	Mark S. Matkin
Attorney Docket Number:	MI22-4725
Receipt Date:	02-JUL-2014
Filing Date:	12-APR-2011
Time Stamp:	14:13:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Amendment-7-2-2014.pdf	43858 8f4e31793ec583e7961b9413134cc0a29fdd7794	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Response to Election / Restriction Filed	1	1
	Claims	2	10
	Applicant Arguments/Remarks Made in an Amendment	11	11

Warnings:

Information:

Total Files Size (in bytes):	43858
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/085,083	Filing Date 04/12/2011	☐ To be Mailed
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 ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	07/02/2014	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 34	Minus	** 34	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 6	Minus	***6	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

 SLIE
 /INEZ MCMILLIAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/085,083	04/12/2011	Sanh D. Tang	MI22-4725	1403
21567	7590	08/05/2014		
Wells St. John P.S. 601 West First Avenue Suite 1300 Spokane, WA 99201-3828			EXAMINER NGUYEN, CUONG QUANG	
			ART UNIT	PAPER NUMBER
			2811	
			MAIL DATE	DELIVERY MODE
			08/05/2014	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/085,083	Applicant(s) TANG ET AL.	
	Examiner CUONG Q. NGUYEN	Art Unit 2811	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07-02-14.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-33 and 39 is/are pending in the application.
5a) Of the above claim(s) 33 and 39 is/are withdrawn from consideration.
- 6) ☒ Claim(s) 1-32 is/are allowed.
- 7) ☐ Claim(s) ____ is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 05-04-11.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group II and embodiment I, claims 1-25 and 28-32 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Allowable Subject Matter

2. Claims 1-25 and 28-32 are allowed. Non-elected claims 26-27 also allowed because these claims are depending on the allowed. The following is an examiner's statement of reasons for allowance: prior art fails to teach the following: "forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion; and removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing" (claim 1), "forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the plates in the end portion; forming horizontally elongated openings through the structures to form horizontally elongated

Art Unit: 2811

and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures; and removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings” **(claim 12)**, “forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures; and removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures” **(claim 17)**, and “after the removing, forming conductive material into the horizontally elongated openings and the void spaces; removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure; and forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion” (claim 25).

Conclusion

This application is in condition for allowance except for the following formal matters:

Non-elected claims 33 and 39 should be canceled.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 25 USPQ 74, 453 O.G. 213, (Comm'r Pat. 1935).

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong Nguyen whose telephone number is (571) 272-1661. The examiner can normally be reached on 8:00 am to 5:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

Art Unit: 2811

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

/Cuong Q Nguyen/

Primary Examiner, Art Unit 2811

8/4/2014

Notice of References Cited	Application/Control No. 13/085,083	Applicant(s)/Patent Under Reexamination TANG ET AL.	
	Examiner CUONG Q. NGUYEN	Art Unit 2811	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2012/0052674	03-2012	LEE et al.	438/591
*	B	US-2014/0106569	04-2014	OH et al.	438/703
*	C	US-2012/0003831	01-2012	Kang et al.	438/639
*	D	US-2014/0162420	06-2014	OH et al.	438/270
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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BIB DATA SHEET

CONFIRMATION NO. 1403

SERIAL NUMBER 13/085,083	FILING or 371(c) DATE 04/12/2011 RULE	CLASS 257	GROUP ART UNIT 2811	ATTORNEY DOCKET NO. M122-4725	
APPLICANTS INVENTORS Sanh D. Tang, Boise, ID; Roger W. Lindsay, Boise, ID; Krishna K. Parat, Palo Alto, CA; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 04/20/2011					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /CUONG QUANG NGUYEN/ Acknowledged Examiner's Signature	☐ Met after Allowance /CN/ Initials	STATE OR COUNTRY ID	SHEETS DRAWINGS 18	TOTAL CLAIMS 34	INDEPENDENT CLAIMS 6
ADDRESS Wells St. John P.S. 601 West First Avenue Suite 1300 Spokane, WA 99201-3828 UNITED STATES					
TITLE Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells					
FILING FEE RECEIVED 2478	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	2	((dummy adj2 (structure or cell or gate)) and (stack\$3 or vertical) and transistor and memory and (sacrificial adj2 (layer or material))).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/07/23 13:18

7/ 23/ 2014 1:19:45 PM
C:\ Users\ cnguyen4\ Documents\ EAST\ Workspaces\ EASTPush.wsp

<i>Index of Claims</i> 	Application/Control No. 13085083	Applicant(s)/Patent Under Reexamination TANG ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant											☐ CPA	☐ T.D.	☐ R.1.47
CLAIM		DATE											
Final	Original	07/23/2014											
	1	=											
	2	=											
	3	=											
	4	=											
	5	=											
	6	=											
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	30	=											
	31	=											
	32	=											
	33	N											
	34	-											
	35	-											
	36	-											

<i>Index of Claims</i> 	Application/Control No. 13085083	Applicant(s)/Patent Under Reexamination TANG ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	07/23/2014								
	37	-								
	38	-								
	39	N								

Under the Paperwork reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Sheet	1	of	2
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IPR2025-00098 Page 00124

PTO/SB/08b (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	13085083
				Filing Date	04-12-11
				First Named Inventor	Sanh D. Tang
				Art Unit	2827
				Examiner Name	Unknown
Sheet	2	of	2	Attorney Docket Number	MI22-4725

NON PATENT LITERATURE DOCUMENTS			
Examiner initial *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	7	Katsumata et al., "Pipe-shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Cooperation for Ultra High Density Storage Devices", Toshiba Corporation, 2009 Symposium on VLSI Technology Digest of Technical Papers, pp. 136-137.	☐
	8	Komori et al., "Disturbless Flash Memory due to High Boost Efficiency on BiCS Structure and Optimal Memory Film Stack for Ultra High Density Storage Device", Center for Semiconductor Research & Development, Toshiba Corporation, IEEE, 2008, pp. 851-854.	☐
	9	Niklaus et al., "Wafer-Level 3D Integration Technology Platforms for ICs and MEMS", Research Paper, Center for Integrated Institute, Rennselaer Polytechnic Institute (RPI).	☐
		un-known date	☐
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			☐
			☐
			☐

Examiner Signature	/Cuong Nguyen/	Date Considered	08-04-2014
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* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1. Applicants unique citation designation number. (optional) 2. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.N./

Search Notes 	Application/Control No. 13085083	Applicant(s)/Patent Under Reexamination TANG ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 27/11582, 11556, 11551, 1157, 11578, H01L 21/8221	07-23-14	CN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
438	216, 261, 591, 270-273, 639, E21.645	07-23-14	CN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST, EPO, JPO, inventor name (in eDAN)	07-23-14	CN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	143	(dummy adj2 (structure or cell or gate)) and (stack\$3 or vertical) and transistor and memory and (sacrificial adj2 (layer or material))	USPAT	OR	ON	2014/07/23 12:56
L2	206	(dummy adj2 (structure or cell or gate)) and (stack\$3 or vertical) and transistor and memory and (sacrificial adj2 (layer or material))	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/23 13:06

7/ 23/ 2014 1:17:04 PM
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 13/085083
Filing Date April 12, 2011
Confirmation No. 1403
Inventor..... Sanh D. Tang
Assignee Micron Technology, Inc.
Group Art Unit 2811
Examiner Cuong Quang Nguyen
Attorney's Docket No. MI22-4725
Title:..... Stack Of Horizontally Extending And Vertically Overlapping
Features, Methods Of Forming Circuitry Components, And Methods Of
Forming An Array Of Memory Cells

RESPONSE TO AUGUST 5, 2014 QUAYLE ACTION

To: Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: Mark S. Matkin (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

AMENDMENTS

Responsive to the Quayle Action dated August 5, 2014, Applicant amends and remarks as follows:

Amendments to the Specification:

Amend the “Title” as follows:

~~Stack Of Horizontally Extending And Vertically
Overlapping Features,~~ Methods Of Forming Circuitry
~~Components, And~~ Components And Methods Of
Forming An Array Of Memory Cells

Amendments to the Claims:

1. (Original): A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion; and

removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing.

2. (Original): The method of claim 1 wherein the operative and dummy structures comprise the same material.

3. (Previously Presented): The method of claim 2 wherein the operative and dummy structures comprise a plurality of the same materials.

4. (Original): The method of claim 3 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

5. (Original): The method of claim 2 wherein the operative and dummy structures consist essentially of the same material.

6. (Original): The method of claim 1 wherein the features comprise plates.

7. (Original): The method of claim 1 wherein the operative and dummy structures comprise programmable material.

8. (Original): The method of claim 1 wherein the operative and dummy structures comprise semiconductive material.

9. (Original): The method of claim 8 wherein the semiconductive material of the operative structures comprises interconnected channels of a plurality of vertically oriented transistors.

10. (Original): The method of claim 9 wherein interconnected channels are of vertically oriented charge storage transistors.

11. (Original): The method of claim 1 wherein the operative and dummy structures comprise conductive material.

12. (Original): A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the plates in the end portion;

forming horizontally elongated openings through the structures to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures; and

removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings.

13. (Original): The method of claim 12 wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures.

14. (Original): The method of claim 12 wherein the operative and dummy structures comprise hollow cylinders.

15. (Original): The method of claim 12 wherein the operative and dummy structures comprise laterally solid pillars.

16. (Original): The method of claim 12 wherein the features comprise plates.

17. (Original): A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming primary portion openings through the features in the primary portion and forming end portion openings through the features in the in the end portion;

forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the end portion openings and forming operative structures therewith within the primary portion openings and forming dummy structures therewith within the end portion openings;

forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures; and

removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.

18. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings at the same time.

19. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings at different times.

20. (Original): The method of claim 17 comprising forming at least some of the end portion openings horizontally overlap ends of individual ones of the features.

21. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings to have the same horizontal and vertical cross sections.

22. (Original): The method of claim 17 comprising forming the primary portion openings and the end portion openings to have at least one of different horizontal cross sections or different vertical cross sections.

23. (Original): The method of claim 17 wherein said at least one of conductive material, semiconductive material, and programmable material is deposited simultaneously into the primary portion openings and the end portion openings.

24. (Original): The method of claim 17 wherein the features comprise plates.

25. (Original): A method of forming an array of memory cells, comprising:

- forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion, the end portion having sacrificial material-comprising stairs;

- forming a plurality of first openings into the primary portion of the stack;

- forming a plurality of second openings into the end portion of the stack;

- simultaneously forming at least one of conductive material, semiconductive material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and forming dummy structures therewith within the second openings in the end portion;

- forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings;

- removing at least a portion of the sacrificial material that is laterally between the horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material;

- after the removing, forming conductive material into the horizontally elongated openings and the void spaces;

- removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure; and

forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion.

26. (Original): The method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel regions of a NAND string.

27. (Original): The method of claim 25 wherein the memory cells comprise cross-point memory cells and the at least one formed material comprises programmable material.

28. (Original): The method of claim 25 comprising forming the first and second openings using the same masking step.

29. (Original): The method of claim 25 comprising forming the first and second openings using different masking steps.

30. (Original): The method of claim 25 wherein the sacrificial material is dielectric.

31. (Original): The method of claim 25 wherein the sacrificial material is at least one of semiconductive and conductive.

32. (Original): The method of claim 25 wherein the features comprise plates.

Claims 33-41 (Canceled).

REMARKS

Claims 33 and 39 are canceled. Claims 1-32 are in the application for consideration.

The Title is amended to conform to the presently pending claims.

A Notice Of Allowance is requested.

Respectfully submitted,

Dated: September 15, 2015

By: /Mark S. Matkin/

Mark S. Matkin

Reg. No. 32,268

Electronic Acknowledgement Receipt

EFS ID:	20139523
Application Number:	13085083
International Application Number:	
Confirmation Number:	1403
Title of Invention:	Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	21567
Filer:	Mark S. Matkin/natalie king
Filer Authorized By:	Mark S. Matkin
Attorney Docket Number:	MI22-4725
Receipt Date:	15-SEP-2014
Filing Date:	12-APR-2011
Time Stamp:	15:28:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Amendment-9-15-2014.pdf	37189 78397a294ffe62c8b91138288e0570d3a3448218	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Response after Ex Parte Quayle Action	1	1
	Specification	2	2
	Claims	3	9
	Applicant Arguments/Remarks Made in an Amendment	10	10

Warnings:

Information:

Total Files Size (in bytes):	37189
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/085,083	Filing Date 04/12/2011	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	09/15/2014	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 32	Minus	** 34	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 6	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/BRENDA MURPHY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

21567 7590 09/23/2014
Wells St. John P.S.
601 West First Avenue
Suite 1300
Spokane, WA 99201-3828

EXAMINER

NGUYEN, CUONG QUANG

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 09/23/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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13/085,083

04/12/2011

Sanh D. Tang

MI22-4725

1403

TITLE OF INVENTION: METHODS OF FORMING FIRCUITRY COMPONENTS AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/23/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

21567 7590 09/23/2014
Wells St. John P.S.
601 West First Avenue
Suite 1300
Spokane, WA 99201-3828

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/085,083	04/12/2011	Sanh D. Tang	MI22-4725	1403

TITLE OF INVENTION: METHODS OF FORMING FIRCUTRY COMPONENTS AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/23/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, CUONG QUANG	2811	257-202000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/085,083	04/12/2011	Sanh D. Tang	MI22-4725	1403

21567 7590 09/23/2014
Wells St. John P.S.
601 West First Avenue
Suite 1300
Spokane, WA 99201-3828

EXAMINER

NGUYEN, CUONG QUANG

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 09/23/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/085,083	Applicant(s) TANG ET AL.	
	Examiner CUONG Q. NGUYEN	Art Unit 2811	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 09/15/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-32. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☐ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/CUONG Q NGUYEN/
Primary Examiner, Art Unit 2811

Issue Classification 	Application/Control No. 13085083	Applicant(s)/Patent Under Reexamination TANG ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

CPC						
Symbol					Type	Version
H01L		27	/	101	F	2013-01-01
			/			
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CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
				
				

NONE		Total Claims Allowed: 32	
(Assistant Examiner)	(Date)		
/CUONG Q NGUYEN/ Primary Examiner.Art Unit 2811	09/19/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Search Notes 	Application/Control No. 13085083	Applicant(s)/Patent Under Reexamination TANG ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 27/11582, 11556, 11551, 1157, 11578, H01L 21/8221	09-19-2014	CN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
438	216, 128,261, 591, 270-273, 639, E21.645	09-19-2014	CN

SEARCH NOTES		
Search Notes	Date	Examiner
inventor name (in eDAN)	09-19-2014	CN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
see search note		09-19-2014	CN

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<i>Index of Claims</i> 	Application/Control No. 13085083	Applicant(s)/Patent Under Reexamination TANG ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	07/23/2014	09/19/2014						
	1	=	=						
	2	=	=						
	3	=	=						
	4	=	=						
	5	=	=						
	6	=	=						
	7	=	=						
	8	=	=						
	9	=	=						
	10	=	=						
	11	=	=						
	12	=	=						
	13	=	=						
	14	=	=						
	15	=	=						
	16	=	=						
	17	=	=						
	18	=	=						
	19	=	=						
	20	=	=						
	21	=	=						
	22	=	=						
	23	=	=						
	24	=	=						
	25	=	=						
	26	=	=						
	27	=	=						
	28	=	=						
	29	=	=						
	30	=	=						
	31	=	=						
	32	=	=						
	33	N	-						
	34	-	-						
	35	-	-						
	36	-	-						

<i>Index of Claims</i> 	Application/Control No. 13085083	Applicant(s)/Patent Under Reexamination TANG ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47									
CLAIM		DATE							
Final	Original	07/23/2014	09/19/2014						
	37	-	-						
	38	-	-						
	39	N	-						

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	((circuitry adj components) and stack and (sacrificial adj material) and features and (vertical adj movement) and (end adj portion)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 09:14

9/ 19/ 2014 9:15:00 AM
C:\ Users\ cnguyen4\ Documents\ EAST\ Workspaces\ EASTPush.wsp

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	((circuitry adj components) and stack and (sacrificial adj material) and features and (vertical adj movement) and (end adj portion)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 09:14

9/ 19/ 2014 9:15:47 AM
C:\ Users\ cnguyen4\ Documents\ EAST\ Workspaces\ EASTPush.wsp



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/085,083	04/12/2011	2811	2478	MI22-4725	34	6

CONFIRMATION NO. 1403

CORRECTED FILING RECEIPT



21567
Wells St. John P.S.
601 West First Avenue
Suite 1300
Spokane, WA 99201-3828

Date Mailed: 10/30/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Sanh D. Tang, Boise, ID;
Roger W. Lindsay, Boise, ID;
Krishna K. Parat, Palo Alto, CA;

Applicant(s)

Sanh D. Tang, Boise, ID;
Roger W. Lindsay, Boise, ID;
Krishna K. Parat, Palo Alto, CA;

Power of Attorney: The patent practitioners associated with Customer Number 021567

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 04/20/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/085,083**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

METHODS OF FORMING CIRCUITRY COMPONENTS AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the **ISSUE FEE** and **PUBLICATION FEE** (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

21567 7590 09/23/2014
Wells St. John P.S.
601 West First Avenue
Suite 1300
Spokane, WA 99201-3828

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Filed electronically

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/085,083	04/12/2011	Sanh D. Tang	MI22-4725	1403

TITLE OF INVENTION: METHODS OF FORMING ~~XXXXXX~~ COMPONENTS AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS
CIRCUITRY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/23/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, CUONG QUANG	2811	257-202000

Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47, Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1. Wells St. John, P.S.

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2.

3.

ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Micron Technology, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Boise, Idaho USA

Check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

The following fee(s) are submitted:

☒ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☒ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number (enclose an extra copy of this form).

Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

TE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Mark S. Matkin/

Date December 22, 2014

Typed or printed name Mark S. Matkin

Registration No. 32268

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☒ Customer Number: **26809**

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	13/085,083

Completed by (check one):

☐ Applicant/Inventor

/Mark S. Matkin/

Signature

☒ Attorney or Agent of record 32268
 (Reg. No.)

Mark S. Matkin

Typed or printed name

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
 Statement under 37 CFR 3.73(b) is enclosed.
 (Form PTO/SB/96)

509-624-4276

Requester's telephone number

☐ Assignee recorded at Reel _____ Frame _____

December 22, 2014

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETE D FORMS TO THIS ADDRESS.

SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

IPR2025-00098 Page 00158

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal				
Application Number:		13085083		
Filing Date:		12-Apr-2011		
Title of Invention:		METHODS OF FORMING CIRCUITRY COMPONENTS AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS		
First Named Inventor/Applicant Name:		Sanh D. Tang		
Filer:		Mark S. Matkin/natalie king		
Attorney Docket Number:		MI22-4725		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	21035120
Application Number:	13085083
International Application Number:	
Confirmation Number:	1403
Title of Invention:	METHODS OF FORMING CIRCUITRY COMPONENTS AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	21567
Filer:	Mark S. Matkin/natalie king
Filer Authorized By:	Mark S. Matkin
Attorney Docket Number:	MI22-4725
Receipt Date:	22-DEC-2014
Filing Date:	12-APR-2011
Time Stamp:	14:52:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	1207
Deposit Account	230925
Authorized User	MATKIN, MARK S.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	IssueFeePayment.pdf	315488	no	2
			48187d4f23b357df676c49acbaa0a9fcee0dd363		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30434	no	2
			3ca6a4b4750ce7c3ad49a536211f5cea2f747eb8		

Warnings:

Information:

Total Files Size (in bytes):			345922
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/085,083	02/03/2015	8945996	MI22-4725	1403

21567 7590 01/14/2015
Wells St. John P.S.
601 West First Avenue
Suite 1300
Spokane, WA 99201-3828

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 967 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Sanh D. Tang, Boise, ID;
Roger W. Lindsay, Boise, ID;
Krishna K. Parat, Palo Alto, CA;

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IN UNITED STATES PATENT AND TRADEMARK OFFICE

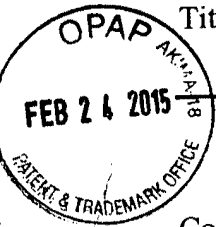
Patent No.: 8,945,996

Docket No: MI22-4725

Issue Date: February 3, 2015

Patentee: Sanh D. Tang et al.

Title: METHODS OF FORMING CIRCUITRY COMPONENTS AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS



REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
ATTN: Certificate of Correction Branch

It is requested that a Certificate of Correction be issued correcting printing errors appearing in the above-identified United States patent. Two copies of the text of the Certificate in the suggested form are enclosed.

Pursuant to 1.20(a), the examiner is authorized to charge the Certificate of Correction fee of \$100.00 to the Deposit Account No. 13-3092.

Issuance of the Certificate of Correction would neither expand nor contract the scope of the claims as properly allowed, and re-examination is not required.

Respectfully submitted,

Customer Number: 26809

A handwritten signature in black ink, appearing to read "Steven P. Arnold".

Date: February 18, 2015

By: _____

Steven P. Arnold
Reg. No. 33,354

CERTIFICATE UNDER 37 CFR § 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on this 18 day of February 2015

Julie Bergemann

Name

/Julie Bergemann/

Signature

A handwritten signature in black ink, appearing to read "Julie Bergemann".

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 8,945,996

Page 1 of 1

DATED : February 3, 2015

INVENTOR(S) : Sanh D. Tang et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 12, line 25, in Claim 17, delete "in the in the" and insert -- in the --, therefor.

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 8,945,996

Page 1 of 1

DATED : February 3, 2015

INVENTOR(S) : Sanh D. Tang et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 12, line 25, in Claim 17, delete "in the in the" and insert - - in the - -, therefor.

Notice of Fee Due

Application Number:

Date:

08945996

022515

Fees are due for the application or document date 022415 payment was not collectable for the reason indicated below.

Note: If the fee due is for any of the filing fees, the surcharge for late payment of the filing fees is now due as well.

- ☐ Insufficient payment by check or money order.
- ☐ No authorization to charge a deposit account.
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- ☐ User name not listed in deposit account _____ at _____:_____ (time).
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- ☐ Insufficient payment by credit card.
- ☐ Declined credit card _____:_____ (time).

Fee code(s) to be applied:

1811\$100

Amount in holding fee code:

1506\$1622/2622\$1206/2206\$1999\$

Total remaining due from applicant:

\$100

053013

RAM Operator ZJ



13/085,083

CNK

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sanh D. Tang et al.

Examiner: CUONG QUANG NGUYEN

Patent No.: 8,945,996

Group Art Unit: 2811

Issue Date: February 3, 2015

Docket No: MI22-4725

Title: METHODS OF FORMING CIRCUITRY COMPONENTS AND METHODS OF FORMING AN
ARRAY OF MEMORY CELLS

Commissioner for Patents
Office of Patent Publication
ATTN: Certificate of Correction Branch

We are transmitting herewith the attached:

- ☒ Authorization to charge the Certificate of Correction fee of \$100.00 to the Deposit Account No. 13-3092.
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Respectfully submitted,

Date: February 18, 2015 By: _____

Steven P. Arnold
Reg. No. 33,354

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Julie Bergemann

Name

/Julie Bergemann/

Signature

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 8,945,996 B2
APPLICATION NO. : 13/085083
DATED : February 3, 2015
INVENTOR(S) : Sanh D. Tang et al.

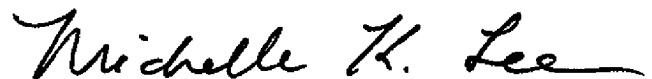
Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

In column 12, line 25, in Claim 17, delete “in the in the” and insert -- in the --, therefor.

Signed and Sealed this
Fifth Day of May, 2015



Michelle K. Lee
Director of the United States Patent and Trademark Office