

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

**YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.**

Petitioner,

v.

**MICRON TECHNOLOGY, INC.**

Patent Owner.

---

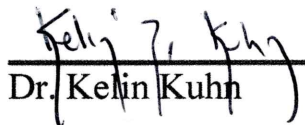
Case IPR2025-00098

U.S. Patent No. 8,945,996

---

**DECLARATION OF DR. KELIN J. KUHN IN SUPPORT  
OF PETITION FOR *INTER PARTES* REVIEW  
OF U.S. PATENT NO. 8,945,996**

Executed this 16th day of November 2024, in Gig Harbor, Washington.

  
Dr. Kelin Kuhn

## TABLE OF CONTENTS

|                                                                                          | Page      |
|------------------------------------------------------------------------------------------|-----------|
| <b>I. INTRODUCTION .....</b>                                                             | <b>1</b>  |
| <b>II. QUALIFICATIONS.....</b>                                                           | <b>4</b>  |
| <b>III. LEGAL UNDERSTANDING.....</b>                                                     | <b>10</b> |
| A. My Understanding of Claim Construction.....                                           | 10        |
| B. My Understanding of Anticipation .....                                                | 12        |
| C. My Understanding of Obviousness.....                                                  | 13        |
| <b>IV. BACKGROUND OF THE TECHNOLOGY.....</b>                                             | <b>17</b> |
| <b>V. THE '996 PATENT .....</b>                                                          | <b>20</b> |
| A. '996 Patent Overview.....                                                             | 20        |
| B. The Prosecution History.....                                                          | 21        |
| <b>VI. LEVEL OF ORDINARY SKILL IN THE ART .....</b>                                      | <b>23</b> |
| <b>VII. CLAIM CONSTRUCTION.....</b>                                                      | <b>25</b> |
| <b>VIII. GROUNDS OF UNPATENTABILITY.....</b>                                             | <b>25</b> |
| <b>IX. SPECIFIC GROUNDS FOR CHALLENGE .....</b>                                          | <b>26</b> |
| A. GROUND 1: Chae (Claims 1-4, 6-10, 12-13, 16-18, 23-26, 28, 30, 32)<br>.....           | 27        |
| 1. Overview of Chae.....                                                                 | 27        |
| 2. Invalidity of Claims 1-4, 6-10, 12-13, 16-18, 23-26, 28,<br>30, and 32 Over Chae..... | 29        |
| 1. Element [1.pre] .....                                                                 | 29        |
| 2. Element [1.a] .....                                                                   | 31        |
| 3. Element [1.b] .....                                                                   | 33        |
| 4. Element [1.c] .....                                                                   | 35        |
| 5. Claim [2].....                                                                        | 38        |
| 6. Claim [3].....                                                                        | 39        |

|                                   |    |
|-----------------------------------|----|
| 7. Claim [4].....                 | 39 |
| 8. Claim [6].....                 | 41 |
| 9. Claim [7].....                 | 41 |
| 10. Claim [8].....                | 42 |
| 11. Claim [9].....                | 43 |
| 12. Claim [10].....               | 46 |
| 13. Element [12.pre].....         | 47 |
| 14. Element [12.a] .....          | 47 |
| 15. Element [12.b] .....          | 47 |
| 16. Element [12.c] .....          | 48 |
| 17. Element [12.d] .....          | 51 |
| 18. Claim [13].....               | 53 |
| 19. Claim [16].....               | 55 |
| 20. Element [17.pre].....         | 55 |
| 21. Element [17.a] .....          | 55 |
| 22. Element [17.b] .....          | 56 |
| 23. Element [17.c] .....          | 57 |
| 24. Element [17.d].....           | 59 |
| 25. Element [17.e] .....          | 59 |
| 26. Claim [18].....               | 59 |
| 27. Claim [23].....               | 62 |
| 28. Claim [24].....               | 64 |
| 29. Element [25.pre].....         | 64 |
| 30. Element [25.a] .....          | 65 |
| 31. Elements [25.b], [25.c] ..... | 67 |
| 32. Element [25.d] .....          | 69 |
| 33. Element [25.e] .....          | 69 |
| 34. Element [25.f].....           | 70 |
| 35. Element [25.g] .....          | 72 |
| 36. Element [25.h] .....          | 74 |

|     |                                                                                        |     |
|-----|----------------------------------------------------------------------------------------|-----|
| 37. | Element [25.i].....                                                                    | 78  |
| 38. | Claim [26].....                                                                        | 79  |
| 39. | Claim [28].....                                                                        | 82  |
| 40. | Claim [30].....                                                                        | 84  |
| 41. | Claim [32].....                                                                        | 85  |
| B.  | GROUND 2: Chae in view of Kiyotoshi (Claims 18, 23, 25-26, 28, 30, 32).....            | 85  |
| 1.  | Overview of Kiyotoshi .....                                                            | 85  |
| 2.  | Invalidity of Claims 18, 23, 25-26, 28, 30, and 32 Over Chae in view of Kiyotoshi..... | 86  |
| 3.  | Motivation to Apply Kiyotoshi’s Teachings to Chae.....                                 | 89  |
| C.  | GROUND 3: Chae in view of Hwang (Claim 22) .....                                       | 93  |
| 1.  | Overview of Hwang.....                                                                 | 93  |
| 2.  | Invalidity of Claim 22 Over Chae in view of Hwang.....                                 | 94  |
| 3.  | Motivation to Apply Hwang’s Teachings to Chae .....                                    | 97  |
| D.  | GROUND 4: Chae in view of Pekny (Claims 12-13, 16).....                                | 99  |
| 1.  | Overview of Pekny .....                                                                | 99  |
| 2.  | Invalidity of Claims 12-13 and 16 Over Chae in view of Pekny .....                     | 99  |
| 3.  | Motivation to Apply Pekny’s Teachings to Chae.....                                     | 101 |
| X.  | SECONDARY CONSIDERATIONS .....                                                         | 107 |
| XI. | CONCLUSION .....                                                                       | 107 |

## I. INTRODUCTION

1. My name is Dr. Kelin J. Kuhn and I am an adjunct professor in the Materials Science and Engineering Department at Cornell University. I have been retained on behalf of Yangtze Memory Technologies Company, Ltd. (“YMTC”), to provide my opinions on certain issues related to U.S. Patent No. 8,945,996 (“the ’996 patent”) in connection with the above-captioned *inter partes* review (IPR) proceeding. In particular, I have been asked to provide my insights, analysis, and opinions regarding whether claims 1-4, 6-10, 12-13, 16-18, 22-26, 28, 30, and 32 of the ’996 patent (“Challenged Claims”) are anticipated by and/or obvious over the prior art references identified below.

2. I understand that the ’996 patent is titled “Methods of forming circuitry components and methods of forming an array of memory cells,” names as inventors Sanh D. Tang, Roger W. Lindsay, and Krishna K. Parat, and is currently owned by Micron Technology, Inc. I have considered the ’996 patent. I understand that the ’996 patent has been provided as Ex. 1001.

3. I understand that the file history of the ’996 patent has been provided as Ex. 1002. I have considered this file history, and I will refer to it as “the ’996 File History.”

4. I understand that the ’996 patent claims a priority date of April 12, 2011, the filing date of U.S. Patent Application No. 13/085,083. I have been asked

to assume that priority date for purposes of rendering my opinions in this declaration. I have not been asked to opine on whether the claims of the '996 patent are entitled to this priority date, and do not provide any opinion on that subject.

5. My analysis and conclusions set forth in this declaration are based on my educational background and experiences in the field (see Section II). Before April 12, 2011, my level of skill in the art was at least that of a person of ordinary skill. I am qualified to opine concerning what a person of ordinary skill in the art would have known and understood at the time of the '996 patent's purported invention. My analysis and conclusions herein are from the perspective of a person of ordinary skill in the art as of April 12, 2011.

6. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this art during the time before the earliest claimed priority date for the '996 patent; my own knowledge and experiences gained from my work experience in the field of the '996 patent and related disciplines; and my experience in working with others involved in this field and related disciplines.

7. I have considered the following non-exhaustive list of references in preparing my declaration. I have been instructed to assume that each of these references qualifies as prior art.

- **U.S. Patent Application Publication No. U.S. 2010/0133598** to Soodoo Chae and Myoungbum Lee (“Chae”), titled “Nonvolatile memory device and method for fabricating the same” filed on December 3, 2009, and published on June 3, 2010. I understand that a copy of this reference has been designated as Exhibit 1004.
- **U.S. Patent Application Publication No. U.S. 2011/0156132** to Masahiro Kiyotoshi (“Kiyotoshi”), titled “Nonvolatile semiconductor memory device” filed on May 20, 2010, and published on June 30, 2011. I understand that a copy of this reference has been designated as Exhibit 1005.
- **U.S. Patent Application Publication No. U.S. 2011/0151667** to Sung-Min Hwang, Hansoo Kim, Wonseok Cho, and Jaehoon Jang (“Hwang”), titled “Methods of Manufacturing Three-Dimensional Semiconductor Devices and Related Devices” filed on December 8, 2010, and published on June 23, 2011. I understand that a copy of this reference has been designated as Exhibit 1006.
- **U.S. Patent No. U.S. 7,906,818** to Theodore T. Pekny (“Pekny”), titled “Memory array with a pair of memory-cell strings to a single conductive pillar” filed on March 13, 2008, published on September 17, 2009, and issued on March 15, 2011. I understand that a copy of this reference has been designated as Exhibit 1007.

8. I understand that there is a pending district court litigation between Petitioner and Micron Technology, Inc. (“YMTC Litigation”) involving the ’996 patent.

9. I am being compensated by YMTC at my standard hourly consulting rate of \$600 for my time on this matter. My compensation is not dependent on the

outcome of this proceeding or any other proceeding between the parties.

10. As set forth herein, I have concluded that each of the Challenged Claims is anticipated and/or rendered obvious by the prior art based on the references described below and as described herein. In forming my opinions, I relied on the documents cited in this declaration and the documents identified in the attached Appendix B. These documents comprise patents, file histories, printed publications, and other related documents. As discussed below, each document is a type that experts in my field would have reasonably relied upon when forming their opinions. Further, experts in my field would have had access to each document either through the applicable patent offices and/or well-known libraries, conferences, or publications in the field. My opinions are also based upon my personal and professional experience.

## **II. QUALIFICATIONS**

11. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

12. I am qualified by education and experience to testify as an expert in the field of manufacturing nonvolatile memory devices. Additionally, the following overview of my background pertains to my qualifications for providing expert testimony in this matter. I am over the age of 18 and am competent to write this

declaration. I have personal knowledge, or have developed knowledge, of these technologies based upon education, training, or experience of the matters set forth herein.

13. I received my B.S., magna cum laude, in Electrical Engineering from the University of Washington, Seattle in 1980, and received an M.S. and a Ph.D. in Electrical Engineering from Stanford University in 1985. I undertook post-doctoral work at Stanford from 1985 to 1987.

14. I am presently retired from industry. However, I still periodically engage in engineering projects for select clients and have a small business (Confluence Technology Services) to support that activity.

15. I am also currently an adjunct professor of Materials Science and Engineering at Cornell University, where my research interests are in the areas of quantum materials, post-CMOS technology, and spintronics.

16. For nearly a decade, beginning in 1987, I held faculty positions at the University of Washington, Seattle, beginning as a Research Assistant Professor in Material Science and Engineering, then as Assistant Professor in Electrical and Computer Engineering, and finally as a tenured Associate Professor of Electrical and Computer Engineering. During this period, I worked in III-V molecular beam epitaxy and optoelectronics, and was awarded the University's highest accolade for a faculty member, the Distinguished Teaching Award, in 1995.

17. In 1997, I joined Intel Corporation (“Intel”) at the Aloha Campus in Oregon as a Senior Process Engineer. I focused on front-end integration on the Intel 0.35 $\mu$ m process technology. In this role, I was responsible for the silicide section of the process flow, interaction with the reliability community, and integration on the CMOS camera chip project.

18. In 1999, I was transferred to Portland Technology Development at Ronler Acres, Oregon, as a Senior Process Engineer. I worked on front-end integration on the 130 nm CMOS generation. In this role, I was responsible for the isolation section of the process flow as well as integration of Optical Proximity Correction technologies into 130 nm.

19. In 2001, I advanced to the title of Principal Engineer. In 2002, I was promoted to the role of Process Program Manager for Intel’s 90 nm communications process technology. Over a three-year period, my team developed a derivative analog/RF technology (including a SiGe bipolar junction transistor (“BJT”)) on top of Intel’s premium 90 nm microprocessor process.

20. In 2004, I advanced to the title of Senior Principal Engineer and was promoted to the role of Device Technology Manager of the pathfinding team at Intel that was responsible for the high-k metal-gate transistor architecture of Intel’s 45 nm microprocessor processor technology. I received an Intel Achievement Award in 2006 for my work on the high-k metal gate.

21. In 2007, I achieved the title of Intel Fellow and became Director of Advanced Device Technology. Fellow is the highest level of technical achievement within Intel, with approximately 50 Fellows among approximately 100,000 total employees. My work evolved to a strategic role in overseeing the transition of advanced device technologies from research into development. In this role, I played an active part in the transfer of transistor technology for the 32 nm node, 22 nm node, and 14 nm node (the last two nodes involving Intel's FinFET device). I received a second Intel achievement award in 2008 for my work on Intel's FinFET device.

22. In 2009, my title remained the same, but my role transitioned from development (in Portland Technology Development, at Ronler Acres) to research (in the Components Research Group, still at Ronler Acres). From 2009 until my retirement from Intel in 2014, I researched advanced device architectures for Intel processes in the five-to-ten year time frame.

23. While much of my later work at Intel still remains confidential, certain aspects of my work during this period are featured in my book CMOS And Beyond: Logic Switches for Terascale Integrated Circuits (Co-Editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015), as well as in my paper "Considerations for Ultimate CMOS Scaling" (IEEE Trans. on Elec. Dev., Vol. 59, No. 7, 2012), winner of the 2013 Paul Rappaport Award.

24. Since my retirement in 2014, my consulting work has included a variety of semiconductor related projects. While the detailed technical content is, of course, protected by client confidentiality, these projects include, FinFETs, vertical power transistors, solar cells, conventional (planar) MOS, and flash.

25. I am the author of more than 100 technical papers in electronics and photonics. I am currently the Associate Editor in Chief (AEiC) of IEEE Electron Device Letters, having served as an editor since 2015, and as AEiC since 2024.

26. A few of my other representative journal publications include: “Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results,” (Symposium on VLSI Technology, 2012); “Process Technology Variation,” (IEEE Transactions on Electron Devices, Vol. 58, No. 8, 2011); “A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging,” (2007 IEEE International Electron Devices Meeting); and “Comparison of Junctionless and Conventional Trigate Transistors With L<sub>g</sub> Down to 26 nm,” (IEEE Electron Device Letters, Vol. 32, No. 9, 2011).

27. A few representative book chapters include, “The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8. Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS

Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616).

28. I am an inventor on approximately 80 granted U.S. patents in the field of semiconductor technology.

29. A few of my other relevant honors include being a Fellow at the Institute of Electrical and Electronics Engineers (“IEEE”), a recipient of the IEEE Frederik Philips Award (2016), a recipient of the IEEE Paul Rappaport Award (2013), the recipient of eleven Intel Divisional Awards, and election to the National Academy of Engineering (2023). Earlier in my career, I received the NSF Presidential Young Investigator Award.

30. As specifically relevant to this project, I want to highlight the 3’D gate-last vertical gate-all-around (GAA) devices and the 3’D vertical GAA arrays that are discussed at some length in “Considerations for Ultimate CMOS Scaling” (see Fig. 15 in particular). I also want to highlight on-going proprietary and confidential work, in the matter of Silicon Storage Technology, Inc. vs. Taiwan Semiconductor Manufacturing Company involving flash.

31. Attached as Appendix A to this report is a current copy of my curriculum vitae, which outlines my academic, professional and experiential qualifications in the semiconductor and integrated circuit industries, as well as a list of publications I have authored and co-authored and presentations I have given.

### **III. LEGAL UNDERSTANDING**

32. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

33. In formulating my opinions, I have been informed of certain legal understandings relevant to my opinions. In formulating my opinions, I have relied on the legal understandings I have been provided with as set forth in this declaration.

34. I have been informed that in *inter partes* review proceedings, invalidity must be shown under a preponderance of the evidence standard.

#### **A. My Understanding of Claim Construction**

35. I have been informed that patent claims are construed from the viewpoint of a person of ordinary skill in the art of the patent at the time of the invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a person of ordinary skill in the art in the relevant time period (i.e., at the time of the purported invention, or the so called “effective filing date” of the patent application), after reviewing the patent claim language, the specification, and the prosecution history (i.e., the intrinsic record).

36. I have further been informed that a person of ordinary skill in the art must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner's rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or clearly and unambiguously disavowing claim coverage.

37. In interpreting the meaning of the claim language, I understand that a person of ordinary skill in the art may also consider "extrinsic" evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of ordinary skill in the art at the time of the claimed invention. For example, this can be useful for a technical term whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts

or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

**B. My Understanding of Anticipation**

38. I understand that a patent claim is invalid as “anticipated” if all the limitations of the claim are present, either expressly or inherently, in a single prior art publication or patent.

39. I also understand that a prior art reference can disclose a claimed feature because the feature is expressly described or because the feature is inherent in the disclosure. I understand that something is inherent in a prior art reference if the missing descriptive matter must necessarily be present, not merely probably or possibly present, and it would be so recognized by a person of ordinary skill in the art as of the priority date of the patent. I understand that it is acceptable to examine evidence outside of the prior art reference (i.e., extrinsic evidence) in determining whether a feature, while not expressly discussed in the reference, is necessarily present in it.

40. I have further been informed that where a reference discloses multiple embodiments, the reference should not be limited to a preferred embodiment. Instead, each disclosed embodiment may anticipate.

41. Moreover, I have been informed that as part of an anticipation analysis, it is proper to take into account not only specific teachings of the

reference, but also the inferences that one skilled in the art would reasonably be expected to draw therefrom. A reference can anticipate a claim even if it does not expressly spell out all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would at once envisage the claimed arrangement or combination.

### **C. My Understanding of Obviousness**

42. I understand that a claim may be invalid if the subject matter described by the claim as a whole would have been obvious to a hypothetical person of ordinary skill in the art in view of a prior art reference or in view of a combination of references at the time the claimed invention was made. Therefore, I understand that obviousness is determined from the perspective of a hypothetical person of ordinary skill in the art and that the asserted claims of the patent should be read from the point of view of such a person at the time the claimed invention was made. I further understand that a hypothetical person of ordinary skill in the art is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent in suit.

43. I have been informed that there are two criteria for determining whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee's endeavor, whether the reference

still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee's attention in considering their problem.

44. I have also been advised that an analysis of whether a claimed invention would have been obvious should be considered in light of the scope and content of the prior art, the differences (if any) between the prior art and the claimed invention, and the level of ordinary skill in the pertinent art involved. I understand as well that a prior art reference should be viewed as a whole.

45. I have also been advised that in considering whether a claimed invention would have been obvious over a combination of prior art references, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the marketplace, and/or the background knowledge possessed by a person of ordinary skill in the art. I understand that other principles may be relied on in evaluating

whether a claimed invention would have been obvious, and that these principles include the following:

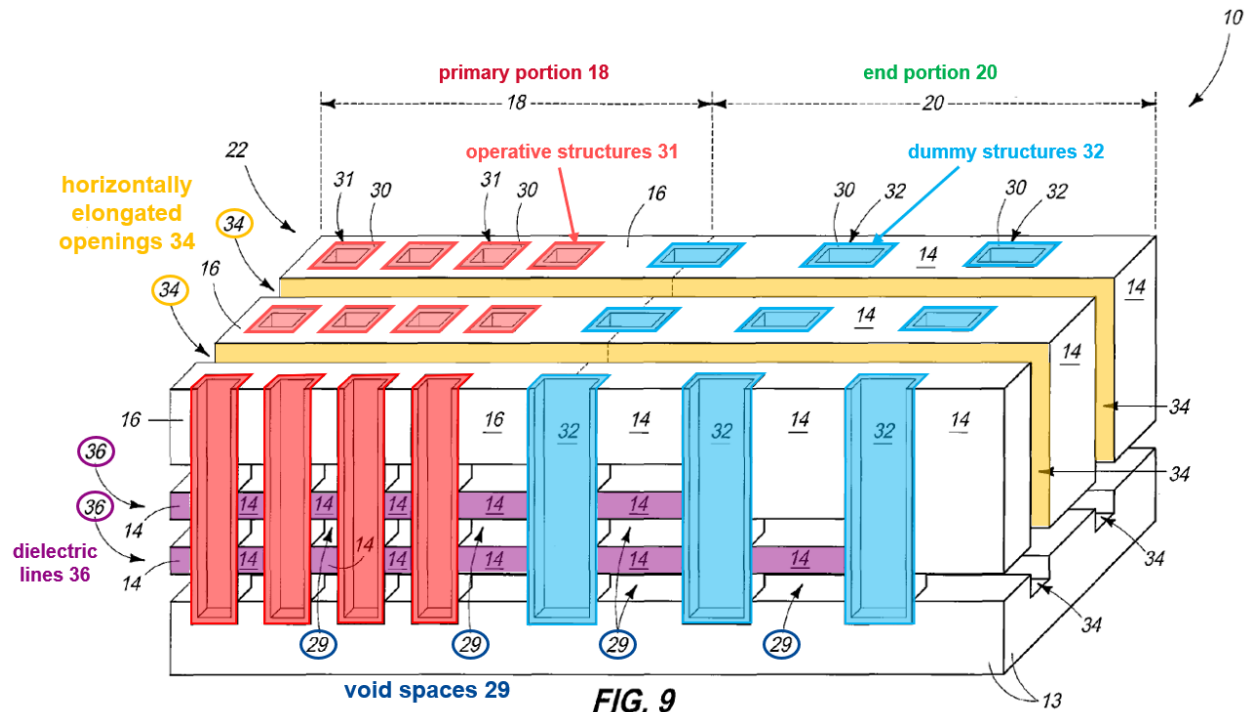
- A combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results;
- When a device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a person of ordinary skill can implement a predictable variation, the variation is likely obvious;
- If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond their skill;
- An explicit or implicit teaching, suggestion, or motivation to combine two prior art references to form the claimed combination may demonstrate obviousness, but proof of obviousness does not depend on or require showing a teaching, suggestion, or motivation to combine;
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the particular motivation nor the avowed purpose of the named inventor controls whether the claim is obvious;
- One of the ways in which a patent's subject can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;
- Any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed;
- "Common sense" teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle;

- A person of ordinary skill in the art is also a person of ordinary creativity, and is not an automaton;
- A patent claim can be proved obvious by showing that the claimed combination of elements was “obvious to try,” particularly when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions such that a person of ordinary skill in the art would have had good reason to pursue the known options within his or her technical grasp; and
- One should be cautious of using hindsight in evaluating whether a claimed invention would have been obvious.

46. I further understand that, in making a determination as to whether the claimed invention would have been obvious to a person of ordinary skill, the Board may consider certain objective factors if they are present, such as: commercial success of products practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. These factors are generally referred to as “secondary considerations” or “objective indicia” of nonobviousness. I understand, however, that for such objective evidence to be relevant to the obviousness of a claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence, and that this nexus must be based on a novel element of the claim rather than something in the prior art. I also understand that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (such as motivation to combine with predictable results) that is sufficiently strong.

#### IV. BACKGROUND OF THE TECHNOLOGY

47. As I discuss in Section V, the claims of the '996 patent and its specification are generally directed to a method of forming an array of memory cells. '996 patent, 1:7-10. The method includes forming a **stack of “features,”** such as **dielectric “plates”** in a **primary portion** and an **end portion**, and then forming **operative structures** and **inoperative “dummy” structures** through the **stack** in the **primary** and **end portions**, respectively. '996 patent, 4:37-52, 6:18-31; cl. 1. Then, sacrificial material between the **dielectric layers** is removed, during which process the **“dummy” structures** support the features from vertical movement in the end portion during removal. '996 patent, 6:53-56, 7:19-22; cl. 1. As part of this process, **“horizontally elongated openings”** are formed through the **dielectric layers** to form **“horizontally elongated and vertically overlapping lines”** from the dielectric material. '996 patent, 6:39-43, 6:53-56, cl. 12.

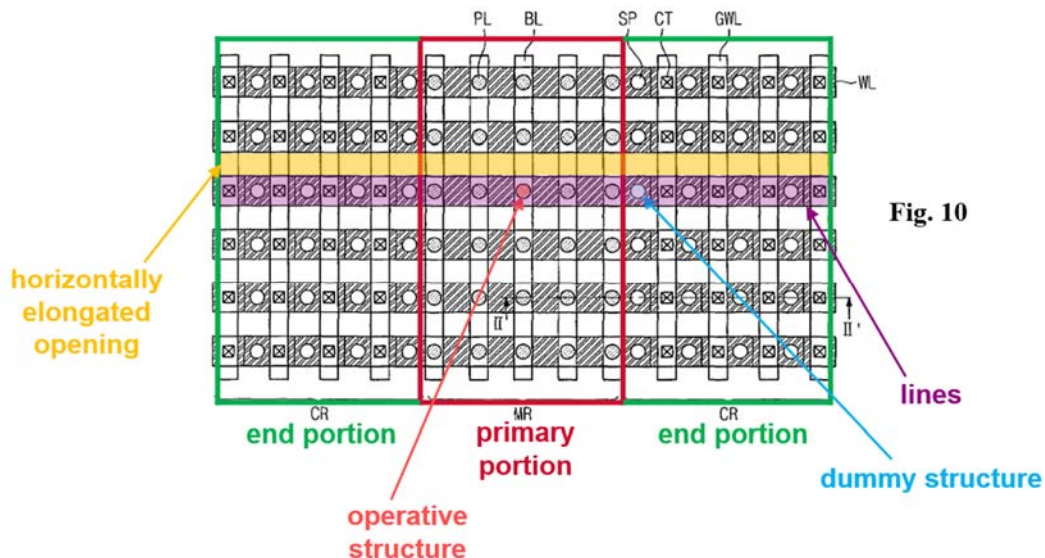
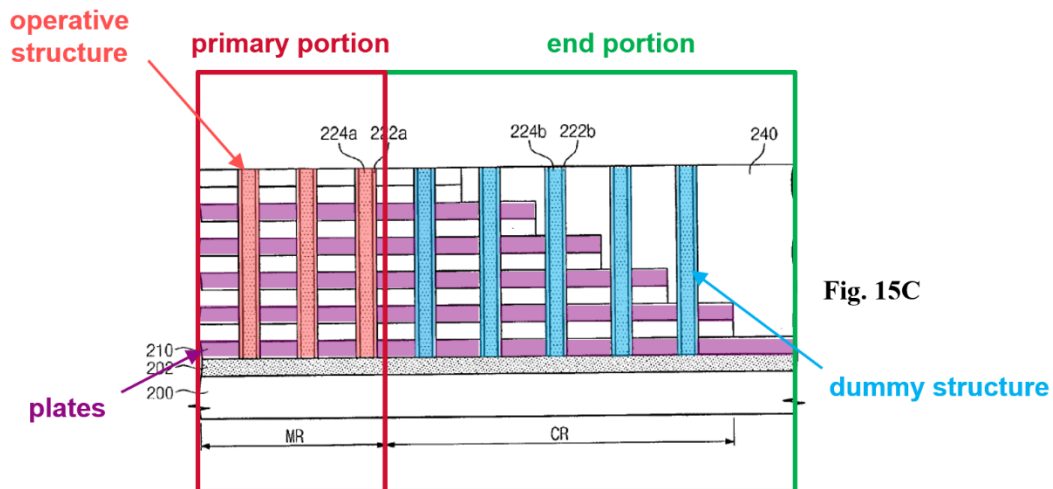


'996, Fig. 9 (annotated).

48. Based on my experience in the field, however, such a process of fabricating three-dimensional memory devices were well known in the art prior to the '996 patent's priority date.

49. For example, Chae discloses a method of forming a nonvolatile memory device. The method includes forming a **stack of dielectric layers** in a **"memory cell region"** (i.e., a primary portion) and a **"contact region"** (i.e., an end portion) and then forming **"active pillars"** (i.e., operative structures) and **"supporters"** (i.e., dummy structures) through the **stack of dielectric layers** in the **"memory cell region"** and **"contact region,"** respectively. Chae, [0116]. Then, dielectric layers between the **stack of dielectric layers** are removed, during which

process the “**supporters**” “prevent” the layers “from collapsing or getting near to each other during the removing.” Chae, [0129]. Chae also discloses, as part of this process, the “plate-shaped” layers are then “patterned to form **line-shaped stack structures**,” thereby forming **elongated openings** through the stack. Chae, [0116], [0129].



Chae, Figures 15C (cross-section view) (annotated) and 10 (top down view) (annotated).

## V. THE '996 PATENT

### A. '996 Patent Overview

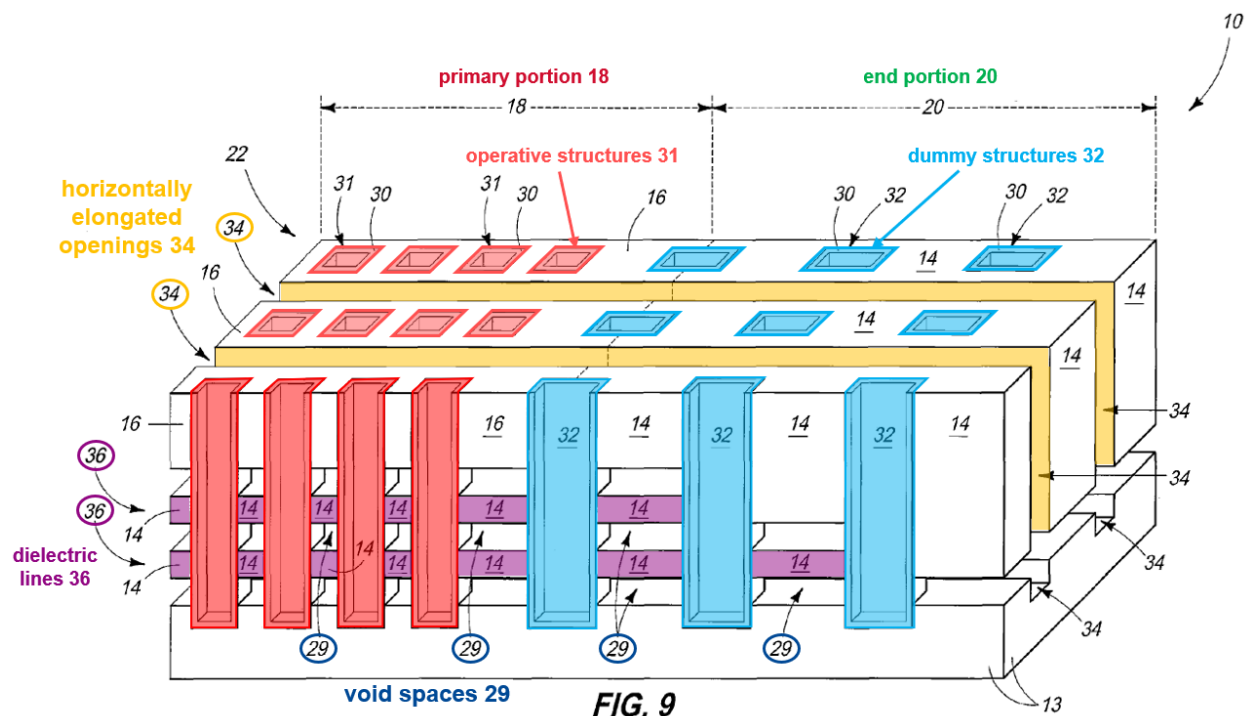
50. The '996 patent describes a method of forming circuitry components and an array of memory cells. '996, 1:7-10.

51. The '996 patent's method includes forming a vertical stack of “features (*e.g.*, plates)” such as “**dielectric material 14**” and “**sacrificial material 12**” horizontally extending across a “**primary portion 18**” and an “**end portion 20.**” '996, 3:65-67, 4:28-39. The “**end portion 20**” is formed with a “stair step-like construction” where the features “extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion.” '996, 4:28-46.

52. The '996 patent forms “primary portion openings” and “end portion openings” in the primary portion and the end portion, respectively, using a masking process. '996, 5:8-36. Then, by depositing “programmable material 30” followed by “conductive material 64” into “primary portion openings 25” and “end portion openings 27,” “**operative structures 31**” and “**dummy structures 32**” are formed, respectively. '996, 5:40-42, 6:18-23, 8:35-39.

53. The '996 patent also describes that the stacked features are patterned with “**horizontally elongated openings 34**” which extend from the “**primary portion 18**” into the “**end portion 20**” to form **lines** from the material of the plates. '996, 6:39-60. This exposes the sides of **sacrificial material 12** and

**dielectric lines 36.** '996, 6:39-60. Then, **sacrificial material 12** is “removed from being laterally between horizontally elongated openings 34,” leading to **“void spaces 29”** being formed vertically between **dielectric lines 36.** '996, 6:57-59. In the process of removing the **“sacrificial material 12,” “dummy structures 32”** provide support for the features so that they are prevented “from vertical movement in the end portion.” '996, 7:19-22, 30-35. As a result, “vertically spaced horizontal conductive lines 42 within the void spaces” are formed. '996, 7:39-47.



'996, Fig. 9.

## B. The Prosecution History

54. The prosecution of the '996 patent did not involve any rejections of

claims over prior art. The Examiner issued a restriction requirement, requiring the Applicant to elect a subset of claims, and the elected claims were allowed. '996FH, 92-98, 113-118, 141-143. The Examiner's reason for allowance was that the prior art of record did not teach the following claim limitations:

Claim 1:

[1.b] ("forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion")

[1.c] ("forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion")

Claim 12:

[12.b] ("forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion")

[12.c] ("forming horizontally elongated openings through the structures to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures")

[12.d] ("removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings")

Claim 17:

[17.d] ("forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures")

[17.e] ("removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines,

the operative structures, and the dummy structures”)

Claim 25:

[25.g] (“after the removing, forming conductive material into the horizontally elongated openings and the void spaces”)

[25.h] (“removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure”)

[25.i] (“forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion”)

’996FH, 115-116.

## **VI. LEVEL OF ORDINARY SKILL IN THE ART**

55. In rendering the opinions set forth in this declaration, I was asked to consider the patent claims and the prior art through the eyes of a person having ordinary skill in the art at the time of the alleged invention. I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field, the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a person having ordinary skill in the art is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors

above. I understand that a person having ordinary skill in the art would also have knowledge from the teachings of the prior art including the art cited below.

56. I have been asked to assume the Claims are entitled to the April 12, 2011 filing date of Application No. 13/085,083 for the purposes of this declaration only.

57. Upon consideration of the relevant factors listed above, in my opinion, on or before the priority date, a person of ordinary skill in the art, at the time the application that matured into the '996 patent was filed, would have had a Bachelor's degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. A higher level of education might make up for less experience, and vice versa.

58. Well before April 12, 2011, my level of skill in the art was at least that of a person having ordinary skill. I am qualified to opine concerning what a person having ordinary skill in the art would have known and understood at the time of the '903 patent's purported invention. My analysis and conclusions herein are from the perspective of a person having ordinary skill in the art as of April 12, 2011. A different priority date would not change my opinions as long as the identified prior art were still prior art.

## VII. CLAIM CONSTRUCTION

59. I have been instructed that the Challenged Claims 1-4, 6-10, 12-13, 16-18, 22-26, 28, 30, and 32 of the '996 patent are to be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of the alleged invention in light of the specification and the prosecution history pertaining to the patent; except that for the term “dummy structure,” I have been asked to assume it means “electrically inoperable structure that mimics a physical property of an operative structure.” I have followed these principles in my analysis set forth in this document. I reserve the right to supplement my opinions in this declaration to the extent that any parties later propose claim constructions for any claim terms in the '903 patent.

## VIII. GROUNDS OF UNPATENTABILITY

60. As I explain above in Section IV, the method of forming a memory device claimed in the Challenged Claims was well-known in the art.

61. In this section, I will explain why the teachings or combinations of teachings from the following references anticipate and/or render obvious each of the Challenged Claims:

| Name      | Ex.  | Publication/<br>Patent No. | Filed     |
|-----------|------|----------------------------|-----------|
| Chae      | 1004 | US2010/0133598             | 12/3/2009 |
| Kiyotoshi | 1005 | US2011/0156132             | 5/20/2010 |
| Hwang     | 1006 | US2011/0151667             | 12/8/2010 |

| Name  | Ex.  | Publication/<br>Patent No. | Filed     |
|-------|------|----------------------------|-----------|
| Pekny | 1007 | US7,906,818                | 3/13/2008 |

I have been instructed to assume that each of these references qualifies as prior art.

62. As I explain below, the Challenged Claims are invalid based upon the following prior art grounds:

- **Ground 1:** Challenged Claims 1-4, 6-10, 12-13, 16-18, 23-26, 28, 30, and 32 of the '996 patent are anticipated and at least rendered obvious by Chae.
- **Ground 2:** Challenged Claims 1-4, 18, 23, 25-26, 28, 30, and 32 of the '996 patent are rendered obvious by Chae in view of Kiyotoshi.
- **Ground 3:** Challenged Claim 22 of the '996 patent is rendered obvious by Chae in view of Hwang.
- **Ground 4:** Challenged Claims 12-13 and 16 of the '996 patent are rendered obvious by Chae in view of Pekny.

## IX. SPECIFIC GROUNDS FOR CHALLENGE

63. It is my opinion that Challenged Claims 1-4, 6-10, 12-13, 16-18, 22-26, 28, 30, 32 of the '996 patent are unpatentable as explained below. As I explain above in Section IV, although the '996 patent purports to have invented a method of forming an array of memory cells, such methods were well-known in the art. As described below, the cited prior art provides these teachings.

64. In this section, I explain why claims 1-4, 6-10, 12-13, 16-18, 23-26, 28, 30, and 32 of the '996 patent are anticipated and at least rendered obvious by the teachings of Chae (Ex. 1004), why claims 1-4, 18, 23, 25-26, 28, 30, and 32 are

rendered obvious by the teachings of Chae in view of Kiyotoshi (Ex. 1005), why claim 22 is rendered obvious by the teachings of Chae in view of Hwang (Ex. 1006), and why claims 12-13 and 16 are rendered obvious by the teachings of Chae in view of Pekny (Ex. 1007).

65. I note that, in this discussion, I may focus on the particular language in specific claims, but it should be understood that my analysis applies to the corresponding limitations of all claims containing identical or substantially identical language.

**A. GROUND 1: Chae (Claims 1-4, 6-10, 12-13, 16-18, 23-26, 28, 30, 32)**

**1. Overview of Chae**

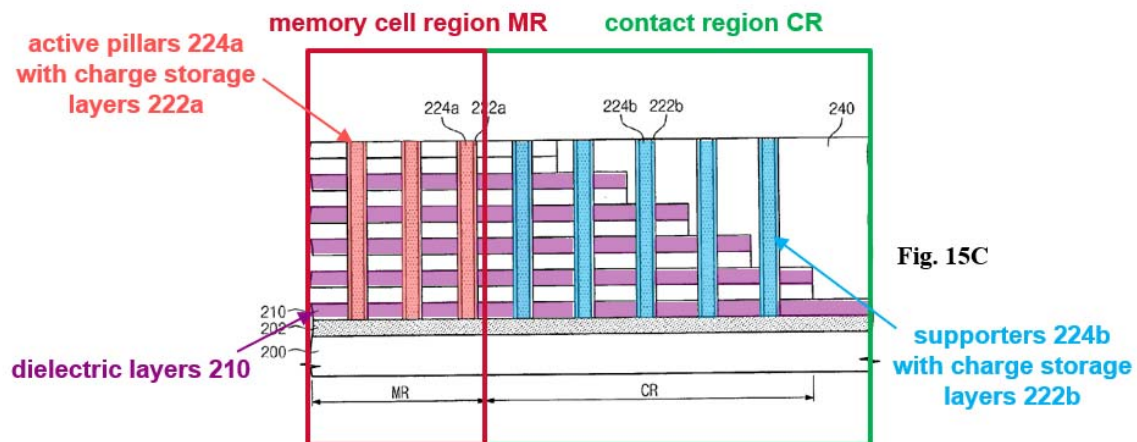
66. Chae is directed to a “method for manufacturing” “nonvolatile memory devices.” Chae, [0002].

67. Chae teaches forming a “plate-shaped stack” of “**first and second dielectric layers 210 and 215**” horizontally extending “across a **memory cell region MR** and a **contact region CR**.” Chae, [0123]. The “stack” in the “**contact region CR**” is “patterned in a stair shape” such that “the stack height of the first and second dielectric layers 210 and 215 decreases toward the edge.” *Id.*, [0124].

68. Chae also teaches that through “a photolithography process,” “**channel holes**” and “**dummy holes**” are formed in the “**memory cell region MR**” and “**contact region CR**,” respectively. Chae, [0127]. “Thereafter, charge

storage layers 222a and 222b are formed at the sidewalls of the **dummy holes** and the **channel holes**,” and the resulting structure is “filled with semiconductor material to form **active pillars 224a** and **supporters 224b**.” *Id.*, [0128]. Chae’s “**supporters 224b**” are electrically inoperable “[b]ecause a conductive pattern such as the global word line 275 or the bit line 270 is not formed on the supporters 224b.” *Id.*, [0134].

69. Chae teaches that the “stack” is subsequently “patterned to form line-shaped stack structures,” thereby forming **horizontally elongated openings** through the stack to “expose[]” the “sidewalls of the **first and second dielectric layers 210 and 215**.” Chae, [0129]. Thereafter, by removing the “**second dielectric layers 215**,” “empty space” is formed “between the **first dielectric layers 210**.” *Id.*, [0129]. The **first dielectric layers 210** are prevented from collapsing, because “**first dielectric layers 210** spaced apart from each other may be supported by...the **supporters 224b** of the **contact region CR**.” *Id.*, [0129].



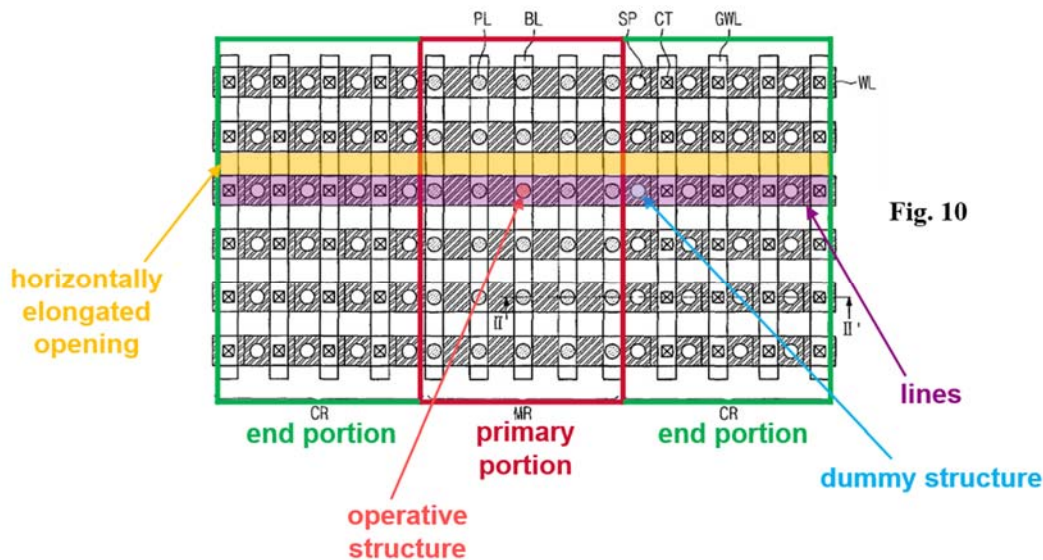


Fig. 10

Chae, Figures 15C (cross-section view) and 10 (top down view).

## 2. Invalidity of Claims 1-4, 6-10, 12-13, 16-18, 23-26, 28, 30, and 32 Over Chae

70. As I discuss below, Claims 1-4, 6-10, 12-13, 16-18, 23-26, 28, 30, and 32 are anticipated and at least rendered obvious by Chae. The following discussion identifies example disclosures followed by bulleted excerpts that each disclose Claims 1-4, 6-10, 12-13, 16-18, 23-26, 28, 30, and 32.

### 1. Element [1.pre]

71. Element [1.pre] recites “A method of forming circuitry components, comprising.” This element is met by Chae.

72. To the extent the preamble is limiting, Chae discloses a method of forming circuitry components (*e.g.*, “method for manufacturing” “nonvolatile memory devices”). *See, e.g.*, Chae:

- [0002] (“The present inventive concept relates to ***nonvolatile memory devices and methods for fabricating the same***, and more particularly, to three-dimensional nonvolatile memory devices capable of reducing the resistance of gate electrodes and preventing process defects, and methods for fabricating the same.”)
- [0007] (“Embodiments of the inventive concept provide three-dimensional nonvolatile memory devices capable of reducing the resistance of gate electrodes, and methods for fabricating the same.”)
- [0017] (“FIG. 1 is ***a circuit diagram of a nonvolatile memory device*** according to exemplary embodiments of the inventive concept.”)
- [0030] (“FIGS. 13A to 13G are sectional views illustrating ***a method for fabricating the nonvolatile memory devices*** according to the first and fourth exemplary embodiments of the inventive concept.”)
- [0031] (“FIGS. 14A to 14F are sectional views illustrating ***a method for fabricating the nonvolatile memory devices*** according to the second and fifth exemplary embodiments of the inventive concept.”)
- [0032] (“FIGS. 15A to 15E are sectional views illustrating ***another method for fabricating the nonvolatile memory devices*** according to the second and fifth exemplary embodiments of the inventive concept.”)
- [0033] (“FIGS. 16A to 16E are sectional views illustrating ***a method for fabricating the nonvolatile memory devices*** according to the third and sixth exemplary embodiments of the inventive concept.”)
- [0082] (“Hereinafter, ***methods for fabricating nonvolatile memory devices*** according to exemplary embodiments of the inventive concept will be described in detail.”)
- [0083] (“***A method for fabricating the nonvolatile memory devices*** according to the first and fourth exemplary embodiments of the inventive concept will be described below in detail with reference to FIGS. 13A to 13G.”)
- [0084] (“FIGS. 13A to 13G are sectional views illustrating ***a method for fabricating the nonvolatile memory devices*** according to the first and fourth exemplary embodiments of the inventive concept. In ***the method***

*for fabricating the nonvolatile memory devices* according to the first and fourth exemplary embodiments, the planar structure will be described with reference to FIG. 2A.”)

73. **Chae** discloses “nonvolatile memory devices and methods for fabricating the same.” Chae, Abstract.

## **2. Element [1.a]**

74. **Element [1.a]** recites “**forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion.**” This element is met by Chae.

75. Chae discloses forming a stack of horizontally extending and vertically overlapping features (*e.g.*, “first dielectric layers 210...stacked on a semiconductor substrate”), the stack comprising a primary portion (*e.g.*, “memory cell region MR”) and an end portion (*e.g.*, “contact region CR”), at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion (*e.g.*, “the first and second dielectric layers 210 and 215 stacked on the contact region CR are patterned in a stair shape”). *See, e.g.*, Chae:

- Fig. 15A (annotated)

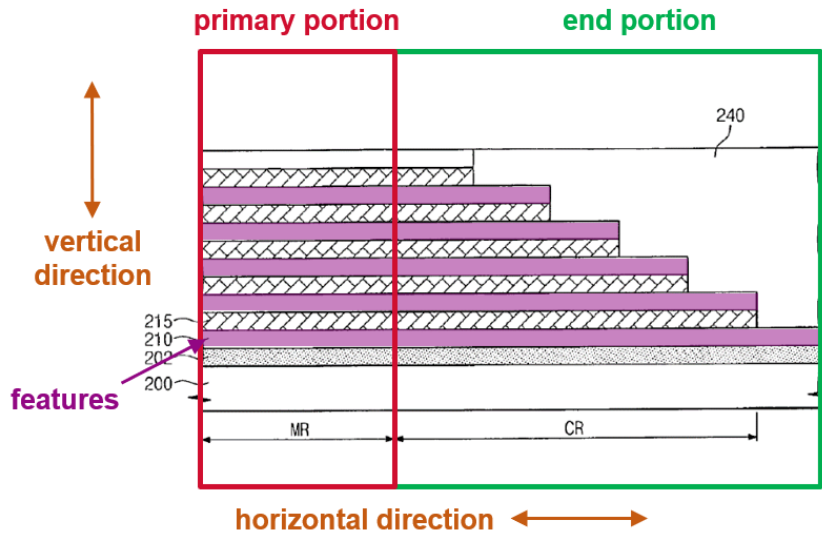


Fig. 15A

- [0123] (“Referring to FIG. 15A, first and second dielectric layers 210 and 215 with different etch selectivity are alternately stacked on a semiconductor substrate 200, and a plate-shaped stack structure is formed across a memory cell region MR and a contact region CR. That is, the sidewalls of the stacked first and second dielectric layers 210 and 215 are aligned.”)
- [0124] (“In the plate-shaped stack structure, the first and second dielectric layers 210 and 215 stacked on the contact region CR are patterned in a stair shape. That is, on the contact region CR, the stack height of the first and second dielectric layers 210 and 215 decreases toward the edge.”)

76. Chae discloses forming horizontally extending “first and second dielectric layers 210 and 215” in a vertically stacked layer structure, such that the first dielectric layers 210 form a stack.<sup>1</sup> Chae, [0123]-[0124], Fig. 15A. Chae

<sup>1</sup> This “stack” of first dielectric layers 210 not being formed directly on top of one another is consistent with the ’996 patent specification. In particular, the ’996 patent discloses alternating “dielectric material 14” and “sacrificial material 12” as the

further discloses the “stack” comprises a primary portion in a “memory cell region MR” and an end portion in “a contact region CR”. Chae, [0123]. Chae also discloses the first dielectric layers 210 form a stair-case structure in contact region CR, in which lower steps of first dielectric layers 210 extend farther into contact region CR than higher steps. Chae, [0124], Fig. 15A.

### 3. Element [1.b]

77. **Element [1.b] recites “forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion.”** This element is met by Chae.

78. Chae discloses forming operative structures (*e.g.*, collectively, “charge storage layers 222a” and “active pillars 224a”) vertically through the features (*e.g.*, through “first dielectric layers 210”) in the primary portion (*see* [1.a]) and forming dummy structures (*e.g.*, collectively, “charge storage layers 222b” and “supporters 224b”) vertically through the features (*e.g.*, through “first dielectric layers 210”) in the end portion (*see* [1.a]). *See, e.g.*, Chae:

- Fig. 15B (annotated)

---

“stack” of overlapping features, even though the dielectric material 14 alone constitutes the “features.” ’996 Patent, 3:65-67, 4:38-46, 6:67-7:5.

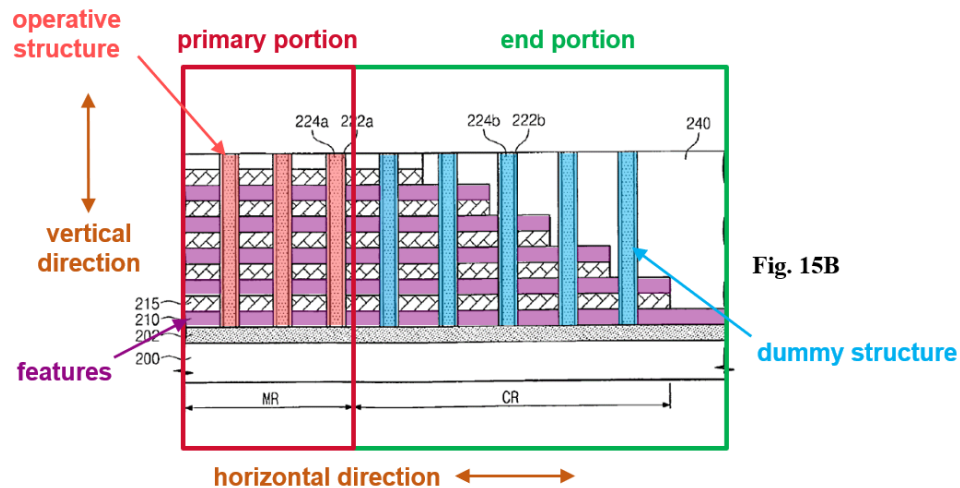


Fig. 15B

- [0126] (“Referring to FIG. 15B, active pillars 224a are formed in the memory cell region MR and supporters 224b are formed in the contact region CR.”)
- [0128] (“Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b. That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the contact region CR and the active pillars 224a of the memory cell region MR. Also, the active pillars 224a and the supporters 224b may be formed to the same length. The active pillars 224a of the memory cell region MR may penetrate all of the stacked first and second dielectric layers 210 and 215, and the supporters 224b of the contact region CR may penetrate some of the stacked first and second dielectric layers 210 and 215.”)

79. See my discussion for element [1.a] above (Section IX.A.2.2).

80. Chae further discloses forming “active pillars 224a of the memory cell region MR” such that they “penetrate all of the stacked first and second dielectric layers 210 and 215,” and forming “charge storage layers 222a...around...active pillars 224.” Chae, [0128]. Charge storage layers 222a and active pillars 224a are parts of memory cells, and are thus operative structures. Chae further discloses

forming “supporters 224b of the contact region CR” such that they “penetrate some of the stacked first and second dielectric layers 210 and 215,” and forming “charge storage layers 224b...around the supporters 224b.” Chae, [0128].

81. Charge storage layers 222b and supporters 224b collectively form dummy structures under the construction “electrically inoperable structure that mimics a physical property of an operative structure.” First, charge storage layers 222b and supporters 224b are not electrically connected to other components, and are thus electrically inoperable. As Chae explains, “[b]ecause a conductive pattern such as the global word line 275 or the bit line 270 is not formed on the supporters 224b, it does not affect the operation of the nonvolatile memory device....” Chae, [0134]. Second, the charge storage layers 222b and supporters 224b mimic a physical property of the charge storage layers 222a and active pillars 224a because they are formed of identical (or at least similar) materials in the same process. Chae, [0128] In this regard, Chae teaches that “similar reference numerals refer to like elements,” consistent with charge storage layers 222a and charge storage layers 222b being formed of the same material, and consistent with active pillars 224a and supporters 224b being formed of the same material.

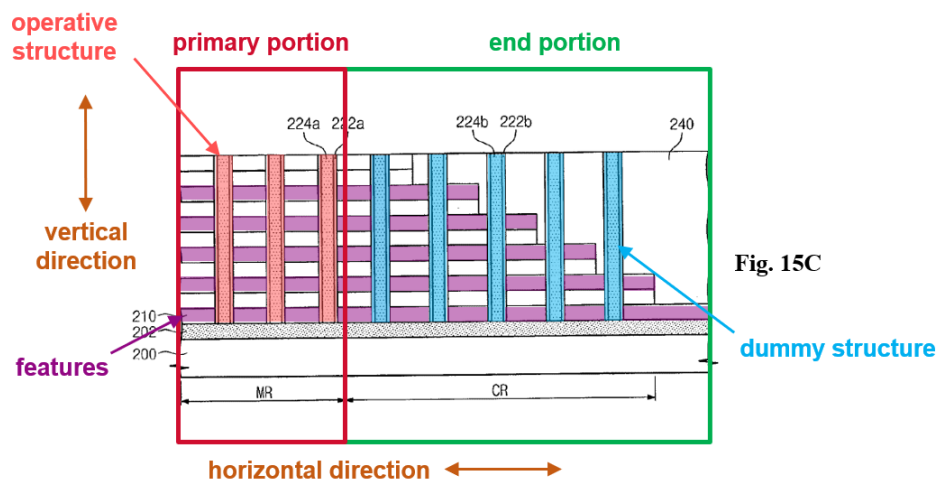
#### **4. Element [1.c]**

82. **Element [1.c] recites “removing at least some sacrificial material that is elevationally between material of the features in the primary and end**

portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing.” This element is met by Chae.

83. Chae discloses removing at least some sacrificial material (*e.g.*, “remove the second dielectric layers 215”) that is elevationally between material of the features (*e.g.*, between “first dielectric layers 210” as illustrated in Fig. 15A-15B) in the primary and end portions (*see* [1.a]), wherein the dummy structures support material of the features from vertical movement in the end portion during said removing (*e.g.*, “first dielectric layers 210 spaced apart from each other...supported by...supporters 224b of the contact region CR” to prevent “collapsing”). *See, e.g.*, Chae:

- Fig. 15C (annotated)



- [0129] (“Referring to FIG. 15C, the plate-shaped stack structure including the active pillars 224a and the supporters 224b are patterned to form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and

215 may be exposed. ***Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.*** Accordingly, an empty space is formed between the first dielectric layers 210 that are perpendicular to the semiconductor substrate 200 and are spaced apart from each other. ***The first dielectric layers 210 spaced apart from each other may be supported by the active pillars 224a of the memory cell region MR, which are perpendicular to the semiconductor substrate 200, and the supporters 224b of the contact region CR. That is, the second dielectric layers 215 can be prevented from collapsing or getting near to each other during the removing of the second dielectric layers 215 through a wet etch process.***)

84. See my discussion for elements [1.a]-[1.b] above (Sections IX.A.2.2-3).

85. Chae further discloses “first and second dielectric layers 210 and 215...are alternately stacked” “across a memory cell region MR and a contact region CR” and that by supplying “an etchant between the...stack structure,” “second dielectric layers 215” is removed. Chae, [0123], [0129]. Chae further discloses that “first dielectric layers 210...may be supported by...the supporters 224b of the contact region CR” such that layers are “prevented from collapsing or getting near each other.” Chae, [0129].<sup>2</sup> This support is illustrated in Figure 15C,

---

<sup>2</sup> Chae states: “the second dielectric layers 215 can be prevented from collapsing or getting near to each other during the removing of the *second dielectric layers 215* through a wet etch process.” Chae, [0129]. The first reference to “dielectric layers 215” being prevented from collapsing is a typographical error, and instead, first

in which first dielectric layers 210 are separated from each other, but do not collapse despite the lack of an intervening structure after layers second dielectric layers 215 are removed. Charge storage layers 222b are formed on the sides of supporters 224b, such that charge storage layers 222b are in direct contact with the first dielectric layer, and the combination works together to support first dielectric layers 210.

## 5. Claim [2]

86. **Claim 2 recites “The method of claim 1 wherein the operative and dummy structures comprise the same material.”** See my discussion of the elements of claim 1 above (Sections IX.A.2.1-4). The limitation added by claim 2 is met by Chae.

87. Chae discloses the operative (e.g., “active pillars 224a” with “charge storage layers 222a”) and dummy structures (e.g., “supporters 224b” with “charge storage layers...222b”) comprise the same material (“e.g., “semiconductor material” and “charge storage” material). *See, e.g.,* Chae:

- [0128] (***“Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the***

---

dielectric layer 210 is the layer prevented from collapsing. Fig. 15C illustrates after the second dielectric layers 215 are removed, the first dielectric layers 210 do not collapse, despite the lack of structure between them.

***dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.”)***

88. See my discussion for element [1.b] above (Section IX.A.2.3).

89. Chae further discloses “charge storage layers 222a and 222b” and “active pillars 224a and supporters 224b” are formed in the same respective processes. Chae, [0128]. Because the same processes are used, the respective structures are formed of the same materials.

## **6. Claim [3]**

90. **Claim 3 recites “The method of claim 2 wherein the operative and dummy structures comprise a plurality of the same materials.”** See my discussion for claim 2 above (Section IX.A.2.5). The limitation added by claim 3 is met by Chae.

91. Chae discloses the operative and dummy structures (*see* [2]) comprise a plurality of the same materials (*e.g.*, each comprises “semiconductor material” and “charge storage” material).

92. As I explain in my discussion for claim 2, Chae discloses that “charge storage layers 222a and 222b” and “active pillars 224a and supporters 224b” are formed in the same respective processes, and thus comprise a plurality of the same materials (“semiconductor material” and “charge storage” material).

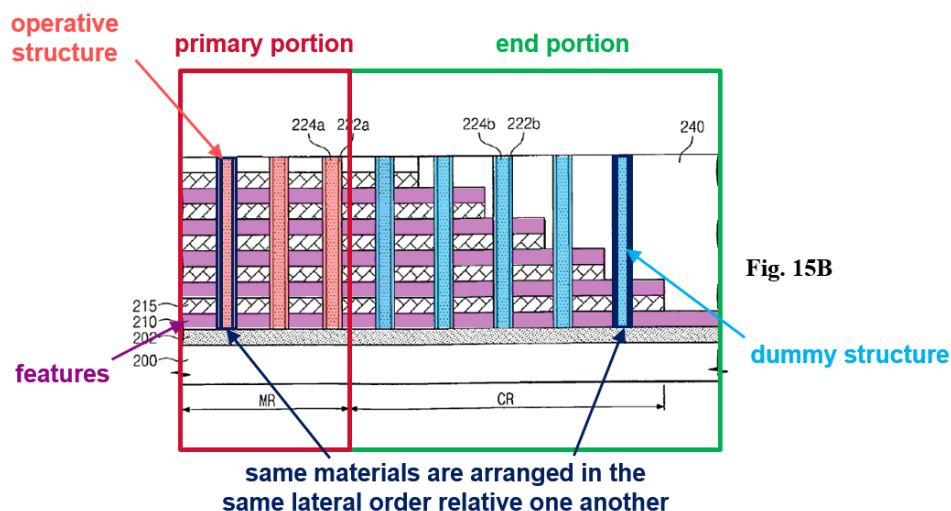
## **7. Claim [4]**

93. **Claim 4 recites “The method of claim 3 wherein the same**

materials are arranged in the same lateral order relative one another in the operative and dummy structures.” See my discussion for claim 3 above (Section IX.A.2.6). The limitation added by claim 4 is met by Chae.

94. Chae discloses the same materials (*e.g.*, collectively, “semiconductor material” and “charge storage” material) are arranged in the same lateral order relative one another in the operative and dummy structures (*see* [3]). *See, e.g.*, Chae:

- Fig. 15B (annotated)



95. As I explain in my discussion for claims 2-3, Chae discloses that “charge storage layers 222a and 222b” and “active pillars 224a and supporters 224b” are formed in the same respective processes, and thus comprise a plurality of the same materials (“semiconductor material” and “charge storage” material) arranged in the same lateral order relative to one another.

## 8. Claim [6]

96. **Claim 6 recites “The method of claim 1 wherein the features comprise plates.”** See my discussion for claim 1 above (Sections IX.A.2.1-4). The limitation added by claim 6 is met by Chae.

97. Chae discloses the features (*e.g.*, “first dielectric layers 210”) comprise plates (*e.g.*, “plate-shaped”). See, *e.g.*, Chae:

- [0123] (“Referring to FIG. 15A, ***first and second dielectric layers 210 and 215 with different etch selectivity are alternately stacked on a semiconductor substrate 200, and a plate-shaped stack structure is formed*** across a memory cell region MR and a contact region CR.”)
- [0124] (“***In the plate-shaped stack structure, the first and second dielectric layers 210 and 215 stacked on the contact region CR are patterned in a stair shape.*** That is, on the contact region CR, the stack height of the first and second dielectric layers 210 and 215 decreases toward the edge.”)
- [0125] (“Thereafter, ***the plate-shaped stack structure*** is covered with a dielectric layer, and it is planarized to equalize the heights of the memory cell region MR and the contact region CR. That is, a dielectric layer 240 may be formed on the stair-shaped stack structure.”)

98. See my discussion for element [1.a] above (Section IX.A.2.2). Chae further discloses that “first dielectric layers 210” are “plate-shaped.”

## 9. Claim [7]

99. **Claim 7 recites “The method of claim 1 wherein the operative and dummy structures comprise programmable material.”** See my discussion for claim 1 above (Sections IX.A.2.1-4). The limitation added by claim 7 is met by Chae.

100. Chae discloses the operative and dummy structures (*see* [2]) comprise programmable material (*e.g.*, “charge storage layer”).

101. As I explain in my discussion for element [1.b] above (Section IX.A.2.3), Chae discloses the operative and dummy structures comprise “semiconductor material” with sidewalls of “charge storage layers 222a and 222b.” Chae, [0128]. A charge storage layer surrounding semiconductor material comprises programmable material, as charge stored in the charge storage layer changes the threshold voltage that must be applied to the corresponding gate electrode 250 to allow current flow through the semiconductor material, indicating the storage of information (*i.e.*, programming).

#### **10. Claim [8]**

102. **Claim 8 recites “The method of claim 1 wherein the operative and dummy structures comprise semiconductive material.”** See my discussion for claim 1 above (Sections IX.A.2.1-4). The limitation added by claim 3 is met by Chae.

103. Chae discloses the operative and dummy structures (*see* [2]) comprise semiconductive material (*e.g.*, “semiconductor material”).

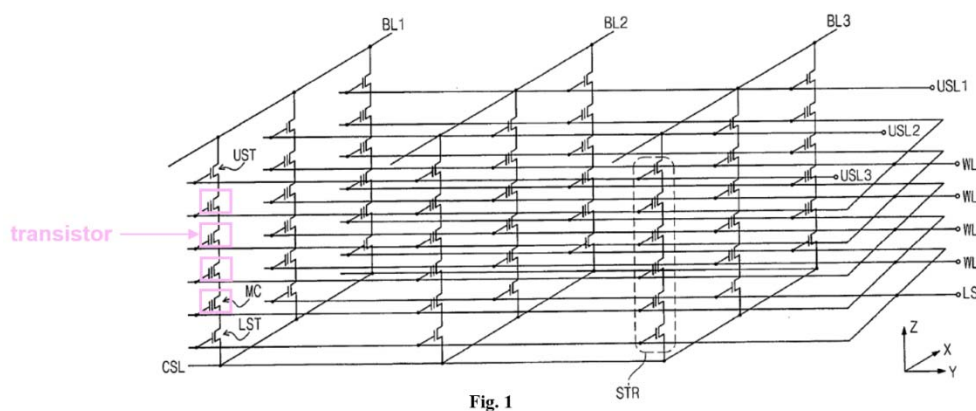
104. See my discussion for element [1.b] above (Section IX.A.2.3). As I explain in my discussion for claim 2 above (Section IX.A.2.5), Chae discloses active pillars 224a and supporters 224b comprise semiconductor material.

## 11. Claim [9]

105. Claim 9 recites “The method of claim 8 wherein the semiconductive material of the operative structures comprises interconnected channels of a plurality of vertically oriented transistors.” See my discussion for claim 8 above (Section IX.A.2.10). The limitation added by claim 9 is met by Chae.

106. Chae discloses the semiconductive material of the operative structures (see [8]) comprises interconnected channels (e.g., “active pillars 224a”) of a plurality of vertically oriented transistors (e.g., “memory cell transistors MC”). See, e.g., Chae:

- Fig. 1 (annotated)



- [0042] (“Referring to FIG. 1, a nonvolatile memory device according to exemplary embodiments of the inventive concept includes a cell array including a plurality of strings STR. The cell array includes bit lines BL1~BL3, word lines WL1~WL4, upper and lower select lines USL1~USL3 and LSL, and a common source line CSL. The strings STR are provided between the common source line CSL and the bit lines BL1~BL3.”)

- [0043] (***“Each string STR includes upper and lower select transistors UST and LST, and memory cell transistors MC that are connected in series between the upper and lower select transistors UST and LST. The drains of the upper select transistors UST are connected to the bit lines BL1~BL3, and the sources of the lower select transistors LST are connected in common to the common source line CSL.”***)
- [0044] (***“The upper select transistors UST are connected to the upper select lines USL1~USL3, and the lower select transistors LST are connected respectively to the lower select lines LSL. The memory cells MC are connected respectively to the word lines WL1~WL4.”***)
- [0045] (***“The cell array has a three-dimensional structure. That is, the strings STR are configured in such a way that the memory cells MC are connected in series in a Z-axis direction perpendicular to an XY plane parallel to the top surface of a semiconductor substrate. Accordingly, the channel of the memory cell transistors MC and the select transistors UST and LST may be formed perpendicular to the XY plane.”***)
- [0054] (***“Active pillars PL are formed in the memory cell region MR perpendicular to the plane of the semiconductor substrate 100. The active pillars PL are formed of semiconductor material. The active pillars PL may penetrate the gate electrodes LSL, WL and USL of the memory cell region MR. The pillars PL may be spaced apart from each other, and may be arranged in a matrix configuration on a plane. Also, the active pillars PL may be electrically connected to the impurity region 102 of the semiconductor substrate 100 by penetrating the gate electrodes LSL, WL and USL. The active pillars PL are provided for the channels of transistors, which correspond to the strings of the nonvolatile memory device according to the embodiments of the inventive concept. That is, the channels of memory cell transistors and select transistors (LST, UST and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.”***)
- [0041] (***“FIG. 1 is a circuit diagram of a nonvolatile memory device according to exemplary embodiments of the inventive concept.”***)
- [0121] (***“Another method for fabricating the nonvolatile memory devices according to the second and fifth exemplary embodiments of the***

*inventive concept will be described below with reference to FIGS. 15A to 15E.”)*

- [0004] (“Nonvolatile memory devices include various types of memory cell transistors. Nonvolatile memory devices are classified into NAND-type nonvolatile memory devices and NOR-type nonvolatile memory devices, depending on the cell array structures. The NAND-type nonvolatile memory device and the NOR-type nonvolatile memory device have the advantages and disadvantages of high integration and high operation speed.”)
- [0005] (“In particular, the NAND-type nonvolatile memory device is advantageous for high integration because it includes a cell string structure having a plurality of memory cell transistors connected in series. Also, the NAND-type nonvolatile memory device has a much higher data update speed than the NOR-type nonvolatile memory device because it uses an operation scheme of simultaneously changing data stored in a plurality of memory cell transistors. Due to such a high integration level and high update speed, the NAND-type nonvolatile memory device is widely used in portable electronic products requiring mass storage, such as digital cameras and MP3 players.”)

107. Chae discloses “active pillars PL,” which “are formed of semiconductor material,” and “are provided for the channels of transistors.” Chae, [0054]. Chae also discloses that “upper and lower select transistors UST and LST, and memory cell transistors MC” connected in series form a “string STR.” Chae, [0043], Fig. 1. These “strings STR are configured in such a way that the memory cells MC are connected in series in a Z-axis direction perpendicular to an XY plane,” i.e., the transistors (“MC”) are vertically oriented. Chae, [0045], Fig. 1. Chae also discloses that the channels of these vertically oriented transistors are “electrically connected through the active pillars PL,” which form channels. Chae,

[0054]. Figure 1 and related paragraphs [0041]-[0057] apply to “exemplary embodiments of the inventive concept” ([0041]) and a person of ordinary skill in the art would have understood that descriptions of “active pillars PL” in [0054] apply to “active pillars 224a” in the “fifth exemplary embodiment of the inventive concept,” which I rely upon for my analysis for claims 1 to 8. Chae, [0121]. For example, a person of skill in the art would have understood the illustration in Figure 1 and corresponding disclosure relate to a general memory structure, including the general electrical interconnection of memory cells, word lines, select lines and bit lines, and provide an overview of the overall connections in Chae’s embodiments.

## **12. Claim [10]**

108. **Claim 10 recites “The method of claim 9 wherein interconnected channels are of vertically oriented charge storage transistors.”** See my discussion for claim 9 above (Section IX.A.2.11). The limitation added by claim 10 is met by Chae.

109. Chae discloses that interconnected channels (*e.g.*, “active pillars 224a”) are of vertically oriented charge storage transistors (*e.g.*, “memory cell transistors MC”).

110. As I explain in my discussion for claim 9 above (Section IX.A.2.11), the “semiconductor material” of Chae’s “active pillars” comprises interconnected

channels of a plurality of vertically oriented transistors. Chae further discloses that “charge storage layers 222a...may be formed around...the active pillars 224a.” Chae, [0055]. As I explain in [7], the charge storage layers are programmable because they hold charge, which impacts the threshold voltage of the transistors. Therefore, Chae’s vertically oriented transistors are vertically oriented charge storage transistors. Chae, [0128] (“***That is, charge storage layers 222a and 222b may be formed around*** the supporters 224b of the contact region CR and ***the active pillars 224a of the memory cell region MR.***”).

### 13. Element [12.pre]

111. Element [12.pre] recites “**A method of forming circuitry components, comprising.**” This element is met by Chae. See my discussion for element [1.pre] above (Section IX.A.2.1).

### 14. Element [12.a]

112. Element [12.a] recites “**forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion.**” This element is met by Chae. See my discussion for element [1.a] above (Section IX.A.2.2).

### 15. Element [12.b]

113. Element [12.b] recites “**forming operative structures vertically**

**through the features in the primary portion and forming dummy structures vertically through the plates in the end portion.”** This element is met by Chae. See my discussion for element [1.b] above (Section IX.A.2.3). As explained in my discussion of claim 6 above (Section IX.A.2.8), the “first dielectric layers 210” are plates.

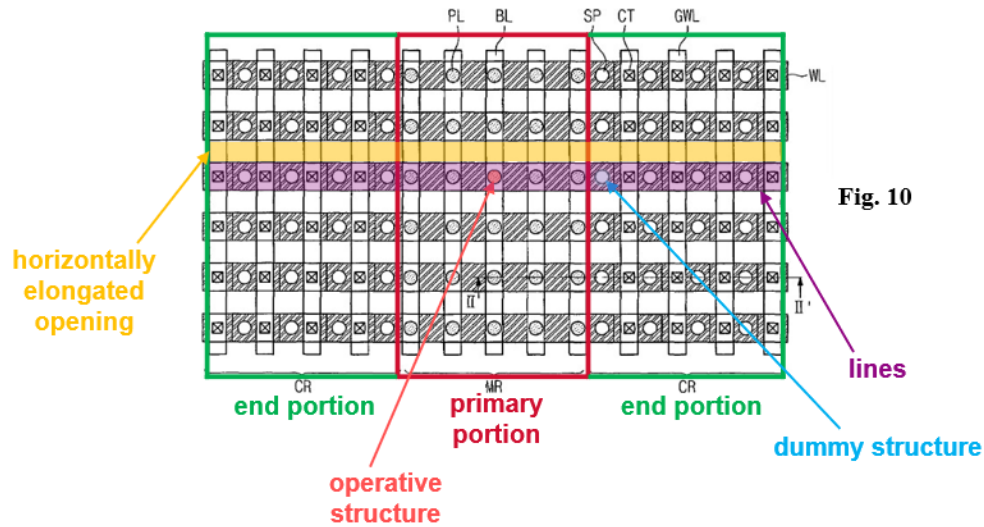
#### **16. Element [12.c]**

114. **Element [12.c] recites “forming horizontally elongated openings through the structures to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures.”** This element is met by Chae.

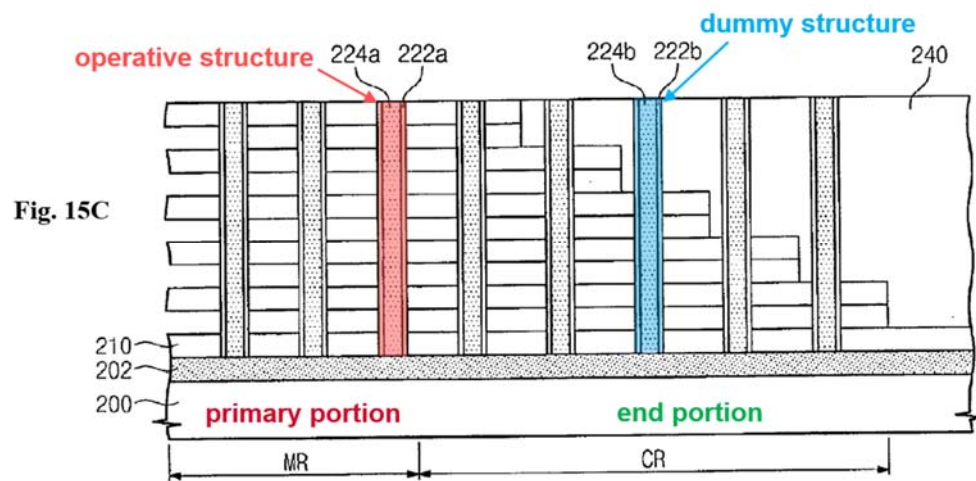
115. Chae discloses forming horizontally elongated openings (*e.g.*, openings illustrated in Fig. 10) through the structures (*e.g.*, between the “active pillars 224a” with “charge storage layers” and “supporters 224b” with “charge storage layers 222b”; *see* [2]) to form horizontally elongated and vertically overlapping lines (*e.g.*, “line-shaped stack structures”) from material of the features (*e.g.*, “first dielectric layers 210”), the lines individually extending from the primary portion (*e.g.*, “memory cell region MR”) and into the end portion (*e.g.*, “contact region CR”) and individually laterally about sides of vertically extending

portions of both the operative structures and the dummy structures (see [2]). See, e.g., Chae:

- Fig. 10 (annotated)



- Fig. 15C (annotated)



- [0123] (“Referring to FIG. 15A, first and second dielectric layers 210 and 215 with different etch selectivity are alternately stacked on a semiconductor substrate 200, and **a plate-shaped stack structure is formed across a memory cell region MR and a contact region CR.**”)

- [0129] (“**Referring to FIG. 15C, the plate-shaped stack structure including the active pillars 224a and the supporters 224b are patterned to form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and 215 may be exposed.** Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.”)

116. See my discussions for elements [1.a]-[1.b] and [2] above (Sections IX.A.2.2-3, IX.A.2.5).

117. Chae further discloses forming “line-shaped stack structures” by patterning the “plate-shaped stack structures,” thereby opening trenches through the “active pillars 224a” with “charge storage layers 222a” and “supporters 224b” with “charge storage layers 222b,” as shown in Fig. 10. Chae, [0129].<sup>3</sup> These lines are vertically overlapping because they are “stacked.” Chae, [0129]. As illustrated in Fig. 10, the “line-shaped stack structures” extend across the cell region MR and contact region CR. Chae, [0123], Fig. 10. Chae also discloses that

---

<sup>3</sup> The ’996 Patent discloses forming horizontally elongated openings amongst operative and dummy structures, not directly through individual such structures. ’996 Patent, Figs. 5-11, 12-13, 15-17. However, the term “through” as used in the specification consistently refers to structures passing directly through other structures. I address the case where the horizontally elongated openings extend directly through the structures in my discussion of Ground 4 (Section IX.D).

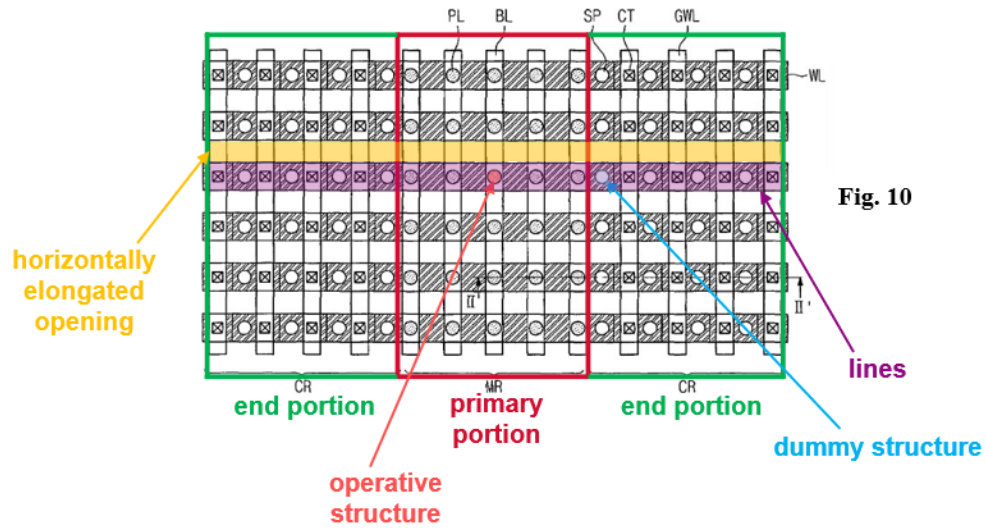
by opening the trenches, “the sidewalls of the first and second dielectric layers 210 and 215 may be exposed” such that the lines extend laterally about the “active pillars 224a” and “supporters 224b,” which vertically extend through the lines. Chae, [0129], Figs. 10, 15C. Moreover, the trenches are formed “through” the structures in the same way PO asserts openings pass through structures in its infringement contentions in the NDCA Case, *i.e.*, the openings pass between the alleged structures. For example, on page 21 of Ex. B-2 of Ex. 1016, PO asserts that openings passing between the asserted structures both in the primary portion and the end portion pass through the asserted structures. Ex. 1016, Ex. B-2 at 20-23. This arrangement is the same as the arrangement disclosed in Chae.

#### **17. Element [12.d]**

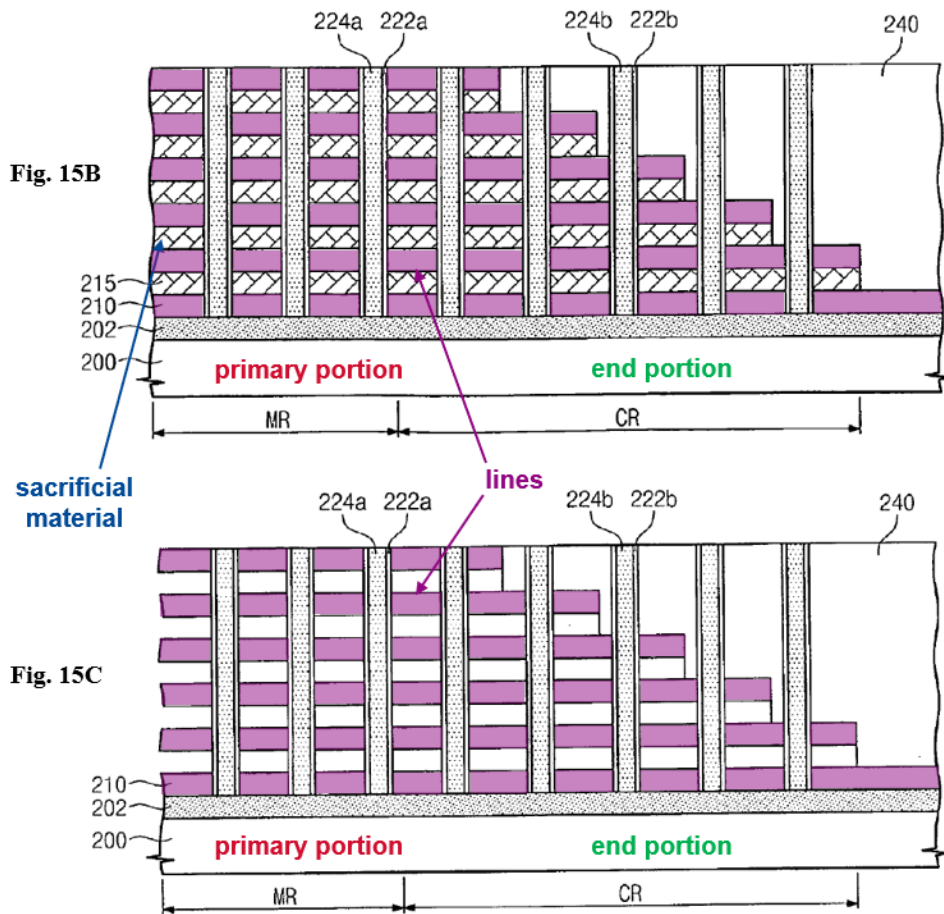
118. **Element [12.d] recites “removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings.”** This element is met by Chae.

119. Chae discloses removing at least some sacrificial material (*e.g.*, removing “second dielectric layers 215”) that is elevationally between the lines (*e.g.*, between the “first dielectric layers 210” of “line-shaped stack structures”) in the primary and end portions (*see* [1.a]) laterally between the openings (*e.g.*, slots illustrated in Fig. 10). *See, e.g.*, Chae:

- Fig. 10 (annotated)



- Figs. 15B, 15C (annotated)



- [0129] (“Referring to FIG. 15C, the plate-shaped stack structure including the active pillars 224a and the supporters 224b are patterned to

form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and 215 may be exposed. ***Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.***)

120. See my discussions for elements [1.a] and [12.c] above (Section IX.A.2.2, IX.A.2.16). Chae further discloses removing portions of “second dielectric layers 215” elevationally between the “line-shaped” “stacked first dielectric layers 210,” which are laterally between the slots, as illustrated in Fig. 10. Chae, [0129]. “[S]econd dielectric layers 215” are sacrificial because they are not included in the final product, but are instead removed and replaced with “line-shaped gate electrodes 250”—see Fig. 15C. *Id.*, [0129].

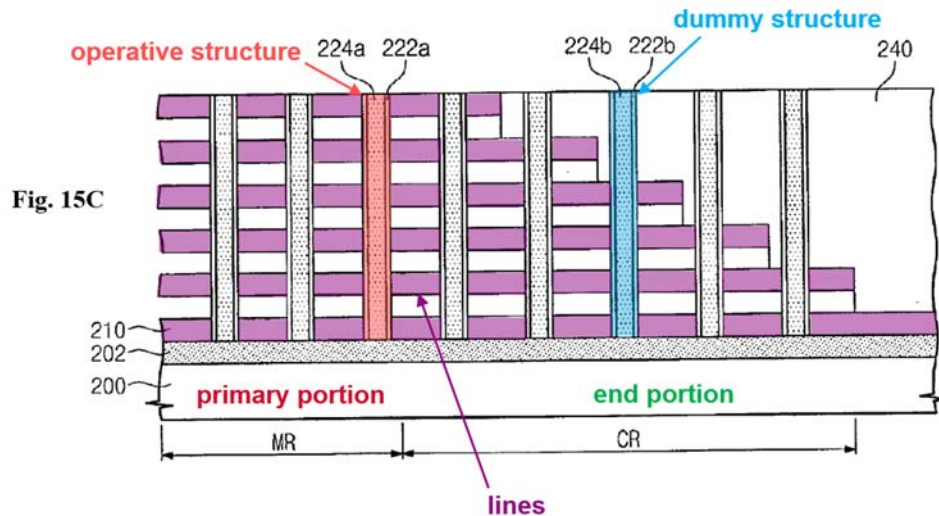
#### **18. Claim [13]**

121. **Claim 13 recites “The method of claim 12 wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures.”** See my discussions for claim 12 above (Sections IX.A.2.13-17). The limitation added by claim 13 is met by Chae.

122. Chae discloses the removing comprises etching of the sacrificial material (*e.g.*, “etch[ing]” “second dielectric layers 215”) selectively (*e.g.*, with “different etch selectivity”) relative to material of the lines (*e.g.*, relative to “first dielectric layers 210” of “line-shaped stack structures”), the operative structures

(see [2]), and the dummy structures (see [2]). See, e.g., Chae:

- Fig. 15C (annotated)



- [0129] (“When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and 215 may be exposed. **Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.**”)
- [0138] (“Referring to FIG. 16A, **first and second dielectric layers 210 and 215 with different etch selectivity are alternately stacked** on a semiconductor substrate 200. Line-shaped first trenches T1 exposing the semiconductor substrate 200 are formed in the stacked first and second dielectric layers 210 and 215. When the first trenches T1 are formed, the first sidewalls of the stacked first and second dielectric layers 210 and 215 may be exposed.”)
- [0143] (“Referring to FIG. 16D, **through a wet etch process, the second dielectric layers 215 between the stacked first dielectric layers 210 are removed.** Accordingly, second trenches T2’ exposing the sidewalls of the active pillars 224 may be formed. **The supporters SP on the contact region CR are formed of a material having an etch selectivity with respect to the second dielectric layer 215,** thus supporting the first dielectric layers 210 vertically spaced apart by a predetermined distance.”)

123. See my discussions for elements [2] and [12.d] above (Sections

IX.A.2.5, IX.A.2.17).

124. Chae discloses removing the second dielectric layers 215 using an etchant with “high selectivity with respect to the first dielectric layer 210” forming the “line-shaped stack structures.” Chae, [0129]. Moreover, the etching is also selective relative to the charge storage layers 222a and 222b (*i.e.*, operative and dummy structures) because those structures remain after the etching process, as shown in Fig. 15C. Chae, [0129].

#### **19. Claim [16]**

125. **Claim 16 recites “The method of claim 12 wherein the features comprise plates.”** See my discussions for claim 6 above (Section IX.A.2.8). The limitation added by claim 16 is met by Chae.

#### **20. Element [17.pre]**

126. **Element [17.pre] recites “A method of forming circuitry components, comprising.”** This element is met by Chae. See my discussion for element [1.pre] above (Section IX.A.2.1).

#### **21. Element [17.a]**

127. **Element [17.a] recites “forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion.”** This element is met by Chae. See my discussion for element [1.a] above

(Section IX.A.2.2).

## 22. Element [17.b]

128. Element [17.b] recites **“forming primary portion openings through the features in the primary portion and forming end portion openings through the features in the in the end portion.”** This element is met by Chae.

129. Chae discloses forming primary portion openings (*e.g.*, “channel holes”) through the features (*e.g.*, “first dielectric layers 210”) in the primary portion (*e.g.*, “memory cell region MR”) and forming end portion openings (*e.g.*, “dummy holes”) through the features in the in the end portion (*e.g.*, “contact region CR”). *See, e.g.*, Chae:

- [0127] (“More specifically, ***channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR.*** The channel holes and the dummy holes may be formed through a photolithography process, and the channel holes may be formed in a matrix configuration on the plane. Also, as illustrated in FIG. 5, the dummy holes may be formed respectively at one side of the channel holes located at the edge of the memory cell region MR. Also, as illustrated in FIG. 10, the dummy holes may be formed on the same line as the channel holes, and the dummy holes on the same line are spaced apart from each other. ***The dummy hole adjacent to the channel hole may penetrate all of the stacked first and second dielectric layers 210 and 215. Also, the number of the penetrated first and second dielectric layers 210 and 215 may decrease with an increase in the distance from the memory cell region MR.***”)
- [0128] (“Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b. That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the

contact region CR and the active pillars 224a of the memory cell region MR. Also, the active pillars 224a and the supporters 224b may be formed to the same length. ***The active pillars 224a of the memory cell region MR may penetrate all of the stacked first and second dielectric layers 210 and 215, and the supporters 224b of the contact region CR may penetrate some of the stacked first and second dielectric layers 210 and 215.***)

130. See my discussion for element [1.a] above (Section IX.A.2.2).

131. Chae further discloses “channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR,” and these holes “penetrate” dielectric layers 210. Chae, [0127]-[0128].

### **23. Element [17.c]**

132. **Element [17.c] recites “forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the end portion openings and forming operative structures therewith within the primary portion openings and forming dummy structures therewith within the end portion openings.”** This element is met by Chae.

133. Chae discloses forming at least one of...semiconductive material (*e.g.*, “semiconductor material”), and programmable material (*e.g.*, “charge storage layer”; *see* [7]) in the primary portion openings (*e.g.*, “channel holes”) and the end portion openings (*e.g.*, “dummy holes”) and forming operative structures therewith within the primary portion openings (*e.g.*, collectively, “charge storage layers

222a” and “active pillars 224a” in “channel holes”) and forming dummy structures therewith within the end portion openings (*e.g.*, collectively, “charge storage layers 222b” and “supporters 224b” in “dummy holes”). *See, e.g.*, Chae:

- [0128] (“***Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.*** That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the contact region CR and the active pillars 224a of the memory cell region MR. Also, the active pillars 224a and the supporters 224b may be formed to the same length. The active pillars 224a of the memory cell region MR may penetrate all of the stacked first and second dielectric layers 210 and 215, and the supporters 224b of the contact region CR may penetrate some of the stacked first and second dielectric layers 210 and 215.”)

134. See my discussion for element [1.b] above (Section IX.A.2.3).

135. Chae further discloses “charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes,” which are then “filled with semiconductor material to form active pillars 224a and supporters 224b,” respectively. Chae, [0128]. Chae’s “charge storage layers 222a” and “active pillars 224a” collectively constitute operative structures in “channel holes” and “charge storage layers 222b” and “supporters 224b” collectively constitute dummy structures in “dummy holes.” Both “active pillars 224a” and “supporters 224b” comprise “semiconductor material.” Chae, [0128]. Furthermore, as discussed in [7], charge storage layers 222a and 222b comprise programmable material.

#### **24. Element [17.d]**

136. **Element [17.d] recites “forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures.”** This element is met by Chae. See my discussion for element [12.c] above (Section IX.A.2.16).

#### **25. Element [17.e]**

137. **Element [17.e] recites “removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.”** This element is met by Chae. See my discussions for elements [12.d] and [13] above (Section IX.A.2.17-18).

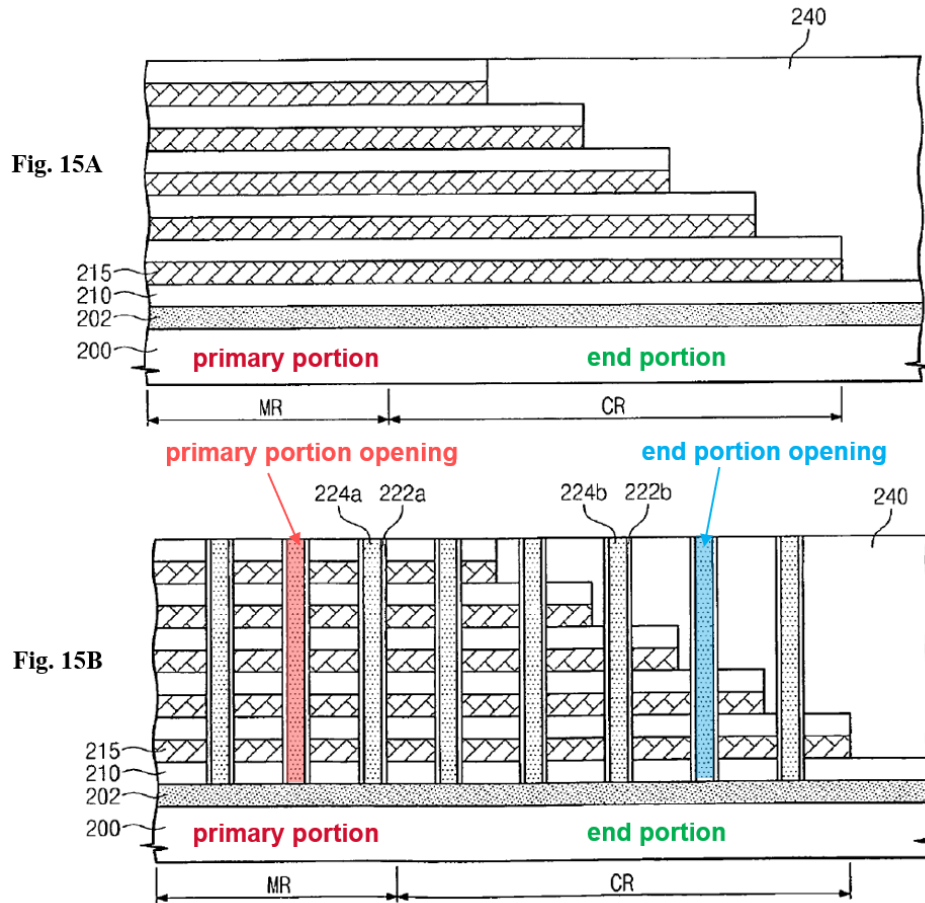
#### **26. Claim [18]**

138. **Claim 18 recites “The method of claim 17 comprising forming the primary portion openings and the end portion openings at the same time.”** See my discussion for claim 17 above (Sections IX.A.2.20-25). The limitation added by claim 18 is met by Chae.

139. Chae discloses forming the primary portion openings (*e.g.*, “channel holes”) and the end portion openings (*e.g.*, “dummy holes”) at the same time (*e.g.*,

“through a photolithography process”). See, e.g., Chae:

- Figs. 15A, 15B (annotated)



- [0127] (“More specifically, channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR. ***The channel holes and the dummy holes may be formed through a photolithography process,*** and the channel holes may be formed in a matrix configuration on the plane. Also, as illustrated in FIG. 5, the dummy holes may be formed respectively at one side of the channel holes located at the edge of the memory cell region MR. Also, as illustrated in FIG. 10, the dummy holes may be formed on the same line as the channel holes, and the dummy holes on the same line are spaced apart from each other.”)

140. See my discussion for element [17.b] above (Section IX.A.2.22).

141. Chae further discloses “channel holes and the dummy holes may be

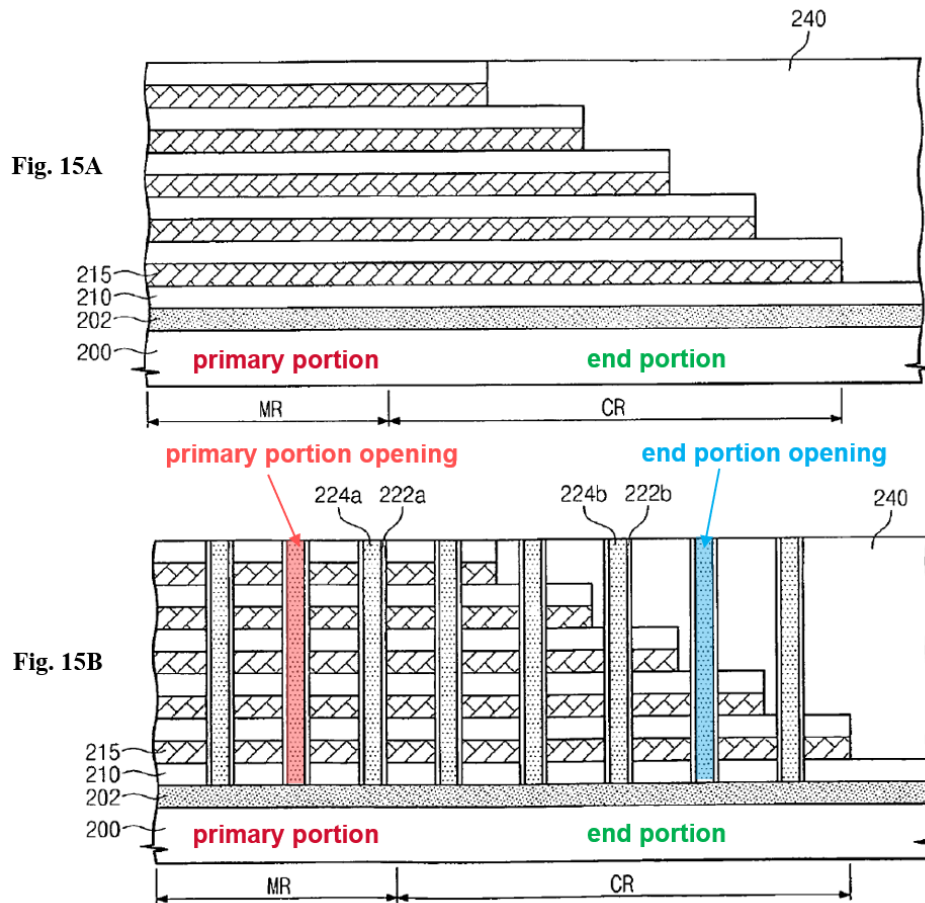
formed through a photolithography process.” Chae, [0127]. A person of ordinary skill in the art would have understood (or at least found it obvious) that forming the “channel holes” and “dummy holes” using the same “photolithography process” would be advantageously performed at the same time. A photolithography process includes using a mask pattern. *See, e.g.,* Chae, [0099] (describing the formation of the same channel holes in a different embodiment as “[t]he channel holes may be formed by forming a mask pattern”). By forming the holes through a mask pattern that has the right size and pattern to form both channel holes and dummy holes, the holes are formed at the same time. This would have had the advantage of minimizing the number of processing steps required. For example, U.S. Patent Application Publication No. 2007/0057328 (“Taniguchi”), which I understand has been designated as Exhibit 1017, recognizes this is advantageous to use fewer processing and masking steps, teaching that “it is preferable that[] mask pattern is made the same” for different manufacturing steps “so as not to increase the number of mask patterns.” Ex.1017, [0062]; *see also id.*, [0066]-[0067]. Using the same mask pattern would also allow different components (e.g., memory hole and source-side hole 24) to be formed at the same time, and thus “[t]he number of processes can therefore be reduced.” *Id.*, [0043]; *see also id.*, [0034], [0036], [0042], [0142].

## 27. Claim [23]

142. Claim 23 recites “The method of claim 17 wherein said at least one of conductive material, semiconductive material, and programmable material is deposited simultaneously into the primary portion openings and the end portion openings.” See my discussion for claim 17 above (Sections IX.A.2.20-25). The limitation added by claim 23 is met by Chae.

143. Chae discloses that at least one of...semiconductive material, and programmable material (*see* [17.c]) is deposited simultaneously into the primary portion openings (*e.g.*, “channel holes”) and the end portion openings (*e.g.*, “dummy holes”). *See, e.g.*, Chae:

- Figs. 15A, 15B (annotated)



- [0128] (“**Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.** That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the contact region CR and the active pillars 224a of the memory cell region MR. Also, the active pillars 224a and the supporters 224b may be formed to the same length. The active pillars 224a of the memory cell region MR may penetrate all of the stacked first and second dielectric layers 210 and 215, and the supporters 224b of the contact region CR may penetrate some of the stacked first and second dielectric layers 210 and 215.”)

144. See my discussion for element [17.c] above (Section IX.A.2.23).

145. Chae further discloses “charge storage layers 222a and 222b are

formed at the sidewalls of the dummy holes and the channel holes,” and “the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.” Chae, [0128]. A person of ordinary skill in the art would have understood (or at least found it obvious) the “dummy holes” and the “channel holes” are “filled with semiconductor material” simultaneously, and programmable material (“charge storage layers”) are formed in the “dummy holes” and the “channel holes” simultaneously. Forming these materials in the channel holes and dummy holes simultaneously would have had the advantage of minimizing the number of processing steps required. As I note above in connection with claim [18], minimizing the number of processing steps was recognized as advantageous in the art. See Ex. 1017, [0034], [0036], [0042], [0043], [0142].

## **28. Claim [24]**

146. **Claim 24 recites “The method of claim 17 wherein the features comprise plates.”** This claim is met by Chae. See my discussions for claims 6 and 17 above (Sections IX.A.2.8, IX.A.2.20-25).

## **29. Element [25.pre]**

147. **Element [25.pre] recites “A method of forming an array of memory cells, comprising.”** This element is met by Chae.

148. To the extent the preamble is limiting, Chae discloses a method of

forming (*e.g.*, “method for manufacturing,” *see* [1.pre]) an array of memory cells (*e.g.*, “cell array”). *See, e.g.*, Chae:

- [0042] (“Referring to FIG. 1, ***a nonvolatile memory device according to exemplary embodiments of the inventive concept includes a cell array*** including a plurality of strings STR. The cell array includes bit lines BL1~BL3, word lines WL1~WL4, upper and lower select lines USL1~USL3 and LSL, and a common source line CSL.”)

149. *See* my discussion for element [1.pre] above (Section IX.A.2.1).

Chae further discloses its “nonvolatile memory device...includes a cell array.”

Chae, [0042].

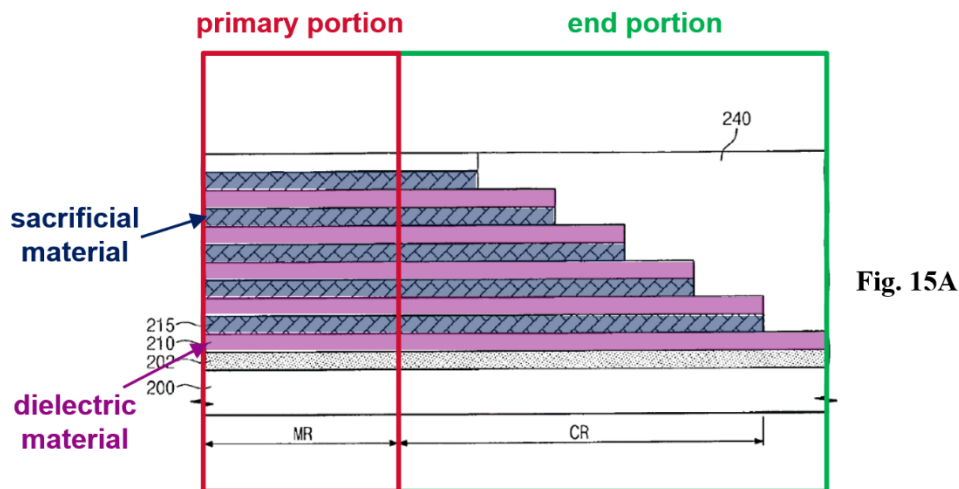
### **30. Element [25.a]**

150. **Element [25.a] recites “forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion, the end portion having sacrificial material-comprising stairs.”**

This element is met by Chae. *See* my discussion for element [1.pre] above (Section IX.A.2.1).

151. Chae discloses forming a stack of alternating (*e.g.*, “alternately stacked”) dielectric material (*e.g.*, “first dielectric layer 210”) and sacrificial material (*e.g.*, “second dielectric layer 215”), the stack comprising a primary portion (*e.g.*, “memory cell region MR”) and an end portion (*e.g.*, “contact region CR”), the end portion having sacrificial material-comprising stairs (*e.g.*, “patterned in a stair shape”). *See, e.g.*, Chae:

- Fig. 15A (annotated)



- [0123] (“Referring to FIG. 15A, first and second dielectric layers 210 and 215 with different etch selectivity are alternately stacked on a semiconductor substrate 200, and a plate-shaped stack structure is formed across a memory cell region MR and a contact region CR. That is, the sidewalls of the stacked first and second dielectric layers 210 and 215 are aligned.”)
- [0124] (“In the plate-shaped stack structure, the first and second dielectric layers 210 and 215 stacked on the contact region CR are patterned in a stair shape. That is, on the contact region CR, the stack height of the first and second dielectric layers 210 and 215 decreases toward the edge.”)
- [0129] (“Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215. Accordingly, an empty space is formed between the first dielectric layers 210 that are perpendicular to the semiconductor substrate 200 and are spaced apart from each other.”)
- [0130] (“Referring to FIG. 15D, the space between the first dielectric layers 210 may be filled with conductive material to form line-shaped gate electrodes 250.”)

152. Chae discloses forming “first and second dielectric layers 210 and

215” that are “alternately stacked.” Chae, [0123]-[0124], Fig. 15A. A person of ordinary skill in the art would have understood “second dielectric layers 215” are sacrificial because they are not included in the final product, but are instead removed and replaced with “line-shaped gate electrodes 250.” Chae, [0129]-[0130]. It was understood at the time of the ’996 patent’s filing to name such layers that are removed later in the fabrication process “sacrificial.” *See, e.g.*, Kiyotoshi, [0120], [0127]. Chae further discloses the “stack” comprises a primary portion in a “memory cell region MR” and an end portion in “a contact region CR”. Chae, [0123]. Chae also discloses “the first and second dielectric layers 210 and 215” in “the contact region CR” have “a stair shape.” Chae, [0124].

### **31. Elements [25.b], [25.c]**

153. **Element [25.b] recites “forming a plurality of first openings into the primary portion of the stack.” Element [25.c] recites “forming a plurality of second openings into the end portion of the stack.”** These elements are met by Chae.

154. Chae discloses forming a plurality of first openings (*e.g.*, “channel holes”) into the primary portion (*e.g.*, “memory cell region MR”) of the stack (*e.g.*, “stack structure”) and forming a plurality of second openings (*e.g.*, “dummy holes”) into the end portion (*e.g.*, “contact region CR”) of the stack (*e.g.*, “stack structure”). *See, e.g.*, Chae:

- [0127] (“More specifically, ***channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR.*** The channel holes and the dummy holes may be formed through a photolithography process, and the channel holes may be formed in a matrix configuration on the plane. Also, as illustrated in FIG. 5, the dummy holes may be formed respectively at one side of the channel holes located at the edge of the memory cell region MR. Also, as illustrated in FIG. 10, the dummy holes may be formed on the same line as the channel holes, and the dummy holes on the same line are spaced apart from each other. ***The dummy hole adjacent to the channel hole may penetrate all of the stacked first and second dielectric layers 210 and 215. Also, the number of the penetrated first and second dielectric layers 210 and 215 may decrease with an increase in the distance from the memory cell region MR.***”)
- [0128] (“Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b. That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the contact region CR and the active pillars 224a of the memory cell region MR. Also, the active pillars 224a and the supporters 224b may be formed to the same length. ***The active pillars 224a of the memory cell region MR may penetrate all of the stacked first and second dielectric layers 210 and 215, and the supporters 224b of the contact region CR may penetrate some of the stacked first and second dielectric layers 210 and 215.***”)

155. See my discussion for element [17.b] above (Section IX.A.2.22).

156. Chae further discloses “channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR, and that these holes “penetrate” “the stacked first and second dielectric layers 210 and 215.”

Chae, [0127]-[0128].

### 32. Element [25.d]

157. Element [25.d] recites **“simultaneously forming at least one of conductive material, semiconductive material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and forming dummy structures therewith within the second openings in the end portion.”** This element is met by Chae. See my discussions for elements [17.c] and [23] above (Section IX.A.2.23, IX.A.2.27), where “primary portion opening” of [17.c] corresponds to “first opening” and “end portion opening” of [17.c] corresponds to “second opening.”

### 33. Element [25.e]

158. Element [25.e] recites **“forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings.”** This element is met by Chae. See my discussions for elements [17.d] and [23] above (Section IX.A.2.24, IX.A.2.27), where “primary portion opening” of [17.d] corresponds to “first opening” and “end portion opening” of [17.d] corresponds to “second opening.” Furthermore, “horizontally elongated openings” of [17.d] which are formed through Chae’s “features” (*e.g.*, “first dielectric layers 210”) correspond to “horizontally elongated openings” of [25.e]

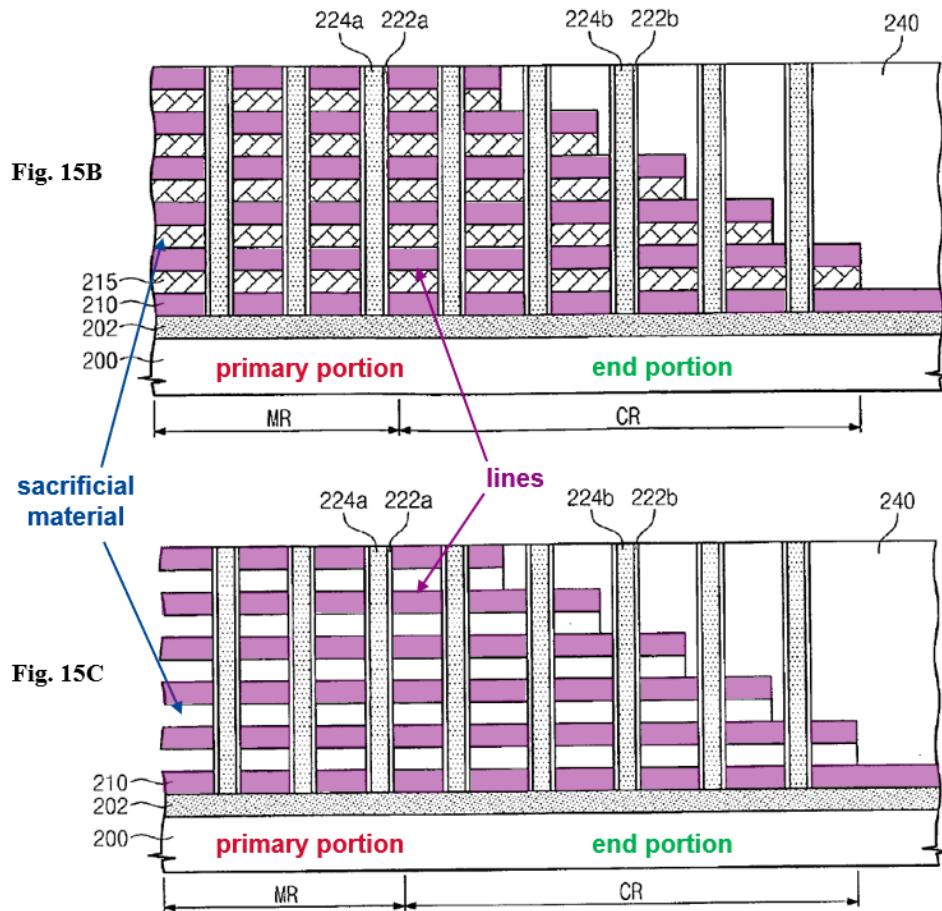
because they are also formed into Chae's "stack" (*e.g.*, "stack structure" including "first dielectric layers 210"). See also my discussion for elements [25.b], [25.c] above (Section IX.A.2.31).

### **34. Element [25.f]**

159. **Element [25.f] recites "removing at least a portion of the sacrificial material that is laterally between the horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material."** This element is met by Chae.

160. Chae discloses removing at least a portion of the sacrificial material (*e.g.*, "second dielectric layers 215") that is laterally between the horizontally elongated openings (*e.g.*, openings illustrated in Fig. 10, *see* [12.c]) selectively (*e.g.*, by having "different etch selectivity") relative to the dielectric material (*e.g.*, "first dielectric layers 210") to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material (*e.g.*, "spaces between" "line-shaped" "stacked first dielectric layers 210"). *See, e.g.*, Chae:

- Figs. 15B, 15C (annotated)



- [0129] (“Referring to FIG. 15C, the plate-shaped stack structure including the active pillars 224a and the supporters 224b are patterned to form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and 215 may be exposed. **Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.**”)
- [0130] (“Referring to FIG. 15D, **the space between the first dielectric layers 210** may be filled with conductive material to form line-shaped gate electrodes 250.”)

161. See my discussions for elements [12.c] and [25.e] above (Section IX.A.2.16, IX.A.2.33). Chae further discloses removing at least a portion of the sacrificial material (“the second dielectric layers 215”) laterally between the

openings formed in the previous step. Chae also discloses that this removing is done selectively by having sacrificial material with different etch selectivity relative to the dielectric material. Chae, [0129]-[0130]; *see also* my discussions of [12.d], [13] above. This process leads to the formation of void spaces, which are elevationally (vertically) between the layers of “dielectric material 210” that are “line-shaped” because of the openings that divide them into lines. Chae, [0129]-[0130], Figs. 15B, 15C.

### **35. Element [25.g]**

162. **Element [25.g] recites “after the removing, forming conductive material into the horizontally elongated openings and the void spaces.”** This element is met by Chae. See my discussions for elements [25.e] and [25.f] above (Sections IX.A.2.33-34).

163. Chae discloses after the removing, forming conductive material (*e.g.*, forming “conductive layer 250”) into the horizontally elongated openings (*e.g.*, “between the adjacent line-shaped stack structures”) and the void spaces (*e.g.*, “spaces between” “line-shaped” “stacked first dielectric layers 210”). *See, e.g.*, Chae:

- Fig. 10 (annotated)

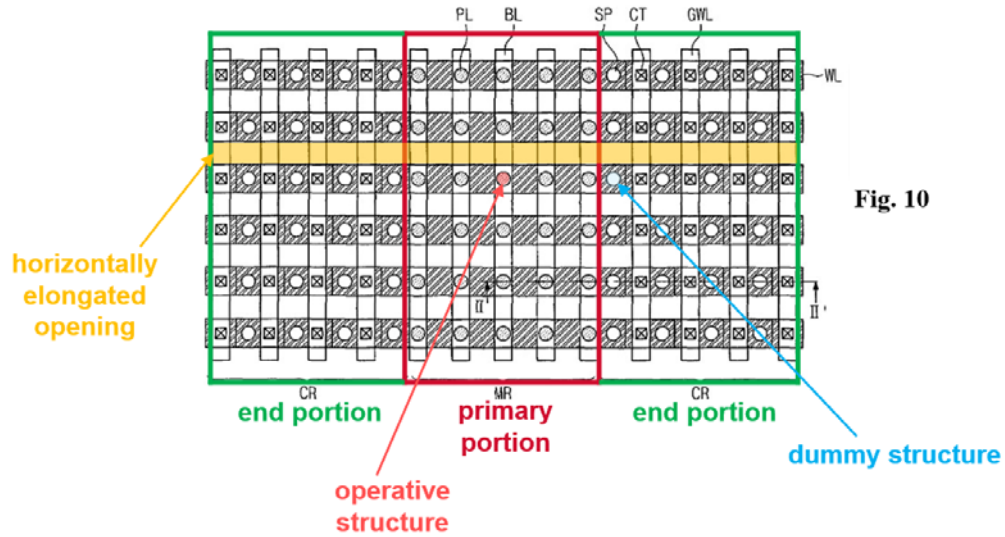


Fig. 10

- Figs. 15C, 15D (annotated)

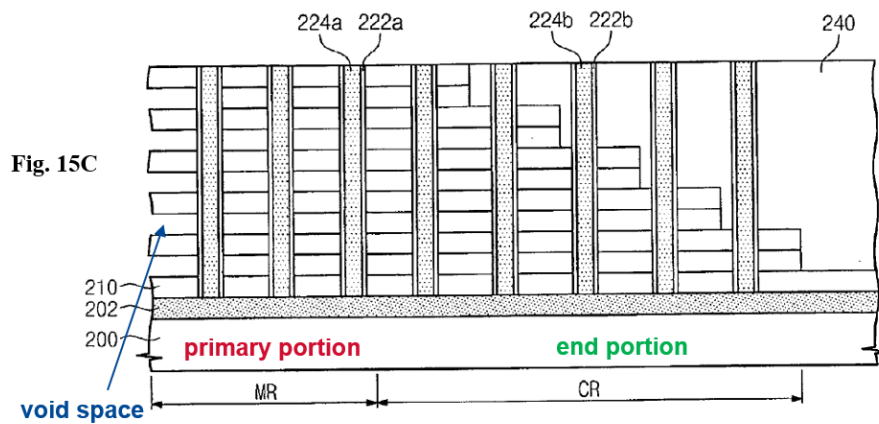


Fig. 15C

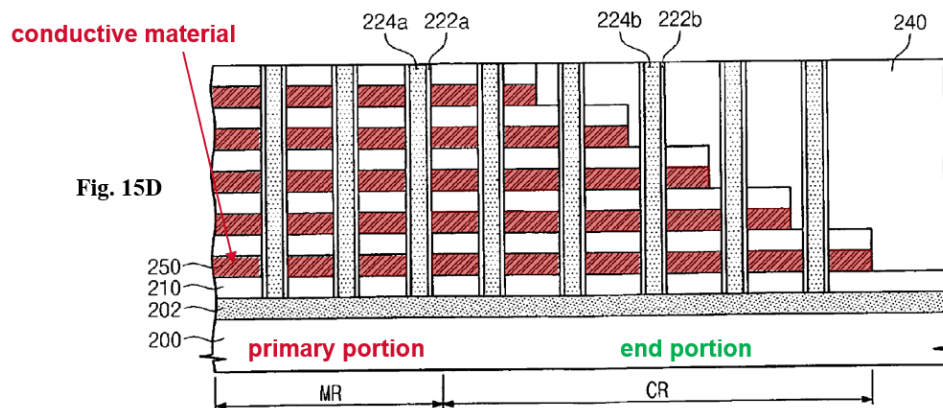


Fig. 15D

- [0129] ("Referring to FIG. 15C, the plate-shaped stack structure including the active pillars 224a and the supporters 224b are patterned to form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and

215 may be exposed. Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.”)

- [0130] (“**Referring to FIG. 15D, the space between the first dielectric layers 210 may be filled with conductive material to form line-shaped gate electrodes 250.** Specifically, when conductive material is deposited between the first dielectric layers 210, conductive layers 250 may be formed around the active pillars 224a and the supporters 224b. Thereafter, the conductive layer 250 filling the space between the adjacent line-shaped stack structures may be removed to form line-shaped gate electrodes 250 between the first dielectric layers 210.”)

164. See my discussions for elements [25.e] and [25.f] above (Section IX.A.2.33-34). Chae further discloses after removing “sacrificial layers 215,” forming “conductive layer 250” into the openings “between the adjacent line-shaped stack structures” and the void spaces “on/under the first dielectric layers 210.” Chae, [0129]-[0130], [0143]-[0144].

### **36. Element [25.h]**

165. Element [25.h] recites “**removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure.**” This element is met by

Chae.

166. Chae discloses removing at least a portion of the conductive material (*e.g.*, removing a portion of “conductive layer 250”) from the horizontally elongated openings to form vertically spaced horizontal conductive lines (*e.g.*, to form “line-shaped gate electrodes 250”) from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material (*e.g.*, from “spaces between” “line-shaped” “stacked first dielectric layers 210”), the conductive lines collectively crossing a row of the operative and dummy structures (*e.g.*, crossing row of “active pillars 224a and charge storage layers 222a” and “supporters 224b and charge storage layers 222b”) at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line (*e.g.*, intersection of “line-shaped gate electrode 250” at different heights) and an individual operative structure (*e.g.*, “active pillar 224a” with “charge storage layer 222b”). *See, e.g.*, Chae:

- Fig. 10 (annotated)

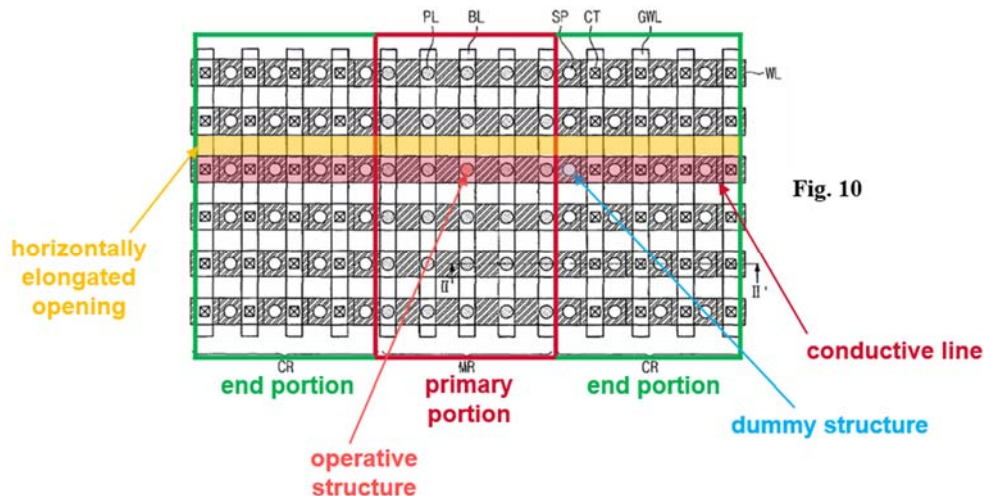


Fig. 10

- Figs. 15D (annotated)

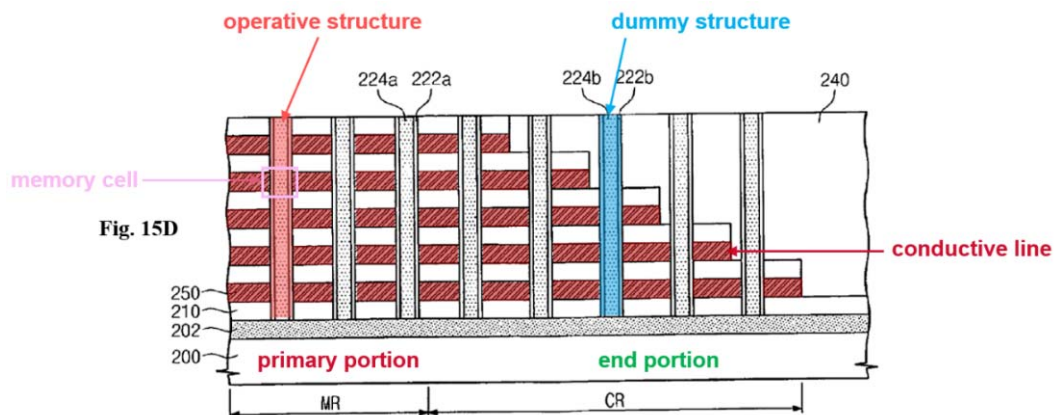


Fig. 15D

- [0054] (“Active pillars PL are formed in the memory cell region MR perpendicular to the plane of the semiconductor substrate 100. The active pillars PL are formed of semiconductor material. The active pillars PL may penetrate the gate electrodes LSL, WL and USL of the memory cell region MR. The pillars PL may be spaced apart from each other, and may be arranged in a matrix configuration on a plane. Also, the active pillars PL may be electrically connected to the impurity region 102 of the semiconductor substrate 100 by penetrating the gate electrodes LSL, WL and USL. **The active pillars PL are provided for the channels of transistors, which correspond to the strings of the nonvolatile memory device according to the embodiments of the inventive concept. That is, the channels of memory cell transistors and select transistors (LST, UST and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.**”)

- [0130] (***“Referring to FIG. 15D, the space between the first dielectric layers 210 may be filled with conductive material to form line-shaped gate electrodes 250. Specifically, when conductive material is deposited between the first dielectric layers 210, conductive layers 250 may be formed around the active pillars 224a and the supporters 224b. Thereafter, the conductive layer 250 filling the space between the adjacent line-shaped stack structures may be removed to form line-shaped gate electrodes 250 between the first dielectric layers 210.”***)

167. See my discussions for elements [25.a]-[25.g] above (Sections IX.A.2.30-35).

168. Chae further discloses “conductive layer 250 filling the space between the adjacent line-shaped stack structures” (the conductive material in the openings) “may be removed to form line-shaped gate electrodes 250” (vertically spaced horizontal conductive lines) “between the first dielectric layers 21.” Chae, [0130]. These horizontal conductive lines are vertically spaced because they are formed within the void spaces between the line-shaped “first dielectric layers 210,” i.e., the dielectric layers and the newly formed line-shaped gate electrodes are alternately stacked. Chae also discloses that “line-shaped gate electrodes 250” cross a row of the operative and dummy structures. Chae, [0128] (“active pillars 224a” with “charge storage layers 222a” and “supporters 224b” with “charge storage layers 222b”), Fig. 10. Because the conductive lines are vertically stacked, they cross a row of the operative and dummy structures at different respective elevations. Fig. 15D. Chae teaches that the “active pillars” are “channels of transistors” and “correspond to” vertical “strings of the nonvolatile memory device.” *Id.*, [0054].

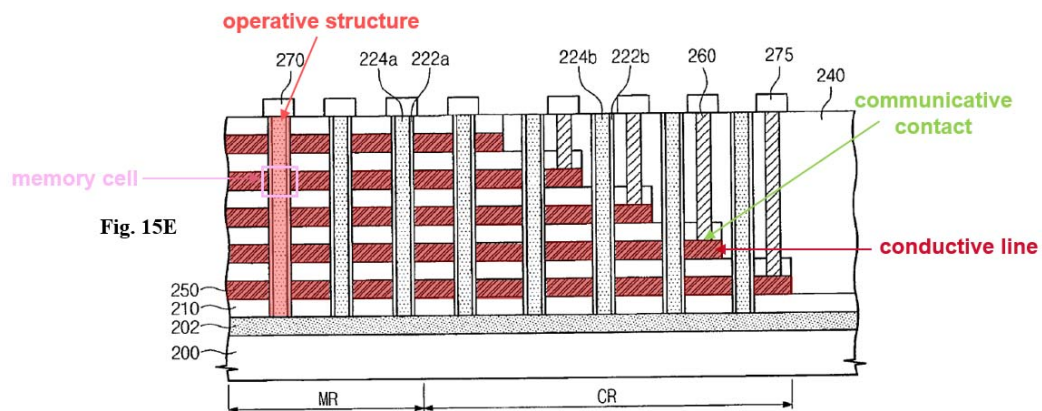
Therefore, memory cells exist at each intersection of an individual “line-shaped gate electrode 250” and an individual “active pillar 224”–“charge storage layer 222a” combination.

### 37. Element [25.i]

169. Element [25.i] recites “forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion.” This element is met by Chae.

170. Chae discloses forming a respective communicative contact (e.g., forming “contact plugs 260”) to a stair extension of individual ones of the horizontal conductive lines (e.g., portion of “line-shaped gate electrodes 250” “formed in a stair shape”) in the end portion (e.g., “contact region CR”). See, e.g., Chae:

- Fig. 15E (annotated)



- [0131] (“Referring to FIG. 15E, contact plugs 260, connected respectively to the gate electrodes 250 of each layer, are formed in the contact region CR of the gate electrodes 250.”)

- [0132] (***“Because the gate electrodes 250 of the contact region CR are formed in a stair shape, the contact plugs 260 may differ in length.”***)

171. See my discussions for element [25.h] above (Section IX.A.2.36).

Chae further discloses forming “contact plugs 260, connected respectively to the gate electrodes 250 of each layer,” “in the contact region CR of the gate electrodes 250.” Chae, [0131]. Chae discloses “contact plugs 260” form communicative contact with stair extensions of individual “line-shaped gate electrodes 250.” *Id.*, [0131], Fig. 15E.

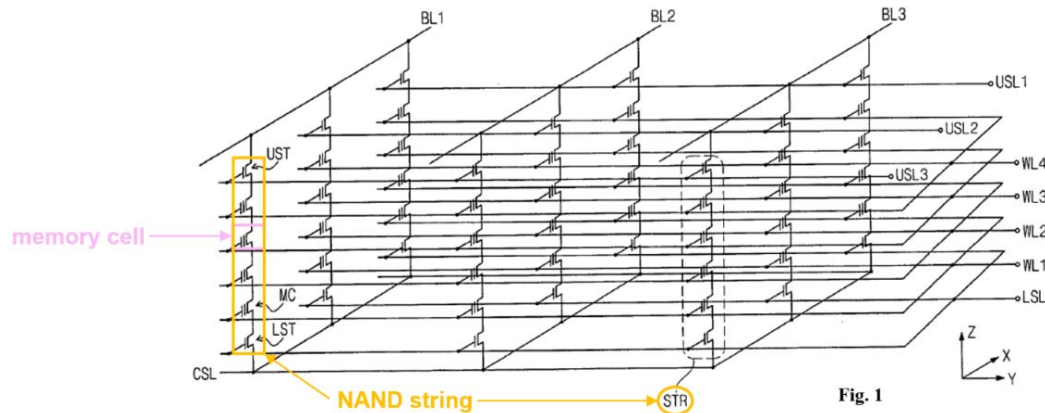
### **38. Claim [26]**

172. **Claim 26 recites “The method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel regions of a NAND string.”** See my discussion for claim 25 above (Sections IX.A.2.29-37). The limitation added by claim 26 is met by Chae.

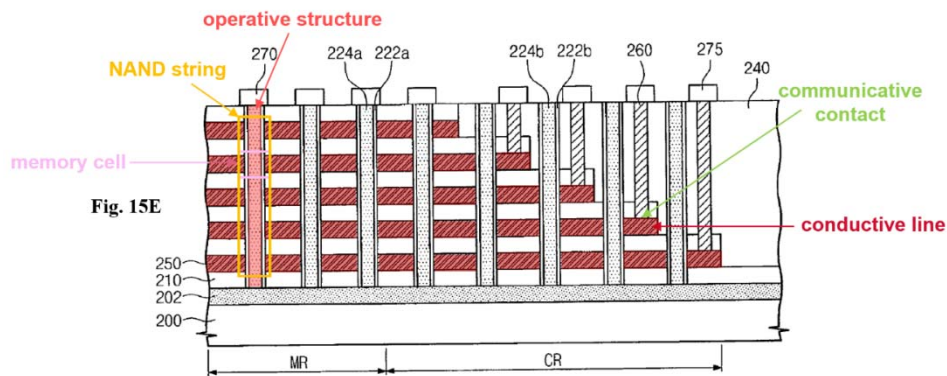
173. Chae discloses the memory cells (*e.g.*, “memory cells MC”; “memory cell transistors MC”) comprise a portion of NAND architecture (*e.g.*, comprise a portion of the “NAND-type nonvolatile memory device”), the at least one formed material (*see* [25.d]) comprises semiconductive material (*e.g.*, “semiconductor material”), and the operative structures (*e.g.*, “active pillars 224a” with “charge storage layers 222a”) comprise interconnected channel regions of a NAND string

(e.g., “string STR”). See, e.g., Chae:

- Fig. 1 (annotated)



- Fig. 15E (annotated)



- [0005] (“In particular, *the NAND-type nonvolatile memory device is advantageous for high integration because it includes a cell string structure having a plurality of memory cell transistors connected in series.*”)
- [0043] (“*Each string STR includes upper and lower select transistors UST and LST, and memory cell transistors MC that are connected in series between the upper and lower select transistors UST and LST. The drains of the upper select transistors UST are connected to the bit lines BL1~BL3, and the sources of the lower select transistors LST are connected in common to the common source line CSL.*”)
- [0054] (“Active pillars PL are formed in the memory cell region MR perpendicular to the plane of the semiconductor substrate 100. The active

pillars PL are formed of semiconductor material. The active pillars PL may penetrate the gate electrodes LSL, WL and USL of the memory cell region MR. The pillars PL may be spaced apart from each other, and may be arranged in a matrix configuration on a plane. Also, the active pillars PL may be electrically connected to the impurity region 102 of the semiconductor substrate 100 by penetrating the gate electrodes LSL, WL and USL. ***The active pillars PL are provided for the channels of transistors, which correspond to the strings of the nonvolatile memory device according to the embodiments of the inventive concept. That is, the channels of memory cell transistors and select transistors (LST, UST and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.***")

- [0041] (***"FIG. 1 is a circuit diagram of a nonvolatile memory device according to exemplary embodiments of the inventive concept."***)
- [0121] (***"Another method for fabricating the nonvolatile memory devices according to the second and fifth exemplary embodiments of the inventive concept will be described below with reference to FIGS. 15A to 15E."***)
- [0004] (***"Nonvolatile memory devices include various types of memory cell transistors. Nonvolatile memory devices are classified into NAND-type nonvolatile memory devices and NOR-type nonvolatile memory devices, depending on the cell array structures. The NAND-type nonvolatile memory device and the NOR-type nonvolatile memory device have the advantages and disadvantages of high integration and high operation speed."***)
- [0042] (***"Referring to FIG. 1, a nonvolatile memory device according to exemplary embodiments of the inventive concept includes a cell array including a plurality of strings STR. The cell array includes bit lines BL1~BL3, word lines WL1~WL4, upper and lower select lines USL1~USL3 and LSL, and a common source line CSL. The strings STR are provided between the common source line CSL and the bit lines BL1~BL3."***)
- [0044] (***"The upper select transistors UST are connected to the upper select lines USL1~USL3, and the lower select transistors LST are connected respectively to the lower select lines LSL. The memory cells MC are connected respectively to the word lines WL1~WL4."***)

- [0045] (“The cell array has a three-dimensional structure. That is, the strings STR are configured in such a way that the memory cells MC are connected in series in a Z-axis direction perpendicular to an XY plane parallel to the top surface of a semiconductor substrate. Accordingly, the channel of the memory cell transistors MC and the select transistors UST and LST may be formed perpendicular to the XY plane.”)

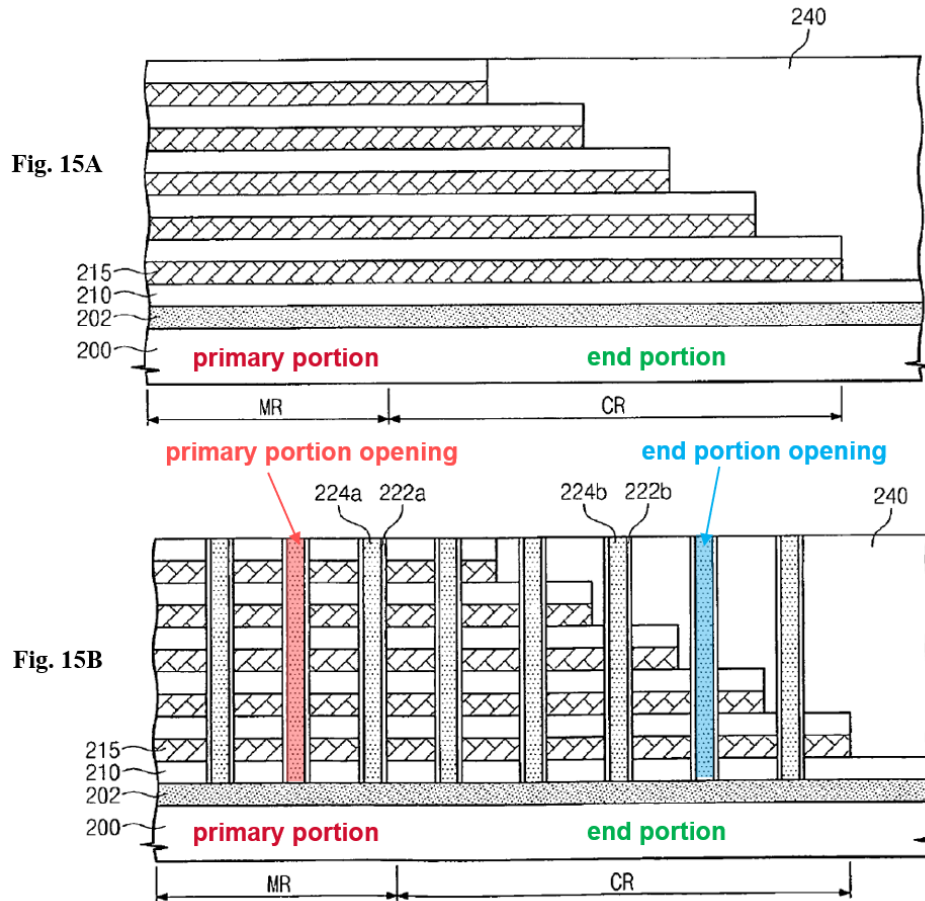
174. As I explain in my discussions for elements [9] and [25.d], Chae discloses its “active pillars 224a” comprise “semiconductor material” (*see also* my discussion of element [25.d]) and constitute interconnected channels of memory cell transistors, which are connected in series to form strings. Sections IX.A.2.11, IX.A.2.32. Chae further discloses a “NAND-type nonvolatile memory device” including “a cell string structure,” such that each memory cell transistor string is a NAND string. Chae, [0005]. Therefore, Chae’s “active pillars 224a” comprise interconnected channel regions of a NAND string.

### 39. Claim [28]

175. **Claim 28 recites “The method of claim 25 comprising forming the first and second openings using the same masking step.”** See my discussion for claim 25 above (Sections IX.A.2.29-37). The limitation added by claim 28 is met by Chae.

176. Chae discloses forming the first and second openings (*e.g.*, “channel holes” and “dummy holes”) using the same masking step (*e.g.*, using masking as part of “photolithography”). *See, e.g.*, Chae:

- Figs. 15A, 15B (annotated)



- [0099] (“Referring to FIG. 13F, after the forming of the gate electrodes on the semiconductor substrate 100, a dielectric layer 160 may be formed to fully cover the stacked gate electrodes. Active pillars 174 penetrating the stacked gate electrodes, and a charge storage layer 172 surrounding the active layers 174, may be formed in the memory cell region MR. Specifically, a plurality of channel holes are formed to penetrate the interlayer dielectrics 110 and the conductive layers 122 stacked in the memory cell region MR. **The channel holes may be formed by forming a mask pattern (not illustrated) on the uppermost dielectric layer 150 and selectively and anisotropically etching the stacked interlayer dielectrics 110 and conductive layers 122 by means of the mask pattern.** The formed channel holes may expose the impurity region 102 of the semiconductor substrate 100. Also, the channel holes may be formed in a matrix configuration on the plane.”)
- [0127] (“More specifically, channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR. **The**

***channel holes and the dummy holes may be formed through a photolithography process, and the channel holes may be formed in a matrix configuration on the plane.*** Also, as illustrated in FIG. 5, the dummy holes may be formed respectively at one side of the channel holes located at the edge of the memory cell region MR. Also, as illustrated in FIG. 10, the dummy holes may be formed on the same line as the channel holes, and the dummy holes on the same line are spaced apart from each other. The dummy hole adjacent to the channel hole may penetrate all of the stacked first and second dielectric layers 210 and 215. Also, the number of the penetrated first and second dielectric layers 210 and 215 may decrease with an increase in the distance from the memory cell region MR.”)

177. See my discussions for elements [25.b] and [25.c]. Chae discloses “channel holes and the dummy holes may be formed through a photolithography process,” which is a process that involves masking. *See, e.g.*, [0099] (describing the formation of the same channel holes in a different embodiment as “[t]he channel holes may be formed by forming a mask pattern”). A person of ordinary skill in the art would have understood (and found it obvious) that forming the “channel holes” and “dummy holes” using the same “photolithography process” would also use the same masking step. This would have had the advantage of minimizing the number of processing steps required. As I note above in connection with claim [18] (above, Section IX.A.2.26), minimizing the number of processing steps was recognized as advantageous in the art. *See* Ex. 1017, [0034], [0036], [0042], [0043], [0142].

#### **40. Claim [30]**

178. **Claim 30** recites “The method of claim 25 wherein the sacrificial

**material is dielectric.”** See my discussion for claim 25 above (Sections IX.A.2.29-37). The limitation added by claim 30 is met by Chae.

179. Chae discloses the sacrificial material (*e.g.*, “second dielectric layer 215”) is dielectric.

180. See my discussion for element [25.a] (Section IX.A.2.30).

#### **41. Claim [32]**

181. **Claim 32 recites “The method of claim 25 wherein the features comprise plates.”** This claim is met by Chae. See my discussions for claims 6 and 25 above (Sections IX.A.2.8, IX.A.2.29-37).

### **B. GROUND 2: Chae in view of Kiyotoshi (Claims 1-4, 18, 23, 25-26, 28, 30, 32)**

#### **1. Overview of Kiyotoshi**

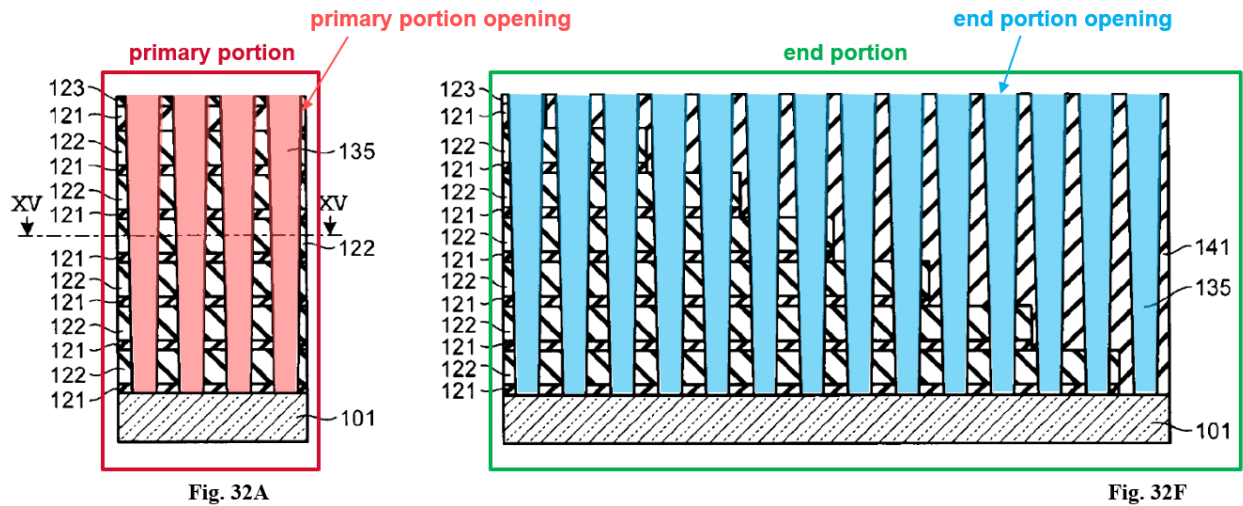
182. Kiyotoshi is directed to a method for manufacturing “nonvolatile semiconductor memory devices” in which a “stacked film in the **memory cell region** and the **word-line contact region** is collectively processed by the lithography technique and RIE method to form the **through-holes 135.**”

Kiyotoshi, [0019], [0123]. “Semiconductor films 131” in the memory cell and word-line contact regions are “deposited in the **through-holes 135** and formed such that the lower ends thereof are connected to the semiconductor substrate 101.”

*Id.*, [0124]. Subsequently, “dielectric films 132 formed of a silicon oxide film or the like are formed to fill the inside of the hollow cylindrical semiconductor films



region and the word-line contact region is collectively processed by the lithography technique and RIE method to form the through-holes 135” in both regions simultaneously. Kiyotoshi, [0123].

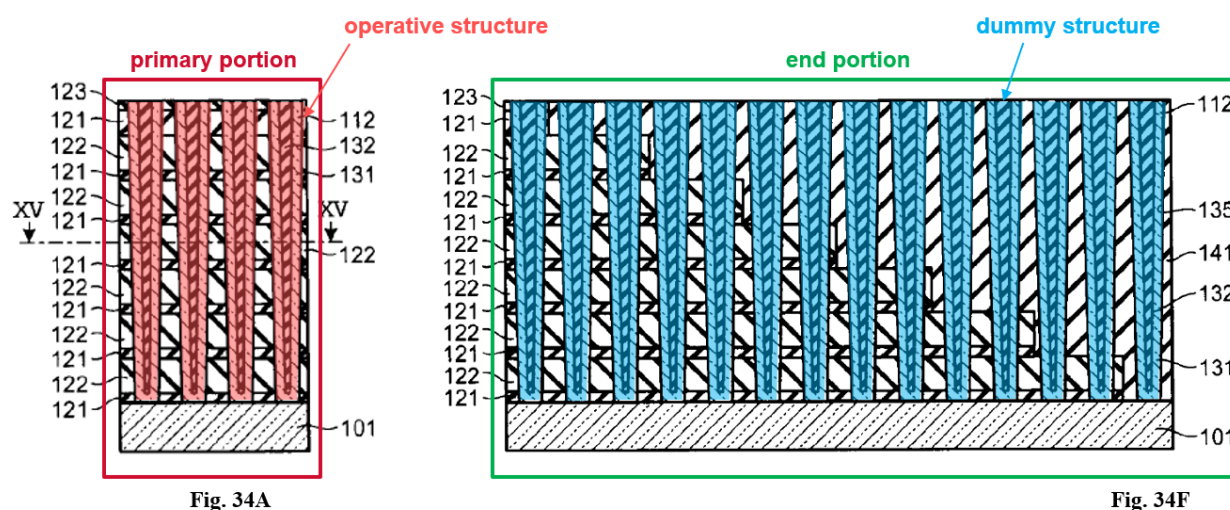


Kiyotoshi, Figures 32A and 32F.

185. To the extent further disclosure of depositing a semiconductive material simultaneously in primary portion openings and end portions openings (claim 23) to simultaneously form operative and dummy structures (claim 25) is needed, Kiyotoshi discloses forming “semiconductor films 131” and “dielectric films 132” in “through holes 135” (both in the memory cell region and the word-line contact region) using a “film forming method such as the LPCVD method.” Kiyotoshi, [0124]-[0125]. Kiyotoshi’s “semiconductor films 131” and “dielectric films 132” collectively constitute operative structures in “memory cell region” because they form “memory strings MS;” however in “word-line contact region,” they “do not form the memory strings MS” and hence are dummy structures.

Kiyotoshi, [0116].

186. Because Kiyotoshi discloses forming “semiconductor film 131” followed by “dielectric film 132” “to fill the inside of the hollow cylindrical semiconductor films 131” in order to form the operative and dummy structures, it discloses that the operative and dummy structures comprise the same material (claim 2) and a plurality of the same materials, i.e., “semiconductor film 131” and “dielectric film 132” (claim 3), wherein the same materials are arranged in the same lateral order (claim 4). Kiyotoshi, [0124]-[0125], Fig. 34A, 34F. Similarly, for element [1.b], to the extent further disclosure of the supporters 224b mimicking a physical property of the active pillars 224a is needed (to meet the “dummy structure” limitation) on the basis that the supports 224b and active pillars 224a are formed of different materials, it would have been obvious to form the structures of the same materials, as Kiyotoshi expressly teaches.



Kiyotoshi, Figures 34A and 34F.

187. Furthermore, because claims 26, 30, and 32 depend from claim 25, Chae in view of Kiyotoshi renders these claims obvious for the same Ground 1 reasons Chae discloses them or at least renders them obvious, as I explain in my discussion in Section IX.A.2.

### **3. Motivation to Apply Kiyotoshi's Teachings to Chae**

188. Chae and Kiyotoshi are analogous art, in the same field as the '996—which includes the field of manufacturing nonvolatile memory devices. '996, 1:8-10, Chae, [0002]; Kiyotoshi, [0019]. Moreover, Chae and Kiyotoshi are pertinent to the purported problem addressed by the '996 of supporting dielectric layers while replacing sacrificial layers between the dielectric layers with gate layers. '996, 7:25-35; Chae, [0129]; Kiyotoshi, [0127].

189. With respect to claims 18 and 28, a person of ordinary skill in the art would have been motivated to apply Kiyotoshi's teaching of forming the primary portion openings (first openings) and the end portion openings (second openings) at the same time (using the same masking step) to Chae's method to simplify the process and advantageously reduce the number of processing steps. Reducing the number of processing steps would have been advantageous because it would have reduced the chance of defects and shortened the manufacturing time, allowing higher fabrication yield. For example, in the context of the use of lithography in fabricating memory devices, it was recognized that additional processing steps

adds additional defects and reduces yield. For example, in a 2009 article for the well-known and readily accessible *IEEE Spectrum* publication (that would have been accessible to a person of ordinary skill in the art, e.g., through the IEEE website or a library) titled “Shrinking Possibilities,” B. Arnold identifies the importance of minimizing the number of masking steps: “Double patterning also demands more process steps, which again adds to the cost by cutting effective throughput, increasing fab cycle time, and adding additional defects. If your original process could yield 100 wafers an hour, using double patterning will leave you with much less. If you’d been turning a profit at 100 per hour, there’s no guarantee you will at 50.” Ex. 1010.

190. Moreover, Chae discloses that “channel holes and the dummy holes may be formed through a photolithography process.” Chae, [0127].

Photolithography is a process of using a mask to etch material from a semiconductor device in a desired pattern. See Ex. 1011 (U.S. Patent No. 8,039,176, titled “Method for fracturing and forming a pattern using curvilinear characters with charged particle beam lithography”) at 1:28-32 (“Optical lithography is a printing process in which a lithographic mask or photomask manufactured from a reticle is used to transfer patterns to a substrate such as a semiconductor or silicon wafer to create the integrated circuit.”). Thus, a person of ordinary skill in the art would have found it straightforward to use a single mask to

form holes in both channel and dummy holes as taught by Kiyotoshi when performing Chae's photolithography process.

191. Thus, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Kiyotoshi's teaching of using a single mask process to form through-holes to Chae's memory device fabrication process, and would have known such combination (yielding the claimed limitations) would predictably work and provide the expected resulting structure.

192. With respect to claims 23 and 25, a person of ordinary skill in the art would have been motivated to apply Kiyotoshi's teaching of depositing semiconductive material simultaneously into the primary portion openings (first openings) and the end portion openings (second openings) to Chae's method to simplify the process and advantageously reduce the number of processing steps. As I noted above in connection with claims 18 and 28, fewer processing steps would have been advantageous because it would have reduced the chance of defects and shortened the manufacturing time.

193. Chae discloses that "the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b." Chae, [0128]. A person of ordinary skill in the art would have found it straightforward to apply Kiyotoshi's express disclosures to form semiconductor material in channel and dummy holes simultaneously when forming these

structures in Chae's fabrication process. Although Kiyotoshi teaches forming charge storage layers after filling the holes with semiconductive material (followed by dielectric material) and Chae teaches forming charge storage layers in the holes before forming the semiconductive material, this difference is not relevant to Kiyotoshi's teaching about forming the semiconductive material in the holes simultaneously. Regardless of the order in which the layers are deposited, the advantage of forming layers in holes at the same time remains the same. A person of ordinary skill in the art would have found this teaching of filling the holes simultaneously with semiconductive material to be applicable to Chae.

194. With respect to claims 1-4, a POSITA would have been motivated to apply Kiyotoshi's teaching of forming the operative and dummy structures using the same semiconductor and dielectric materials with the same lateral order to Chae's method to simplify the process and advantageously reduce the number of materials used.

195. Thus, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Kiyotoshi's teaching of simultaneously forming operative and dummy structures to Chae's memory device fabrication process, and would have known such combination (yielding the claimed limitations) would predictably work and provide the expected resulting structure.

### C. GROUND 3: Chae in view of Hwang (Claim 22)

#### 1. Overview of Hwang

196. Hwang is directed to methods of manufacturing three-dimensional memory devices. Hwang, [0002]-[0003]. Hwang discloses forming a stack of “inter-layer insulating layers 120” and “lower sacrificial layers 130” which are “laminated alternately and repeatedly” in a “cell array region CAR” and “contact regions UWCTR and LWCTR.” *Id.*, [0032]-[0033]. Within the contact regions, “a terraced shape is formed” by “patterning.” *Id.*, [0036].

197. Hwang further discloses that “lower through-holes 140 are formed in the cell array region CAR to penetrate the lower thin film structure 100, and then lower semiconductor patterns 150 are formed in the lower through-holes 140.” Hwang, [0044]. Similarly, “supporting members 175 are formed perpendicular to the substrate 10” “in the lower word line contact region LWCTR.” *Id.*, [0119]. The “supporting members 175 may prevent and/or reduce collapse of the lower inter-layer insulating layers 120...in the subsequent process of removing the lower sacrificial layers 130.” *Id.*, [0120].

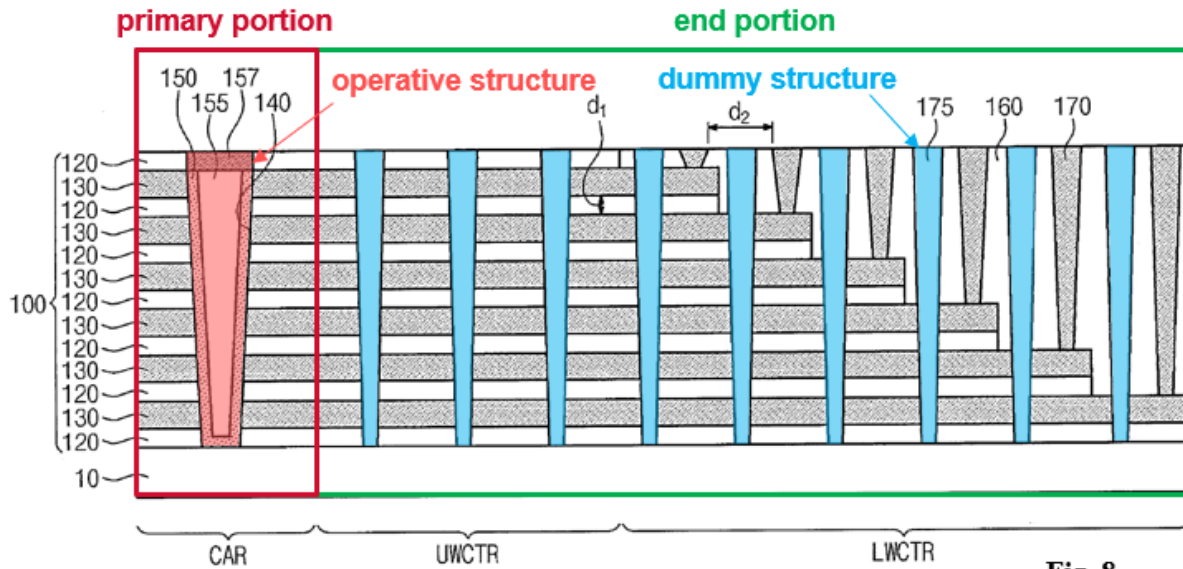


Fig. 8

Hwang, Figure 8.

## 2. Invalidity of Claim 22 Over Chae in view of Hwang

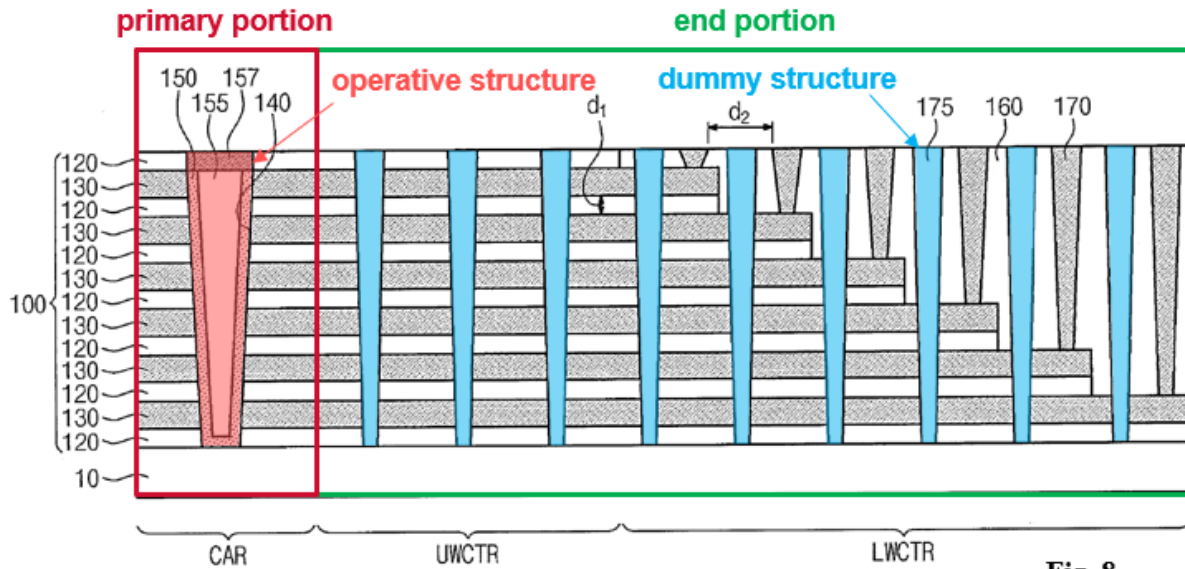
198. As discussed in §IX.A, Chae anticipates and at least renders obvious claim 17. **With respect to claim 22 (dependent from claim 17), Hwang discloses forming the primary portion openings (e.g., “lower through-holes 140”) and the end portion openings (e.g., openings that are filled to form “supporting members 175”) to have at least one of different horizontal cross sections or different vertical cross sections (e.g., different widths).**

199. Hwang discloses that “lower through-holes 140 are formed in the cell array region CAR.” Hwang, [0044]. Then, a semiconductor material is deposited to form “semiconductor patterns 150” in through-holes 140 in the cell array region with a “hollow cylindrical shape substantially covering the inner sidewalls of the

lower through-holes 140,” thereby partially filling the holes. *Id.*, [0044], [0047].

Hwang also discloses that “supporting members 175” are formed in the contact region and “formed together with the lower semiconductor patterns 150” of the cell array region. *Id.*, [0119]. A person of ordinary skill in the art would have understood from Hwang’s teachings that supporting members 175 are formed by forming holes in the contact region and then filling them. For example, Figure 8 of Hwang illustrates the holes are completely filled with supporting members 175, and Hwang does not teach any further material being filled into the holes in the contact region. Subsequently, the remainder of the through-holes 140 lined with “semiconductor patterns 150” are filled with “buried patterns 155,” thereby completing the filling of the through-holes 140. *Id.*, [0050], [0119], Fig. 8. Hwang also teaches that the filling of these holes with semiconductor material occurs “by an epitaxial technique and/or chemical vapor deposition.” *Id.*, [0047]. A person of ordinary skill in the art would have understood that an epitaxial technique and/or chemical vapor deposition result in films with uniform thickness, i.e., the same amount of material sticks to the same amount of surface area across the surface onto which the material is deposited. For example, in a book chapter titled “Epitaxial Layer Characterization and Metrology” in a textbook titled *Semiconductors and Semimetals* published by Academic Press in 2001, which would have been accessible to a person of ordinary skill in the art, e.g., at a library,

V.-M. Airaksinen recognized epitaxial growth is used to produce a uniform layer, noting that “[t]he purpose of epitaxy is to grow a silicon layer of uniform thickness and accurately controlled electrical properties and so provide a perfect substrate for the subsequent device processing.” Ex. 1012, p. 2. Similarly, in a book chapter titled “Chemical Vapor Deposition” in a book titled *Handbook of Deposition Technologies for Films and Coatings* published by Elsevier Science in 2010, which would have been accessible to a person of ordinary skill in the art, e.g., at a library, J.-O. Carlsson and P. M. Martin noted that CVD provides layers of uniform thickness, explaining that “[a] characteristic feature of the CVD technique is its excellent throwing power, enabling the production of **coatings of uniform thickness** and properties with a low porosity even on substrates of complicated shape.” Ex. 1013, pp. 1-3. Because the same amount of semiconductor material completely fills the holes in the end portion to form “supporting members 175” but it forms “lower semiconductor patterns 150” which only partially fill respective through-holes 140, the through-holes 140 have a greater width than the holes in the end portion, consistent with the depictions of Fig. 8—and at minimum it would have been obvious to have greater width to accommodate the material but not fill the through-holes 140.



Hwang, Figure 8.

### 3. Motivation to Apply Hwang's Teachings to Chae

200. Chae and Hwang are analogous art, in the same field as the '996, which includes methods for manufacturing nonvolatile memory devices. Chae, [0002]; Hwang, [0002]. Moreover, Chae and Hwang are pertinent to the purported problem solved by the '996 of supporting dielectric layers while replacing sacrificial layers between the dielectric layers with gate layers. '996, 7:25-35; Chae, [0129]; Hwang, [0120].

201. A person of ordinary skill in the art would have been motivated to apply Hwang's teaching of forming holes in the contact region to have smaller widths than holes in the memory cell array region to Chae's method of forming a memory device so that the memory device would be reduced in size. Hwang,

[0120]. Hwang’s teaching of smaller holes for dummy structures enables Chae’s device to have a smaller contact region. At the time of the ’996 patent’s filing, it was desired in the art to make memory devices smaller. For example, U.S. Patent No. 8,397,132 notes the objective of “decreas[ing] the size and cost of a memory device.” Ex. 1018, 1:41-44. *See, also*, Ex. 1010 (“That map was, and is, a collection of the global semiconductor industry’s best ideas about how it was going to fulfill the Moore’s Law prophecy of a 30 percent shrink in transistor size—and consequent doubling in density—on chips every two years.”). By making Chae’s contact region smaller, a person of ordinary skill in the art would have directly contributed to this goal. Moreover, Hwang’s supporting members serve the same function as Chae’s supporters because they “prevent and/or reduce collapse of the lower inter-layer insulating layers 120 and the lower insulating layers 160 in the subsequent process of removing the lower sacrificial layers 130.” Hwang, [0120].

202. Thus, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Hwang’s teaching of smaller dummy structures to Chae’s memory device fabrication process, and would have known such a combination (yielding the claimed limitations) would predictably work and provide the expected resulting structure.

## **D. GROUND 4: Chae in view of Pekny (Claims 12-13, 16)**

### **1. Overview of Pekny**

203. Pekny is directed to “methods of forming memory arrays.” Pekny, Abstract. Pekny discloses forming “alternating dielectric layers 222 and conductive layers 224” in a “memory cell portion 220.” Pekny, 5:8:29. Pekny also discloses forming “holes 226...passing through dielectric layers 222 and conductive layers 224,” which are then filled to form “conductive pillars 230.” *Id.*, 5:30-52. Pekny discloses subsequently forming “slots 410” in “dielectric layers 222 and conductive layers 224,” resulting in “isolated activation lines, such as word lines.” Pekny, 6:1-25.

### **2. Invalidity of Claims 12-13 and 16 Over Chae in view of Pekny**

204. As discussed in §IX.A, **Chae** anticipates and at least renders obvious claim 12. To the extent that further disclosure is required, **Chae** in view of **Pekny** renders this claim obvious.

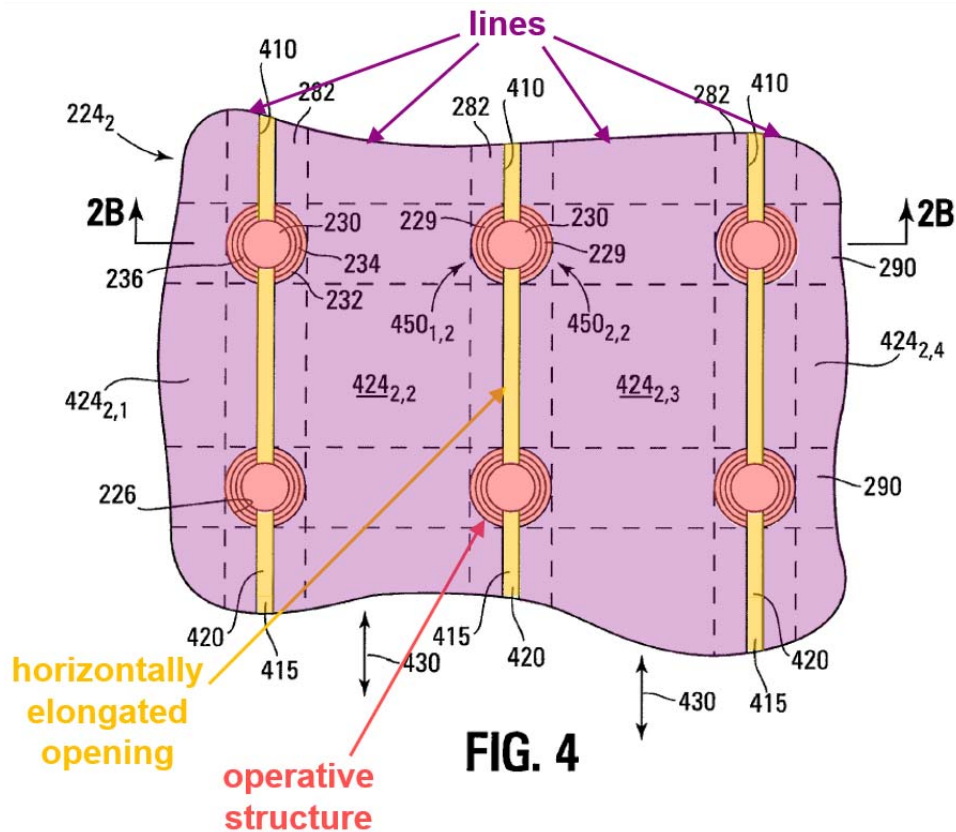
205. Limitation [12.c] requires “forming horizontally elongated openings through the structures.” **To the extent the limitation requires the elongated openings to pass directly through the structures, this is disclosed by Pekny.**

206. Pekny discloses forming horizontally elongated openings (*e.g.*, “slots 410”) through the structures (*e.g.*, “conductive pillar 230,” “oxide layer 232,” “nitride layer 234,” and “oxide layer 236”) to form horizontally elongated and

vertically overlapping lines from material of the features (*e.g.*, lines of “dielectric layers 222”), the lines individually extending...laterally about sides of vertically extending portions of the operative structures (*e.g.*, “conductive pillars 230”).

While Pekny does not illustrate dummy structures, as noted below, when applying Pekny’s relevant teachings to Chae, the openings would extend about sides of vertically extending portions of the dummy structures.

207. Pekny discloses forming horizontally elongated “slots 410” in “dielectric layers 222 and conductive layers 224” thereby forming these layers into line-shaped stacks. Pekny, 6:1-42. The line-shaped stacks extend laterally about sides of the operative structures that each comprise “conductive pillar 230,” “oxide layer 232,” “nitride layer 234,” and “oxide layer 236.” Pekny, 6:31-42, Fig. 4. Pekny’s slots 410 pass through the operative structures. Pekny, Fig. 4. Slots 410 are then “filled with a dielectric material 415” to form “isolation regions 420” which “cut each conductive layer 224 into electrically isolated activation lines, such as word lines, 424.” Pekny further explains that “[e]ach isolation region 420 extends between conductive pillars 230 in a direction transverse to the depth of that isolation region 420, *e.g.*, in a direction substantially parallel to the word-line direction indicated by arrows 430.” Pekny, 6:1-42.



Pekny, Figure 4.

208. Furthermore, because claims 13 and 16 depend from claim 12, Chae in view of Pekny renders these claims obvious for the same Ground 1 reasons Chae discloses them or at least renders them obvious, as I discussed in Section IX.A.2.

### 3. Motivation to Apply Pekny's Teachings to Chae

209. Chae and Pekny are analogous art, in the same field as the '996, which includes methods for manufacturing nonvolatile memory devices. Chae, [0002]; Pekny, Abstract.

210. A person of ordinary skill in the art would have been motivated to apply Pekny's teaching of forming a slot through the pillars to Chae because it

would double the number of memory cells. Pekny explains that “[c]utting a charge trapping layer 228 with an isolation region 420 forms a pair of isolated memory cells 450<sub>1,2</sub>, 450<sub>2,2</sub>,” therefore, the number of charge traps—and thus, the number of memory cells—doubles. Pekny, 6:43-49. This would advantageously increase the memory storage capacity in the same volume, *i.e.*, density. Pekny, 1:56-60. At the time of the ’996 patent’s filing, increasing the number of memory cells in the same volume was highly desired in the field. *See, e.g.*, Ex. 1010 (“Memory makers focused on reducing the size of each memory cell on their chips so that they could squeeze ever more bits into less and less real estate.”).

211. Moreover, because Chae’s slots are linear and formed through the primary portion and the end portion, and the operative and dummy structures are linearly arranged, when applying Pekny’s teaching of forming slots through the operative structures, a person of ordinary skill in the art would have formed slots through both the operative and dummy structures in Chae’s device, such that the resulting lines would extend laterally about sides of vertically extending portions of the pillars 224a (operative structures) and 224b (dummy structures).

212. A person of ordinary skill in the art would have found the application of Pekny’s teaching of forming slots that pass through operative structures to Chae’s memory fabrication process straightforward. For example, while Chae teaches forming the select gates in the same process as gate electrodes for the

memory cells (Chae, [0129]-[0130], Figs. 15C-15D), a person of ordinary skill in the art would have recognized that shifting Chae's slots as taught by Pekny would cause a misalignment between the pillars 224a and the select gates, impacting the ability to obtain double the number of memory cells. Pekny teaches a solution to this problem, which a person of ordinary skill in the art would have recognized. In particular, Pekny teaches a three-stage fabrication process: (1) a "source-select-gate portion 201" is formed on the substrate (Pekny, 4:11-13, Fig. 2A); (2) a "memory cell portion 220" is formed on top of the previously formed layers (Pekny, 5:8-10, Fig. 2B); (3) a "drain-select-gate portion 250" is formed on the previously formed layers (Pekny, 7:14-16, Fig. 2C). A person of ordinary skill in the art would have used Pekny's method for stages (1) and (3), and apply Pekny's teachings regarding the slot to Chae's method for stage (2). According to Pekny, the select gate structure below the memory cells and aligned with operative structures (including conductive pillar 230, oxide layer 232, nitride layer 234 and oxide layer 234) is formed before memory cells are formed, and the slots between word lines do not extend down to the lower select gates. Pekny, 6:1-9. This teaching is also applicable to Chae. Thereafter, the word lines would be formed using the process described by Chae, with the modification that the patterns on an etch mask used in the photolithography process to create the slot structures would be shifted so that the exposed regions for etching pass through the charge storage

layers (222a or 222b). Chae, [0129]. This would result in the increased memory cell density taught by Pekny. In this regard, as Pekny teaches, the memory cell fabrication process would not impact the lower select gates. Pekny, 5:8-10, 6:1-9, Figs. 2A-2B. Thereafter, the upper select lines would be formed directly above the operative structures and aligned with the lower select lines, using, e.g., a process similar to that taught by Pekny. Pekny, 7:15-17, Fig. 2C.

213. Moreover, a person of ordinary skill in the art would have understood that the steps after forming the slots through the operative structures would not negatively impact other structures in the device. In Chae, slots are involved in further processing, and forming them through the operative structures would not have disturbed these steps. In particular, after the slots are formed, (1) dielectric layers 215 are removed by using the slots to supply the etchant, (2) conductive material is deposited in their place through the slots, (3) the conductive material remaining in the slots is removed, and (4) the slots are filled with dielectric material. Chae, [0129]-[0130]. With respect to (1), a POSITA would have recognized that using silicon nitride for both the sacrificial dielectric layers 215 and the charge storage layers 222a and 222b as taught by Chae could potentially cause the charge trap layer to be selectively removed with the sacrificial material when the slot is shifted to pass through Chae's operative and dummy structures. Chae, [0107]. Thus, to obtain the benefit of doubling the density of memory cells

taught by Pekny, a person of ordinary skill in the art would have used another sacrificial dielectric material that can be etched selectively to silicon nitride (for charge storage layers 222a and 222b) and silicon oxide (for dielectric layers 210). Chae, [0100], [0107]. A person of ordinary skill in the art would have had options for such a sacrificial material, and would have known that doped boron nitride is such a dielectric. Using hot phosphoric acid, a person of ordinary skill in the art would have etched doped boron nitride selectively to silicon oxide and silicon nitride. The etch rate of hot phosphoric acid for doped boron nitride would have been more than 40 times for its rate for silicon nitride. For example, U.S. Patent No. 5,536,360 discloses that, when hot phosphoric acid is used as an etchant, the etch rate for doped boron nitride is 10782 nm/hr and for doped silicon nitride is 228 nm/hr. Ex. 1015, Table 1. Similarly, the etch rate of hot phosphoric acid for doped boron nitride would have been more than 40 times for its rate for silicon oxide. For example, a 2003 article published by IEEE in the well-known and readily accessible *Journal of Microelectromechanical Systems* (that would have been accessible to a person of ordinary skill in the art, e.g., through the IEEE website or a library) titled “Etch Rates for Micromachining Processing Part II” authored by K. R. Williams *et al.* (“Williams”) discloses that when hot phosphoric acid is used as an etchant, the etch rate for silicon dioxide is 3.7 nm/min or less,

which is the same as 222 nm/hr.<sup>4</sup> Ex. 1014 Table III. The deposition of conductive material (step 2) or dielectric material (step 4) does not impact other structures. Moreover, it was understood how to etch conductive material (for step 3) selectively to the semiconductor material used to form pillars 224a and 224b such that these materials would not be damaged in the etching process. For example, Chae gives aluminum as an example for the conductive material that is etched. Chae, [0053]. Etchants that are highly selective to aluminum and do not etch through common semiconductors were known. For example, Williams discloses that “Al Etch A” has an etch rate of 530 nm/min for aluminum, but has a negligible etch rate for silicon, at <1 nm/min or less. Ex. 1014, Table II, Table V. Additionally, in Chae, the contact plugs 260 in the contact region for controlling the word lines are linearly aligned with operative and dummy structures. Chae, [0132]-[0133], Figures 10, 15E. A POSITA would have recognized that, when applying Pekny’s teachings of shifting the slot to pass through the operative and dummy structures, to ensure contact with the respective word lines, the location of the contacts would be shifted to be between the slots. Thus, a POSITA would have known how to apply Pekny’s teachings of forming slots through operative structures without negatively impacting the remainder of the fabrication process or

---

<sup>4</sup> To convert the nm/min units to nm/hr, the number should be multiplied by 60.

the operation of the resulting device.

214. Thus, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Pekny's teaching of forming slots through the structures to Chae's memory device fabrication process, and would have known such a combination (yielding the claimed limitations) would predictably work and provide the expected resulting structure.

## **X. SECONDARY CONSIDERATIONS**

215. I have seen no evidence in the '996 patent's prosecution history or elsewhere supporting any secondary considerations arguments, or evidence of nexus to any of the Challenged Claims. See generally '996 File History. Indeed, per my discussion of the prior art referenced herein, any purported solutions to problems or unexpected results in the '996 patent were already well known. To the extent Patent Owner asserts the existence of any secondary considerations in its responses, I reserve my right to address any such evidence.

## **XI. CONCLUSION**

216. In summary, I have concluded that the Challenged Claims are anticipated and/or rendered obvious by the prior art references as discussed above. Specifically, in my opinion, for at least the reasons above, the Challenged Claims of the '996 patent are anticipated and/or rendered obvious.

217. To the extent it is argued that any further disclosure is required for an

element in the Challenged Claims that I have identified as being disclosed, a person of ordinary skill in the art would certainly have found that element obvious to include based on the sample explicit disclosure or inherent disclosures and analysis I have identified above.

218. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner or its expert(s) may raise and to take into account new information as it becomes available to me.

219. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

220. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

# **APPENDIX A**

**CURRICULUM VITAE**  
**Dr. Kelin J. Kuhn**

**CONTACT INFORMATION:**

Kelin J. Kuhn  
P.O. Box 609  
Winthrop, WA 98862  
kjkuhn@confluence-tech.com

**EDUCATION:**

Ph.D., Electrical Engineering, Stanford University, Stanford, CA. June 1985  
M.S., Electrical Engineering, Stanford University, Stanford, CA. June 1985  
B.S., Electrical Engineering, University of Washington, Seattle, WA. March 1980  
(magna cum laude)

**PRESENT ROLE:**

**Confluence Technology Services, Winthrop, WA (kjkuhn@confluence-tech.com);  
present role**

Dr. Kuhn's business (Confluence Technology Services) supports a variety of engineering services in electronics and photonics, with emphasis on CMOS and beyond-CMOS technologies.

**Cornell University, Ithaca, NY; Materials Science and Engineering (kjk236@cornell.edu)  
2014 to date**

Position: Adjunct Professor  
Key Collaborator: Darrell Schlom

Prof. Kuhn's role is collaborating with a diverse group of faculty (both at Cornell and elsewhere) for establishment of long-term research programs in the area of valleytronics, inverse-design, quantum materials, post-CMOS technology, and spintronics.

**CLIENTS / SIGNIFICANT INTERACTIONS POST-2014:**

**Pillsbury Winthrop Shaw Pittman LLP:** Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *MicroSemi Corporation v. Commissioner of Internal Revenue*.

**Ropes and Gray:** Initiated 2023 and on-going. Technical evaluation and consulting on the matters related to *Yangtze Memory Technologies Company, LTD. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 5-23-cv-05792*.

**Heim, Payne & Chorush:** Initiated 2023 and on-going. Technical evaluation and consulting representing *Microchip Corporation* and its subsidiary *Silicon Storage Technology, Inc.* with regards to a dispute with *Taiwan Semiconductor Manufacturing Company*.

**Smith Baluch LLP:** Initiated 2022 and on-going. Technical evaluation and consultation to advise and assist Smith Baluch LLP matters relating to semiconductor processing.

**Carter Arnett:** Initiated 2022 and ongoing. Technical evaluation and consultation to advise and assist Carter Arnett PLLC in representing *Katana Silicon Technologies, LLC* in IPR2022-00763 and litigation related to Case No. 6:22-cv-00191 (W.D. Tex), adverse to *GlobalFoundries, Inc., GlobalFoundries, U.S. Inc., and GlobalFoundries U.S. 2 LLC*.

**Mintz:** Completed 2022-2023. Technical evaluation and consulting representing *Daedalus Prime LLC* with regards to the ITC Case: 337-TA-133, Certain Semiconductor Devices, Mobile Devices Containing Same (Taiwan Semiconductor Manufacturing Company).

**Heim, Payne & Chorush:** Completed 2021-2023. Technical evaluation and consulting representing *Arigna Technology Limited* with regards to IPR2021-01321 (*Volkswagen*) and IPR2021-01382 (*Infineon*).

**Quinn Emanuel Urquhart & Sullivan:** Believed complete 2021-2023. Technical evaluation and consulting representing *Hanwha* with regards to ITC Inv. No. 337-TA-1271.

**Ropes and Gray:** Completed 2021-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge I v. Micron Technology et al.*

**Lawrence and Phillips:** Completed 2021-2022. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.* with regards to *inter partes reviews* (IPRs) filed by Samsung.

**Wolf Greenfield:** Completed 2020-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge I v. Micron Technology et al.* with regards to *inter partes reviews* (IPRs) filed by Micron.

**Hueston Henningan:** Completed 2020-22. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.*

**Skadden Arps:** Initiated 2020 and on-going. Technical consulting for the *Audit Committee of the Intel Board of Directors* on matters related to Technology Development.

**PARADIM:** Initiated 2016 and on-going. PARADIM's mission is to create new interface materials with unprecedented properties for the next generation of electronic devices. Dr. Kuhn is a member of the External Advisory Committee. In this role, Dr. Kuhn provides technical and management support with regards to PARADIM operations.

**Quinn Emanuel Urquhart & Sullivan:** Completed, 2020-2021. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

**Susman Godfrey:** Completed 202-2023. Technical evaluation and consulting with regards to *Arigna Technology Limited* on matters related to CMOS transistor design.

**Womble Bond Dickinson:** Completed, 2020. Technical consulting for KIPB LLC (formerly KAIST IP US LLC) on an *ex parte reexamination* (“EPR”) proceeding in the United States Patent and Trademark Office with regards to patent 6,885,055.

**Womble Bond Dickinson:** Completed, 2019-2020. Technical evaluation and consulting in the matter of *KIPB LLC v. Samsung Electronics et al.* Dr. Kuhn supported this litigation for the plaintiff as an expert witness, including completion of the Infringement and Rebuttal Reports, as well as completing a deposition conducted on the contents of the Infringement and Rebuttal Reports. This case was settled out of court in September 2020.

**Lathrop Gage:** Completed, 2018-2020. Technical evaluation and consulting for KIPB LLC (formerly KAIST IP US LLC) on Korean Patent 10-0458288 (Korean counterpart to US 6,885,055).

**Ropes & Gray:** Completed, 2018. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Qualcomm Inc. et al.*

**GlaserWeil:** Completed, 2016-2018. Technical evaluation and consulting in the matter of *KAIST IP US LLC v. Samsung Electronics Co., Ltd., Case No. 2:16-cv-01314*. Dr. Kuhn supported this litigation for the plaintiff as an expert witness. This included IPR proceedings (a total of 6 IPRs were presented to the PTO in this case). This also included completion and submission of the Claim Construction Declaration, the Infringement Report, and the Rebuttal Report, as well as depositions conducted on the contents of these Reports. This case went to trial June 11-15, where Dr. Kuhn presented both Direct testimony on infringement (6/12/18) and Rebuttal (6/14/18) testimony on validity.

**yoR Labs Inc.:** Completed. 2015-2017. yoR Labs is a medical instrumentation start-up, focusing on non-invasive medical imaging instrumentation. Dr. Kuhn served first as a member of the External Advisory Committee and later as a member of the Board of Directors. In this role, Dr. Kuhn provided technical and management support with regards to yoR labs operations.

**Oregon State University, Department of Electrical Engineering and Computer Science:** Completed. 2015 to 2018: Professor-courtesy. Prof. Kuhn’s role was establishment of long-term research programs in the area advanced CMOS technology and post-CMOS technology.

## **FORMER ROLES (2014 and PRIOR)**

### **Intel, Portland, OR, (advanced development / research) 2008-2014 (retired in 2014)**

Grade level: 12 (Fellow)

Manager: Mike Mayberry, VP

Dr. Kuhn's role was researching advanced device architectures for Intel processes in the 5-10 year time frame. While much of her work as an Intel Fellow remains proprietary, some of the public domain aspects are captured in her book *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits* (Cambridge, 2015) and her paper "Considerations for Ultimate CMOS Scaling," (IEEE Trans. on Elec. Dev., Vol: 59, No: 7, 2012, pp. 1813 – 1828 which won the Paul Rappaport Award). She received an Intel IAA in 2008 for her work on the TriGate transistor.

### **Intel, Portland, OR, (45nm Device technology manager in pathfinding) 2004-2008**

Grade level: 10/11 (Principal Engineer / Sr. Principal Engineer)

Manager: Mark Bohr, Senior Intel Fellow / Kaizad Mistry, VP

Dr. Kuhn's role was as device technology manager of the pathfinding team responsible for the high-k metal-gate transistor architecture for Intel's 45nm microprocessor processor technology. She received an Intel IAA in 2006 for her work on high-k metal-gate.

### **Intel, Portland, OR, (90nm communication process manager) 2001-2004+**

Grade level: 9/10 (Sr. Engineer / Principal engineer)

Manager: Scott Thompson (was Intel Fellow at the time, now a professor at Univ. of Florida).

Dr. Kuhn's role in this time frame was Process Program Manager of the team responsible for Intel's 90nm communications process technology. Over a 4-year period, this team developed a derivative analog/RF technology (including a SiGe BJT) on top of Intel's premium 90nm microprocessor process.

## **Other Intel experience:**

### **Intel, Portland, OR, (130nm front-end integration engineer) 1998-2001**

### **Intel, Portland, OR, (0.35um front-end integration engineer) 1997-1998**

Grade level: 7-9 (Sr. engineering grades)

During the 130nm generation, Dr. Kuhn was an integration engineer responsible for the isolation section of the flow. 130nm was the last of the "classic" CMOS generations, and her work in that generation was updating the isolation process. She had the satisfaction of watching the work she did in the 130nm successfully scale through 90nm, 65nm, 45nm, and 32nm, with little change in the base process.

Dr. Kuhn joined Intel on the 0.35um generation as a sustaining integration engineer in F15. She was responsible for the silicide section of the flow. Additionally, she participated in the DIVD camera chip project (Intel's historical project to build CMOS camera chips).

**Other relevant experience:**

Univ. of Washington, Seattle, WA (Assoc. Prof., Ass't. Prof., Res. Ass't. Prof.), 1987-1997

Dr. Kuhn held faculty positions at the University of Washington (in Seattle) for roughly a decade in the order of Research Assistant Professor (Materials Science and Engineering), Assistant Professor (Electrical and Computer Engineering), and Associate Professor (Electrical and Computer Engineering). She left the University in 1997 as a tenured Associate Professor of Electrical and Computer Engineering. While at the Univ. of Washington, she achieved distinction in both research and teaching.

**Highlights include:**

- University of Washington, Distinguished Teaching Award, 1995 (UW's highest level of achievement for a faculty member)
- NSF Presidential Young Investigator award, 1991-6 (The National Science foundation is the most prestigious funding agency for faculty and the NSF PYI award is the most prestigious national level award for junior faculty).
- Single-author on a textbook, Laser Engineering, Prentice-Hall, 1998, ISBN 0-02-366921-7 (this is a mezzanine text discussing the theory and practice of building conventional and diode laser systems).

**BOOKS**

Laser Engineering, (sole author) Prentice-Hall, 1998, ISBN 0-02-366921-7

CMOS and Beyond: Logic Switches for Terascale Integrated Circuits (Co-editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015, ISBN 978-1107043183).

**BOOK CHAPTERS**

“The Magic of MOSFET Manufacturing,” Chapter in the 75<sup>th</sup> Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8.

Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616) .

**AWARDS:**

Elected to the National Academy of Engineering (2023)  
IEEE Frederik Philips Award (2016)  
IEEE Paul Rappaport Award (2013)  
IEEE Fellow (2011)

Intel Achievement Awards (Intel's highest technical award): IAA 2006 (for HiK-MG) and IAA 2008 (for key contributions to Intel's 22nm TriGate technology)

Intel Divisional Awards: Turbo operation (2009), RF Vccmin (2007), TCC (2005), SCD 1213.4 SCD/ICG (2004), LAD NW/Ophir A-1 (2003), SiGe BJT (2002), Hitachi etch (2002), 2um2SRAM (2001), Gamma Test chip (2000), Certification P854.6 (1999), F15 ISO 9000 (1998)

Academic Engineer of the Year Award, Puget Sound Engineering Council, 1996

University of Washington, Distinguished Teaching Award, 1995

College of Engineering, Outstanding Faculty Achievement Award, 1994

NSF Presidential Young Investigator award, 1991-6

NSF Research Initiation Award, 1989-91

IBM Graduate Fellowship, 1983-5

Hertz Graduate Fellowship, 1982-3

National Merit Scholar, 1976-80

## **JOURNAL PUBLICATIONS:**

49. "First principles modeling of defects in the  $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  system", G. Greene-Diniz, K. Kuhn, P. Hurley, and J. Greer, *J. Appl. Phys.*, Vol. 121, No. 7, Jan. 2017.
48. "Doping top-down e-beam fabricated germanium nanowires using molecular monolayers," B. Long, G. Alessio Verni, J. O'Connell, M. Shayesteh, A. Gangnaik, Y.M. Georgiev, P. Carolan, D. O'Connell, K.J. Kuhn, S.B. Clendenning, R. Nagle, R. Duffy, and J.D. Holmes, *Materials Science in Semiconductor Processing*, Vol. 62, May 2017, pp. 196-200.
47. "Device Physics Modeling of Surfaces and Interfaces from an Induced Gap State Perspective," J. Wager and K. Kuhn, *Critical Reviews in Solid State and Materials Science*, Oct. 4, 2016.
46. "Adhesion Limits and Design Criteria for Nanorelays", Kevin L. Lin, Graham L. W. Cross, Peter Gleeson, Johann P. de Silva, Alejandro Levander, Jorge A. Muñoz, Chytra Pawashe, Alexis Potie, Patrick Theofanis, John J. Boland, and Dr. Kuhn J. Kuhn, *IEEE Trans. on Elec. Dev.*, Vol. 63, No. 1, Jan. 2016, 465-470.
45. Distributive Quasi-Ballistic Drift Diffusion Model Including Effects of Stress and High Driving Field, Roza Kotlyar,, Rafael Rios, Cory E. Weber, Thomas D. Linton, Mark Armstrong and Dr. Kuhn Kuhn, *IEEE Trans. on Elec. Dev.*, Vol. 62, No. 3, March 2015. Pp. 743-750.
44. Improved MOSFET characterization technique for single channel length, scaled transistors, Ferdousi, F., Rios, R., Kuhn K.J. *Solid State Electronics*, Vol. 104, pp. 44-6, Feb. 2015
43. Capacitance and Conductance for an MOS System in Inversion, with Oxide Capacitance and Minority Carrier Lifetime Extractions, Monaghan, S. O'Connor, E., Rios, R., Ferdousi, F., Floyd, L., Ryan, E., Cherhaoui, K., Povey, I.M., Kuhn, K.J., Hurley, P.K. *IEEE Transactions on Electron Devices*, Vol. 61, No. 12, pp. 4176-85, Dec. 2014.

42. First principle-based analysis of single-walled carbon nanotube and silicon nanowire Junctionless transistors, Ansari, L., Feldman, B., Faga, G., Martinez, L.C., Haverty, M.G., Kuhn, K.J., Shankar, S., Greer, J.C., IEEE Transactions on Nanotechnology, Vol. 12, No. 6, pp. 1075-81, Nov. 2013.
41. Scaling Limits of Electrostatic Nanorelays, Pawashe, C., Lin, K., Kuhn, K.J., IEEE Transactions on Electron Devices, Vol. 60, No. 9, pp. 2936-42, Sept. 2013,
40. Bandgap engineering of group IV materials for complementary n and p tunneling field effect transistors, Kotlyar, R.; Avci, U.E.; Cea, S.; Rios, R.; Linton, T.D.; Kuhn, K.J.; Young, I.A., Applied Physics Letters, v 102, n 11, March 18, 2013.
39. Effects of alternating current voltage amplitude and oxide capacitance on mid-gap interface state defect density extractions in InGaAs capacitors, Monaghan, Scott ; O'Connor, Eamon ; Povey, Ian M. ; Sheehan, Brendan J. ; Cherkaoui, Karim ; Hutchinson, Barry J. A. ; Hurley, Paul K. ; Ferdousi, Fahmida ; Rios, Rafael ; Kuhn, Dr. Kuhn J. ; Rahman, Anisur, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, Vol: 31 , No: 1, 2013, pp: 01A119 - 01A119-8.
38. Considerations for Ultimate CMOS Scaling, Dr. Kuhn J. Kuhn, invited review paper, IEEE Trans. on Elec. Dev., Vol: 59 , No: 7, 2012 , pp. 1813 – 1828 (won the Paul Rappaport Award)
37. Does the low hole transport mass in <110> and <111> Si nanowires lead to mobility enhancements at high field and stress: a self-consistent tight-binding study, R. Kotlyar, T. D. Linton, R. Rios, M. D. Giles, S. M. Cea, K. J. Kuhn, Michael Povolotskyi, Tillmann Kubis, and Gerhard Klimeck, Vol: 111 , No: 12, 2012, pp 123718 - 123718-11
36. Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm, Rios, R.; Cappellani, A.; Armstrong, M.; Budrevich, A.; Gomez, H.; Pai, R.; Rahhal-orabi, N.; Kuhn, K., IEEE Electron Device Letters, Vol. 32, No. 9, 2011, pp. 1170 - 1172
35. Process Technology Variation, Kuhn, K.J.; Giles, M.D.; Becher, D.; Kolar, P.; Kornfeld, A.; Kotlyar, R.; Ma, S.T.; Maheshwari, A.; Mudanai, S., IEEE Transactions on Electron Devices, Aug. 2011, vol.58, no.8, pp. 2197-208.
34. Moore's crystal ball: Device physics and technology past the 15nm generation, Kuhn, K.J., Microelectronic Engineering, July 2011, vol.88, no.7, pp. 1044-9.
33. Variability in nanoscale CMOS technology, Kuhn, K.J., K. Sci. China Inf. Sci. (2011) 54: 936. doi:10.1007/s11432-011-4219-6 (May 5, 2011).
32. Compressive Uniaxial Stress Bandstructure Engineering for Transferred-Hole Devices, Kotlyar, R.; Giles, M.D.; Mudanai, S.P.; Kuhn, K.J.; Cea, S.M.; Linton, T.D.; Pillarisetty, R.; IEEE Elec. Dev. Lett. Vol. 31, No. 8, 2010, pp. 878-880.

31. Managing process variation in Intel's 45 nm CMOS technology, Kuhn, K., Kenyon, C., Kornfeld, A., et al. Intel Technology Journal Volume: 12 Issue: 2 Pages: 93-4 Published: 17 June 2008
30. Analytical Modeling of Output Conductance in Long-Channel Halo-Doped MOSFETs, Electron Devices, Mudanai, S.; Shih, W.-K.; Rios, R.; Xi, X.; Rhew, J.-H.; Kuhn, K.; Packan, P.;, IEEE Transactions on Volume 53, Issue 9, Sept. 2006 Page(s):2091 - 2097
29. A 90-nm logic technology featuring strained-silicon, Thompson, S.E.; Armstrong, M.; Auth, C.; Alavi, M.; Buehler, M.; Chau, R.; Cea, S.; Ghani, T.; Glass, G.; Hoffman, T.; Jan, C.-H.; Kenyon, C.; Klaus, J.; Kuhn, K.; Zhiyong Ma; McIntyre, B.; Mistry, K.; Murthy, A.; Obradovic, B.; Nagisetty, R.; Phi Nguyen; Sivakumar, S.; Shaheed, R.; Shifren, L.; Tufts, B.; Tyagi, S.; Bohr, M.; El-Mansy, Y., IEEE Transactions on Electron Devices, vol.51, no.11, Nov. 2004. p. 1790-7.
28. Integration of mixed-signal elements into a high-performance digital CMOS process. Kuhn, K.J.; Ahmed, S.; Vandervoom, P.; Murthy, A. Intel Technology Journal, no.2, 2002
27. Elevated temperature performance of pseudomorphic AlGaAs/InGaAs MODFETs. Zurek, S.J.; Darling, R.B.; Kuhn, K.J.; Foisy, M.C. IEEE Transactions on Electron Devices, vol.45, no.1, Jan. 1998. p. 2-8
26. Synthetic wide bandpass X-ray polarizers. Cross, J.O.; Bennett, B.R.; Bell, M.I.; Kuhn, K.J. Applied Physics Letters, vol.70, no.17, 28 April 1997. p. 2224-6
25. Electro-optic polymer light modulator based on surface plasmon resonance. Jung, C.; Yee, S.; Kuhn, K. Applied Optics, vol.34, no.6, 20 Feb. 1995. p. 946-9
24. A "hands-on" course in consumer electronics design. Hannaford, B.; Kuhn, K. Mechatronics, vol.5, no.7, Oct. 1995. p. 753-62 Journal Paper
23. Finite element solutions to GaAs-AlAs quantum wells with connection matrices at heterojunctions. Li, T.L.; Kuhn, K.J. Journal of Computational Physics, vol.115, no.2, Dec. 1994. p. 288-95
22. Integrated optics waveguide modulator based on surface plasmon resonance. Jung, C.; Yee, S.; Kuhn, K. Journal of Lightwave Technology, vol.12, no.10, Oct. 1994. p. 1802-6
21. Effects of spin-orbit interaction on the envelope-function equations for semiconductor heterostructures. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.50, no.12, 15 Sept. 1994. p. 8589-601
20. Effects of mass discontinuity on the numerical solutions to quantum wells using the effective mass equation. Li, T.L.; Kuhn, K.J. Journal of Computational Physics, vol.110, no.2, Feb. 1994. p. 292-300

19. Validity of the connection-matrix approach to GaAs-Al/sub  $x$ /Ga/sub  $1-x$ /As quantum wells. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.49, no.4, 15 Jan. 1994. p. 2608-14
18. Optical properties due to intersubband transitions in n-type quantum wells including the effects of the exchange interaction. Sengers, A.J.; Tsang, L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.48, no.20, 15 Nov. 1993. p. 15116-22
17. Band-offset ratio dependence on the effective-mass Hamiltonian based on a modified profile of the GaAs-Al/sub  $x$ /Ga/sub  $1-x$ /As quantum well. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.47, no.19, 15 May 1993. p. 12760-70
16. Use of active loads with MSM photodetectors in digital GaAs MESFET photoreceivers. Darling, R.B.; Youn, H.J.; Kuhn, K.J. Journal of Lightwave Technology, vol.10, no.11, Nov. 1992. p. 1597-605
15. Mobility of strained and dislocated In/sub  $x$ /Ga/sub  $1-x$ /As semiconductor material. Kuhn, K.J.; Darling, R.B. IEEE Transactions on Electron Devices, vol.39, no.6, June 1992. p. 1288-94
14. Dislocation scattering in n-type modulation doped Al/sub 0.3/Ga/sub 0.7/As/In/sub  $x$ /Ga/sub  $1-x$ /As/Al/sub 0.3/Ga/sub 0.7/As quantum wells. Zhao, D.; Kuhn, K.J. IEEE Transactions on Electron Devices, vol.38, no.12, Dec. 1991. p. 2582-9
13. Free carrier induced changes in the absorption and refractive index for intersubband optical transitions in Al/sub  $x$ /Ga/sub  $1-x$ /As/GaAs/Al/sub  $x$ /Ga/sub  $1-x$ /As quantum wells. Kuhn, K.J.; Iyengar, G.U.; Yee, S. Journal of Applied Physics, vol.70, no.9, 1 Nov. 1991. p. 5010-17
12. Electric field effects in AlGaAs-GaAs symmetric and asymmetric coupled quantum wells. Juang, C.; Kuhn, K.J.; Darling, R.B. IEEE Journal of Quantum Electronics, vol.27, no.9, Sept. 1991. p. 2122-8
11. Effect of etch treatment prior to Schottky contact fabrication on In/sub 0.05/Ga/sub 0.95/As. Johnson, M.J.; Kuhn, K.J.; Darling, R.B. Applied Physics Letters, vol.58, no.17, 29 April 1991. p. 1893-5
10. An enhanced and linear Stark shift in n-i-n AlGaAs/GaAs symmetric and asymmetric coupled quantum wells. Kuhn, K.J.; Cheng Juang; Darling, R.B. Journal of Applied Physics, vol.69, no.5, 1 March 1991. p. 3135-41
9. AlGaAs-GaAs multiple-quantum-well spectrally tunable photoconductors. Youn, H.J.; Darling, R.B.; Kuhn, K.J. IEEE Photonics Technology Letters, vol.3, no.2, Feb. 1991. p. 159-61
8. Effect of AlGaAs window and buffer layers on the response characteristics of GaAs photoconductive detectors. Youn, H.J.; Darling, R.B.; Kuhn, K.J. Applied Physics Letters, vol.57, no.19, 5 Nov. 1990. p. 2001-3

7. Selective etching of GaAs and Al/sub 0.30/Ga/sub 0.70/As with citric acid/hydrogen peroxide solutions. Juang, C.; Kuhn, K.J.; Darling, R.B. Journal of Vacuum Science & Technology B (Microelectronics Processing and Phenomena), vol.8, no.5, Sept.-Oct. 1990. p. 1122-4
6. Stark shift and field-induced tunneling in Al/sub x/Ga/sub 1-x/As/GaAs quantum-well structures. Juang, C.; Kuhn, K.J.; Darling, R.B. Physical Review B (Condensed Matter), vol.41, no.17, 15 June 1990. p. 12047-53
5. An indium-free substrate holder for radiative heating of quarter-wafer molecular-beam epitaxy samples. Kuhn, K.J. Review of Scientific Instruments, vol.61, no.1, pt.1, Jan. 1990. p. 184-5
4. Variation in GaAs surface oxide desorption temperature as a function of shuttered aluminum oven temperature. Kuhn, K.J.; Pubanz, G.A. Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films), vol.7, no.6, Nov.-Dec. 1989. p. 3265-8
3. Static gas conduction cooled slab geometry Nd:glass laser. Reed, M.; Kuhn, K.; Unternahrer, J.; Byer, R.L. IEEE Journal of Quantum Electronics, vol.QE-21, no.5, May 1985. p. 412-14
2. The slab geometry laser. I. Theory. Eggleston, J.M.; Kane, T.J.; Kuhn, K.; Unternahrer, J. IEEE Journal of Quantum Electronics, vol.QE-20, no.3, March 1984. p. 289-301
1. Implementation of Distributed Microprocessor Systems in Custom Heavy Trucks, K.J. Kuhn, 1979-80 IEEE Student Papers, Vol. TT0114 IEEE, pg. 334-342.

## CONFERENCE PUBLICATIONS

54. Bias temperature instability variation on SiON/Poly, HK/MG and trigate architectures, C. Prasad, M. Agostinelli, J. Hicks, S. Ramey, C. Auth, K. Mistry, S. Natarajan, P. Packan, I. Post, S. Bodapati, M. Giles, S. Gupta, S. Mudani and K. Kuhn, 2014 IEEE International Reliability Physics Symposium (IRPS), June 2014.
53. Semiconductors Stand Aside, the Age of Metals is Here! K. Kuhn, A. Sanchez, C. George, R. Rios, J. Clarke, J. Greer, Lester Eastman Conference, Cornell, May 2014.
52. The ultimate CMOS device and beyond, Kuhn, K.J. ; Avci, U. ; Cappellani, A. ; Giles, M.D. ; Haverty, M. ; Seiyon Kim ; Kotlyar, R. ; Manipatruni, S. ; Nikonov, D. ; Pawashe, C. ; Radosavljevic, M. ; Rios, R. ; Shankar, S. ; Vedula, R. ; Chau, R. ; Young, I. 2012 IEEE International Electron Devices Meeting (IEDM), pp. 171-174.
51. Understanding the feasibility of scaled III-V TFET for logic by bridging atomistic simulations and experimental results, Avci, U.E. ; Hasan, S. ; Nikonov, D.E. ; Rios, R. ; Kuhn, K. ; Young, I.A., Symposium on VLSI Technology (VLSIT), 2012, pp: 183 – 184.
50. Beyond the Planar Transistor: Progress in Next Generation Switches, K. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

49. Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation, K. Kuhn, INFOS 2011 (June 22, 2011, France)
48. Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET, Avci, U.E.; Rios, R.; Kuhn, K.J.; Young, I.A., IEEE Conference on Nanotechnology (IEEE-NANO), 2011 11<sup>th</sup>, pp. 869 – 872
47. Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic, Avci, U.E.; Rios, R.; Kuhn, K.; Young, I.A., 2011 Symposium on VLSI Technology (VLSIT), 2011 , pp. 124 – 125
46. CMOS scaling for the 22nm node and beyond: Device physics and technology, Kuhn, K.J., 2011 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2011 , pp. 1 – 2
45. Past, Present and Future: SiGe and CMOS Transistor Scaling. K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, ECS 2010, Oct. 10, Las Vegas, CA, USA.
44. Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, K. J. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29<sup>th</sup>, 2010; Albany, NY, USA.
43. CMOS transistor scaling past 32nm and implications on variation, K. Kuhn, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA, pp. 241-246.
42. Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, K. Kuhn, Nikkei Electronics Symposium, June 29<sup>th</sup>, 2010.
41. Technology options for 22nm and beyond, K. Kuhn, Technology, Kuhn, K.J.; Liu, M.Y.; Kennel, H.; 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.
40. CMOS technology beyond 22nm, K. Kuhn, 12<sup>th</sup> IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California
39. Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10<sup>th</sup> September 2009, Leixlip, Co. Kildare.
38. Moore's Law Past 32nm: The Challenges in Physics and Technology Scaling, K. Kuhn, Solid State Devices and Materials Conference (SSDM), September 18, 2009, Sendai, Japan.
37. CMOS scaling beyond 32 nm: challenges and opportunities, Kuhn, K.J., 2009 46th ACM/IEEE Design Automation Conference (DAC), 26-31 July 2009, San Francisco, CA, USA, Pages: 310-13 Published: 2009

36. Future device scaling: beyond traditional CMOS, Tyagi, S., Auth, C., Ban, I., et al., 2009 2nd International Workshop on Electron Devices and Semiconductor Technology (IEDST), 1-2 June 2009, Mumbai, India, (IEDST) Pages: 4 pp. Published: 2009
35. Variation in 45nm and Implications for 32nm and Beyond, K. Kuhn, NMI International Conference on CMOS Variability, 12th & 13th May 2009, London, UK.
34. Moore's law past 32 nm: future challenges in device scaling, Kuhn, K.J., 2009 13th International Workshop on Computational Electronics (IWCE 2009), 27-29 May 2009, Beijing, China, (IWCE 2009) Pages: 6 pp. Published: 2009
33. 22 nm Device Architecture and Performance Elements, K.J. Kuhn, IEEE International Electron Devices Meeting, 15-17 December 2008, San Francisco, CA, USA , IEDM short course.
32. High performance hi-k + metal gate strain enhanced transistors on (110) silicon, Packan, P., Cea, S., Deshpande, H., Kuhn, K, et. al. IEDM 2008. IEEE International Electron Devices Meeting, 15-17 December 2008, San Francisco, CA, USA, IEDM 2008. IEEE International Electron Devices Meeting. Technical Digest Pages: 4 pp. Published: 2008
31. 45 nm high-k + metal gate strain-enhanced transistors, Auth, C., Cappellani, A., Chun, J.-S., Kuhn, K. et al, 2008 Symposium on VLSI Technology, 17-20 June 2008, Honolulu, HI, USA, Pages: 128-9 Published: 17 June 2008
30. Dielectric breakdown in a 45 nm high-K/metal gate process technology, Prasad, C., Agostinelli, M., Auth, C., Kuhn, K. et al, 2008 IEEE International Reliability Physics Symposium (IRPS), 27 April-1 May 2008, Phoenix, AZ, USA, Pages: 667-8 Published: 2008
29. BTI reliability of 45 nm high-K + metal-gate process technology, Pae, S., Agostinelli, M., Brazier, M., Kuhn, K, et al. 2008 IEEE International Reliability Physics Symposium (IRPS), 27 April-1 May 2008, Phoenix, AZ, USA, (IRPS) Pages: 352-7 Published: 2008
28. Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4 Published: 2007
27. A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging, Mistry, K., Allen, C., Auth, C., Kuhn, K. et al., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA , IEDM '07 Pages: 247-50 Published: 2007
26. High performance 35nm L/sub GATE/ CMOS transistors featuring NiSi metal gate (FUSI), uniaxial strained silicon channels and 1.2nm gate oxide, Ranade, P.; Ghani, T.; Kuhn, K.; Mistry, K.; Pae, S.; Shifren, L.; Stettler, M.; Tone, K.; Tyagi, S.; Bohr, M.; Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International, 5-7 Dec. 2005 Page(s):4 pp.

25. Noise performance of 90 nm CMOS technology, Becher, D.; Banerjee, G.; Basco, R.; Hung, C.; Kuhn, K.; Wei-Kai Shih, 2004 IEEE MTT-S International Microwave Symposium Digest (IEEE Cat. No.04CH37535). Piscataway, NJ, USA: IEEE, 2004. p. 17-20 Vol.1. Conference Paper.
24. A comparison of state-of-the-art NMOS and SiGe HBT devices for analog/mixed-signal/RF circuit applications, Kuhn, K.; Basco, R.; Becher, D.; Hattendorf, M.; Packan, P.; Post, I.; Vandervoorn, P.; Young, I., 2004 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.04CH37526). Gaithersburg, MD, USA: Widerkehr and Associates, 2004. p. 224-5. Conference Paper.
23. A 90 nm communication technology featuring SiGe HBT transistors, RF CMOS, precision R-L-C RF elements and 1 /spl mu/m/sup 2/ 6-T SRAM cell, Kuhn, K.; Agostinelli, M.; Ahmed, S.; Chambers, S.; Cea, S.; Christensen, S.; Fischer, P.; Gong, J.; Kardas, C.; Letson, T.; Henning, L.; Murthy, A.; Muthali, H.; Obradovic, B.; Packan, P.; Pae, S.W.; Post, I.; Putna, S.; Raol, K.; Roskowski, A.; Soman, R, "" Electron Devices Meeting, 2002. IEDM '02. Digest. International , 8-11 Dec. 2002 Page(s): 73 -76
22. A 90 nm Generation BiCMOS Technology for Analog, Mixed-signal, and RF Applications, K. Kuhn, S. Chambers, C. Kardas, T. Letson, A.-Murthy and P. Packan, Intel Process Technology Conference, October, 17, 2002. (Best of session paper award)
21. Scaling challenges for 0.13 mu m generation shallow trench isolation, Kuhn, K.J.; Din-how Mei; Post, I.; Neiryneck, J., 2001 IEEE International Symposium on Semiconductor Manufacturing. ISSM 2001. Conference Proceedings (Cat. No.01CH37203). Piscataway, NJ, USA: IEEE, 2001. p. 187-90 Conference Paper
20. Scaling challenges for 0.13 mu m generation shallow trench isolation, Kuhn, K.J.; Din-how Mei; Post, I.; Neiryneck, J., and Au, W., Intel Process Technology Conference, October, 10, 2000.
19. Electrical critical dimension metrology for 100 nm linewidths and below. Grenville, A.; Coombs, B.; Hutchinson, J.; Kuhn, K. Proceedings of the SPIE - The International Society for Optical Engineering, vol.4000, pt.1-2, 2000. p. 452-9 Conference Paper
18. The performance of a wide band X-ray Bragg polarizer grown by molecular beam epitaxy, Cross, J.O.; Bennett, B.R.; Bell, M.I.; Kuhn, K.J., , AIP Conference Proceedings, no.417, 1997. p. 117
17. Solving the 3 and 4 state laser systems, Dr. Kuhn Kuhn, regular paper, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.
16. An integrated course in laser engineering, K. Kuhn, regular paper #1232, ASEE 1996 annual conference, Washington DC, June 22-26, 1996.

15. Development of a course in Consumer Electronics, K. Kuhn and B. Hannaford, regular paper #3232, ASEE 1996 annual conference, Washington DC, June 22-26, 1996.
14. An Erbium-doped fiber laser, C. Cornish and K. Kuhn, 1995 Progress in Electromagnetics Research Symposium, July 24-28, 1995.
13. Development of a course in Consumer Electronics, K. Kuhn and B. Hannaford, Session 3B, Mechatronics Conference, Stanford, July 15-17, 1994.
12. Integrated optical waveguide modulator using long range surface plasmon resonance, C. Jung, S. Yee and K. Kuhn, OSA Integrated Photonics Research Conference, San Francisco, CA. February 17-19 (1994)
11. Evaluation of an ion-exchanged integrated optic waveguide for solution phase chemical sensing. Kuhn, K.J.; Burgess, L.W. Proceedings of the SPIE - The International Society for Optical Engineering, vol.1796, 1993. p. 332-42 Conference Paper
10. A. Sengers, G. Iyengar, L. Tsang and K. Kuhn, "Optical Properties due to Intersubband Transitions in n-type Quantum Wells Including the Effects of the Exchange Interaction", 1993 March meeting of the American Physical Society, Seattle, WA 22-26 March 1993.
9. Free carrier induced changes in the absorption and refractive index for intersubband optical transitions in  $\text{Al}_{\text{sub } x}/\text{Ga}_{\text{sub } 1-x}/\text{As}/\text{GaAs}/\text{Al}_{\text{sub } x}/\text{Ga}_{\text{sub } 1-x}/\text{As}$  quantum wells. Iyengar, G.U.; Kuhn, K.J.; Yee, S. In: Gallium Arsenide and Related Compounds 1991. Proceedings of the Eighteenth International Symposium. Bristol, UK: IOP, 1992. p. 431-6 Conference Paper
8. Free carrier induced changes in the absorption and refractive index for intersubband optical transitions in  $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$  quantum wells, G. Iyengar, K. Kuhn, and S. Yee, Conference Proceedings, 17th International Symposium on GaAs and Related Compounds, September 9-12, 1991; Seattle, WA.
7. Applications of Molecular Beam Epitaxy to Integrable Optical Devices, K.J. Kuhn, Professional program, Northcon/88, October 5, 1988.
6. Laser annealing of AlGaAs, E. Riemer, K. Song, K. Kuhn and T. Stoebe, Atomic and Molecular Processing of Electronics and Ceramic Materials, 23 Conf. on Ceramic Science, UW, August 30 to September 3, 1987.
5. Amplified Spontaneous Emission in Slab Lasers, D.C. Brown, K.J. Kuhn, Kotik K. Lee and R.L. Byer, paper WE-5, Conference on Lasers and Electro-optics (CLEO), Anaheim, CA, June 1984.
4. Progress in high peak and average power lasers for soft X-ray production. Byer, R.L.; Kuhn, K.; Reed, M.; Trail, J. Proceedings of the SPIE - The International Society for Optical Engineering, vol.448, 1984. p. 2-7 Conference Paper

3. Conductive-cooling of Slab Lasers, K.J. Kuhn, T.J. Kane, and R.L. Byer, paper WE-3, 1982 Annual meeting of the Optical Society of America, Tucson, Arizona, October 1982.
2. Progress in slab geometry solid state lasers. Eggleston, J.M.; Kane, T.; Kuhn, K.; Byer, R.L. Proceedings of the SPIE - The International Society for Optical Engineering, vol.335, 1982. p. 104-8 Conference Paper
1. Implementation of distributed microprocessor systems in custom heavy trucks. Kuhn, K.J. In: Wescon/80 Conference Record. El Segundo, CA, USA: Electron. Conventions, 1980. p. SS2-3/1-8 Conference Paper.

## PATENTS

|    | PAT. NO.   | Title                                                                                                          |
|----|------------|----------------------------------------------------------------------------------------------------------------|
| 1  | 11,302,777 | Integration methods to fabricate internal spacers for nanowire devices                                         |
| 2  | 11,195,919 | Method of fabricating a semiconductor device with strained SiGe fins and a Si cladding layer                   |
| 3  | 11,139,400 | Non-planar semiconductor device having hybrid geometry-based active region                                     |
| 4  | 11,024,714 | Nanowire transistor fabrication with hardmask layers                                                           |
| 5  | 10,991,799 | Silicon and silicon germanium nanowire structures                                                              |
| 6  | 10,825,752 | Integrated thermoelectric cooling                                                                              |
| 7  | 10,804,357 | Integration methods to fabricate internal spacers for nanowire devices                                         |
| 8  | 10,636,871 | Silicon and silicon germanium nanowire structures                                                              |
| 9  | 10,593,804 | Non-planar semiconductor device having hybrid geometry-based active region                                     |
| 10 | 10,586,868 | Non-planar semiconductor device having hybrid geometry-based active region                                     |
| 11 | 10,580,899 | Nanowire structures having non-discrete source and drain regions                                               |
| 12 | 10,580,860 | Integration methods to fabricate internal spacers for nanowire devices                                         |
| 13 | 10,535,770 | Scaled TFET transistor formed using nanowire with surface termination                                          |
| 14 | 10,424,580 | Semiconductor devices having modulated nanowire counts                                                         |
| 15 | 10,283,589 | Integration methods to fabricate internal spacers for nanowire devices                                         |
| 16 | 10,121,861 | Nanowire transistor fabrication with hardmask layers                                                           |
| 17 | 10,121,856 | Integration methods to fabricate internal spacers for nanowire devices                                         |
| 18 | 10,115,822 | Methods of forming low band gap source and drain structures in microelectronic devices                         |
| 19 | 10,109,711 | CMOS FinFET device having strained SiGe fins and a strained Si cladding layer on the NMOS channel              |
| 20 | 10,074,573 | CMOS nanowire structure                                                                                        |
| 21 | 10,074,357 | Integrated acoustic phase array                                                                                |
| 22 | 10,026,829 | Semiconductor device with isolated body portion                                                                |
| 23 | 9,978,636  | Isolated and bulk semiconductor devices formed on a same bulk substrate                                        |
| 24 | 9,947,805  | Nanowire-based mechanical switching device                                                                     |
| 25 | 9,935,205  | Internal spacers for nanowire transistors and method of fabrication thereof                                    |
| 26 | 9,935,107  | CMOS FinFET device with dual strained cladding layers on relaxed SiGe fins, and method of fabricating the same |
| 27 | 9,926,193  | Magnetic nanomechanical devices for stiction compensation                                                      |

|    |           |                                                                                                                                    |
|----|-----------|------------------------------------------------------------------------------------------------------------------------------------|
| 28 | 9,911,835 | Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs            |
| 29 | 9,893,167 | Integration methods to fabricate internal spacers for nanowire devices                                                             |
| 30 | 9,882,053 | Molded dielectric fin-based nanostructure                                                                                          |
| 31 | 9,859,368 | Integration methods to fabricate internal spacers for nanowire devices                                                             |
| 32 | 9,825,130 | Leakage reduction structures for nanowire transistors                                                                              |
| 33 | 9,812,524 | Nanowire transistor devices and forming techniques                                                                                 |
| 34 | 9,691,843 | Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition |
| 35 | 9,680,013 | Non-planar device having uniaxially strained semiconductor body and method of making same                                          |
| 36 | 9,673,302 | Conversion of strain-inducing buffer to electrical insulator                                                                       |
| 37 | 9,614,060 | Nanowire transistor with underlayer etch stops                                                                                     |
| 38 | 9,608,059 | Semiconductor device with isolated body portion                                                                                    |
| 39 | 9,595,581 | Silicon and silicon germanium nanowire structures                                                                                  |
| 40 | 9,583,602 | Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs            |
| 41 | 9,583,491 | CMOS nanowire structure                                                                                                            |
| 42 | 9,564,522 | Nanowire structures having non-discrete source and drain regions                                                                   |
| 43 | 9,559,160 | Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition |
| 44 | 9,508,796 | Internal spacers for nanowire transistors and method of fabrication thereof                                                        |
| 45 | 9,484,447 | Integration methods to fabricate internal spacers for nanowire devices                                                             |
| 46 | 9,472,613 | Conversion of strain-inducing buffer to electrical insulator                                                                       |
| 47 | 9,425,212 | Isolated and bulk semiconductor devices formed on a same bulk substrate                                                            |
| 48 | 9,412,872 | N-type and P-type tunneling field effect transistors (TFETs)                                                                       |
| 49 | 9,385,221 | Nanowire transistor with underlayer etch stops                                                                                     |
| 50 | 9,362,074 | Nanowire-based mechanical switching device                                                                                         |
| 51 | 9,355,242 | Method and apparatus for managing and accessing personal data                                                                      |
| 52 | 9,343,559 | Nanowire transistor devices and forming techniques                                                                                 |
| 53 | 9,287,576 | Self-powered internal medical device                                                                                               |
| 54 | 9,258,114 | Quantum key distribution (QSD) scheme using photonic integrated circuit (PIC)                                                      |
| 55 | 9,224,810 | CMOS nanowire structure                                                                                                            |
| 56 | 9,183,829 | Integrated acoustic phase array                                                                                                    |

|    |           |                                                                                                         |
|----|-----------|---------------------------------------------------------------------------------------------------------|
| 57 | 9,129,829 | Silicon and silicon germanium nanowire structures                                                       |
| 58 | 9,129,827 | Conversion of strain-inducing buffer to electrical insulator                                            |
| 59 | 9,105,344 | Shut-off mechanism in an integrated circuit device                                                      |
| 60 | 9,087,863 | Nanowire structures having non-discrete source and drain regions                                        |
| 61 | 9,064,944 | Nanowire transistor with underlayer etch stops                                                          |
| 62 | 9,029,221 | Semiconductor devices having three-dimensional bodies with modulated heights                            |
| 63 | 9,012,284 | Nanowire transistor devices and forming techniques                                                      |
| 64 | 8,890,120 | Tunneling field effect transistors (TFETs) for CMOS approaches to fabricating N-type and P-type TFETs   |
| 65 | 8,853,741 | Junctionless accumulation-mode devices on decoupled prominent architectures                             |
| 66 | 8,766,372 | Copper-filled trench contact for transistor performance improvement                                     |
| 67 | 8,753,942 | Silicon and silicon germanium nanowire structures                                                       |
| 68 | 8,558,279 | Non-planar device having uniaxially strained semiconductor body and method of making same               |
| 69 | 8,507,948 | Junctionless accumulation-mode devices on prominent architectures, and methods of making same           |
| 70 | 8,487,348 | Methods and apparatus to reduce layout based strain variations in non-planar transistor structures      |
| 71 | 8,269,283 | Methods and apparatus to reduce layout based strain variations in non-planar transistor structures      |
| 72 | 8,258,057 | Copper-filled trench contact for transistor performance improvement                                     |
| 73 | 7,999,607 | Power switches having positive-channel high dielectric constant insulated gate field effect transistors |
| 74 | 7,888,710 | CMOS fabrication process utilizing special transistor orientation                                       |
| 75 | 7,737,770 | Power switches having positive-channel high dielectric constant insulated gate field effect transistors |
| 76 | 7,312,485 | CMOS fabrication process utilizing special transistor orientation                                       |
| 77 | 6,627,506 | Thin tensile layers in shallow trench isolation and method of making same                               |
| 78 | 6,368,931 | Thin tensile layers in shallow trench isolation and method of making same                               |
| 79 | 4,617,669 | Method and apparatus for pumping laser slabs                                                            |
| 80 | 4,563,763 | Method and apparatus for cooling a slab laser                                                           |

## **INVITED TECHNICAL PRESENTATIONS/SEMINARS :**

Invited panel, IEDM, Variation and the End of the World, December, 2013.

Keynote, The End of Scaling?, ICTC, December 2013.

Invited seminar, CMOS and Beyond, Portland State University, October, 2013.

Keynote panel, CMOS and Beyond: Future Device Technology, ENF 2013, Ireland, June 2013.

Invited seminar, CMOS and Beyond: Future Device Technology for the Mobile World, IDF, May 2013.

Invited Workshop, The Future is Already Here: Evolving Concepts in Device and Materials Technology, AMAT, March 2013.

Invited paper, "The Ultimate CMOS Device and Beyond," IEDM 2012, San Francisco.

Invited talk, Beyond Simply Small: Progress in Advanced Transistor Architectures, Cornell, November 2012.

Invited seminar, Demystifying Moore's Law How it Really Works!, IDF, Sept. 2012, San Francisco.

Invited talk, The Ultimate CMOS Device and Beyond, Ireland, April 2012.

Keynote: "MOS scaling for the 22nm node and beyond: Device physics and technology," April 24, 2011, Taiwan, VLSI-TSA

Plenary: "Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation," INFOS 2011 (June 22, 2011, France)

Keynote: "Beyond the Planar Transistor: Progress in Next Generation Switches," Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

Invited seminar - "Polishing Moore's Crystal Ball: Advanced Transistor Architectures ...and Beyond," K. Kuhn, March 30th. 2011, MIT, MTL seminar series.

Invited seminar - "Emerging Devices: Moore's Law and Advanced Transistor Architectures," K. Kuhn, Varian Technology Symposium, March 31st. 2011.

Keynote: "Scaling Electronics:Trends and Bottlenecks," K. Kuhn, April 4th. 2011, MIT Microphotonics meeting.

Invited seminar - "Gazing into Moore's Crystal Ball: Transistor Scaling after the 15nm node," K. Kuhn, Feb. 17<sup>th</sup>, 2010, Berkeley.

IEDM 2010 Short Course chair for 15nm technology, December 2010.

Plenary: Past, Present and Future: SiGe and CMOS Transistor Scaling, ECS 2010, Oct. 10, Las Vegas, CA, USA.

Keynote: Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.

Plenary: CMOS transistor scaling past 32nm and implications on variation, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA

Keynote: Technology options for 22nm and beyond, K. Kuhn, 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.

Invited seminar: Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, Nikkei Electronics Symposium / June 29th, 2010.

Plenary - CMOS technology beyond 22nm, K. Kuhn, 12<sup>th</sup> IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California

Keynote - Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10<sup>th</sup> September 2009, Leixlip, Co. Kildare.

Plenary - Moore's Law Past 32nm: The Challenges in Physics and Technology Scaling, K. Kuhn, Solid State Devices and Materials Conference (SSDM), September 18, 2009, Sendai, Japan.

Invited talk - CMOS scaling beyond 32 nm: challenges and opportunities, Kuhn, K.J., 2009 46th ACM/IEEE Design Automation Conference (DAC), 26-31 July 2009, San Francisco, CA, USA, Pages: 310-13 Published: 2009

Keynote - Variation in 45nm and Implications for 32nm and Beyond, K. Kuhn, NMI International Conference on CMOS Variability, 12th & 13th May 2009, London, UK.

Invited talk - Moore's law past 32 nm: future challenges in device scaling, Kuhn, K.J., 2009 13th International Workshop on Computational Electronics (IWCE 2009), 27-29 May 2009, Beijing, China, (IWCE 2009) Pages: 6 pp. Published: 2009

Invited – International Electron Device meeting – short course.  
[http://download.intel.com/pressroom/pdf/kkuhn/Kuhn\\_22nm\\_Device.pdf](http://download.intel.com/pressroom/pdf/kkuhn/Kuhn_22nm_Device.pdf)

Invited seminar - "45nm High-k + Metal Gate Logic Technology," K. Kuhn, May 2008, MIT, MTL laboratory.

Invited talk - Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4

Invited seminar - "CMOS Transistor Architecture Challenges and Opportunities," K. Kuhn, September 2005, MIT, MTL laboratory.

Keynote - "Nanotechnology Challenges and Opportunities," K. Kuhn, January 2005, MIT, MTL laboratory.

Invited seminar - "Transistor Scaling and its Impact on Analog/RF Device Performance", Dr. Kuhn Kuhn, March 2005, Stanford University, invited seminar.

Invited seminar - "Advanced transistor architecture approaches and their implications for device and circuit performance," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2004.

Invited seminar - "Moore's Law meets Materials Science", Dr. Kuhn Kuhn, September 2004, University of Washington.

Invited seminar - "Centrino, convergence of computing and communications," November 2003, Dr. Kuhn Kuhn, Stanford University, invited seminar.

Invited seminar - "Challenges in the parallel development of the 90nm communications (121x) and microprocessor (1262) process technologies," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2003.

Invited seminar - "RF/analog integration with 90nm digital CMOS", Dr. Kuhn Kuhn, MIT invited seminar, March 2003

Invited seminar - "Femtosecond pulse laser technology", Dr. Kuhn Kuhn, Oregon State University, March 10, 1997.

Invited talk- "Symbolic Solvers and their impact on engineering education", Dr. Kuhn Kuhn, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.

# **APPENDIX B**

## Appendix B

### List of Materials Considered

| Exhibit No. | DESCRIPTION                                                                                                                                                                                                                                                    |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1001        | U.S. Patent No. 8,945,996                                                                                                                                                                                                                                      |
| 1002        | File History of U.S. Patent Application No. 13/085,083                                                                                                                                                                                                         |
| 1004        | U.S. App. Pub. No. 2010/0133598 (“Chae”)                                                                                                                                                                                                                       |
| 1005        | U.S. App. Pub. No. 2011/0156132 (“Kiyotoshi”)                                                                                                                                                                                                                  |
| 1006        | U.S. App. Pub. No. 2011/0151667 (“Hwang”)                                                                                                                                                                                                                      |
| 1007        | U.S. Patent No. 7,906,818 (“Pekny”)                                                                                                                                                                                                                            |
| 1008        | Joint Claim Construction and Prehearing Statement (Patent Local Rule 4-3), Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC., No. 3:23-cv-05792-RFL, D.I. 105 (ND. Cal. August 19, 2024)                |
| 1010        | “Shrinking Possibilities” by B. Arnold (2009)                                                                                                                                                                                                                  |
| 1011        | U.S. Patent No. 8,039,176 (“Fujimura”)                                                                                                                                                                                                                         |
| 1012        | “Epitaxial layer characterization and metrology” by V.-M. Airaksinen (2001)                                                                                                                                                                                    |
| 1013        | “Chemical Vapor Deposition” by J.-O. Carlsson and P. M. Martin (2010)                                                                                                                                                                                          |
| 1014        | “Etch Rates for Micromachining Processing Part II” by K. R. Williams, K. Gupta, and M. Wasilik (2003)                                                                                                                                                          |
| 1015        | U.S. Patent No. 5,536,360 (“Nguyen”)                                                                                                                                                                                                                           |
| 1016        | Counterclaim Plaintiff Micron Technology’s Disclosure of Asserted Claims and Infringement Contentions and Document Production Accompanying Disclosure (Patent Local Rules 3-1 and 3-2), <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc.</i> |

| Exhibit No. | DESCRIPTION                                                                         |
|-------------|-------------------------------------------------------------------------------------|
|             | <i>and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL (N.D. Cal.) |
| 1017        | U.S. App. Pub. No. 2007/0057328 (“Taniguchi”)                                       |
| 1018        | U.S. Patent No. 8,397,132 (“Fukuyama”)                                              |