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(54) NONVOLATILE MEMORY DEVICE AND METHOD FOR FABRICATING THE SAME

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(57) **ABSTRACT**

A three-dimensional nonvolatile memory device and a method for fabricating the same include a semiconductor substrate, a plurality of active pillars, and a plurality of gate electrodes. The semiconductor substrate includes a memory cell region and a contact region. The active pillars extend in the memory cell region perpendicular to the semiconductor substrate. The gate electrodes include a first gate electrode and a second gate electrode. The first gate electrode is disposed on the memory cell region to intersect the active pillars. The second gate electrode is disposed on the contact region, connected to the first gate electrode and comprising metal material.

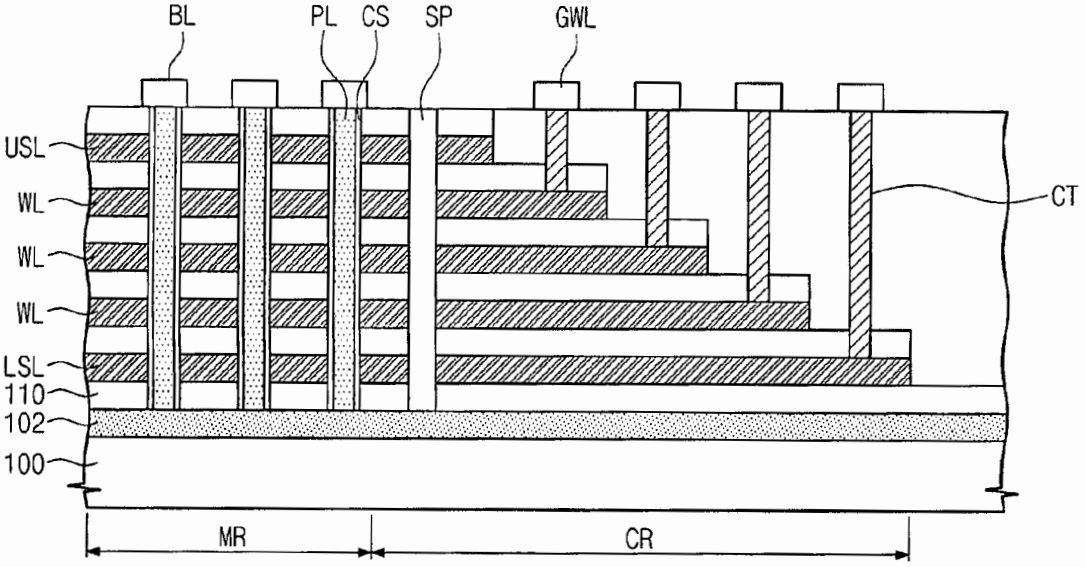
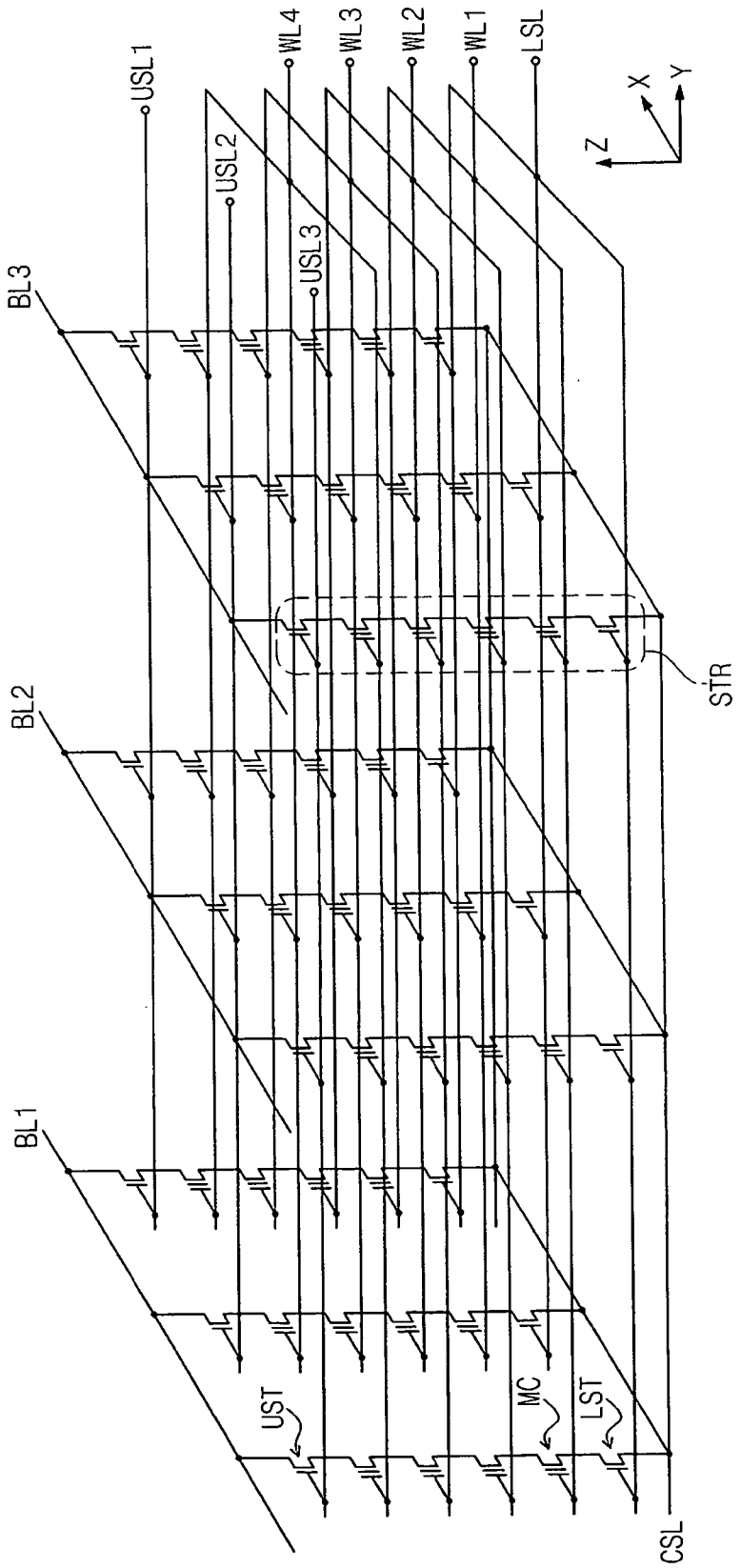


Fig. 1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USL3
WL4
WL3
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MC
LST
CSL

Fig. 2A

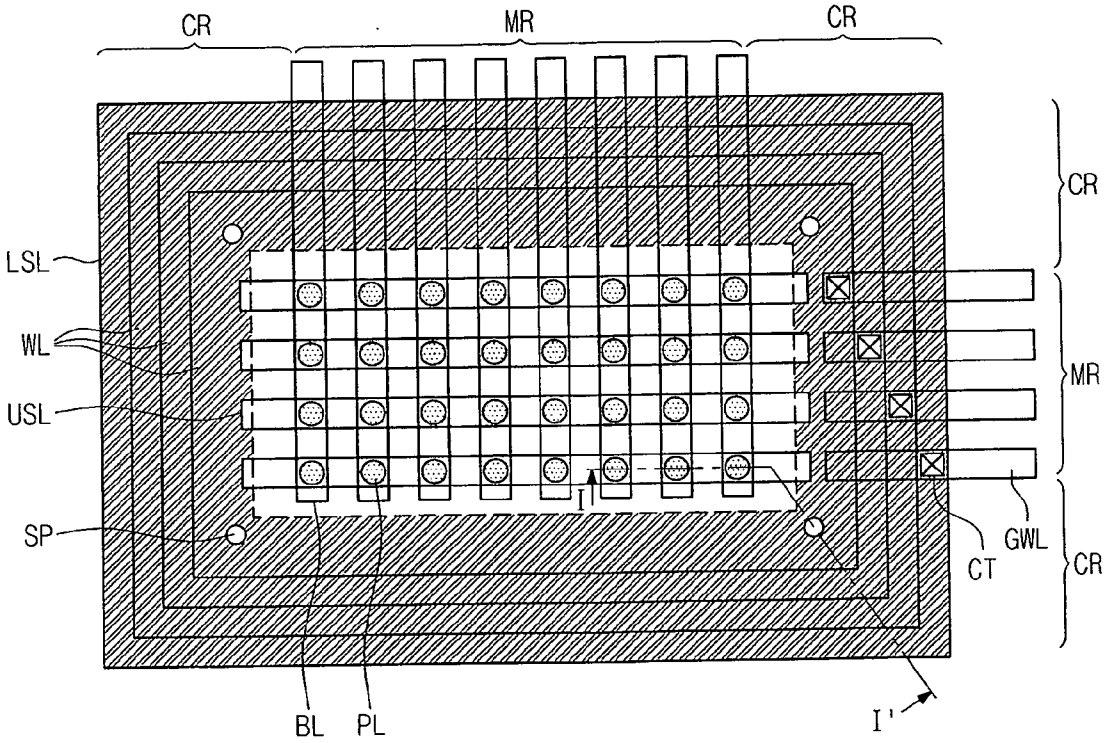


Fig. 2B

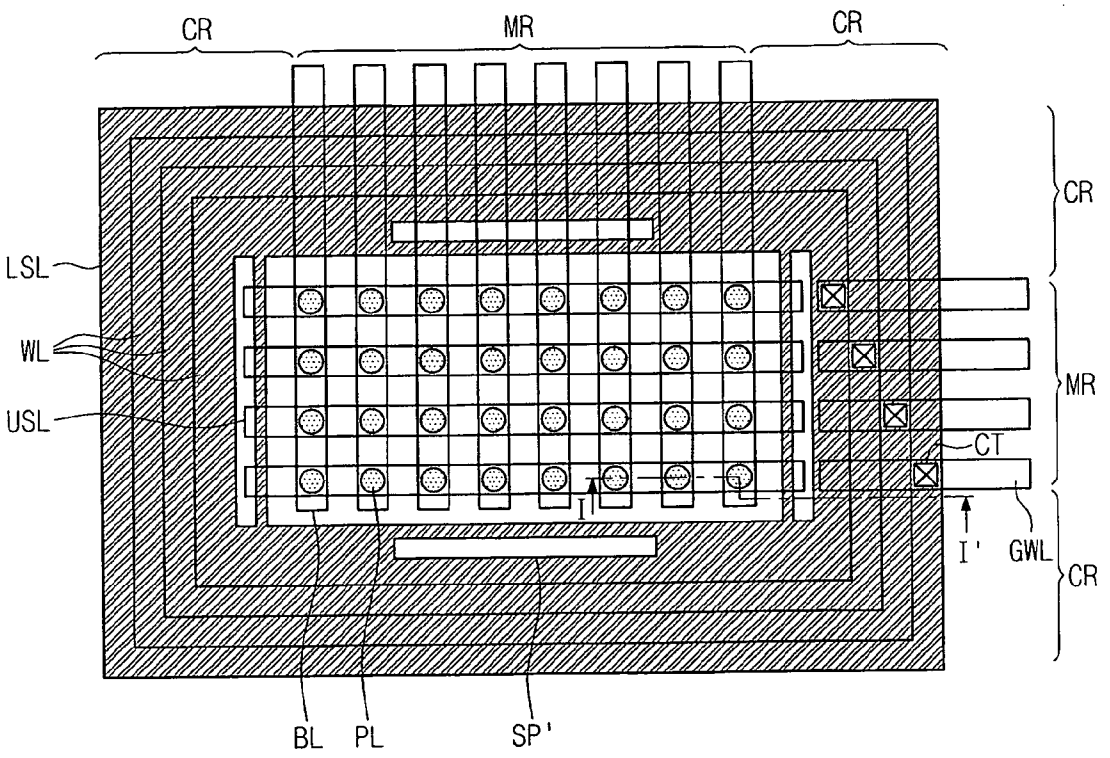


Fig. 2C

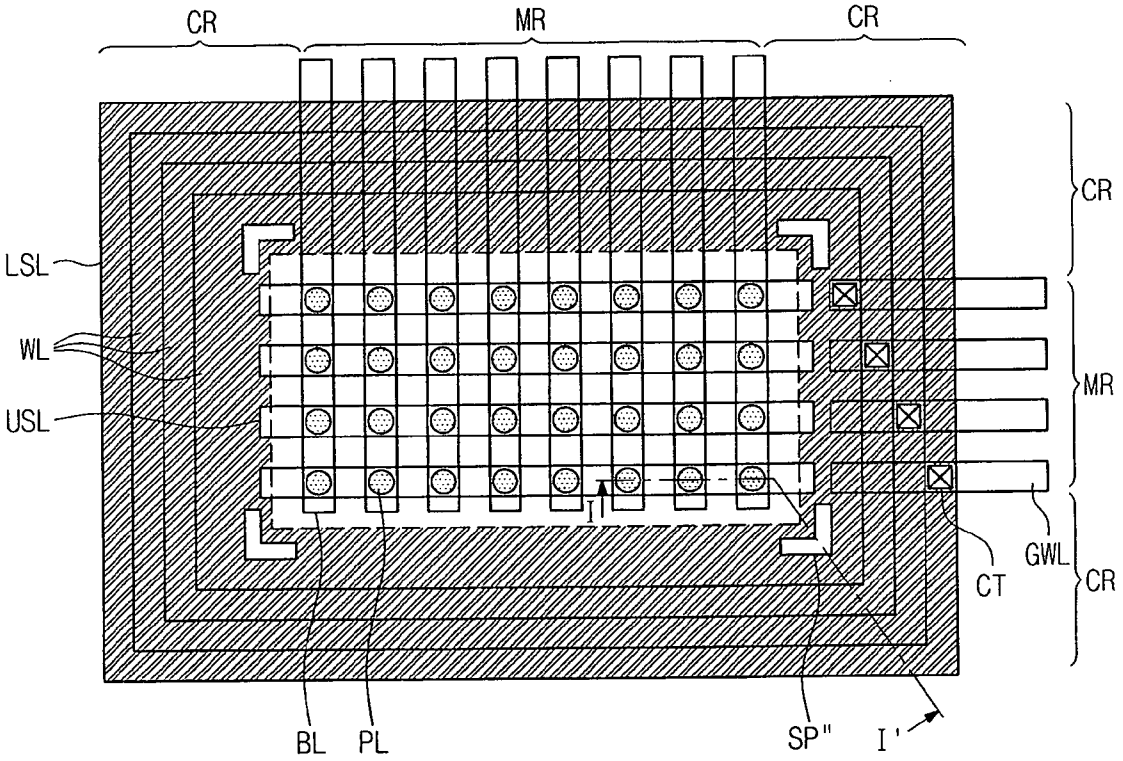


Fig. 3

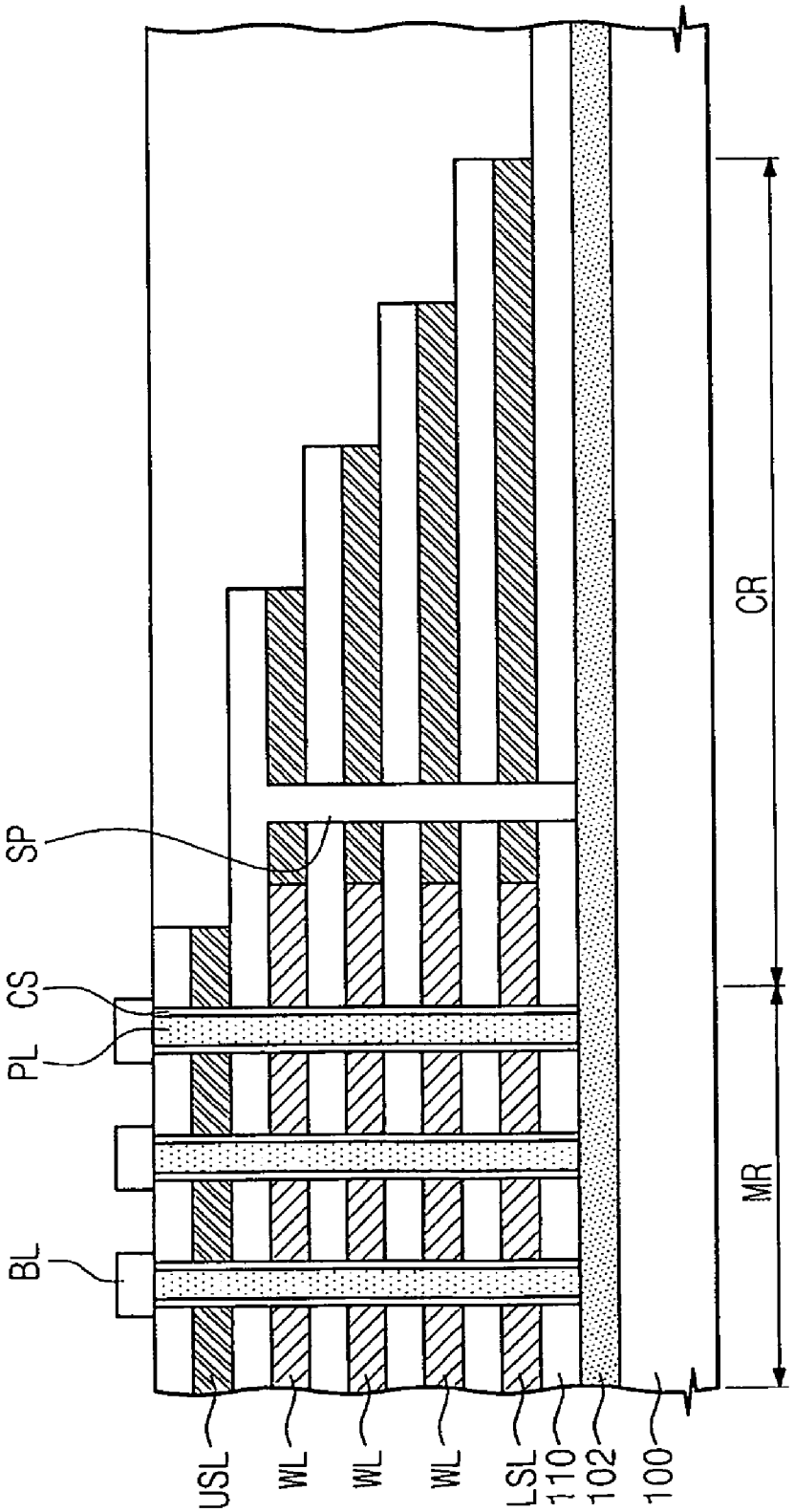
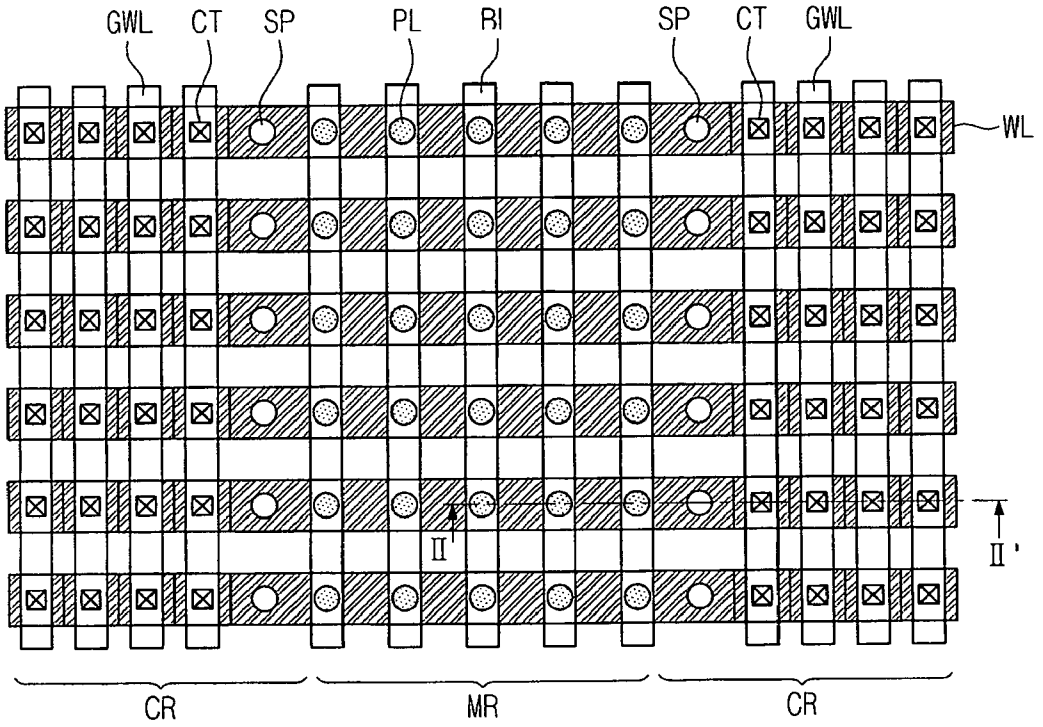


Fig. 4



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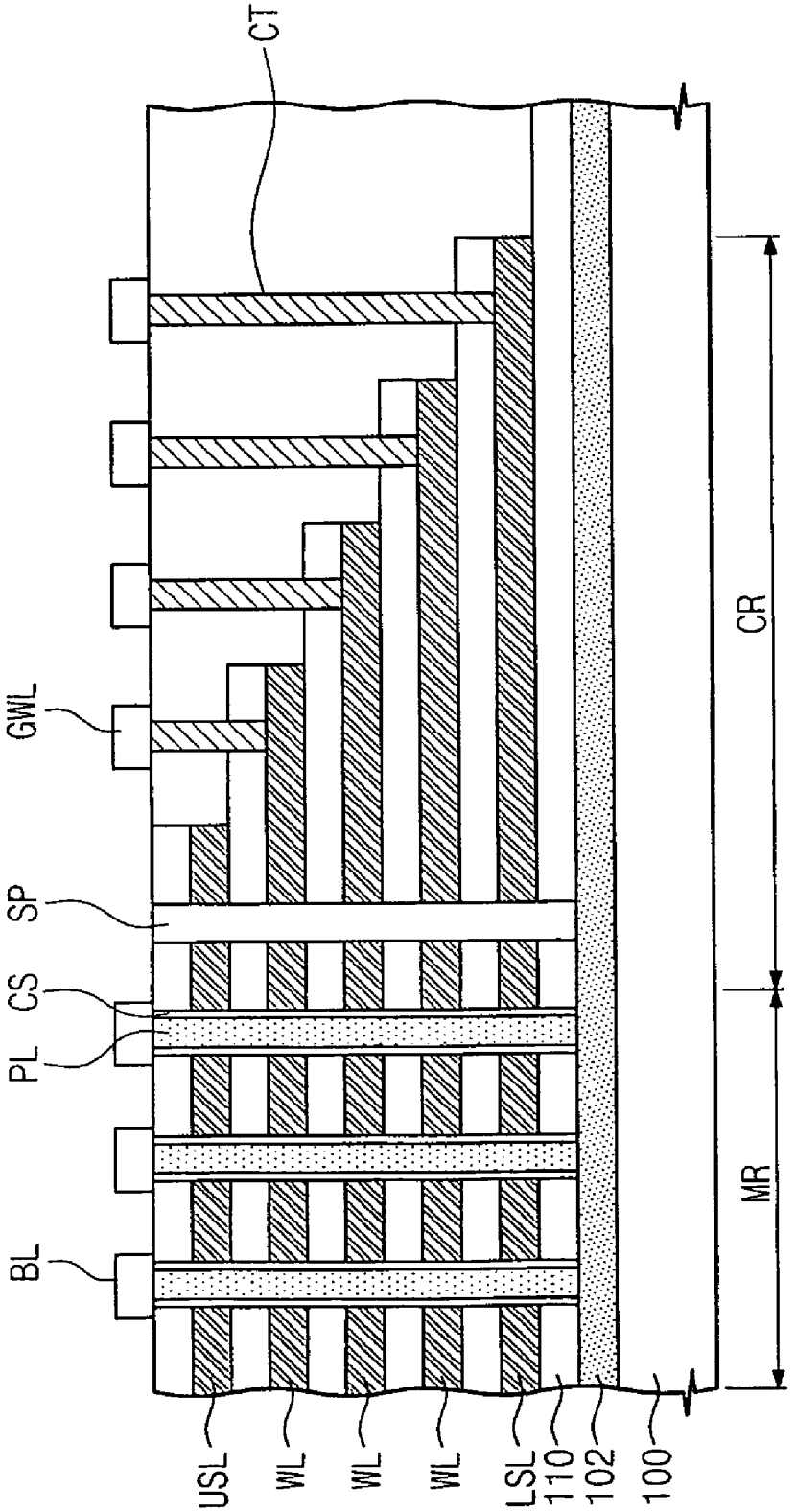


Fig. 6

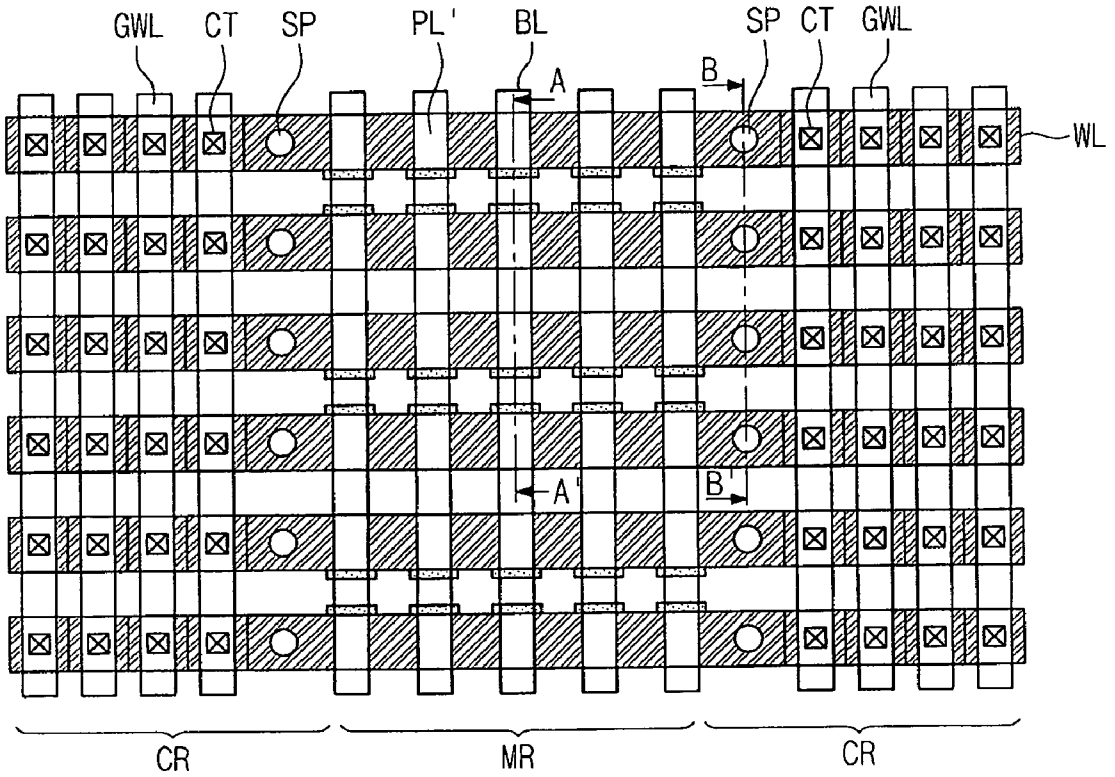


Fig. 7

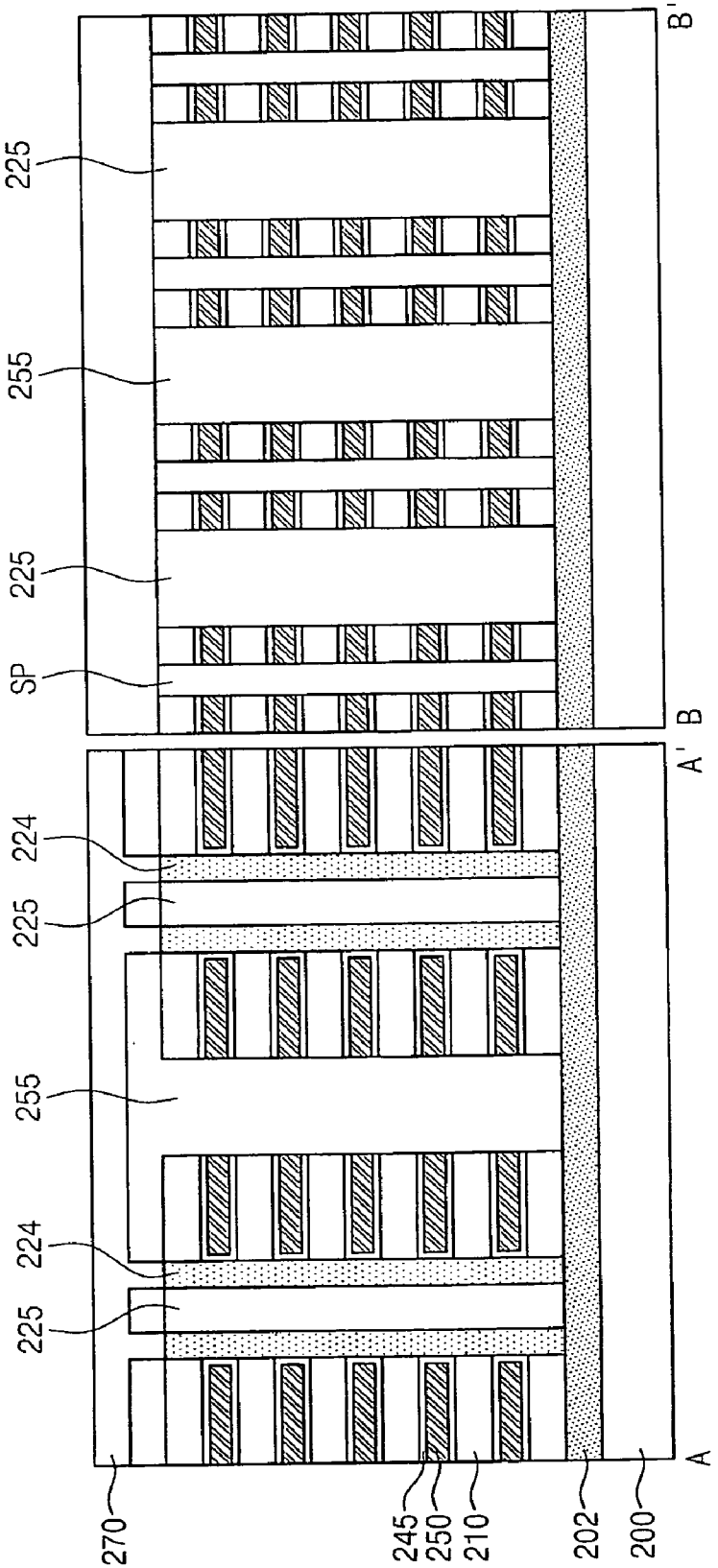


Fig. 8

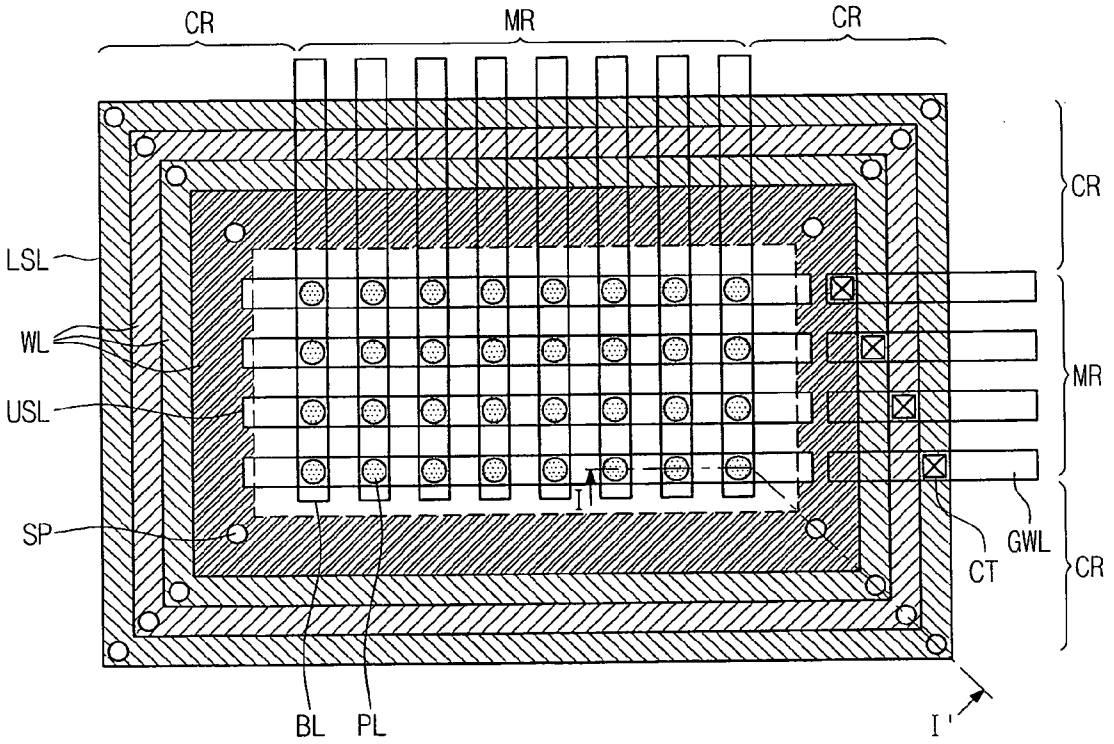


Fig. 9

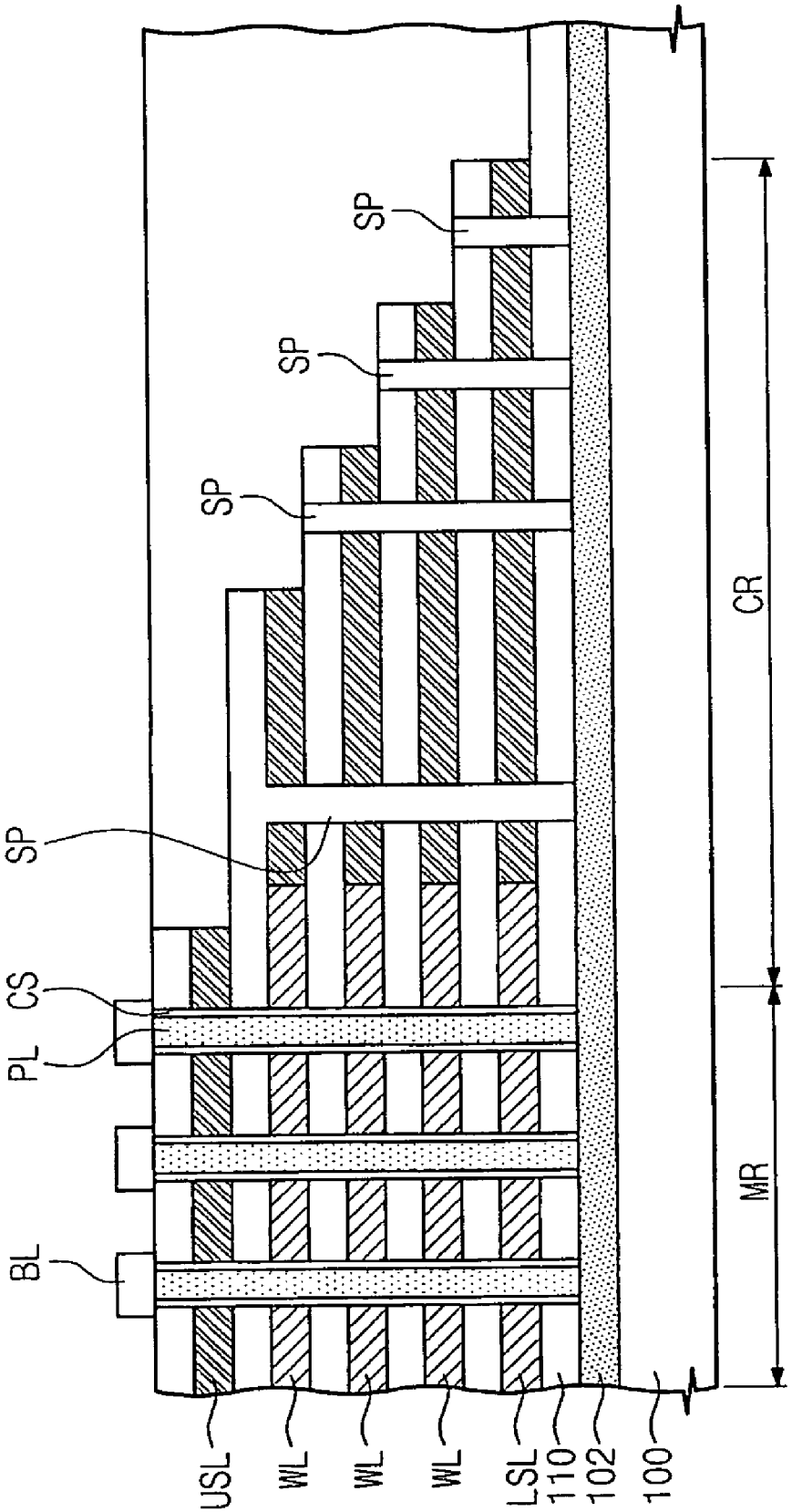


Fig. 10

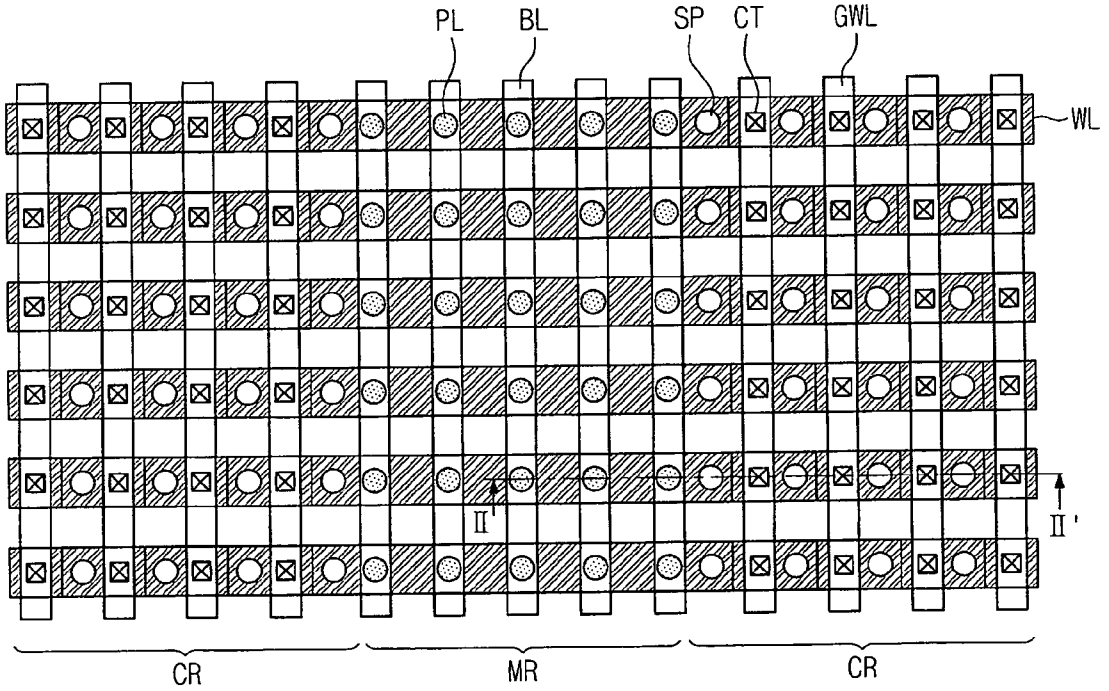


Fig. 11

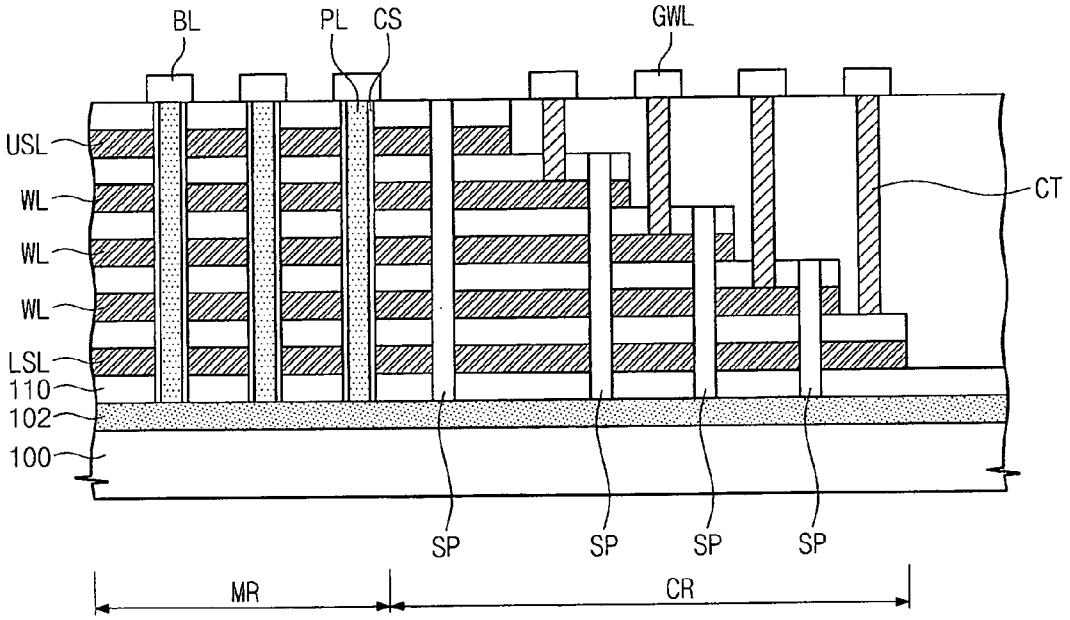


Fig. 12

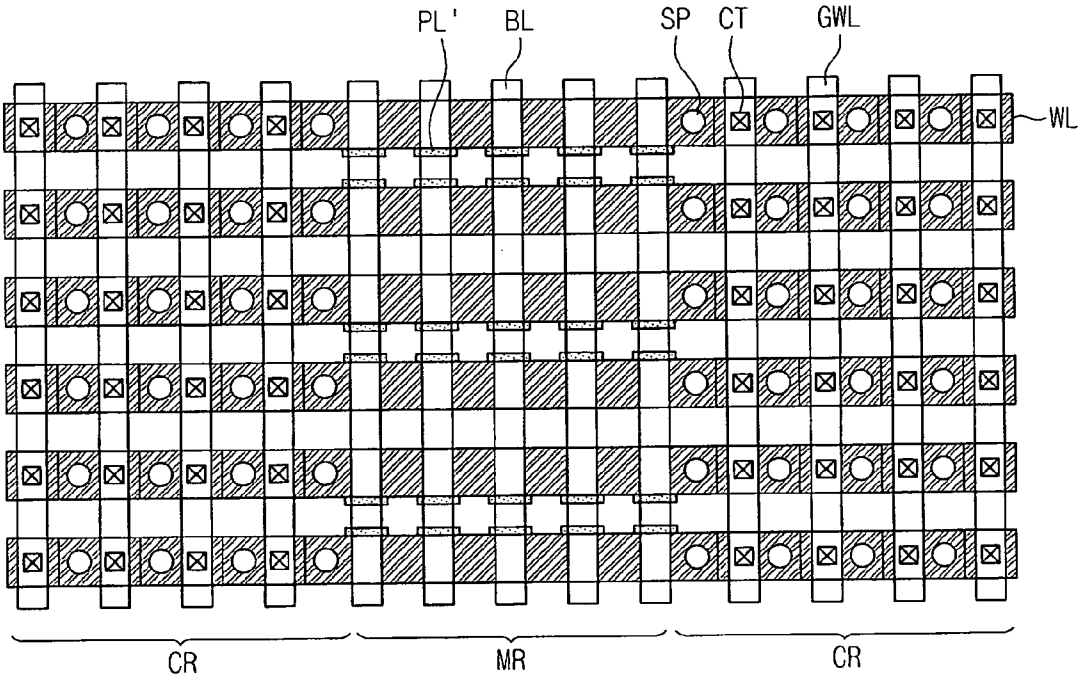


Fig. 13A

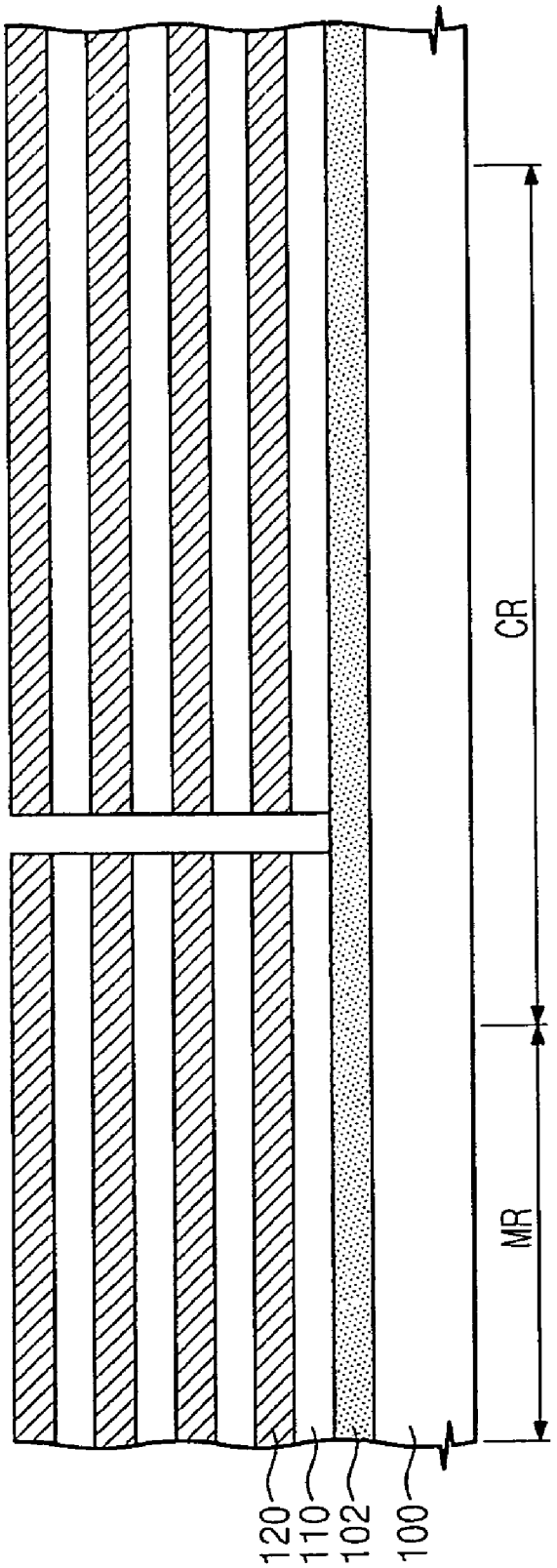


Fig. 13B

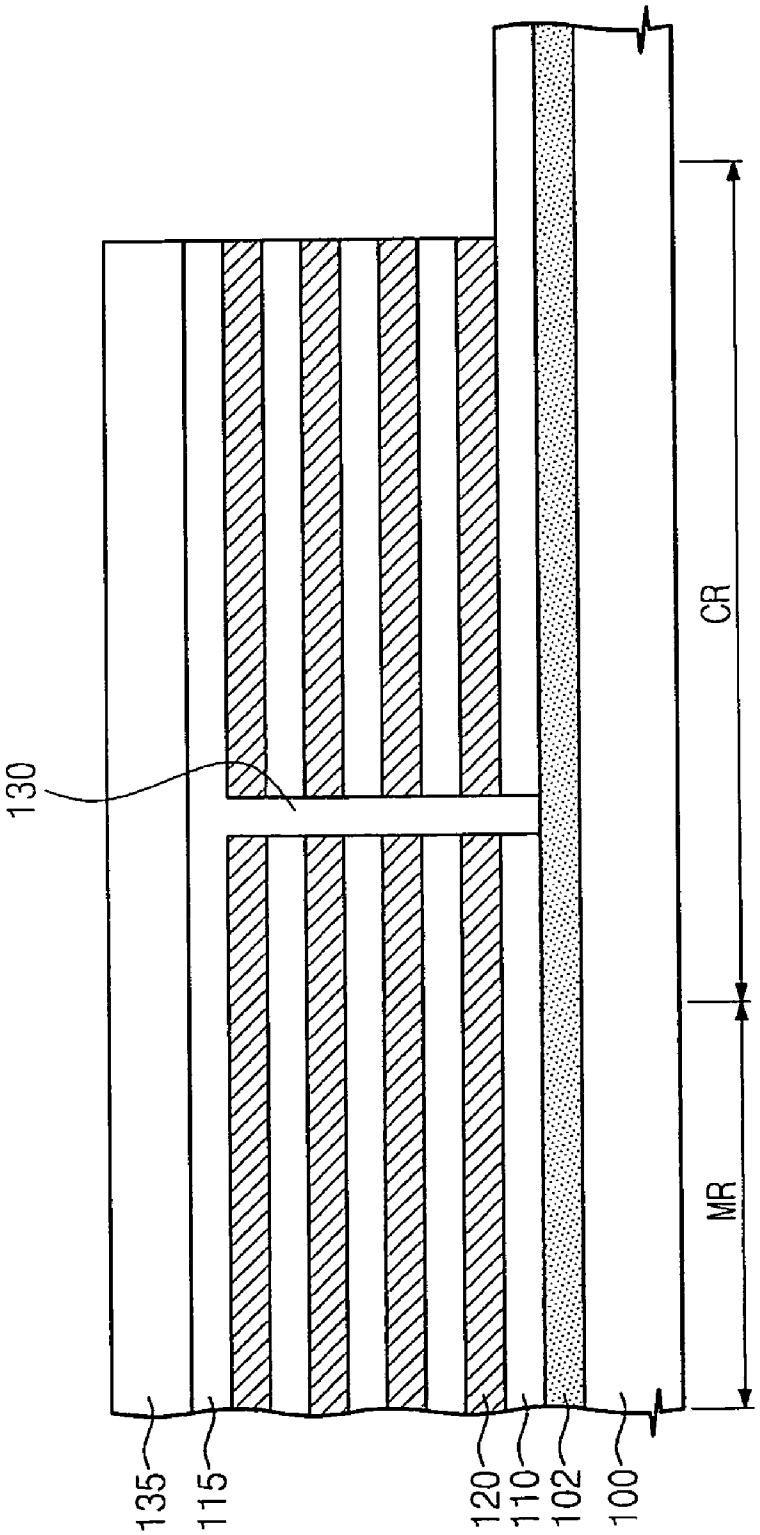


Fig. 13C

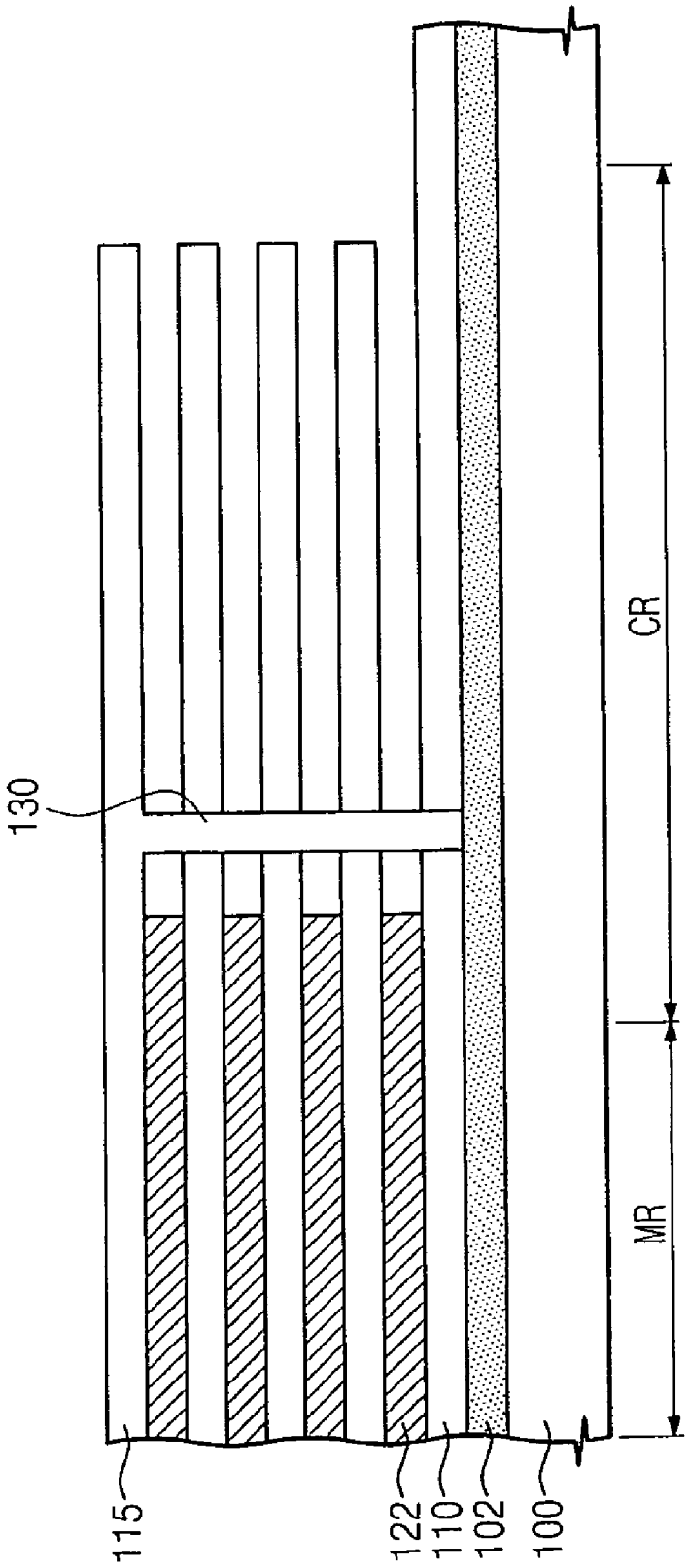


Fig. 13D

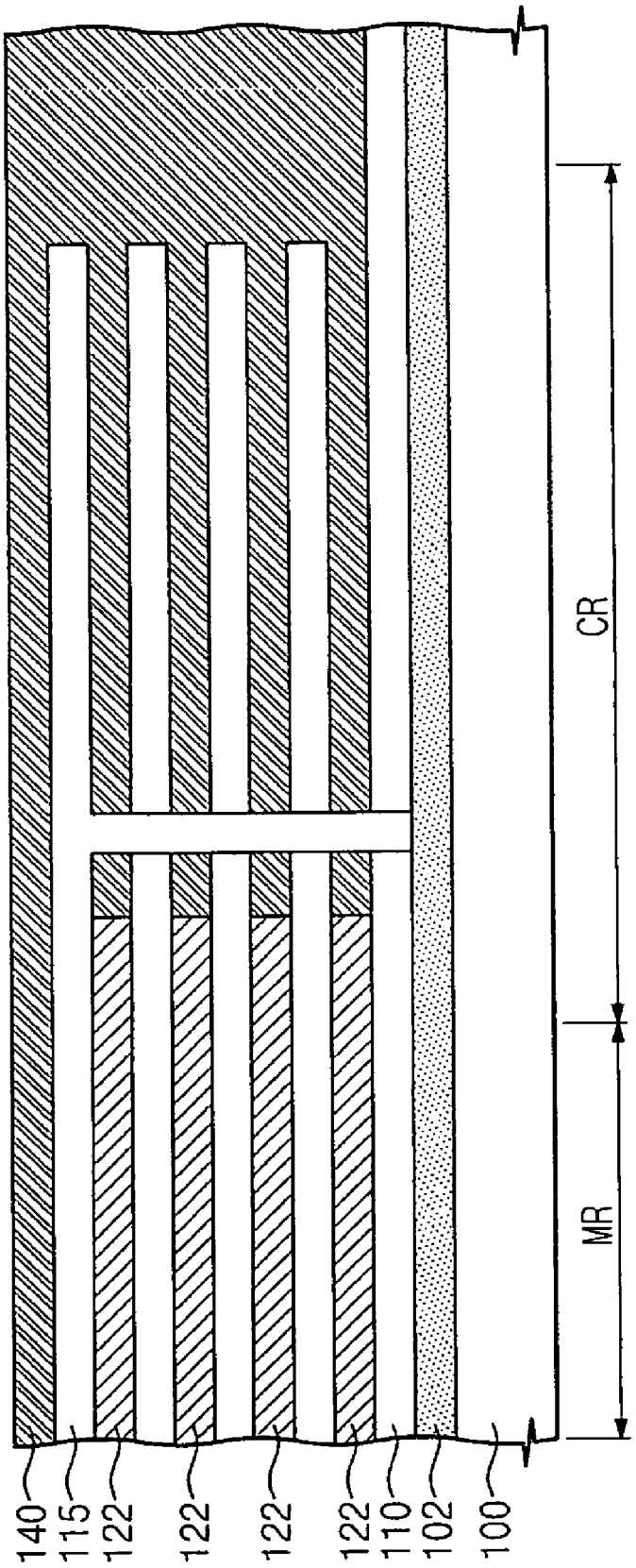


Fig. 13E

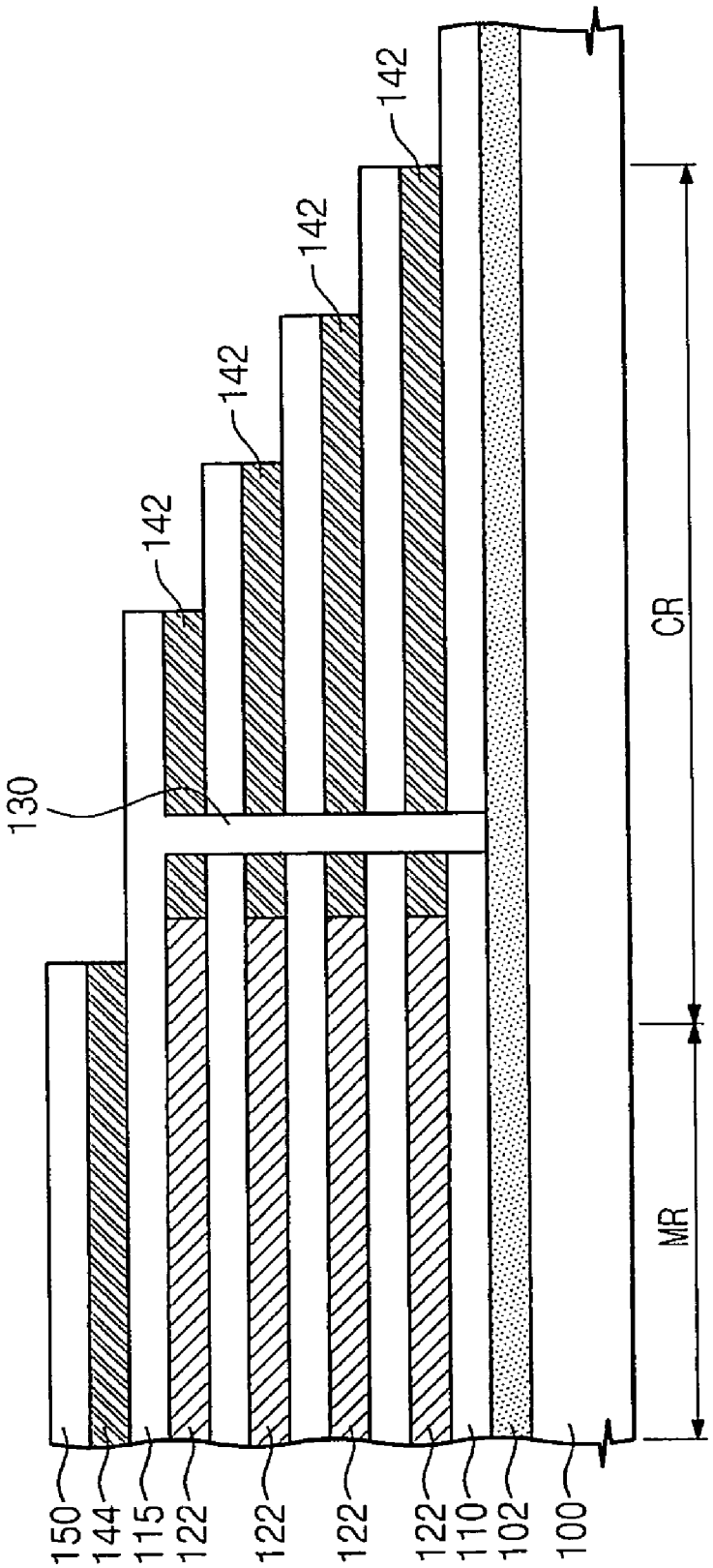
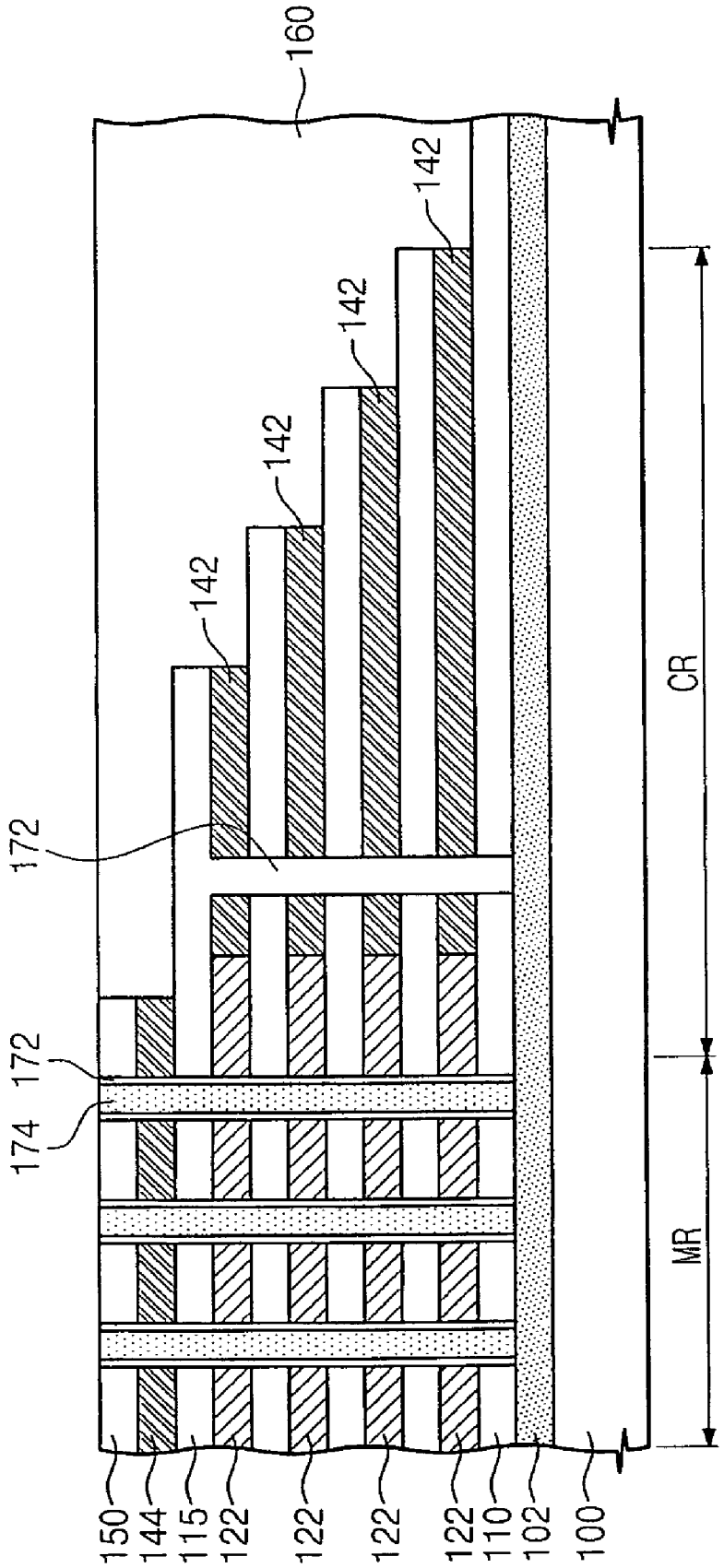


Fig. 13F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142
142
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142
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CR
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Fig. 13G

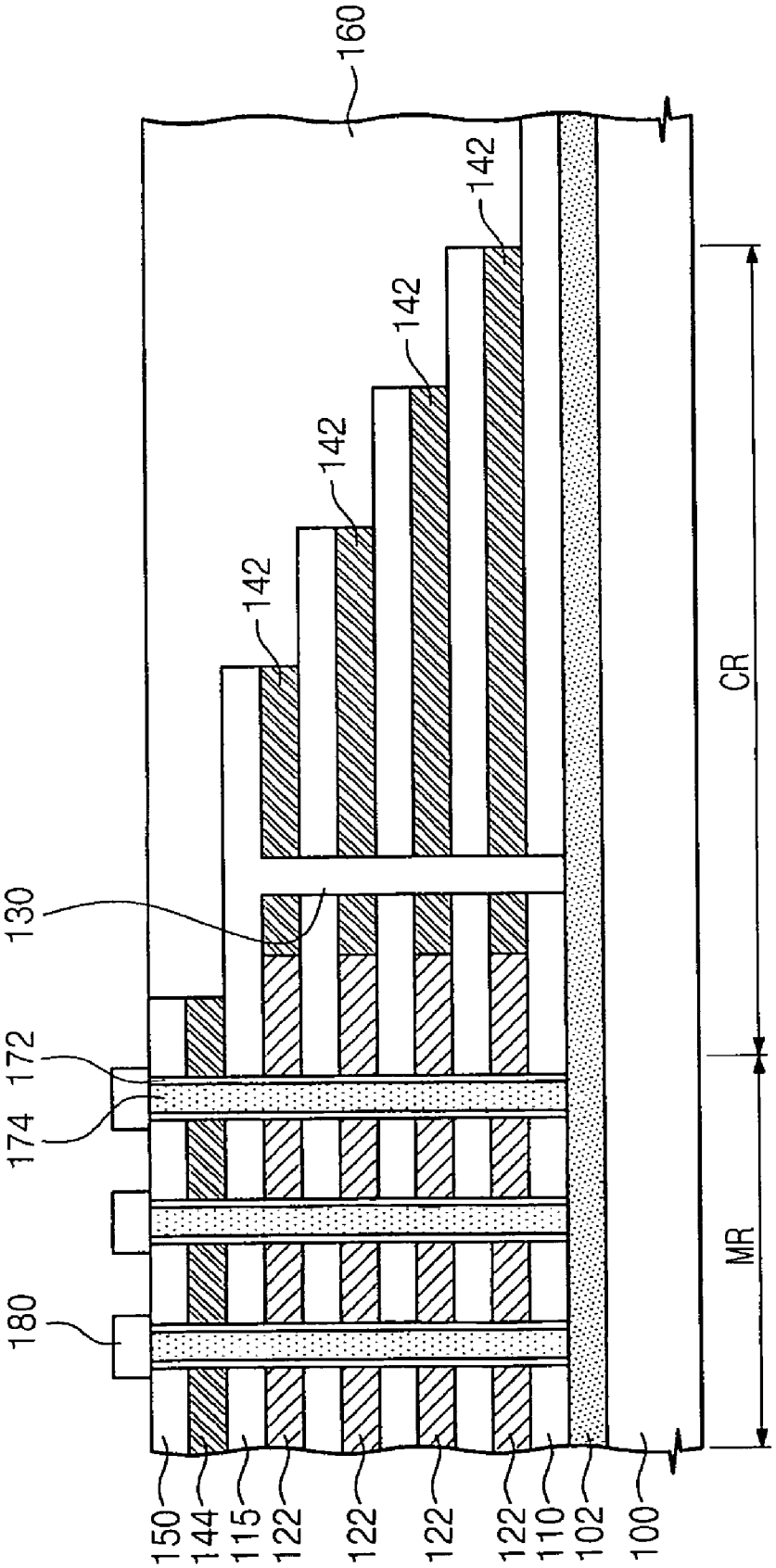
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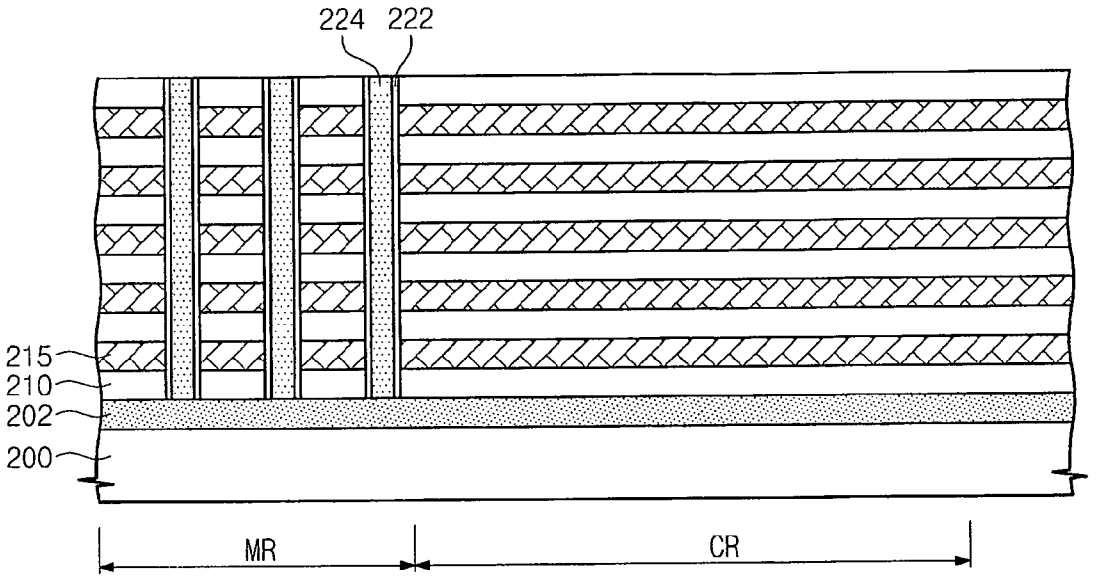
Fig. 14A



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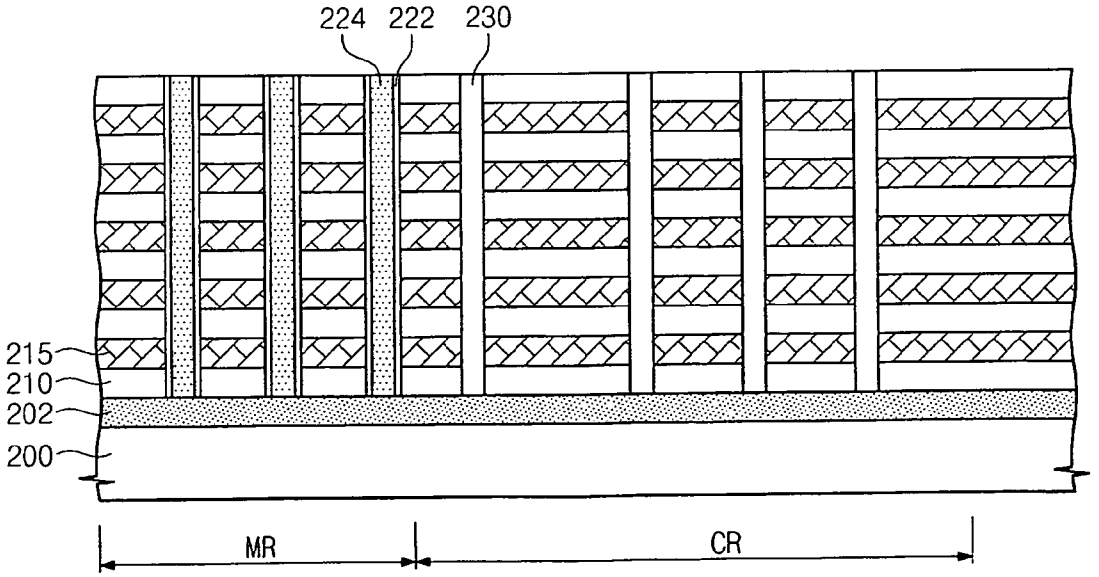

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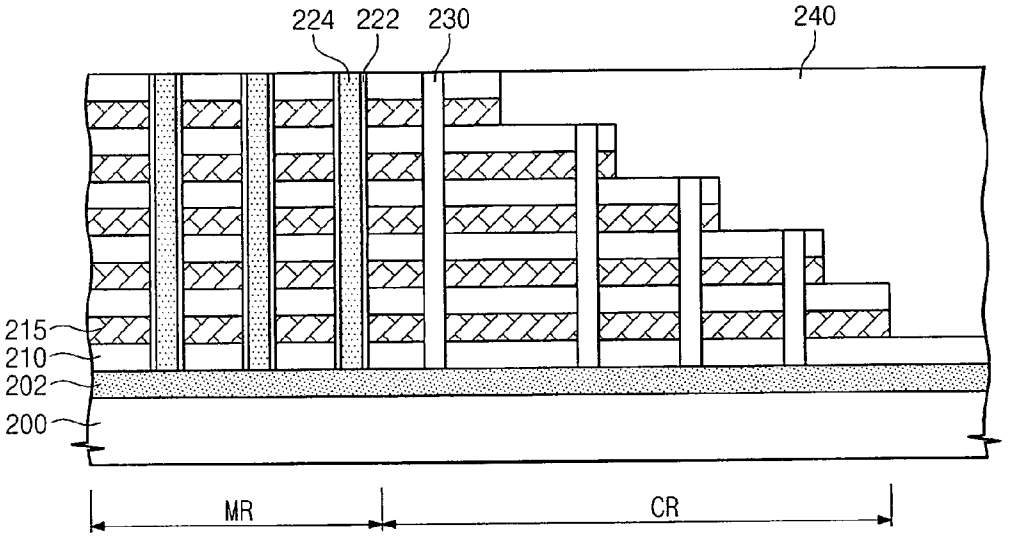

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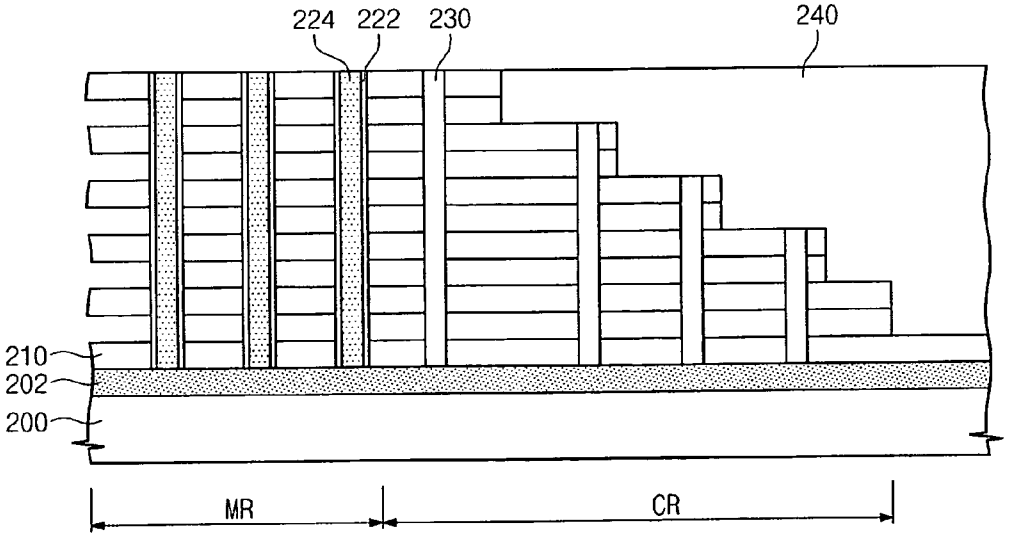


Fig. 14E

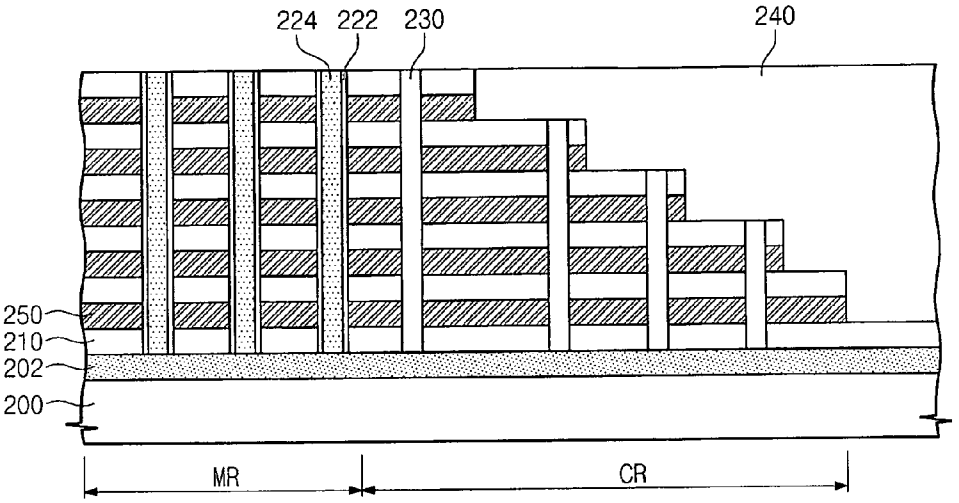


Fig. 14F

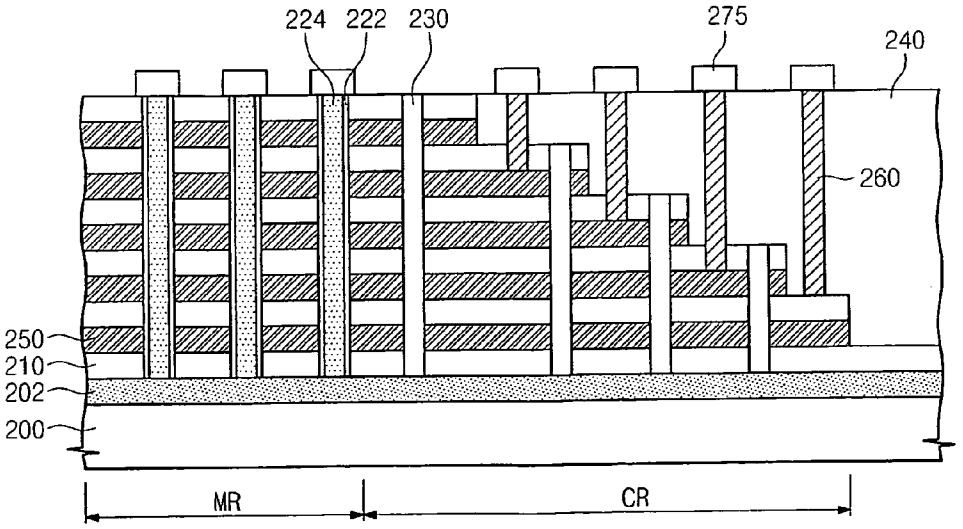


Fig. 15A

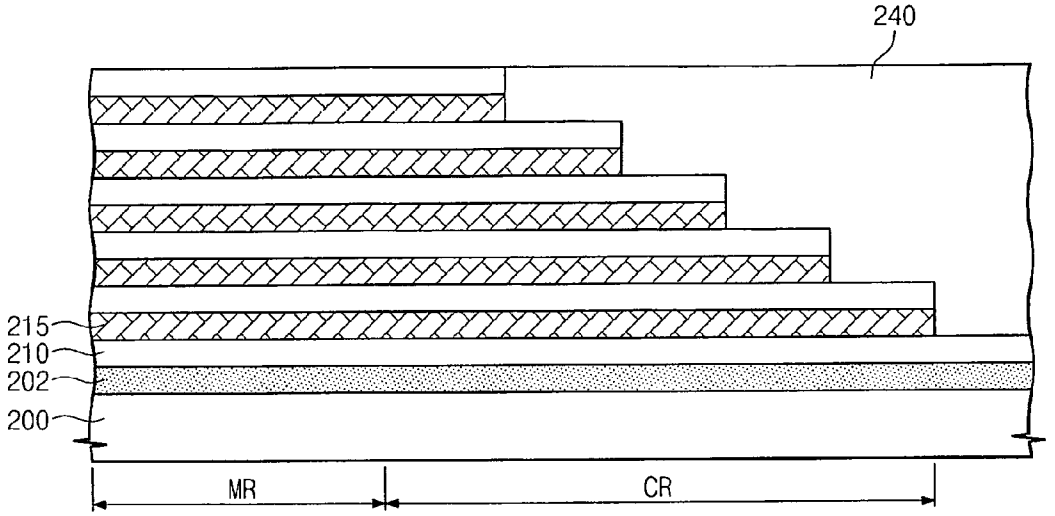
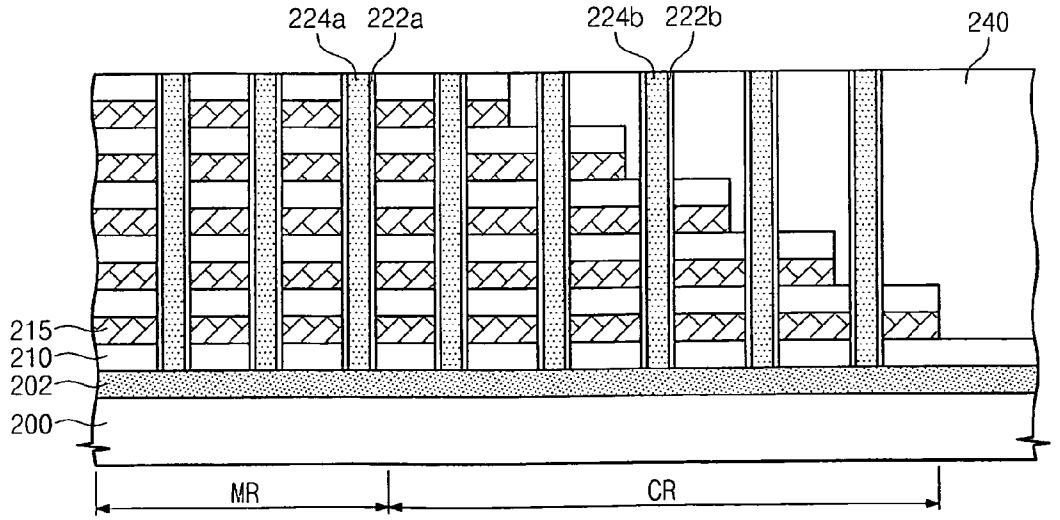


Fig. 15B



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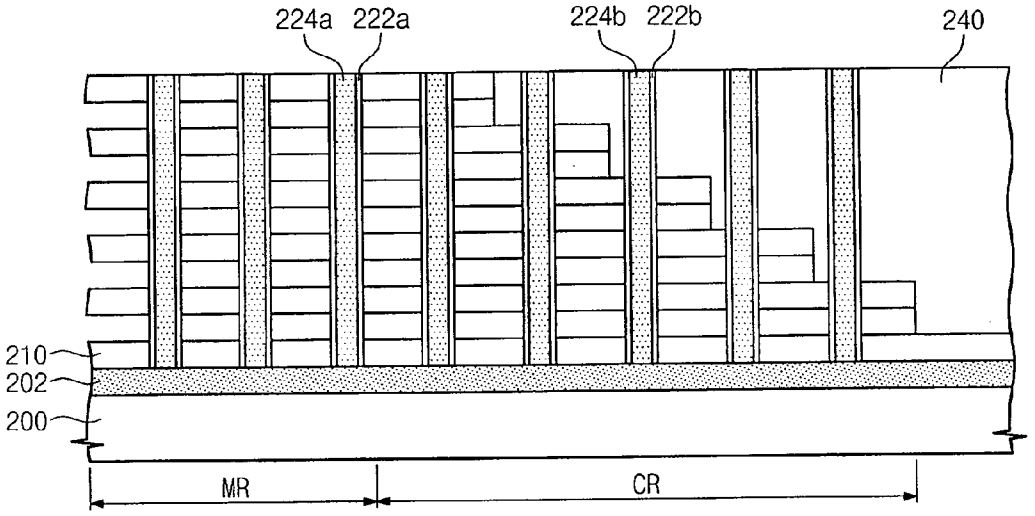


Fig. 15D

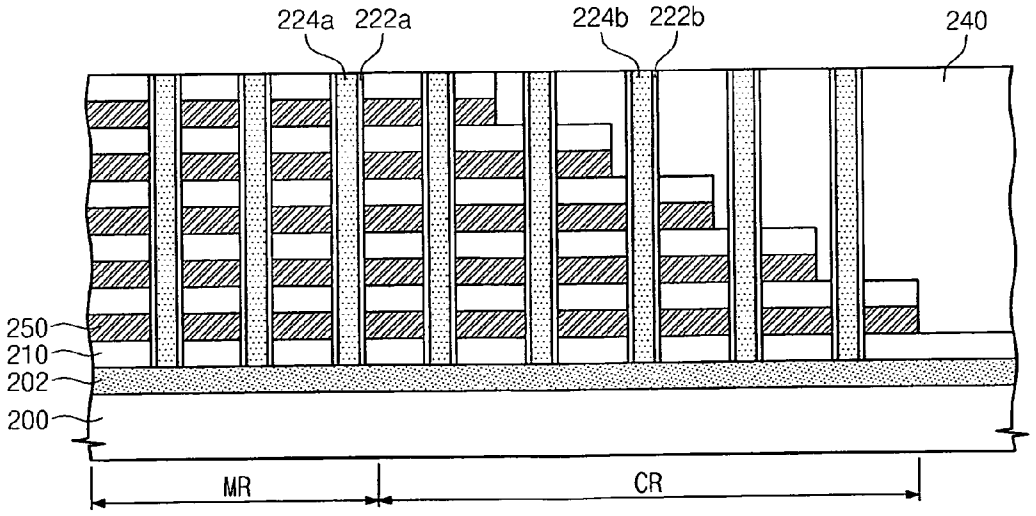


Fig. 15E

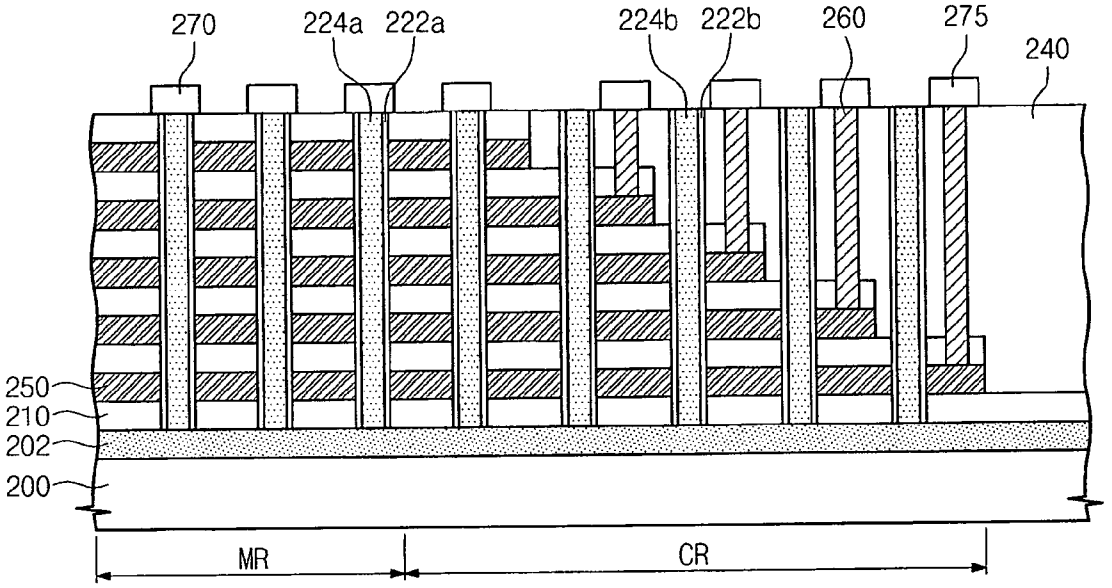


Fig. 16A

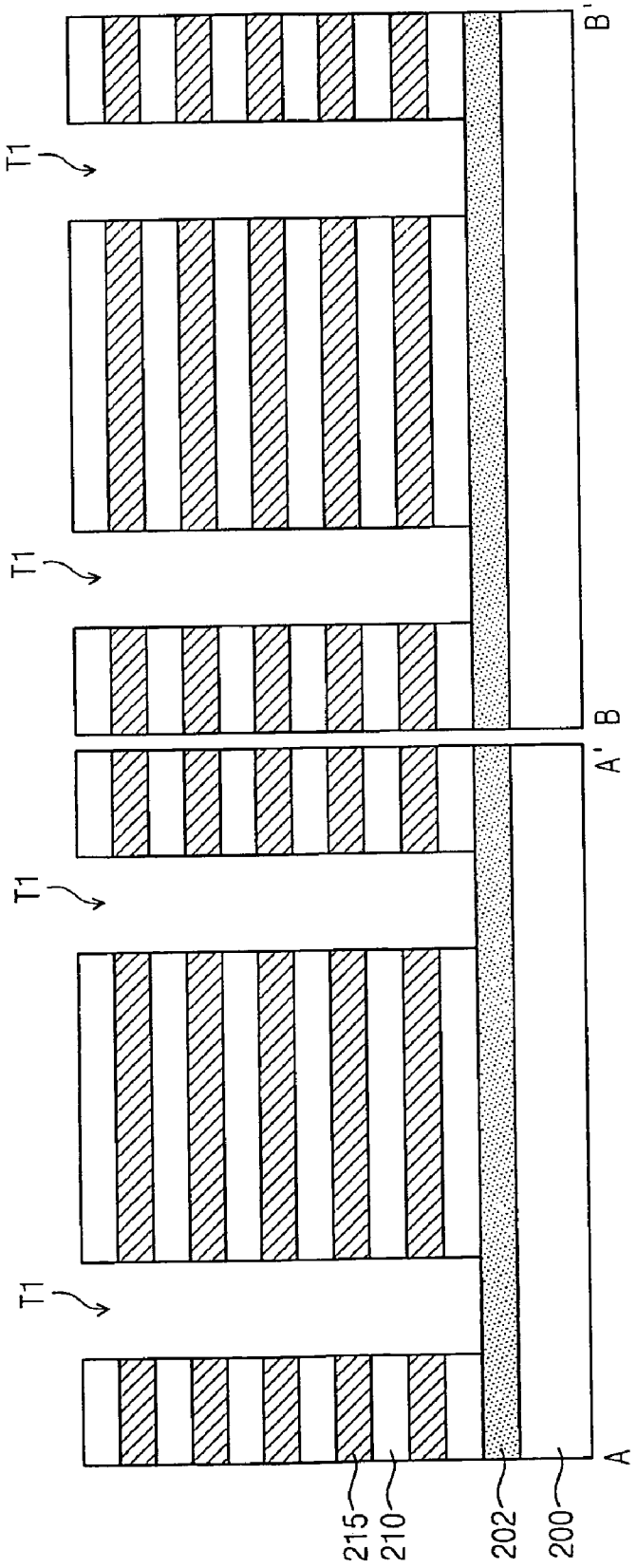


Fig. 16B

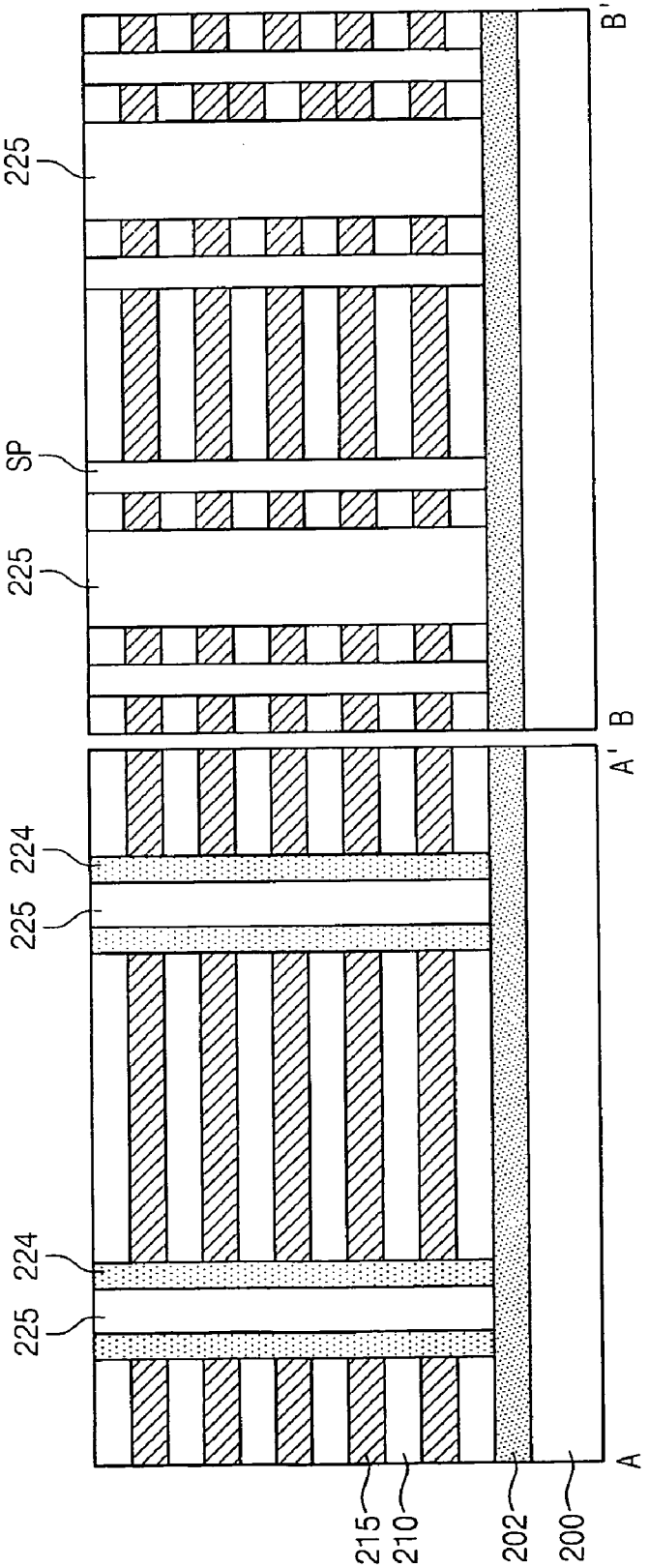


Fig. 16C

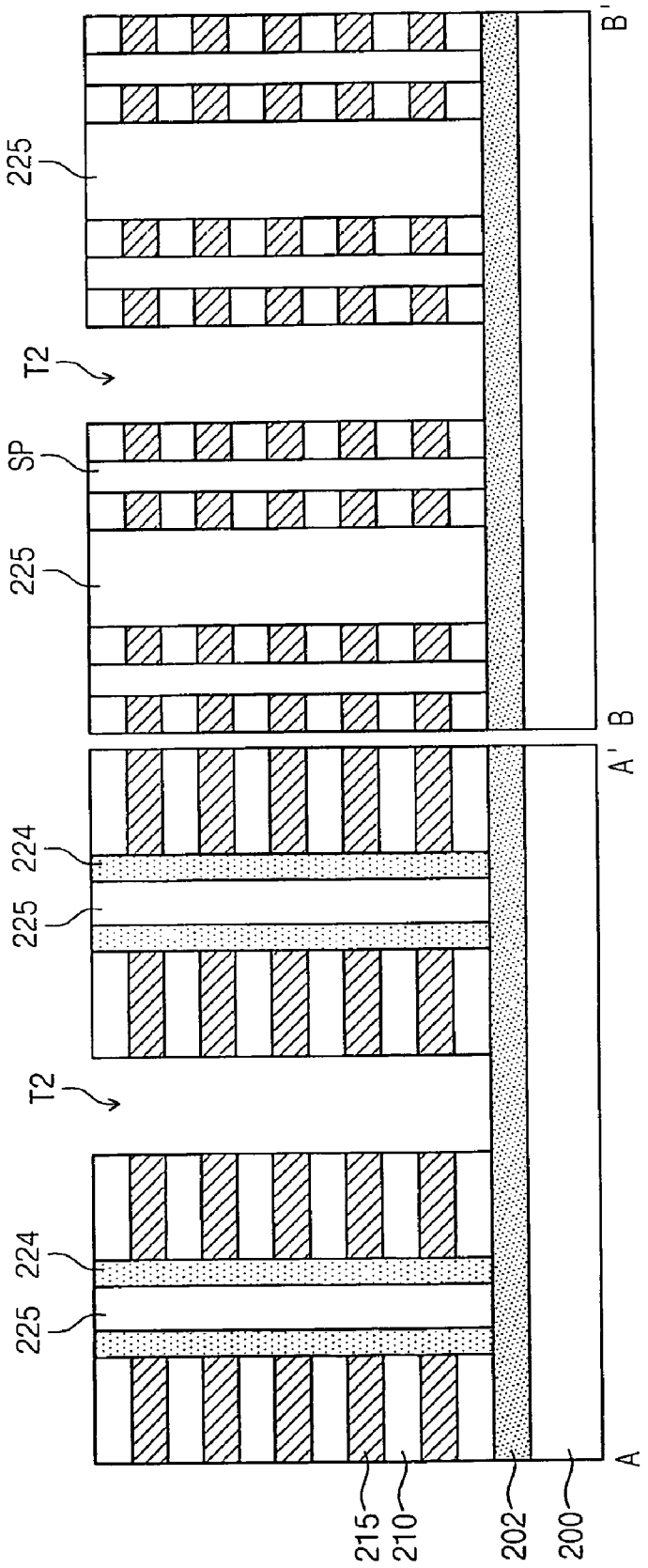


Fig. 16D

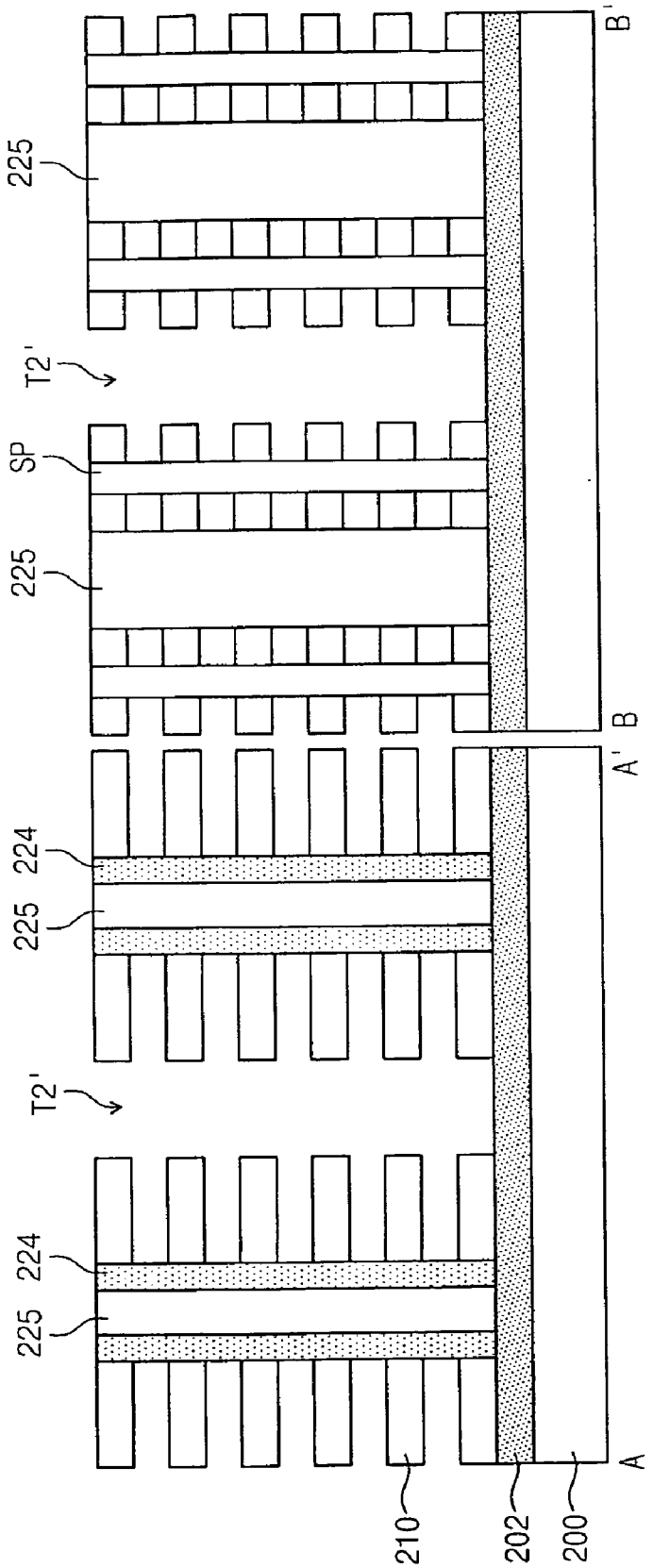


Fig. 16E

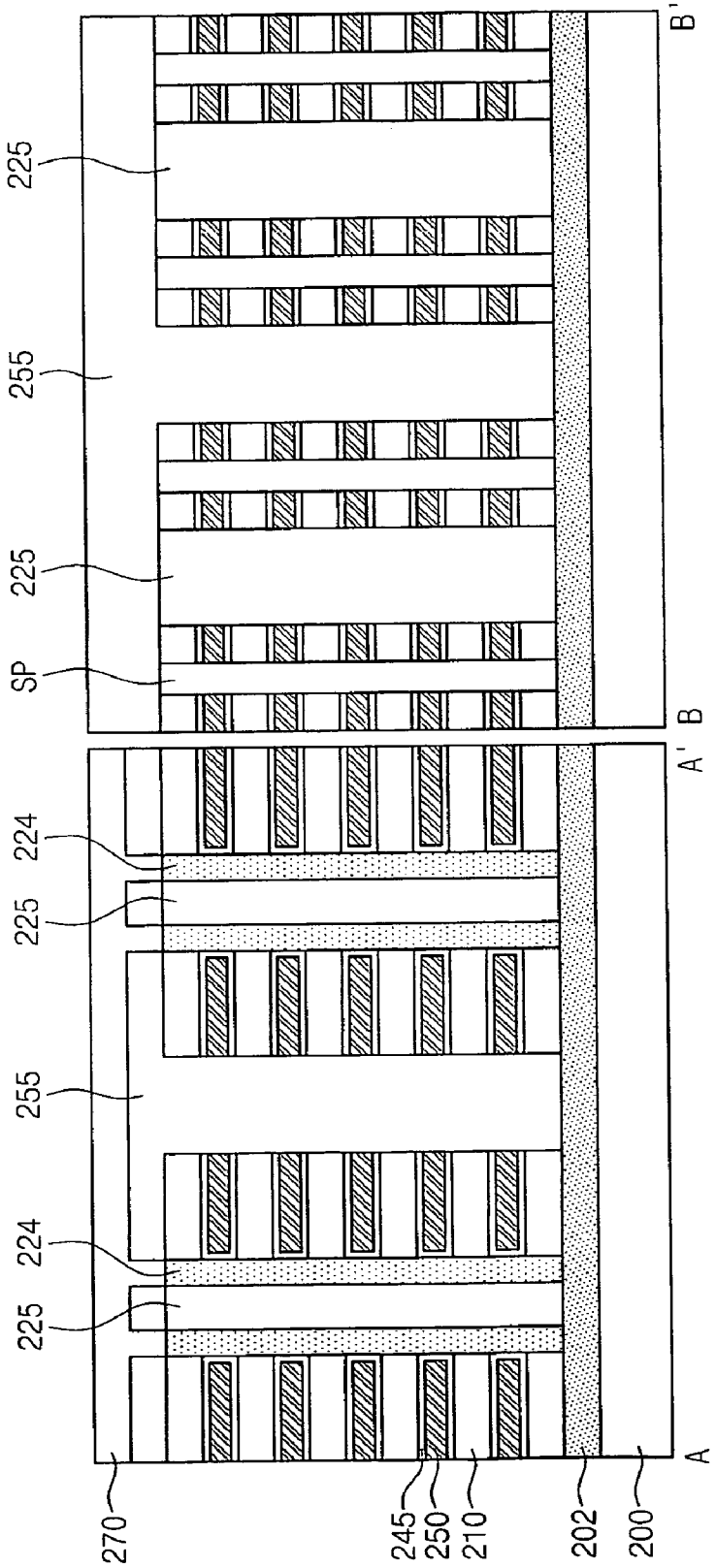
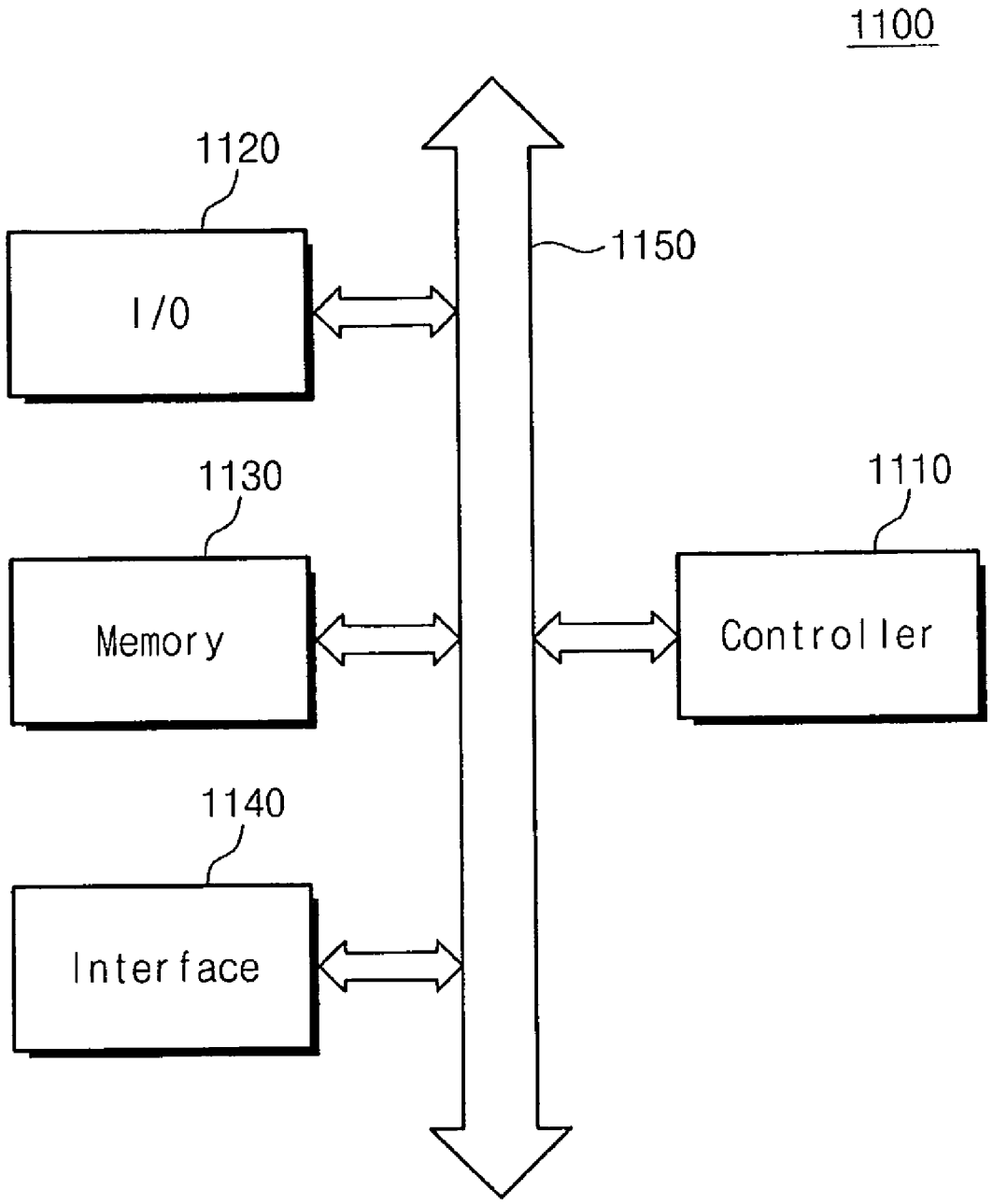


Fig. 17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1120
I/O
1150
1130
Memory
1110
Controller
1140
Interface

Fig. 18

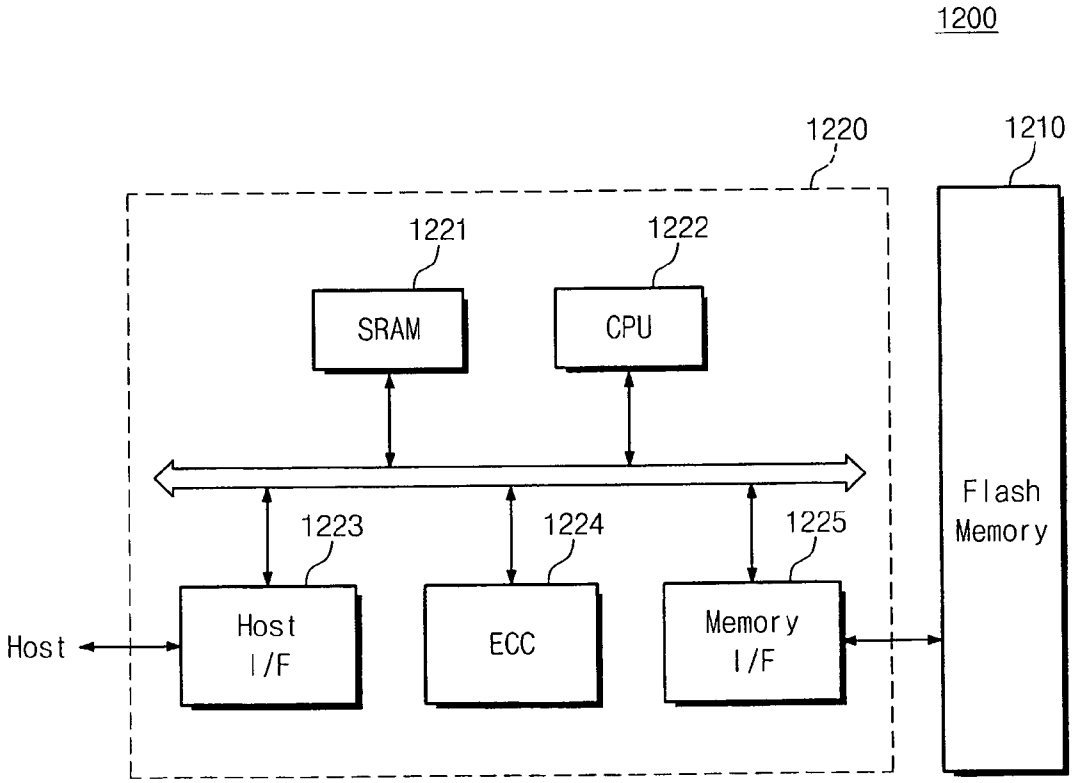
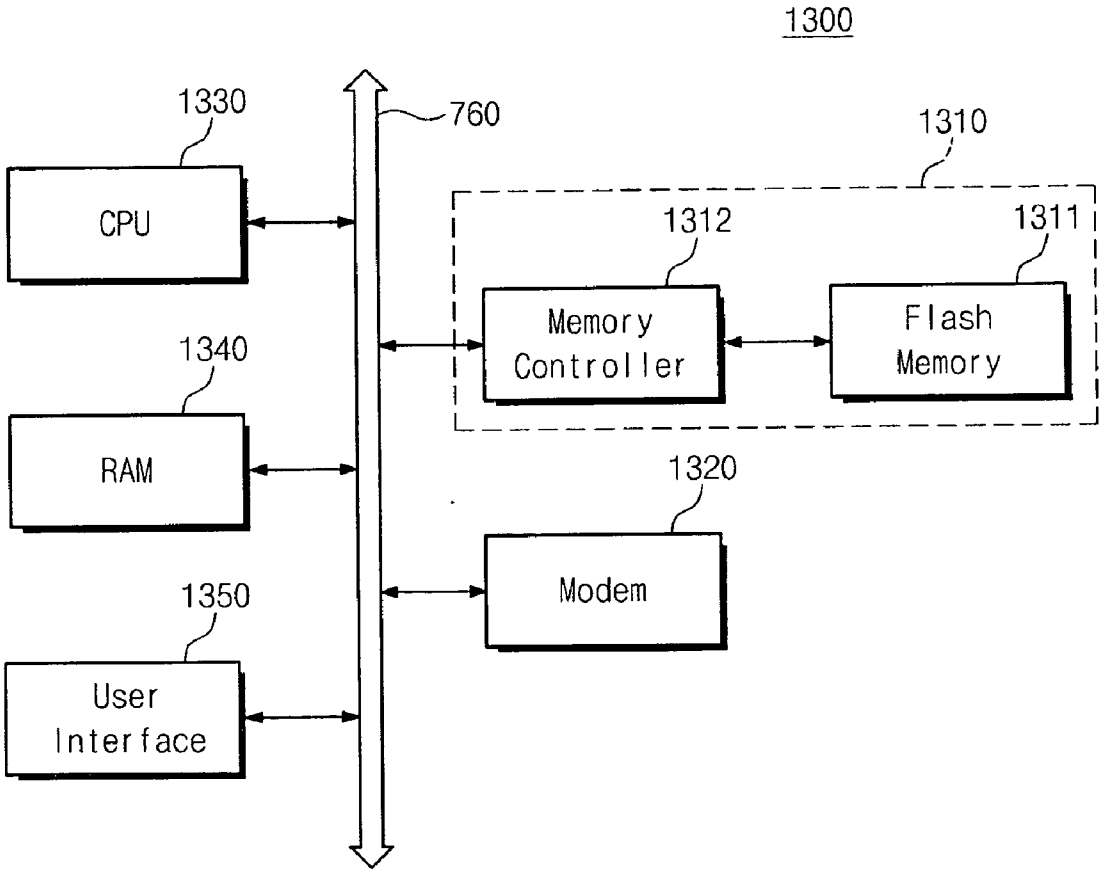

1200
1220
1210
1221
1222
SRAM
CPU
1223
1224
1225
Host
Host I/F
ECC
Memory I/F
Flash Memory

Fig. 19


1300
1330
760
1310
CPU
1312
1311
Memory Controller
Flash Memory
1340
RAM
1320
Modem
1350
User Interface

NONVOLATILE MEMORY DEVICE AND METHOD FOR FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This U.S. non-provisional patent application claims priority under 35 U.S.C. § 119 of Korean Patent Application Nos. 10-2008-0121886, filed on Dec. 3, 2008, and 10-2009-0049950, filed on Jun. 5, 2009, the entire contents of which are hereby incorporated by reference.

BACKGROUND

[0002] The present inventive concept relates to nonvolatile memory devices and methods for fabricating the same, and more particularly, to three-dimensional nonvolatile memory devices capable of reducing the resistance of gate electrodes and preventing process defects, and methods for fabricating the same.

[0003] Nonvolatile memory devices can electrically erase and write (or program) data and can retain data even when the power supply is interrupted. Accordingly, the use of nonvolatile memory devices is increasing in various fields.

[0004] Nonvolatile memory devices include various types of memory cell transistors. Nonvolatile memory devices are classified into NAND-type nonvolatile memory devices and NOR-type nonvolatile memory devices, depending on the cell array structures. The NAND-type nonvolatile memory device and the NOR-type nonvolatile memory device have the advantages and disadvantages of high integration and high operation speed.

[0005] In particular, the NAND-type nonvolatile memory device is advantageous for high integration because it includes a cell string structure having a plurality of memory cell transistors connected in series. Also, the NAND-type nonvolatile memory device has a much higher data update speed than the NOR-type nonvolatile memory device because it uses an operation scheme of simultaneously changing data stored in a plurality of memory cell transistors. Due to such a high integration level and high update speed, the NAND-type nonvolatile memory device is widely used in portable electronic products requiring mass storage, such as digital cameras and MP3 players.

[0006] Research is being conducted to facilitate and promote the advantages of NAND-type nonvolatile memory devices. Accordingly, a three-dimensional nonvolatile memory device is being developed.

SUMMARY OF THE INVENTIVE CONCEPT

[0007] Embodiments of the inventive concept provide three-dimensional nonvolatile memory devices capable of reducing the resistance of gate electrodes, and methods for fabricating the same.

[0008] Embodiments of the inventive concept also provide three-dimensional nonvolatile memory devices capable of preventing process defects, and methods for fabricating the same.

[0009] According to one aspect, the inventive concept is directed to a nonvolatile memory device including: a semiconductor substrate including a memory cell region and a contact region; a plurality of active pillars extending in the memory cell region perpendicular to the semiconductor substrate; and a plurality of gate electrodes including a first gate electrode disposed on the memory cell region to intersect the active pillars and a second gate electrode disposed on the contact region, connected to the first gate electrode and comprising metal material.

[0010] In one embodiment, the device further comprises a plurality of supporters extending in the contact region perpendicular to the semiconductor substrate to penetrate the gate electrodes.

[0011] In one embodiment, the first gate electrode of the memory cell region is comprised of metal material.

[0012] In one embodiment, the gate electrodes are stacked on the semiconductor substrate, with an interlayer dielectric therebetween; and the upper second gate electrode among the gate electrodes exposes the top of an edge portion of the lower second gate electrode.

[0013] In one embodiment, the device further comprises contact plugs connected respectively to the second gate electrodes of the contact region.

[0014] According to another aspect, the inventive concept is directed to a method for fabricating a nonvolatile memory device including: preparing a semiconductor substrate including a memory cell region and a contact region; forming a stack structure, in which gate conductive layers and dielectric layers are stacked alternately at least two or more times, on the semiconductor substrate; removing the gate conductive layers of the contact region from the stack structure to form first gate electrodes in the memory cell region; forming second gate electrodes, which are connected to the first gate electrodes and are comprised of metal material, in the contact region; and forming active pillars penetrating the first gate electrodes in the memory cell region.

[0015] In one embodiment, the forming of the first gate electrodes comprises removing the gate conductive layers on the contact region by supplying an etchant having an etch selectivity with respect to the gate conductive layer to the sidewall of the stack structure. In one embodiment, the forming of the second gate electrodes comprises filling the space between the dielectric layers on the contact region with metal material. In one embodiment, the method further comprises, before the forming of the first gate electrodes, forming a plurality of supporters penetrating the stack structure in the contact region. In one embodiment, the method further comprises, after the forming of the second gate electrodes, patterning the stack structure to expose an edge portion of the lower second gate electrode by the upper second gate electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The foregoing and other features and advantages of the inventive concept will be apparent from the more particular description of preferred embodiments of the inventive concept, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the inventive concept. In the drawings, the thickness of layers and regions are exaggerated for clarity.

[0017] FIG. **1** is a circuit diagram of a nonvolatile memory device according to exemplary embodiments of the inventive concept.

[0018] FIG. **2**A is a plan view of a nonvolatile memory device according to a first exemplary embodiment of the inventive concept.

[0019] FIGS. **2**B and **2**C are plan views of nonvolatile memory devices according to modifications of the first exemplary embodiment of the inventive concept.

[0020] FIG. **3** is a sectional view of the nonvolatile memory device according to the first exemplary embodiment of the inventive concept, which is taken along a line I-I' of FIGS. **2**A to **2**C.

[0021] FIG. **4** is a plan view of a nonvolatile memory device according to a second exemplary embodiment of the inventive concept.

[0022] FIG. **5** is a sectional view of the nonvolatile memory device according to the second exemplary embodiment of the inventive concept, which is taken along a line II-II' of FIG. **4**.

[0023] FIG. **6** is a plan view of a nonvolatile memory device according to a third exemplary embodiment of the inventive concept.

[0024] FIG. **7** is a sectional view of the nonvolatile memory device according to the third exemplary embodiment of the inventive concept, which is taken along lines A-A' and B-B' of FIG. **6**.

[0025] FIG. **8** is a plan view of a nonvolatile memory device according to a fourth exemplary embodiment of the inventive concept.

[0026] FIG. **9** is a sectional view of the nonvolatile memory device according to the fourth exemplary embodiment of the inventive concept, which is taken along a line I-I' of FIG. **8**.

[0027] FIG. **10** is a plan view of a nonvolatile memory device according to a fifth exemplary embodiment of the inventive concept.

[0028] FIG. **11** is a sectional view of the nonvolatile memory device according to the fifth exemplary embodiment of the inventive concept, which is taken along a line II-II' of FIG. **10**.

[0029] FIG. **12** is a plan view of a nonvolatile memory device according to a sixth exemplary embodiment of the inventive concept.

[0030] FIGS. **13**A to **13**G are sectional views illustrating a method for fabricating the nonvolatile memory devices according to the first and fourth exemplary embodiments of the inventive concept.

[0031] FIGS. **14**A to **14**F are sectional views illustrating a method for fabricating the nonvolatile memory devices according to the second and fifth exemplary embodiments of the inventive concept.

[0032] FIGS. **15**A to **15**E are sectional views illustrating another method for fabricating the nonvolatile memory devices according to the second and fifth exemplary embodiments of the inventive concept.

[0033] FIGS. **16**A to **16**E are sectional views illustrating a method for fabricating the nonvolatile memory devices according to the third and sixth exemplary embodiments of the inventive concept.

[0034] FIG. **17** is a block diagram of a memory system including a nonvolatile memory device according to exemplary embodiments of the inventive concept.

[0035] FIG. **18** is a block diagram of a memory card provided with a flash memory device according to an exemplary embodiment of the inventive concept.

[0036] FIG. **19** is a block diagram of an information processing system provided with a flash memory system according to the inventive concept.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0037] Preferred embodiments of the inventive concept will be described below in more detail with reference to the accompanying drawings. The inventive concept may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this description will be thorough and complete, and will fully convey the scope of the inventive concept to those skilled in the art. Throughout the specification, like reference numerals refer to like elements.

[0038] In the following description, the technical terms are used only for describing specific exemplary embodiments while not limiting the inventive concept. The terms of a singular form may include plural forms unless otherwise specified. The meaning of "include," "comprise," "including," or "comprising," specifies a property, a region, a fixed number, a step, a process, an element and/or a component but does not exclude other properties, regions, fixed numbers, steps, processes, elements and/or components. It will also be understood that when a layer (or film) is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present.

[0039] Additionally, the embodiments in the detailed description will be described with reference to sectional views or plan views as ideal exemplary views of the inventive concept. In the drawings, the dimensions of layers and regions are exaggerated for clarity of illustration. Accordingly, shapes of the exemplary views may be modified according to manufacturing techniques and/or allowable errors. Therefore, the embodiments of the inventive concept are not limited to the specific shape illustrated in the exemplary views, but may include other shapes that may be created according to manufacturing processes. For example, although an etched region is illustrated as being angled, it may also be rounded. Areas exemplified in the drawings have general properties, and are used to illustrate specific shapes of device regions. Thus, these should not be construed as limiting the scope of the inventive concept.

[0040] Hereinafter, exemplary embodiments of the inventive concept will be described in detail with reference to the accompanying drawings. Nonvolatile memory devices according to the exemplary embodiments of the inventive concept have a three-dimensional structure.

[0041] FIG. **1** is a circuit diagram of a nonvolatile memory device according to exemplary embodiments of the inventive concept.

[0042] Referring to FIG. **1**, a nonvolatile memory device according to exemplary embodiments of the inventive concept includes a cell array including a plurality of strings STR. The cell array includes bit lines BL**1**~BL**3**, word lines WL**1**~WL**4**, upper and lower select lines USL**1**~USL**3** and LSL, and a common source line CSL. The strings STR are provided between the common source line CSL and the bit lines BL**1**~BL**3**.

[0043] Each string STR includes upper and lower select transistors UST and LST, and memory cell transistors MC that are connected in series between the upper and lower select transistors UST and LST. The drains of the upper select transistors UST are connected to the bit lines BL**1**~BL**3**, and the sources of the lower select transistors LST are connected in common to the common source line CSL.

[0044] The upper select transistors UST are connected to the upper select lines USL**1**~USL**3**, and the lower select transistors LST are connected respectively to the lower select lines LSL. The memory cells MC are connected respectively to the word lines WL**1**~WL**4**.

[0045] The cell array has a three-dimensional structure. That is, the strings STR are configured in such a way that the memory cells MC are connected in series in a Z-axis direction perpendicular to an XY plane parallel to the top surface of a semiconductor substrate. Accordingly, the channel of the memory cell transistors MC and the select transistors UST and LST may be formed perpendicular to the XY plane.

[0046] In the three-dimensional nonvolatile memory device, 'm' memory cells may be formed on each XY plane, and XY planes with 'm' memory cells may be stacked in 'n' layers (where 'm' and 'n' are natural numbers).

[0047] Hereinafter, a nonvolatile memory device according to a first exemplary embodiment of the inventive concept will be described with reference to FIGS. **2**A to **2**C and FIG. **3**.

[0048] FIG. **2**A is a plan view of a nonvolatile memory device according to a first exemplary embodiment of the inventive concept. FIGS. **2**B and **2**C are plan views of nonvolatile memory devices according to modifications of the first exemplary embodiment of the inventive concept. FIG. **3** is a sectional view of the nonvolatile memory device according to the first exemplary embodiment of the inventive concept, which is taken along a line I-I' of FIGS. **2**A to **2**C.

[0049] Referring to FIGS. **2**A and **3**, interlayer dielectrics **110** and gate electrodes LSL, WL and USL are alternately stacked on a semiconductor substrate **100**. More specifically, the semiconductor substrate **100** includes a memory cell region MR and a contact region CR that is disposed on the edge portion of the memory cell region MR. In the first exemplary embodiment of the inventive concept, the contact region CR is disposed around the memory cell region MR. In exemplary embodiments of the inventive concept, the memory cell region MR and the contact region CR are regions for gate electrodes.

[0050] An impurity region (or well) **102**, provided as a common source line (CSL of

[0051] FIG. **1**), is formed in the semiconductor substrate **100**, and interlayer dielectrics **110** and gate electrodes LSL, WL and USL are alternately stacked on the impurity region **102**. Among the stacked gate electrodes LSL, WL and USL, the lowermost and uppermost gate electrodes LSL and USL are used as select lines, and the other gate electrodes WL are used as word lines.

[0052] The lower select line LSL (i.e., the lowermost gate electrode) may be formed in the shape of a plate or in the shape of lines separated from each other. The upper select line USL (i.e., the uppermost gate electrode) may be formed in the shape of lines separated from each other. The word lines WL between the lower select line LSL and the upper select line USL may be formed in the shape of a plate. Also, the areas of the gate electrodes LSL, WL, and USL may decrease with an increase in the distance from the semiconductor substrate **100**.

[0053] More specifically, the gate electrodes LSL, WL and USL may extend from the memory cell region MR to the contact region CR. The gate electrodes LSL, WL and USL of the memory cell region MR and the gate electrodes of the contact region CR may be formed of different conductive materials. That is, the gate electrodes LSL, WL and USL of the memory cell region MR may be formed of polysilicon, while the gate electrodes LSL, WL and USL of the contact region CR may comprise metal material that is lower in specific resistance than polysilicon. For example, the gate electrodes LSL, WL and USL of the contact region CR may be formed of tungsten (W), aluminum (Al), titanium (Ti), or tantalum (Ta). Accordingly, the resistance of the gate electrodes LSL, WL and USL can be reduced in comparison with the case where the gate electrodes LSL, WL and USL are formed of polysilicon. Therefore, a signal delay due to an increase in the resistance of the gate electrodes LSL, WL and USL can be reduced, thus making it possible to improve the operation speed of the nonvolatile memory device. For the uppermost line-shaped gate electrodes USL, both the memory cell region MR and the contact region MR may comprise metal material.

[0054] Active pillars PL are formed in the memory cell region MR perpendicular to the plane of the semiconductor substrate **100**. The active pillars PL are formed of semiconductor material. The active pillars PL may penetrate the gate electrodes LSL, WL and USL of the memory cell region MR. The pillars PL may be spaced apart from each other, and may be arranged in a matrix configuration on a plane. Also, the active pillars PL may be electrically connected to the impurity region **102** of the semiconductor substrate **100** by penetrating the gate electrodes LSL, WL and USL. The active pillars PL are provided for the channels of transistors, which correspond to the strings of the nonvolatile memory device according to the embodiments of the inventive concept. That is, the channels of memory cell transistors and select transistors (LST, UST and MC of FIG. **1**) in each string may be electrically connected through the active pillars PL.

[0055] Also, in the memory cell region MR, a charge storage layer CS is formed to surround each of the active pillars PL. That is, the charge storage layer CS is disposed between the active pillar PL and the gate electrodes LSL, WL and USL. Also, bit lines are electrically connected on the active pillars PL.

[0056] The gate electrodes LSL, WL and USL of the contact region CR may be stacked in the shape of a stair. That is, the areas of the plate-type gate electrodes LSL, WL and USL stacked on the semiconductor substrate **100** may decrease with an increase in the distance from the semiconductor substrate **100**, so that the upper gate electrode may be stacked to expose the end portion of the lower gate electrode. That is, the end portion of each of the gate electrodes LSL, WL and USL is not aligned with the sidewalls of the upper and lower gate electrodes LSL, WL and USL. Therefore, the gate electrodes LSL, WL and USL of the contact region CR may be electrically connected through contacts CT to global word lines GWL.

[0057] Also, in the contact region CR, supporters SP may penetrate some of the gate electrodes LSL, WL and USL. The supporters SP may serve to support the edge portions of the interlayer dielectrics **110** and the gate electrodes LSL, WL and USL that are alternately stacked on the semiconductor substrate **100**. Specifically, the supporters SP may be formed in a pillar shape to penetrate the gate electrodes LSL, WL and USL and the interlayer dielectrics **110**. The supporters SP may be formed of dielectric material, so that they may be electrically connected to the interlayer dielectrics **110** between the gate electrodes LSL, WL and USL. In the first exemplary embodiment of the inventive concept, the supporters SP may penetrate the gate electrodes LSL and WL (i.e., all but the uppermost gate electrode USL). Also, in the first exemplary embodiment of the inventive concept, the supporters SP may have the same length. The supporters SP of the same length may be formed in the edge portion of the memory cell region MR. That is, the supporters SP may be formed in corner portion of the memory cell region MR. As well as in

the corner portion of the memory cell region MS, the supporters SP may be formed in certain regions of the edge portions of the gate electrodes LSL, WL and USL in such a way that they are spaced apart from each other.

[0058] Referring to FIGS. **2**B, **2**C and **3**, the supporters SP according to the first exemplary embodiment of the inventive concept may have various shapes instead of the shape of a cylindrical pillar.

[0059] That is, as illustrated in FIG. **2**B, supporters SP' may be pillars that are line-shaped in the plan view. The line-shaped supporters SP' are disposed in the contact region MR of the gate electrodes LSL, WL and USL, and are formed around the memory cell region MR. The line-shaped supporters SP' are spaced apart from each other, and may have the same length or different lengths.

[0060] Also, as illustrated in FIG. **2**C, supporters SP" may have line patterns that are connected to each other and extend in different directions on the plane. The supporters SP" may be formed to surround the corner portions of the memory cell region MR as illustrated in FIG. **2**C.

[0061] Hereinafter, a nonvolatile memory device according to a second exemplary embodiment of the inventive concept will be described with reference to FIGS. **4** and **5**. In describing the second exemplary embodiment, detailed description of elements of the first exemplary embodiment will not be repeated.

[0062] FIG. **4** is a plan view of a nonvolatile memory device according to a second exemplary embodiment of the inventive concept. FIG. **5** is a sectional view of the nonvolatile memory device according to the second exemplary embodiment of the inventive concept, which is taken along a line II-II' of FIG. **4**.

[0063] Referring to FIGS. **4** and **5**, in a nonvolatile memory device according to a second exemplary embodiment of the inventive concept, gate electrodes LSL, WL and USL have the shape of a line that extends from a memory cell region MR to a contact region CR. That is, the memory cell region MR corresponds to a central portion of the line-shaped gate electrodes LSL, WL and USL, and the contact region CR corresponds to one or both end portions of the line-shaped gate electrodes LSL, WL and USL. In the description of the second exemplary embodiment of the inventive concept, the contact region CR corresponds to both edge portions of the memory cell region MR.

[0064] All of the line-shaped gate electrodes LSL, WL and USL of the memory cell region MR and the contact region CR may be formed of the same material. Alternatively, the gate electrodes LSL, WL and USL of the memory cell region MR and the gate electrodes LSL, WL and USL of the contact region CR may be formed of different conductive materials, as in the first exemplary embodiment. That is, all of the gate electrodes LSL, WL and USL of the memory cell region MR and the contact region CR may comprise metal material. Alternatively, the gate electrodes LSL, WL and USL of the memory cell region MR may be formed of polysilicon, and the gate electrodes LSL, WL and USL of the contact region CR may comprise metal material.

[0065] Active pillars PL penetrate the gate electrodes LSL, WL and USL stacked in the memory cell region MR, and supporters SP penetrate the gate electrodes LSL, WL and USL stacked in the contact region CR.

[0066] The active pillars PL are formed of semiconductor material, and are connected to a semiconductor substrate **100** by penetrating the stacked gate electrodes LSL, WL and USL. A charge storage layer CS is formed around each of the active pillars PL, and bit lines intersecting the gate electrodes LSL, WL and USL are electrically connected on the active pillars PL.

[0067] The supporters SP may be pillars formed of dielectric material, and may be formed in both end portions of the gate electrodes LSL, WL and USL (i.e., the contact region CR) in such a way that they are spaced apart from the active pillars PL. Specifically, in the second exemplary embodiment of the inventive concept, the supporters SP may be formed on one side of the active pillars PL located at the edge portion of the memory region MR, and may penetrate all of the stacked gate electrodes LSL, WL and USL. Also, the gate electrodes LSL, WL and USL of the contact region CR may be electrically connected to global word lines GWL through contacts CT.

[0068] The active pillars PL of the nonvolatile memory device according to the second exemplary embodiment of the inventive concept may be formed on one sidewall of the gate electrodes LSL, WL and USL as illustrated in FIG. **7**.

[0069] FIG. **6** is a plan view of a nonvolatile memory device according to a third exemplary embodiment of the inventive concept. FIG. **7** is a sectional view of the nonvolatile memory device according to the third exemplary embodiment of the inventive concept, which is taken along lines A-A' and B-B' of FIG. **6**.

[0070] Referring to FIGS. **6** and **7**, line-shaped gate electrodes (WL, **250**) are stacked, and bit lines (BL, **270**) intersecting the gate electrodes (WL, **250**) may be disposed on the stacked gate electrodes (WL, **250**). Active pillars (PL', **224**) may be formed perpendicularly to a semiconductor substrate **200** and intersect one sidewall of the stacked gate electrodes (WL, **250**). In the third exemplary embodiment, instead of being a cylindrical shape, the active pillars (PL', **224**) may be a structure that is formed by patterning on one sidewall of the stacked gate electrodes (WL, **250**). That is, the active pillars (PL', **224**) may be disposed on one sidewall of the stacked gate electrodes (WL, **250**) in such a way that they are spaced apart from each other. The active pillars (PL', **224**) formed on one sidewall of the stacked gate electrodes (WL, **250**) may be formed to face the active pillars (PL', **224**) intersecting one sidewall of the adjacent gate electrodes (WL, **250**). Also, a charge storage layer **245** is disposed between the top and bottom surfaces of the gate electrodes (WL, **250**) and one sidewall contacting the active pillars (PL', **224**).

[0071] Also, as in the second exemplary embodiment, supporters SP supporting the gate electrodes (WL, **250**) are formed in the contact region CR. The supporters SP may be circular pillars formed of dielectric material, and may penetrate all of the stacked gate electrodes (WL, **250**). Also, the gate electrodes (WL, **250**) of the contact region CR may be electrically connected to global word lines GWL through contacts CT.

[0072] Hereinafter, nonvolatile memory devices according to exemplary embodiments 4 to 6 of the inventive concept will be described in detail.

[0073] FIG. **8** is a plan view of a nonvolatile memory device according to a fourth exemplary embodiment of the inventive concept. FIG. **9** is a sectional view of the nonvolatile memory device according to the fourth exemplary embodiment of the inventive concept, which is taken along a line I-I' of FIG. **8**. In describing the fourth exemplary embodiment, detailed description of elements of other exemplary embodiments will not be repeated.

[0074] Referring to FIGS. **8** and **9**, plate-shaped gate electrodes LSL, WL and USL are formed on a semiconductor substrate **100**, with interlayer dielectrics **110** disposed therebetween. The plate-shaped gate electrodes LSL, WL and USL are formed over a memory cell region MR and contact regions CR around the memory cell region MR. The stacked gate electrodes LSL, WL and USL in the contact region CR may have a stair shape. That is, the upper gate electrode is formed to expose the lower gate electrode. Because the gate electrodes LSL, WL and USL are stacked in a stair shape, the interlayer dielectrics between the gate electrodes LSL, WL and USL may have a stair-shaped stack structure.

[0075] Active pillars PL penetrate the gate electrodes LSL, WL and USL of the memory cell region MR. Supporters SP of different lengths may be formed at the gate electrodes LSL, WL and USL of the contract region CR. The supporters SP are formed between the interlayer dielectrics **110** spaced apart from each other, and penetrate the gate electrodes LSL, WL and USL between the interlayer dielectrics **110**.

[0076] The supporters SP of different lengths may be formed at each edge portion of the plate-shaped gate electrodes LSL, WL and USL of each layer. The lengths of the adjacent supporters SP may decrease with an increase in the distance from the memory cell region MR. The number of the gate electrodes LSL, WL and USL penetrating the supporters SP differs because the supporters SP are formed to different heights. Therefore, the supporters SP may penetrate all or some of the gate electrodes LSL, WL and USL. Also, the interface between the upper and lower gate electrodes may be formed between the adjacent supporters SP. Also, the supporters SP formed to different lengths in the contact region CR may be formed between the sidewalls of the vertically-adjacent gate electrodes gate electrodes LSL, WL and USL.

[0077] FIG. **10** is a plan view of a nonvolatile memory device according to a fifth exemplary embodiment of the inventive concept. FIG. **11** is a sectional view of the nonvolatile memory device according to the fifth exemplary embodiment of the inventive concept, which is taken along a line II-II of FIG. **10**.

[0078] Referring to FIGS. **10** and **11**, gate electrodes LSL, WL and USL are formed in a line shape, and active pillars PL penetrate the gate electrodes LSL, WL and USL of a memory cell region MR. Also, supporters SP of different lengths penetrate the gate electrodes LSL, WL and USL of a contact region CR. That is, the supporters SP are located at both end portions of the gate electrodes LSL, WL and USL. The supporters SP may be formed in plurality on the same line as the active pillars PL, and the supporters SP on the same line are spaced apart from each other. The supporters SP adjacent to the active pillars PL may penetrate all of the stacked gate electrodes LSL, WL and USL. Also, the number of the interlayer dielectrics **110** and the stacked gate electrodes LSL, WL and USL penetrated the supporters SP may decrease with an increase in the distance of the supporters SP from the memory cell region MR.

[0079] FIG. **12** is a plan view of a nonvolatile memory device according to a sixth exemplary embodiment of the inventive concept.

[0080] Referring to FIG. **12**, active pillars PL' may be formed across stacked gate electrodes LSL, WL and USL. A charge storage layer CS is formed between the active pillars PL' and the gate electrodes LSL, WL and USL. Also, as in the embodiment of FIGS. **6** and **7**, supporters SP of different lengths penetrate the gate electrodes LSL, WL and USL of a contact region CR.

[0081] Although it has been described in the first to sixth exemplary embodiments that the supporters SP formed at the gate electrodes LSL, WL and USL of the contact region CR are pillars formed of dielectric material, the supporters SP may have the same structure as the active pillars PL. That is, the supporters SP of the contact region CR may also be formed of semiconductor material, and the charge storage layer CS surrounding the supporters SP may be formed between the supporters SP and the gate electrodes LSL, WL and USL. In this embodiment, because the supporters SP of the contact region CR are not connected to the bit lines BL, they do not affect the operation of the nonvolatile memory device.

[0082] Hereinafter, methods for fabricating nonvolatile memory devices according to exemplary embodiments of the inventive concept will be described in detail.

[0083] A method for fabricating the nonvolatile memory devices according to the first and fourth exemplary embodiments of the inventive concept will be described below in detail with reference to FIGS. **13**A to **13**G.

[0084] FIGS. **13**A to **13**G are sectional views illustrating a method for fabricating the nonvolatile memory devices according to the first and fourth exemplary embodiments of the inventive concept. In the method for fabricating the nonvolatile memory devices according to the first and fourth exemplary embodiments, the planar structure will be described with reference to FIG. **2**A.

[0085] Referring to FIG. **13**A, interlayer dielectrics **110** and conductive layers **120** are alternately stacked on a semiconductor substrate **100**. The semiconductor substrate **100** includes a memory cell region MR and a contact region CR around the memory cell region MR. In the exemplary embodiments of the inventive concept, the memory cell region MR and the contact region CR are regions for gate electrodes. Also, the semiconductor substrate **100** may include an impurity region (or well) **102**, and the interlayer dielectrics **110** and the conductive layers **120** are formed over the semiconductor substrate **100**. The interlayer dielectrics **110** may be formed of silicon oxide, silicon oxynitride, or silicon nitride, and the conductive layers **120** may be formed of polysilicon. The number of the stacked conductive layers **120** may depend on the capacity of the nonvolatile memory device.

[0086] After the interlayer dielectrics **110** and the conductive layers **120** are stacked over the semiconductor substrate **100**, dummy holes for supporters **130** may be formed around a region for memory cells. For example, a photolithography process is performed on the stacked interlayer dielectrics **110** and conductive layers **120** to form dummy holes in the contact region CR. The dummy holes may penetrate the interlayer dielectrics **110** and the conductive layers **120** to expose the semiconductor substrate **100**.

[0087] The dummy holes may be formed around the memory cell region MR. Specifically, the dummy holes may be formed at the corner portions of the contact region CR as illustrated in FIG. **2**. The planar structure of the dummy holes formed at the corner portions of the contact region CR may vary as illustrated in FIGS. **2**A to **2**C.

[0088] Also, the dummy holes may be formed in plurality at each of the corner portions of the contact region CR as illustrated in FIG. **8**. The dummy holes increase in the distance

from the memory cell region MR. Also, the positions of the dummy holes may be the interface between upper and lower gate electrodes that will be formed through the subsequent process.

[0089] Referring to FIG. **13**B, the dummy holes are filled with dielectric material to form supporters **130**. The supporters **130** may be formed of the same material as the interlayer dielectrics **110**. Also, a dielectric layer **115** may be formed up to on the uppermost layer when the supporters **130** are formed. The formed supporters **130** penetrate the stacked interlayer dielectrics **120** and conductive layers **120** to contact the semiconductor substrate **100**.

[0090] Thereafter, a plate-shaped interlayer dielectric **110** and a conductive layer **120** are formed across the memory cell region MR and the contact region CR. That is, the stacked interlayer dielectrics **110** and conductive layers **120** may be patterned to form square-shaped gate electrodes across the memory cell region MR and the contact region CR. That is, the stacked interlayer dielectrics **110** and conductive layers **120** may be patterned to form a square-shaped stack structure in the memory cell region MR and the contact region CR of the semiconductor substrate **100**. In the exemplary embodiments of the inventive concept, the stack structure means a structure where the interlayer dielectrics **110** and the conductive layers **120** are alternately stacked. When the square-shaped stack structure is formed, the sidewalls of the stacked interlayer dielectrics **110** and conductive layers **120** may be exposed.

[0091] Alternatively, the forming of the square-shaped stack structure may be performed before the forming of the supporters **130**.

[0092] Referring to FIG. **13**C, an etchant having a high etch selectivity with respect to the conductive layers **120** is supplied to the sidewall of the square-shaped stack structure to remove portions of the conductive layers **120**. The etchant infiltrates from the edge to the center of the stack structure to selectively etch the conductive layers **120**. Because the supporters **130** are spaced apart from each other in the contact region CR, the conductive layers **120** may be removed up to the inside of the supporters **130**. That is, through a wet etch process, the conductive layers **120** may remain only in the memory cell region MR, and the interlayer dielectrics **110** and the supporters **130** penetrating the interlayer dielectrics **110** remain in the contact region CR. The conditions for the wet etch process, such as the supply time of the etchant, the concentration of the etchant and the supply rate of the etchant, may be controlled to remove the conductive layers **120** of the contact region CR. In this manner, after the wet etch process, the remaining conductive layers **122** may define the memory cell region MR of the gate electrodes.

[0093] During the removing of the conductive layers **120** of the contact region CR through the wet etch process, a capillary force may be generated at the interlayer dielectrics **110** due to the empty space between the interlayer dielectrics **110**. Accordingly, the upper and lower interlayer dielectrics **110** may tend to bond together. Therefore, when an etchant is continuously supplied between the interlayer dielectrics **110**, the interlayer dielectrics **110** may collapse. However, in the exemplary embodiments of the inventive concept, the supporters **130** of the contact region CR are formed perpendicularly to the interlayer dielectrics **110**, thus making it possible to prevent the upper and lower interlayer dielectrics **110** from collapsing or bonding together. That is, when the conductive layers **120** of the contact region CR are removed, the supporters **130** may serve to maintain the spacing distance between the stacked interlayer dielectrics **110**.

[0094] That is, during the removing of the conductive layers **120** of the contact region CR, the interlayer dielectrics **110**, which are parallel to the semiconductor substrate **100** and spaced apart from each other, and the supporters **130**, which are perpendicular to the semiconductor substrate **100**, remain in the contact region CR. That is, in the contact region CR, an empty space is formed between the interlayer dielectrics **110**, and the supporters **130** support the interlayer dielectrics **110** that are spaced apart from each other.

[0095] Referring to FIG. **13**D, a metal layer **140** is deposited on the entire surface of the stack structure from which the conductive layers **120** of the contact region CR have been removed. That is, the metal layer **140** may fill the space between the interlayer dielectrics **110** of the contact region CR, and may also be deposited on the top surface of the stack structure and the semiconductor substrate **100** around the stack structure. The metal layer **140**, filling the space between the interlayer dielectrics **110** of the contact region CR, may contact the conductive layers **120** of the memory cell region MR. The metal layer **140** may be formed of one of metal materials such as W, Al, Cu, Pt, Ru and Ir, conductive metal nitrides such as TiN, TaN and WN, conductive metal oxides such as RuO_2 and IrO_2, and a combination thereof.

[0096] Referring to FIG. **13**E, the metal layer **140** covering the stack structure is patterned to form stair-shaped metal layer patterns **142** in the contact region CR. When the metal layer **140** is formed also on the top surface of the stack structure, the uppermost metal layer **140** may be covered by a dielectric layer **150**. Accordingly, the areas of the metal layer patterns **142** may decrease with an increase in the distance from the semiconductor substrate **100**. That is, when the metal layer **140** is patterned in a stair shape, gate electrodes **122** and **142** may be formed to have a plate shape and decrease in area with an increase in the height from the semiconductor substrate **100**. Also, the gate electrodes **122** and **142** may have the memory cell region MR including the conductive layers **122**, and the contact region CR including the metal layers **142**.

[0097] When the metal layer patterns **142** are formed in the contact region CR, the metal layer **140** deposited on the uppermost dielectric layer **115** may be patterned in separate line patterns **144**. That is, line-shaped gate electrodes **144** may be formed on the uppermost dielectric layer **115**. In the memory cell region MR and the contact region CR, the uppermost gate electrodes **144** may comprise metal material. The line-shaped gate electrodes **144** formed on the stack structure are used as the upper select lines (USL**1**~USL**3** of FIG. **1**) in the exemplary embodiments of the inventive concept. Also, because the uppermost gate electrodes **144** are formed after the forming of the supporters **130**, the supporters **130** do not penetrate the uppermost gate electrodes **144**.

[0098] Also, as illustrated in FIG. **8**, when a plurality of the supporters SP are formed in the contact region CR, the supporters **130** adjacent to each other may also be etched in a stair shape during the forming of the stair-shaped metal layer patterns **142**.

[0099] Referring to FIG. **13**F, after the forming of the gate electrodes on the semiconductor substrate **100**, a dielectric layer **160** may be formed to fully cover the stacked gate electrodes. Active pillars **174** penetrating the stacked gate electrodes, and a charge storage layer **172** surrounding the active layers **174**, may be formed in the memory cell region

MR. Specifically, a plurality of channel holes are formed to penetrate the interlayer dielectrics **110** and the conductive layers **122** stacked in the memory cell region MR. The channel holes may be formed by forming a mask pattern (not illustrated) on the uppermost dielectric layer **150** and selectively and anisotropically etching the stacked interlayer dielectrics **110** and conductive layers **122** by means of the mask pattern. The formed channel holes may expose the impurity region **102** of the semiconductor substrate **100**. Also, the channel holes may be formed in a matrix configuration on the plane.

[0100] Thereafter, a charge storage layer **172** is deposited conformally along the surface of the channel holes. That is, the charge storage layer **172** may be formed on the sidewalls of the conductive layers **122** and the interlayer dielectrics **110** exposed by the channel holes. In an exemplary embodiment, the charge storage layer **172** may be formed by sequentially depositing a charge tunneling layer, a charge trapping layer, and a charge blocking layer. That is, an oxide layer, a nitride layer, and an oxide layer may be sequentially formed on the surface of the channel holes.

[0101] The channel holes including the charge storage layer **172** is filled with semiconductor material to form active pillars **174**. The filling of the channel holes with semiconductor material may include: performing an epitaxial process using the semiconductor substrate **100** as a seed layer; or depositing semiconductor material. The semiconductor material may be monocrystalline or polycrystalline semiconductor material. Thereafter, the semiconductor material filling the channel holes may be planarized to expose the top surface of the uppermost dielectric layer **150**.

[0102] Referring to FIG. **13**G, contacts (CT of FIG. **2**A) may be formed to be connected respectively to the gate electrodes **142** of the contact region CR. Because the gate electrodes **142** of the contact region CR are formed in a stair shape, the contacts may differ in length.

[0103] After the forming of the contacts, bit lines **180** are formed to be connected to the active pillars **174**. The bit lines **174** are formed across the uppermost gate electrodes **144**.

[0104] At the formation of the bit lines **180**, global word lines (GWL of FIG. **2**) connected to the gate electrodes **142** of each layer may be formed on the contacts.

[0105] A method for fabricating the nonvolatile memory devices according to the second and fifth exemplary embodiments of the inventive concept will be described in detail with reference to FIGS. **14**A to **14**F.

[0106] FIGS. **14**A to **14**F are sectional views illustrating a method for fabricating the nonvolatile memory devices according to the second and fifth exemplary embodiments of the inventive concept, which are taken along the line II-II of FIG. **10**.

[0107] Referring to FIG. **14**A, first and second dielectric layers **210** and **215** with different etch selectivity are alternately staked on a semiconductor substrate **200** including a memory cell region MR and a contact region CR. Specifically, the first and second dielectric layers **210** and **215** are formed of materials with different wet etch rates. For example, the first and second dielectric layers **210** and **215** may be formed of silicon oxide and silicon nitride, respectively.

[0108] Thereafter, active pillars **224** penetrating the first and second dielectric layers **210** and **215** and a charge storage layer **222** surrounding the active pillars **224** are formed in the memory cell region MR.

[0109] Specifically, a plurality of channel holes penetrating the stacked first and second dielectric layers **210** and **215** are formed in the memory cell region MR. The channel holes may be formed through a photolithography process. The channel holes may expose an impurity region **202** of the semiconductor substrate **200**, and may be formed in a matrix configuration on the plane in the memory cell region MR. Thereafter, a charge storage layer **222** is formed conformally along the surface of the channel holes, and the deposited charge storage layer is anisotropically etched to leave the charge storage layer **222** only on the sidewalls of the first and second dielectric layers **210** and **215** and expose the surface of the semiconductor substrate **200**. For example, the charge storage layer **222** may be formed by sequentially depositing a charge tunneling layer, a charge trapping layer, and a charge blocking layer. Thereafter, the channel holes are filled with semiconductor material to form active pillars **224**. The semiconductor material may be monocrystalline or polycrystalline semiconductor material. Also, the forming of the active pillars **224** may include: performing an epitaxial process using the semiconductor substrate **200** as a seed layer; or depositing semiconductor material. Thereafter, the semiconductor material filling the channel holes may be planarized to expose the top surface of the uppermost first dielectric layer **210**.

[0110] Referring to FIG. **14**B, supporters **230** penetrating the first and second dielectric layers **210** and **215** are formed in the contact region CR. More specifically, a plurality of dummy holes for supporters **230** are formed around the memory cell region MR. The dummy holes may expose the surface of the semiconductor substrate **200**. Thereafter, the dummy holes are filled with dielectric material, and the top portion is planarized to form pillar-shaped supporters **230**.

[0111] Specifically, the supporters **230** may be formed on the same line as the active pillars **224** of the memory cell region MR, and may be symmetrically formed with the memory cell region MR therebetween. That is, the supporters **230** may be formed in one-to-one correspondence with each of both sides of the memory cell region MR as illustrated in FIG. **5**, or may be formed in plurality at each of the both sides of the memory cell region MR as illustrated in FIG. **10**. A plurality of the supporters **230** formed at both sides of the memory cell region MR may be spaced apart from each other by a predetermined distance.

[0112] Referring to FIG. **14**C, the first and second dielectric layers **210** and **215** of the contact region CR, with the supporters **230** formed therein, are patterned in a stair shape.

[0113] The heights of the first and second dielectric layers **210** and **215** decrease toward the edge of the contact region CR. The supporters **230** of the contact region CR may also be etched simultaneously with the patterning of the first and second dielectric layers **210** and **215** in a stair shape. That is, the supporter adjacent to the memory cell region MR penetrates all of the first and second dielectric layers **210** and **215**, and the other supporters may be etched sequentially. Therefore, if a plurality of the supporters **230** are formed at both sides of the memory cell region MR, the lengths of the supporters **230** decrease toward the edge of the contact region CR.

[0114] On the other hand, if the supporters **230** are formed in one-to-one correspondence with each of both sides of the memory cell region MR, the supporters **230** are not etched during the patterning of the first and second dielectric layers

210 and **215** in a stair shape. That is, the supporters **230** may penetrate all of the first and second dielectric layers **210** and **215**.

[0115] After the patterning of the first and second dielectric layers **210** and **215** of the contact region CR in a stair shape, a dielectric layer **240** may be formed on the stair-shaped first and second dielectric layers **210** and **215**.

[0116] Thereafter, the first and second dielectric layers **210** and **215**, stacked in a plate shape across the memory cell region MR and the contact region CR, are patterned to form line-shaped stack structures. The patterning of the first and second dielectric layers **210** and **215** in a line shape may be performed before the forming of the active pillars **224** or the supporters **230**. The line-shaped stack structure may expose the sidewalls of the first and second dielectric layers **210** and **215**, and may include the aligned active pillars **224** and supporters **230**.

[0117] Referring to FIG. **14**D, the second dielectric layers **215** formed between the first dielectric layers **210** are removed. Specifically, an etchant having a high etch selectivity with respect to the second dielectric layers **215** may be supplied to the semiconductor substrate **200** with the line-shaped stack structures to remove the second dielectric layers **215**. Accordingly, an empty space is formed between the first dielectric layers **210**, and the first dielectric layers **210** spaced apart from each other may be supported by the supporters **230** of the contact region CR and the active pillars **224** of the memory cell region MR.

[0118] Referring to FIG. **14**E, the space between the first dielectric layers **210** may be filled with conductive material to form line-shaped gate electrodes **250**. Specifically, when conductive material is deposited between the first dielectric layers **210**, a conductive layer **250** surrounding the supporters **230** and the active pillars **224** may be formed between the first dielectric layers **210**. Thereafter, the conductive layer **250** filling the space between the adjacent line-shaped stack structures may be removed to form line-shaped gate electrodes **250**. The conductive material may be polysilicon or metal material.

[0119] Referring to FIG. **14**F, contact plugs **260**, connected respectively to the gate electrodes **250** of each layer, are formed in the contact region CR of the gate electrodes **250**. Because the gate electrodes **250** of the contact region CR are formed in a stair shape, the contact plugs **260** may differ in length.

[0120] Bit lines **270**, which are electrically connected to the active pillars **224** and intersect the gate electrodes **250**, are formed after the forming of the contact plugs **260**. Also, global word lines **275** may be formed on the contact plugs **260**.

[0121] Another method for fabricating the nonvolatile memory devices according to the second and fifth exemplary embodiments of the inventive concept will be described below with reference to FIGS. **15**A to **15**E.

[0122] FIGS. **15**A to **15**E are sectional views illustrating another method for fabricating the nonvolatile memory devices according to the second and fifth exemplary embodiments of the inventive concept, which are taken along the line II-II of FIG. **10**.

[0123] Referring to FIG. **15**A, first and second dielectric layers **210** and **215** with different etch selectivity are alternately stacked on a semiconductor substrate **200**, and a plate-shaped stack structure is formed across a memory cell region MR and a contact region CR. That is, the sidewalls of the stacked first and second dielectric layers **210** and **215** are aligned.

[0124] In the plate-shaped stack structure, the first and second dielectric layers **210** and **215** stacked on the contact region CR are patterned in a stair shape. That is, on the contact region CR, the stack height of the first and second dielectric layers **210** and **215** decreases toward the edge.

[0125] Thereafter, the plate-shaped stack structure is covered with a dielectric layer, and it is planarized to equalize the heights of the memory cell region MR and the contact region CR. That is, a dielectric layer **240** may be formed on the stair-shaped stack structure.

[0126] Referring to FIG. **15**B, active pillars **224***a* are formed in the memory cell region MR and supporters **224***b* are formed in the contact region CR.

[0127] More specifically, channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR. The channel holes and the dummy holes may be formed through a photolithography process, and the channel holes may be formed in a matrix configuration on the plane. Also, as illustrated in FIG. **5**, the dummy holes may be formed respectively at one side of the channel holes located at the edge of the memory cell region MR. Also, as illustrated in FIG. **10**, the dummy holes may be formed on the same line as the channel holes, and the dummy holes on the same line are spaced apart from each other. The dummy hole adjacent to the channel hole may penetrate all of the stacked first and second dielectric layers **210** and **215**. Also, the number of the penetrated first and second dielectric layers **210** and **215** may decrease with an increase in the distance from the memory cell region MR.

[0128] Thereafter, charge storage layers **222***a* and **222***b* are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars **224***a* and supporters **224***b*. That is, charge storage layers **222***a* and **222***b* may be formed around the supporters **224***b* of the contact region CR and the active pillars **224***a* of the memory cell region MR. Also, the active pillars **224***a* and the supporters **224***b* may be formed to the same length. The active pillars **224***a* of the memory cell region MR may penetrate all of the stacked first and second dielectric layers **210** and **215**, and the supporters **224***b* of the contact region CR may penetrate some of the stacked first and second dielectric layers **210** and **215**.

[0129] Referring to FIG. **15**C, the plate-shaped stack structure including the active pillars **224***a* and the supporters **224***b* are patterned to form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers **210** and **215** may be exposed. Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer **210** are supplied between the line-shaped stack structures to remove the second dielectric layers **215**. Accordingly, an empty space is formed between the first dielectric layers **210** that are perpendicular to the semiconductor substrate **200** and are spaced apart from each other. The first dielectric layers **210** spaced apart from each other may be supported by the active pillars **224***a* of the memory cell region MR, which are perpendicular to the semiconductor substrate **200**, and the supporters **224***b* of the contact region CR. That is, the second dielectric layers **215** can be prevented from collapsing or getting near to each other during the removing of the second dielectric layers **215** through a wet etch process.

[0130] Referring to FIG. **15**D, the space between the first dielectric layers **210** may be filled with conductive material to form line-shaped gate electrodes **250**. Specifically, when conductive material is deposited between the first dielectric layers **210**, conductive layers **250** may be formed around the active pillars **224***a* and the supporters **224***b*. Thereafter, the

conductive layer **250** filling the space between the adjacent line-shaped stack structures may be removed to form line-shaped gate electrodes **250** between the first dielectric layers **210**. The conductive material may be polysilicon or metal material.

[0131] Referring to FIG. **15**E, contact plugs **260**, connected respectively to the gate electrodes **250** of each layer, are formed in the contact region CR of the gate electrodes **250**.

[0132] Because the gate electrodes **250** of the contact region CR are formed in a stair shape, the contact plugs **260** may differ in length.

[0133] Bit lines **270**, which are electrically connected to the active pillars **224** and intersect the gate electrodes **250**, are formed after the forming of the contact plugs **260**. Also, global word lines **275** may be formed on the contact plugs **260**.

[0134] Because a conductive pattern such as the global word line **275** or the bit line **270** is not formed on the supporters **224***b*, it does not affect the operation of the nonvolatile memory device according to the exemplary embodiment of the inventive concept.

[0135] A method for fabricating the nonvolatile memory devices according to the third and sixth exemplary embodiments of the inventive concept will be described below with reference to FIGS. **16**A to **16**E.

[0136] With the exception of a method of forming the active pillars of the memory cell region, a method of forming the supporters of the contact region of the nonvolatile memory device according to the third and sixth exemplary embodiments may be identical to that of the second and fifth exemplary embodiments. Thus, the method of forming the active pillars of the memory cell region will be described in brief with reference to FIGS. **16**A to **16**E.

[0137] FIGS. **16**A to **16**E are sectional views illustrating a method for fabricating the nonvolatile memory devices according to the third and sixth exemplary embodiments of the inventive concept, which are taken along the lines A-A' and B-B' of FIG. **6**.

[0138] Referring to FIG. **16**A, first and second dielectric layers **210** and **215** with different etch selectivity are alternately stacked on a semiconductor substrate **200**. Line-shaped first trenches T**1** exposing the semiconductor substrate **200** are formed in the stacked first and second dielectric layers **210** and **215**. When the first trenches T**1** are formed, the first sidewalls of the stacked first and second dielectric layers **210** and **215** may be exposed.

[0139] Referring to FIG. **16**B, active pillars **224** are formed on the first sidewalls of the first and second dielectric layers **210** and **215** exposed by the first trenches T**1**. The active pillars **224** extend perpendicularly to the semiconductor substrate **200**. Also, a semiconductor layer is formed conformally along the surfaces of the first trenches, and the semiconductor layer is anisotropically etched. Accordingly, the active pillars **224** may be formed to face each other. After the forming of the active pillars **224**, the first trenches T**1** are filled with dielectric material and it is planarized to form a dielectric layer **225** between the semiconductor layers.

[0140] After the forming of the dielectric layer **225**, the semiconductor layer formed at the first sidewalls of the first and second dielectric layers **210** and **215** may be patterned. Accordingly, active pillars **224** spaced apart from each other may be formed on the first sidewalls of the first and second dielectric layers **210** and **215**.

[0141] Thereafter, supporters SP penetrating the first and second dielectric layers **210** and **215** are formed in the contact region CR. The formation position and method of the supporters SP are substantially identical to those of the second and fourth exemplary embodiments.

[0142] Referring to FIG. **16**C, line-shaped second trenches T**2** are formed at the stacked first and second dielectric layers **210** and **215** to expose the second sidewalls of the first and second dielectric layers **210** and **215**. The second trenches T**2** may be formed between the first trenches T**1** to form line-shaped stack structures. The line-shaped stack structure includes the supporters SP at the edge portion.

[0143] Referring to FIG. **16**D, through a wet etch process, the second dielectric layers **215** between the stacked first dielectric layers **210** are removed. Accordingly, second trenches T**2'** exposing the sidewalls of the active pillars **224** may be formed. The supporters SP on the contact region CR are formed of a material having an etch selectivity with respect to the second dielectric layer **215**, thus supporting the first dielectric layers **210** vertically spaced apart by a predetermined distance.

[0144] Referring to FIG. **16**E, a charge storage layer **245** and a gate electrode **250** are sequentially formed in the second trenches T**2'**. Thereafter, the charge storage layer and a gate conductive layer may be patterned to form the charge storage layer **245** and the gate electrode **250** on/under the first dielectric layers **210**. That is, the gate conductive layer in the second trench T**2'** may be separated into the line-shaped gate electrodes **250**. Thereafter, the space between the line-shaped gate electrodes **250** may be filled with a dielectric layer **255**. Thereafter, bit lines **270** connected electrically to the active pillars **224** may be formed on the stacked gate electrodes **250**.

[0145] FIG. **17** is a block diagram of a memory system including a nonvolatile memory device according to exemplary embodiments of the inventive concept.

[0146] Referring to FIG. **17**, a memory system **1100** may be applicable to PDAs, portable computers, Web tablets, wireless phones, mobile phones, digital music players, memory cards, or any device that can transmit and/or receive information in wireless environments.

[0147] The memory system **1100** includes a controller **1110**, an input/output device **1120** (e.g., a keypad, a keyboard, and a display), a memory **1130**, an interface **1140**, and a bus **1150**. The memory **1130** and the interface **1140** communicate with each other through the bus **1150**.

[0148] The controller **1110** includes at least one microprocessor, a digital signal processor, a microcontroller, or other similar processors. The memory **1130** may be used to store commands executed by the controller **1110**. The input/output device **1120** may receive data or signals from the outside of the memory system **1100**, or may output data or signals to the outside of the memory system **1100**. For example, the input/output device **1120** may include a keyboard unit, a keypad unit, or a display unit.

[0149] The memory **1130** includes the nonvolatile memory devices according to the embodiments of the inventive concept. The memory **1130** may further include random-access volatile memories and other various types of memories.

[0150] The interface **1140** serves to transmit/receive data to/from a communication network.

[0151] FIG. **18** is a block diagram of a memory card provided with a flash memory device according to an exemplary embodiment of the inventive concept.

[0152] Referring to FIG. **18**, a memory card **1200** is provided with a flash memory device **1210** according to the inventive concept to support high-capacity data storage capability. The memory card **1200** includes a memory controller **1220** that controls data exchange between a host and the flash memory device **1210**.

[0153] An SRAM **1221** is used as a working memory of a central processing unit (CPU) **1222**. A host interface (I/F) **1223** has data exchange protocol of a host connected to the memory card **1200**. An error correction block (ECC) **1224** detects and corrects an error in data read from the multi-bit flash memory device **1210**. A memory interface (I/F) **1225** interfaces with the flash memory device **1210**. The CPU **1222** performs an overall control operation for data exchange of the memory controller **1220**. Although not illustrated in FIG. **18**, it will be apparent to those skilled in the art that the memory card **1200** may further include a ROM storing code data for interfacing with the host.

[0154] FIG. **19** is a block diagram of an information processing system provided with a flash memory system according to the inventive concept.

[0155] Referring to FIG. **19**, an information processing system **1300**, such as a mobile device and a desktop computer, is provided with a flash memory system **1310** according to the inventive concept. The information processing system **1300** includes a flash memory system **1310**, a modem **1320**, a central processing unit (CPU) **1330**, a RAM **1340**, and a user interface **1350** that are electrically connected to a system bus **1360**. The flash memory system **1310** may have substantially the same configuration as the aforementioned memory system or flash memory system. Data processed by the CPU **1330** or external input data is stored in the flash memory system **1310**. The flash memory system **1310** may be configured with a semiconductor disk device (SSD). In this case, the information processing system **1300** can stably store high-capacity data in the flash memory system **1310**. Also, as the reliability of the semiconductor device is improved, the flash memory system **1310** can save resources consumed in error correction, thus providing a high-speed data exchange function to the information processing system **1300**. Although not illustrated in FIG. **19**, it will be apparent to those skilled in the art that the information processing system **1300** may further include an application chipset, a camera image processor (CIS), and an input/output device.

[0156] Also, the flash memory device or the memory system according to the inventive concept may be mounted in various types of packages. Examples of the packages of the flash memory device or the memory system according to the inventive concept include

[0157] Package on Package (PoP), Ball Grid Arrays (BGAs), Chip Scale Packages (CSPs), Plastic Leaded Chip Carrier (PLCC), Plastic Dual In-line Package (PDIP), Die in Waffle Pack, Die in Wafer Form, Chip On Board (COB), Ceramic Dual In-line Package (CERDIP), Plastic Metric Quad Flat Pack (MQFP), Thin Quad Flat Pack (TQFP), Small Outline Integrated Circuit (SOIC), Shrink Small Outline Package (SSOP), Thin Small Outline Package (TSOP), Thin

[0158] Quad Flat Pack (TQFP), System In Package (SIP), Multi Chip Package (MCP), Wafer-level Fabricated Package (WFP), and Wafer-level Processed Stack Package (WSP).

[0159] As described above, according to the three-dimensional nonvolatile memory device of the inventive concept, the supporters are formed in the contact region, thereby making it possible to support the edge portions of the stacked gate electrodes. Also, when the wet etch process is performed for fabrication of the three-dimensional nonvolatile memory device, the interlayer dielectrics can be prevented from collapsing during the wet etch process.

[0160] Also, some or all of the three-dimensional stacked gate electrodes are comprised of metal material, thereby making it possible to reduce the resistance of the gate electrode. Therefore, the operation speed of the three-dimensional nonvolatile memory device can be improved.

[0161] Also, according to the method for fabricating the three-dimensional nonvolatile memory device of the inventive concept, the horizontal supporters are formed across the top surfaces of the line-type stack structures in order to form the three-dimensional conductive lines. Accordingly, the top surfaces of the high line-type stack structures can be fixed by the horizontal supporters. Therefore, the line-type stack structure can be prevented from collapsing when forming the openings between the stacked first dielectric layers.

[0162] Also, the vertical supporters penetrating the stacked dielectric layers are formed at the edge portions of the line-type stack structure, thereby making it possible to prevent the first dielectric layers from collapsing when forming the openings between the stacked first dielectric layers.

[0163] The above-disclosed subject matter is to be considered illustrative and not restrictive, and the appended claims are intended to cover all such modifications, enhancements, and other embodiments, which fall within the true spirit and scope of the inventive concept. Thus, to the maximum extent allowed by law, the scope of the inventive concept is to be determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.

1. A nonvolatile memory device comprising:

a semiconductor substrate including a memory cell region and a contact region;

a plurality of active pillars extending in the memory cell region perpendicular to the semiconductor substrate; and

a plurality of gate electrodes including a first gate electrode disposed on the memory cell region to intersect the active pillars and a second gate electrode disposed on the contact region, connected to the first gate electrode and comprising metal material.

2. The nonvolatile memory device of claim **1**, further comprising a plurality of supporters extending in the contact region perpendicular to the semiconductor substrate to penetrate the gate electrodes.

3. The nonvolatile memory device of claim **1**, wherein the first gate electrode of the memory cell region is comprised of metal material.

4. The nonvolatile memory device of claim **1**, wherein

the gate electrodes are stacked on the semiconductor substrate, with an interlayer dielectric therebetween; and

an edge portion of the second gate electrode included in a lower gate electrode among the gate electrodes is exposed by the second gate electrode included in an upper gate electrode which is disposed on the lower gate electrode.

5. The nonvolatile memory device of claim **1**, further comprising contact plugs connected respectively to the second gate electrodes of the contact region.

6-10. (canceled)

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