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8 *Micron Consumer Products Group LLC*

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10 UNITED STATES DISTRICT COURT
11 NORTHERN DISTRICT OF CALIFORNIA
12 SAN FRANCISCO DIVISION

13 YANGTZE MEMORY TECHNOLOGIES
14 COMPANY, LTD.,

15 Plaintiff,

16 v.

17 MICRON TECHNOLOGY, INC., et al.,

18 Defendants.

19

20

21

22 MICRON TECHNOLOGY, INC.,

23 Counterclaim Plaintiff,

24

25 v.

26 YANGTZE MEMORY TECHNOLOGIES
COMPANY, LTD., and YANGTZE
MEMORY TECHNOLOGIES, INC.,

27

Counterclaim Defendants.

28

Case No. 3:23-cv-05792-RFL

**COUNTERCLAIM PLAINTIFF
MICRON TECHNOLOGY'S
DISCLOSURE OF ASSERTED CLAIMS
AND INFRINGEMENT
CONTENTIONS AND DOCUMENT
PRODUCTION ACCOMPANYING
DISCLOSURE (PATENT LOCAL
RULES 3-1 AND 3-2)**

Honorable Rita F. Lin

1 Pursuant to Patent Local Rules 3-1 and 3-2, Counterclaim Plaintiff Micron Technology, Inc.
2 (“MTI”) hereby submits this Disclosure of Asserted Claims and Infringement Contentions for U.S.
3 Patent Nos. 10,475,737 (the “’737 patent”), 8,945,996 (the “’996 patent”), 8,803,214 (the “’214
4 patent”), 10,872,903 (the “’903 patent”), and 10,373,974 (the “’974 patent”) (collectively, the
5 “Asserted Patents”) asserted against counterclaim defendants Yangtze Memory Technologies
6 Company, Ltd. (“YMTCL”), and Yangtze Memory Technologies, Inc. (“YMTI”) (collectively
7 “YMTC”).

8 MTI bases these contentions on its current knowledge, understanding, and belief as to the
9 facts and information available as of the date of these contentions. MTI has not yet completed its
10 investigation, collection of information, discovery, or analysis relating to this action, and additional
11 discovery, including discovery from YMTC and third parties, may lead MTI to further amend,
12 revise, and/or supplement these contentions. Indeed, the accused functionalities relate to
13 microscopic features, and the precise designs and fabrications methods thereof are held secret, at
14 least in part, and are not publicly available in their entirety. As such, an analysis of non-publicly-
15 available documentation and source code, including that of YMTC and/or third-parties may be
16 necessary to fully and accurately describe every infringing functionality.

17 However, merits discovery in this action has barely begun and, as of the date of service of
18 these contentions, is not scheduled to close until March 8, 2025. To date, YMTC has not produced
19 documents responsive to MTI’s outstanding document requests, no depositions have been taken,
20 and there has been no third-party discovery.

21 For at least these reasons, MTI specifically reserves the right to amend, revise and/or
22 supplement these contentions and/or accompanying exhibits in accordance with any orders in this
23 matter, Patent L.R. 3-6, and Federal Rule of Civil Procedure 26(e), as additional documents and
24 information become available and as discovery and investigation proceed. MTI also reserves the
25 right to supplement, modify, or amend these contentions to include additional products or services
26 made, used, sold, or offered for sale in or imported into the United States by YMTC. The
27 information in these contentions is not an admission regarding the scope of any claims or the proper
28 construction of those claims or any terms contained therein, and MTI further reserves the right to

1 revise and/or supplement these contentions to address any claim constructions advanced as the case
2 proceeds.

3 **I. Disclosure of Asserted Claims and Infringement Contentions**

4 **A. Identification of Accused Products Pursuant to Patent L.R. 3-1(b)**

5 Based on the information currently in its possession, MTI contends that the following
6 YMTC products (and methods of making such products) (individually, “**Accused Product**” or
7 collectively, “**Accused Products**”) infringe the Asserted Patents:

8 YMTC’s 64-layer 3D NAND storage technologies and products containing the same
9 (collectively, the “YMTC 64L Accused Products”), including the X1-9050 and X2-9060, any
10 YMTC 64-layer 3D NAND product, and other memory chips (and memory products containing
11 the same) that have the same or similar structures, features, or functionalities, and/or are made by
12 the same or similar Xtacking® technology manufacturing processes as the aforementioned
13 exemplary products.

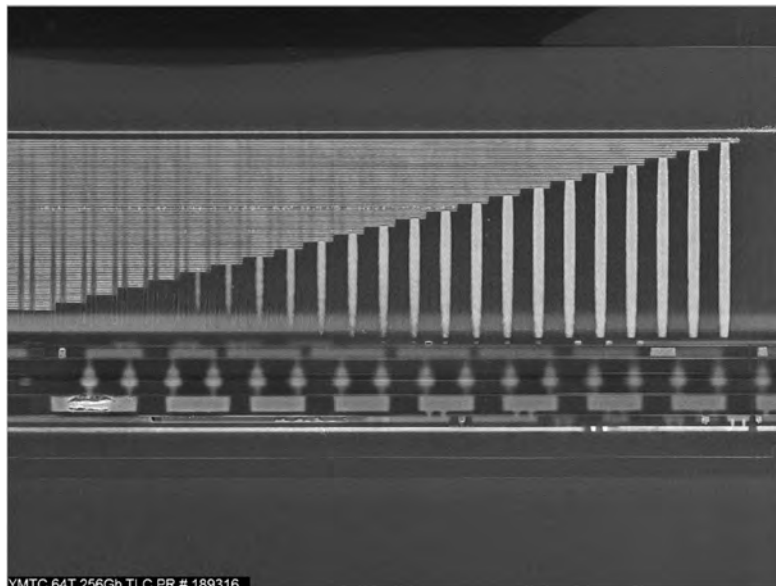
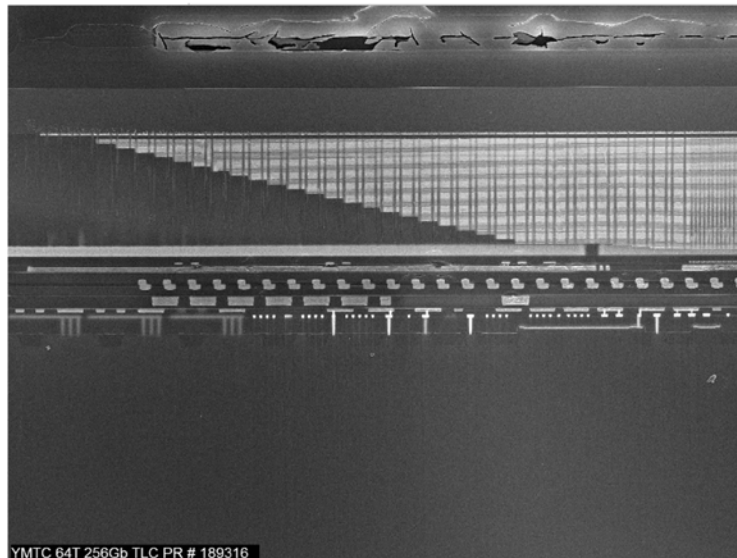
14 YMTC’s 128-layer 3D NAND storage technologies and products containing the same
15 (collectively, the “YMTC 128L Accused Products”), including the X2-6070, any YMTC 128-
16 layer 3D NAND product, and other memory chips (and memory products containing the same)
17 that have the same or similar structures, features, or functionalities, and/or are made by the same
18 or similar Xtacking® technology manufacturing processes as the aforementioned exemplary
19 product.

20 YMTC’s 232-layer 3D NAND storage technologies and products containing the same
21 (collectively, the “YMTC 232L Accused Products”), including the X3-9060, X3-9070, and X3-
22 6070, any YMTC 232-layer 3D NAND product, and other memory chips (and memory products
23 containing the same) that have the same or similar structures, features, or functionalities, and/or
24 are made by the same or similar Xtacking® technology manufacturing processes as the
25 aforementioned exemplary product.

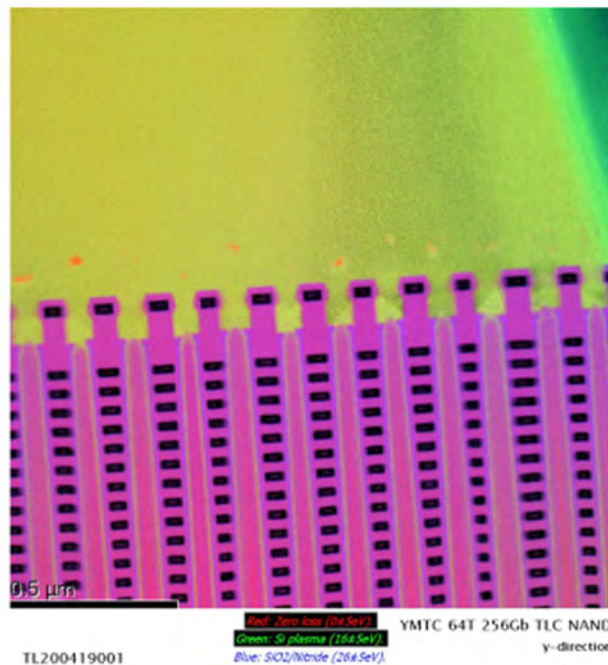
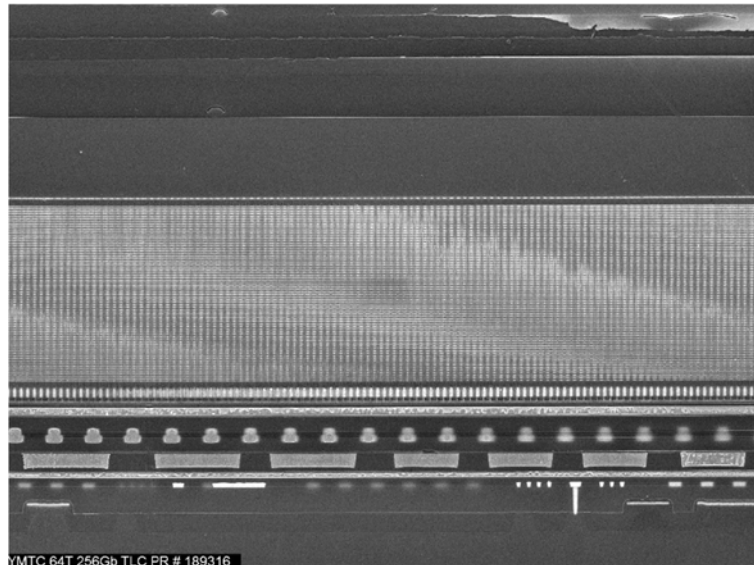
26 Upon information and belief, each of the YMTC 64L Accused Products, YMTC 128L
27 Accused Products, and YMTC 232L Accused Products have the same or similar structures,
28 features, or functionalities, and/or are made by the same or similar manufacturing processes

1 insofar as the structures, features, functionalities, and/or manufacturing processes of the Accused
2 Products relate to the MTI Asserted Patents. Claim charts mapping a YMTC 1T 232L TLC
3 product to the Asserted Claims of the Asserted Patents are provided as exhibits A-1, B-1, C-1,
4 and E-1, and claim charts mapping the YMTC 512G 128L TLC product to the Asserted Claims of
5 the Asserted Patents is provided as exhibits A-2, B-2, C-2, D-2, and E-2.

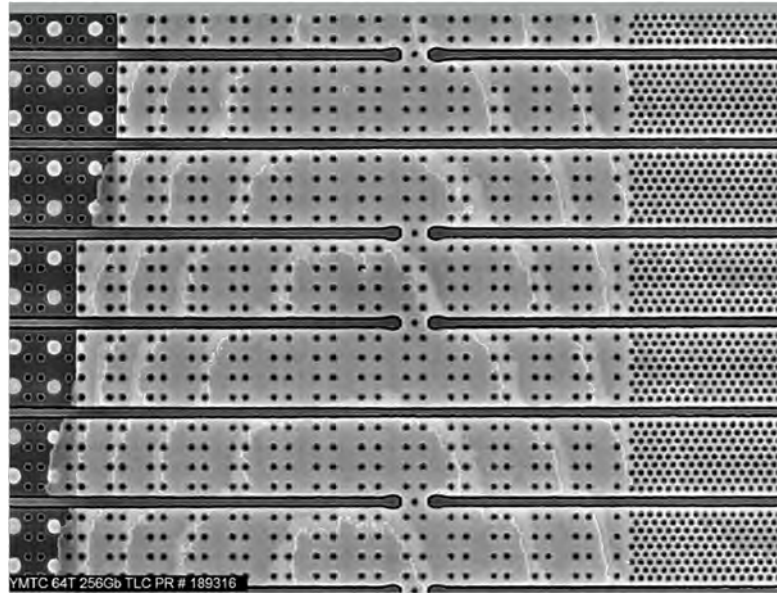
6 The YMTC 128L is representative of the YMTC 64L for the purposes of the Asserted
7 patents. For example, the YMTC 256G 64L TLC product contains staircase regions with contacts
8 and dummy structures that extend through word lines of the memory array structure in the same
9 way as in the YMTC 512G 128L TLC product as shown in the images below:



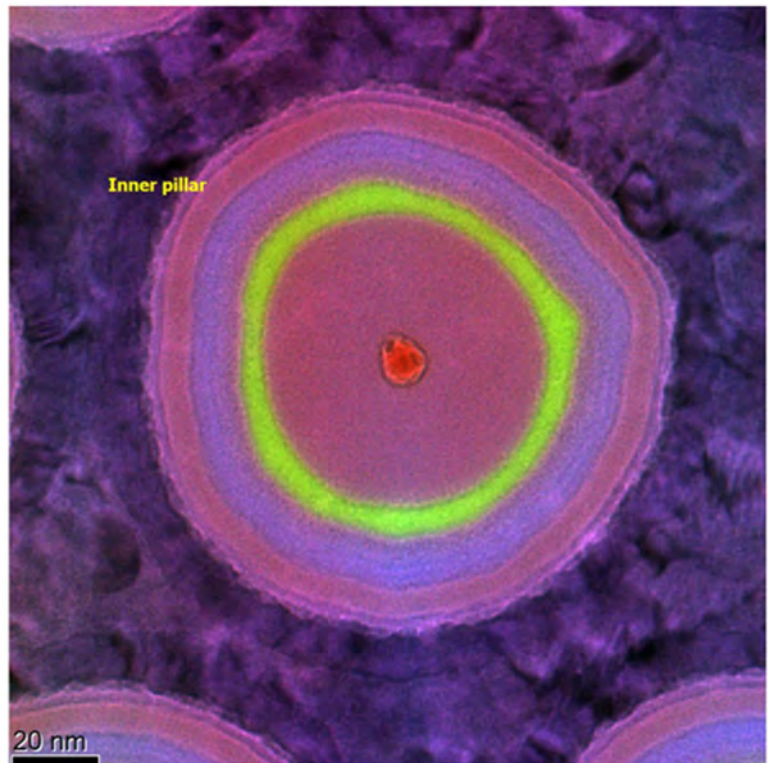
Further, the YMTC 256G 64L TLC product contains a memory storage array portion that is configured in the same way as the memory storage array portion of the YMTC 512G 128L TLC product:



Further, the staircase contact regions, select gate regions, and array regions in the YMTC 256G 64L TLC product are configured the same way as they are in the YMTC 512G 128L TLC product. For example, both have elongated slots that extend from the array portion to the staircase portion and that are used to remove sacrificial material prior to forming word lines:



Lastly, the cell structure of the memory cells in the YMTC 256G 64L TLC product is identical, at least for the purposes of the Asserted Patents, to the cell structure of the memory cells in the YMTC 512G 128L TLC product:



TL200419001
 Red: Zero loss ($0 \pm 5\text{eV}$)
 Green: Si plasma ($16 \pm 5\text{eV}$)
 Blue: SiO₂/Nitride ($26 \pm 5\text{eV}$)
 YMTC 64T 256Gb TLC NAND
 planar, middle of pillar

Further, some product lines such as the YMTC 232L may include products that use, for example, triple level cells (TLC) or quad level cells (QLC); however, for the purpose of the Asserted Patents, such differences are immaterial.

B. Identification of Asserted Claims Pursuant to Patent L.R. 3-1(a)

Based on the information currently in its possession, MTI contends that YMTC infringes the following claims (collectively, the “Asserted Claims”). MTI expressly reserves the right to amend and/or supplement its identification of Asserted Claims should discovery (including YMTC’s technical documentation, source code, and witnesses) reveal additional, relevant information.

U.S. Patent No.	Asserted Claims
10,475,737	1-7, 9, 10-12, 14, 15, 18, 20, 21, and 22
8,945,996	1-4, 6-10, 12, 13, 16, 17, 18, 22-26, 28, 30, and 32
8,803,214	1-12 and 14-20
10,872,903	1-3, 5, 7-9, and 17-20
10,373,974	1, 4, 5, 7, 9, and 11-19

i. Direct Infringement Under 35 U.S.C. § 271(a) & § 271(g)

MTI contends that YMTCL and YMTI have directly infringed, and continue to directly infringe, the Asserted Claims of the Asserted Patents, both individually and as a single enterprise, and literally or under the doctrine of equivalents, at least by offering to sell, selling, using, and/or importing into the United States the YMTC 64L Accused Products and the 128L Accused Products.

MTI contends that YMTCL and YMTI have directly infringed, and continue to directly infringe, the Asserted Claims of the ’717, ’996, ’214, and ’974 Patents, both individually and as a single enterprise, and literally or under the doctrine of equivalents, at least by offering to sell, selling, using, and/or importing into the United States the YMTC 232L Accused Products.

Further, MTI contend that the ’996 Patent and ’974 Patent are directly infringed, both individually and as a single enterprise, and literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least because the Accused Products are made overseas by a process covered by

1 the Asserted Claims of the Asserted Patents and are offered for sale, sold, and/or imported into
2 the United States.

3 In addition to the detailed claims charts demonstrating YMTC's infringement attached as
4 exhibits A-1 through C-1 and E-1, and A-2 through E-2, at least the following facts support
5 YMTC's direct infringement of the Asserted Patents:

6 **Sale or Importation in the U.S.:** On May 22, 2020, YMTCL declared to the USPTO that
7 it sold or transported 3D NAND chips in commerce regulated by U.S. Congress since at least as
8 early as September 9, 2016. Counterclaims¹, Ex. 36 at 4; 15 U.S.C. § 1127 (defining "use in
9 commerce" as when "the goods are sold or transported in commerce" and "commerce" as "all
10 commerce which may lawfully be regulated by Congress"); Trademark Manual of Examining
11 Procedure § 901.03 ("Use of a mark in a foreign country does not give rise to rights in the United
12 States if the goods or services are not sold or rendered in the United States."). Specifically, in
13 connection with YMTCL's trademark filing for its YMTC mark, YMTCL declared under penalty
14 of perjury that "the mark is in use in commerce on or in connection with all the goods/services in
15 the application" and that "[t]he specimen(s) shows the mark as used on in connection with the
16 goods ... in commerce." Counterclaims, Ex. 36 at 6. YMTCL attached specimens showing its
17 Xtacking® chips (Counterclaims, Ex. 6 at 8-9), which are 3D NAND memory chips that Micron
18 accuses of infringement (*id.*, Ex. 37 at 2). Thus for these reasons, MTI, on information and
19 belief, contends that YMTC has sold, offered for sale, or imported 3D NAND memory chips in
20 the U.S. or between the U.S. and a foreign nation (*i.e.* imported from China).²

21 **Sales in California:** Mr. David Duffin identifies himself as "US General Manager and
22 Head of International Customer Sales at Yangtze Memory Technologies," in Santa Clara and San
23 Jose, California, since March 2019. Counterclaims ¶¶ 24-26, Ex. 31 at 2. In his description of
24 that role, he states that he is "responsible for \$5B+ in shipments per year" and that he is "used to
25 regularly and directly interacting with customers," among other things. *Id.* Although he does not

26 ¹ "Counterclaims" as used herein refers to Defendants' Answer to First Amended Complaint and
27 Counterclaims (Dkt. 35).

28 ² Micron did not allege that YMTC makes the accused products in the U.S. Thus, it is plausible
to infer that acts of transportation in the U.S. must begin with an infringing importation.

1 specify which YMTC entity is his current employer, he states that at least from 2016-2019, he
2 worked for “Yangtze Memory Technologies Co.” (*i.e.* YMTCL), which is the Chinese parent
3 company of YMTI. *Id.* And YMTI identifies Mr. Duffin as its Chief Executive Officer and
4 Secretary in its California Secretary of State filings. *Id.*, Ex. 32 at 2. It is proper to infer that he
5 holds a role with both YMTC entities. Thus, YMTC’s Head of International Customer Sales,
6 responsible for billions of dollars of shipments and customer interaction, operates in this District.
7 Therefore, MTI contends, on information and belief, that YMTC sells, offers for sale, and
8 provides customer support for accused products in the U.S. *Id.* ¶¶ 16-18.

9 **Use and Importation in California:** Mr. Duffin states that he worked at YMTCL as
10 “Vice President Product & Test Engineering” from May 2016 to March 2019. Counterclaims,
11 Ex. 31 at 2-3. He led “all product, test and assembly engineering for YMTC” in San Jose,
12 California. Based on this description, it is reasonable to infer that YMTC has imported products
13 into the U.S. for testing and used those products (e.g., tested them) in the U.S. Thus, on
14 information and belief, MTI has concluded that the Accused Products are used and imported into
15 the United States.

16 **YMTC Launched and Showed Accused Products in California:** “In August 2018,
17 YMTC officially launched its ground-breaking Xtacking® architecture at the Flash Memory
18 Summit, and won the ‘Best of Show’ award” in Santa Clara, California. Counterclaims Ex. 37 at
19 7; Ex. 25 at 4 (“In 2018, [CEO Simon Yang] showed off the company’s technology at the Flash
20 Memory Summit in California.”); *see also* Dkt. 29 (“YMTCL’s FAC”) ¶¶ 7, 25, Exs. 38, 39.
21 Based on these representations regarding product launch, trade show attendance, and technology
22 demonstration, MTI believes that YMTC has imported and used the Accused Products to solicit
23 customers in the U.S.

24 **YMTC Participates in a Global Market of 3D NAND Sales:** YMTC participates in the
25 global 3D NAND market, which includes the U.S.:

- 26 • In YMTCL’s own Complaint, “YMTC admits that it is ‘dedicated to the development of
27 memory products for the *global market*’ and that it ‘*maintains ties to Silicon Valley*
28 through a wholly-owned subsidiary, Yangtze Memory Technologies, Inc.’” Counterclaims

¶ 29 (emphasis added); YMTCL’s FAC ¶¶ 8, 24, Ex. 36 (YMTC’s office in Santa Clara, California is one of its “Globalized R&D System and Market Locations”).

- “YMTC has become the world’s sixth-biggest maker of NAND flash memory by output, with about **5% of the global market[,]**” as of 2021. Counterclaims, Ex. 25 at 4.
- “CEO [Simon Yang] worked to bring **YMTC to the global stage.**” *Id.*, Ex. 25 at 4.
- “Yangtze Memory Technologies” Deputy General Counsel and Head of IP Department, Daniel (Tuenlap) Chan sits in Richardson, Texas, from where he helps “navigate through complex issues for advancing **YMTC’s competitive position in the global memory supply chain.**” *Id.*, Ex. 35 at 2. Mr. Chan stated that YMTC’s “patent portfolio is designed to protect our innovations in **markets that matter to YMTC** and its partners.” *Id.* ¶ 29, Ex. 34 at 3. In suing Micron in California, YMTC “allege[s] that its **rival** was using its patented innovations to **force YMTC out of the 3D NAND flash memory market.**” *Id.*

Based on these representations about YMTC’s position in the global market, MTI believes that YMTC sells, offers for sale, and uses the Accused Products in, and imports the Accused Products into, the U.S.

ii. Induced Infringement Under 35 U.S.C. § 271(b)

MTI contends that each Accused Product infringes each Asserted Claim of the Asserted Patents, and that YMTC has actively, knowingly, and intentionally induced (and continues to actively, knowingly, and intentionally induce) others to directly infringe the Asserted Claims in various ways, at least by selling and importing devices containing the Accused Products in violation of 35 U.S.C. § 271(b). MTI incorporates its discussion of YMTC’s U.S. activities in Section I(B)(i) above. In addition to those facts, the following facts further support that YMTC has actively, knowingly, and intentionally induced (and continues to actively, knowingly, and intentionally induce) others to directly infringe the Asserted Claims:

1 **Lexar Products Containing the Accused Products Are Available in the U.S.:** Before
2 filing its Counterclaims, Micron purchased Lexar solid state memory devices that contain the
3 YMTC accused products and shipped them to counsel's offices in this District. Counterclaims,
4 Ex. 28-30. Micron attached to the Counterclaims multiple articles demonstrating that the Lexar
5 products contain YMTC accused products. *Id.* Thus, MTI is informed and believes that Lexar is
6 a customer of YMTC and that products containing YMTC's accused products are sold and
7 imported into the U.S. *Id.*

8 **YMTC's Website and Customer Support in the U.S.:** MTI is informed and believes
9 that the YMTC Entities actively encourage others, such as their customers and distributors, to
10 make, use, offer to sell, import, supply, or otherwise distribute into the United States the Accused
11 Products and products containing the Accused Products. Counterclaims ¶ 22. YMTC describes
12 the applications for which the accused products can be used, which include "enterprise servers,
13 data centers, and other fields to meet the diversified needs for data storage in the era of 5G and
14 AI," and provides product specifications on the YMTC website, which is accessible in the U.S.
15 (*id.*, Ex. 38); provides instructions and encouragement for such use (*id.* ¶ 22); designs its products
16 to comply with U.S. safety standards (*id.* ¶ 23); and provides such materials in the English
17 language (*id.*, Ex. 38). Based on this, the Court can infer that YMTC's intended audience
18 includes U.S. customers or potential customers. Indeed, YMTC's website identifies its office in
19 Santa Clara, California as one of its "Globalized R&D System *and Market Locations.*"
20 YMTCL's FAC ¶¶ 8, 24, Ex. 36 (emphasis added). And YMTC's "US General Manager and
21 Head of International Customer Sales" is located in California as discussed in greater detail
22 above.

23 YMTCL and YMTI have had knowledge of their infringement at least since the filing of
24 the MTI's Counterclaims.

25 **C. Infringement Claim Charts Pursuant to Patent L.R. 3-1(c)**

26 Based on the information currently in its possession, MTI contends that the following
27 claim charts specify where each limitation of each Asserted Claim is found within each Accused
28 Instrumentality (whether literally or under the Doctrine of Equivalents):

1 Exhibit A-1 & A-2: Infringement of '737 Patent

2 Exhibit B-1 & B-2: Infringement of '996 Patent

3 Exhibit C-1 & C-2: Infringement of '214 Patent

4 Exhibit D-2: Infringement of '903 Patent

5 Exhibit E-1 & E-2: Infringement of '974 Patent

6 YMTC has not provided MTI with full discovery regarding its products, including non-
7 public documentation describing the Accused Instrumentalities, detailed written discovery
8 responses, or testimony from YMTC's witnesses. Thus, MTI expressly reserves its right to amend
9 and/or supplement these assertions or to asserted additional claims for infringement under Patent
10 L.R. 3-6 as discovery in this case progresses or as otherwise permitted by the Court.

11 **D. Identification of Indirect Infringement Pursuant to Patent L.R. 3-1(d)**

12 Based on the information currently in its possession, MTI contends that YMTC is liable
13 for indirect infringement of each of the Asserted Claims under 35 U.S.C. §§ 271(b). MTI has
14 identified the acts of direct infringement and provided a description of YMTC's own acts that
15 induce such direct infringement above (§ I(B)(i) & (ii)), as well as in MTI's Answer and
16 Counterclaims (Dkt. No. 35), which are incorporated by reference in their entirety.

17 **E. Identification of Types of Infringement Pursuant to Patent L.R. 3-1(e)**

18 Based on the information currently in its possession, MTI contends that the Accused
19 Products satisfy each limitation of each Asserted Claim both literally and under the doctrine of
20 equivalents.

21 **F. Identification of Priority Dates Pursuant to Patent L.R. 3-1(f)**

22 With respect to claiming priority to an earlier application, MTI contends that: (a) each
23 Asserted Claim of the '737 Patent is entitled to a priority date no later than April 12, 2011; (b)
24 each Asserted Claim of the '966 Patent is entitled to a priority date no later than April 12, 2011;
25 (c) each Asserted Claim of the '214 Patent is entitled to a priority date no later than June 28,
26 2010; (d) each Asserted Claim of the '903 Patent is entitled to a priority date no later than June
27 28, 2010; (e) each Asserted Claim of the '974 Patent is entitled to a priority date no later than
28 Nov. 16, 2015.

1 **G. Identification of Practicing Instrumentalities Pursuant to Patent L.R. 3-1(g)**

2 Pursuant to L.R. 3-1(g), MTI states that MTI's 130 series and beyond practice one or
3 more claims of the '996 patent.

4 MTI states that MTI's 130 series and beyond practice one or more claims of the '737
5 patent.

6 MTI states that MTI's 110 series and beyond practice one or more claims of the '214
7 patent.

8 MTI states that MTI's 130 series and beyond practice one or more claims of the '974
9 patent.

10 The parties have been conferring about a protective order for this case that takes into
11 account the fact that YMTC is a listed entity on the U.S. Department of Commerce Entity List.
12 Once an appropriate protective order is in place, MTI will supplement its disclosure to identify
13 particular claims, which will necessarily disclose technical information about the structure or
14 fabrication of Micron's products. Micron sent YMTC a final proposal on May 2, 2024 and
15 indicated that it was prepared to submit the parties' protective order proposal and remaining
16 disputed issues to the Court. Micron is awaiting a further response from YMTC.

17 **H. Identification of First Infringement and Damages Period Pursuant to Patent**
18 **L.R. 3-1(h)**

19 Based on the information currently in its possession, MTI contends that YMTC's
20 infringement of the Asserted Patents began at least as early as the dates set forth below. To MTI's
21 knowledge, YMTC's infringement remains ongoing and the damages period likewise remains
22 ongoing.

U.S. Patent No.	Date of First Infringement & Start of Damages Period
10,475,737	At least as early as November 2019
8,945,996	At least as early as 2018
8,803,214	At least as early as 2018
10,872,903	At least as early as December 2020
10,373,974	At least as early as August 2019

27 Discovery is ongoing and MTI has sought technical and sales information from YMTC

1 regarding the Accused Products, as that information is in YMTC's possession, custody, or
2 control. As of service of this document, MTI has not received substantive responses to its
3 discovery requests from YMTC. MTI reserves the right to supplement its Infringement
4 Contentions based on YMTC's discovery responses, and other documents and information
5 produced in discovery. MTI further reserves its right to amend and/or modify its Infringement
6 Contentions as discovery in this case progresses, under Patent L.R. 3-6, or as the Court otherwise
7 permits.

8 **I. Identification of Willful Infringement Bases Pursuant to Patent L.R. 3-1(i)**

9 MTI contends that YMTC has willfully infringed each Asserted Claim of each Asserted
10 Patent at least since the filing of the counterclaims in this action. Since at least the filing of
11 MTI's Counterclaims, which identified the Asserted Patents and attached detailed charts
12 demonstrating infringement, YMTC has been on notice of MTI's patents and claims of
13 infringement. Moreover, YMTC had knowledge of Micron's 3D NAND patents from the large
14 number of YMTC 3D NAND engineers who previously worked on 3D NAND development at
15 Micron among other facts. Counterclaims ¶¶ 31, 32, 39, 50, 60, 70, 80. Thus, MTI expects that
16 discovery will reveal that YMTC knew of the Asserted Patents and YMTC's unauthorized use
17 thereof before filing of the Counterclaims. YMTC's infringement remains ongoing.

18 Moreover, discovery that YMTC has not yet produced may provide additional evidence
19 which shows that YMTC has willfully infringed the Asserted Patents. MTI therefore reserves its
20 right to amend and/or modify its willful infringement contentions as discovery in this case
21 progresses, under Patent L.R. 3-6, or as the Court otherwise permits.

22 **II. Document Production & Accompanying Disclosure**

23 **A. Documents Pursuant to Patent L.R. 3-2(a)**

24 MTI is not currently aware of any documents responsive to Patent L.R. 3-2(a). MTI's
25 discovery and investigation are ongoing.

26 **B. Documents Pursuant to Patent L.R. 3-2(b)**

27 The parties have been conferring about a protective order for this case that takes into
28 account the fact that YMTC is a listed entity on the U.S. Department of Commerce Entity List.

1 Once an appropriate protective order is in place, MTI will supplement its document production
2 with excerpts of technical lab notebooks. Micron sent YMTC a final proposal on May 2, 2024,
3 and indicated that it was prepared to submit the parties' protective order proposal and remaining
4 disputed issues to the Court. Micron is awaiting a further response from YMTC.

5 **C. Documents Pursuant to Patent L.R. 3-2(c)**

6 Pursuant to Patent L.R. 3-2(c), MTI has produced documents bearing production numbers
7 MYM0000048 - MYM0000429; MYM0004678 - MYM0004915; MYM0004943 -
8 MYM0005111; MYM0005714 - MYM0005899; and MYM0006291 - MYM0006448; *see*
9 *generally* MYM0000001 - MYM0006448.

10 **D. Documents Pursuant to Patent L.R. 3-2(d)**

11 Pursuant to Patent L.R. 3-2(d), MTI has produced documents bearing production numbers
12 MYM0006449 - MYM0020687.

13 **E. Documents Pursuant to Patent L.R. 3-2(e)**

14 As noted above, the parties have been conferring about a protective order for this case that
15 takes into account the fact that YMTC is a listed entity on the U.S. Department of Commerce
16 Entity List. Once an appropriate protective order is in place, MTI will supplement its technical
17 document production. MTI will also make available for inspection MTI source code materials
18 that demonstrates the structure and fabrication of the MTI products identified above pursuant to
19 L.R. 3-1(g) pursuant to the source code inspection procedures that the parties are negotiating in
20 connection with the protective order.

21 **F. Documents Pursuant to Patent L.R. 3-2(f)**

22 Although MTI is not aware of any agreements that transfer any ownership interest in the
23 Asserted Patents, for the avoidance of doubt, MTI has produced the assignment records filed with
24 the USPTO for each asserted patent bearing production numbers MYM0006449 - MYM0020687

25 **G. Documents Pursuant to Patent L.R. 3-2(g)**

26 MTI is currently not aware of any documents responsive to Patent L.R. 3-2(g). Micron's
27 discovery and investigation are ongoing.

1 **H. Documents Pursuant to Patent L.R. 3-2(h)**

2 In response to Patent L.R. 3-2(h), MTI incorporates its response regarding L.R. 3-2(f) and
3 L.R. 3-2(g).

4 **I. Documents Pursuant to Patent L.R. 3-2(i)**

5 MTI is not currently aware of any documents responsive to the marking portion of Patent
6 L.R. 3-2(i). With respect to sales, revenues, costs and profits, the parties have been meeting and
7 conferring about MTI's production of sales documents in connection with the products that
8 YMTC has accused of infringement, and as a result of those efforts, MTI agreed to produce
9 worldwide information (instead of just U.S. data), which MTI is in the process of collecting.
10 Information responsive to Patent L.R. 3-2(i) regarding the MTI products identified above
11 pursuant to L.R. 3-1(g) will be a subset of this information MTI is collecting and will produce.

12 **J. Documents Pursuant to Patent L.R. 3-2(j)**

13 MTI is currently not aware of any documents specified by Patent L.R. 3-2(j). Micron's
14 discovery and investigation are ongoing.

15
16 Dated: May 6, 2024

ORRICK, HERRINGTON & SUTCLIFFE LLP

17
18 By: /s/Jared Bobrow
19 Jared Bobrow
20 Attorneys for Defendant and Counterclaim
21 Plaintiff Micron Technology, Inc. and
22 Defendant Micron Consumer Products
23 Group, LLC
24
25
26
27
28

1 **CERTIFICATE OF SERVICE**

2 I am employed in the County of San Mateo, State of California. I am over the age of 18
3 years old and not a party to this action. My business address is Orrick, Herrington & Sutcliffe
4 LLP, 1000 Marsh Road, Menlo Park, California 94025. On May 6, 2024, I served the
5 **DEFENDANT AND COUNTERCLAIM PLAINTIFF MICRON TECHNOLOGY's**
6 **DISCLOSURE OF ASSERTED CLAIMS AND INFRINGEMENT CONTENTIONS** on all
7 interested parties to this action in the manner described as follows:

- 8 ☐ **(VIA U.S. MAIL)** On May 6, 2024, by placing a true copy of the document(s) listed
9 above in an envelope, with postage thereon fully prepaid, addressed as set forth below
10 and then sealing the envelope and depositing it in the U.S. mail at Menlo Park, California.
11 ☒ **(VIA EMAIL)** On May 6, 2024, via electronic mail in Adobe PDF format the
12 document(s) listed above to the electronic address(es) set forth below.
13 ☐ **(VIA OVERNIGHT-FED EX)** I caused the within document(s) to be delivered by
14 overnight courier to the address(es) set forth below.

15 Allen S. Cross (Bar. No. 303665)
16 allen.cross@ropesgray.com
17 James R. Batchelder (Bar No. 136347)
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Counsel for Plaintiff, Yangtze Memory Technologies Company, Ltd.

24 I declare under penalty of perjury under the laws of the State of California and the United
25 States that the foregoing is true and correct.

26 Executed on May 6, 2024, at San Mateo, California.

27 /s/Matthew Bonini
28 Matthew Bonini

Infringement Chart for U.S. Patent No. 8,945,996 (the “’996 Patent”)

The following chart provides non-limiting examples, without the benefit of claim construction or discovery, of how YMTC’s Accused Products (as that term is defined in the accompanying cover pleading) meet every limitation, literally or under the doctrine of equivalents, of the claims of U.S. Patent No. 8,945,996. The referenced images are images from a 128L YMTC 512G TLC part. Micron reserves the right to amend, correct, supplement, or otherwise change its explanation of how YMTC’s Accused Products meet the following claim limitations, including as the claims are construed, as discovery progresses, or as Micron’s investigation continues. Micron takes no position on claim interpretation or scope at this time.

’996 Patent Claim	YMTC 128L 3D NAND MEMORY (“YMTC 128L”)
[1.PRE] A method of forming circuitry components, comprising:	YMTC 128L is created by a method of forming circuitry components. Specifically, as shown below, YMTC manufactures the YMTC 128L to include, for example, an end portion, primary portion, dummy structures, and operative structures. For example, the image below depicts a portion of the array of the YMTC 128L product having word lines that extend horizontally and overlap vertically:

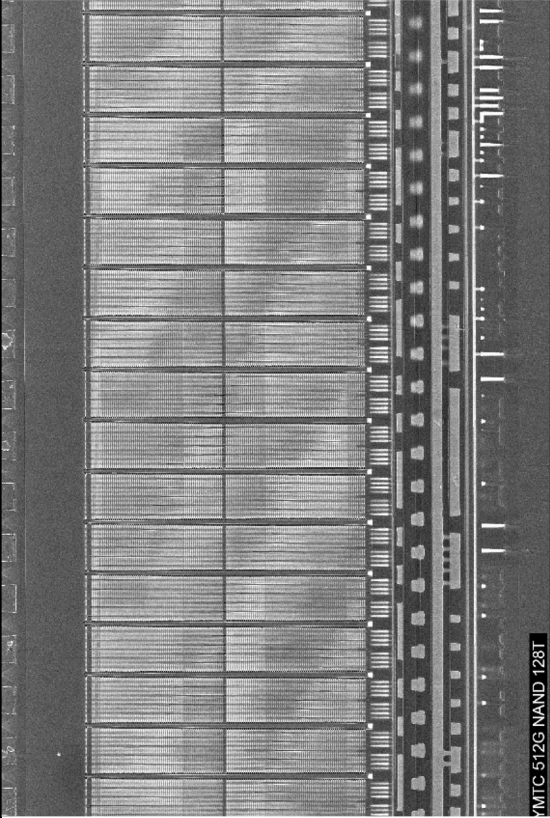
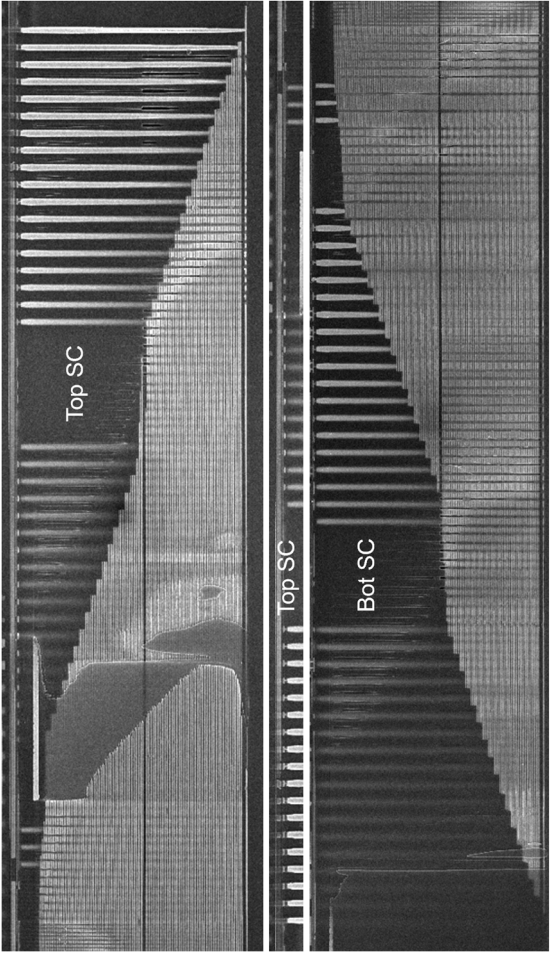
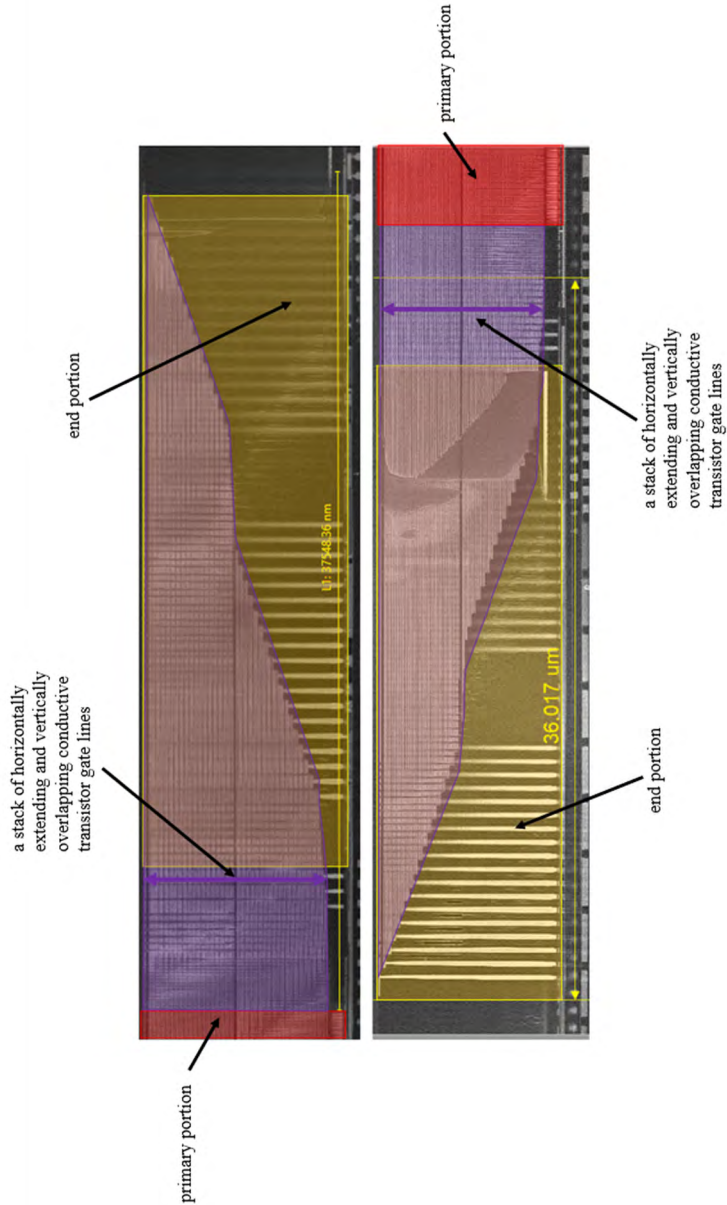
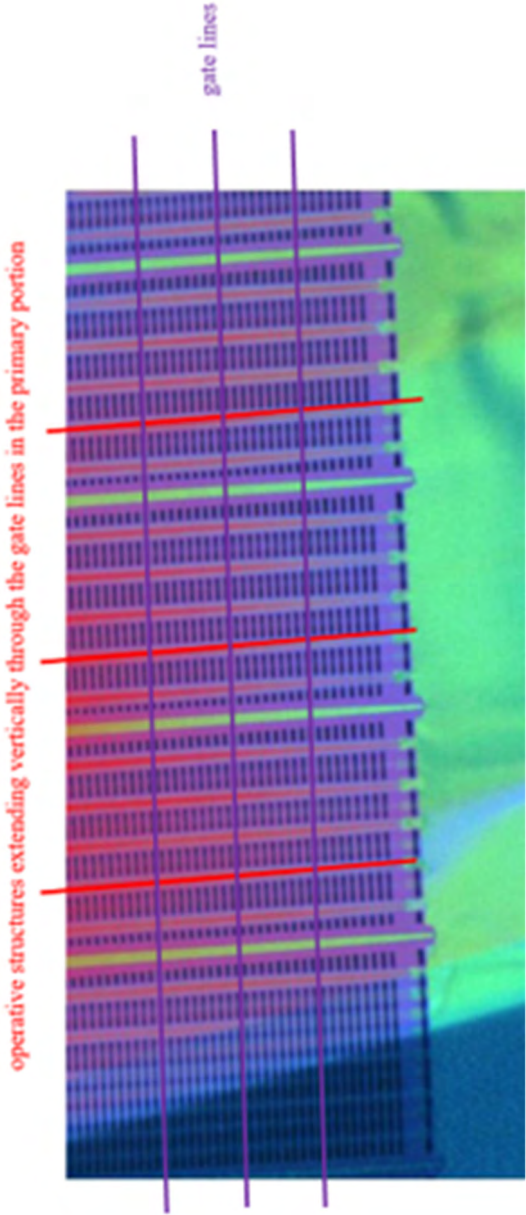
'996 Patent Claim	YMTC 128L 3D NAND MEMORY (“YMTC 128L”)
	 YMTC 512G NAND 128T In the YMTC 128L, these word lines extend horizontally to staircase structures at, for example, ends of the memory array:

EXHIBIT B-2

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC refers to such layers as forming a "stack." See, e.g., U.S. Pat. No. 10,861,872 at Abstract ("stack"). As shown above, there are staircase contacts. These contacts extend down to respective word lines. The supporting circuitry drives these word lines to, for example, access the memory cells.
[1.A] forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;	YMTC 128L is created by forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion. Specifically, as shown below, YMTC forms a stack of alternating gate layers (the word lines) and dielectric layers, which includes a primary portion and end portion. Further, as shown below, at least some of the features (word lines of the stack) extend farther in the horizontal direction in the end portion moving deeper into the stack (e.g., towards the substrate):

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes that the word lines extend further in the end portion, which it refers to as the “staircase region,” than the primary portion, which it refers to as the “core array region.” See, e.g., U.S. Pat. No. 10,861,872 at 6:14-25, Figure 1D.
[1.B] forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion; and	YMTC 128L is created by forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion. Specifically, as shown below, the primary portion includes memory strings that are vertically operative structures including memory cells, and these structures extend through the word line features. Further, as shown below, the end portion includes dummy structures:

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 The micrograph shows a cross-section of the memory array. A yellow arrow points to the 'End Portion' on the left. Red arrows point to 'Dummy structures' in the center. Red lines on the right are labeled 'Gate lines'. YMTC describes replacing the sacrificial gate layer after forming the dummy channel supporting structures. <i>See, e.g., U.S. Pat. No. 10,861,872 at 2:8-18.</i> The dummy channel structures provide a support function during the gate replacement process.
[1.C] removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing.	On information and belief, YMTC 128L is created by removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing. Specifically, as shown below, YMTC employs sacrificial gate layers that it later removes and replaces with functional gate layers, aka, access line ("features") and employs dummy structures to prevent movement of the stack layers: For example, the image below depicts a portion of the array of the YMTC 128L product having word lines that extend horizontally and overlap vertically:

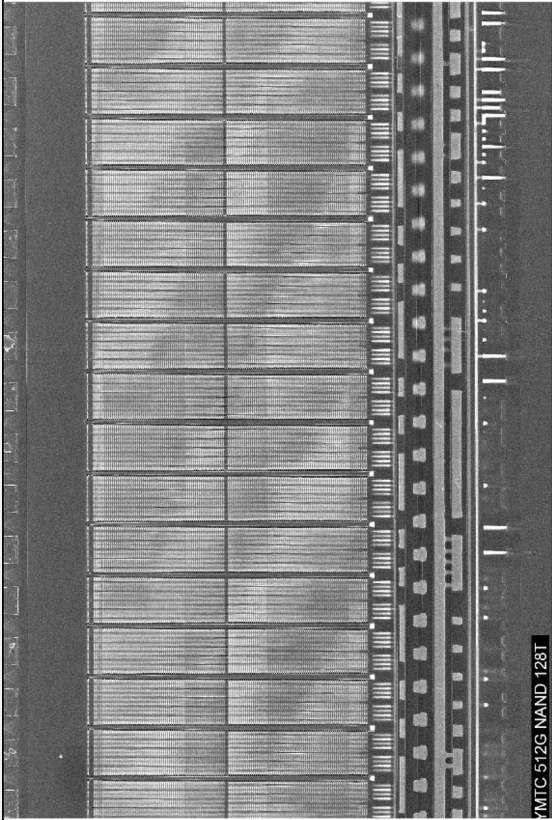
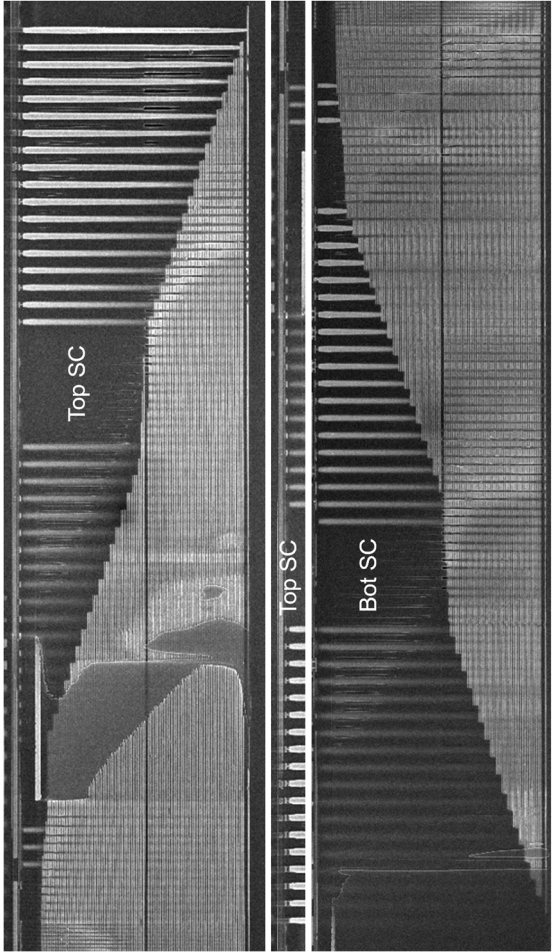
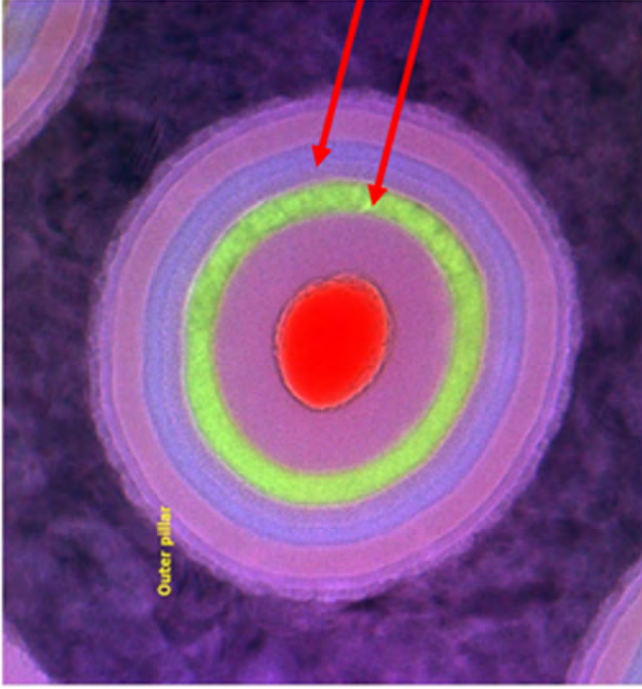
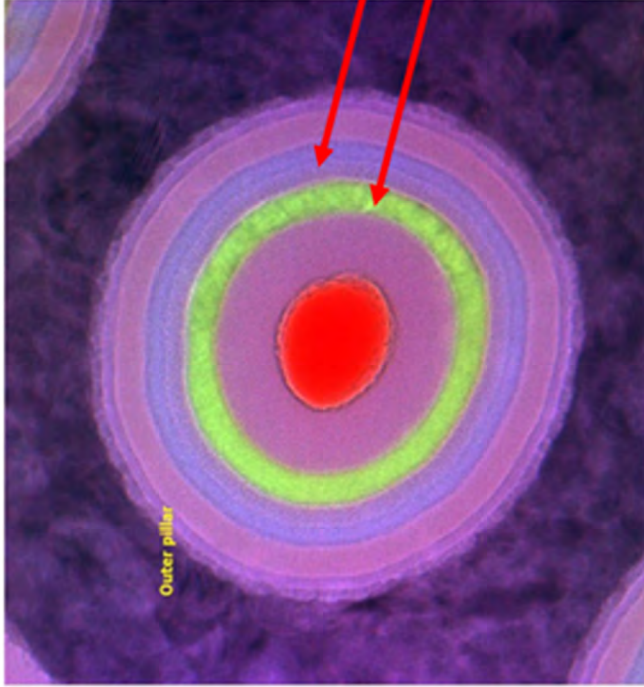
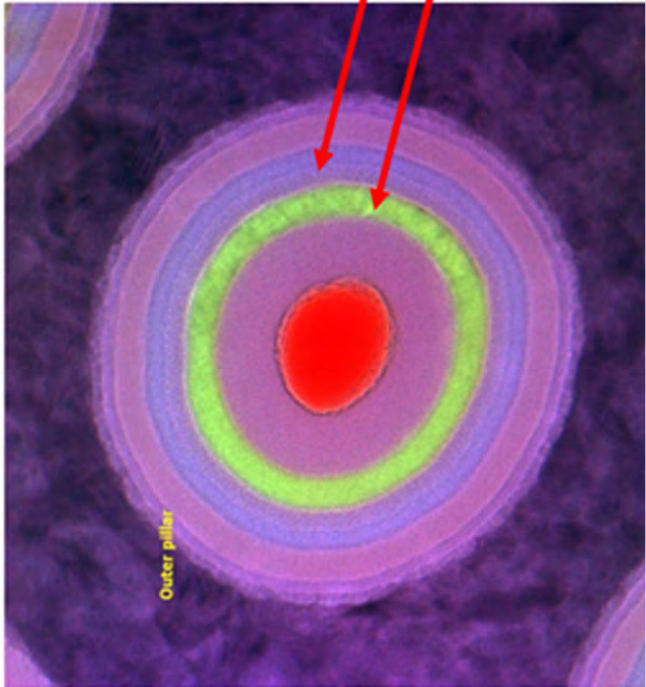
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 In the YMTC 128L these extend horizontally extending and vertically overlapping extend to staircase structures at ends of the memory array:

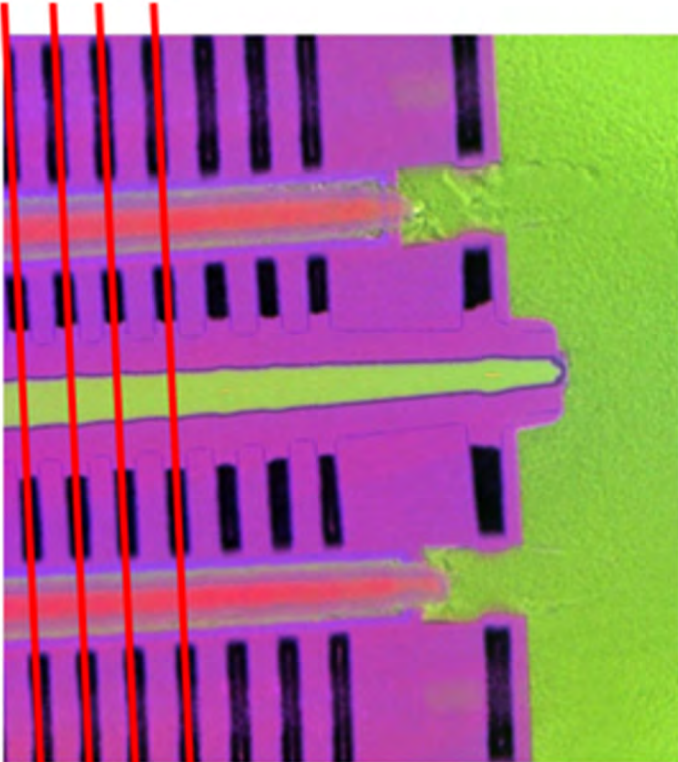
EXHIBIT B-2

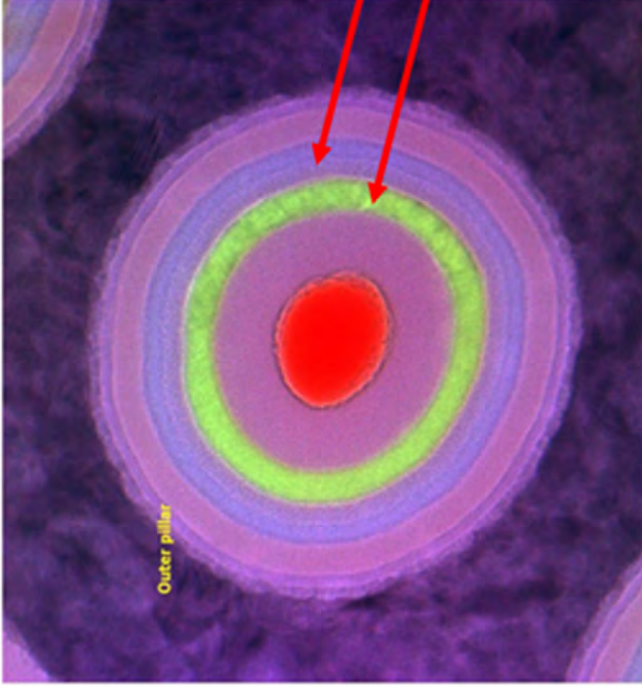
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes replacing the sacrificial gate layer after forming the dummy channel supporting structures. <i>See, e.g.</i>, U.S. Pat. No. 10,861,872 at 2:8-18. The dummy channel structures provide a support function during the gate replacement process.
[2] The method of claim 1 wherein the operative and dummy structures comprise the same material.	On information and belief, YMTC 128L is created by the method of claim 1 wherein the operative and dummy structures comprise the same material. For example, the dummy structures include dummy channel structures.

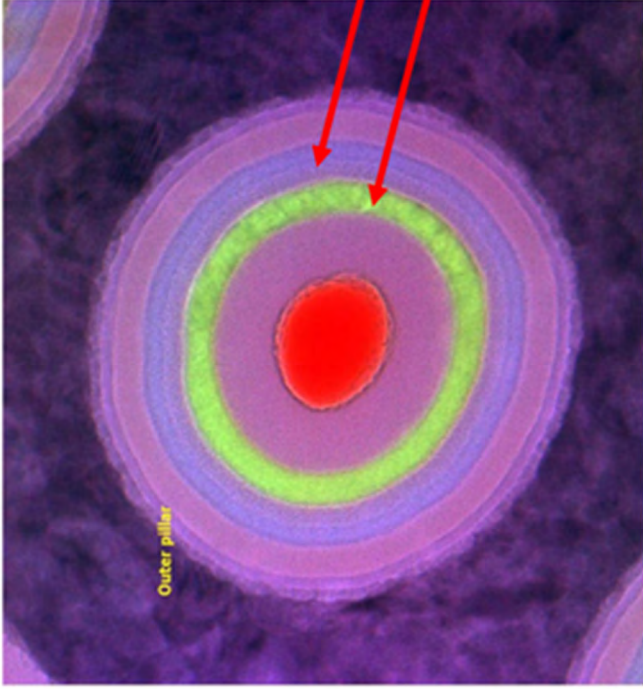
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes that the primary portion, which it refers to as the "core array region," includes these vertical memory strings. <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A.</i> YMTC describes that the end portion, which it refers to as the "staircase region," includes "dummy channel structures." <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:31-50. See also, 2:8-18 ("The 3D memory device also includes an array of dummy channel structures each extending vertically through the staircase structure."), 5:64-67.</i>
[3] The method of claim 2 wherein the operative and dummy structures comprise a plurality of the same materials.	YMTC 128L is created by the method of claim 2 wherein the operative and dummy structures comprise a plurality of the same materials. For example, the dummy structures include dummy channel structures.

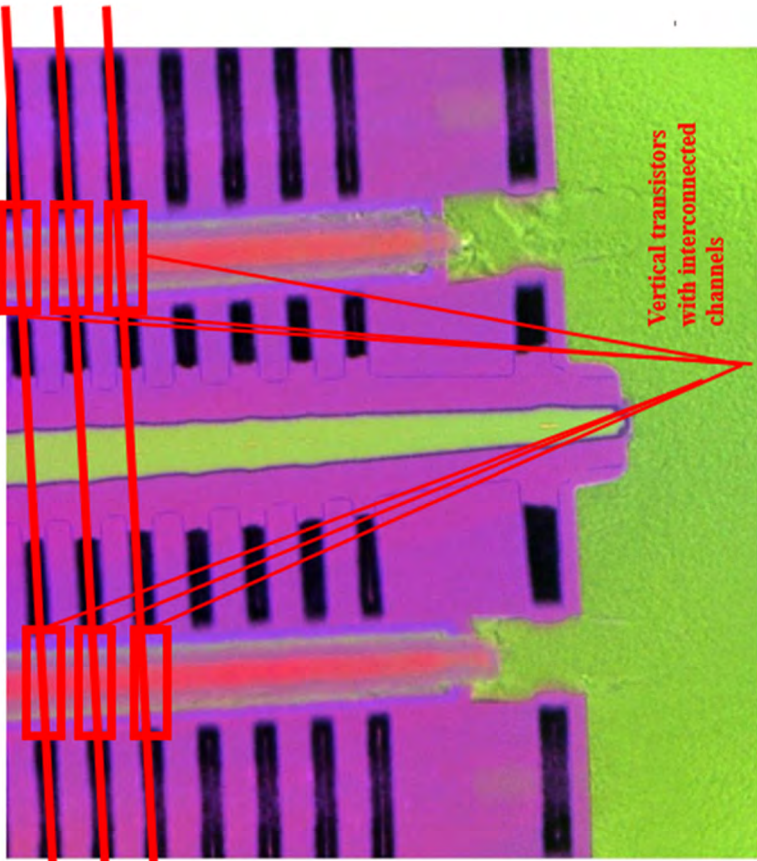
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes that the primary portion, which it refers to as the "core array region," includes these vertical memory strings. <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A.</i> YMTC describes that the end portion, which it refers to as the "staircase region," includes "dummy channel structures." <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:31-50. See also, 2:8-18 ("The 3D memory device also includes an array of dummy channel structures each extending vertically through the staircase structure."), 5:64-67.</i>
[4] The method of claim 3 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.	On information and belief, YMTC 128L is created by the method of claim 3 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures. For example, the dummy structures include dummy channel structures.

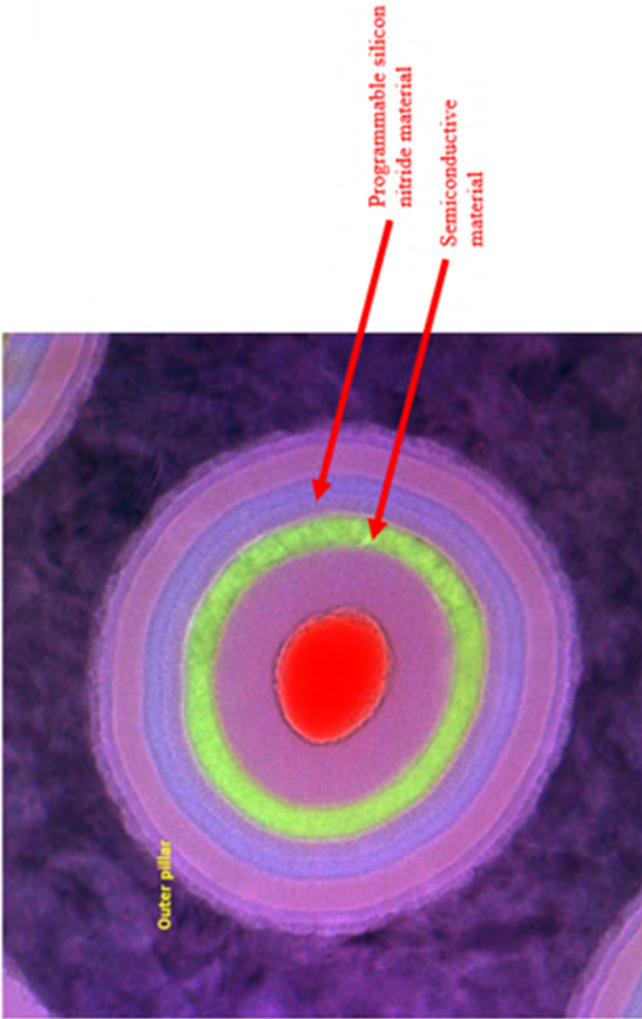
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes that the primary portion, which it refers to as the “core array region,” includes these vertical memory strings. <i>See, e.g.</i>, U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A. YMTC describes that the end portion, which it refers to as the “staircase region,” includes “dummy channel structures.” <i>See, e.g.</i>, U.S. Pat. No. 10,861,872 at 6:31-50. <i>See also</i>, 2:8-18 (“The 3D memory device also includes an array of dummy channel structures each extending vertically through the staircase structure.”), 5:64-67.
[6] The method of claim 1 wherein the features comprise plates.	YMTC 128L is created by the method of claim 1 wherein the features comprise plates.

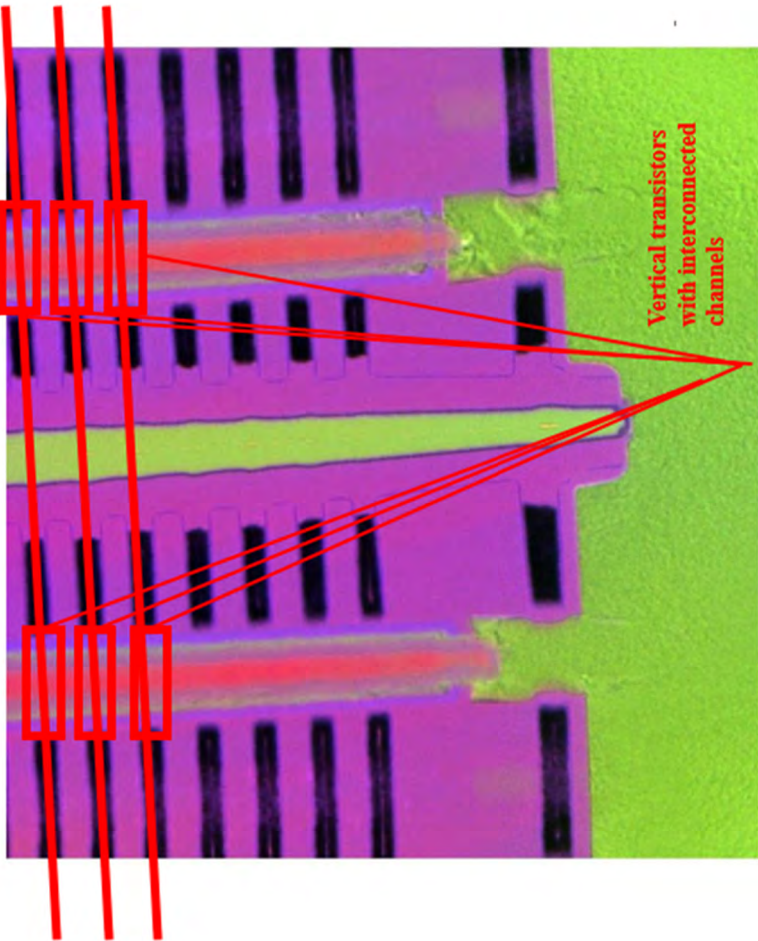
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 Likewise, the insulating material between the word line plates are also plates of insulating material.
[7] The method of claim 1 wherein the operative and dummy structures comprise programmable material.	On information and belief, YMTC 128L is created by the method of claim 1 wherein the operative and dummy structures comprise programmable material.

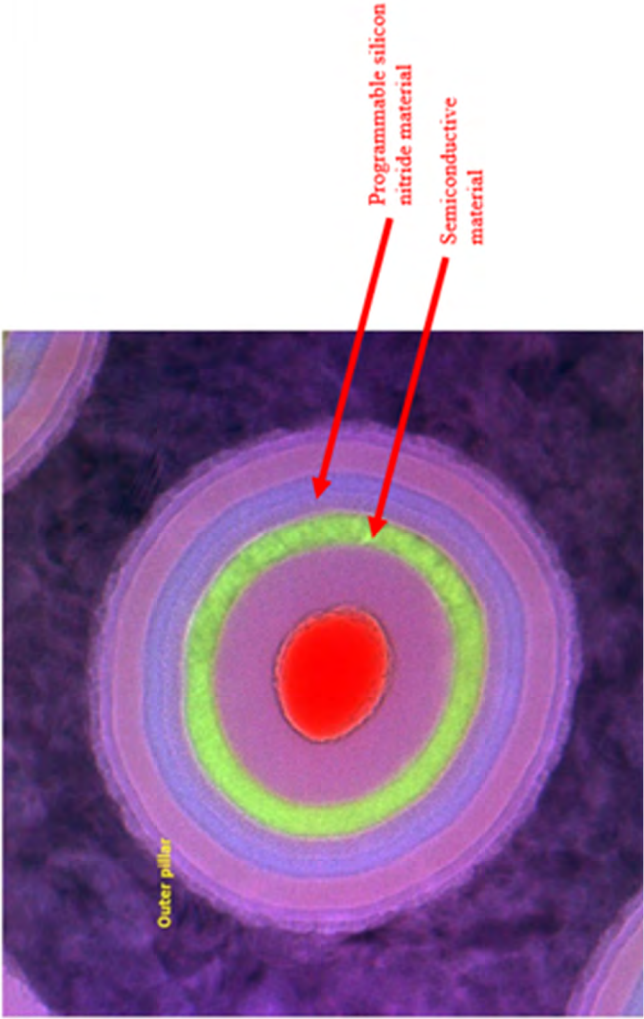
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes that the primary portion, which it refers to as the “core array region,” includes these vertical memory strings. <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A.</i> YMTC describes that the end portion, which it refers to as the “staircase region,” includes “dummy channel structures.” <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:31-50. See also, 2:8-18 (“The 3D memory device also includes an array of dummy channel structures each extending vertically through the staircase structure.”), 5:64-67.</i> On information and belief, both the operative structures and the dummy structures include a silicon nitride layer that can be programmed.
[8] The method of claim 1 wherein the operative and	On information and belief, YMTC 128L is created by the method of claim 1 wherein the operative and dummy structures comprise semiconductive material.

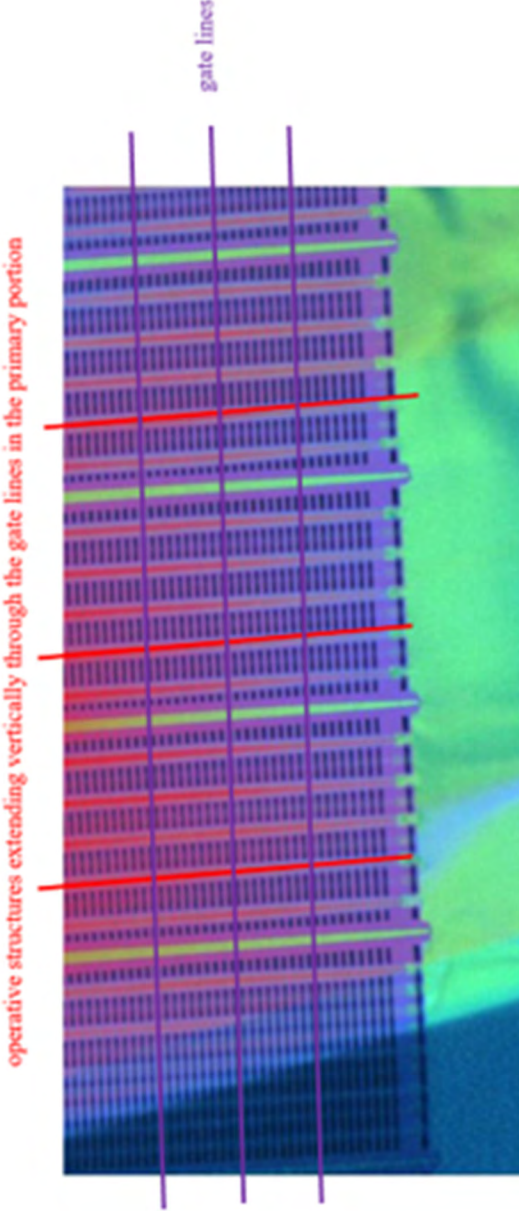
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
dummy structures comprise semiconductive material.	 YMTC describes that the primary portion, which it refers to as the "core array region," includes these vertical memory strings. <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A.</i> YMTC describes that the end portion, which it refers to as the "staircase region," includes "dummy channel structures." <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:31-50. See also, 2:8-18 ("The 3D memory device also includes an array of dummy channel structures each extending vertically through the staircase structure."), 5:64-67.</i>
[9] The method of claim 8 wherein the semiconductive material of the operative structures comprises	YMTC 128L is created by the method of claim 8 wherein the semiconductive material of the operative structures comprises interconnected channels of a plurality of vertically oriented transistors.

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
interconnected channels of a plurality of vertically oriented transistors.	 Word lines of individual vertical transistors Vertical transistors with interconnected channels As shown below, the semiconductor material is a continuous vertical channel.

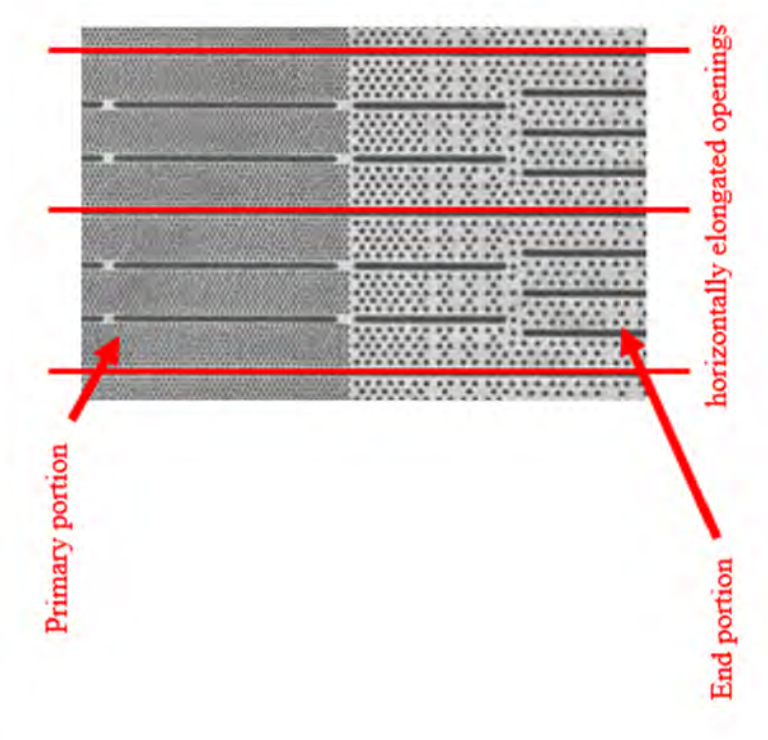
'996 Patent Claim	YMTC 128L 3D NAND MEMORY (“YMTC 128L”)
	
[10] The method of claim 9 wherein interconnected channels are of vertically oriented charge storage transistors.	YMTC 128L is created by the method of claim 9 wherein interconnected channels are of vertically oriented charge storage transistors. The YMTC 128L is a NAND Flash memory device and the vertically oriented transistors are charge storage transistors.

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 Word lines of individual vertical transistors Vertical transistors with interconnected channels For example, as shown below, there is a charge storage layer, e.g., silicon nitride.

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	
[12.PRE] A method of forming circuitry components, comprising:	YMTC 128L is created by 1 method of forming circuitry components. See [1.PRE], <i>supra</i>.
[12.A] forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end	YMTC 128L is created by forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion. See [1.A], <i>supra</i>.

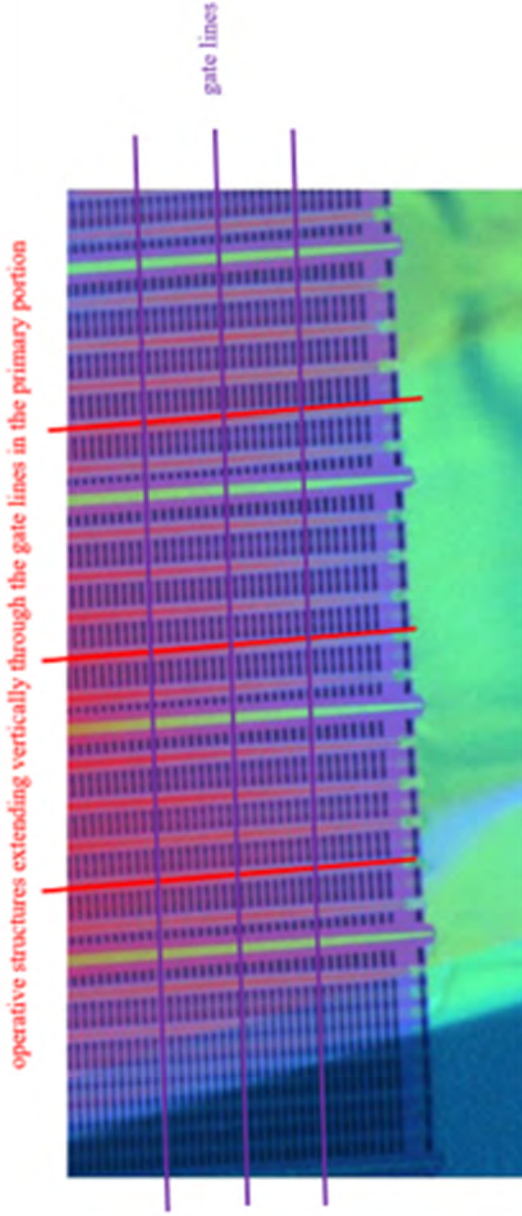
’996 Patent Claim portion moving deeper into the stack in the end portion;	YMTC 128L 3D NAND MEMORY (“YMTC 128L”)
[12.B] forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the plates in the end portion;	YMTC 128L is created by forming operative structures vertically through the features (i.e., gate lines or word lines) in the primary portion and forming dummy structures vertically through the plates (i.e., gate lines or word lines) in the end portion. See [1.B], <i>supra</i>.  Likewise, the insulating material between the word line plates are also plates—plates of insulating material.

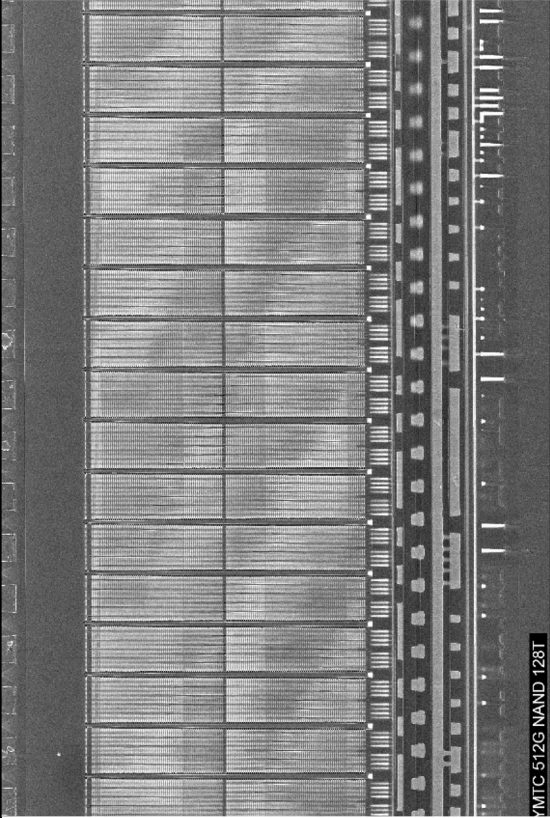
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
[12.C] forming horizontally elongated openings through the structures to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures.	 The micrograph shows a series of parallel, horizontally elongated structures. A yellow arrow points to the 'End Portion' of one structure. Red arrows point to 'Dummy structures' and 'Gate lines'.

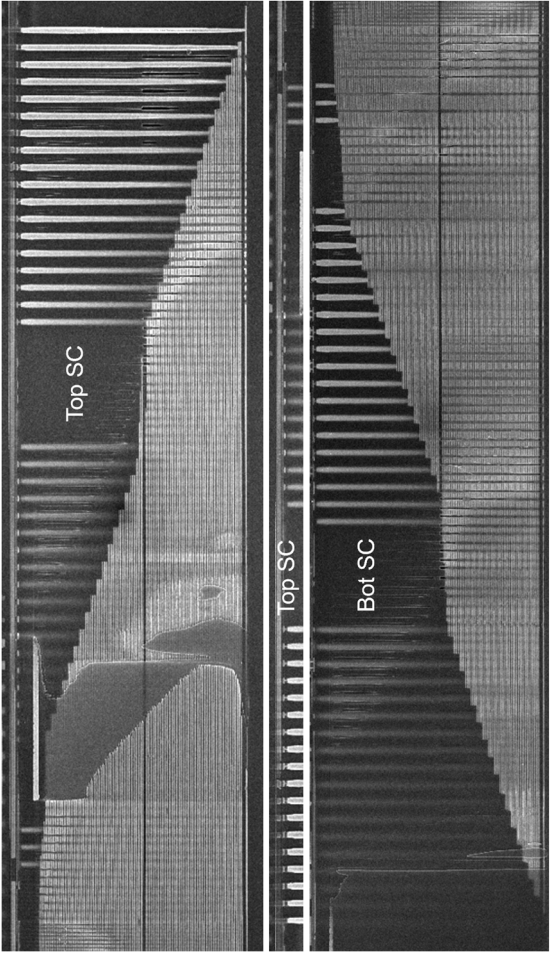
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
extending portions of both the operative structures and the dummy structures; and	 The diagram shows a cross-section of a memory stack with three main regions. The leftmost region is labeled 'Primary portion' with a red arrow. The middle region is labeled 'End portion' with a red arrow. The rightmost region is labeled 'horizontally elongated openings' with a red arrow. The stack consists of alternating layers of material, with the openings being horizontal channels. As shown below, the stack surrounds the dummy and operative structures.

'996 Patent Claim	YMTC 128L 3D NAND MEMORY (“YMTC 128L”)
	

EXHIBIT B-2

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	
[12.D] removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings.	On information and belief, YMTC 128L is created by removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings. Specifically, as shown below, YMTC employs depositing sacrificial gate layers that it later removes and replaces with functional gate layers, aka, access line ("features") and employs dummy structures to prevent movement of the stack layers: See [1.C], <i>supra</i>. For example, the image below depicts a portion of the array of the YMTC 128L product having word lines that extend horizontally and overlap vertically:

'996 Patent Claim	YMTC 128L 3D NAND MEMORY (“YMTC 128L”)
	 YMTC 512G NAND 128T In the YMTC 128L these extend horizontally extending and vertically overlapping extend to staircase structures at ends of the memory array:

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes replacing the sacrificial gate layer after forming the dummy channel supporting structures. <i>See, e.g.</i>, U.S. Pat. No. 10,861,872 at 2:8-18.
[13] The method of claim 12 wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures.	On information and belief, YMTC 128L is created by the method of claim 12 wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures. For example, based on the structure below one of ordinary skill in the art would understand that some materials were removed by a process that did not remove other of the materials and that gate lines or word lines were formed in the spaces where material was removed.

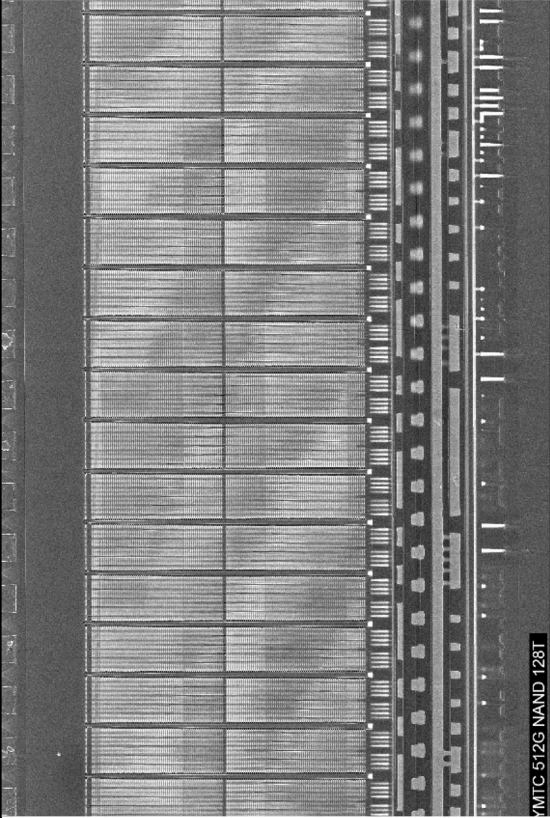
'996 Patent Claim	YMTC 128L 3D NAND MEMORY (“YMTC 128L”)
	 YMTC 512G NAND 128T YMTC describes selectively etching sacrificial material to remove sacrificial material. <i>See, e.g.</i>, U.S. Pat. No. 10,861,872 at 15:16-25. The etch does not remove the lines, operative structures, or dummy structures, as these features remain after the sacrificial gate layer removal.
[16] The method of claim 12 wherein the features comprise plates.	YMTC 128L is created by the method of claim 12 wherein the features comprise plates.

EXHIBIT B-2

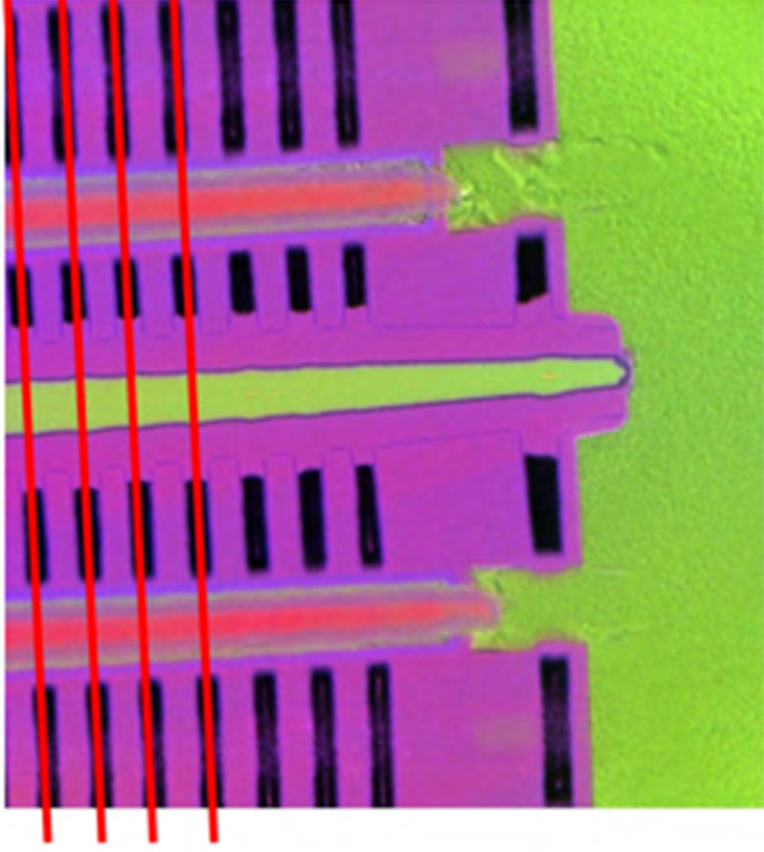
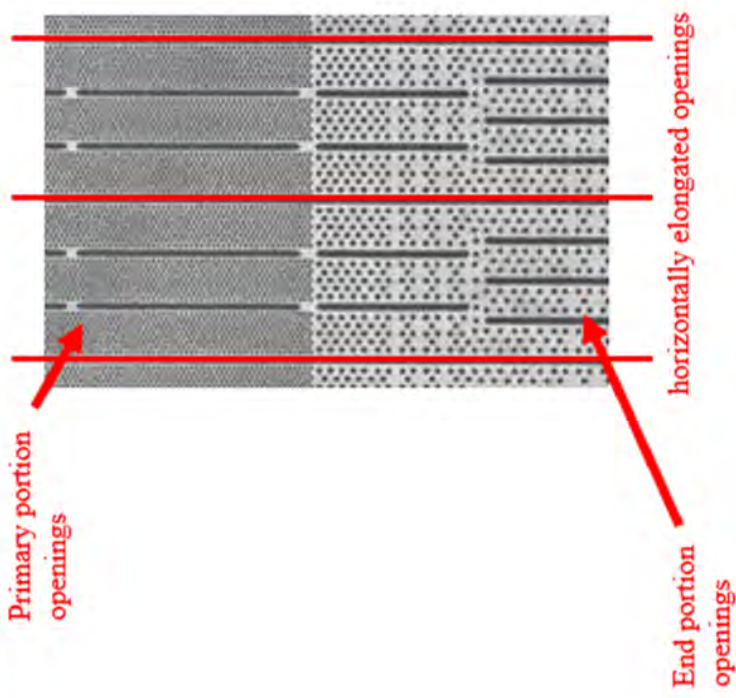
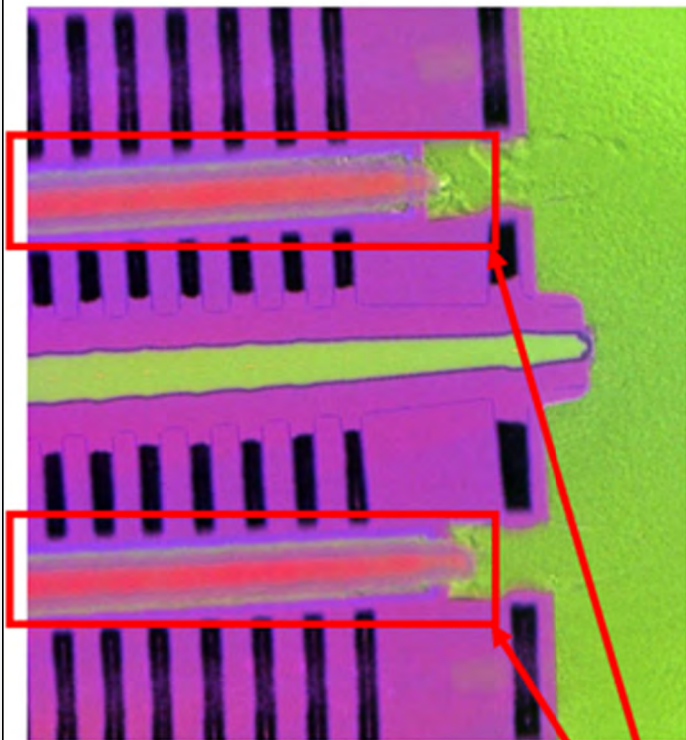
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 Likewise, the insulating material between the word line plates are also plates—plates of insulating material.
[17.PRE] A method of forming circuitry components, comprising:	YMTC 128L is created by a method of forming circuitry components. See [1.PRE], <i>supra</i>.
[17.A] forming a stack of horizontally extending and vertically overlapping features,	YMTC 128L is created by forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features

EXHIBIT B-2

’996 Patent Claim	YMTC 128L 3D NAND MEMORY (“YMTC 128L”)
the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;	extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion <i>See [1.A], supra.</i>
[17.B] forming primary portion openings through the features in the primary portion and forming the end portion openings through the features in the in the end portion;	YMTC 128L is created by forming primary portion openings through the features in the primary portion and forming end portion openings through the features in the in the end portion.

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 The diagram shows a cross-section of a 3D NAND memory stack. It features a central region with a grid of openings, flanked by two regions with horizontal lines. Red arrows point to the top and bottom of the central region, labeled 'Primary portion openings' and 'End portion openings' respectively. A red arrow points to the right side of the central region, labeled 'horizontally elongated openings'. The end portion opening continue until at least the termination of the stair case region.
[17.C] forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the	YMTC 128L is created by forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the end portion openings and forming operative structures therewith within the primary portion openings and forming dummy structures therewith within the end portion openings.

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
end portion openings and forming operative structures therewith within the primary portion openings and forming dummy structures therewith within the end portion openings;	 Strings of vertically interconnected operative structure formed of conductive or semiconductive material On information and belief, the end portion openings are filled with a conductive or semiconductive material to form dummy structures:

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 The micrograph shows a series of horizontal, elongated, overlapping lines representing the features of the memory. A yellow arrow points to the 'End Portion' of these lines. Red arrows point to 'Dummy structures' at the end of the lines. Red lines indicate 'Gate lines' running parallel to the features.
[17.D] forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines	YMTC 128L is created by forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures.

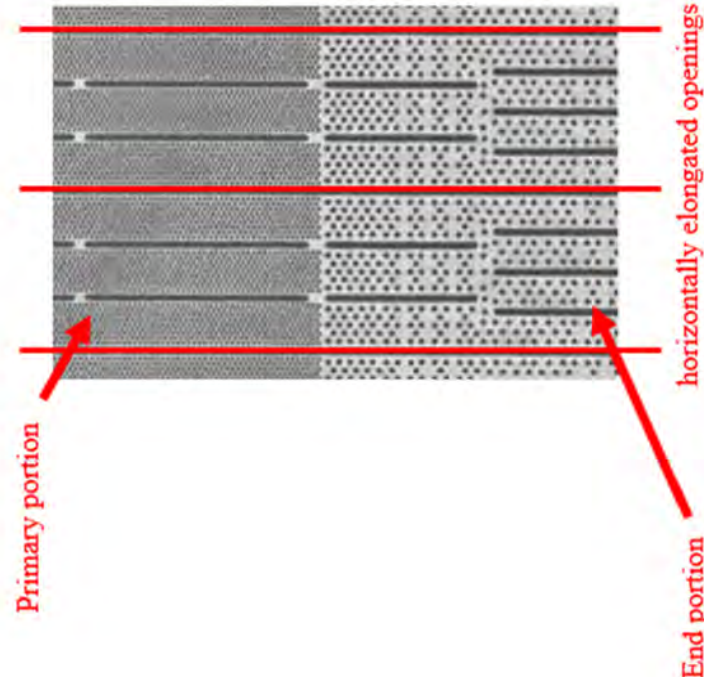
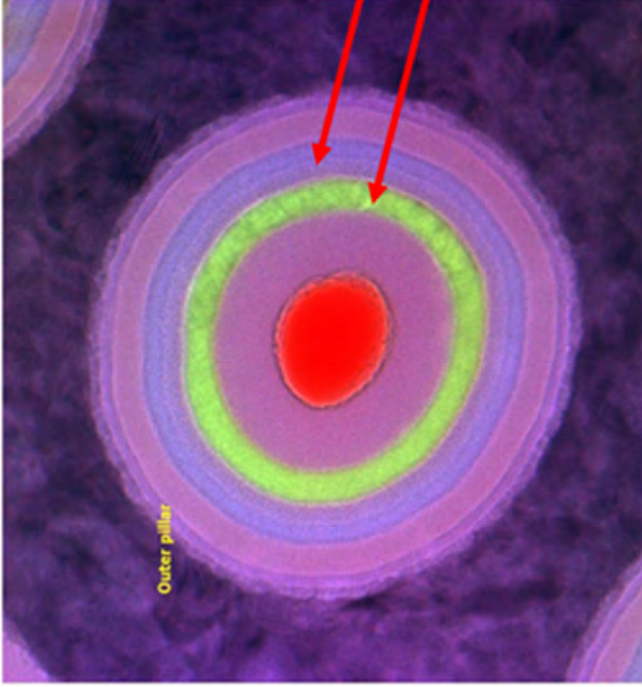
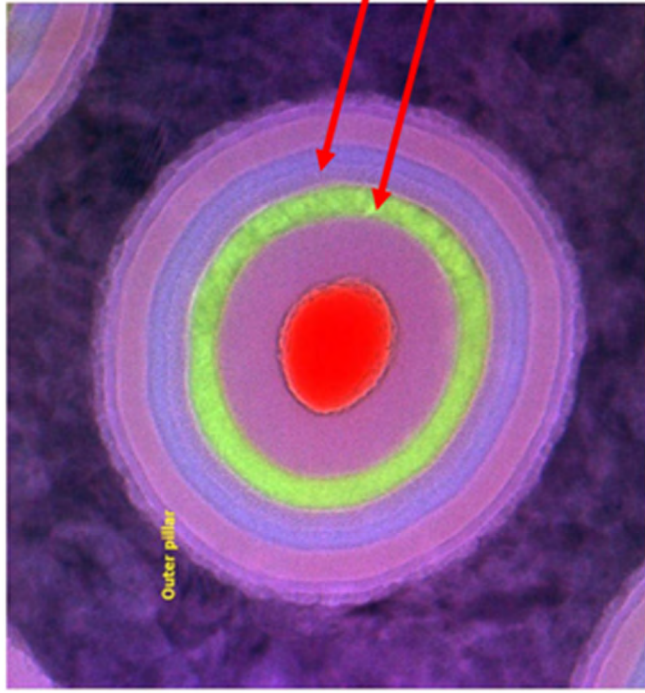
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures; and	 The diagram is a cross-sectional view of a 3D NAND memory stack. It shows a central 'Primary portion' and a side 'End portion'. Both portions contain multiple layers of memory cells, represented by horizontal lines. Between these layers are 'horizontally elongated openings'. Red arrows point from the labels 'Primary portion' and 'End portion' to their respective regions in the diagram.
[17.E] removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions	YMTC 128L is created by removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.

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'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.	See [12.D], [13], <i>supra</i> .
[18] The method of claim 17 comprising forming the primary portion openings and the end portion openings at the same time.	On information and belief, YMTC 128L is created by the method of claim 17 comprising forming the primary portion openings and the end portion openings at the same time. Upon information and belief, YMTC, for example, forms the openings for the channel and dummy channel structures at the same time.

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes that the primary portion, which it refers to as the "core array region," includes these vertical memory strings. <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A.</i> YMTC describes that the end portion, which it refers to as the "staircase region," includes "dummy channel structures." <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:31-50. See also, 2:8-18 ("The 3D memory device also includes an array of dummy channel structures each extending vertically through the staircase structure."), 5:64-67.</i>
[23] The method of claim 17 wherein said at least one of conductive material, semiconductive material, and programmable material is deposited simultaneously into the	YMTC 128L is created by the method of claim 17 wherein said at least one of conductive material, semiconductive material, and programmable material is deposited simultaneously into the primary portion openings and the end portion openings. For example, upon information and belief, the dummy channel structures and channel structures are made at the same time.

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
primary portion openings and the end portion openings.	 YMTC describes that the primary portion, which it refers to as the “core array region,” includes these vertical memory strings. See, e.g., U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A. YMTC describes that the end portion, which it refers to as the “staircase region,” includes “dummy channel structures.” See, e.g., U.S. Pat. No. 10,861,872 at 6:31-50. See <i>also</i>, 2:8-18 (“The 3D memory device also includes an array of dummy channel structures each extending vertically through the staircase structure.”), 5:64-67.

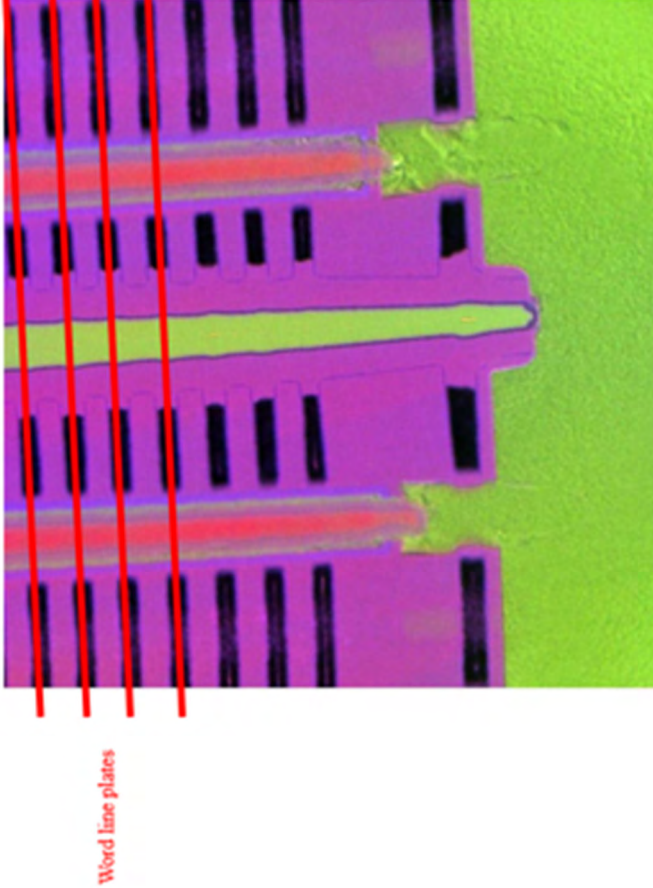
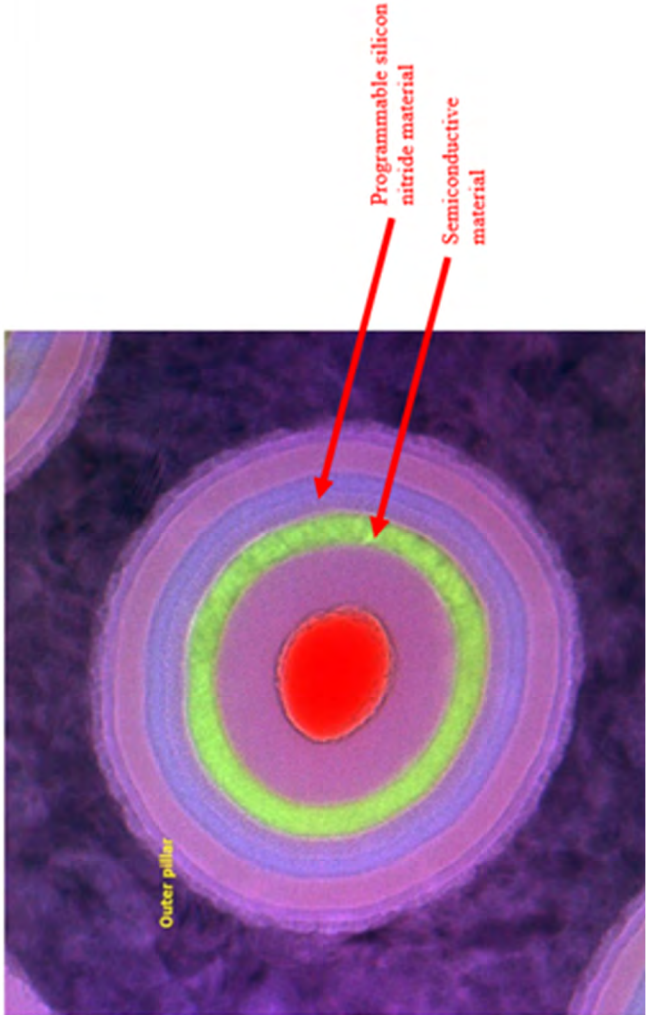
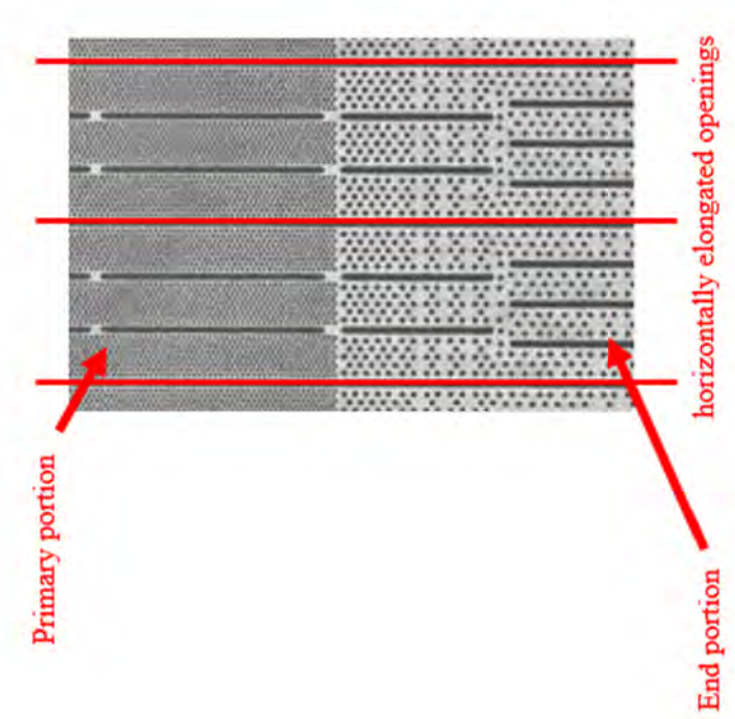
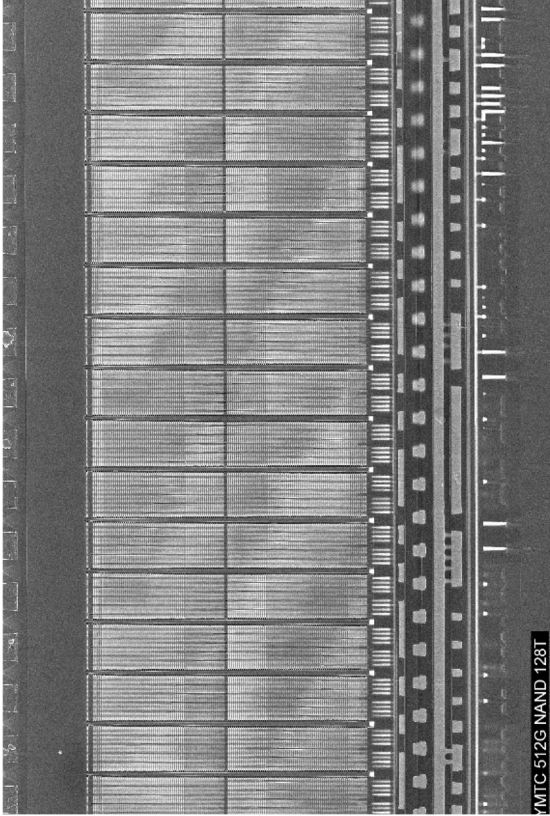
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
[24] The method of claim 17 wherein the features comprise plates.	YMTC 128L is created by the method of claim 17 wherein the features comprise plates.  Likewise, the insulating material between the word line plates are also plates—plates of insulating material.
[25.PRE] A method of forming an array of memory cells, comprising:	YMTC 128L is created by a method of forming an array of memory cells. See [1.PRE], <i>supra</i>.

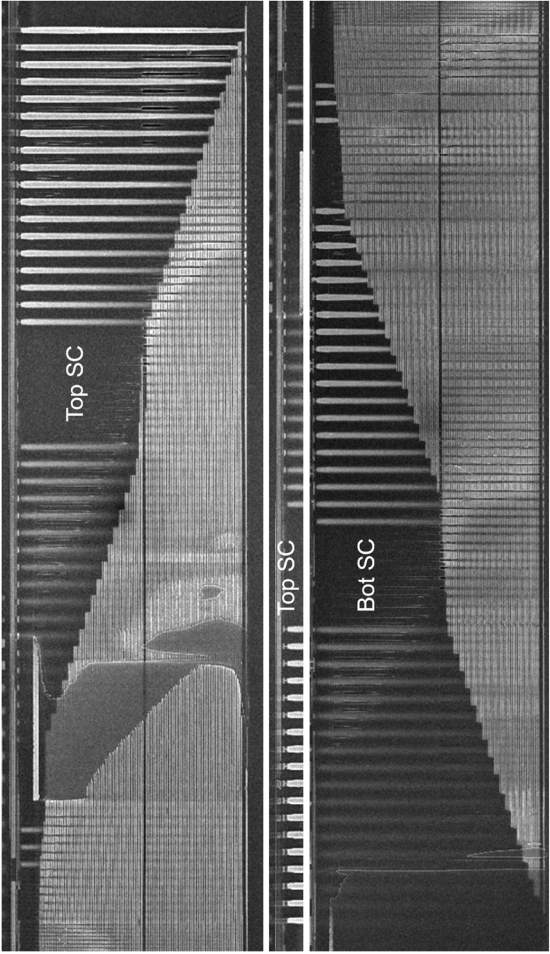
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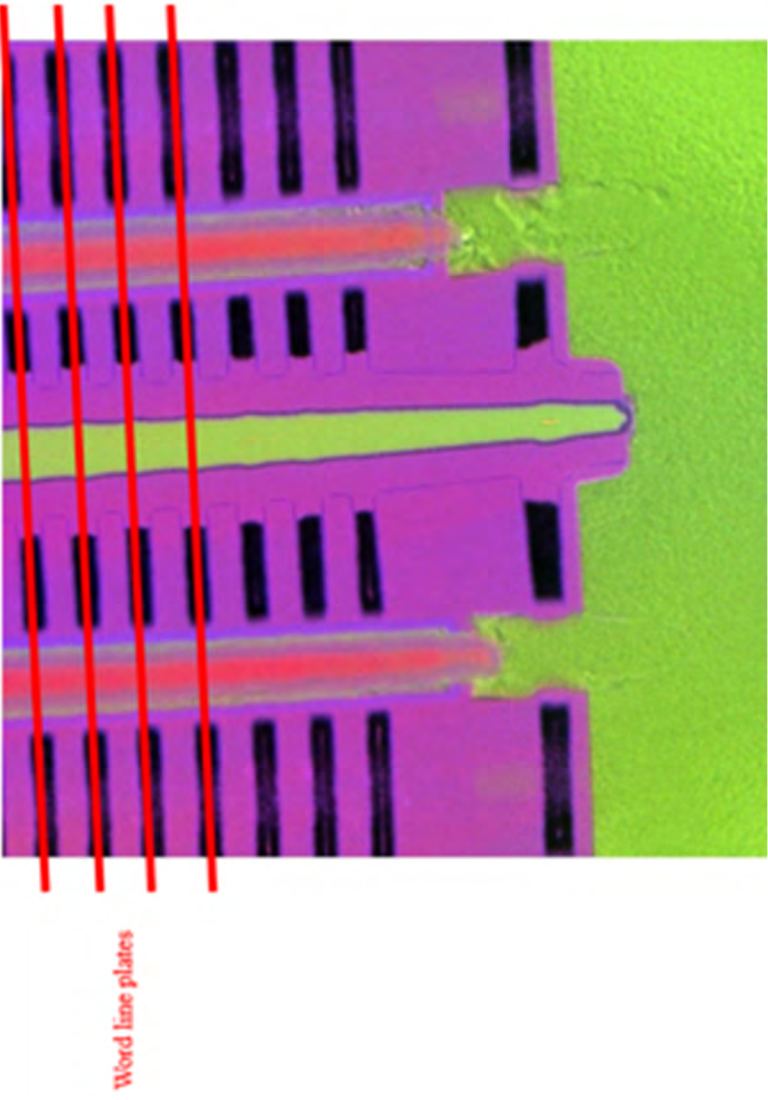
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
[25.A] forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion having sacrificial material-comprising stairs;	YMTC 128L is created by forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion, the end portion having sacrificial material-comprising stairs. <i>See [1.A], supra.</i>
[25.B] forming a plurality of first openings into the primary portion of the stack;	YMTC 128L is created by forming a plurality of first openings into the primary portion of the stack. <i>See [1.B], supra.</i>
[25.C] forming a plurality of second openings into the end portion of the stack;	YMTC 128L is created by forming a plurality of second openings into the end portion of the stack. <i>See [1.B], supra.</i>
[25.D] simultaneously forming at least one of conductive material, semiconductor material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and forming dummy structures therewith within the second openings in the end portion;	YMTC 128L is created by simultaneously forming at least one of conductive material, semiconductor material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and forming dummy structures therewith within the second openings in the end portion.

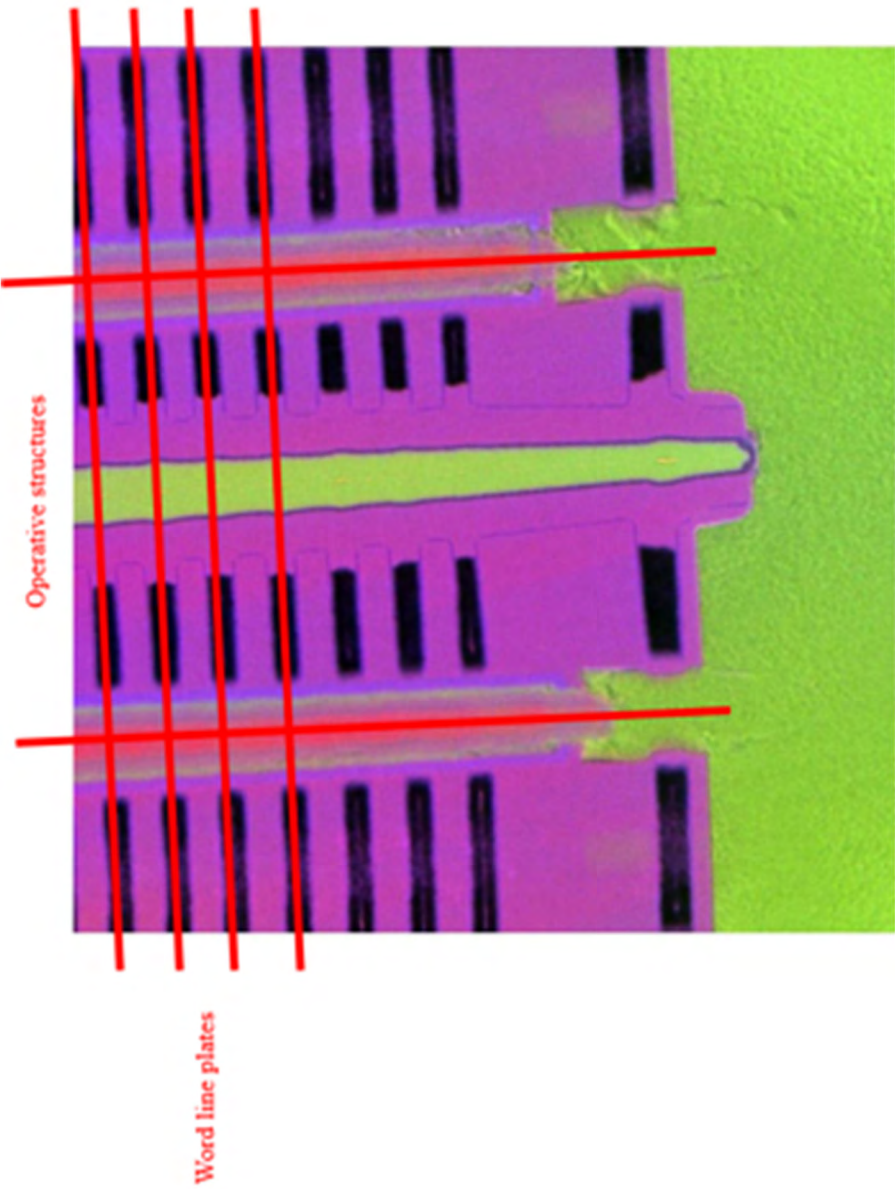
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes that the primary portion, which it refers to as the “core array region,” includes these vertical memory strings. <i>See, e.g.</i>, U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A. YMTC describes that the end portion, which it refers to as the “staircase region,” includes “dummy channel structures.” <i>See, e.g.</i>, U.S. Pat. No. 10,861,872 at 6:31-50. <i>See also</i>, 2:8-18 (“The 3D memory device also includes an array of dummy channel structures each extending vertically through the staircase structure.”), 5:64-67. The structures include at least programmable SiN material and a semiconductive polysilicon layer

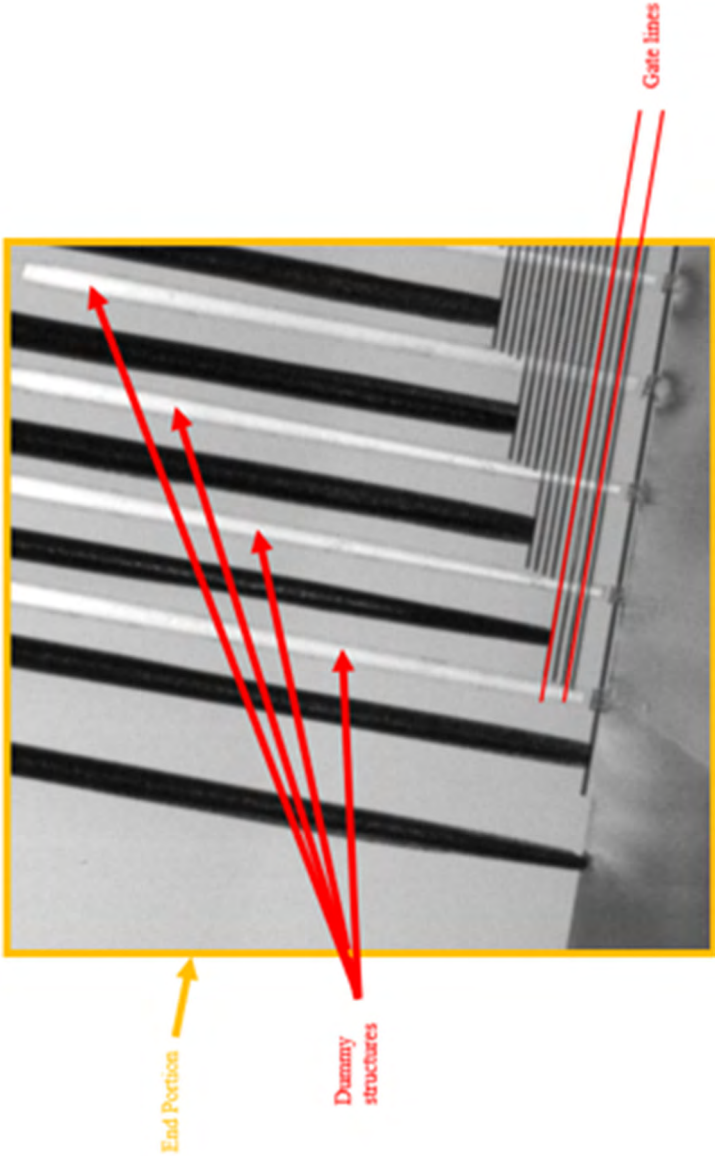
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
[25.E] forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings;	YMTC 128L is created by forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings.  The diagram illustrates a cross-section of a 3D NAND memory stack. It is divided into two main regions: a 'Primary portion' on the left and an 'End portion' on the right, separated by a vertical red line. Both portions contain multiple layers of material, represented by different hatching patterns. Horizontally elongated openings are formed through the stack, extending from the primary portion into the end portion. Red arrows point to these openings, with one arrow labeled 'Primary portion' and another labeled 'End portion'. A red line at the bottom of the stack is labeled 'horizontally elongated openings'.

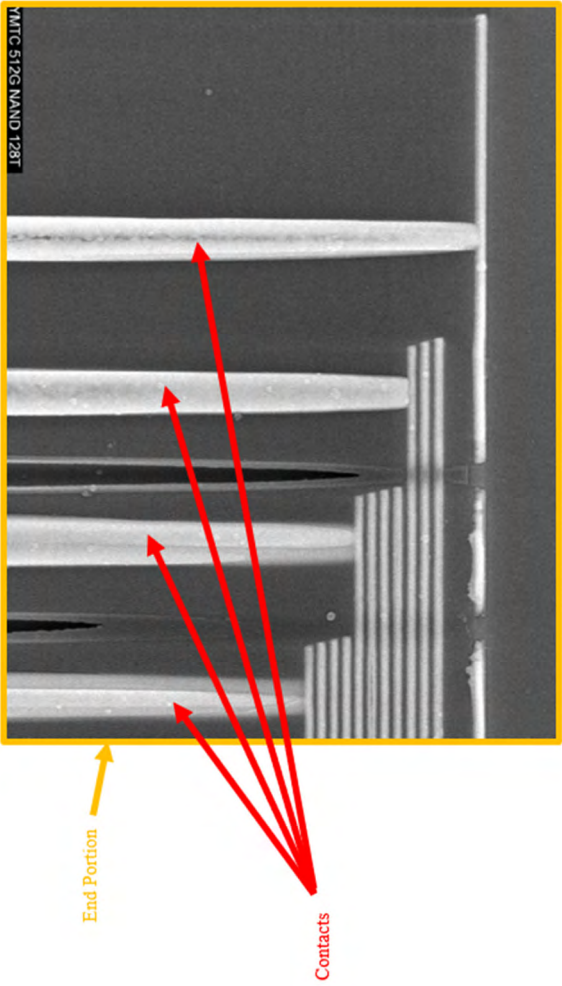
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
[25.F] removing at least a portion of the sacrificial material that is laterally between the horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material;	YMTC 128L is created by removing at least a portion of the sacrificial material that is laterally between the horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material. For example, the image below depicts a portion of the array of the YMTC 128L product having word lines that extend horizontally and overlap vertically:  In the YMTC 128L these extend horizontally extending and vertically overlapping extend to staircase structures at ends of the memory array:

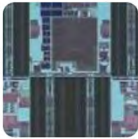
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes replacing the sacrificial gate layer after forming the dummy channel supporting structures. <i>See, e.g., U.S. Pat. No. 10,861,872 at 2:8-18.</i> The dummy channel structures provide a support function during the gate replacement process.
[25.G] after the removing, forming conductive material into the horizontally elongated openings and the void spaces;	YMTC 128L is created by after the removing, forming conductive material into the horizontally elongated openings and the void spaces. Specifically, word lines are formed of a conductive material such as a metal.

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	
[25.H] removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the	YMTC 128L is created by removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure. A

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure; and	specifically conductive word line material is removed to allow for operative structure and dummy structures. 

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 The micrograph shows a cross-section of a 3D NAND memory array. The structure consists of multiple layers of alternating light and dark horizontal bands, representing different material layers. A yellow arrow points to the 'End Portion' of the structure. Red arrows point to 'Dummy structures' and 'Gate lines'. The 'Gate lines' are shown as thin, parallel lines on the right side of the structure.

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[25.I] forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion.	YMTC 128L is created by forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion. 

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[26] The method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel regions of a NAND string.	On information and belief, YMTC 128L is created by the method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel regions of a NAND string.¹  TechnoInsights https://www.technoinsights.com › products › ame-2109-801 › YMTC YMN09TC1B1HC6C 128L 3D NAND 512 Gb TLC ... Apr 5, 2022 — This report presents an advanced memory essentials (AME) analysis of the YMTC YMN09TC1B1HC6C (CDT1B die) 128-layer 3D NAND 512 Gb flash ... 

¹ <https://www.technoinsights.com/blog/memory/ymtc-128l-3d-xtacking-20-tlc-nand>

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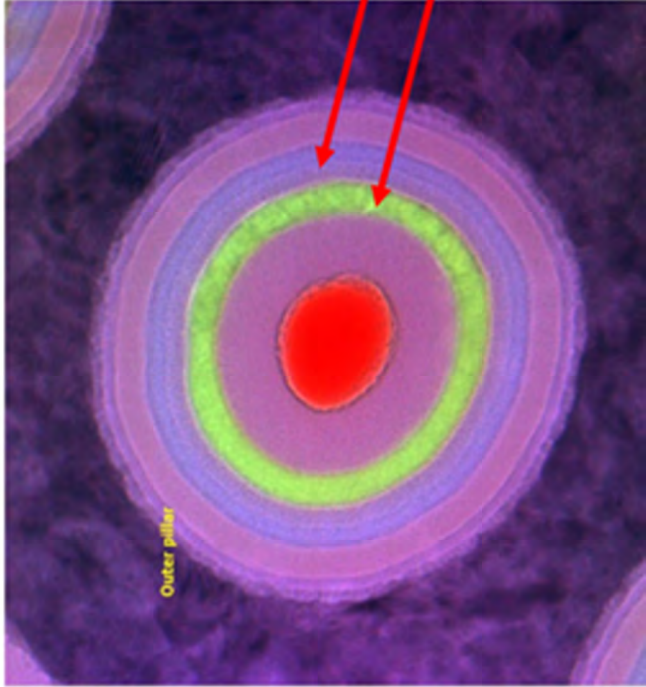
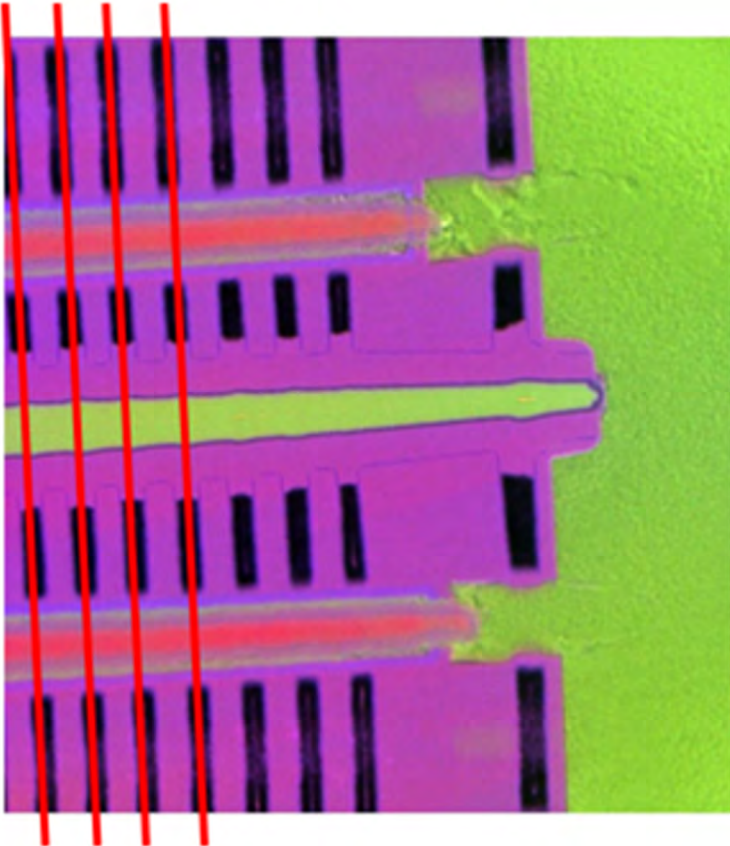
'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 YMTC describes that the primary portion, which it refers to as the "core array region," includes these vertical memory strings. <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A.</i> YMTC describes that the end portion, which it refers to as the "staircase region," includes "dummy channel structures." <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:31-50. See also, 2:8-18 ("The 3D memory device also includes an array of dummy channel structures each extending vertically through the staircase structure.")</i>, 5:64-67.
[28] The method of claim 25 comprising forming the first and second openings using the same masking step.	On information and belief, YMTC 128L is created by the method of claim 25 comprising forming the first and second openings using the same masking step. YMTC describes that the primary portion, which it refers to as the "core array region," includes these vertical memory strings. <i>See, e.g., U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A.</i> YMTC

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'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	describes that the end portion, which it refers to as the "staircase region," includes "dummy channel structures." <i>See, e.g.,</i> U.S. Pat. No. 10,861,872 at 6:31-50. <i>See also</i> , 2:8-18, 5:64-67.
[30] The method of claim 25 wherein the sacrificial material is dielectric.	YMTC 128L is created by the method of claim 25 wherein the sacrificial material is dielectric. YMTC describes selectively etching sacrificial material to remove sacrificial material. <i>See, e.g.,</i> U.S. Pat. No. 10,861,872 at 15:16-25. The etch does not remove the lines, operative structures, or dummy structures, as these features remain after the sacrificial gate layer removal.
[32] The method of claim 25 wherein the features comprise plates.	YMTC 128L is created by the method of claim 25 wherein the features comprise plates.

'996 Patent Claim	YMTC 128L 3D NAND MEMORY ("YMTC 128L")
	 Word line plates Likewise, the insulating material between the word line plates are also plates—plates of insulating material.