

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

Petitioner,

v.

MICRON TECHNOLOGY, INC.

Patent Owner.

Case IPR2025-00098

U.S. Patent No. 8,945,996

PETITION FOR *INTER PARTES* REVIEW

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EXHIBIT LIST

Exhibit No.	DESCRIPTION
1001	U.S. Patent No. 8,945,996 (“’996”)
1002	File History of U.S. Application No. 13/085,083 (“’996FH”)
1003	Declaration of Keln Kuhn (“Kuhn”)
1004	U.S. App. Pub. No. 2010/0133598 (“Chae”)
1005	U.S. App. Pub. No. 2011/0156132 (“Kiyotoshi”)
1006	U.S. App. Pub. No. 2011/0151667 (“Hwang”)
1007	U.S. Patent No. 7,906,818 (“Pekny”)
1008	Joint Claim Construction and Prehearing Statement (Patent Local Rule 4-3), <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 105 (ND. Cal. August 19, 2024)
1009	Scheduling Order, <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 141 (N.D. Cal. Sept. 18, 2024)
1010	“Shrinking Possibilities” by B. Arnold (2009)
1011	U.S. Patent No. 8,039,176 (“Fujimura”)
1012	“Epitaxial layer characterization and metrology” by V.-M. Airaksinen (2001)
1013	“Chemical Vapor Deposition” by J.-O. Carlsson and P. M. Martin (2010)
1014	“Etch Rates for Micromachining Processing Part II” by K. R. Williams, K. Gupta, and M. Wasilik (2003)
1015	U.S. Patent No. 5,536,360 (“Nguyen”)

Exhibit No.	DESCRIPTION
1016	Counterclaim Plaintiff Micron Technology’s Disclosure of Asserted Claims and Infringement Contentions and Document Production Accompanying Disclosure (Patent Local Rules 3-1 and 3-2), <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL (N.D. Cal.)
1017	U.S. App. Pub. No. 2007/0057328 (“Taniguchi”)
1018	U.S. Patent No. 8,397,132 (“Fukuyama”)

TABLE OF ABBREVIATIONS

Abbreviation	DESCRIPTION
'996	U.S. Patent No. 8,945,996 (Ex. 1001)
'996FH	File History of U.S. Application No. 13/085,083 (Ex. 1002)
IPR	<i>Inter Partes</i> Review
Petitioner	Petitioner
PO	Patent Owner
POSITA	Person of Ordinary Skill in the Art
PTAB	Patent Trial and Appeal Board
USPTO	United States Patent and Trademark Office

LIST OF CHALLENGED CLAIMS

[1.pre] A method of forming circuitry components, comprising:

[1.a] forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

[1.b] forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion; and

[1.c] removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing.

[2] The method of claim 1 wherein the operative and dummy structures comprise the same material.

[3] The method of claim 2 wherein the operative and dummy structures comprise a plurality of the same materials.

[4] The method of claim 3 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

[6] The method of claim 1 wherein the features comprise plates.

[7] The method of claim 1 wherein the operative and dummy structures comprise programmable material.

[8] The method of claim 1 wherein the operative and dummy structures comprise semiconductive material.

[9] The method of claim 8 wherein the semiconductive material of the operative structures comprises interconnected channels of a plurality of vertically oriented transistors.

[10] The method of claim 9 wherein interconnected channels are of vertically oriented charge storage transistors.

[12.pre] A method of forming circuitry components, comprising:

[12.a] forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

[12.b] forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the plates in the end portion;

[12.c] forming horizontally elongated openings through the structures to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into

the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures; and **[12.d]** removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings.

[13] The method of claim 12 wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures.

[16] The method of claim 12 wherein the features comprise plates.

[17.pre] A method of forming circuitry components, comprising:

[17.a] forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

[17.b] forming primary portion openings through the features in the primary portion and forming end portion openings through the features in the in the end portion;

[17.c] forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the end portion openings and forming operative structures therewith within the

primary portion openings and forming dummy structures therewith within the end portion openings;

[17.d] forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures; and

[17.e] removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.

[18] The method of claim 17 comprising forming the primary portion openings and the end portion openings at the same time.

[22] The method of claim 17 comprising forming the primary portion openings and the end portion openings to have at least one of different horizontal cross sections or different vertical cross sections.

[23] The method of claim 17 wherein said at least one of conductive material, semiconductive material, and programmable material is deposited simultaneously into the primary portion openings and the end portion openings.

[24] The method of claim 17 wherein the features comprise plates.

[25.pre] A method of forming an array of memory cells, comprising:

[25.a] forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion, the end portion having sacrificial material-comprising stairs;

[25.b] forming a plurality of first openings into the primary portion of the stack;

[25.c] forming a plurality of second openings into the end portion of the stack;

[25.d] simultaneously forming at least one of conductive material, semiconductive material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and forming dummy structures therewith within the second openings in the end portion;

[25.e] forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings;

[25.f] removing at least a portion of the sacrificial material that is laterally between the horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material;

[25.g] after the removing, forming conductive material into the horizontally elongated openings and the void spaces;

[25.h] removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure; and;

[25.i] forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion.

[26] The method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel regions of a NAND string.

[28] The method of claim 25 comprising forming the first and second openings using the same masking step.

[30] The method of claim 25 wherein the sacrificial material is dielectric.

[32] The method of claim 25 wherein the features comprise plates.

Pursuant to §§311-319 and §42.1,¹ Yangtze Memory Technologies Company, Ltd. (“Petitioner”) petitions for *inter partes* review (“IPR”) of claims 1-4, 6-10, 12-13, 16-18, 22-26, 28, 30, 32 (“Claims”) of U.S. Patent No. 8,945,996 (“’996”), assigned to Micron Technology, Inc. (“PO”). There is a reasonable likelihood—and it is highly likely—that at least one challenged claim is unpatentable as explained herein. Petitioner requests review of the Claims and judgment finding them unpatentable under §§102/103.

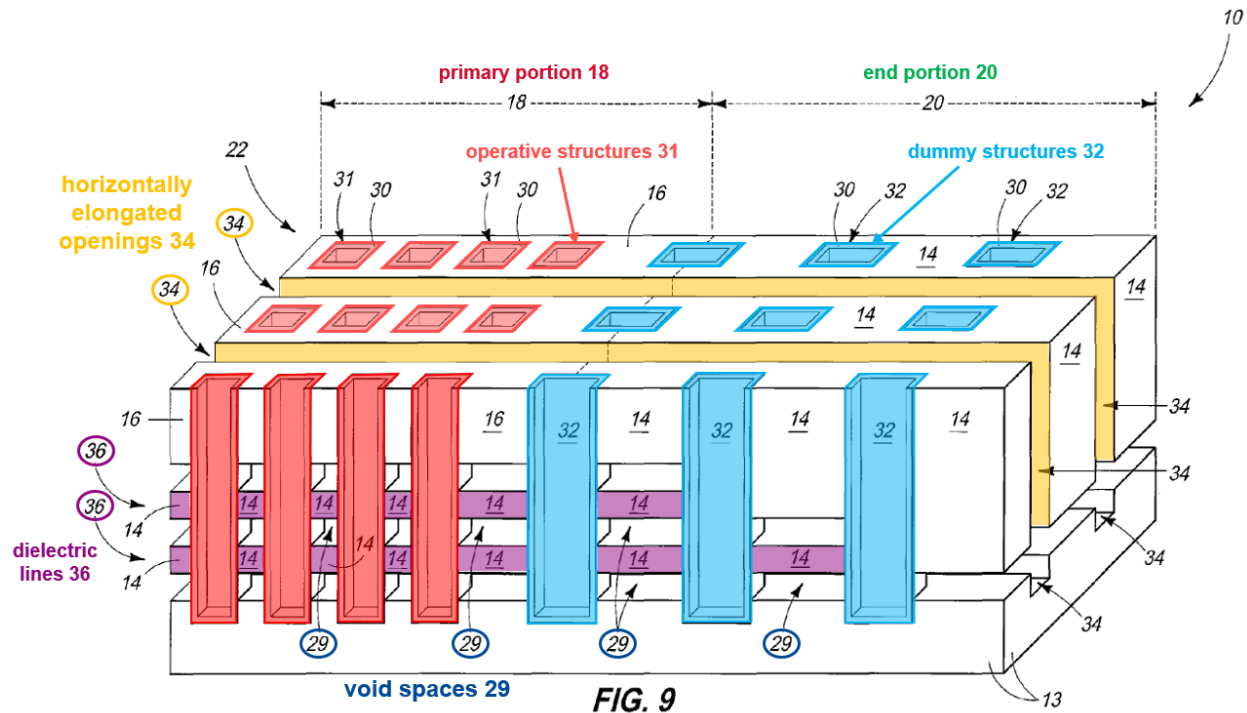
I. INTRODUCTION

The ’996 is generally directed to and claims a method of forming an array of memory cells. ’996, 1:7-10. The method includes forming **operative structures** and **inoperative “dummy” structures** through a **stack of “features,”** such as **dielectric “plates”** in a **primary portion** and an **end portion**, respectively, and removing sacrificial material between the dielectric layers, where the “dummy” structures support the features from vertical movement in the end portion during removal. ’996, 4:37-52, 5:64-6:4; cl. 1. The ’996 also discusses forming

¹ Section cites reference 35 U.S.C. (pre-AIA) or 37 C.F.R. as context indicates. All emphasis/annotations added unless noted. Figure annotations herein generally quote the Claims for reference. Citations herein are exemplary and not meant to be limiting.

“horizontally elongated openings,” which form “horizontally elongated and vertically overlapping lines” from the dielectric material of the “features” “plates.”

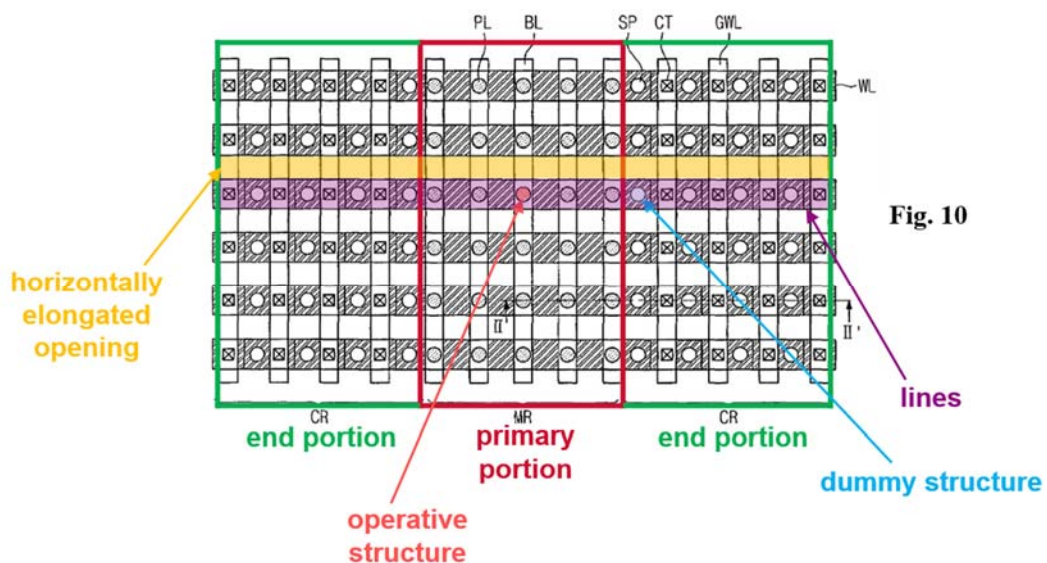
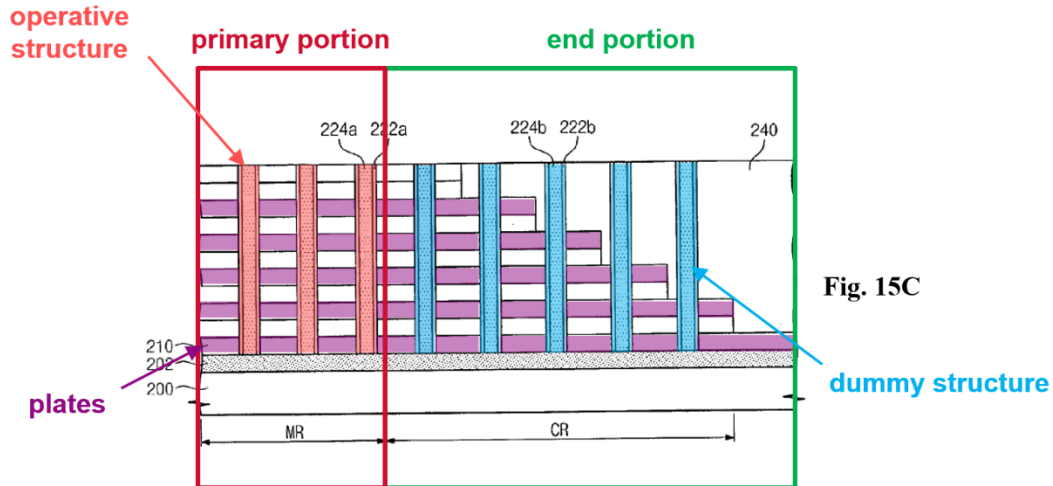
’996, 6:39-43, 6:53-56, cl. 12. Kuhn, ¶47.



’996, Fig. 9.

But these concepts were not new. **Chae** (Ex. 1004) discloses a method of forming a nonvolatile memory device that includes forming **operative “active” structures** and **inoperative dummy “supporter” structures** through a **stack of dielectric layers** in a **primary “memory cell region”** and **end “contact region,”** respectively, and removing certain dielectric layers wherein the inoperative “support” structures can “prevent” the layers “from collapsing or getting near to each other during the removing.” **Chae** also discloses that these “plate-shaped” layers

are then “patterned to form **line-shaped stack structures**,” thereby forming **elongated openings** through the stack. Chae, [0116], [0129]. Kuhn, ¶¶48-49.



Chae, Figures 15C (cross-section view) and 10 (top-down view).

Accordingly, Petitioner requests that the Board institute trial and find the Claims unpatentable.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner is the real party-in-interest. No other parties had access to or control over the present Petition, and no other party funded or participated in preparation of the present Petition.

B. Related Matters

The '996 is the subject of the following co-pending civil action: *Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. et al.*, No. 3:23-cv-05792-RFL, D.I. 105 (ND. Cal.) (“NDCA Case”).

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Petitioner consents to electronic service of documents to the email addresses of the counsel identified above.

III. PAYMENT OF FEES

The undersigned authorizes the Office to charge the fee required by §42.15(a) and any additional fees that might be due to Deposit Account No. 18-1945, under Order No. 118880-0002-663.

IV. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Pursuant to §42.104(a), Petitioner certifies that the '996 is available for IPR. Petitioner and any real parties-in-interest are not barred or estopped from requesting IPR challenging the Claims on the Grounds identified herein.

B. Identification of Challenge

Pursuant to §§42.104(b)-(b)(1), Petitioner requests IPR of the Claims, and that the Board cancel the same as unpatentable.

1. Specific Art on Which the Challenge Is Based

Petitioner relies on the following prior art (Kuhn, ¶¶60-61):

Name	Ex.	Publication	Filed	Prior art under at least
Chae	1004	US2010/0133598	12/3/2009	§102(e)

Kiyotoshi	1005	US2011/0156132	5/20/2010	§102(e)
Hwang	1006	US2011/0151667	12/8/2010	§102(e)
Pekny	1007	US7,906,818	3/13/2008	§102(e)

Each of these references was filed before the earliest possible claimed priority date of the '996 of 4/12/2011, and therefore qualifies as prior art under §102(e).

2. Statutory Grounds on Which the Challenge Is Based²

Ground	Claims	Basis	References
1	1-4, 6-10, 12-13, 16-18, 23-26, 28, 30, 32	§§102/103	Chae
2	1-4, 18, 23, 25-26, 28, 30, 32	§103	Chae in view of Kiyotoshi
3	22		Chae in view of Hwang
4	12-13, 16		Chae in view of Pekny

V. '996 PATENT AND PROSECUTION HISTORY

A. '996

The '996 generally describes a method of forming circuitry components and array of memory cells. '996, 1:7-10. Kuhn, ¶50.

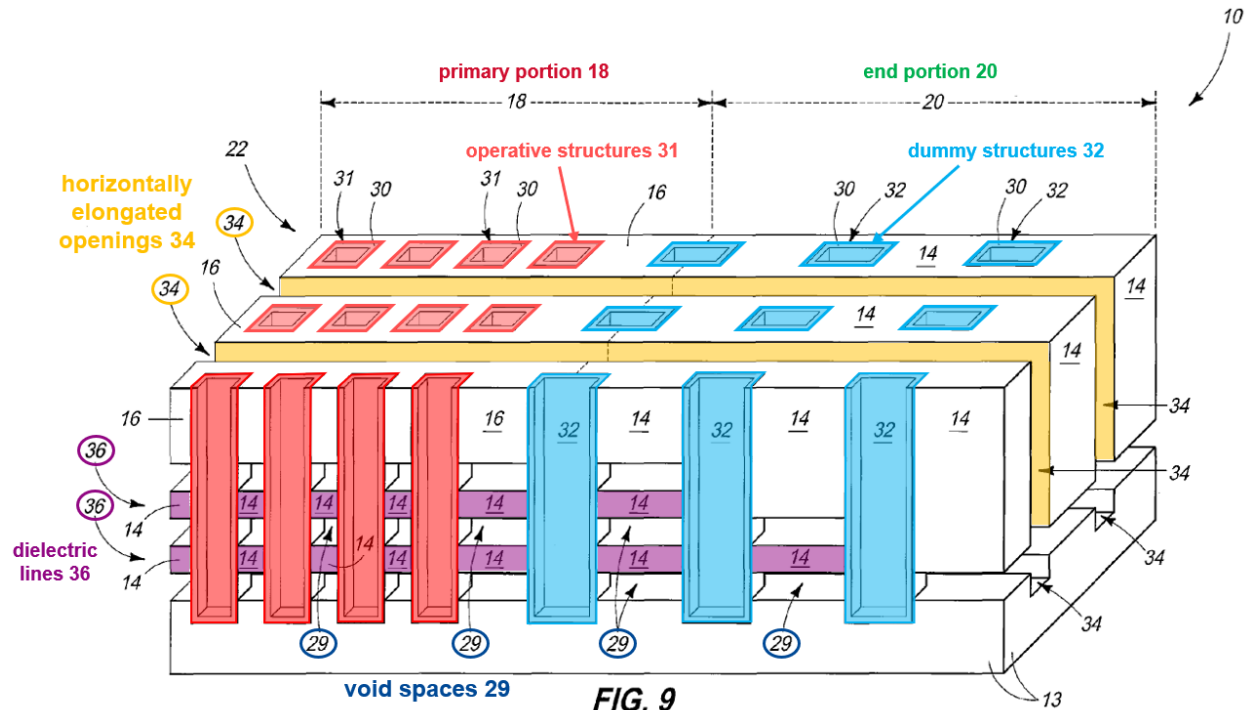
The method includes forming a stack of vertically overlapping “dielectric lines 36” and “sacrificial material 12” horizontally extending across “primary portion 18” and “end portion 20.” '996, 6:39-60. “End portion 20” has a “stair

² See Kuhn, ¶¶62-65.

step-like construction” where the features extend farther in the horizontal direction in the end portion moving deeper into the stack. ’996, 4:28-46. Kuhn, ¶51.

Using a masking process, “primary portion openings” and “end portion openings” are formed in the primary portion and the end portion, respectively. ’996, 5:8-36. **“Operative structures 31”** and **“dummy structures 32”** are formed in the “primary portion openings 25” and “end portion openings 27,” respectively, by depositing “programmable material 30” followed by “conductive material 64.” ’996, 5:40-42, 6:18-23, 8:35-39. Kuhn, ¶52.

The stacked features are patterned with **“horizontally elongated openings 34”** extending from the **“primary portion 18”** into the **“end portion 20”** to expose **sacrificial material 12** and **dielectric lines 36**. ’996, 6:39-60. **Sacrificial material 12** is “removed from being laterally between horizontally elongated openings 34,” resulting in **“void spaces 29”** between **dielectric lines 36**. ’996, 6:57-59. When **“sacrificial material 12”** between the features is removed, **“dummy structures 32”** support the features “from vertical movement in the end portion.” ’996, 7:19-22, 30-35. Subsequently, “vertically spaced horizontal conductive lines 42 within the void spaces” are formed. ’996, 7:39-47. Kuhn, ¶53.



'996, Fig. 9.

B. Prosecution History

There was no substantive prosecution of the '996. Following a restriction requirement, the elected claims were allowed. '996FH, 92-98, 113-118, 141-143. The Examiner's reason for allowance was that the prior art of record did not teach claim limitations [1.b-c], [12.b-d], [17.d-e], and [25.g-i]. '996FH, 115-116. Kuhn, ¶54.

VI. §325(d) AND §314(a) DISCRETION DOES NOT APPLY

A. §325(d)

Under the two-part *Advanced Bionics* framework, the Board should not exercise discretion.

The Grounds raised by this Petition are not the same or substantially the same as the art or arguments raised during '996's prosecution. There were no rejections issued, and **Chae, Kiyotoshi, Hwang, and Pekny** were not considered during prosecution. As explained below, the Claims are anticipated and/or obvious under the identified Grounds, which disclose the [1.b-c], [12.b-d], [17.d-e], and [25.g-i] claim limitations identified in the Notice of Allowance. See §IX.

Even if the art or arguments were substantially the same, the Examiner erred in a manner material to the patentability of the Claims. Because the Examiner did not consider **Chae, Kiyotoshi, Hwang, and Pekny** as prior art, “[i]t is...difficult, if not impossible, to discern exactly why the Examiner allowed the claims of the ['996] patent, or how the Examiner might have considered the arguments presented in the Petition, had they been presented to the Examiner.” *Bowtech, Inc. v. MCP IP, LLP*, IPR2019-00379, Pap. 14, *19-20 (declining to exercise §325(d) discretion where Petitioner did not “even attempt[] to explain how the Examiner erred in any way”); see §IX.

B. §314(a)

The PTAB should not exercise its §314(a) discretion where, as here, trial in the co-pending litigation (NDCA Case) is scheduled for 6/16/2026—after an expected FWD. Ex. 1009.

VII. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this Petition only, Petitioner assumes the Claims are entitled to the 4/12/2011 filing date of Application No. 13/085,083. Kuhn, ¶¶55-56.

A person of ordinary skill in the art (POSITA) at the time of the claimed invention would have had a Bachelor's degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. A higher level of education might make up for less experience, and vice versa. Kuhn, ¶¶57-58.

VIII. CLAIM CONSTRUCTION

Claim terms subject to IPR are construed using *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). 37 C.F.R. §42.100(b). Only terms necessary to resolve the controversy need construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). The only term needing construction is “dummy structure,” which the parties agreed in the NDCA case means “electrically inoperable structure that mimics a physical property of an operative structure.” Ex. 1008. For all other limitations, because the prior art asserted herein discloses embodiments indisputably within the Claims' scope, the Board need not construe the Claims' outer bounds, and all other claim terms should be construed according to their plain and ordinary meaning. Kuhn, ¶59.

IX. GROUNDS OF UNPATENTABILITY

This Petition is supported by the Declaration of Kelin Kuhn, which describes the prior art's scope and content at the time of and well before the '996. *See* Ex. 1003. The prior art renders the Claims unpatentable based on the below Grounds.

A. Ground 1: Chae (Claims 1-4, 6-10, 12-13, 16-18, 23-26, 28, 30, 32)

1. Overview of Chae

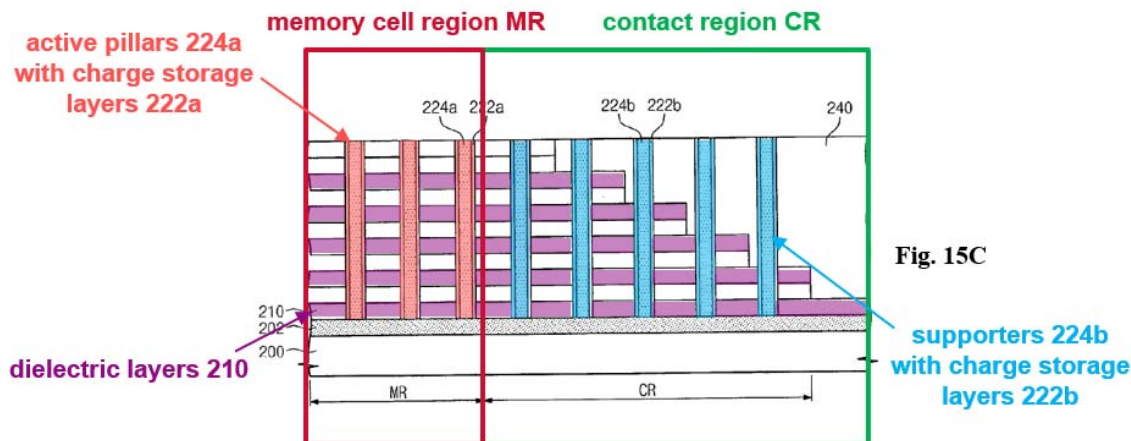
Chae is directed to a “method for manufacturing” “nonvolatile memory devices.” Chae, [0002]. Kuhn, ¶66.

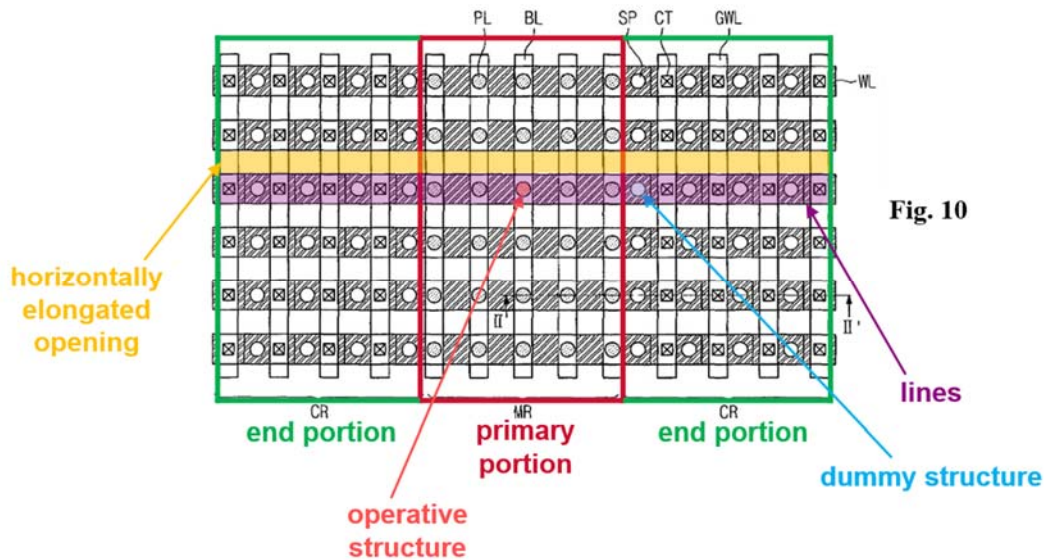
Chae discloses forming a “plate-shaped stack” of “**first and second dielectric layers 210 and 215**” horizontally extending “across a **memory cell region MR** and a **contact region CR**.” Chae, [0123]. The “stack” in the “**contact region CR**” is “patterned in a stair shape” where “the stack height of the first and second dielectric layers 210 and 215 decreases toward the edge.” *Id.*, [0124]. Kuhn, ¶67.

Chae further discloses forming “**channel holes**” and “**dummy holes**” in the “**memory cell region MR**” and “**contact region CR**,” respectively, through “a photolithography process.” Chae, [0127]. “Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the **dummy holes** and the **channel holes**,” and the resulting structure is “filled with semiconductor material to form **active pillars 224a** and **supporters 224b**.” *Id.*, [0128]. The “**supporters**

224b” are electrically inoperable “[b]ecause a conductive pattern such as the global word line 275 or the bit line 270 is not formed on the supporters 224b.” *Id.*, [0134]. Kuhn, ¶68.

The “stack” is then “patterned to form line-shaped stack structures,” thereby forming **horizontally elongated openings** through the stack to “expose[]” the “sidewalls of the **first and second dielectric layers 210 and 215.**” Chae, [0129]. Thereafter, “**second dielectric layers 215**” are removed, resulting in “empty space” “between the **first dielectric layers 210.**” *Id.*, [0129]. The “**first dielectric layers 210** spaced apart from each other may be supported by...the **supporters 224b** of the **contact region CR.**” *Id.*, [0129]. Kuhn, ¶69.





Chae, Figures 15C (cross-section view) and 10 (top-down view).

2. Claim Chart

8,945,996	US 2010/0133598 A1 (“Chae”)
[1.pre] A method of forming circuitry components, comprising:	To the extent the preamble is limiting, Chae discloses a method of forming circuitry components (<i>e.g.</i>, “method for manufacturing” “nonvolatile memory devices”). <u>E.g., Chae:</u> Chae discloses “nonvolatile memory devices and methods for fabricating the same.” Abstract. Kuhn, ¶¶70-73. [0002] (“The present inventive concept relates to <i>nonvolatile memory devices and methods for fabricating the same</i>, and more particularly, to three-dimensional nonvolatile memory devices capable of reducing the resistance of gate electrodes and preventing process defects, and methods for fabricating the same.”) - See also [0007], [0017], [0030]-[0033], [0082]-[0084].
[1.a] forming a stack of horizontally	Chae discloses forming a stack of horizontally extending and vertically overlapping features (<i>e.g.</i>, “first dielectric layers 210...stacked on a semiconductor substrate”), the stack

8,945,996	US 2010/0133598 A1 (“Chae”)
extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;	comprising a primary portion (<i>e.g.</i>, “memory cell region MR”) and an end portion (<i>e.g.</i>, “contact region CR”), at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion (<i>e.g.</i>, “the first and second dielectric layers 210 and 215 stacked on the contact region CR are patterned in a stair shape”). <u>E.g., Chae:</u> Chae discloses forming horizontally extending “first and second dielectric layers 210 and 215” in a vertically stacked layer structure, such that the first dielectric layers 210 form a stack.³ [0123]-[0124], Fig. 15A. Chae further discloses the “stack” comprises a primary portion in a “memory cell region MR” and an end portion in “a contact region CR”. [0123]. Chae also discloses the first dielectric layers 210 form a stair-case structure in contact region CR, in which lower steps of first dielectric layers 210 extend farther into contact region CR than higher steps. [0124], Fig. 15A. Kuhn, ¶¶74-76. • Figure 15A:

³ This is consistent with the ’996 specification, which discloses alternating “dielectric material 14” and “sacrificial material 12” as the “stack” of overlapping features.’996 Patent, 3:65-67, 4:38-46, 6:67-7:5.

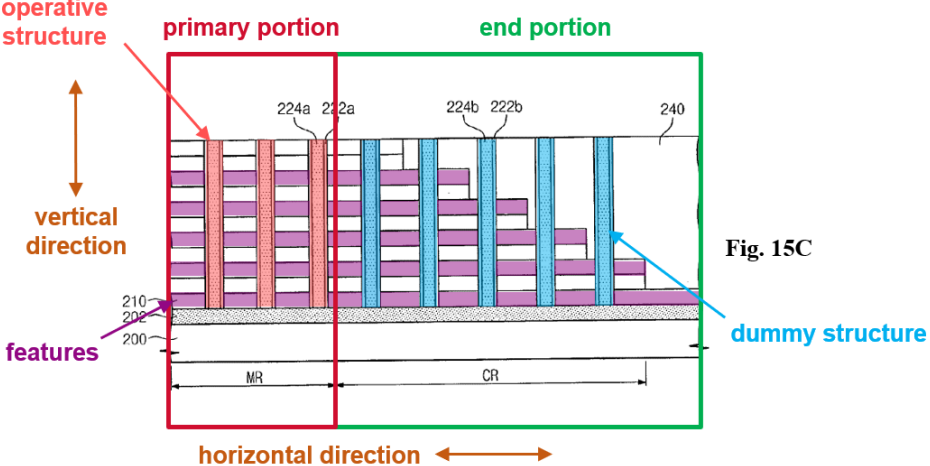
8,945,996	US 2010/0133598 A1 (“Chae”)
	Fig. 15A • [0123] (“Referring to FIG. 15A, first and second dielectric layers 210 and 215 with different etch selectivity are alternately stacked on a semiconductor substrate 200, and a plate-shaped stack structure is formed across a memory cell region MR and a contact region CR. That is, the sidewalls of the stacked first and second dielectric layers 210 and 215 are aligned.”) • [0124] (“In the plate-shaped stack structure, the first and second dielectric layers 210 and 215 stacked on the contact region CR are patterned in a stair shape. That is, on the contact region CR, the stack height of the first and second dielectric layers 210 and 215 decreases toward the edge.”)
[1.b] forming operative structures vertically through the features in the primary portion and forming dummy	Chae discloses forming operative structures (e.g., collectively, “charge storage layers 222a” and “active pillars 224a”) vertically through the features (e.g., through “first dielectric layers 210”) in the primary portion (see [1.a]) and forming dummy structures (e.g., collectively, “charge storage layers 222b” and “supporters 224b”) vertically through the features (e.g., through “first dielectric layers 210”) in the end portion (see [1.a]). <u>E.g., Chae:</u>

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structures vertically through the features in the end portion; and	See [1.a]. Chae further discloses forming “active pillars 224a of the memory cell region MR” such that they “penetrate all of the stacked first and second dielectric layers 210 and 215,” and forming “charge storage layers 222a...around...active pillars 224.” [0128]. Charge storage layers 222a and active pillars 224a are parts of memory cells, and are thus operative structures. Chae further discloses forming “supporters 224b of the contact region CR” such that they “penetrate some of the stacked first and second dielectric layers 210 and 215,” and forming “charge storage layers 224b...around the supporters 224b.” [0128]. Kuhn, ¶¶77-80. Charge storage layers 222b and supporters 224b collectively form dummy structures under the construction “electrically inoperable structure that mimics a physical property of an operative structure.” Ex. 1008 at 2. First, charge storage layers 222b and supporters 224b are not electrically connected to other components “[b]ecause a conductive pattern such as the global word line 275 or the bit line 270 is not formed on the supporters 224b,” and supporters 224b do not “affect the operation of the nonvolatile memory device,” and are thus electrically inoperable. [0134]. Second, they mimic a physical property of the operative structures because they are formed of identical (or at least similar) materials in the same process as charge storage layers 222a and active pillars 224a. [0128], [0037] (explaining that “similar reference numerals refer to like elements”). Kuhn, ¶81. • Figure 15B:

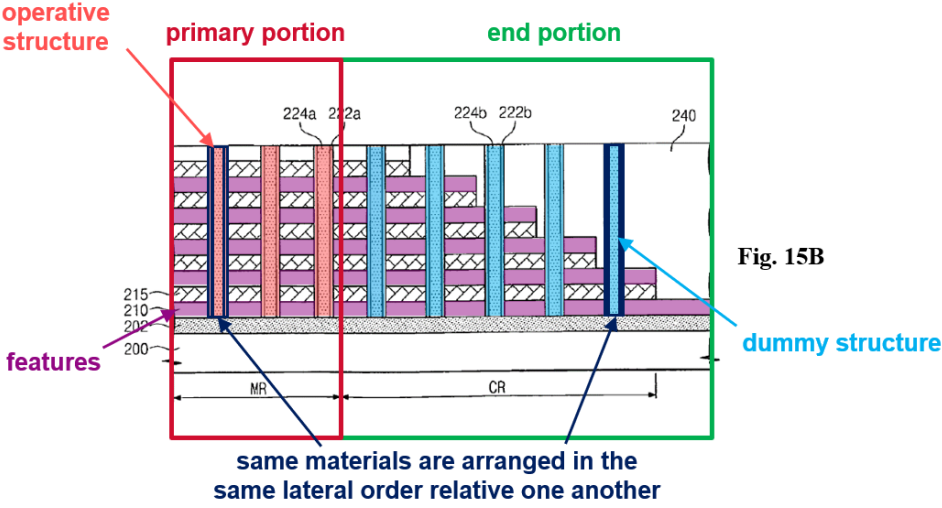
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	Fig. 15B [0126] (“Referring to FIG. 15B, active pillars 224a are formed in the memory cell region MR and supporters 224b are formed in the contact region CR.”) [0128] (“Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b. That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the contact region CR and the active pillars 224a of the memory cell region MR. Also, the active pillars 224a and the supporters 224b may be formed to the same length. The active pillars 224a of the memory cell region MR may penetrate all of the stacked first and second dielectric layers 210 and 215, and the supporters 224b of the contact region CR may penetrate some of the stacked first and second dielectric layers 210 and 215.”)
[1.c] removing at least some sacrificial material that is elevationally	Chae discloses removing at least some sacrificial material (e.g., “remove the second dielectric layers 215”) that is elevationally between material of the features (e.g., between “first dielectric layers 210” as illustrated in Fig. 15A-15B) in the primary and end portions (see [1.a]), wherein the dummy structures support material of the features from vertical movement in the end portion during said removing (e.g., “first

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between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing.	dielectric layers 210 spaced apart from each other...supported by...supporters 224b of the contact region CR” to prevent “collapsing”). <u>E.g., Chae:</u> See [1.a]-[1.b]. Chae further discloses “first and second dielectric layers 210 and 215...are alternately stacked” “across a memory cell region MR and a contact region CR” and that by supplying “an etchant between the...stack structure,” “second dielectric layers 215” is removed. [0123], [0129]. Chae further discloses that “first dielectric layers 210...may be supported by...the supporters 224b of the contact region CR” such that layers are “prevented from collapsing or getting near each other.” [0129].⁴ This support is illustrated in Figure 15C, in which first dielectric layers 210 are separated from each other, but do not collapse despite the lack of an intervening structure after layers second dielectric layers 215 are removed. Kuhn, ¶¶84-85. Because charge storage layers 222b are formed on the sides of supporters 224b, the combination works together to support first dielectric layers 210. Kuhn, ¶¶82-85. • Figure 15C:

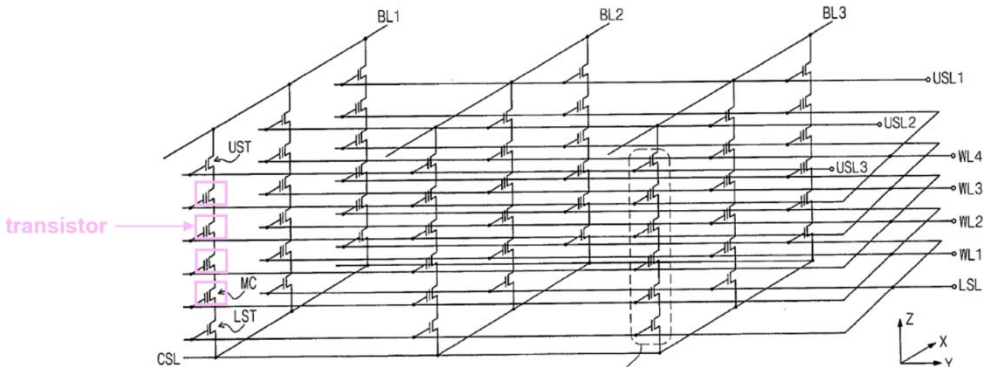
⁴ Chae states: “the second dielectric layers 215 can be prevented from collapsing or getting near to each other during the removing of the *second dielectric layers 215* through a wet etch process.” [0129]. The first reference to “dielectric layers 215” being prevented from collapsing is a typographical error, and instead, first dielectric layer 210 is the layer prevented from collapsing—as Fig. 15C illustrates the dielectric layers 210 remain after layers 215 are removed and the first dielectric layers 210 do not collapse, despite the lack of structure between them. Kuhn, ¶85.

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	 Fig. 15C [0129] (“Referring to FIG. 15C, the plate-shaped stack structure including the active pillars 224a and the supporters 224b are patterned to form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and 215 may be exposed. <i>Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.</i> Accordingly, an empty space is formed between the first dielectric layers 210 that are perpendicular to the semiconductor substrate 200 and are spaced apart from each other. <i>The first dielectric layers 210 spaced apart from each other may be supported by the active pillars 224a of the memory cell region MR, which are perpendicular to the semiconductor substrate 200, and the supporters 224b of the contact region CR. That is, the second dielectric layers 215 can be prevented from collapsing or getting near to each other during the removing of the second dielectric layers 215 through a wet etch process.</i>”)
[2] The method of claim 1 wherein the	See [1]. Chae discloses the operative (e.g., “active pillars 224a” with “charge storage layers 222a”) and dummy structures (e.g.,

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operative and dummy structures comprise the same material.	“supporters 224b” with “charge storage layers...222b”) comprise the same material (“e.g., “semiconductor material” and “charge storage” material). <u>E.g., Chae:</u> See [1.b]. Chae further discloses “charge storage layers 222a and 222b” and “active pillars 224a and supporters 224b” are formed in the same respective processes, and thus the resulting structures comprise the same material. [0128]. Kuhn, ¶¶86-89. • [0128] (“<i>Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.</i>”)
[3] The method of claim 2 wherein the operative and dummy structures comprise a plurality of the same materials.	See [2]. Chae discloses the operative and dummy structures (see [2]) comprise a plurality of the same materials (e.g., each comprises “semiconductor material” and “charge storage” material). <u>E.g., Chae:</u> As discussed in [2], Chae discloses that “charge storage layers 222a and 222b” and “active pillars 224a and supporters 224b” are formed in the same respective processes, and thus comprise a plurality of the same materials (“semiconductor material” and “charge storage” material). Kuhn, ¶¶90-92.
[4] The method of claim 3 wherein the same materials are arranged in the same	See [3]. Chae discloses the same materials (e.g., collectively, “semiconductor material” and “charge storage” material) are arranged in the same lateral order relative one another in the operative and dummy structures (see [3]). <u>E.g., Chae:</u>

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lateral order relative one another in the operative and dummy structures.	As discussed in [2]-[3], Chae discloses that “charge storage layers 222a and 222b” and “active pillars 224a and supporters 224b” are formed in the same respective processes, and thus comprise a plurality of the same materials (“semiconductor material” and “charge storage” material) arranged in the same lateral order relative to one another. Kuhn, ¶¶93-95. Figure 15B:  same materials are arranged in the same lateral order relative one another
[6] The method of claim 1 wherein the features comprise plates.	See [1]. Chae discloses the features (e.g., “first dielectric layers 210”) comprise plates (e.g., “plate-shaped”). <u>E.g., Chae:</u> See [1.a]. Chae further discloses “first dielectric layers 210” are “plate-shaped.” [0123]-[0125]. Kuhn, ¶¶96-98. [0123] (“Referring to FIG. 15A, <i>first and second dielectric layers 210 and 215 with different etch selectivity are alternately stacked on a semiconductor substrate 200, and a plate-shaped stack structure is formed</i> across a memory cell region MR and a contact region CR.”) - See also [0124]-[0125].

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[7] The method of claim 1 wherein the operative and dummy structures comprise programmable material.	See [1]. Chae discloses the operative and dummy structures (see [2]) comprise programmable material (e.g., “charge storage layer”). <u>E.g., Chae:</u> As explained in [1.b], Chae discloses the operative and dummy structures comprise “semiconductor material” with sidewalls of “charge storage layers 222a and 222b.” [0128]. A charge storage layer surrounding semiconductor material comprises programmable material, as charge stored in the charge storage layer changes the threshold voltage that must be applied to the corresponding gate electrode 250 to allow current flow through the semiconductor material, indicating the storage of information (i.e., programming). Kuhn, ¶¶99-101.
[8] The method of claim 1 wherein the operative and dummy structures comprise semiconductive material.	See [1]. Chae discloses the operative and dummy structures (see [2]) comprise semiconductive material (e.g., “semiconductor material”). See [1.b]. As discussed in [2], Chae discloses active pillars 224a and supporters 224b comprise semiconductor material. Kuhn, ¶¶102-104.
[9] The method of claim 8 wherein the semiconductive material of the operative structures comprises interconnected channels of a	See [8]. Chae discloses the semiconductive material of the operative structures (see [8]) comprises interconnected channels (e.g., “active pillars 224a”) of a plurality of vertically oriented transistors (e.g., “memory cell transistors MC”). <u>E.g., Chae:</u> Chae discloses “active pillars PL,” which “are formed of semiconductor material,” “are provided for the channels of

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plurality of vertically oriented transistors.	transistors.” [0054]. Chae also discloses that “upper and lower select transistors UST and LST, and memory cell transistors MC” connected in series form a “string STR.” [0043], Fig. 1. These “strings STR are configured in such a way that the memory cells MC are connected in series in a Z-axis direction perpendicular to an XY plane,” i.e., the transistors (“MC”) are vertically oriented. [0045], Fig. 1. Chae also discloses that the channels of these vertically oriented transistors are “electrically connected through the active pillars PL,” which form channels. [0054]. Figure 1 and related paragraphs [0041]-[0057] apply to “exemplary embodiments of the inventive concept” ([0041]) and a POSITA would have understood that descriptions of “active pillars PL” in [0054] apply to “active pillars 224a” in the “fifth exemplary embodiment of the inventive concept,” which is the embodiment Petitioner relies upon for [1] to [8]. [0121]. Kuhn, ¶¶105-107. - Fig. 1:  Fig. 1 [0042] (“Referring to FIG. 1, a nonvolatile memory device according to exemplary embodiments of the inventive concept includes a cell array including a plurality of strings STR. The cell array includes bit lines BL1~BL3, word lines WL1~WL4, upper and lower select lines USL1~USL3 and LSL, and a common source line CSL. The strings STR are provided between the common source line CSL and the bit lines BL1~BL3.”) [0043] (“Each string STR includes upper and lower select transistors UST and LST, and memory cell transistors

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	<i>MC that are connected in series between the upper and lower select transistors UST and LST. The drains of the upper select transistors UST are connected to the bit lines BL1~BL3, and the sources of the lower select transistors LST are connected in common to the common source line CSL.”)</i> • [0044] (“The upper select transistors UST are connected to the upper select lines USL1~USL3, and the lower select transistors LST are connected respectively to the lower select lines LSL. The memory cells MC are connected respectively to the word lines WL1~WL4.”) • [0045] (“<i>The cell array has a three-dimensional structure. That is, the strings STR are configured in such a way that the memory cells MC are connected in series in a Z-axis direction perpendicular to an XY plane parallel to the top surface of a semiconductor substrate. Accordingly, the channel of the memory cell transistors MC and the select transistors UST and LST may be formed perpendicular to the XY plane.</i>”) • [0054] (“The active pillars PL are formed of semiconductor material....<i>The active pillars PL are provided for the channels of transistors, which correspond to the strings of the nonvolatile memory device according to the embodiments of the inventive concept. That is, the channels of memory cell transistors and select transistors (LST, UST and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.</i>”) • [0041] (“<i>FIG. 1 is a circuit diagram of a nonvolatile memory device according to exemplary embodiments of the inventive concept.</i>”) • [0121] (“Another method for fabricating <i>the nonvolatile memory devices according to the second and fifth exemplary embodiments of the inventive concept will be described below with reference to FIGS. 15A to 15E.</i>”) • See also [0004]-[0005].

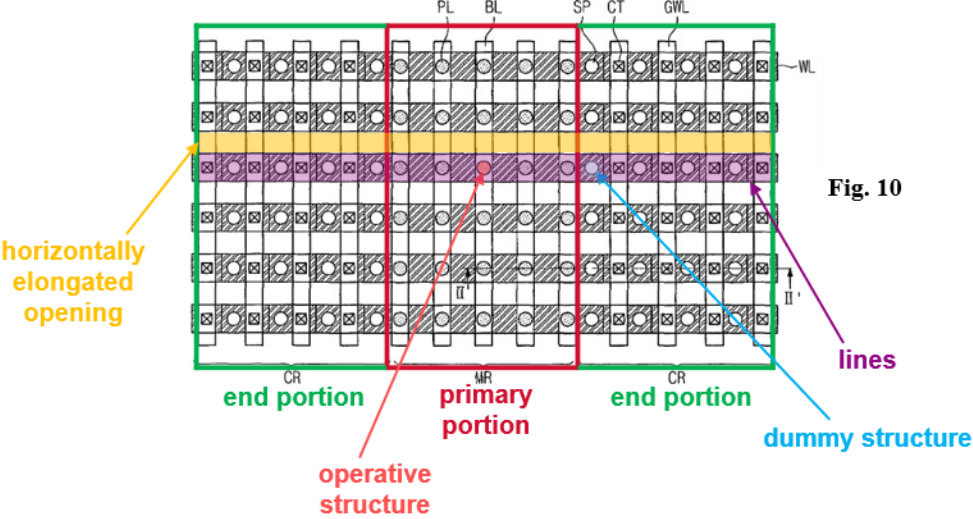
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[10] The method of claim 9 wherein interconnected channels are of vertically oriented charge storage transistors.	<i>See</i> [9]. Chae discloses that interconnected channels (<i>e.g.</i>, “active pillars 224a”) are of vertically oriented charge storage transistors (<i>e.g.</i>, “memory cell transistors MC”). <u>E.g., Chae:</u> <i>See</i> [9]. As discussed in [9], the “semiconductor material” of Chae’s “active pillars” comprises interconnected channels of a plurality of vertically oriented transistors. Chae further discloses that “charge storage layers 222a...may be formed around...the active pillars 224a.” [0055]. As explained in [7], the charge storage layers are programmable. Therefore, Chae’s vertically oriented transistors are vertically oriented charge storage transistors. [0128] (“<i>That is, charge storage layers 222a and 222b may be formed around</i> the supporters 224b of the contact region CR and <i>the active pillars 224a of the memory cell region MR.</i>”). Kuhn, ¶¶108-110.
[12.pre] A method of forming circuitry components, comprising:	<i>See</i> [1.pre]. Kuhn, ¶111.
[12.a] forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at	<i>See</i> [1.a]. Kuhn, ¶112.

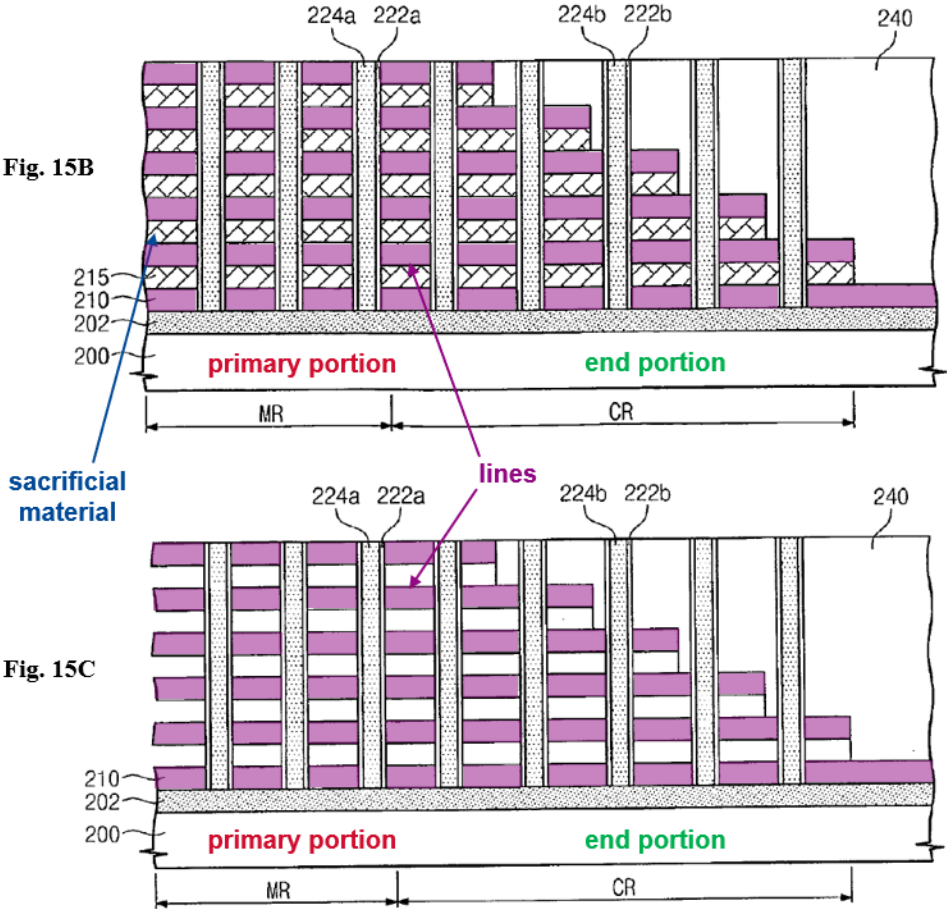
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least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;	
[12.b] forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the plates in the end portion;	See [1.b]. As explained in [6], the “first dielectric layers 210” are plates. Kuhn, ¶113.
[12.c] forming horizontally elongated openings through the structures to form horizontally	Chae discloses forming horizontally elongated openings (<i>e.g.</i> , openings illustrated in Fig. 10) through the structures (<i>e.g.</i> , between the “active pillars 224a” with “charge storage layers” and “supporters 224b” with “charge storage layers 222b”; <i>see</i> [2]) to form horizontally elongated and vertically overlapping lines (<i>e.g.</i> , “line-shaped stack structures”) from material of the features (<i>e.g.</i> , “first dielectric layers 210”), the lines individually extending from the primary portion (<i>e.g.</i> ,

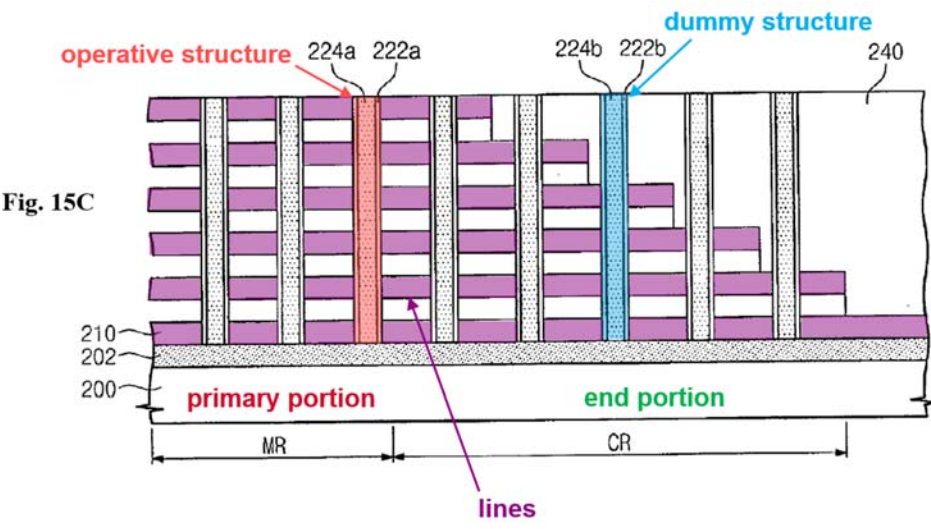
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elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures; and	“memory cell region MR”) and into the end portion (<i>e.g.</i>, “contact region CR”) and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures (<i>see</i> [2]). <u>E.g., Chae:</u> <i>See</i> [1.a]-[1.b], [2]. Chae further discloses forming “line-shaped stack structures” by patterning the “plate-shaped stack structures,” thereby opening trenches through the “active pillars 224a” with “charge storage layers 222a” and “supporters 224b” with “charge storage layers 222b,” as shown in Fig. 10. [0129].⁵ These lines are vertically overlapping because they are “stacked.” [0129]. As illustrated in Fig. 10, the “line-shaped stack structures” extend across the cell region MR and contact region CR. [0123], Fig. 10. Chae also discloses that by opening the trenches, “the sidewalls of the first and second dielectric layers 210 and 215 may be exposed” such that the lines extend laterally about the “active pillars 224a” and “supporters 224b,” which vertically extend through the lines. [0129], Figs. 10, 15C. Moreover, the trenches are formed “through” the structures in the same way PO asserts openings pass through structures in its infringement contentions in the NDCA Case, i.e., the openings pass between the alleged structures. Ex. 1016, Ex. B-2 at 20-23. Kuhn, ¶¶114-117. • Figure 10:

⁵ The ’996 Patent discloses forming horizontally elongated openings amongst operative and dummy structures, not directly through individual such structures. ’996 Patent, Figs. 5-11, 12-13, 15-17. However, the term “through” as used in the specification consistently refers to structures passing directly through other structures.

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	- Figure 15C: [0123] ("Referring to FIG. 15A, first and second dielectric layers 210 and 215 with different etch selectivity are alternately stacked on a semiconductor substrate 200, and a plate-shaped stack structure is formed across a memory cell region MR and a contact region CR.") [0129] ("Referring to FIG. 15C, the plate-shaped stack structure including the active pillars 224a and the supporters 224b are patterned to form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric

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	<i>layers 210 and 215 may be exposed.</i> Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.”)
[12.d] removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings.	Chae discloses removing at least some sacrificial material (e.g., removing “second dielectric layers 215”) that is elevationally between the lines (e.g., between the “first dielectric layers 210” of “line-shaped stack structures”) in the primary and end portions (see [1.a]) laterally between the openings (e.g., slots illustrated in Fig. 10). <u>E.g., Chae:</u> See [1.a], [12.c]. Chae further discloses removing portions of “second dielectric layers 215” elevationally between the “line-shaped” “stacked first dielectric layers 210,” which are laterally between the slots, as illustrated in Fig. 10. [0129]. “[S]econd dielectric layers 215” are sacrificial because they are not included in the final product, but are instead removed and replaced with “line-shaped gate electrodes 250”—see Fig. 15C. [0129]. Kuhn, ¶¶118-120. Figure 10:  Fig. 10

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	- Figures 15B, 15C:  [0129] ("Referring to FIG. 15C, the plate-shaped stack structure including the active pillars 224a and the supporters 224b are patterned to form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and 215 may be exposed. Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.")
[13] The method of claim 12	See [12]. Chae discloses the removing comprises etching of the sacrificial material (e.g., "etch[ing]" "second dielectric layers

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wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures.	215”) selectively (e.g., with “different etch selectivity”) relative to material of the lines (e.g., relative to “first dielectric layers 210” of “line-shaped stack structures”), the operative structures (see [2]), and the dummy structures (see [2]). <u>E.g., Chae:</u> See [2], [12.d]. Chae discloses removing the second dielectric layers 215 using an etchant with “high selectivity with respect to the first dielectric layer 210” forming the “line-shaped stack structures.” [0129]. Moreover, the etching is also selective relative to the charge storage layers 222a and 222b (i.e., operative and dummy structures) because those structures remain after the etching process, as shown in Fig. 15C. [0129]. Kuhn, ¶¶121-124. - Figure 15C:  Fig. 15C [0129] (“When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and 215 may be exposed. Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.”) - See also [0138], [0143]

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[16] The method of claim 12 wherein the features comprise plates.	See [6]. Kuhn, ¶125.
[17.pre] A method of forming circuitry components, comprising:	See [1.pre]. Kuhn, ¶126.
[17.a] forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving	See [1.a]. Kuhn, ¶127.

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deeper into the stack in the end portion;	
[17.b] forming primary portion openings through the features in the primary portion and forming end portion openings through the features in the in the end portion;	Chae discloses forming primary portion openings (e.g., “channel holes”) through the features (e.g., “first dielectric layers 210”) in the primary portion (e.g., “memory cell region MR”) and forming end portion openings (e.g., “dummy holes”) through the features in the in the end portion (e.g., “contact region CR”). <u>E.g., Chae:</u> See [1.a]. Chae further discloses “channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR,” and these holes “penetrate” dielectric layers 210. [0127]-[0128]. Kuhn, ¶¶128-131. • [0127] (“More specifically, <i>channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR....The dummy hole adjacent to the channel hole may penetrate all of the stacked first and second dielectric layers 210 and 215. Also, the number of the penetrated first and second dielectric layers 210 and 215 may decrease with an increase in the distance from the memory cell region MR.</i>”) • [0128] (“Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b. That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the contact region CR and the active pillars 224a of the memory cell region MR. Also, the active pillars 224a and the supporters 224b may be formed to the same length. <i>The active pillars 224a of the memory cell region MR may penetrate all of the stacked first and second dielectric</i>

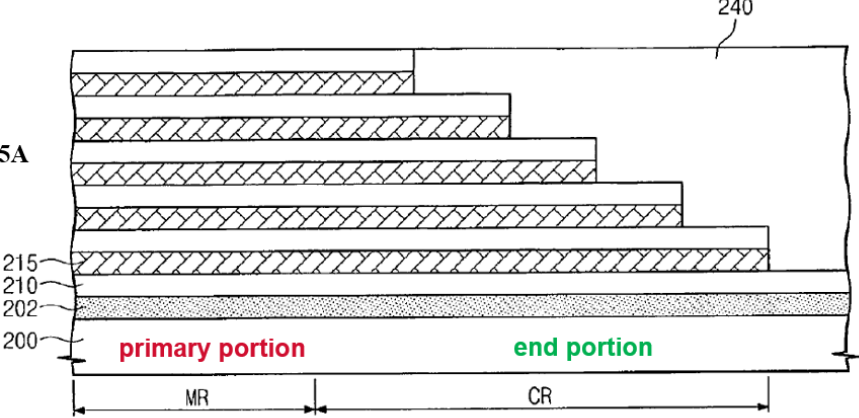
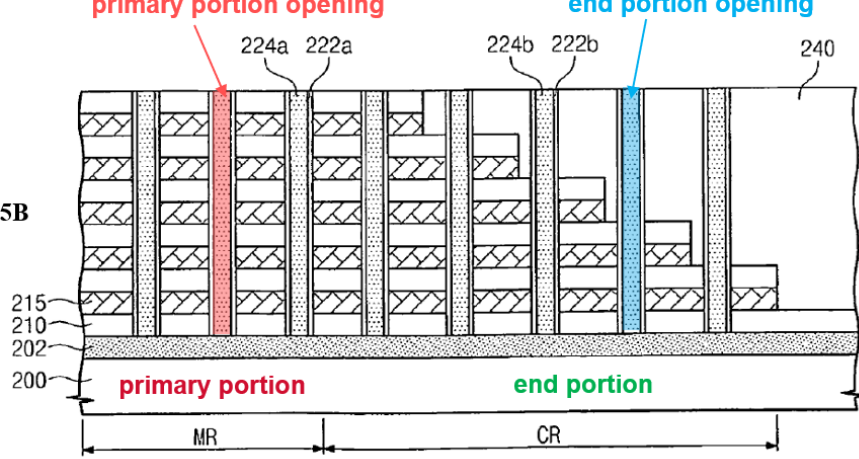
8,945,996	US 2010/0133598 A1 (“Chae”)
	<i>layers 210 and 215, and the supporters 224b of the contact region CR may penetrate some of the stacked first and second dielectric layers 210 and 215.”)</i>
[17.c] forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the end portion openings and forming operative structures therewith within the primary portion openings and forming dummy structures therewith within the end portion openings;	Chae discloses forming at least one of...semiconductive material (e.g., “semiconductor material”), and programmable material (e.g., “charge storage layer”; see [7]) in the primary portion openings (e.g., “channel holes”) and the end portion openings (e.g., “dummy holes”) and forming operative structures therewith within the primary portion openings (e.g., collectively, “charge storage layers 222a” and “active pillars 224a” in “channel holes”) and forming dummy structures therewith within the end portion openings (e.g., collectively, “charge storage layers 222b” and “supporters 224b” in “dummy holes”). <u>E.g., Chae:</u> See [1.b]. Chae further discloses “charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes,” which are then “filled with semiconductor material to form active pillars 224a and supporters 224b,” respectively. [0128]. Chae’s “charge storage layers 222a” and “active pillars 224a” collectively constitute operative structures in “channel holes” and “charge storage layers 222b” and “supporters 224b” collectively constitute dummy structures in “dummy holes.” Both “active pillars 224a” and “supporters 224b” comprise “semiconductor material.” [0128]. Furthermore, as discussed in [7], charge storage layers 222a and 222b comprise programmable material. Kuhn, ¶¶132-135. • [0128] (“Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b. That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the contact region CR and the active pillars 224a of the memory cell region MR. Also, the active

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	pillars 224a and the supporters 224b may be formed to the same length. The active pillars 224a of the memory cell region MR may penetrate all of the stacked first and second dielectric layers 210 and 215, and the supporters 224b of the contact region CR may penetrate some of the stacked first and second dielectric layers 210 and 215.”)
[17.d] forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures; and	See [12.c]. Kuhn, ¶136.

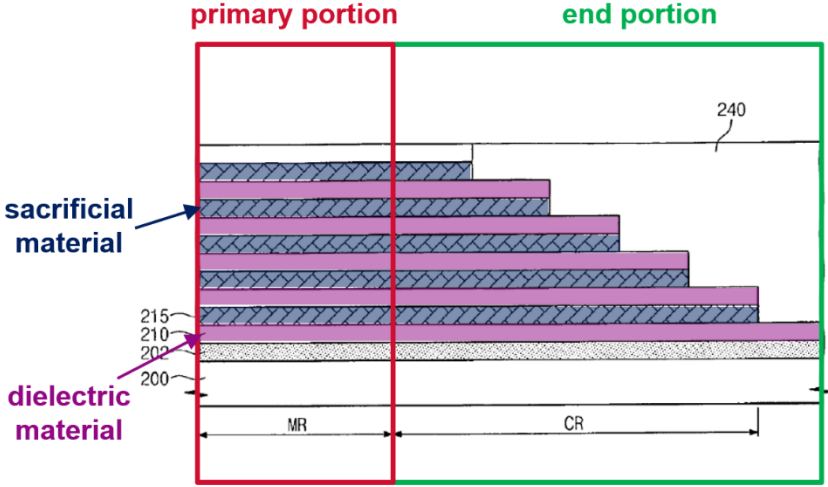
8,945,996	US 2010/0133598 A1 (“Chae”)
[17.e] removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.	See [12.d] and [13]. Kuhn, ¶137.
[18] The method of claim 17 comprising forming the primary portion openings and the end portion openings at the same time.	See [17]. Chae discloses forming the primary portion openings (e.g., “channel holes”) and the end portion openings (e.g., “dummy holes”) at the same time (e.g., “through a photolithography process”). <u>E.g., Chae:</u> See [17.b]. Chae further discloses “channel holes and the dummy holes may be formed through a photolithography process.” [0127]. A POSITA would have understood (or at least found it obvious) that forming the “channel holes” and “dummy holes” using the same “photolithography process” would be

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	advantageously performed at the same time, thereby minimizing the number of processing steps required. Kuhn, ¶¶138-141. - Figures 15A, 15B: [0127] (“More specifically, channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR. The channel holes and the dummy holes may be formed through a photolithography process, and the channel holes may be formed in a matrix configuration on the plane....”)
[23] The method of claim 17 wherein said at least one of	See [17]. Chae discloses that at least one of...semiconductive material, and programmable material (see [17.c]) is deposited simultaneously into the primary portion openings (e.g.,

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conductive material, semiconductor material, and programmable material is deposited simultaneously into the primary portion openings and the end portion openings.	“channel holes”) and the end portion openings (e.g., “dummy holes”). <u>E.g., Chae:</u> See [17.c]. Chae further discloses “charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes,” and “the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.” [0128]. A POSITA would have understood (or at least found it obvious) the “dummy holes” and the “channel holes” are “filled with semiconductor material” simultaneously, and programmable material (“charge storage layers”) are formed in the “dummy holes” and the “channel holes” simultaneously to advantageously reduce the number of processing steps. Kuhn, ¶¶142-145. • Figures 15A, 15B:

8,945,996	US 2010/0133598 A1 (“Chae”)
	Fig. 15A  Fig. 15B  [0128] (“<i>Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.</i> That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the contact region CR and the active pillars 224a of the memory cell region MR. Also, the active pillars 224a and the supporters 224b may be formed to the same length. The active pillars 224a of the memory cell region MR may penetrate all of the stacked first and second dielectric layers 210 and 215, and the supporters 224b of the contact region CR may penetrate some of the stacked first and second dielectric layers 210 and 215.”)

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[24] The method of claim 17 wherein the features comprise plates.	See [6], [17]. Kuhn, ¶146.
[25.pre] A method of forming an array of memory cells, comprising:	To the extent the preamble is limiting, Chae discloses a method of forming (<i>e.g.</i>, “method for manufacturing,” <i>see</i> [1.pre]) an array of memory cells (<i>e.g.</i>, “cell array”). <u>E.g., Chae:</u> <i>See</i> [1.pre]. Chae further discloses that its “nonvolatile memory device...includes a cell array.” [0042]. Kuhn, ¶¶147-149. • [0042] (“Referring to FIG. 1, a nonvolatile memory device according to exemplary embodiments of the inventive concept includes a cell array including a plurality of strings STR. The cell array includes bit lines BL1~BL3, word lines WL1~WL4, upper and lower select lines USL1~USL3 and LSL, and a common source line CSL.”)
[25.a] forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion, the end portion having sacrificial	Chae discloses forming a stack of alternating (<i>e.g.</i>, “alternately stacked”) dielectric material (<i>e.g.</i>, “first dielectric layer 210”) and sacrificial material (<i>e.g.</i>, “second dielectric layer 215”), the stack comprising a primary portion (<i>e.g.</i>, “memory cell region MR”) and an end portion (<i>e.g.</i>, “contact region CR”), the end portion having sacrificial material-comprising stairs (<i>e.g.</i>, “patterned in a stair shape”). <u>E.g., Chae:</u> Chae discloses forming “first and second dielectric layers 210 and 215” that are “alternately stacked.” [0123]-[0124], Fig. 15A. A POSITA would have understood “second dielectric layers 215” are sacrificial because they are not included in the final product, but are instead removed and replaced with “line-shaped gate

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material-comprising stairs;	electrodes 250.” [0129]-[0130]. Chae further discloses the “stack” comprises a primary portion in a “memory cell region MR” and an end portion in “a contact region CR”. [0123]. Chae also discloses “the first and second dielectric layers 210 and 215” in “the contact region CR” have “a stair shape.” [0124]. Kuhn, ¶¶150-152. - Figure 15A:  Fig. 15A [0123] (“Referring to FIG. 15A, first and second dielectric layers 210 and 215 with different etch selectivity are alternately stacked on a semiconductor substrate 200, and a plate-shaped stack structure is formed across a memory cell region MR and a contact region CR. That is, the sidewalls of the stacked first and second dielectric layers 210 and 215 are aligned.”) [0124] (“In the plate-shaped stack structure, the first and second dielectric layers 210 and 215 stacked on the contact region CR are patterned in a stair shape. That is, on the contact region CR, the stack height of the first and second dielectric layers 210 and 215 decreases toward the edge.”) [0129] (“Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to

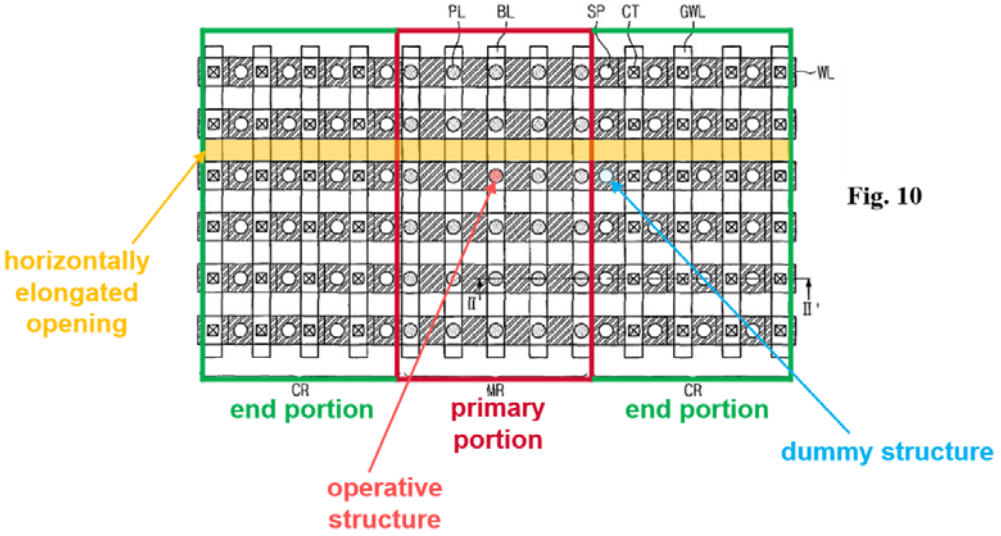
8,945,996	US 2010/0133598 A1 (“Chae”)
	<i>remove the second dielectric layers 215.</i> Accordingly, an empty space is formed between the first dielectric layers 210 that are perpendicular to the semiconductor substrate 200 and are spaced apart from each other.”) • [0130] (“Referring to FIG. 15D, <i>the space between the first dielectric layers 210</i> may be filled with conductive material to <i>form line-shaped gate electrodes 250.</i>”)
[25.b] forming a plurality of first openings into the primary portion of the stack; [25.c] forming a plurality of second openings into the end portion of the stack;	Chae discloses forming a plurality of first openings (e.g., “channel holes”) into the primary portion (e.g., “memory cell region MR”) of the stack (e.g., “stack structure”) and forming a plurality of second openings (e.g., “dummy holes”) into the end portion (e.g., “contact region CR”) of the stack (e.g., “stack structure”). <u>E.g., Chae:</u> See [17.b]. Chae further discloses “channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR, and that these holes “penetrate” “the stacked first and second dielectric layers 210 and 215.” [0127]-[0128]. Kuhn, ¶¶153-156. • [0127] (“More specifically, <i>channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR.</i> The channel holes and the dummy holes may be formed through a photolithography process, and the channel holes may be formed in a matrix configuration on the plane. Also, as illustrated in FIG. 5, the dummy holes may be formed respectively at one side of the channel holes located at the edge of the memory cell region MR. Also, as illustrated in FIG. 10, the dummy holes may be formed on the same line as the channel holes, and the dummy holes on the same line are spaced apart from each other. <i>The dummy hole adjacent to the channel hole may penetrate all of the stacked first and second dielectric layers 210 and 215. Also, the number of the penetrated first and second dielectric layers 210 and 215</i>

8,945,996	US 2010/0133598 A1 (“Chae”)
	<i>may decrease with an increase in the distance from the memory cell region MR.”)</i> • [0128] (“Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b. That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the contact region CR and the active pillars 224a of the memory cell region MR. Also, the active pillars 224a and the supporters 224b may be formed to the same length. <i>The active pillars 224a of the memory cell region MR may penetrate all of the stacked first and second dielectric layers 210 and 215, and the supporters 224b of the contact region CR may penetrate some of the stacked first and second dielectric layers 210 and 215.”)</i>
[25.d] simultaneously forming at least one of conductive material, semiconductor material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and	See [17.c] and [23], where “primary portion opening” of [17.c] corresponds to “first opening” and “end portion opening” of [17.c] corresponds to “second opening.” Kuhn, ¶157.

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forming dummy structures therewith within the second openings in the end portion;	
[25.e] forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings;	See [17.d] and [23], where “primary portion opening” of [17.d] corresponds to “first opening” and “end portion opening” of [17.d] corresponds to “second opening.” Furthermore, “horizontally elongated openings” of [17.d] which are formed through Chae’s “features” (<i>e.g.</i> , “first dielectric layers 210”) correspond to “horizontally elongated openings” of [25.e] because they are also formed into Chae’s “stack” (<i>e.g.</i> , “stack structure” including “first dielectric layers 210”). <i>See also</i> [25.b], [25.c]. Kuhn, ¶158.
[25.f] removing at least a portion of the sacrificial material that is laterally between the	Chae discloses removing at least a portion of the sacrificial material (<i>e.g.</i> , “second dielectric layers 215”) that is laterally between the horizontally elongated openings (<i>e.g.</i> , openings illustrated in Fig. 10, <i>see</i> [12.c]) selectively (<i>e.g.</i> , by having “different etch selectivity”) relative to the dielectric material (<i>e.g.</i> , “first dielectric layers 210”) to form void spaces elevationally between vertically spaced horizontal lines of the

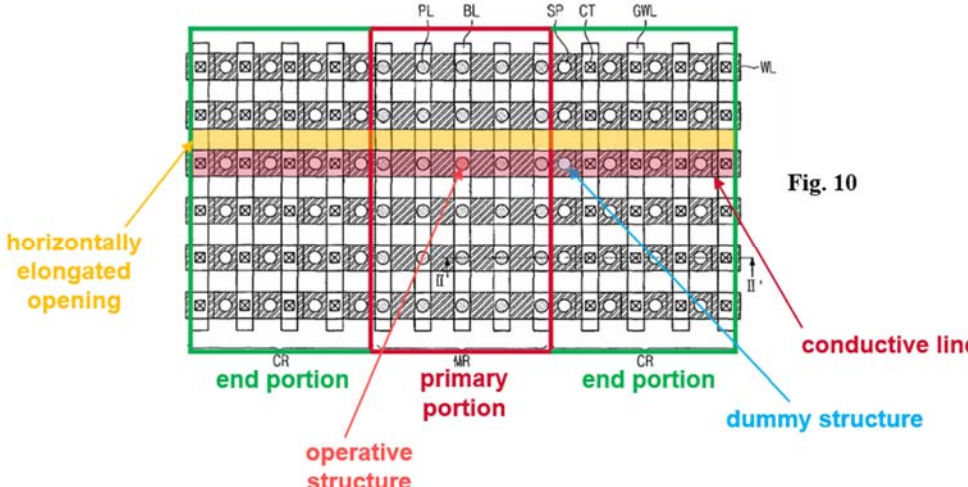
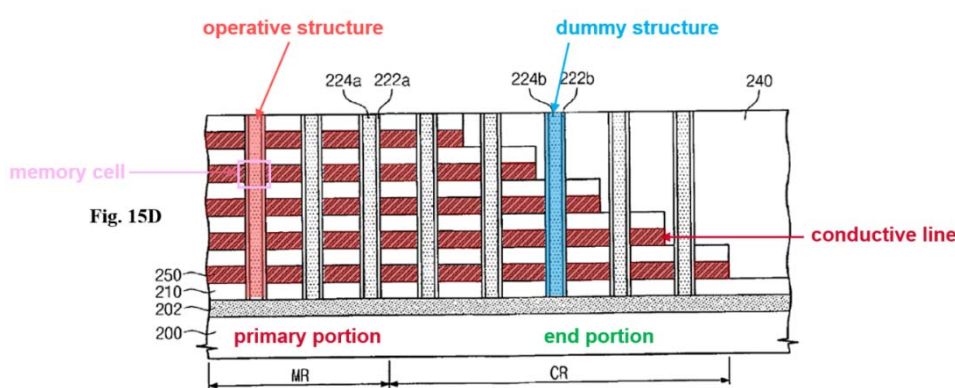
8,945,996	US 2010/0133598 A1 (“Chae”)
horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material;	dielectric material (<i>e.g.</i>, “spaces between” “line-shaped” “stacked first dielectric layers 210”). <u>E.g., Chae:</u> See [12.c], [25.e]. Chae further discloses removing at least a portion of the sacrificial material (“the second dielectric layers 215”) laterally between the openings formed in the previous step. Chae also discloses that this removing is done selectively by having sacrificial material with different etch selectivity relative to the dielectric material. [0129]-[0130]; <i>see also</i> [12.d], [13]. This process leads to the formation of void spaces, which are elevationally (vertically) between the layers of “dielectric material 210” that are “line-shaped” because of the openings that divide them into lines. [0129]-[0130], Figs. 15B, 15C. Kuhn, ¶¶159-161. • Figures 15B, 15C:

8,945,996	US 2010/0133598 A1 ("Chae")
	Fig. 15B 224a 222a 224b 222b 240 215 210 202 200 primary portion end portion MR CR Fig. 15C 224a 222a 224b 222b 240 210 202 200 primary portion end portion MR CR sacrificial material lines [0129] (“Referring to FIG. 15C, the plate-shaped stack structure including the active pillars 224a and the supporters 224b are patterned to form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and 215 may be exposed. Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.”) [0130] (“Referring to FIG. 15D, the space between the first dielectric layers 210 may be filled with conductive material to form line-shaped gate electrodes 250.”)

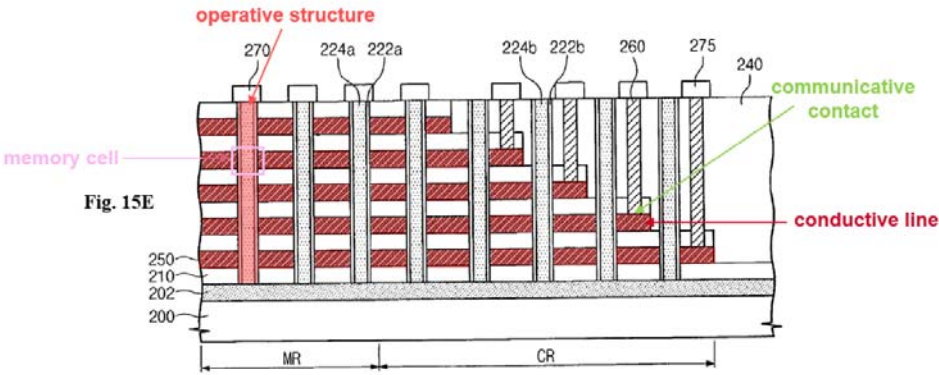
8,945,996	US 2010/0133598 A1 (“Chae”)
[25.g] after the removing, forming conductive material into the horizontally elongated openings and the void spaces;	Chae discloses after the removing, forming conductive material (e.g., forming “conductive layer 250”) into the horizontally elongated openings (e.g., “between the adjacent line-shaped stack structures”) and the void spaces (e.g., “spaces between” “line-shaped” “stacked first dielectric layers 210”). <u>E.g., Chae:</u> See [25.e]-[25.f]. Chae further discloses after removing “sacrificial layers 215,” forming “conductive layer 250” into the openings “between the adjacent line-shaped stack structures” and the void spaces “on/under the first dielectric layers 210.” [0129]-[0130], [0143]-[0144]. Kuhn, ¶¶162-164. - Figure 10:  - Figures 15C, 15D:

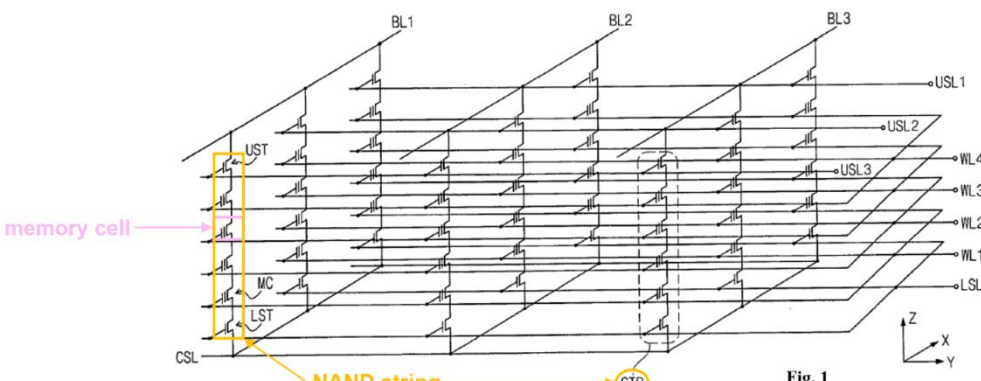
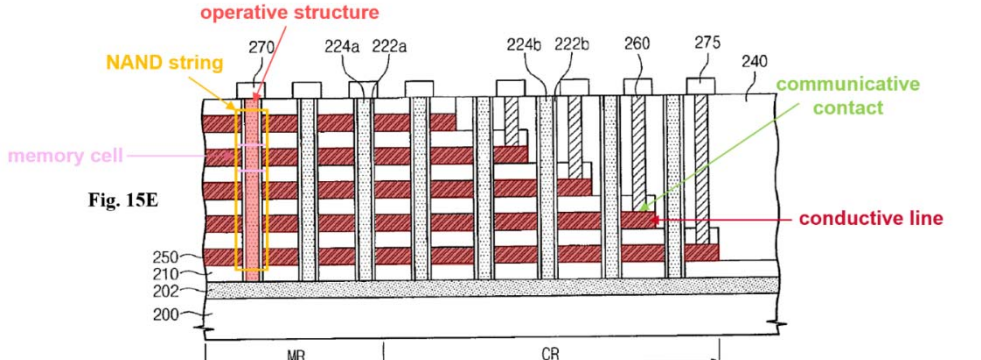
8,945,996	US 2010/0133598 A1 ("Chae")
	Fig. 15C Fig. 15D [0129] ("Referring to FIG. 15C, the plate-shaped stack structure including the active pillars 224a and the supporters 224b are patterned to form line-shaped stack structures. When the line-shaped stack structures are formed, the sidewalls of the first and second dielectric layers 210 and 215 may be exposed. Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215.") [0130] ("Referring to FIG. 15D, the space between the first dielectric layers 210 may be filled with conductive material to form line-shaped gate electrodes 250. Specifically, when conductive material is deposited between the first dielectric layers 210, conductive layers 250 may be formed around the active pillars 224a and the

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	supporters 224b. Thereafter, the conductive layer 250 filling the space between the adjacent line-shaped stack structures may be removed to form line-shaped gate electrodes 250 between the first dielectric layers 210.”)
[25.h] removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy	Chae discloses removing at least a portion of the conductive material (<i>e.g.</i>, removing a portion of “conductive layer 250”) from the horizontally elongated openings to form vertically spaced horizontal conductive lines (<i>e.g.</i>, to form “line-shaped gate electrodes 250”) from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material (<i>e.g.</i>, from “spaces between” “line-shaped” “stacked first dielectric layers 210”), the conductive lines collectively crossing a row of the operative and dummy structures (<i>e.g.</i>, crossing row of “active pillars 224a and charge storage layers 222a” and “supporters 224b and charge storage layers 222b”) at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line (<i>e.g.</i>, intersection of “line-shaped gate electrode 250” at different heights) and an individual operative structure (<i>e.g.</i>, “active pillar 224a” with “charge storage layer 222b”). <u>E.g., Chae:</u> See [25.a]-[25.g]. Chae further discloses “conductive layer 250 filling the space between the adjacent line-shaped stack structures” (the conductive material in the openings) “may be removed to form line-shaped gate electrodes 250” (vertically spaced horizontal conductive lines) “between the first dielectric layers 21.” [0130]. These horizontal conductive lines are vertically spaced because they are formed within the void spaces between the line-shaped “first dielectric layers 210,” i.e., the dielectric layers and the newly formed line-shaped gate electrodes are alternately stacked. Chae also discloses that “line-shaped gate electrodes 250” cross a row of the operative and dummy structures (“active pillars 224a and charge storage layers 222a” and “supporters 224b and charge storage layers 222b”). Fig. 10. Because the conductive lines are vertically stacked, they cross a

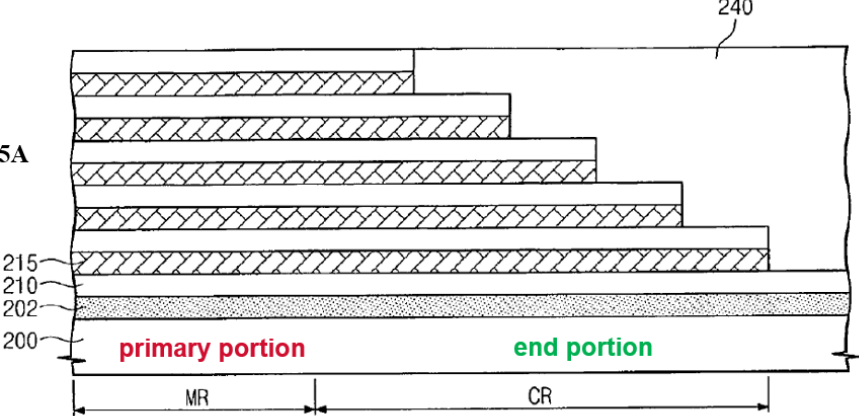
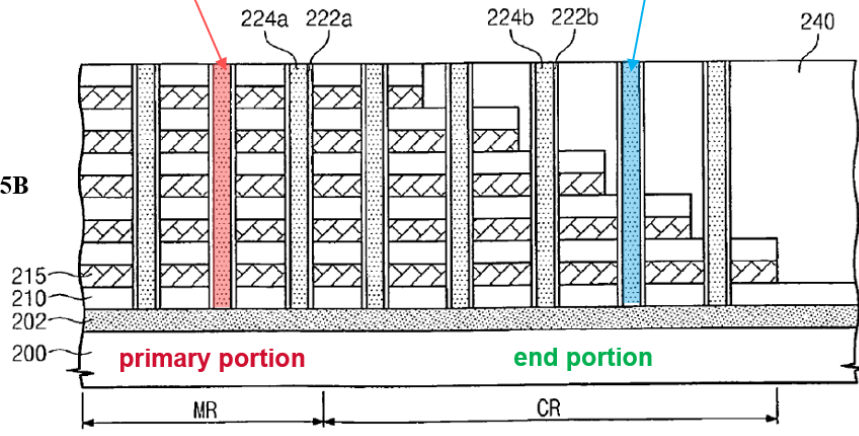
8,945,996	US 2010/0133598 A1 (“Chae”)
structures at different respective elevations. Fig. 15D. Chae teaches that the “active pillars” are “channels of transistors” and “correspond to” vertical “strings of the nonvolatile memory device.” [0054]. Therefore, memory cells exist at each intersection of an individual “line-shaped gate electrode 250” and an individual “active pillar 224”–“charge storage layer 222a” combination. Kuhn, ¶¶165-168.	row of the operative and dummy structures at different respective elevations. Fig. 15D. Chae teaches that the “active pillars” are “channels of transistors” and “correspond to” vertical “strings of the nonvolatile memory device.” [0054]. Therefore, memory cells exist at each intersection of an individual “line-shaped gate electrode 250” and an individual “active pillar 224”–“charge storage layer 222a” combination. Kuhn, ¶¶165-168. - Figure 10:  - Figure 15D:  [0054] (“<i>The active pillars PL are provided for the channels of transistors, which correspond to the strings of the nonvolatile memory device according to the embodiments of the inventive concept. That is, the channels of memory cell transistors and select transistors</i>”)

8,945,996	US 2010/0133598 A1 (“Chae”)
	<i>(LST, UST and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.”)</i> • [0130] (“Referring to FIG. 15D, the space between the first dielectric layers 210 may be filled with conductive material to form line-shaped gate electrodes 250. Specifically, when conductive material is deposited between the first dielectric layers 210, conductive layers 250 may be formed around the active pillars 224a and the supporters 224b. Thereafter, the conductive layer 250 filling the space between the adjacent line-shaped stack structures may be removed to form line-shaped gate electrodes 250 between the first dielectric layers 210.”)
[25.i] forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion.	Chae discloses forming a respective communicative contact (e.g., forming “contact plugs 260”) to a stair extension of individual ones of the horizontal conductive lines (e.g., portion of “line-shaped gate electrodes 250” “formed in a stair shape”) in the end portion (e.g., “contact region CR”). <u>E.g., Chae:</u> See [25.h]. Chae further discloses forming “contact plugs 260, connected respectively to the gate electrodes 250 of each layer,” “in the contact region CR of the gate electrodes 250.” [0131]. Chae discloses “contact plugs 260” form communicative contact with stair extensions of individual “line-shaped gate electrodes 250.” [0131], Fig. 15E. Kuhn, ¶¶169-171. • Figure 15E:

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	 • [0131] (“Referring to FIG. 15E, contact plugs 260, connected respectively to the gate electrodes 250 of each layer, are formed in the contact region CR of the gate electrodes 250.”) • [0132] (“Because the gate electrodes 250 of the contact region CR are formed in a stair shape, the contact plugs 260 may differ in length.”)
[26] The method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel	See [25]. Chae discloses the memory cells (e.g., “memory cells MC”; “memory cell transistors MC”) comprise a portion of NAND architecture (e.g., comprise a portion of the “NAND-type nonvolatile memory device”), the at least one formed material (see [25.d]) comprises semiconductive material (e.g., “semiconductor material”), and the operative structures (e.g., “active pillars 224a” with “charge storage layers 222a”) comprise interconnected channel regions of a NAND string (e.g., “string STR”). <u>E.g., Chae:</u> See [9], [25.d]. As explained in [9], Chae discloses its “active pillars 224a” comprise “semiconductor material” (see also [25.d]) and constitute interconnected channels of memory cell transistors, which are connected in series to form strings. Chae further discloses a “NAND-type nonvolatile memory device” including “a cell string structure,” such that each memory cell transistor string is a NAND string. [0005]. Therefore, Chae’s “active

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regions of a NAND string.	pillars 224a” comprise interconnected channel regions of a NAND string. Kuhn, ¶¶172-174. - Fig. 1:  - Figure 15E:  [0005] (“In particular, <i>the NAND-type nonvolatile memory device is advantageous for high integration because it includes a cell string structure having a plurality of memory cell transistors connected in series.</i>”) [0043] (“Each string STR includes upper and lower select transistors UST and LST, and memory cell transistors MC that are connected in series between the upper and lower select transistors UST and LST. The drains of the upper select transistors UST are connected to the bit lines BL1~BL3, and the sources of the lower select transistors LST are connected in common to the common source line CSL.”)

8,945,996	US 2010/0133598 A1 (“Chae”)
	[0054] (“<i>The active pillars PL are provided for the channels of transistors, which correspond to the strings of the nonvolatile memory device according to the embodiments of the inventive concept. That is, the channels of memory cell transistors and select transistors (LST, UST and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.</i>”) [0041] (“<i>FIG. 1 is a circuit diagram of a nonvolatile memory device according to exemplary embodiments of the inventive concept.</i>”) [0121] (“<i>Another method for fabricating the nonvolatile memory devices according to the second and fifth exemplary embodiments of the inventive concept will be described below with reference to FIGS. 15A to 15E.</i>”) - See also [0004]-[0005], [0041]-[0045].
[28] The method of claim 25 comprising forming the first and second openings using the same masking step.	See [25]. Chae discloses forming the first and second openings (e.g., “channel holes” and “dummy holes”) using the same masking step (e.g., using masking as part of “photolithography”). <u>E.g., Chae:</u> See [25.b]-[25.c]. Chae discloses “channel holes and the dummy holes may be formed through a photolithography process,” which is a process that involves masking. See, e.g., [0099] (describing the formation of the same channel holes in a different embodiment as “[t]he channel holes may be formed by forming a mask pattern”). A POSITA would have understood (and found it obvious) that forming the “channel holes” and “dummy holes” using the same “photolithography process” would also use the same masking step, which advantageously reduces the number of processing steps. Kuhn, ¶¶175-177. Figures 15A, 15B:

8,945,996	US 2010/0133598 A1 ("Chae")
	Fig. 15A  Fig. 15B  [0099] ("Referring to FIG. 13F, after the forming of the gate electrodes on the semiconductor substrate 100, a dielectric layer 160 may be formed to fully cover the stacked gate electrodes. Active pillars 174 penetrating the stacked gate electrodes, and a charge storage layer 172 surrounding the active layers 174, may be formed in the memory cell region MR. Specifically, a plurality of channel holes are formed to penetrate the interlayer dielectrics 110 and the conductive layers 122 stacked in the memory cell region MR. The channel holes may be formed by forming a mask pattern (not illustrated) on the uppermost dielectric layer 150 and selectively and anisotropically etching the stacked interlayer dielectrics 110 and conductive layers 122 by means of the mask pattern. The formed channel holes may expose the

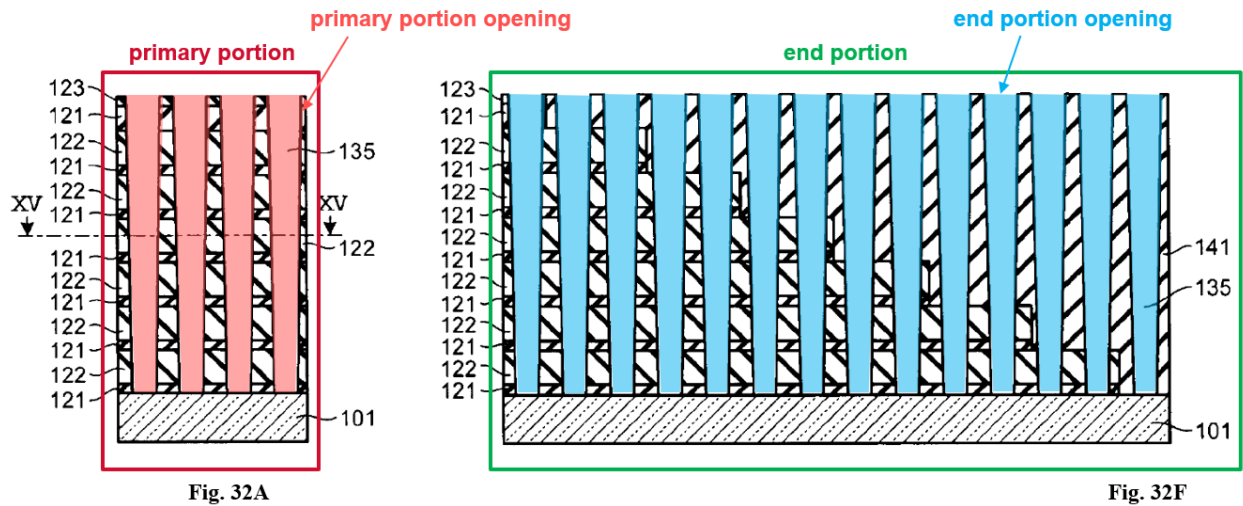
8,945,996	US 2010/0133598 A1 (“Chae”)
	impurity region 102 of the semiconductor substrate 100. Also, the channel holes may be formed in a matrix configuration on the plane.”) [0127] (“More specifically, channel holes are formed in the memory cell region MR and dummy holes are formed in the contact region CR. <i>The channel holes and the dummy holes may be formed through a photolithography process, and the channel holes may be formed in a matrix configuration on the plane....</i>”)
[30] The method of claim 25 wherein the sacrificial material is dielectric.	See [25]. Chae discloses the sacrificial material (e.g., “second dielectric layer 215”) is dielectric. <u>E.g., Chae:</u> See [25.a]. Kuhn, ¶¶178-180.
[32] The method of claim 25 wherein the features comprise plates.	See [25], [6]. Kuhn, ¶181.

B. Ground 2: Chae in View of Kiyotoshi (Claims 1-4, 18, 23, 25-26, 28, 30, 32)

As discussed in §IX.A, **Chae** anticipates and at least renders obvious claims 1-4, 18, 23, 25, and 28. To the extent further disclosure is required, **Chae** in view of **Kiyotoshi** renders these claims obvious. Kuhn, ¶183.

Kiyotoshi is directed to a method for manufacturing “nonvolatile semiconductor memory devices” in which a “stacked film in the **memory cell region** and the **word-line contact region** is collectively processed...to form the **through-holes 135**.” Kiyotoshi, [0019], [0123]. “Semiconductor films 131” in the memory cell and word-line contact regions are “deposited in the **through-holes 135**” followed by “dielectric films 132.” *Id.*, [0124]-[0125]. The “semiconductor films 131” in the “**memory cell region**” form operative “memory strings MS” while the “semiconductor films 131” in the “**contact region**” “are dummy semiconductor films 131.” *Id.*, [0116]. Kuhn, ¶182.

To the extent further disclosure is needed for forming primary portion openings and end portion openings at the same time (claim 18) using the same masking step (claim 28), **Kiyotoshi** discloses a “mask film is formed over the entire surface of the stopper film 123” and “[t]he stacked film in the memory cell region and the word-line contact region is collectively processed by the lithography technique and RIE method to form the through-holes 135” in both regions simultaneously. Kiyotoshi, [0123]. Kuhn, ¶184.

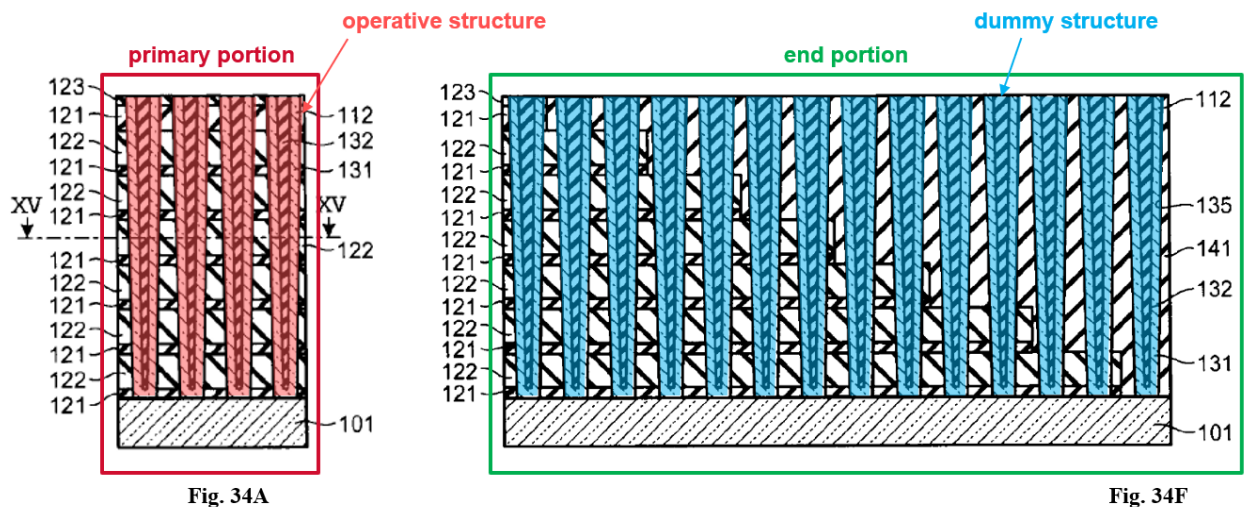


Kiyotoshi, Figures 32A and 32F.

Moreover, to the extent further disclosure of depositing a semiconductive material simultaneously in primary portion openings and end portions openings (claim 23) to simultaneously form operative and dummy structures (claim 25), **Kiyotoshi** discloses forming “semiconductor films 131” and “dielectric films 132” in “through holes 135” (both in the memory cell region and the word-line contact region) using a “film forming method such as the LPCVD method.” Kiyotoshi, [0124]-[0125]. **Kiyotoshi**’s “semiconductor films 131” and “dielectric films 132” collectively constitute operative structures in “memory cell region” because they form “memory strings MS;” however in “word-line contact region,” they “do not form the memory strings MS” and hence are dummy structures. Kiyotoshi, [0116]. Kuhn, ¶185.

Because **Kiyotoshi** discloses forming “semiconductor film 131” followed by “dielectric film 132” “to fill the inside of the hollow cylindrical semiconductor films

131” to form the operative and dummy structures, it discloses that the operative and dummy structures comprise the same material (claim 2) and a plurality of the same materials, i.e., “semiconductor film 131” and “dielectric film 132” (claim 3), wherein the same materials are arranged in the same lateral order (claim 4). Kiyotoshi, [0124]-[0125], Fig. 34A, 34F. Similarly, for element [1.b], to the extent PO argues supporters 224b do not mimic a physical property of the active pillars 224a on the basis that they are formed of different materials, **Kiyotoshi** teaches forming the structures of the same materials. Kuhn, ¶186.



Kiyotoshi, Figures 34A and 34F.

Chae and **Kiyotoshi** are analogous art, in the same field as the '996—which includes the field of manufacturing nonvolatile memory devices. '996, 1:8-10, Chae, [0002]; Kiyotoshi, [0019]. Moreover, **Chae** and **Kiyotoshi** are pertinent to the purported problem addressed by the '996 of supporting dielectric layers while

replacing sacrificial layers between the dielectric layers with gate layers. '996, 7:25-35; Chae, [0129]; Kiyotoshi, [0127]. Kuhn, ¶188.

With respect to claims 18 and 28, a POSITA would have been motivated to apply **Kiyotoshi's** teaching of forming the primary portion openings (first openings) and the end portion openings (second openings) at the same time (using the same masking step) to **Chae's** method to simplify the process and advantageously reduce the number of processing steps. Reducing the number of processing steps would have been advantageous because it would have reduced the chance of defects and shortened the manufacturing time, allowing higher fabrication yield. Ex. 1010, Kuhn, ¶189.

Moreover, **Chae** discloses that “channel holes and the dummy holes may be formed through a photolithography process.” Chae, [0127]. Photolithography is a process of using a mask to etch material from a semiconductor device in a desired pattern. Ex. 1011. Thus, a POSITA would have found it straightforward to use a single mask to form holes in both channel and dummy holes as taught by **Kiyotoshi** when performing **Chae's** photolithography process. Kuhn, ¶190.

Thus, a POSITA would have found it routine, straightforward and advantageous to apply **Kiyotoshi's** teaching of using a single mask process to form through-holes to **Chae's** memory device fabrication process, and would have known

such combination (yielding the claimed limitations) would predictably work and provide the expected resulting structure. Kuhn, ¶191.

With respect to claims 23 and 25, a POSITA would have been motivated to apply **Kiyotoshi**'s teaching of depositing semiconductive material simultaneously into the primary portion openings (first openings) and the end portion openings (second openings) to **Chae**'s method to simplify the process and advantageously reduce the number of processing steps. As noted in connection with claims 18 and 28, fewer processing steps would have been advantageous because it would have reduced the chance of defects and shortened the manufacturing time. Kuhn, ¶192.

Chae discloses that "the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b." Chae, [0128]. A POSITA would have found it straightforward to apply **Kiyotoshi**'s express disclosures to form semiconductor material in channel and dummy holes simultaneously when forming these structures in **Chae**'s fabrication process. Although **Kiyotoshi** teaches forming charge storage layers after filling the holes with semiconductive material (followed by dielectric material) and **Chae** teaches forming charge storage layers in the holes before forming the semiconductive material, this difference is not relevant to **Kiyotoshi**'s teaching about forming the semiconductive material in the holes simultaneously, which a POSITA would have found to be applicable to **Chae**. Kuhn, ¶193.

With respect to claims 1-4, a POSITA would have been motivated to apply **Kiyotoshi**'s teaching of forming the operative and dummy structures using the same semiconductor and dielectric materials with the same lateral order to **Chae**'s method to simplify the process and advantageously reduce the number of materials used. Kuhn, ¶194.

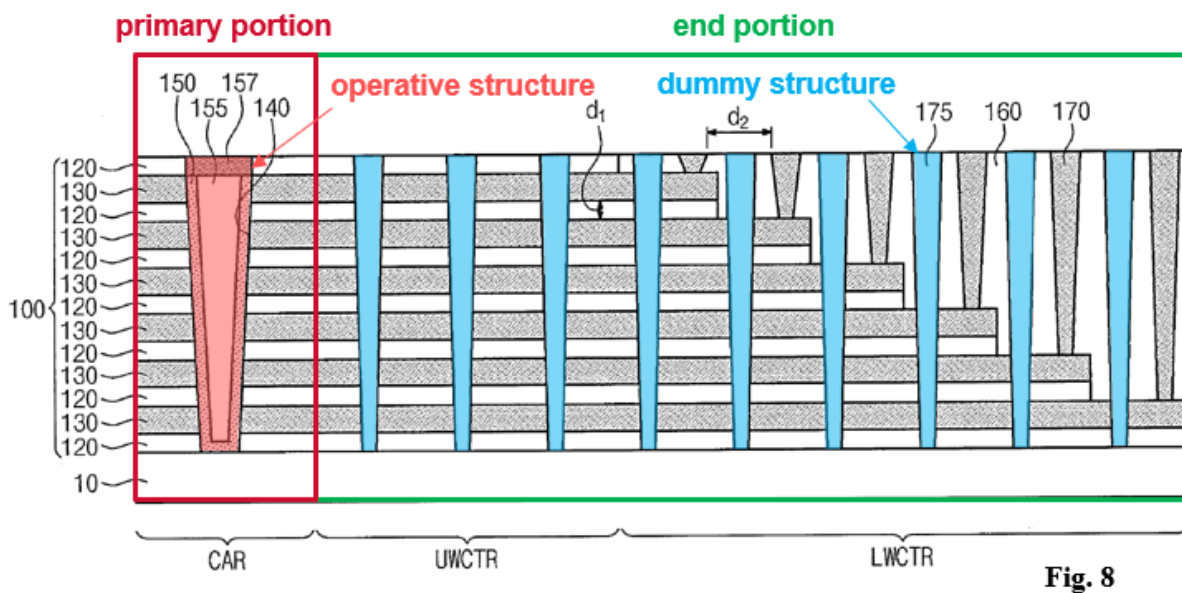
Thus, a POSITA would have found it routine, straightforward and advantageous to apply **Kiyotoshi**'s teaching of simultaneously forming operative and dummy structures to **Chae**'s memory device fabrication process, and would have known such combination (yielding the claimed limitations) would predictably work and provide the expected resulting structure. Kuhn, ¶195.

Furthermore, because claims 26, 30, and 32 depend from claim 25, **Chae** in view of **Kiyotoshi** renders these claims obvious for the same reasons **Chae** discloses them or at least renders them obvious, as discussed in Ground 1. Kuhn, ¶187.

C. Ground 3: Chae in View of Hwang (Claim 22)

Hwang is directed to methods of manufacturing three-dimensional memory devices. Hwang, [0002]-[0003]. **Hwang** discloses forming a stack of “inter-layer insulating layers 120” and “lower sacrificial layers 130” divided into a “cell array region CAR” and “contact regions UWCTR and LWCTR.” *Id.*, [0032]-[0033]. Within the contact regions, “a terraced shape is formed” by “patterning.” *Id.*, [0036]. Kuhn, ¶196.

Hwang further discloses that “**lower through-holes 140** are formed in the **cell array region CAR**...and then lower semiconductor patterns 150 are formed in the lower through-holes 140.” Hwang, [0044]. Similarly, “**supporting members 175** are formed” “in the **lower word line contact region LWCTR**.” *Id.*, [0119]. The “**supporting members 175** may prevent and/or reduce collapse of the **lower inter-layer insulating layers 120**...in the subsequent process of removing the **lower sacrificial layers 130**.” *Id.*, [0120]. Kuhn, ¶197.



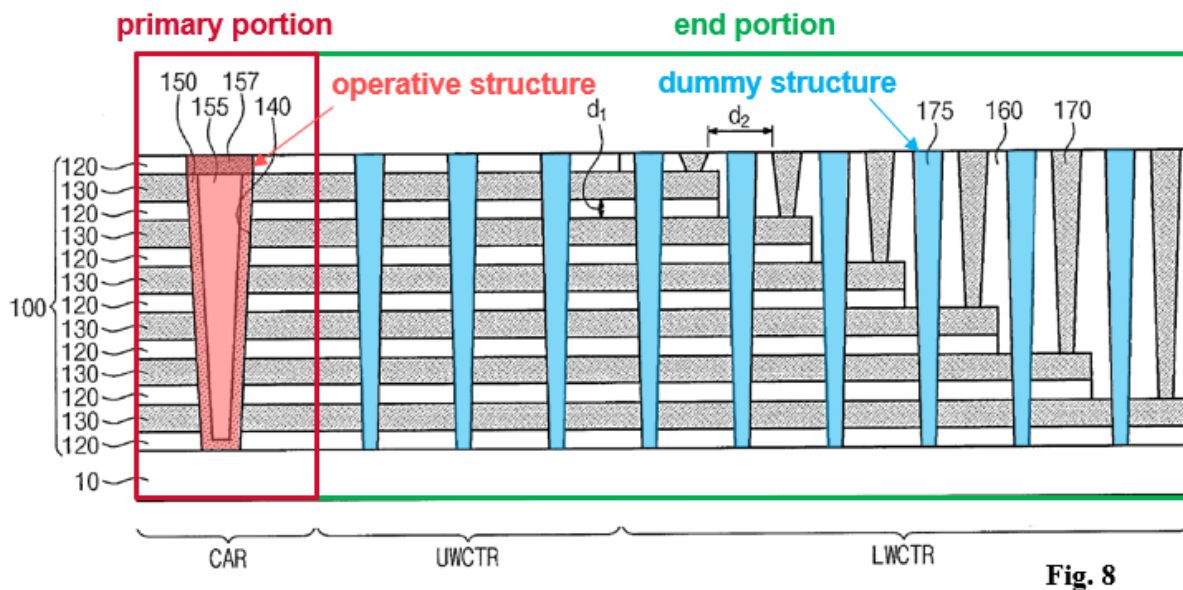
Hwang, Figure 8.

As discussed in §IX.A, Chae discloses and at least renders obvious claim 17. With respect to claim 22 (dependent from claim 17), Hwang discloses forming the primary portion openings (e.g., “lower through-holes 140”) and the end portion openings (e.g., openings that are filled to form “supporting members 175”)

to have at least one of different horizontal cross sections or different vertical cross sections (*e.g.*, different widths). Kuhn, ¶198.

Hwang discloses that “lower through-holes 140 are formed in the cell array region CAR.” Hwang, [0044]. Then, a semiconductor material is deposited to form “semiconductor patterns 150” in through-holes 140 in the cell array region with a “hollow cylindrical shape substantially covering the inner sidewalls of the lower through-holes 140,” thereby partially filling the holes. *Id.*, [0044], [0047]. **Hwang** also discloses that “supporting members 175” are formed in the contact region and “formed together with the lower semiconductor patterns 150” of the cell array region. *Id.*, [0119]. A POSITA would have understood from **Hwang**’s teachings that supporting members 175 are formed by forming holes in the contact region and then filling them. Subsequently, the remainder of the through-holes 140 lined with “semiconductor patterns 150” are filled with “buried patterns 155,” thereby completing the filling of the through-holes 140. *Id.*, [0050], [0119]. **Hwang** also teaches that the filling of these holes with semiconductor material occurs “by an epitaxial technique and/or chemical vapor deposition.” *Id.*, [0047]. A POSITA would have understood that an epitaxial technique and/or chemical vapor deposition result in films with uniform thickness, *i.e.*, the same amount of material sticks to the same amount of surface area across the surface onto which the material is deposited. Exs. 1012, 1013. Because the same amount of semiconductor material completely

fills the holes in the end portion to form “supporting members 175” but “lower semiconductor patterns 150” only partially fill respective through-holes 140, the through-holes 140 have a greater width than the holes in the end portion, consistent with the depictions of Fig. 8—and at minimum it would have been obvious to have greater width to accommodate the material for buried patterns 155, but not fill the through-holes 140. Kuhn, ¶¶199.



Hwang, Figure 8.

Chae and **Hwang** are analogous art, in the same field as the '996, which includes methods for manufacturing nonvolatile memory devices. Chae, [0002]; Hwang, [0002]. Moreover, **Chae** and **Hwang** are pertinent to the purported problem addressed by the '996 of supporting dielectric layers while replacing sacrificial

layers between the dielectric layers with gate layers. '996, 7:25-35; Chae, [0129]; Hwang, [0120]. Kuhn, ¶200.

A POSITA would have been motivated to apply **Hwang's** teaching of forming holes for dummy structures in the contact region to have smaller widths than holes in the memory cell array region to **Chae's** method of forming a memory device so that the memory device would be reduced in size. Hwang, [0120]. **Hwang's** teaching of smaller holes for dummy structures enables **Chae's** device to have a smaller contact region. Moreover, while the greater hole width in the memory region is necessary to accommodate the operational structure needed for each memory cell, this width is not necessary for **Chae's** supporters in the contact region. In this regard, **Hwang's** supporting members serve the same function as **Chae's** supporters because they "prevent and/or reduce collapse of the lower inter-layer insulating layers 120 and the lower insulating layers 160 in the subsequent process of removing the lower sacrificial layers 130." Hwang, [0120]. Kuhn, ¶201.

Thus, a POSITA would have found it routine, straightforward and advantageous to apply **Hwang's** teaching of smaller dummy structures to **Chae's** memory device fabrication process, and would have known such a combination (yielding the claimed limitations) would predictably work and provide the expected resulting structure. Kuhn, ¶202.

D. Ground 4: Chae in View of Pekny (Claims 12-13, 16)

As discussed in §IX.A, **Chae** anticipates and at least renders obvious claim 12. To the extent that further disclosure is required, **Chae** in view of **Pekny** renders this claim obvious. Kuhn, ¶204.

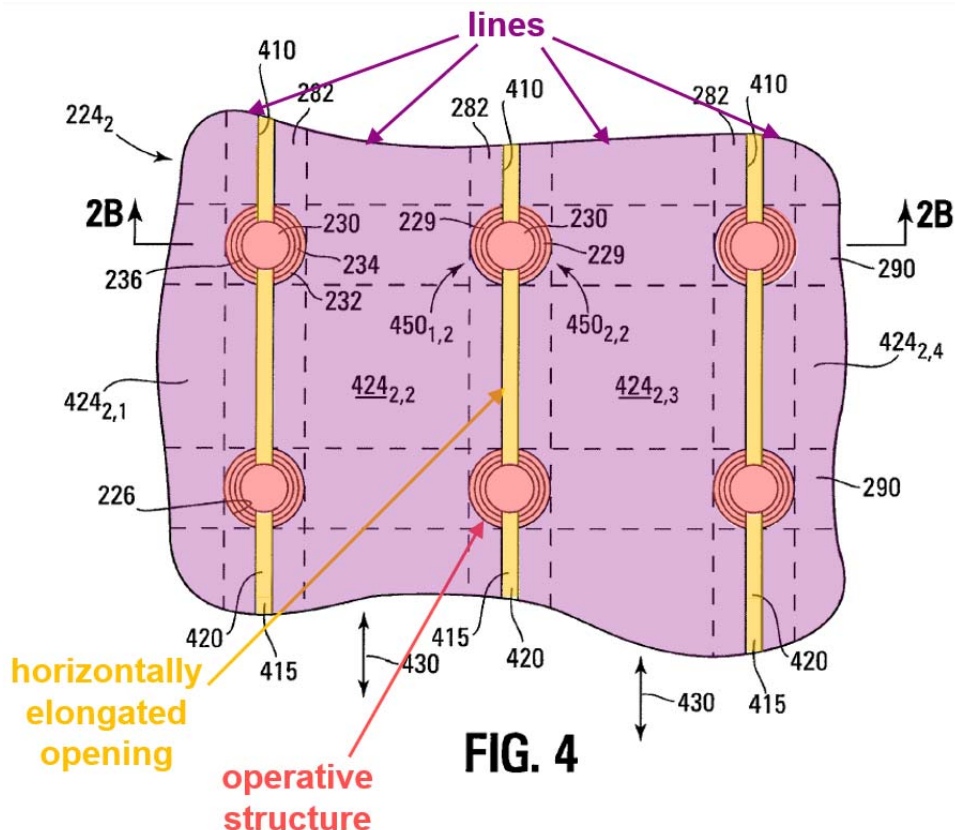
Pekny is directed to “methods of forming memory arrays.” **Pekny**, Abstract. **Pekny** discloses forming “alternating dielectric layers 222 and conductive layers 224” in the “memory cell portion 220.” **Pekny**, 5:8:29. **Pekny** also discloses forming “holes 226...passing through dielectric layers 222 and conductive layers 224,” which are then filled to form “conductive pillars 230.” *Id.*, 5:30-52. Kuhn, ¶203.

Limitation [12.c] requires “forming horizontally elongated openings through the structures.” **To the extent the limitation requires the elongated openings to pass directly through the structures, this is disclosed by Pekny.** Kuhn, ¶205.

Pekny discloses forming horizontally elongated openings (*e.g.*, “slots 410”) **through the structures** (*e.g.*, “conductive pillar 230,” “oxide layer 232,” “nitride layer 234,” and “oxide layer 236”) **to form horizontally elongated and vertically overlapping lines from material of the features** (*e.g.*, lines of “dielectric layers 222”), **the lines individually extending...laterally about sides of vertically extending portions of the operative structures** (*e.g.*, “conductive pillars 230”). While **Pekny** does not illustrate dummy structures, as noted below, when applying

Pekny's relevant teachings to **Chae**, the openings would extend about sides of vertically extending portions of the dummy structures. Kuhn, ¶206.

Pekny discloses forming “slots 410” in “dielectric layers 222 and conductive layers 224,” thereby forming line-shaped stacks. Pekny, 6:1-42. The line-shaped stacks extend laterally about sides of the operative structures that each comprise “conductive pillar 230,” “oxide layer 232,” “nitride layer 234,” and “oxide layer 236.” Pekny, 6:31-42, Fig. 4. **Pekny's** slots 410 pass through the operative structures. Pekny, Fig. 4. Slots 410 are then “filled with a dielectric material 415” to form “isolation regions 420” which “cut each conductive layer 224 into electrically isolated activation lines, such as word lines, 424.” Pekny, 6:1-42. Kuhn, ¶207.



Pekny, Figure 4.

Chae and **Pekny** are analogous art, in the same field as the '996, which includes methods for manufacturing nonvolatile memory devices. Chae, [0002]; Pekny, Abstract. Kuhn, ¶209.

A POSITA would have been motivated to apply **Pekny**'s teaching of forming a slot through the pillars to **Chae** because it would double the number of memory cells. **Pekny** explains that "[c]utting a charge trapping layer 228 with an isolation region 420 forms a pair of isolated memory cells 450_{1,2}, 450_{2,2}," therefore, the number of charge traps—and thus, the number of memory cells—doubles. Pekny,

6:43-49. This would advantageously increase the memory storage capacity in the same volume, *i.e.*, density. Pekny, 1:56-60. Kuhn, ¶210.

Moreover, because **Chae's** slots are linear and formed through the primary portion and the end portion, and the operative and dummy structures are linearly arranged, when applying **Pekny's** teaching of forming slots through operative structures, a POSITA would have formed slots through both the operative and dummy structures in **Chae's** device, such that the resulting lines would extend laterally about sides of vertically extending portions of the pillars 224a (operative structures) and 224b (dummy structures). Kuhn, ¶211.

A POSITA would have found the application of **Pekny's** teaching of forming slots that pass through operative structures to **Chae's** memory fabrication process straightforward. Kuhn, ¶212. For example, while **Chae** teaches forming the select gates in the same process as gate electrodes for the memory cells (Chae, [0129]-[0130], Figs. 15C-15D), a POSITA would have recognized that shifting **Chae's** slots as taught by **Pekny** would cause a misalignment between the pillars 224a and the select gates, impacting the ability to obtain double the number of memory cells. Kuhn, ¶212. A POSITA would have recognized that **Pekny** teaches a solution to this problem. In particular, **Pekny** discloses the select gate structure below the memory cells and aligned with operative structures (including conductive pillar 230, oxide layer 232, nitride layer 234 and oxide layer 234) is formed before memory

cells are formed, and the slots between word lines do not extend down to the lower select gates. Pekny, 6:1-9. Thereafter, the word lines would be formed using the process described by **Chae**, but the patterns on an etch mask used in the photolithography process to create the slot structures would be shifted so that the exposed regions for etching pass through the charge storage layers (222a or 222b) to obtain the increased memory cell density taught by **Pekny**. Chae, [0129]. Kuhn, ¶212. In this regard, as **Pekny** teaches, the memory cell fabrication process would not impact the lower select gates. Pekny, 5:8-10, 6:1-9, Figs. 2A-2B. Thereafter, the upper select lines would be formed directly above the operative structures and aligned with the lower select lines, using, e.g., a process similar to that taught by Pekny. Pekny, 7:15-17, Fig. 2C. Kuhn, ¶212.

Moreover, a POSITA would have understood that the steps after forming the slots through the operative structures would not negatively impact other structures in the device. In **Chae**, after the slots are formed, (1) dielectric layers 215 are removed by using the slots to supply the etchant, (2) conductive material is deposited in place of dielectric layers 215 through the slots, (3) the conductive material remaining in the slots is removed, and (4) the slots are filled with dielectric material. Chae, [0129]-[0130]. With respect to (1), a POSITA would have recognized that using silicon nitride for both the sacrificial dielectric layers 215 and the charge storage layers 222a and 222b as taught by **Chae** could potentially cause the charge

trap layer to be selectively removed with the sacrificial material when the slot is shifted to pass through **Chae's** operative and dummy structures. Chae, [0107]. Kuhn, ¶213. Thus, to obtain the benefit of doubling the density of memory cells taught by **Pekny**, a POSITA would have used another sacrificial dielectric material that can be etched selectively to silicon nitride (for charge storage layers 222a and 222b) and silicon oxide (for dielectric layers 210). Chae, [0100], [0107]. A POSITA would have known that doped boron nitride is such a dielectric. Exs. 1014, 1015, Kuhn, ¶213. The deposition of conductive material (step 2) or dielectric material (step 4) does not impact other structures. Kuhn, ¶213. Moreover, it was understood how to etch conductive material (for step 3) selectively to the semiconductor material used to form pillars 224a and 224b such that these materials would not be damaged in the etching process. Ex. 1014. Additionally, in **Chae**, the contact plugs 260 in the contact region for controlling the word lines are linearly aligned with operative and dummy structures. Chae, [0132]-[0133], Figures 10, 15E. A POSITA would have recognized that, when applying **Pekny's** teachings of shifting the slot to pass through the operative and dummy structures, to ensure contact with the respective word lines, the location of the contacts would be shifted to be between the slots. Kuhn, ¶213. Thus, a POSITA would have known how to apply **Pekny's** teachings of forming slots through operative structures without negatively impacting

the remainder of the fabrication process or the operation of the resulting device. Kuhn, ¶213.

Thus, a POSITA would have found it routine, straightforward and advantageous to apply **Pekny**'s teaching of forming slots through the structures to **Chae**'s memory device fabrication process, and would have known such a combination (yielding the claimed limitations) would predictably work and provide the expected resulting structure. Kuhn, ¶214.

Furthermore, because claims 13 and 16 depend from claim 12, **Chae** in view of **Pekny** renders these claims obvious for the same Ground 1 reasons **Chae** discloses them or at least renders them obvious, as discussed in §IX.A. Kuhn, ¶208.

X. SECONDARY CONSIDERATIONS

There is no evidence in the '996's prosecution history or elsewhere supporting any secondary considerations arguments, or evidence of nexus to any challenged claim. *See generally* '996FH; Kuhn, ¶215. Indeed, as demonstrated by the prior art referenced herein, any purported solutions to problems or unexpected results in the '996 were already well known. Kuhn, ¶215. To the extent PO asserts the existence of any secondary considerations in its responses, Petitioner reserves the right to address any such evidence.

XI. CONCLUSION

There is a reasonable likelihood that Petitioner will prevail as to the Claims.

Inter partes review of the Claims is accordingly requested.

Respectfully submitted,

Dated: November 18, 2024

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Registration No. 57,325
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to §42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,945,996 contains, as measured by the word-processing system used to prepare this paper, 13,743 words. This word count does not include the items excluded by §42.24 as not counting towards the word limit.

Dated: November 18, 2024

By: /James L. Davis, Jr./
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CERTIFICATE OF SERVICE

I hereby certify that on November 18, 2024, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,945,996 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on Patent Center:

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