

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Attorney Docket No.: 303.B12US6

Customer No.: 73115

PATENT APPLICATION TRANSMITTAL

Commissioner for Patents
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X CONTINUATION under 37 CFR 1.53(b) of prior Patent Application No. 16/125,242 comprising:

- X** Specification (27 pgs, including claims numbered 1 through 20 and a 1 page Abstract).
- X** Formal Drawing(s) (38 sheets).
- X** Application Data Sheet (7 pgs).
- X** Copy of signed Declaration (2 pgs).
- X** Power of Attorney (1 pg), Statement Under 37 C.F.R. § 3.73(c)(2 pgs).
- X** **Authorization to charge Deposit Account 19-0743 in the amount of \$1,720.00**

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[] MULTIPLE DEPENDENT CLAIMS PRESENTED				\$0.00
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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		
First Named Inventor/Applicant Name:		Sanh D. Tang		
Filer:		Daniel J. Mertes/Kathleen Gannon		
Attorney Docket Number:		303.B12US6		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1720

Electronic Acknowledgement Receipt

EFS ID:	38046412
Application Number:	16716177
International Application Number:	
Confirmation Number:	3036
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Daniel J. Mertes/Kathleen Gannon
Filer Authorized By:	Daniel J. Mertes
Attorney Docket Number:	303.B12US6
Receipt Date:	16-DEC-2019
Filing Date:	
Time Stamp:	18:25:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303B12US6.pdf	1672469	yes	78
			7bfbac2853abd4fe45cbbf9ecb272ac92139780a2		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Drawings-only black and white line drawings		41	78	
	Abstract		40	40	
	Claims		35	39	
	Specification		14	34	
	Oath or Declaration filed		12	13	
	Application Data Sheet		5	11	
	Assignee showing of ownership per 37 CFR 3.73		3	4	
	Power of Attorney		2	2	
	Transmittal of New Application		1	1	
Warnings:					
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2	Fee Worksheet (SB06)	fee-info.pdf	34537	no	2
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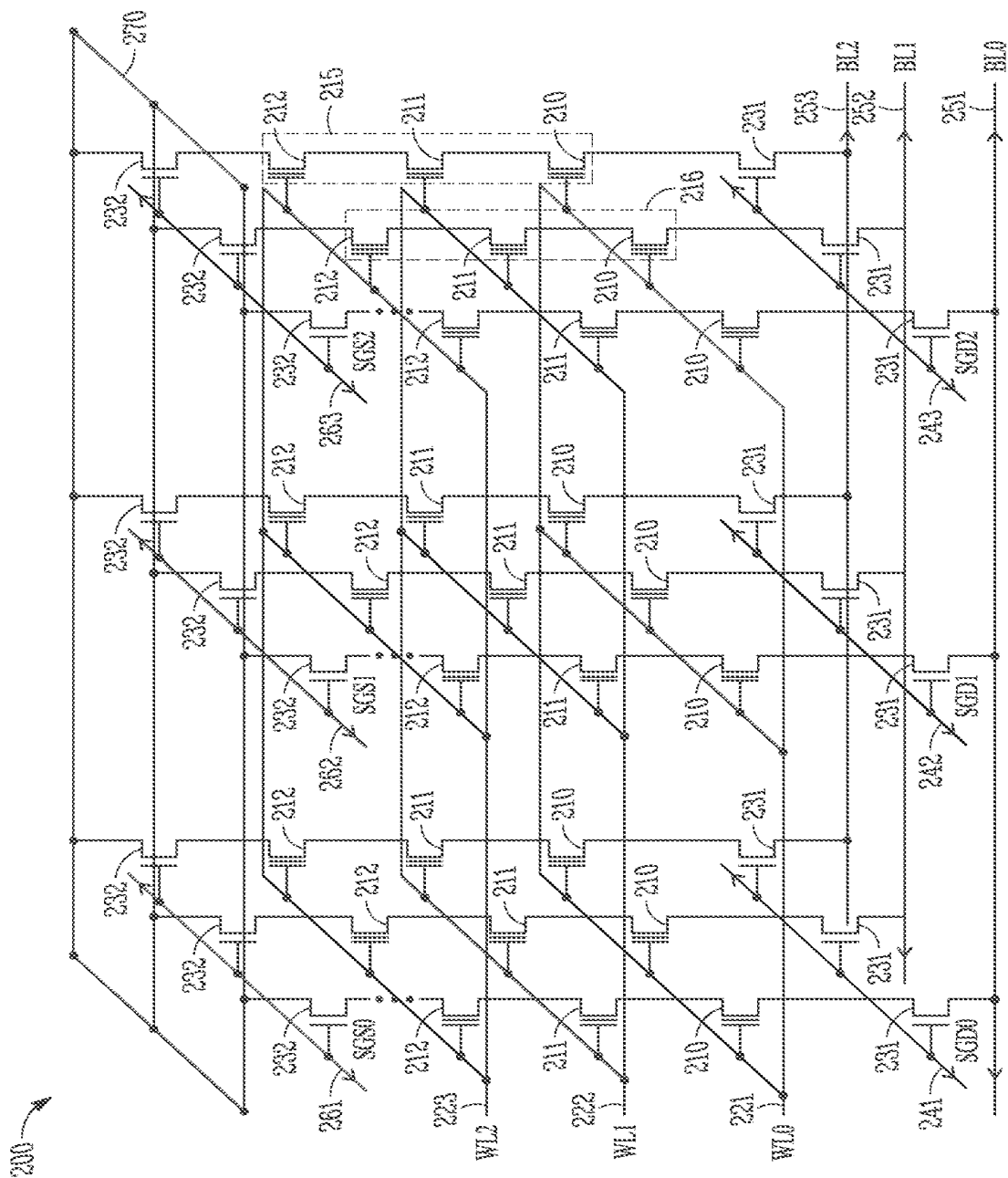


FIG. 2

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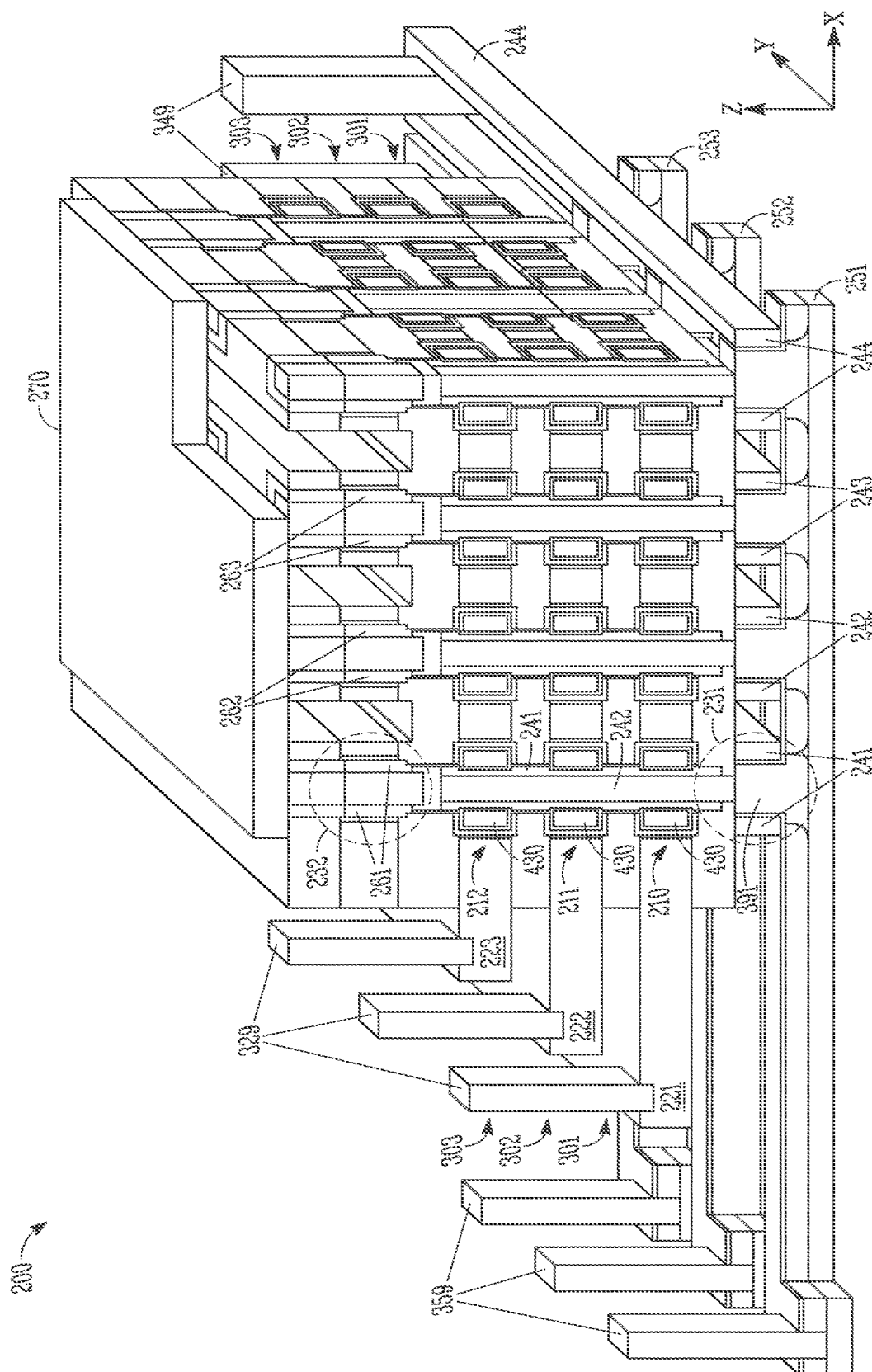


FIG. 3

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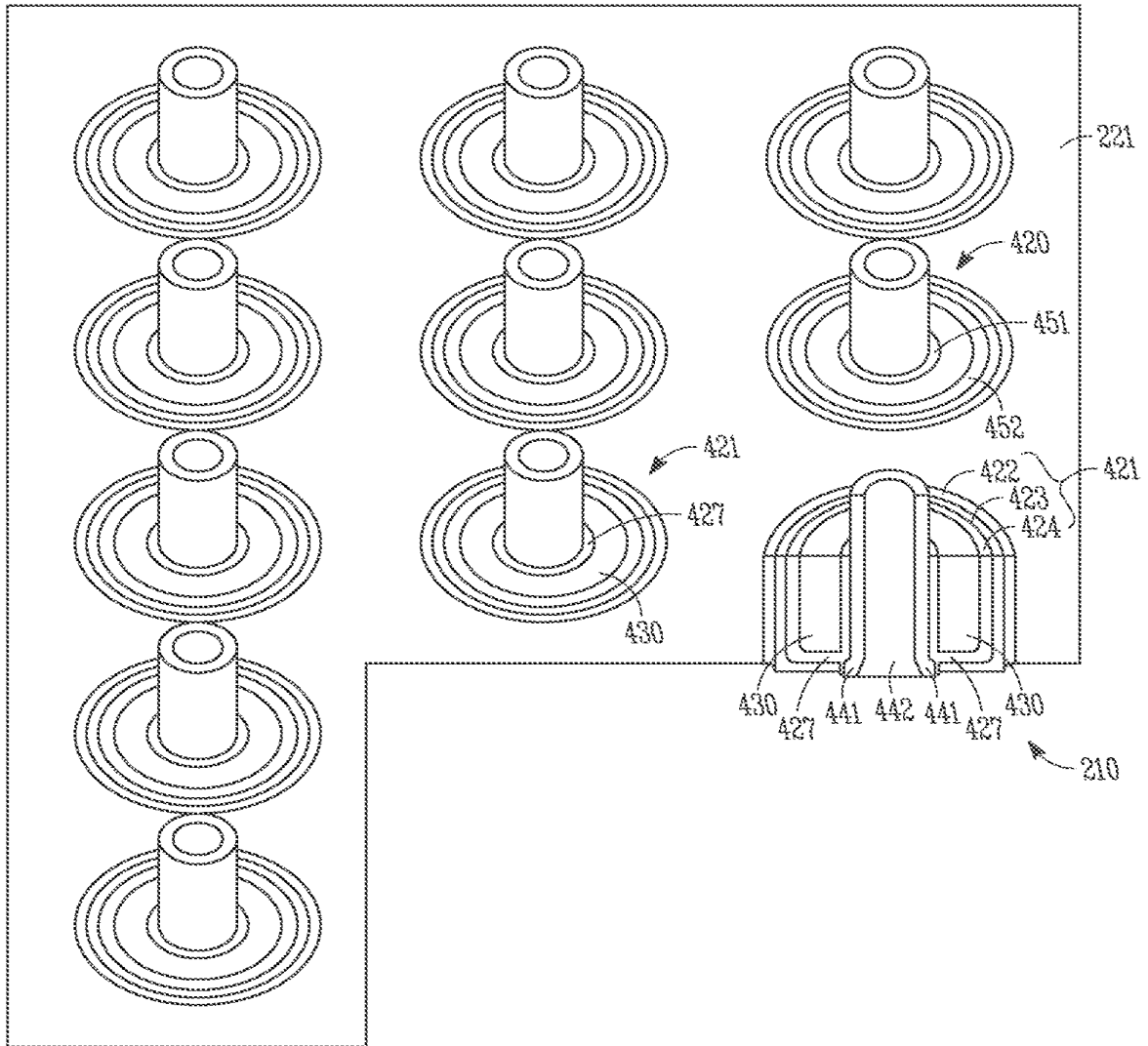
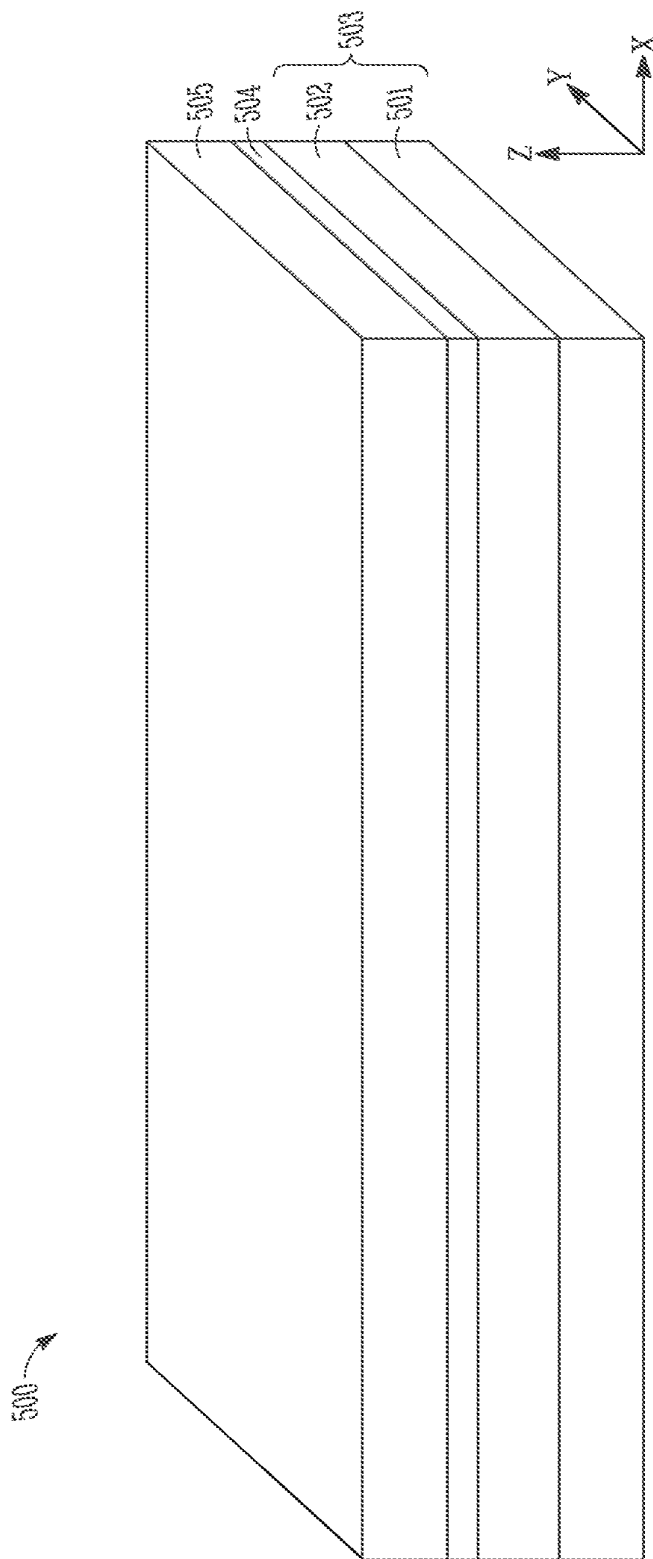


FIG. 4

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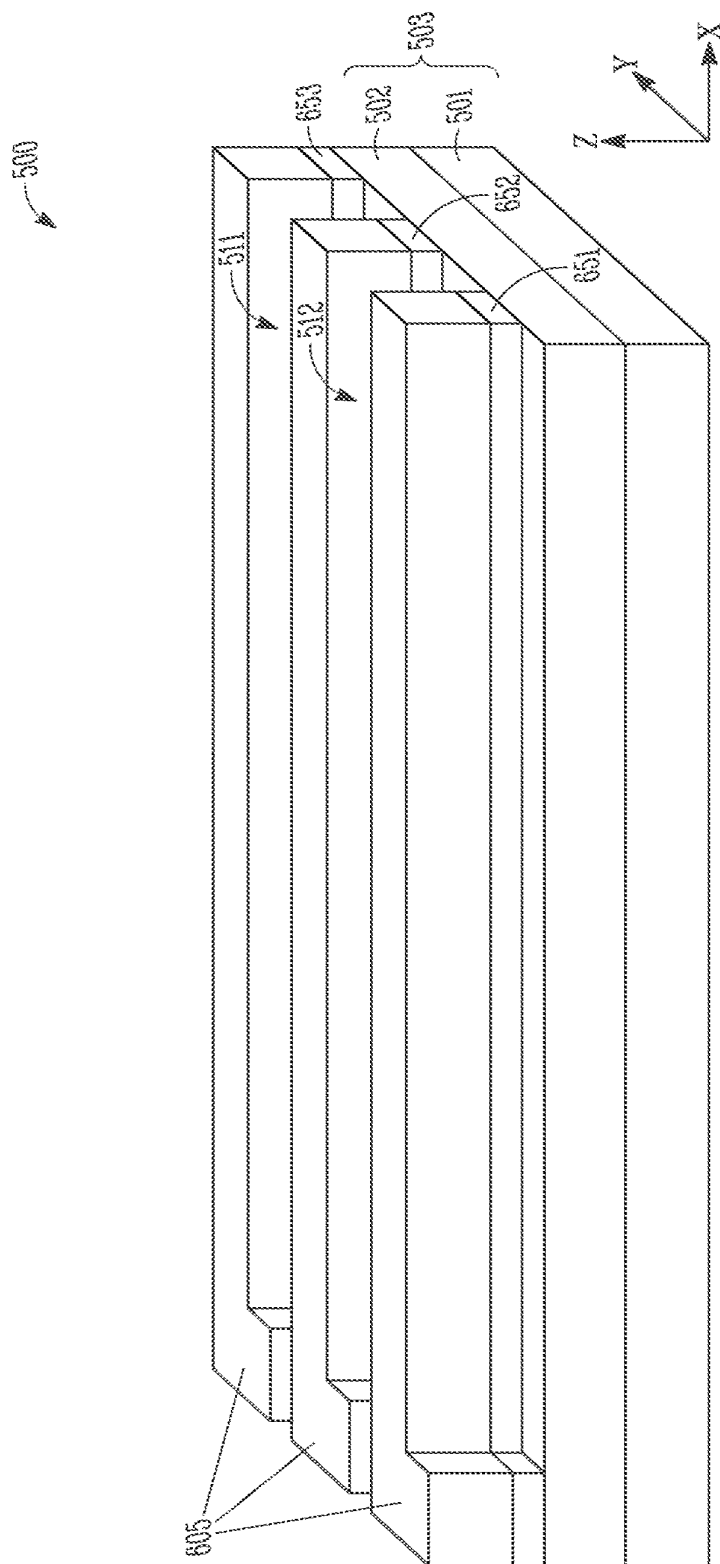


FIG. 6

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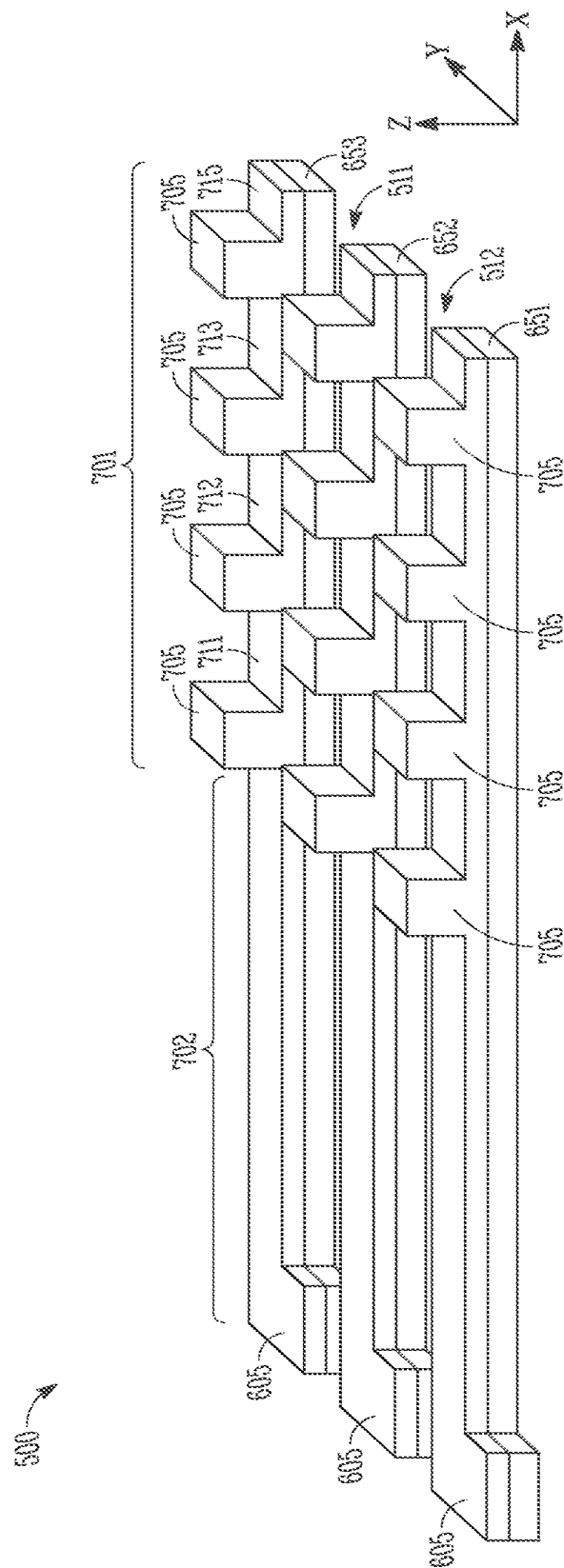
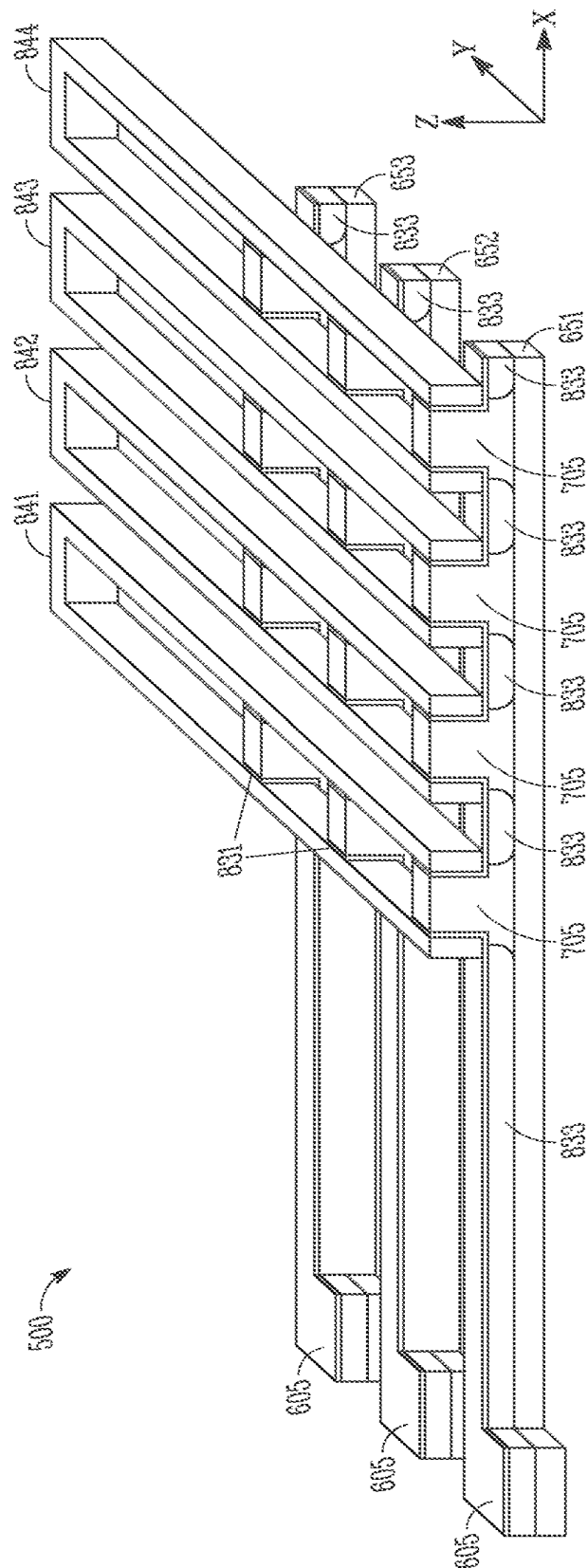
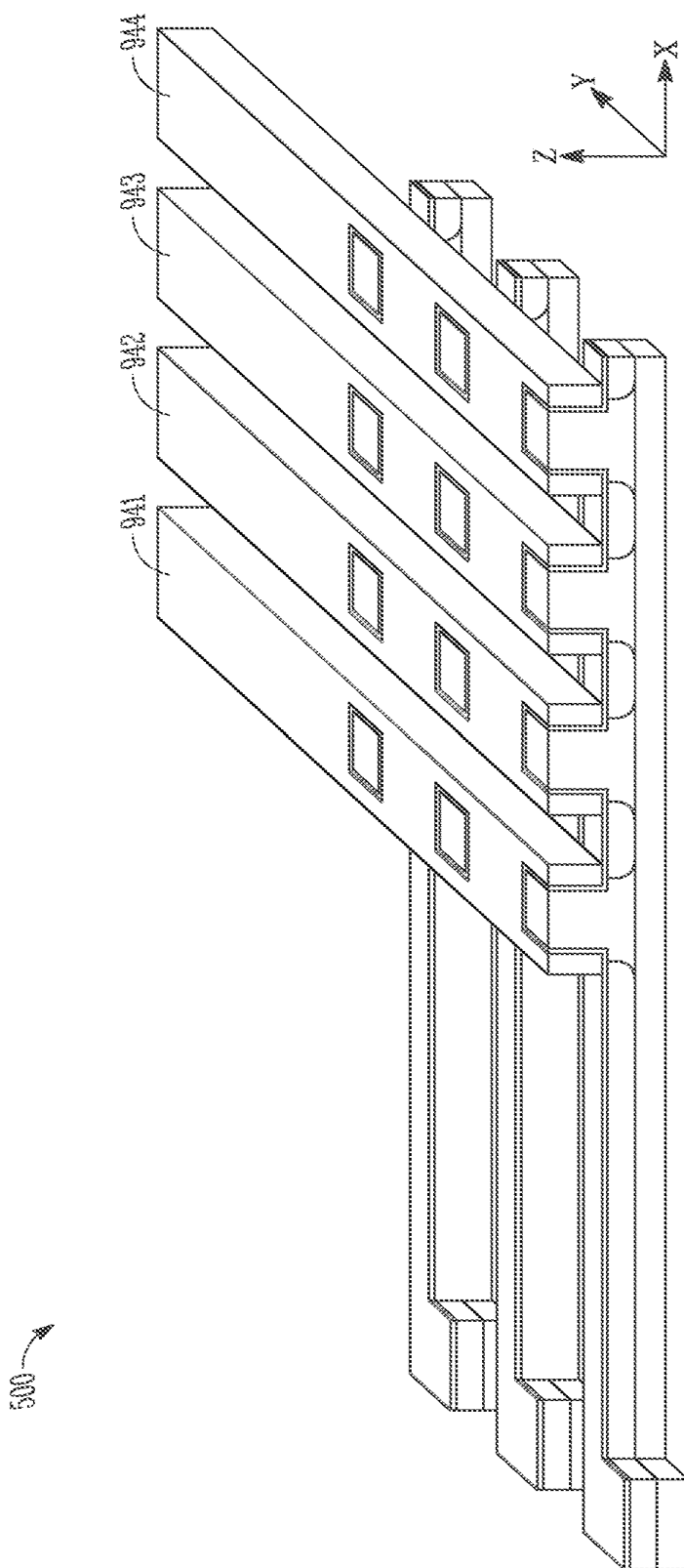


FIG. 7



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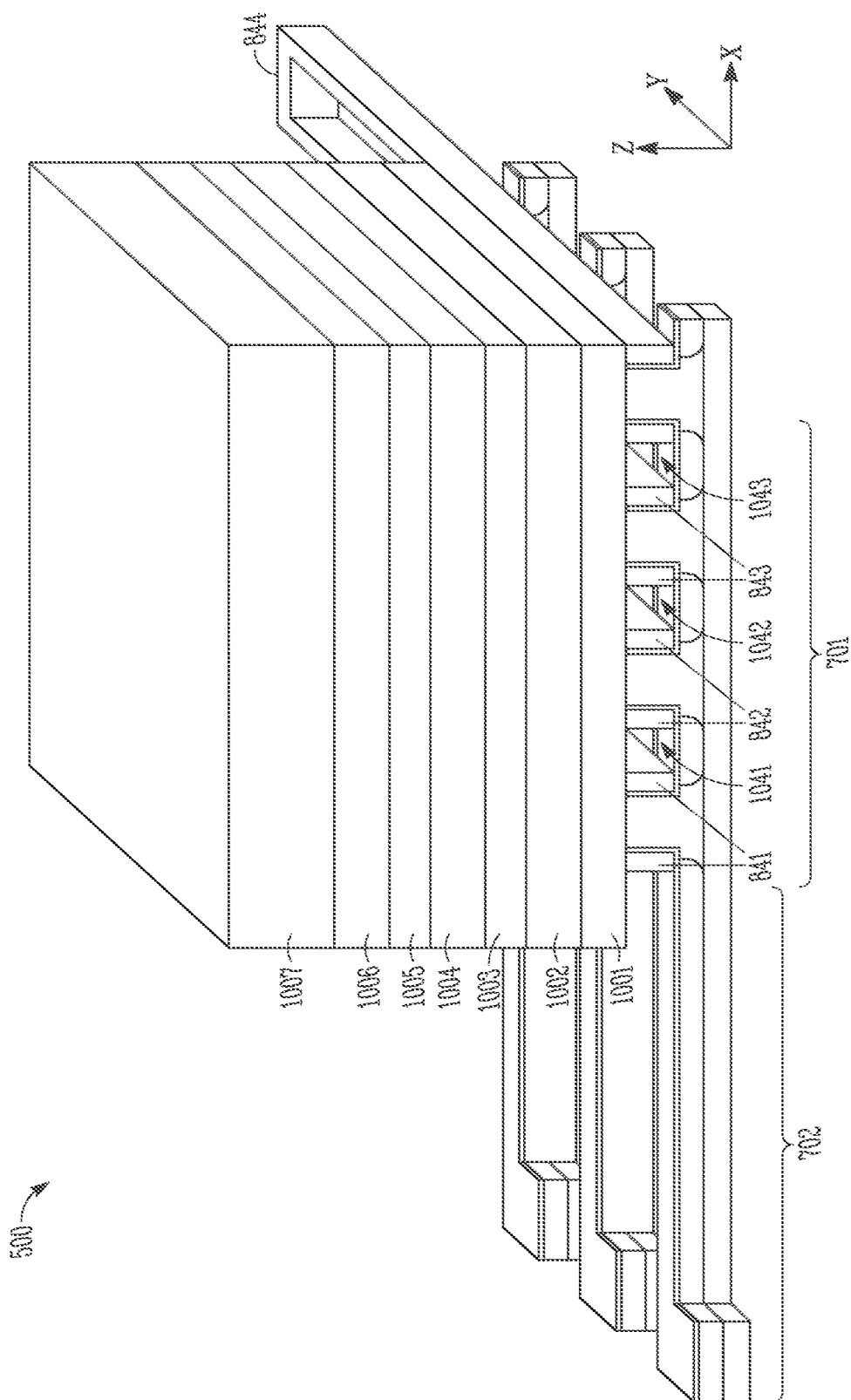


FIG. 10

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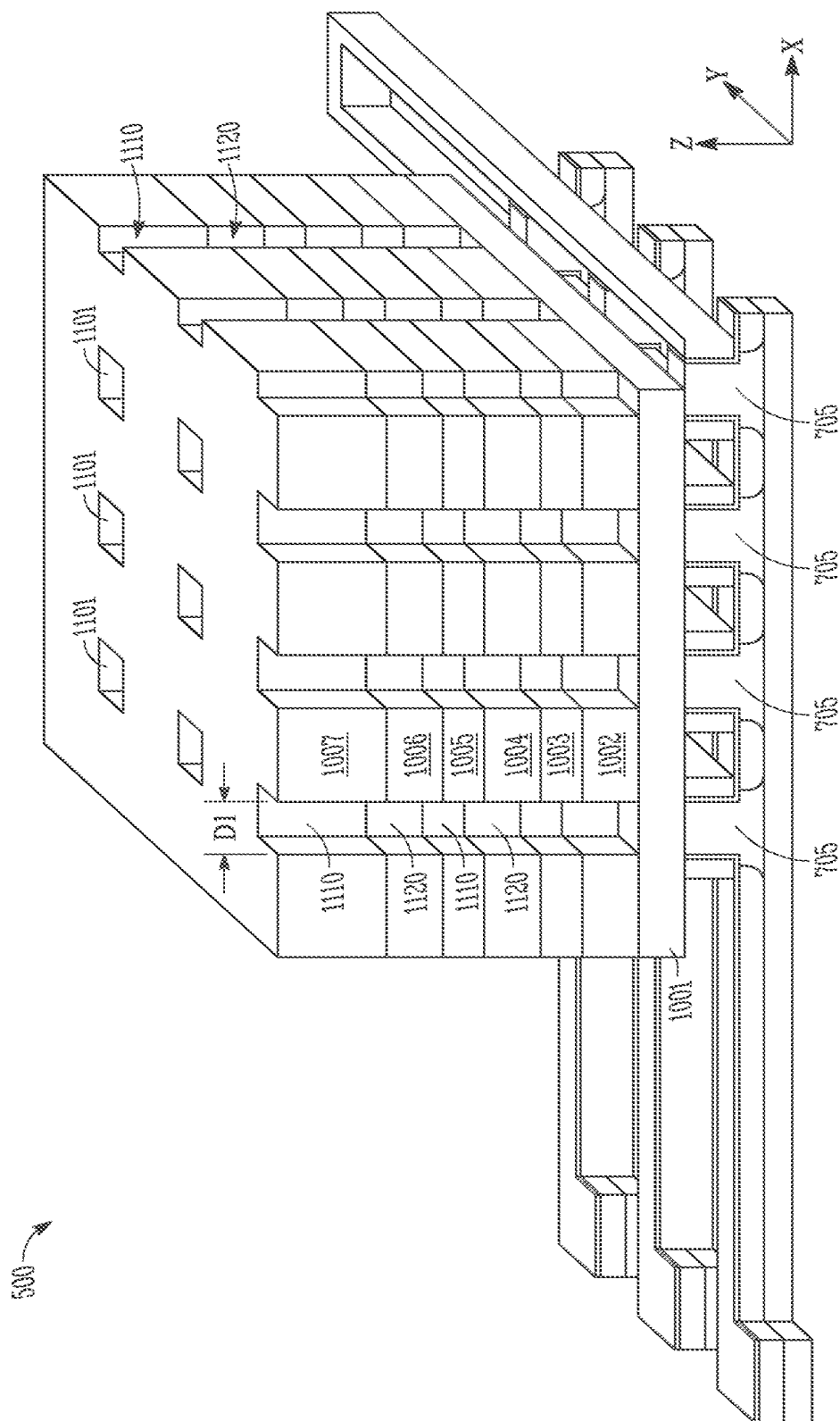


FIG. 11

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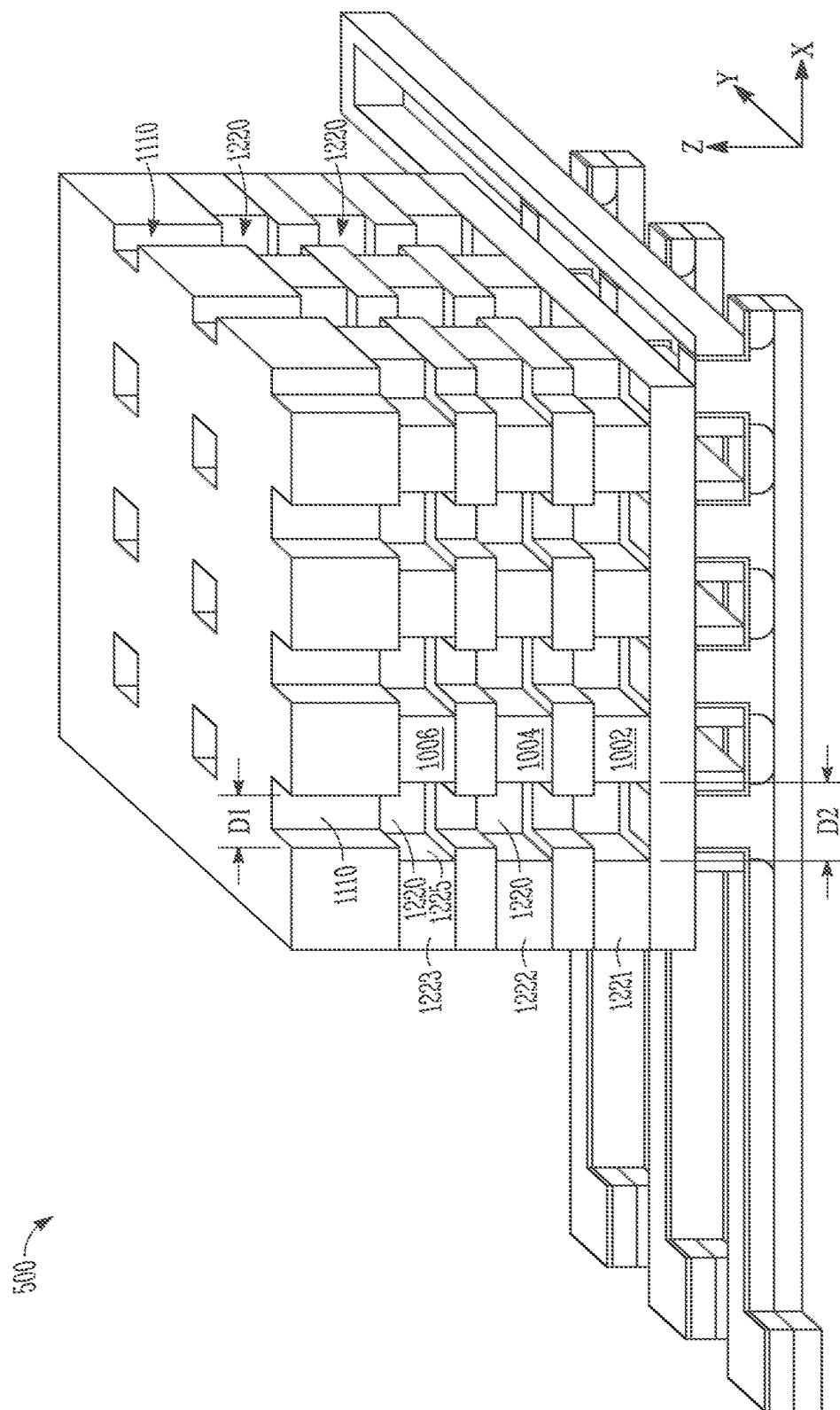


FIG. 12

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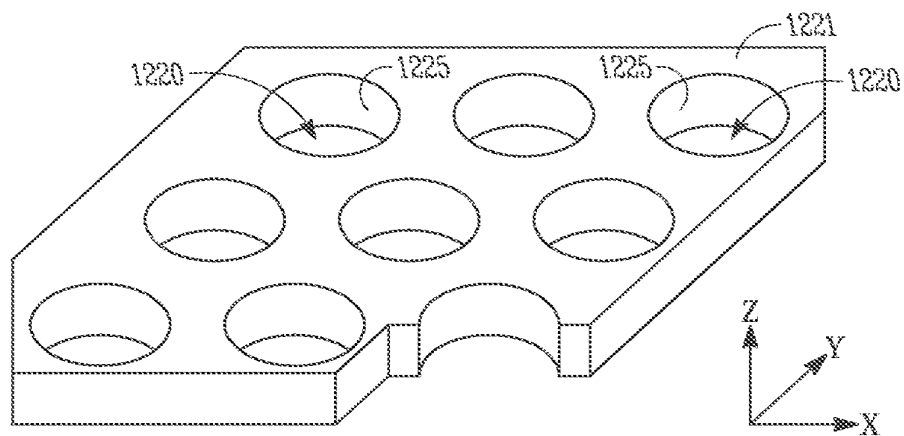


FIG. 13

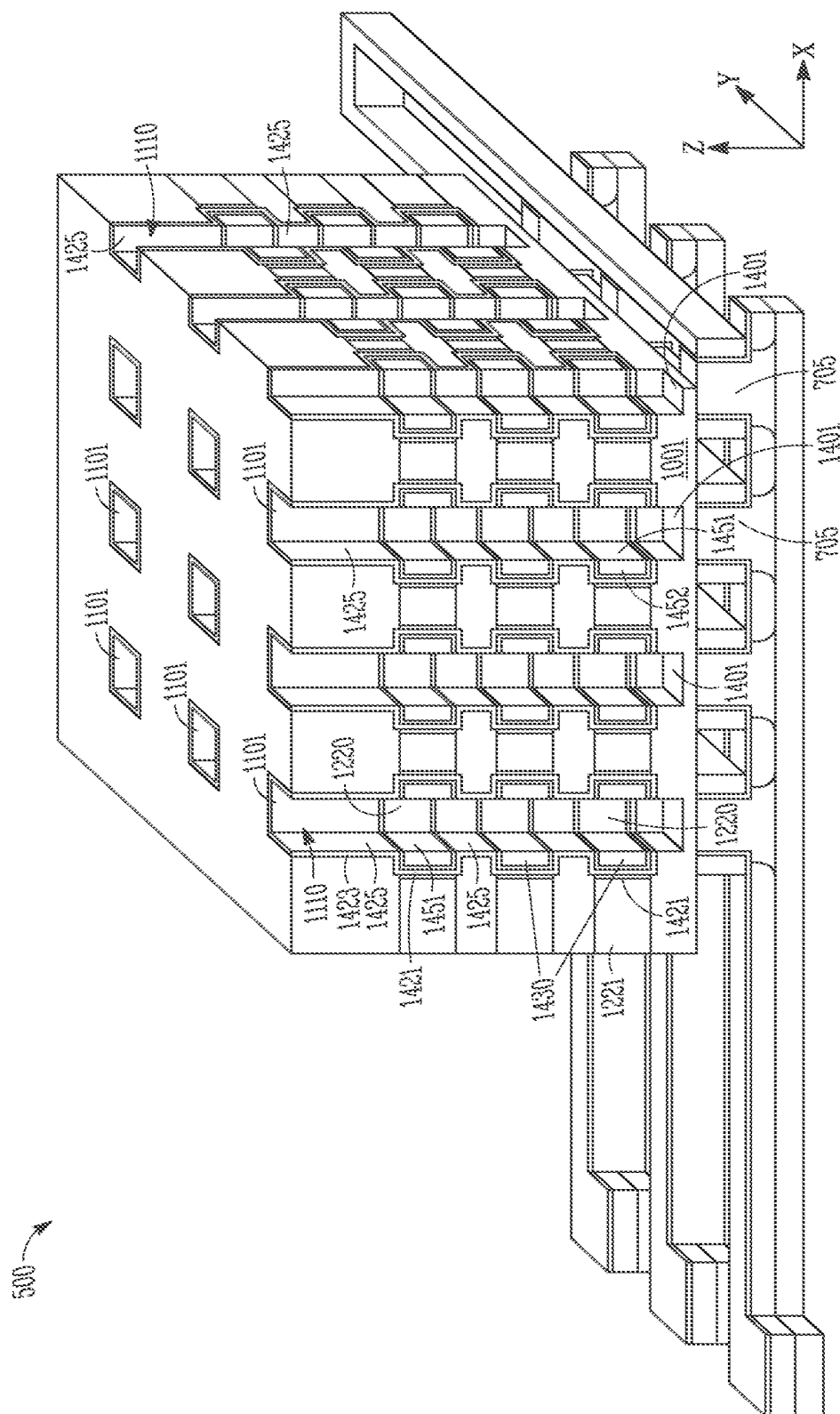


FIG. 14

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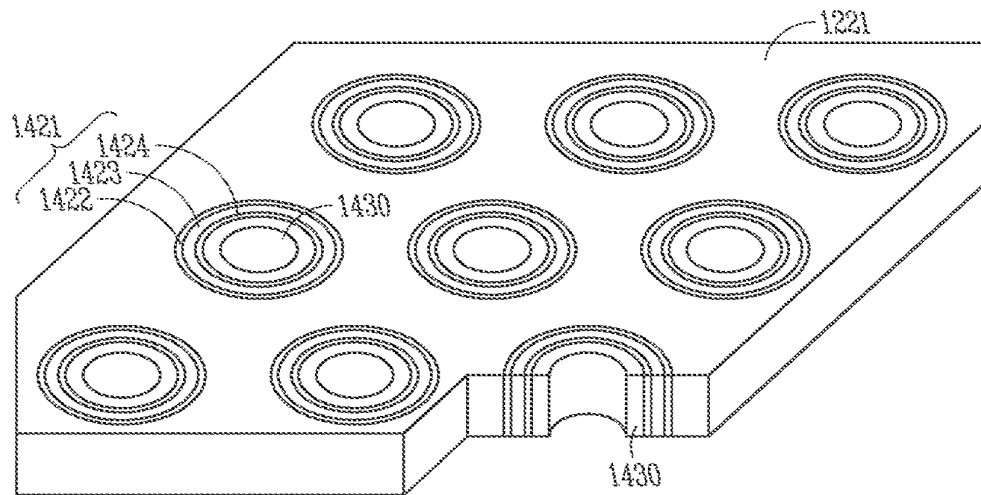
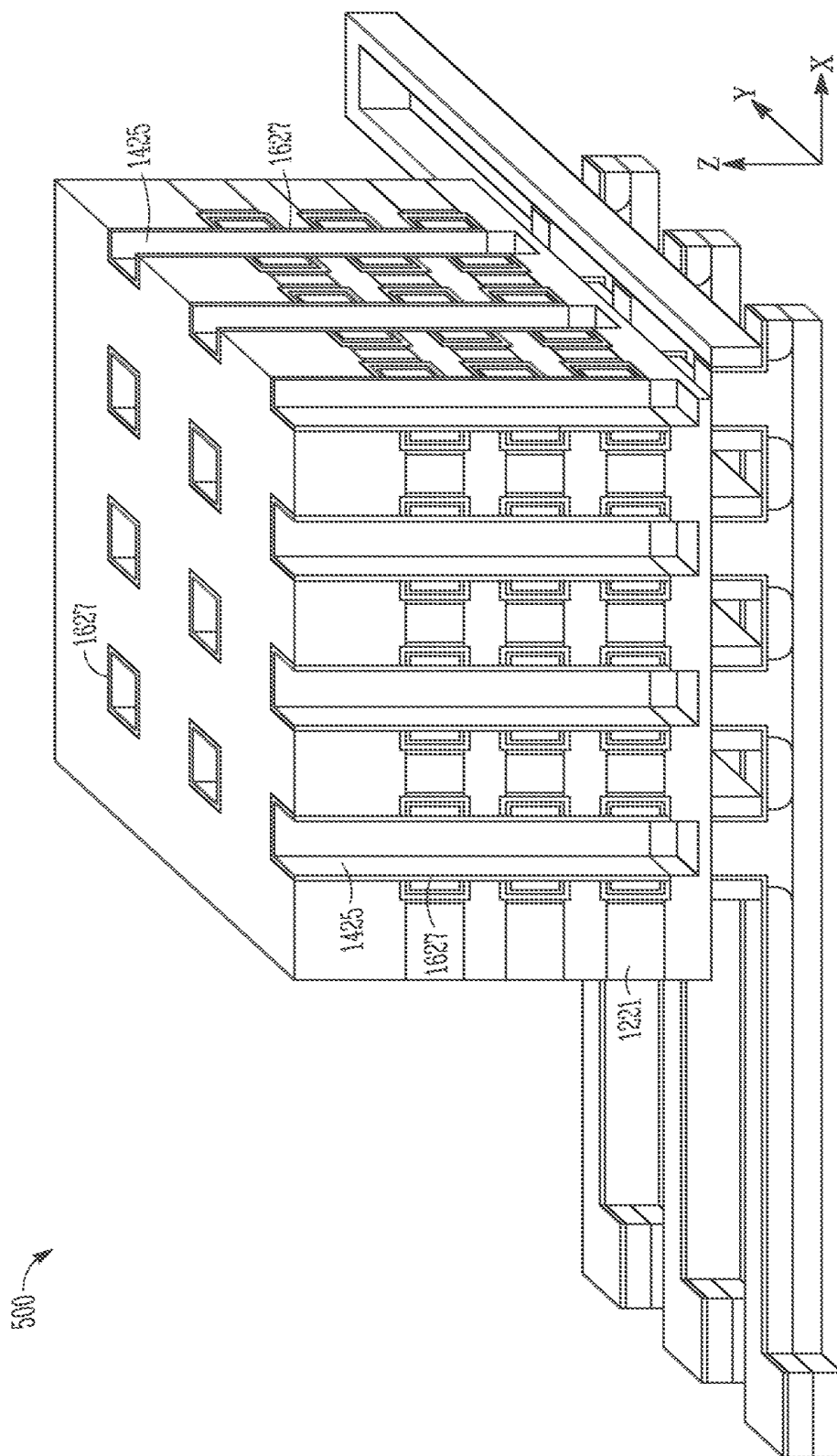


FIG. 15

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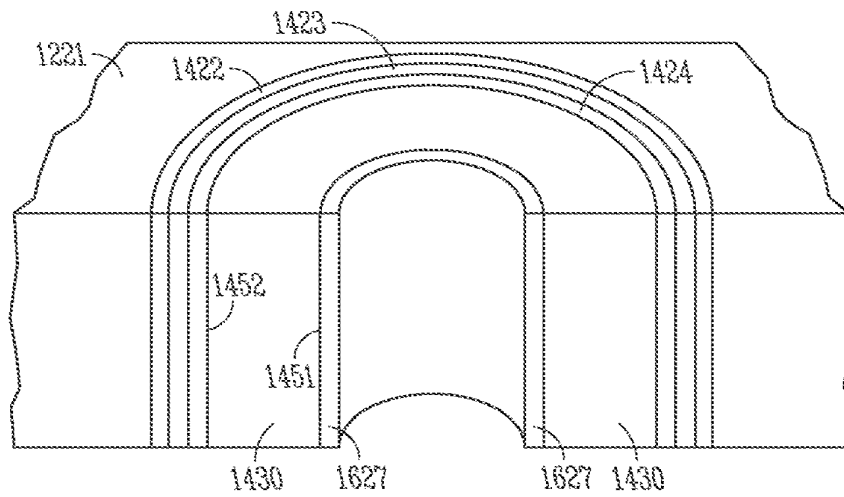


FIG. 17

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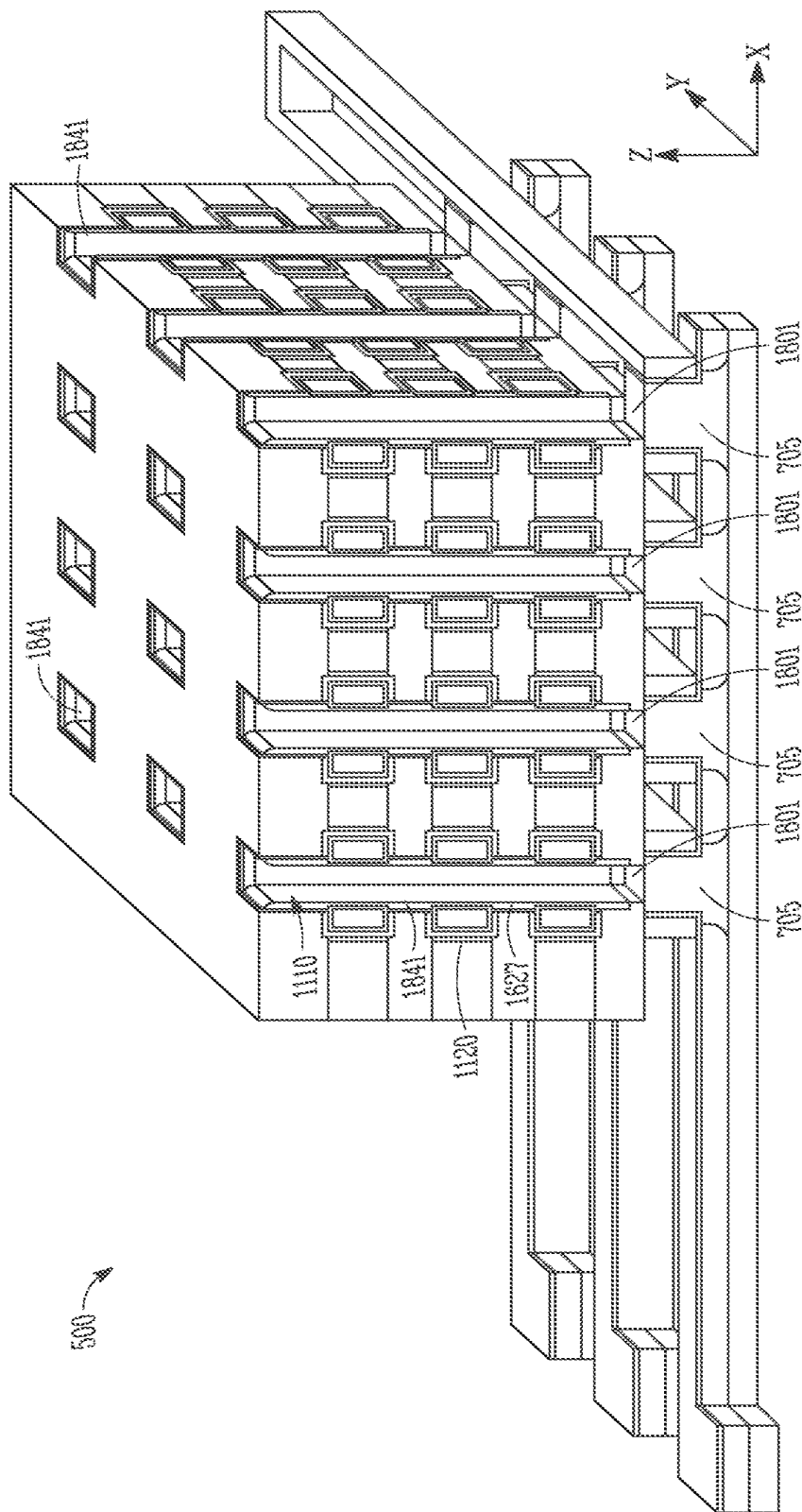


FIG. 18

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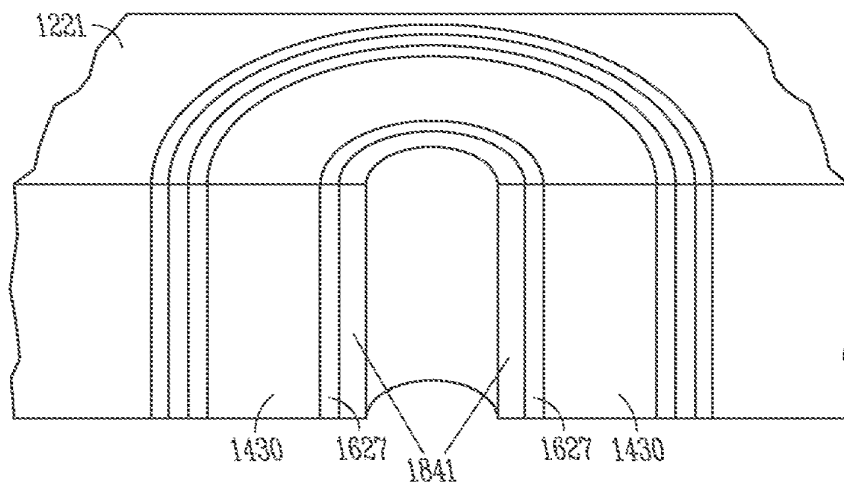


FIG. 19

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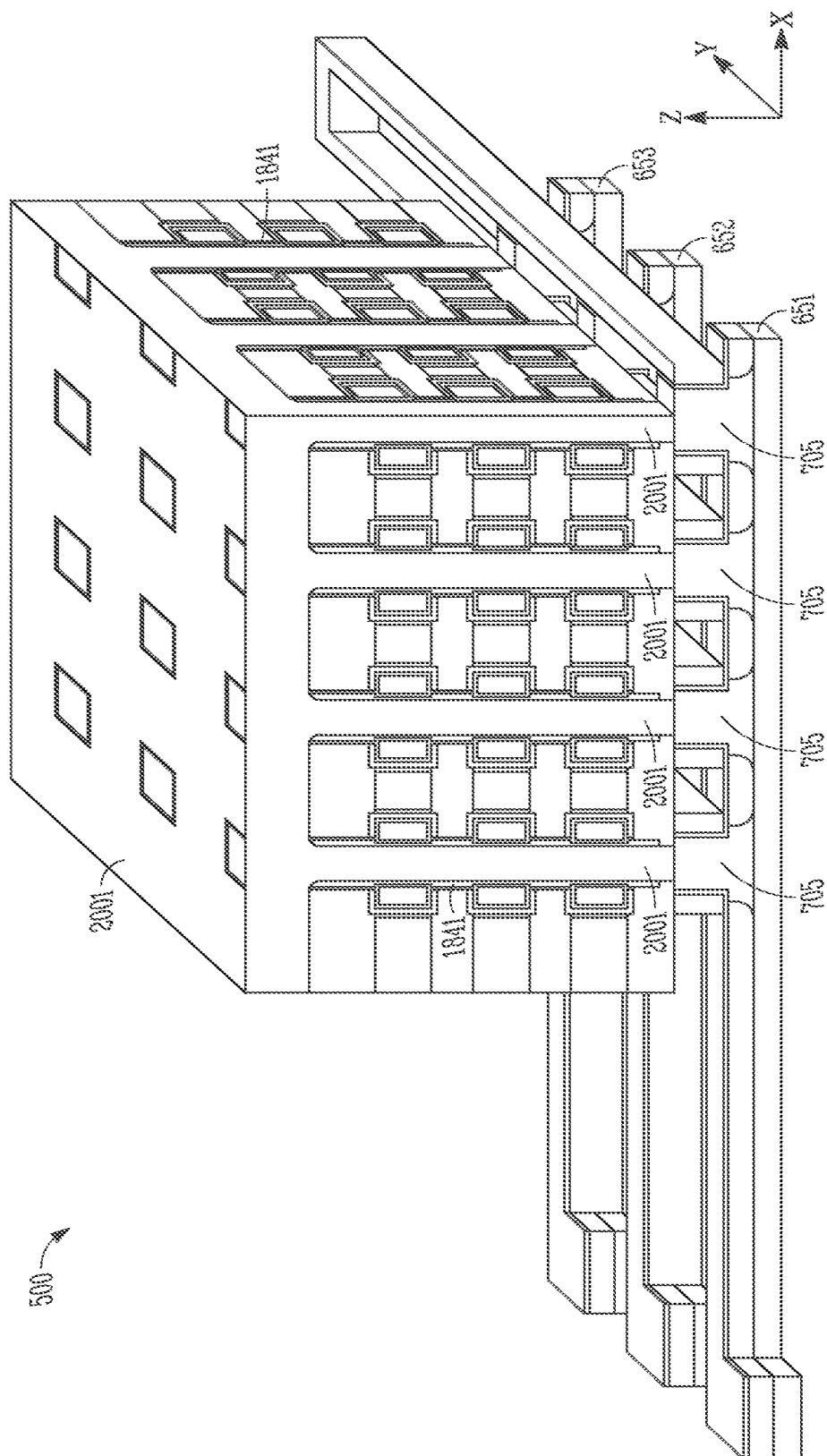
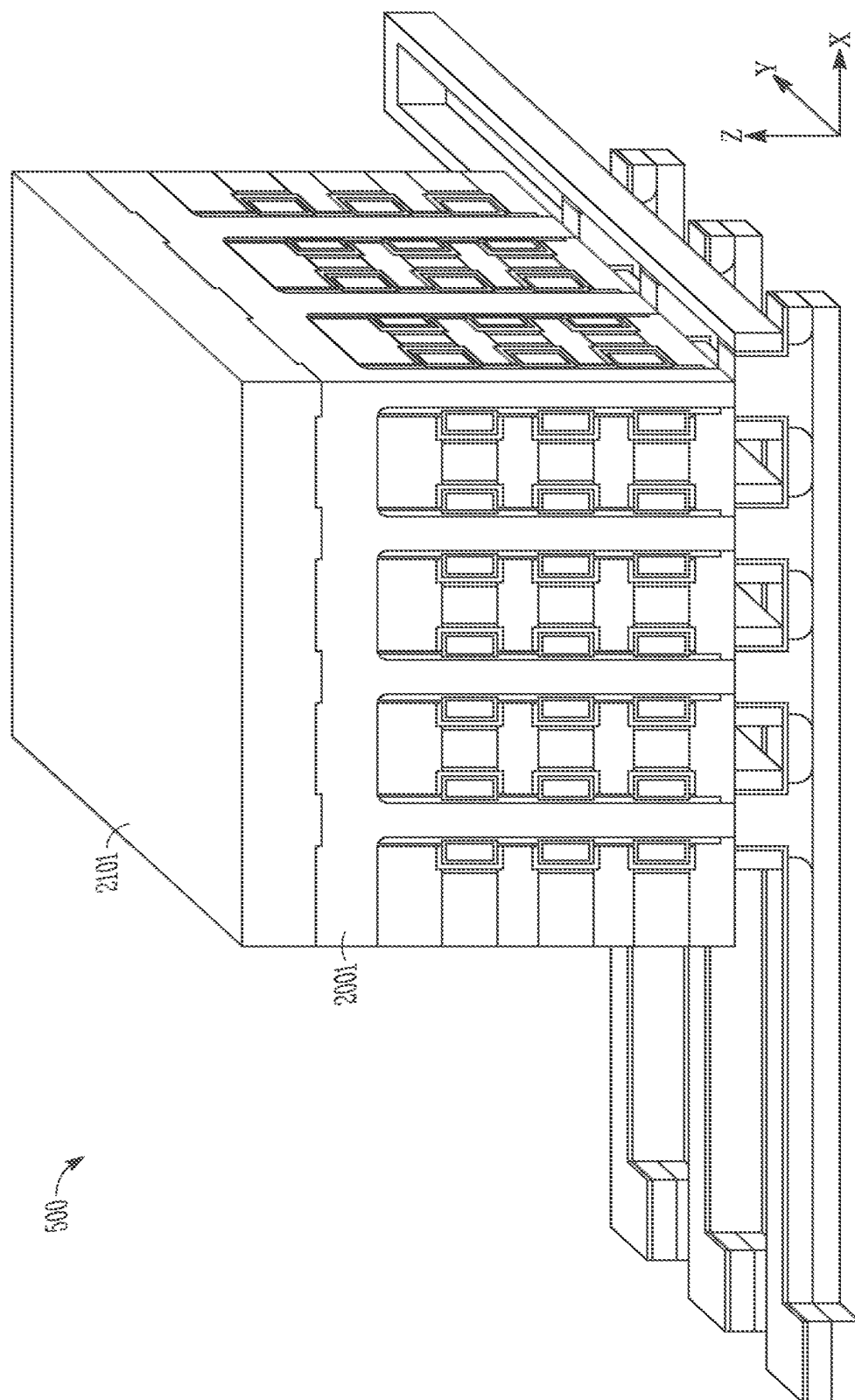


FIG. 20

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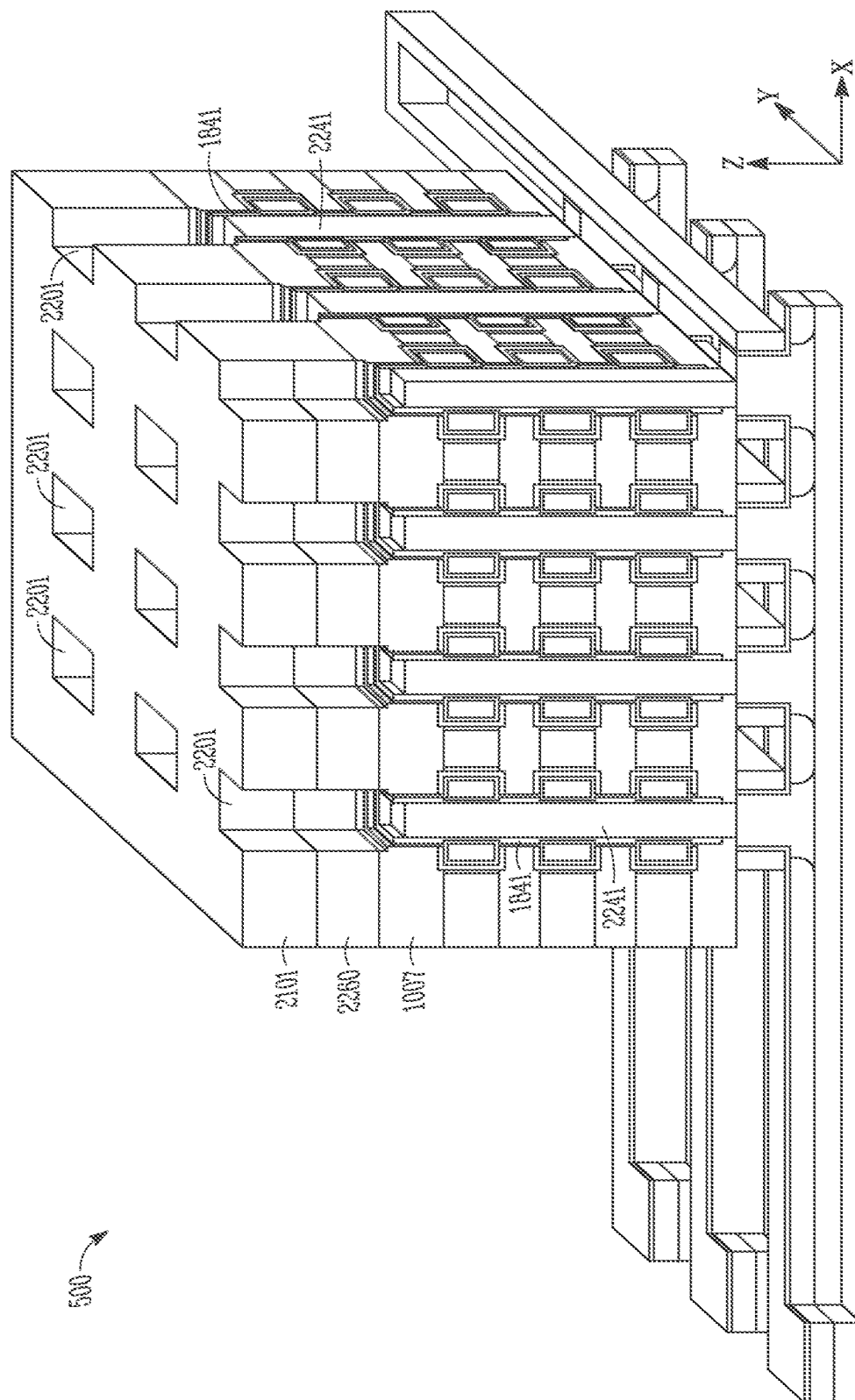
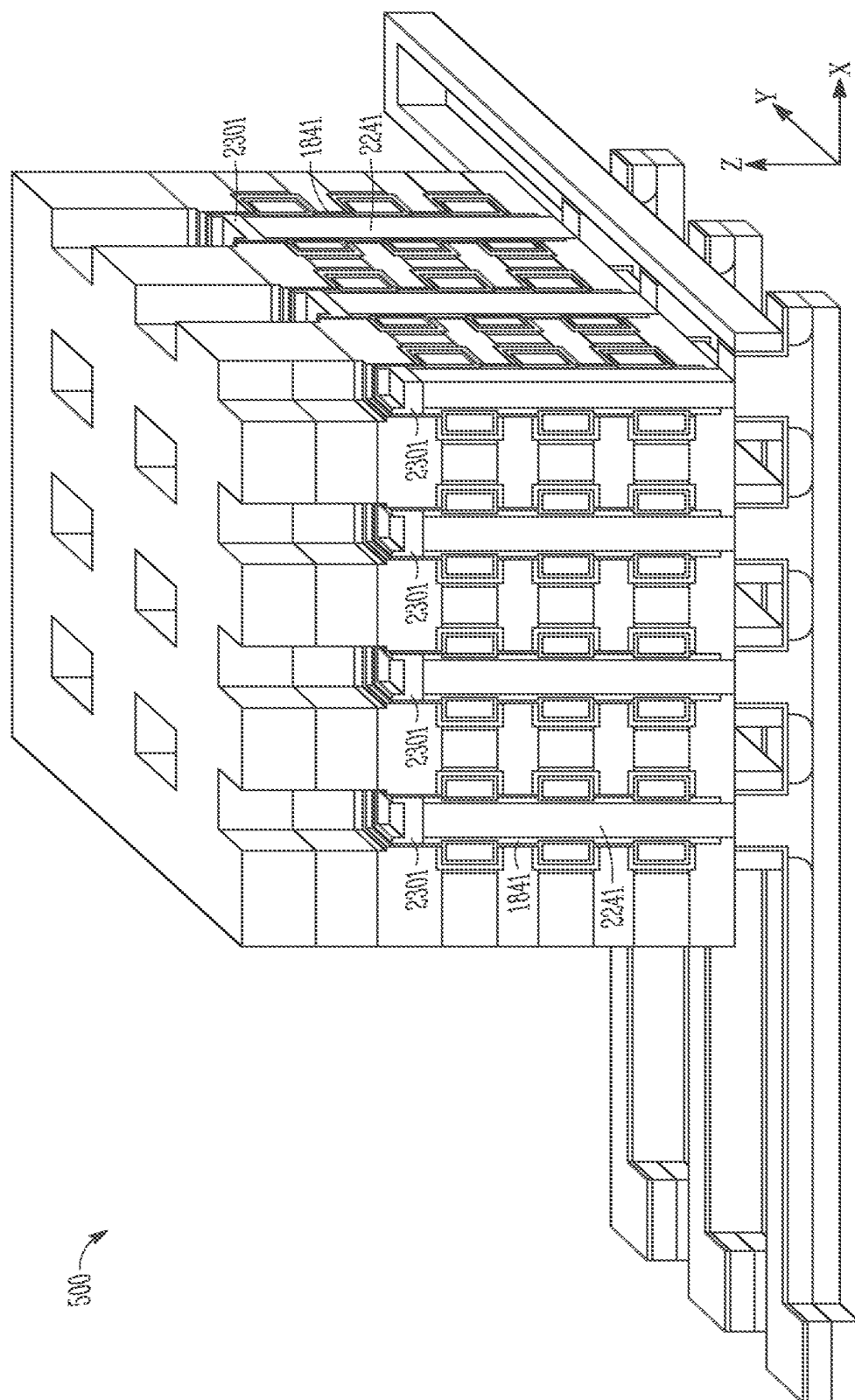


FIG. 22

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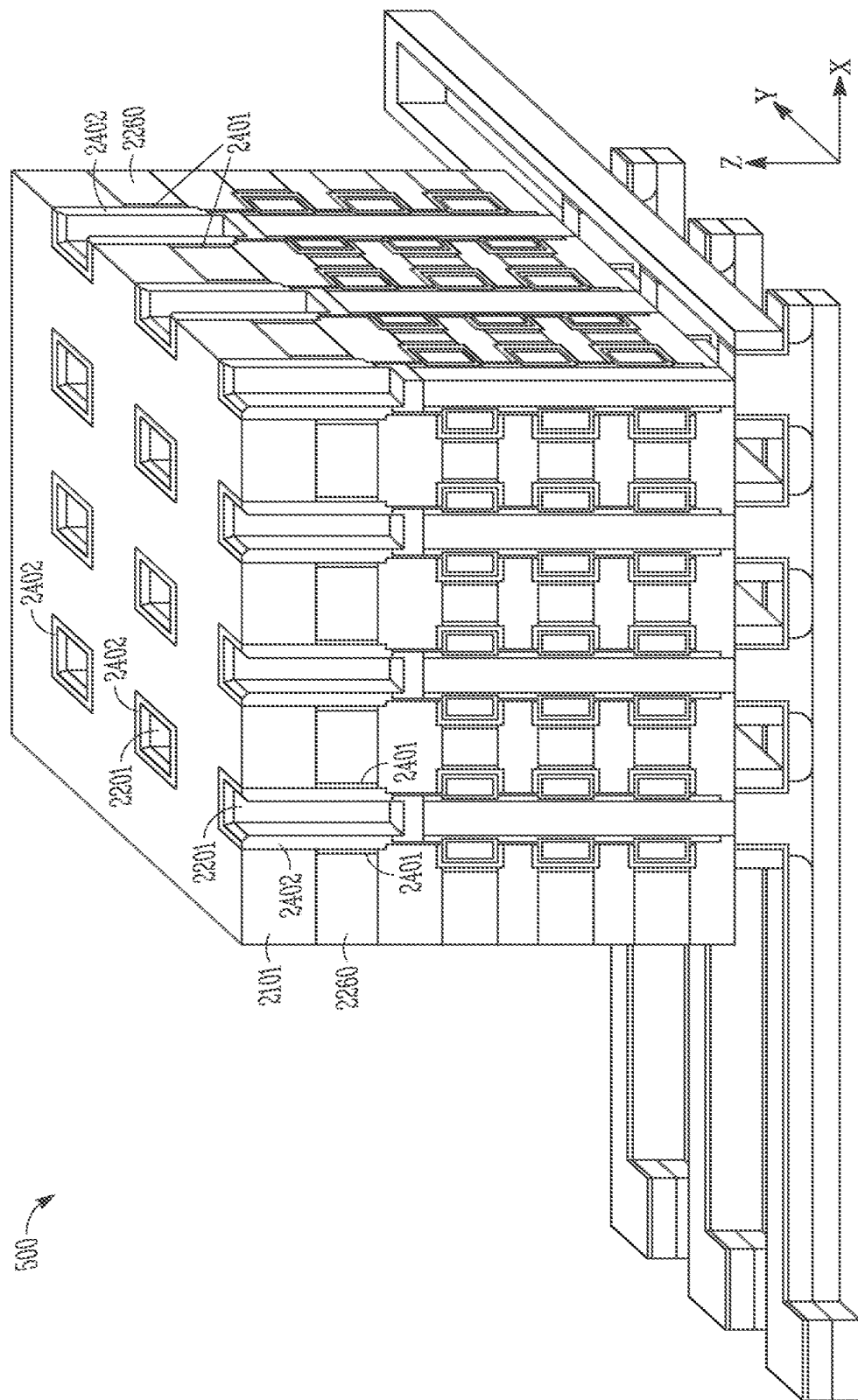


FIG. 24

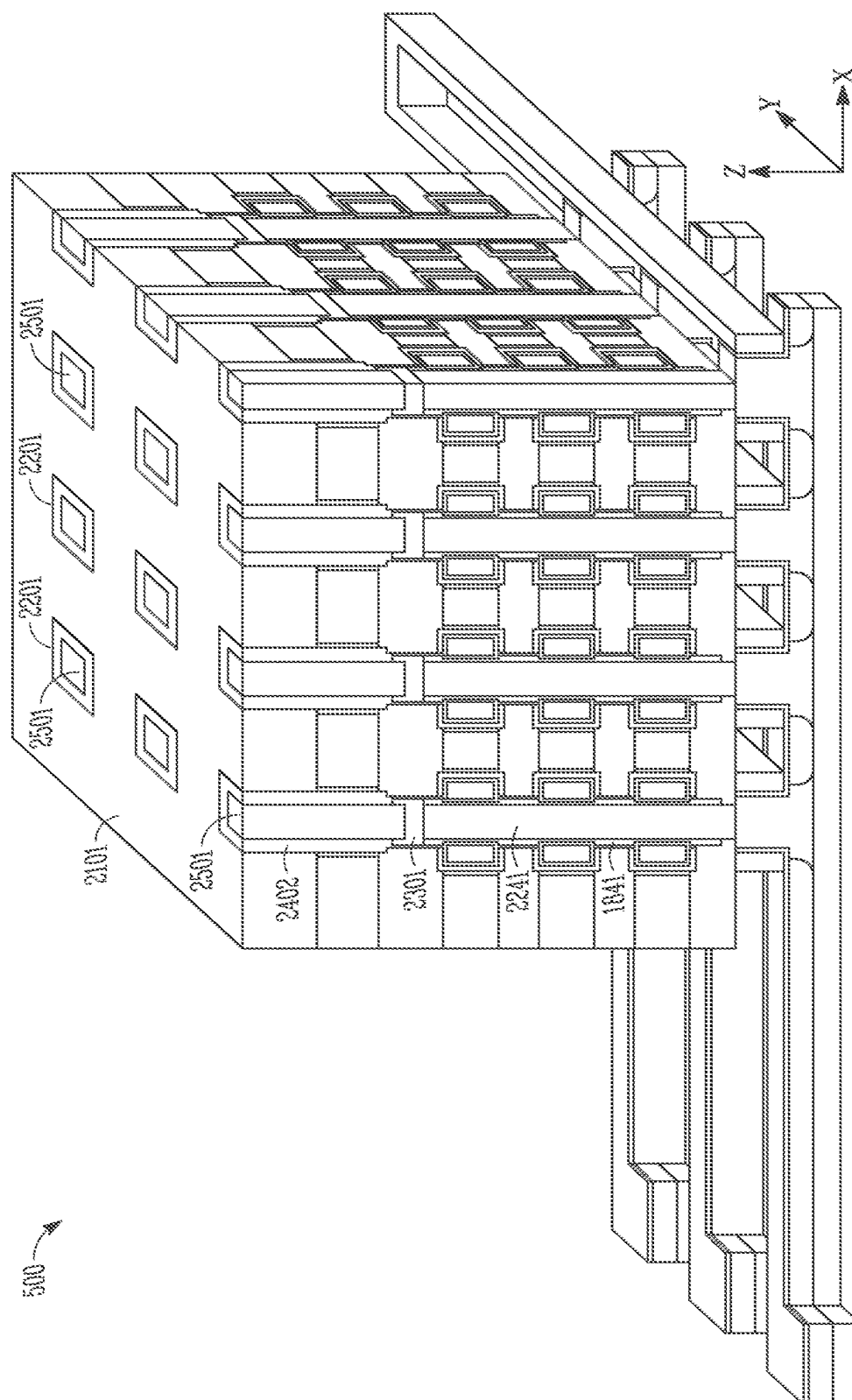


FIG. 25

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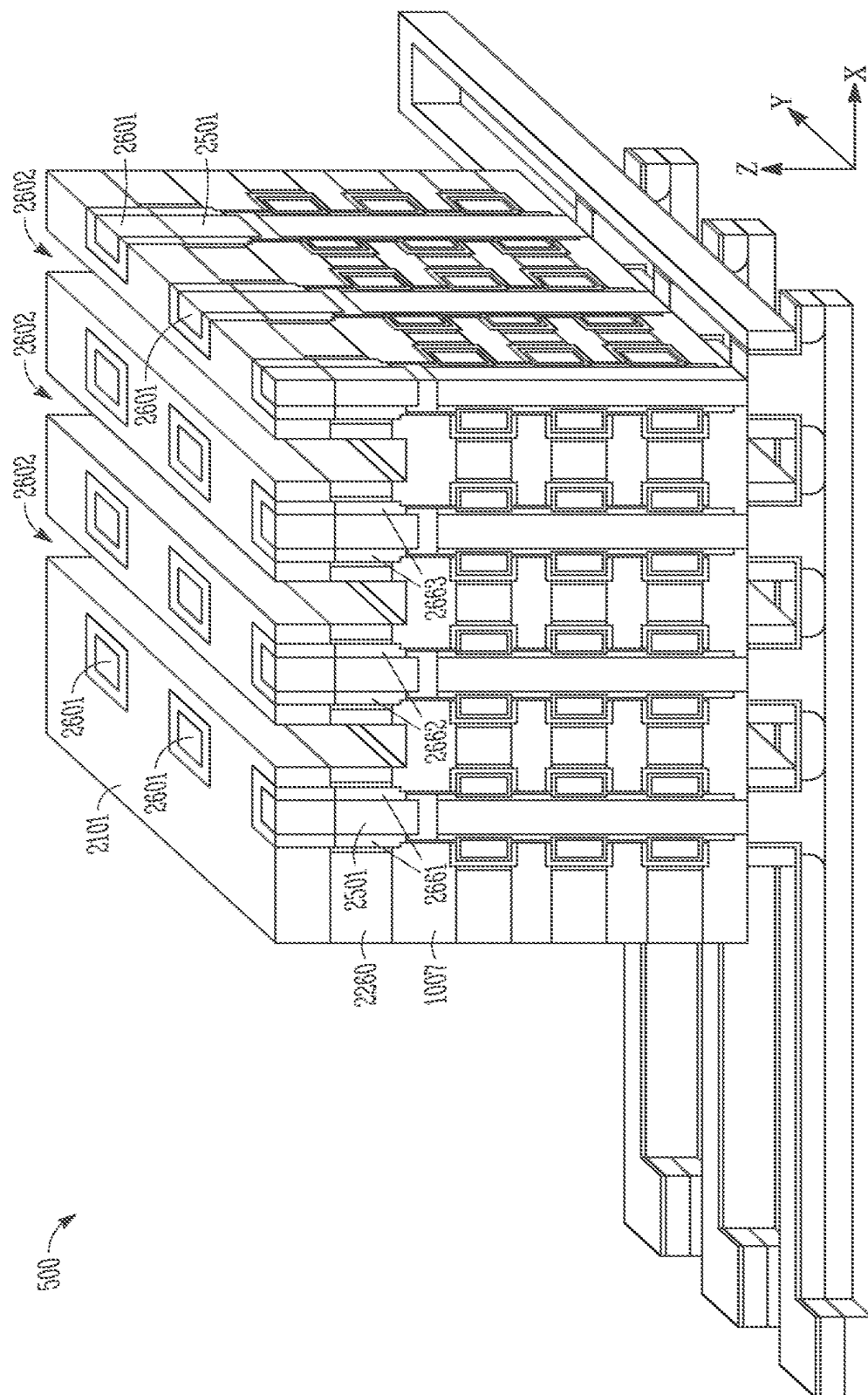


FIG. 26

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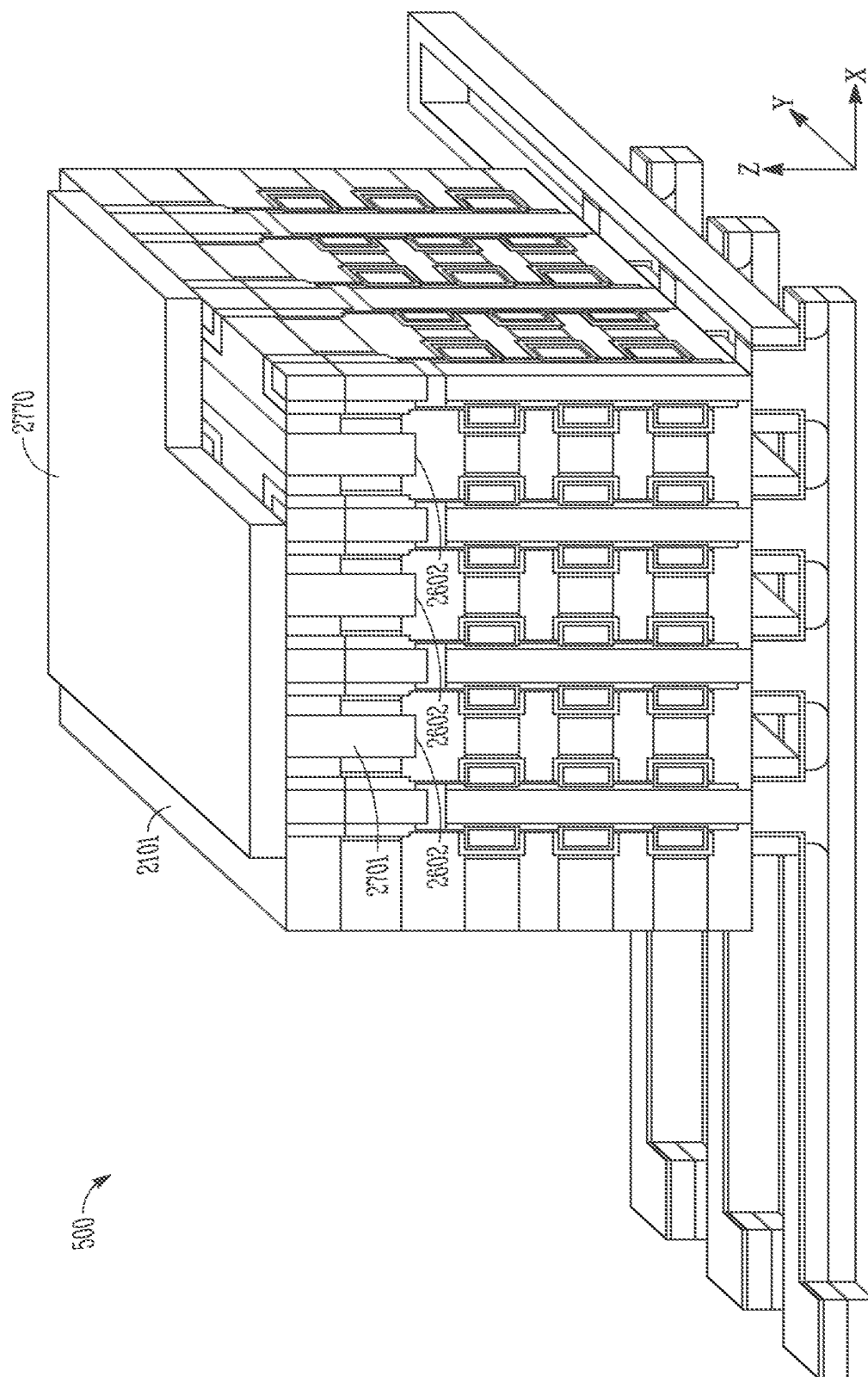
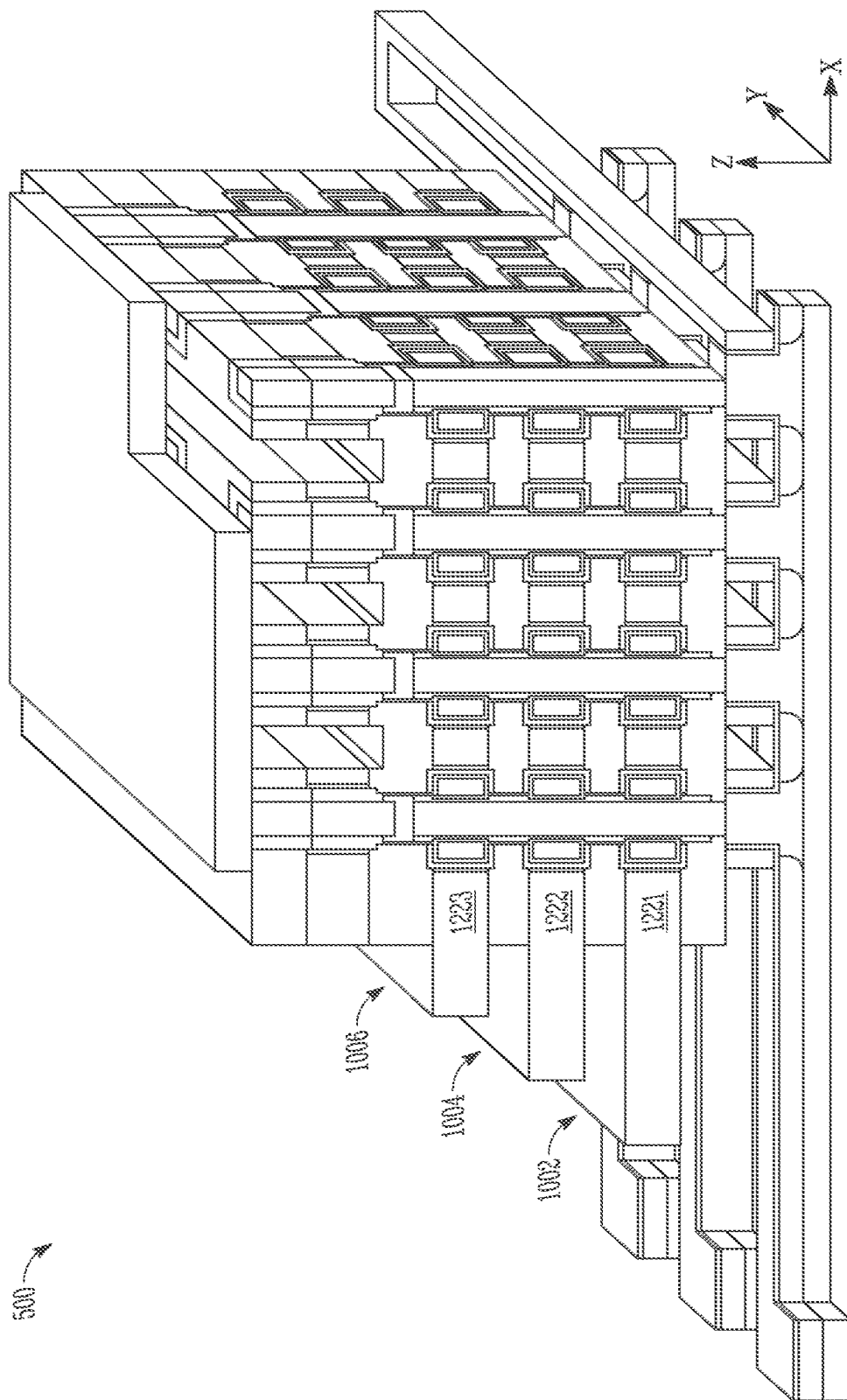


FIG. 27

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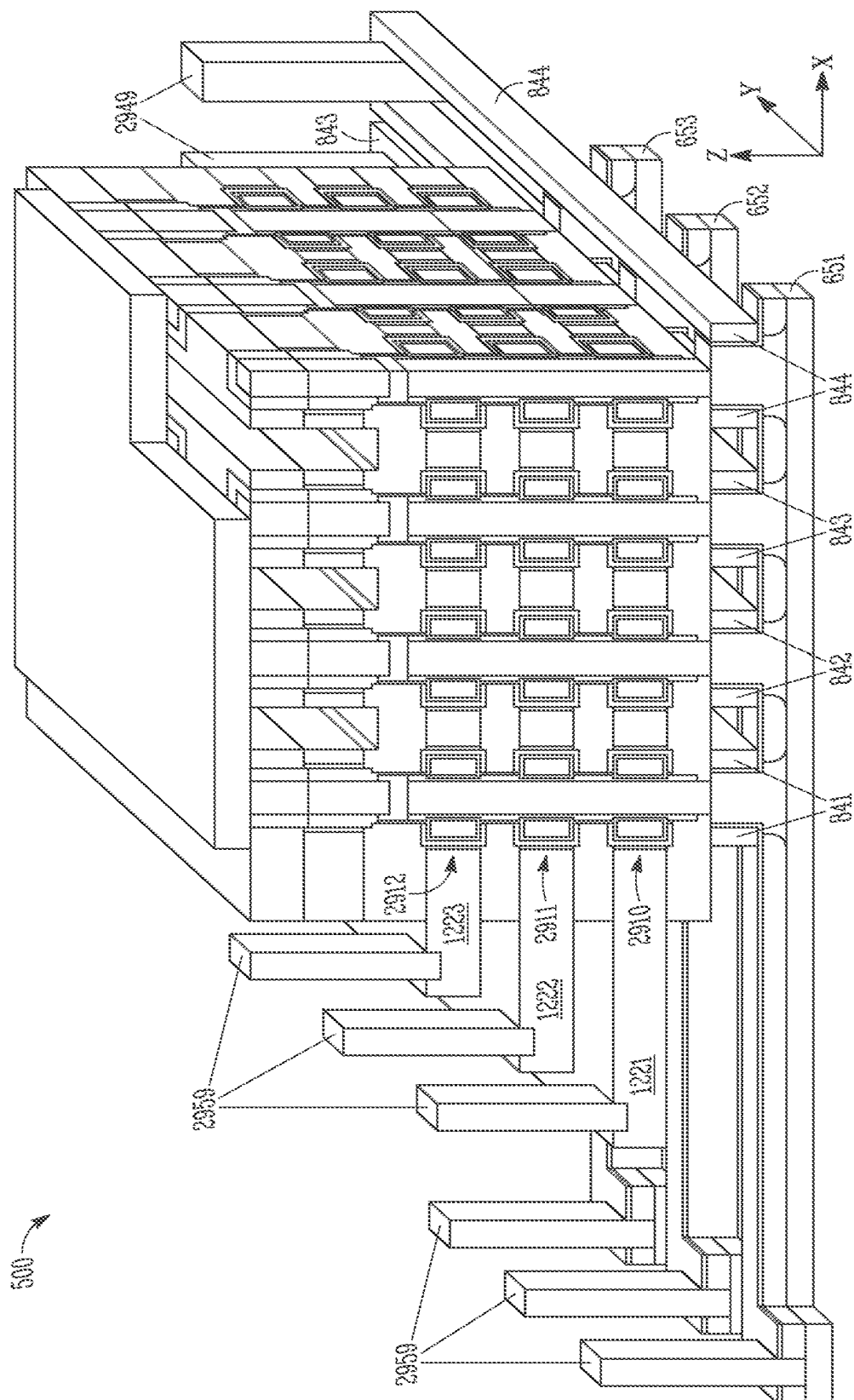


FIG. 29

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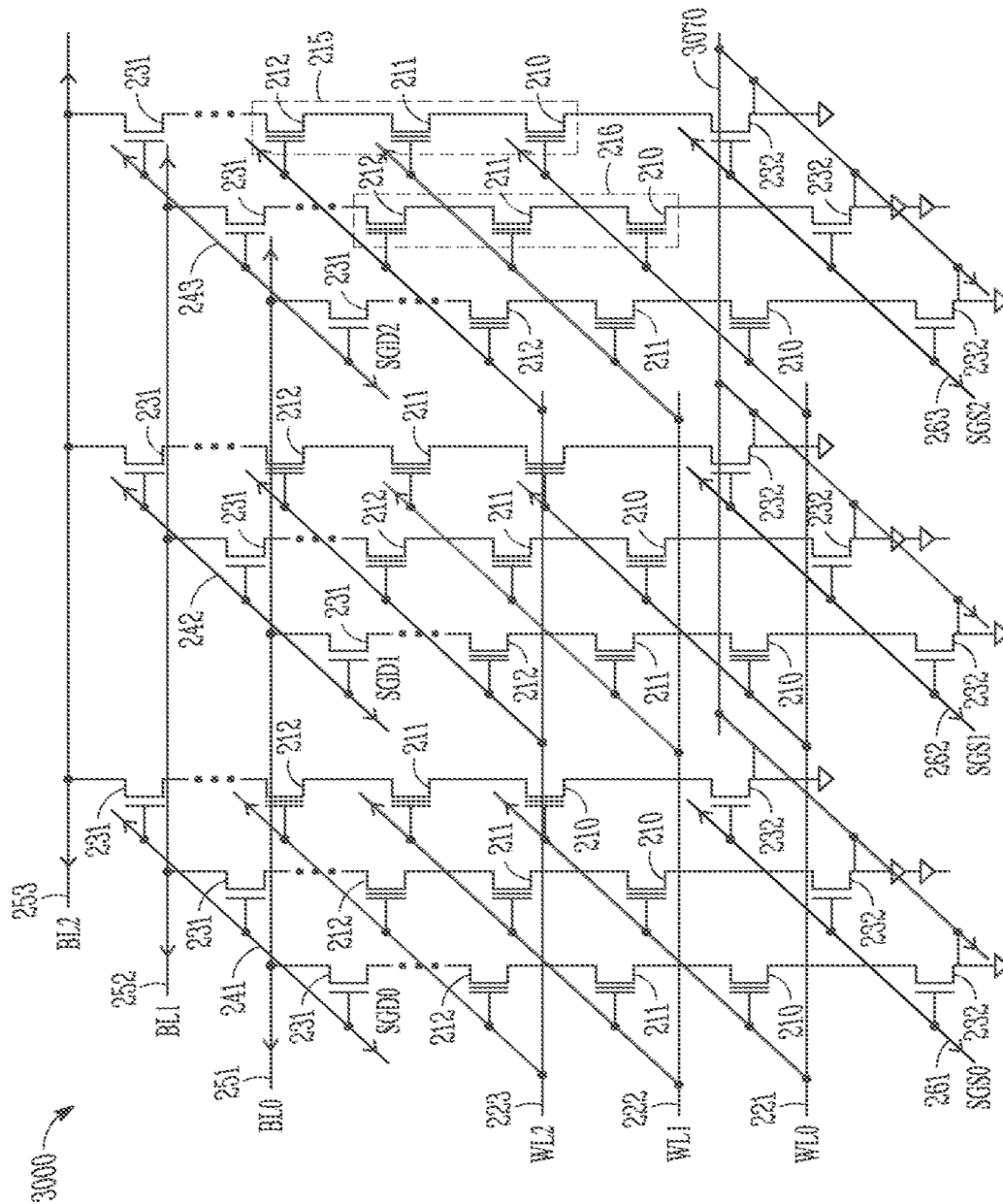
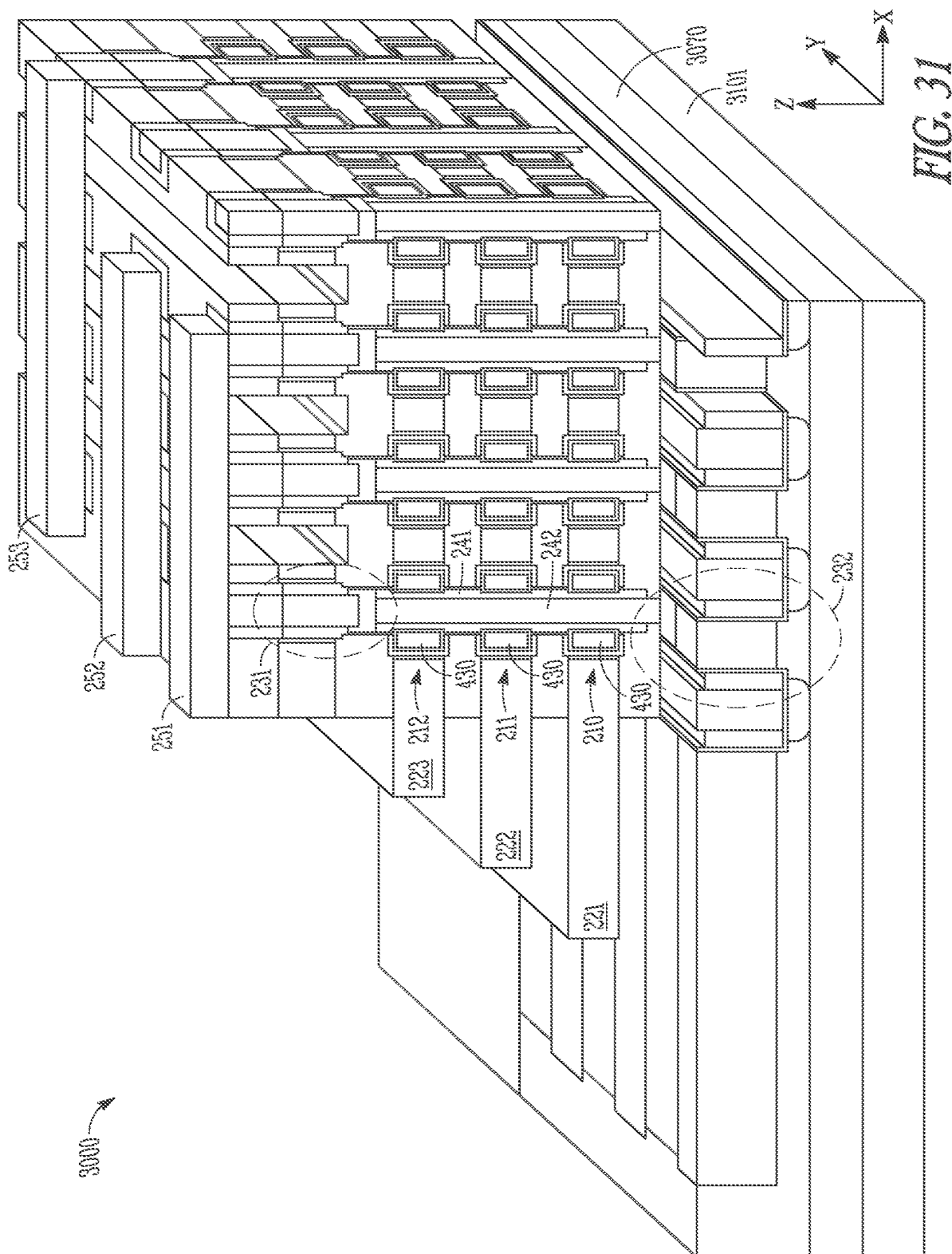


FIG. 30

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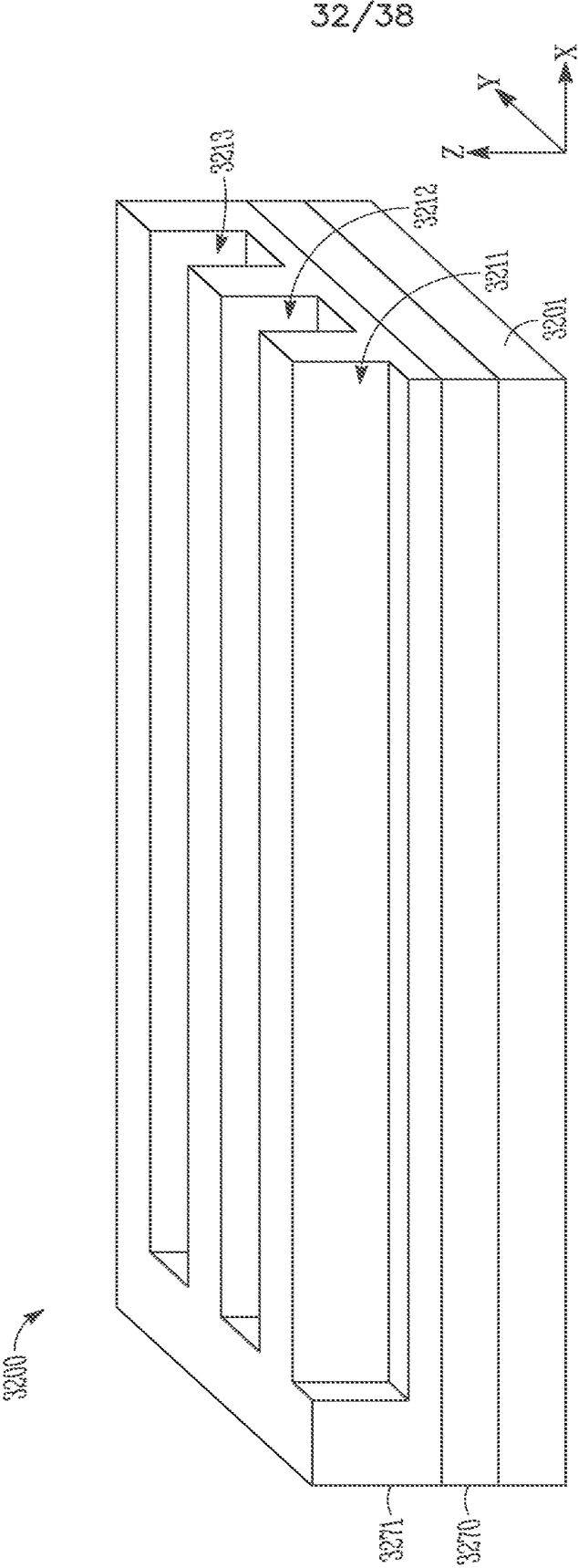


FIG. 32

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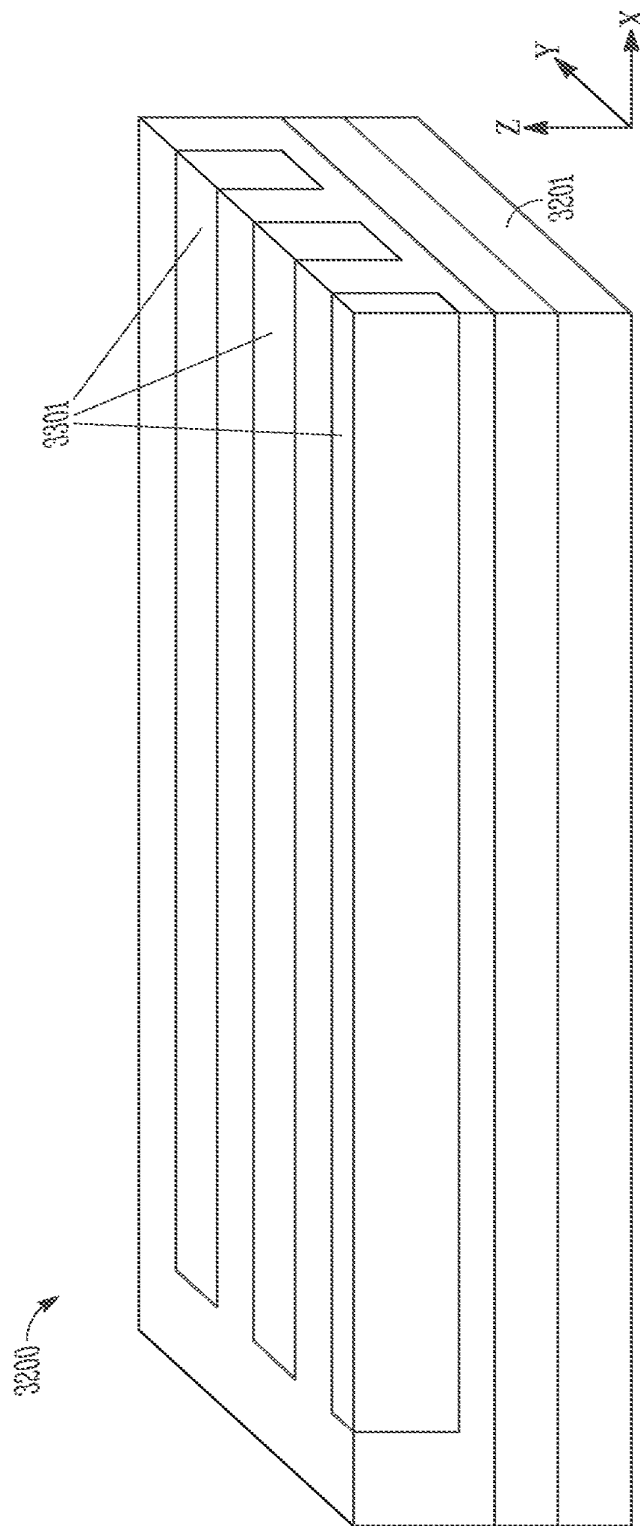


FIG. 33

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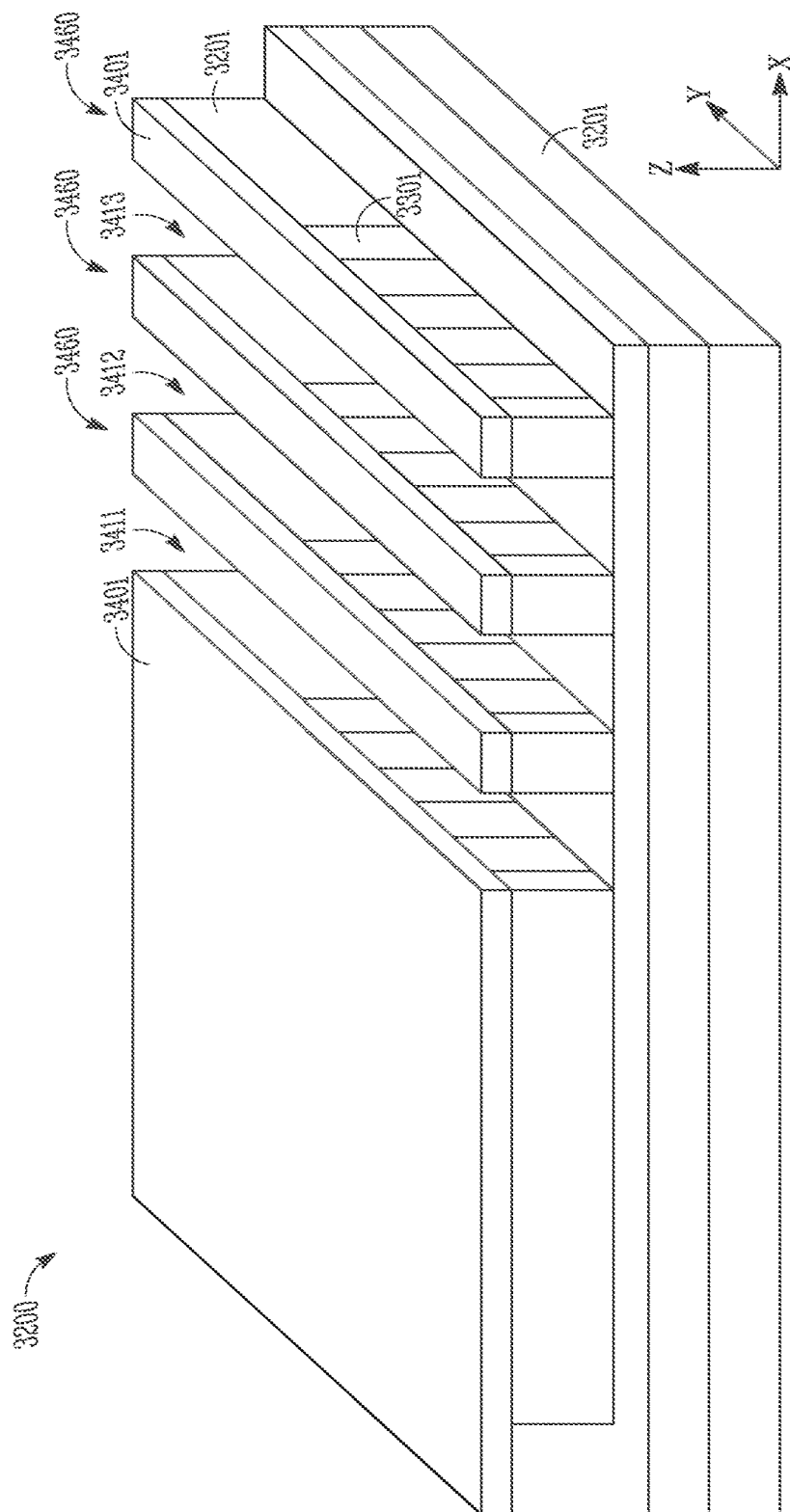


FIG. 34

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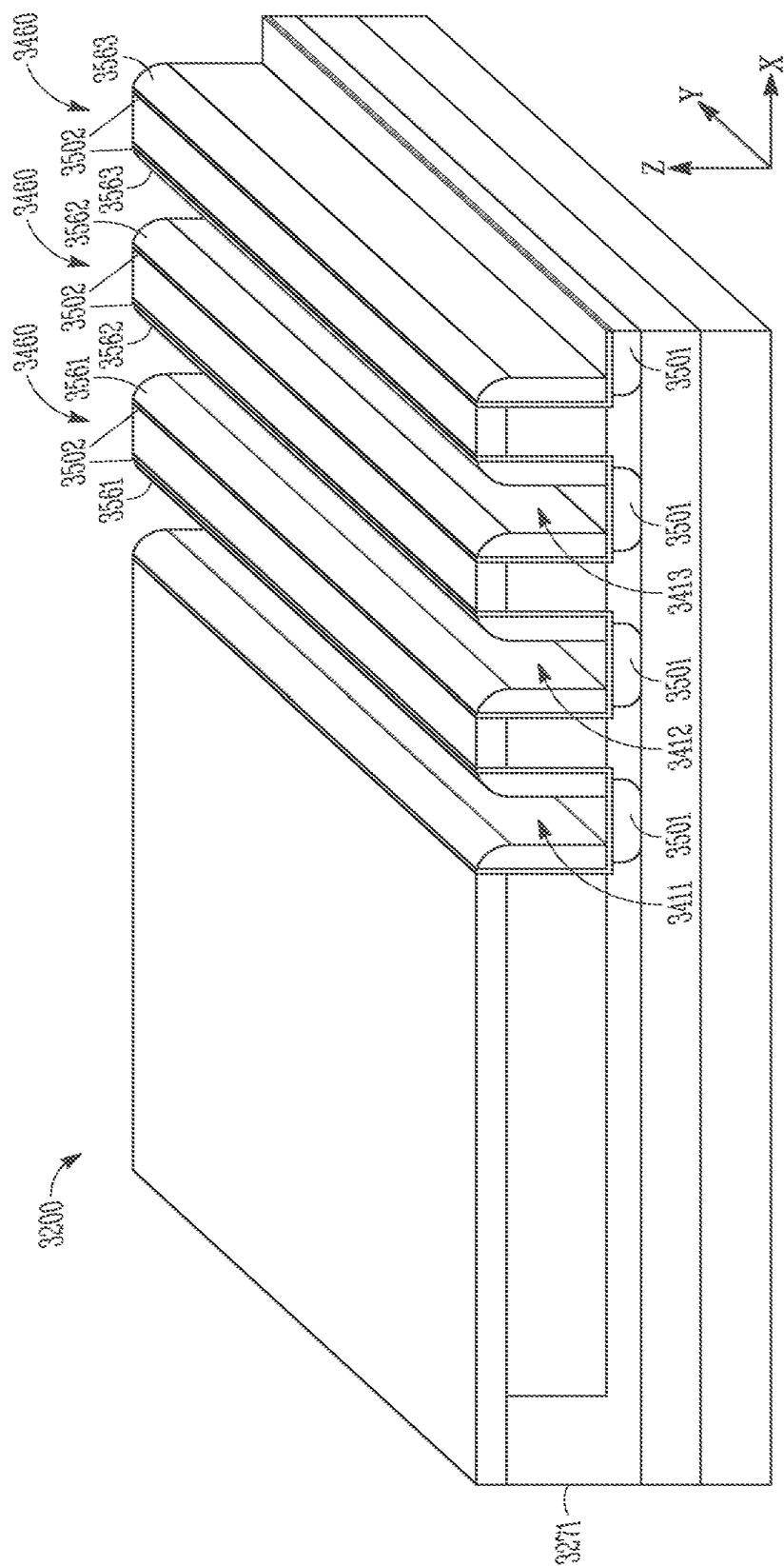


FIG. 35

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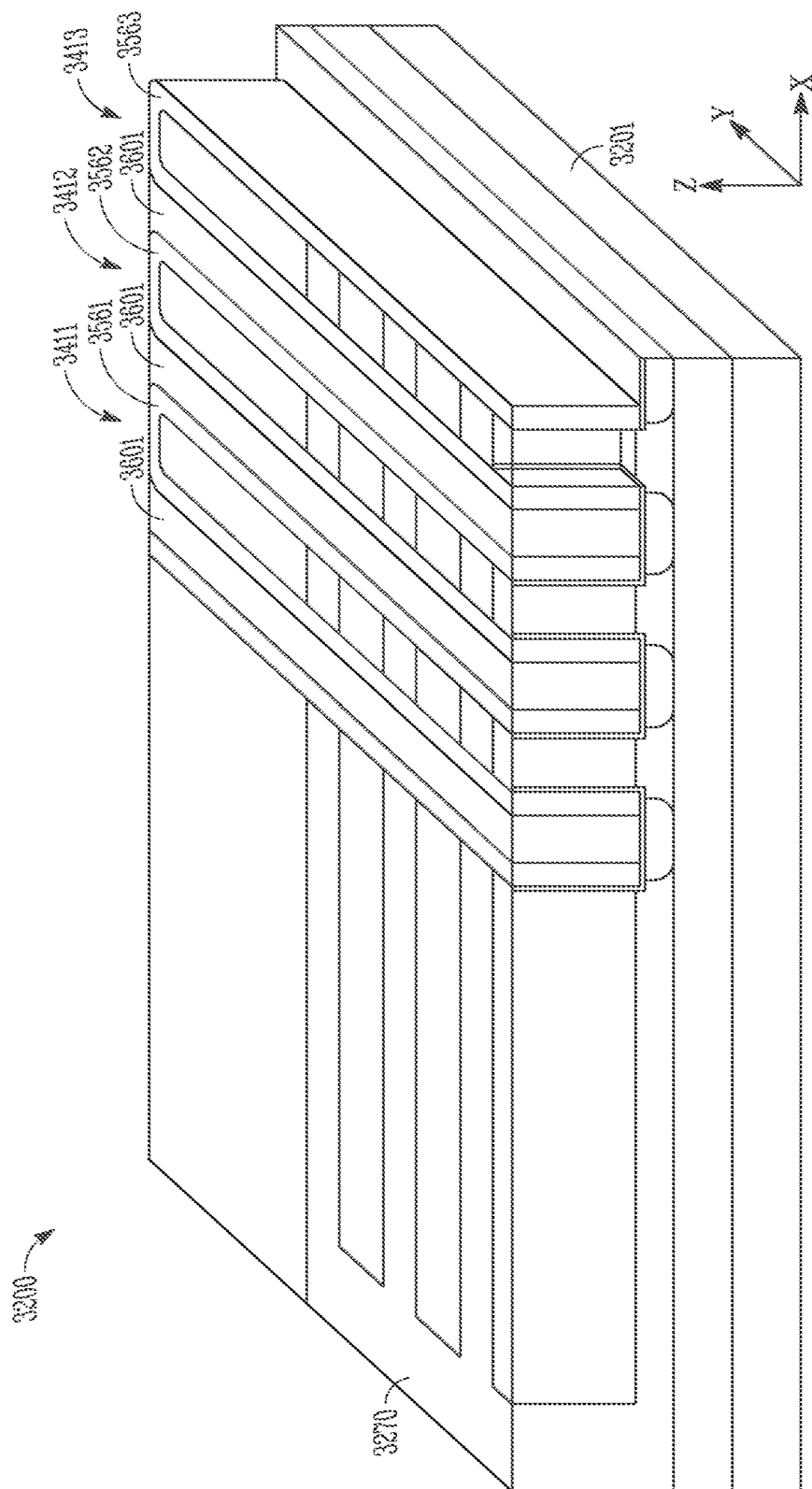


FIG. 36

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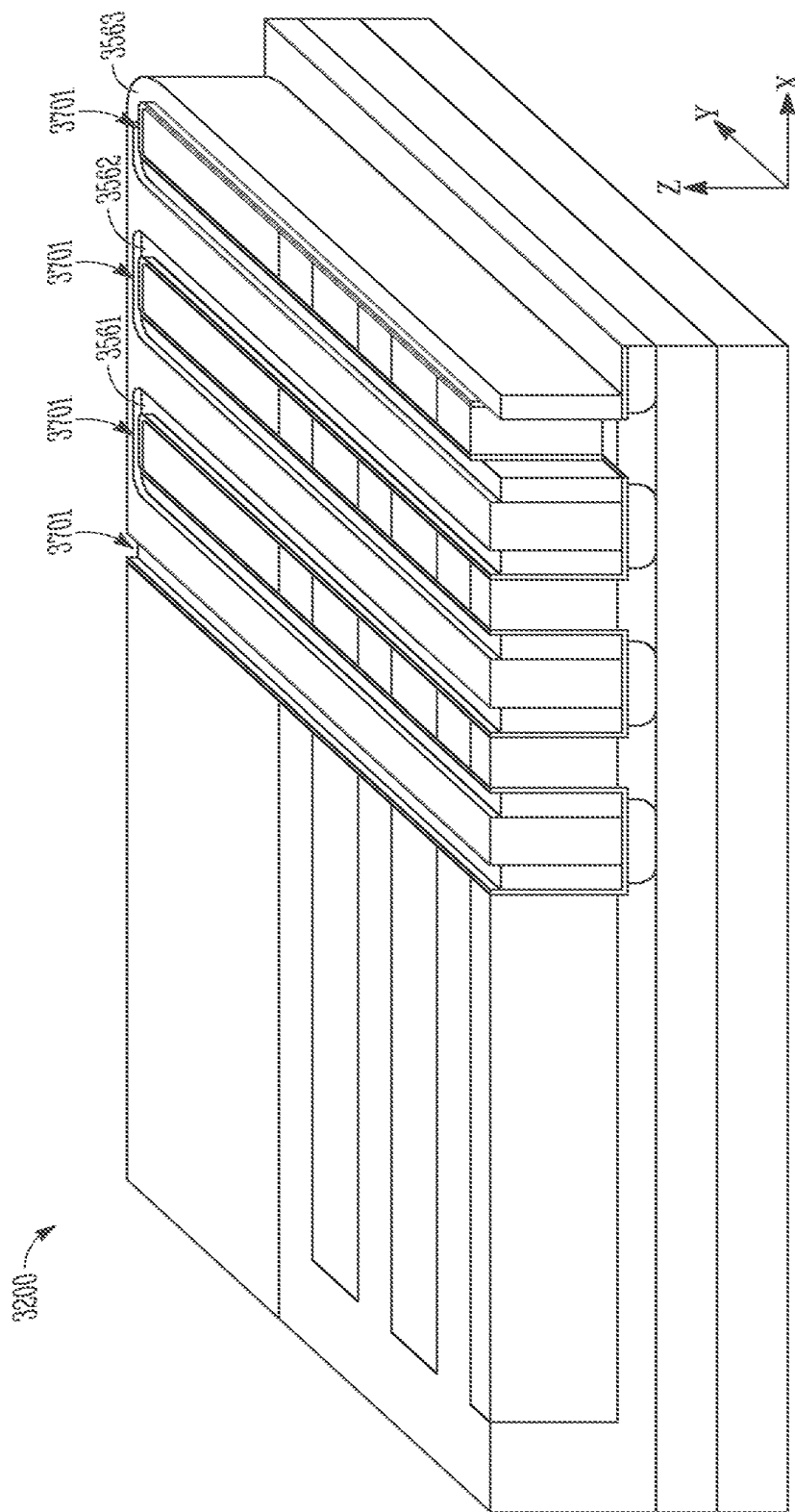
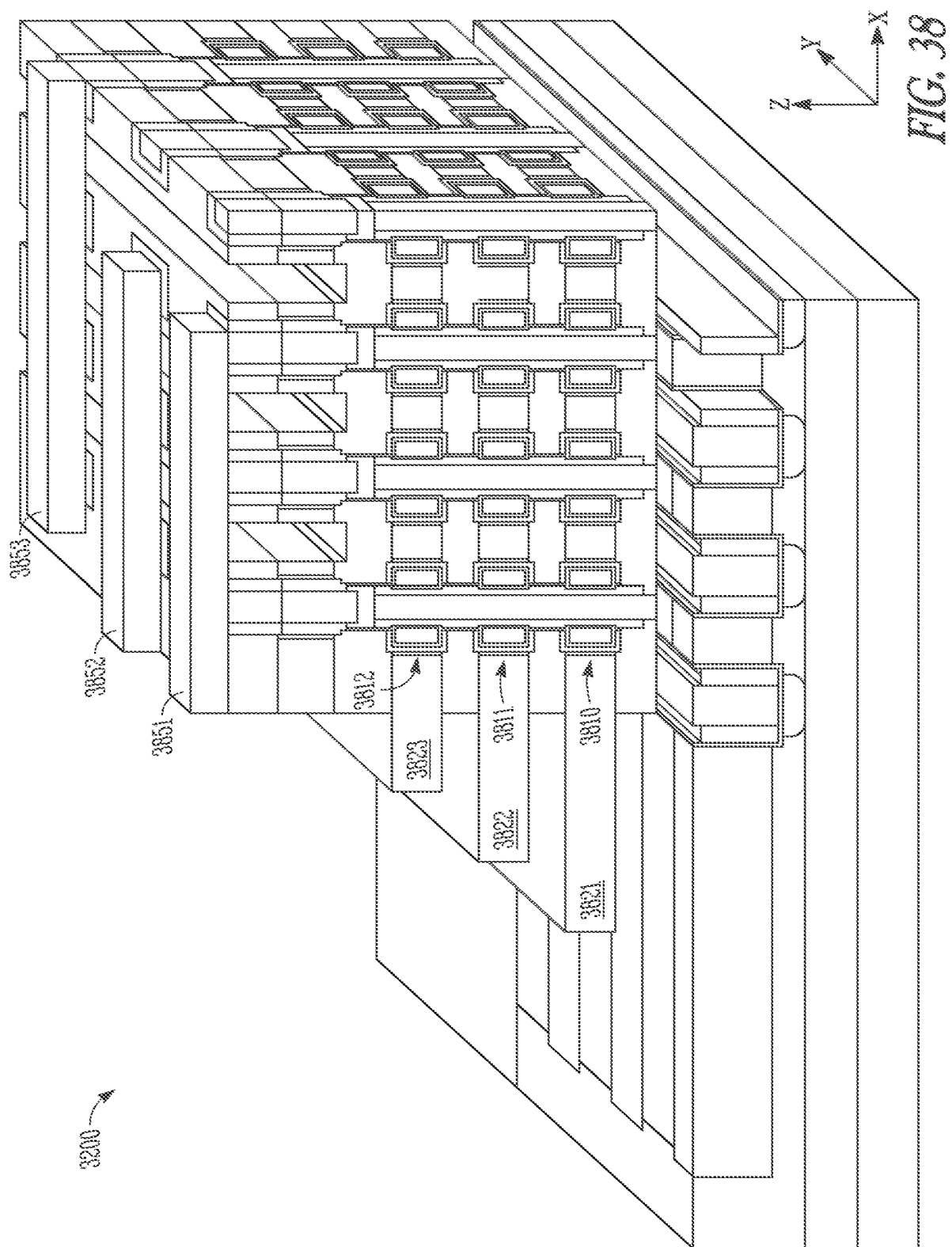


FIG. 37

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Abstract of the Disclosure

Some embodiments include a memory device and methods of forming the memory device. One such memory device includes a first group of memory cells, each of the memory cells of the first group being formed in a cavity of a first control gate located in one device level of the memory device. The memory device also includes a second group of memory cells, each of the memory cells of the second group being formed in a cavity of a second control gate located in another device level of the memory device. Additional apparatus and methods are described.

What is claimed is:

1. An apparatus comprising:
first memory cells located in a first device level of a memory device;
second memory cells located in a second device level of the memory device;
a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate; and
a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate.
2. The apparatus of claim 1, wherein each of the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, further comprising:
a common source; and
data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.
3. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.

4. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.
5. The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.
6. The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.
7. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.
8. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.
9. An apparatus comprising:
 - a first non-volatile memory cell including a first memory element, the first memory element having a ring shape;
 - a second non-volatile memory cell including a second memory element, the second memory element having a ring shape; and
 - a conductive material extending through the first and second memory elements.

10. The apparatus of claim 9, further comprising:

a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells are located; and

a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in a second device level of the memory device.

11. The apparatus of claim 10, wherein each of the memory cells further includes a first dielectric between the respective memory element and the conductive material.

12. The apparatus of claim 11, wherein each of the memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.

13. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the data line is located between the substrate and the first memory cell.

14. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the first and second memory cells are located between the substrate and the data line.

15. An apparatus comprising:
- a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;
 - a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;
 - a first dielectric formed on the first sidewall and the second sidewall;
 - a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;
 - a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;
 - a second dielectric formed on a side of the first memory element and on a side of the second memory element; and
 - a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.
16. The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.
17. The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.
18. The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.

19. The apparatus of claim 15, further comprising:
a substrate; and
a data line configured to be selectively coupled to the conductive channel,
wherein the data line is located between the second conductive material and the
substrate.
20. The apparatus of claim 15, further comprising:
a substrate; and
a data line configured to be selectively coupled to the conductive channel,
wherein the first and second memory elements are located between the data line and
the substrate.

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Priority Application

[0001] This application is a continuation of U.S. Application Serial No. 16/125,242, filed September 7, 2018, which is a continuation of U.S. Application Serial No. 15/722,580, filed October 2, 2017, now issued as U.S. Patent No. 10,090,324, which is a continuation of U.S. Application Serial No. 15/188,273, filed June 21, 2016, now issued as U.S. Patent No. 9,780,115, which is a continuation of U.S. Application Serial No. 14/041,928, filed September 30, 2013, now issued as U.S. Patent No. 9,379,005, which is a divisional of U.S. Application Serial No. 12/825,211, filed June 28, 2010, now issued as U.S. Patent No. 8,803,214, all of which are incorporated herein by reference in their entireties.

Background

[0002] Non-volatile memory devices such as flash memory devices are used in many computers and electronic devices to store information. A flash memory device usually has a write operation to store information (e.g., data and instruction codes), a read operation to retrieve the stored information, and an erase operation to clear information from the memory. As demand for higher density memory device increases, three-dimensional (3D) memory devices have been proposed. An example of a conventional 3D memory device is described by Jiyoung Kim et al. in an article titled “Novel 3-D Structure for Ultra High Density Flash Memory with Vertical-Array-Transistor (VRAT) and Planarized Integration on the same Plane (PIPE)”, published in the 2008 Symposium on VLSI Technology Digest of Technical Papers, pages 22-23. Since 3D memory devices are relatively new, manufacturing these devices can pose fabrication process challenges.

Brief Description of the Drawings

[0003] FIG. 1 shows a block diagram of a memory device having a memory array with memory cells, according to an embodiment of the invention.

[0004] FIG. 2 shows a schematic diagram of a portion of a memory device having data lines located below memory cells, according to an embodiment of the invention.

[0005] FIG. 3 shows a three-dimensional view of a portion of the memory device of FIG. 2, according to an embodiment of the invention.

[0006] FIG. 4 shows a portion of a control gate and a memory cell of the memory device of FIG. 3, according to an embodiment of the invention.

[0007] FIG. 5 through FIG. 29 show various processes of forming a memory device having data lines located below memory cells, according to an embodiment of the invention.

[0008] FIG. 30 shows a schematic diagram of a portion of a memory device having data lines located above memory cells, according to an embodiment of the invention.

[0009] FIG. 31 shows a three-dimensional view of a portion of the memory device of FIG. 30, according to an embodiment of the invention.

[0010] FIG. 32 through FIG. 38 show various processes of forming a memory device with data lines located above memory cells, according to an embodiment of the invention.

Detailed Description

[0011] FIG. 1 shows a block diagram of a memory device 100 having a memory array 102 with memory cells 110 according to an embodiment of the invention. Memory cells 110 can be arranged in rows and columns along with access lines 123 (e.g., wordlines having signals WL0 through WLM) and lines 124 (e.g., bit lines having signals BL0 through BLN). Memory device 100 uses lines 124 and 128 to transfer information within memory cells 110. Memory cells 110 can be physically located in multiple device levels such that one group of memory cells 110 can be stacked on one or more groups of other memory cells 110. Row decoder 132 and column decoder 134 decode address signals A0 through AX on lines 125 (e.g., address lines) to determine which memory cells 110 are to be

accessed. Row and column level decoders 136 and 138 of row and column decoders 132 and 134, respectively, determine which of the multiple device levels of memory device 100 that the memory cells 110 to be accessed are located.

[0012] A sense amplifier circuit 140 operates to determine the value of information read from memory cells 110 and provide the information in the form of signals to lines 124 and 128. Sense amplifier circuit 140 can also use the signals on lines 124 and 128 to determine the value of information to be written to memory cells 110. Memory device 100 can include circuitry 150 to transfer information between memory array 102 and lines (e.g., data lines) 126. Signals DQ0 through DQN on lines 126 can represent information read from or written into memory cells 110. Lines 126 can include nodes within memory device 100 or nodes (e.g., pins or solder balls) on a package where memory device 100 resides. Other devices external to memory device 100 (e.g., a memory controller or a processor) may communicate with memory device 100 through lines 125, 126, and 127.

[0013] Memory device 100 performs memory operations such as a read operation to read information from memory cells 110 and a write operation (sometime referred to as a programming operation) to store information into memory cells 110. A memory control unit 118 controls the memory operations based on control signals on lines 127. Examples of the control signals on lines 127 include one or more clock signals and other signals to indicate which operation, (e.g., a write or read operation) that memory device 100 performs. Other devices external to memory device 100 (e.g., a processor or a memory controller) may control the values of the control signals on lines 127. Specific values of a combination of the signals on these lines can produce a command (e.g., a write or read command) that causes memory device 100 to perform a corresponding memory operation (e.g., a write or read operation).

[0014] Each of memory cells 110 can store information representing a value of a single bit or a value of multiple bits such as two, three, four, or other numbers of bits. For example, each of memory cells 110 can store information representing a binary value "0" or "1" of a single bit. In another example, each of memory cells

110 can store information representing a value of multiple bits, such as one of four possible values "00", "01", "10", and "11" of two bits, one of eight possible values "000", "001", "010", "011", "100", "101", "110" and "111", or one of other values of other number of multiple bits.

[0015] Memory device 100 can receive a supply voltage, including supply voltage signals Vcc and Vss, on lines 141 and 142, respectively. Supply voltage signal Vss may operate at a ground potential (e.g., having a value of approximately zero volts). Supply voltage signal Vcc may include an external voltage supplied to memory device 100 from an external power source such as a battery or an alternating-current to direct-current (AC-DC) converter circuitry.

[0016] Circuitry 150 of memory device 100 can include a select circuit 152 and an input/output (I/O) circuit 116. Select circuit 152 responds to signals SEL0 through SELn to select the signals on lines 124 and 128 that can represent the information read from or written into memory cells 110. Column decoder 134 selectively activates the SEL0 through SELn signals based on address signals A0 through AX. Select circuit 152 selects the signals on lines 124 and 128 to provide communication between memory array 102 and I/O circuit 116 during read and write operations.

[0017] Memory device 100 can be a non-volatile memory device and memory cells 110 can be non-volatile memory cells such that memory cells 110 can retain information stored thereon when power (e.g., Vcc or Vss, or both) is disconnected from memory device 100. For example, memory device 100 can be a flash memory device such as a NAND flash or a NOR flash memory device, or other kinds of memory devices, such as a variable resistance memory device (e.g., phase change random-access-memory (PCRAM), resistive RAM (RRAM), etc.).

[0018] One skilled in the art may recognize that memory device 100 may include other features that are not shown in FIG. 1, to help focus on the embodiments described herein.

[0019] Memory device 100 may include at least one of the memory devices and memory cells described below with reference to FIG. 2 through FIG. 38.

[0020] FIG. 2 shows a schematic diagram of a portion of a memory device 200 having data lines 251, 252, and 253 located below memory cells 210, 211, and 212, according to an embodiment of the invention. Memory cells 210, 211, and 212 can be grouped into groups, such as a group of memory cells 210, a group of memory cells 211, and a group of memory cells 212. As shown in FIG. 2, the memory cells in each group share the same control gate, such as control gate 221, 222, or 223 (with associated signals WL0, WL1, and WL2). The memory cells are coupled in series as strings, such as strings 215 and 216. Each string can include one of the memory cells from different groups and is coupled between one of transistors 231 and one of transistors 232.

[0021] As shown in FIG. 2, transistors 231 have gates coupled to select lines 241, 242, and 243 (with associated signals SGD0, SGD1, and SGD2). Transistors 231 have nodes (e.g., sources) coupled to data lines 251, 252, and 253 (with associated signals BL0, BL1, and BL2). Data lines 251, 252, and 253 sometimes correspond to bit lines or sense lines of a non-volatile memory device.

[0022] Transistors 232 have gates coupled to select lines 261, 262, and 263 (with associated signals SGS0, SGS1, and SGS2). Transistors 232 have nodes (e.g., drains) coupled to a common source 270 of memory cell strings in a non-volatile memory device.

[0023] FIG. 2 shows three groups of memory cells with associated components coupled to them, as an example. The number of groups of memory cells and their associated components (e.g., control gates and data lines) can vary.

[0024] Memory device 200 uses control gates 221, 221, and 223 to control access to memory cells 210, 211, and 212 during a read operation to sense (e.g., read) information stored in memory cells 210, 211, and 212, and during a write operation to store information into memory cells 210, 211, and 212. Memory device 200 uses data lines 251, 252, and 253 to transfer the information read from these memory cells during a read operation.

[0025] Transistors 231 and 232 are responsive to signals SGD0, SGD1, and SGD2, and signals SGS0, GS1, and SGS2, respectively, to selectively couple the

memory cells to data lines 251, 252, and 253 and common source 270 during a read or write operation.

[0026] To help focus on the description herein, the description herein omits detailed description of operations of memory device, such as write, read, and erase operation. One skill in the art would recognize these operations. For example, in an erase operation of memory device 200, a voltage of approximately 20 volts can be applied to data lines 251, 252, and 253 while control gates 221, 221, and 223, select lines 241, 242, and 243, and select lines 261, 262, and 263 can be “floated” (e.g., leave unconnected to a voltage). In this erase operation, electrons from memory elements of memory cells 210, 211, and 212 may move to data lines 251, 253, and 253.

[0027] FIG. 3 shows a 3D view of a portion of memory device 200, according to an embodiment of the invention. FIG. 3 also shows X, Y, and Z directions, and device levels 301, 302, and 303 arranged in the Z-direction. Memory cells 210 of the same group can be arranged in rows and columns in the X-direction and Y-direction. Each group of memory cells is located in different device levels 301, 302, or 303. For example, the group having memory cells 210 is located in device level 301. The group having memory cells 211 is located in device level 302. The group having memory cells 212 is located in device level 303.

[0028] As shown in FIG. 3, memory cells 210, 211, and 212 in each string (e.g., memory cells between transistors 231 and 232) are substantially vertically aligned in the Z-direction with respect to a substrate underneath data lines 251, 252, and 253. The substrate is not shown in FIG. 3, but can be similar to substrate 503 of FIG. 5 and FIG. 6. FIG. 3 also shows a channel 241 and a conductive material portion 242 extending vertically in the Z-direction and through memory element 430 of memory cells 210, 211, and 212 in the same string between transistors 231 and 232, which corresponds to transistors 231 and 232 of FIG. 2. As shown in FIG. 3, transistor 231 can include a double-gate coupled to a body 391 (e.g., transistor channel) to control (turn on or off) the transistor. The structure of the double-gate

can include two segments of the same select line 241 (as shown in FIG. 3), such that the two segments are located on only two respective sides of body 391.

[0029] Memory device 200 in FIG. 3 also can include contacts 329, 349, and 359. Contacts 329 provide electrical connections to control gates 221, 222, and 223. Contacts 349 provide electrical connections to select lines 241, 242, 243, and 244. Contacts 359 provide electrical connections to and from data lines 251, 252, and 253. Select line 244 and the memory cell associated with it in the Z-direction are not shown in FIG. 2.

[0030] FIG. 4 shows a portion of control gate 221 and a memory cell 210 of memory device 200 of FIG. 3. Control gates 222 and 223 and memory cells 211 and 212 of FIG. 2 have structures similar to control gate 221 and memory cell 210, respectively. As shown in FIG. 4, control gate 221 can include a homogenous material with cavities 420, each cavity being filed with various components, including materials different from the homogenous material. The various components include: a memory element 430; a channel 441, a conductive material portion 442, and dielectrics 421 and 427. Dielectric 421 can include multiple materials 422, 423, and 424 arranged as different layers. As shown in FIG. 4, memory element 430 of each memory cell 210 has a ring shape (e.g., donut shape) with an inner side 451 and an outer side 452. Each of the other memory cells 211 and 212 shown in FIG. 3 also has a ring shape. As shown in FIG. 3, within memory cells 210, 211, and 212 in the same string (e.g., between transistors 231 and 232), the entire ring-shape memory element 430 of each memory cell is substantially vertically aligned (in the Z-direction) with the entire ring-shape memory element of each of the other memory cells in the same string.

[0031] Each memory element 430 can store information, such as based on the amount of charge (e.g., number of electrons) therein. In each such memory element 430, the amount of charge corresponds to the value of information store that memory element. The amount of charge can be controlled in a write operation or in erase operation. For example, electrons from channel 441 or conductive material portion 442, or both, can move to memory element 430 during a write operation due

to a tunneling effect known to those skilled in the art. In an erase operation, electrons from memory element 430 can move back to channel 441 or conductive material portion 442, or both, to data lines 251, 253, and 253 (FIG. 2 and FIG. 3). Alternative embodiments might use a memory element 430 that can store information, such as based on the resistance of the element 430, for example.

[0032] Memory device 200 of FIG. 3 can be formed using processes similar to or identical to those described below with reference to FIG. 5 through FIG. 29.

[0033] FIG. 5 through FIG. 29 show various processes of forming a memory device 500 having data lines located below memory cells, according to an embodiment of the invention. Memory device 500 (shown in more details in FIG. 29) can correspond to memory device 300 of FIG. 3.

[0034] FIG. 5 shows memory device 500 having a substrate 503, which can include materials 501 and 502 arranged as layers. Material 501 can include bulk silicon or could be another semiconductor material. Material 502 can be a dielectric material, for example, silicon oxide. FIG. 5 also shows materials 504 and 505 formed over substrate 503. Forming materials 504 and 505 can include depositing a conductive material over substrate 503 and then depositing another conductive material over material 504. Material 504 can include a metal or other conductive materials. Material 505 can include undoped polysilicon or doped polysilicon, such as p-type silicon or another conductive materials.

[0035] FIG. 5 also shows an X-direction, a Y-direction perpendicular to the X-direction, and a Z-direction perpendicular to both the X-direction and the Y-direction. As shown in FIG. 5, materials 504 and 505 can be formed as different layers, one layer over (e.g., on) one or more other layers in the Z-direction.

[0036] As used herein, the term “on” used with respect to two or more materials, one “on” the other, means at least some contact between the materials, while “over” or “overlying” could refer to either a material being “on” another material or where there is one or more additional intervening materials between the materials (e.g., contact is not necessarily required). The term “on”, “over”, or

“overlying” does not imply any directionality as used herein unless otherwise explicitly stated as such.

[0037] FIG. 6 shows memory device 500 after data lines 651, 652, and 653 and device structures 605 have been formed. A process such as etching (e.g., dry etching) can be used to remove portions of materials 504 and 505 (FIG. 5) to form trenches 511 and 512, which have trench bottoms at material 502. Each of data lines 651, 652, and 653 and each of device structures 605 has a greater dimension (e.g., length) extending in the X-direction. A mask (not shown in FIG. 6) having separate openings extending in the X-direction can be used to form trenches 511 and 512. As shown in FIG. 6, trenches 511 and 512 divide material 504 (FIG. 5) into separate data lines 651, 652, and 653, which can correspond to data lines 251, 252, and 253 of FIG. 2.

[0038] FIG. 7 shows memory device 500 after pillars 705 have been formed in area 701 of memory device 500. Pillars 705 are not formed in area 702 of memory device 500. For simplicity, FIG. 7 through FIG. 29 do not show substrate 503 of FIG. 6. In FIG. 7, a process such as etching (e.g., dry etch) can be used to remove portions of device structures 605 to form trenches 711, 712, and 713 in the Y-direction, perpendicular to trenches 511 and 512, such that pillars 705 can be formed as shown in FIG. 7. A mask (not shown in FIG. 7) having separate openings extending in the Y-direction can be used to form trenches 711, 712, and 713. Each pillar 705 can include a height in the Z-direction of approximately 20 to 50 nanometers. As shown in FIG. 7, pillars 705 are arranged in rows and columns (e.g., in a matrix) in the X-direction and Y-direction. For simplicity, FIG. 7 does not show a dielectric material filled in trenches 511 and 512. However, forming memory device 500 in FIG. 7 also can include forming a dielectric material (e.g., silicon oxide) to fill trenches 511 and 512 up to a top surface 715 of device structure 605.

[0039] FIG. 8 shows memory device 500 after dielectric 831 and select lines 841, 842, 843, and 844 have been formed. Select lines 841, 842, 843, and 844 can correspond to select lines 241, 242, 243, and 244, respectively, of FIG. 3. In FIG. 8,

dielectrics 831 are formed to electrically isolate select lines 841, 842, 843, and 844 from pillars 705. Dielectrics 831 can be formed by, for example, depositing a dielectric material (e.g., silicon oxide) on at least two sides of each pillar 705 or by oxidizing pillars 705. After dielectrics 831 are formed, select lines 841, 842, 843, and 844 can be formed by, for example, depositing a conductive material over pillars 705 and trenches 711, 712, and 713 (FIG. 7) and then removing (e.g., etching) a portion of the conductive material to form select lines 841, 842, 843, and 844 having the structure shown in FIG. 8. Examples of the conductive materials for select lines 841, 842, 843, and 844 include polysilicon, metal, or other conductive materials, such as TiN and TaN.

[0040] FIG. 8 also shows doped regions 833, which can be formed by inserting (e.g., implanting) n-type impurities into selective portions of device structure 605. Examples of n-type impurities include elements such as phosphorus (P) or arsenic (As). The remaining portion of device structures 605 that has not been inserted with n-type impurities may maintain its original material, such as p-type silicon, as described above with reference to FIG. 5.

[0041] FIG. 9 shows memory device 500 with select lines 941, 942, 943, and 944, which are alternative structures for select lines 841, 842, 843, and 844 of FIG. 8. In FIG. 8, opposite sides of each pillar 705 are associated with two different segments of the same select line 841, 842, 843, or 844. In FIG. 9, except for the top surfaces of pillars 705, each pillar 705 can be completely surrounded by the material of one of the select line 941, 942, 943, or 944 (e.g., four sides of each pillar 705 are associated with four different segments of the same select line). Higher efficient memory device may be achieved with select lines 941, 942, 943, and 944 in comparison to select lines 841, 842, 843, and 844. Select lines 941, 942, 943, and 944 can also be alternative structures for select lines 241, 242, 243, and 244, respectively, of FIG. 3. Thus, each transistor 231 of FIG. 2 and FIG. 3 can include a surrounded gate with a structure shown in FIG. 9. Thus, instead of a double-gate shown in FIG. 3, each transistor 231 of FIG. 3 can alternatively include a

surrounded gate having four different segments of the same select line (such as select line 941) surrounding body 391 (FIG. 3).

[0042] FIG. 10 shows memory device 500 after materials 1001 through 1007 are formed over pillars 705 and select lines 841, 842, 843, and 844. Materials 1001 through 1007 can be formed in both areas 701 and 702 of memory device 500. However, to focus on the description herein, FIG. 10 does not show some portions of materials 1001 through 1007 in area 702. The description below with reference to FIG. 28 and FIG. 29 describes forming additional components (e.g., components similar to contacts 329 of FIG. 3) in area 702 of memory device 500.

[0043] In FIG. 10 through FIG. 29, for simplicity, some number designations associated with some components of memory device 500 may not be repeated from one figure to another figure. In FIG. 10, before forming materials 1001 through 1007, a dielectric material (not shown in FIG. 10), such as silicon oxide, can be formed to fill gaps 1041, 1042, and 1043. Forming materials 1001 through 1007 can include alternately depositing dielectric material and conductive material in an interleave fashion, such that these materials are alternately stacked over each other in the Z-direction, as shown in FIG. 10. Materials 1001, 1003, 1005, and 1007 can include dielectric materials, such as silicon oxide. Materials 1002, 1004, and 1006 can include conductive materials, such as metal or polysilicon (e.g., n-type silicon for p-type silicon). As shown in FIG. 10, materials 1001 through 1007 are formed such that materials 1002, 1004, and 1006 are electrically isolated from each other by materials 1001, 1003, 1005, and 1007.

[0044] FIG. 11 shows memory device 500 after openings (e.g., holes) 1101 have been formed in material 1002 through 1107. Holes 1101 are formed such that each hole 1101 can be aligned substantially directly over a corresponding pillar 705, as illustrated in FIG. 11. Forming holes 1101 can include removing (e.g., etching) a portion of each of materials 1002 through 1007, stopping at material 1001, such that at least a portion of material 1001 or the entire material 1001 remains to separate holes 1101 from pillars 705. Forming holes 1101 results in forming cavities 1110 in each of materials 1003, 1005, and 1007, and cavities 1120 in each of materials 1002,

1004, and 1006. As shown in FIG. 12, cavities 1110 in the materials 1003, 1005, and 1007 are substantially aligned directly over cavities 1120 in the other materials 1002, 1004, and 1006. Each cavity 1110 and each cavity 1120 may have substantially the same diameter, D1. Diameter D1 can also be considered the diameter of each hole 1101 at the location of each cavity 1110 and each cavity 1120.

[0045] FIG. 12 shows memory device 500 after cavities 1220 have been formed in materials 1002, 1004, and 1006 (used to form control gates 1221, 1222, and 1223). Forming cavities 1220 can include enlarging the size of cavities 1120 (FIG. 11) while keeping the size of cavities 1110 substantially unchanged (e.g., remaining substantially at diameter D1). For example, enlarging the size of cavities 1120 (FIG. 11) can include selectively removing (e.g., selective wet or dry etching) a portion of each of materials 1002, 1004, and 1006 at each cavity 1120 (FIG. 11) such that the diameter of each cavity 1220 increases to substantially diameter D2, while the diameter D1 at each cavity 1110 remains substantially unchanged. Diameter D2 is greater than diameter D1. Forming cavities 1120 in materials 1002, 1004, and 1006 also form control gates 1221, 1222, and 1223, which can correspond to control gates control gates 221, 222, and 223 of FIG. 2.

[0046] FIG. 13 shows more details of control gate 1221 of FIG. 12. Control gates 1222 and 1223 of FIG. 12 have a similar structure as control gate 1221. As shown in FIG. 13, control gate 1221 can include a homogenous material with cavities 1220 of FIG. 11 being arranged in rows and columns in the X-direction and Y-direction. Each cavity 1220 can include a sidewall 1225.

[0047] FIG. 14 and FIG. 15 shows memory device 500 after dielectrics 1421 and memory elements 1430 have been formed in cavities 1220. For simplicity, FIG. 15 does not show dielectrics 1421 and memory elements 1430 in all cavities 1220. Each dielectric 1421 can be formed on sidewall 1225, such that each dielectric 1421 and can be located between the material of control gate 1221 and memory element 1430, and such that memory element 1430 can be electrically isolated from the material of control gate 1221 by at least a portion of dielectric 1421. Forming dielectric 1421 can include forming multiple materials 1422, 1423, and 1424 (FIG.

15) at different times, one material after another. Forming material 1422 can include oxidizing a portion (e.g., a surface) of sidewall 1225 to form dielectric material (e.g., silicon oxide) on sidewall 1225. Alternatively, forming material 1422 can include depositing dielectric material (e.g., silicon oxide) on sidewall 1225. Forming material 1423 can include depositing dielectric material (e.g., silicon nitride) on material 1422, wherein a portion of that dielectric material may also form on sidewall 1425 of each cavity 1110. Forming material 1424 can include depositing dielectric material (e.g., silicon oxide) on material 1423.

[0048] Memory elements 1430 can be formed after dielectrics 1421 are formed. As shown in FIG. 15, each memory element 1430 has a ring shape (e.g., a donut shape) with an inner side 1451 and an outer side 1452 of FIG. 14. Forming memory elements 1430 can include depositing a material in holes 1101. Since cavities 1220 of FIG. 14 are substantially aligned with cavities 1110, the material (that forms memory element 1430) may fill both cavities 1110 and 1120. Then, a portion (e.g., center portion in each hole) of the material that forms memory elements 1430 can be removed (e.g., by etching in the same, single, etching step) such that the material in cavities 1110 can be removed (e.g., completely removed) and the material in cavities 1220 is not completely removed but partially removed. As shown in FIG. 14, after the material that forms memory elements 1430 is removed from cavities 1110, a portion of dielectric material 1423 (e.g., silicon nitride, that was formed on material 1422) may be exposed. As shown in FIG. 14, after the material that forms memory elements 1430 is partially removed from cavities 1220, memory element 1430 (formed by the remaining material in a cavity 1220) associated with the same hole 1101 may have its inner side 1451 substantially aligned with sidewall 1425 (or sidewall 1425 with portions of materials 1422 and 1423 of cavities 1110) of cavities 1110.

[0049] The material of memory elements 1430 can include, for example, semiconductor material (e.g., polysilicon), dielectric charge trapping material, such as silicon nitride or other dielectric charge trapping materials, or a variable resistance material, such as a phase change material (e.g., GST). During removing

(e.g., etching) a portion of the material that forms memory elements 1430, portions 1401 of material 1001 located over pillars 705 can also be removed to reduce the thickness of portions 1401.

[0050] FIG. 16 and FIG. 17 show memory device 500 after dielectric 1627 has been formed on inner side 1451 of memory element 1430 and in cavities 1110. Forming dielectric 1627 can include depositing dielectric material (e.g., silicon oxide) on inner side 1451. Alternatively, forming dielectric 1627 can include oxidizing a portion (e.g., inner side 1451) of memory element 1430. Forming dielectric 1627 (e.g., by oxidation) may also consume material 1423 (FIG. 14) formed on material 1422, which formed on sidewall 1425 of cavities 1110. Thus, dielectric 1627 may also form in cavities over material 1422.

[0051] FIG. 18 and FIG. 19 show memory device 500 after channels 1841 have been formed on dielectrics 1627 in both cavities 1110 and 1220. Forming channels 1841 can include depositing a conductive material on dielectrics 1627. An etching process can be used to reduce the thickness of the conductive material after it is deposited. The conductive material of channels 1841 can include doped polysilicon, which can have the same material type (e.g., p-type) as pillars 705. FIG. 18 also shows a formation of openings 1801, which can be formed by removing (e.g., by etching) portions 1401 (FIG. 14) located over pillars 705. As shown in FIG. 19, channel 1841 is facing memory elements 1430 and is electrically isolated from memory element 1430 by at least a portion of dielectric 1627.

[0052] FIG. 20 shows memory device 500 after a conductive material 2001 has been formed by, for example, depositing undoped or lightly doped polysilicon to place channels 1841 in electrical communication with pillars 705. As shown in FIG. 20, conductive material 2001 forms a continuous conductive path between channels 1841 and data lines 651, 652, and 653 through pillars 705.

[0053] FIG. 21 shows memory device 500 after dielectric material 2101 (e.g., silicon oxide) has been formed over conductive material 2001.

[0054] FIG. 22 shows memory device 500 after a formation of openings (e.g., holes 2201), a conductive material portion 2260, and conductive material

portions 2241. Holes 2201 are formed such that each hole 2201 can be aligned substantially directly over channels 1841, as illustrated in FIG. 22. Forming holes 2201 can include removing (e.g., etching) a portion of dielectric material 2101 and a portion of conductive material 2001 (FIG. 21), stopping at a location in material 1007. Holes 2201 can be formed such that after a portion of conductive material 2001 is removed during the formation of holes 2201, conductive material 2001 is separated into conductive material portion 2260 and conductive material portions 2241, as illustrated in FIG. 22.

[0055] FIG. 23 shows memory device 500 after doped regions 2301 have been formed. Forming doped regions 2301 can include inserting (e.g., implanting) n-type impurities into top parts of conductive material portions 2241. Doped regions 2301 can provide a relatively low resistance connection between channels 1841 and other components of memory device 500.

[0056] FIG. 24 shows memory device 500 after dielectrics 2401 and channels 2402 have been formed. Dielectrics 2401 (e.g., silicon oxide) is formed on sidewalls of conductive material portion 2260 at the location of holes 2201. Channels 2402 are formed on sidewalls of dielectric material 2101 and on dielectrics 2401.

[0057] FIG. 25 shows memory device 500 after conductive material 2501 has been formed in each of holes 2201, such that channel 2402 can be electrically coupled to channel 1841 through conductive material 2501, doped region 2301, and conductive material portion 2241. Forming conductive material 2501 in each of holes 2201 can include depositing a conductive material (e.g., polysilicon) over material, such that the conductive material fills holes 2201. Then, a top portion of the conductive material can be removed by, for example, etching back the conductive material or by chemical mechanical planarization (CMP).

[0058] FIG. 26 shows memory device 500 after doped regions 2601 and select lines 2661, 2662, and 2663 have been formed. Forming doped regions 2601 can include inserting (e.g., implanting) n-type impurities into top portions of conductive material 2501. Forming select lines 2661, 2662, and 2663 can include

removing parts of dielectric material 2101 and conductive material portion 2260 to form trenches 2602, which have trench bottoms partially extending into material 1007. As shown in FIG. 26, trenches 2602 separate conductive material portion 2260 into select lines 2661, 2662, and 2663, which can correspond to select lines 261, 262, and 263 of FIG. 2.

[0059] FIG. 27 shows memory device 500 after material 2701 and a common source 2770 have been formed. Forming material 2701 can include depositing a dielectric material (e.g., silicon dioxide) over material 2101, such that the dielectric material fills trenches 2602. Then, a top portion of the dielectric material can be removed by, for example, etching back the dielectric material or by CMP. Forming common source 2770 can include depositing a conductive material (e.g., metal) over materials 2701 and 2101.

[0060] FIG. 28 shows memory device 500 after materials 1001 through 1007 in area 702 (FIG. 10) are processed (e.g., by patterning) to form a stair like pattern with material between the stairs are not shown in FIG. 28. As mentioned above in the description of FIG. 10, some portions of materials 1001 through 1007 are omitted from area 702 of FIG. 10 through FIG. 27 for clarity. FIG. 28 shows material 1001 through 1007 in area 702 after they have been processed to form the stair like pattern. As shown in FIG. 28, control gates 1221, 1222, and 1223 are formed from materials 1002, 1004, and 1006, respectively, which are formed in the stair like pattern.

[0061] FIG. 29 shows memory device 500 after contacts 2929, 2949, and 2959 have been formed. Contacts 2929 provide electrical connections to control gates 1221, 1222, and 1223. Contacts 2949 provide electrical connections to select lines 841, 842, 843, and 844. Contacts 2959 provide electrical connections to and from data lines 651, 652, and 653.

[0062] As shown in FIG. 29, memory device 500 can include components and memory cells 2910, 2911, and 2912 similar to or identical to components and memory cells 210, 211, and 212 of memory device 300 described above with reference to FIG. 2 and FIG. 3.

[0063] One skilled in the art may readily recognize that additional processes may be performed to form additional features of a memory device, such as memory device 500 described above. Thus, to help focus on the embodiments described herein, FIG. 5 through FIG. 29 described above and FIG. 30 through FIG. 38 described below show only some of the features of a memory device, such as memory device 500.

[0064] FIG. 30 shows a schematic diagram of a portion of a memory device 300 having data lines 251, 252, and 253 located above memory cells 210, 211, and 212, according to an embodiment of the invention. Memory device 300 can include components similar to those of memory device 200 of FIG. 3. Thus, for simplicity, similar or same components between memory device 200 and memory device 3000 are given the same number designations. The detailed description of these similar components is not repeated in FIG. 30. Main differences between memory device 3000 and memory device 200 include the locations of data lines 251, 252, and 253 and common source 3070 of memory device 3000 to enable global erase operation. As shown in FIG. 30, data lines 251, 252, and 253 are located above memory cells 210, 211, and 212. Common source 3070 is located below memory cells 210, 211, and 212 and can couple directly to at least a portion of a substrate of memory device 3000 (e.g., substrate 3101 in FIG. 31). This main difference may allow voltages to be applied to various components of memory device 3000 in a different way during an erase operation and memory device 3000 function differently (e.g., during the global erase operation) in comparison with the erase operation (e.g., local erase operation) of memory device 200. For example, in an erase operation of memory device 3000, a voltage of approximately 20 volts can be applied to common source 3070, while control gates 221, 221, and 223, data lines 251, 252, and 253, select lines 241, 242, and 243, and select lines 261, 262, and 26 can be “floated”. In this erase operation, electrons from memory elements of memory cells 210, 211, and 212 may move (e.g., by tunneling) to common source 3070 (e.g., global erase). In memory 200, as described above with reference to FIG. 2, FIG. 3, and FIG. 4,

during an erase operation, electrons from memory elements of memory cells 210, 211, and 212 may move to data lines 251, 252, and 253 (e.g., local erase)

[0065] FIG. 31 shows a 3D view of a portion of the memory device 3000 of FIG. 30, according to an embodiment of the invention. As shown in FIG. 31, data lines 251, 252, and 253 are located above memory cells 210, 211, and 212, common source 3070 is located below memory cells 210, 211, and 212 and is coupled to a substrate 3101. Substrate 3101 can include semiconductor material, such as p-type silicon.

[0066] As shown in FIG. 31, memory cells 210, 211, and 212 in each string (e.g., memory cells between transistors 231 and 232) are substantially vertically aligned in the Z-direction with respect to substrate 3101. Transistor 232 can include a double-gate or surrounded gate similar to the double-gate (FIG. 3) or surrounded gate (FIG. 9) of transistor 231 of FIG. 3. FIG. 31 also shows a channel 441 and a conductive material portion 442 extending vertically in the Z-direction and through memory element 430 of memory cells 210, 211, and 212 in the same string between transistors 231 and 232, which corresponds to transistors 231 and 232 of FIG. 30.

[0067] Memory element 430 in each of memory cells 210, 211, and 212 has a ring shape. As shown in FIG. 31, within memory cells 210, 211, and 212 in the same string, the entire ring-shape memory element 430 of each memory cell is substantially vertically aligned (in the Z-direction) with the entire ring-shape memory element of each of the other memory cells in the same string.

[0068] FIG. 32 through FIG. 38 show various processes of forming a memory device 3200 having data lines located above memory cells, according to an embodiment of the invention. Memory device 3200 (shown in more details in FIG. 38) can correspond to memory device 3000 of FIG. 31.

[0069] FIG. 32 shows memory device 3200 having a substrate 3201 and trenches 3211, 3212, and 3213, and substrate portions 3270 and 3271 formed on a top portion of substrate 3201. Substrate 3201 can include semiconductor material, such as bulk silicon. Top substrate portions 3270 and 3271 can be formed by inserting (e.g., implanting) p-type impurities into a top portion of substrate 3201.

Thus, substrate portions 3270 and 3271 can include p-type silicon. Forming trenches 3211, 3212, and 3213 and substrate portion 3270 can include removing (e.g., etching) a portion of substrate portion 3271. During a write or read operation of memory device 3200, substrate portion 3270 can be coupled to a potential, such as to ground. During an erase operation of memory device 3200, substrate portion 3270 can be coupled to a voltage, for example, approximately 20 volts.

[0070] FIG. 33 shows memory device 3200 after material 3301 has been formed in trenches 3211, 3212, and 3213 (FIG. 32). Forming material 3301 can include depositing dielectric material (e.g., silicon oxide) over substrate 3201 to fill trenches 3211, 3212, and 3213. Then, a top portion of the dielectric material can be removed by, for example, CMP.

[0071] FIG. 34 shows memory device 3200 after material 3401 and trenches 3411, 3412, and 3413, and device structures 3460 have been formed. Forming material 3401 can include depositing dielectric material (e.g., silicon oxide, or silicon nitride) over substrate 3201 and material 3301. Forming trenches 3411, 3412, and 3413 can include removing (e.g., etching) portions of substrate 3201, material 3301, and material 3401. Device structures 3460 are formed as a result of the formation of trenches 3411, 3412, and 3413.

[0072] FIG. 35 shows memory device 3200 after a formation of doped regions 3501, material 3502, and select lines 3561, 3562, and 3563. Forming doped regions 3501 can include inserting (e.g., implanting) n-type impurities into selective portions of substrate portion 3271. Material 3502 (e.g., silicon oxide) can be formed on both sides of each device structure 3460 to electrically isolate select lines 3561, 3562, and 3563 from device structures 3460. Materials of select lines 3561, 3562, and 3563 can include one or more conductive materials, such as one or more metals, alloys, other conductive materials, or a combination thereof. Select lines 3561, 3562, and 3563 can correspond to select lines 261, 262, and 263 of memory device 3000 of FIG. 30.

[0073] FIG. 36 shows memory device 3200 after material 3601 have been formed in trenches 3411, 3412, and 3413. Forming material 3601 can include

depositing dielectric material (e.g., silicon dioxide) to fill trenches 3411, 3412, and 3413. Then, a top portion of the dielectric material can be removed by, for example, etching back the conductive material or by CMP, stopping at substrate portion 3270.

[0074] FIG. 37 shows memory device 3200 after grooves 3701 have been formed by removing (e.g., by wet etching) a top portion of the material used to form select lines 3561, 3562, and 3563. Alternatively, forming grooves 3701 can be omitted.

[0075] FIG. 38 shows memory device 3200 after other components have been formed. The processes for forming the components of memory device 3200 in FIG. 38 can include similar or identical processes for forming the component of memory device 500 described above with reference to FIG. 10 through FIG. 29. For example, control gates 3821, 3822, and 3823 of FIG. 38 can be formed using processes similar to or identical to those of forming control gates 1221, 1222, and 1223 of memory device 500 described above with described above with reference to FIG. 5 through FIG. 29. Data lines 3851, 3852, and 3853 of FIG. 38, can correspond to data lines 251, 252, and 253 of FIG. 30 and FIG. 31. As shown in FIG. 38, memory device 3200 can include memory cells 3810, 3811, and 3812, which can be formed using processes similar to or identical to those of forming memory cells 2910, 2911, and 2912 of memory device 500 described above with reference to FIG. 5 through FIG. 29.

[0076] One or more embodiments described herein include a memory device and methods of forming the memory device. One such memory device can include a first group of memory cells, each cell of the first group being formed in a respective cavity of a first control gate located in one device level of the memory device. The memory device also can include a second group of memory cells, each cell of the second group being formed in a cavity of in a second control gate located in another device level of the memory device. Additional apparatus and methods are described. Other embodiments including additional apparatus and methods are described above with reference to FIG. 1 through FIG. 38.

[0077] The illustrations of apparatus such as memory devices 100, 200, 500, 3000, and 3200, and memory cells 210, 211, 212, 2910, 2911, 2912, 3010, 3811, and 3812 are intended to provide a general understanding of the structure of various embodiments and not a complete description of all the elements and features of the apparatus that might make use of the structures described herein.

[0078] The apparatus of various embodiments may include or be included in electronic circuitry used in high-speed computers, communication and signal processing circuitry, memory modules, portable memory storage devices (e.g., thumb drives), single or multi-processor modules, single or multiple embedded processors, multi-core processors, data switches, and application-specific modules including multilayer, multi-chip modules. Such apparatus may further be included as sub-components within a variety of electronic systems, such as televisions, cellular telephones, personal computers (e.g., laptop computers, desktop computers, handheld computers, tablet computers, etc.), workstations, radios, video players, audio players (e.g., MP3 (Motion Picture Experts Group, Audio Layer 3) players), vehicles, medical devices (e.g., heart monitor, blood pressure monitor, etc.), set top boxes, and others.

[0079] The above description and the drawings illustrate some embodiments of the invention to enable those skilled in the art to practice the embodiments of the invention. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Examples merely typify possible variations. Portions and features of some embodiments may be included in, or substituted for, those of others. Many other embodiments will be apparent to those of skill in the art upon studying and understanding the above description.

[0080] The Abstract is provided to comply with 37 C.F.R. §1.72(b) requiring an abstract that will allow the reader to quickly ascertain the nature and gist of the technical disclosure. The Abstract of the Disclosure is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
As the below named inventor, I hereby declare that: This declaration is directed to: ☐ The attached application, or ☒ United States application or PCT international application number <u>14/041,928</u>, filed on <u>September 30, 2013</u>. The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR Inventor: <u>Sanh D. Tong</u> Date (Optional): _____ Signature: <u>Sanh D. Tong</u>	

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form.
Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9198 and select option 2.

303.812US2

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of
Invention

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

As the below named inventor, I hereby declare that:

This declaration

is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 14/041,928,
filed on September 30, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001
by fine or imprisonment of not more than (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: John K. Zahurak

Date (Optional): 7/10/14

Signature: 

Note: An application data sheet (PTO/58/14 or equivalent), including naming the entire inventive entity, must accompany this form.
Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing this form, call 1-800-PTO-9198 and select option 2.

303.812US2

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	303.B12US6
	Application Number	Unknown
Title of Invention	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.

This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--

Inventor Information:

Inventor 1: Sanh D. Tang					
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Sanh	D.	Tang		
Residence Information (Select One)					
☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
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Address 2					
City	Boise	State/Province	ID		
Postal Code	83709	Country	United States of America		
Inventor 2: John K. Zahurak					
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	John	K.	Zahurak		
Residence Information (Select One)					
☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
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Mailing Address of Inventor:					
Address 1	2633 W. Sugarberry Drive				
Address 2					
City	Eagle	State/Province	ID		
Postal Code	83616	Country	United States of America		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	303.B12US6
	Application Number	Unknown
Title of Invention	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence information of this application.

Customer Number	73115
Email Address	request@slwip.com

Application Information:

Title of the Invention	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		
Attorney Docket Number	303.B12US6	Small Entity Status Claimed ☐	
Application Type	Non-Provisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	38	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country Publication

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	303.B12US6
	Application Number	Unknown

Title of Invention	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
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Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	73115		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status	Pending		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
The current application is a	continuation of	16/125,242	2018-09-07
Prior Application Status	Patented		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/125,242 is a	continuation of	15/722,580	2017-10-02
Prior Application Status	Patented		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/722,580 is a	continuation of	15/188,273	2016-06-21
Prior Application Status	Patented		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/188,273 is a	continuation of	14/041,928	2013-09-30
Prior Application Status	Patented		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/041,928 is a	division of	12/825,211	2010-06-28

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	303.B12US6
	Application Number	Unknown
Title of Invention	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME	
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.		

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the POX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country	Parent Filing Date (YYYY-MM-DD)	Access Code (if applicable)

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	303.B12US6
	Application Number	Unknown
Title of Invention	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant must opt-out of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is ONLY reviewed and processed with the INITIAL filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby grants the USPTO authority to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

- A. Applicant DOES NOT authorize the USPTO to permit a participating foreign IP office access to the instant**
☐ application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.
- B. Applicant DOES NOT authorize the USPTO to transmit to the EPO any search results from the instant patent**
☐ application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	303.B12US6
	Application Number	Unknown
Title of Invention	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.

This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Applicant: Micron Technology, Inc.				
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.				
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117		☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign		☐ Person who shows sufficient proprietary interest		
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:				
☐ Deceased		☐ Legally incapacitated		
Name of the Deceased or Legally Incapacitated Inventor :				
If the Applicant is an Organization check here: ☒				
Organization Name: Micron Technology, Inc.				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information:				
Address 1	8000 So. Federal Way			
Address 2				
City	Boise	State/Province	ID	
Country	United States of America	Postal Code	83716-9632	
Phone Number				
Email Address				

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	303.B12US6
	Application Number	Unknown
Title of Invention	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.

This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country		Postal Code		
Phone Number		Fax Number		
Email Address				

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the <u>INITIAL</u> filing of the application and either box A or B is <u>not</u> checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c). This Application Data Sheet must be signed by a patent practitioner if one or more of the applicants is a juristic entity (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, <u>all</u> joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of <u>all</u> joint inventor-applicants. See 37 CFR 1.4(d) for the manner of making signatures and certifications.					
Signature	/ Viet Tong /			Date (YYYY-MM-DD)	2019-12-16
First Name	Viet	Last Name	Tong	Registration Number	45,416

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-14**

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Micron Technology, Inc.

Application No./Patent No.: Unknown Filed/Issue Date: Herewith

Titled: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Micron Technology, Inc. a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
 - ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
 - ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 025076, Frame 0771-0775, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

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2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)

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Reel _____, Frame _____, or for which a copy thereof is attached.☐ Additional documents in the chain of title are listed on a supplemental sheet(s).☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

 / Viet Tong /
SignatureDecember 16, 2019
DateViet V. Tong
Printed or Typed NameUSPTO Reg. No. 45,416
Title or Registration Number

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:



Practitioners associated with Customer Number:

73115

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:



The address associated with Customer Number:

73115

OR

☐	Firm or Individual Name			
	Address			
	City	State	Zip	
	Country			
	Telephone	Email		

Assignee Name and Address: Micron Technology, Inc
8000 So. Federal Way
Boise ID 83716-9632
United States of America

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	7/9/14
Name	Joel L. Poppen	Telephone	
Title	VP of Legal Affairs, General Counsel and Corporate Secretary for Micron Technology, Inc.		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	<i>Complete if Known</i>	
	Application Number	16/716,177
	Filing Date	December 16, 2019
	First Named Inventor	Sanh D. Tang
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 1 of 6	Attorney Docket No: 303.B12US6	

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	US-5,473,179	12/5/1995	Hong, Gary
	US-7,705,388	4/27/2010	Iwata, Yoshihisa
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	Application Number	16/716,177
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	First Named Inventor	Sanh D. Tang
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 2 of 6		Attorney Docket No: 303.B12US6

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	First Named Inventor	Sanh D. Tang
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 3 of 6	Attorney Docket No: 303.B12US6	

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Examiner Initial *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T 1
	"Chinese Application Serial No. 201180037212.1, Amendment filed 06-22-16", w/English Translation, 11 pgs		
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Group Art Unit	Unknown												
Examiner Name	Unknown												
Sheet 4 of 6	Attorney Docket No: 303.B12US6												

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Sheet 5 of 6	Attorney Docket No: 303.B12US6	

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Examiner Initial *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 1
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Examiner Initial *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 1
	"Taiwanese Application Serial No. 101105342, Response filed 07-24-15 to Office Action mailed 04-28-15", W/ English Claims, 10 pgs	
	KIM, JIYOUNG, et al., "Novel 3-D structure for ultra high density flash memory with VRAT (Vertical-Recess-Array-Transistor) and PIPE (Planarized Integration on the same PlanE)", 2008 Symposium on VLSI Technology, (June 17-19, 2008), 122-23	
	KOMORI, YOSUKE, et al., "Disturbless Flash Memory due to High Boost Efficiency on BiCS Structure and Optimal Memory Film Stack for Ultra High Density Storage Device", International Electron Devices Meeting Technical Digest, (Dec., 2008), 851-854	
	TANAKA, H., et al., "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory", IEEE Symposium on VLSI Technology, (2007), 14-15	

EXAMINER

DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant is to place a check mark here if English language Translation is attached

S/N 16/716,177

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Sanh D. Tang et al.	Examiner:	Unknown
Serial No.:	16/716,177	Group Art Unit:	Unknown
Filed:	December 16, 2019	Docket:	303.B12US6
Customer No.:	73115	Confirmation No.:	3036
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached PTO 1449 Form be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the PTO 1449 Form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. § 1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed after filing of the application or after the filing of the most recent RCE, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Pursuant to 37 C.F.R. § 1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicant's prior U.S. application, Serial No. 16/125,242, filed on September 7, 2018, which is relied upon for an earlier filing date under 35 U.S.C. § 120.

Applicant brings to the attention of the Examiner the following Office Actions and responses associated with one or more of the inventors of the instant application and/or the assignee of the instant application. This material is available and accessible at the United States

INFORMATION DISCLOSURE STATEMENT

Serial Number: 16/716,177

Filing Date: December 16, 2019

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Page 2

Dkt: 303.B12US6

Patent and Trademark Office.

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Application Serial No. 12/825,211, Preliminary Amendment filed 03-21-11, 3 pgs

Application Serial No. 12/825,211, Restriction Requirement mailed 02-21-12, 5 pgs

Application Serial No. 12/825,211, Response filed 03-22-12 to Restriction Requirement mailed 02-21-12, 9 pgs

Application Serial No. 12/825,211, Non Final Office Action mailed 06-07-12, 15 pgs

Application Serial No. 12/825,211, Response filed 09-07-12 to Non Final Office Action mailed 06-07-12, 13 pgs

Application Serial No. 12/825,211, Final Office Action mailed 02-01-13, 11 pgs

Application Serial No. 12/825,211, Response filed 04-30-13 to Final Office Action mailed 02-01-13, 10 pgs

Application Serial No. 12/825,211, Notice of Allowance mailed 05-28-13, 12 pgs

Application Serial No. 12/825,211, Preliminary Amendment filed 09-26-13, 11 pgs

Application Serial No. 12/825,211, Notice of Allowance mailed 03-31-14, 8 pgs

SEMICONDUCTOR CHARGE STORAGE APPARATUS AND METHODS

Application Serial No. 13/035,700, Restriction Requirement mailed 10-19-11, 9 pgs

Application Serial No. 13/035,700, Non Final Office Action mailed 02-13-12, 8 pgs

Application Serial No. 13/035,700, Response filed 05/14/12 to Non Final Office Action mailed 02/13/12, 13 pgs.

Application Serial No. 13/035,700, Final Office Action mailed 07-27-12, 9 pgs

Application Serial No. 13/035,700, Response filed 10-29-12 to Final Office Action mailed 07-27-12, 10 pgs

Application Serial No. 13/035,700, Notice of Allowance mailed 03-20-13, 8 pgs

Application Serial No. 13/035,700, Notice of Allowance mailed 10-09-13, 9 pgs

Application Serial No. 13/035,700, Notice of Allowance mailed 02-24-14, 7 pgs

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Application Serial No. 14/041,928, Preliminary Amendment filed 11-06-13, 6 pgs

Application Serial No. 14/041,928, Non Final Office Action mailed 09-17-14, 12 pgs

Application Serial No. 14/041,928, Response filed 12-17-14 to Non Final Office Action mailed 09-17-14, 7 pgs

Application Serial No. 14/041,928, Final Office Action mailed 03-26-15, 12 pgs

Application Serial No. 14/041,928, Response to Final Office Action mailed 03-26-15, 5 pgs.

Application Serial No. 14/041,928, Non Final Office Action mailed 08-19-15, 7 pgs

Application Serial No. 14/041,928, Response filed 11-19-15 to Non Final Office Action mailed 08-19-15, 9 pgs

Application Serial No. 14/041,928, Notice of Allowance mailed 02-24-16, 9 pgs

CHARGE STORAGE APPARATUS AND METHODS

Application Serial No. 14/310,790, Non Final Office Action mailed 10-30-14, 8 pgs

Application Serial No. 14/310,790, Response filed 01-16-15 to Non Final Office Action mailed 10-30-14, 7 pgs.

Application Serial No. 14/310,790, Notice of Allowance mailed 04-29-15, 7 pgs

Application Serial No. 14/310,790, Notice of Allowance mailed 09-01-15, 7 pgs

CHARGE STORAGE APPARATUS AND METHODS

Application Serial No. 14/987,370, Non Final Office Action mailed 07-15-16, 10 pgs

Application Serial No. 14/987,370, Response filed 11-15-16 to Non Final Office Action mailed 07-15-16, 8 pgs

INFORMATION DISCLOSURE STATEMENT

Serial Number: 16/716,177

Filing Date: December 16, 2019

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

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Dkt: 303.B12US6

Application Serial No. 14/987,370, Notice of Allowance mailed 12-20-16, 7 pgs

Application Serial No. 14/987,370, Notice of Allowance mailed 05-08-17, 7 pgs

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Application Serial No. 15/188,273, Non Final Office Action mailed 12-01-16, 22 pgs

Application Serial No. 15/188,273, Resonse filed 04-28-17 to Non Final Office Action mailed 12-01-16, 9 pgs.

Application Serial No. 15/188,273, Notice of Allowance mailed 07-13-17, 10 pgs

CHARGE STORAGE APPARATUS AND METHODS

Application Serial No. 15/691,442, Restriction Requirement mailed 06-20-18, 6 pgs

Application Serial No. 15/691,442, Response filed 08-20-18 to Restriction Requirement mailed 08-20-18, 7 pgs.

Application Serial No. 15/691,442, Non Final Office Action mailed 02-15-19, 12 pgs

Application Serial No. 15/691,442, Response filed 6-17-19 to Non-Final Office Action mailed 2-15-19, 11 pgs

Application Serial No. 15/691,442, Final Office Action mailed 08-15-19, 4 pgs

Application Serial No. 15/691,442, Response filed 10-15-19 to Final Office Action mailed 8-15-19, 5 pgs

Application Serial No. 15/691,442, Notice of Allowance mailed 10-29-19, 5 pgs

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Application Serial No. 15/722,580, Preliminary Amendment filed 10-31-17, 7 pgs

Application Serial No. 15/722,580, Non Final Office Action mailed 03-07-18, 14 pgs

Application Serial No. 15/722,580, Response filed 6-7-18 to Non-Final Office Action mailed 3-7-18, 7 pgs

Application Serial No. 15/722,580, Notice of Allowance mailed 07-27-18, 11 pgs

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Application Serial No. 16/125,242, Non Final Office Action mailed 06-25-19, 12 pgs

Application Serial No. 16/125,242 Response filed 07-18-19 to Non Final Office Action mailed 05-25-19, 8 pgs.

Application Serial No. 16/125,242, Notice of Allowance mailed 08-09-19, 8 pgs

Pursuant to 37 C.F.R. § 1.98(a)(2), copies of cited U.S. Patents and Published Applications, and Non-Published Applications identifiable by USPTO Serial Number, are no longer required to be provided to the Office. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R § 1.98(a)(2).

INFORMATION DISCLOSURE STATEMENT

Serial Number: 16/716.177

Filing Date: December 16, 2019

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

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Dkt: 303.B12US6

The Examiner is invited to contact the undersigned at the telephone number indicated if there are any questions regarding this communication.

Respectfully submitted,

SCHWEGMAN LUNDBERG & WOESSNER, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 373-6969

Date 12-18-19 By / Viet Tong /

VVT:mlsl

Viet V. Tong

Reg. No. 45,416

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Sanh D. Tang et al.	Examiner:	Unknown
Serial No.:	16/716,177	Group Art Unit:	Unknown
Filed:	December 16, 2019	Docket:	303.B12US6
Customer No.:	73115	Confirmation No.:	3036
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

COMMUNICATION CONCERNING PRIOR OR COPENDING APPLICATION(S)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Pursuant to the guidance of MPEP §§ 2001.06(b) and 2004(9), Applicant would like to bring the following additional application(s) to the Examiner's attention. The identification of these applications is not intended to suggest that the subject matter claimed in any listed application is, or has been, substantially similar to any claim or claims in the present application.

<u>Serial No./ Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
12/825,211 8,803,214	June 28, 2010	303.B12US1	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
14/041,928 9,379,005	September 30, 2013	303.B12US2	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
15/188,273 9,780,115	June 21, 2016	303.B12US3	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
15/722,580 10,090,324	October 2, 2017	303.B12US4	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
16/125,242 10,510,769	September 7, 2018	303.B12US5	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
13/035,700 8,759,895	February 25, 2011	303.B44US1	SEMICONDUCTOR CHARGE STORAGE APPARATUS AND METHODS

COMMUNICATION CONCERNING PRIOR OR COPENDING APPLICATIONS

Page 2

Serial Number: 16/716,177

Dkt: 303 B12US6

Filing Date: December 16, 2019

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

14/987,370 9,754,953	January 4, 2016	303.B44US3	CHARGE STORAGE APPARATUS AND METHODS
14/310,790 9,231,117	June 20, 2014	303.B44US2	CHARGE STORAGE APPARATUS AND METHODS
15/691,442	August 30, 2017	303.B44US4	CHARGE STORAGE APPARATUS AND METHODS

Respectfully submitted,

SCHWEGMAN LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 12-18-19 By / Viet Tong /
Viet V. Tong
Reg. No. 45,416

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.: 303.B12US6
Filed: December 16, 2019

Examiner: Unknown

Customer No.: 73115

Serial No.: 16/716,177

Due Date: N/A

Group Art Unit: Unknown

Confirmation No.: 3036

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ Communication Concerning Prior and Copending Applications (2 pgs.)
- ☒ Information Disclosure Statement (4 pgs.), Form 1449 (6 pgs.) Documents NOT enclosed, cited in parent application

If not provided for in a separate paper filed herewith, please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743. If applicable, any papers or fees supplied herewith are considered to be timely filed pursuant to 37 C.F.R. § 1.7(a), the response period falling on a Federal Holiday, Saturday or Sunday being extended to the next succeeding business day.

SCHWEGMAN LUNDBERG & WOESSNER, P.A.

Customer No.: 73115

/ Viet Tong /

By: _____

Viet V. Tong

Reg. No. 45,416

Electronic Acknowledgement Receipt

EFS ID:	38075367
Application Number:	16716177
International Application Number:	
Confirmation Number:	3036
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Ognyan I. Beremski/Marcie Svitoris
Filer Authorized By:	Ognyan I. Beremski
Attorney Docket Number:	303.B12US6
Receipt Date:	18-DEC-2019
Filing Date:	
Time Stamp:	16:20:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		16716177_IDS_12-18-19.pdf	243080	yes	13
			df59722d77f1806303e2b05255f9d130766d1029		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Information Disclosure Statement (IDS) Form (SB08)	8	13
	Transmittal Letter	4	7
	Miscellaneous Incoming Letter	2	3
	Miscellaneous Incoming Letter	1	1

Warnings:

Information:

Total Files Size (in bytes):	243080
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/716,177				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760			
TOTAL CLAIMS (37 CFR 1.16(j))	20	minus 20 = *			OR	x 100 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 460 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1720			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/716,177	12/16/2019	2827	1720	303.B12US6	20	3

CONFIRMATION NO. 3036

FILING RECEIPT

73115
SCHWEGMAN LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402



Date Mailed: 01/10/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Sanh D. Tang, Boise, ID;
John K. Zahurak, Eagle, ID;

Applicant(s)

Micron Technology, Inc., Boise, ID;

Power of Attorney: The patent practitioners associated with Customer Number 73115

Domestic Priority data as claimed by applicant

This application is a CON of 16/125,242 09/07/2018 PAT 10510769
which is a CON of 15/722,580 10/02/2017 PAT 10090324
which is a CON of 15/188,273 06/21/2016 PAT 9780115
which is a CON of 14/041,928 09/30/2013 PAT 9379005
which is a DIV of 12/825,211 06/28/2010 PAT 8803214

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/08/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/716,177**

Projected Publication Date: 04/16/2020

Non-Publication Request: No

Early Publication Request: No
Title

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	<i>Complete if Known</i>	
	Application Number	16/716,177
	Filing Date	December 16, 2019
	First Named Inventor	Sanh D. Tang
	Group Art Unit	2827
	Examiner Name	Unknown
Sheet 1 of 1		Attorney Docket No: 303.B12US6

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Examiner Initial *	Foreign Document Number	Publication Date	Name of Patentee or Applicant of cited Document	T 1
	KR-102005475B1	7/24/2019	Tang, Sanh D., et al.	
	SG-10201907425TA	9/27/2019	Tang, Sanh, et al.	

OTHER DOCUMENTS – NON PATENT LITERATURE DOCUMENTS

Examiner Initial *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 1
	"European Application Serial No. 11807258.6, Communication Pursuant to Article 94(3) EPC mailed 10-07-19", 4 pgs	
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	"Korean Application Serial No. 10-2019-7021776, Response filed 01-22-20 to Notice of Preliminary Rejection mailed 11-22-19", w/ English Claims, 16 pgs	

EXAMINER

DATE CONSIDERED

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Espacenet

Bibliographic data: KR20130131285 (A) — 2013-12-03

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Inventor(s): TANG SANH D [US]; ZAHURAK JOHN K [US] ± (TANG SANH D, ; ZAHURAK JOHN K, ; 탕, 산흐, 디., ; 자후락, 존, 케이.)

Applicant(s): MICRON TECHNOLOGY INC [US] ± (MICRON TECHNOLOGY, INC, ; 마이크론 테크놀로지, 인크.)

Classification: - international: H01L21/8247; H01L27/115
 - cooperative: G11C13/004; G11C13/0069; G11C13/0097;
G11C16/10; G11C16/14; G11C16/26;
H01L21/76838; H01L23/528; H01L27/0688;
H01L27/11519; H01L27/11548; H01L27/11551;
H01L27/11556; H01L27/11565; H01L27/11575;
H01L27/11578; H01L27/11582; H01L27/2454;
H01L27/249; H01L29/40114; H01L29/66825;
H01L29/66833; H01L29/7889; H01L29/7926;
G11C2213/71; H01L45/06 more

Application number: KR20137001962 20110624 Global Dossier

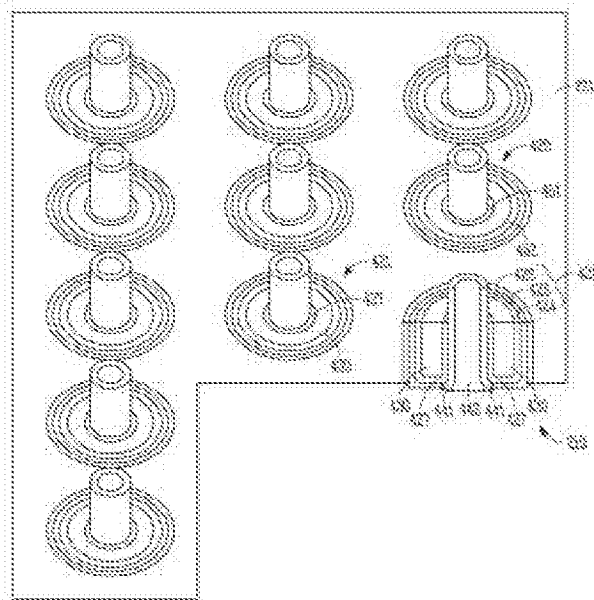
Priority number(s): US20100825211 20100628 ; WO2011US41888 20110624

Also published as: CN103038882 (A) CN103038882 (B) EP2586060 (A2)
EP2586060 (A4) JP2013533628 (A) more

Abstract not available for KR20130131285 (A)

Abstract of corresponding document: US2011316063 (A1)

Some embodiments include a memory device and methods of forming the memory device. One such memory device includes a first group of memory cells, each of the memory cells of the first group being formed in a cavity of a first control gate located in one device level of the memory device. The memory device also includes a second group of memory cells, each of the memory cells of the second group being formed in a cavity of a second control gate located in another device level of the memory device. Additional apparatus and methods are described.



(translation)

LETTERS PATENT

Registration No. : 10-2005475

Registration Date : July 24, 2019

Application No. : 10-2013-7001962

Date of Entry of Korean National Phase : January 24, 2013
(International Filing Date : June 24, 2011)

Term : From July 24, 2019
To June 24, 2031

Title : THREE DIMENSIONAL MEMORY AND METHODS OF
FORMING THE SAME

Owner(s) : MICRON TECHNOLOGY, INC.

Inventor(s) : TANG, Sanh, D.
ZAHURAK, John, K.

* Annuities Due : July 24 each year starting from 2022

* Number of Claims : 27

특허증

CERTIFICATE OF PATENT

특허

Patent Number

제 10-2005475 호

출원번호

Application Number

제 10-2013-7001962 호

출원일

Filing Date

2013년 01월 24일

등록일

Registration Date

2019년 07월 24일

발명의 명칭 Title of the invention

3차원 메모리 및 이를 형성하는 방법들

특허권자 Patentee

마이크론 테크놀로지, 인크.

미국, 아이다호, 보이세, 사우스 페더럴 웨이 8000

발명자 Inventor

등록사항란에 기재

위의 발명은 「특허법」에 따라 특허등록원부에 등록되었음을 증명합니다.

This is to certify that, in accordance with the Patent Act, a patent for the invention has been registered at the Korean Intellectual Property Office.



특허청

Korean Intellectual
Property Office

2019년 07월 24일

특허청장

COMMISSIONER,

KOREAN INTELLECTUAL PROPERTY OFFICE

박원주



QR코드로 현재기준
등록사항을 확인하세요

등 록 사 항

특 허

등록 제 10-2005475 호

Patent Number

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(19) 대한민국특허청(KR)

(12) 등록특허공보(B1)

(45) 공고일자 2019년07월31일

(11) 등록번호 10-2005475

(24) 등록일자 2019년07월24일

(51) 국제특허분류(Int. Cl.)

H01L 27/115 (2017.01) H01L 21/8247 (2006.01)

(21) 출원번호 10-2013-7001962

(22) 출원일자(국제) 2011년06월24일

심사청구일자 2016년06월24일

(85) 번역문제출일자 2013년01월24일

(65) 공개번호 10-2013-0131285

(43) 공개일자 2013년12월03일

(86) 국제출원번호 PCT/US2011/041888

(87) 국제공개번호 WO 2012/009140

국제공개일자 2012년01월19일

(30) 우선권주장

12/825,211 2010년06월28일 미국(US)

(56) 선행기술조사문헌

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(뒷면에 계속)

전체 청구항 수 : 총 27 항

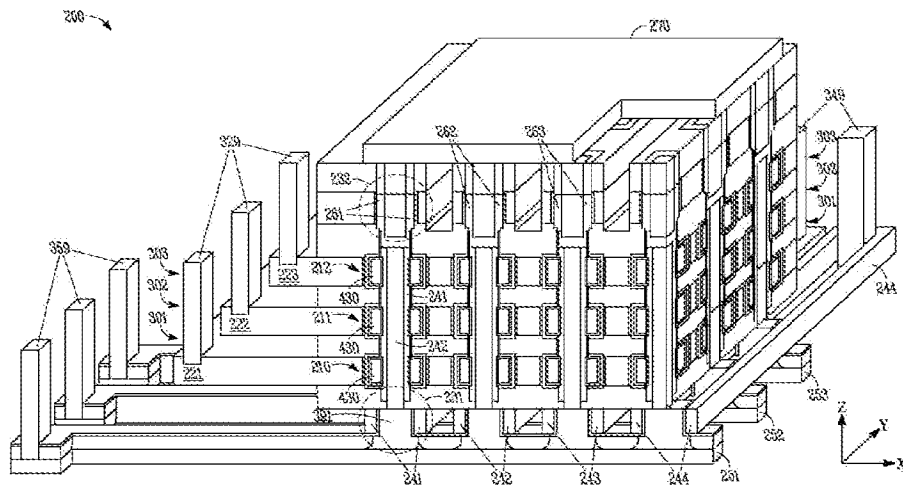
심사관 : 고연화

(54) 발명의 명칭 3차원 메모리 및 이를 형성하는 방법들

(57) 요약

몇몇 실시예들은 메모리 디바이스 및 메모리 디바이스를 형성하는 방법들을 포함한다. 하나의 이러한 메모리 디바이스는 제 1 그룹의 메모리 셀들을 포함하며, 제 1 그룹의 각각의 메모리 셀들은 메모리 디바이스의 하나의 디바이스 레벨에 위치된 제 1 제어 게이트의 공동에 형성된다. 또한, 메모리 디바이스는 제 2 그룹의 메모리 셀들을 포함하며, 제 2 그룹의 각각의 메모리 셀들은 메모리 디바이스의 또 다른 디바이스 레벨에 위치된 제 2 제어 게이트의 공동에 형성된다. 추가적인 장치 및 방법들이 설명된다.

배치도



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명세서

청구범위

청구항 1

메모리 디바이스(memory device)의 제 1 디바이스 레벨에 위치한 제 1 메모리 셀들:

상기 메모리 디바이스의 제 2 디바이스 레벨에 위치한 제 2 메모리 셀들:

상기 제 1 디바이스 레벨에 형성된 제 1 제어 게이트(control gate)로서, 상기 제 1 제어 게이트는 상기 제 1 메모리 셀들에 대한 액세스(access)를 제어하기 위한 것이며, 상기 제 1 메모리 셀들의 각각은 상기 제 1 제어 게이트의 공동(cavity)에 형성된 메모리 소자를 포함하는, 상기 제 1 제어 게이트:

상기 제 2 디바이스 레벨에 형성된 제 2 제어 게이트로서, 상기 제 2 제어 게이트는 상기 제 2 메모리 셀들에 대한 액세스를 제어하기 위한 것이며, 상기 제 2 메모리 셀들의 각각은 상기 제 2 제어 게이트의 공동에 형성된 메모리 소자를 포함하는, 상기 제 2 제어 게이트; 및

상기 제 1 및 제 2 메모리 셀들에 저장된 정보의 값들을 나타내는 신호들을 전달하기 위한, 기판 위의 데이터 라인

을 포함하고,

상기 데이터 라인은 상기 기판과 상기 제 1 메모리 셀들 사이에 위치되는, 장치.

청구항 2

삭제

청구항 3

삭제

청구항 4

청구항 1에 있어서,

공통 소스를 더 포함하고,

상기 공통 소스는 상기 기판 위에 형성되어, 상기 제 1 및 제 2 메모리 셀들이 상기 공통 소스와 상기 기판 사이에 있도록 하는, 장치.

청구항 5

청구항 1에 있어서,

상기 제 1 메모리 셀들은 상기 제 2 메모리 셀들과 실질적으로 수직으로 정렬되는, 장치.

청구항 6

청구항 1에 있어서,

상기 제 1 메모리 셀들 각각의 상기 메모리 소자는 상기 제 2 메모리 셀들 중 하나의 상기 메모리 소자와 실질적으로 수직으로 정렬되는, 장치.

청구항 7

청구항 1에 있어서,

상기 메모리 디바이스의 메모리 동작 동안, 상기 데이터 라인에 상기 제 1 및 제 2 메모리 셀들을 선택적으로 결합하기 위한 트랜지스터(transistor)로서, 상기 트랜지스터들 중 적어도 하나는 이중-게이트(double-gate)를 포함하는, 상기 트랜지스터들을 더 포함하는, 장치.

청구항 8

청구항 1에 있어서,

상기 메모리 디바이스의 메모리 동작 동안, 상기 데이터 라인에 상기 제 1 및 제 2 메모리 셀들을 선택적으로 결합하기 위한 트랜지스터로서, 상기 트랜지스터들 중 적어도 하나는 둘러싸인 게이트(surrounded gate)를 포함하는, 상기 트랜지스터들을 더 포함하는, 장치.

청구항 9

제 1 메모리 소자를 포함하는 제 1 비-휘발성 메모리 셀로서, 상기 제 1 메모리 소자는 링(ring) 형상을 갖는, 상기 제 1 비-휘발성 메모리 셀;

제 2 메모리 소자를 포함하는 제 2 비-휘발성 메모리 셀로서, 상기 제 2 메모리 소자는 링 형상을 갖는, 상기 제 2 비-휘발성 메모리 셀;

상기 제 1 및 제 2 메모리 소자들을 지나 연장하는 도전 재료; 및

상기 제 1 및 제 2 메모리 셀들에 저장된 정보의 값들을 나타내는 신호들을 전달하기 위한, 기판 위의 데이터 라인을 포함하며,

상기 데이터 라인은 상기 기판 및 상기 제 1 메모리 셀 사이에 위치되는, 장치.

청구항 10

청구항 9에 있어서,

상기 제 1 메모리 셀에 액세스하기 위한 제어 게이트로서 동작하도록 구성된 제 1 부가적인 도전 재료로서, 상기 제 1 메모리 소자 및 상기 제 1 부가적인 도전 재료는 상기 제 1 및 제 2 메모리 셀들이 위치되는 메모리 디바이스의 제 1 디바이스 레벨에 위치되는, 상기 제 1 부가적인 도전 재료; 및

상기 제 2 메모리 셀에 액세스하기 위한 제어 게이트로서 동작하도록 구성된 제 2 부가적인 도전 재료로서, 상기 제 2 메모리 소자 및 상기 제 2 부가적인 도전 재료는 상기 메모리 디바이스의 제 2 디바이스 레벨에 위치되는, 상기 제 2 부가적인 도전 재료를 더 포함하는, 장치.

청구항 11

청구항 10에 있어서,

상기 메모리 셀들의 각각은 상기 각각의 메모리 소자 및 상기 도전 재료 사이에 제 1 유전체(dielectric)를 더 포함하는, 장치.

청구항 12

청구항 11에 있어서,

상기 메모리 셀들의 각각은 상기 각각의 메모리 소자 및 상기 각각의 부가적인 도전 재료 사이에 제 2 유전체를 더 포함하는, 장치.

청구항 13

삭제

청구항 14

삭제

청구항 15

메모리 디바이스의 제 1 디바이스 레벨에 위치된 제 1 도전 재료로서, 상기 제 1 도전 재료는 제 1 공동을 포함하며, 상기 제 1 공동은 제 1 측벽(sidewall)을 갖는, 상기 제 1 도전 재료;

상기 메모리 디바이스의 제 2 디바이스 레벨에 위치된 제 2 도전 재료로서, 상기 제 2 도전 재료는 제 2 공동을

포함하며, 상기 제 2 공동은 제 2 측벽을 갖는, 상기 제 2 도전 재료;

상기 제 1 측벽 및 상기 제 2 측벽 상에 형성된 제 1 유전체;

상기 제 1 공동에 위치되며, 상기 제 1 유전체의 제 1 부분에 의해 상기 제 1 도전 재료로부터 전기적으로 분리된 제 1 메모리 소자;

상기 제 2 공동에 위치되며, 상기 제 1 유전체의 제 2 부분에 의해 상기 제 2 도전 재료로부터 전기적으로 분리된 제 2 메모리 소자;

상기 제 1 메모리 소자의 측면 상에 및 상기 제 2 메모리 소자의 측면 상에 형성된 제 2 유전체;

상기 제 1 디바이스 레벨로부터 상기 제 2 디바이스 레벨로 연장하며 상기 제 1 및 제 2 메모리 소자들을 향하는 도전 채널로서, 상기 도전 채널은 상기 제 2 유전체의 적어도 각각의 부분에 의해 상기 제 1 및 제 2 메모리 소자들로부터 전기적으로 분리되도록 하는, 상기 도전 채널;

가판; 및
상기 도전 채널에 선택적으로 결합되도록 구성된 데이터 라인으로서, 상기 데이터 라인은 상기 제 2 도전 재료와 상기 기판 사이에 위치되는, 상기 데이터 라인

를 포함하는, 장치.

청구항 16

청구항 15에 있어서,

상기 제 1 및 제 2 메모리 소자들은 폴리실리콘(polysilicon)을 포함하는, 장치.

청구항 17

청구항 15에 있어서,

상기 제 1 및 제 2 메모리 소자들은 유전 재료를 포함하는, 장치.

청구항 18

청구항 17에 있어서,

상기 유전 재료는 질리콘 질화물(silicon nitride)을 포함하는, 장치.

청구항 19

청구항 15에 있어서,

상기 제 1 및 제 2 도전 재료를 사이에 유전 재료를 더 포함하는, 장치.

청구항 20

삭제

청구항 21

청구항 15에 있어서,

제 1 및 제 2 메모리 소자들은 상기 데이터 라인과 상기 기판 사이에 위치되는, 장치.

청구항 22

삭제

청구항 23

링 형상을 갖는 제 1 메모리 소자를 포함하는 제 1 비-휘발성 메모리 셀을 형성하는 단계; 및

링 형상을 갖는 제 2 메모리 소자를 포함하는 제 2 비-휘발성 메모리 셀을 형성하는 단계; 및

상기 제 1 및 제 2 메모리 소자들을 지나 연장하는 도전 재료를 형성하는 단계 - 상기 제 1 비-휘발성 메모리 셀을 형성하는 단계는 제 1 도전 재료에 제 1 공동을 형성하는 단계를 포함하고, 상기 제 1 메모리 소자는 상기 제 1 공동에 형성되며, 상기 제 2 비-휘발성 메모리 셀을 형성하는 단계는 제 2 도전 재료에 제 2 공동을 형성하는 단계를 포함하고, 상기 제 2 메모리 소자는 상기 제 2 공동에 형성되며, 상기 제 1 및 제 2 비-휘발성 메모리 셀들은 기판 위에 형성됨 -; 및

상기 기판 위에 데이터 라인을 형성하는 단계

를 포함하고, 상기 데이터 라인은 상기 기판 및 상기 제 1 및 제 2 비-휘발성 메모리 셀들 사이에 위치되는, 방법.

청구항 24

청구항 23에 있어서,

상기 제 1 공동은 상기 제 2 공동 위에 실질적으로 정렬되는, 방법.

청구항 25

링 형상을 갖는 제 1 메모리 소자를 포함하는 제 1 비-휘발성 메모리 셀을 형성하는 단계;

링 형상을 갖는 제 2 메모리 소자를 포함하는 제 2 비-휘발성 메모리 셀을 형성하는 단계;

상기 제 1 및 제 2 메모리 소자들을 지나 연장하는 도전 재료를 형성하는 단계; 및

기판 위에 데이터 라인을 형성하는 단계를 포함하고, 상기 데이터 라인은 상기 기판 및 상기 제 1 및 제 2 메모리 셀들 사이에 위치되는, 방법.

청구항 26

삭제

청구항 27

도전 재료 층들이 유전 재료 층들에 의해 서로로부터 전기적으로 분리되도록, 상기 도전 재료 층들 및 상기 유전 재료 층들을 기판 위에 형성하는 단계;

상기 도전 재료 층들의 각각에 공동들을 형성하는 단계;

상기 공동들의 각각에 메모리 소자를 형성하는 단계; 및

상기 기판 위에 데이터 라인을 형성하는 단계

를 포함하고,

상기 데이터 라인은 상기 기판 및 상기 상기 도전 재료 층들 및 상기 유전 재료 층들 사이에 위치되는, 방법.

청구항 28

청구항 27에 있어서,

상기 도전 재료 층들의 각각은 상기 유전 재료 층들 중 두 개 사이에 있으며,

상기 도전 재료 층들 중 적어도 하나는 상기 도전 재료 층들 중 두 개 사이에 있는, 방법.

청구항 29

청구항 27에 있어서,

상기 메모리 소자는 폴리실리콘을 포함하는, 방법.

청구항 30

청구항 27에 있어서,

상기 메모리 소자는 유전 재료를 포함하는, 방법.

청구항 31

청구항 27에 있어서,

상기 공동들을 형성하는 단계는,

상기 도전 재료 층들에 초기 공동들을 형성하는 단계; 및

상기 도전 재료 층들의 각각에 상기 공동들을 형성하기 위해 상기 초기 공동들의 크기를 확대하는 단계를 포함하는, 방법.

청구항 32

청구항 31에 있어서,

상기 초기 공동들을 형성하기 위해, 상기 도전 재료 층들 및 상기 유전 재료 층들을 통해 개구(opening)들을 형성하는 단계를 더 포함하는, 방법.

청구항 33

청구항 32에 있어서,

상기 개구들이 형성될 때 제 2 공동들이 상기 유전 재료 층들의 각각에 형성되며,

상기 초기 공동들의 크기가 확대될 때 상기 제 2 공동들의 크기는 실질적으로 변하지 않은 채로 있는, 방법.

청구항 34

청구항 33에 있어서,

상기 제 2 공동들의 각각 및 상기 초기 공동들의 각각은 실질적으로 동일한 직경을 갖는, 방법.

발명의 설명

기술 분야

[0001] 우선권 출원

[0002] 본 출원은 참조로서 본 출원에 통합되는, 2010년 6월 28일에 출원된 미국 출원 번호 제12/825,211호로부터의 우선권 이득을 주장한다.

배경 기술

[0003] 플래시 메모리 디바이스(flash memory device)들과 같은 비-휘발성 메모리 디바이스들은 정보를 저장하기 위해 많은 컴퓨터들 및 전자 디바이스들에서 사용된다. 플래시 메모리 디바이스는 보통 정보(예컨대, 데이터(data) 및 명령 코드(instruction code)들)를 저장하기 위한 기록 동작, 저장된 정보를 검색하기 위한 읽기 동작, 및 메모리로부터 정보를 제거하기 위한 소거 동작을 가진다. 고밀도 메모리 디바이스들에 대한 요구가 증가하면서, 3-차원(3D: three-dimensional) 메모리 디바이스들이 제안되어 왔다. 종래의 3D 메모리 디바이스의 일 예는 Jiyoung Kim 김 등에 의해 Technical Papers의 VLSI Technology Digest에 대한 2008 심포지엄에서 공개된, "Novel 3-D Structure for Ultra High Density Flash Memory with Vertical-Array-Transistor(VRAT) and Planarized Integration on the same Plane(PIPE)"로 명명된 기사, 22-23쪽에 설명된다. 3D 메모리 디바이스들이 비교적 새롭기 때문에, 이들 디바이스들을 제조하는 것은 제작 프로세스(process) 과제들을 제기할 수 있다.

발명의 내용

도면의 간단한 설명

[0004] 도 1은 본 발명의 일 실시예에 따른, 메모리 셀들을 갖는 메모리 어레이(memory array)를 가진 메모리 디바이스의 블록도를 도시한다.

도 2는 본 발명의 일 실시예에 따른, 메모리 셀들 아래에 위치된 데이터 라인(data line)들을 가진 메모리 디바이스의 일부의 개략도를 도시한다.

도 3은 본 발명의 일 실시예에 따른, 도 2의 메모리 디바이스의 일부의 3-차원 뷰를 도시한다.

도 4는 본 발명의 일 실시예에 따른, 도 3의 메모리 디바이스의 제어 게이트(control gate) 및 메모리 셀의 일부를 도시한다.

도 5 내지 도 29는 본 발명의 일 실시예에 따른, 메모리 셀들 아래에 위치된 데이터 라인들을 가진 메모리 디바이스를 형성하는 다양한 프로세스들을 도시한다.

도 30은 본 발명의 일 실시예에 따른, 메모리 셀들 위에 위치된 데이터 라인들을 가진 메모리 디바이스의 일부의 개략도를 도시한다.

도 31은 본 발명의 일 실시예에 따른, 도 30의 메모리 디바이스의 일부의 3-차원 뷰를 도시한다.

도 32 내지 도 38은 본 발명의 일 실시예에 따른, 메모리 셀들 위에 위치된 데이터 라인들을 가진 메모리 디바이스를 형성하는 다양한 프로세스들을 도시한다.

발명을 실시하기 위한 구체적인 내용

[0005] 도 1은 본 발명의 일 실시예에 따른 메모리 셀들(110)을 갖는 메모리 어레이(102)를 가진 메모리 디바이스(100)의 블록도를 도시한다. 메모리 셀들(110)은 액세스 라인(access line)들(123)(예컨대, 신호들(WL0 내지 WLM))을 가진 워드라인(wordline)들 및 라인들(124)(예컨대, 신호들(BL0 내지 BLN))을 가진 비트 라인(bit line)들에 따라 트루(row)들 및 컬럼(column)들로 배열될 수 있다. 메모리 디바이스(100)는 메모리 셀들(110) 내에 정보를 전달하기 위해 라인들(124, 128)을 사용한다. 메모리 셀들(110)은 다수의 디바이스 레벨들에 물리적으로 위치될 수 있어, 메모리 셀들(110)의 하나의 그룹이 다른 메모리 셀들(110)의 하나 이상의 그룹들 상에 적층될 수 있다. 로우 디코더(row decoder)(132) 및 컬럼 디코더(column decoder)(134)는 어느 메모리 셀들(110)이 액세스되는지를 결정하기 위해 라인들(125)(예컨대, 어드레스 라인(address line)들) 상에서 어드레스 신호들(A0 내지 AX)을 디코딩한다. 로우 및 컬럼 디코더들(132, 134) 각각의 로우 및 컬럼 레벨 디코더들(136, 138)은 액세스될 메모리 셀들(110)이 메모리 디바이스(100)의 다수의 디바이스 레벨들 중 어느 것에 위치되는지를 결정한다.

[0006] 감지 증폭기 회로(140)는 메모리 셀들(110)로부터 판독된 정보의 값을 결정하며, 정보를 신호들의 형태로 라인들(124, 128)에 제공한다. 또한, 감지 증폭기 회로(140)는 메모리 셀들(110)에 기록될 정보의 값을 결정하기 위해 라인들(124, 128) 상에서 신호들을 사용할 수 있다. 메모리 디바이스(100)는 메모리 어레이(102) 및 라인들(예컨대, 데이터 라인들)(126) 사이에서 정보를 전달하기 위해 회로(150)를 포함할 수 있다. 라인들(126) 상에서의 신호들(DQ0 내지 DQN)은 메모리 셀들(110)로부터 판독되거나 또는 메모리 셀들에 기록된 정보를 나타낼 수 있다. 라인들(126)은 메모리 디바이스(100) 내의 노드(node)들 또는 메모리 디바이스(100)가 존재하는 패키지(package) 상의 노드들(예컨대, 핀(pin)들 또는 솔더 볼(solder ball)들)을 포함할 수 있다. 메모리 디바이스(100)(예컨대, 메모리 제어기 또는 프로세서) 외부의 다른 디바이스들은 라인들(125, 126, 및 127)을 통해 메모리 디바이스(100)와 통신할 수 있다.

[0007] 메모리 디바이스(100)는 메모리 셀들(110)로부터 정보를 판독하기 위한 판독 동작 및 정보를 메모리 셀들(110)에 저장하기 위한 기록 동작(때때로 프로그래밍 동작(programming operation)으로서 불리우는)과 같은, 메모리 동작들을 수행한다. 메모리 제어 유닛(118)은 라인들(127) 상에서 제어 신호들에 기초하여 메모리 동작들을 제어한다. 라인들(127) 상에서의 제어 신호들의 예들은 메모리 디바이스(100)가 수행하는 동작(예컨대, 기록 또는 판독 동작)을 나타내기 위해 하나 이상의 클럭 신호(clock signal)들 및 다른 신호들을 포함한다. 메모리 디바이스(100) 외부에 있는 다른 디바이스들(예컨대, 프로세서 또는 메모리 제어기)은 라인들(127) 상에서의 제어 신호들의 값들을 제어할 수 있다. 이들 라인들 상에서의 신호들의 조합의 특정 값들은 메모리 디바이스(100)가 대응하는 메모리 동작(예컨대, 기록 또는 판독 동작)을 수행하게 하는 명령어(command)(예컨대, 기록 또는 판독 명령어)를 생성할 수 있다.

[0008] 각각의 메모리 셀들(110)은 단일 비트의 값 또는 2, 3, 4, 또는 다른 다수의 비트들과 같은, 다중 비트들의 값을 나타내는 정보를 저장할 수 있다. 예를 들면, 각각의 메모리 셀들(110)은 단일 비트의 이진 값(binary value)("0" 또는 "1")을 나타내는 정보를 저장할 수 있다. 또 다른 예에서, 각각의 메모리 셀들(110)은 2 비트들의 4개의 가능한 값들("00", "01", "10", 및 "11") 중 하나, 8개의 가능한 값들("000", "001", "010",

"011", "100", "101", "110", 및 "111") 중 하나 또는 다중 비트들의 다른 수의 다른 값들 중 하나를 나타내는 정보를 저장할 수 있다.

- [0009] 메모리 디바이스(100)는 각각 라인들(141, 142) 상에서 공급 전압 신호들(Vcc, Vss)을 포함하는, 공급 전압을 수신할 수 있다. 공급 전압 신호(Vss)는 접지 전위(예컨대, 대략 제로 볼트들의 값을 갖는)에서 동작할 수 있다. 공급 전압 신호(Vcc)는 배터리 또는 교류 대 직류(AC-DC: alternating-current to direct-current) 변환기 회로와 같은, 외부 전원으로부터 메모리 디바이스(100)에 공급된 외부 전압을 포함할 수 있다.
- [0010] 메모리 디바이스(100)의 회로(150)는 선택 회로(152) 및 입력/출력(I/O: input/output) 회로(116)를 포함할 수 있다. 선택 회로(152)는 메모리 셀들(110)로부터 판독되거나 또는 메모리 셀들에 기록된 정보를 나타낼 수 있는 라인들(124, 128) 상에서 신호들을 선택하기 위해 신호들(SELO 내지 SELn)에 대응한다. 컬럼 디코더(134)는 어드레스 신호들(A0 내지 AX)에 기초하여 신호들(SELO 내지 SELn)을 선택적으로 활성화한다. 선택 회로(152)는 판독 및 기록 동작들 동안 메모리 어레이(102) 및 I/O 회로(116) 사이에 통신을 제공하기 위해 라인들(124, 128) 상에서 신호들을 선택한다.
- [0011] 메모리 디바이스(100)는 비-휘발성 메모리 디바이스일 수 있으며, 메모리 셀들(110)은 전력(예컨대, Vcc 또는 Vss, 또는 둘 모두)이 메모리 디바이스(100)로부터 연결해제될 때 메모리 셀들(110)이 메모리셀들 상에 저장된 정보를 유지할 수 있도록 비-휘발성 메모리 셀들일 수 있다. 예를 들면, 메모리 디바이스(100)는 NAND 플래시 또는 NOR 플래시 메모리 디바이스와 같은 플래시 메모리 디바이스, 또는 가변 저항 메모리 디바이스(예컨대, 위상 변화 랜덤-액세스-메모리(PCRAM: phase change random-access-memory), 저항 RAM(RRAM: resistive RAM) 등)와 같은 다른 종류들의 메모리 디바이스들일 수 있다.
- [0012] 이 기술분야의 숙련자는 본 출원에 설명된 실시예들에 초점을 맞추도록 돕기 위해 메모리 디바이스(100)가 도 1에 도시되지 않은 다른 피쳐(feature)들을 포함할 수 있다는 것을 인식할 수 있다.
- [0013] 메모리 디바이스(100)는 도 2 내지 도 38을 참조하여 이하에 설명되는 메모리 디바이스들 및 메모리 셀들 중 적어도 하나를 포함할 수 있다.
- [0014] 도 2는 본 발명의 일 실시예에 따른, 메모리 셀들(210, 211, 및 212) 아래에 위치한 데이터 라인들(251, 252, 및 253)을 가진 메모리 디바이스(200)의 일부의 개략도를 도시한다. 메모리 셀들(210, 211, 및 212)은 메모리 셀들(210)의 그룹, 메모리 셀들(211)의 그룹, 및 메모리 셀들(212)의 그룹과 같은, 그룹들로 그룹화될 있다. 도 2에 도시된 바와 같이, 각각의 그룹에서의 메모리 셀들은 제어 게이트(221, 222, 또는 223)(연관된 신호들(WL0, WL1, 및 WL2)을 가진)와 같은, 동일한 제어 게이트를 공유한다. 메모리 셀들은 스트링(string)들(215, 216)과 같이, 스트링들로서 직렬로 결합된다. 각각의 스트링은 상이한 그룹들로부터 메모리 셀들 중 하나를 포함할 수 있으며, 트랜지스터들(231) 중 하나와 트랜지스터들(232) 중 하나 사이에 결합된다.
- [0015] 도 2에 도시된 바와 같이, 트랜지스터들(231)은 라인들(241, 242, 및 243)(연관된 신호들(SGD0, SGD1, 및 SGD2)을 가진)을 선택하기 위해 결합된 게이트들을 가진다. 트랜지스터들(231)은 데이터 라인들(251, 252, 및 253)(연관된 신호들(BL0, BL1, 및 BL2)을 가진)에 결합된 노드들(예컨대, 소스(source)들)을 가진다. 데이터 라인들(251, 252, 및 253)은 때때로 비-휘발성 메모리 디바이스의 비트 라인들 또는 감지 라인들에 대응한다.
- [0016] 트랜지스터들(232)은 선택 라인들(261, 262, 및 263)(연관된 신호들(SGS0, SGS1, 및 SGS2)을 가진)에 결합된 게이트들을 가진다. 트랜지스터들(232)은 비-휘발성 메모리 디바이스에서 메모리 셀 스트링들의 공통 소스(270)에 결합된 노드들(예컨대, 드레인(drain)들)을 가진다.
- [0017] 도 2는 일 예로서, 메모리 셀들에 결합된 연관된 구성요소들을 가진 메모리 셀들의 3개의 그룹들을 도시한다. 메모리 셀들의 그룹들의 수 및 메모리 셀들과 연관된 구성요소들(예컨대, 제어 게이트들 및 데이터 라인들)은 변할 수 있다.
- [0018] 메모리 디바이스(200)는 메모리 셀들(210, 211, 및 212)에 저장된 정보를 감지(예컨대, 판독)하기 위한 판독 동작 동안, 및 정보를 메모리 셀들(210, 211, 및 212)에 저장하기 위한 기록 동작 동안, 메모리 셀들(210, 211, 및 212)에 대한 액세스를 제어하기 위해 제어 게이트들(221, 221, 및 223)을 사용한다. 메모리 디바이스들(200)은 판독 동작 동안, 이들 메모리 셀들로부터 판독된 정보를 전달하기 위해 데이터 라인들(251, 252, 및 253)을 사용한다.
- [0019] 트랜지스터들(231, 232)은 판독 또는 기록 동작 동안, 데이터 라인들(251, 252, 및 253) 및 공통 소스(270)에 메모리 셀들을 선택적으로 결합하기 위해, 각각, 신호들(SGD0, SGD1, 및 SGD2) 및 신호들(SGS0, GS1, 및 SGS

2)에 반응한다.

[0020] 본 출원에 설명에 초점을 맞추도록 돕기 위해, 본 출원에서의 설명은 판독, 기록, 및 소거 동작과 같은, 메모리 디바이스의 동작들의 상세한 설명을 생략한다. 이 기술분야의 숙련자는 이들 동작들을 인식할 것이다. 예를 들면, 메모리 디바이스(200)의 소거 동작에서, 제어 게이트들(221, 221, 및 223), 선택 라인들(241, 242, 및 243), 및 선택 라인들(261, 262, 및 263)이 "플로팅(floating)"될 수 있는(예컨대, 전압에 연결되지 않은 채로 있는) 동안, 대략 20 볼트들의 전압이 데이터 라인들(251, 252, 및 253)에 인가될 수 있다. 이러한 소거 동작에서, 메모리 셀들(210, 211, 및 212)의 메모리 소자들로부터의 전자들은 데이터 라인들(251, 253, 및 253)로 이동할 수 있다.

[0021] 도 3은 본 발명의 일 실시예에 따른, 메모리 디바이스(200)의 일부의 3D 뷰를 도시한다. 또한, 도 3은 X, Y, 및 Z 방향들, 및 Z-방향으로 배열된 디바이스 레벨들(301, 302, 및 303)을 도시한다. 동일한 그룹의 메모리 셀들(210)은 X-방향 및 Y-방향에서 로우들 및 컬럼들로 배열될 수 있다. 각각의 메모리 셀들의 그룹은 상이한 디바이스 레벨들(301, 302, 또는 303)에 위치된다. 예를 들면, 메모리 셀들(210)을 가진 그룹은 디바이스 레벨(301)에 위치된다. 메모리 셀들(211)을 가진 그룹은 디바이스 레벨(302)에 위치된다. 메모리 셀들(212)을 가진 그룹은 디바이스 레벨(303)에 위치된다.

[0022] 도 3에 도시된 바와 같이, 각각의 스트링에서의 메모리 셀들(210, 211, 및 212)(예컨대, 트랜지스터들(231, 232) 사이에서의 메모리 셀들)은 데이터 라인들(251, 252, 및 253) 아래의 기판에 대하여 Z-방향으로 실질적으로 수직으로 정렬된다. 기판은 도 3에 도시되지 않지만, 도 5 및 도 6의 기판(503)과 유사할 수 있다. 또한, 도 3은 Z-방향에서 수직으로 및 도 2의 트랜지스터들(231, 232)에 대응하는, 트랜지스터들(231, 232) 사이의 동일한 스트링에서의 메모리 셀들(210, 211, 및 212)의 메모리 소자(430)를 지나 연장하는 도전 재료 부분(242) 및 채널(241)을 도시한다. 도 3에 도시된 바와 같이, 트랜지스터(231)는 트랜지스터를 제어하기 위해(턴 온(turn on) 또는 오프) 몸체(391)(예컨대, 트랜지스터 채널)에 결합된 이중-게이트를 포함할 수 있다. 이중-게이트의 구조는 동일한 선택 라인(241)(도 3에 도시된 바와 같이)의 두 개의 세그먼트(segment)들을 포함할 수 있어, 두 개의 세그먼트들은 몸체(391)의 단지 두 개의 각각의 측면들 상에 위치된다.

[0023] 또한, 도 3에서의 메모리 디바이스(200)는 접촉부들(329, 349, 및 359)을 포함할 수 있다. 접촉부들(329)은 제어 게이트들(221, 222, 및 223)로 전기적 연결들을 제공한다. 접촉부들(349)은 선택 라인들(241, 242, 243, 및 244)로 전기적 연결들을 제공한다. 접촉부들(359)은 데이터 라인들(251, 252, 및 253)로 및 그로부터 전기적 연결들을 제공한다. 선택 라인(244) 및 Z-방향에서의 선택 라인과 연관된 메모리 셀은 도 2에 도시되지 않는다.

[0024] 도 4는 도 3의 메모리 디바이스(200)의 메모리 셀(210) 및 제어 게이트(221)의 일부를 도시한다. 도 2의 제어 게이트들(222, 223) 및 메모리 셀들(211, 212)은 각각, 제어 게이트(221) 및 메모리 셀(210)과 유사한 구조들을 가진다. 도 4에 도시된 바와 같이, 제어 게이트(221)는 공동(cavity)들(420)을 가진 동질 재료를 포함할 수 있으며, 각각의 공동은 동질 재료와 상이한 재료들을 포함하는, 다양한 구성요소들을 갖고 파일링(filing)된다. 다양한 구성요소들은: 메모리 소자(430); 채널(channel)(441), 도전 재료 부분(442), 및 유전체(dielectric)들(421, 427)을 포함한다. 유전체(421)는 상이한 층들로서 배열된 다수의 재료들(422, 423, 및 424)을 포함할 수 있다. 도 4에 도시된 바와 같이, 각각의 메모리 셀(210)의 메모리 소자(430)는 내부 측면(451) 및 외부 측면(452)을 가진 링(ring) 형상(예컨대, 도넛(donut) 형상)을 가진다. 도 3에 도시된 각각의 다른 메모리 셀들(211, 212)도 링 형상을 가진다. 도 3에 도시된 바와 같이, 동일한 스트링(예컨대, 트랜지스터들(231, 232) 사이)에서의 메모리 셀들(210, 211, 및 212) 내에서, 각각의 메모리 셀의 전체 링-형상 메모리 소자(430)는 동일한 스트링에서 각각의 다른 메모리 셀들의 전체 링-형상 메모리 소자와 실질적으로 수직으로 정렬된다(Z-방향으로).

[0025] 각각의 메모리 소자(430)는 메모리 소자 내의 전하의 양(예컨대, 전자들의 수)에 기초하여서와 같은, 정보를 저장할 수 있다. 각각의 이러한 메모리 소자(430)에서, 전하의 양은 메모리 소자에 저장된 정보의 값에 대응한다. 전하의 양은 기록 동작에서 또는 소거 동작에서 제어될 수 있다. 예를 들면, 채널(441) 또는 도전 재료 부분(442), 또는 둘 모두로부터의 전자들은 이 기술분야의 숙련자들에게 알려진 터널링 효과(tunneling effect)로 인해 기록 동작 동안 메모리 소자(430)로 이동할 수 있다. 소거 동작에서, 메모리 소자(430)로부터의 전자들은 채널(441) 또는 도전 재료 부분(442) 또는 둘 모두로, 데이터 라인들(251, 253, 및 253)로 돌아갈 수 있다(도 2 및 도 3). 대안적인 실시예들은 예를 들면, 소자(430)의 저항에 기초하여서와 같은, 정보를 저장할 수 있는 메모리 소자(430)를 사용할 수 있다.

[0026] 도 3의 메모리 디바이스(200)는 도 5 내지 도 29를 참조하여 이하에 설명된 내용과 유사하거나 또는 동일한 프

로세스들을 사용하여 형성될 수 있다.

[0027] 도 5 내지 도 29는 본 발명의 일 실시예에 따른, 메모리 셀들 아래에 위치한 데이터 라인들을 가진 메모리 디바이스(500)를 형성하는 다양한 프로세스들을 도시한다. 메모리 디바이스(500)(도 29에 보다 상세히 도시된)는 도 3의 메모리 디바이스(300)에 대응할 수 있다.

[0028] 도 5는 기판(503)을 가진 메모리 디바이스(500)를 도시하며, 이것은 층들로서 배열된 재료들(501, 502)을 포함할 수 있다. 재료(501)는 벌크 실리콘(bulk silicon)을 포함하거나, 또는 또 다른 반도체 재료일 수 있다. 재료(502)는 유전 재료, 예를 들면, 실리콘 산화물(silicon oxide)일 수 있다. 또한, 도 5는 기판(503) 위에 형성된 재료들(504, 505)을 도시한다. 재료들(504, 505)을 형성하는 것은 기판(503) 위에 도진 재료를 증착(depositing)시키는 것 및 그 후 재료(504) 위에 또 다른 도진 재료를 증착시키는 것을 포함할 수 있다. 재료(504)는 금속 또는 다른 도진 재료들을 포함할 수 있다. 재료(505)는 p-형 실리콘 또는 또 다른 도진 재료들과 같이, 도핑(doping)되지 않은 폴리실리콘(polysilicon) 또는 도핑된 폴리실리콘을 포함할 수 있다.

[0029] 또한, 도 5는 X-방향, X-방향에 수직인 Y-방향, 및 X-방향 및 Y-방향 둘 모두에 수직인 Z-방향을 도시한다. 도 5에 도시된 바와 같이, 재료들(504, 505)은 Z-방향으로 하나 이상의 다른 층들 위에(예컨대, 상에(on)) 하나의 층, 상이한 층들로서 형성될 수 있다.

[0030] 본 출원에 사용된 바와 같이, 둘 이상의 재료들에 대하여 사용된 용어 "상에(on)", 즉 다른 하나 "상위(on)" 하나는 재료들 사이에서의 적어도 몇몇 접촉을 의미하는 한편, "위에(over)" 또는 "오버레이하는(overlaying)"은 또 다른 재료 "상에(on)" 있거나 또는 재료들 사이에 하나 이상의 부가적인 매개 재료들이 존재하는 재료를 나타낼 수 있다(예컨대, 접촉이 반드시 요구되지는 않는다). 별도로 이와 같이 명확하게 서술된 것이 없으면, 용어 "상에(on)", "위에(over)", 또는 "오버레이하는(overlaying)"은 본 출원에 사용된 바와 같이 임의의 방향성을 내포하지 않는다.

[0031] 도 6은 데이터 라인들(651, 652, 및 653) 및 디바이스 구조들(605)이 형성된 후의 메모리 디바이스(500)를 도시한다. 에칭(etching)(예컨대, 드라이 에칭(dry etching))과 같은 프로세스는 재료(502)에서 트렌치 바텀(trench bottom)들을 갖는, 트렌치들(511, 512)을 형성하기 위해 재료들(504, 505)(도 5)의 일부들을 제거하기 위해 사용될 수 있다. 각각의 데이터 라인들(651, 652, 및 653) 및 각각의 디바이스 구조들(605)은 X-방향으로 연장하는 보다 큰 치수(예컨대, 길이)를 가진다. X-방향으로 연장하는 별개의 개구들을 갖는 마스크(mask)(도 6에 도시되지 않음)가 트렌치들(511, 512)을 형성하기 위해 사용될 수 있다. 도 6에 도시된 바와 같이, 트렌치들(511, 512)은 재료(504)(도 5)를 별개의 데이터 라인들(651, 652, 및 653)로 분리하며, 이것은 도 2의 데이터 라인들(251, 252, 및 253)에 대응할 수 있다.

[0032] 도 7은 필러(pillar)들(705)이 메모리 디바이스(500)의 영역(701)에 형성된 후의 메모리 디바이스(500)를 도시한다. 필러들(705)은 메모리 디바이스(500)의 영역(702)에 형성되지 않는다. 단순함을 위해, 도 7 내지 도 29는 도 6의 구조(503)를 도시하지 않는다. 도 7에서, 에칭(예컨대, 드라이 에칭)과 같은 프로세스는 트렌치들(511, 512)에 수직인, Y-방향으로 트렌치들(711, 712, 및 713)을 형성하기 위해 디바이스 구조들(605)의 부분들을 제거하기 위해 사용될 수 있어, 필러들(705)이 도 7에 도시된 바와 같이 형성될 수 있다. Y-방향으로 연장하는 별개의 개구들을 갖는 마스크(도 7에 도시되지 않음)가 트렌치들(711, 712, 및 713)을 형성하기 위해 사용될 수 있다. 각각의 필러(705)는 대략 20 내지 50 나노미터(nanometer)들의 Z-방향으로의 높이를 포함할 수 있다. 도 7에 도시된 바와 같이, 필러들(705)은 X-방향 및 Y-방향에서 로우들 및 컬럼들로(예컨대, 매트릭스(matrix)로) 배열된다. 단순함을 위해, 도 7은 트렌치들(511, 512)에 채워진 유전 재료를 도시하지 않는다. 그러나, 도 7에서의 메모리 디바이스(500)를 형성하는 것은 디바이스 구조(605)의 최상부 표면(715)까지 트렌치들(511, 512)을 채우기 위해 유전 재료(예컨대, 실리콘 산화물)를 형성하는 것을 포함할 수도 있다.

[0033] 도 8은 유전체(831) 및 선택 라인들(841, 842, 843, 및 844)이 형성된 후의 메모리 디바이스(500)를 도시한다. 선택 라인들(841, 842, 843, 및 844)은 각각, 도 3의 선택 라인들(241, 242, 243, 및 244)에 대응할 수 있다. 도 8에서, 유전체들(831)은 필러들(705)로부터 선택 라인들(841, 842, 843, 및 844)을 전기적으로 분리하기 위해 형성된다. 유전체들(831)은 예를 들면, 각각의 필러(705)의 적어도 두 개의 측면들 상에 유전 재료(예컨대, 실리콘 산화물)를 증착시킴으로써, 또는 필러들(705)을 산화시킴으로써 형성될 수 있다. 유전체들(831)이 형성된 후, 선택 라인들(841, 842, 843, 및 844)이 예를 들면, 필러들(705) 및 트렌치들(711, 712, 및 713)(도 7) 위에 도진 재료를 증착시키고, 그 후 도 8에 도시된 구조를 가진 선택 라인들(841, 842, 843, 및 844)을 형성하기 위해 도진 재료의 일부를 제거(예컨대, 에칭)함으로써 형성될 수 있다. 선택 라인들(841, 842, 843, 및 844)에 대한 도진 재료들의 예들은 폴리실리콘, 금속, 또는 TiN 및 TaN과 같은, 다른 도진 재료들을 포함한다.

[0034] 또한, 도 8은 도핑된 영역들(833)을 도시하며, 이것은 디바이스 구조(605)의 선택 부분들로 n-형 불순물들을 삽입함으로써(예컨대, 주입함으로써) 형성될 수 있다. n-형 불순물들의 예들은 인(P: phosphorus) 또는 비소(As: arsenic)와 같은, 원소들을 포함한다. n-형 불순물들을 갖고 삽입되지 않는 디바이스 구조들(605)의 나머지 부분은 도 5를 참조하여 위에서 설명된 바와 같이, p-형 실리콘과 같은, 그것의 원래 재료를 유지할 수 있다.

[0035] 도 9는 선택 라인들(941, 942, 943, 및 944)을 가진 메모리 디바이스(500)를 도시하며, 이것은 도 8의 선택 라인들(841, 842, 843, 및 844)에 대한 대안적인 구조들이다. 도 8에서, 각각의 필터(705)의 반대 측면들은 동일한 선택 라인(841, 842, 843, 또는 844)의 두 개의 상이한 세그먼트들과 연관된다. 도 9에서, 필터들(705)의 최상부 표면들을 제외하고는, 각각의 필터(705)는 선택 라인(941, 942, 943, 또는 944) 중 하나의 재료에 의해 완전히 둘러싸여질 수 있다(예컨대, 각각의 필터(705)의 4개의 측면들이 동일한 선택 라인의 4개의 상이한 세그먼트들과 연관된다). 보다 효율적인 메모리 디바이스가 선택 라인들(841, 842, 843, 및 844)과 비교하여 선택 라인들(941, 942, 943, 및 944)을 갖고 달성될 수 있다. 또한, 선택 라인들(941, 942, 943, 및 944)은 각각, 도 3의 선택 라인들(241, 242, 243, 및 244)에 대한 대안적인 구조들일 수 있다. 따라서, 도 2 및 도 3의 각각의 트랜지스터(231)는 도 9에 도시된 구조를 가진 둘러싸인 게이트를 포함할 수 있다. 따라서, 도 3에 도시된 이중-게이트 대신에, 도 3의 각각의 트랜지스터(231)는 대안적으로 몸체(391)(도 3)를 둘러싸는 동일한 선택 라인(선택 라인(941)과 같은)의 4개의 상이한 세그먼트들을 가진 둘러싸인 게이트를 포함할 수 있다.

[0036] 도 10은 재료들(1001 내지 1007)이 필터들(705) 및 선택 라인들(841, 842, 843, 및 844) 위에 형성된 후의 메모리 디바이스(500)를 도시한다. 재료들(1001 내지 1007)은 메모리 디바이스(500)의 영역들(701, 702) 양쪽 모두에 형성될 수 있다. 그러나, 본 출원에서 설명에 초점을 맞추기 위해, 도 10은 영역(702)에서 재료들(1001 내지 1007)의 몇몇 부분들을 도시하지 않는다. 도 28 및 도 29를 참조하는 이하의 설명은 메모리 디바이스(500)의 영역(702)에 추가적인 구성요소들(예컨대, 도 3의 접촉부들(329)과 유사한 구성요소들)을 형성하는 것을 설명한다.

[0037] 도 10 내지 도 29에서, 단순함을 위해, 메모리 디바이스(500)의 몇몇 구성요소들과 연관된 몇몇 숫자 지정들은 하나의 도면에서 또 다른 도면으로 반복되지 않을 수 있다. 도 10에서, 재료들(1001 내지 1007)을 형성하기 전에, 실리콘 산화물과 같은, 유전 재료(도 10에 도시되지 않음)는 갭(gap)들(1041, 1042, 및 1043)을 채우기 위해 형성될 수 있다. 재료들(1001 내지 1007)을 형성하는 것은 인터리빙(interleaving) 방식으로 유전 재료 및 도전 재료를 교대로 증착시키는 것을 포함할 수 있으며, 따라서 이들 재료들은 도 10에 도시된 바와 같이 Z-방향에서 서로의 위에 교대로 증착된다. 재료들(1001, 1003, 1005, 및 1007)은 실리콘 산화물과 같은 유전 재료들을 포함할 수 있다. 재료들(1002, 1004, 및 1006)은 금속 또는 폴리실리콘(예컨대, p-형 실리콘을 위한 n-형 실리콘)과 같은, 도전 재료를 포함할 수 있다. 도 10에 도시된 바와 같이, 재료들(1001 내지 1007)은 재료들(1002, 1004, 및 1006)이 재료들(1001, 1003, 1005, 및 1007)에 의해 서로로부터 전기적으로 분리되도록, 형성된다.

[0038] 도 11은 개구(opening)들(예컨대, 홈(hole)들)(1101)이 재료(1002 내지 1007)에 형성된 후의 메모리 디바이스(500)를 도시한다. 홈들(1101)은 각각의 홈(1101)이 도 11에 도시된 바와 같이 대응하는 필터(705) 위에 실질적으로 직접 정렬될 수 있도록, 형성된다. 홈들(1101)을 형성하는 것은 재료들(1002 내지 1007)의 각각의 일부를 제거(예컨대, 에칭)하는 것, 재료(1001)에서 정지하는 것을 포함할 수 있으며, 따라서 적어도 재료(1001)의 일부 또는 재료(1001) 전체는 필터들(705)로부터 홈들(1101)을 분리한 채로 남아있다. 홈들(1101)을 형성하는 것은 각각의 재료들(1003, 1005, 및 1007)에 공동들(1110), 및 각각의 재료들(1002, 1004, 및 1006)에 공동들(1120)을 형성하는 것을 초래한다. 도 12에 도시된 바와 같이, 재료들(1003, 1005, 및 1007)에서의 공동들(1110)은 다른 재료들(1002, 1004, 및 1006)에서의 공동들(1120) 위에 실질적으로 직접 정렬된다. 각각의 공동(1110) 및 각각의 공동(1120)은 실질적으로 동일한 직경(D1)을 가질 수 있다. 또한, 직경(D1)은 각각의 공동(1110) 및 각각의 공동(1120)의 위치에서 각각의 홈(1101)의 직경으로 고려될 수 있다.

[0039] 도 12는 공동들(1220)이 재료들(1002, 1004, 및 1006)(제어 게이트들(1221, 1222, 및 1223)을 형성하기 위해 사용됨)에 형성된 후의 메모리 디바이스(500)를 도시한다. 공동들(1220)을 형성하는 것은 공동들(1110)의 크기를 실질적으로 변경하지 않은 채로 유지하면서(예컨대, 실질적으로 직경(D1)에 유지하면서), 공동들(1120)(도 11)의 크기를 확대시키는 것을 포함할 수 있다. 예를 들면, 공동들(1120)(도 11)의 크기를 확대시키는 것은 각각의 공동(1220)의 직경이 실질적으로 직경(D2)으로 증가하도록, 각각의 공동(1120)(도 11)에서의 각각의 재료들(1002, 1004, 및 1006)의 일부를 선택적으로 제거하는 것(예컨대, 선택적 웨트(wet) 또는 드라이 에칭)을 포함할 수 있는 한편, 각각의 공동(1110)에서의 직경(D1)은 실질적으로 변하지 않은 채로 있다. 직경(D2)은 직경(D1)보다 더 크다. 또한, 재료들(1002, 1004, 및 1006)에 공동들(1120)을 형성하는 것은 제어 게이트들(1221,

1222, 및 1223)을 형성하며, 이것은 도 2의 제어 게이트들(221, 222, 및 223)에 대응할 수 있다.

[0040]

도 13은 도 12의 제어 게이트(1221)의 보다 상세한 것들을 도시한다. 도 12의 제어 게이트들(1222, 1223)은 제어 게이트(1221)와 유사한 구조를 가진다. 도 13에 도시된 바와 같이, 제어 게이트(1221)는 X-방향 및 Y-방향에서 로우들 및 컬럼들로 배열되는 도 11의 공동들(1220)을 가진 동결 재료를 포함할 수 있다. 각각의 공동(1220)은 측벽(sidewall)(1225)을 포함할 수 있다.

[0041]

도 14 및 도 15는 유전체들(1421) 및 메모리 소자들(1430)이 공동들(1220)에 형성된 후의 메모리 디바이스(500)를 도시한다. 단순함을 위해, 도 15는 모든 공동들(1220)에 유전체들(1421) 및 메모리 소자들(1430)을 도시하지 않는다. 각각의 유전체(1421)는 측벽(1225) 상에 형성될 수 있으며, 따라서 각각의 유전체(1421)는 제어 게이트(1221)의 재료 및 메모리 소자(1430) 사이에 위치될 수 있으며, 따라서 메모리 소자(1430)는 유전체(1421)의 적어도 일부에 의해 제어 게이트(1221)의 재료로부터 전기적으로 분리될 수 있다. 유전체(1421)를 형성하는 것은 상이한 시간들에서 하나의 재료 후 또 다른 재료로 다수의 재료들(1422, 1423, 및 1424)(도 15)을 형성하는 것을 포함할 수 있다. 재료(1422)를 형성하는 것은 측벽(1225) 상에 유전 재료(예컨대, 실리콘 산화물)를 형성하기 위해 측벽(1225)의 일부(예컨대, 표면)를 산화시키는 것을 포함할 수 있다. 대안적으로, 재료(1422)를 형성하는 것은 측벽(1225) 상에 유전 재료(예컨대, 실리콘 산화물)를 증착시키는 것을 포함할 수 있다. 재료(1423)를 형성하는 것은 재료(1422) 상에 유전 재료(예컨대, 실리콘 산화물)를 증착시키는 것을 포함할 수 있으며, 여기서 유전 재료의 일부는 각각의 공동(1110)의 측벽(1425) 상에 형성될 수도 있다. 재료(1424)를 형성하는 것은 재료(1423) 상에 유전 재료(예컨대, 실리콘 산화물)를 증착시키는 것을 포함할 수 있다.

[0042]

메모리 소자들(1430)은 유전체들(1421)이 형성된 후 형성될 수 있다. 도 15에 도시된 바와 같이, 각각의 메모리 소자(1430)는 도 14의 내부 측면(1451) 및 외부 측면(1452)을 가진 링 형상(예컨대, 도넛 형상)을 가진다. 메모리 소자들(1430)을 형성하는 것은 홀들(1101)에 재료를 증착시키는 것을 포함할 수 있다. 도 14의 공동들(1220)은 실질적으로 공동들(1110)과 정렬되기 때문에, 재료(메모리 소자(1430)를 형성하는)는 공동들(1110, 1120) 모두를 채울 수 있다. 그 후, 메모리 소자들(1430)을 형성하는 재료의 일부(예컨대, 각각의 홀에서의 중심 부분)가 제거될 수 있으며(예컨대, 동일한, 단일의 에칭 단계에서의 에칭에 의해), 따라서 공동들(1110)에서의 재료는 제거될 수 있고(예컨대, 완전히 제거되고) 공동들(1220)에서의 재료는 완전히 제거되지 않지만 부분적으로 제거될 수 있다. 도 14에 도시된 바와 같이, 메모리 소자들(1430)을 형성하는 재료가 공동들(1110)로부터 제거된 후, 유전 재료(1423)(예컨대, 실리콘 질화물(silicon nitride), 재료(1422) 상에 형성된)의 일부가 노출될 수 있다. 도 14에 도시된 바와 같이, 메모리 소자들(1430)을 형성하는 재료가 공동들(1220)로부터 부분적으로 제거된 후, 동일한 홀(1101)과 연관된 메모리 소자(1430)(공동(1220)에서의 나머지 재료에 의해 형성된)는 공동들(1110)의 측벽(1425)(또는 공동들(1110)의 재료들(1422, 1423)의 부분들을 가진 측벽(1425))과 실질적으로 정렬된 그것의 내부 측면(1451)을 가질 수 있다.

[0043]

메모리 소자들(1430)의 재료는 예를 들면, 반도체 재료(semiconductor material)(예컨대, 폴리실리콘), 실리콘 질화물 또는 다른 유전 전하 트래핑 재료들과 같은 유전 전하 트래핑 재료(dielectric charge trapping material), 또는 위상 변화 재료(예컨대, GST)와 같은 가변 저항 재료(variable resistance material)를 포함할 수 있다. 메모리 소자들(1430)을 형성하는 재료의 일부를 제거(예컨대, 에칭)하는 동안, 필러들(705) 위에 위치된 재료(1001)의 부분들(1401)은 부분들(1401)의 두께를 감소시키기 위해 제거될 수도 있다.

[0044]

도 16 및 도 17은 유전체(1627)가 메모리 소자(1430)의 내부 측면(1451) 상에 및 공동들(1110)에 형성된 후의 메모리 디바이스(500)를 도시한다. 유전체(1627)를 형성하는 것은 내부 측면(1451) 상에 유전 재료(예컨대, 실리콘 산화물)를 증착시키는 것을 포함할 수 있다. 대안적으로, 유전체(1627)를 형성하는 것은 메모리 소자(1430)의 일부(예컨대, 내부 측면(1451))를 산화시키는 것을 포함할 수 있다. 유전체(1627)를 형성하는 것은(예컨대, 산화에 의해) 재료(1422) 상에 형성된 재료(1423)(도 14)를 소비할 수도 있으며, 이것은 공동들(1110)의 측벽(1425) 상에 형성된다. 따라서, 유전체(1627)는 재료(1422) 위의 공동들에 형성할 수도 있다.

[0045]

도 18 및 도 19는 채널들(1841)이 공동들(1110, 1220) 모두에서의 유전체들(1627) 상에 형성된 후의 메모리 디바이스(500)를 도시한다. 채널들(1841)을 형성하는 것은 유전체들(1627) 상에 도전 재료를 증착시키는 것을 포함할 수 있다. 에칭 프로세스는 도전 재료가 증착된 후 도전 재료의 두께를 감소시키기 위해 사용될 수 있다. 채널들(1841)의 도전 재료는 도핑된 폴리실리콘을 포함할 수 있으며, 이것은 필러들(705)과 동일한 재료 유형(예컨대, p-형)을 가질 수 있다. 또한, 도 18은 개구들(1801)의 형성을 도시하며, 이것은 필러들(705) 위에 위치된 부분들(1401)(도 14)을 제거함으로써(예컨대, 에칭에 의해) 형성될 수 있다. 도 19에 도시된 바와 같이, 채널(1841)은 메모리 소자들(1430)을 향하고 있으며, 적어도 유전체(1627)의 일부에 의해 메모리 소자(1430)로

부터 전기적으로 분리된다.

- [0046] 도 20은 도전 재료(2001)가 예컨대, 필터들(705)과의 전기적 통신에 채널들(1841)을 위치시키기 위해 도핑되지 않거나 또는 저농도 도핑된 폴리실리콘을 증착시킴으로써 형성된 후의 메모리 디바이스(500)를 도시한다. 도 20에 도시된 바와 같이, 도전 재료(2001)는 필터들(705)을 통해 채널들(1841) 및 데이터 라인들(651, 652, 및 653) 사이에 연속적인 도전 경로를 형성한다.
- [0047] 도 21은 유전 재료(2101)(예컨대, 실리콘 산화물)가 도전 재료(2001) 위에 형성된 후의 메모리 디바이스(500)를 도시한다.
- [0048] 도 22는 개구들(예컨대, 홀들(2201)), 도전 재료 부분(2260), 및 도전 재료 부분들(2241)의 형성 후의 메모리 디바이스(500)를 도시한다. 도 22에 도시된 바와 같이, 홀들(2201)은 각각의 홀(2201)이 채널들(1841) 위에 실질적으로 직접 정렬될 수 있도록, 형성된다. 홀들(2201)을 형성하는 것은 유전 재료(2101)의 일부 및 도전 재료(2001)(도 21)의 일부를 제거(예컨대, 에칭)하는 것, 재료(1007)에서의 위치에서 정지하는 것을 포함할 수 있다. 도 22에 도시된 바와 같이, 홀들(2201)은 도전 재료(2001)의 일부가 홀들(2201)의 형성 동안 제거된 후, 도전 재료(2001)가 도전 재료 부분(2260) 및 도전 재료 부분들(2241)로 분리되도록, 형성될 수 있다.
- [0049] 도 23은 도핑된 영역들(2301)이 형성된 후의 메모리 디바이스(500)를 도시한다. 도핑된 영역들(2301)을 형성하는 것은 n-형 불순물들을 도전 재료 부분들(2241)의 최상부 부분들에 삽입(예컨대, 주입)하는 것을 포함할 수 있다. 도핑된 영역들(2301)은 채널들(1841) 및 메모리 디바이스(500)의 다른 구성요소들 사이에 비교적 낮은 저항 연결을 제공할 수 있다.
- [0050] 도 24는 유전체들(2401) 및 채널들(2402)이 형성된 후의 메모리 디바이스(500)를 도시한다. 유전체들(2401)(예컨대, 실리콘 산화물)은 홀들(2201)의 위치에 도전 재료 부분(2260)의 측면들 상에 형성된다. 채널들(2402)은 유전 재료(2101)의 측면들 상에 및 유전체들(2401) 상에 형성된다.
- [0051] 도 25는 도전 재료(2501)가 각각의 홀들(2201)에 형성된 후의 메모리 디바이스(500)를 도시하며, 따라서 채널(2402)은 도전 재료(2501), 도핑된 영역(2301) 및 도전 재료 부분(2241)을 통해 채널(1841)에 전기적으로 결합될 수 있다. 각각의 홀들(2201)에 도전 재료(2501)를 형성하는 것은 재료 위에 도전 재료(예컨대, 폴리실리콘)를 증착시키는 것을 포함할 수 있으며, 따라서 도전 재료는 홀들(2201)을 채운다. 그 후, 도전 재료의 최상부 부분은 예를 들면, 도전 재료를 에칭 백(etching back)함으로써 또는 화학적 기계적 평탄화(CMP: chemical mechanical planarization)에 의해 제거될 수 있다.
- [0052] 도 26은 도핑된 영역들(2601) 및 선택 라인들(2661, 2662, 및 2663)이 형성된 후의 메모리 디바이스(500)를 도시한다. 도핑된 영역들(2601)을 형성하는 것은 n-형 불순물들을 도전 재료(2501)의 최상부 부분들로 삽입(예컨대, 주입)하는 것을 포함할 수 있다. 선택 라인들(2661, 2662, 및 2663)을 형성하는 것은 트렌치들(2602)을 형성하기 위해 유전 재료(2101)의 부분들 및 도전 재료 부분(2260)을 제거하는 것을 포함할 수 있으며, 이것은 재료(1007)로 부분적으로 연장하는 트렌치 바텀들을 가진다. 도 26에 도시된 바와 같이, 트렌치들(2602)은 도전 재료 부분(2260)을 선택 라인들(2661, 2662, 및 2663)로 분리하며, 이것은 도 2의 선택 라인들(261, 262, 및 263)에 대응할 수 있다.
- [0053] 도 27은 재료(2701) 및 공통 소스(2770)가 형성된 후의 메모리 디바이스(500)를 도시한다. 재료(2701)를 형성하는 것은 재료(2101) 위에 유전 재료(예컨대, 실리콘 이산화물(silicon dioxide))를 증착시키는 것을 포함할 수 있으며, 따라서 유전 재료는 트렌치들(2602)을 채운다. 그 후, 유전 재료의 최상부 부분은 예를 들면, 유전 재료를 에칭 백함으로써 또는 CMP에 의해 제거될 수 있다. 공통 소스(2770)를 형성하는 것은 재료들(2701, 2101) 위에 도전 재료(예컨대, 금속)를 증착시키는 것을 포함할 수 있다.
- [0054] 도 28은 영역(702)(도 10)에서의 재료들(1001 내지 1007)이 도 28에 도시되지 않은 계단들 사이에 재료를 가진 계단형 패턴을 형성하기 위해 처리(예컨대, 패턴링(patterning)에 의해)된 후의 메모리 디바이스(500)를 도시한다. 도 10의 설명에서 언급된 바와 같이, 재료들(1001 내지 1007)의 몇몇 부분들은 명료함을 위해 도 10 내지 도 27의 영역(702)으로부터 생략된다. 도 28은 그것들이 계단형 패턴을 형성하기 위해 처리된 후 영역(702)에서의 재료(1001 내지 1007)를 도시한다. 도 28에 도시된 바와 같이, 게이트 게이트들(1221, 1222, 및 1223)은 각각 재료들(1002, 1004, 및 1006)로 형성되며, 이것은 계단형 패턴에 형성된다.
- [0055] 도 29는 접촉부들(2929, 2949, 및 2959)이 형성된 후의 메모리 디바이스(500)를 도시한다. 접촉부들(2929)은 게이트 게이트들(1221, 1222, 및 1223)로 전기적 연결들을 제공한다. 접촉부들(2949)은 선택 라인들(841, 842, 843, 및 844)로 전기적 연결들을 제공한다. 접촉부들(2959)은 데이터 라인들(651, 652, 및 653)로 및 그로부터

의 전기적 연결들을 제공한다.

[0058] 도 29에 도시된 바와 같이, 메모리 디바이스(500)는 도 2 및 도 3을 참조하여 설명된 메모리 디바이스(300)의 구성요소들 및 메모리 셀들(210, 211, 및 212)과 유사하거나 또는 동일한 구성요소들 및 메모리 셀들(2910, 2911, 및 2912)을 포함할 수 있다.

[0057] 이 기술분야의 숙련자는 부가적인 프로세스들이 위에서 설명된 메모리 디바이스(500)와 같은, 메모리 디바이스의 부가적인 피쳐(feature)들을 형성하기 위해 수행될 수 있다는 것을 용이하게 인식할 것이다. 따라서, 본 출원에 설명된 실시예들에 초점을 맞추도록 돕기 위해, 위에서 설명된 도 5 내지 도 29 및 이하에 설명되는 도 30 내지 도 38은 단지 메모리 디바이스(500)와 같은, 메모리 디바이스의 피쳐들의 일부만을 도시한다.

[0058] 도 30은 본 발명의 일 실시예에 따른, 메모리 셀들(210, 211, 및 212) 위에 위치된 데이터 라인들(251, 252, 및 253)을 가진 메모리 디바이스(300)의 일부의 개략도를 도시한다. 메모리 디바이스(300)는 도 3의 메모리 디바이스(200)의 구성요소들과 유사한 구성요소들을 포함할 수 있다. 따라서, 단순함을 위해, 메모리 디바이스(200)와 메모리 디바이스(3000) 사이의 유사하거나 또는 동일한 구성요소들은 동일한 번호 지정들을 제공받는다. 이들 유사한 구성요소들에 대한 상세한 설명은 도 30에 반복되지 않는다. 메모리 디바이스(3000)와 메모리 디바이스(200) 사이의 주요 차이점은 전역적 소거 동작을 가능하게 하기 위해 메모리 디바이스(3000)의 공통 소스(3070) 및 데이터 라인들(251, 252, 및 253)의 위치들을 포함한다. 도 30에 도시된 바와 같이, 데이터 라인들(251, 252, 및 253)은 메모리 셀들(210, 211, 및 212) 위에 위치된다. 공통 소스(3070)는 메모리 셀들(210, 211, 및 212) 아래에 위치되며, 메모리 디바이스(3000)의 기판(예컨대, 도 31에서의 기판(3101))의 적어도 일부에 직접 결합할 수 있다. 이러한 주요 차이는 전압들이 소거 동작 동안 상이한 방식으로 메모리 디바이스(3000)의 다양한 구성요소들에 인가되도록 허용할 수 있으며, 메모리 디바이스(3000)는 메모리 디바이스(200)의 소거 동작(예컨대, 국소적 소거 동작)과 비교하여 상이하게 기능한다(예컨대, 전역적 소거 동작 동안). 예를 들면, 메모리 디바이스(3000)의 소거 동작에서, 대략 20 볼트들의 전압이 공통 소스(3070)에 인가될 수 있는 한편, 게이트 라인들(221, 221, 및 223), 데이터 라인들(251, 252, 및 253), 선택 라인들(241, 242, 및 243), 및 선택 라인들(261, 262, 및 26)은 "플로팅(floating)"될 수 있다. 이러한 소거 동작에서, 메모리 셀들(210, 211, 및 212)의 메모리 소자들로부터의 전자들은 공통 소스(3070)로(예컨대, 전역적 소거) 이동할 수 있다(예컨대, 터널링(tunneling)에 의해). 도 2, 도 3, 및 도 4를 참조하여 위에서 설명된 바와 같이, 메모리(200)에서, 소거 동작 동안, 메모리 셀들(210, 211, 및 212)의 메모리 소자들로부터의 전자들은 데이터 라인들(251, 253, 및 253)(예컨대, 국소적 소거)로 이동할 수 있다.

[0059] 도 31은 본 발명의 일 실시예에 따른, 도 30의 메모리 디바이스(3000)의 일부의 3D 뷰를 도시한다. 도 31에 도시된 바와 같이, 데이터 라인들(251, 252, 및 253)은 메모리 셀들(210, 211, 및 212) 위에 위치되고, 공통 소스(3070)는 메모리 셀들(210, 211, 및 212) 아래에 위치되며 기판(3101)에 결합된다. 기판(3101)은 p-형 실리콘과 같은, 반도체 재료를 포함할 수 있다.

[0060] 도 31에 도시된 바와 같이, 각각의 스트링에서의 메모리 셀들(210, 211, 및 212)(예컨대, 트랜지스터들(231, 232) 사이의 메모리 셀들)은 기판(3101)에 대하여 Z-방향으로 실질적으로 수직 정렬된다. 트랜지스터(232)는 이중-게이트(도 3) 또는 도 3의 트랜지스터(231)의 둘러싸인 게이트(도 9)와 유사한 이중-게이트 또는 둘러싸인 게이트를 포함할 수 있다. 또한, 도 31은 Z-방향으로 수직으로 및 도 30의 트랜지스터들(231, 232)에 대응하는 트랜지스터들(231, 232) 사이의 동일한 스트링에서 메모리 셀들(210, 211, 및 212)의 메모리 소자(430)를 지나 연장하는 도전 재료 부분(442) 및 채널(441)을 도시한다.

[0061] 각각의 메모리 셀들(210, 211, 및 212)에서의 메모리 소자(430)는 링 형상을 가진다. 도 31에 도시된 바와 같이, 동일한 스트링에서의 메모리 셀들(210, 211, 및 212) 내에서, 각각의 메모리 셀의 링-형상 메모리 소자(430) 전체는 동일한 스트링에서의 다른 각각의 메모리 셀들의 링-형상 메모리 소자 전체와 실질적으로 수직 정렬된다(Z-방향에서).

[0062] 도 32 내지 도 38은 본 발명의 일 실시예에 따른, 메모리 셀들 위에 위치된 데이터 라인들을 가진 메모리 디바이스(3200)를 형성하는 다양한 프로세스들을 도시한다. 메모리 디바이스(3200)(도 38에 보다 상세히 도시된)는 도 31의 메모리 디바이스(3000)에 대응할 수 있다.

[0063] 도 32는 기판(3201) 및 트렌치들(3211, 3212, 및 3213)을 가진 메모리 디바이스(3200), 및 기판(3201)의 최상부 부분 상에 형성된 기판 부분들(3270, 3271)을 도시한다. 기판(3201)은 벌크 실리콘과 같은 반도체 재료를 포함할 수 있다. 최상부 기판 부분들(3270, 3271)은 p-형 불순물들을 기판(3201)의 최상부 부분에 삽입(예컨대,

주입)함으로써 형성될 수 있다. 따라서, 기판 부분들(3270, 3271)은 p-형 실리콘을 포함할 수 있다. 트렌치들(3211, 3212, 및 3213) 및 기판 부분(3270)을 형성하는 것은 기판 부분(3271)의 일부를 제거(예컨대, 에칭)하는 것을 포함할 수 있다. 메모리 디바이스(3200)의 기록 또는 판독 동작 동안, 기판 부분(3270)은 접지와 같은, 전위에 결합될 수 있다. 메모리 디바이스(3200)의 소거 동작 동안, 기판 부분(3270)은 전압, 예를 들면, 대략 20 볼트들에 결합될 수 있다.

[0064] 도 33은 재료(3301)가 트렌치들(3211, 3212, 및 3213)(도 32)에 형성된 후의 메모리 디바이스(3200)를 도시한다. 재료(3301)를 형성하는 것은 트렌치들(3211, 3212, 및 3213)을 채우기 위해 기판(3201) 위에 유전 재료(예컨대, 실리콘 산화물)를 증착시키는 것을 포함할 수 있다. 그 후, 유전 재료의 최상부 부분은 예를 들면, CMP에 의해 제거될 수 있다.

[0065] 도 34는 재료(3401) 및 트렌치들(3411, 3412, 및 3413), 및 디바이스 구조들(3460)이 형성된 후의 메모리 디바이스(3200)를 도시한다. 재료(3401)를 형성하는 것은 기판(3201) 및 재료(3301) 위에 유전 재료(예컨대, 실리콘 산화물 또는 실리콘 질화물)를 증착시키는 것을 포함할 수 있다. 트렌치들(3411, 3412, 및 3413)을 형성하는 것은 기판(3201), 재료(3301), 및 재료(3401)의 부분들을 제거(예컨대, 에칭)하는 것을 포함할 수 있다. 디바이스 구조들(3460)은 트렌치들(3411, 3412, 및 3413)의 형성의 결과로서 형성된다.

[0066] 도 35는 도핑된 영역들(3501), 재료(3502), 및 선택 라인들(3561, 3562, 및 3563)의 형성 후의 메모리 디바이스(3200)를 도시한다. 도핑된 영역들(3501)을 형성하는 것은 기판 부분(3271)의 선택적 부분들에 n-형 불순물들을 삽입(예컨대, 주입)하는 것을 포함할 수 있다. 재료(3502)(예컨대, 실리콘 산화물)는 디바이스 구조들(3460)로부터 선택 라인들(3561, 3562, 및 3563)을 전기적으로 분리하기 위해 각각의 디바이스 구조(3460)의 양쪽 측면들 모두 상에 형성될 수 있다. 선택 라인들(3561, 3562, 및 3563)의 재료들은 하나 이상의 금속들, 합금(alloy)들, 다른 도전 재료들, 또는 그것들의 조합과 같은, 하나 이상의 도전 재료들을 포함할 수 있다. 선택 라인들(3561, 3562, 및 3563)은 도 30의 메모리 디바이스(3000)의 선택 라인들(261, 262, 및 263)에 대응할 수 있다.

[0067] 도 36은 재료(3601)가 트렌치들(3411, 3412, 및 3413)에 형성된 후의 메모리 디바이스(3200)를 도시한다. 재료(3601)를 형성하는 것은 트렌치들(3411, 3412, 및 3413)을 채우기 위해 유전 재료(예컨대, 실리콘 이산화물)를 증착시키는 것을 포함할 수 있다. 그 후, 유전 재료의 최상부 부분은 예를 들면, 도전 재료를 에칭백함으로써, 또는 CMP에 의해, 기판 부분(3270)에서 정지시킴으로써 제거될 수 있다.

[0068] 도 37은 홈(groove)들(3701)이 선택 라인들(3561, 3562, 및 3563)을 형성하기 위해 사용된 재료의 최상부 부분을 제거함으로써(예컨대, 웨트 에칭에 의해) 형성된 후의 메모리 디바이스(3200)를 도시한다. 대안적으로, 홈들(3701)을 형성하는 것은 생략될 수 있다.

[0069] 도 38은 다른 구성요소들이 형성된 후의 메모리 디바이스(3200)를 도시한다. 도 38에서 메모리 디바이스(3200)의 구성요소들을 형성하는 프로세스들은 도 10 내지 도 29를 참조하여 위에서 설명된 메모리 디바이스(500)의 구성요소를 형성하는 유사하거나 또는 동일한 프로세스들을 포함할 수 있다. 예를 들면, 도 38의 제어 게이트들(3821, 3822, 및 3823)은 도 5 내지 도 29를 참조하여 위에서 설명된 메모리 디바이스(500)의 제어 게이트들(1221, 1222, 및 1223)을 형성하는 프로세스들과 유사하거나 또는 동일한 프로세스들을 사용하여 형성될 수 있다. 도 38의 데이터 라인들(3851, 3852, 및 3853)은 도 30 및 도 31의 데이터 라인들(251, 252, 및 253)에 대응할 수 있다. 도 38에 도시된 바와 같이, 메모리 디바이스(3200)는 메모리 셀들(3810, 3811, 및 3812)을 포함할 수 있으며, 이것은 도 5 내지 도 29를 참조하여 위에서 설명된 메모리 디바이스(500)의 메모리 셀들(2910, 2911, 및 2912)을 형성하는 프로세스들과 유사하거나 또는 동일한 프로세스들을 사용하여 형성될 수 있다.

[0070] 본 출원에 설명된 하나 이상의 실시예들은 메모리 디바이스 및 메모리 디바이스를 형성하는 방법들을 포함한다. 하나의 이러한 메모리 디바이스는 제 1 그룹의 메모리 셀들을 포함할 수 있으며, 제 1 그룹의 각각의 셀은 메모리 디바이스의 하나의 디바이스 레벨에 위치한 제 1 제어 게이트의 각각의 공동(cavity)에 형성된다. 또한, 메모리 디바이스는 제 2 그룹의 메모리 셀들을 포함할 수 있으며, 제 2 그룹의 각각의 셀은 메모리 디바이스의 또 다른 디바이스 레벨에 위치한 제 2 제어 게이트의 공동에 형성된다. 부가적인 장치 및 방법들이 설명된다. 부가적인 장치 및 방법들을 포함한 다른 실시예들이 도 1 내지 도 38을 참조하여 위에서 설명된다.

[0071] 메모리 디바이스들(100, 200, 500, 3000, 및 3200), 및 메모리 셀들(210, 211, 212, 2910, 2911, 2912, 3010, 3811, 및 3812)와 같은, 장치의 예시들은 본 출원에 설명된 구조들을 이용할 수 있는 장치의 모든 특징들 및 요소들에 대한 완전한 설명이 아닌, 다양한 실시예들의 구조에 대한 일반적인 이해를 제공하도록 의도된다.

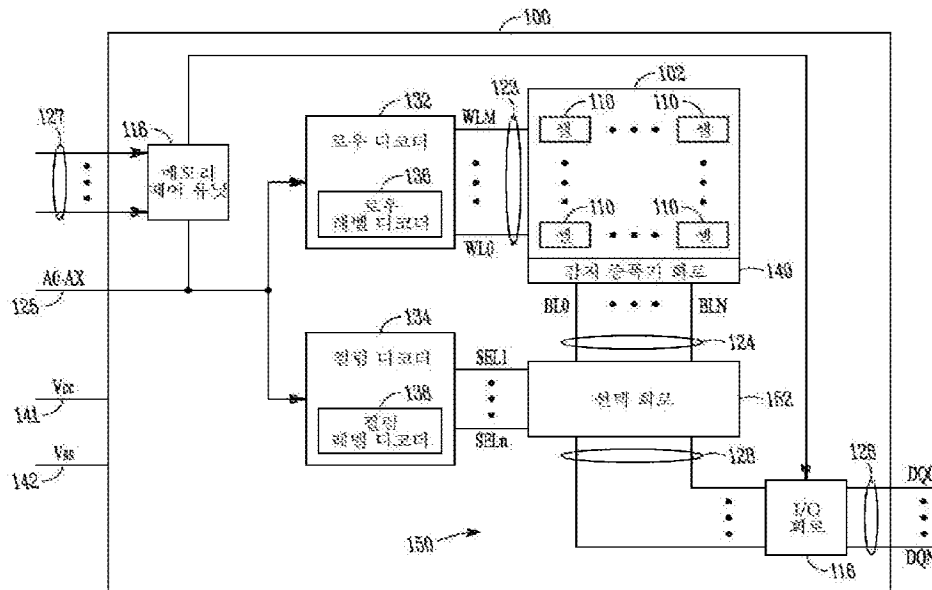
[0072] 다양한 실시예들의 장치는 고속 컴퓨터들, 통신 및 신호 처리 회로, 메모리 모듈(memory module)들, 휴대용 메모리 저장 디바이스들(예컨대, 썸 드라이브(thumb drive)들), 단일 또는 다중-프로세서 모듈들, 단일 또는 다수의 임베디드 프로세서(embedded processor)들, 다중-코어 프로세서(multi-core processor)들, 데이터 스위치(data switch)들, 및 다층(multilayer)을 포함한 애플리케이션-특정 모듈(application-specific module)들, 다중-칩 모듈(multi-chip module)들에 사용되는 전자 회로를 포함하거나 또는 그것에 포함될 수 있다. 또한, 이러한 장치는 텔레비전(television)들, 셀룰러 전화기(cellular telephone)들, 개인용 컴퓨터들(예컨대, 랩탑 컴퓨터(laptop computer)들, 데스크탑 컴퓨터(desktop computer)들, 핸드헬드 컴퓨터(handheld computer)들, 태블릿 컴퓨터(tablet computer)들 등), 워크스테이션(workstation)들, 라디오(radio)들, 비디오 플레이어(video player)들, 오디오 플레이어(audio player)들(예컨대, MP3(동영상 전문가 그룹, 오디오 계층 3(Motion Picture Experts Group, Audio Layer 3)) 플레이어들), 차량들, 의료 디바이스들(예컨대, 심장 모니터, 혈압 모니터 등), 셋 탑 박스(set top box)들 등과 같은, 다양한 전자 시스템들 내에서의 서브-구성요소들로서 포함될 수 있다.

[0073] 상기 설명 및 도면들은 이 기술분야의 숙련자들이 본 발명의 실시예들을 실시할 수 있게 하기 위해 본 발명의 몇몇 실시예들을 도시한다. 다른 실시예들은 구조적, 논리적, 전기적, 프로세스 및 다른 변화들을 통합할 수 있다. 예들은 단지 가능한 변화들을 대표한다. 몇몇 실시예들의 부분들 및 특징들은 다른 것들의 부분들 및 특징들에 포함되거나 또는 그것들로 대체될 수 있다. 상기 설명을 연구 및 이해할 때, 많은 다른 실시예들은 이 기술분야의 숙련자들에게 명백할 것이다.

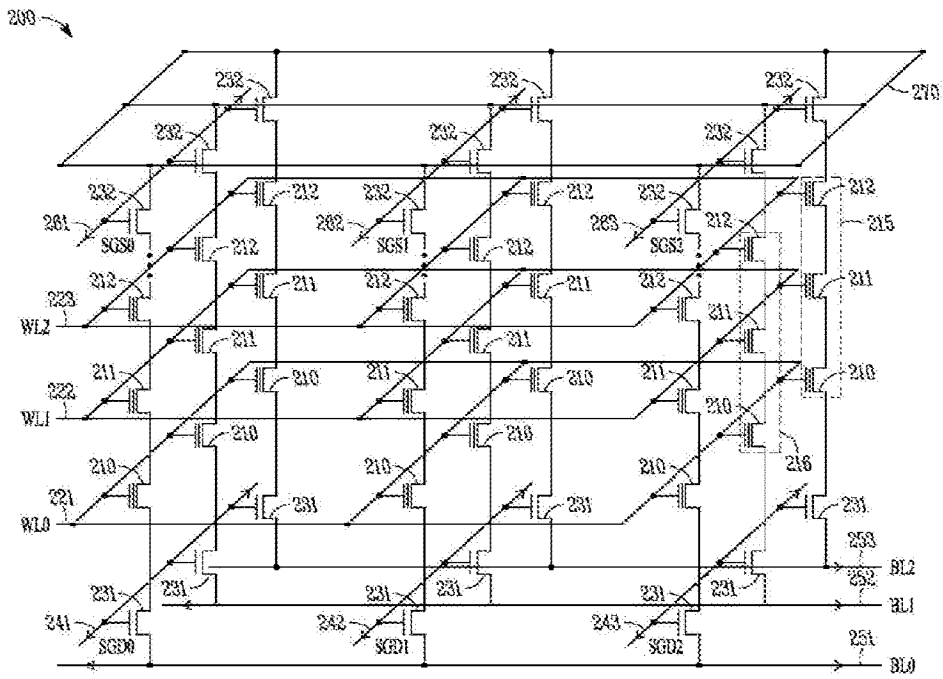
[0074] 요약은 독자가 기술적 발명의 특성 및 요지를 빠르게 알아내도록 허용하는 요약을 요구하는 37 C.F.R. § 1.72(b)를 따르기 위해 제공된다. 본 발명의 요약은 그것이 청구항들의 범위 또는 의미를 해석하거나 또는 제한하기 위해 사용되지 않을 것이라는 이해를 갖고 제시된다.

도면

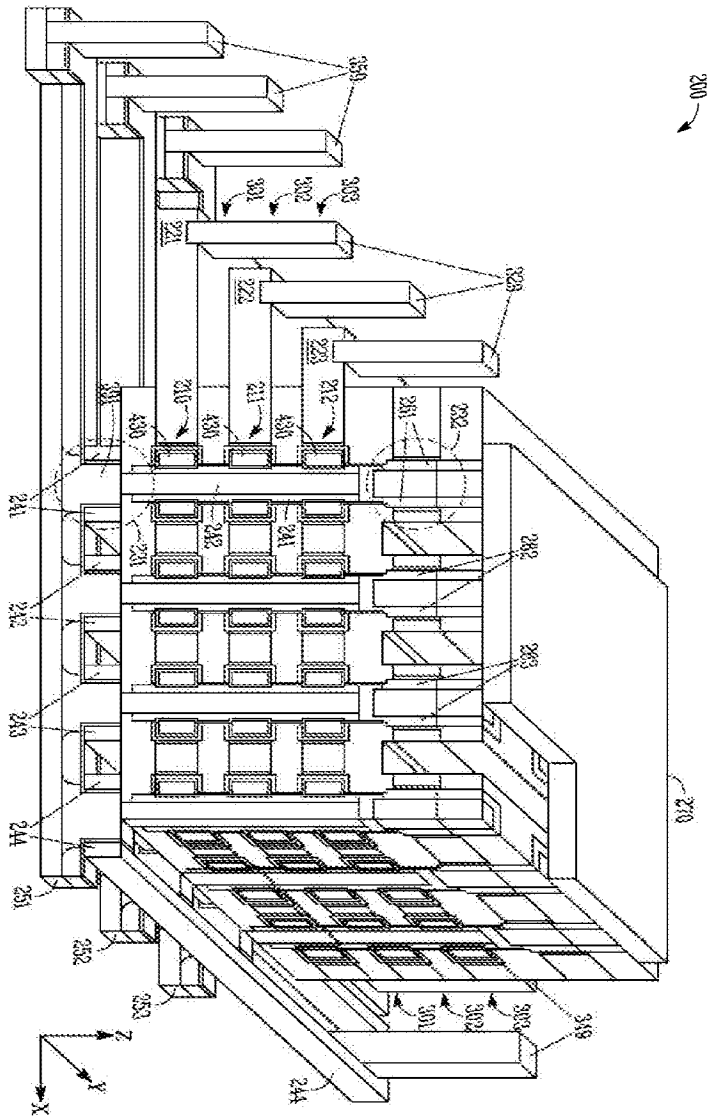
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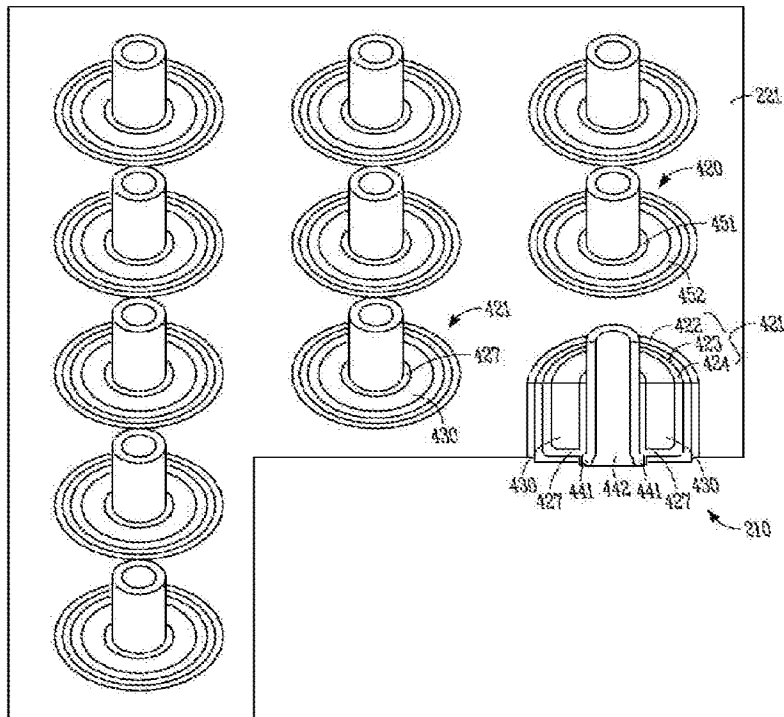
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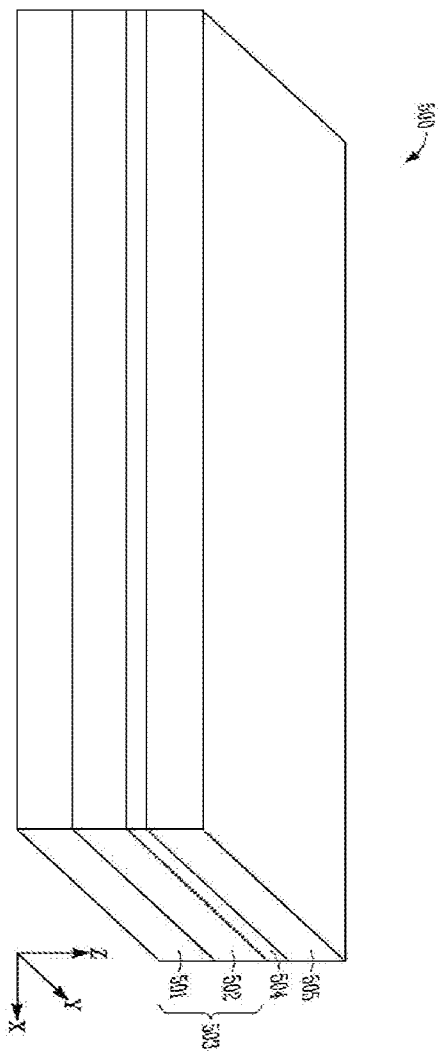
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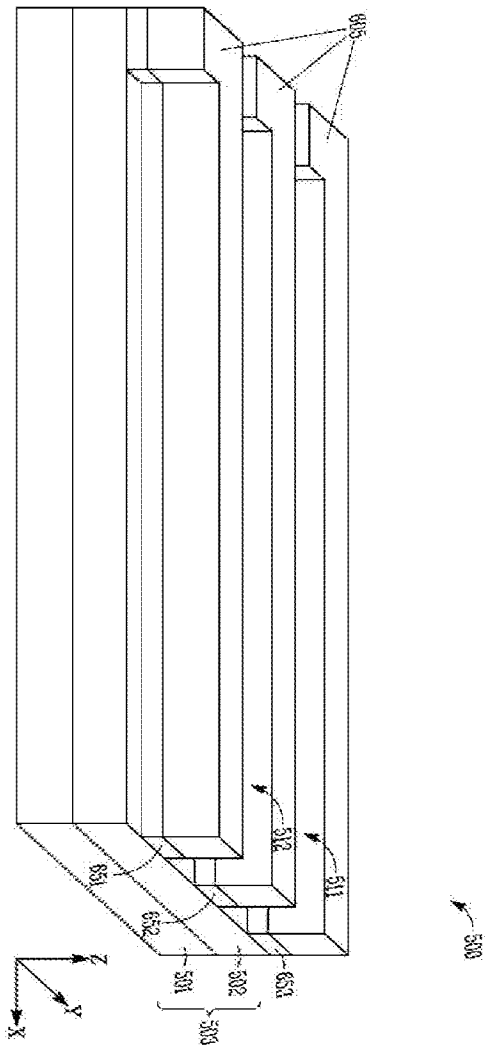
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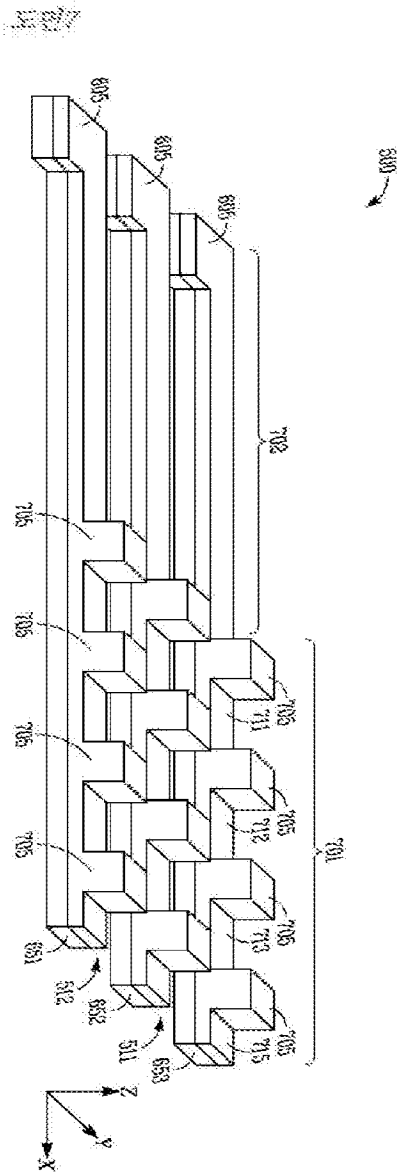


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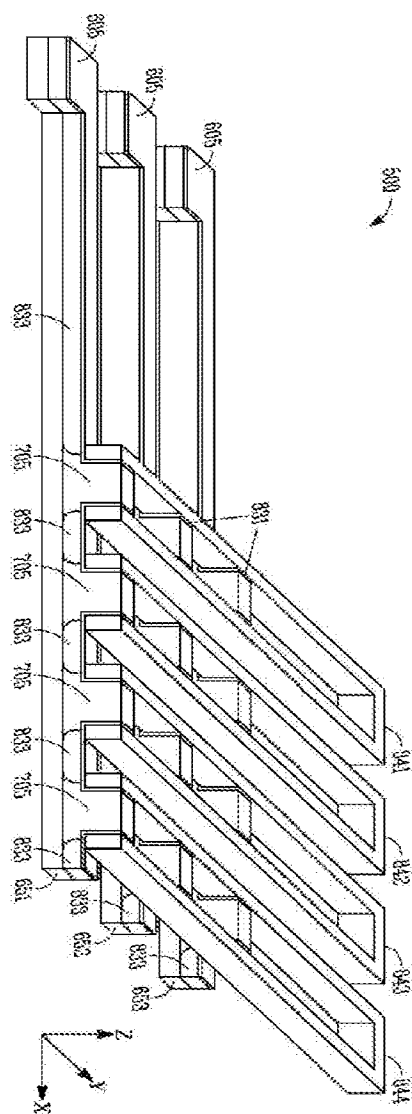


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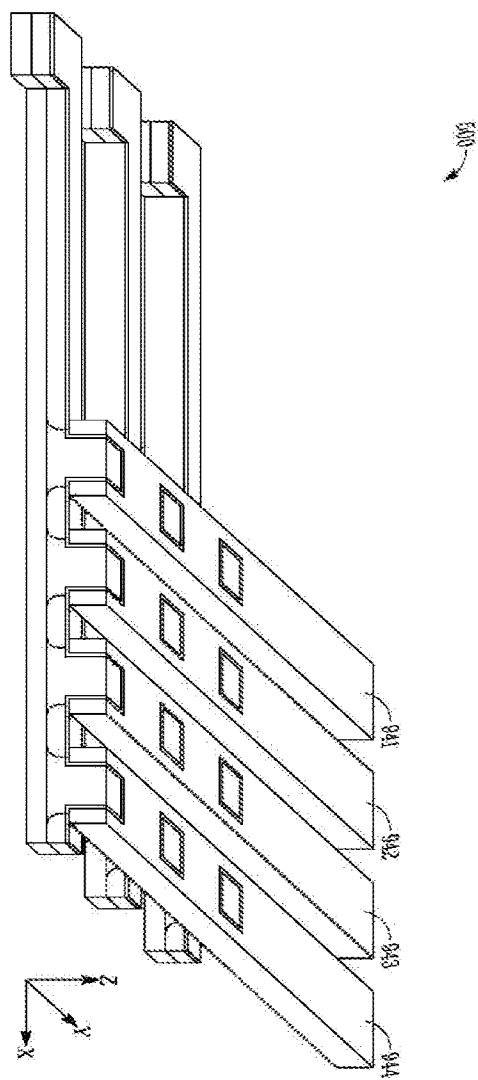




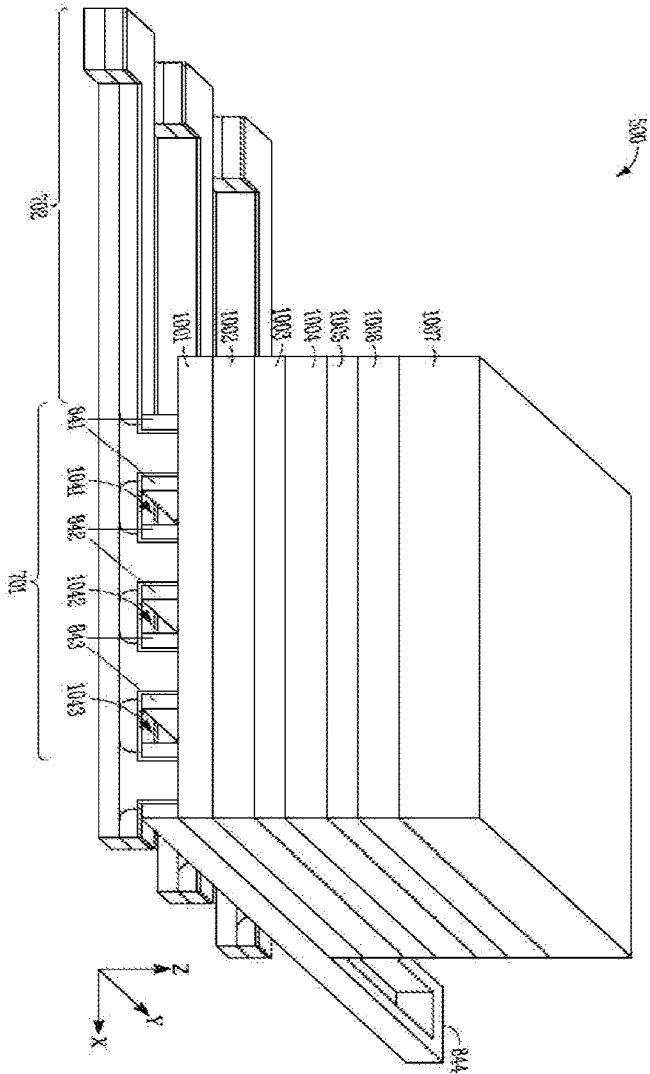
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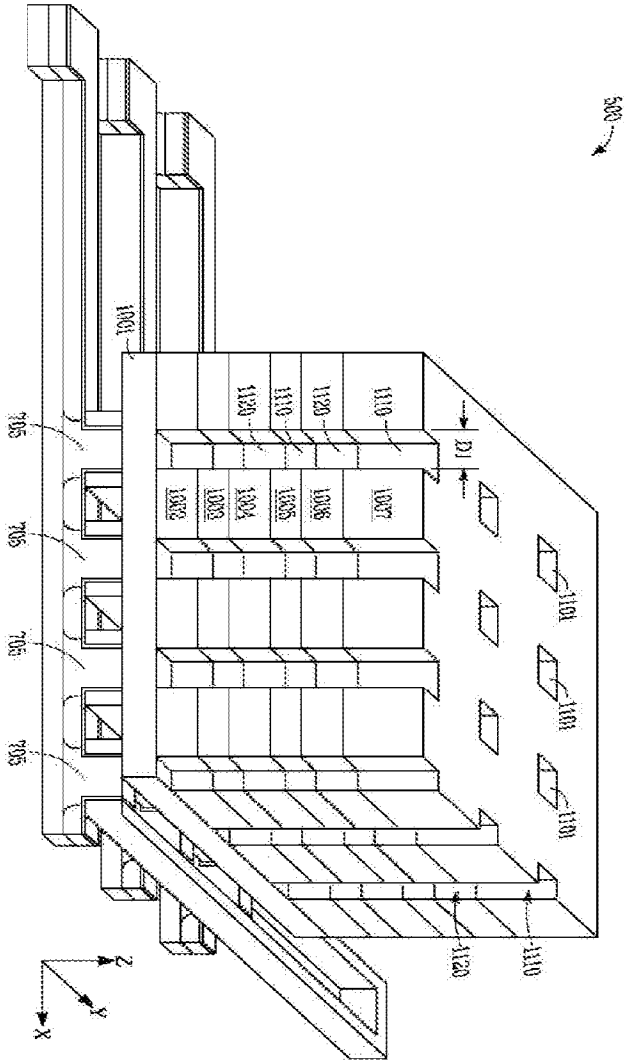
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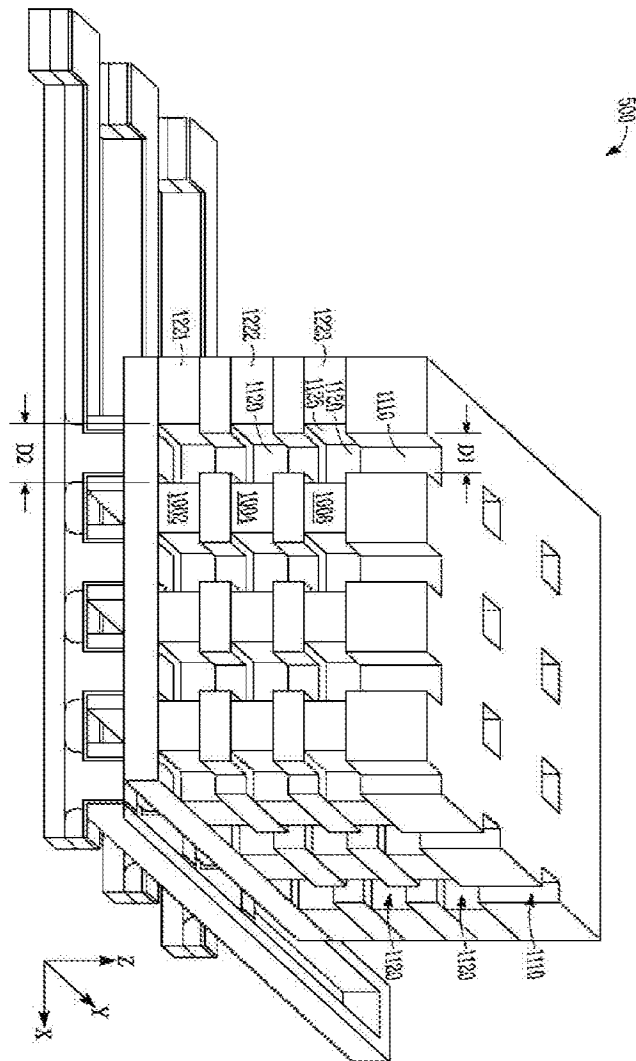
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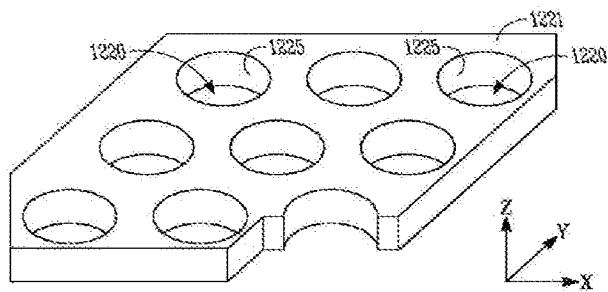
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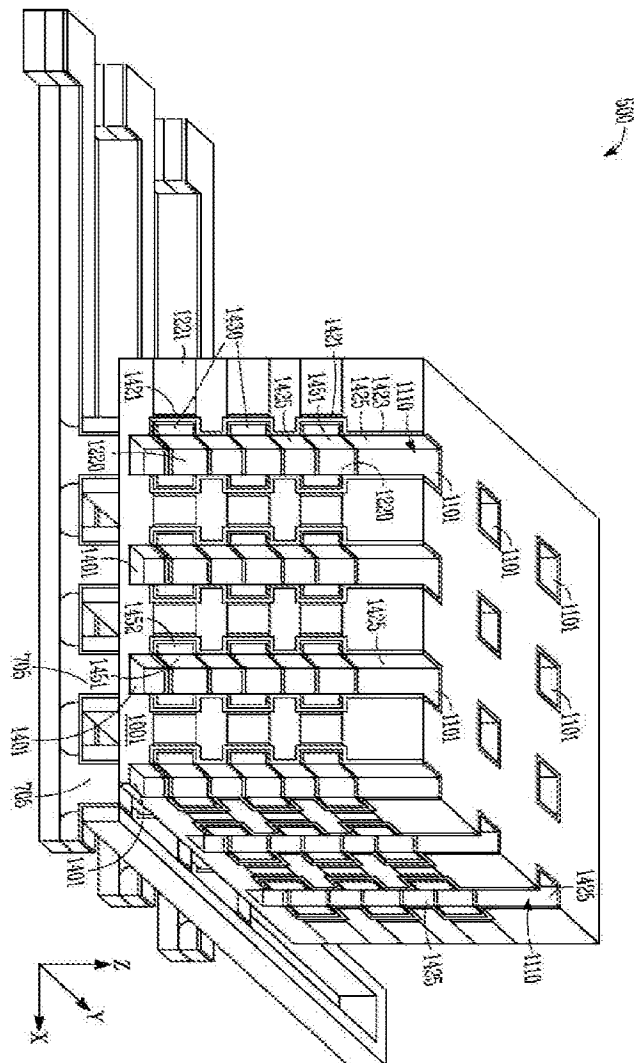
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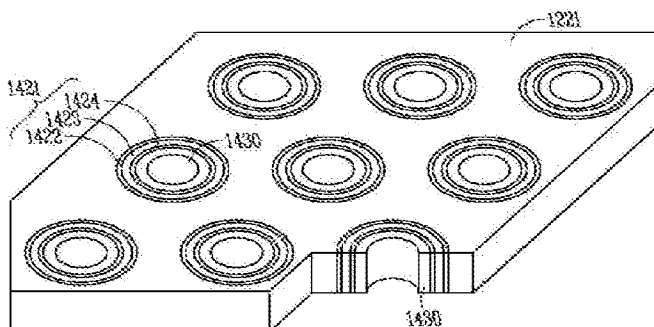
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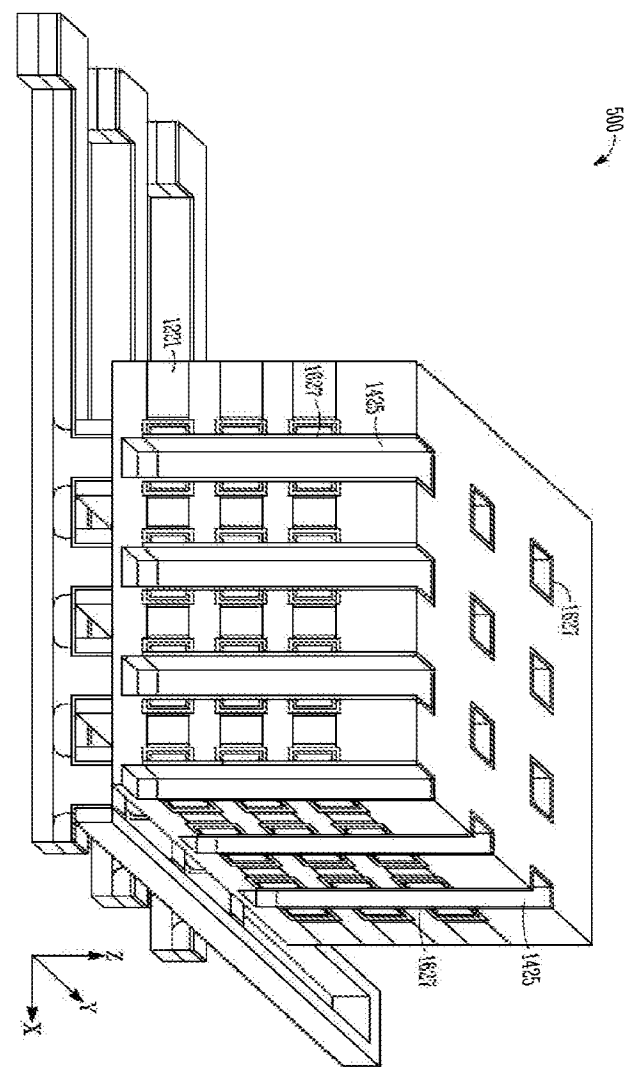
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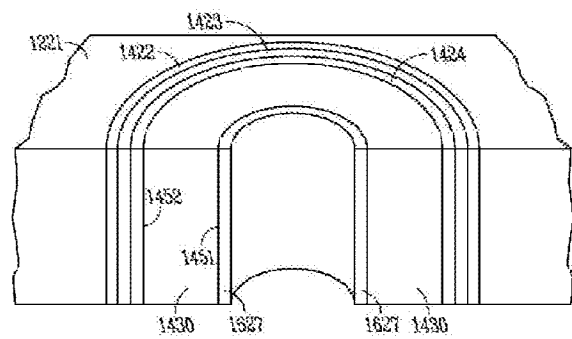
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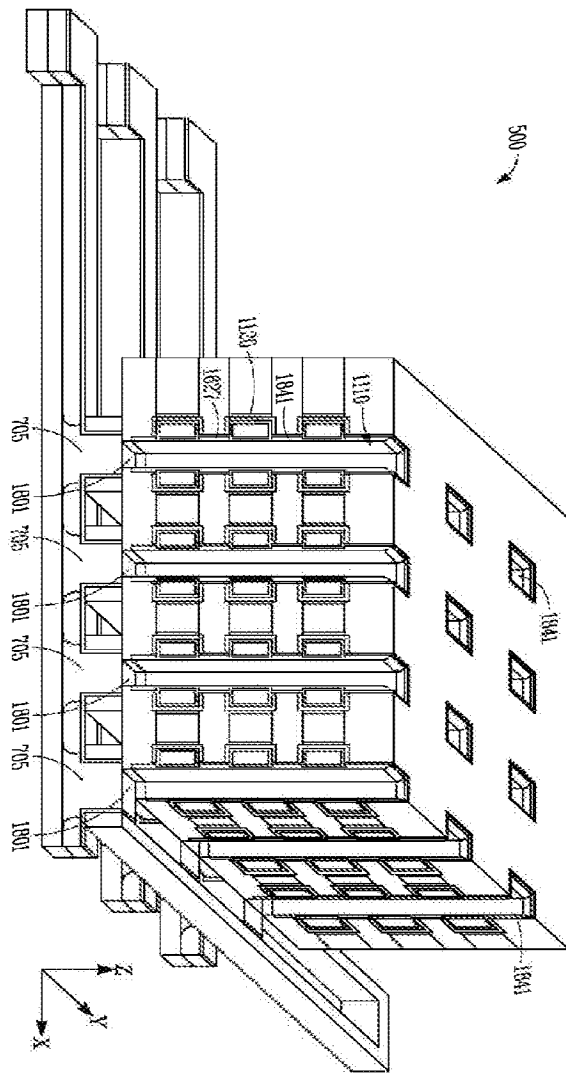
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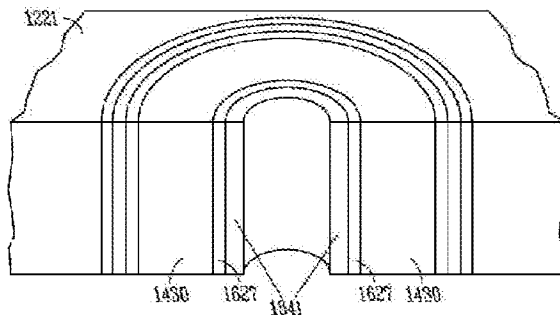
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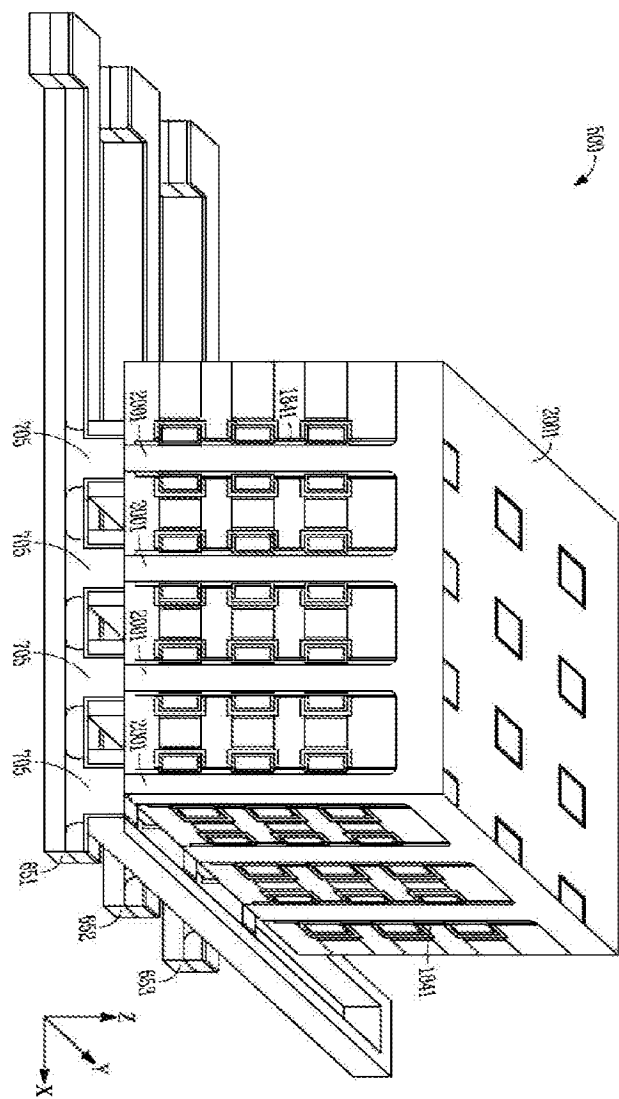
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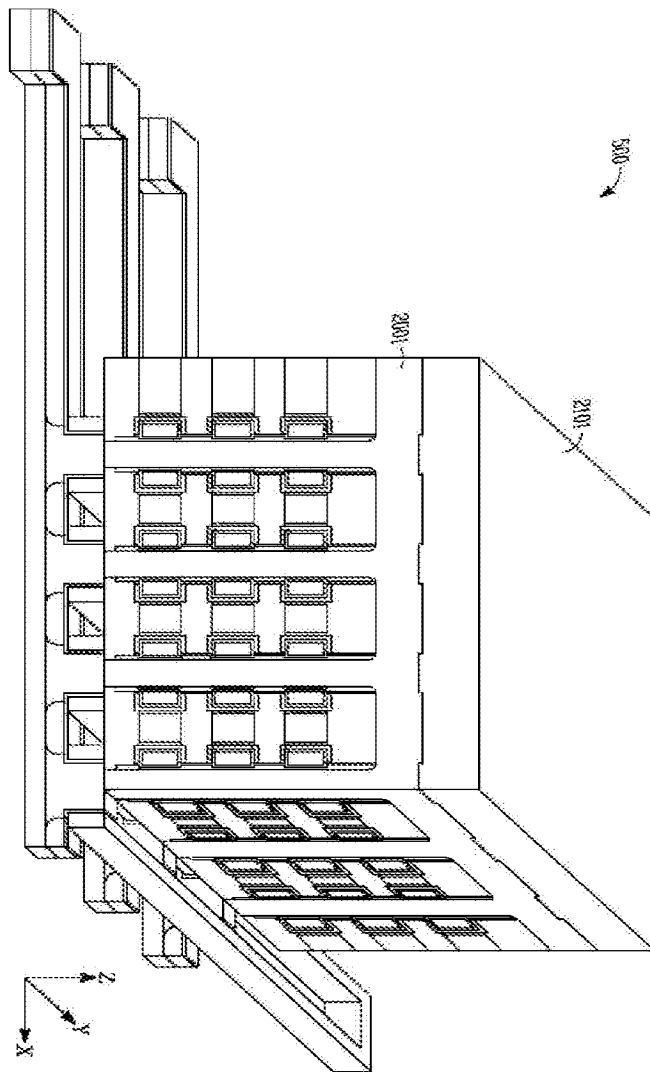
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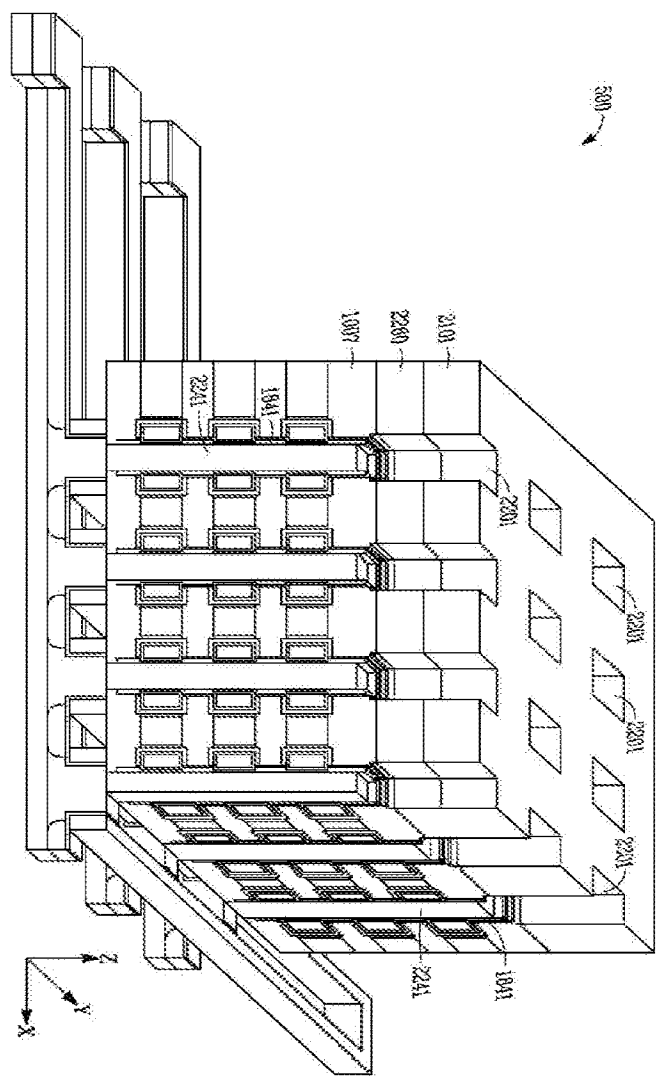
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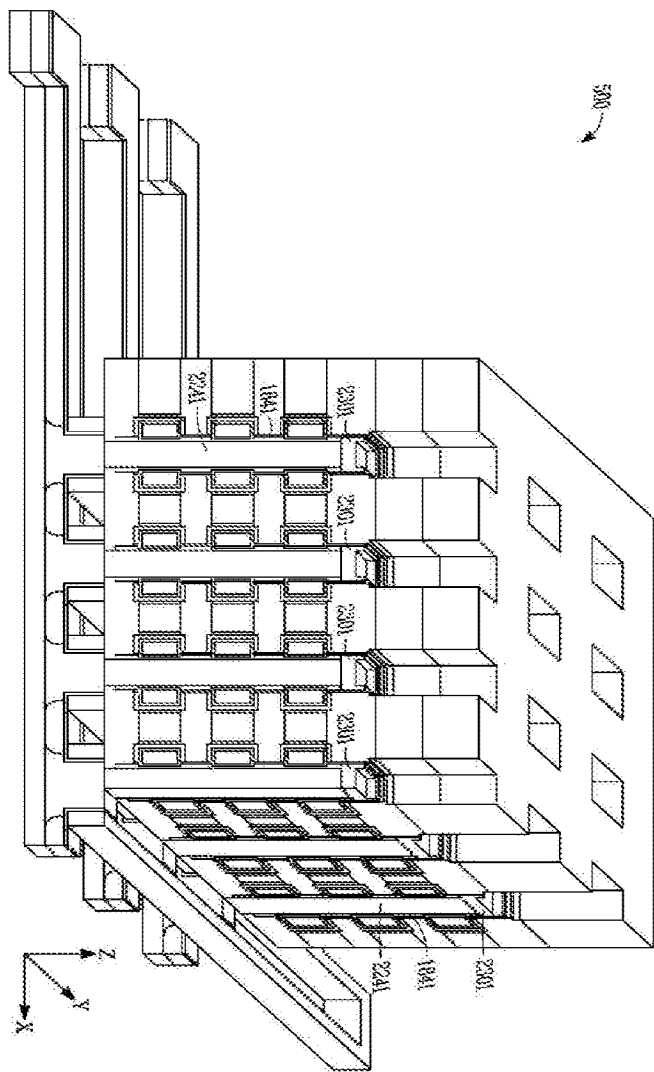
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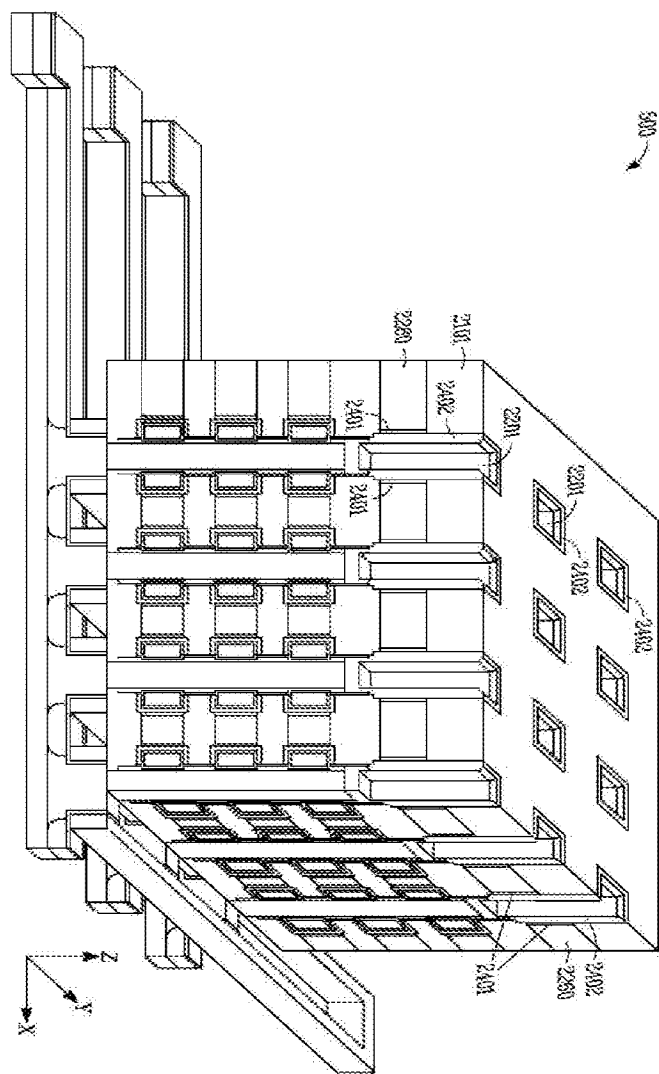
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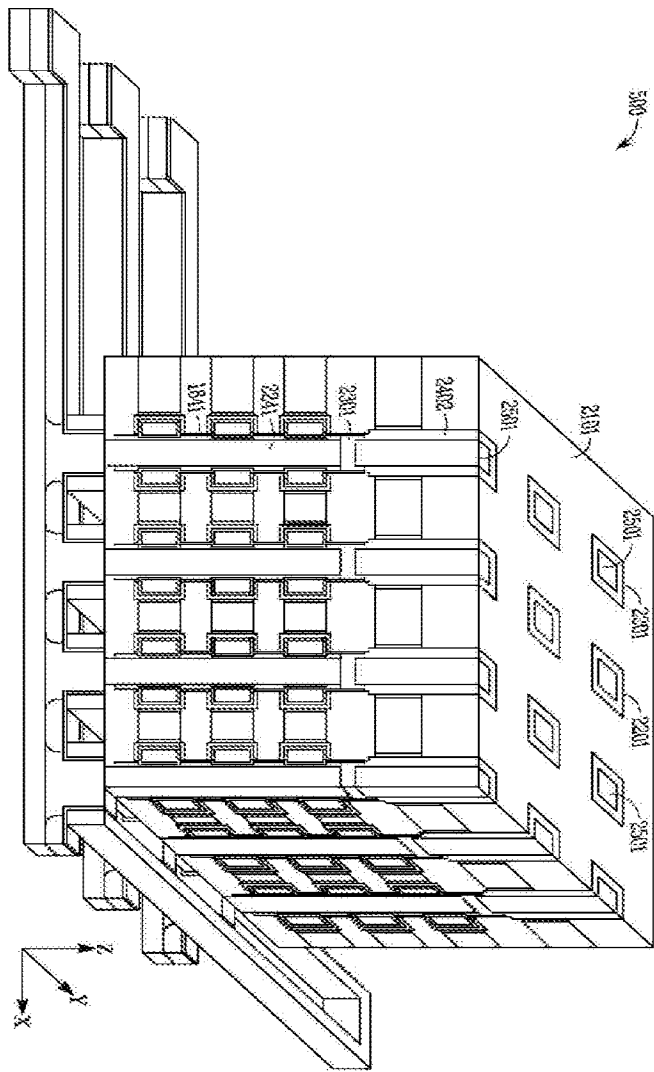
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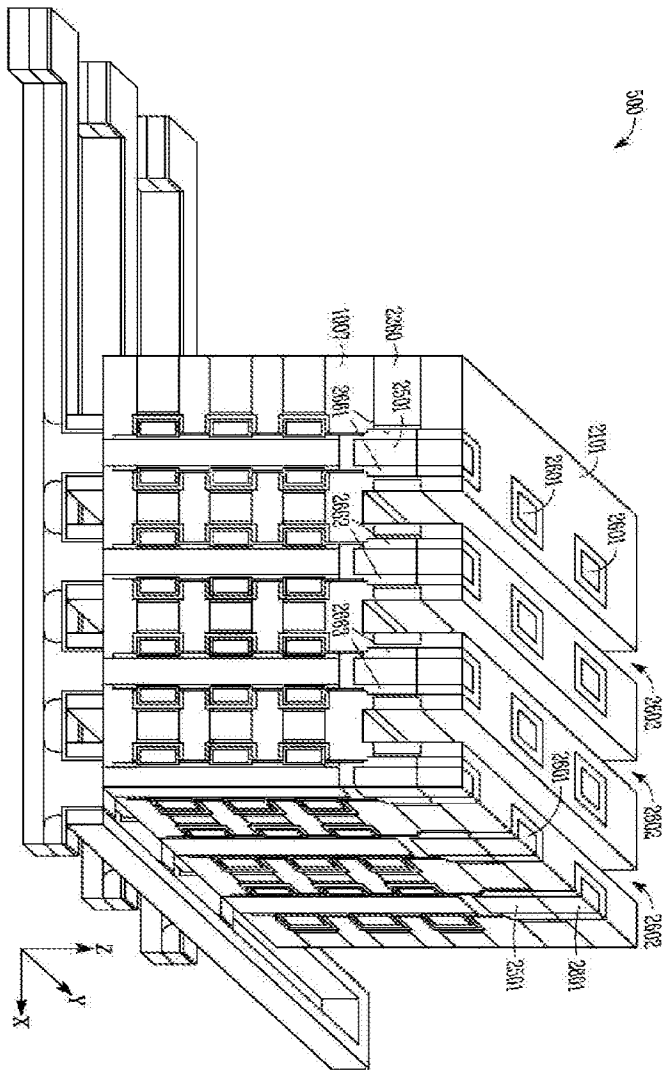
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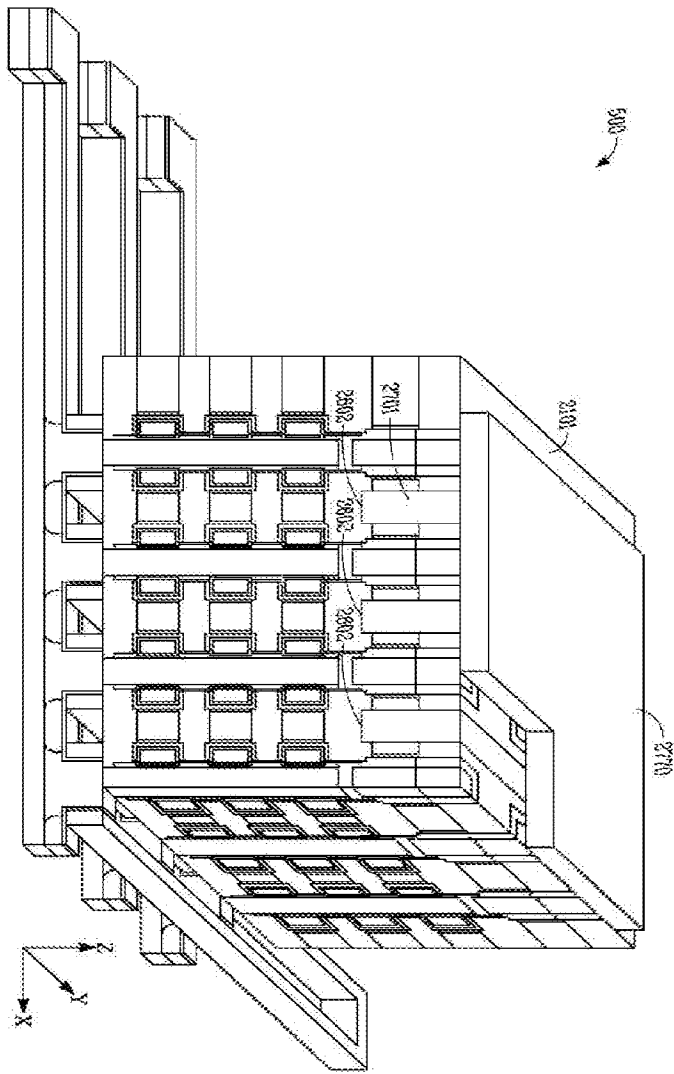
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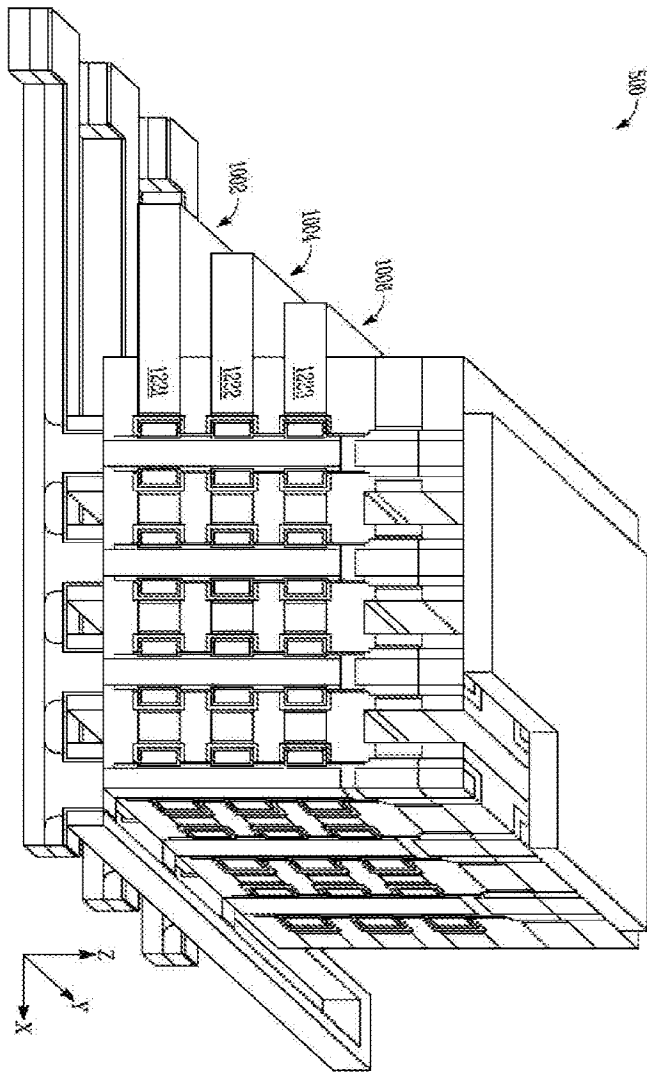
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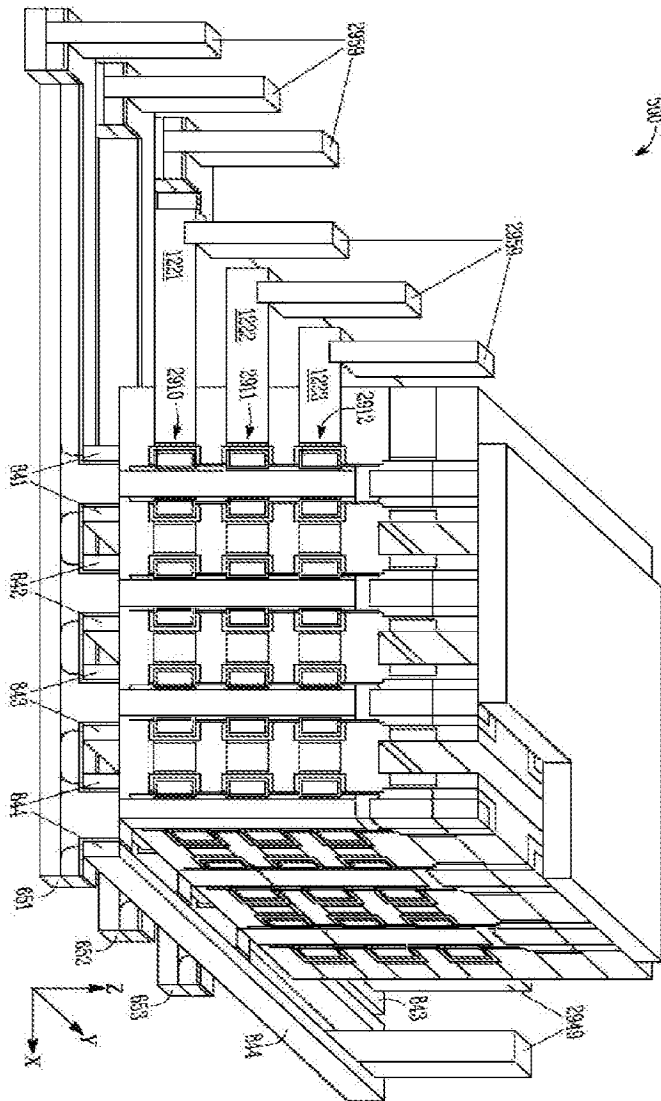
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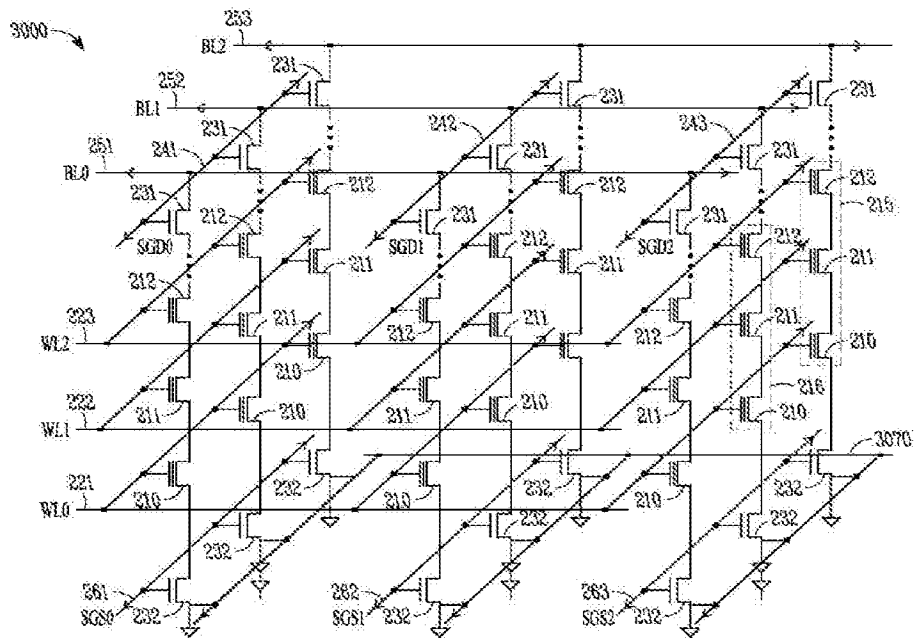
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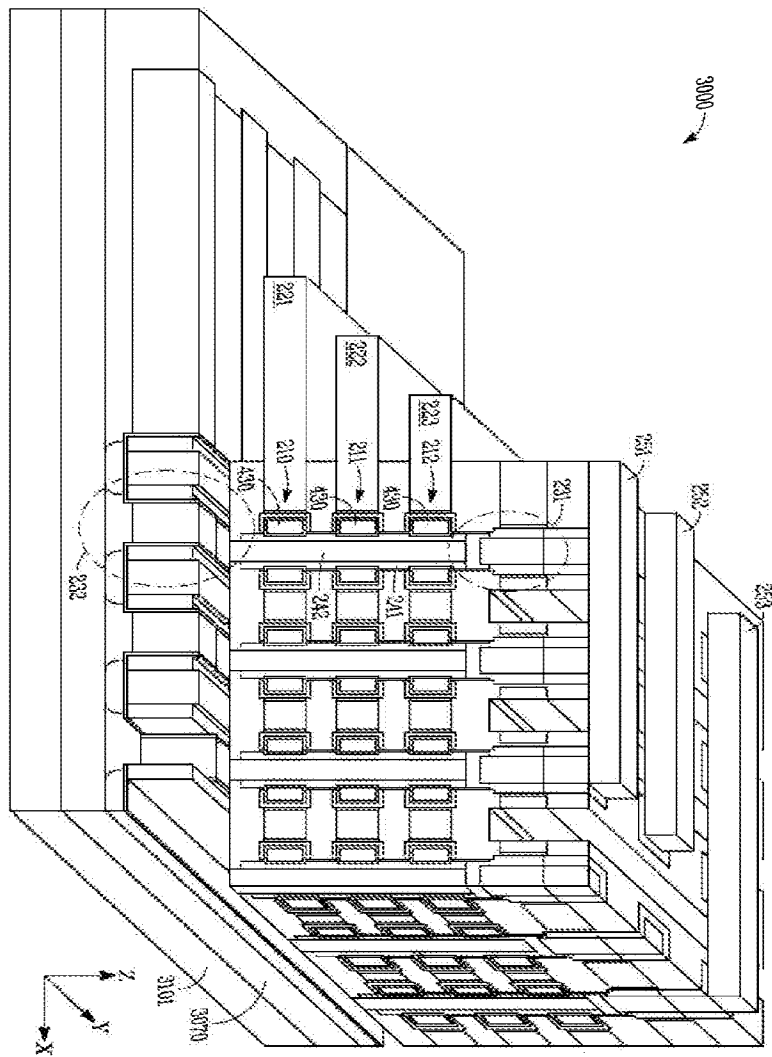
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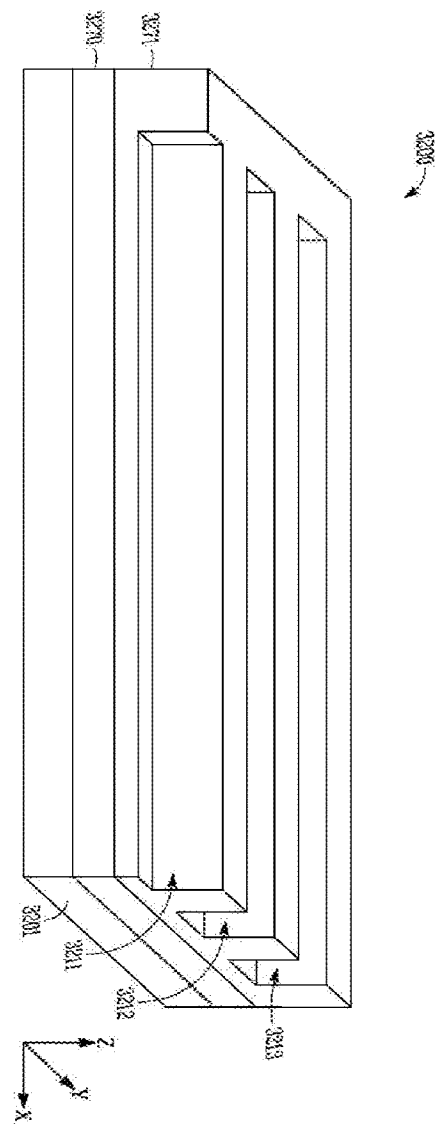
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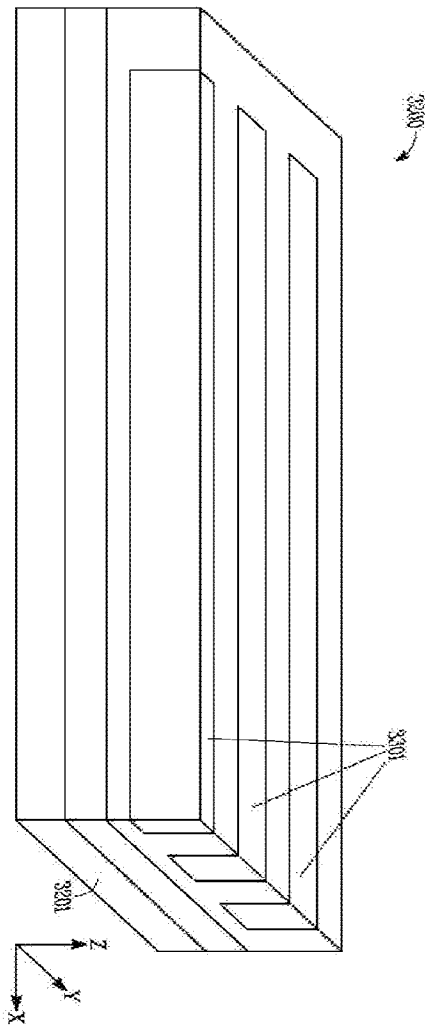
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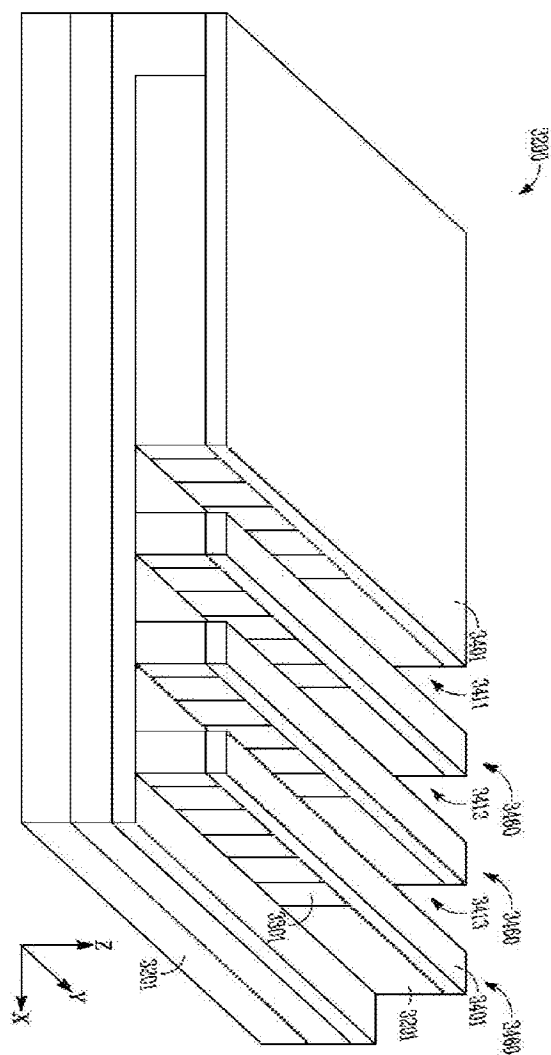
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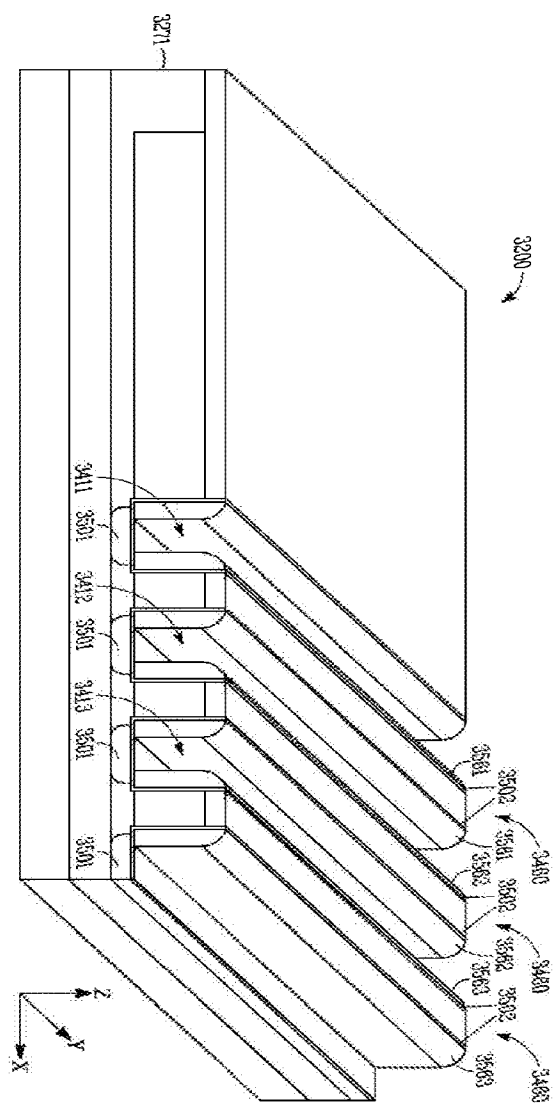
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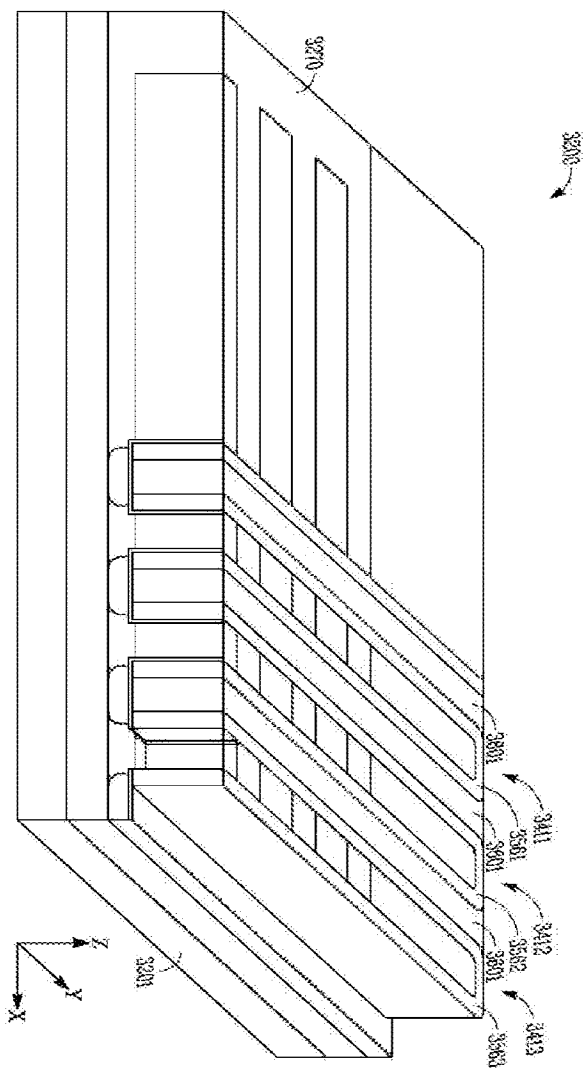
도 8/34



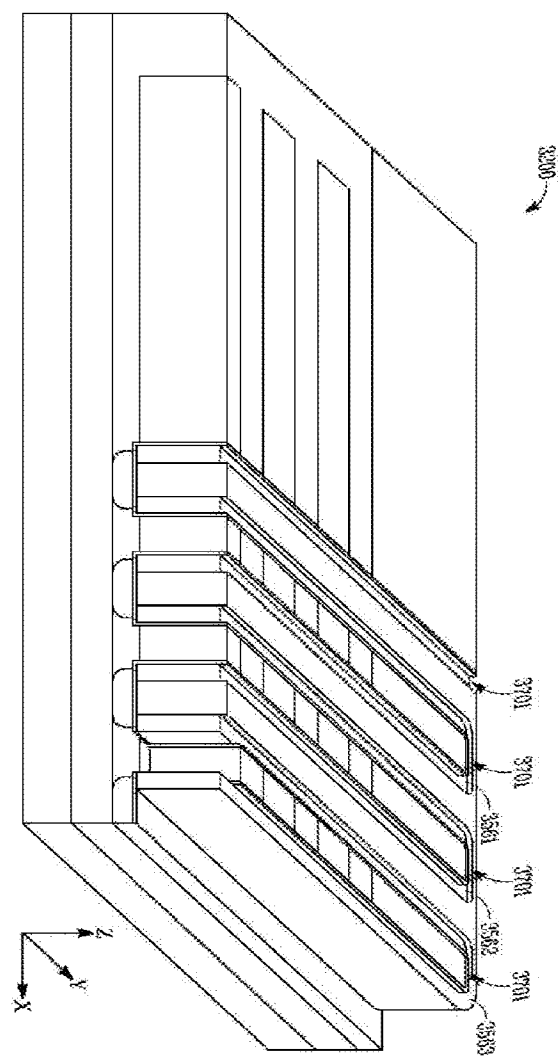
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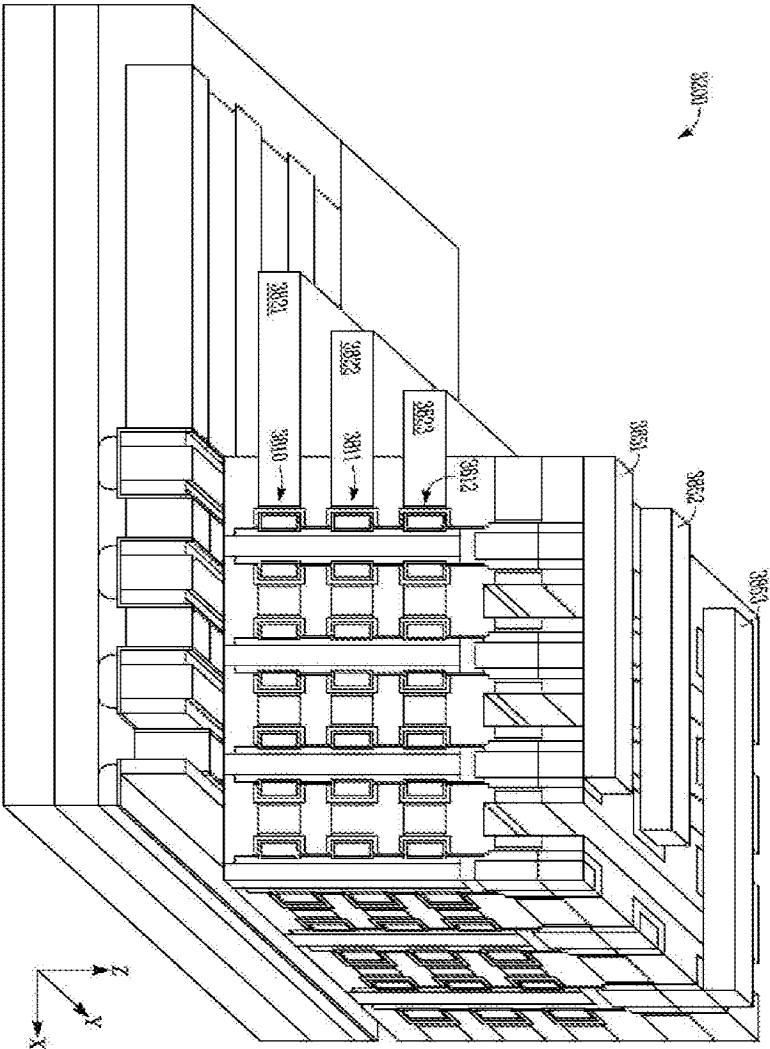
도면 36



도면37



도면36



(12) SG PATENT APPLICATION

(13) A

(43) Publication Date: 27 September 2019

(21) Application No : 10201907425T

(71) Applicant(s): MICRON TECHNOLOGY, INC.

(22) Date of filing : 24/06/2011

(72) Inventor(s): TANG, SANH, D. ; ZAHURAK, JOHN, K.

(30) Priority Data:

(74) Agent(s): DREW & NAPIER LLC

12/825,211

28/06/2010

US

(54) Title: **THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME**

(57) Abstract:

Some embodiments include a memory device and methods of forming the memory device. One such memory device includes a first group of memory cells, each of the memory cells of the first group being formed in a cavity of a first control gate located in one device level of the memory device. The memory device also includes a second group of memory cells, each of the memory cells of the second group being formed in a cavity of a second control gate located in another device level of the memory device. Additional apparatus and methods are described.

FIG. 3

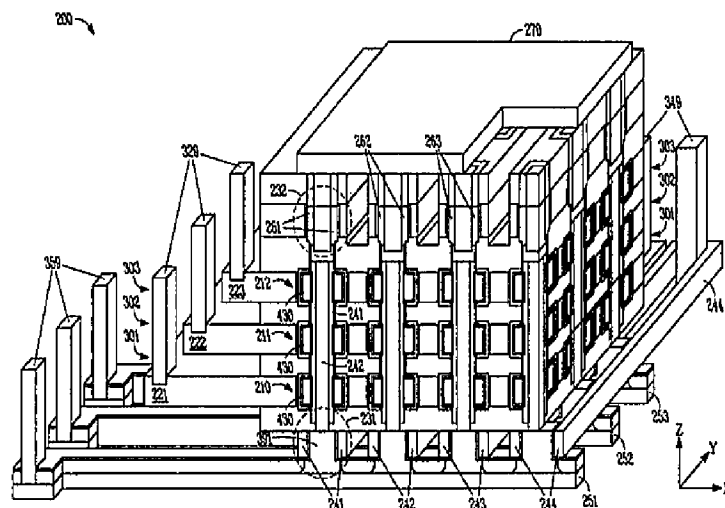


FIG. 3

Electronic Acknowledgement Receipt

EFS ID:	38593148
Application Number:	16716177
International Application Number:	
Confirmation Number:	3036
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Ognyan I. Beremski/Marcie Svitoris
Filer Authorized By:	Ognyan I. Beremski
Attorney Docket Number:	303.B12US6
Receipt Date:	14-FEB-2020
Filing Date:	16-DEC-2019
Time Stamp:	14:16:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		16716177_SIDS_2-14-20.pdf	163291	yes	4
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	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Miscellaneous Incoming Letter		1	1	
	Transmittal Letter		2	3	
	Information Disclosure Statement (IDS) Form (SB08)		4	4	
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2	Foreign Reference	0001_1_for_kr102005475b1_f.pdf	13286542	no	55
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Information:					
Total Files Size (in bytes):			15615039		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.: 303.B12US6
Filed: December 16, 2019
Examiner: Unknown
Customer No.: 73115

Serial No.: 16/716,177
Due Date: N/A
Group Art Unit: 2827
Confirmation No.: 3036

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

☒ Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.) Copies of Cited References (5).

If not provided for in a separate paper filed herewith, please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743. If applicable, any papers or fees supplied herewith are considered to be timely filed pursuant to 37 C.F.R. § 1.7(a), the response period falling on a Federal Holiday, Saturday or Sunday being extended to the next succeeding business day.

SCHWEGMAN LUNDBERG & WOESSNER, P.A.
Customer No.: 73115

By: */ Viet Tong /*
Viet V. Tong
Reg. No. 45,416

S/N 16/716,177

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sanh D. Tang et al.

Examiner: Unknown

Serial No.: 16/716,177

Group Art Unit: 2827

Filed: December 16, 2019

Docket: 303.B12US6

Customer No.: 73115

Confirmation No.: 3036

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE
SAME

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached PTO 1449 Form be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the PTO 1449 Form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. § 1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed after filing of the application or after the filing of the most recent RCE, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Applicant brings to the attention of the Examiner the following Office Actions and responses associated with one or more of the inventors of the instant application and/or the assignee of the instant application. This material is available and accessible at the United States Patent and Trademark Office.

CHARGE STORAGE APPARATUS AND METHODS

Application Serial No. 15/691,442, Response filed 6-17-19 to Non-Final Office Action mailed 2-15-19, 11 pgs

Application Serial No. 15/691,442, Final Office Action mailed 08-15-19, 4 pgs

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Serial Number: 16/716,177

Filing Date: December 16, 2019

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Page 2

Dkt: 303.B12US6

Application Serial No. 15/691,442, Response filed 10-15-19 to Final Office Action mailed 8-15-19, 5 pgs

Application Serial No. 15/691,442, Notice of Allowance mailed 10-29-19, 5 pgs

Application Serial No. 15/691,442, Corrected Notice of Allowability mailed 12-31-19, 2 pgs

Pursuant to 37 C.F.R. § 1.98(a)(2), copies of cited U.S. Patents and Published Applications, and Non-Published Applications identifiable by USPTO Serial Number, are no longer required to be provided to the Office. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R § 1.98(a)(2).

The Examiner is invited to contact the undersigned at the telephone number indicated if there are any questions regarding this communication.

Respectfully submitted,

SCHWEGMAN LUNDBERG & WOESSNER, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 373-6969

Date 2-14-20 By / Viet Tong /

VVT:mls1

Viet V. Tong

Reg. No. 45,416



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/716,177	12/16/2019	Sanh D. Tang	303.B12US6	3036
73115	7590	03/19/2020	EXAMINER	
SCHWEGMAN LUNDBERG & WOESSNER/MICRON			JEAN BAPTISTE, WILNER	
P.O. BOX 2938				
MINNEAPOLIS, MN 55402				
			ART UNIT	PAPER NUMBER
			2899	
			NOTIFICATION DATE	DELIVERY MODE
			03/19/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

SLW@blackhillsip.com
uspto@slwip.com

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

CROSS-REFERENCE TO RELATED APPLICATIONS

2. This application is a continuation of U.S. Application Serial No. 16/125,242, filed September 7, 2018, which is a continuation of U.S. Application Serial No. 15/722,580, filed October 2, 2017, now issued as U.S. Patent No. 10,090,324, which is a continuation of U.S. Application Serial No. 15/188,273, filed June 21, 2016, now issued as U.S. Patent No. 9,780,115, which is a continuation of U.S. Application Serial No. 14/041,928, filed September 30, 2013, now issued as U.S. Patent No. 9,379,005, which is a divisional of U.S. Application Serial No. 12/825,211, filed June 28, 2010, now issued as U.S. Patent No. 8,803,214, all of which are incorporated herein by reference in their entireties.

Double Patenting

3. The non-statutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper time wise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A non-statutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patent-ably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-8 is/are rejected on the ground of non-statutory obviousness-type double patenting as being un-patentable over claims 1-8 of U.S. Patent No. 9,780,115 (here and after '115). Although the conflicting claims are not identical, they are not patent-ably distinct from each other because the following rationale.

Although the conflicting claims are not identical, the scope of the claimed limitations of the instant application as claimed in claim 1 is similar to that of the claimed limitations of U.S. Patent No. 9,780,115 (here and after '115), as claimed in claim 1. The only difference is that in the parent case, it was "wherein a material of the memory element of the memory cell of the first memory cells is discontinuous from a material of the memory element of the memory cell of the second memory cells", while the present application does not claim. Therefore, the claims are not patent-ably distinct from each other.

5. The following table shows the corresponding conflicting claims between the instant application and U.S. Patent No. 9,780,115 (here and after '115).

Application # 16/716177	U.S. Patent No. 9,780,115

1. An apparatus comprising: first memory cells located in a first device level of a memory device; second memory cells located in a second device level of the memory device; a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate; and a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate.	1. An apparatus comprising: first memory cells located in a first device level of a memory device; second memory cells located in a second device level of the memory device; a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein the first memory cells includes a memory cell having a memory element formed in a cavity of the first control gate; and a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein the second memory cells includes a memory cell having a memory element formed in a cavity of the second control gate; and a conductive channel extending between the memory cell of the first memory cell and the memory cell of the second memory cells, wherein a material of the memory element of the memory cell of the first memory cells is discontinuous from a material of the memory element of the memory cell of the second memory cells.
2. The apparatus of claim 1, wherein each of the first and second memory cells include multiple	2. The apparatus of claim 1, wherein the first and second memory cells include multiple memory

memory cells arranged in a first direction and multiple memory cells arranged in a second direction, further comprising: a common source; and data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.	cells arranged in a first direction and multiple memory cells arranged in a second direction, further comprising: a common source; and data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.
3. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.	3. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.
4. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.	4. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

5. The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.	5. The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.
6. The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.	6. The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.
7. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.	7. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.
8. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.	8. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.

6. Claims 9-14 is/are rejected on the ground of non-statutory obviousness-type double patenting as being un-patentable over claims 9-14 of U.S. Patent No. 9,780,115 (here and after '115). Although the

conflicting claims are not identical, they are not patent-ably distinct from each other because the following rationale.

Although the conflicting claims are not identical, the scope of the claimed limitations of the instant application as claimed in claim 9 is similar to that of the claimed limitations of U.S. Patent No. 9,780,115 (here and after '115), as claimed in claim 9. The only difference is that in the parent case, it was "a material of the first memory element is discontinuous from a material of the second memory element", while the present application does not claim. Therefore, the claims are not patent-ably distinct from each other.

7. The following table shows the corresponding conflicting claims between the instant application and U.S. Patent No. 9,780,115 (here and after '115).

Application # 16/716177	U.S. Patent No. 9,780,115
9. An apparatus comprising: a first non-volatile memory cell including a first memory element, the first memory element having a ring shape; a second non-volatile memory cell including a second memory element, the second memory element having a ring shape; and a conductive material extending through the first and second memory elements.	9. An apparatus comprising: a first non-volatile memory cell including a first memory element, the first memory element having a ring shape; a second non-volatile memory cell including a second memory element, the second memory element having a ring shape; and a conductive material extending through the first and second memory elements, wherein a material of the first memory element is discontinuous from a material of the second memory element.
10. The apparatus of claim 9, further comprising: a first additional conductive material configured	10. The apparatus of claim 9, further comprising: a first additional conductive material configured

to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells are located; and a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in a second device level of the memory device.	to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells are located; and a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in a second device level of the memory device.
11. The apparatus of claim 10, wherein each of the memory cells further includes a first dielectric between the respective memory element and the conductive material.	11. The apparatus of claim 10, wherein each of the memory cells further includes a first dielectric between the respective memory element and the conductive material.
12. The apparatus of claim 11, wherein each of the memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.	12. The apparatus of claim 11, wherein each of the memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.
13. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the data	13. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the data

line is located between the substrate and the first memory cell.	line is located between the substrate and the first memory cell.
14. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the first and second memory cells are located between the substrate and the data line.	14. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the first and second memory cells are located between the substrate and the data line.

8. Claims 15-20 is/are rejected on the ground of non-statutory obviousness-type double patenting as being un-patentable over claims 15-20 of U.S. Patent No. 9,780,115 (here and after '115). Although the conflicting claims are not identical, they are not patent-ably distinct from each other because the following rationale.

Although the conflicting claims are not identical, the scope of the claimed limitations of the instant application as claimed in claim 15 is similar to that of the claimed limitations of U.S. Patent No. 9,780,115 (here and after '115), as claimed in claim 15. The only difference is that in the parent case, it was "a material of the first memory element is discontinuous from a material of the second memory element", while the present application does not claim. Therefore, the claims are not patent-ably distinct from each other.

9. The following table shows the corresponding conflicting claims between the instant application and U.S. Patent No. 9,780,115 (here and after '115).

Application # 16/716177	U.S. Patent No. 9,780,115
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15. An apparatus comprising: a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall; a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall; a first dielectric formed on the first sidewall and the second sidewall; a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric; a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric; a second dielectric formed on a side of the first memory element and on a side of the second memory element; and a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from	15. An apparatus comprising: a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall; a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall; a first dielectric formed on the first sidewall; a second dielectric formed on the second sidewall; a first memory element located in the first cavity and electrically isolated from the first conductive material by the first dielectric; a second memory element located in the second cavity and electrically isolated from the second conductive material by the second dielectric; a first additional dielectric formed on a side of the first memory element; a second additional dielectric formed on a side of the second memory element; and a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from
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the first and second memory elements by at least a respective portion of the second dielectric.	the first memory element by the first additional dielectric and from the second memory element by the second additional dielectric, wherein a material of the first memory element is discontinuous from a material of the second memory element.
16. The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.	16. The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.
17. The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.	17. The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.
18. The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.	18. The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.
19. The apparatus of claim 15, further comprising: a substrate; and a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.	19. The apparatus of claim 15, further comprising: a substrate; and a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.
20. The apparatus of claim 15, further comprising: a substrate; and a data line	20. The apparatus of claim 15, further comprising: a substrate; and a data line

configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.	configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.
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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILNER JEAN BAPTISTE whose telephone number is (571)270-7394. The examiner can normally be reached on M-T 8:00-6:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dale Page can be reached on 571-270-7877. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W.J/
Examiner, Art Unit 2899
/DALE E PAGE/
Supervisory Patent Examiner, Art Unit 2899

<i>Notice of References Cited</i>	Application/Control No. 16/716,177		Applicant(s)/Patent Under Reexamination Tang et al.	
	Examiner WILNER JEAN BAPTISTE		Art Unit 2899	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9780115-B2	10-2017	Tang; Sanh D.	G11C16/26	1/1
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 16/716,177	Applicant(s)/Patent Under Reexamination Tang et al.
	Examiner WILNER JEAN BAPTISTE	Art Unit 2899

CPC - Searched*		
Symbol	Date	Examiner
(H01L27/11517-1156 H01L2924/1438 H01L29/42324-42336 H01L29/788-7889)	03/16/2020	wj

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
CPC-CAT-EPO-EAST	03/16/2020	wj
Text search	03/16/2020	wj

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/W.J/ Examiner, Art Unit 2899	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S38	67625	Micron-Technology-Inc.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/28 17:09
S39	777	Tang-Sanh-D.in. Zahurak-John-K.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/28 17:09
S40	65133	(H01L27/11517-1156 H01L2924/1438 H01L29/42324-42336 H01L29/788-7889).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/28 17:12
S41	67654	Micron-Technology-Inc.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/29 15:14
S42	777	Tang-Sanh-D.in. Zahurak-John-K.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/29 15:15
S43	65153	(H01L27/11517-1156 H01L2924/1438 H01L29/42324-42336 H01L29/788-7889).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/29 15:15
S44	431	S43 and ((memory near\$2 elements) with ((conductive contact interconnect) with ((initial or first) near\$2 (cavities or grooves or vias or openings)) same (aligned or adjust or straighten or even or fix) same (second near\$2 (cavities or groove or vias or opening)) same substrate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/29 15:16

S47	4	S42 and ((memory near\$2 elements) with ((conductive contact interconnect) with ((initial or first) near\$2 (cavities or grooves or vias or openings)) same (aligned or adjust or straighten or even or fix) same (second near\$2 (cavities or groove or vias or opening)) same substrate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/29 15:32
S48	90	S41 and ((memory near\$2 elements) with ((conductive contact interconnect) with ((initial or first) near\$2 (cavities or grooves or vias or openings)) same (aligned or adjust or straighten or even or fix) same (second near\$2 (cavities or groove or vias or opening)) same substrate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/29 15:33

3/16/2020 10:09:43 AM
C:\Users\wjeanbaptiste\Documents\EAST\Workspaces\16-716177 (Three Dimensional Memory).wsp

S/N 16/716,177**PATENT****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor(s):	Sanh D. Tang et al.	Examiner:	Unknown
Serial No.:	16/716,177	Group Art Unit:	Unknown
Filed:	December 16, 2019	Docket:	303.B12US6
Customer No.:	73115	Confirmation No.:	3036
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

COMMUNICATION CONCERNING PRIOR OR COPENDING APPLICATION(S)

Mail Stop Amendment
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Pursuant to the guidance of MPEP §§ 2001.06(b) and 2004(9), Applicant would like to bring the following additional application(s) to the Examiner's attention. The identification of these applications is not intended to suggest that the subject matter claimed in any listed application is, or has been, substantially similar to any claim or claims in the present application.

<u>Serial No./ Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
12/825,211 8,803,214	June 28, 2010	303.B12US1	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
14/041,928 9,379,005	September 30, 2013	303.B12US2	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
15/188,273 9,780,115	June 21, 2016	303.B12US3	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
15/722,580 10,090,324	October 2, 2017	303.B12US4	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
16/125,242 10,510,769	September 7, 2018	303.B12US5	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
13/035,700 8,759,895	February 25, 2011	303.B44US1	SEMICONDUCTOR CHARGE STORAGE APPARATUS AND METHODS

COMMUNICATION CONCERNING PRIOR OR COPENDING APPLICATIONS

Page 2

Serial Number: 16/716,177

Dkt: 303 B12US6

Filing Date: December 16, 2019

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

14/987,370 9,754,953	January 4, 2016	303.B44US3	CHARGE STORAGE APPARATUS AND METHODS
14/310,790 9,231,117	June 20, 2014	303.B44US2	CHARGE STORAGE APPARATUS AND METHODS
15/691,442	August 30, 2017	303.B44US4	CHARGE STORAGE APPARATUS AND METHODS

Respectfully submitted,

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Date 12-18-19 By / Viet Tong /
Viet V. Tong
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/WILNER JEAN BAPTISTE/

03/16/2020

Modified form PTO/SB/08A(04-07) OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	<i>Complete if Known</i>	
	Application Number	16/716,177
	Filing Date	December 16, 2019
	First Named Inventor	Sanh D. Tang
	Group Art Unit	2827
	Examiner Name	Unknown
Sheet 1 of 1		Attorney Docket No: 303.B12US6

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document
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FOREIGN PATENT DOCUMENTS

Examiner Initial *	Foreign Document Number	Publication Date	Name of Patentee or Applicant of cited Document	T 1
	KR-102005475B1	7/24/2019	Tang, Sanh D., et al.	
	SG-10201907425TA	9/27/2019	Tang, Sanh, et al.	

OTHER DOCUMENTS – NON PATENT LITERATURE DOCUMENTS

Examiner Initial *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 1
	"European Application Serial No. 11807258.6, Communication Pursuant to Article 94(3) EPC mailed 10-07-19", 4 pgs	
	"Korean Application Serial No. 10-2019-7021776, Notice of Preliminary Rejection mailed 11-22-19", w/ English Translation, 5 pgs	
	"Korean Application Serial No. 10-2019-7021776, Response filed 01-22-20 to Notice of Preliminary Rejection mailed 11-22-19", w/ English Claims, 16 pgs	

EXAMINER

/WILNER JEAN BAPTISTE/

DATE CONSIDERED

03/16/2020

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant is to place a check mark here if English language Translation is attached

S/N 16/716,177PATENTIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sanh D. Tang et al.

Examiner: Unknown

Serial No.: 16/716,177

Group Art Unit: Unknown

Filed: December 16, 2019

Docket: 303.B12US6

Customer No.: 73115

Confirmation No.: 3036

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE
SAME

INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached PTO 1449 Form be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the PTO 1449 Form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. § 1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed after filing of the application or after the filing of the most recent RCE, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Pursuant to 37 C.F.R. § 1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicant's prior U.S. application, Serial No. 16/125,242, filed on September 7, 2018, which is relied upon for an earlier filing date under 35 U.S.C. § 120.

Applicant brings to the attention of the Examiner the following Office Actions and responses associated with one or more of the inventors of the instant application and/or the assignee of the instant application. This material is available and accessible at the United States

INFORMATION DISCLOSURE STATEMENT

Serial Number: 16/716,177

Filing Date: December 16, 2019

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Page 2

Dkt: 303.B12US6

Patent and Trademark Office.

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

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Serial Number: 16/716,177

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Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

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INFORMATION DISCLOSURE STATEMENT

Serial Number: 16/716,177

Filing Date: December 16, 2019

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

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The Examiner is invited to contact the undersigned at the telephone number indicated if there are any questions regarding this communication.

Respectfully submitted,

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Date 12-18-19 By / Viet Tong /

VVT:mlsl

Viet V. Tong

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	Application Number	16/716,177
	Filing Date	December 16, 2019
	First Named Inventor	Sanh D. Tang
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 1 of 6	Attorney Docket No: 303.B12US6	

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	Group Art Unit	Unknown
	Examiner Name	Unknown
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Sheet 4 of 6	Attorney Docket No: 303.B12US6	

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Sheet 6 of 6	Attorney Docket No: 303.B12US6	

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Examiner Initial *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 1
	"Taiwanese Application Serial No. 101105342, Response filed 07-24-15 to Office Action mailed 04-28-15", W/ English Claims, 10 pgs	
	KIM, JIYOUNG, et al., "Novel 3-D structure for ultra high density flash memory with VRAT (Vertical-Recess-Array-Transistor) and PIPE (Planarized Integration on the same PlanE)", 2008 Symposium on VLSI Technology, (June 17-19, 2008), 122-23	
	KOMORI, YOSUKE, et al., "Disturbless Flash Memory due to High Boost Efficiency on BiCS Structure and Optimal Memory Film Stack for Ultra High Density Storage Device", International Electron Devices Meeting Technical Digest, (Dec., 2008), 851-854	
	TANAKA, H., et al., "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory", IEEE Symposium on VLSI Technology, (2007), 14-15	

EXAMINER /WILNER JEAN BAPTISTE/

DATE CONSIDERED

03/16/2020

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant is to place a check mark here if English language Translation is attached



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/716,177	12/16/2019	Sanh D. Tang	303.B12US6

CONFIRMATION NO. 3036

PUBLICATION NOTICE



OC000000116289835

73115
SCHWEGMAN LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

Title:THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Publication No.US-2020-0119046-A1

Publication Date:04/16/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/716,177	Filing Date 12/16/2019	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *		x \$100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *		x \$460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED - PART II

	(Column 1)		(Column 2)	(Column 3)	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	06/19/2020		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x \$100 = 0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	x \$460 = 0
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						0
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/DELEACHES M YOUNG/
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A/N 16/716,177

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sanh D. Tang

Examiner: WILNER JEAN BAPTISTE

Application No.: 16/716,177

Group Art Unit: 2899

Filed: December 16, 2019

Docket No.: 303.B12US6

Confirmation No.: 3036

Title: **THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME**

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.111

Mail Stop Amendment
Commissioner for Patents
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Alexandria, VA 22313-1450

Applicant has received the Non-Final Office Action dated March 19, 2020. Please enter the following.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.: 303.B12US6
Filed: December 16, 2019
Examiner: Wilner Jean Baptiste
Customer No.: 73115

Serial No.: 16/716,177
Due Date: June 19, 2020
Group Art Unit: 2899
Confirmation No.: 3036

Mail Stop Amendment
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X Amendment and Response under 37 C.F.R. § 1.111 (9 pgs.)

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SCHWEGMAN LUNDBERG & WOESSNER, P.A.
Customer No.: 73115

By: / Viet Tong /
Viet V. Tong
Reg. No. 45,416

Electronic Acknowledgement Receipt

EFS ID:	39777753
Application Number:	16716177
International Application Number:	
Confirmation Number:	3036
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	John I. Fischer/Amy Moriarty
Filer Authorized By:	John I. Fischer
Attorney Docket Number:	303.B12US6
Receipt Date:	19-JUN-2020
Filing Date:	16-DEC-2019
Time Stamp:	17:22:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303B12US6SIGNEDoaresp.pdf	84794	yes	10
			5a39efb1c0b138d4c5007384a239c287d7aaf28f		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Applicant Arguments/Remarks Made in an Amendment	9	10
	Claims	3	8
	Amendment/Req. Reconsideration-After Non-Final Reject	2	2
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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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REMARKS

This responds to the Non-Final Office Action dated March 19, 2020.

Claims 1-20 are presently canceled. Claims 21-40 are presently added. Thus, claims 21-40 are now pending in this application.

Support for the amendments made to the claims can be found in the application, for example, in at least FIG. 2, FIG. 3, FIG. 7, FIG. 8, FIG. 29, FIG. 30, and FIG. 31 of the drawings. No new matter has been added. Reconsideration of the claims in view of the amendments above and the remarks that follow is respectfully requested.

Double Patenting Rejection

Claims 1-8 were rejected on the ground of non-statutory obviousness-type double patenting as being un-patentable over claims 1-8 of U.S. Patent No. 9,780,115 (here and after '115).

Claims 9-14 were rejected on the ground of non-statutory obviousness-type double patenting as being un-patentable over claims 9-14 of U.S. Patent No. 9,780,115 (here and after '115).

Claims 15-20 were rejected on the ground of non-statutory obviousness-type double patenting as being un-patentable over claims 15-20 of U.S. Patent No. 9,780,115 (here and after '115).

Applicant does not admit that claims 1-20 are obvious in view of U.S. Patent No. 9,780,115. However, claims 1-20 are canceled without disclaimer or prejudice. Thus, the rejection of claims 1-20 is moot.

New Claims

Claims 21-40 are new. Consideration and allowance of claims 21-40 is respectfully requested.

CONCLUSION

It is respectfully submitted that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone the undersigned at (612) 373-6900 to facilitate prosecution of this application.

If necessary, please charge any additional fees or deficiencies, or credit any overpayments to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402-0938
(612) 373-6900

Date June 19, 2020

By / Viet Tong /
Viet V. Tong
Reg. No. 45,416

IN THE CLAIMS

Please amend the claims as follows:

1-20. (Canceled)

21. (New) An apparatus comprising:

conductive pillars extending outward from a substrate;

memory cell strings, each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars;

a first control gate formed in a first device level, the memory cell strings including a memory cell string, the memory cell string including a first memory cell having a memory element formed in a cavity of the first control gate;

a second control gate formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the second control gate; and

a conductive channel extending between the first memory cell and the second memory cell and electrically coupled to a conductive pillar of the conductive pillars.

22. (New) The apparatus of claim 21, further comprising:

a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material; and

a second conductive region located on a second side opposite from the first side of the conductive pillar and separated from the conductive pillar by a second dielectric material.

23. (New) The apparatus of claim 22, wherein the first conductive region is coupled to the second conductive region.

24. (New) The apparatus of claim 22, wherein each of the first and second conductive regions comprises polysilicon.

25. (New) The apparatus of claim 22, wherein each of the first and second conductive regions comprises metal.

26. (New) The apparatus of claim 21, further comprising a data line coupled to the conductive channel, wherein the data line is located between the substrate and the first and second memory cells.

27. (New) The apparatus of claim 21, further comprising a data line coupled to the conductive channel, wherein the first and second memory cells are located between the data line and the substrate.

28. (New) The apparatus of claim 21, wherein the memory element comprises polysilicon.

29. (New) The apparatus of claim 21, wherein the memory element comprises a dielectric material.

30. (New) An apparatus comprising:

- a first conductive pillar and a second conductive pillar extending outward from a substrate;
- a first data line coupled to the first and second conductive pillars, the first data line located between the first and second conductive pillars and the substrate;
- a third conductive pillar and a fourth conductive pillars extending outward from the substrate;

- a second data line coupled to the third and fourth conductive pillars, the second data line located between the third and fourth conductive pillars and the substrate;

- a first memory cell string formed over the first conductive pillar;

- a second memory cell string formed over the second conductive pillar;

- a third memory cell string formed over the third conductive pillar;

- a fourth memory cell string formed over the fourth conductive pillar;

- a first control gate formed in a first device level;

- a second control gate formed in a second device level, wherein,

the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate;

the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate;

the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate; and

the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.

31. (New) The apparatus of claim 30, further comprising:

a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells;

a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells;

a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells; and

a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells.

32. (New) The apparatus of claim 30, further comprising a first conductive gate including a first segment and a second segment coupled to the first segment, wherein:

the first segment is located on a first side of each of the first and third conductive pillars and separated from the first and third conductive pillars by a first dielectric material; and

the second segment is located on a second side of each of the first and third conductive pillars and separated from the first and third conductive pillars by a second dielectric material.

33. (New) The apparatus of claim 32, further comprising a second conductive gate including a third segment and a fourth segment coupled to the third segment, wherein:

the third segment is located on a first side of each of the second and fourth conductive pillars and separated from the second and fourth conductive pillars by a third dielectric material; and

the fourth segment is located on a second side of each of the second and fourth conductive pillars and separated from the second and fourth conductive pillars by a fourth dielectric material.

34. (New) The apparatus of claim 33, wherein each of the first and second conductive gates comprises polysilicon.

35. (New) The apparatus of claim 33, wherein each of the first and second conductive gates comprises metal.

36. (New) The apparatus of claim 30, wherein the memory element of each of the first, second, third, and fourth memory cells comprises one of polysilicon and a dielectric material.

37. (New) An apparatus comprising:

a first conductive pillar and a second conductive pillar extending outward from a substrate;

a third conductive pillar and a fourth conductive pillars extending outward from the substrate;

a region including a conductive material, the region coupled to the first, second, third, and fourth conductive pillars, the region located between substrate and the first, second, third, and fourth conductive pillars;

a first memory cell string formed over the first conductive pillar;

a second memory cell string formed over the second conductive pillar;

a third memory cell string formed over the third conductive pillar;

a fourth memory cell string formed over the fourth conductive pillar;

a first data line coupled to the first and second memory cell strings, the first and second memory cell strings located between the first data line and the substrate;

a second data line coupled to the third and fourth memory cell strings, the third and fourth memory cell strings located between the second data line and the substrate;

a first control gate formed in a first device level;

a second control gate formed in a second device level, wherein,

the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate;

the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate;

the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate; and

the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.

38. (New) The apparatus of claim 37, wherein the memory element of each of the first, second, third, and fourth memory cells comprises polysilicon.

39. (New) The apparatus of claim 37, wherein the memory element of each of the first, second, third, and fourth memory cells comprises a silicon nitride.

40. (New) The apparatus of claim 37, further comprising:

a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells;

a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells;

a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells; and

a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells.



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73115 7590 08/19/2020
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P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER

JEAN BAPTISTE, WILNER

ART UNIT

PAPER NUMBER

2899

DATE MAILED: 08/19/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/716,177	12/16/2019	Sanh D. Tang	303.B12US6	3036

TITLE OF INVENTION: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	11/19/2020

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	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/716,177	12/16/2019	Sanh D. Tang	303.B12US6	3036

TITLE OF INVENTION: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	11/19/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
JEAN BAPTISTE, WILNER	2899	257-316000

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(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/716,177	12/16/2019	Sanh D. Tang	303.B12US6	3036
73115	7590	08/19/2020	EXAMINER	
SCHWEGMAN LUNDBERG & WOESSNER/MICRON			JEAN BAPTISTE, WILNER	
P.O. BOX 2938			ART UNIT	
MINNEAPOLIS, MN 55402			PAPER NUMBER	
			2899	
DATE MAILED: 08/19/2020				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/716,177	Applicant(s) Tang et al.	
	Examiner WILNER JEAN BAPTISTE	Art Unit 2899	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 6/19/2020.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 21-40. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____ 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____
--	---

/W.J/ Examiner, Art Unit 2899	/DALE E PAGE/ Supervisory Patent Examiner, Art Unit 2899
----------------------------------	---

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

CROSS REFERENCE TO RELATED APPLICATIONS

2. This application is a continuation of U.S. Application Serial No. 16/125,242, filed September 7, 2018, which is a continuation of U.S. Application Serial No. 15/722,580, filed October 2, 2017, now issued as U.S. Patent No. 10,090,324, which is a continuation of U.S. Application Serial No. 15/188,273, filed June 21, 2016, now issued as U.S. Patent No. 9,780,115, which is a continuation of U.S. Application Serial No. 14/041,928, filed September 30, 2013, now issued as U.S. Patent No. 9,379,005, which is a divisional of U.S. Application Serial No. 12/825,211, filed June 28, 2010, now issued as U.S. Patent No. 8,803,214, all of which are incorporated herein by reference in their entireties.

Allowable Subject Matter

3. Claims 21-40 are allowed.

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance:
5. Regarding claims 21-29, the prior art failed to disclose or reasonably suggest a first control gate formed in a first device level, the memory cell strings including a memory cell string, the memory cell string including a first memory cell having a memory element formed in a cavity of the first control gate; a second control gate formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the second control gate; and a conductive

channel extending between the first memory cell and the second memory cell and electrically coupled to a conductive pillar of the conductive pillars.

7. Regarding claims 30-36, the prior art failed to disclose or reasonably suggest a third memory cell string formed over the third conductive pillar; a fourth memory cell string formed over the fourth conductive pillar; a first control gate formed in a first device level; a second control gate formed in a second device level, wherein, the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate; the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate; the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate; and the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.

8. Regarding claims 37-40, the prior art failed to disclose or reasonably suggest a first data line coupled to the first and second memory cell strings, the first and second memory cell strings located between the first data line and the substrate; a second data line coupled to the third and fourth memory cell strings, the third and fourth memory cell strings located between the second data line and the substrate; a first control gate formed in a first device level; a second control gate formed in a second device level, wherein, the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element

formed in a first cavity of the second control gate; the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate; the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate; and the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILNER JEAN BAPTISTE whose telephone number is (571)270-7394. The examiner can normally be reached on M-T 8:00-6:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dale Page can be reached on 571-270-7877. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2899

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W.J/

Examiner, Art Unit 2899

/DALE E PAGE/

Supervisory Patent Examiner, Art Unit 2899

Issue Classification 	Application/Control No. 16/716,177	Applicant(s)/Patent Under Reexamination Tang et al.	
	Examiner WILNER JEAN BAPTISTE	Art Unit 2899	

CPC						
Symbol					Type	Version
H01L	/	27	/	11582	F	2013-01-01
H01L	/	29	/	40114	I	2019-08-01
H01L	/	27	/	0688	I	2013-01-01
H01L	/	27	/	11551	I	2013-01-01
H01L	/	27	/	11556	I	2013-01-01
H01L	/	27	/	11578	I	2013-01-01
H01L	/	27	/	249	I	2013-01-01
H01L	/	29	/	66825	I	2013-01-01
H01L	/	29	/	66833	I	2013-01-01
H01L	/	29	/	7889	I	2013-01-01
H01L	/	29	/	7926	I	2013-01-01
H01L	/	27	/	2454	I	2013-01-01
H01L	/	27	/	11548	I	2013-01-01
H01L	/	27	/	11575	I	2013-01-01
H01L	/	21	/	76838	I	2013-01-01
G11C	/	13	/	004	I	2013-01-01
G11C	/	13	/	0069	I	2013-01-01
G11C	/	13	/	0097	I	2013-01-01
G11C	/	16	/	10	I	2013-01-01
G11C	/	16	/	14	I	2013-01-01
G11C	/	16	/	26	I	2013-01-01
H01L	/	23	/	528	I	2013-01-01
H01L	/	27	/	11519	I	2013-01-01
H01L	/	27	/	11565	I	2013-01-01
H01L	/	45	/	06	A	2013-01-01
G11C	/	2213	/	71	A	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
/				

/WILNER JEAN BAPTISTE/ Examiner, Art Unit 2899 (Assistant Examiner)	06 August 2020 (Date)	Total Claims Allowed: 20	
/DALE E PAGE/ Supervisory Patent Examiner, Art Unit 2899 (Primary Examiner)	13 August 2020 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4

Issue Classification 	Application/Control No. 16/716,177	Applicant(s)/Patent Under Reexamination Tang et al.
	Examiner WILNER JEAN BAPTISTE	Art Unit 2899

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L	/	27	/ 11582
H01L	/	27	/ 11565
H01L	/	23	/ 528
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

/WILNER JEAN BAPTISTE/ Examiner, Art Unit 2899 (Assistant Examiner)	06 August 2020 (Date)	Total Claims Allowed: 20	
/DALE E PAGE/ Supervisory Patent Examiner, Art Unit 2899 (Primary Examiner)	13 August 2020 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4

Issue Classification 	Application/Control No. 16/716,177	Applicant(s)/Patent Under Reexamination Tang et al.
	Examiner WILNER JEAN BAPTISTE	Art Unit 2899

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47
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CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
-	1	--	10	--	19	8	28	17	37						
--	2	--	11	--	20	9	29	18	38						
--	3	--	12	1	21	10	30	19	39						
--	4	--	13	2	22	11	31	20	40						
--	5	--	14	3	23	12	32								
--	6	--	15	4	24	13	33								
--	7	--	16	5	25	14	34								
--	8	-	17	6	26	15	35								
--	9	--	18	7	27	16	36								

/WILNER JEAN BAPTISTE/ Examiner, Art Unit 2899 (Assistant Examiner)	06 August 2020 (Date)	Total Claims Allowed: 20	
/DALE E PAGE/ Supervisory Patent Examiner, Art Unit 2899 (Primary Examiner)	13 August 2020 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4

<i>Search Notes</i> 	Application/Control No. 16/716,177	Applicant(s)/Patent Under Reexamination Tang et al.
	Examiner WILNER JEAN BAPTISTE	Art Unit 2899

CPC - Searched*		
Symbol	Date	Examiner
(H01L27/11517-1156 H01L2924/1438 H01L29/42324-42336 H01L29/788-7889)	03/16/2020	wj
(H01L27/11582 H01L27/11519 H01L23/528)	08/06/2020	wj

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
CPC-CAT-EPO-EAST	03/16/2020	wj
Text search	03/16/2020	wj
Text search updated		

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H01L27	11582,11519	08/06/2020	wj
H01L23	528	08/06/2020	wj

/W.J/ Examiner, Art Unit 2899	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S50	2	"20200119046".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/05 22:58
S51	30	"10510769".pn. "10090324".pn. "97801158".pn. "9379005".pn. "8803214".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/05 23:04
S52	45,190	(H01L27/11582 H01L27/11519 H01L23/528).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/06 10:18
S53	30	((memory near\$2 cells) with (control adj gate) with ((conductive contact interconnect pillars) with ((initial or first) near\$2 (cavities or grooves or vias or openings)) same (aligned or adjust or straighten or even or fix) same (second near\$2 (cavities or groove or vias or opening)) same substrate)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/06 10:25
S54	1,291	S52 and ((memory near\$2 cells) with (control adj gate) with (conductive contact interconnect pillars) with (((initial or first) near\$2 (cavities or grooves or vias or openings)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/06 10:29
S55	13	("10115681" "20160079255" "20170103995" "20170125538" "20180012903" "20180130743" "20180342455" "20180366487" "20190371813" "5915167" "9691784" "9793139" "9806088").PN. OR ("10665607").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/08/06 10:32

8/6/2020 12:22:11 PM

C:\Users\wjeanbaptiste\Documents\EAST\Workspaces\16-716177 (Three Dimensional Memory).wsp

Bibliographic Data

Application No: 16/716,177

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged:

/WILNER JEAN BAPTISTE/

Examiner's Signature

Initials

Title:

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/16/2019	257	2899	303.B12US6
RULE			

APPLICANTS

Micron Technology, Inc., Boise, ID, UNITED STATES

INVENTORS

Sanh D. Tang, Boise, ID, UNITED STATES

John K. Zahurak, Eagle, ID, UNITED STATES

CONTINUING DATA

This application is a CON of 16125242 09/07/2018 PAT 10510769

16125242 is a CON of 15722580 10/02/2017 PAT 10090324

15722580 is a CON of 15188273 06/21/2016 PAT 9780115

15188273 is a CON of 14041928 09/30/2013 PAT 9379005

14041928 is a DIV of 12825211 06/28/2010 PAT 8803214

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

01/08/2020

STATE OR COUNTRY

UNITED STATES

ADDRESS

SCHWEGMAN LUNDBERG & WOESSNER/MICRON

P.O. BOX 2938

MINNEAPOLIS, MN 55402

UNITED STATES

FILING FEE RECEIVED

\$1,720

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S56	30	((memory near\$2 cells) with (control adj gate) with ((conductive contact interconnect pillars) with ((initial or first) near\$2 (cavities or grooves or vias or openings)) same (aligned or adjust or straighten or even or fix) same (second near\$2 (cavities or groove or vias or opening)) same substrate)).clm.	US-PGPUB; USPAT	OR	ON	2020/08/06 10:27

8/6/2020 12:22:38 PM

C:\Users\wjeanbaptiste\Documents\EAST\Workspaces\16-716177 (Three Dimensional Memory).wsp

S/N 16/716,177

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Sanh D. Tang et al.	Examiner:	Wilner Jean Baptiste
Serial No.:	16/716,177	Group Art Unit:	2899
Filed:	December 16, 2019	Docket No.:	303.B12US6
Customer No.:	26809	Confirmation No.:	3036
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

COMMUNICATION RE: FEE ADDRESS

Mail Stop Issue Fee
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

In response to the Notice of Allowance and Issue Fee Due, please record the Fee Address under the provisions of 37 CFR 1.363 as the following:

Customer Number 26809

Please direct any inquiries to the undersigned attorney at (612) 373-6969.

Respectfully submitted,

SCHWEGMAN LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 11-19-20

By / Viet Tong /

VVT:CMG:jan

Viet V. Tong
Reg. No. 45,416

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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73115 7590 08/19/2020
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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Julie A. Nelson	(Typed or printed name)
<i>Julie A. Nelson</i>	(Signature)
November 19, 2020	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/716,177	12/16/2019	Sanh D. Tang	303.B12US6	3036

TITLE OF INVENTION: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	11/19/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
JEAN BAPTISTE, WILNER	2899	257-316000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Schwegman Lundberg

2 & Woessner, P.A.

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Micron Technology, Inc.

Boise, Idaho

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

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☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 19-0743

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature

Viet Tong

Date

11-19-20

Typed or printed name

Viet V. Tong

Registration No.

45,416

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.: 303.B12US6

Serial No.: 16/716,177

Filed: December 16, 2019

Due Date: November 19, 2020

Examiner: Wilner Jean Baptiste

Group Art Unit: 2899

Customer No.: 73115

Confirmation No.: 3036

Notice of Allowance Date: August 19, 2020

Mail Stop Issue Fee

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

We are transmitting herewith the following:

- ☒ Authorization to charge Deposit 19-0743 in the amount of \$1,000.00 to cover the Large Entity Issue Fee Payment.
- ☒ Issue Fee Transmittal (Form PTOL-85).
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By

/ Viet Tong /

Customer No.: 73115

Viet V. Tong

VVT:CMG:jan

Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 19th day of November, 2020.

Julie A. Nelson

Name

Signature

/ Julie A. Nelson /

Electronic Patent Application Fee Transmittal				
Application Number:		16716177		
Filing Date:		16-Dec-2019		
Title of Invention:		THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		
First Named Inventor/Applicant Name:		Sanh D. Tang		
Filer:		Edward James Sandor/Julie Nelson		
Attorney Docket Number:		303.B12US6		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt

EFS ID:	41168441
Application Number:	16716177
International Application Number:	
Confirmation Number:	3036
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Edward James Sandor/Julie Nelson
Filer Authorized By:	Edward James Sandor
Attorney Docket Number:	303.B12US6
Receipt Date:	19-NOV-2020
Filing Date:	16-DEC-2019
Time Stamp:	12:29:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1000
RAM confirmation Number	E2020AIC29366616
Deposit Account	190743
Authorized User	Julie Nelson

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303B12US6_XMIT_IFEE_signed.pdf	439328	yes	3
			0a60b7dcb3daad40c5449799daf4dd9e54ae6f3c		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Change of Address		3	3	
	Issue Fee Payment (PTO-85B)		2	2	
	Transmittal Letter		1	1	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30271	no	2
			10a7a05dbe358fd29d8e2464aae908741f6dc3da		
Warnings:					
Information:					
Total Files Size (in bytes):			469599		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/716,177	12/22/2020	10872903	303.B12US6	3036

73115 7590 12/02/2020

SCHWEGMAN LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Sanh D. Tang, Boise, ID;
Micron Technology, Inc., Boise, ID;
John K. Zahurak, Eagle, ID;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.