

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

Petitioner,

v.

MICRON TECHNOLOGY, INC.

Patent Owner.

Case IPR2025-00099

U.S. Patent No. 10,872,903

**DECLARATION OF DR. KELIN J. KUHN IN SUPPORT
OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,872,903**

Executed this 16th day of November 2024, in Gig Harbor, Washington.


Dr. Kelin Kuhn

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
II. QUALIFICATIONS.....	4
III. LEGAL UNDERSTANDING.....	10
IV. BACKGROUND OF THE TECHNOLOGY.....	17
V. THE '903 PATENT	20
A. '903 Patent Overview	20
B. The Prosecution History	23
VI. LEVEL OF ORDINARY SKILL IN THE ART	24
VII. CLAIM CONSTRUCTION.....	25
A. “cavity” of the “control gate” ([1.c]-[1.d], [17.l]-[17.o])	26
VIII. GROUNDS OF UNPATENTABILITY.....	26
IX. SPECIFIC GROUNDS FOR CHALLENGE	27
A. GROUND 1: Ahn (Claims 1-3, 5, 7-9, 17-20).....	28
1. Overview of Ahn.....	28
2. Invalidity of Claims 1-3, 5, 7-9, and 17-20 Over Ahn.....	30
B. GROUND 2: Ahn in view of Ishikawa (Claims 7, 17).....	91
C. GROUND 3: Fukuzumi (Claims 1-3, 7, 9, 17, 19-20).....	96
1. Overview of Fukuzumi	96
2. Invalidity of Claims 1-3, 7, 9, 17, and 19-20 Over Fukuzumi	98
D. GROUND 4: Fukuzumi in view of Ahn (Claims 5, 8, 18)	159
1. Invalidity of Claim [5] Over Fukuzumi in view of Ahn.	161
2. Invalidity of Claims [8] and [18] Over Fukuzumi in view of Ahn.	164

X.	SECONDARY CONSIDERATIONS	168
XI.	CONCLUSION	168

I. INTRODUCTION

1. My name is Dr. Kelin J. Kuhn and I am an adjunct professor in the Materials Science and Engineering Department at Cornell University. I have been retained on behalf of Yangtze Memory Technologies Company, Ltd. (“YMTC”), to provide my opinions on certain issues related to U.S. Patent No. 10,872,903 (“the ’903 patent”) in connection with the above-captioned inter partes review (IPR) proceeding. In particular, I have been asked to provide my insights, analysis, and opinions regarding whether claims 1-3, 5, 7-9, and 17-20 of the ’903 patent (“Challenged Claims” or “Claims”) are anticipated and/or obvious over the prior art references identified below.

2. I understand that the ’903 patent is titled “Three Dimensional Memory and Methods of Forming the Same,” names as inventors Sanh D. Tang and John K. Zahurak, and is currently owned by Micron Technology, Inc. I have considered the ’903 patent. I understand that the ’903 patent has been provided as Ex. 1001.

3. I understand that the file history of the ’903 patent has been provided as Ex. 1002. I have considered this file history, and I will refer to it as “the ’903 File History” or by its exhibit number.

4. I understand that the ’903 patent is a continuation of U.S. Patent Application No. 16/125,242, which is a continuation of U.S. Patent Application No. 15/722,580, which is a continuation of U.S. Patent Application No.

15/188,273, which is a continuation of U.S. Patent Application No. 14/041,928, which is a divisional of U.S. Patent Application No. 12/825,211. I have considered this file history.

5. I understand that the '903 patent claims a priority date of June 28, 2010, the filing date of U.S. Patent Application No. 12/825,211. I have been asked to assume that priority date for purposes of rendering my opinions in this declaration. I have not been asked to opine on whether the Challenged Claims of the '903 patent are entitled to this priority date, and do not provide any opinion on that subject.

6. My analysis and conclusions set forth in this declaration are based on my educational background and experiences in the field (see Section II). Before June 28, 2010, my level of skill in the art was at least that of a person of ordinary skill. I am qualified to opine concerning what a person of ordinary skill in the art would have known and understood at the time of the '903 patent's purported invention. My analysis and conclusions herein are from the perspective of a person of ordinary skill in the art as of June 28, 2010.

7. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this art during the time before the earliest claimed priority date for the '903 patent; my own knowledge and

experiences gained from my work experience in the field of the '903 patent and related disciplines; and my experience in working with others involved in this field and related disciplines.

8. I have considered the following non-exhaustive list of references in preparing my declaration. I have been instructed to assume that each of these references qualifies as prior art.

- **Korean Publication No. KR10-2010-0034612** to Jung-yeol Ahn (“Ahn”), titled “Method for Manufacturing a Flash Memory Device Having a Three-dimensional Structure” filed on September 24, 2008, and published April 1, 2010. I understand that a copy of this reference has been designated as Exhibit 1005, and a certified translation of this reference has been designated as Exhibit 1004.
- **U.S. Patent Application Publication No. U.S. 2009/0146190** to Yoshiaki Fukuzumi, Ryota Katsumata, Masaru Kidoh, Masaru Kito, Hiroyasu Tanaka, Hideaki Aochi, and Yasuyuki Matsuoka (“Fukuzumi”), titled “Semiconductor memory device and method for fabricating semiconductor memory device” filed on Dec. 1, 2008, and published June 11, 2009. I understand that a copy of this reference has been designated as Exhibit 1006.
- **U.S. Patent Application Publication No. U.S. 2009/0283819** to Masao Ishikawa and Katsunori Yahashi (“Ishikawa”), titled “Nonvolatile semiconductor memory device and method for manufacturing same” filed on March 20, 2009, and published November 19, 2009. I understand that a copy of this reference has been designated as Exhibit 1007.

9. I understand that there is a pending district court litigation between Petitioner and Micron Technology, Inc. (“YMTC Litigation”) involving the '903 patent.

10. I am being compensated by YMTC at my standard hourly consulting

rate of \$600 for my time on this matter. My compensation is not dependent on the outcome of this proceeding or any other proceeding between the parties.

11. As set forth herein, I have concluded that each of Challenged Claims is anticipated and/or rendered obvious by the prior art based on the references described below and as explained herein. In forming my opinions, I relied on the documents cited in this declaration and the documents identified in the attached **Appendix B**. These documents comprise patents, file histories, printed publications, and other related documents. As discussed below, each document is a type that experts in my field would have reasonably relied upon when forming their opinions. Further, experts in my field would have had access to each document either through the applicable patent offices and/or well-known libraries, conferences, or publications in the field. My opinions are also based upon my personal and professional experience.

II. QUALIFICATIONS

12. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as **Appendix A**. Here, I provide a brief summary of my qualifications.

13. I am qualified by education and experience to testify as an expert in the field of three-dimensional memory devices. Additionally, the following overview of my background pertains to my qualifications for providing expert testimony in this

matter. I am over the age of 18 and am competent to write this declaration. I have personal knowledge, or have developed knowledge, of these technologies based upon education, training, or experience of the matters set forth herein.

14. I received my B.S., magna cum laude, in Electrical Engineering from the University of Washington, Seattle in 1980, and received an M.S. and a Ph.D. in Electrical Engineering from Stanford University in 1985. I undertook post-doctoral work at Stanford from 1985 to 1987.

15. I am presently retired from industry. However, I still periodically engage in engineering projects for select clients and have a small business (Confluence Technology Services) to support that activity.

16. I am also currently an adjunct professor of Materials Science and Engineering at Cornell University, where my research interests are in the areas of quantum materials, post-CMOS technology, and spintronics.

17. For nearly a decade, beginning in 1987, I held faculty positions at the University of Washington, Seattle, beginning as a Research Assistant Professor in Material Science and Engineering, then as Assistant Professor in Electrical and Computer Engineering, and finally as a tenured Associate Professor of Electrical and Computer Engineering. During this period, I worked in III-V molecular beam epitaxy and optoelectronics and was awarded the University's highest accolade for a faculty member, the Distinguished Teaching Award, in 1995.

18. In 1997, I joined Intel Corporation (“Intel”) at the Aloha Campus in Oregon as a Senior Process Engineer. I focused on front-end integration on the Intel 0.35 μ m process technology. In this role, I was responsible for the silicide section of the process flow, interaction with the reliability community, and integration on the CMOS camera chip project.

19. In 1999, I was transferred to Portland Technology Development at Ronler Acres, Oregon, as a Senior Process Engineer. I worked on front-end integration on the 130 nm CMOS generation. In this role, I was responsible for the isolation section of the process flow as well as integration of Optical Proximity Correction technologies into 130 nm.

20. In 2001, I advanced to the title of Principal Engineer. In 2002, I was promoted to the role of Process Program Manager for Intel’s 90 nm communications process technology. Over a three-year period, my team developed a derivative analog/RF technology (including a SiGe bipolar junction transistor (“BJT”)) on top of Intel’s premium 90 nm microprocessor process.

21. In 2004, I advanced to the title of Senior Principal Engineer and was promoted to the role of Device Technology Manager of the pathfinding team at Intel that was responsible for the high-k metal-gate transistor architecture of Intel’s 45 nm microprocessor processor technology. I received an Intel Achievement Award in 2006 for my work on the high-k metal gate.

22. In 2007, I achieved the title of Intel Fellow and became Director of Advanced Device Technology. Fellow is the highest level of technical achievement within Intel, with approximately 50 Fellows among approximately 100,000 total employees. My work evolved to a strategic role in overseeing the transition of advanced device technologies from research into development. In this role, I played an active part in the transfer of transistor technology for the 32 nm node, 22 nm node, and 14 nm node (the last two nodes involving Intel's FinFET device). I received a second Intel achievement award in 2008 for my work on Intel's FinFET device.

23. In 2009, my title remained the same, but my role transitioned from development (in Portland Technology Development, at Ronler Acres) to research (in the Components Research Group, still at Ronler Acres). From 2009 until my retirement from Intel in 2014, I researched advanced device architectures for Intel processes in the five-to-ten-year time frame.

24. While much of my later work at Intel still remains confidential, certain aspects of my work during this period are featured in my book CMOS And Beyond: Logic Switches for Terascale Integrated Circuits (Co-Editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015), as well as in my paper "Considerations for Ultimate CMOS Scaling" (IEEE Trans. on Elec. Dev., Vol. 59, No. 7, 2012), winner of the 2013 Paul Rappaport Award.

25. Since my retirement in 2014, my consulting work has included a variety of semiconductor related projects. While the detailed technical content is, of course, protected by client confidentiality, these projects include, FinFETs, vertical power transistors, solar cells, conventional (planar) MOS, and flash.

26. I am the author of more than 100 technical papers in electronics and photonics. I am currently the Associate Editor in Chief (AEiC) of IEEE Electron Device Letters, having served as an editor since 2015, and as AEiC since 2024.

27. A few of my other representative journal publications include: “Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results,” (Symposium on VLSI Technology, 2012); “Process Technology Variation,” (IEEE Transactions on Electron Devices, Vol. 58, No. 8, 2011); “A 45 nm logic technology with high- k +metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging,” (2007 IEEE International Electron Devices Meeting); and “Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm,” (IEEE Electron Device Letters, Vol. 32, No. 9, 2011).

28. A few representative book chapters include, “The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8. Chapter 1, CMOS and Beyond

CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616).

29. I am an inventor on approximately 80 granted U.S. patents in the field of semiconductor technology.

30. A few of my other relevant honors include being a Fellow at the Institute of Electrical and Electronics Engineers (“IEEE”), a recipient of the IEEE Frederik Philips Award (2016), a recipient of the IEEE Paul Rappaport Award (2013), the recipient of eleven Intel Divisional Awards, and election to the National Academy of Engineering (2023). Earlier in my career, I received the NSF Presidential Young Investigator Award.

31. As specifically relevant to this project, I want to highlight the 3’D gate-last vertical gate-all-around (GAA) devices and the 3’D vertical GAA arrays that are discussed at some length in “Considerations for Ultimate CMOS Scaling” (see Fig. 15 in particular). I also want to highlight on-going proprietary and confidential work, in the matter of Silicon Storage Technology, Inc. vs. Taiwan Semiconductor Manufacturing Company involving flash.

32. Attached as **Appendix A** to this report is a current copy of my curriculum vitae, which outlines my academic, professional and experiential

qualifications in the semiconductor and integrated circuit industries, as well as a list of publications I have authored and co-authored and presentations I have given.

III. LEGAL UNDERSTANDING

33. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

34. I have been informed of certain legal understandings relevant to my opinions. In formulating my opinions, I have relied on the legal understandings I have been provided with as set forth in this declaration.

35. I have been informed that in *inter partes* review proceedings, invalidity must be shown under a preponderance of the evidence standard.

A. My Understanding of Claim Construction

36. I have been informed that patent claims are construed from the viewpoint of a person of ordinary skill in the art of the patent at the time of the invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a person of ordinary skill in the art in the relevant time period (i.e., at the time of the purported invention, or the so called “effective filing date” of the patent application), after reviewing the patent claim language, the specification, and the prosecution history (i.e., the intrinsic record).

37. I have further been informed that a person of ordinary skill in the art must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner's rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or clearly and unambiguously disavowing claim coverage.

38. In interpreting the meaning of the claim language, I understand that a person of ordinary skill in the art may also consider "extrinsic" evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of ordinary skill in the art at the time of the claimed invention. For example, this can be useful for a technical term whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts

or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

B. My Understanding of Anticipation

39. I understand that a patent claim is invalid as “anticipated” if all the limitations of the claim are present, either expressly or inherently, in a single prior art publication or patent.

40. I also understand that a prior art reference can disclose a claimed feature because the feature is expressly described or because the feature is inherent in the disclosure. I have been informed that something is inherent in a prior art reference if the missing descriptive matter must necessarily be present, not merely probably or possibly present, and it would be so recognized by a person of ordinary skill in the art as of the priority date of the patent. I understand that it is acceptable to examine evidence outside of the prior art reference (i.e., extrinsic evidence) in determining whether a feature, while not expressly discussed in the reference, is necessarily present in it.

41. I have further been informed that where a reference discloses multiple embodiments, the reference should not be limited to a preferred embodiment. Instead, each disclosed embodiment may anticipate.

42. Moreover, I have been informed that as part of an anticipation analysis, it is proper to take into account not only specific teachings of the reference, but also

the inferences that one skilled in the art would reasonably be expected to draw therefrom. A reference can anticipate a claim even if it does not expressly spell out all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would at once envisage the claimed arrangement or combination.

C. My Understanding of Obviousness

43. I understand that a claim may be invalid if the subject matter described by the claim as a whole would have been obvious to a hypothetical person of ordinary skill in the art in view of a prior art reference or in view of a combination of references at the time the claimed invention was made. Therefore, I understand that obviousness is determined from the perspective of a hypothetical person of ordinary skill in the art and that the asserted claims of the patent should be read from the point of view of such a person at the time the claimed invention was made. I further understand that a hypothetical person of ordinary skill in the art is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent in suit.

44. I have been informed that there are two criteria for determining whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee's endeavor, whether the reference

still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee's attention in considering their problem.

45. I have also been advised that an analysis of whether a claimed invention would have been obvious should be considered in light of the scope and content of the prior art, the differences (if any) between the prior art and the claimed invention, and the level of ordinary skill in the pertinent art involved. I understand as well that a prior art reference should be viewed as a whole.

46. I have also been advised that in considering whether a claimed invention would have been obvious over a combination of prior art references, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the marketplace, and/or the background knowledge possessed by a person of ordinary skill in the art. I understand that other principles may be relied on in evaluating

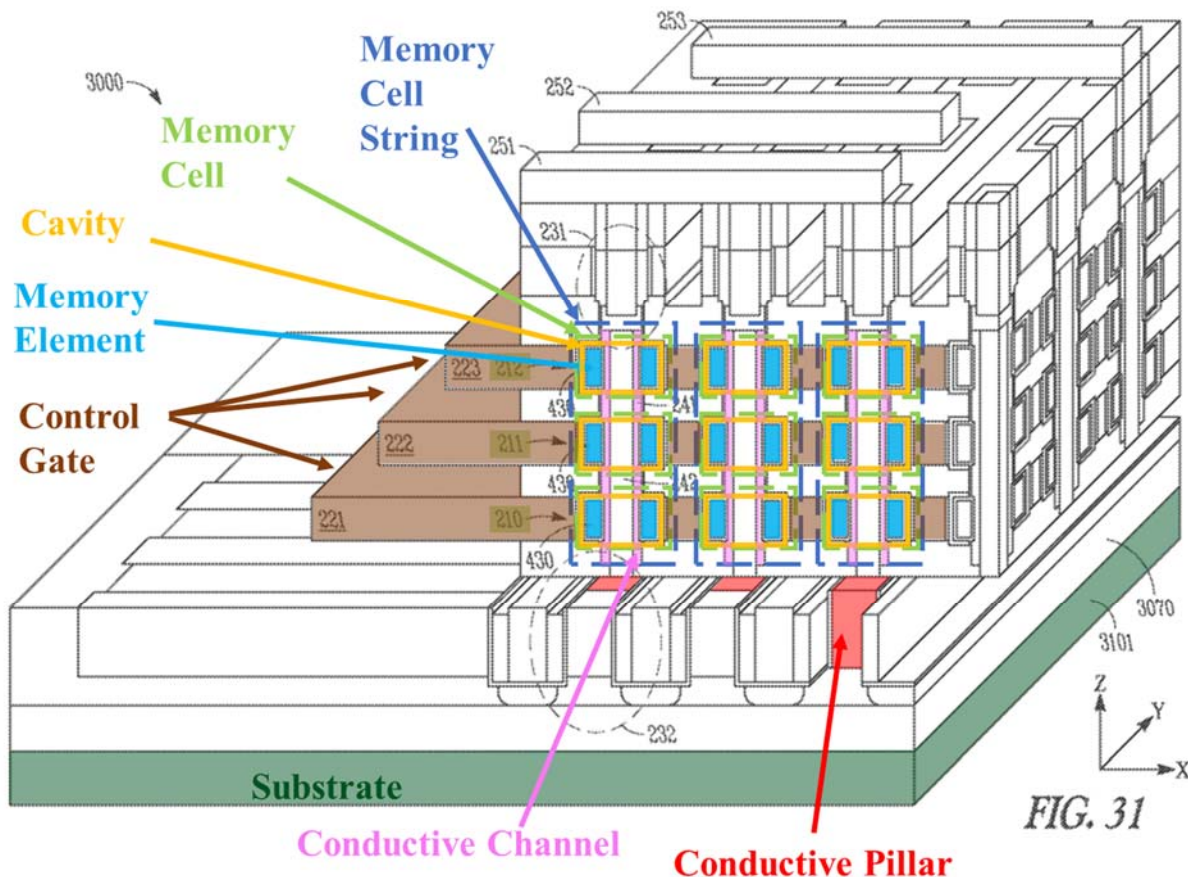
whether a claimed invention would have been obvious, and that these principles include the following:

- A combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results;
- When a device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a person of ordinary skill can implement a predictable variation, the variation is likely obvious;
- If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond their skill;
- An explicit or implicit teaching, suggestion, or motivation to combine two prior art references to form the claimed combination may demonstrate obviousness, but proof of obviousness does not depend on or require showing a teaching, suggestion, or motivation to combine;
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the particular motivation nor the avowed purpose of the named inventor controls whether the claim is obvious;
- One of the ways in which a patent's subject can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;
- Any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed;
- "Common sense" teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle;

- A person of ordinary skill in the art is also a person of ordinary creativity, and is not an automaton;
- A patent claim can be proved obvious by showing that the claimed combination of elements was “obvious to try,” particularly when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions such that a person of ordinary skill in the art would have had good reason to pursue the known options within his or her technical grasp; and
- One should be cautious of using hindsight in evaluating whether a claimed invention would have been obvious.

47. I further understand that, in making a determination as to whether the claimed invention would have been obvious to a person of ordinary skill, the Board may consider certain objective factors if they are present, such as: commercial success of products practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. These factors are generally referred to as “secondary considerations” or “objective indicia” of nonobviousness. I understand, however, that for such objective evidence to be relevant to the obviousness of a claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence, and that this nexus must be based on a novel element of the claim rather than something in the prior art. I also understand that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (such as motivation to combine with predictable results) that is sufficiently strong.

48. As discussed in Section V, the '903 patent is generally directed to a non-volatile, three-dimensional memory device. Fig. 31 of the '903 patent shows an embodiment. As shown in Fig. 31, **memory cells** arranged in the X-, Y-, and Z-directions—**memory cells** in the Z-direction form a **memory cell string** above a **conductive pillar**, which is formed on a **substrate**. '903 patent, 6:49-54, 11:17-41. Each **memory cell** includes a **conductive channel** and a **memory element**, where the **memory element** is formed in a **cavity** of a **control gate**. '903 patent, 11:17-41, Fig. 4, 4:49-5:3, 12:46-51.



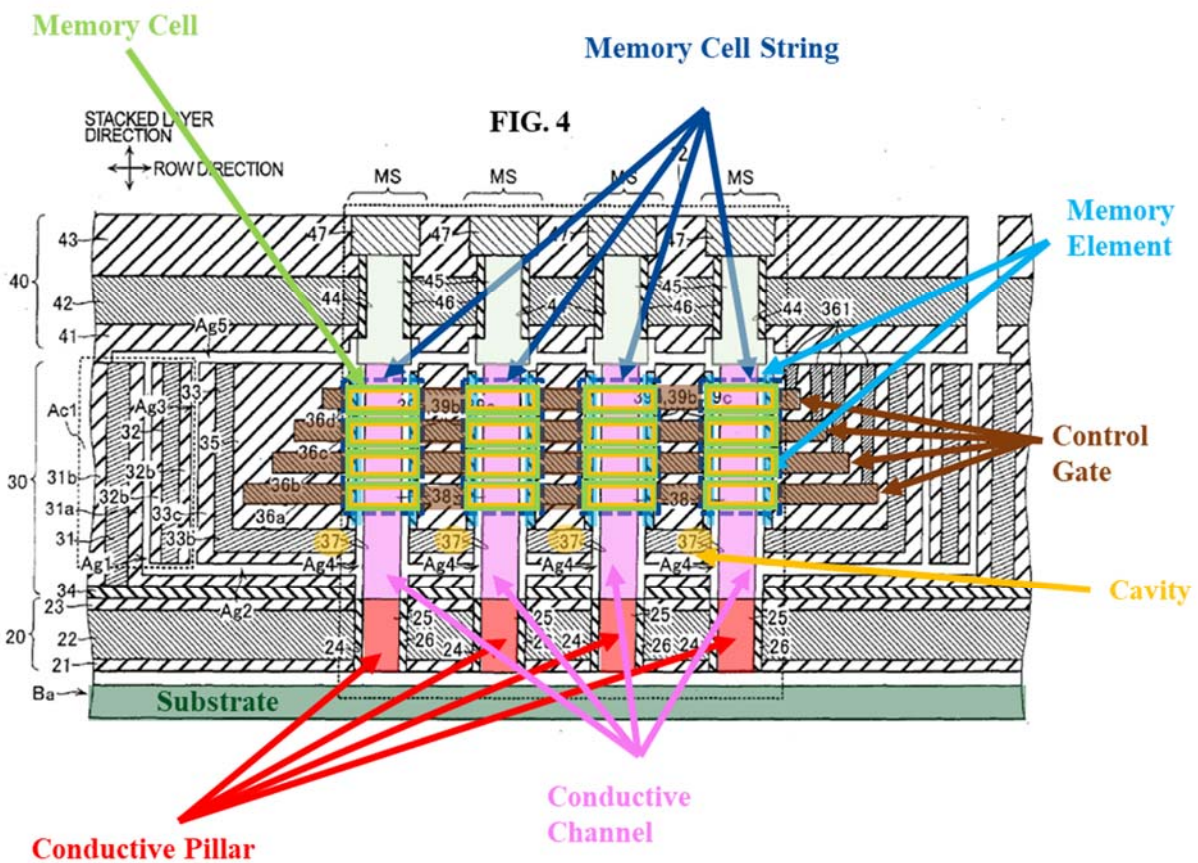
'903 patent, Fig. 31 (annotated).

49. Based on my experience in the field, however, such three-dimensional memory devices were well known in the art prior to the '903 patent's priority date.

50. For example, Ahn discloses a three-dimensional memory device, including **memory cells** arranged in a vertical direction, such that they form a **cell string** above **channel region (170)** formed on a **substrate 100**. Ahn, [0025]-[0028], Figure 1. Further, Ahn's **memory cells** include **channel region (260)** formed inside **through hole (230)** (*i.e.*, a cavity) such that it penetrates through **conductive layers (220)**, in addition to **a charge trap layer** (*i.e.*, a memory element) that is also formed inside **through hole (230)**. Ahn, [0037], [0040], [0043].

memory cell **MTr1mn-MTr4mn** includes a **memory 38** (i.e., a conductive channel) formed in a **memory hole 37** (i.e., a cavity) that penetrates through **word line conduction layers 36a-d** (i.e., a control gate), in addition to **charge storage layer 39b** (i.e., a memory element) that is also formed inside **memory hole 37**.

Fukuzumi, [0103]-[0104].



Fukuzumi, Fig. 4 (annotated).

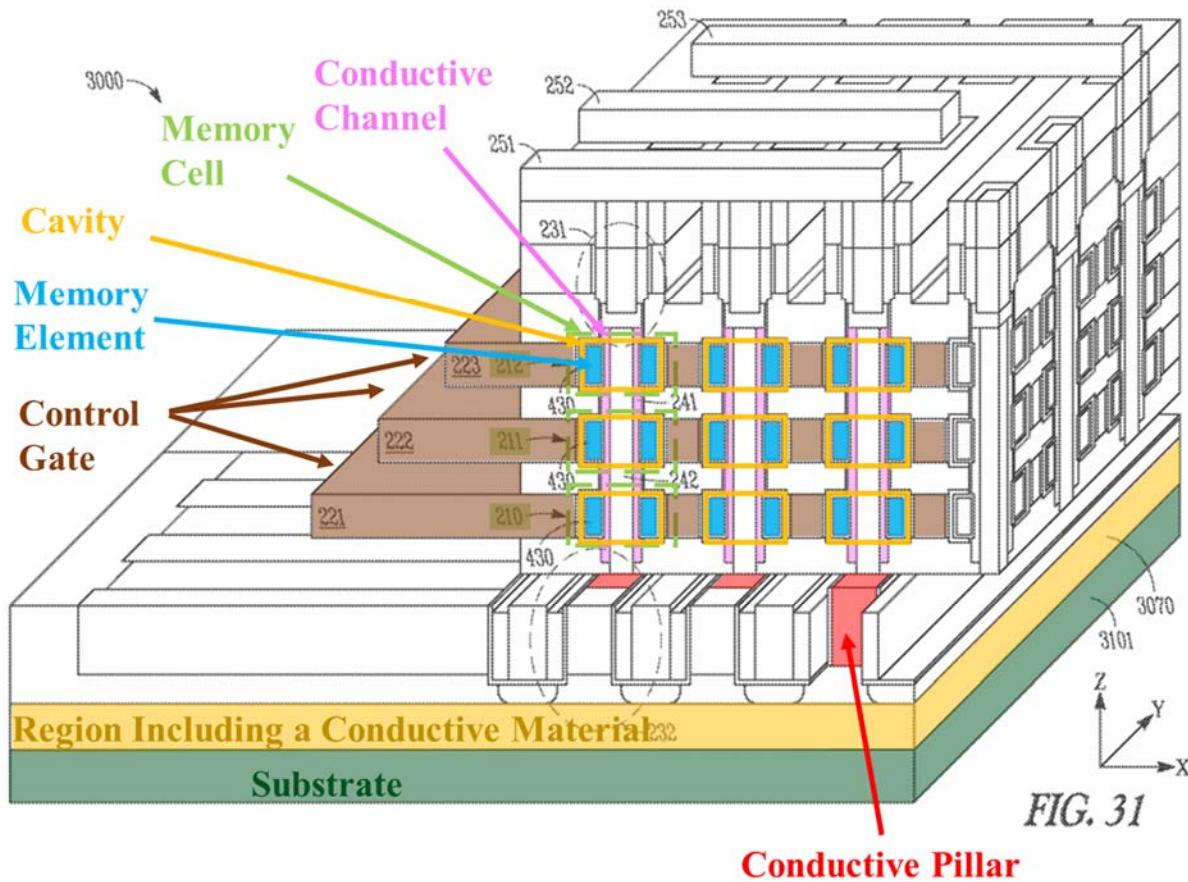
V. THE '903 PATENT

A. '903 Patent Overview

52. The Challenged Claims recite a three-dimensional memory device and

components within the device. '903 patent, 1:66-2:1. For example, claim 1 of the '903 patent recites an apparatus that includes “conductive pillars extending outward from a substrate,” “memory cell strings” formed over the conductive pillars, “a first control gate” and “a second control gate” formed in a first and second “device level,” respectively, “memory element[s]” formed in a cavity of those control gates, and “a conductive channel extending between the first memory cell and the second memory cell and electrically coupled to a conductive pillar of the conductive pillars.”

53. Fig. 31 shown below provides an embodiment of a memory device:



'903 patent, Fig. 31 (annotated).

54. The memory device of Fig. 31 comprises **memory cells 210-212** formed as a string in the Z-direction, where **channels 241** extend vertically in the Z-direction and through ring-shaped **memory elements 430** of **memory cells 210-212**. '903 patent, Fig. 31, 11:24-41. **Memory elements 430**, formed in **cavities** of **control gates 221-223**, store charges of the **memory cells 210-212**. '903 patent, 5:4-19, 8:4-26, 12:46-51. **Common source 3070**, located beneath **pillars**, is formed by injecting p-type impurities into a top portion of **substrate 3101**. '903 patent, 10:63-65, 11:51-61, 11:26-30, 11:47-12:34.

55. **Pillars** (e.g., pillar 705) are further illustrated in Fig. 9, which shows the **pillars** arranged in a matrix in the X- and Y-direction. '903 patent, Fig. 9, 3:36-38, 6:11-24, 6:45-49, 11:27-34, 12:10-22. As shown above in Fig. 31, such **Pillars** are coupled to and located below **channels 241**. '903 patent, Fig. 31, 9:4-24.

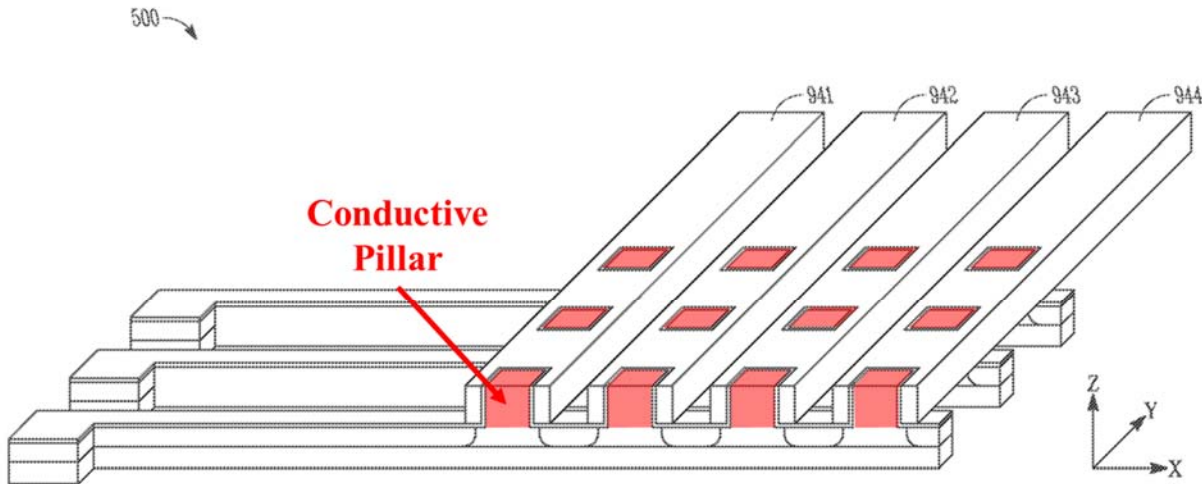


FIG. 9

Fukuzumi, Fig. 9 (annotated).

B. The Prosecution History

56. In formulating my opinions, I considered the contents of the prosecution history of the '903 patent, a copy of which I understand has been designated as Exhibit 1002. During prosecution of U.S. Patent Application No. 16/716,177, which matured into the '903 patent, the Examiner rejected the original claims on the ground of non-statutory obviousness-type double patenting over U.S. Patent No. 9,780,115. Ex. 1002, 169-179. In response, Applicant cancelled all

original claims and added the Challenged Claims that newly included recitations of (1) memory cell strings formed over the “conductive pillar extending outward from a substrate”; and (2) “a first data line coupled to the first and second memory cell strings” and “a second data line coupled to the third and fourth memory cell strings.” Ex. 1002, 207-212; *compare* Ex. 1002 (“’903FH), 46-50, *with id.*, 207-212. The Examiner allowed the resulting claims. Ex. 1002, 213-221.

VI. LEVEL OF ORDINARY SKILL IN THE ART

57. In rendering the opinions set forth in this declaration, I was asked to consider the patent claims and the prior art through the eyes of a person having ordinary skill in the art at the time of the alleged invention. I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field, the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a person having ordinary skill in the art is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a person having ordinary skill in the art would also have knowledge from the teachings of the prior art including the art cited below.

58. I have been asked to assume that the Challenged Claims are entitled to the priority date of June 28, 2010. Upon consideration of the relevant factors listed

above, in my opinion, on or before the priority date, a person of ordinary skill in the art, at the time the application that matured into the '903 patent was filed, would have had a Bachelor's degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. A higher level of education might make up for less experience, and vice versa.

59. Well before June 28, 2010, my level of skill in the art was at least that of a person having ordinary skill. I am qualified to opine concerning what a person having ordinary skill in the art would have known and understood at the time of the '903 patent's purported invention. My analysis and conclusions herein are from the perspective of a person having ordinary skill in the art as of June 28, 2010. A different priority date would not change my opinions as long as the identified prior art were still prior art.

VII. CLAIM CONSTRUCTION

60. I have been instructed that the Challenged Claims 1-3, 5, 7-9, 17-20 of the '903 patent are to be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of the alleged invention in light of the specification and the prosecution history pertaining to the patent, except as provided below. I have followed these principles in my analysis set forth in this document. I reserve the right to supplement my opinions in this declaration

to the extent that any parties later propose claim constructions for any claim terms in the '903 patent.

A. “cavity” of the “control gate” ([1.c]-[1.d], [17.l]-[17.o])

61. I understand that in the YMTC Litigation, Petitioner proposes that “[first-fourth] cavity of [first/second] control gate” should be construed as “a [first-fourth] hole with a larger diameter than holes in the layers immediately above and below the [first/second] control gate.” (“Petitioner’s Construction”). Ex. 1014, Appendix B at 10-11. I also understand that Patent Owner asserts that those terms should be given their plain and ordinary meaning, without specifying what it believes the plain and ordinary meaning is (“PO’s Construction”). *Id.* For the purposes of this declaration, I was instructed to evaluate the prior art under both constructions. As I explain below, both under Patent Owner’s Construction (see, e.g., Grounds 1-4) and Petitioner’s construction (see, e.g., Grounds 3-4), the Challenges Claims are either anticipated and/or rendered obvious by the prior art. See Section IX; Ex. 1014, Appendix B at 10-11.

VIII. GROUNDS OF UNPATENTABILITY

62. As I explain above in Section IV, the three-dimensional memory device claimed in the Challenged Claims was well-known in the art.

63. In this section, I will explain why the teachings or combinations of teachings from the following references anticipate and/or render obvious each of the Challenged Claims:

Name	Ex.	Publication/ Patent No.	Published/ Issued
Ahn	1004 & 1005	KR10-2010-0034612	4/1/2010
Fukuzumi	1006	U.S. 2009/0146190	6/11/2009
Ishikawa	1007	U.S. 2009/0283819	11/19/2009

I have been instructed to assume that each of these references qualifies as prior art.

64. As I explain below, the Challenged Claims are invalid based upon the following prior art grounds:

- **Ground 1:** Challenged Claims 1-3, 5, 7-9, and 17-20 of the '903 patent are anticipated and rendered obvious by Ahn.
- **Ground 2:** Challenged Claims 7 and 17 of the '903 patent are rendered obvious by Ahn in view of Ishikawa.
- **Ground 3:** Challenged Claims 1-3, 7, 9, 17, 19, and 20 of the '903 patent are anticipated and rendered obvious by Fukuzumi.
- **Ground 4:** Challenged Claims 5, 8, and 18 of the '903 patent are rendered obvious by Fukuzumi in view of Ahn.

IX. SPECIFIC GROUNDS FOR CHALLENGE

65. It is my opinion that Challenged Claims 1-3, 5, 7-9, and 17-20 of the '903 patent are unpatentable as explained below. As I explain above in Section IV, although the '903 patent discloses a three-dimensional memory device with conductive pillars, memory cell strings, control gates, and conductive channels,

such devices were well-known in the art. As described below, the cited prior art provides these teachings.

66. In this section, I explain why claims 1-3, 5, 7-9, and 17-20 of the '903 patent are anticipated and rendered obvious by the teachings of Ahn (Ex. 1004), why claims 7 and 17 are rendered obvious by the teachings of Ahn in view of Ishikawa (Ex. 1007), why claims 1-3, 7, 9, 17, 19, and 20 are anticipated and rendered obvious by the teachings of Fukuzumi (Ex. 1006), and why claims 5, 8, and 18 are rendered obvious by the teachings of Fukuzumi in view of Ahn.

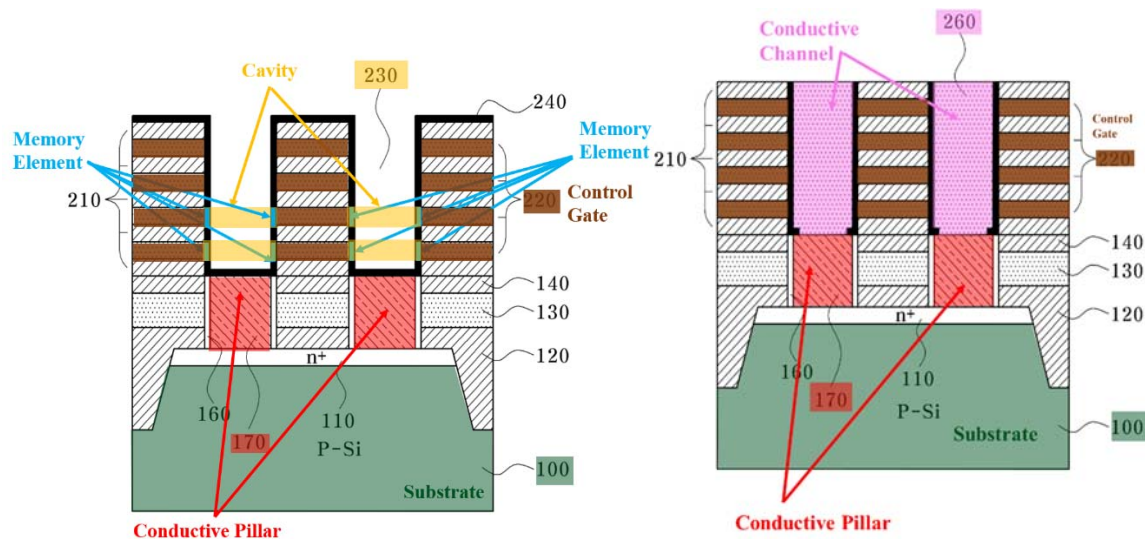
67. I note that, in this discussion, I may focus on the particular language in specific claims, but it should be understood that my analysis applies to the corresponding limitations of all claims containing identical or substantially identical language.

A. GROUND 1: Ahn (Claims 1-3, 5, 7-9, 17-20)

1. Overview of Ahn

68. Ahn is generally directed to a three-dimensional memory device that includes memory cells that store data and from which data can be erased. Ahn, [0002], [0022], [0038]. Figure 1 shows an embodiment:

holes (230) expose channel region (170) at their bottom, in addition to a charge trap layer (i.e., a memory element) “formed on the inner wall” of through hole (230) in each conductive layer (220). Ahn, [0036]-[0040]. The through holes (230) expose channel region (170) and are filled to form channel region (260) (i.e., a conductive channel) of the memory cells. Ahn, [0043].



Ahn, Fig. 7 and Fig. 9 (annotated).

2. Invalidity of Claims 1-3, 5, 7-9, and 17-20 Over Ahn

71. As I discuss below, it is my opinion that Claims 1-3, 5, 7-9, and 17-20 are anticipated and rendered obvious by Ahn, at least under Patent Owner’s construction of the “cavity” limitations.

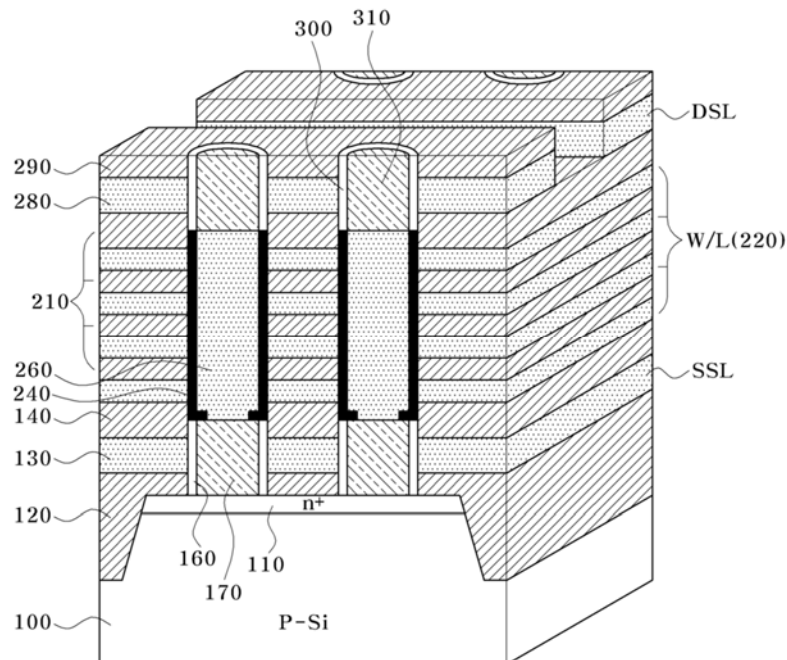
72. In addition to my discussion in Section IX.A.1, the following discussion identifies example disclosures followed by bulleted excerpts that disclose Claims 1-3, 5, 7-9, and 17-20.

a. Element [1.pre]

73. Element [1.pre] recites “An apparatus comprising.” To the extent the preamble is limiting, this element is met by Ahn.

74. Ahn discloses an apparatus (*e.g.*, “a flash memory device having a three-dimensional structure”). *See, e.g.*, Ahn:

- Figure 1



- [0001]: “The present invention relates to a method for manufacturing **a flash memory device**, and more particularly, to a method for manufacturing **a flash memory device having a three-dimensional structure**.”
- [0007]: “In order to fulfill the above technical tasks, a method for manufacturing **a flash memory device** according to the present invention is characterized by including a step of forming a source region on a substrate, a step of forming a source select transistor connected to the source region on the substrate, a step of forming gates of a plurality of memory cells by alternately forming insulating layers and conductive layers multiple times on a substrate on which a source select transistor is formed, a step of forming a through hole by etching the insulating layer

and the conductive layer to expose the channel region of the source select transistor, a step of forming a charge storage region consisting of a tunneling layer, a charge trap layer, and a blocking layer on the inner wall of the through hole, a step of forming a protective film on the inner sidewall of a through hole in which a charge storage region is formed, a step of exposing a channel region of a source select transistor, a step of forming a channel region of a cell transistor by filling the through hole with a semiconductor layer, and a step of forming a drain select transistor on the cell transistor.”

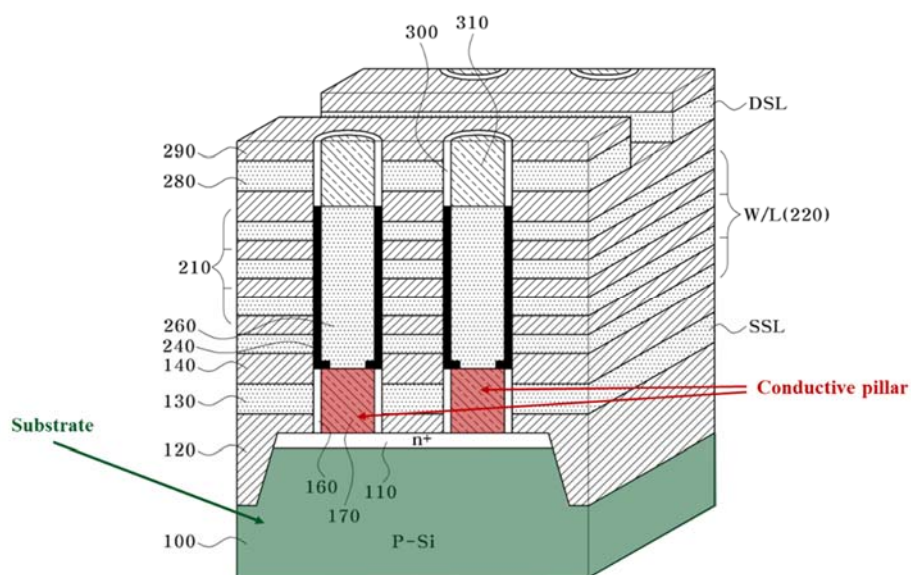
75. Ahn discloses a “a flash memory device having a three-dimensional structure.” Ahn, [0001].

b. Element [1.a]

76. **Element [1.a] recites “conductive pillars extending outward from a substrate.”** This element is met by Ahn.

77. Ahn discloses conductive pillars (*e.g.*, “channel region (170)”) extending outward from a substrate (*e.g.*, “substrate (100)”). *See, e.g.*, Ahn:

- Figure 1 (annotated)



- [0026] “**A source select transistor**, a plurality of memory cells, and a drain select transistor are **arranged vertically on a substrate (100) to form one cell string, and a plurality of such cell strings are arranged on the substrate (100).**”
- [0027]: “The source select transistor consists of a gate conductive layer (130) formed on a substrate (100) to be separated by insulating layers (120, 140), a gate insulating layer (16) formed on the inner wall of a through hole penetrating the above gate conductive layer (130) and the insulating layers (120, 140), and **a channel region (170) formed to fill the through hole in which the above gate insulating layer is formed. The channel region is connected to a source (110) formed on the substrate. The above channel region (170) is formed of a silicon epitaxial layer, or has a structure in which a silicon epitaxial layer and a polysilicon film are sequentially stacked** from the sidewall of the gate insulating layer within the above through hole.”
- [0032] “Referring to Figure 3, a conductive layer (130) for forming a gate of a select transistor is sequentially formed on a substrate on which an insulating film (120) is formed, and an insulating layer (140) for separating the conductive layer above and the conductive layer formed thereon is sequentially formed. The above conductive layer (130) can be formed with a thickness of 10 to 1,000 Å using polysilicon film doped with impurities, a metal such as tungsten (W), or another conductive material.”
- [0033] “Next, the above conductive layer (130) and the insulating layer (140) in the region where the channel of the source select transistor is to be formed are etched to form a hole (150) that exposes the impurity layer (110) formed on the above substrate (100). **The above hole (150) is a region in which a channel of a source select transistor is formed**, and is formed to have a diameter of 10 to 1,000 Å. The etching process for forming a hole (150) can be performed using wet etching, dry etching, or a mixed method thereof.”
- [0035] “**Next, the interior of the hole where the gate insulating film (160) is formed is filled with a semiconductor layer such as single crystal silicon (Si). The above semiconductor layer can be formed by using, for example, a selective epitaxial growth (SEG) method, such that a silicon (Si) film is selectively grown from the above impurity**

layer (110) in a gas atmosphere containing silicon (Si), and becomes a channel region (170) of the select transistor. Like this, a source select transistor is formed, which consists of a channel region (170), a gate insulating film (160), and a conductive layer (130) as a gate electrode.”

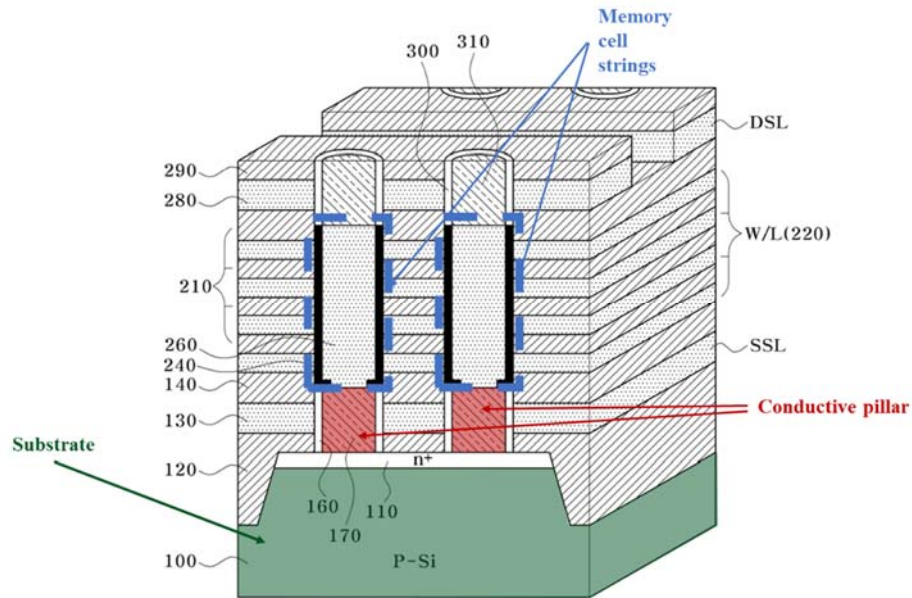
78. Ahn discloses channel region (170). Ahn, [0027]. This channel region (170) is formed on the substrate (100). Ahn, [0027], [0035], Fig. 1.

c. Element [1.b]

79. **Element [1.b] recites “memory cell strings, each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars.”** This element is met by Ahn.

80. Ahn discloses memory cell strings (*e.g.*, “memory cells” of “cell strings”), each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars (*e.g.*, “arranged vertically” over “channel region (170)”). *See, e.g.*, Ahn:

- Figure 1 (annotated)



- [0025]: “Referring to Figure 1, a flash memory device having a three-dimensional structure according to one embodiment of the present invention includes a source select transistor formed on a substrate (100), **gate stacks (220) formed on the above source select transistor and repeatedly stacked to be separated by an insulating layer (210), a charge storage region (240) formed by a blocking layer, a charge trap layer, and a tunneling layer formed on a sidewall of a through hole penetrating the above gate stacks, memory cells formed by a channel region (260) formed to fill the above through hole,** and a drain select transistor formed to be connected to the above memory cells.”
- [0026]: “A source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string, and a plurality of such cell strings are arranged on the substrate (100).”
- [0036]: “...on the resulting structure in which the source select transistor is formed, an interlayer insulating film (210) and a conductive layer (220) are repeatedly deposited several times. ...The above conductive layer (220) can be repeatedly stacked as many times as the number of memory cells connected to one cell string, for example, 2 times, 4 times, 8 times, ... up to 1,000 times. **The above conductive layer (220) serves as a control gate of the memory cell,** and the interlayer

insulating film (210) serves to separate the vertically-stacked memory cells.”

- [0037]: “...after stacking the conductive layers (220) and interlayer insulating films (210) as many times as the number of memory cells connected to the cell string, a through hole (230) is formed to form an ONO film for the channel of the cell transistor and charge storage.”
- [0038]: “an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (230).”
- [0042]: “***In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, charge trap layer, and blocking layer at the bottom of the through hole are etched to expose the channel region (170) of the source select transistor.***”
- [0043]: “***...a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of the cell transistor.*** The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities.”

81. See my discussion of element [1.a] above in Section IX.A.2.b.

82. Ahn further discloses “a plurality of cell strings,” where each such cell string includes “[a] source select transistor, a plurality of memory cells, and a drain select transistor.” Ahn, [0026]. Ahn further discloses that channel region (260) of the memory cells is formed on channel region (170) of the source select transistor. Ahn, [0026], [0042]-[0043].

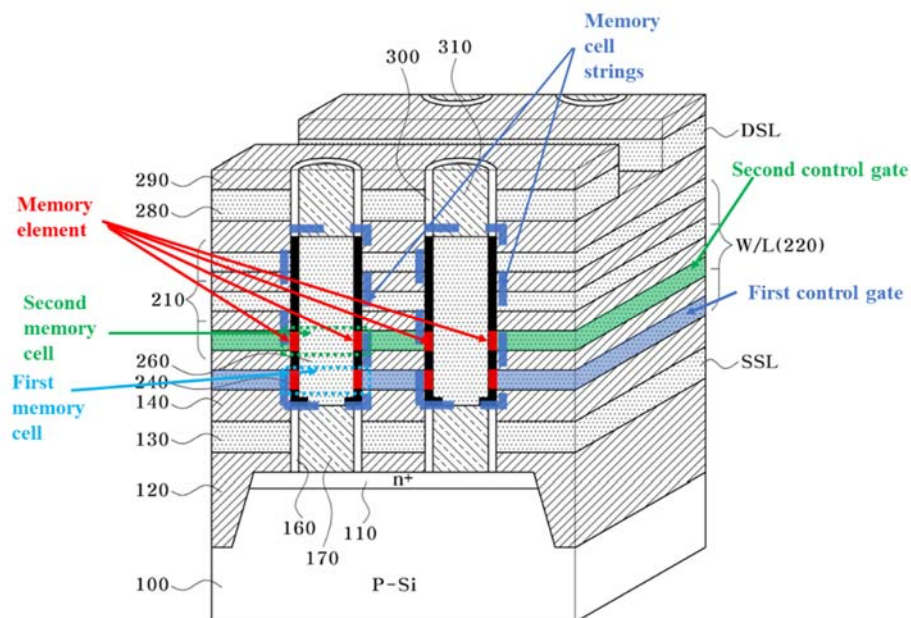
d. Element [1.c]

83. **Element [1.c] recites “a first control gate formed in a first device**

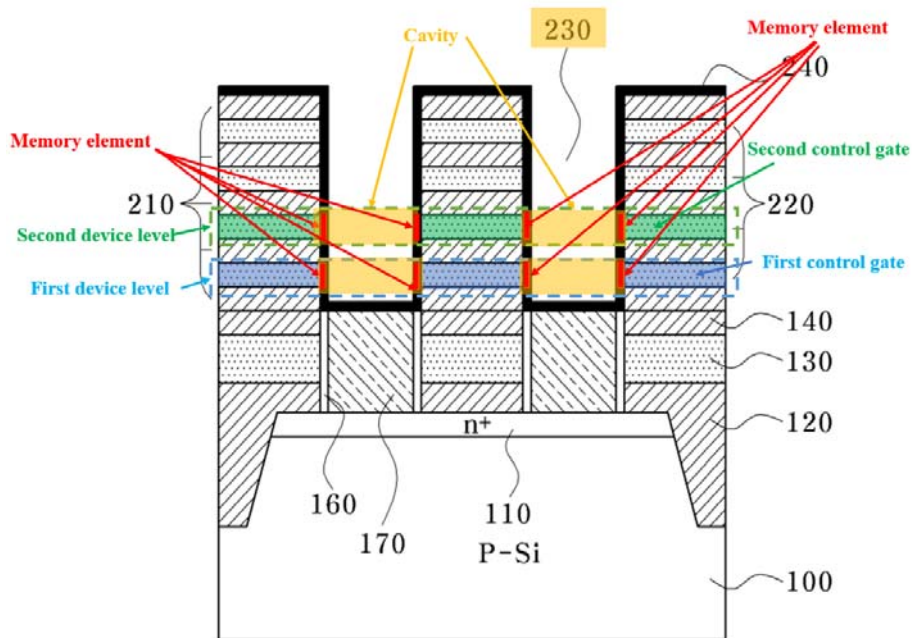
level, the memory cell strings including a memory cell string, the memory cell string including a first memory cell having a memory element formed in a cavity of the first control gate.” This element is met by Ahn.

84. Ahn discloses a first control gate formed in a first device level (*e.g.*, lowest “conductive layer (220)”), the memory cell strings (*e.g.*, “memory cells” of “cell strings”) including a memory cell string, the memory cell string including a first memory cell (*e.g.*, “memory cell” at the lowest “conductive layer (220)” in Fig. 1) having a memory element (*e.g.*, “charge trap layer”) formed in a cavity (*e.g.*, “through hole (230)”) of the first control gate. *See, e.g.*, Ahn:

- Figure 1 (annotated)



- Figure 7 (annotated)



- [0026]: “A source select transistor, **a plurality of memory cells**, and a drain select transistor are arranged vertically on a substrate (100) to **form one cell string**, and a plurality of such cell strings are arranged on the substrate (100).”
- [0028]: “The **gate stack (220) constituting the above memory cell is repeatedly stacked as many times as the number of memory cells connected to one cell string**. The memory cells connected to one cell string are separated by an insulating layer (210), and the memory cells arranged in the same layer constitute one page.”
- [0036]: “...on the resulting structure in which the source select transistor is formed, **an interlayer insulating film (210) and a conductive layer (220) are repeatedly deposited several times**. ...The above conductive layer (220) can be repeatedly stacked as many times as the number of memory cells connected to one cell string, for example, 2 times, 4 times, 8 times, ... up to 1,000 times. **The above conductive layer (220) serves as a control gate of the memory cell**, and the interlayer insulating film (210) serves to separate the vertically-stacked memory cells.”
- [0037]: “Referring to Figure 6, after **stacking the conductive layers (220) and interlayer insulating films (210) as many times as the number of memory cells connected to the cell string**, a through hole (230) is

formed to form an ONO film for the channel of the cell transistor and charge storage. Specifically, the alternately-stacked conductive layers (210) and interlayer insulating films (220) are anisotropically etched so that the gate insulating film (160) and channel region (170) of the source select transistor are exposed. At this time, the etching process can use a wet or dry etching method, and the size of the through hole (230) is formed to a size that can be gap-filled with a semiconductor layer that acts as a channel of the cell transistor and an ONO film that acts as a charge storage film. In this embodiment, the above through hole (230) was formed with a diameter of 10 to 1,000 Å.”

- [0038]: “**an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (230).**”
- [0040]: “Next, **a charge trap layer is formed** by depositing, for example, a silicon nitride film or a polysilicon film to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (230). The charge trap layer can be deposited using atomic layer deposition (ALD) or chemical vapor deposition (CVD). An oxide film is deposited on the charge trap layer on the inner wall of the through hole (230) to a thickness of 10 to 1,000 Å to form a tunneling layer of the memory cell. When forming the above tunneling layer, it is possible to form an oxygen nitride film (SiON) by performing the process in an atmosphere containing both oxygen and nitrogen. In addition, the film quality of the tunneling layer can be improved by heat-treating in an NO gas or N₂O gas atmosphere after forming the tunneling layer.”
- [0042]: “In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, **charge trap layer**, and blocking layer at the bottom of the through hole are etched to expose the channel region (170) of the source select transistor. As a protective film (250) having an etching selectivity with respect to the above dielectric layer is formed on the side of the ONO dielectric layer (240), etching or etching damage to the dielectric layer does not occur during the etching process for the dielectric layer.”
- [0043]: “...**a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of**

the cell transistor. The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities.”

85. See my discussion of element [1.b] above in Section IX.A.2.c.

86. Further, Ahn’s conductive layer (220) is a “control gate of the memory cell.” Ahn, [0036]. Ahn also discloses through hole (230) passing through conductive layers (220) and a charge trap layer, where the charge trap layer is “formed on the inner wall” of “through hole (230).” Ahn, [0037]-[0038]. Gate stack or conductive layer (220) “constituting the [] memory cell is repeatedly stacked as many times as the number of memory cells connected to one cell string” and the lowest conductive layer (220) combined with the charge trap layer (as shown in Figure 1) forms a first memory cell. Ahn, [0028], [0036], [0040].

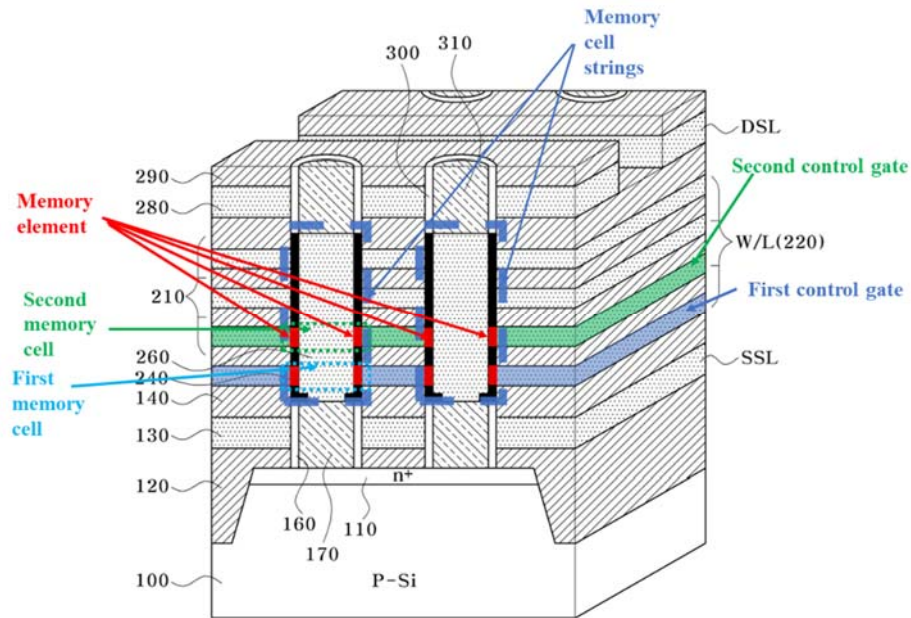
e. Element [1.d]

87. **Element [1.d] recites “a second control gate formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the second control gate.”** This element is met by Ahn.

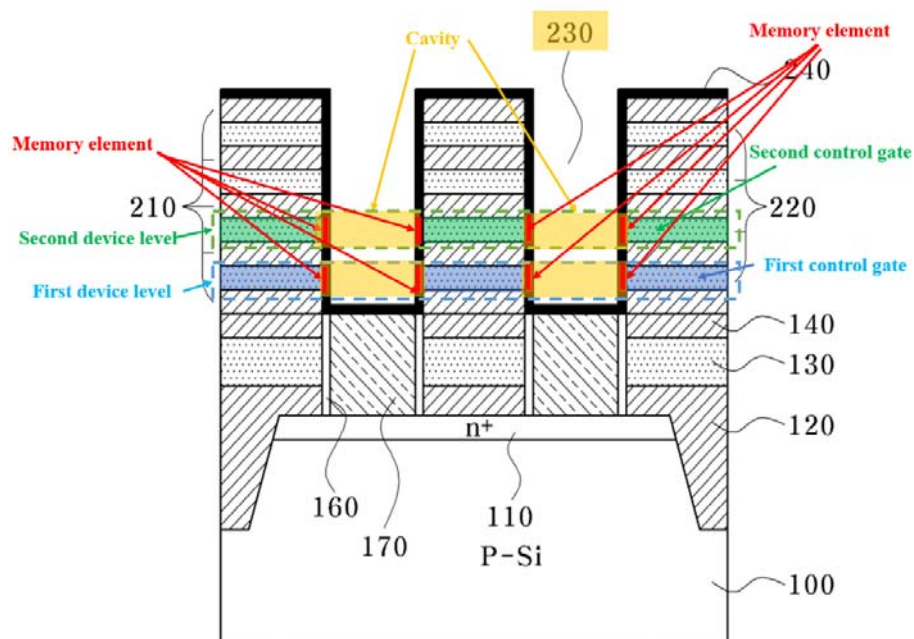
88. Ahn discloses a second control gate formed in a second device level (*e.g.*, second lowest “conductive layer (220)”), the memory cell string (*e.g.*, “cell string”) including a memory cell string, the memory cell string including a second memory cell (*e.g.*, “memory cell” at the second lowest “conductive layer (220) in

Fig. 1) having a memory element (e.g., “charge trap layer”) formed in a cavity (e.g., “through hole (230)”) of the second control gate. See, e.g., Ahn:

- Figure 1 (annotated)



- Figure 7 (annotated)



- [0026]: “A source select transistor, **a plurality of memory cells**, and a drain select transistor are arranged vertically on a substrate (100) **to form one cell string**, and a plurality of such cell strings are arranged on the substrate (100).”
- [0028]: “The **gate stack (220) constituting the above memory cell is repeatedly stacked as many times as the number of memory cells connected to one cell string**. The memory cells connected to one cell string are separated by an insulating layer (210), and the memory cells arranged in the same layer constitute one page.”
- [0036]: “...on the resulting structure in which the source select transistor is formed, **an interlayer insulating film (210) and a conductive layer (220) are repeatedly deposited several times**. ...The above conductive layer (220) can be repeatedly stacked as many times as the number of memory cells connected to one cell string, for example, 2 times, 4 times, 8 times, ... up to 1,000 times. **The above conductive layer (220) serves as a control gate of the memory cell**, and the interlayer insulating film (210) serves to separate the vertically-stacked memory cells.”
- [0037]: “Referring to Figure 6, after **stacking the conductive layers (220) and interlayer insulating films (210) as many times as the number of memory cells connected to the cell string**, **a through hole (230) is formed to form an ONO film for the channel of the cell transistor and charge storage**. Specifically, the alternately-stacked conductive layers (210) and interlayer insulating films (220) are anisotropically etched so that the gate insulating film (160) and channel region (170) of the source select transistor are exposed. At this time, the etching process can use a wet or dry etching method, and the size of the through hole (230) is formed to a size that can be gap-filled with a semiconductor layer that acts as a channel of the cell transistor and an ONO film that acts as a charge storage film. In this embodiment, the above through hole (230) was formed with a diameter of 10 to 1,000 Å.”
- [0038]: “**an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (230)**.”
- [0040]: “Next, **a charge trap layer is formed** by depositing, for example, a silicon nitride film or a polysilicon film to a thickness of 10 to 1,000 Å

on the blocking layer formed on the inner wall of the through hole (230). The charge trap layer can be deposited using atomic layer deposition (ALD) or chemical vapor deposition (CVD). An oxide film is deposited on the charge trap layer on the inner wall of the through hole (230) to a thickness of 10 to 1,000 Å to form a tunneling layer of the memory cell. When forming the above tunneling layer, it is possible to form an oxygen nitride film (SiON) by performing the process in an atmosphere containing both oxygen and nitrogen. In addition, the film quality of the tunneling layer can be improved by heat-treating in an NO gas or N₂O gas atmosphere after forming the tunneling layer.”

- [0042]: “In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, **charge trap layer**, and blocking layer at the bottom of the through hole are etched to expose the channel region (170) of the source select transistor. As a protective film (250) having an etching selectivity with respect to the above dielectric layer is formed on the side of the ONO dielectric layer (240), etching or etching damage to the dielectric layer does not occur during the etching process for the dielectric layer.”
- [0043]: “...***a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of the cell transistor.*** The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities.”

89. See my discussion of elements [1.b] and [1.c] above in Section

IX.A.2.c-d.

90. Further, Ahn’s second lowest conductive layer (220) combined with the charge trap layer (as shown in Figure 1) forms a second memory cell.

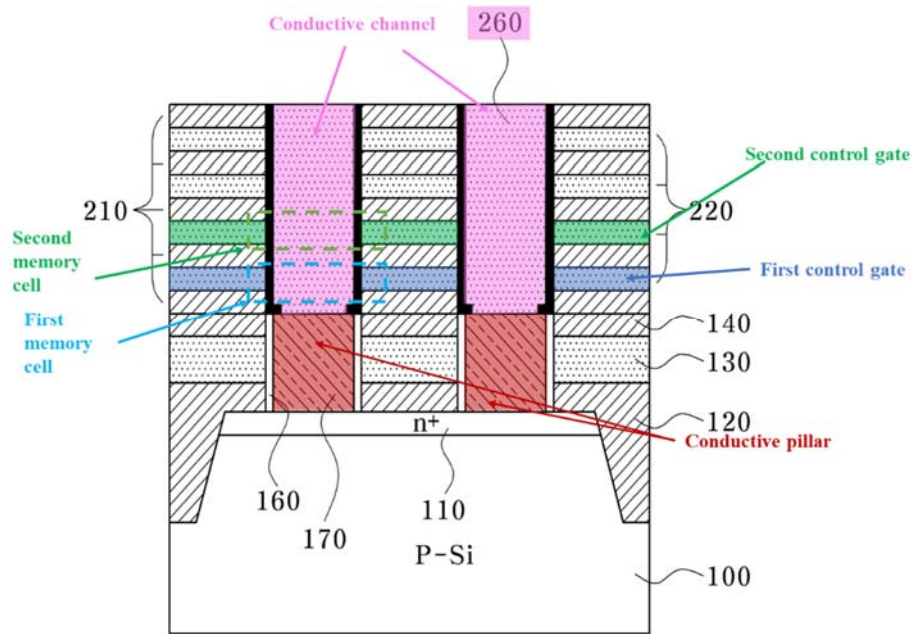
f. Element [1.e]

91. Element [1.e] recites “a conductive channel extending between the

first memory cell and the second memory cell and electrically coupled to a conductive pillar of the conductive pillars.” This element is met by Ahn.

- Figure 1 (annotated)%

- Figure 9 (annotated)_%



- [0025]: “Referring to Figure 1, a flash memory device having a three-dimensional structure according to one embodiment of the present invention includes a source select transistor formed on a substrate (100), **gate stacks (220) formed on the above source select transistor and repeatedly stacked to be separated by an insulating layer (210), a charge storage region (240) formed by a blocking layer, a charge trap layer, and a tunneling layer formed on a sidewall of a through hole penetrating the above gate stacks, memory cells formed by a channel region (260) formed to fill the above through hole, and a drain select transistor formed to be connected to the above memory cells.**”
- [0026]: “A source select transistor, **a plurality of memory cells**, and a drain select transistor are arranged vertically on a substrate (100) **to form one cell string**, and a plurality of such cell strings are arranged on the substrate (100).”
- [0028]: “The **gate stack (220) constituting the above memory cell is repeatedly stacked as many times as the number of memory cells connected to one cell string. The memory cells connected to one cell string** are separated by an insulating layer (210), and the memory cells arranged in the same layer constitute one page.”
- [0036]: “...**on the resulting structure in which the source select transistor is formed, an interlayer insulating film (210) and a conductive layer (220) are repeatedly deposited several times. ...The**

- above conductive layer (220) can be repeatedly stacked as many times as the number of memory cells connected to one cell string, for example, 2 times, 4 times, 8 times, ... up to 1,000 times. ***The above conductive layer (220) serves as a control gate of the memory cell***, and the interlayer insulating film (210) serves to separate the vertically-stacked memory cells.”
- [0037]: “Referring to Figure 6, after ***stacking the conductive layers (220) and interlayer insulating films (210) as many times as the number of memory cells connected to the cell string, a through hole (230) is formed to form an ONO film for the channel of the cell transistor and charge storage***. Specifically, the alternately-stacked conductive layers (210) and interlayer insulating films (220) are anisotropically etched so that the gate insulating film (160) and channel region (170) of the source select transistor are exposed. At this time, the etching process can use a wet or dry etching method, and the size of the through hole (230) is formed to a size that can be gap-filled with a semiconductor layer that acts as a channel of the cell transistor and an ONO film that acts as a charge storage film. In this embodiment, the above through hole (230) was formed with a diameter of 10 to 1,000 Å.”
 - [0038]: “***an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (230).***”
 - [0040]: “Next, ***a charge trap layer is formed*** by depositing, for example, a silicon nitride film or a polysilicon film to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (230). The charge trap layer can be deposited using atomic layer deposition (ALD) or chemical vapor deposition (CVD). An oxide film is deposited on the charge trap layer on the inner wall of the through hole (230) to a thickness of 10 to 1,000 Å to form a tunneling layer of the memory cell. When forming the above tunneling layer, it is possible to form an oxygen nitride film (SiON) by performing the process in an atmosphere containing both oxygen and nitrogen. In addition, the film quality of the tunneling layer can be improved by heat-treating in an NO gas or N₂O gas atmosphere after forming the tunneling layer.”
 - [0042]: “***In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, charge trap layer, and blocking layer at the***

bottom of the through hole are etched to expose the channel region (170) of the source select transistor.”

- [0043]: “***...a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of the cell transistor.*** The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities.”

93. See my discussion of elements [1.a]-[1.d] above in Section IX.A.2.b-

e.

94. Ahn further discloses channel region (260) that passes through conductive layers (220), where the channel region (260) connects the memory cells and is in direct contact with channel region (170). Ahn, [0025], [0037], [0042]-[0043], Fig. 1. Because the channel region (260) directly contacts channel region (170), charge can flow between the two, and thus the channel regions are electrically coupled to each other.

g. Element [2.a]

95. **Element [2.a] recites “The apparatus of claim 1, further comprising: a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material.”**

See my discussion of claim [1] above in Section IX.A.2.a-f. The added limitation of element [2.a] is met by **Ahn**.

96. Ahn discloses a first conductive region (*e.g.*, left portion of “gate

- [0034]: “...*a silicon oxide film is deposited on the side of the above hole to a thickness of, for example, 10 to 500 Å to form a gate insulating film (160) of a source select transistor.*”
- [0035]: “...*the interior of the hole where the gate insulating film (160) is formed is filled with a semiconductor layer such as single crystal silicon (Si). The above semiconductor layer ... becomes a channel region (170) of the select transistor.* Like this, a source select transistor is formed, which consists of a channel region (170), a gate insulating film (160), and a conductive layer (130) as a gate electrode.”

97. See my discussion of claim [1.a] above in Section IX.A.2.b.

98. Ahn further discloses channel region (170) that passes through gate conductive layer (130), resulting in a region of gate conductive layer (130) on, e.g., the left side of channel region (170). Ahn, [0033], [0035]. Ahn further discloses gate insulating film (160) formed between and separating gate conductive layer (130) and channel region (170). Ahn, [0034]. An insulating material is a dielectric material.

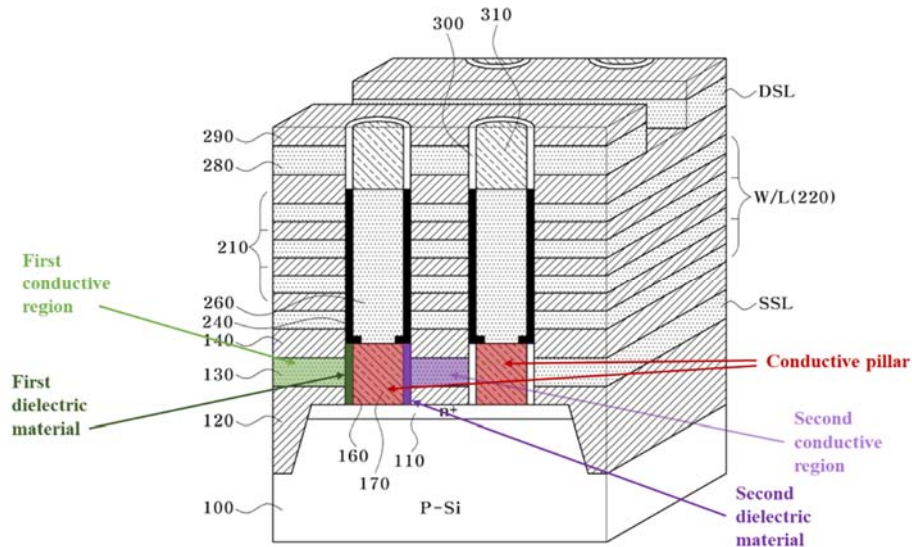
h. Element [2.b]

99. **Element [2.b] recite “a second conductive region located on a second side opposite from the first side of the conductive pillar and separated from the conductive pillar by a second dielectric material.”** This limitation is met by Ahn.

100. Ahn discloses a second conductive region (e.g., right portion of “gate conductive layer (130) in Fig. 1) located on a second side of the conductive pillar (e.g., on right side of “channel region (170)” in Fig. 1) and separated from the

conductive pillar by a second dielectric material (e.g., portion of “gate insulating layer (160)” on right side of “channel region (170)” in Fig. 1). See, e.g., Ahn:

- Figure 1 (annotated)



- [0032]: “Referring to Figure 3, **a conductive layer (130) for forming a gate of a select transistor is sequentially formed on a substrate on which an insulating film (120) is formed**, and an insulating layer (140) for separating the conductive layer above and the conductive layer formed thereon is sequentially formed. The above conductive layer (130) can be formed with a thickness of 10 to 1,000 Å using a polysilicon film doped with impurities, a metal such as tungsten (W), or another conductive material.”
- [0033]: “...the above conductive layer (130) and the insulating layer (140) in the region where the channel of the source select transistor is to be formed are etched to **form a hole (150) that exposes the impurity layer (110) formed on the above substrate (100). The above hole (150) is a region in which a channel of a source select transistor is formed....**”
- [0034]: “...**a silicon oxide film is deposited on the side of the above hole to a thickness of, for example, 10 to 500 Å to form a gate insulating film (160) of a source select transistor.**”

- [0035]: “...*the interior of the hole where the gate insulating film (160) is formed is filled with a semiconductor layer such as single crystal silicon (Si). The above semiconductor layer ... becomes a channel region (170) of the select transistor.*”

101. See my discussion of elements [1.e] and [2.a] above in Section IX.A.2.f-g.

102. Ahn further discloses a portion of gate conductive layer (130) on the right side of channel region (170), i.e., a second portion of gate conductive layer (130). See [2.a] (Section IX.A.2.g). Similarly, a second portion of gate insulating layer (160) on the right side of channel region (170) is a second dielectric material that separates channel region (170) and gate conductive layer (130). See [2.a] (IX.A.2.g).

103. I have reviewed Patent Owner’s Disclosure of Asserted Claims and Infringement Contentions and Document Production Accompanying Disclosure (Patent Local Rules 3-1 and 3-2) in the YMTC Litigation, which I understand has been designated as Exhibit 1018. Ex. 1018, Ex. D-2 at 6-8. My analysis above in ¶¶ 100-102 is consistent with Patent Owner’s assertion in its Infringement Contentions in that the first and second conductive regions and dielectric materials are located on opposite sides of the conductive pillar. For example, in its Infringement Contentions, Patent Owner points to a cross section of a source-select transistor and refers to a portion of a gate plane as a “First conductive region” and another portion of the same gate plane on the opposite side of the channel as a

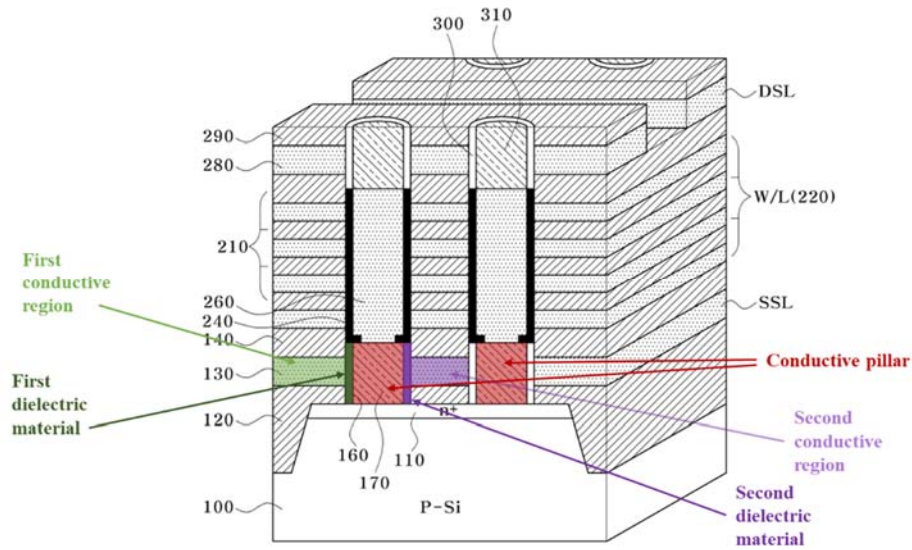
“Second conductive region.” Ex. 1018, Ex. D-2 at 6-8. Similarly, Patent Owner points to a portion of a dielectric material surrounding the channel of the source-select transistor as a “First dielectric material” and another portion of the same dielectric material on the opposite side of the channel as a “Second dielectric material.” *Id.*

i. Claim [3]

104. **Claim [3] recites “The apparatus of claim 2, wherein the first conductive region is coupled to the second conductive region.”** See my discussion of claim [2] above in Section IX.A.2.g-h. The added limitation of claim [3] is met by Ahn.

105. Ahn discloses the first conductive region (*e.g.*, left portion of “gate conductive layer (130)” in Fig. 1) is coupled to the second conductive region (*e.g.*, right portion of “gate conductive layer (130)” in Fig. 1). *See, e.g.*, Ahn:

- Figure 1 (annotated)



- [0032]: “Referring to Figure 3, **a conductive layer (130) for forming a gate of a select transistor is sequentially formed on a substrate on which an insulating film (120) is formed**, and an insulating layer (140) for separating the conductive layer above and the conductive layer formed thereon is sequentially formed. The above conductive layer (130) can be formed with a thickness of 10 to 1,000 Å using a polysilicon film doped with impurities, a metal such as tungsten (W), or another conductive material.”
- [0033]: “...the above conductive layer (130) and the insulating layer (140) in the region where the channel of the source select transistor is to be formed are etched to **form a hole (150) that exposes the impurity layer (110) formed on the above substrate (100)**. The above hole (150) is a region in which a channel of a source select transistor is formed....”
- [0034]: “...a silicon oxide film is deposited on the side of the above hole to a thickness of, for example, 10 to 500 Å to form a gate insulating film (160) of a source select transistor.”
- [0035]: “...the interior of the hole where the gate insulating film (160) is formed is filled with a semiconductor layer such as single crystal silicon (Si). The above semiconductor layer ... becomes a channel region (170) of the select transistor.”

106. See my discussion of element [2.a] and [2.b] above in Section

IX.A.2.g-h.

107. Ahn further discloses channel region (170) formed in hole (150) in gate conductive layer (130), where portions of gate conductive layer (130) on the left and right sides of channel region (170) are coupled to each other. Ahn, [0096]; Fig. 2.

108. I have reviewed Patent Owner's Disclosure of Asserted Claims and Infringement Contentions and Document Production Accompanying Disclosure (Patent Local Rules 3-1 and 3-2) in the YMTC Litigation. Ex. 1018, Ex. D-2 at 8-9. My analysis above in ¶¶ 105-107 is consistent with Patent Owner's assertion in its Infringement Contentions. For example, in its Infringement Contentions, Patent Owner points to a cross section of a source-select transistor and refers to a portion of a gate plane as a "First conductive region" and another portion of the same gate plane on the opposite side of the channel as a "Second conductive region." Ex. 1018, Ex. D-2 at 8-9. Patent Owner argues that those portions of the conductive region are coupled because the "conductive region around the conductive pillar also wrap around the conductive pillar," just like Ahn's "gate conductive layer (130)" wraps around "channel region (170)." *Id.*

j. Claim [5]

109. **Claim [5] recites "The apparatus of claim 2, wherein each of the first and second conductive regions comprises metal."** See my discussion of

claim [2] above in Section IX.A.2.g-h. The added limitation of claim [5] is met by Ahn.

110. Ahn discloses each of the first and second conductive regions (*e.g.*, left and right portions of “gate conductive layer (130)” in Fig. 1) comprises metal (*e.g.*, “tungsten”). *See, e.g.*, Ahn:

- [0032]: “a conductive layer (130) for forming a gate of a select transistor is sequentially formed on a substrate on which an insulating film (120) is formed, and an insulating layer (140) for separating the conductive layer above and the conductive layer formed thereon is sequentially formed. ***The above conductive layer (130) can be formed*** with a thickness of 10 to 1,000 Å ***using*** a polysilicon film doped with impurities, ***a metal such as tungsten (W)***, or another conductive material.

111. Ahn’s conductive layer (130) comprises tungsten. Ahn, [0032].

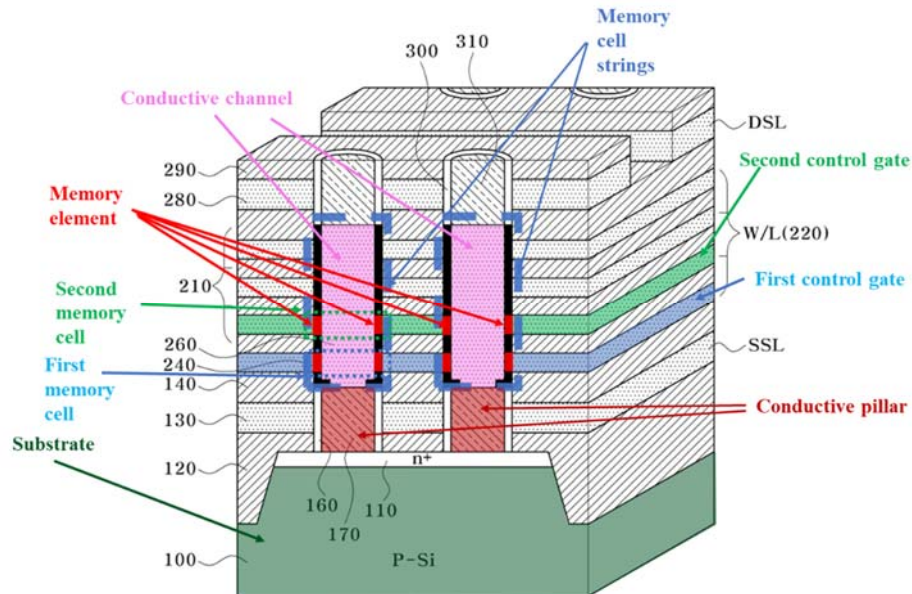
k. Claim [7]

112. **Claim [7] recites “The apparatus of claim 1, further comprising a data line coupled to the conductive channel, wherein the first and second memory cells are located between the data line and the substrate.”** See my discussion of claim [1] above in Section IX.A.2.a-f. The added limitation of claim [7] is met by Ahn.

113. A person of ordinary skill in the art would have understood that Ahn’s memory device includes a data line (*e.g.*, bit line completing circuit on drain side of “cell strings”) coupled to the conductive channel (*e.g.*, “channel region (260)” of cell transistors), wherein the first and second memory cells (*e.g.*, “memory cells” at

the lowest and second lowest “conductive layers (220)” in Fig. 1) are located between the data line and the substrate (e.g., “substrate (100)”). See, e.g., Ahn:

- Figure 1 (annotated)



- [0022]: “According to the present invention, ... by forming wells in vertically arranged memory cells, ***data in the memory cells can be simultaneously erased*** using the F-N tunneling method.”
- [0025]: “Referring to Figure 1, a flash memory device having a three-dimensional structure according to one embodiment of the present invention includes ***a source select transistor formed on a substrate (100), gate stacks (220) formed on the above source select transistor and repeatedly stacked to be separated by an insulating layer (210), a charge storage region (240) formed by a blocking layer, a charge trap layer, and a tunneling layer formed on a sidewall of a through hole penetrating the above gate stacks, memory cells formed by a channel region (260) formed to fill the above through hole, and a drain select transistor formed to be connected to the above memory cells.***”
- [0026]: “***A source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string***, and a plurality of such cell strings are arranged on the substrate (100).”

- [0037]: "... after stacking the conductive layers (220) and interlayer insulating films (210) as many time as the number of memory cells connected to the cell string, **a through hole (230) is formed to form an ONO film for the channel of the cell transistor and charge storage.** Specifically, the alternately-stacked conductive layers (210) and interlayer insulating films (220) are anisotropically etched so that the gate insulating film (160) and channel region (170) of the source select transistor are exposed...."
- [0038]: "**an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (230).**"
- [0042]: "**In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, charge trap layer, and blocking layer at the bottom of the through hole are etched to expose the channel region (170) of the source select transistor.**"
- [0043]: "...**a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of the cell transistor.** The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities."
- [0044]: "Referring to Figure 10, **a drain select transistor for string selection is formed on the resulting material in which a plurality of memory cells are formed.**"
- [0046]: "Next, **in order to connect the drain select transistor and the memory cell transistor, the conductive layer (280) and the insulating film (270, 290) are anisotropically etched to form a hole....**"
- [0048]: "Next, **in order to connect the channel region of the memory cell and the channel region of the drain select transistor, the gate insulating film (300) at the bottom of the hole is etched so that the channel region of the memory cell is exposed....**"
- [0049]: "**A semiconductor layer is formed on the resulting material in which the channel region of the memory cell is exposed so that the**

above hole is filled, thereby forming a channel region (310) of the drain select transistor....”

114. See my discussion of element [1.a]-[1.e] above in Section IX.A.2.b-f.

115. Furthermore, Ahn teaches data lines coupled to channel region (260). Ahn discloses that its device is a “flash memory.” Ahn, [0025]. A person of ordinary skill in the art would have understood flash memory includes bit lines connected to the memory cells that allow for the selection of memory cells as part of basic operations of the memory cell, such as read, write and erase.

116. For example, Ahn’s further discloses that its memory cells store and erase data in a charge trap layer. Ahn, [0022], [0038]. A person of ordinary skill in the art would have understood that bit lines perform the basic operation of providing current to store (i.e., write) and erase data. For instance, U.S. Patent Application Publication No. 2009/0242967 (“Katsumata”), which I understand has been designated as Exhibit 1011, discloses a three-dimensional non-volatile semiconductor storage device where “respective voltages of the bit lines BL1 to BL3, the drain-side selection gate lines SGD, the word lines WL1 to WL4, the source-side selection gate line SGS, and the source lines SL are controlled by bit line driving circuits,[] the drain-side selection gate line driving circuit 15, the word line driving circuits 13, the source-side selection gate line driving circuit 14, and a

source line driving circuit” such that “data is written and erased by controlling charges of the charge accumulation layer in a predetermined memory transistor MTrmn.” Ex.1011, [0055]. Similarly, U.S. Patent No. 5,596,523 (“Endoh”), which I understand has been designated as Exhibit 1008, discloses that “[a] NAND cell type EEPROM is one of the most typical non-volatile semiconductor memory devices of the above type” and that “[b]y causing the select transistor to turn on, the NAND cell unit may be selectively coupled to a corresponding data transfer line associated therewith, which is called the ‘bit line.’” See Ex. 1008, 1:44-51. Endoh further discloses that “[a] logic ‘1’ or ‘0,’ which is supplied by the bit line associated with the subject NAND cell unit, is selectively programmed in the target memory cell.” See Ex. 1008, 1:44-60. Further, U.S. Patent No. 6,765,825 (“Scott”), which I understand has been designated as Exhibit 1009, discloses that “[t]he floating gate transistor of each EEPROM memory cell is coupled to a unique combination of word and bit lines” and that “[i]n order to read a bit of information stored on a particular EEPROM memory cell, the associated bit line is raised above ground at the same time as the associated word line.” See Ex. 1009, 1:65-2:9, 2:38-46, Fig. 5.

117. A person of ordinary skill in the art would have further understood that the bit line is conventionally located above (*i.e.*, further away from the substrate) channel region (310) of the drain select transistor such that the first and

second memory cells are located between the data line and the substrate.

Consistent with Figure 1 of Ahn, which shows the memory structure up to the drain select transistor, Ahn provides a detailed manufacturing process from the substrate to the drain select transistor. Ahn, [0031]-[0049]. Accordingly, a person of ordinary skill in the art would have understood that the bit lines are located above the drain select transistors, formed after the memory device up to the drain select transistors as illustrated in Figure 1 of Ahn are formed.

118. At the very least, a person of ordinary skill in the art would have found it obvious to form bit lines above (e.g. on top of) the components explicitly taught by Ahn. This would obviate any modification of the manufacturing process or memory structure described in Ahn. In this regard, it was well known to place bit lines in 3D flash memory such that the memory cells are located between the bit lines and substrate. For example, U.S. Patent Application Publication No. 2010/0240205 (“Son”), which I understand has been designated as Exhibit 1010, discloses a “nonvolatile memory device [that] includes a plurality of strings STRs between the bit lines BL1 to BL4 and the common source line CSL.” Ex. 1010, [0039], [0053]. Similarly, Katsumata further discloses “four memory transistors MTr1 mn to MTr4 nm as well as two transistors, a source-side selection transistor SSTRmn and a drain-side selection transistor SDTrmn, are connected in series to each other (see FIG. 3)” such that bit lines BLmn are connected to and placed

above drain-side selection transistors SDTrmn. Ex. 1011, [0047]-[0055], Fig. 2.

119. In light of the above teachings, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to place bit lines over (e.g. above, or on top of) Ahn's flash memory and would have known that applying bit lines to Ahn's flash memory to yield the claimed limitations would predictably work and provide the expected functionality. Indeed, a person of ordinary skill in the art would have had a reasonable expectation of success in placing bit lines over Ahn's channel region (310) of the drain select transistor, because it would involve no modification of the flash memory structure disclosed in Ahn.

I. Claim [8]

120. Claim [8] recites **"The apparatus of claim 1, wherein the memory element comprises polysilicon."** See my discussion of claim [1] above in Section IX.A.2a-f. The added limitation of claim [8] is met by Ahn.

121. Ahn discloses that the memory element (e.g., "charge trap layer") comprises polysilicon (e.g., "polysilicon"). See, e.g., Ahn:

- [0040] "...***a charge trap layer is formed by depositing, for example, a silicon nitride film or a polysilicon film*** to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (230).

122. See my discussion of element [1.c] above in Section IX.A.2.d. Ahn further discloses that its "charge trap layer" is formed by depositing "a polysilicon

film.” Ahn, [0040].

m. Claim [9]

123. **Claim [9] recites “The apparatus of claim 1, wherein the memory element comprises a dielectric material.”** See my discussion of claim [1] above in Section IX.A.2.a-f. The added limitation of claim [9] is met by Ahn.

124. Ahn discloses that the memory element (*e.g.*, “charge trap layer”) comprises a dielectric material (*e.g.*, “silicon-nitride”). *See, e.g.*, Ahn:

- [0040]: “...***a charge trap layer is formed by depositing, for example, a silicon nitride film*** or a polysilicon film to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (230).”

125. See my discussion of element [1.c] above in Section IX.A.2.d.

126. Ahn further discloses that its “charge trap layer” is formed of “a silicon nitride film.” Ahn, [0040]. As made clear in U.S. Patent Application Publication No. 2008/0116441 (“Raghuram”), which I understand has been designated as Exhibit 1019, “dielectric material can be any known electrically insulating material, such as silicon oxide, silicon nitride, or silicon oxynitride.” Ex. 1019, [0071].

n. Element [17.pre]

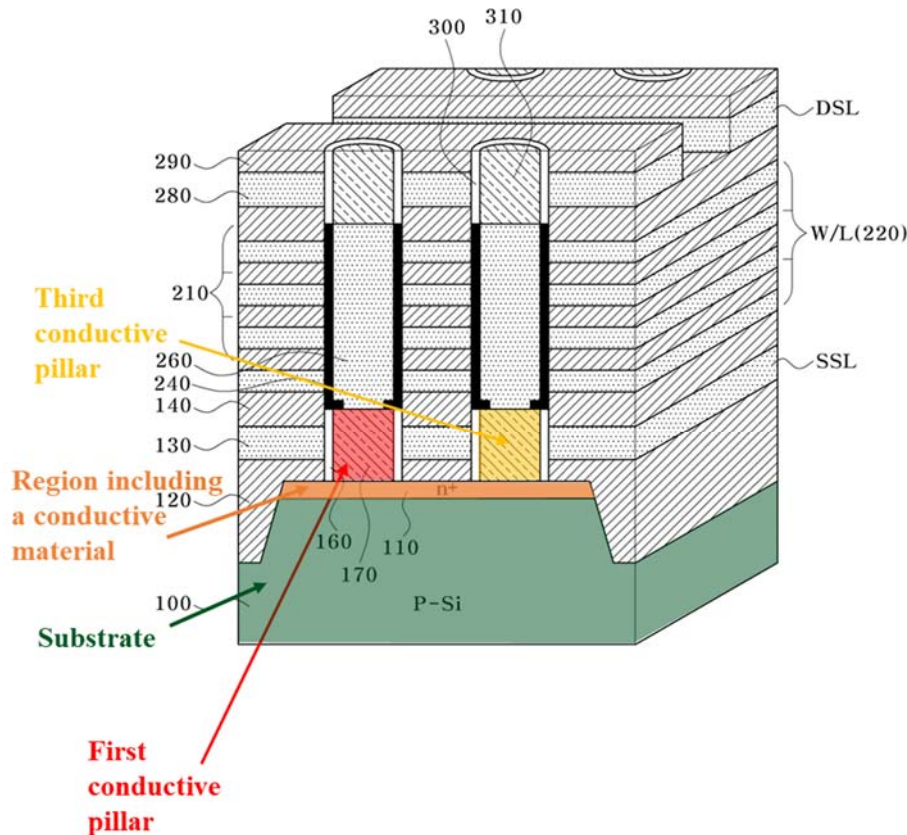
127. **Element [17.pre] recites “An apparatus comprising.”** This element is met by Ahn. See my discussion of element [1.pre] above in Section IX.A.2.a.

o. Elements [17.a] and [17.b]

128. Elements [17.a] and [17.b] recite “a first conductive pillar and a second conductive pillar extending outward from a substrate” and “a third conductive pillar and a fourth conductive pillars extending outward from the substrate.” These elements are met by Ahn.

129. Ahn discloses a first conductive pillar (*e.g.*, the front-left “channel region (170)” in Fig. 1), a second conductive pillar (*e.g.*, the back-left “channel region (170)” in Fig. 1), a third conductive pillar (*e.g.*, the front-right “channel region (170)” in Fig. 1), and a fourth conductive pillars (*e.g.*, the back-right “channel region (170)” in Fig. 1) extending outward from the substrate (*e.g.*, “substrate (100)”). *See, e.g.*, Ahn:

- Figure 1 (annotated)



- [0004]: “To improve the shortcomings of these two-dimensional structures, a three-dimensional cell structure has been proposed. **The three-dimensional cell structure is largely divided into a structure that equally layers a two-dimensional structure on top, and a structure that forms a channel in a vertical direction with respect to the silicon substrate, which is different from the existing concept.** However, in the case of a structure that equally stacks the same two-dimensional structure as the current one on top, there is a limit to the increase in integration, and in the case of a method of forming a channel in a vertical direction with the silicon substrate, the cell structure is formed as a depletion transistor structure and a well is not formed, so as the erasure operation is performed using a hole injection method based on hot hole formation rather than the conventional Fowler-Nordheim tunneling (F-N tunneling), there is a disadvantage in that it is difficult to implement above a certain level of integration.”
- [0026]: “A source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string, and **a plurality of such cell strings are arranged on the**

substrate (100).”

- [0027]: “The source select transistor consists of a gate conductive layer (130) formed on a substrate (100) to be separated by insulating layers (120, 140), a gate insulating layer (16) formed on the inner wall of a through hole penetrating the above gate conductive layer (130) and the insulating layers (120, 140), and...***a channel region (170) formed to fill the through hole in which the above gate insulating layer is formed. The channel region is connected to a source (110) formed on the substrate. The above channel region (170) is formed of a silicon epitaxial layer, or has a structure in which a silicon epitaxial layer and a polysilicon film are sequentially stacked*** from the sidewall of the gate insulating layer within the above through hole.”
- [0032] “Referring to Figure 3, a conductive layer (130) for forming a gate of a select transistor is sequentially formed on a substrate on which an insulating film (120) is formed, and an insulating layer (140) for separating the conductive layer above and the conductive layer formed thereon is sequentially formed. The above conductive layer (130) can be formed with a thickness of 10 to 1,000 Å using polysilicon film doped with impurities, a metal such as tungsten (W), or another conductive material.”
- [0033] “Next, the above conductive layer (130) and the insulating layer (140) in the region where the channel of the source select transistor is to be formed are etched to form a hole (150) that exposes the impurity layer (110) formed on the above substrate (100). ***The above hole (150) is a region in which a channel of a source select transistor is formed***, and is formed to have a diameter of 10 to 1,000 Å. The etching process for forming a hole (150) can be performed using wet etching, dry etching, or a mixed method thereof.”
- [0035] “***Next, the interior of the hole where the gate insulating film (160) is formed is filled with a semiconductor layer such as single crystal silicon (Si). The above semiconductor layer can be formed by using, for example, a selective epitaxial growth (SEG) method, such that a silicon (Si) film is selectively grown from the above impurity layer (110) in a gas atmosphere containing silicon (Si), and becomes a channel region (170) of the select transistor.*** Like this, a source select transistor is formed, which consists of a channel region (170), a gate insulating film (160), and a conductive layer (130) as a gate electrode.”

130. See my discussion of element [1.a] above in Section IX.A.2.b.

131. As illustrated in Figure 1, Ahn further discloses a cell unit comprising a matrix of two rows and two columns of cell strings. Ahn, Fig. 1. Ahn discloses “a plurality of cell strings[] arranged on the substrate (100)” where, as discussed in element [1.a], each such cell string includes a source select transistor having a channel region (170) within it. (Section IX.A.2.b). While only two of the cell strings of the front row are illustrated in Ahn’s figures (including the first and third conductive pillars), a person of ordinary skill in the art would have understood (and at least found obvious) that the two cell strings of the rear row (including the second and fourth conductive pillars) are identical. Indeed, Ahn’s manufacturing process does not distinguish memory cells in different rows of the cell strings in the rows in Figure 1. See Ahn, [0031]-[0049], Figure 1.

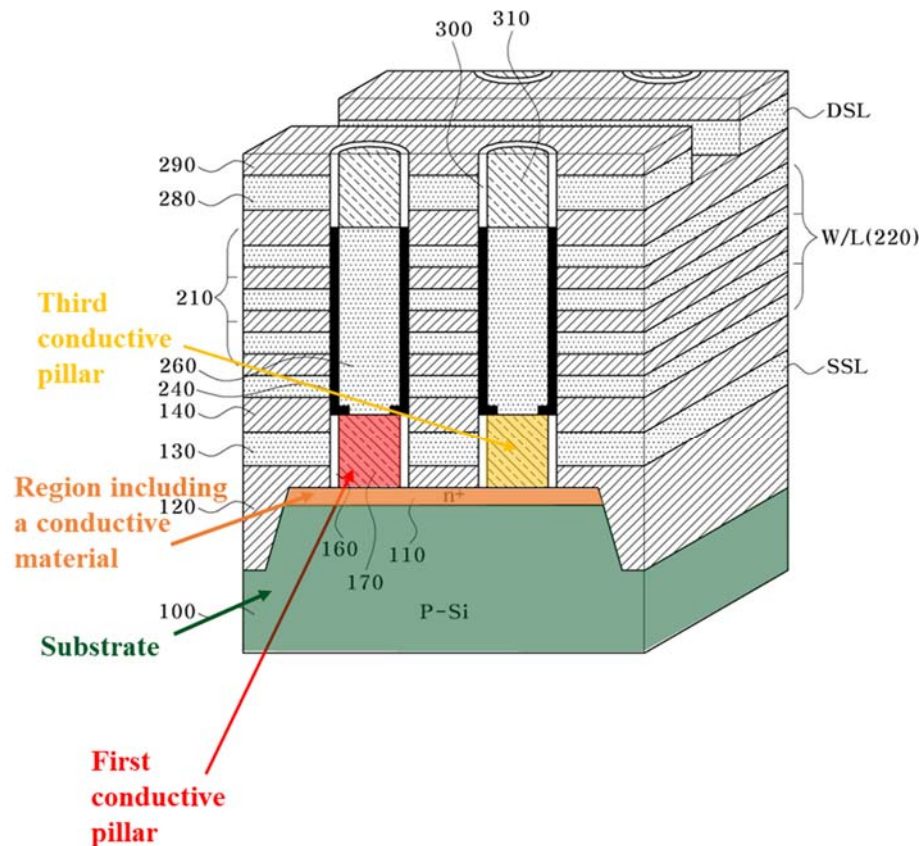
p. Element [17.c]

132. **Element [17.c] recites “a region including a conductive material, the region coupled to the first, second, third, and fourth conductive pillars, the region located between substrate and the first, second, third, and fourth conductive pillars.”** This element is met by Ahn.

133. Ahn discloses a region including a conductive material (*e.g.*, “source 110” or “impurity layer (110)”), the region coupled to the first, second, third, and fourth conductive pillars (*e.g.*, the four “channel regions (170)” of the source select

transistor formed on “source 110,” as shown in Fig. 1), the region located between substrate (*e.g.*, “substrate 100”) and the first, second, third, and fourth conductive pillars (*e.g.*, channel regions (170)). *See, e.g.*, Ahn:

- Figure 1 (annotated)



- [0026]: “***A source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string, and a plurality of such cell strings are arranged on the substrate (100).***”
- [0027]: “***The source select transistor consists of...a channel region (170) formed to fill the through hole in which the above gate insulating layer is formed. The channel region is connected to a source (110) formed on the substrate....***”
- [0031]: “***Referring to Figure 2, an impurity layer (110) is formed on a substrate (100) to form a common source of cells. The above substrate***

(100) may be a single crystal silicon (Si) substrate doped with P-type impurities. The above impurity layer (110) can be formed by ion-implanting impurities of the conductivity type opposite to that of the semiconductor substrate (100), for example, N type....”

- [0032] “Referring to Figure 3, a conductive layer (130) for forming a gate of a select transistor is sequentially formed on a substrate on which an insulating film (120) is formed, and an insulating layer (140) for separating the conductive layer above and the conductive layer formed thereon is sequentially formed. The above conductive layer (130) can be formed with a thickness of 10 to 1,000 Å using polysilicon film doped with impurities, a metal such as tungsten (W), or another conductive material.”
- [0033] “Next, the above conductive layer (130) and the insulating layer (140) in the region where the channel of the source select transistor is to be formed are etched to form a hole (150) that exposes the impurity layer (110) formed on the above substrate (100). ***The above hole (150) is a region in which a channel of a source select transistor is formed***, and is formed to have a diameter of 10 to 1,000 Å. The etching process for forming a hole (150) can be performed using wet etching, dry etching, or a mixed method thereof.”
- [0035] “***Next, the interior of the hole where the gate insulating film (160) is formed is filled with a semiconductor layer such as single crystal silicon (Si). The above semiconductor layer can be formed by using, for example, a selective epitaxial growth (SEG) method, such that a silicon (Si) film is selectively grown from the above impurity layer (110) in a gas atmosphere containing silicon (Si), and becomes a channel region (170) of the select transistor.*** Like this, a source select transistor is formed, which consists of a channel region (170), a gate insulating film (160), and a conductive layer (130) as a gate electrode.”

134. See my discussion of element [1.a] and [17.a]-[17.b] above in Section IX.A.2.b & IX.A.2.o.

135. Ahn further discloses that an impurity layer (110) (also referred to as source (110)) that is formed on a substrate (100) constitutes a common source of

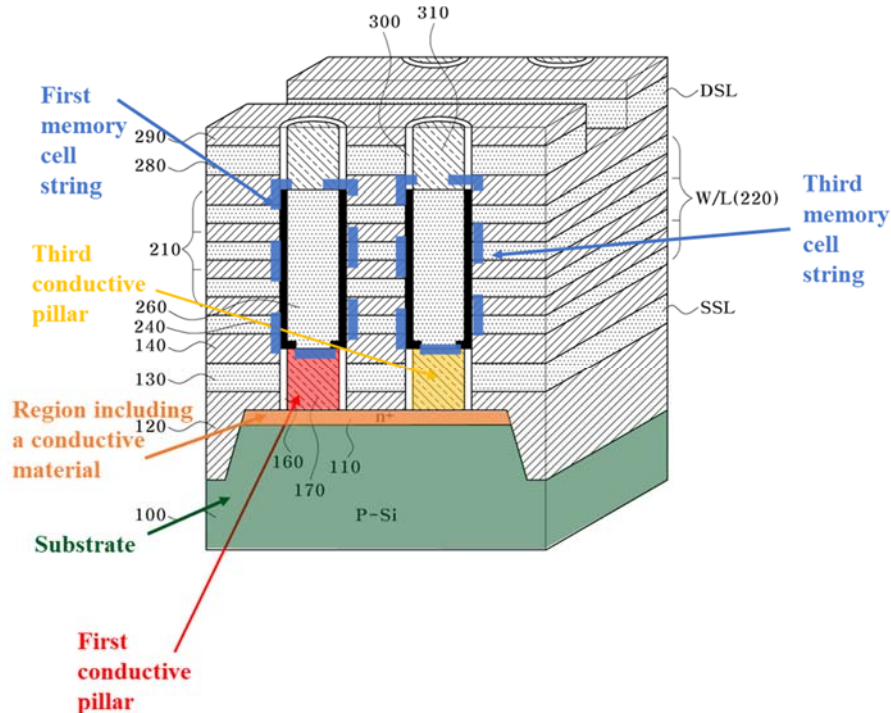
cells. Ahn, [0031]. Impurity layer (110) is “formed by ion-implanting impurities of the conductivity type opposite to that of the semiconductor substrate (100), for example, N type” and insulating film (120) “separate[s] the impurity layer from **other** conductive layers.” Ahn, [0031]. Because an insulating layer separates the impurity from other conductive layers, the impurity layer (110) is itself formed of conductive material. Ahn further discloses that channel region (170) is formed on impurity layer (110) such that the impurity layer or source (110) is coupled to channel region (170). In this arrangement, source (110) is located between the channel region (170) and substrate (100) for each of the four channel regions (see [17.a]-[17.b]). Ahn, [0027], [0031]-0035].

q. Elements [17.d]-[17.g]

136. **Elements [17.d]-[17.g] respectively recite “a [first/second/third/fourth] memory cell string formed over the first conductive pillar.”** These elements are met by Ahn.

137. Ahn discloses a first memory cell string formed over the first conductive pillar, a second memory cell string formed over the second conductive pillar, a third memory cell string formed over the third conductive pillar, a fourth memory cell string formed over the fourth conductive pillar (*e.g.*, “memory cells” of “cell string” over four “channel region (170)” of Fig. 1—see [17.a]-[17.b]). See, *e.g.*, Ahn:

- Figure 1 (annotated front portion)



- [0025]: “Referring to Figure 1, a flash memory device having a three-dimensional structure according to one embodiment of the present invention includes a source select transistor formed on a substrate (100), **gate stacks (220) formed on the above source select transistor and repeatedly stacked to be separated by an insulating layer (210), a charge storage region (240) formed by a blocking layer, a charge trap layer, and a tunneling layer formed on a sidewall of a through hole penetrating the above gate stacks, memory cells formed by a channel region (260) formed to fill the above through hole,** and a drain select transistor formed to be connected to the above memory cells.”
- [0026]: “**A source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string,** and a plurality of such cell strings are arranged on the substrate (100).”
- [0036]: “**...on the resulting structure in which the source select transistor is formed, an interlayer insulating film (210) and a conductive layer (220) are repeatedly deposited several times.** ...The above conductive layer (220) can be repeatedly stacked as many times as the number of memory cells connected to one cell string, for example, 2

- times, 4 times, 8 times, ... up to 1,000 times. The above conductive layer (220) serves as a control gate of the memory cell, and the interlayer insulating film (210) serves to separate the vertically-stacked memory cells.”
- [0037]: “...after stacking the conductive layers (220) and interlayer insulating films (210) as many times as the number of memory cells connected to the cell string, ***a through hole (230) is formed to form an ONO film for the channel of the cell transistor and charge storage.***”
 - [0038]: “***an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (230).***”
 - [0042]: “In order to ***connect the channel region of the source select transistor and the channel region of the memory cell***, the protective film (250), tunneling layer, charge trap layer, and blocking layer at the bottom of the through hole are etched to expose the channel region (170) of the source select transistor.”
 - [0043]: “...***a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of the cell transistor.*** The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities.”

138. See my discussion of elements [1.a]-[1.b], [17.a]-[17.c] above in Section IX.A.2.b-c & IX.A.2.o-p.

139. Ahn further discloses that each “source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string.” Ahn, [0026]. Ahn also discloses that each of those source select transistors includes channel region (170), which is formed under the channel region (260) of the memory cells—in other words, a first, second, third,

and fourth set of memory cells are respectively formed over the first, second, third and fourth channel regions (170) illustrated in Figure 1, as identified in elements [17.a]-[17.d]. Ahn, [0026], [0042]-[0043], Fig. 1.

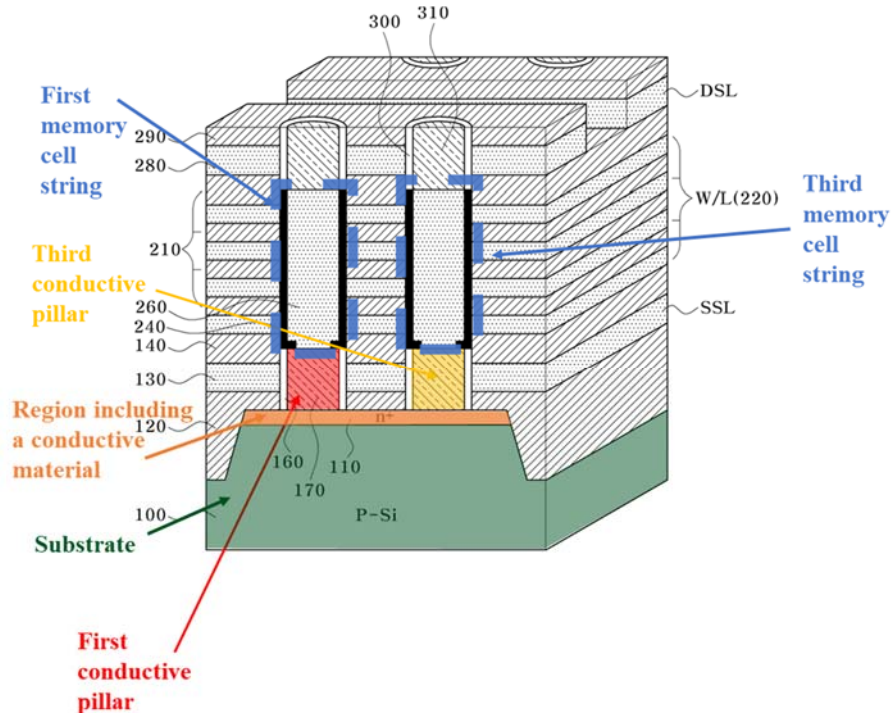
r. Elements [17.h] and [17.i]

140. **Elements [17.h] and [17.i] recite “a first data line coupled to the first and second memory cell strings, the first and second memory cell strings located between the first data line and the substrate; a second data line coupled to the third and fourth memory cell strings, the third and fourth memory cell strings located between the second data line and the substrate.”**

These elements are met by Ahn.

141. A person of ordinary skill in the art would have understood that Ahn’s memory device includes a first data line (*e.g.*, line completing circuit on drain side of “cell strings”) coupled to the first and second memory cell strings (*e.g.*, “memory cells” of front-left and back-left “cell strings” of Fig. 1), the first and second memory cell strings located between the first data line and the substrate (*e.g.*, “substrate (100)"); and a second data line (*e.g.*, line completing circuit on drain side of “cell strings”) coupled to the third and fourth memory cell strings (*e.g.*, “memory cells” of front-right and back-right “cell strings” of Fig. 1), the third and fourth memory cell strings located between the second data line and the substrate (*e.g.*, “substrate (100)"). *See, e.g.*, Ahn:

- Figure 1 (annotated)



- [0022]: “According to the present invention, ... by forming wells in vertically arranged memory cells, ***data in the memory cells can be simultaneously erased*** using the F-N tunneling method.”
- [0025]: “Referring to Figure 1, a flash memory device having a three-dimensional structure according to one embodiment of the present invention includes ***a source select transistor formed on a substrate (100), gate stacks (220) formed on the above source select transistor and repeatedly stacked to be separated by an insulating layer (210), a charge storage region (240) formed by a blocking layer, a charge trap layer, and a tunneling layer formed on a sidewall of a through hole penetrating the above gate stacks, memory cells formed by a channel region (260) formed to fill the above through hole, and a drain select transistor formed to be connected to the above memory cells.***”
- [0026]: “***A source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string***, and a plurality of such cell strings are arranged on the substrate (100).”

- [0037]: "... after stacking the conductive layers (220) and interlayer insulating films (210) as many time as the number of memory cells connected to the cell string, **a through hole (230) is formed to form an ONO film for the channel of the cell transistor and charge storage.** Specifically, the alternately-stacked conductive layers (210) and interlayer insulating films (220) are anisotropically etched so that the gate insulating film (160) and channel region (170) of the source select transistor are exposed...."
- [0038]: "**an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (230).**"
- [0042]: "**In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, charge trap layer, and blocking layer at the bottom of the through hole are etched to expose the channel region (170) of the source select transistor.**"
- [0043]: "...**a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of the cell transistor.** The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities."
- [0044]: "Referring to Figure 10, **a drain select transistor for string selection is formed on the resulting material in which a plurality of memory cells are formed.**"
- [0046]: "Next, **in order to connect the drain select transistor and the memory cell transistor, the conductive layer (280) and the insulating film (270, 290) are anisotropically etched to form a hole....**"
- [0048]: "Next, **in order to connect the channel region of the memory cell and the channel region of the drain select transistor, the gate insulating film (300) at the bottom of the hole is etched so that the channel region of the memory cell is exposed....**"
- [0049]: "**A semiconductor layer is formed on the resulting material in which the channel region of the memory cell is exposed so that the**

above hole is filled, thereby forming a channel region (310) of the drain select transistor....”

142. See my discussion of elements [7] and [17.a]-[17.g] above in Section IX.A.2.k & IX.A.2.o-q.

143. As discussed in [7], a person of ordinary skill in the art would have understood that Ahn’s memory device includes bit lines (data lines) coupled to “channel region (260),” such that Ahn’s memory cell strings are located between the bit lines and substrate (100).

144. A person of ordinary skill in the art would have further understood (or at least found it obvious) that the bit lines are coupled to the cell strings in a direction perpendicular to drain select lines DSL in order to allow selection of individual memory cells. In particular, each of the drain select lines DSL is able to select one row of cell strings (e.g., the front row or back row in Figure 1) and bit lines perpendicular to the drain select lines DSL are able to select one column of cell strings (e.g., the left or right column of cell strings), such that any pair of drain select line DSL and bit line would select a unique cell string. In this arrangement, the front-left and back-left memory strings would be between one bit line and the substrate, and the front-right and back-right memory strings would be between another bit line and the substrate.

145. Moreover, a person of ordinary skill in the art would have at least found it obvious to arrange bit lines perpendicular to drain select lines DSL in

Ahn's memory device to advantageously select cell strings. Indeed, this approach was well known in the art. For instance, Son, which I discussed above in Section IX.A.2.k., discloses a "nonvolatile memory device [that] includes a plurality of strings STRs between the bit lines BL1 to BL4 and the common source line CSL" and that the bit lines are "disposed to intersect with the upper selection lines USLs" such that "each of the semiconductor pillars PLs may be disposed at places where the bit lines BLs and the upper selection lines USLs are intersected with each other," thereby allowing individual semiconductor pillar PL or memory string to be selected. Ex. 1010, [0039], [0053]. Similarly, Katsumata discloses that "a bit line BL_{nm} is connected to the drain of each drain-side selection transistor SDTr_{nm}," where the bit lines are placed above and in a direction perpendicular to the drain-side selection gate lines SGD. Ex. 1011, [0047]-[0055], FIGs. 1-2. A person of ordinary skill in the art would thus have found it routine, straightforward and advantageous to place bit lines over and perpendicular to Ahn's drain select lines and would have known that applying bit lines to Ahn's flash memory so as to yield the claimed limitations would predictably work and provide the expected functionality.

s. Elements [17.j] and [17.k]

146. Elements [17.j] and [17.k] recite "a first control gate formed in a first device level" and "a second control gate formed in a second device level."

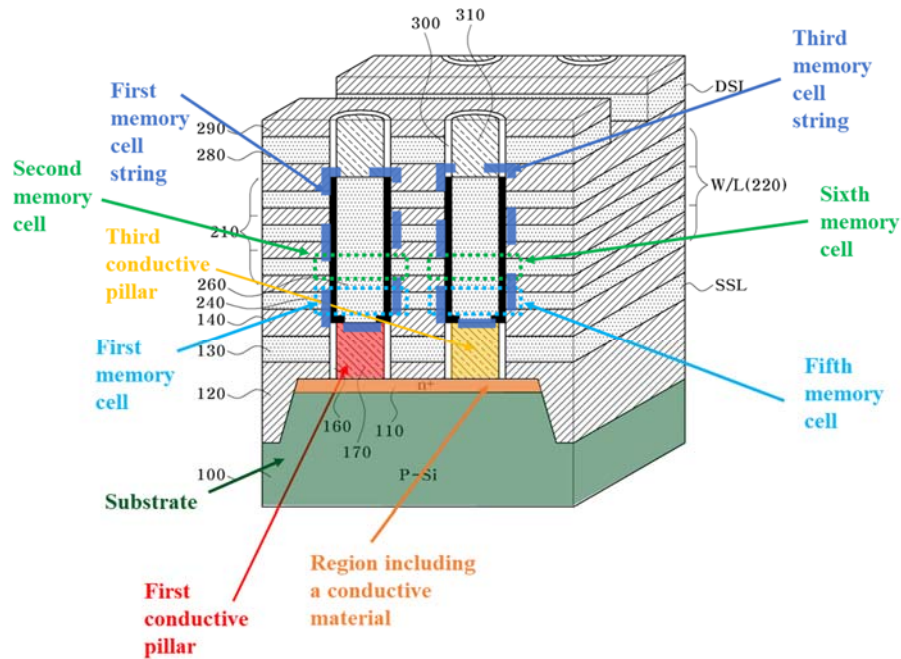
These elements are met by Ahn. See my discussion of elements [1.c] and [1.d] above in Section IX.A.2.d-e.

t. Element [17.l]

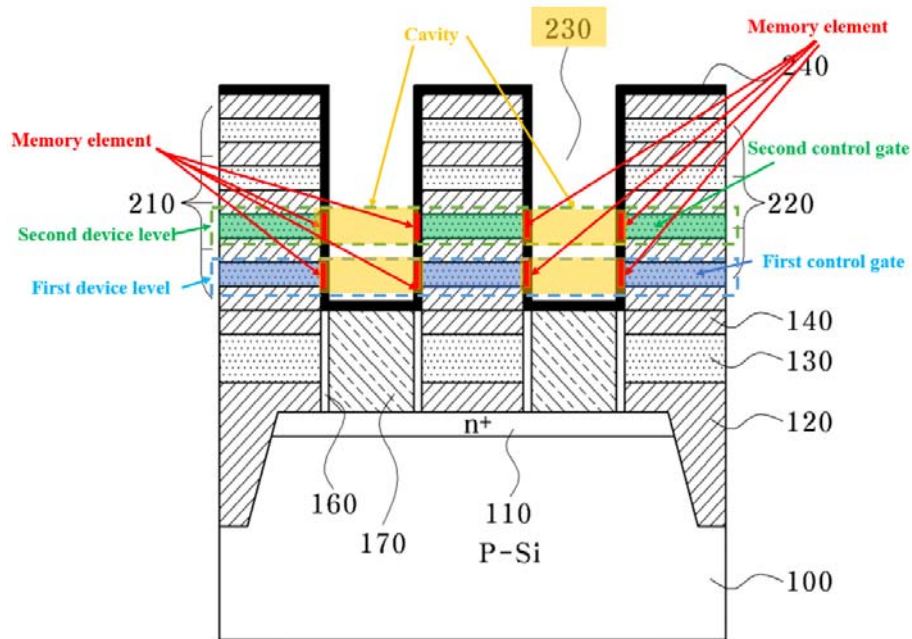
147. **Element [17.l] recites “the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate.”** This element is met by Ahn.

148. Ahn discloses that the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate (*e.g.*, front-left “cell string” including “memory cells” at the lowest and second lowest “conductive layer (220)” in Fig. 1, with “charge storage layer” formed on the inner wall of “through hole (230)” in those layers—*see* [17.d]). *See, e.g.*, Ahn:

- Figure 1 (annotated)



- Figure 7 (annotated)



- [0025]: “Referring to Figure 1, a flash memory device having a three-dimensional structure according to one embodiment of the present invention includes a source select transistor formed on a substrate (100), **gate stacks (220) formed on the above source select transistor and repeatedly stacked to be separated by an insulating layer (210), a**

charge storage region (240) formed by a blocking layer, a charge trap layer, and a tunneling layer formed on a sidewall of a through hole penetrating the above gate stacks, memory cells formed by a channel region (260) formed to fill the above through hole, and a drain select transistor formed to be connected to the above memory cells.”

- [0026]: “A source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string, and a plurality of such cell strings are arranged on the substrate (100).”
- [0028]: “***The gate stack (220) constituting the above memory cell is repeatedly stacked as many times as the number of memory cells connected to one cell string.*** The memory cells connected to one cell string are separated by an insulating layer (210), and the memory cells arranged in the same layer constitute one page.”
- [0036]: “...on the resulting structure in which the source select transistor is formed, an interlayer insulating film (210) and a conductive layer (220) are repeatedly deposited several times. ...The above conductive layer (220) can be repeatedly stacked as many times as the number of memory cells connected to one cell string, for example, 2 times, 4 times, 8 times, ... up to 1,000 times. ***The above conductive layer (220) serves as a control gate of the memory cell,*** and the interlayer insulating film (210) serves to separate the vertically-stacked memory cells.”
- [0037]: “...after stacking the conductive layers (220) and interlayer insulating films (210) as many times as the number of memory cells connected to the cell string, ***a through hole (230) is formed to form an ONO film for the channel of the cell transistor and charge storage.***”
- [0038]: “an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, ***a charge trap layer,*** and a tunneling layer, are ***sequentially formed on the inner wall of the above through hole (230).***”
- [0040]: “Next, ***a charge trap layer is formed by depositing, for example, a silicon nitride film or a polysilicon film to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (230)....***”

- [0042]: “In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, charge trap layer, and blocking layer at the bottom of the through hole are etched to expose the channel region (170) of the source select transistor.”
- [0043]: “...***a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of the cell transistor.*** The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities.”

149. See my discussion of elements [1.b]-[1.d], [17.d]-[17.g], and [17.j]-[17.k] above in Section IX.A.2.c-e, IX.A.2.q, IX.A.2.s.

150. Further, as discussed in [1.c]-[1.d], Ahn discloses multiple memory cells arranged in a vertical direction in each cell string, where each memory cell includes a charge trap layer on the inner wall of through hole (230) in conductive layer (220). Ahn, [0028], [0036], [0040]. In Figure 1 above, in the front-left memory string, the lowest conductive layer (220) in combination with the charge trap layer form a first memory cell, and the second lowest conductive layer (220) in combination with the charge trap layer form a second memory cell.

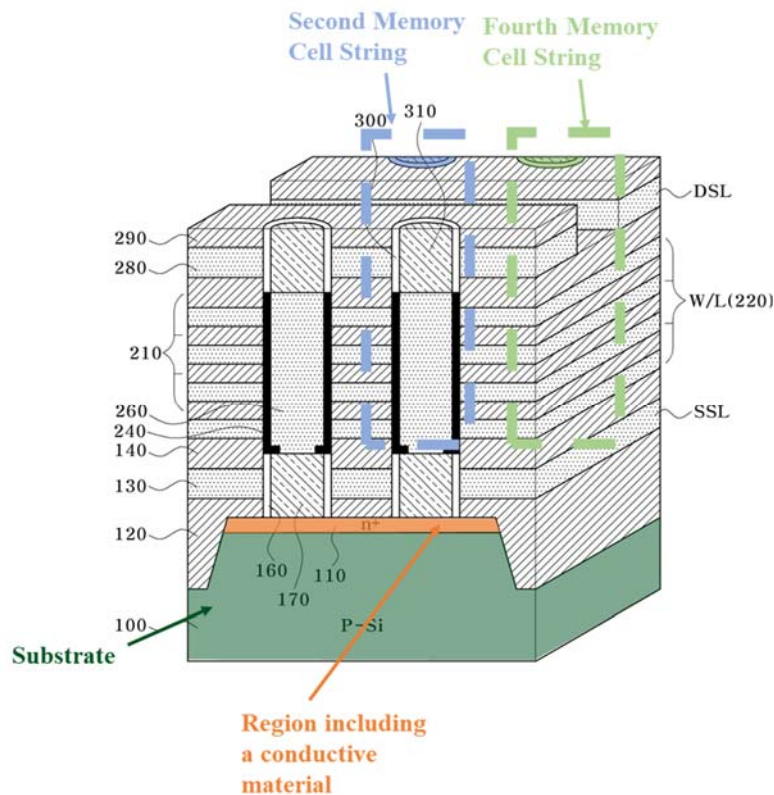
u. Element [17.m]

151. **Element [17.m] recites “the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed**

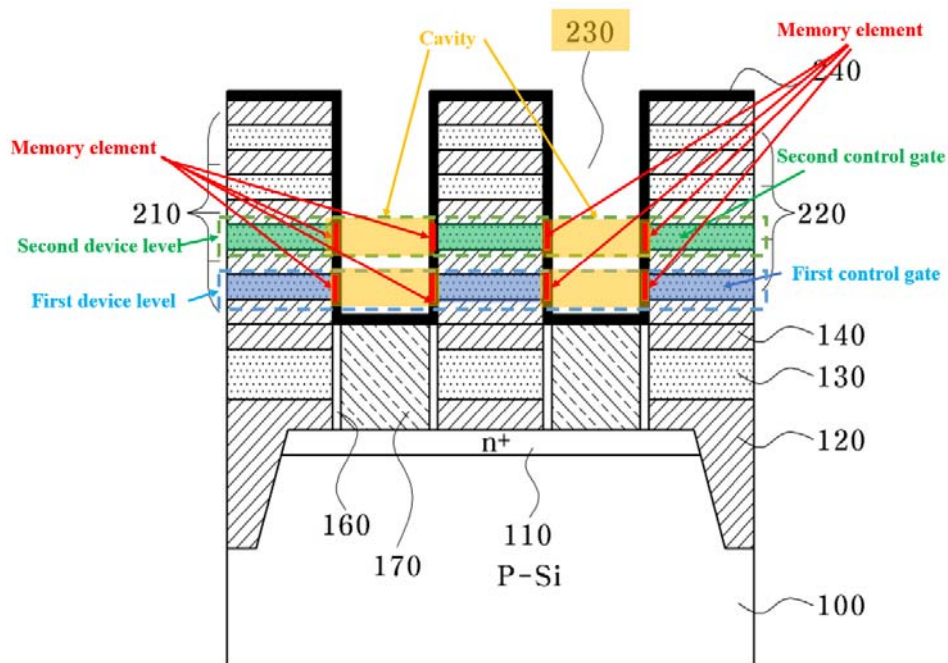
in a second cavity of the second control gate.” This element is met by Ahn.

152. Ahn discloses that the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate (*e.g.*, back-left “cell string” including “memory cells” at the lowest and second lowest “conductive layer (220)” in Fig. 1, with “charge storage layer” formed on the inner wall of “through hole (230)” in those layers—*see* [17.e]). *See, e.g.*, Ahn:

- Figure 1 (annotated)



- Figure 7 (annotated)



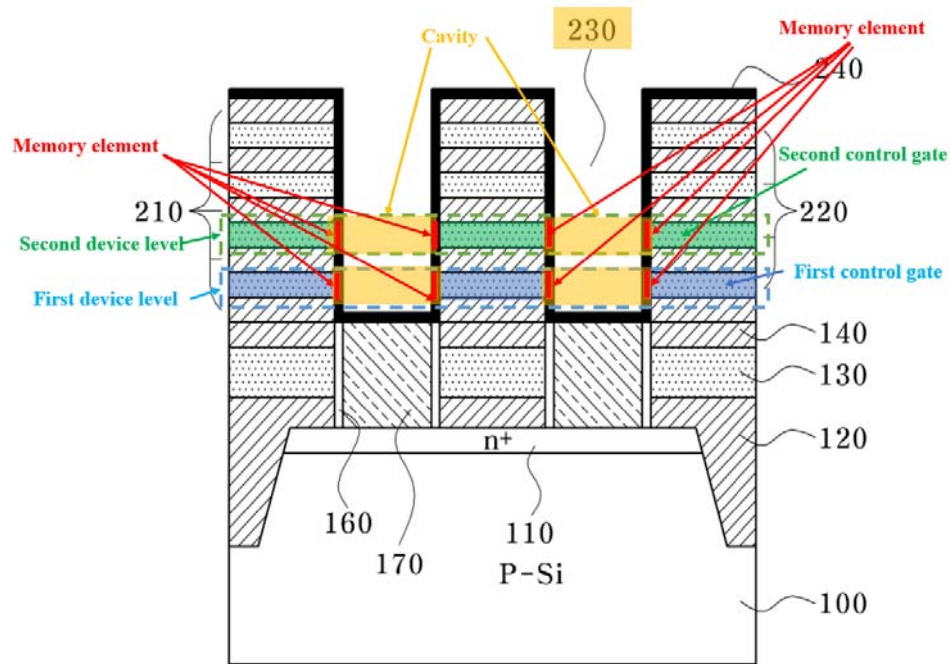
153. See my discussion of elements [1.b]-[1.d], [17.d]-[17.g], and [17.j]-[17.l] above in Section IX.A.2.c-e, IX.A.2.q, IX.A.2.s-t.

154. Further, the same analysis provided for [17.l] applies for this limitation. For this element, however, the third and fourth memory cells are in the back-left memory string of Fig. 1.

v. Element [17.n]

155. Element [17.n] recites “the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate.” This element is met by Ahn.

156. Ahn discloses that the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control



157. See my discussion of elements [1.b]-[1.d], [17.d]-[17.g], and [17.j]-[17.l] above in Section IX.A.2.c-e, IX.A.2.q, IX.A.2.s-t.

158. Further, the same analysis provided for [17.l] applies for this limitation. For this element, however, the fifth and sixth memory cells are in the front-right memory string of Fig. 1.

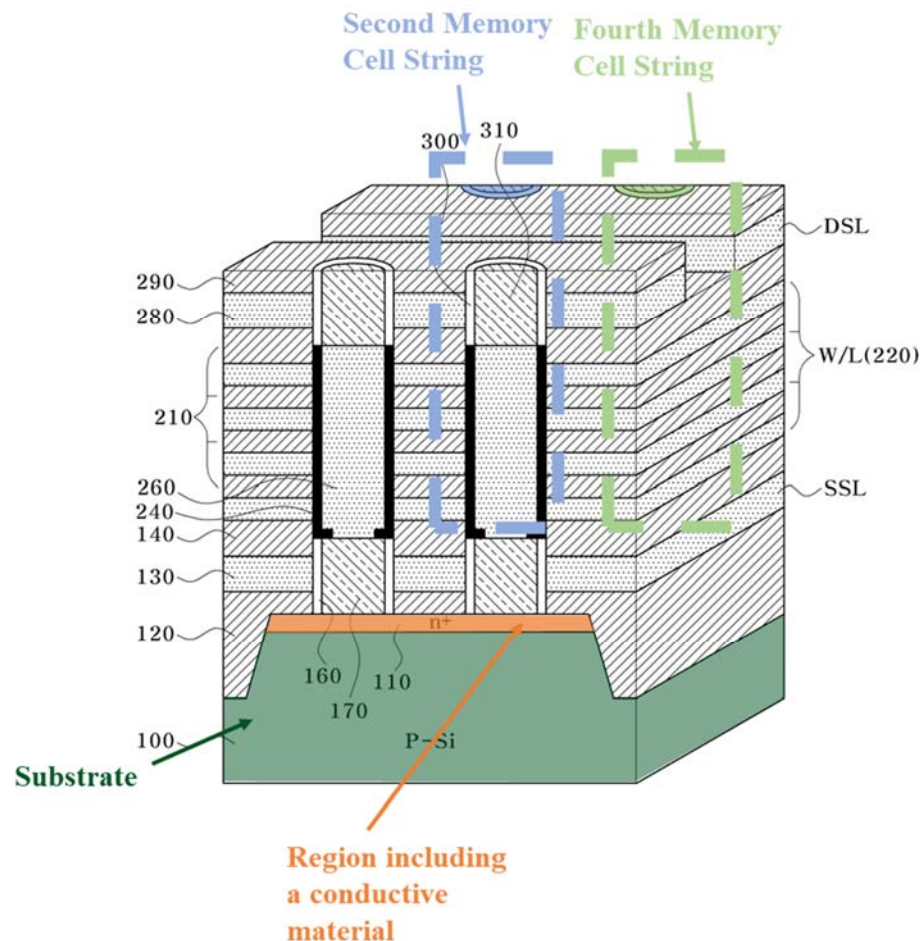
w. Element [17.o]

159. **Element [17.o] recites “the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.”** This element is met by Ahn.

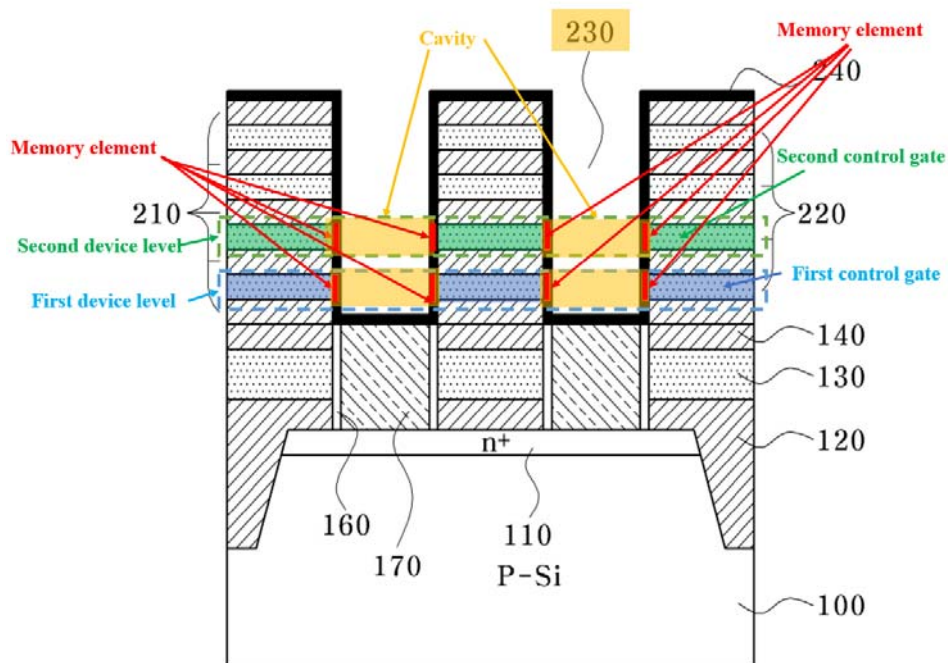
160. Ahn discloses that the fourth memory cell string includes a seventh

memory cell having a memory element formed in a fourth cavity of the first control gate, and a eighth memory cell having a memory element formed in a fourth cavity of the second control gate (*e.g.*, back-right “cell string” including “memory cells” at the lowest and second lowest “conductive layer (220)” in Fig. 1, with “charge storage layer” formed on the inner wall of “through hole (230)” in those layers—*see* [17.g]). *See, e.g.*, Ahn:

- Figure 1 (annotated)



- Figure 7 (annotated)



161. See my discussion of elements [1.b]-[1.d], [17.d]-[17.g], and [17.j]-[17.l]. above in Section IX.A.2.c-e, IX.A.2.q, IX.A.2.s-t.

162. Further, the same analysis provided for [17.l] applies for this limitation. For this element, however, the seventh and eighth memory cells are in the back-right memory string of Fig. 1.

x. Claim [18]

163. **Claim 18 recites “The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises polysilicon.”** This claim is met by Ahn. See my discussion of claims [8] and [17] above in Section IX.A.2.1, IX.A.2.n-w. As I noted above in connection with claim [8], each memory element comprises polysilicon.

y. Claim [19]

164. **Claim [19] recites “The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises a silicon nitride.”** This claim is met by Ahn. See my discussion of claims [9] and [17] above in Section IX.A.2.m, IX.A.2.n-w. As I note above in connection with claim [9], each memory cell comprises silicon nitride.

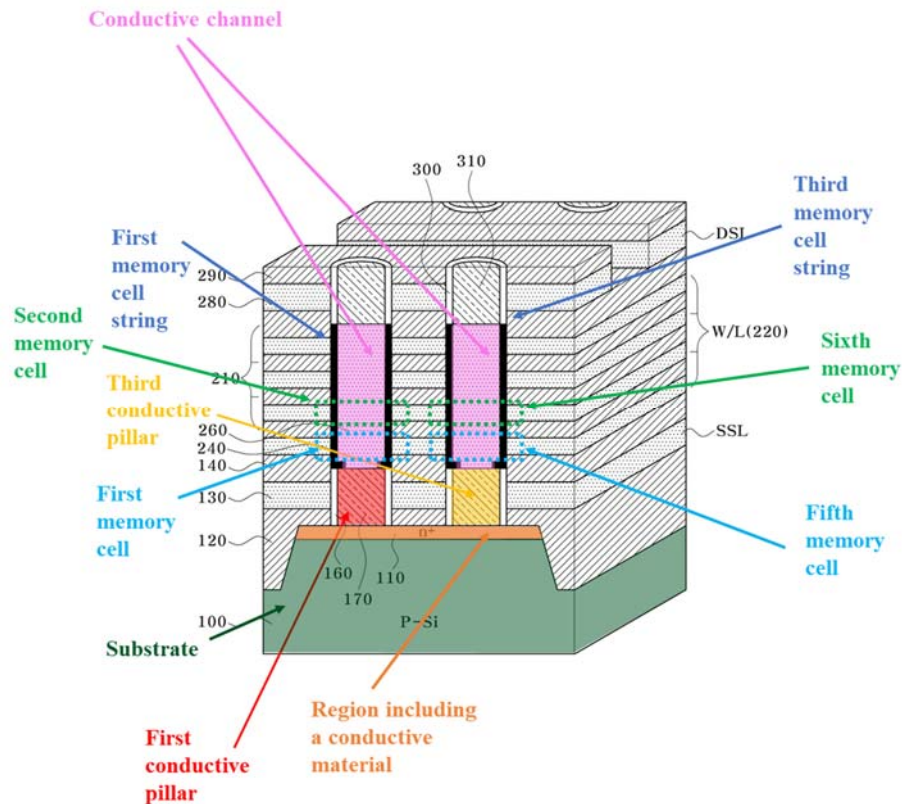
z. Claim [20]

165. **Claim [20] recites “The apparatus of claim 17, further comprising: a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells; a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells; a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells; and a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells.”** See my discussion of claim [17] above in Section IX.A.2.n-w. The added limitation of claim [20] is met by Ahn.

166. Ahn discloses a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells, a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells, a third conductive channel coupled to

the third conductive pillar and extending between the fifth and sixth memory cells, and a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells (e.g., four “channel region (260)” formed over four “channel region (170)” of Fig. 1, extending between “memory cells” at the lowest and second-lowest “conductive layers (220)”—see [17.a]-[17.b], [17.l]-[17.o]). See, e.g., Ahn:

- Figure 1 (annotated)



- [0025]: “Referring to Figure 1, a flash memory device having a three-dimensional structure according to one embodiment of the present invention includes a source select transistor formed on a substrate (100), **gate stacks (220) formed on the above source select transistor and repeatedly stacked to be separated by an insulating layer (210), a charge storage region (240) formed by a blocking layer, a charge trap**

layer, and a tunneling layer formed on a sidewall of a through hole penetrating the above gate stacks, memory cells formed by a channel region (260) formed to fill the above through hole, and a drain select transistor formed to be connected to the above memory cells.”

- [0026]: “A source select transistor, **a plurality of memory cells**, and a drain select transistor are arranged vertically on a substrate (100) **to form one cell string**, and a plurality of such cell strings are arranged on the substrate (100).”
- [0028]: “The **gate stack (220) constituting the above memory cell is repeatedly stacked as many times as the number of memory cells connected to one cell string**. The memory cells connected to one cell string are separated by an insulating layer (210), and the memory cells arranged in the same layer constitute one page.”
- [0036]: “...**on the resulting structure in which the source select transistor is formed, an interlayer insulating film (210) and a conductive layer (220) are repeatedly deposited several times**. ...The above conductive layer (220) can be repeatedly stacked as many times as the number of memory cells connected to one cell string, for example, 2 times, 4 times, 8 times, ... up to 1,000 times. **The above conductive layer (220) serves as a control gate of the memory cell**, and the interlayer insulating film (210) serves to separate the vertically-stacked memory cells.”
- [0037]: “Referring to Figure 6, after **stacking the conductive layers (220) and interlayer insulating films (210) as many times as the number of memory cells connected to the cell string, a through hole (230) is formed to form an ONO film for the channel of the cell transistor and charge storage**. Specifically, the alternately-stacked conductive layers (210) and interlayer insulating films (220) are anisotropically etched so that the gate insulating film (160) and channel region (170) of the source select transistor are exposed. At this time, the etching process can use a wet or dry etching method, and the size of the through hole (230) is formed to a size that can be gap-filled with a semiconductor layer that acts as a channel of the cell transistor and an ONO film that acts as a charge storage film. In this embodiment, the above through hole (230) was formed with a diameter of 10 to 1,000 Å.”

- [0038]: “***an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (230).***”
- [0040]: “Next, ***a charge trap layer is formed*** by depositing, for example, a silicon nitride film or a polysilicon film to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (230). The charge trap layer can be deposited using atomic layer deposition (ALD) or chemical vapor deposition (CVD). An oxide film is deposited on the charge trap layer on the inner wall of the through hole (230) to a thickness of 10 to 1,000 Å to form a tunneling layer of the memory cell. When forming the above tunneling layer, it is possible to form an oxygen nitride film (SiON) by performing the process in an atmosphere containing both oxygen and nitrogen. In addition, the film quality of the tunneling layer can be improved by heat-treating in an NO gas or N₂O gas atmosphere after forming the tunneling layer.”
- [0042]: “***In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, charge trap layer, and blocking layer at the bottom of the through hole are etched to expose the channel region (170) of the source select transistor.***”
- [0043]: “***...a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of the cell transistor.*** The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities.”

167. See my discussion of elements [1.e], [17.a]-[17.b], [17.d]-[17.g], and [17.i]-[17.o] above in Section IX.A.2.f, IX.A.2.o, IX.A.2.q, IX.A.2.t-w.

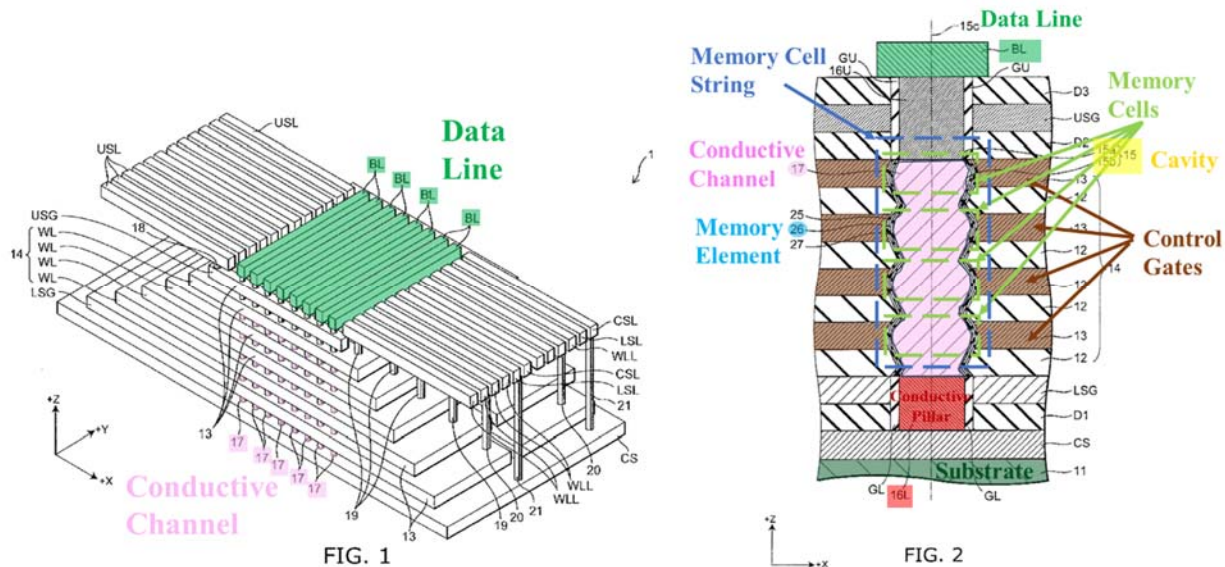
168. Further, as discussed for elements [1.e] and [17.d]-[17.g], the first, second, third, and fourth cell strings each include channel region (260), where the channel regions (260) are formed over and coupled to first, second, third, and fourth channel regions (170), respectively.

B. GROUND 2: Ahn in view of Ishikawa (Claims 7, 17)

169. As I discuss in connection with claims 7 and 17 in Section IX.A.2.k & IX.A.2.n-w, Ahn discloses and at least renders obvious these claims. To the extent further disclosure of the “data line” limitations of these claims is required, Ishikawa provides explicit teachings of these limitations.

170. Ishikawa discloses a data line (*e.g.*, “bit interconnect BL”) coupled to a conductive channel (*e.g.*, “semiconductor pillar 17”), wherein the first and second memory cells (*e.g.*, “memory cells”) are located between the data line and the substrate (*e.g.*, “substrate 11”) (claim 7). Ishikawa also discloses a first data line (*e.g.*, a first “bit interconnect BL”) coupled to first and second memory cell strings (*e.g.*, “memory strings” along the first bit interconnect BL), the first and second memory cell strings located between the first data line and a substrate (*e.g.*, “substrate 11”) ([17.h]) and a second data line (*e.g.*, a second “bit interconnect BL”) coupled to third and fourth memory cell strings (*e.g.*, “memory strings” along the second bit interconnect BL), the third and fourth memory cell strings located between the second data line and the substrate (*e.g.*, “silicon substrate 11”) ([17.i]).

171. Ishikawa is directed to a three-dimensional nonvolatile semiconductor memory device. Ishikawa, [0003], [0007]-[0008].



Ishikawa, Fig. 1 and Fig. 2 (annotated).

172. As shown in FIG. 1, Ishikawa discloses a plurality of **bit interconnects BL**, each of which extends in the Y direction. Specifically, **Bit interconnects BL** are formed perpendicular to the upper select gate interconnects USL and immediately above the columnar electrode 16U of the upper select gate USG. Ishikawa, [0033]-[0035], FIG. 2. FIG. 2 provides a cross-sectional view of the embodiment in FIG. 1, where a columnar electrode 16U is formed above and coupled to **semiconductor pillar 17** (i.e., a conductive channel). The **semiconductor pillar 17**, in turn, is formed above the **columnar electrode 16L** (i.e., a conductive pillar) (which is on **substrate 11**) and is inside each **through hole 15** (i.e., a cavity) of the **electrode films 13** (i.e., a control gate). Ishikawa, [0029], [0033]. The **semiconductor pillar 17** is surrounded by a dielectric layer 25, a **charge storage layer 26** (i.e., a memory element), and a dielectric layer 27—

combined with the **electrode films 13** serving as control gates, they form memory cells. Ishikawa, [0029]-[0030], [0033], [0050].

173. It is my opinion that a person of ordinary skill in the art would have been motivated to apply Ishikawa's teachings of a bit line to Ahn's memory device.

174. Ahn and Ishikawa are in the same field as the '903 patent, which includes a three-dimensional memory device, with memory cells arranged in the X, Y, and Z direction. '903 patent, Abstract, 1:20-35; 1:65-2:9 ("Fig. 1 shows a block diagram of a memory device 100 having a memory array 102 with memory cells 110 according to an embodiment of the invention [...] Memory cells 110 can be physically located in multiple device levels such that one group of memory cells 110 can be stacked on one or more groups of other memory cells 110."); Ishikawa, [0030], [0005] ("Thus, memory cells are three-dimensionally arranged at the intersections between the columnar electrodes and the electrode films."); Ahn, [0004], [0001] ("The present invention relates to a method for manufacturing a flash memory device, and more particularly, to a method for manufacturing a flash memory device having a three-dimensional structure.").

175. Ahn and Ishikawa are also reasonably pertinent to the problems addressed by the '903 patent, e.g., increasing density of memory devices. '903 patent, 1:26-28 ("As demand for higher density memory device increases, three-

dimensional (3D) memory devices have been proposed.”); Ishikawa, [0005]-[0006] (“Recently, to increase the density of flash memory, a technique for multilayering cells has been developed. [...] However, in such a stacked flash memory, with the advance of downscaling, the amount of charge stored in each memory cell decreases and causes the problem of decreased reliability.”); Ahn, [0005] (“A technical task to be achieved by the present invention is to provide a method for manufacturing a flash memory device having a structure capable of increasing the integration density of memory cells without being limited by the substrate area by implementing memory cells in a vertical direction with respect to a semiconductor substrate.”).

176. A person of ordinary skill in the art would have been motivated to apply Ishikawa’s teachings of data lines to Ahn’s memory device to advantageously read from, write to, and erase individual memory cells. For example, Ishikawa discloses bit lines BL formed above upper select gates USG and in the direction perpendicular to upper select gate interconnects USL (i.e., drain select lines), and as a result, “the X coordinate of a memory cell is selected by selecting a bit line BL” and “the Y coordinate can be selected by selecting an upper select gate USG,” thereby allowing for a selection of a single memory cell string. Ishikawa, [0005], [0034], [0053]. With the selection of word line WL in the Z coordinate, Ishikawa’s arrangement of bit lines BL allows “one memory cell [to

be] selected, and data is stored or erased by charge injection into or extraction” from each memory cell. Ishikawa, [0053]. Accordingly, a person of ordinary skill in the art would have been motivated to incorporate Ishikawa’s data line to Ahn’s memory device, such that each data line is formed above drain select transistors and coupled to the cell strings underneath in a direction perpendicular to drain select lines DSL, to advantageously select individual memory cells for storing and erasing data.

177. A person of ordinary skill in the art would have had a reasonable expectation of success in applying Ishikawa’s teaching of data lines to Ahn’s memory device. As I explain in Section IX.B.2.k, it was well known in the art to use data lines for data storage and erase. For instance, Katsumata discloses a three-dimensional non-volatile semiconductor storage device where “respective voltages of the bit lines BL1 to BL3, the drain-side selection gate lines SGD, the word lines WL1 to WL4, the source-side selection gate line SGS, and the source lines SL are controlled by bit line driving circuits,[] the drain-side selection gate line driving circuit 15, the word line driving circuits 13, the source-side selection gate line driving circuit 14, and a source line driving circuit” such that “data is written and erased by controlling charges of the charge accumulation layer in a predetermined memory transistor MTrmn.” Ex.1011, [0055]. Similarly, Endoh discloses that “[a] logic ‘1’ or ‘0,’ which is supplied by the bit line associated with

the subject NAND cell unit, is selectively programmed in the target memory cell.”

See Ex. 1008, 1:44-60. Further, Scott discloses that “[t]he floating gate transistor of each EEPROM memory cell is coupled to a unique combination of word and bit lines” and that “[i]n order to read a bit of information stored on a particular EEPROM memory cell, the associated bit line is raised above ground at the same time as the associated word line.” See Ex. 1009, 1:65-2:9, 2:38-46, Fig. 5.

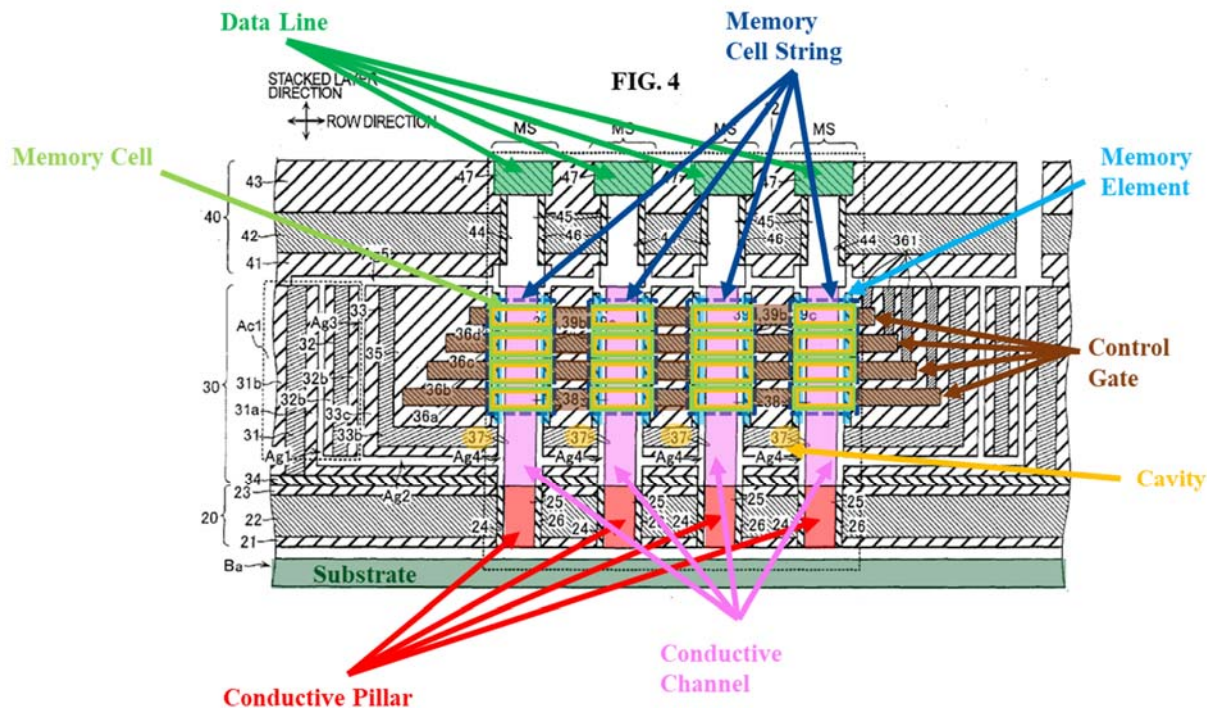
Moreover, no modification in Ahn’s manufacturing would have been needed in implementing Ishikawa’s teachings, other than the minimal modification of adding data lines above (e.g. on top of) Ahn’s memory device (to the extent they do not already exist).

178. Thus, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Ishikawa’s teaching of bit lines to Ahn’s memory device and would have known such combination would yield the claimed limitations and would predictably work and provide the expected resulting structure.

C. GROUND 3: Fukuzumi (Claims 1-3, 7, 9, 17, 19-20)

1. Overview of Fukuzumi

179. Fukuzumi is directed to “a nonvolatile semiconductor memory device,” with memory cells arranged in X, Y, and Z directions. Fukuzumi, [0002]-[0004]. FIG. 4 shows a cross-sectional view of an embodiment:



Fukuzumi, FIG 4 (annotated).

180. Fukuzumi's memory device comprises a matrix of "memory strings MS," where the "memory strings MS" include **memory cells MTr1mn-MTr4mn**. The indices "m" and "n" are counting numbers indicating the **memory cells'** X and Y coordinates. Fukuzumi, [0079]. Each memory string MS further includes a columnar semiconductor CLmn comprising **source-side columnar semiconductor layer 25** (i.e., a conductive pillar), which is formed on the **substrate**, **memory 38** (i.e., a conductive channel) formed above and coupled to **source-side columnar semiconductor layer 25**, and drain-side columnar semiconductor layer 45 connecting the **bit line layer 47** and **memories 38** along the column direction. Fukuzumi, [0086], [0088]-[0089], [0096], [0103], [0108]-[0109].

181. Fukuzumi’s **memory cells MTr1mn-MTr4mn** further include **word lines WL1-WL4** (e.g., **word line conduction layer 36a-d**) “connected to each gate of the memory cells,” in addition to a **charge storage layer 39b** (i.e., a memory element) that is formed on sidewalls of the **word lines WL1-WL4** in the **memory hole 37** (i.e., a cavity). Fukuzumi, [0080], [0085].

2. Invalidity of Claims 1-3, 7, 9, 17, and 19-20 Over Fukuzumi

182. As I discuss below, it is my opinion that Claims 1-3, 7, 9, 17, and 19-20 are anticipated and rendered obvious by Fukuzumi, regardless of whether the “cavity” limitation is construed based on Petitioner’s or Patent Owner’s constructions.

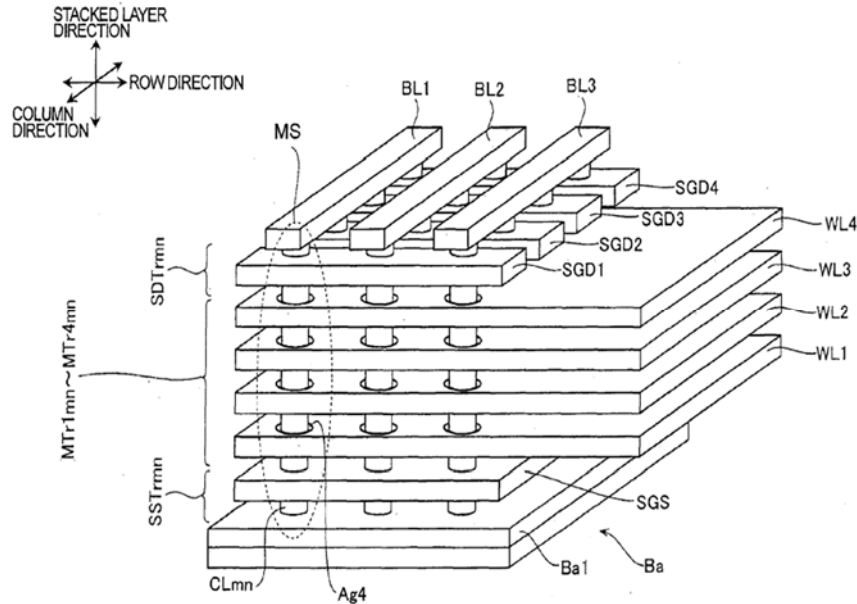
183. In addition to my discussion in Section IX.C.1, the following discussion identifies example disclosures followed by bulleted excerpts that each disclose Claims 1-3, 7, 9, 17, and 19-20.

a. Element [1.pre]

184. **Element [1.pre] recites “An apparatus comprising.”** To the extent the preamble is limiting, this element is met by Fukuzumi.

185. **Fukuzumi discloses an apparatus** (e.g., “semiconductor memory device”). *See, e.g.,* Fukuzumi:

- Figure 2



- [0002] “The present invention relates to an electrically erasable **semiconductor memory device**”
- [0005]: “According to an aspect of the invention, **there is provided a nonvolatile semiconductor memory device**, comprising a plurality of memory strings, each of the memory strings being constituted with a plurality of electrically erasable memory cells being serially connected each other....”[0093]: “As shown in FIG. 4, the **nonvolatile semiconductor memory device 100** (the memory cell strings MS)....”

186. **Fukuzumi** discloses a “nonvolatile semiconductor memory device.”

Fukuzumi, [0093].

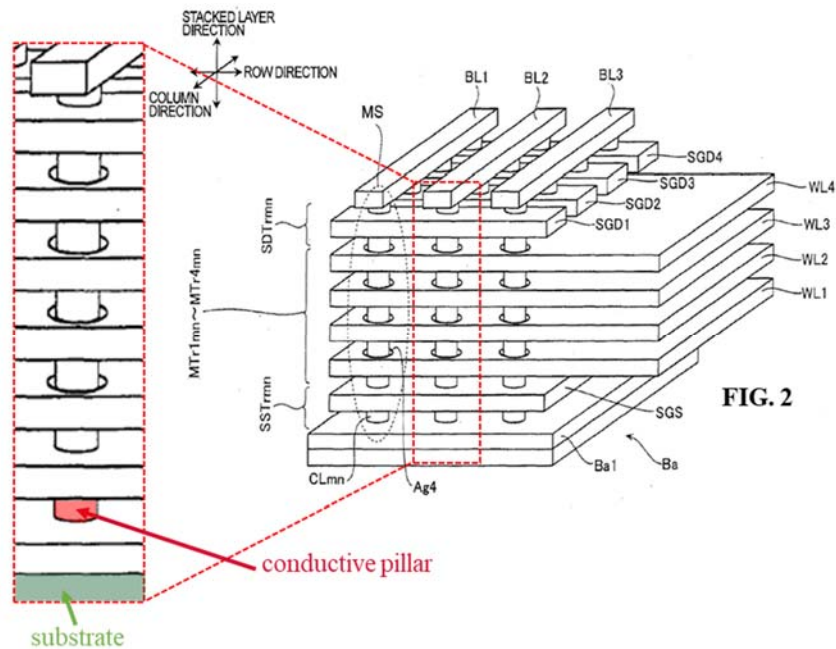
b. Element [1.a]

187. **Element [1.a]** recites “**conductive pillars extending outward from a substrate.**” This element is met by Fukuzumi.

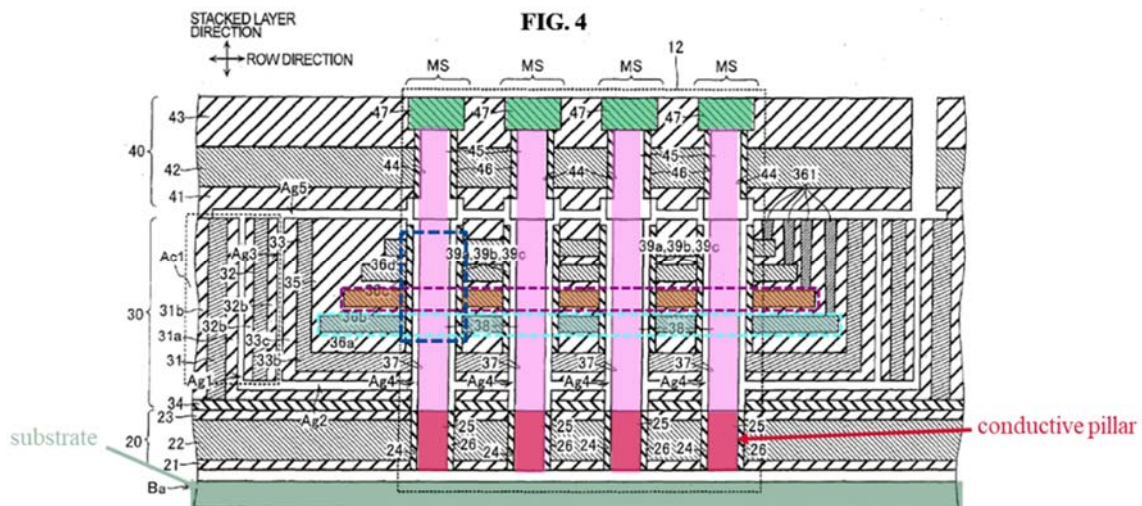
188. Fukuzumi discloses conductive pillars (*e.g.*, “source-side columnar semiconductor layer 25”; “source-side columnar semiconductor 25”) extending outward from a substrate (*e.g.*, “formed to perpendicular the semiconductor

substrate Ba’’). See, e.g., Fukuzumi:

- Figure 2 (annotated)



- Figure 4 (annotated)



- Abstract: “a *columnar semiconductor layer perpendicularly extending toward a substrate;*”
- [0081]: “*Each of the memory strings MS includes columnar semiconductors CLmn on a p-well region Ba1 formed in an n+region*

of a semiconductor substrate Ba. In FIG. 2, for example, m equals from 1 to 3 and n equals from 1 to 4. Each of the columnar semiconductors CL_{mn} are formed to perpendicular the semiconductor substrate Ba, and the columnar semiconductors CL_{mn} are displaced like a matrix above the semiconductor substrate Ba and the word lines WL1-WL4. Thus, the memory strings MS are also displaced like a matrix in a plane perpendicular to the columnar semiconductors CL_{mn}.”

- [0088]: “*The source-side selection transistors SST_{rmn} includes the columnar semiconductor CL_{mn}, the insulation layer surrounding the columnar semiconductor CL_{mn} and the source-side selection gate line SGS surrounding the insulation layer.*”
- [0095]: “*The source-side selection transistor layer 20 includes a first source-side insulation layer 21 formed on the source line layer (acting as the source line SL) of the semiconductor substrate Ba, a source-side conductive layer 22 formed on the first source-side insulation layer 21 and a second source-side insulation layer 23 formed on the source-side conductive layer 22.*”
- [0096]: “Further, *the source-side selection transistor layer 20 includes a source-side hole 24 passing through the first source-side insulation layer 21, the source-side conductive layer 22, the second source-side insulation layer 23 and a source-side columnar semiconductor layer 25.*”
- [0116]: “...the source-side transistor layer 20 is formed on the semiconductor substrate Ba.”

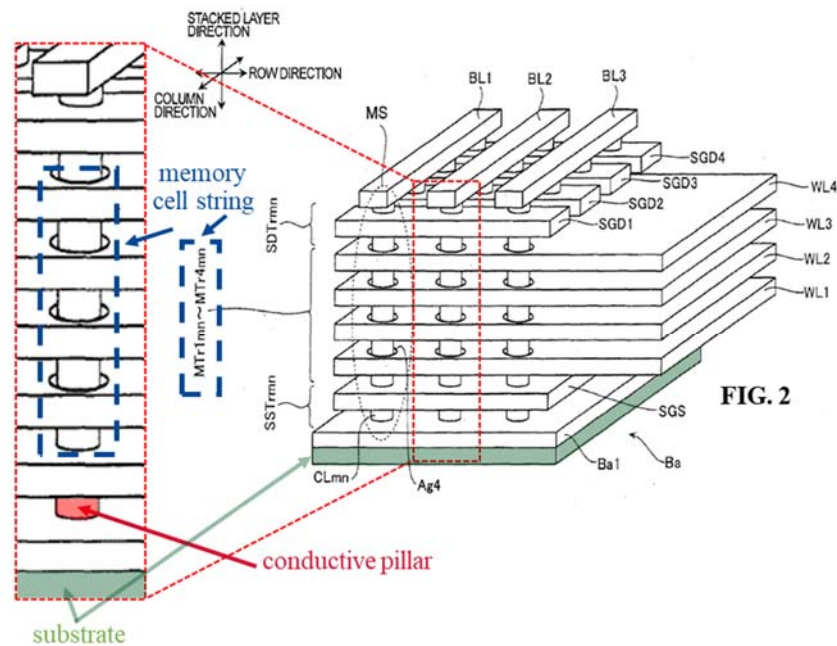
189. Fukuzumi discloses source-side columnar semiconductor layers 25, which extends perpendicular to and, therefore outward from, semiconductor substrate Ba. Fukuzumi, [0081], [0096], Fig. 4.

c. Element [1.b]

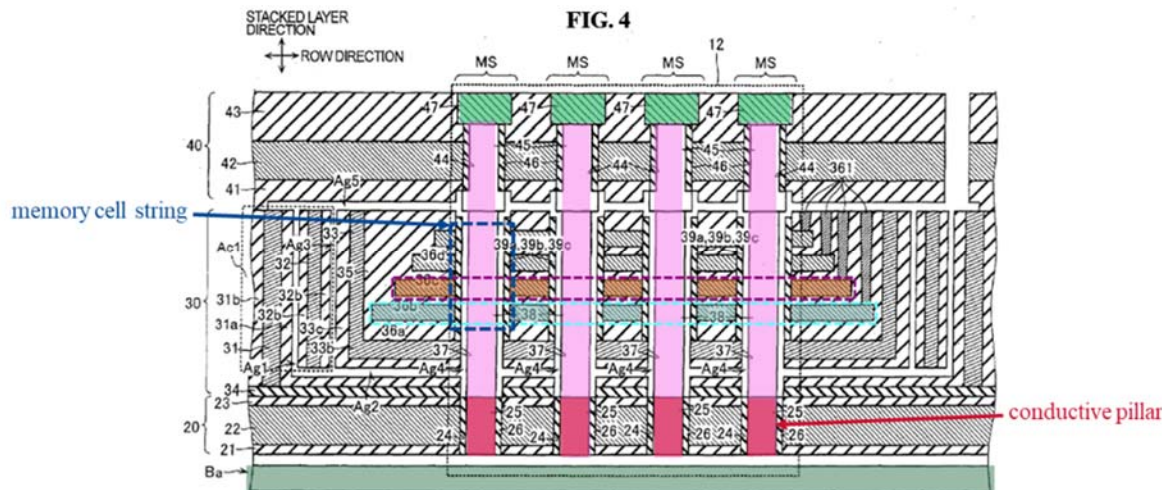
190. Element [1.b] recites “memory cell strings, each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars.” This element is met by Fukuzumi.

191. Fukuzumi discloses memory cell strings (*e.g.*, “MTr1mn-MTr4mn”), each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars (*e.g.*, formed over an “aligning source-side columnar semiconductor layer 25”). *See, e.g.*, Fukuzumi:

- Figure 2 (annotated)



- Figure 4 (annotated)



- [0076]: "...The memory cell region 12 **includes memory cells memorizing data....**"
- [0077]: "...**the memory cells constituting the memory cell region 12 are formed by stacking a plurality of semiconductor layers in order. Further, each layer of the word lines WL is two-dimensionally extended in a prescribed area as shown in FIG. 1.** Each layer of the word lines WL has a plane structure of a single layer."
- [0078]: "FIG. 2 is a part of a perspective schematic view **showing the memory cell region 12 in the nonvolatile semiconductor memory device 100 according to the first embodiment.**"
- [0079]: "...**the memory cell region 12 includes $m \times n$ numbers (m and n being counting numbers) of memory strings MS being constituted with memory cells $MTr1mn-MTr4mn$, source-side selection transistors $SSTrmn$ and drain-side selection transistor $SDTrmn$.** In Fig. 2, m and n equals to three and four, respectively, as an example."
- [0080]: "**Each of the word lines WL1-WL4 is connected to each gate of the memory cells $MTr1mn-MTr4mn$ in each of the memory strings MS** and each of the word lines WL1-WL4 are formed of the same conductive layer and are common in plane each other. ... Further, each of the word line WL1-WL4 is configured nearly perpendicular to the memory strings MS."
- [0081]: "**Each of the memory strings MS includes columnar semiconductors $CLmn$** on a p-well region Ba1 formed in an n+region of

a semiconductor substrate Ba. In FIG. 2, for example, ***m equals from 1 to 3 and n equals from 1 to 4***. Each of the columnar semiconductors CL_{mn} are formed to perpendicular the semiconductor substrate Ba, and the ***columnar semiconductors CL_{mn} are displaced like a matrix above the semiconductor substrate Ba and the word lines WL1-WL4.***

- [0085]: “In the first embodiment as shown in FIG. 2 and FIG. 3, the memory string MS includes ***four memory cells MTr1_{mn}-MTr4_{mn}***, the source-side selection transistors SST_{rm} and the drain-side selection transistor SDTr_{mn}.”
- [0093]: “As shown in Fig. 4, the nonvolatile semiconductor memory device 100 (the memory strings MS) includes a source-side selection transistor layer 20, a memory layer 30 and a drain-side selection transistor layer 40 in order from a lower layer towards an upper layer....***The memory layer 30 acts as the memory cells Mtr_{mn}.***”
- [0103]: “Further, ***a memory hole 37 is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth word line conduction layers 36a-36d***, the third frame bottom layer 33b, the third protective layer 33c, the first protective layer 31a and the isolation insulator 34. ***A memory 38 is formed at a portion as aligning the source-side columnar semiconductor 25 in the memory hole 37.***”
- [0104]: “...a block insulation layer 39a, ***a charge storage layer 39b*** and a tunnel insulation layer 39c are ***formed on sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37*** in order.”

192. See my discussion of element [1.a] above in Section IX.C.2.b.

193. Fukuzumi further discloses each of the memory cells MTr1_{mn}-MTr4_{mn} in “memory hole 37” “formed at a portion as aligning” such that they are coupled to and formed above “the source-side columnar semiconductor 25.”

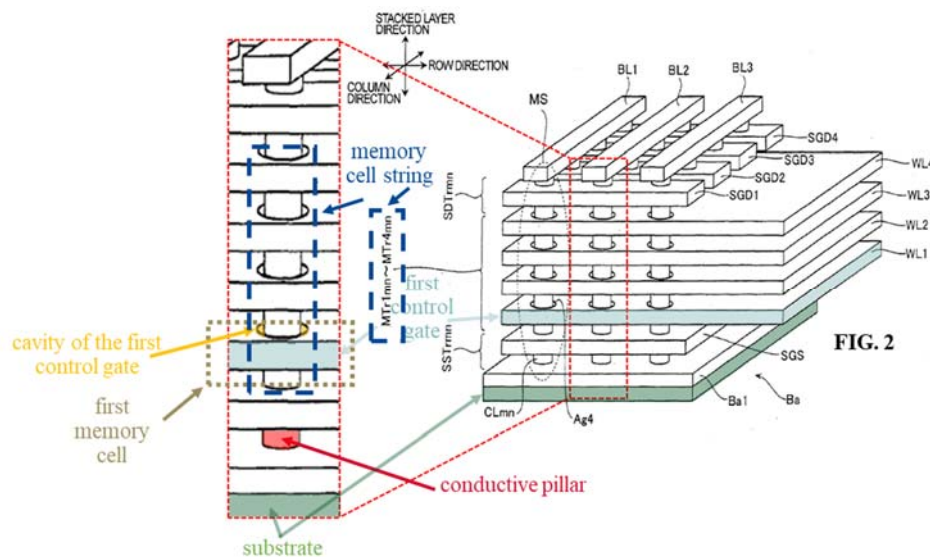
Fukuzumi, [0087], [0093], [0103], Fig. 4.

d. Element [1.c]

194. Element [1.c] recites “a first control gate formed in a first device level, the memory cell strings including a memory cell string, the memory cell string including a first memory cell having a memory element formed in a cavity of the first control gate.” This element is met by Fukuzumi.

195. Fukuzumi discloses a first control gate formed in a first device level (e.g., “end portion” of “word line” WL1 “acts as a control gate”; “word line conduction layer” 36a), the memory cell strings including a memory cell string (e.g., “memory cells MTr1mn-MTr4mn”), the memory cell string including a first memory cell (e.g., “memory cell” at “word line” WL1) having a memory element (e.g., “charge storage layer” 39b) formed in a cavity (e.g., “memory hole 37”) of the first control gate. See, e.g., Fukuzumi:

- Figure 2 (annotated)



- Figure 6 (annotated)

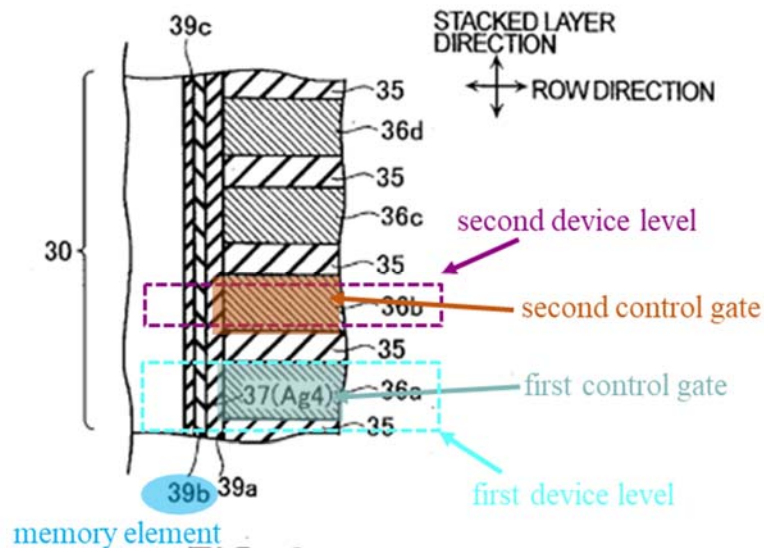


FIG. 6

- [0079]: “...**the memory cell region 12 includes $m \times n$ numbers (m and n being counting numbers) of memory strings MS being constituted with memory cells $MTr1mn$ - $MTr4mn$, source-side selection transistors $SSTrnm$ and drain-side selection transistor $SDTrmn$. In FIG. 2, m and n equals to three and four, respectively, as an example.**”
- [0080]: “Each of the word lines $WL1$ - $WL4$ is connected to each gate of the memory cells $MTr1\ mn$ - $MTr4\ mn$ in each of the memory strings MS and each of the word lines $WL1$ - $WL4$ are formed of the same conductive layer and are common in plane each other. **The memory cell $MTr1\ mn$ in each of the memory strings MS has a structure of a transistor and all gates of memory cells $MTr1\ mn$ are connected to a word line $WL1$.** Further, all gates of memory cells $MTr2\ mn$ in each of the memory strings MS are connected to a word line $WL2$. Further, all gates of memory cells $MTr3\ mn$ in each of the memory strings MS are connected to a word line $WL3$. Further, all gates of memory cells $MTr4\ mn$ in each of the memory strings MS are connected to a word line $WL4$.”
- [0087]: “**Each of the memory cells $Mtrmm$ includes the columnar semiconductor $CLmn$, the insulation layer surrounding the columnar semiconductor $CLmn$ via the space $Ag4$ as shown in Fig. 2, a charge storage layer (not illustrated in FIG. 2 and FIG. 3) and the word line WL surrounding the insulation layer and the charge storage layer. And end portion of the word line WL contacting with the charge storage layer**

surrounded by the insulator act as a control gate of the memory cell MTrmn. A source and a drain of each of the memory cells MTrmn are formed in each of the columnar semiconductors CLmn.”

- [0090] “...*reading out data, writing in data and erasing data are performed by controlling electrical charges of the charge storage layer* in the prescribed memory cell.”
- [0101]: “An interlayer insulator 35 is formed on a top surface of the third frame bottom layer 33. Further, first-fourth word line conduction layers 36 a-36 d between the interlayer insulators 35 are formed. ***The first-fourth word line conduction layer layers 36 a-36 d act as the word lines WL1-WL4.***”
- [0103]: “Further, a memory hole is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth word line conduction layers 36a-36d, the third frame bottom layer 33b, the third protective layer 33c, the first protective layer 31a and the isolation insulator 34. ***A memory 38 is formed at a portion as aligning the source-side columnar semiconductor in the memory hole 37.*** The memory 38 is formed of silicon....”
- [0104]: “...a block insulation layer 39a, ***a charge storage layer 39b*** and a tunnel insulation layer 39c are ***formed on sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37 in order.***”
- [0114]: “...when the fourth word line conduction layer 36d is applied to voltage, the memory 38 is performed to ***write in data into the approached portion of the charge storage layer 39b and read out data from the approached portion of the charge storage layer 39b.***”

196. See my discussion of element [1.b] above in Section IX.C.2.c.

197. Fukuzumi also discloses word lines WL1-WL4, which are also called “first-fourth word line conduction layers 36a-36d,” “connected to each gate of the memory cells MTr1mn-MTr4mn in each of the memory strings MS,” such that an “end portion of the word line WL” acts as the “control gate of the memory cell.”

Fukuzumi, [0080], [0087], [0101]. Fukuzumi further discloses “memory hole 37” that passes through the word line conduction layers 36a-36d. Fukuzumi, [0103]. Fukuzumi’s charge storage layer 39b is formed on “sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37” to store charges. Fukuzumi, [0090], [0104].

198. For example, first word line conduction layer 36a or WL1 serves as a first control gate, and first memory cell includes charge storage layer 39b formed inside memory hole 37 on the sidewall of word line conduction layer 36a.

199. To the extent the term “cavity of the first control gate” requires the memory hole in the control gate to have a larger diameter than the holes in the layers above and below the control gate, Fukuzumi also discloses a second embodiment where “charge storage layer 391b” is formed as “a concavo-convex shape accompanying” word line conduction layer 361a. Fukuzumi, [0148]. In this embodiment, interlayer layers 351 above and below word line conduction layer 361a have holes with smaller diameters than the memory hole at word line conduction layer 361a. *See, e.g.*, Fukuzumi:

- Figure 28 (annotated)

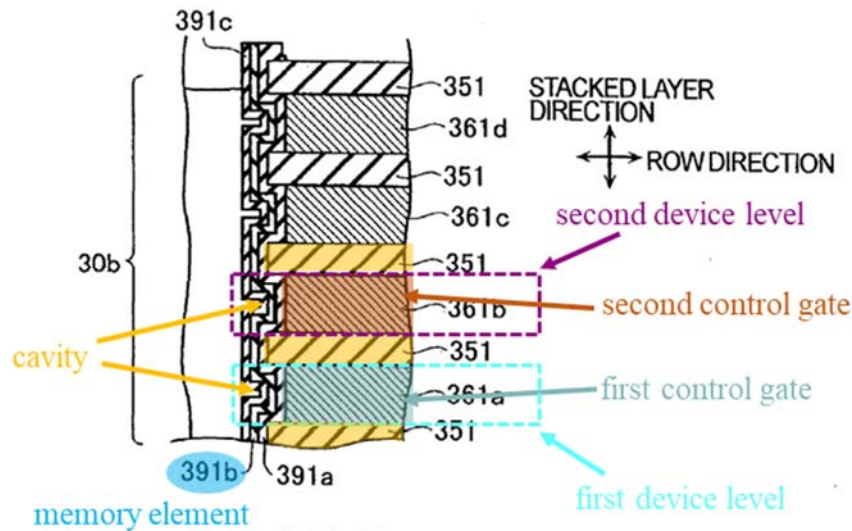


FIG. 28

- [0146]: “**FIG. 28 is a partially enlarged cross-sectional schematic view showing the nonvolatile memory semiconductor device according to the second embodiment.** It is to be noted that the same or similar reference numerals in the second embodiment are applied to the same or similar parts and elements throughout the drawings as the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified.”
- [0148]: “**A sidewall of first-fourth word line conduction layers 361 a-361 d faced to the fourth space Ag4 are formed as recesses corresponding to a side wall of an interlayer insulator 351. Further, surfaces of a block insulation layer 391 a, a charge storage layer 391 b and a tunnel insulation layer 391 c faced to the fourth space Ag4 (not illustrated) are formed as a concavo-convex shape accompanying with the first-fourth word line conduction layer 361 a-361 d.**”
- [0200]: “Other embodiments of the present invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and example embodiments be considered as exemplary only, with a true scope and spirit of the invention being indicated by the claims that follow. **The invention can be carried out by being variously modified within a range not deviated from the gist of the invention.**”

200. Fukuzumi explains that the parts omitted in this second embodiment

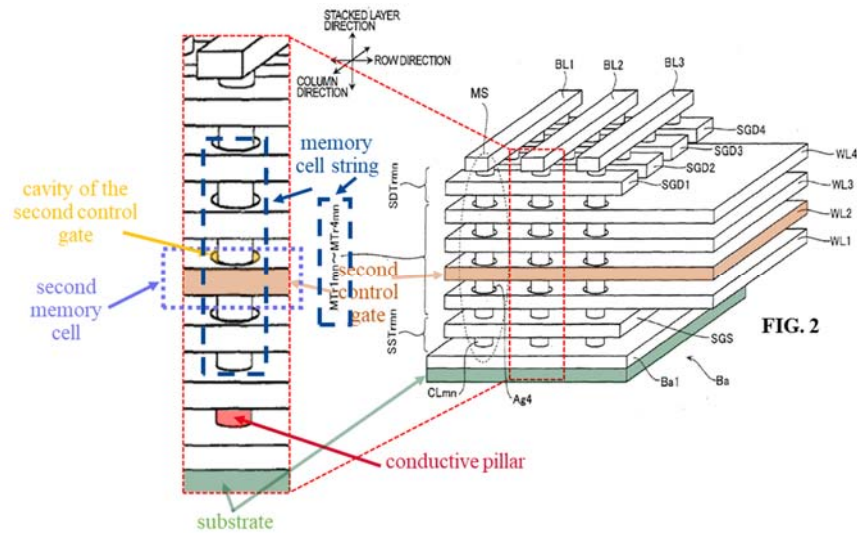
are “the same or similar” as the first embodiment discussed in the rest of this Ground. Fukuzumi, [0146]-[0151]. Figure 28, which illustrates the second embodiment, shows only the word line conduction layer 361, interlayer layers 351, and block insulation layer 391a, a charge storage layer 391b and a tunnel insulation layer 391c. Fukuzumi, [0146]-[0151], Fig. 28. Thus, a person of ordinary skill in the art would have understood (or at least found it obvious) that the analysis for other limitations based on the first embodiment of Fukuzumi would apply equally to Fukuzumi’s second embodiment. [0146].

e. Element [1.d]

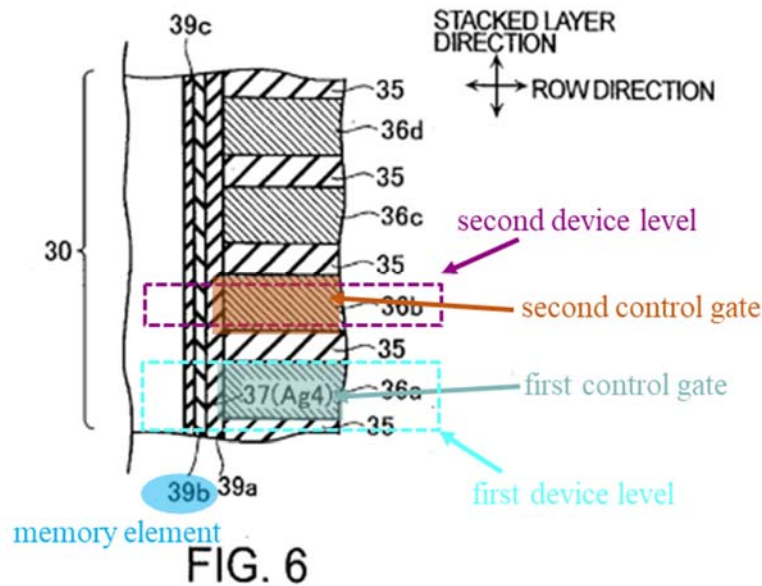
201. **Element [1.d] recites “a second control gate formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the second control gate.”** This element is met by Fukuzumi.

202. Fukuzumi discloses a second control gate formed in a second device level (*e.g.*, “end portion” of “word line” WL2 or “word line conduction layer” 36b “acts as a control gate”), the memory cell strings (*e.g.*, “memory cells MTr1 *mn*-MTr4 *mn*”) including a memory cell string, the memory cell string including a second memory cell (*e.g.*, “memory cell” at “word line” WL2) having a memory element (*e.g.*, “charge storage layer” 39b) formed in a cavity (*e.g.*, “memory hole 37”) of the second control gate. *See, e.g.*, Fukuzumi:

- Figure 2 (annotated)



- Figure 6 (annotated)



- [0079]: “...the memory cell region 12 includes $m \times n$ numbers (m and n being counting numbers) of memory strings MS being constituted with memory cells $MTr1mn-MTr4mn$, source-side selection transistors $SSTrmn$ and drain-side selection transistor $SDTrmn$. In FIG. 2, m and n equals to three and four, respectively, as an example.”

- [0080]: “Each of the word lines WL1-WL4 is connected to each gate of the memory cells MTr1 *mn*-MTr4 *mn* in each of the memory strings MS and each of the word lines WL1-WL4 are formed of the same conductive layer and are common in plane each other. ***The memory cell MTr1 mn in each of the memory strings MS has a structure of a transistor and all gates of memory cells MTr1 mn are connected to a word line WL1.*** Further, all gates of memory cells MTr2 *mn* in each of the memory strings MS are connected to a word line WL2. Further, all gates of memory cells MTr3 *mn* in each of the memory strings MS are connected to a word line WL3. Further, all gates of memory cells MTr4 *mn* in each of the memory strings MS are connected to a word line WL4.”
- [0087]: “***Each of the memory cells Mtrmm includes the columnar semiconductor CLmn***, the insulation layer surrounding the columnar semiconductor CLmn via the space Ag4 as shown in Fig. 2, a charge storage layer (not illustrated in FIG. 2 and FIG. 3) ***and the word line WL surrounding the insulation layer and the charge storage layer. And end portion of the word line WL contacting with the charge storage layer surrounded by the insulator act as a control gate of the memory cell Mtrmn.*** A source and a drain of each of the memory cells MTrmn are formed in each of the columnar semiconductors CLmn.”
- [0090] “***...reading out data, writing in data and erasing data are performed by controlling electrical charges of the charge storage layer in the prescribed memory cell.***”
- [0101]: “An interlayer insulator 35 is formed on a top surface of the third frame bottom layer 33. Further, first-fourth word line conduction layers 36 a-36 d between the interlayer insulators 35 are formed. ***The first-fourth word line conduction layer layers 36 a-36 d act as the word lines WL1-WL4.***”
- [0103]: “Further, a memory hole is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth word line conduction layers 36a-36d, the third frame bottom layer 33b, the third protective layer 33c, the first protective layer 31a and the isolation insulator 34. ***A memory 38 is formed at a portion as aligning the source-side columnar semiconductor in the memory hole 37.*** The memory 38 is formed of silicon....”

- [0104]: “...a block insulation layer 39a, **a charge storage layer 39b** and a tunnel insulation layer 39c are **formed on sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37 in order.**”
- [0114]: “...when the fourth word line conduction layer 36d is applied to voltage, the memory 38 is performed to **write in data into the approached portion of the charge storage layer 39b and read out data from the approached portion of the charge storage layer 39b.**”

203. See my discussion of elements [1.b] and [1.c] above in Section IX.C.2.c-d.

204. Fukuzumi further discloses a second device level at which second word line conduction layer 36b or WL2 is located—a second memory cell includes charge storage layer 39b formed on second word line conduction layer 36b in memory hole 37. Fukuzumi, [0080], [0101], [0103]-[0104].

205. Further, as I explain in connection with element [1.c], to the extent the term “cavity of the second control gate” requires the memory hole in the control gate to have a larger diameter than the holes in the layers above and below the control gate, Fukuzumi also discloses this limitation.

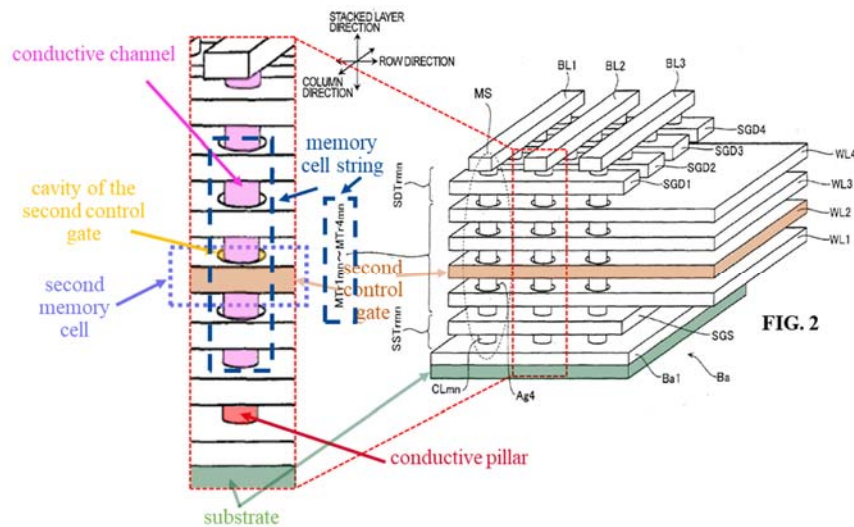
f. Element [1.e]

206. Element [1.e] recites “**a conductive channel extending between the first memory cell and the second memory cell and electrically coupled to a conductive pillar of the conductive pillars.**”

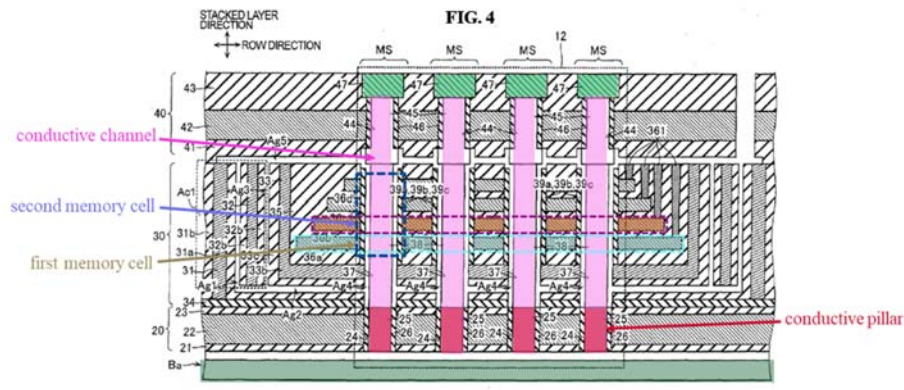
207. Fukuzumi discloses a conductive channel (*e.g.*, “memory 38”)

extending between the first memory cell and the second memory cell (*e.g.*, “memory cells” at “word lines” WL1 and WL2) and electrically coupled to a conductive pillar of the conductive pillars (*e.g.*, formed on and “aligning the source-side columnar semiconductor 25” as illustrated in Fig. 4). See, *e.g.*, Fukuzumi:

- Figure 2 (annotated)%



- Figure 4 (annotated)%



- [0085]: “...the memory string MS includes four memory cells MTr1 *mn*-Mtr4 *mn*, the source-side selection transistors SSTrm and the drain-side selection transistor SDTrmn. **These four memory cells MTr1 *mn*-MTr4**

mn, the source-side selection transistors SStrm and the drain side selection transistor SDtrmn are serially connected each other....”

- [0086]: “As shown in FIG. 4, in the first embodiment of the memory strings MS, ***the columnar semiconductor CLmn is formed on an n+-region formed in a p-type region (p-Well region) Ba1 of a semiconductor substrate Ba. Thus, source line SL is connected to a source of the source-side selection transistors SStrmn.*** The source means the n+-region formed in the p-well region Ba1 of the semiconductor substrate Ba.”
- [0087]: “***Each of the memory cells Mtrmm includes the columnar semiconductor CLmn, the insulation layer surrounding the columnar semiconductor CLmn via the space Ag4 as shown in Fig. 2, a charge storage layer (not illustrated in FIG. 2 and FIG. 3) and the word line WL surrounding the insulation layer and the charge storage layer.*** A source and a drain of each of the memory cells MTrmn are formed in each of the columnar semiconductors CLmn”
- [0088]: “The source-side selection transistors SStrmn ***includes the columnar semiconductor CLmn....”***
- [0089]: “The drain-side selection transistors SDTrmn ***include the columnar semiconductors CLmn....”***
- [0103]: “***...a memory hole 37 is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth wordline conduction layers 36a-36d.... A memory 38 is formed at a portion as aligning the source-side columnar semiconductor 25 in the memory hole 37.***”
- [0104]: “...a block insulation layer 39a, ***a charge storage layer 39b*** and a tunnel insulation layer 39c are ***formed on sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37 in order....”***

208. See my discussion of elements [1.a]-[1.d] above in Section IX.C.2.b-

e.

209. Fukuzumi further discloses silicon “memory 38[] formed at a portion

aligning the source-side columnar semiconductor 25 in the memory hole 37,” which penetrates through the memory cells at word lines WL1 and WL2. Fukuzumi, [0103]. The memory cells (including memory 38 forming the conductive channel) and the source-side selection transistors SSTrmn “are serially connected each other” such that memory 38 in the memory cells and source-side columnar semiconductor 25 in the source-side selection transistors SSTrmn are electrically coupled. Fukuzumi, [0085].

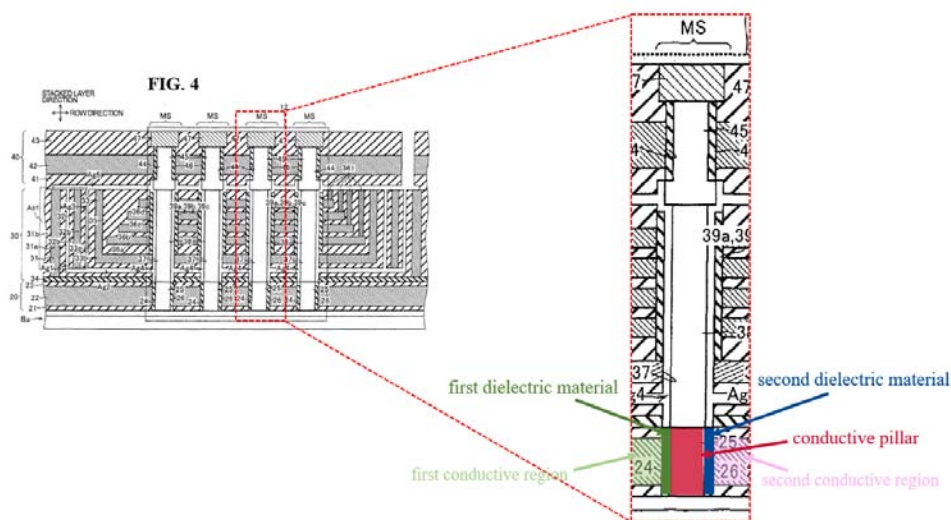
g. Element [2.a] and [2.b]

210. **Element [2.a] recites “The apparatus of claim 1, further comprising: a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material.” Element [2.b] recites “a second conductive region located on a second side opposite from the first side of the conductive pillar and separated from the conductive pillar by a second dielectric material.”** See my discussion of claim [1] above in Section IX.C.2.a-f. The added limitations of elements [2.a] and [2.b] are met by Fukuzumi.

211. Fukuzumi discloses a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material, and a second conductive region located on a second side of the conductive pillar and separated from the conductive pillar by a second dielectric

material (*e.g.*, portions of “source-side conductive layer 22” located on the left and right sides of “source-side columnar semiconductor layer 25,” respectively, and portions of “source-side gate insulation layer 26” respectively separating the left and right sides of “source-side conductive layer 22” from “source-side columnar semiconductor layer 25,” as shown in Fig. 4). *See, e.g.*, Fukuzumi:

- Figure 4 (annotated)



- [0096]: “Further, the source-side selection transistor layer 20 includes a *source-side hole 24 passing through the first source-side insulation layer 21, the source-side conductive layer 22, the second source-side insulation layer 23 and a source-side columnar semiconductor layer 25. A source-side gate insulation layer 26 is formed between a sidewall of the source-side columnar semiconductor layer 25 and the first source-side insulation layer 21, the source-side conductive layer 22 and the second source-side insulation layer 2. The source-side gate insulation layer 26 is formed of silicon-dioxide.*”

212. See my discussion of claim [1.a] above in Section IX.C.2.b.

213. Fukuzumi also discloses source-side hole 24 that passes through source-side conductive layer 22, and source-side columnar semiconductor layer 25

that is formed inside source-side hole 24, such that first and second regions of source-side conductive layer 22 are on the left and right sides of source-side columnar semiconductor layer 25, respectively, as shown in Figure 4. Fukuzumi, [0096], Fig. 4. Fukuzumi further discloses “source-side gate insulation layer 26[] formed between a sidewall of the source-side columnar semiconductor layer 25 and ... the source-side conductive layer 22.” Fukuzumi, [0096]. As a result, first and second portions of source-side gate insulation layer 26 separate the first and second regions of source-side conductive layer 22 from source-side columnar semiconductor layer 25.

214. I have reviewed Patent Owner’s Disclosure of Asserted Claims and Infringement Contentions and Document Production Accompanying Disclosure (Patent Local Rules 3-1 and 3-2) in the YMTC Litigation. Ex. 1018, Ex. D-2 at 6-8. My analysis above in ¶¶ 211-213 is consistent with Patent Owner’s assertion in its Infringement Contentions in that the first and second conductive regions and dielectric materials are located on opposite sides of the conductive pillar. For example, in its Infringement Contentions, Patent Owner points to a cross section of a source-select transistor and refers to a portion of a gate plane as a “First conductive region” and another portion of the same gate plane on the opposite side of the channel as a “Second conductive region.” Ex. 1018, Ex. D-2 at 6-8. Similarly, Patent Owner points to a portion of a dielectric material surrounding the

channel of the source-select transistor as a “First dielectric material” and another portion of the same dielectric material on the opposite side of the channel as a “Second dielectric material.” *Id.*

215. To the extent the term “a second conductive region located on a second side opposite from the first side of the conductive pillar” requires the first and second conductive regions to be located on two opposite sides of the conductive pillar, and otherwise electrically isolated from the pillar, it is still my opinion that Fukuzumi teaches (or at least renders obvious) the limitation.

216. For example, Fukuzumi’s third embodiment discloses a “slit” memory hole 371 where “both ends of the row direction in the memory hole 371 are formed like a line.” Fukuzumi, [0155], Fig. 29. *See, e.g.*, Fukuzumi:

- Figure 29 (annotated)

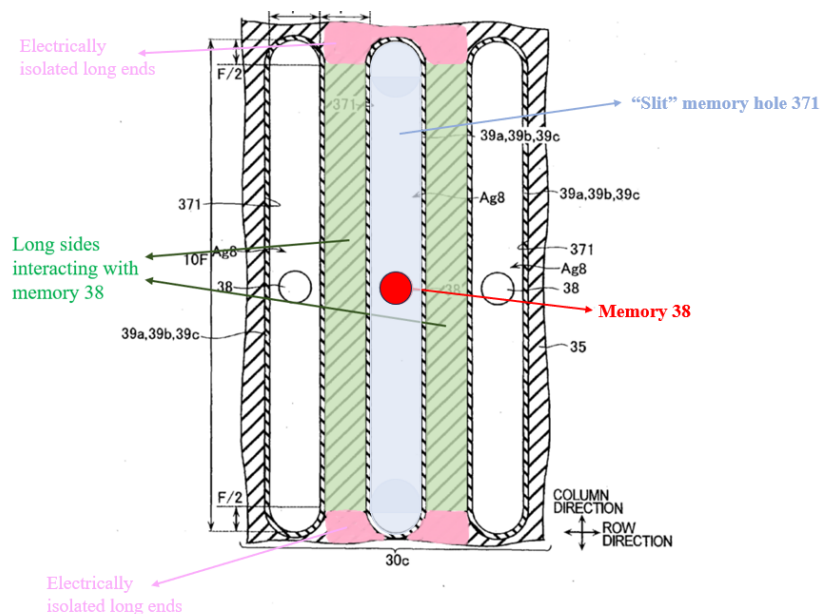
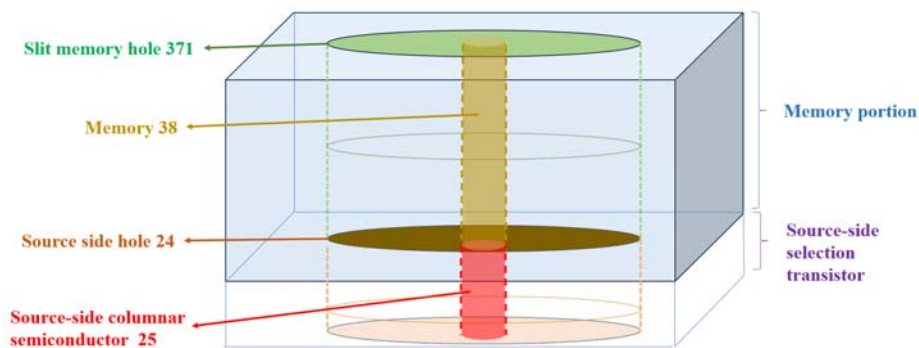


FIG. 29

217. As illustrated above, in this structure, a person of ordinary skill in the art would have understood that the gate surrounding “slit” memory hole 371 functions as a double-gate where word line conduction layers 36a-d on two opposite long sides of slit memory hole 371 electrically interact with memory 38, while the portions of 36a-d at the long ends of slit memory hole 371 are electrically isolated from and, thus, do not impact the operation of memory 38. Fukuzumi, [0155], Fig. 29.

218. Moreover, a person of ordinary skill in the art would have understood (or at least found it obvious) that the same “slit” structure would also be used for source-side hole 24. Fukuzumi, [0153], [0200]. A figure is created to illustrate the configuration below:



219. For example, using the same “slit” memory hole structure to source-side hole 24 would advantageously allow the source-selection and memory transistors in a memory string to be formed within the same hole, including both memory 38 and source-side columnar semiconductor 25, which would allow

simplified manufacturing by, e.g., reducing the number of masks and masking steps needed. Indeed, U.S. Patent Application Publication No. 2007/0057328 (“Taniguchi”), which I understand has been designated as Exhibit 1026, recognizes this is advantageous, teaching that “it is preferable that[] mask pattern is made the same” for different manufacturing steps “so as not to increase the number of mask patterns.” Ex. 1026, [0062]; *see also id.*, [0066]-[0067]. Using the same mask pattern would also allow different components (e.g., memory hole and source-side hole 24) to be formed at the same time, and thus “[t]he number of processes can therefore be reduced.” *Id.*, [0043]; *see also id.*, [0034], [0036], [0042], [0142]. Reducing the number of processes is beneficial in the context of the use of lithography in fabricating memory devices, because additional processing steps add additional defects and reduces yield as recognized by a 2009 article, for the well-known and readily-accessible *IEEE Spectrum* publication (that would have been accessible to a person of ordinary skill in the art, e.g., through the IEEE website or a library), titled “Shrinking Possibilities” by B. Arnold, which I understand has been designated as Exhibit 1027. *See* Ex. 1027 (“Double patterning also demands more process steps, which again adds to the cost by cutting effective throughput, increasing fab cycle time, and adding additional defects. If your original process could yield 100 wafers an hour, using double patterning will leave you with much less. If you’d been turning a profit at 100 per

hour, there's no guarantee you will at 50."). In this implementation, portions of source-side gate insulation layer 26 separate the regions of source-side conductive layer 22 from source-side columnar semiconductor layer 25. Fukuzumi, [0096]. In particular, because the source-side columnar semiconductor layer 25 must be insulated from the source-side conductive layer 22, the same insulation layer 26 used in the first embodiment would also be used in the third embodiment illustrated in Figure 29.

220. A person of ordinary skill in the art would have had a reasonable expectation of success in applying "slit" hole—which is effectively a double-gate—structure to the source-side hole 24, as the use of double-gate structure for source-side selection transistors was well known in the art. For example, U.S. Patent Application Publication No. 2009/0310425 ("Sim"), which I understand has been designated as Exhibit 1012, discloses forming gate patterns that are double-gates, where the "lower-most gate pattern 201'," a double-gate, functioning as a "lower select plate LS_PT." Ex. 1012, [0103]-[0106], Figs. 31-37.

221. Fukuzumi further explains that the parts other than the slit memory hole structure omitted in the third embodiment are "the same or similar" as the first embodiment discussed in the rest of this Ground. Fukuzumi, [0153], Fig. 29. It is therefore my opinion that a person of ordinary skill in the art would have understood (or at least found it obvious) that the analysis for other limitations

relying on the first embodiment of Fukuzumi applies equally to Fukuzumi's third embodiment, as modified to include "slit" source-side hole 24 structure. [0153].

See, e.g., Fukuzumi:

- Figure 29 (as applied to source-side selection transistor)

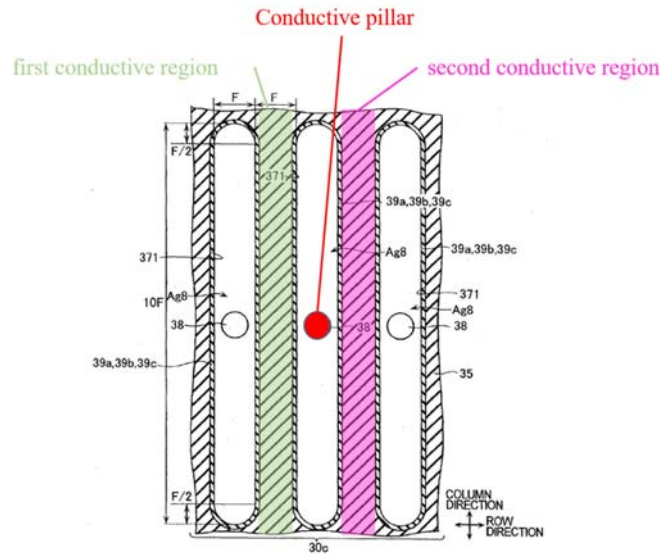


FIG. 29

- [0153]: "FIG. 29 is a part of plain schematic view showing a memory layer of the non-volatile memory semiconductor device according to the third embodiment. It is to be noted that the same or similar reference numerals in the third embodiment are applied to the same or similar parts and elements throughout the drawings in the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified."
- [0155]: "**The memory hole 371 is formed like a slit** which has the row-direction as lateral direction and the column direction as longitudinal direction from top view. **Both ends of the row direction in the memory hole 371 are formed like a line. On the other hand, the column direction of the memory hole 371 is formed like a circular arc.** As a result, an eighth space Ag8 is configured between a sidewall of the memory hole 371 and a sidewall of the memory 38. A perimeter length ratio R1 per unit area of the charge storage layer 39b faced to the

memory hole 371 equals $(18+\pi) F/20F^2$ and nearly equals to $1.06/F$, where, for example, ***a length in the row direction of the both end of the memory hole 371 is “F”, a length in the column direction of the both end of the memory hole 371 is “10F”***, the nearest length of the neighbor memory hole 371 is “F” and the diameter of the circular arc in the both end of the memory hole 371 is “F”).

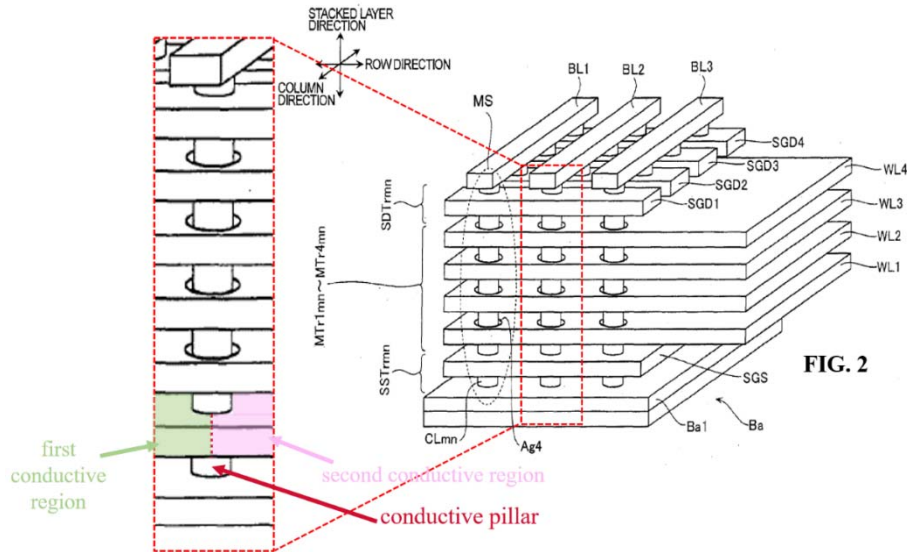
- [0200]: “Other embodiments of the present invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and example embodiments be considered as exemplary only, with a true scope and spirit of the invention being indicated by the claims that follow. ***The invention can be carried out by being variously modified within a range not deviated from the gist of the invention.***”

h. Claim [3]

222. **Claim [3] recites “The apparatus of claim 2, wherein the first conductive region is coupled to the second conductive region.”** See my discussion of claim [2] above in Section IX.C.2.g. The added limitation of claim [3] is met by Fukuzumi.

223. Fukuzumi discloses the first conductive region (*e.g.*, left portion of “source-side conductive layer 22” in Fig. 4) is coupled to the second conductive region (*e.g.*, right portion of “source-side conductive layer 22” in Fig. 4). *See, e.g.*, Fukuzumi:

- Figure 2 (annotated)



- Figure 29 (annotated)

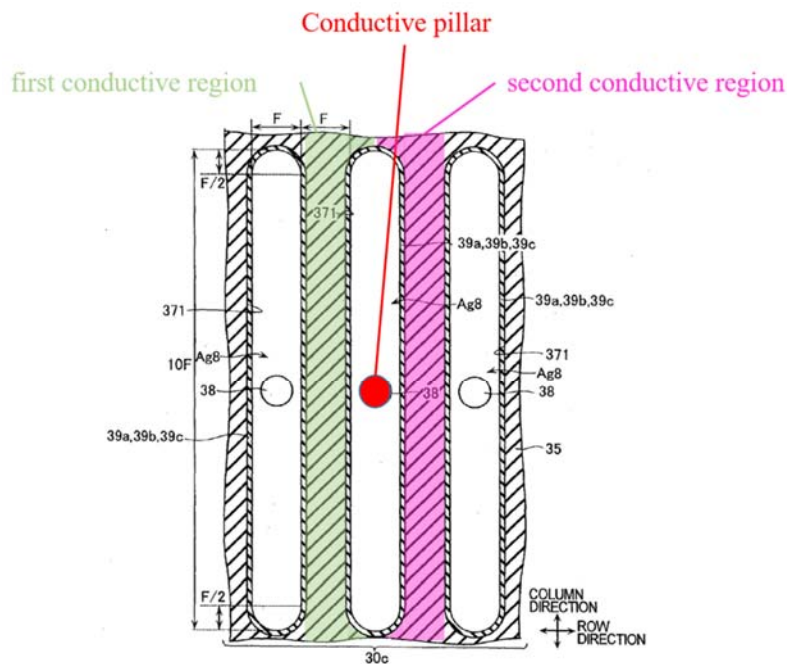


FIG. 29

- [0096]: “Further, the source-side selection transistor layer 20 includes a **source-side hole 24 passing through the first source-side insulation layer 21, the source-side conductive layer 22, the second source-side insulation layer 23 and a source-side columnar semiconductor layer 25. A source-side gate insulation layer 26 is formed between a sidewall of**

the source-side columnar semiconductor layer 25 and the first source-side insulation layer 21, the source-side conductive layer 22 and the second source-side insulation layer 2. The source-side gate insulation layer 26 is formed of silicon-dioxide.”

- [0153]: “FIG. 29 is a part of plain schematic view showing a memory layer of the non-volatile memory semiconductor device according to the third embodiment. It is to be noted that the same or similar reference numerals in the third embodiment are applied to the same or similar parts and elements throughout the drawings in the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified.”
- [0155]: “***The memory hole 371 is formed like a slit*** which has the row-direction as lateral direction and the column direction as longitudinal direction from top view. ***Both ends of the row direction in the memory hole 371 are formed like a line. On the other hand, the column direction of the memory hole 371 is formed like a circular arc.*** As a result, an eighth space Ag8 is configured between a sidewall of the memory hole 371 and a sidewall of the memory 38. A perimeter length ratio R1 per unit area of the charge storage layer 39b faced to the memory hole 371 equals $(18+\pi) F/20F^2$ and nearly equals to $1.06/F$, where, for example, ***a length in the row direction of the both end of the memory hole 371 is “F”, a length in the column direction of the both end of the memory hole 371 is “10F”,*** the nearest length of the neighbor memory hole 371 is “F” and the diameter of the circular arc in the both end of the memory hole 371 is “F”).”

224. See my discussion of element [2.a] and [2.b] above in Section IX.C.2.g.

225. As I explain in connection with element [2.b], Fukuzumi discloses (or at least renders obvious) source-side conductive layer 22 surrounding source-side columnar semiconductor layer 25, such that portions of source-side conductive layer 22 on the first and second sides of source-side columnar semiconductor layer

25 are coupled. Fukuzumi, [0096], [0155]; Figs. 2, 29.

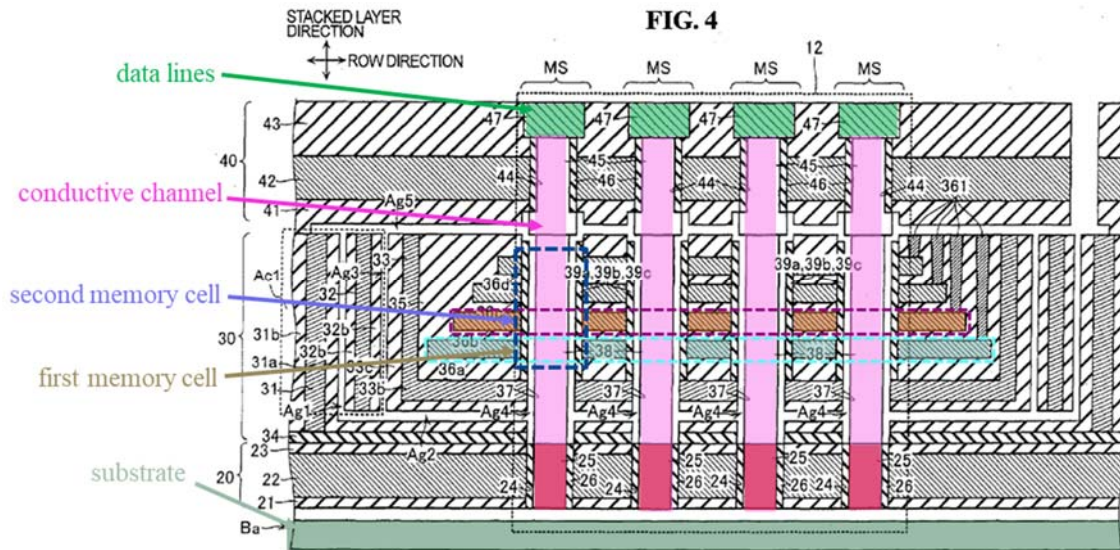
226. I have reviewed Patent Owner’s Disclosure of Asserted Claims and Infringement Contentions and Document Production Accompanying Disclosure (Patent Local Rules 3-1 and 3-2) in the YMTC Litigation. Ex. 1018, Ex. D-2 at 8-9. My analysis above in ¶¶ 223-225 is consistent with Patent Owner’s assertion in its Infringement Contentions. For example, in its Infringement Contentions, Patent Owner points to a cross section of a source-select transistor and refers to a portion of a gate plane as a “First conductive region” and another portion of the same gate plane on the opposite side of the channel as a “Second conductive region.” Ex. 1018, Ex. D-2 at 8-9. Patent Owner argues that those portions of the conductive region are coupled because the “conductive region around the conductive pillar also wrap around the conductive pillar,” just like Fukuzumi’s source-side conductive layer 22 wraps around source-side columnar semiconductor layer 25. *Id.*

i. Claim [7]

227. **Claim [7] recites “The apparatus of claim 1, further comprising a data line coupled to the conductive channel, wherein the first and second memory cells are located between the data line and the substrate.”** See my discussion of claim [1] above in Section IX.C.2.a-f. The added limitation of claim [7] is met by Fukuzumi.

228. Fukuzumi discloses a data line (e.g., “bit line layer 47”) coupled to the conductive channel (e.g., coupled to “memory 38” through drain side columnar semiconductor layer 45), wherein the first and second memory cells (e.g., “memory cells” at “word lines” WL1 and WL2) are located between the data line and the substrate (e.g., between “bit line layer 47” and “substrate Ba”). See, e.g., Fukuzumi:

- Figure 4 (annotated)



- [0081]: “**Each of the memory strings MS includes columnar semiconductors CL_{mn}** on a p-well region Ba1 formed in an n+region of a semiconductor substrate Ba. In FIG. 2, for example, m equals from 1 to 3 and n equals from 1 to 4. **Each of the columnar semiconductors CL_{mn} are formed to perpendicular the semiconductor substrate Ba**, and the columnar semiconductors CL_{mn} are displaced like a matrix above the semiconductor substrate Ba and the word lines WL1-WL4. **Thus, the memory strings MS are also displaced like a matrix in a plane perpendicular to the columnar semiconductors CL_{mn}...**”
- [0083]: “...as shown in FIG. 2, **the drain-side selection gate lines SGD constituting the drain-side selection transistor SDTr_{mn} is configured**

- upper the memory strings MS and contacting the columnar semiconductors CLmn and the insulation layer (not illustrated) via the columnar semiconductor CLmn and the insulation layer.***
- [0085]: “...These four memory cells MTr1mn-MTr4mn, the source-side selection transistors SStrm and the drain side selection transistor SDTrmn are serially connected each other....”
 - [0086]: “...As shown in FIG. 4, ***in the first embodiment of the memory strings MS, the columnar semiconductor CLmn is formed on an n+-region formed in a p-type region (p-Well region) Ba1 of a semiconductor substrate Ba.*** Thus, source line SL is connected to a source of the source-side selection transistors SStrmn. The source means the n+-region formed in the p-well region Ba1 of the semiconductor substrate Ba.... Further, ***the bit line BL is connected to a drain of each of the drain-side selection transistor SDTrmn***”)
 - [0087]: “***Each of the memory cells Mtrmm includes the columnar semiconductor CLmn,*** the insulation layer surrounding the columnar semiconductor CLmn via the space Ag4 as shown in Fig. 2, a charge storage layer (not illustrated in FIG. 2 and FIG. 3) ***and the word line WL surrounding the insulation layer and the charge storage layer.*** A source and a drain of each of the memory cells MTrmn are formed in each of the columnar semiconductors CLmn.”
 - [0089]: “***The drain-side selection transistors SDTrmn include the columnar semiconductors CLmn,*** the insulation layer surrounding the columnar semiconductor CLmn and the drain-side selection gate line SGD surrounding the insulation layer.”
 - [0103]: “Further, a ***memory hole 37 is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth word line conduction layers 36a-36d,*** the third frame bottom layer 33b, the third protective layer 33c, the first protective layer 31a and the isolation insulator 34. ***A memory 38 is formed at a portion as aligning the source-side columnar semiconductor 25 in the memory hole 37....***”
 - [0104]: “...a block insulation layer 39a, ***a charge storage layer 39b*** and a tunnel insulation layer 39c are ***formed on sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37*** in order....”

- [0108]: “Further, *the drain-side selection transistor layer 40* passes through the first drain-side insulation layer 41, the drain-side conductive layer 42 and the second drain-side insulation layer 43, to *include a drain-side hole 44 and a drain-side columnar semiconductor layer 45 formed in the drain-side hole 44.*”
- [0109]: “*A bit line layer 47 is formed at a portion being aligned with the drain-side columnar semiconductor layer 45 and an upper portion of the drain-side columnar semiconductor layer 45.* The bit line layer 47 acts as the bit line BL as shown in FIG. 2.”
- See also Figs. 2-3.

229. See my discussion of element [1.a]-[1.e] above in Section IX.C.2.b-f.

230. Furthermore, Fukuzumi also discloses bit line layers 47 formed on drain-side columnar semiconductor layer 45, where drain-side columnar semiconductor layer 45 is located on memory 38 such that bit line layers 47 are coupled to memory 38 by drain-side columnar semiconductor layer 45. Fukuzumi, [0085], [0089], [0108]-[0109], Fig. 4. Moreover, the first and second memory cells located at WL1 and WL2 along memory 38 are located between bit line layer 47 and substrate Ba. Fukuzumi, Fig. 4

j. Claim [9]

231. Claim [9] recites “**The apparatus of claim 1, wherein the memory element comprises a dielectric material.**” See my discussion of claim [1] above in Section IX.C.2.a-f. The added limitation of claim [9] is met by Fukuzumi.

232. Fukuzumi discloses that the memory element (*e.g.*, “charge storage layer 39b”) comprises a dielectric material (*e.g.*, “silicon-nitride (SiN)”). See, *e.g.*,

Fukuzumi:

- [0104]: “The charge storage layer 39 b is formed of ***silicon-nitride (SiN)***.”

233. See my discussion of element [1.c] above in Section IX.C.2.d.

234. Fukuzumi further discloses charge storage layer 39b formed of silicon nitride. Fukuzumi, [0104]. As disclosed by Raghuram, “dielectric material can be any known electrically insulating material, such as silicon oxide, silicon nitride, or silicon oxynitride.” Ex. 1019, [0071].

k. Element [17.pre]

235. **Element [17.pre] recites “An apparatus comprising.”** This element is met by Fukuzumi. See my discussion of element [1.pre] above in Section IX.C.2.a.

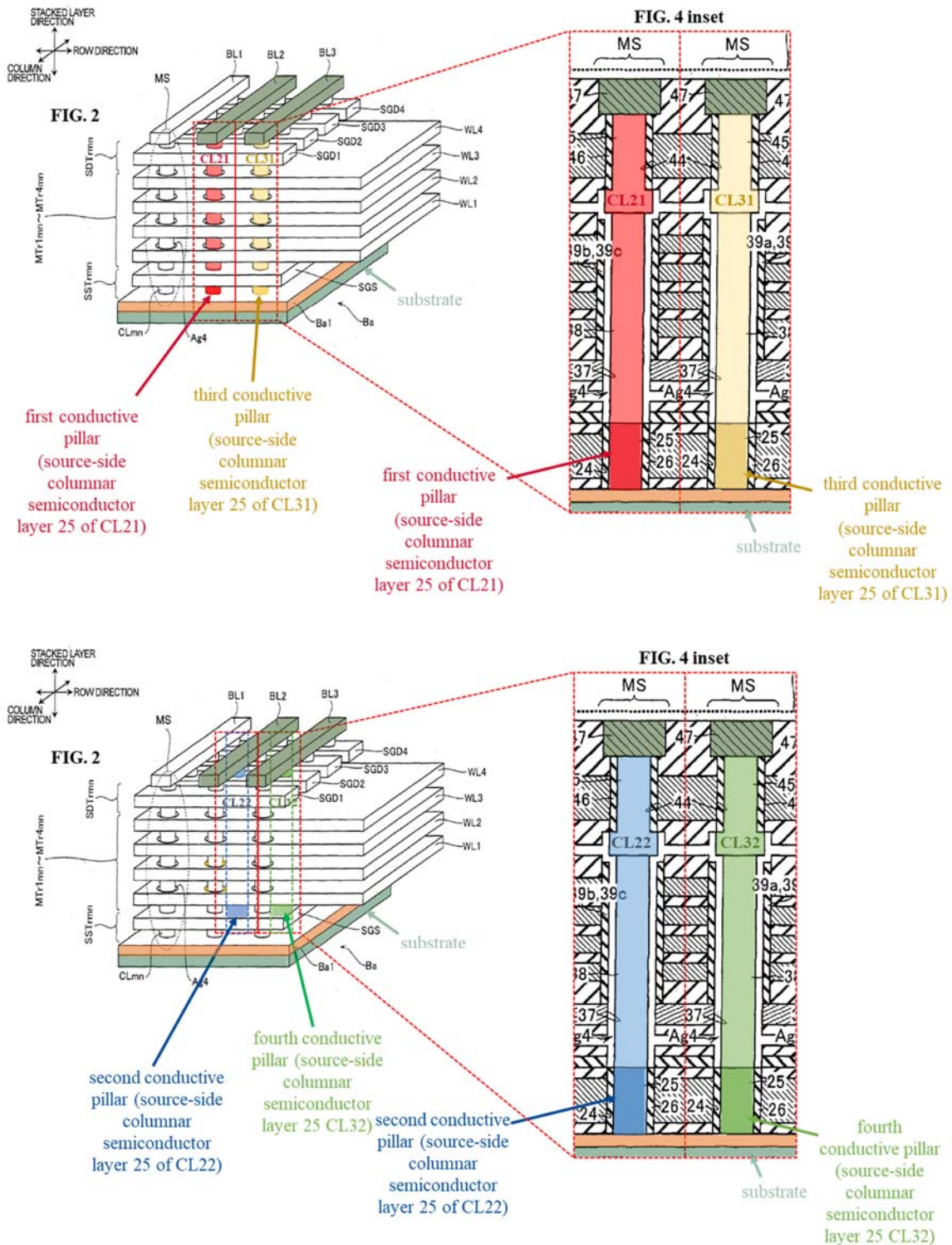
l. Elements [17.a] and [17.b]

236. **Elements [17.a] and [17.b] recites “a first conductive pillar and a second conductive pillar extending outward from a substrate” and “a third conductive pillar and a fourth conductive pillars extending outward from the substrate.”** This element is met by Fukuzumi.

237. Fukuzumi discloses a first conductive pillar, a second conductive pillar, a third conductive pillar, and a fourth conductive pillar (*e.g.*, “source-side columnar semiconductor layer 25” of columnar semiconductors CL21, CL22, CL31, and CL32, respectively) extending outward from the substrate (*e.g.*,

“substrate Ba”). See, e.g., Fukuzumi:

- Figures 2 and 4 (annotated)



- Abstract: “a **columnar semiconductor layer perpendicularly extending toward a substrate;**”
- [0081]: “**Each of the memory strings MS includes columnar semiconductors CL_{mn} on a p-well region Ba1 formed in an n+region of a semiconductor substrate Ba.** In FIG. 2, for example, m equals from 1 to 3 and n equals from 1 to 4. **Each of the columnar semiconductors CL_{mn} are formed to perpendicular the semiconductor substrate Ba, and the columnar semiconductors CL_{mn} are displaced like a matrix above the semiconductor substrate Ba** and the word lines WL1-WL4. Thus, the memory strings MS are also displaced like a matrix in a plane perpendicular to the columnar semiconductors CL_{mn}.”
- [0088]: “**The source-side selection transistors SST_{rmn} includes the columnar semiconductor CL_{mn},** the insulation layer surrounding the columnar semiconductor CL_{mn} and the source-side selection gate line SGS surrounding the insulation layer.”
- [0095]: “**The source-side selection transistor layer 20 includes a first source-side insulation layer 21 formed on the source line layer (acting as the source line SL) of the semiconductor substrate Ba,** a source-side conductive layer 22 formed on the first source-side insulation layer 21 and a second source-side insulation layer 23 formed on the source-side conductive layer 22.”
- [0096]: “Further, **the source-side selection transistor layer 20 includes** a source-side hole 24 passing through the first source-side insulation layer 21, the source-side conductive layer 22, the second source-side insulation layer 23 and **a source-side columnar semiconductor layer 25.**”
- [0116]: “...the source-side transistor layer 20 is formed on the semiconductor substrate Ba.”

238. See my discussion of element [1.a] above in Section IX.C.2.b.

239. Fukuzumi further discloses columnar semiconductors CL_{mn}, where “m equals from 1 to 3 and n equals from 1 to 4” such that they are “displaced like a matrix” on semiconductor substrate Ba in row- and column-directions—CL11

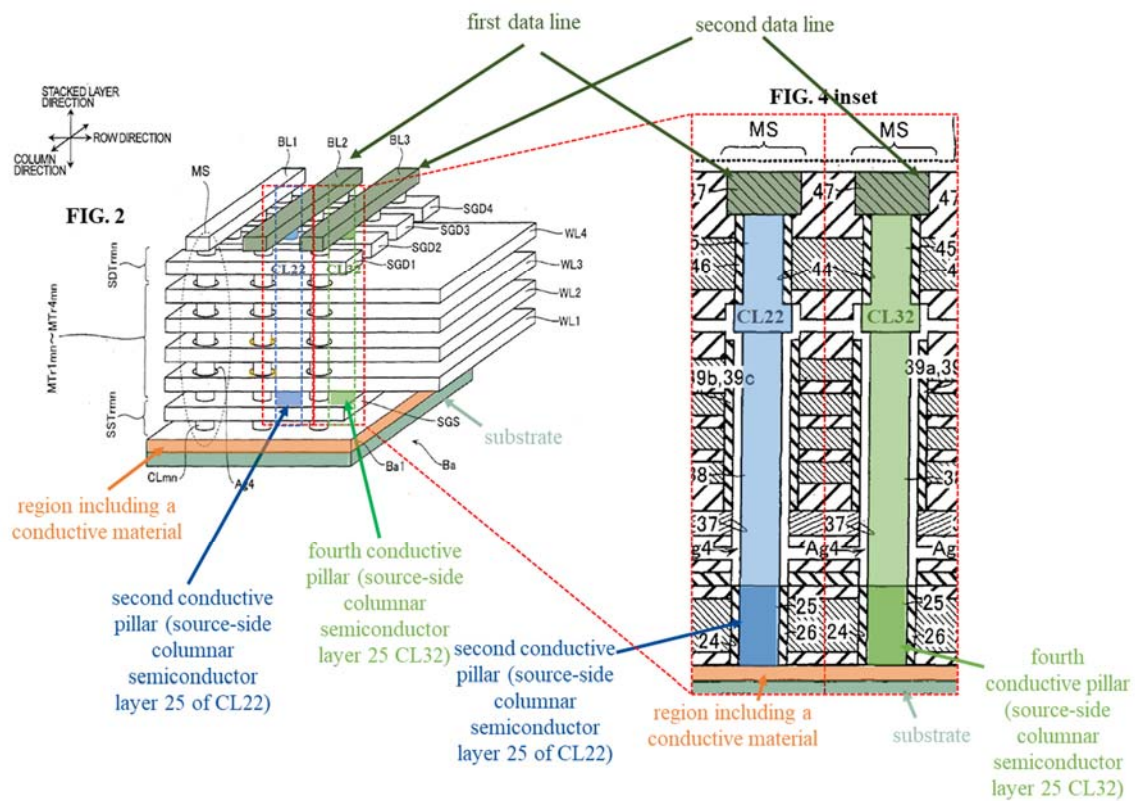
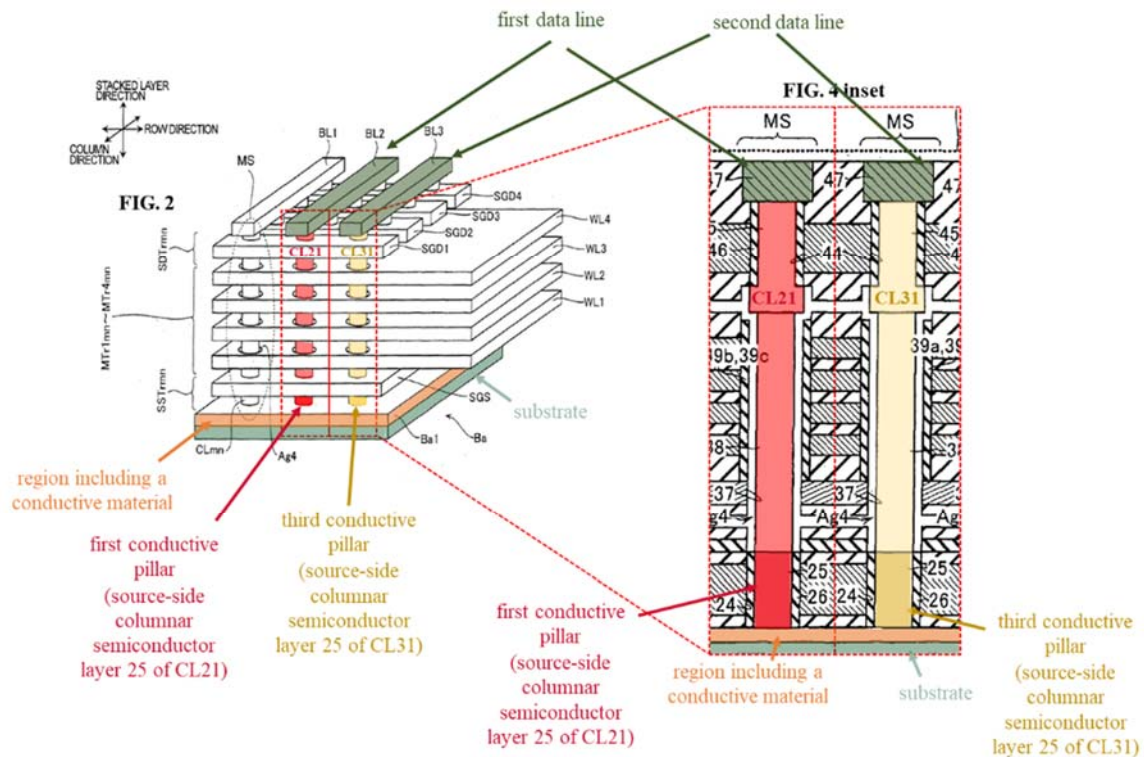
refers to the columnar semiconductor in the first column and first row, CL12 refers to the first column and second row, CL21 refers to the second column and first row, etc. Fukuzumi, [0081], [0088], [0096], [0103], Fig. 2; *see* [7]. Each such columnar semiconductor CL_{mn} includes source-side columnar semiconductor layers 25 at their lower ends, such that first and second source-side columnar semiconductor layers 25 at the lower ends of CL21 and CL22 are arranged in the column-direction, as are third and fourth source-side columnar semiconductor layers 25 at the lower ends of CL31 and CL32. Fukuzumi, [0081]. [0088], [0096], Fig. 2.

m. Element [17.c]

240. **Element [17.c] recites “a region including a conductive material, the region coupled to the first, second, third, and fourth conductive pillars, the region located between substrate and the first, second, third, and fourth conductive pillars.”** This element is met by Fukuzumi.

241. Fukuzumi discloses a region including a conductive material (*e.g.*, “p-well region Ba1”), the region coupled to the first, second, third, and fourth conductive pillars (*e.g.*, “source-side columnar semiconductor layer 25” of columnar semiconductors CL21, CL22, CL31, and CL32 formed on “region Ba1”), the region located between substrate (*e.g.*, “substrate Ba”) and the first, second, third, and fourth conductive pillars. *See, e.g.*, Fukuzumi:

- Figures 2 and 4 (annotated)



- Abstract: “a **columnar semiconductor layer perpendicularly extending toward a substrate;**”
- [0081]: “**Each of the memory strings MS includes columnar semiconductors CL_{mn} on a p-well region Ba1 formed in an n+region of a semiconductor substrate Ba.** In FIG. 2, for example, m equals from 1 to 3 and n equals from 1 to 4. **Each of the columnar semiconductors CL_{mn} are formed to perpendicular the semiconductor substrate Ba, and the columnar semiconductors CL_{mn} are displaced like a matrix above the semiconductor substrate Ba** and the word lines WL1-WL4. Thus, the memory strings MS are also displaced like a matrix in a plane perpendicular to the columnar semiconductors CL_{mn}.”
- [0088]: “**The source-side selection transistors SST_{rmn} includes the columnar semiconductor CL_{mn},** the insulation layer surrounding the columnar semiconductor CL_{mn} and the source-side selection gate line SGS surrounding the insulation layer.”
- [0095]: “**The source-side selection transistor layer 20 includes a first source-side insulation layer 21 formed on the source line layer (acting as the source line SL) of the semiconductor substrate Ba,** a source-side conductive layer 22 formed on the first source-side insulation layer 21 and a second source-side insulation layer 23 formed on the source-side conductive layer 22.”
- [0096]: “Further, **the source-side selection transistor layer 20 includes** a source-side hole 24 passing through the first source-side insulation layer 21, the source-side conductive layer 22, the second source-side insulation layer 23 and **a source-side columnar semiconductor layer 25.**”
- [0116]: “...the source-side transistor layer 20 is formed on the semiconductor substrate Ba.”

242. See my discussion of element [1.a] above in Section IX.C.2.b.

243. Fukuzumi further discloses a “p-well region Ba1” formed on semiconductor substrate Ba in an n+ region, where source-side columnar semiconductor layers 25, such as the lower ends of CL21, CL22, CL31, CL32, are

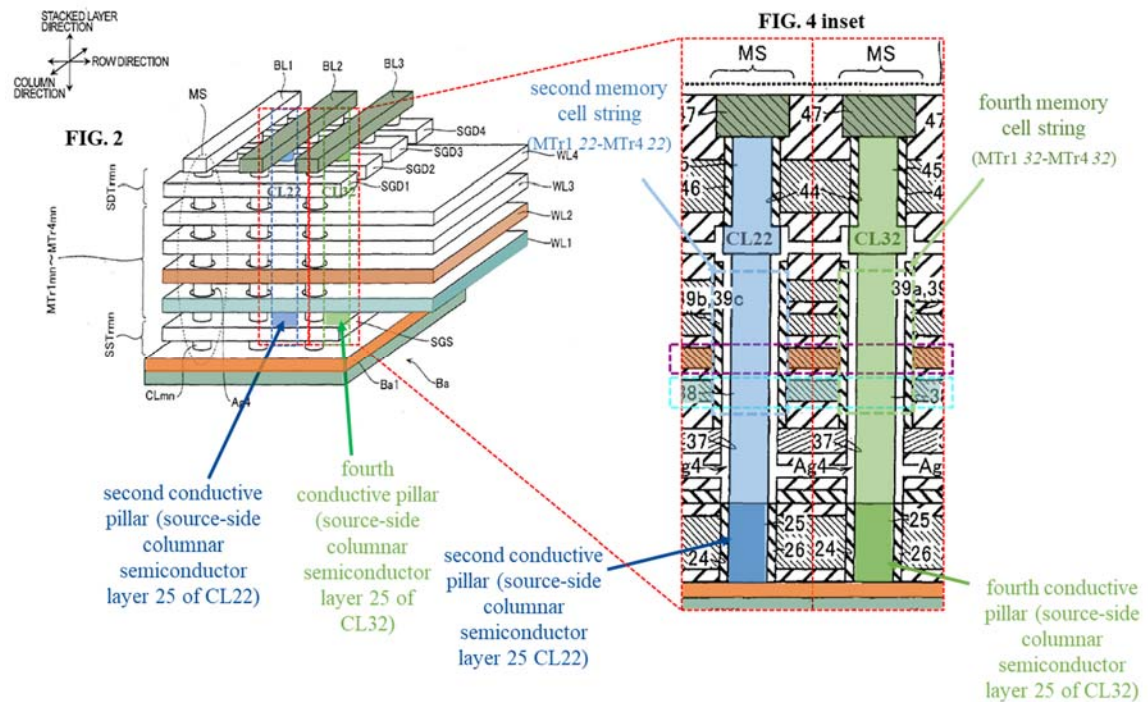
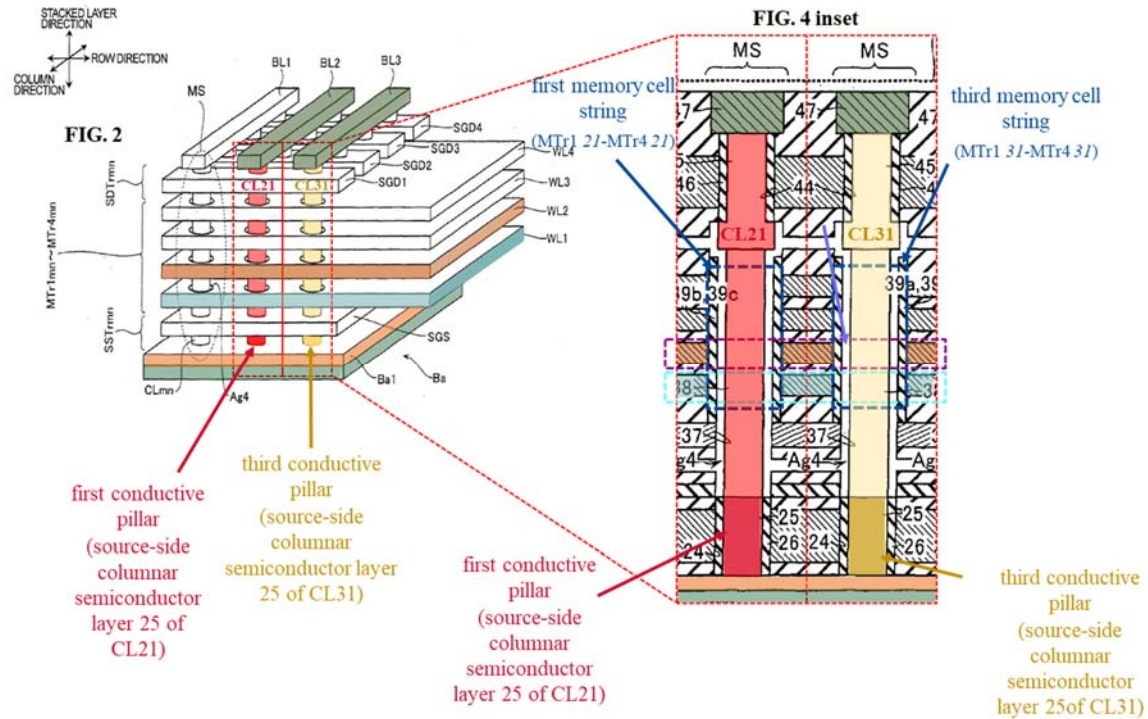
formed on Ba1. Fukuzumi, [0081], [0088], [0116].

n. Elements [17.d]-[17.g]

244. **Elements [17.d]-[17.g] recites “a [first/second/third/fourth] memory cell string formed over the first conductive pillar.”** These elements are met by Fukuzumi.

245. Fukuzumi discloses a first memory cell string formed over the first conductive pillar, a second memory cell string formed over the second conductive pillar, a third memory cell string formed over the third conductive pillar, a fourth memory cell string formed over the fourth conductive pillar (*e.g.*, “memory cells” MTr1*mn*-MTr4*mn* over “source-side columnar semiconductor layer 25” of columnar semiconductors CL21, CL22, CL31, and CL32—see [17.a]-[17.b]). *See, e.g.*, Fukuzumi:

- Figures 2 and 4 (annotated)



- [0076]: "...The memory cell region 12 *includes memory cells memorizing data*...."
- [0077]: "...the memory cells constituting the memory cell region 12 are formed by stacking a plurality of semiconductor layers in order.

Further, each layer of the word lines WL is two-dimensionally extended in a prescribed area as shown in FIG. 1. Each layer of the word lines WL has a plane structure of a single layer.”

- [0079]: “***...the memory cell region 12 includes $m \times n$ numbers (m and n being counting numbers) of memory strings MS being constituted with memory cells $MTr1mn$ - $MTr4mn$, source-side selection transistors $SSTrmn$ and drain-side selection transistor $SDTrmn$. In Fig. 2, m and n equals to three and four, respectively, as an example.***”
- [0080]: “***Each of the word lines WL1-WL4 is connected to each gate of the memory cells $MTr1mn$ - $MTr4mn$ in each of the memory strings MS and each of the word lines WL1-WL4 are formed of the same conductive layer and are common in plane each other. ... Further, each of the word line WL1-WL4 is configured nearly perpendicular to the memory strings MS.***”
- [0081]: “***Each of the memory strings MS includes columnar semiconductors $CLmn$ on a p-well region $Ba1$ formed in an n+region of a semiconductor substrate Ba . In FIG. 2, for example, m equals from 1 to 3 and n equals from 1 to 4. Each of the columnar semiconductors $CLmn$ are formed to perpendicular the semiconductor substrate Ba , and the columnar semiconductors $CLmn$ are displaced like a matrix above the semiconductor substrate Ba and the word lines WL1-WL4.***”
- [0085]: “In the first embodiment as shown in FIG. 2 and FIG. 3, ***the memory string MS includes four memory cells $MTr1mn$ - $MTr4mn$, the source-side selection transistors $SSTrm$ and the drain-side selection transistor $SDTrmn$.***”
- [0088]: “***The source-side selection transistors $SSTrmn$ includes the columnar semiconductor $CLmn$, the insulation layer surrounding the columnar semiconductor $CLmn$ and the source-side selection gate line SGS surrounding the insulation layer.***”
- [0103]: “Further, ***a memory hole 37 is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth word line conduction layers 36a-36d, the third frame bottom layer 33b, the third protective layer 33c, the first protective layer 31a and the isolation insulator 34. A memory 38***

is formed at a portion as aligning the source-side columnar semiconductor 25 in the memory hole 37.”

- [0104]: “...a block insulation layer 39a, **a charge storage layer 39b** and a tunnel insulation layer 39c are **formed on sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37** in order.”

246. See my discussion of elements [1.a]-[1.b], [17.a]-[17.c] above in Section IX.C.2.b-c, IX.C.2.1-m.

247. Fukuzumi further discloses each of memory cells MTr1 mn -MTr4 mn in “memory hole 37” are “formed at a portion as aligning” and above “the source-side columnar semiconductor 25.” Fukuzumi, [0087], [0093], [0103]. Specifically, each of memory cells MTr1 mn -MTr4 mn includes memory 38 of columnar semiconductor CL mn formed above and “aligning the source-side columnar semiconductor 25 in the memory hole.” Fukuzumi, [0087], [0103]-[0104], Fig. 2. For example, first memory string (MTr121-MTr421) is formed over first source-side columnar semiconductor layer 25 of columnar semiconductor CL21. Similarly, second (MTr122-MTr422), third (MTr131-MTr431), and fourth (MTr132-MTr432) memory strings are formed over source-side columnar semiconductor layers 25 of columnar semiconductors CL22, CL31, and CL32, respectively.

o. Elements [17.h] and [17.i]

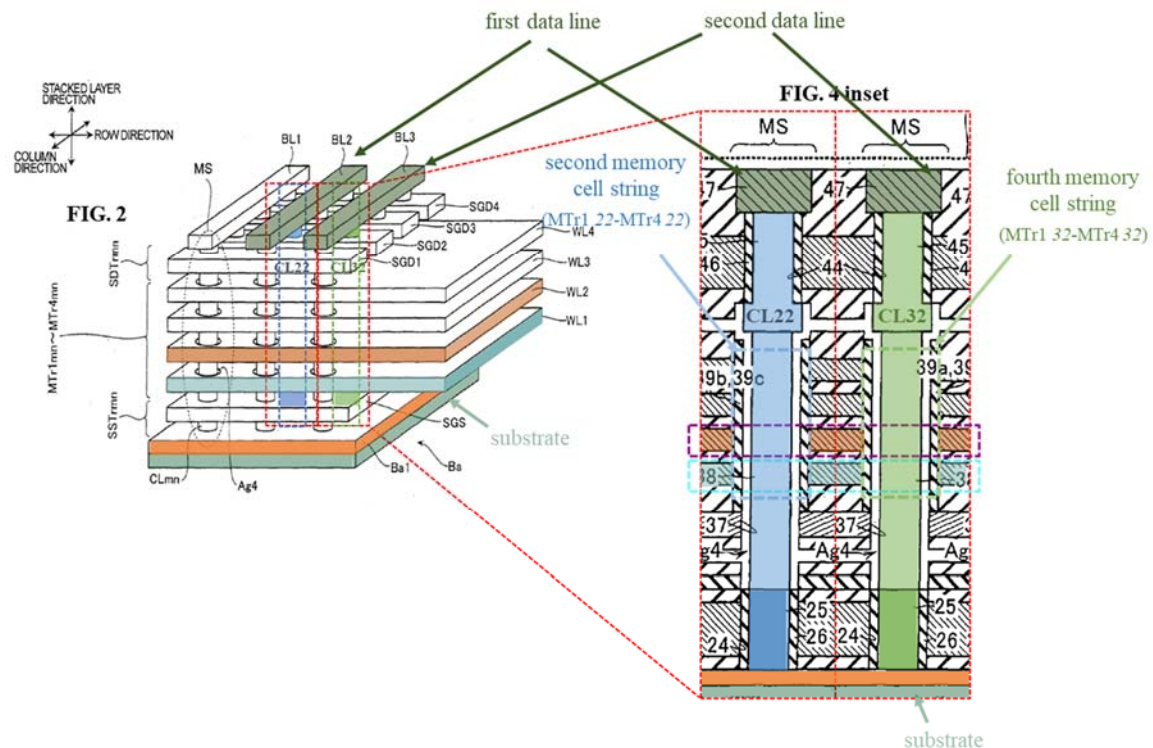
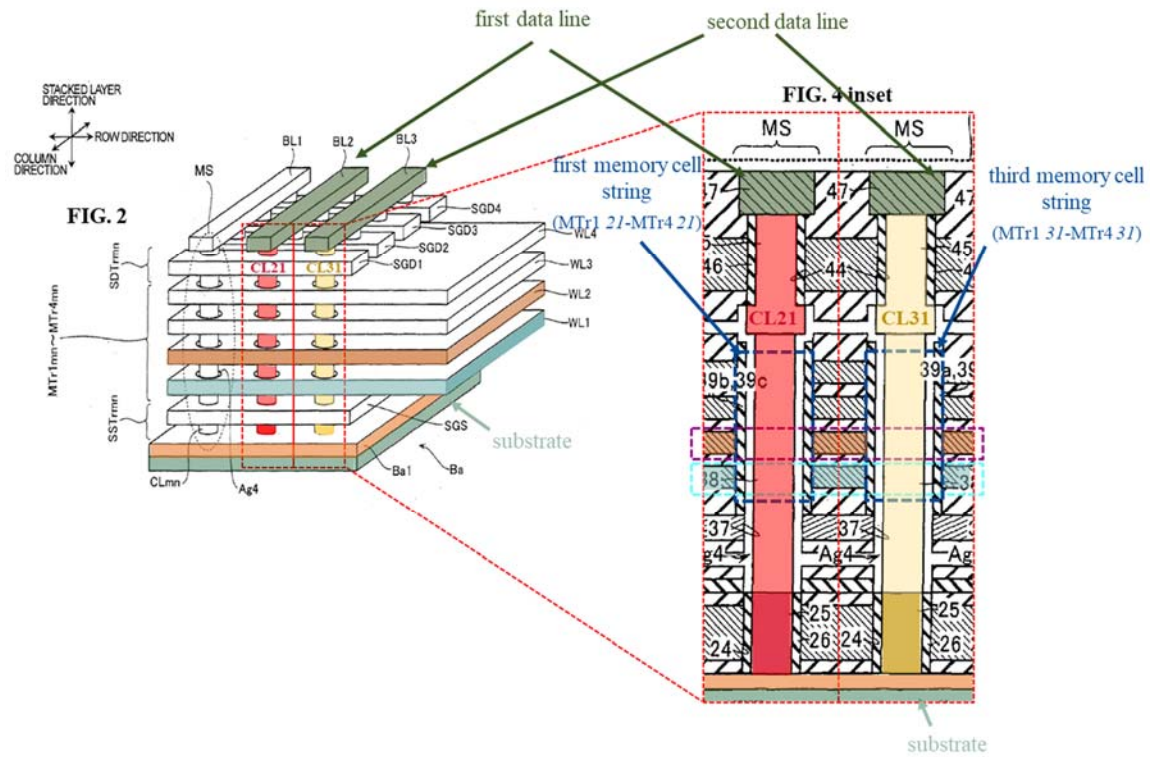
248. **Elements [17.h] and [17.i] recite “a first data line coupled to the first and second memory cell strings, the first and second memory cell strings**

located between the first data line and the substrate” and “a second data line coupled to the third and fourth memory cell strings, the third and fourth memory cell strings located between the second data line and the substrate.”

These elements are met by Fukuzumi.

249. Fukuzumi discloses a first data line (*e.g.*, “bit line BL”) coupled to the first and second memory cell strings (*e.g.*, “memory cells” MTr121-MTr421 and MTr122-MTr422), the first and second memory cell strings located between the first data line and the substrate (*e.g.*, “substrate Ba”). Fukuzumi also discloses a second data line (*e.g.*, “bit line BL”) coupled to the third and fourth memory cell strings (*e.g.*, “memory cells” MTr131-MTr431 and MTr132-MTr432), the third and fourth memory cell strings located between the second data line and the substrate (*e.g.*, “substrate Ba”). *See, e.g.*, Fukuzumi:

- Figures 2 and 4 (annotated)



- [0081]: “Each of the memory strings MS includes columnar semiconductors CLmn on a p-well region Ba1 formed in an n+region of

a semiconductor substrate Ba. In FIG. 2, for example, m equals from 1 to 3 and n equals from 1 to 4. ***Each of the columnar semiconductors CLmn are formed to perpendicular the semiconductor substrate Ba***, and the columnar semiconductors CLmn are displaced like a matrix above the semiconductor substrate Ba and the word lines WL1-WL4. ***Thus, the memory strings MS are also displaced like a matrix in a plane perpendicular to the columnar semiconductors CLmn....***”

- [0083]: “...as shown in FIG. 2, ***the drain-side selection gate lines SGD constituting the drain-side selection transistor SDTrmn is configured upper the memory strings MS and contacting the columnar semiconductors CLmn*** and the insulation layer (not illustrated) via the columnar semiconductor CLmn and the insulation layer.”
- [0085]: “...***These four memory cells MTr1mn-MTr4mn, the source-side selection transistors SStrmn and the drain side selection transistor SDTrmn are serially connected each other....***”
- [0086]: “...As shown in FIG. 4, ***in the first embodiment of the memory strings MS, the columnar semiconductor CLmn is formed on an n+-region formed in a p-type region (p-Well region) Ba1 of a semiconductor substrate Ba***. Thus, source line SL is connected to a source of the source-side selection transistors SStrmn. The source means the n+-region formed in the p-well region Ba1 of the semiconductor substrate Ba.... Further, ***the bit line BL is connected to a drain of each of the drain-side selection transistor SDTrmn***”)
- [0087]: “***Each of the memory cells Mtrmm includes the columnar semiconductor CLmn***, the insulation layer surrounding the columnar semiconductor CLmn via the space Ag4 as shown in Fig. 2, a charge storage layer (not illustrated in FIG. 2 and FIG. 3) ***and the word line WL surrounding the insulation layer and the charge storage layer. A source and a drain of each of the memory cells MTrmn are formed in each of the columnar semiconductors CLmn.***”
- [0088]: “***The source-side selection transistors SStrmn includes the columnar semiconductor CLmn***, the insulation layers surrounding the columnar semiconductor CLmn and the source-side selection gate line SGS surrounding the insulation layer.”

- [0089]: “**The drain-side selection transistors SDTrmn include the columnar semiconductors CLmn**, the insulation layer surrounding the columnar semiconductor CLmn and the drain-side selection gate line SGD surrounding the insulation layer.”
- [0103]: “Further, a **memory hole 37 is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth word line conduction layers 36a-36d**, the third frame bottom layer 33b, the third protective layer 33c, the first protective layer 31a and the isolation insulator 34. **A memory 38 is formed at a portion as aligning the source-side columnar semiconductor 25 in the memory hole 37....**”
- [0104]: “...a block insulation layer 39a, **a charge storage layer 39b** and a tunnel insulation layer 39c are **formed on sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37** in order....”
- [0108]: “Further, **the drain-side selection transistor layer 40** passes through the first drain-side insulation layer 41, the drain-side conductive layer 42 and the second drain-side insulation layer 43, to **include a drain-side hole 44 and a drain-side columnar semiconductor layer 45 formed in the drain-side hole 44.**”
- [0109]: “**A bit line layer 47 is formed at a portion being aligned with the drain-side columnar semiconductor layer 45 and an upper portion of the drain-side columnar semiconductor layer 45.** The bit line layer 47 acts as the bit line BL as shown in FIG. 2.”

250. See my discussion of elements [7] and [17.a]-[17.g] above in Section IX.C.2.i & IX.C.2.l-n.

251. As discussed in [7], Fukuzumi discloses bit line layers 47 coupled to memory 38 of memory cells such that the memory cells are located between bit line layers 47 and substrate Ba. Fukuzumi, [0085], [0109], Fig. 2; Moreover, as shown in Fig. 2, bit lines BL (i.e., bit line layers 47) extend in the column direction such that one bit line BL is coupled to first (MTr121-MTr421) and second

(MTr122-MTr422) memory strings, and a second bit line BL is coupled to third (MTr131-MTr431) and fourth (MTr132-MTr432) memory strings. Fukuzumi, Fig. 2.

p. Elements [17.j] and [17.k]

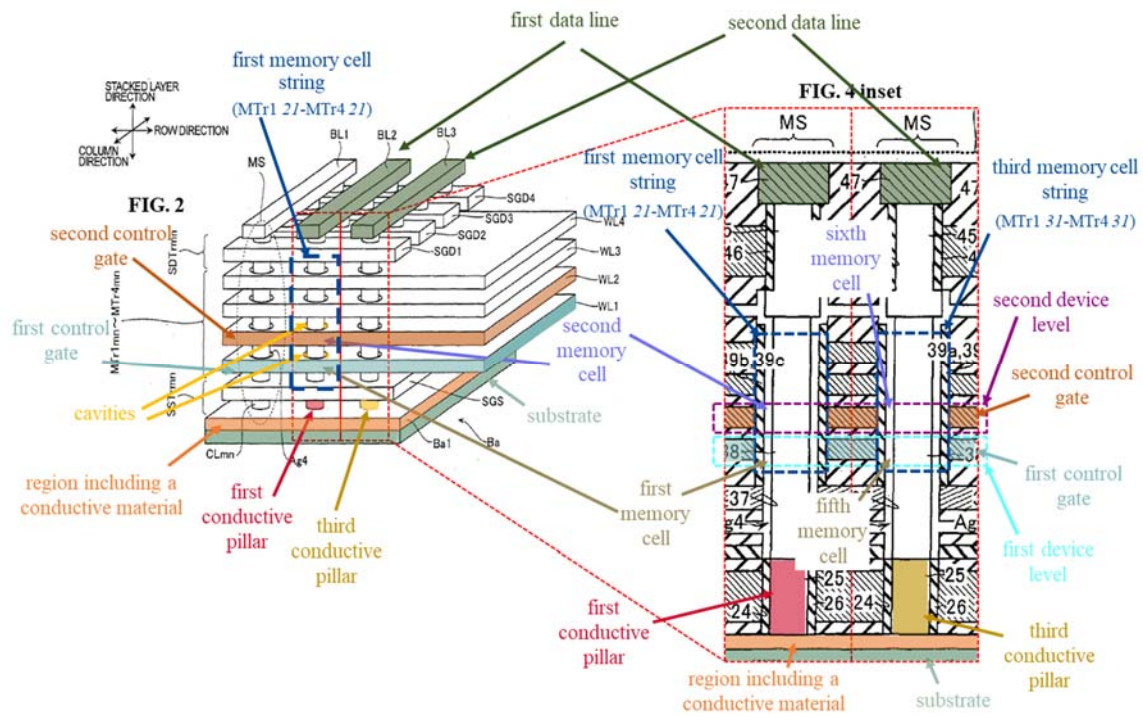
252. **Elements [17.j] and [17.k] recite “a first control gate formed in a first device level” and “a second control gate formed in a second device level.”**

These elements are met by Fukuzumi. See my discussion of elements [1.c] and [1.d] above in Section IX.C.2.d-e.

q. Element [17.l]

253. **Element [17.l] recites “the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate.”** This element is met by Fukuzumi.

254. Fukuzumi discloses that the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate (*e.g.*, “memory cells” MTr121-MTr421 including “memory cells” MTr121 and MTr221 having “charge storage layer 391 b” formed in “memory hole 37” of “end portion” of “word line” WL1 and WL2, or “word line conduction layer” 36a and 36b, respectively). *See, e.g.*, Fukuzumi:



- Figure 6 (annotated)

- [0087]: “**Each of the memory cells Mtrmm includes the columnar semiconductor CLmn**, the insulation layer surrounding the columnar semiconductor CLmn via the space Ag4 as shown in Fig. 2, a charge storage layer (not illustrated in FIG. 2 and FIG. 3) **and the word line WL surrounding the insulation layer and the charge storage layer. And end portion of the word line WL contacting with the charge storage layer surrounded by the insulator act as a control gate of the memory cell Mtrmn.** A source and a drain of each of the memory cells MTrmn are formed in each of the columnar semiconductors CLmn.”
- [0090] “...**reading out data, writing in data and erasing data are performed by controlling electrical charges of the charge storage layer** in the prescribed memory cell.”
- [0101]: “An interlayer insulator 35 is formed on a top surface of the third frame bottom layer 33. Further, first-fourth word line conduction layers 36 a-36 d between the interlayer insulators 35 are formed. **The first-fourth word line conduction layer layers 36 a-36 d act as the word lines WL1-WL4.**”
- [0103]: “Further, a memory hole is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth word line conduction layers 36a-36d, the third frame bottom layer 33b, the third protective layer 33c, the first protective layer 31a and the isolation insulator 34. **A memory 38 is formed at a portion as aligning the source-side columnar semiconductor in the memory hole 37.** The memory 38 is formed of silicon....”
- [0104]: “...a block insulation layer 39a, **a charge storage layer 39b** and a tunnel insulation layer 39c are **formed on sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37 in order.**”
- [0114]: “...when the fourth word line conduction layer 36d is applied to voltage, the memory 38 is performed to **write in data into the approached portion of the charge storage layer 39b and read out data from the approached portion of the charge storage layer 39b.**”

255. See my discussion of elements [1.b]-[1.d], [17.d]-[17.g], and [17.j]-

[17.k] above in Section IX.C.2.c-e, IX.C.2., IX.C.2.p.

256. Further, as I explain in connection with element [1.c]-[1.d], Fukuzumi discloses that each string of memory cells MTr1*mn* to MTr4*mn* includes memory cells with “charge storage layer 391b” in respective memory holes 37 and on the “end portion of the word line[s]” WL1-WL4. Fukuzumi, [0080], [0087], [0101]. For example, first memory string (MTr121-MTr421) includes first memory cell MTr121 at WL1 and second memory cell MTr221 at WL2 with “charge storage layer 391b” in respective memory holes 37 of “end portion of the word line[s]” WL1-WL2, respectively.

257. Moreover, as I explain in connection with elements [1.c]-[1.d], the limitation is disclosed in Fukuzumi even to the extent “cavity of the first control gate” requires the memory hole in the control gate to have a larger diameter than the layers above and below the control gate.

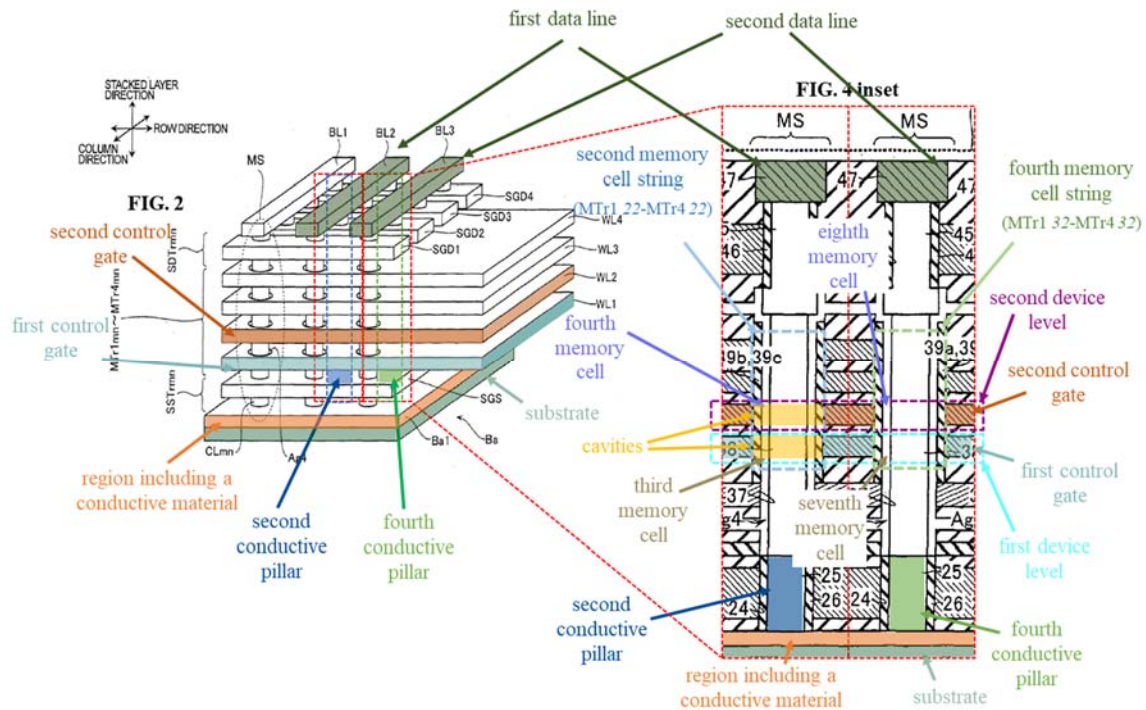
r. Element [17.m]

258. **Element [17.m] recites “the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate.”** This element is met by Fukuzumi.

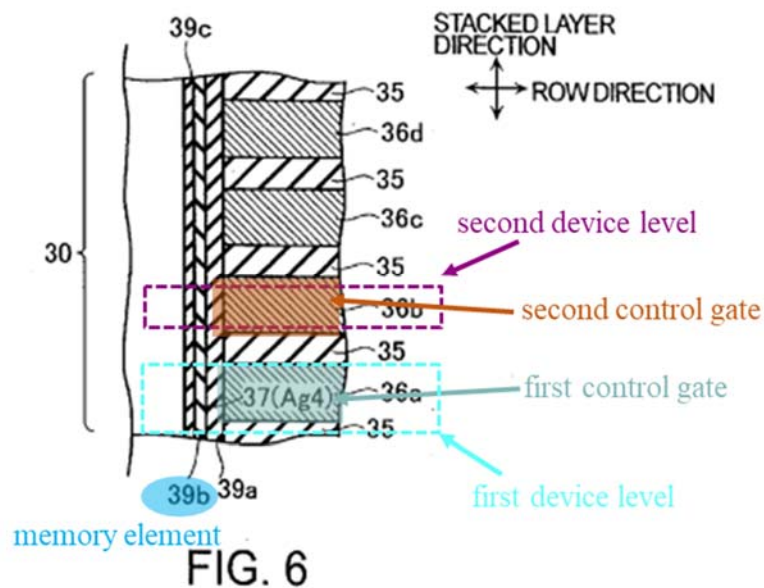
259. A Fukuzumi discloses that the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a

second cavity of the second control gate (e.g., “memory cells” MTr122-MTr422 including “memory cells” MTr122 and MTr222 having “charge storage layer 391 b” formed in “memory hole 37” of “end portion” of “word line” WL1 and WL2, or “word line conduction layer” 36a and 36b, respectively). See, e.g., Fukuzumi:

- Figure 2 and 4 (annotated)



- Figure 6 (annotated)



260. See my discussion of elements [1.b]-[1.d], [17.d]-[17.g], and [17.j]-[17.l] above in Section IX.C.2.c-e, IX.C.2.n, IX.C.2.p-q.

261. Further, the same analysis provided for [17.l] applies for this limitation. For example, for this limitation, the third and fourth memory cells are MTr122 and MTr222.

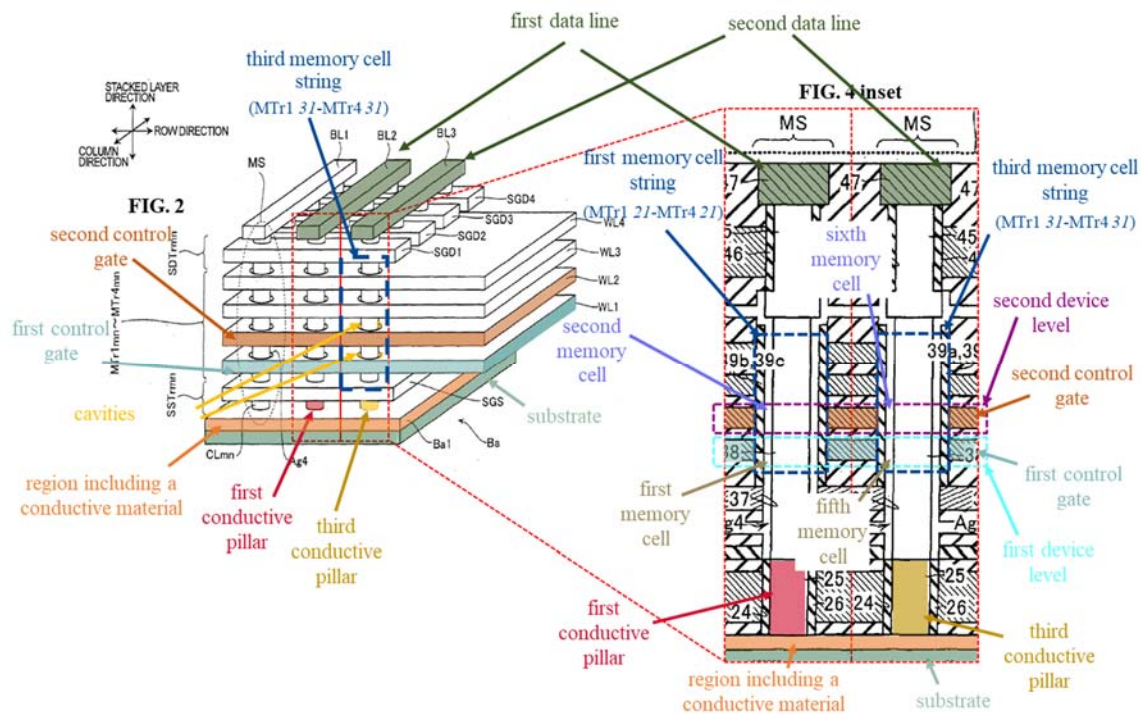
s. **Element [17.n]**

262. **Element [17.n] recites “the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate.”** This element is met by Fukuzumi.

263. Fukuzumi discloses that the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control

gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate (e.g., “memory cells” MTr131-MTr431 including “memory cells” MTr131 and MTr231 having “charge storage layer 391 b” formed in “memory hole 37” of “end portion” of “word line” WL1 and WL2, or “word line conduction layer” 36a and 36b, respectively). See, e.g., Fukuzumi:

- Figures 2 and 4 (annotated)



- Figure 6 (annotated)

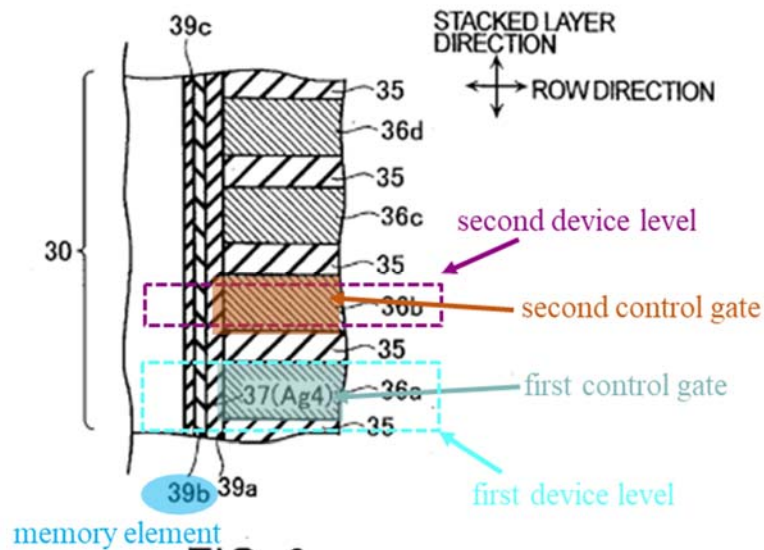


FIG. 6

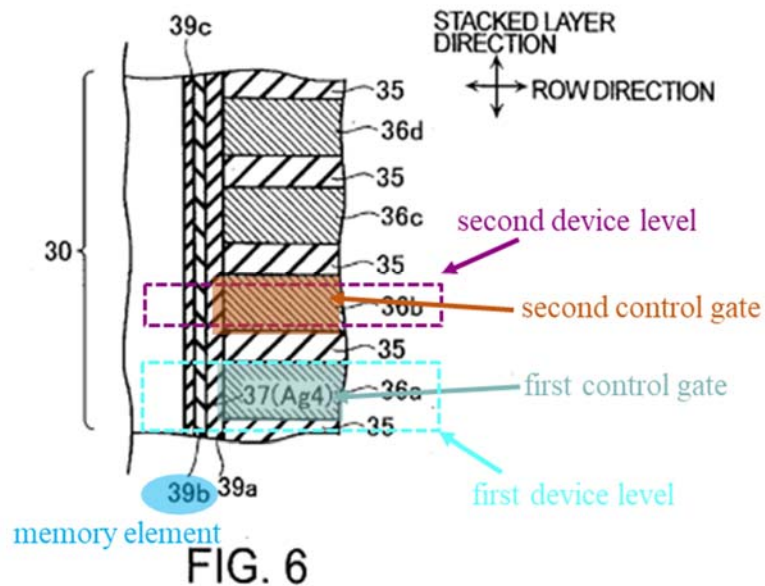
264. See my discussion of elements [1.b]-[1.d], [17.d]-[17.g], and [17.j]-[17.l] above in Section IX.C.2.c-e, IX.C.2.n, IX.C.2.p-q.

265. Further, the same analysis provided for [17.l] applies for this limitation. For example, for this limitation, the fifth and sixth memory cells are MTr131 and MTr232.

t. Element [17.o]

266. **Element [17.o] recites “the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.”** This element is met by Fukuzumi.

267. Fukuzumi discloses that the fourth memory cell string includes a



268. See my discussion of elements [1.b]-[1.d], [17.d]-[17.g], and [17.j]-[17.l]. above in Section IX.C.2.c-e, IX.C.2.n, IX.C.2.p-q.

269. Further, the same analysis provided for [17.l] applies for this limitation. For example, for this limitation, the seventh and eighth memory cells are MTr132 and MTr232.

u. Claim [19]

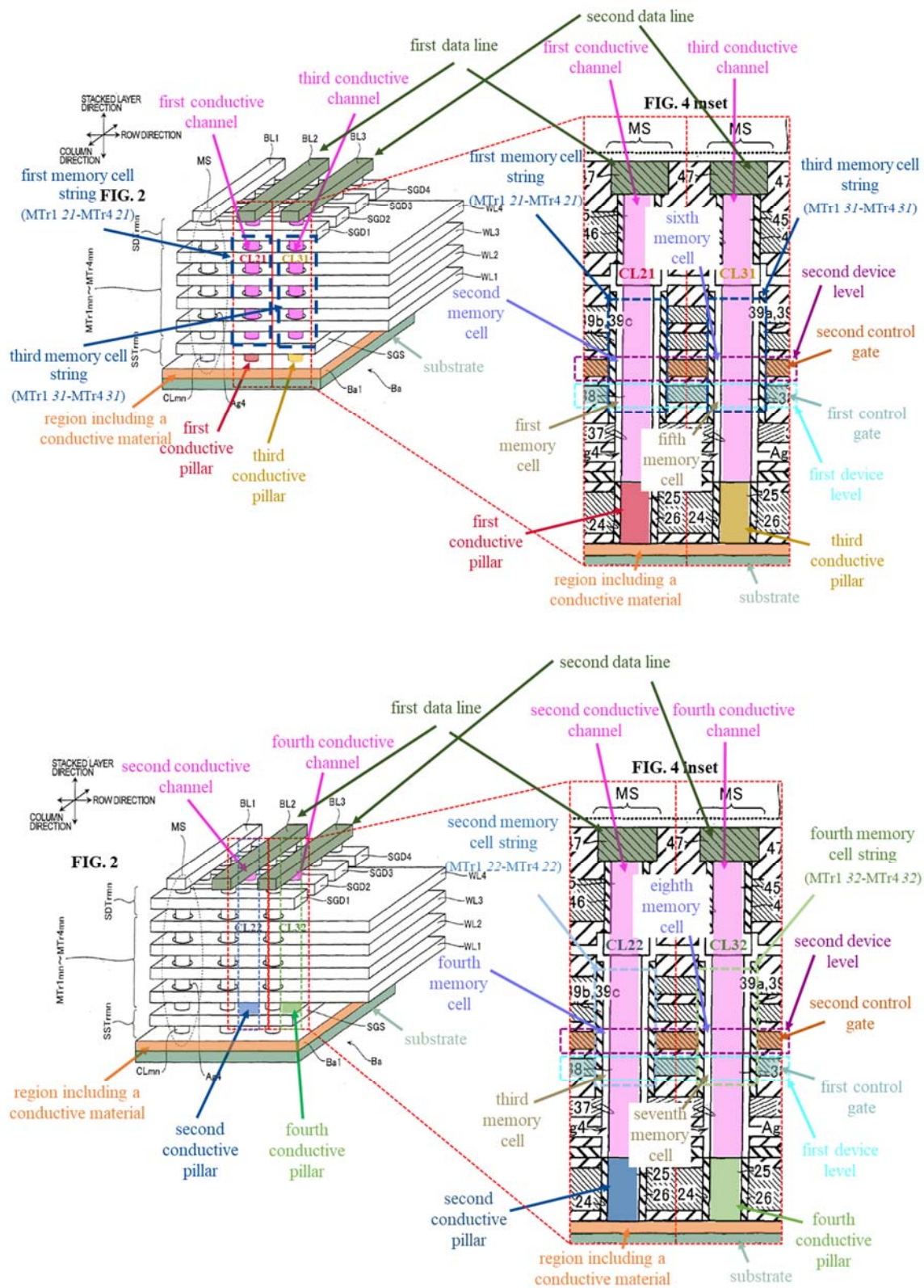
270. **Claim [19] recites “The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises a silicon nitride.”** This claim is met by Fukuzumi. See my discussion of claims [9] and [17] above in Section IX.C.2.j & IX.C.2.k-t. As I note above in connection with claim [9], each memory cell comprises silicon nitride.

v. Claim [20]

271. Claim [20] recites **“The apparatus of claim 17, further comprising: a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells; a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells; a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells; and a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells.”** See my discussion of claim [17] above in Section IX.C.2.k-t. The added limitation of claim [20] is met by Fukuzumi.

272. Fukuzumi discloses a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells, a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells, a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells, and a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells (*e.g.*, “memory 38” extending between “memory cells” MTr1*mn* and MTr2*mn*, and coupled to “source-side columnar semiconductor layer 25” of columnar semiconductor CL21, CL22, CL31, and CL32—*see* [17.a]-[17.b], [17.l]-[17.o]). *See, e.g.*, Fukuzumi:

- Figures 2 and 4 (annotated)



- [0081]: “**Each of the memory strings MS includes columnar semiconductors CLmn on a p-well region Ba1 formed in an n+region of a semiconductor substrate Ba.** In FIG. 2, for example, m equals from 1 to 3 and n equals from 1 to 4. Each of the columnar semiconductors CLmn are formed to perpendicular the semiconductor substrate Ba, and the **columnar semiconductors CLmn are displaced like a matrix above the semiconductor substrate Ba** and the word lines WL1-WL4. Thus, the memory strings MS are also displaced like a matrix in a plane perpendicular to the columnar semiconductors CLmn....”
- [0085]: “...the memory string MS includes four memory cells MTr1 mn-Mtr4 mn, the source-side selection transistors SStrm and the drain-side selection transistor SDTrmn. **These four memory cells MTr1 mn-MTr4 mn, the source-side selection transistors SStrm and the drain side selection transistor SDTrmn are serially connected each other....**”
- [0086]: “As shown in FIG. 4, in the first embodiment of the memory strings MS, **the columnar semiconductor CLmn is formed on an n+-region formed in a p-type region (p-Well region) Ba1 of a semiconductor substrate Ba.** Thus, source line SL is connected to a source of the source-side selection transistors SStrmn. The source means the n+-region formed in the p-well region Ba1 of the semiconductor substrate Ba.”
- [0087]: “**Each of the memory cells Mtrmm includes the columnar semiconductor CLmn,** the insulation layer surrounding the columnar semiconductor CLmn via the space Ag4 as shown in Fig. 2, **a charge storage layer (not illustrated in FIG. 2 and FIG. 3) and the word line WL surrounding the insulation layer and the charge storage layer.** A source and a drain of each of the memory cells MTrmn are formed in each of the columnar semiconductors CLmn”
- [0088]: “The source-side selection transistors SStrmn **includes the columnar semiconductor CLmn....**”
- [0089]: “The drain-side selection transistors SDTrmn **include the columnar semiconductors CLmn....**”
- [0103]: “...**a memory hole 37 is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth wordline conduction layers 36a-36d.... A**

memory 38 is formed at a portion as aligning the source-side columnar semiconductor 25 in the memory hole 37.”

- [0104]: “...a block insulation layer 39a, **a charge storage layer 39b** and a tunnel insulation layer 39c are **formed on sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37 in order....**”

273. See my discussion of elements [1.e], [17.a]-[17.b], [17.d]-[17.g], and [17.l]-[17.o] above in Section IX.C.2.f, IX.C.2.l, IX.C.2.n, IX.C.2.q-t.

274. Further, as I discuss in connection with elements [1.e] and [17.d]-[17.g], first, second, third, and fourth memory strings (MTr1mn-MTr4mn) are formed over and coupled to first, second, third, and fourth source-side columnar semiconductor 25 of columnar semiconductors CL21, CL22, CL31, and CL32, respectively, and as a result, memory 38 (the conductive channels) of the memory strings extend between memory cells of the memory strings and are coupled to the respective source-side columnar semiconductors 25. Fukuzumi, [0085], [0103].

D. GROUND 4: Fukuzumi in view of Ahn (Claims 5, 8, 18)

275. As I explain above, Ahn discloses the limitations of claim 5, 8 and 18 (Sections IX.A.2.j, IX.A.2.l, IX.A.2.x).

276. Fukuzumi and Ahn are in the same field as the '903 patent, which includes three-dimensional memory devices with the same configuration of memory cells arranged above the lower select gates or source-side selection transistors. '903 patent, Abstract, 1:65-2:9 (“Fig. 1 shows a block diagram of a

memory device 100 having a memory array 102 with memory cells 110 according to an embodiment of the invention.... Memory cells 110 can be physically located in multiple device levels such that one group of memory cells 110 can be stacked on one or more groups of other memory cells 110.”); Ahn, [0001] (“The present invention relates to a method for manufacturing a flash memory device, and more particularly, to a method for manufacturing a flash memory device having a three-dimensional structure.”); Fukuzumi, [0010]-[0011] (“According to an aspect of the present invention, there is provided a nonvolatile semiconductor memory device, comprising a plurality of memory strings, each of the memory strings being constituted with a plurality of electrically erasable memory cells being serially connected each other, comprising: forming a source-side transistor layer on a semiconductor substrate”).

277. Fukuzumi and Ahn are reasonably pertinent to the problems addressed by the '903 patent, e.g., increasing integration or density of memory devices. '903 patent, 1:26-28 (“As demand for higher density memory device increases, three-dimensional (3D) memory devices have been proposed.”); Ahn, [0005] (“A technical task to be achieved by the present invention is to provide a method for manufacturing a flash memory device having a structure capable of increasing the integration density of memory cells without being limited by the substrate area by implementing memory cells in a vertical direction with respect to a semiconductor

substrate.”); Fukuzumi, [0004] (“[I]n the case of three-dimensionally stacking memory cells, processing steps in a conventional method are largely increased layer by layer to increase the cost. Further, in a seek-scan type memory device using MEMS, an area of memory storage for retaining data on one bit is fixed by thermal stability or the like so as to limit the memory density.”).

1. Invalidity of Claim [5] Over Fukuzumi in view of Ahn.

278. **Claim [5] recites “The apparatus of claim 2, wherein each of the first and second conductive regions comprises metal.”** See my discussion of claim [2], above in Section IX.C.2.g. As I explain above, Ahn discloses the added limitation of claim [5], for example, because Ahn teaches using a metal such as tungsten for a source-side transistor gate. Section IX.A.2.j.

279. A person of ordinary skill in the art would have been motivated to apply Ahn’s teachings of a metal conductive layer in a lower select gate to Fukuzumi’s source-side selection transistor.

280. Fukuzumi does not teach a particular material for the source-side conductive layer 22 of the source-side selection transistor SSTrmn (*i.e.*, conductive layer on first and second sides of “source-side columnar semiconductor layer 25”), and leaves the selection of that material to a person of ordinary skill in the art. See *generally* Fukuzumi. Ahn explains that a source-side selection transistor is formed of “a conductive material,” and provides two examples of such material: doped

polysilicon and metals such as tungsten. Ahn, [0032].

281. It was well known in the art that gate materials needed to have good electrical conductivity and high temperature resistance, and that Tungsten has these properties. For example, a 1998 textbook published by Springer Science+Business Medica, LLC, which would have been accessible to a person of ordinary skill in the art, e.g., at a library, titled “Polycrystalline Silicon for Integrated Circuits and Displays” by Ted Kamins (“Kamins”), which I understand has been designated as Exhibit 1023, discloses that “[a]s feature sizes become smaller and intrinsic transistor delays decrease on chips of increasing overall dimensions, the resistance of polysilicon interconnections is becoming a more serious limitation on integrated-circuit performance,” noting the importance of electrical conductivity. Ex. 1023, 195. Kamins also discloses that “[t]he material selected for a self-aligned electrode must be compatible with the ... other high-temperature processes that follow gate-electrode formation.” Ex. 1023, 247. Moreover, a person of ordinary skill in the art would have also understood that tungsten was widely used in semiconductor processing due to their relatively higher conductivity compared to polysilicon, in addition to the ability to resist high temperatures. For example, a 1998 article, for the well-known and readily accessible Elsevier Science S.A. publication (that would have been accessible to a person of ordinary skill in the art, e.g., through a library or ScienceDirect.com), titled “Growth characteristics and

electrical resistivity of chemical vapor-deposited tungsten film” by I-Shun Chang, which I understand has been designated as Exhibit 1020, discloses wide-spread use of tungsten “due to its unique properties of low resistivity compared to polycrystalline silicon, high resistance to electromigration compared to aluminum, thermal stability, conformality of deposition and the ability of selective deposition.” Ex. 1020, 1.

282. Thus, a person of ordinary skill in the art would have been motivated to apply Ahn’s teaching of using tungsten to form a source-side transistor gate to Fukuzumi’s source-side conductive layer 22 to advantageously enhance the conductivity and heat resistance of Fukuzumi’s source-side selection transistor SSTrmn. Ex. 1020, 1; Ex. 1023, 195.

283. A person of ordinary skill in the art would have had a reasonable expectation of success in applying Ahn’s teachings of a metal conductive layer to Fukuzumi’s source-side selection transistor. Use of metals for the conductive layer of the lower select gate was well known in the art. For example, Son, which I discussed above in Section IX.A.2.k, also discloses memory devices with conductive layers, where “lower conductive layer 122, the upper conductive layer 126, and the middle conductive layer 124 may be formed of the same material. The conductive layers may contain polysilicon and/or metal material.” Ex. 1010, [0073], [0046]. Further, U.S. Patent Application Publication No. 2010/0019310

(“Sakamoto”), which I understand has been designated as Exhibit 1013, discloses a semiconductor memory device where “[t]he word lines WLL, the lower select-gate line LSL, and the cell source line CSL are formed from, for example, metal material.” Ex. 1013, [0050].

284. Indeed, other than the minimal modification of using a metal layer for Fukuzumi’s source-side selection transistor, no modifications in Fukuzumi’s manufacturing process would have been needed because none of those steps depends on the composition of source-side transistor layer 20. Moreover, Ahn teaches the interchangeability of using polysilicon and metal for a source-side selection transistor gate. Ahn, [0031].

2. Invalidity of Claims [8] and [18] Over Fukuzumi in view of Ahn.

285. **Claim [8] recites “The apparatus of claim 1, wherein the memory element comprises polysilicon.” Claim [18] recites “The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises polysilicon.”** See my discussion of claims [1] and [17], above in Section IX.C.2.a-f & IX.C.2.k-t. As I explain above, Ahn discloses the added limitations of claims [8] and [18], for example, Ahn teaches using polysilicon for charge trap layers. See Sections IX.A.2.1 & IX.A.2.x.

286. A person of ordinary skill in the art would have been motivated to apply Ahn’s teachings of a polysilicon charge trap layer to Fukuzumi’s charge

storage layer. Ahn, [0040].

287. While Fukuzumi teaches the use of silicon nitride as the charge storage layer (Fukuzumi, [0104]), at the time of the alleged invention, polysilicon was commonly used for memory elements. For example, U.S. Patent No. 7,425,742 (“Nazarian”), which I understand has been designated as Ex. 1025, teaches Flash memory as a type of non-volatile memory, and that “[a] typical Flash memory comprises memory array, which includes a large number of memory cells[, and that e]ach of the memory cells includes a floating gate embedded in a field effect transistor (FET).” Ex. 1025, 1:46-56. Nazarian further discloses “that “[a] floating gate [is] typically made of doped polysilicon.” Ex. 1025, 5:26-50. Consistent with Nazarian’s teaching, Son, discussed above in Section IX.A.2.k, also discloses the use of polysilicon floating gate. Ex. 1010, [0080]. On the other hand, there were known reliability concerns with using silicon nitride. For example, as disclosed in a 2009 article, for NASA’s well-known and readily-accessible JPL publication (that would have been accessible to a person of ordinary skill in the art, e.g., at a library or through NASA Jet Propulsion Laboratory’s website), titled “Flash Memory Reliability NEPP 2008 Task Final Report” by Yuan Chen (“Chen”), which I understand has been designated as Exhibit 1017, “[b]oth SONOS and NROM [using silicon nitride] have erase saturation (i.e., hard-to-erase and/or over-erase) and the trap-related reliability issues....” Ex. 1017, 3.

Importantly, Chen further noted that the silicon nitride charge trap technology was not fully understood at the time of the alleged invention. *Id.* (“Both SONOS and NROM ... are still not fully understood.”). Further, as reported in a 1998 article, for IEEE’s 36th Annual International Reliability Physics Symposium (that would have been accessible to a person of ordinary skill in the art, e.g., at the symposium, at a library or through IEEE’s website), titled “Extended Data Retention Process Technology for Highly Reliable Flash EEPROMs of 10^6 to 10^7 W/E Cycles” by F. Arai et al. and a 2010 article, for IEEE’s Reliability Physics Symposium (IRPS) (that would have been accessible to a person of ordinary skill in the art, e.g., at the symposium, at a library or through IEEE’s website), titled “A High-Endurance (>100K) BE-SONOS NAND Flash With a Robust Nitrided Tunnel Oxide/Si Interface” by S. Wang et al., which I understand have been designed as Exhibits 1015 and 1016, respectively, while a floating gate’s data retention was reported to be fully reliable for up to 10^6 - 10^7 write/erase (W/E) cycles, silicon nitride charge trap layers demonstrated degradation due to trap generation after 10^4 W/E cycles. Compare Ex. 1015, 378, 381, with Ex. 1016, 3-4.² Similar concerns with silicon

² As shown in Exhibit 1024, which is a screenshot of IEEE’s website, “A High-Endurance (>100K) BE-SONOS NAND Flash With a Robust Nitrided Tunnel

nitride charge traps were also raised in a 2008 article, for IEEE's 46th Annual International Reliability Physics Symposium (that would have been accessible to a person of ordinary skill in the art, e.g., at the symposium, at a library or through IEEE's website), titled "Nitride Engineering and the Effect of Interfaces on Charge Trap Flash Performance and Reliability" by Sandhya C. et al., which I understand has been designated as Exhibit 1022 , disclosing that "[w]hile the memory window is maintained after 10^4 W/E cycles, a consistent increase in the erase-state VFB is observed for all devices." Ex. 1022, 408. Thus, to avoid such potential reliability issues for the use of silicon nitride as a memory element at the time of the '903 patent's claimed priority date, a person of ordinary skill in the art would have been motivated to use polysilicon for memory elements.

288. A person of ordinary skill in the art would further have had a reasonable expectation of success in applying Ahn's teachings of using a polysilicon layer to Fukuzumi's three-dimensional memory cells. Indeed, Ahn discloses its charge trap layer inside the ONO layer is "formed by depositing, for example, a silicon nitride film or a polysilicon film," teaching the interchangeability of the two materials. Ahn, [0040].

Oxide/Si Interface" by S. Wang et al. was available to the public before the earliest priority date of the '903 patent. Ex. 1024.

289. It is therefore my opinion that a person of ordinary skill in the art would have thus found it routine, straightforward and advantageous to apply Ahn's teachings of using a polysilicon memory element and a metal source side selection transistor gate to Fukuzumi's teachings of a memory device and would have known such a combination to yield the claimed limitations and would predictably work and provide the expected functionality.

X. SECONDARY CONSIDERATIONS

290. I have seen no evidence in the '903 patent's prosecution history or elsewhere supporting any secondary considerations arguments, or evidence of nexus to any of the Challenged Claims. See generally '903 File History. Indeed, per my discussion of the prior art referenced herein, any purported solutions to problems or unexpected results in the '903 patent were already well known. To the extent Patent Owner asserts the existence of any secondary considerations in its responses, I reserve my right to address any such evidence.

XI. CONCLUSION

291. In summary, I have concluded that the Challenged Claims are anticipated and at least rendered obvious over the prior art references as discussed above. Specifically, in my opinion, for at least the reasons above, the Challenged Claims of the '903 patent are either anticipated and/or rendered obvious.

292. To the extent it is argued that any further disclosure is required for an

element in the Challenged Claims that I have identified as being disclosed, a person of ordinary skill in the art would certainly have found that element obvious to include based on the sample explicit disclosure or inherent disclosures and analysis I have identified above.

293. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner or its expert(s) may raise and to take into account new information as it becomes available to me.

294. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

295. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

APPENDIX A

CURRICULUM VITAE
Dr. Kelin J. Kuhn

CONTACT INFORMATION:

Kelin J. Kuhn
P.O. Box 609
Winthrop, WA 98862
kjkuhn@confluence-tech.com

EDUCATION:

Ph.D., Electrical Engineering, Stanford University, Stanford, CA. June 1985
M.S., Electrical Engineering, Stanford University, Stanford, CA. June 1985
B.S., Electrical Engineering, University of Washington, Seattle, WA. March 1980
(magna cum laude)

PRESENT ROLE:

**Confluence Technology Services, Winthrop, WA (kjkuhn@confluence-tech.com);
present role**

Dr. Kuhn's business (Confluence Technology Services) supports a variety of engineering services in electronics and photonics, with emphasis on CMOS and beyond-CMOS technologies.

**Cornell University, Ithaca, NY; Materials Science and Engineering (kjk236@cornell.edu)
2014 to date**

Position: Adjunct Professor
Key Collaborator: Darrell Schlom

Prof. Kuhn's role is collaborating with a diverse group of faculty (both at Cornell and elsewhere) for establishment of long-term research programs in the area of valleytronics, inverse-design, quantum materials, post-CMOS technology, and spintronics.

CLIENTS / SIGNIFICANT INTERACTIONS POST-2014:

Pillsbury Winthrop Shaw Pittman LLP: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *MicroSemi Corporation v. Commissioner of Internal Revenue*.

Ropes and Gray: Initiated 2023 and on-going. Technical evaluation and consulting on the matters related to *Yangtze Memory Technologies Company, LTD. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 5-23-cv-05792*.

Heim, Payne & Chorush: Initiated 2023 and on-going. Technical evaluation and consulting representing *Microchip Corporation* and its subsidiary *Silicon Storage Technology, Inc.* with regards to a dispute with *Taiwan Semiconductor Manufacturing Company*.

Smith Baluch LLP: Initiated 2022 and on-going. Technical evaluation and consultation to advise and assist Smith Baluch LLP matters relating to semiconductor processing.

Carter Arnett: Initiated 2022 and ongoing. Technical evaluation and consultation to advise and assist Carter Arnett PLLC in representing *Katana Silicon Technologies, LLC* in IPR2022-00763 and litigation related to Case No. 6:22-cv-00191 (W.D. Tex), adverse to *GlobalFoundries, Inc., GlobalFoundries, U.S. Inc., and GlobalFoundries U.S. 2 LLC*.

Mintz: Completed 2022-2023. Technical evaluation and consulting representing *Daedalus Prime LLC* with regards to the ITC Case: 337-TA-133, Certain Semiconductor Devices, Mobile Devices Containing Same (Taiwan Semiconductor Manufacturing Company).

Heim, Payne & Chorush: Completed 2021-2023. Technical evaluation and consulting representing *Arigna Technology Limited* with regards to IPR2021-01321 (*Volkswagen*) and IPR2021-01382 (*Infineon*).

Quinn Emanuel Urquhart & Sullivan: Believed complete 2021-2023. Technical evaluation and consulting representing *Hanwha* with regards to ITC Inv. No. 337-TA-1271.

Ropes and Gray: Completed 2021-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge I v. Micron Technology et al.*

Lawrence and Phillips: Completed 2021-2022. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.* with regards to *inter partes* reviews (IPRs) filed by Samsung.

Wolf Greenfield: Completed 2020-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge I v. Micron Technology et al.* with regards to *inter partes* reviews (IPRs) filed by Micron.

Hueston Henningan: Completed 2020-22. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.*

Skadden Arps: Initiated 2020 and on-going. Technical consulting for the *Audit Committee of the Intel Board of Directors* on matters related to Technology Development.

PARADIM: Initiated 2016 and on-going. PARADIM's mission is to create new interface materials with unprecedented properties for the next generation of electronic devices. Dr. Kuhn is a member of the External Advisory Committee. In this role, Dr. Kuhn provides technical and management support with regards to PARADIM operations.

Quinn Emanuel Urquhart & Sullivan: Completed, 2020-2021. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Susman Godfrey: Completed 202-2023. Technical evaluation and consulting with regards to *Arigna Technology Limited* on matters related to CMOS transistor design.

Womble Bond Dickinson: Completed, 2020. Technical consulting for KIPB LLC (formerly KAIST IP US LLC) on an *ex parte reexamination* (“EPR”) proceeding in the United States Patent and Trademark Office with regards to patent 6,885,055.

Womble Bond Dickinson: Completed, 2019-2020. Technical evaluation and consulting in the matter of *KIPB LLC v. Samsung Electronics et al.* Dr. Kuhn supported this litigation for the plaintiff as an expert witness, including completion of the Infringement and Rebuttal Reports, as well as completing a deposition conducted on the contents of the Infringement and Rebuttal Reports. This case was settled out of court in September 2020.

Lathrop Gage: Completed, 2018-2020. Technical evaluation and consulting for KIPB LLC (formerly KAIST IP US LLC) on Korean Patent 10-0458288 (Korean counterpart to US 6,885,055).

Ropes & Gray: Completed, 2018. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Qualcomm Inc. et al.*

GlaserWeil: Completed, 2016-2018. Technical evaluation and consulting in the matter of *KAIST IP US LLC v. Samsung Electronics Co., Ltd., Case No. 2:16-cv-01314*. Dr. Kuhn supported this litigation for the plaintiff as an expert witness. This included IPR proceedings (a total of 6 IPRs were presented to the PTO in this case). This also included completion and submission of the Claim Construction Declaration, the Infringement Report, and the Rebuttal Report, as well as depositions conducted on the contents of these Reports. This case went to trial June 11-15, where Dr. Kuhn presented both Direct testimony on infringement (6/12/18) and Rebuttal (6/14/18) testimony on validity.

yoR Labs Inc.: Completed. 2015-2017. yoR Labs is a medical instrumentation start-up, focusing on non-invasive medical imaging instrumentation. Dr. Kuhn served first as a member of the External Advisory Committee and later as a member of the Board of Directors. In this role, Dr. Kuhn provided technical and management support with regards to yoR labs operations.

Oregon State University, Department of Electrical Engineering and Computer Science: Completed. 2015 to 2018: Professor-courtesy. Prof. Kuhn’s role was establishment of long-term research programs in the area advanced CMOS technology and post-CMOS technology.

FORMER ROLES (2014 and PRIOR)

Intel, Portland, OR, (advanced development / research) 2008-2014 (retired in 2014)

Grade level: 12 (Fellow)

Manager: Mike Mayberry, VP

Dr. Kuhn's role was researching advanced device architectures for Intel processes in the 5-10 year time frame. While much of her work as an Intel Fellow remains proprietary, some of the public domain aspects are captured in her book *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits* (Cambridge, 2015) and her paper "Considerations for Ultimate CMOS Scaling," (IEEE Trans. on Elec. Dev., Vol: 59, No: 7, 2012, pp. 1813 – 1828 which won the Paul Rappaport Award). She received an Intel IAA in 2008 for her work on the TriGate transistor.

Intel, Portland, OR, (45nm Device technology manager in pathfinding) 2004-2008

Grade level: 10/11 (Principal Engineer / Sr. Principal Engineer)

Manager: Mark Bohr, Senior Intel Fellow / Kaizad Mistry, VP

Dr. Kuhn's role was as device technology manager of the pathfinding team responsible for the high-k metal-gate transistor architecture for Intel's 45nm microprocessor processor technology. She received an Intel IAA in 2006 for her work on high-k metal-gate.

Intel, Portland, OR, (90nm communication process manager) 2001-2004+

Grade level: 9/10 (Sr. Engineer / Principal engineer)

Manager: Scott Thompson (was Intel Fellow at the time, now a professor at Univ. of Florida).

Dr. Kuhn's role in this time frame was Process Program Manager of the team responsible for Intel's 90nm communications process technology. Over a 4-year period, this team developed a derivative analog/RF technology (including a SiGe BJT) on top of Intel's premium 90nm microprocessor process.

Other Intel experience:

Intel, Portland, OR, (130nm front-end integration engineer) 1998-2001

Intel, Portland, OR, (0.35um front-end integration engineer) 1997-1998

Grade level: 7-9 (Sr. engineering grades)

During the 130nm generation, Dr. Kuhn was an integration engineer responsible for the isolation section of the flow. 130nm was the last of the "classic" CMOS generations, and her work in that generation was updating the isolation process. She had the satisfaction of watching the work she did in the 130nm successfully scale through 90nm, 65nm, 45nm, and 32nm, with little change in the base process.

Dr. Kuhn joined Intel on the 0.35um generation as a sustaining integration engineer in F15. She was responsible for the silicide section of the flow. Additionally, she participated in the DIVD camera chip project (Intel's historical project to build CMOS camera chips).

Other relevant experience:

Univ. of Washington, Seattle, WA (Assoc. Prof., Ass't. Prof., Res. Ass't. Prof.), 1987-1997

Dr. Kuhn held faculty positions at the University of Washington (in Seattle) for roughly a decade in the order of Research Assistant Professor (Materials Science and Engineering), Assistant Professor (Electrical and Computer Engineering), and Associate Professor (Electrical and Computer Engineering). She left the University in 1997 as a tenured Associate Professor of Electrical and Computer Engineering. While at the Univ. of Washington, she achieved distinction in both research and teaching.

Highlights include:

- University of Washington, Distinguished Teaching Award, 1995 (UW's highest level of achievement for a faculty member)
- NSF Presidential Young Investigator award, 1991-6 (The National Science foundation is the most prestigious funding agency for faculty and the NSF PYI award is the most prestigious national level award for junior faculty).
- Single-author on a textbook, Laser Engineering, Prentice-Hall, 1998, ISBN 0-02-366921-7 (this is a mezzanine text discussing the theory and practice of building conventional and diode laser systems).

BOOKS

Laser Engineering, (sole author) Prentice-Hall, 1998, ISBN 0-02-366921-7

CMOS and Beyond: Logic Switches for Terascale Integrated Circuits (Co-editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015, ISBN 978-1107043183).

BOOK CHAPTERS

“The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8.

Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616) .

AWARDS:

Elected to the National Academy of Engineering (2023)
IEEE Frederik Philips Award (2016)
IEEE Paul Rappaport Award (2013)
IEEE Fellow (2011)

Intel Achievement Awards (Intel's highest technical award): IAA 2006 (for HiK-MG) and IAA 2008 (for key contributions to Intel's 22nm TriGate technology)

Intel Divisional Awards: Turbo operation (2009), RF Vccmin (2007), TCC (2005), SCD 1213.4 SCD/ICG (2004), LAD NW/Ophir A-1 (2003), SiGe BJT (2002), Hitachi etch (2002), 2um2SRAM (2001), Gamma Test chip (2000), Certification P854.6 (1999), F15 ISO 9000 (1998)

Academic Engineer of the Year Award, Puget Sound Engineering Council, 1996

University of Washington, Distinguished Teaching Award, 1995

College of Engineering, Outstanding Faculty Achievement Award, 1994

NSF Presidential Young Investigator award, 1991-6

NSF Research Initiation Award, 1989-91

IBM Graduate Fellowship, 1983-5

Hertz Graduate Fellowship, 1982-3

National Merit Scholar, 1976-80

JOURNAL PUBLICATIONS:

49. "First principles modeling of defects in the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ system", G. Greene-Diniz, K. Kuhn, P. Hurley, and J. Greer, *J. Appl. Phys.*, Vol. 121, No. 7, Jan. 2017.

48. "Doping top-down e-beam fabricated germanium nanowires using molecular monolayers," B. Long, G. Alessio Verni, J. O'Connell, M. Shayesteh, A. Gangnaik, Y.M. Georgiev, P. Carolan, D. O'Connell, K.J. Kuhn, S.B. Clendenning, R. Nagle, R. Duffy, and J.D. Holmes, *Materials Science in Semiconductor Processing*, Vol. 62, May 2017, pp. 196-200.

47. "Device Physics Modeling of Surfaces and Interfaces from an Induced Gap State Perspective," J. Wager and K. Kuhn, *Critical Reviews in Solid State and Materials Science*, Oct. 4, 2016.

46. "Adhesion Limits and Design Criteria for Nanorelays", Kevin L. Lin, Graham L. W. Cross, Peter Gleeson, Johann P. de Silva, Alejandro Levander, Jorge A. Muñoz, Chytra Pawashe, Alexis Potie, Patrick Theofanis, John J. Boland, and Dr. Kuhn J. Kuhn, *IEEE Trans. on Elec. Dev.*, Vol. 63, No. 1, Jan. 2016, 465-470.

45. Distributive Quasi-Ballistic Drift Diffusion Model Including Effects of Stress and High Driving Field, Roza Kotlyar,, Rafael Rios, Cory E. Weber, Thomas D. Linton, Mark Armstrong and Dr. Kuhn Kuhn, *IEEE Trans. on Elec. Dev.*, Vol. 62, No. 3, March 2015. Pp. 743-750.

44. Improved MOSFET characterization technique for single channel length, scaled transistors, Ferdousi, F., Rios, R., Kuhn K.J. *Solid State Electronics*, Vol. 104, pp. 44-6, Feb. 2015

43. Capacitance and Conductance for an MOS System in Inversion, with Oxide Capacitance and Minority Carrier Lifetime Extractions, Monaghan, S. O'Connor, E., Rios, R., Ferdousi, F., Floyd, L., Ryan, E., Cherhaoui, K., Povey, I.M., Kuhn, K.J., Hurley, P.K. *IEEE Transactions on Electron Devices*, Vol. 61, No. 12, pp. 4176-85, Dec. 2014.

42. First principle-based analysis of single-walled carbon nanotube and silicon nanowire Junctionless transistors, Ansari, L., Feldman, B., Faga, G., Martinez, L.C., Haverty, M.G., Kuhn, K.J., Shankar, S., Greer, J.C., IEEE Transactions on Nanotechnology, Vol. 12, No. 6, pp. 1075-81, Nov. 2013.
41. Scaling Limits of Electrostatic Nanorelays, Pawashe, C., Lin, K., Kuhn, K.J., IEEE Transactions on Electron Devices, Vol. 60, No. 9, pp. 2936-42, Sept. 2013,
40. Bandgap engineering of group IV materials for complementary n and p tunneling field effect transistors, Kotlyar, R.; Avci, U.E.; Cea, S.; Rios, R.; Linton, T.D.; Kuhn, K.J.; Young, I.A., Applied Physics Letters, v 102, n 11, March 18, 2013.
39. Effects of alternating current voltage amplitude and oxide capacitance on mid-gap interface state defect density extractions in InGaAs capacitors, Monaghan, Scott ; O'Connor, Eamon ; Povey, Ian M. ; Sheehan, Brendan J. ; Cherkaoui, Karim ; Hutchinson, Barry J. A. ; Hurley, Paul K. ; Ferdousi, Fahmida ; Rios, Rafael ; Kuhn, Dr. Kuhn J. ; Rahman, Anisur, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, Vol: 31 , No: 1, 2013, pp: 01A119 - 01A119-8.
38. Considerations for Ultimate CMOS Scaling, Dr. Kuhn J. Kuhn, invited review paper, IEEE Trans. on Elec. Dev., Vol: 59 , No: 7, 2012 , pp. 1813 – 1828 (won the Paul Rappaport Award)
37. Does the low hole transport mass in <110> and <111> Si nanowires lead to mobility enhancements at high field and stress: a self-consistent tight-binding study, R. Kotlyar, T. D. Linton, R. Rios, M. D. Giles, S. M. Cea, K. J. Kuhn, Michael Povolotskyi, Tillmann Kubis, and Gerhard Klimeck, Vol: 111 , No: 12, 2012, pp 123718 - 123718-11
36. Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm, Rios, R.; Cappellani, A.; Armstrong, M.; Budrevich, A.; Gomez, H.; Pai, R.; Rahhal-orabi, N.; Kuhn, K., IEEE Electron Device Letters, Vol. 32, No. 9, 2011, pp. 1170 - 1172
35. Process Technology Variation, Kuhn, K.J.; Giles, M.D.; Becher, D.; Kolar, P.; Kornfeld, A.; Kotlyar, R.; Ma, S.T.; Maheshwari, A.; Mudanai, S., IEEE Transactions on Electron Devices, Aug. 2011, vol.58, no.8, pp. 2197-208.
34. Moore's crystal ball: Device physics and technology past the 15nm generation, Kuhn, K.J., Microelectronic Engineering, July 2011, vol.88, no.7, pp. 1044-9.
33. Variability in nanoscale CMOS technology, Kuhn, K.J., K. Sci. China Inf. Sci. (2011) 54: 936. doi:10.1007/s11432-011-4219-6 (May 5, 2011).
32. Compressive Uniaxial Stress Bandstructure Engineering for Transferred-Hole Devices, Kotlyar, R.; Giles, M.D.; Mudanai, S.P.; Kuhn, K.J.; Cea, S.M.; Linton, T.D.; Pillarisetty, R.; IEEE Elec. Dev. Lett. Vol. 31, No. 8, 2010, pp. 878-880.

31. Managing process variation in Intel's 45 nm CMOS technology, Kuhn, K., Kenyon, C., Kornfeld, A., et al. Intel Technology Journal Volume: 12 Issue: 2 Pages: 93-4 Published: 17 June 2008
30. Analytical Modeling of Output Conductance in Long-Channel Halo-Doped MOSFETs, Electron Devices, Mudanai, S.; Shih, W.-K.; Rios, R.; Xi, X.; Rhew, J.-H.; Kuhn, K.; Packan, P.;, IEEE Transactions on Volume 53, Issue 9, Sept. 2006 Page(s):2091 - 2097
29. A 90-nm logic technology featuring strained-silicon, Thompson, S.E.; Armstrong, M.; Auth, C.; Alavi, M.; Buehler, M.; Chau, R.; Cea, S.; Ghani, T.; Glass, G.; Hoffman, T.; Jan, C.-H.; Kenyon, C.; Klaus, J.; Kuhn, K.; Zhiyong Ma; McIntyre, B.; Mistry, K.; Murthy, A.; Obradovic, B.; Nagisetty, R.; Phi Nguyen; Sivakumar, S.; Shaheed, R.; Shifren, L.; Tufts, B.; Tyagi, S.; Bohr, M.; El-Mansy, Y., IEEE Transactions on Electron Devices, vol.51, no.11, Nov. 2004. p. 1790-7.
28. Integration of mixed-signal elements into a high-performance digital CMOS process. Kuhn, K.J.; Ahmed, S.; Vandervoom, P.; Murthy, A. Intel Technology Journal, no.2, 2002
27. Elevated temperature performance of pseudomorphic AlGaAs/InGaAs MODFETs. Zurek, S.J.; Darling, R.B.; Kuhn, K.J.; Foisy, M.C. IEEE Transactions on Electron Devices, vol.45, no.1, Jan. 1998. p. 2-8
26. Synthetic wide bandpass X-ray polarizers. Cross, J.O.; Bennett, B.R.; Bell, M.I.; Kuhn, K.J. Applied Physics Letters, vol.70, no.17, 28 April 1997. p. 2224-6
25. Electro-optic polymer light modulator based on surface plasmon resonance. Jung, C.; Yee, S.; Kuhn, K. Applied Optics, vol.34, no.6, 20 Feb. 1995. p. 946-9
24. A "hands-on" course in consumer electronics design. Hannaford, B.; Kuhn, K. Mechatronics, vol.5, no.7, Oct. 1995. p. 753-62 Journal Paper
23. Finite element solutions to GaAs-AlAs quantum wells with connection matrices at heterojunctions. Li, T.L.; Kuhn, K.J. Journal of Computational Physics, vol.115, no.2, Dec. 1994. p. 288-95
22. Integrated optics waveguide modulator based on surface plasmon resonance. Jung, C.; Yee, S.; Kuhn, K. Journal of Lightwave Technology, vol.12, no.10, Oct. 1994. p. 1802-6
21. Effects of spin-orbit interaction on the envelope-function equations for semiconductor heterostructures. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.50, no.12, 15 Sept. 1994. p. 8589-601
20. Effects of mass discontinuity on the numerical solutions to quantum wells using the effective mass equation. Li, T.L.; Kuhn, K.J. Journal of Computational Physics, vol.110, no.2, Feb. 1994. p. 292-300

19. Validity of the connection-matrix approach to GaAs-Al/sub x /Ga/sub $1-x$ /As quantum wells. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.49, no.4, 15 Jan. 1994. p. 2608-14
18. Optical properties due to intersubband transitions in n-type quantum wells including the effects of the exchange interaction. Sengers, A.J.; Tsang, L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.48, no.20, 15 Nov. 1993. p. 15116-22
17. Band-offset ratio dependence on the effective-mass Hamiltonian based on a modified profile of the GaAs-Al/sub x /Ga/sub $1-x$ /As quantum well. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.47, no.19, 15 May 1993. p. 12760-70
16. Use of active loads with MSM photodetectors in digital GaAs MESFET photoreceivers. Darling, R.B.; Youn, H.J.; Kuhn, K.J. Journal of Lightwave Technology, vol.10, no.11, Nov. 1992. p. 1597-605
15. Mobility of strained and dislocated In/sub x /Ga/sub $1-x$ /As semiconductor material. Kuhn, K.J.; Darling, R.B. IEEE Transactions on Electron Devices, vol.39, no.6, June 1992. p. 1288-94
14. Dislocation scattering in n-type modulation doped Al/sub 0.3/Ga/sub 0.7/As/In/sub x /Ga/sub $1-x$ /As/Al/sub 0.3/Ga/sub 0.7/As quantum wells. Zhao, D.; Kuhn, K.J. IEEE Transactions on Electron Devices, vol.38, no.12, Dec. 1991. p. 2582-9
13. Free carrier induced changes in the absorption and refractive index for intersubband optical transitions in Al/sub x /Ga/sub $1-x$ /As/GaAs/Al/sub x /Ga/sub $1-x$ /As quantum wells. Kuhn, K.J.; Iyengar, G.U.; Yee, S. Journal of Applied Physics, vol.70, no.9, 1 Nov. 1991. p. 5010-17
12. Electric field effects in AlGaAs-GaAs symmetric and asymmetric coupled quantum wells. Juang, C.; Kuhn, K.J.; Darling, R.B. IEEE Journal of Quantum Electronics, vol.27, no.9, Sept. 1991. p. 2122-8
11. Effect of etch treatment prior to Schottky contact fabrication on In/sub 0.05/Ga/sub 0.95/As. Johnson, M.J.; Kuhn, K.J.; Darling, R.B. Applied Physics Letters, vol.58, no.17, 29 April 1991. p. 1893-5
10. An enhanced and linear Stark shift in n-i-n AlGaAs/GaAs symmetric and asymmetric coupled quantum wells. Kuhn, K.J.; Cheng Juang; Darling, R.B. Journal of Applied Physics, vol.69, no.5, 1 March 1991. p. 3135-41
9. AlGaAs-GaAs multiple-quantum-well spectrally tunable photoconductors. Youn, H.J.; Darling, R.B.; Kuhn, K.J. IEEE Photonics Technology Letters, vol.3, no.2, Feb. 1991. p. 159-61
8. Effect of AlGaAs window and buffer layers on the response characteristics of GaAs photoconductive detectors. Youn, H.J.; Darling, R.B.; Kuhn, K.J. Applied Physics Letters, vol.57, no.19, 5 Nov. 1990. p. 2001-3

7. Selective etching of GaAs and Al/sub 0.30/Ga/sub 0.70/As with citric acid/hydrogen peroxide solutions. Juang, C.; Kuhn, K.J.; Darling, R.B. Journal of Vacuum Science & Technology B (Microelectronics Processing and Phenomena), vol.8, no.5, Sept.-Oct. 1990. p. 1122-4
6. Stark shift and field-induced tunneling in Al/sub x/Ga/sub 1-x/As/GaAs quantum-well structures. Juang, C.; Kuhn, K.J.; Darling, R.B. Physical Review B (Condensed Matter), vol.41, no.17, 15 June 1990. p. 12047-53
5. An indium-free substrate holder for radiative heating of quarter-wafer molecular-beam epitaxy samples. Kuhn, K.J. Review of Scientific Instruments, vol.61, no.1, pt.1, Jan. 1990. p. 184-5
4. Variation in GaAs surface oxide desorption temperature as a function of shuttered aluminum oven temperature. Kuhn, K.J.; Pubanz, G.A. Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films), vol.7, no.6, Nov.-Dec. 1989. p. 3265-8
3. Static gas conduction cooled slab geometry Nd:glass laser. Reed, M.; Kuhn, K.; Unternahrer, J.; Byer, R.L. IEEE Journal of Quantum Electronics, vol.QE-21, no.5, May 1985. p. 412-14
2. The slab geometry laser. I. Theory. Eggleston, J.M.; Kane, T.J.; Kuhn, K.; Unternahrer, J. IEEE Journal of Quantum Electronics, vol.QE-20, no.3, March 1984. p. 289-301
1. Implementation of Distributed Microprocessor Systems in Custom Heavy Trucks, K.J. Kuhn, 1979-80 IEEE Student Papers, Vol. TT0114 IEEE, pg. 334-342.

CONFERENCE PUBLICATIONS

54. Bias temperature instability variation on SiON/Poly, HK/MG and trigate architectures, C. Prasad, M. Agostinelli, J. Hicks, S. Ramey, C. Auth, K. Mistry, S. Natarajan, P. Packan, I. Post, S. Bodapati, M. Giles, S. Gupta, S. Mudani and K. Kuhn, 2014 IEEE International Reliability Physics Symposium (IRPS), June 2014.
53. Semiconductors Stand Aside, the Age of Metals is Here! K. Kuhn, A. Sanchez, C. George, R. Rios, J. Clarke, J. Greer, Lester Eastman Conference, Cornell, May 2014.
52. The ultimate CMOS device and beyond, Kuhn, K.J. ; Avci, U. ; Cappellani, A. ; Giles, M.D. ; Haverty, M. ; Seiyon Kim ; Kotlyar, R. ; Manipatruni, S. ; Nikonov, D. ; Pawashe, C. ; Radosavljevic, M. ; Rios, R. ; Shankar, S. ; Vedula, R. ; Chau, R. ; Young, I. 2012 IEEE International Electron Devices Meeting (IEDM), pp. 171-174.
51. Understanding the feasibility of scaled III-V TFET for logic by bridging atomistic simulations and experimental results, Avci, U.E. ; Hasan, S. ; Nikonov, D.E. ; Rios, R. ; Kuhn, K. ; Young, I.A., Symposium on VLSI Technology (VLSIT), 2012, pp: 183 – 184.
50. Beyond the Planar Transistor: Progress in Next Generation Switches, K. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

49. Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation, K. Kuhn, INFOS 2011 (June 22, 2011, France)
48. Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET, Avci, U.E.; Rios, R.; Kuhn, K.J.; Young, I.A., IEEE Conference on Nanotechnology (IEEE-NANO), 2011 11th, pp. 869 – 872
47. Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic, Avci, U.E.; Rios, R.; Kuhn, K.; Young, I.A., 2011 Symposium on VLSI Technology (VLSIT), 2011 , pp. 124 – 125
46. CMOS scaling for the 22nm node and beyond: Device physics and technology, Kuhn, K.J., 2011 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2011 , pp. 1 – 2
45. Past, Present and Future: SiGe and CMOS Transistor Scaling. K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, ECS 2010, Oct. 10, Las Vegas, CA, USA.
44. Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, K. J. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.
43. CMOS transistor scaling past 32nm and implications on variation, K. Kuhn, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA, pp. 241-246.
42. Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, K. Kuhn, Nikkei Electronics Symposium, June 29th, 2010.
41. Technology options for 22nm and beyond, K. Kuhn, Technology, Kuhn, K.J.; Liu, M.Y.; Kennel, H.; 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.
40. CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California
39. Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10th September 2009, Leixlip, Co. Kildare.
38. Moore's Law Past 32nm: The Challenges in Physics and Technology Scaling, K. Kuhn, Solid State Devices and Materials Conference (SSDM), September 18, 2009, Sendai, Japan.
37. CMOS scaling beyond 32 nm: challenges and opportunities, Kuhn, K.J., 2009 46th ACM/IEEE Design Automation Conference (DAC), 26-31 July 2009, San Francisco, CA, USA, Pages: 310-13 Published: 2009

36. Future device scaling: beyond traditional CMOS, Tyagi, S., Auth, C., Ban, I., et al., 2009 2nd International Workshop on Electron Devices and Semiconductor Technology (IEDST), 1-2 June 2009, Mumbai, India, (IEDST) Pages: 4 pp. Published: 2009
35. Variation in 45nm and Implications for 32nm and Beyond, K. Kuhn, NMI International Conference on CMOS Variability, 12th & 13th May 2009, London, UK.
34. Moore's law past 32 nm: future challenges in device scaling, Kuhn, K.J., 2009 13th International Workshop on Computational Electronics (IWCE 2009), 27-29 May 2009, Beijing, China, (IWCE 2009) Pages: 6 pp. Published: 2009
33. 22 nm Device Architecture and Performance Elements, K.J. Kuhn, IEEE International Electron Devices Meeting, 15-17 December 2008, San Francisco, CA, USA , IEDM short course.
32. High performance hi-k + metal gate strain enhanced transistors on (110) silicon, Packan, P., Cea, S., Deshpande, H., Kuhn, K, et. al. IEDM 2008. IEEE International Electron Devices Meeting, 15-17 December 2008, San Francisco, CA, USA, IEDM 2008. IEEE International Electron Devices Meeting. Technical Digest Pages: 4 pp. Published: 2008
31. 45 nm high-k + metal gate strain-enhanced transistors, Auth, C., Cappellani, A., Chun, J.-S., Kuhn, K. et al, 2008 Symposium on VLSI Technology, 17-20 June 2008, Honolulu, HI, USA, Pages: 128-9 Published: 17 June 2008
30. Dielectric breakdown in a 45 nm high-K/metal gate process technology, Prasad, C., Agostinelli, M., Auth, C., Kuhn, K. et al, 2008 IEEE International Reliability Physics Symposium (IRPS), 27 April-1 May 2008, Phoenix, AZ, USA, Pages: 667-8 Published: 2008
29. BTI reliability of 45 nm high-K + metal-gate process technology, Pae, S., Agostinelli, M., Brazier, M., Kuhn, K, et al. 2008 IEEE International Reliability Physics Symposium (IRPS), 27 April-1 May 2008, Phoenix, AZ, USA, (IRPS) Pages: 352-7 Published: 2008
28. Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4 Published: 2007
27. A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging, Mistry, K., Allen, C., Auth, C., Kuhn, K. et al., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA , IEDM '07 Pages: 247-50 Published: 2007
26. High performance 35nm L/sub GATE/ CMOS transistors featuring NiSi metal gate (FUSI), uniaxial strained silicon channels and 1.2nm gate oxide, Ranade, P.; Ghani, T.; Kuhn, K.; Mistry, K.; Pae, S.; Shifren, L.; Stettler, M.; Tone, K.; Tyagi, S.; Bohr, M.; Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International, 5-7 Dec. 2005 Page(s):4 pp.

25. Noise performance of 90 nm CMOS technology, Becher, D.; Banerjee, G.; Basco, R.; Hung, C.; Kuhn, K.; Wei-Kai Shih, 2004 IEEE MTT-S International Microwave Symposium Digest (IEEE Cat. No.04CH37535). Piscataway, NJ, USA: IEEE, 2004. p. 17-20 Vol.1. Conference Paper.
24. A comparison of state-of-the-art NMOS and SiGe HBT devices for analog/mixed-signal/RF circuit applications, Kuhn, K.; Basco, R.; Becher, D.; Hattendorf, M.; Packan, P.; Post, I.; Vandervoorn, P.; Young, I., 2004 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.04CH37526). Gaithersburg, MD, USA: Widerkehr and Associates, 2004. p. 224-5. Conference Paper.
23. A 90 nm communication technology featuring SiGe HBT transistors, RF CMOS, precision R-L-C RF elements and 1 /spl mu/m/sup 2/ 6-T SRAM cell, Kuhn, K.; Agostinelli, M.; Ahmed, S.; Chambers, S.; Cea, S.; Christensen, S.; Fischer, P.; Gong, J.; Kardas, C.; Letson, T.; Henning, L.; Murthy, A.; Muthali, H.; Obradovic, B.; Packan, P.; Pae, S.W.; Post, I.; Putna, S.; Raol, K.; Roskowski, A.; Soman, R, "" Electron Devices Meeting, 2002. IEDM '02. Digest. International , 8-11 Dec. 2002 Page(s): 73 -76
22. A 90 nm Generation BiCMOS Technology for Analog, Mixed-signal, and RF Applications, K. Kuhn, S. Chambers, C. Kardas, T. Letson, A.-Murthy and P. Packan, Intel Process Technology Conference, October, 17, 2002. (Best of session paper award)
21. Scaling challenges for 0.13 mu m generation shallow trench isolation, Kuhn, K.J.; Din-how Mei; Post, I.; Neiryneck, J., 2001 IEEE International Symposium on Semiconductor Manufacturing. ISSM 2001. Conference Proceedings (Cat. No.01CH37203). Piscataway, NJ, USA: IEEE, 2001. p. 187-90 Conference Paper
20. Scaling challenges for 0.13 mu m generation shallow trench isolation, Kuhn, K.J.; Din-how Mei; Post, I.; Neiryneck, J., and Au, W., Intel Process Technology Conference, October, 10, 2000.
19. Electrical critical dimension metrology for 100 nm linewidths and below. Grenville, A.; Coombs, B.; Hutchinson, J.; Kuhn, K. Proceedings of the SPIE - The International Society for Optical Engineering, vol.4000, pt.1-2, 2000. p. 452-9 Conference Paper
18. The performance of a wide band X-ray Bragg polarizer grown by molecular beam epitaxy, Cross, J.O.; Bennett, B.R.; Bell, M.I.; Kuhn, K.J., , AIP Conference Proceedings, no.417, 1997. p. 117
17. Solving the 3 and 4 state laser systems, Dr. Kuhn Kuhn, regular paper, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.
16. An integrated course in laser engineering, K. Kuhn, regular paper #1232, ASEE 1996 annual conference, Washington DC, June 22-26, 1996.

15. Development of a course in Consumer Electronics, K. Kuhn and B. Hannaford, regular paper #3232, ASEE 1996 annual conference, Washington DC, June 22-26, 1996.
14. An Erbium-doped fiber laser, C. Cornish and K. Kuhn, 1995 Progress in Electromagnetics Research Symposium, July 24-28, 1995.
13. Development of a course in Consumer Electronics, K. Kuhn and B. Hannaford, Session 3B, Mechatronics Conference, Stanford, July 15-17, 1994.
12. Integrated optical waveguide modulator using long range surface plasmon resonance, C. Jung, S. Yee and K. Kuhn, OSA Integrated Photonics Research Conference, San Francisco, CA. February 17-19 (1994)
11. Evaluation of an ion-exchanged integrated optic waveguide for solution phase chemical sensing. Kuhn, K.J.; Burgess, L.W. Proceedings of the SPIE - The International Society for Optical Engineering, vol.1796, 1993. p. 332-42 Conference Paper
10. A. Sengers, G. Iyengar, L. Tsang and K. Kuhn, "Optical Properties due to Intersubband Transitions in n-type Quantum Wells Including the Effects of the Exchange Interaction", 1993 March meeting of the American Physical Society, Seattle, WA 22-26 March 1993.
9. Free carrier induced changes in the absorption and refractive index for intersubband optical transitions in $\text{Al}_{\text{sub } x}/\text{Ga}_{\text{sub } 1-x}/\text{As}/\text{GaAs}/\text{Al}_{\text{sub } x}/\text{Ga}_{\text{sub } 1-x}/\text{As}$ quantum wells. Iyengar, G.U.; Kuhn, K.J.; Yee, S. In: Gallium Arsenide and Related Compounds 1991. Proceedings of the Eighteenth International Symposium. Bristol, UK: IOP, 1992. p. 431-6 Conference Paper
8. Free carrier induced changes in the absorption and refractive index for intersubband optical transitions in $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$ quantum wells, G. Iyengar, K. Kuhn, and S. Yee, Conference Proceedings, 17th International Symposium on GaAs and Related Compounds, September 9-12, 1991; Seattle, WA.
7. Applications of Molecular Beam Epitaxy to Integrable Optical Devices, K.J. Kuhn, Professional program, Northcon/88, October 5, 1988.
6. Laser annealing of AlGaAs, E. Riemer, K. Song, K. Kuhn and T. Stoebe, Atomic and Molecular Processing of Electronics and Ceramic Materials, 23 Conf. on Ceramic Science, UW, August 30 to September 3, 1987.
5. Amplified Spontaneous Emission in Slab Lasers, D.C. Brown, K.J. Kuhn, Kotik K. Lee and R.L. Byer, paper WE-5, Conference on Lasers and Electro-optics (CLEO), Anaheim, CA, June 1984.
4. Progress in high peak and average power lasers for soft X-ray production. Byer, R.L.; Kuhn, K.; Reed, M.; Trail, J. Proceedings of the SPIE - The International Society for Optical Engineering, vol.448, 1984. p. 2-7 Conference Paper

3. Conductive-cooling of Slab Lasers, K.J. Kuhn, T.J. Kane, and R.L. Byer, paper WE-3, 1982 Annual meeting of the Optical Society of America, Tucson, Arizona, October 1982.
2. Progress in slab geometry solid state lasers. Eggleston, J.M.; Kane, T.; Kuhn, K.; Byer, R.L. Proceedings of the SPIE - The International Society for Optical Engineering, vol.335, 1982. p. 104-8 Conference Paper
1. Implementation of distributed microprocessor systems in custom heavy trucks. Kuhn, K.J. In: Wescon/80 Conference Record. El Segundo, CA, USA: Electron. Conventions, 1980. p. SS2-3/1-8 Conference Paper.

PATENTS

	PAT. NO.	Title
1	11,302,777	Integration methods to fabricate internal spacers for nanowire devices
2	11,195,919	Method of fabricating a semiconductor device with strained SiGe fins and a Si cladding layer
3	11,139,400	Non-planar semiconductor device having hybrid geometry-based active region
4	11,024,714	Nanowire transistor fabrication with hardmask layers
5	10,991,799	Silicon and silicon germanium nanowire structures
6	10,825,752	Integrated thermoelectric cooling
7	10,804,357	Integration methods to fabricate internal spacers for nanowire devices
8	10,636,871	Silicon and silicon germanium nanowire structures
9	10,593,804	Non-planar semiconductor device having hybrid geometry-based active region
10	10,586,868	Non-planar semiconductor device having hybrid geometry-based active region
11	10,580,899	Nanowire structures having non-discrete source and drain regions
12	10,580,860	Integration methods to fabricate internal spacers for nanowire devices
13	10,535,770	Scaled TFET transistor formed using nanowire with surface termination
14	10,424,580	Semiconductor devices having modulated nanowire counts
15	10,283,589	Integration methods to fabricate internal spacers for nanowire devices
16	10,121,861	Nanowire transistor fabrication with hardmask layers
17	10,121,856	Integration methods to fabricate internal spacers for nanowire devices
18	10,115,822	Methods of forming low band gap source and drain structures in microelectronic devices
19	10,109,711	CMOS FinFET device having strained SiGe fins and a strained Si cladding layer on the NMOS channel
20	10,074,573	CMOS nanowire structure
21	10,074,357	Integrated acoustic phase array
22	10,026,829	Semiconductor device with isolated body portion
23	9,978,636	Isolated and bulk semiconductor devices formed on a same bulk substrate
24	9,947,805	Nanowire-based mechanical switching device
25	9,935,205	Internal spacers for nanowire transistors and method of fabrication thereof
26	9,935,107	CMOS FinFET device with dual strained cladding layers on relaxed SiGe fins, and method of fabricating the same
27	9,926,193	Magnetic nanomechanical devices for stiction compensation

28	9,911,835	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
29	9,893,167	Integration methods to fabricate internal spacers for nanowire devices
30	9,882,053	Molded dielectric fin-based nanostructure
31	9,859,368	Integration methods to fabricate internal spacers for nanowire devices
32	9,825,130	Leakage reduction structures for nanowire transistors
33	9,812,524	Nanowire transistor devices and forming techniques
34	9,691,843	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
35	9,680,013	Non-planar device having uniaxially strained semiconductor body and method of making same
36	9,673,302	Conversion of strain-inducing buffer to electrical insulator
37	9,614,060	Nanowire transistor with underlayer etch stops
38	9,608,059	Semiconductor device with isolated body portion
39	9,595,581	Silicon and silicon germanium nanowire structures
40	9,583,602	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
41	9,583,491	CMOS nanowire structure
42	9,564,522	Nanowire structures having non-discrete source and drain regions
43	9,559,160	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
44	9,508,796	Internal spacers for nanowire transistors and method of fabrication thereof
45	9,484,447	Integration methods to fabricate internal spacers for nanowire devices
46	9,472,613	Conversion of strain-inducing buffer to electrical insulator
47	9,425,212	Isolated and bulk semiconductor devices formed on a same bulk substrate
48	9,412,872	N-type and P-type tunneling field effect transistors (TFETs)
49	9,385,221	Nanowire transistor with underlayer etch stops
50	9,362,074	Nanowire-based mechanical switching device
51	9,355,242	Method and apparatus for managing and accessing personal data
52	9,343,559	Nanowire transistor devices and forming techniques
53	9,287,576	Self-powered internal medical device
54	9,258,114	Quantum key distribution (QSD) scheme using photonic integrated circuit (PIC)
55	9,224,810	CMOS nanowire structure
56	9,183,829	Integrated acoustic phase array

57	9,129,829	Silicon and silicon germanium nanowire structures
58	9,129,827	Conversion of strain-inducing buffer to electrical insulator
59	9,105,344	Shut-off mechanism in an integrated circuit device
60	9,087,863	Nanowire structures having non-discrete source and drain regions
61	9,064,944	Nanowire transistor with underlayer etch stops
62	9,029,221	Semiconductor devices having three-dimensional bodies with modulated heights
63	9,012,284	Nanowire transistor devices and forming techniques
64	8,890,120	Tunneling field effect transistors (TFETs) for CMOS approaches to fabricating N-type and P-type TFETs
65	8,853,741	Junctionless accumulation-mode devices on decoupled prominent architectures
66	8,766,372	Copper-filled trench contact for transistor performance improvement
67	8,753,942	Silicon and silicon germanium nanowire structures
68	8,558,279	Non-planar device having uniaxially strained semiconductor body and method of making same
69	8,507,948	Junctionless accumulation-mode devices on prominent architectures, and methods of making same
70	8,487,348	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
71	8,269,283	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
72	8,258,057	Copper-filled trench contact for transistor performance improvement
73	7,999,607	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
74	7,888,710	CMOS fabrication process utilizing special transistor orientation
75	7,737,770	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
76	7,312,485	CMOS fabrication process utilizing special transistor orientation
77	6,627,506	Thin tensile layers in shallow trench isolation and method of making same
78	6,368,931	Thin tensile layers in shallow trench isolation and method of making same
79	4,617,669	Method and apparatus for pumping laser slabs
80	4,563,763	Method and apparatus for cooling a slab laser

INVITED TECHNICAL PRESENTATIONS/SEMINARS :

Invited panel, IEDM, Variation and the End of the World, December, 2013.

Keynote, The End of Scaling?, ICTC, December 2013.

Invited seminar, CMOS and Beyond, Portland State University, October, 2013.

Keynote panel, CMOS and Beyond: Future Device Technology, ENF 2013, Ireland, June 2013.

Invited seminar, CMOS and Beyond: Future Device Technology for the Mobile World, IDF, May 2013.

Invited Workshop, The Future is Already Here: Evolving Concepts in Device and Materials Technology, AMAT, March 2013.

Invited paper, "The Ultimate CMOS Device and Beyond," IEDM 2012, San Francisco.

Invited talk, Beyond Simply Small: Progress in Advanced Transistor Architectures, Cornell, November 2012.

Invited seminar, Demystifying Moore's Law How it Really Works!, IDF, Sept. 2012, San Francisco.

Invited talk, The Ultimate CMOS Device and Beyond, Ireland, April 2012.

Keynote: "MOS scaling for the 22nm node and beyond: Device physics and technology," April 24, 2011, Taiwan, VLSI-TSA

Plenary: "Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation," INFOS 2011 (June 22, 2011, France)

Keynote: "Beyond the Planar Transistor: Progress in Next Generation Switches," Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

Invited seminar - "Polishing Moore's Crystal Ball: Advanced Transistor Architectures ...and Beyond," K. Kuhn, March 30th. 2011, MIT, MTL seminar series.

Invited seminar - "Emerging Devices: Moore's Law and Advanced Transistor Architectures," K. Kuhn, Varian Technology Symposium, March 31st. 2011.

Keynote: "Scaling Electronics:Trends and Bottlenecks," K. Kuhn, April 4th. 2011, MIT Microphotonics meeting.

Invited seminar - "Gazing into Moore's Crystal Ball: Transistor Scaling after the 15nm node," K. Kuhn, Feb. 17th, 2010, Berkeley.

IEDM 2010 Short Course chair for 15nm technology, December 2010.

Plenary: Past, Present and Future: SiGe and CMOS Transistor Scaling, ECS 2010, Oct. 10, Las Vegas, CA, USA.

Keynote: Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.

Plenary: CMOS transistor scaling past 32nm and implications on variation, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA

Keynote: Technology options for 22nm and beyond, K. Kuhn, 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.

Invited seminar: Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, Nikkei Electronics Symposium / June 29th, 2010.

Plenary - CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California

Keynote - Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10th September 2009, Leixlip, Co. Kildare.

Plenary - Moore's Law Past 32nm: The Challenges in Physics and Technology Scaling, K. Kuhn, Solid State Devices and Materials Conference (SSDM), September 18, 2009, Sendai, Japan.

Invited talk - CMOS scaling beyond 32 nm: challenges and opportunities, Kuhn, K.J., 2009 46th ACM/IEEE Design Automation Conference (DAC), 26-31 July 2009, San Francisco, CA, USA, Pages: 310-13 Published: 2009

Keynote - Variation in 45nm and Implications for 32nm and Beyond, K. Kuhn, NMI International Conference on CMOS Variability, 12th & 13th May 2009, London, UK.

Invited talk - Moore's law past 32 nm: future challenges in device scaling, Kuhn, K.J., 2009 13th International Workshop on Computational Electronics (IWCE 2009), 27-29 May 2009, Beijing, China, (IWCE 2009) Pages: 6 pp. Published: 2009

Invited – International Electron Device meeting – short course.
http://download.intel.com/pressroom/pdf/kkuhn/Kuhn_22nm_Device.pdf

Invited seminar - “45nm High-k + Metal Gate Logic Technology,” K. Kuhn, May 2008, MIT, MTL laboratory.

Invited talk - Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4

Invited seminar - "CMOS Transistor Architecture Challenges and Opportunities," K. Kuhn, September 2005, MIT, MTL laboratory.

Keynote - "Nanotechnology Challenges and Opportunities," K. Kuhn, January 2005, MIT, MTL laboratory.

Invited seminar - "Transistor Scaling and its Impact on Analog/RF Device Performance", Dr. Kuhn Kuhn, March 2005, Stanford University, invited seminar.

Invited seminar - "Advanced transistor architecture approaches and their implications for device and circuit performance," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2004.

Invited seminar - "Moore's Law meets Materials Science", Dr. Kuhn Kuhn, September 2004, University of Washington.

Invited seminar - "Centrino, convergence of computing and communications," November 2003, Dr. Kuhn Kuhn, Stanford University, invited seminar.

Invited seminar - "Challenges in the parallel development of the 90nm communications (121x) and microprocessor (1262) process technologies," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2003.

Invited seminar - "RF/analog integration with 90nm digital CMOS", Dr. Kuhn Kuhn, MIT invited seminar, March 2003

Invited seminar - "Femtosecond pulse laser technology", Dr. Kuhn Kuhn, Oregon State University, March 10, 1997.

Invited talk- "Symbolic Solvers and their impact on engineering education", Dr. Kuhn Kuhn, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.

APPENDIX B

Appendix B

List of Materials Considered

Exhibit No.	DESCRIPTION
1001	U.S. Patent No. 10,872,903 (“’903”)
1002	File History of U.S. Patent Application No. 16/716,177 (“’903FH”)
1004	Certified Translation of Korean Patent Application Publication No. 10-2010-0034612 (“Ahn”)
1005	Korean Patent Application Publication No. 10-2010-0034612
1006	U.S. Patent Application Publication No. 2009/0146190 (“Fukuzumi”)
1007	U.S. Patent Application Publication No. 2009/0283819 (“Ishikawa”)
1008	U.S. Patent No. 5,596,523 (“Endoh”)
1009	U.S. Patent No. 6,765,825 (“Scott”)
1010	U.S. Patent Application Publication No. 2010/0240205 (“Son”)
1011	U.S. Patent Application Publication No. 2009/0242967 (“Katsumata”)
1012	U.S. Patent Application Publication No. 2009/0310425 (“Sim”)
1013	U.S. Patent Application Publication No. 2010/0019310 (“Sakamoto”)
1014	Joint Claim Construction and Prehearing Statement (Patent Local Rule 4-3), <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 105 (N.D. Cal. August 19, 2024)
1015	“Extended Data Retention Process Technology for Highly Reliable Flash EEPROMs of 10^6 to 10^7 W/E Cycles” by F. Arai et al. (1998)

Exhibit No.	DESCRIPTION
1016	“A High-Endurance (>100K) BE-SONOS NAND Flash With a Robust Nitrided Tunnel Oxide/Si Interface” by S. Wang et al. (2010)
1017	“Flash Memory Reliability NEPP 2008 Task Final Report” by Y. Chen (2009)
1018	Counterclaim Plaintiff Micron Technology’s Disclosure of Asserted Claims and Infringement Contentions and Document Production Accompanying Disclosure (Patent Local Rules 3-1 and 3-2), <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL (N.D. Cal.)
1019	U.S. Patent Application Publication No. 2008/0116441A1 (Raghuram)
1020	“Growth characteristics and electrical resistivity of chemical vapor-deposited tungsten film” by I-Shun Chang (1998)
1022	“Nitride Engineering and the Effect of Interfaces on Charge Trap Flash Performance and Reliability” by Sandhya C. (2008)
1023	Excerpts of “Polycrystalline Silicon for Integrated Circuits and Displays” by Ted Kamins (1998)
1024	Print-out of IEEE webpage (dated November 8, 2024)
1025	U.S. Patent No. 7,425,742 (Nazarian)
1026	U.S. Patent Application Publication No. 2007/0057328 (“Taniguchi”)
1027	“Shrinking Possibilities” by B. Arnold (2009)