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I, Somee Lee, hereby declare:

That, I, possess advanced knowledge of Korean and English. My qualifications are:

4.5 years of experience as Korean-English translator, including patents, contracts, etc.

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I attach the translation herein, which is, to the best of my knowledge and belief, a true and accurate translation of Korean patent application publication KR10- 2010-0034612, which is in Korean, to English. All statements made in this declaration of my own knowledge are true and all statements made on information and belief are believed to be true. I make these statements with the understanding that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001).

I declare under penalty of perjury that the forgoing is true and correct.

Executed on this 8th day of September, 2024.
At: Queens, New York

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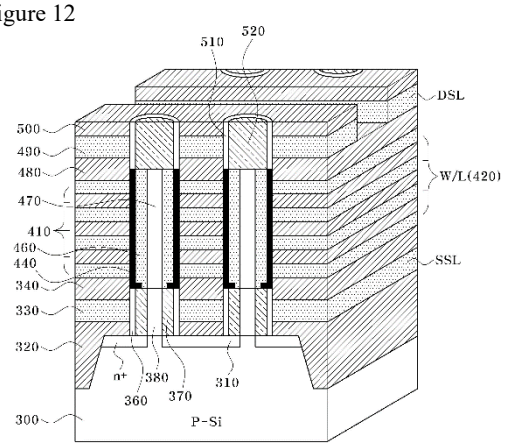
(54) Method for Manufacturing a Flash Memory Device Having a Three-dimensional Structure

(57) Summary

A method for manufacturing a flash memory device of the present invention includes a step of forming a source region on a substrate, a step of forming a source select transistor connected to the source region on the substrate, a step of forming gates of a plurality of memory cells by alternately forming insulating layers and conductive layers multiple times on a substrate on which a source select transistor is formed, a step of forming a through hole by etching the insulating layer and the conductive layer to expose the channel region of the source select transistor, a step of forming a charge storage region consisting of a tunneling layer, a charge trap layer, and a blocking layer on the inner wall of the through hole, a step of forming a protective film on the inner sidewall of a through hole in which a charge storage region is formed, a step of exposing a channel region of a source select transistor, a step of forming a channel region of a cell transistor by filling the through hole with a semiconductor layer, and a step of forming a drain select transistor on the cell transistor.

Representative Figure - Figure 12



Scope of Claims

Claim 1

A method for manufacturing a flash memory device, characterized by including a step of forming a source region on a substrate;

a step of forming a source select transistor connected to the source region on the above substrate;

a step of forming gates of a plurality of memory cells by alternately forming insulating layers and conductive layers multiple times on a substrate on which the above source select transistor is formed;

a step of forming a through hole by etching the above insulating layer and the conductive layer to expose the channel region of the above source select transistor;

a step of forming a charge storage region consisting of a tunneling layer, a charge trap layer, and a blocking layer on the inner wall of the above through hole;

a step of forming a protective film on the inner sidewall of a through hole in which the above charge storage region is formed;

a step of exposing a channel region of the above source select transistor;

a step of forming a channel region of a cell transistor by filling the above through hole with a semiconductor layer; and

a step of forming a drain select transistor on the above cell transistor.

Claim 2

In Claim 1,

A method for manufacturing a flash memory device, characterized in that the step of forming the source select transistor is composed of,

a step of sequentially stacking an insulating layer and a conductive layer on the above substrate,

a step of etching the insulating layer and the conductive layer to form a through hole exposing the above source region,

a step of forming a gate insulating film on the inner wall of the above through hole,

a step of etching the above gate insulating film so that the above source region is exposed,

and a step of forming a channel region of a source select transistor by filling the above through hole with a semiconductor layer.

Claim 3

In Claim 1,

A method for manufacturing a flash memory device, characterized in that the above protective film is formed of a polysilicon film or a nitride film.

Claim 4

In Claim 1,

A method for manufacturing a flash memory device, characterized in that the above protective film is removed before filling the above through hole with a semiconductor layer.

Claim 5

In Claim 1,

A method for manufacturing a flash memory device, characterized in that the above conductive layer for forming a gate of the above memory cell is formed of polysilicon or metal.

Claim 6

In Claim 1,A method for manufacturing a flash memory device, characterized in that, in the step of forming the above tunneling layer,

a silicon compound is deposited in an atmosphere containing oxygen or oxygen and nitrogen.

Claim 7

In Claim 6,

A method for manufacturing a flash memory device, characterized in that, after the above step of forming the tunneling layer,

it further includes a step of heat treatment in an NO or N2O atmosphere.

Claim 8

A method for manufacturing a flash memory device, characterized by including a step of forming a source region on a

substrate;

a step of forming an insulating film and a conductive layer on the above substrate;

a step of forming a first through hole exposing the above source region;

a step of sequentially forming a gate insulating film and a channel region of a source select transistor on a sidewall of the first through hole above;

a step of forming a well in the above source region of the region exposed by the first through hole;

a step of forming a well of a source select transistor by filling the above first through hole;

a step of forming gates of a plurality of memory cells by alternately forming insulating layers and conductive layers multiple times on a substrate on which a well of the above source select transistor is formed;

a step of forming a second through hole by etching the above insulating layer and the conductive layer to expose the channel region of the above source select transistor;

a step of forming a charge storage region consisting of a tunneling layer, a charge trap layer, and a blocking layer on the inner wall of the above second through hole;

a step of etching the charge storage region at the bottom of the above second through hole so that the channel region of the above source select transistor is exposed;

a step of forming a channel region of a memory cell on the inner wall of the above second through hole;

a step of forming a well of a cell transistor by filling the above second through hole; and

a step of forming a drain select transistor on the above cell transistor.

Claim 9

In Claim 8,

A method for manufacturing a flash memory device, characterized in that the step of forming a well in a source region of a region exposed by a first through hole, includes

a step of opening the region where the well of the source select transistor will be formed, and

a step of doping the opened region with the conductivity type opposite to the above source region.

Claim 10

In Claim 9,

A method for manufacturing a flash memory device, characterized by

a step of doping the open region with a conductivity type opposite to that of the source region comprises injecting a dopant of the conductivity type opposite to that of the source region into the open region,

or over-etching the substrate of the open region.

Claim 11

In Claim 8,

A method for manufacturing a flash memory device, characterized in that the step of forming a well of the above source select transistor includes

a step of depositing a silicon film of a first conductivity type or depositing an un-doped silicon film and then doping it by injecting a dopant of the first conductivity type.

Claim 12

In Claim 8,

A method for manufacturing a flash memory device, characterized by

a step of forming a tunneling layer on the inner wall of the above second through hole performed by depositing a silicon compound in an atmosphere containing oxygen or oxygen and nitrogen.

Claim 13

In Claim 12,

A method for manufacturing a flash memory device, characterized in that, after the above step of forming the tunneling layer,

it further includes a step of heat treatment in an NO or N2O atmosphere.

Claim 14

In Claim 8,

A method for manufacturing a flash memory device, characterized in that after a step of forming a charge storage region on the inner wall of the above second through hole,

the method further includes the step of forming a protective film on the inner wall of the above second through hole in which the above charge storage region is formed.

Claim 15

In Claim 14,

A method for manufacturing a flash memory device, characterized in that the above protective film is formed of a polysilicon film or a nitride film.

Claim 16

In Claim 8,

A method for manufacturing a flash memory device, characterized in that the step of forming a well of the above cell transistor includes

a step of depositing a silicon film of a first conductivity type or depositing an un-doped silicon film and then doping it by injecting a dopant of the first conductivity type.

Specifications

Detailed Description of the Invention

Technology Field

[0001] The present invention relates to a method for manufacturing a flash memory device, and more particularly, to a method for manufacturing a flash memory device having a three-dimensional structure.

Background Technology

[0002] In general, semiconductor memory devices used to store data can be distinguished into volatile memory devices and non-volatile memory devices. Volatile memory devices lose stored data when power is cut off, but non-volatile memory devices retain stored data even when power is cut off. Therefore, non-volatile memory devices are widely used in situations in which power is not always available or is frequently interrupted, or where low power usage is required, such as in mobile phone systems, memory cards for storing music and/or video data, and other applications. A representative example of this type of non-volatile memory device is a flash memory device that can be erased in bulk.

[0003] As electronic devices become smaller and lighter, the demand for smaller cells in flash memory devices is also increasing. However, in the current two-dimensional cell structure in which memory cells are formed in a single layer on a semiconductor substrate, the integration level of memory cells is determined by the limitations of patterning technology and packaging technology. To overcome the limitations of this packaging technology, the line width size of the devices has been continuously reduced to increase the integration density of memory devices. However, as patterning technology reaches certain limits, the integration of memory devices is limited, and the market demands continuous increases in integration, making it difficult to meet these demands with the current two-dimensional cell structure.

[0004] To improve the shortcomings of these two-dimensional structures, a three-dimensional cell structure has been proposed. The three-dimensional cell structure is largely divided into a structure that equally layers a two-dimensional structure on top, and a structure that forms a channel in a vertical direction with respect to the silicon substrate, which is different from the existing concept. However, in the case of a structure that equally stacks the same two-dimensional structure as the current one on top, there is a limit to the increase in integration, and in the case of a method of forming a channel in a vertical direction with the silicon substrate, the cell structure is formed as a depletion transistor structure and a well is not formed, so as the erasure operation is performed using a hole injection method based on hot hole formation rather than the conventional Fowler-Nordheim tunneling (F-N tunneling), there is a disadvantage in that it is difficult to implement above a certain level of integration.

Details of the Invention

Tasks to Be Solved

[0005] A technical task to be achieved by the present invention is to provide a method for manufacturing a flash memory device having a structure capable of increasing the integration density of memory cells without being limited by the substrate area by implementing memory cells in a vertical direction with respect to a semiconductor substrate.

[0006] Another technical task that the present invention seeks to achieve is to provide a method for manufacturing a flash memory device having a structure in which memory cells arranged vertically on a substrate can be erased by using the F-N tunneling method that simultaneously erases the entire string, rather than the hot hole injection method.

Solutions to the Tasks

[0007] In order to fulfill the above technical tasks, a method for manufacturing a flash memory device according to the present invention is characterized by including a step of forming a source region on a substrate, a step of forming a source select transistor connected to the source region on the substrate, a step of forming gates of a plurality of memory cells by alternately forming insulating layers and conductive layers multiple times on a substrate on which a source select transistor is formed, a step of

forming a through hole by etching the insulating layer and the conductive layer to expose the channel region of the source select transistor, a step of forming a charge storage region consisting of a tunneling layer, a charge trap layer, and a blocking layer on the inner wall of the through hole, a step of forming a protective film on the inner sidewall of a through hole in which a charge storage region is formed, a step of exposing a channel region of a source select transistor, a step of forming a channel region of a cell transistor by filling the through hole with a semiconductor layer, and a step of forming a drain select transistor on the cell transistor.

[0008] The steps of forming the above source select transistor can consist of a step of sequentially stacking an insulating layer and a conductive layer on the above substrate, a step of etching the insulating layer and the conductive layer to form a through hole exposing the above source region, a step of forming a gate insulating film on the inner wall of the above through hole, a step of etching the above gate insulating film so that the above source region is exposed, and a step of forming a channel region of a source select transistor by filling the above through hole with a semiconductor layer.

[0009] The above protective film can be formed of a polysilicon film or a nitride film.

[0010] Before filling the above through hole with a semiconductor layer, the above protective film can be removed.

[0011] The above conductive layer for forming the gate of the above memory cell can be formed of polysilicon or metal.

[0012] In the step of forming the above tunneling layer, a silicon compound can be deposited in an atmosphere containing oxygen or oxygen and nitrogen.

[0013] After the step of forming the above tunneling layer, a step of heat treatment in an NO or N2O atmosphere may be further included.

[0014] To achieve the above technical tasks, another method for manufacturing a flash memory device according to the present invention is characterized by including a step of forming a source region on a substrate, a step of forming an insulating film and a conductive layer on the substrate, a step of forming a first through hole exposing the source region, a step of sequentially forming a gate insulating film and a channel region of a source select transistor on the sidewall of the first through hole, a step of forming a well in the source region of the region exposed by the first through hole, a step of forming a well of a source select transistor by filling the first through hole, a step of forming gates of a plurality of memory cells by alternately forming an insulating layer and a conductive layer on a substrate on which a well of a source select transistor is formed, a step of forming a second through hole exposing a channel region of a source select transistor by etching the insulating layer and the conductive layer, a step of forming a charge storage region consisting of a tunneling layer, a charge trap layer, and a blocking layer on the inner wall of the second through hole, a step of etching the charge storage region on the bottom of the second through hole so that the channel region of the source select transistor is exposed, a step of forming a channel region of a memory cell on the inner wall of a second through hole, a step of forming a well of a cell transistor by filling the second through hole, and a step of forming a drain select transistor on the cell transistor.

[0015] The step of forming a well in the source region of the region exposed by the first through hole may include the step of opening a region in which a well of the source select transistor is to be formed, and the step of doping the opened region with a conductivity type opposite to that of the above source region.

[0016] In the step of doping the above open region with a conductivity type opposite to that of the source region, the above open region may be injected with a dopant having a conductivity type opposite to that of the source region, or the substrate of the open region may be over-etched.

[0017] The step of forming a well of the above source select transistor may include a step of depositing a silicon film of a first conductivity type or a step of depositing an un-doped silicon film and then doping it by injecting a dopant of the first conductivity type.

[0018] The step of forming a tunneling layer on the inner wall of the second through hole above can deposit a silicon compound in an atmosphere containing oxygen or oxygen and nitrogen. After the step of forming the above tunneling layer, a step of heat treatment in an NO or N2O atmosphere may be further included.

[0019] After the step of forming a charge storage region on the inner wall of the above second through hole, the step of forming a protective film on the inner wall of the above second through hole in which the above charge storage region is formed may be further included.

[0020] The above protective film can be formed of a polysilicon film or a nitride film.

[0021] The step of forming a well of the above cell transistor may include a step of depositing a silicon film of a first conductivity type or a step of depositing an un-doped silicon film and then doping it by injecting a dopant of the first conductivity type.

Effects

[0022] According to the present invention, the integration density of a flash memory device can be increased by arranging memory cells in a vertical direction from a semiconductor substrate. Additionally, by forming wells in vertically arranged memory cells, data in the memory cells can be simultaneously erased using the F-N tunneling method.

Specific Details for the Implementation of the Invention

[0023] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the attached figures. However, the embodiments of the present invention may be modified in several different forms, and the scope of the present

invention should not be construed as being limited by the embodiments described below.

[0024] Figure 1 is a three-dimensional diagram illustrating a flash memory device having a three-dimensional structure according to one embodiment of the present invention.

[0025] Referring to Figure 1, a flash memory device having a three-dimensional structure according to one embodiment of the present invention includes a source select transistor formed on a substrate (100), gate stacks (220) formed on the above source select transistor and repeatedly stacked to be separated by an insulating layer (210), a charge storage region (240) formed by a blocking layer, a charge trap layer, and a tunneling layer formed on a sidewall of a through hole penetrating the above gate stacks, memory cells formed by a channel region (260) formed to fill the above through hole, and a drain select transistor formed to be connected to the above memory cells.

[0026] A source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string, and a plurality of such cell strings are arranged on the substrate (100).

[0027] The source select transistor consists of a gate conductive layer (130) formed on a substrate (100) to be separated by insulating layers (120, 140), a gate insulating layer (160) formed on the inner wall of a through hole penetrating the above gate conductive layer (130) and the insulating layers (120, 140), and a channel region (170) formed to fill the through hole in which the above gate insulating layer is formed. The channel region is connected to a source (110) formed on the substrate (100). The above channel region (170) is formed of a silicon epitaxial layer, or has a structure in which a silicon epitaxial layer and a polysilicon film are sequentially stacked from the sidewall of the gate insulating layer within the above through hole.

[0028] The gate stack (220) constituting the above memory cell is repeatedly stacked as many times as the number of memory cells connected to one cell string. The memory cells connected to one cell string are separated by an insulating layer (210), and the memory cells arranged in the same layer constitute one page.

[0029] The drain select transistor consists of the same structure as the source select transistor, and the channel region (310) is connected to the channel region (260) of the memory cell.

[0030] Figures 2 to 11 are cross-sectional views illustrating a method for manufacturing a three-dimensional flash memory device according to one embodiment of the present invention. The same reference numbers as in Figure 1 indicate the same parts.

[0031] Referring to Figure 2, an impurity layer (110) is formed on a substrate (100) to form a common source of cells. The above substrate (100) may be a single crystal silicon (Si) substrate doped with P-type impurities. The above impurity layer (110) can be formed by ion-implanting impurities of the conductivity type opposite to that of the semiconductor substrate (100), for example, N type. Next, in order to limit the common source region, the impurity layer (110) and the semiconductor substrate (100) in the regions other than the source are etched using a photolithography process. An insulating film (120) is deposited on the resulting layer to separate the impurity layer from other conductive layers.

[0032] Referring to Figure 3, a conductive layer (130) for forming a gate of a select transistor is sequentially formed on a substrate on which an insulating film (120) is formed, and an insulating layer (140) for separating the conductive layer above and the conductive layer formed thereon is sequentially formed. The above conductive layer (130) can be formed with a thickness of 10 to 1,000 Å using a polysilicon film doped with impurities, a metal such as tungsten (W), or another conductive material.

[0033] Next, the above conductive layer (130) and the insulating layer (140) in the region where the channel of the source select transistor is to be formed are etched to form a hole (150) that exposes the impurity layer (110) formed on the above substrate (100). The above hole (150) is a region in which a channel of a source select transistor is formed, and is formed to have a diameter of 10 to 1,000 Å. The etching process for forming a hole (150) can be performed using wet etching, dry etching, or a mixed method thereof.

[0034] Referring to Figure 4, a silicon oxide film is deposited on the side of the above hole to a thickness of, for example, 10 to 500 Å to form a gate insulating film (160) of a source select transistor. When forming the above gate insulating film (160), oxidation can be performed in an atmosphere containing both oxygen and nitrogen so that an oxygen nitride film (SiON) is formed. In addition, the film quality of the gate insulating film can be improved by performing heat treatment in an NO gas or N2O gas atmosphere after forming the gate insulating film (160).

[0035] Next, the interior of the hole where the gate insulating film (160) is formed is filled with a semiconductor layer such as single crystal silicon (Si). The above semiconductor layer can be formed by using, for example, a selective epitaxial growth (SEG) method, such that a silicon (Si) film is selectively grown from the above impurity layer (110) in a gas atmosphere containing silicon (Si), and becomes a channel region (170) of the select transistor. Like this, a source select transistor is formed, which consists of a channel region (170), a gate insulating film (160), and a conductive layer (130) as a gate electrode.

[0036] Referring to Figure 5, on the resulting structure in which the source select transistor is formed, an interlayer insulating film (210) and a conductive layer (220) are repeatedly deposited several times. The interlayer insulating film (210) is used to separate vertically-stacked memory cells, and can be formed of a silicon oxide film, a silicon nitride film, or a laminated film of a silicon oxide film and a silicon nitride film. The above conductive layer (220) can be formed by depositing, for example, a polysilicon film or a polysilicon germanium film doped with a P-type impurity, a metal film, or another conductive material to a thickness of 10 to 1,000 Å. The above conductive layer (220) can be repeatedly stacked as many times as the number of memory cells connected to one cell string, for example, 2 times, 4 times, 8 times, ... up to 1,000 times. The above conductive layer (220) serves as a control gate of the memory cell, and the interlayer insulating film (210) serves to separate the vertically-stacked memory cells.

[0037] Referring to Figure 6, after stacking the conductive layers (220) and interlayer insulating films (210) as many times as the number of memory cells connected to the cell string, a through hole (230) is formed to form an ONO film for the channel of the cell transistor and charge storage. Specifically, the alternately-stacked conductive layers (210) and interlayer insulating films

(220) are anisotropically etched so that the gate insulating film (160) and channel region (170) of the source select transistor are exposed. At this time, the etching process can use a wet or dry etching method, and the size of the through hole (230) is formed to a size that can be gap-filled with a semiconductor layer that acts as a channel of the cell transistor and an ONO film that acts as a charge storage film. In this embodiment, the above through hole (230) was formed with a diameter of 10 to 1,000 Å.

[0038] Referring to Figure 7, an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (230).

[0039] Specifically, a blocking layer is formed on the inner wall of the through hole (230) to prevent the movement of charges from the charge trap layer (not shown) to the control gate electrode. The blocking layer can be formed by depositing an oxide film using a chemical vapor deposition (CVD) method, or can be formed of a high-k material such as aluminum oxide (Al2O3), hafnium oxide (HfO2), zirconium oxide (ZrO2), hafnium aluminum oxide (HfAlO), or hafnium silicon oxide (HfSiO). After forming the blocking layer, a rapid thermal annealing process can be performed on the semiconductor substrate on which the blocking layer has been formed.

[0040] Next, a charge trap layer is formed by depositing, for example, a silicon nitride film or a polysilicon film to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (230). The charge trap layer can be deposited using atomic layer deposition (ALD) or chemical vapor deposition (CVD). An oxide film is deposited on the charge trap layer on the inner wall of the through hole (230) to a thickness of 10 to 1,000 Å to form a tunneling layer of the memory cell. When forming the above tunneling layer, it is possible to form an oxygen nitride film (SiON) by performing the process in an atmosphere containing both oxygen and nitrogen. In addition, the film quality of the tunneling layer can be improved by heat-treating in an NO gas or N2O gas atmosphere after forming the tunneling layer.

[0041] Referring to Figure 8, a protective film (250) is formed on the tunneling layer formed on the inner wall of the through hole to protect the ONO dielectric layer (240) during the process of etching the subsequent ONO dielectric layer. The above protective film (250) can be formed of a conductive film such as a doped polysilicon film or an insulating film such as a nitride film, and is formed to a thickness of 10 to 1,000 Å. When the protective film (250) is formed as a conductive film such as a doped polysilicon film, it can be used as a part of a channel region or a channel region of a memory cell.

[0042] In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, charge trap layer, and blocking layer at the bottom of the through hole are etched to expose the channel region (170) of the source select transistor. As a protective film (250) having an etching selectivity with respect to the above dielectric layer is formed on the side of the ONO dielectric layer (240), etching or etching damage to the dielectric layer does not occur during the etching process for the dielectric layer.

[0043] Referring to Figure 9, a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of the cell transistor. The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities. The protective film formed on the side wall of the ONO dielectric layer may be removed before forming the above channel region. In this embodiment, a channel region is formed after removing the protective film. On the other hand, when the protective film on the above ONO dielectric layer (240) is formed as a conductive film such as a doped polysilicon film and used as a channel of a memory cell, the above through hole where the protective film is formed may be filled with an insulating film such as an oxide film or a nitride film. In this way, a plurality of memory cells separated from the substrate (100) by a source select transistor and an insulating layer (140, 210) are formed.

[0044] Referring to Figure 10, a drain select transistor for string selection is formed on the resulting material in which a plurality of memory cells are formed.

[0045] Specifically, an insulating film (270) is formed on the resulting material in which a through hole is filled to form a channel region of a memory cell to separate the drain select transistor and the uppermost memory cell. A doped polysilicon film, metal film, or other conductive material film is formed on an insulating film (270) to a thickness of 10 to 1,000 Å to form a conductive layer (280) for forming a gate of a drain select transistor. Next, an insulating film (290) is formed to separate the gate conductive layer (280) of the drain select transistor from the upper conductive layer.

[0046] Next, in order to connect the drain select transistor and the memory cell transistor, the conductive layer (280) and the insulating film (270, 290) are anisotropically etched to form a hole. The etching process for forming the above hole can be performed using wet etching, dry etching, or a mixed method thereof. The above hole is formed with a diameter of 10 to 1,000 Å, and is formed so that the ONO dielectric layer and the channel region (260) of the memory cell are exposed, as shown.

[0047] Referring to Figure 11, a gate insulating film (300) of a drain select transistor is formed by depositing, for example, a silicon oxide film to a thickness of 10 to 500 Å on the inner wall of the above hole formed so as to expose the ONO dielectric layer (240) and the channel region (260) of the memory cell. When forming the gate insulating film (300) of the above drain select transistor, it is possible to form an oxygen nitride film (SiON) by performing the process in an atmosphere containing both oxygen and nitrogen. In addition, the film quality of the above gate insulating film can be improved by performing heat treatment in an NO gas or N2O gas atmosphere after forming the gate insulating film (300).

[0048] Next, in order to connect the channel region of the memory cell and the channel region of the drain select transistor, the gate insulating film (300) at the bottom of the hole is etched so that the channel region of the memory cell is exposed. Before etching the above gate insulating film (300), a protective film made of a conductive film such as a polysilicon film can be formed on the gate insulating film (300) formed on the inner wall of the hole, and then etching can be performed to protect the gate insulating film (300) on the side wall of the hole. In this case, the conductive film used as the above protective film can be used as a part of a channel region or the channel region of the drain select transistor.

[0049] A semiconductor layer is formed on the resulting material in which the channel region of the memory cell is exposed so that the

above hole is filled, thereby forming a channel region (310) of the drain select transistor. The semiconductor layer may be formed by using, for example, a selective epitaxial growth (SEG) method, such that a silicon (Si) film is grown from the channel region of the memory cell in a gas atmosphere containing silicon (Si). On the other hand, when the protective film on the gate insulating film is formed as a conductive film such as a doped polysilicon film and used as a channel of the memory cell, the contact hole can also be filled with an insulating film such as an oxide film or a nitride film. Next, an etching process is performed to separate the drain select transistors.

[0050] According to one embodiment of the present invention, by vertically stacking memory cells from a semiconductor substrate, the integration density of memory elements can be dramatically increased regardless of the area of the substrate and patterning limitations. In addition, by forming a protective film after forming the ONO dielectric layer, which is the charge storage area of the memory cell, in the process of etching an ONO dielectric layer to connect the channel region of a memory cell and the channel region of a source select transistor, etching or etching damage to the ONO dielectric layer can be prevented, thereby preventing deterioration of the characteristics of a flash device.

[0051] Figures 12 and 13 are three-dimensional diagrams illustrating a flash memory device having a three-dimensional structure according to another embodiment of the present invention.

[0052] Referring to Figures 12 and 13, a three-dimensionally structured flash memory device according to another embodiment of the present invention includes a source select transistor formed on a substrate (300), gate stacks (420) formed on the above source select transistor and repeatedly stacked to be separated by an insulating layer (410), a charge storage region (440) composed of a blocking layer, a charge trap layer, and a tunneling layer formed on the sidewall of a through hole penetrating the above gate stacks, a channel region (460) formed on the charge storage region (440) within the above through hole, memory cells formed to fill a through hole in which the above channel region is formed and formed with a well region (470) of the conductivity type opposite to the above channel region, and a drain select transistor formed to be connected to the above memory cell.

[0053] As in the case of the first embodiment illustrated in Figure 1, a source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (300) to form a cell string, and the memory cells arranged on the same layer form one page. The source select transistor consists of a gate conductive layer (330) formed on the above substrate (300) so as to be separated by an insulating layer (320, 340), a gate insulating layer (360) formed on the inner wall of a through hole penetrating the above gate conductive layer (330) and the insulating layer (320, 340), a channel region (370) formed on the side wall of the above gate insulating layer, and a well region (380) formed to fill the above through hole where the channel region is formed. The channel region of the source select transistor is connected to the source (310) formed on the substrate (300), and is formed of a silicon epitaxial layer, or has a structure in which a silicon epitaxial layer and a polysilicon film are sequentially stacked from the sidewall of the gate insulating layer within the above through hole.

[0054] The gate stack (420) constituting the above memory cell is repeatedly stacked as many times as the number of memory cells connected to one cell string. Memory cells connected to one cell string are separated by an insulating layer (410). Inside the channel region of the source select transistor and inside the channel region of the memory cell, a well region (380, 470) doped with a dopant of the conductivity type opposite to the above channel region, for example, a P-type dopant, is arranged. The well region (380, 470) is for simultaneously removing charges trapped in the charge trap layer of the memory cell. In the case of conventional charge trap type flash devices, data cannot be erased by F-N tunneling, so data is erased using hot electron injection (HEI), which has the disadvantage of slow erase speed. However, in the case of the present invention, by simultaneously removing charges stored in the charge trap layer of the memory cell to the well region (470) and injecting them into the well region (380) of the source select transistor, temporary erasing, which is an advantage of the flash memory device, becomes possible.

[0055] In the case of a drain select transistor, as it is necessary to perform the function of selecting a string, it may have a well region (530) as shown in Figure 13, or it may not have a well region as shown in Figure 12.

[0056] Figures 14 to 20 are cross-sectional views illustrating a method for manufacturing a three-dimensional flash memory device according to another embodiment of the present invention.

[0057] Referring to Figure 14, an impurity layer (310) is formed on a substrate (300) to form a common source of cells. The above substrate (300) may be a single crystal silicon (Si) substrate doped with P-type impurities. The above impurity layer (310) can be formed by ion-implanting impurities of the conductivity type opposite to that of the substrate (100), for example, N-type. Next, in order to limit the common source region, the impurity layer (310) and the substrate (300) in the regions other than the source are etched using a photolithography process. An insulating film (320) is deposited on the resulting material to separate the source region from other conductive layers.

[0058] A conductive layer (330) for forming a gate of a select transistor is sequentially formed on a substrate on which an insulating film (320) is formed, and an insulating layer (340) for separating the conductive layer above and the conductive layer formed thereon is sequentially formed. The above conductive layer (330) can be formed with a thickness of 10 to 1,000 Å using a polysilicon film doped with impurities, a metal such as tungsten (W), or another conductive material.

[0059] Next, the above conductive layer (330) and the insulating layer (340) in the region where the channel of the source select transistor is to be formed are etched to form a hole (350) that exposes the impurity layer (310) of the substrate. The above hole (350) is a region in which a channel of a source select transistor is formed, and is formed to have a diameter of 10 to 1,000 Å. The etching process for forming a hole (350) can be performed using wet etching, dry etching, or a mixed method thereof.

[0060] Referring to Figure 15, a silicon oxide film is deposited on the side of the above hole to a thickness of, for example, 10 to 500 Å to form a gate insulating film (360) of a source select transistor. When forming the above gate insulating film (360), oxidation can be performed in an atmosphere containing both oxygen and nitrogen so that an oxygen nitride film (SiON) is formed. In addition, the film quality of the gate insulating film can be improved by performing heat treatment in an NO gas or N2O gas atmosphere after forming the gate insulating film (360).

[0061] Next, a semiconductor layer such as single crystal silicon (Si) is formed on the side of the hole where the gate insulating film (360) is formed to form a channel of the source select transistor. The above semiconductor layer is formed of a silicon layer doped with a conductivity type opposite to that of the substrate (300), for example, an N-type. The above semiconductor layer can be formed by using, for example, a selective epitaxial growth (SEG) method, such that a silicon (Si) film is grown from the above impurity layer (310) in a gas atmosphere containing silicon (Si), and becomes a channel region (370) of the select transistor. At this time, unlike the case of the first embodiment, the hole is not filled with a semiconductor layer, but a semiconductor layer is formed only on the sidewalls of the hole to form a P-well in the center of the hole.

[0062] Next, in order to connect the P-well formed in the source select transistor region and the substrate, the impurity layer (310) at the bottom of the well is doped with P type by ion implanting P-type impurities through the hole, or the impurity layer (310) exposed through the above hole is over-etched to expose the P-type substrate. Next, the center of the hole is filled with a P-type silicon layer to form a P-well (380) to connect to the P-well of the memory cell.

[0063] Referring to Figure 16, on the resulting material in which the source select transistor is formed, an interlayer insulating film (410) and a conductive layer (420) are repeatedly deposited several times. The interlayer insulating film (410) is used to separate vertically-stacked memory cells, and can be formed of a silicon oxide film, a silicon nitride film, or a stacked film of a silicon oxide film and a silicon nitride film. The above conductive layer (420) can be formed by depositing, for example, a polysilicon or a polysilicon germanium film doped with a P-type impurity, a metal film, or another conductive material to a thickness of 10 to 1,000 Å. The above conductive layer (420) can be repeatedly stacked as many times as the number of memory cells connected to one cell string. The above conductive layer (420) serves as a control gate of the memory cell, and the interlayer insulating film (410) serves to separate the vertically-stacked memory cells.

[0064] After stacking conductive layers (420) and interlayer insulating films (410) as many times as the number of memory cells connected to the cell string, a through hole (430) is formed to form an ONO film for the channel of the cell transistor and charge storage. Specifically, the alternately-stacked conductive layers (410) and interlayer insulating films (420) are anisotropically etched so that the gate insulating film (360) and channel region (370) of the source select transistor are exposed. At this time, the etching process can use a wet or dry etching method, and the size of the through hole (430) can be formed to a size that can be gap-filled with a semiconductor layer and an ONO film that will serve as a channel of the cell transistor. In this embodiment, the above through hole (430) was formed with a diameter of 10 to 1,000 Å.

[0065] Referring to Figure 17, an ONO dielectric layer (440) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (430).

[0066] Specifically, a blocking layer is formed on the inner wall of the above through hole (430) to prevent the movement of charges from the charge trap layer (not shown) to the control gate electrode. The blocking layer can be formed by depositing an oxide film using a chemical vapor deposition (CVD) method, or can be formed of a high-k material such as aluminum oxide (Al2O3), hafnium oxide (HfO2), zirconium oxide (ZrO2), hafnium aluminum oxide (HfAlO), or hafnium silicon oxide (HfSiO). After forming the blocking layer, rapid thermal annealing can be performed on the semiconductor substrate on which the blocking layer has been formed.

[0067] Next, a charge trap layer is formed by depositing, for example, a silicon nitride film or a polysilicon film to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (430). The charge trap layer can be deposited using atomic layer deposition (ALD) or chemical vapor deposition (CVD). An oxide film is deposited on the charge trap layer on the inner wall of the above through hole (430) to a thickness of 10 to 1,000 Å to form a tunneling layer of the memory cell. When forming the above tunneling layer, it is possible to form an oxygen nitride film (SiON) by performing the process in an atmosphere containing both oxygen and nitrogen. In addition, the film quality can be improved by heat-treating in an NO gas or N2O gas atmosphere after forming the tunneling layer.

[0068] A protective film (450) is formed on the tunneling layer formed on the inner wall of the through hole to protect the tunneling layer during the process of etching the subsequent ONO dielectric layer. The above protective film (450) can be formed of a conductive film such as a doped polysilicon film or an insulating film such as a nitride film, and can be formed to a thickness of 10 to 1,000 Å. When the protective film (450) is formed as a conductive film such as a doped polysilicon film, it can be used as a part of a channel region or a channel region of a memory cell.

[0069] Referring to Figure 18, in order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (450), tunneling layer, charge trap layer, and blocking layer at the bottom of the through hole are etched to expose the channel region of the source select transistor. In some cases, an etching process may be performed to expose the channel region of the source select transistor without forming the above protective film (450).

[0070] For example, a silicon film doped with N type is deposited on the resulting material to form a channel region (460) of the memory cell. The channel region (460) of the above memory cell is connected to the channel region (370) of the source select transistor. Next, in order to connect the well region of the memory cell and the well region formed in the source select transistor, the doped silicon film at the bottom of the through hole is etched to expose the well region of the source select transistor. Next, a doped silicon film is filled in the center of the through hole to form a well region (470). The above well region (470) has a conductivity type opposite to that of the channel region (460) and can be formed by depositing a silicon film doped with a P-type dopant having the same conductivity type as the substrate (300). Alternatively, a silicon film doped with the same conductivity type as the channel region (460) of the memory cell may be deposited and then formed by count-doping with P type using a doping method such as ion implantation.

[0071] Referring to Figure 19, a drain select transistor for string selection is formed. Specifically, an insulating film (480) is formed on the resulting material in which the through hole is filled to separate the drain select transistor and the memory cell. A doped polysilicon film, metal film, or other conductive material film is formed on an insulating film (480) to a thickness of 10 to 1,000 Å to form a conductive layer (490) for the gate of a drain select transistor. Next, an insulating film (500) is formed to separate the gate conductive layer (490) of the above drain select transistor from the upper conductive layer.

[0072] Next, in order to connect the drain select transistor and the memory cell transistor, the conductive layer (490) and the insulating film (480, 500) are anisotropically etched to form a hole exposing the channel region of the memory cell transistor. The etching process for forming the above hole can be performed using wet etching, dry etching, or a mixed method thereof. The above hole can be formed with a diameter of 10 to 1,000 Å.

[0073] For example, a silicon oxide film is deposited on the inner wall of the above hole to a thickness of 10 to 500 Å to form a gate insulating film (510) of the drain select transistor. When forming the gate insulating film (510) of the above drain select transistor, it is possible to form an oxygen nitride film (SiON) by performing the process in an atmosphere containing both oxygen and nitrogen. In addition, the film quality of the above gate insulating film can be improved by performing heat treatment in an NO gas or N2O gas atmosphere after forming the gate insulating film (510).

[0074] Next, in order to connect the channel region of the memory cell and the channel region of the drain select transistor, the gate insulating film (510) at the bottom of the hole is etched so that the channel region of the memory cell is exposed. Before etching the above gate insulating film (510), a protective film made of a conductive film such as a polysilicon film can be formed on the gate insulating film (510) formed on the inner wall of the hole, and then etching can be performed to protect the gate insulating film (510) on the side wall of the hole. In this case, the conductive film used as the above protective film can be used as a part of a channel region or the channel region of the drain select transistor.

[0075] A semiconductor layer is formed on the resulting material in which the channel region of the memory cell is exposed so that the above hole is filled, thereby forming a channel region (520) of the drain select transistor. The semiconductor layer may be formed by using, for example, a selective epitaxial growth (SEG) method, such that a silicon (Si) film is grown from the channel region of the memory cell in a gas atmosphere containing silicon (Si).

[0076] On the other hand, as illustrated in Figure 20, in the case of a drain select transistor, a P-well (530) can be formed in the channel region, similarly to the case of a source select transistor.

[0077] Next, an etching process is performed to separate the drain select transistors.

[0078] Although the present invention has been described in detail with reference to preferred embodiments, the present invention is not limited to the above embodiments, and it is obvious that various modifications can be made by those skilled in the art within the technical spirit of the present invention.

Brief Description of the Figures

[0079] Figure 1 is a three-dimensional diagram illustrating a flash memory device having a three-dimensional structure according to one embodiment of the present invention.

[0080] Figures 2 to 11 are cross-sectional views illustrating a method for manufacturing a three-dimensional flash memory device according to one embodiment of the present invention.

[0081] Figure 12 is a three-dimensional diagram illustrating a flash memory device having a three-dimensional structure according to another embodiment of the present invention.

[0082] Figure 14 is a three-dimensional diagram illustrating a flash memory device having a three-dimensional structure according to yet another embodiment of the present invention.

[0083] Figures 15 to 20 are cross-sectional views illustrating a method for manufacturing a three-dimensional flash memory device according to another embodiment of the present invention.

FIGURES

Figure 1

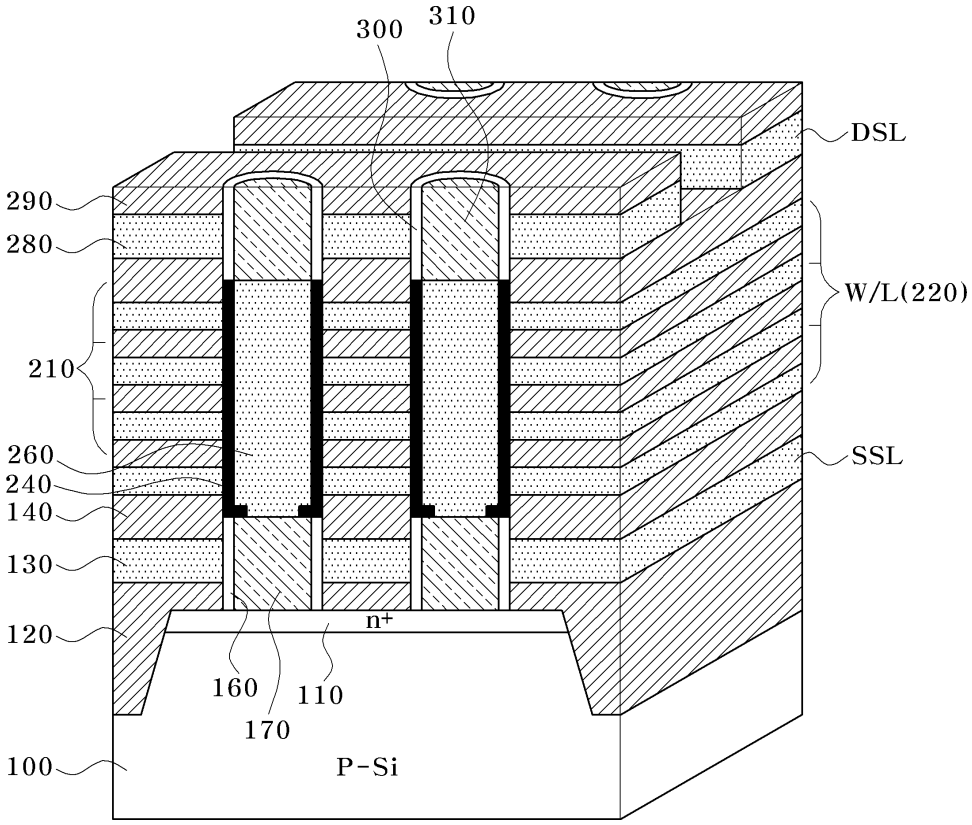


Figure 2

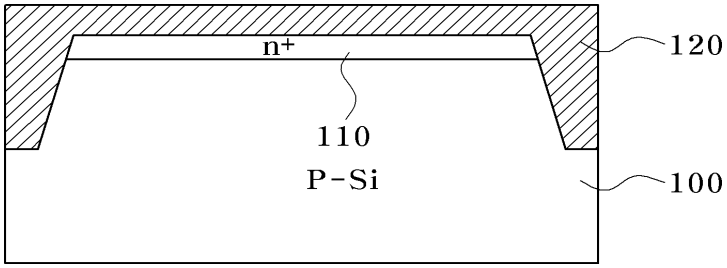
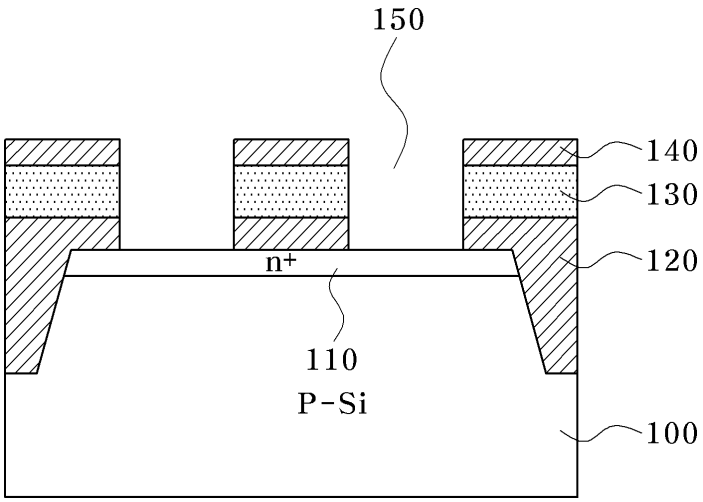


Figure 3



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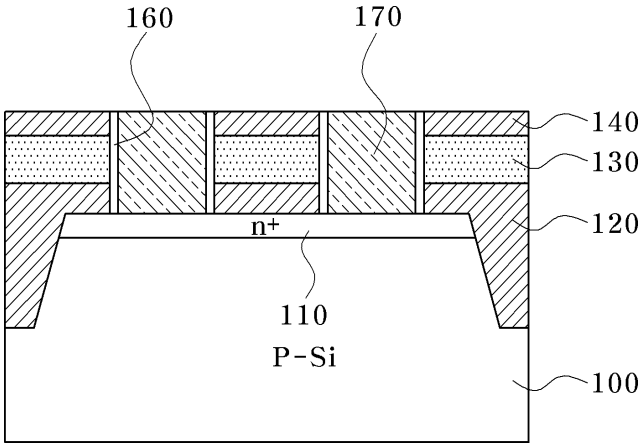
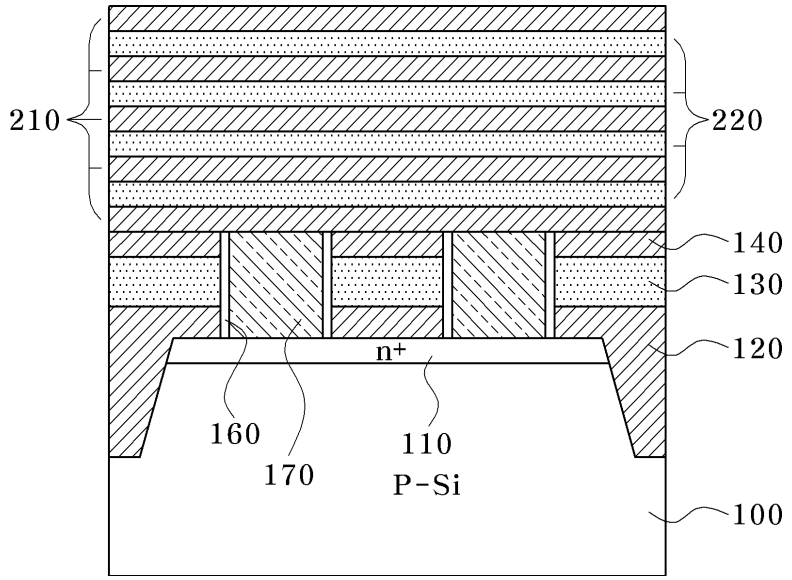


Figure 5



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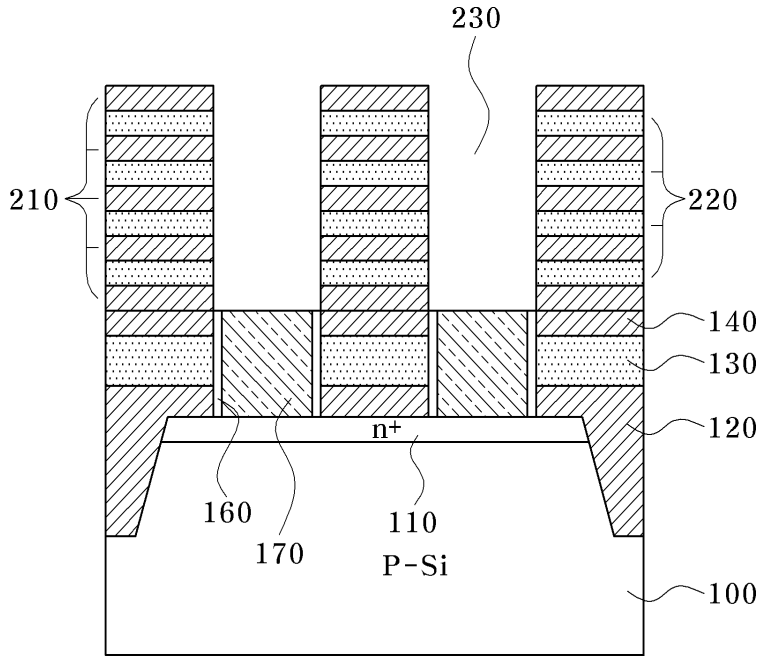


Figure 7

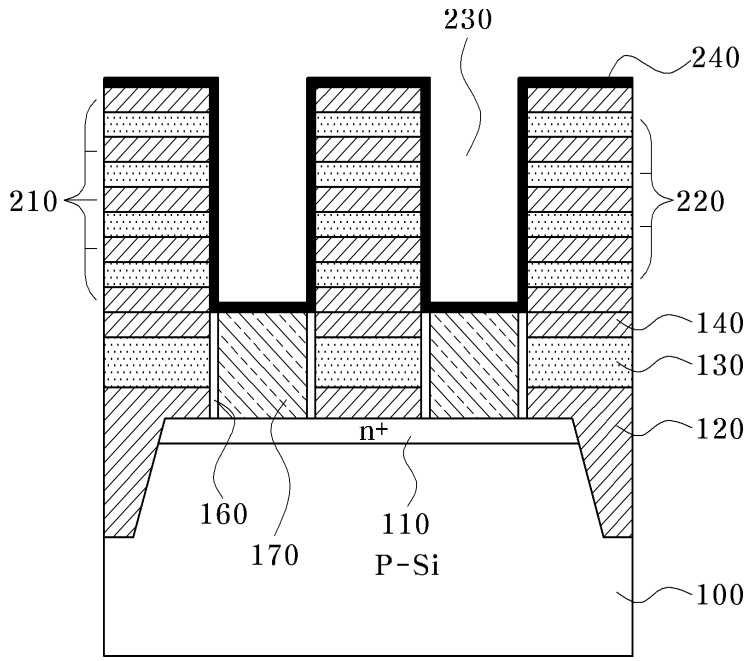


Figure 8

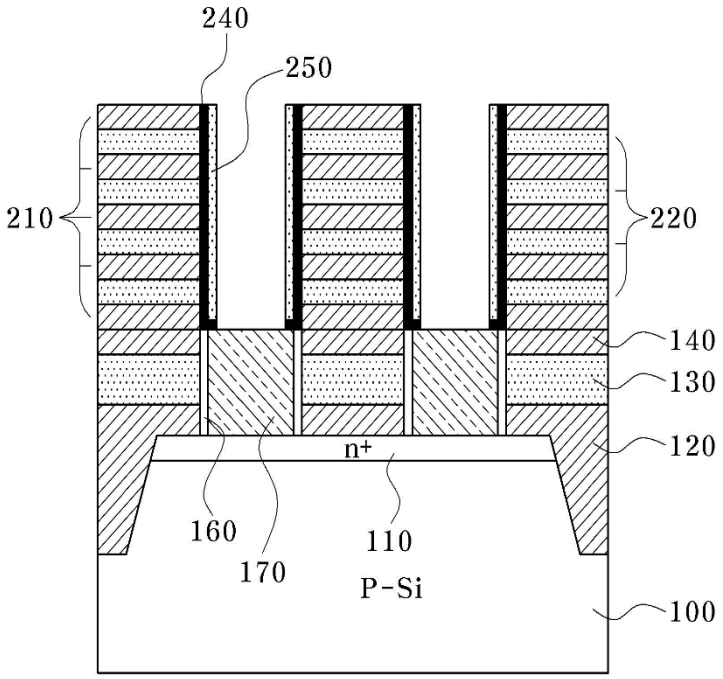


Figure 9

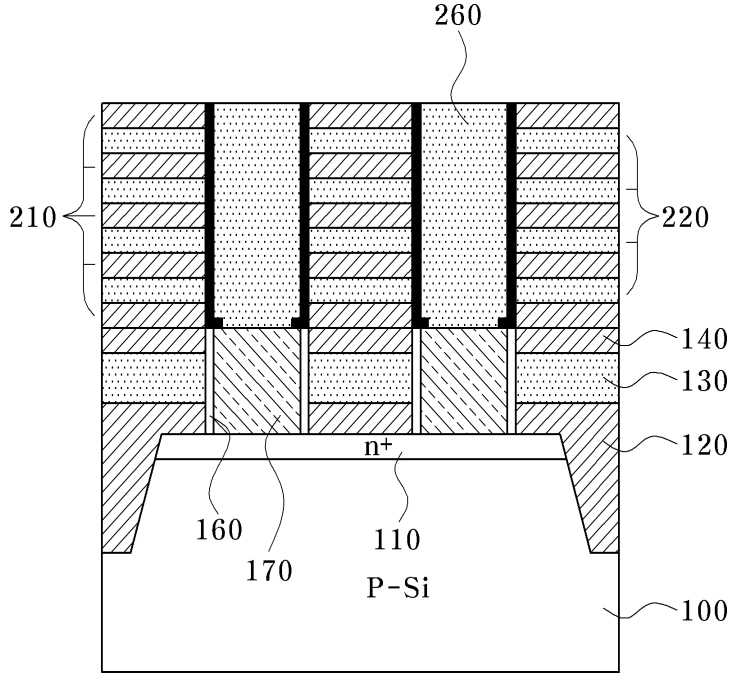
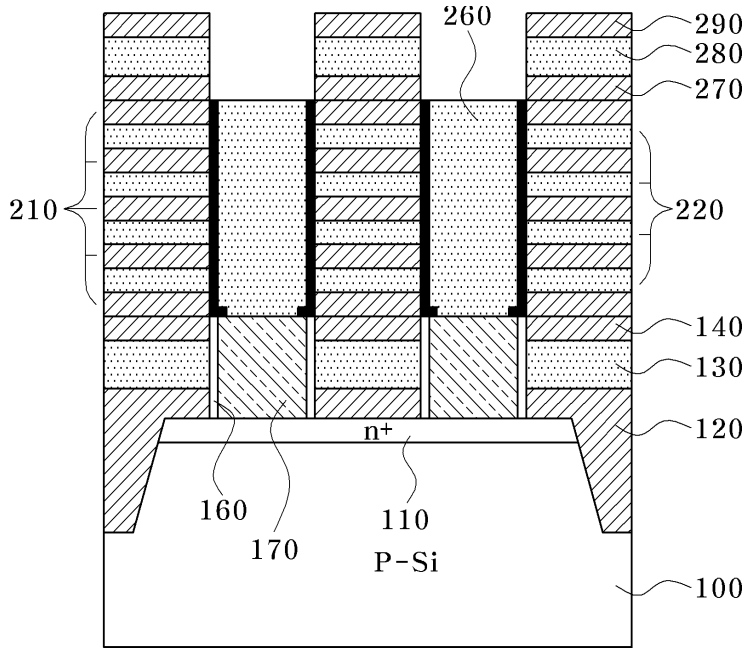


Figure 10



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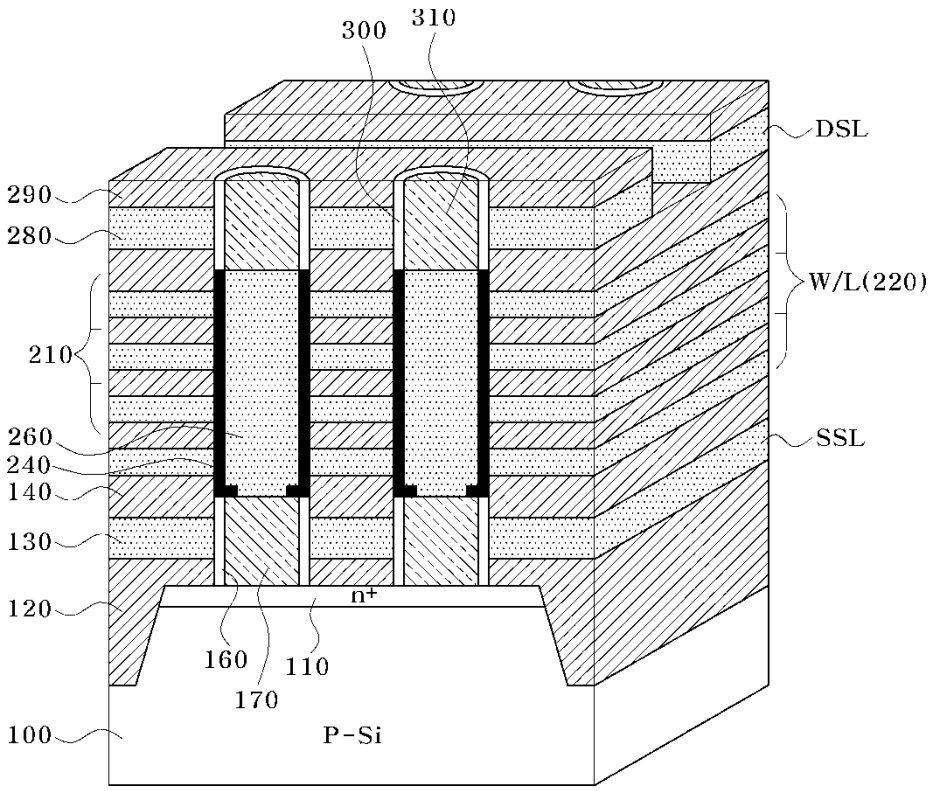
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Figure 12

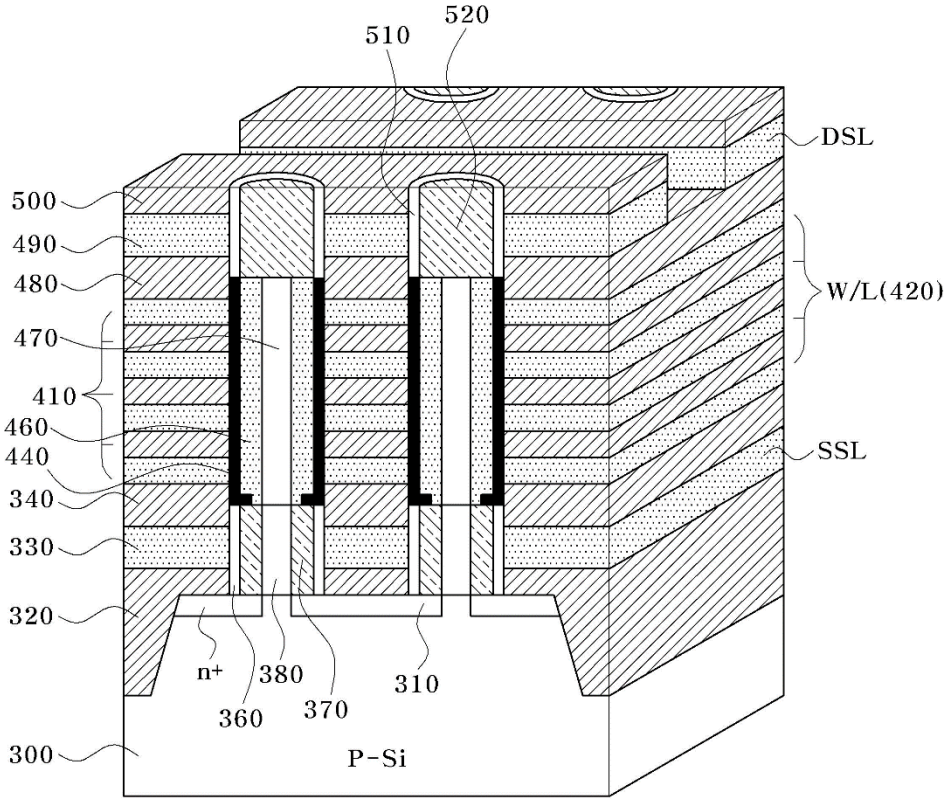
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Figure 13

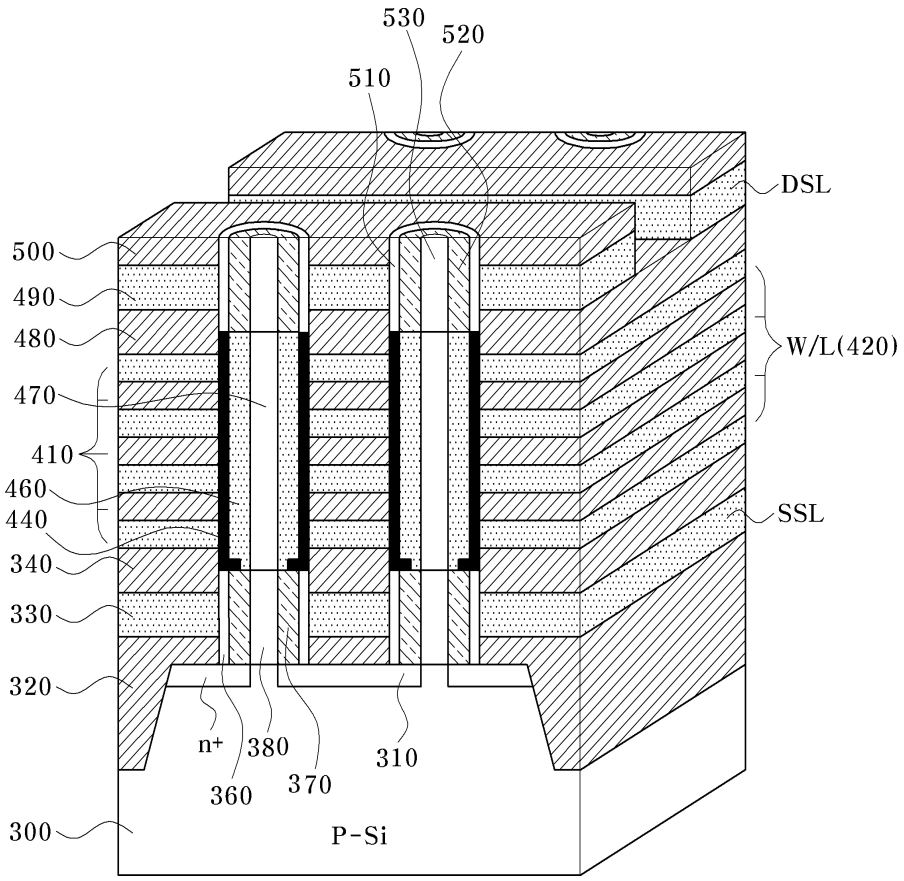

Figure 14

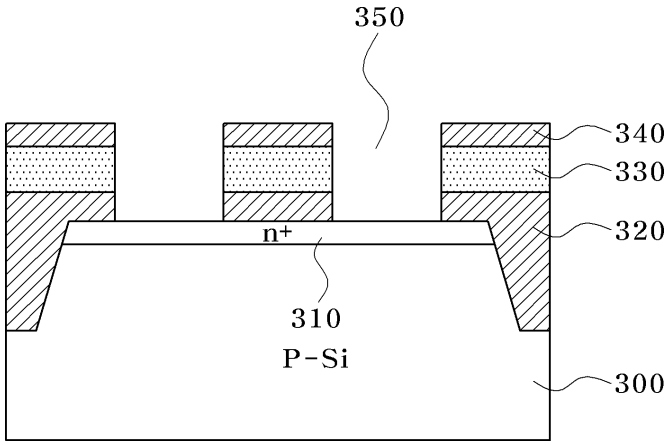

Figure 15

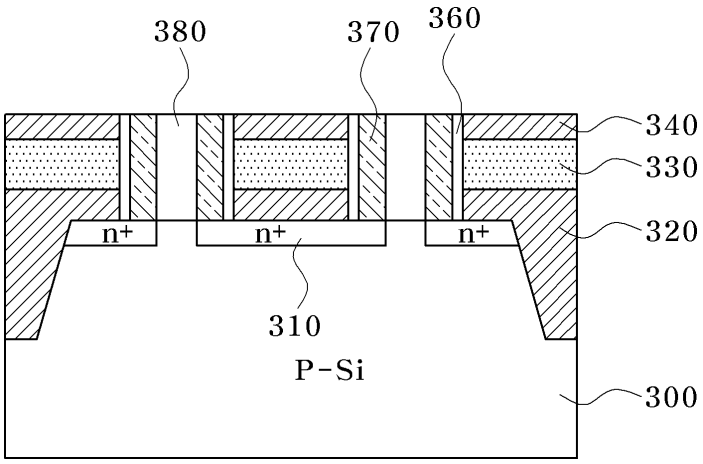

Figure 16

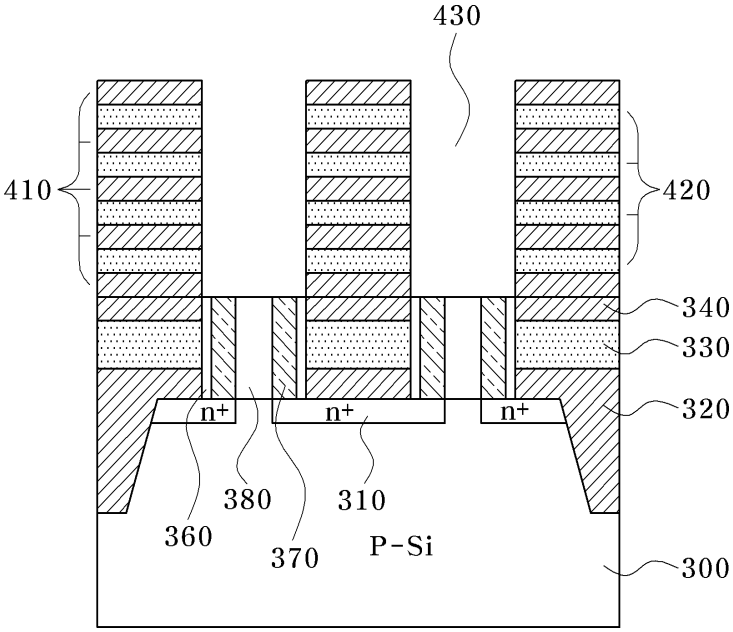

Figure 17

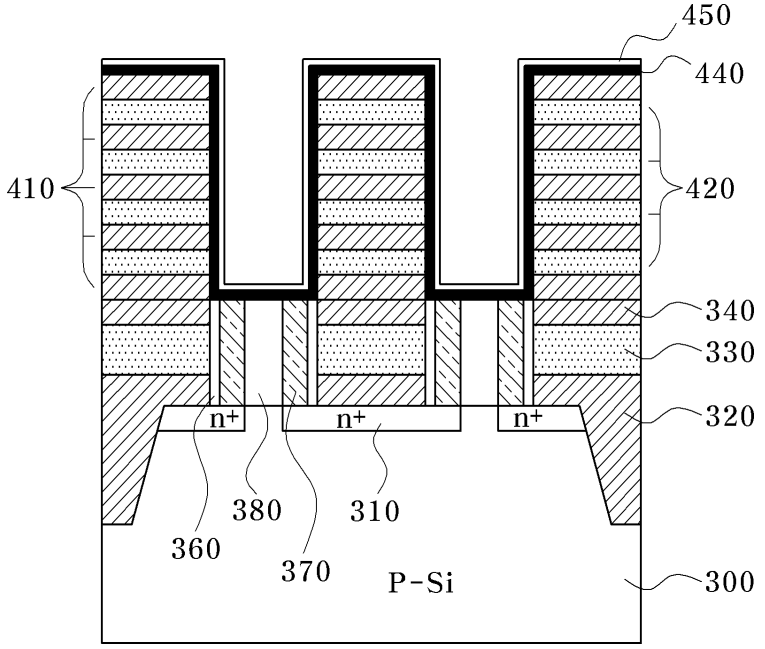

Figure 18

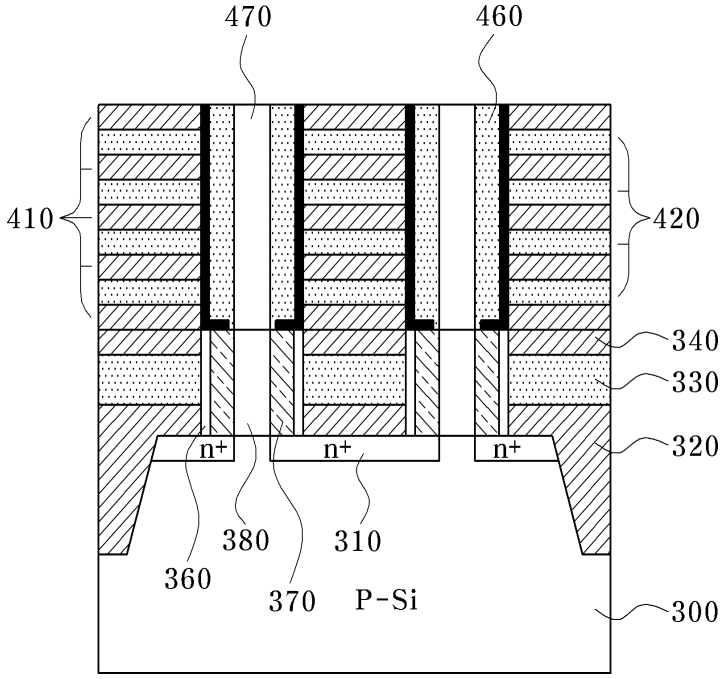

Figure 19

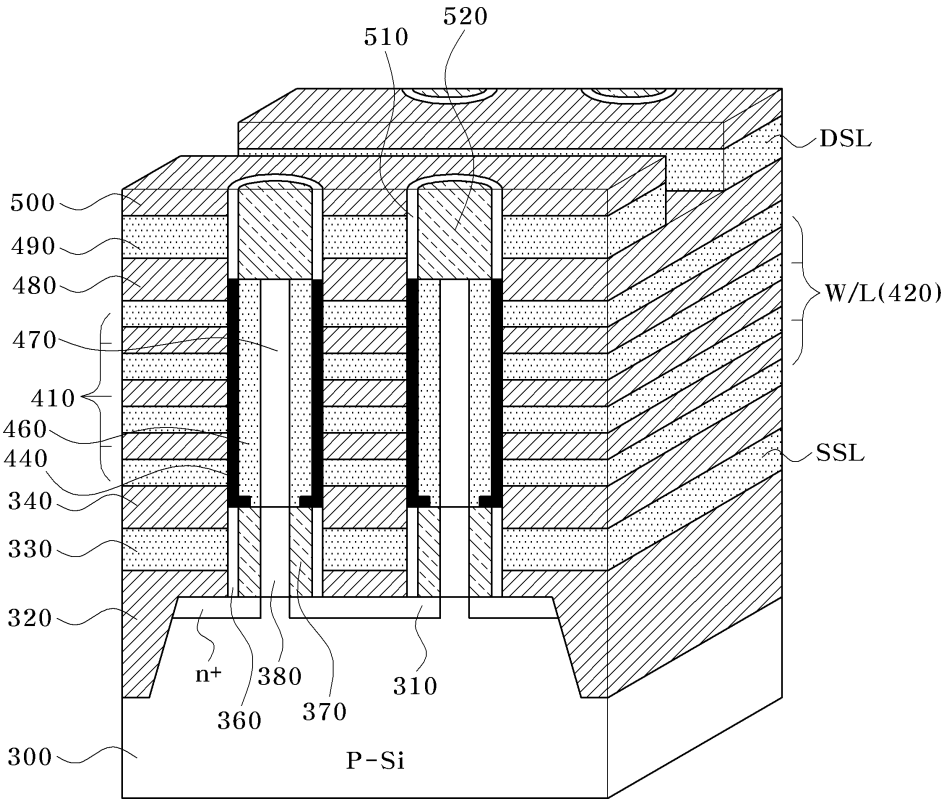
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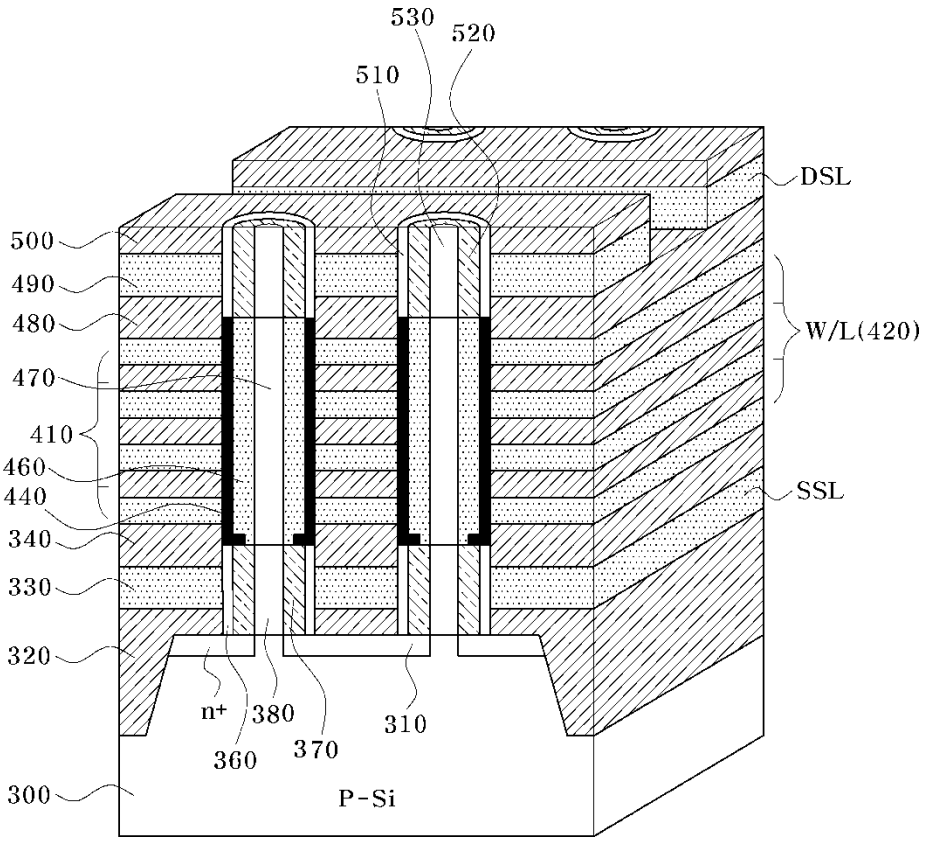
Figure 20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