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(54) SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING SEMICONDUCTOR MEMORY DEVICE

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H01L 21/8247 (2006.01)

(52) **U.S. Cl.** **257/204**; 438/128; 257/E27.103; 257/E21.692

(57) **ABSTRACT**

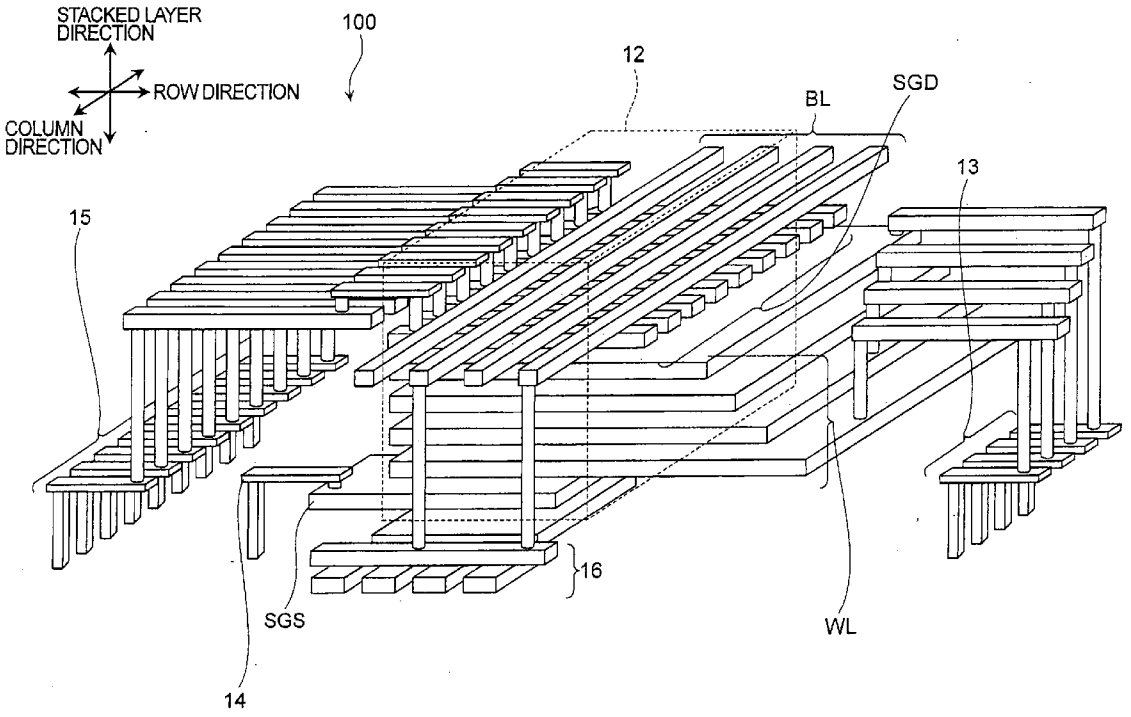
According to an aspect of the present invention, there is provided a nonvolatile semiconductor memory device, comprising a plurality of memory strings, each of the memory strings being constituted with a plurality of electrically erasable memory cells being serially connected each other, the memory strings comprising:

a columnar semiconductor layer perpendicularly extending toward a substrate;

a plurality of conductive layers being formed in parallel to the substrate and including a first space between a sidewall of the columnar semiconductor layers; and

characteristic change layer being formed on the sidewall of the columnar semiconductor layer faced to the first space or a sidewall of the conductive layer faced to the first space and changing characteristics accompanying with applied voltage;

wherein the plurality of the conductive layers have a function of a relative movement to a prescribed direction for the columnar semiconductor layer.



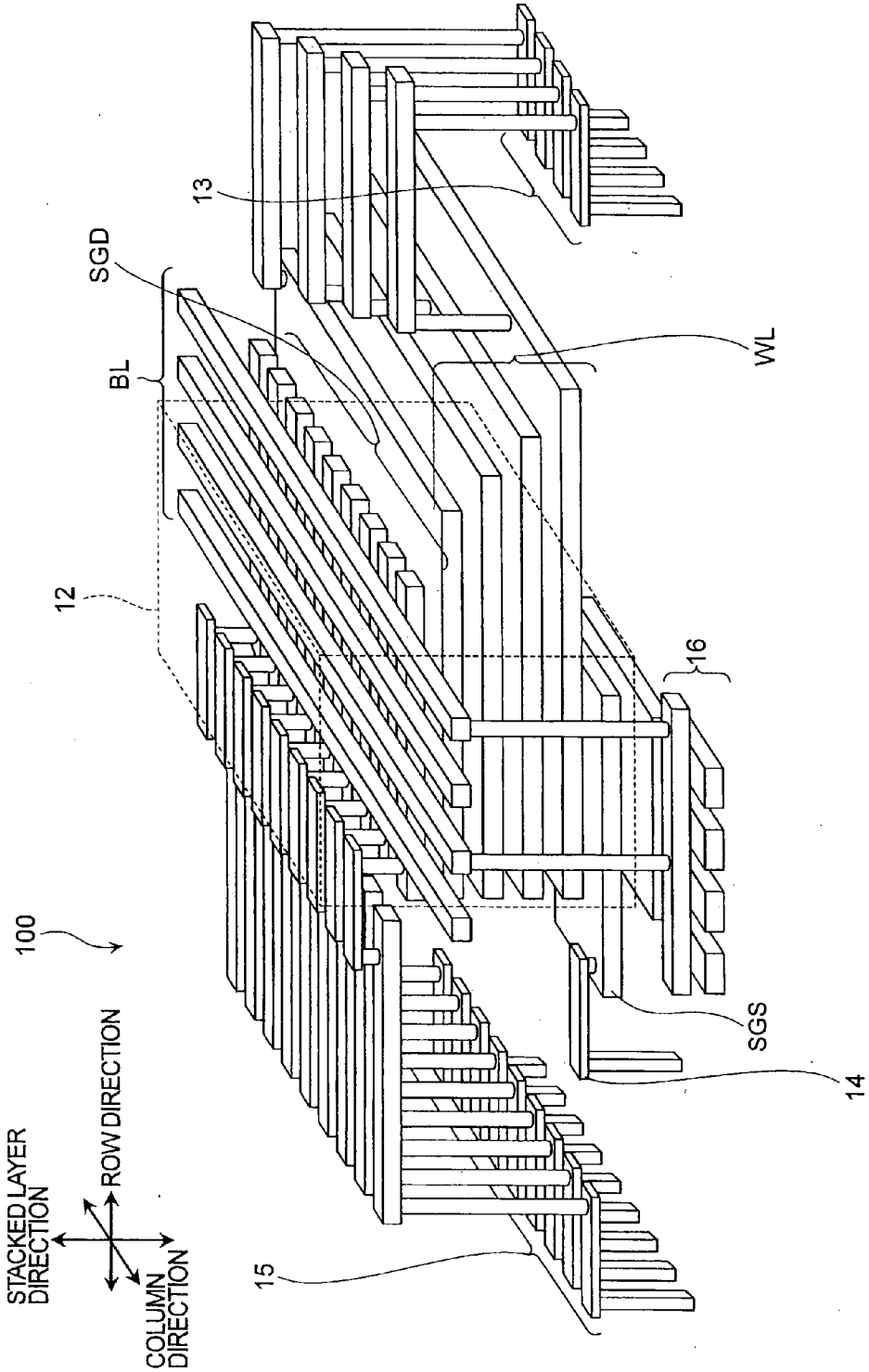

100
STACKED LAYER DIRECTION
ROW DIRECTION
COLUMN DIRECTION
12
BL
SGD
13
WL
15
16
SGS
14

FIG. 1

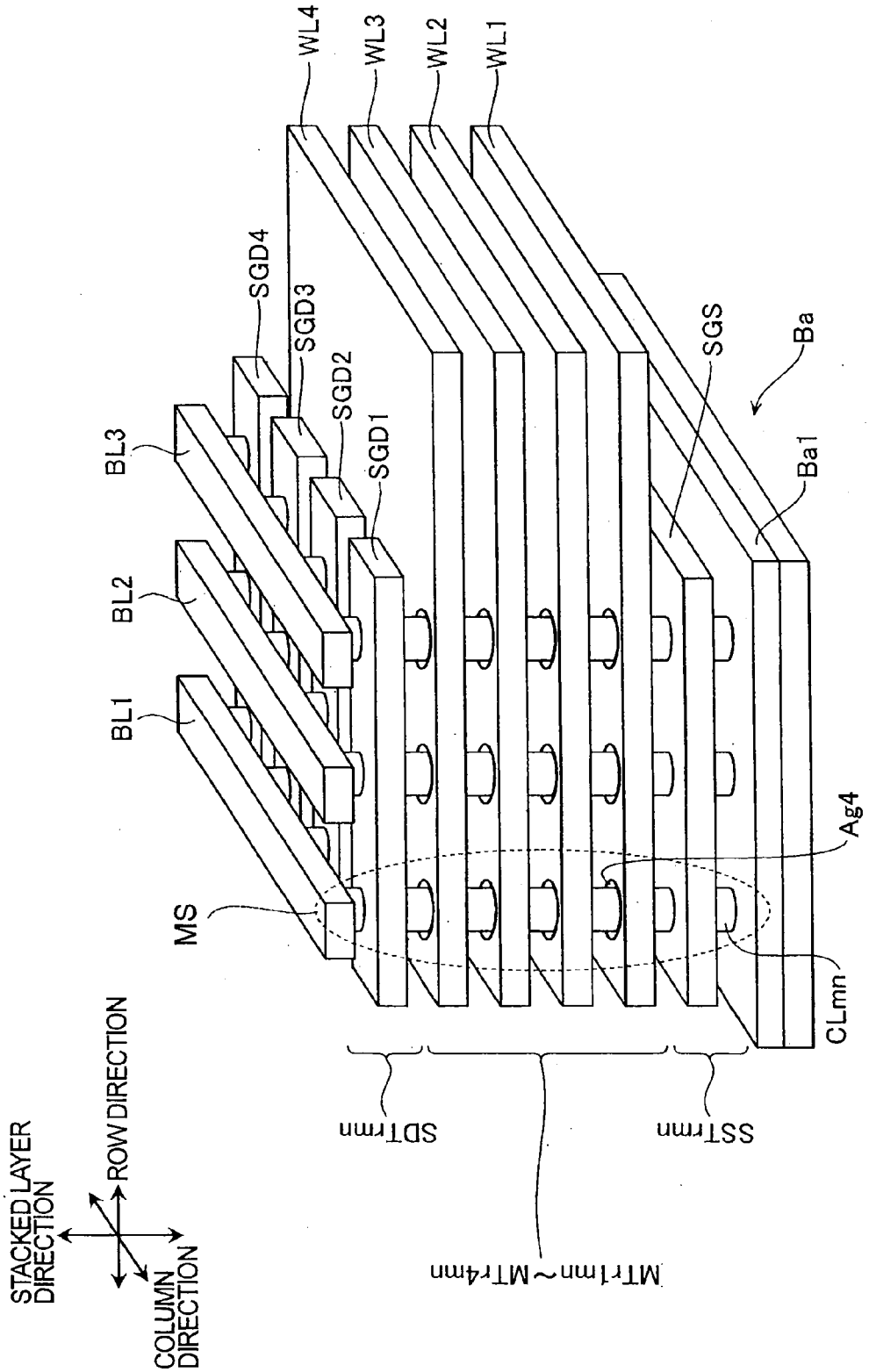

WL4
WL3
WL2
WL1
SGD4
SGD3
SGD2
SGD1
SGS
Ba
Ba1
BL3
BL2
BL1
MS
Ag4
CLmn
SDTrmn
SSTrmn
MTr1mn~MTr4mn
STACKED LAYER DIRECTION
ROW DIRECTION
COLUMN DIRECTION

FIG. 2

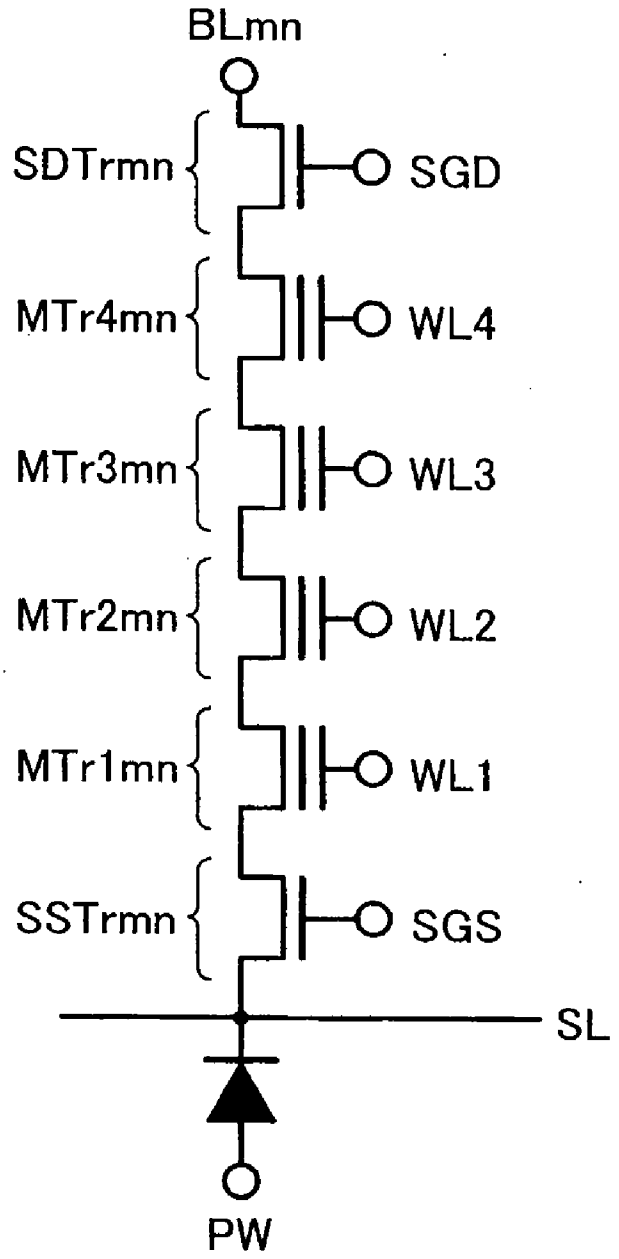

BLmn
SDTrmn
SGD
MTr4mn
WL4
MTr3mn
WL3
MTr2mn
WL2
MTr1mn
WL1
SSTrmn
SGS
SL
PW

FIG. 3

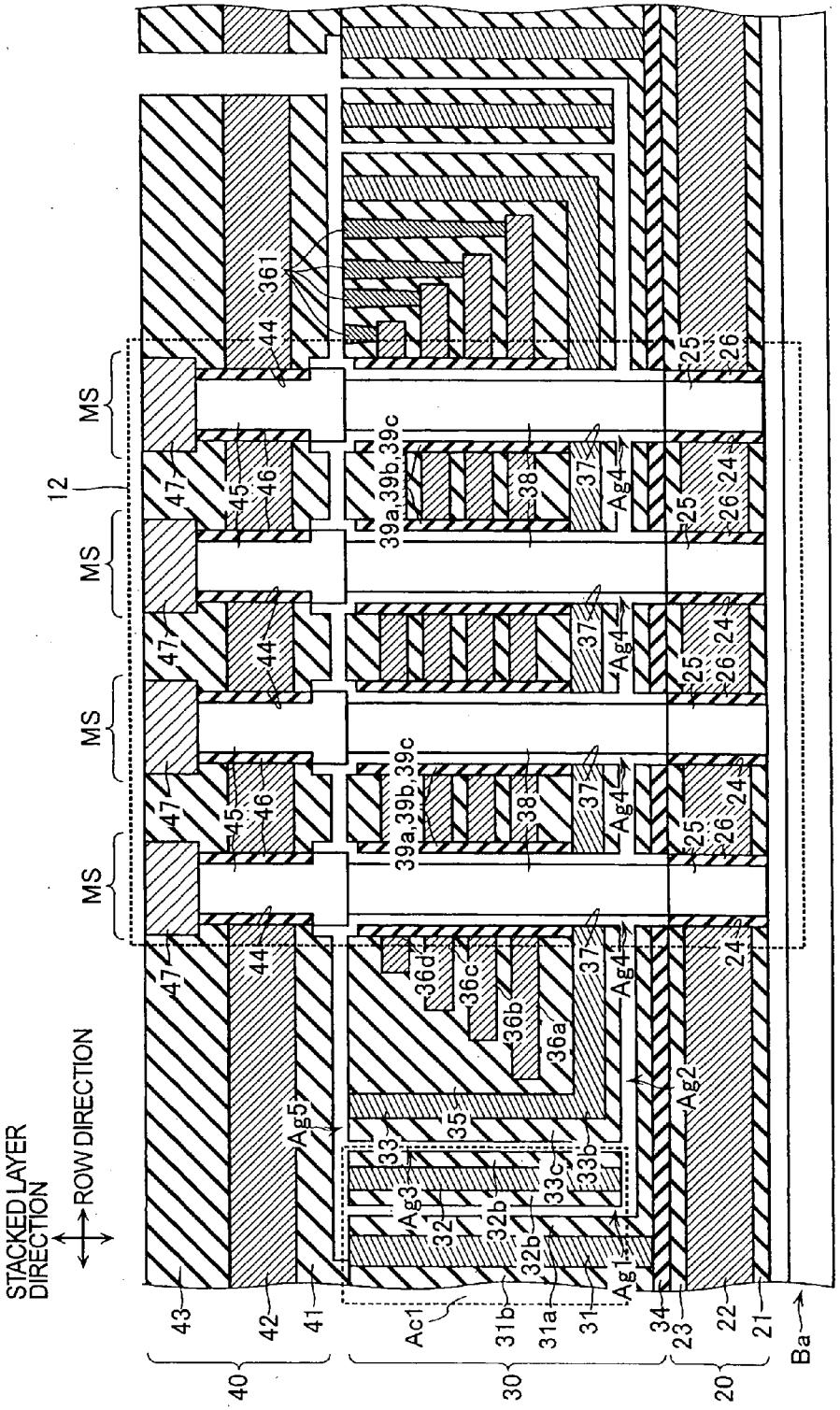

STACKED LAYER DIRECTION
ROW DIRECTION
MS
MS
MS
MS
12
361
44
47
45
46
39a,39b,39c
38
37
Ag4
25
26
24
36d
36c
36b
36a
35
33
Ag3
32
32b
33c
33b
Ag1
Ac1
31b
31a
31
34
23
22
21
Ba
Ag2
Ag5
43
42
41
40
30
20

FIG. 4

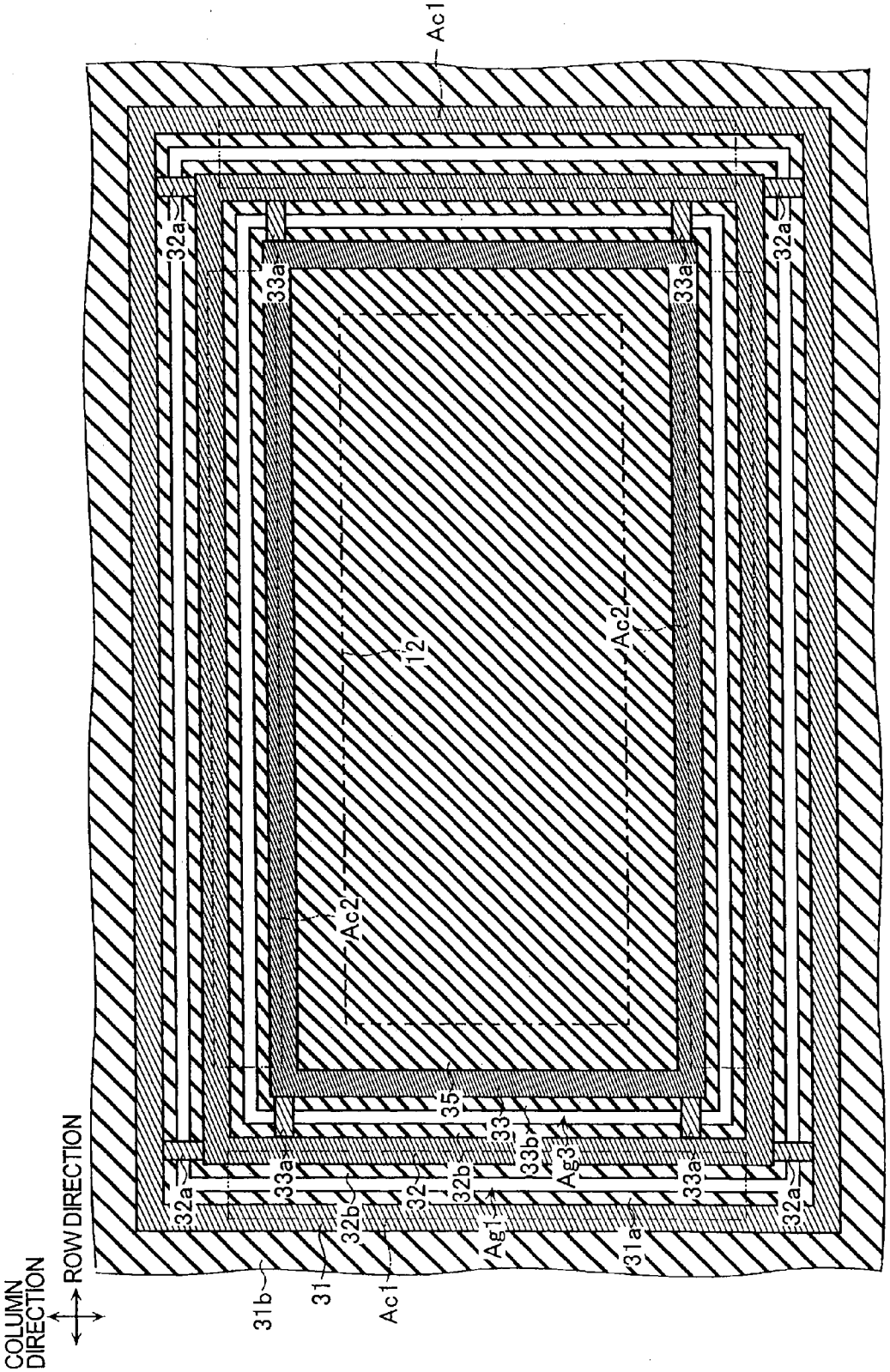

Ac1
32a
33a
12
Ac2
35
33
33b
Ag3
32
32b
Ag1
31a
31b
31
COLUMN DIRECTION
ROW DIRECTION

FIG. 5

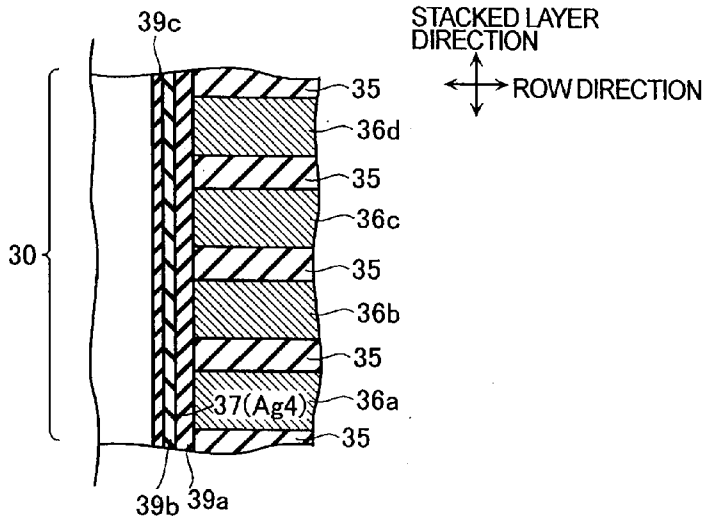

39c
STACKED LAYER DIRECTION
ROW DIRECTION
35
36d
35
36c
30
35
36b
35
37(Ag4)
36a
35
39b
39a

FIG. 6

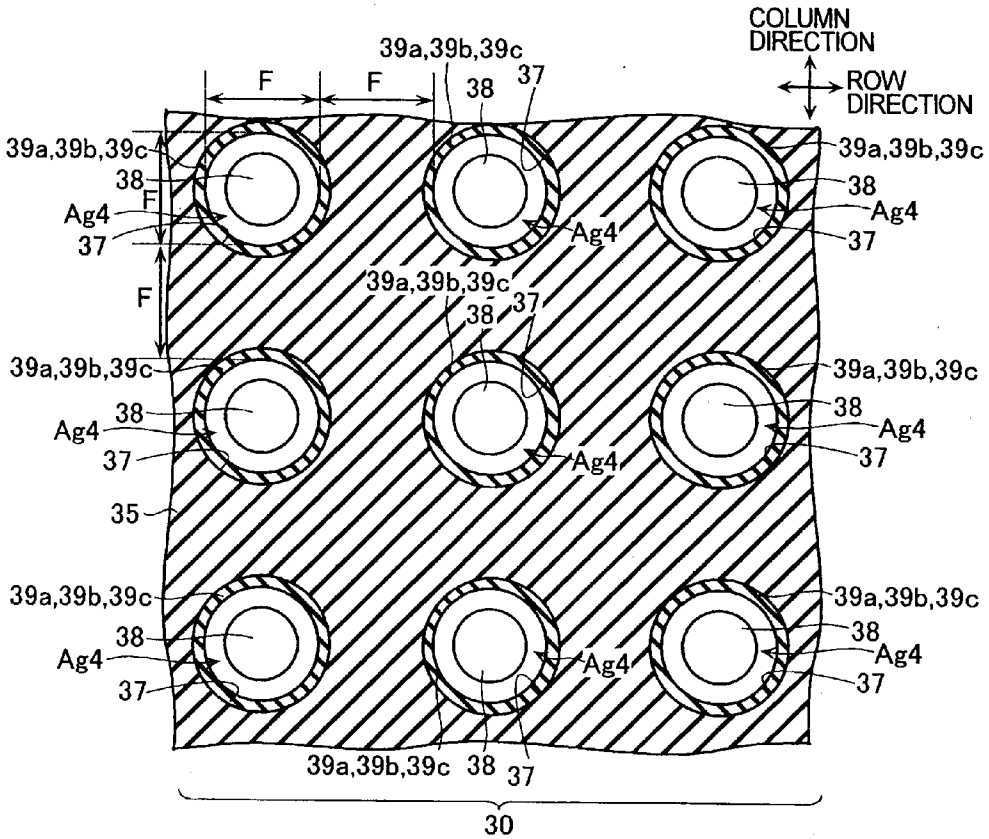

COLUMN DIRECTION
ROW DIRECTION
39a,39b,39c
F
F
38
37
Ag4
35
30

FIG. 7

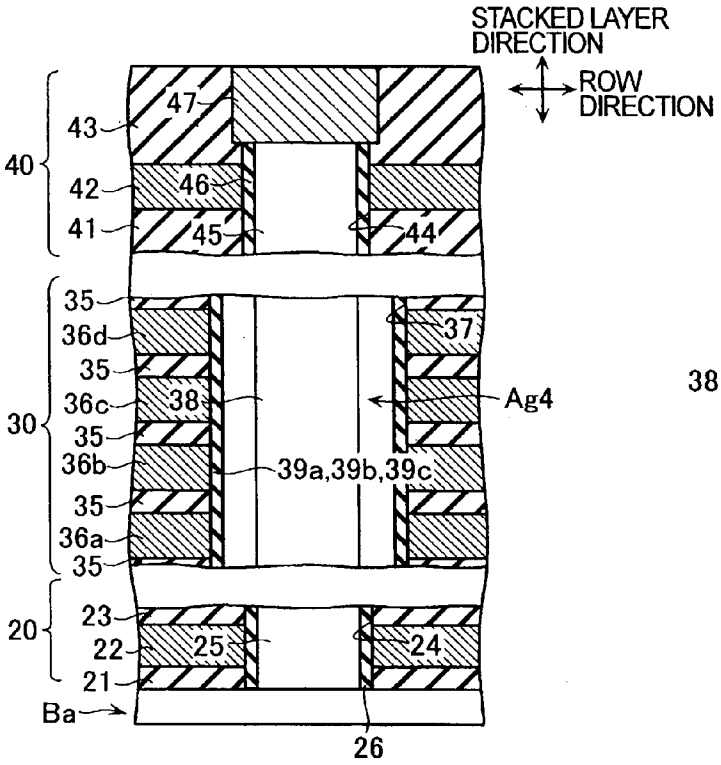

STACKED LAYER DIRECTION
ROW DIRECTION
40
43
47
42
46
41
45
44
35
36d
37
35
36c
38
Ag4
30
35
36b
39a,39b,39c
35
36a
35
20
23
22
25
24
21
Ba
26

FIG. 8A

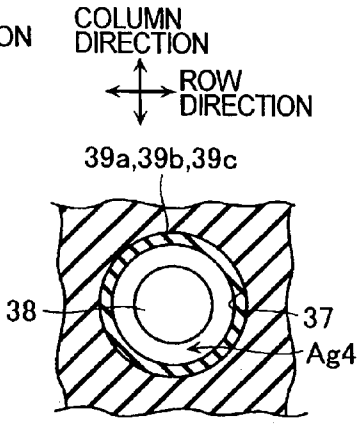

COLUMN DIRECTION
ROW DIRECTION
39a,39b,39c
38
37
Ag4

FIG. 8B

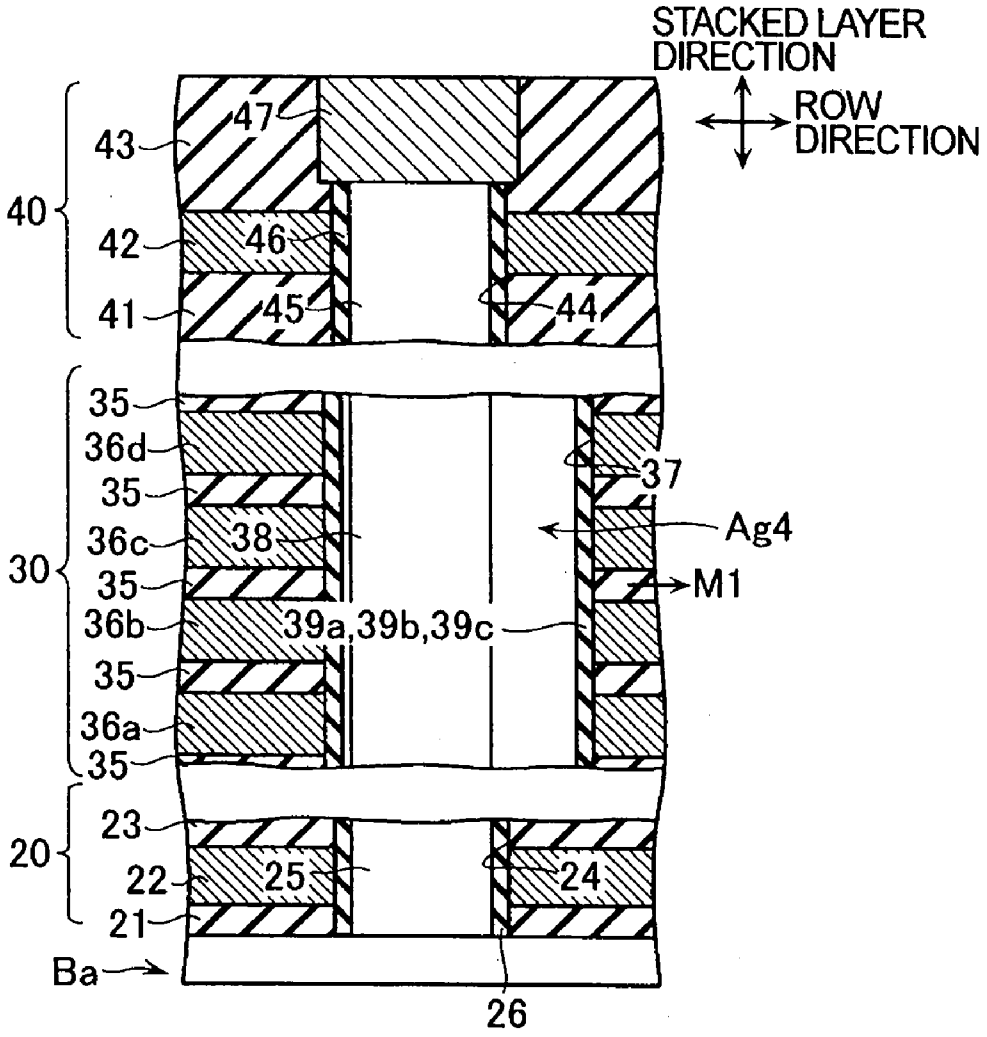

STACKED LAYER DIRECTION
ROW DIRECTION
40
43
47
42
46
41
45
44
30
35
36d
35
36c
38
35
36b
39a,39b,39c
35
36a
35
37
Ag4
M1
20
23
22
25
24
21
Ba
26

FIG. 9A

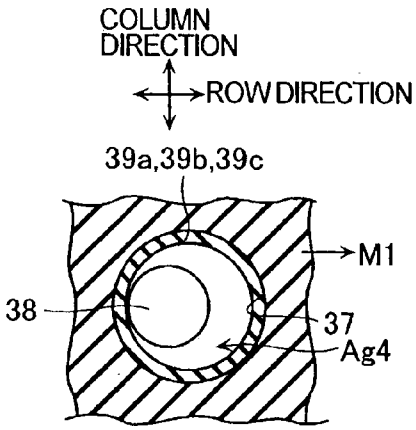


FIG. 9B

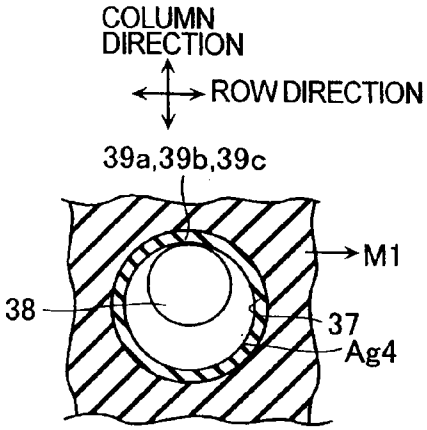


FIG. 9C

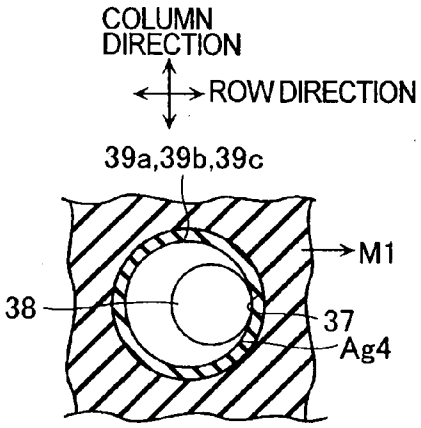


FIG. 9D

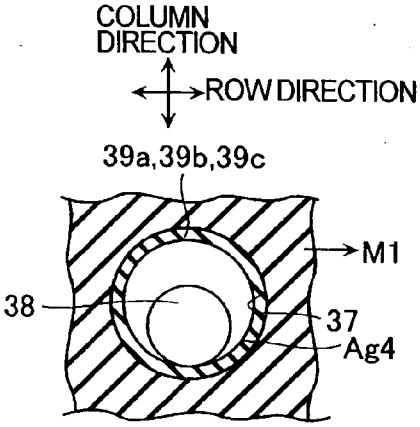


FIG. 9E

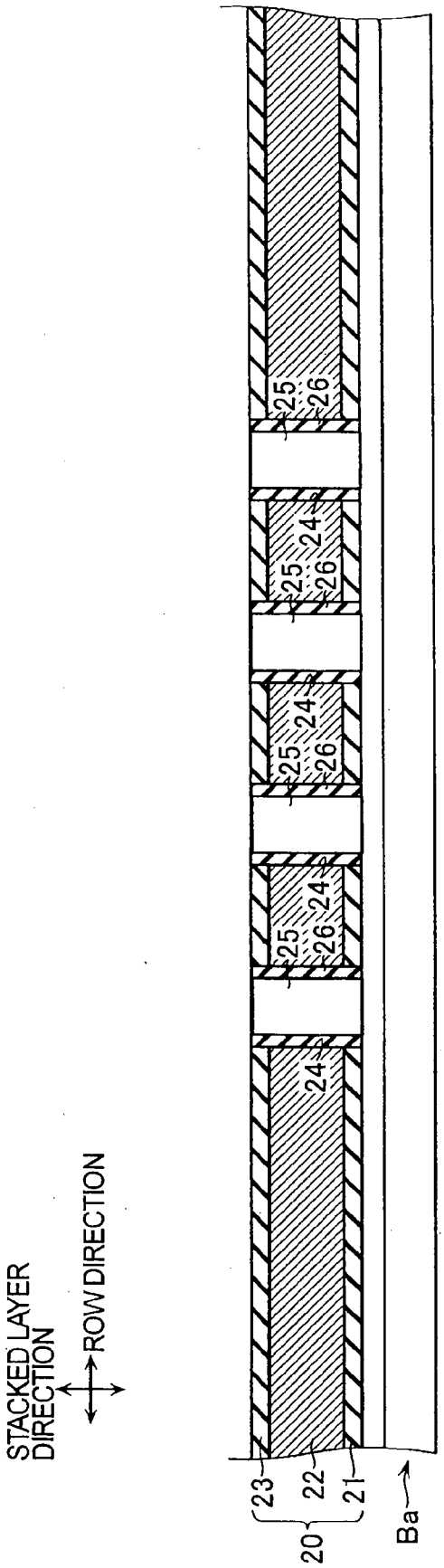


FIG. 10

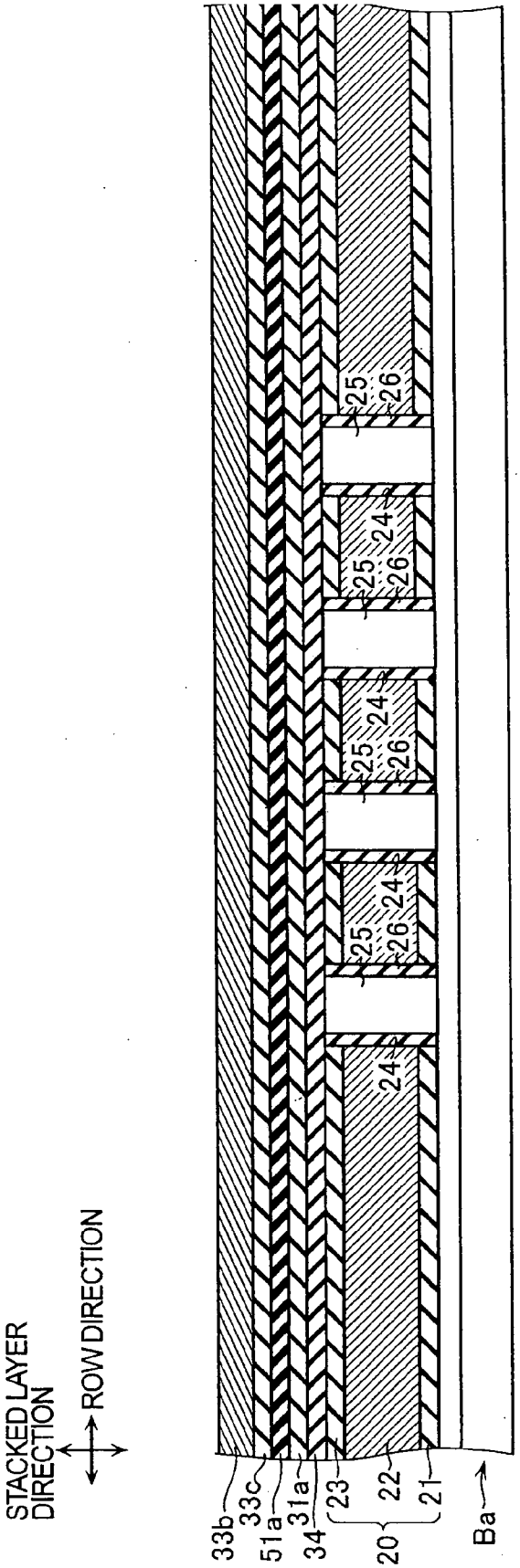

STACKED LAYER DIRECTION
ROW DIRECTION
33b
33c
51a
31a
34
23
20
22
21
Ba
24
25
26

FIG. 11

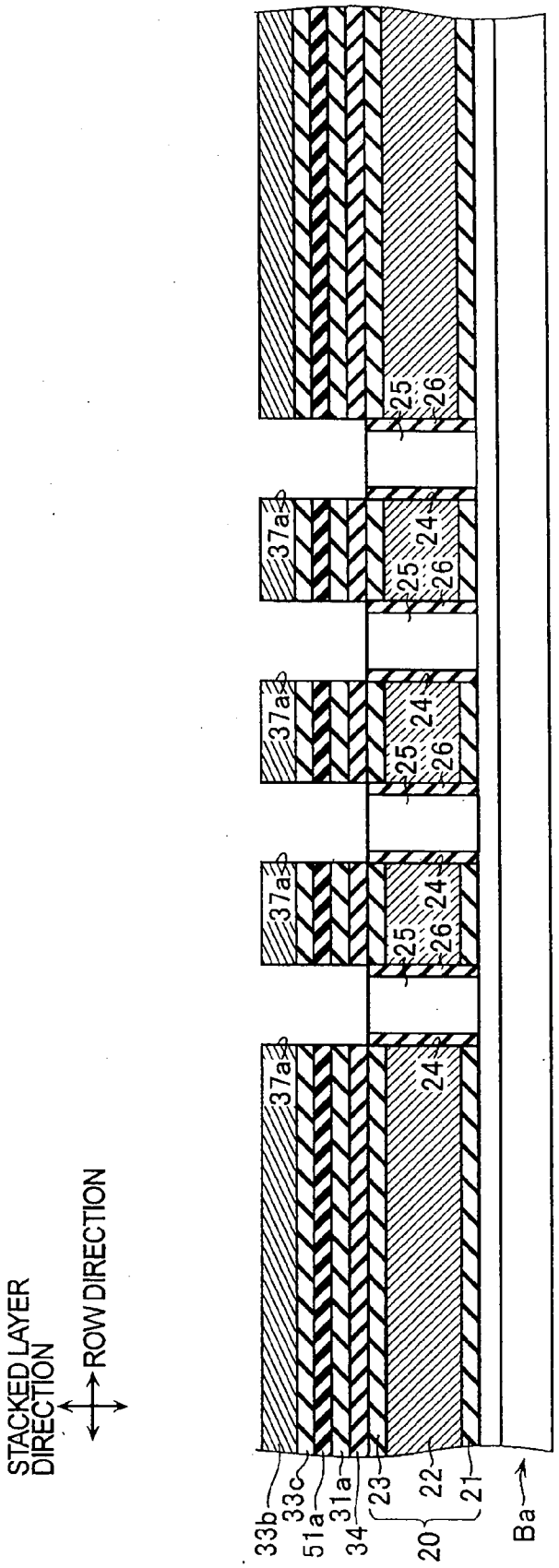

STACKED LAYER DIRECTION
ROW DIRECTION
33b
33c
51a
31a
34
23
20
22
21
Ba
37a
24
25
26

FIG. 12

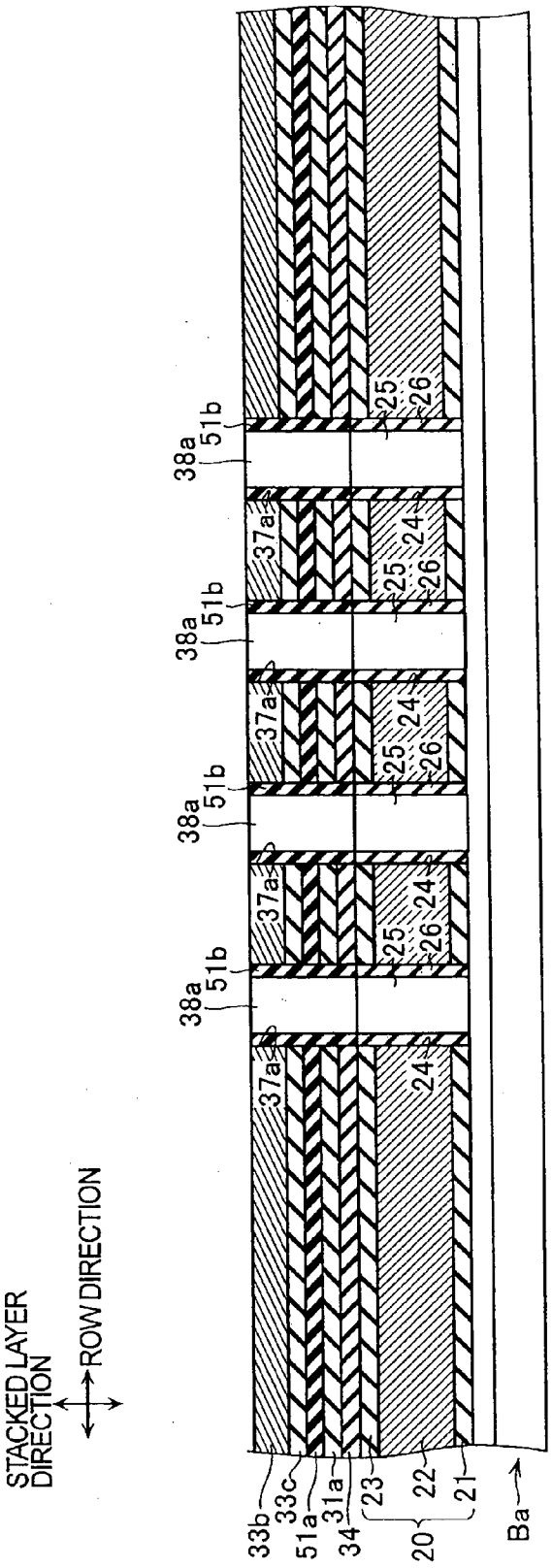

STACKED LAYER DIRECTION
ROW DIRECTION
33b
33c
51a
31a
34
23
20
22
21
Ba
37a
24
25
26
38a
51b

FIG. 13

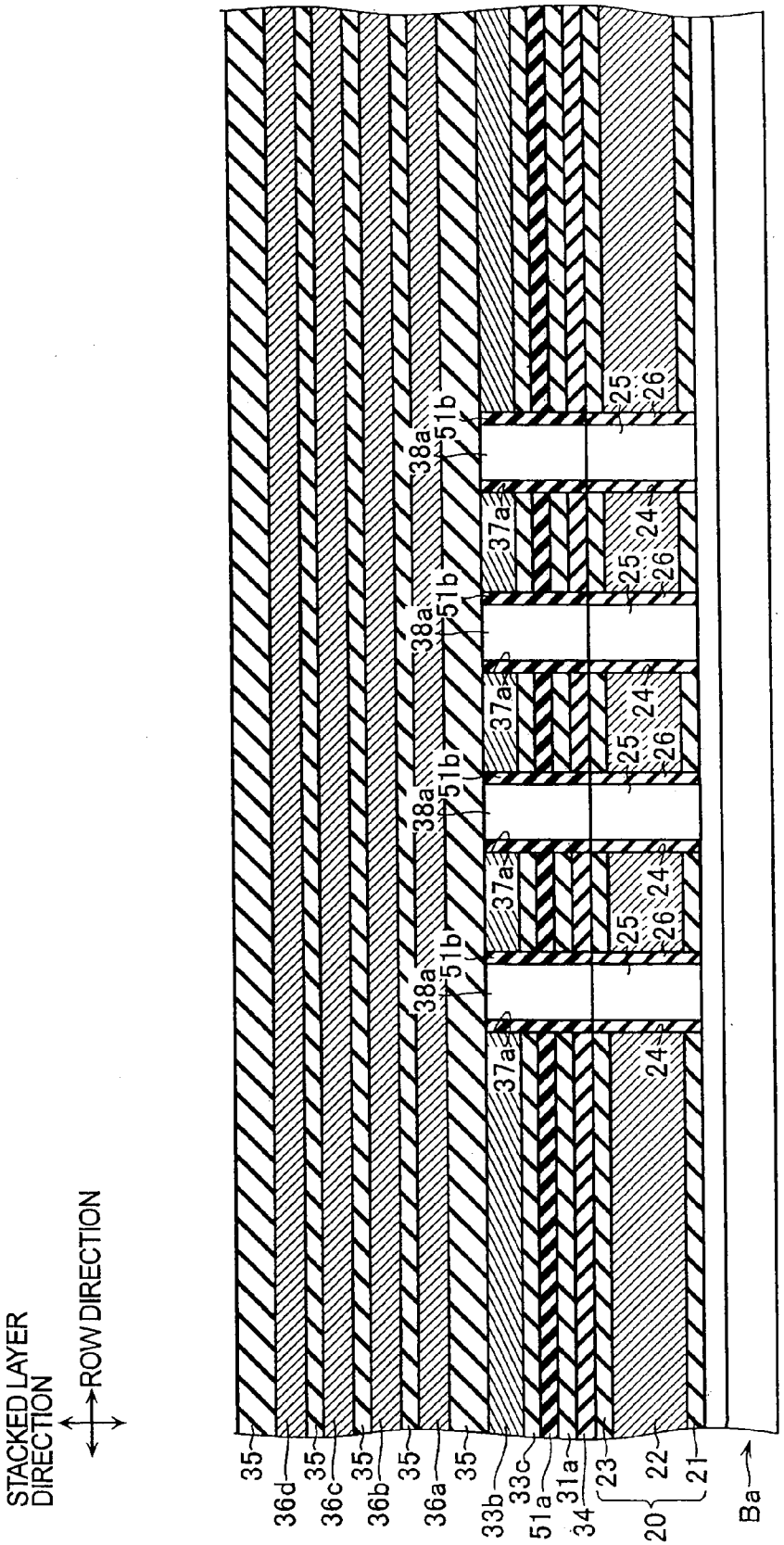

STACKED LAYER DIRECTION
ROW DIRECTION
35
36d
35
36c
35
36b
35
36a
35
33b
33c
51a
31a
34
23
20
22
21
Ba
37a
38a
51b
24
25
26

FIG. 14

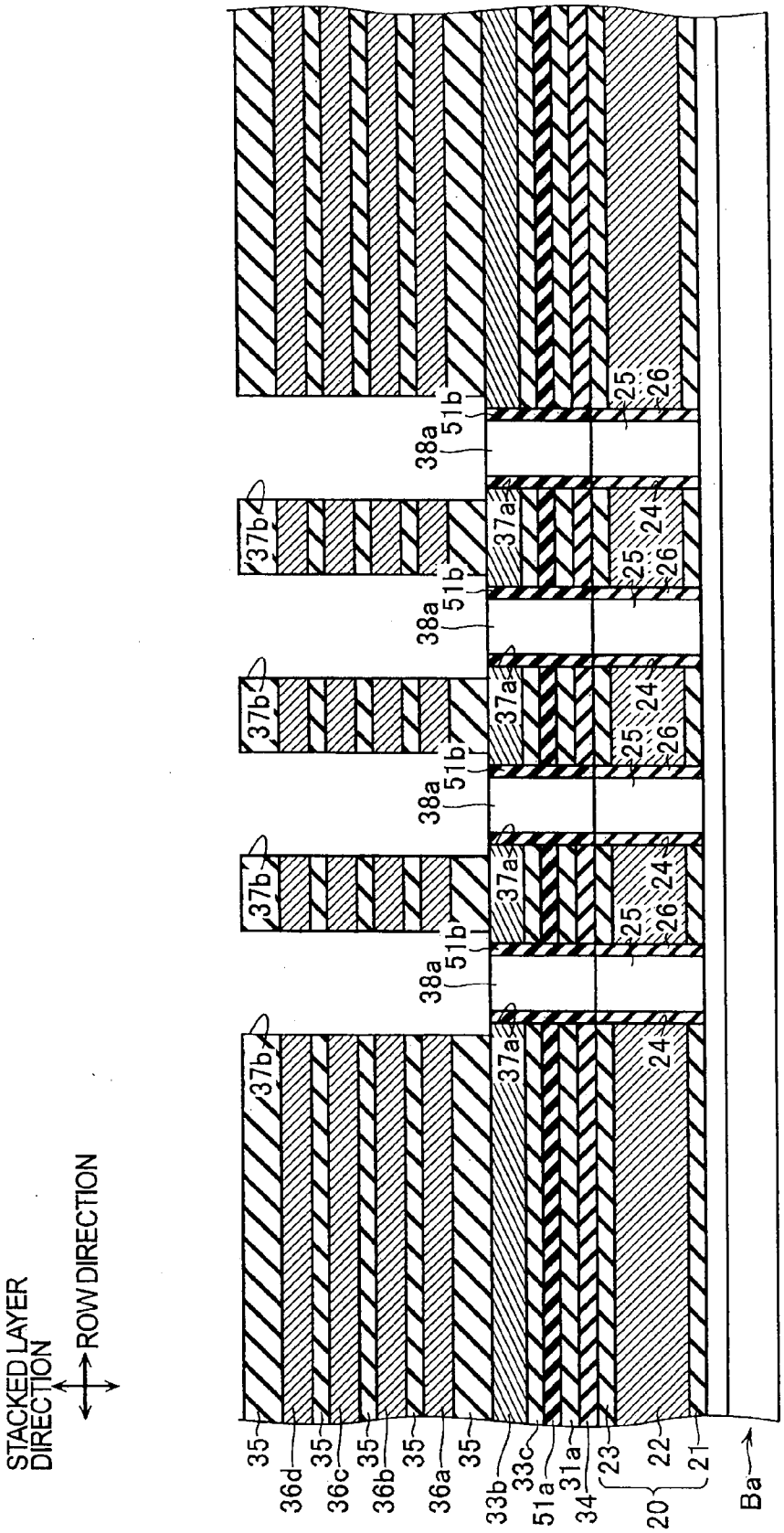

STACKED LAYER DIRECTION
ROW DIRECTION
35
36d
35
36c
35
36b
35
36a
35
33b
33c
51a
31a
34
23
20
22
21
Ba
37b
37a
38a
51b
24
25
26

FIG. 15

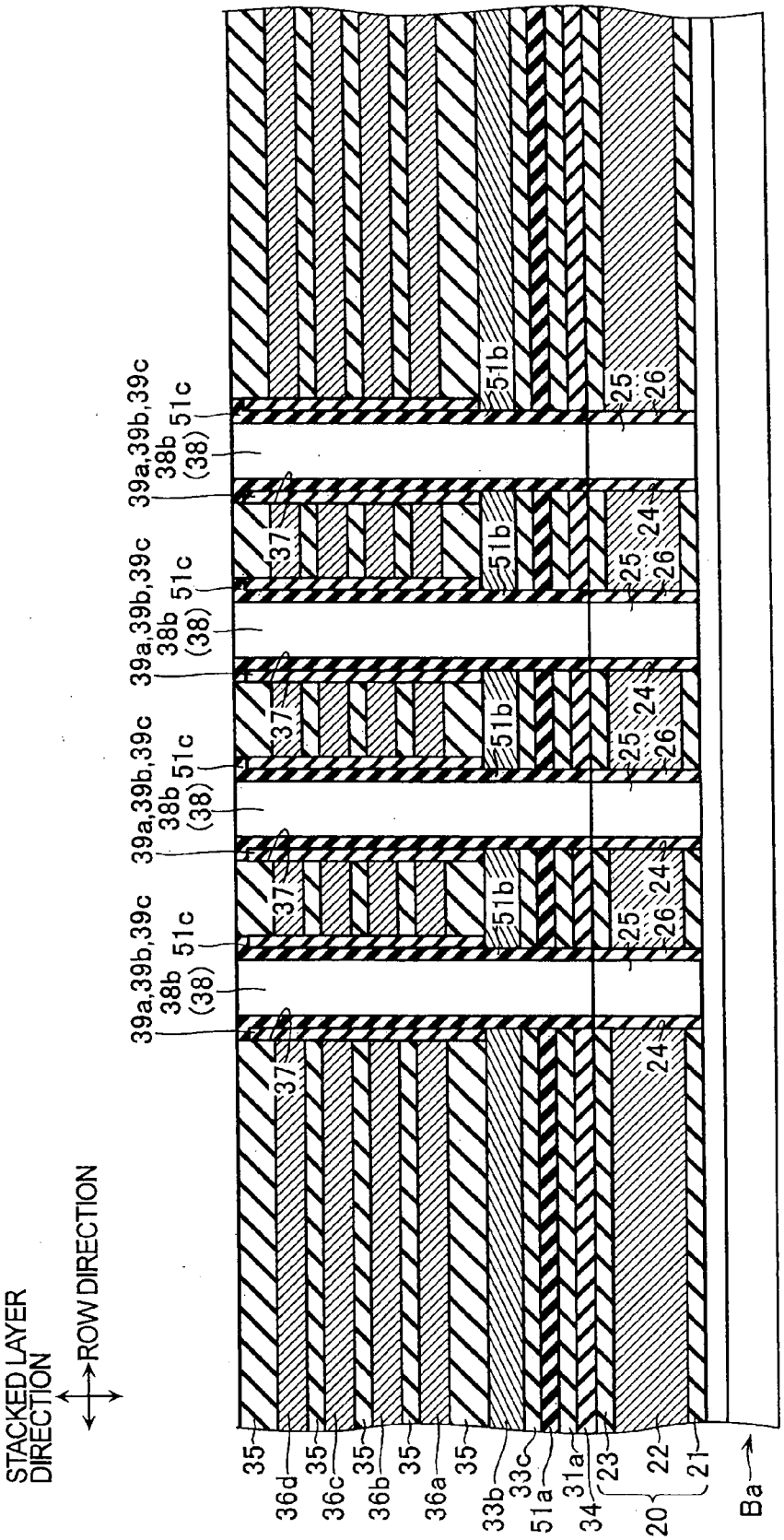

STACKED LAYER DIRECTION
ROW DIRECTION
39a,39b,39c
38b
(38)
51c
37
51b
25
26
24
35
36d
36c
36b
36a
33b
33c
51a
31a
34
23
20
22
21
Ba

FIG. 16

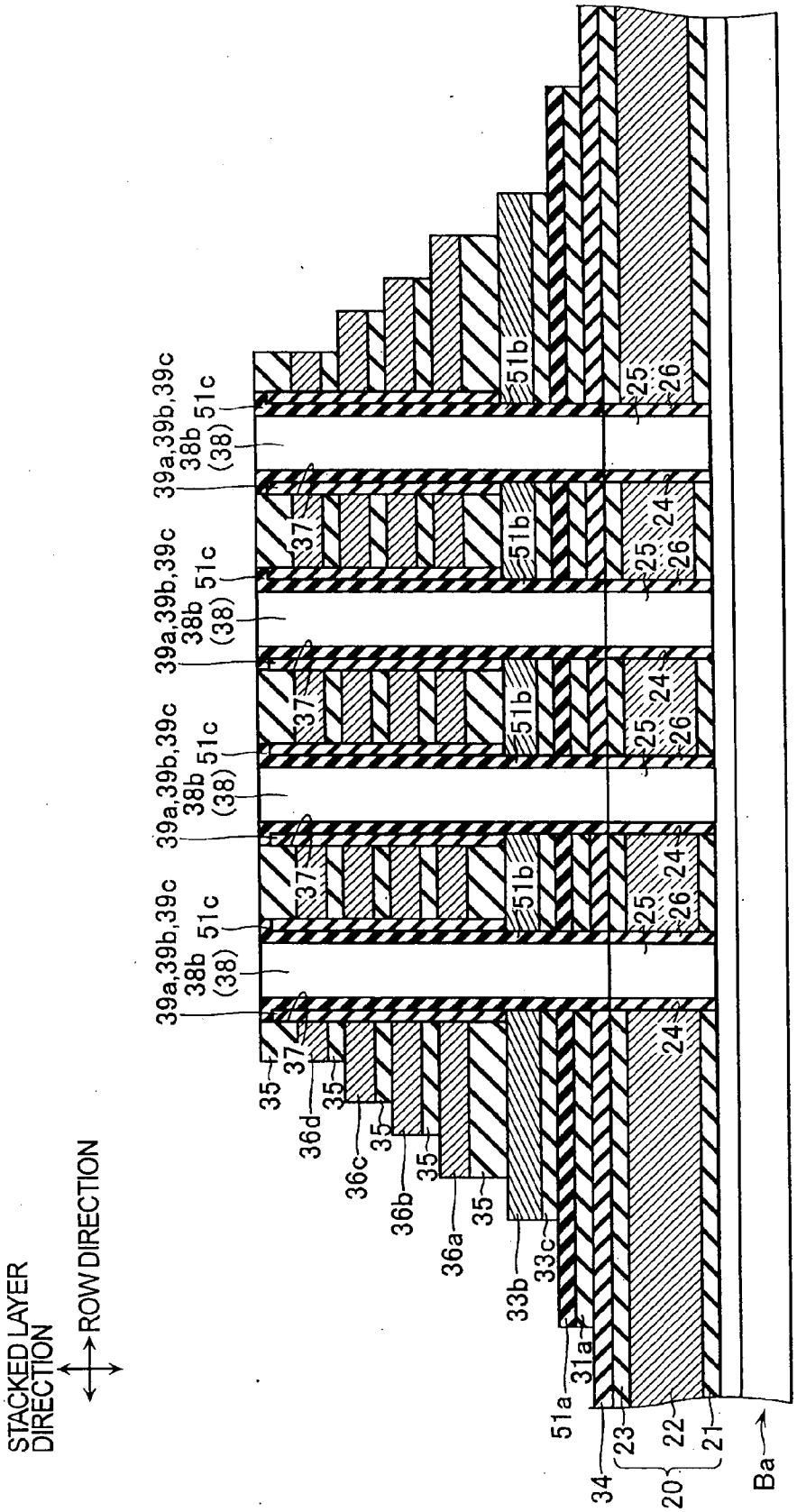

STACKED LAYER DIRECTION
ROW DIRECTION
39a,39b,39c
38b
(38)
51c
37
51b
25
26
24
35
36d
36c
36b
36a
33b
33c
31a
51a
34
23
22
21
20
Ba

FIG. 17

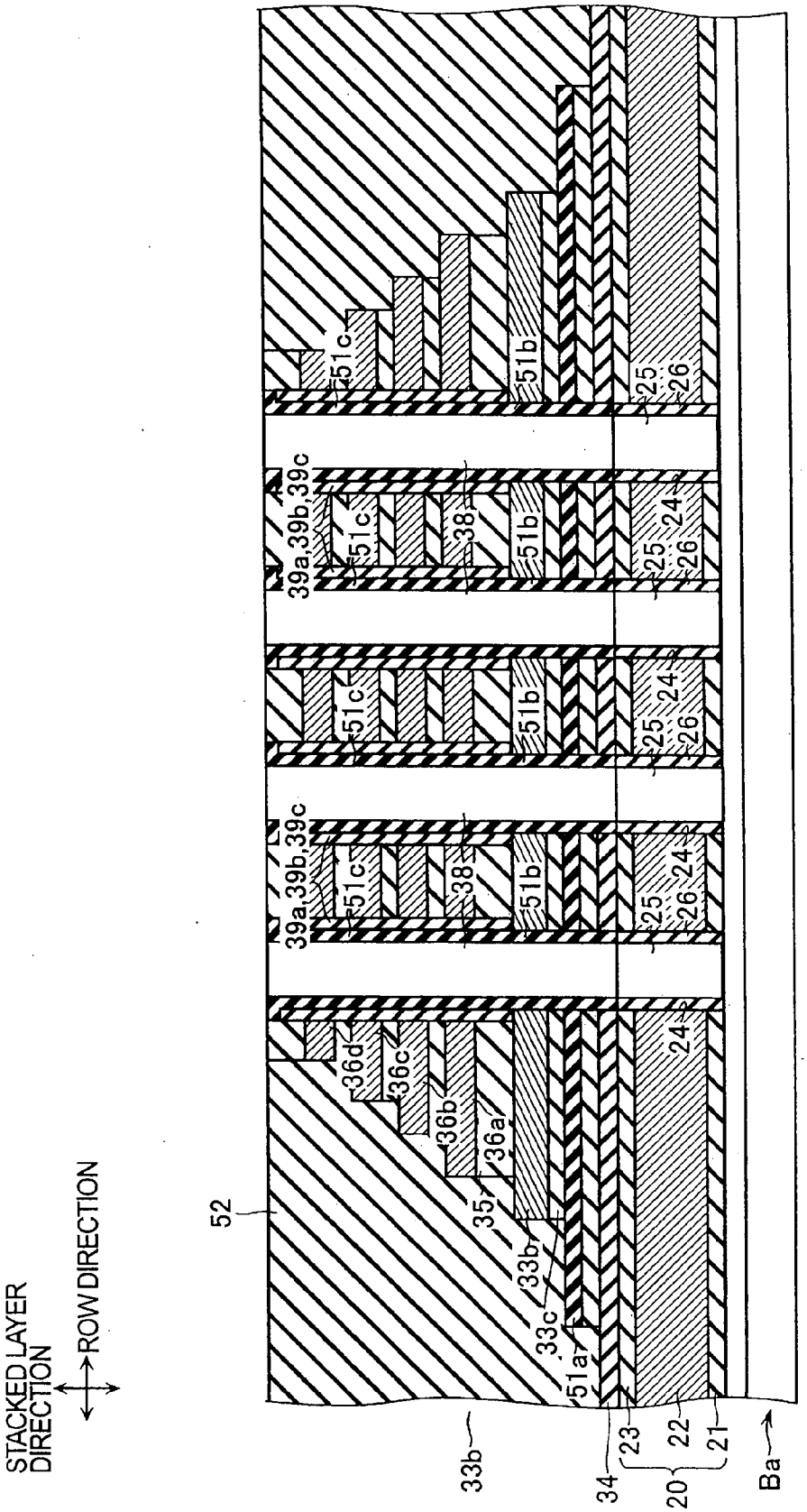

STACKED LAYER DIRECTION
ROW DIRECTION
52
36d
36c
36b
36a
35
33b
33c
51a
39a,39b,39c
51c
38
51b
24
25
26
23
22
21
20
34
Ba

FIG. 18

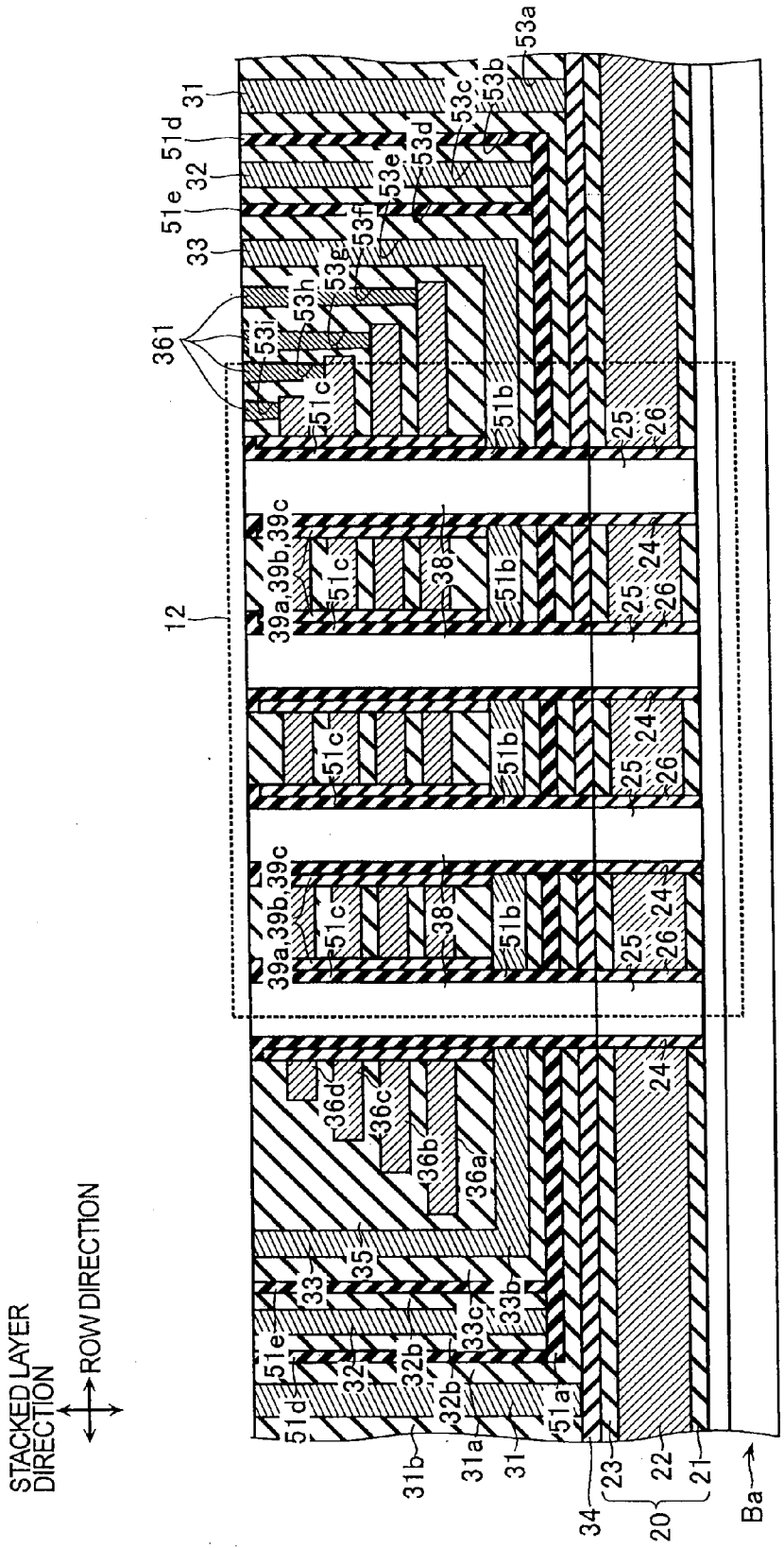

STACKED LAYER DIRECTION
ROW DIRECTION
12
20
21
22
23
24
25
26
31
31a
31b
32
32b
33
33b
33c
34
35
36a
36b
36c
36d
38
39a,39b,39c
51a
51b
51c
51d
51e
53a
53b
53c
53d
53e
53f
53g
53h
53i
361
Ba

FIG. 19

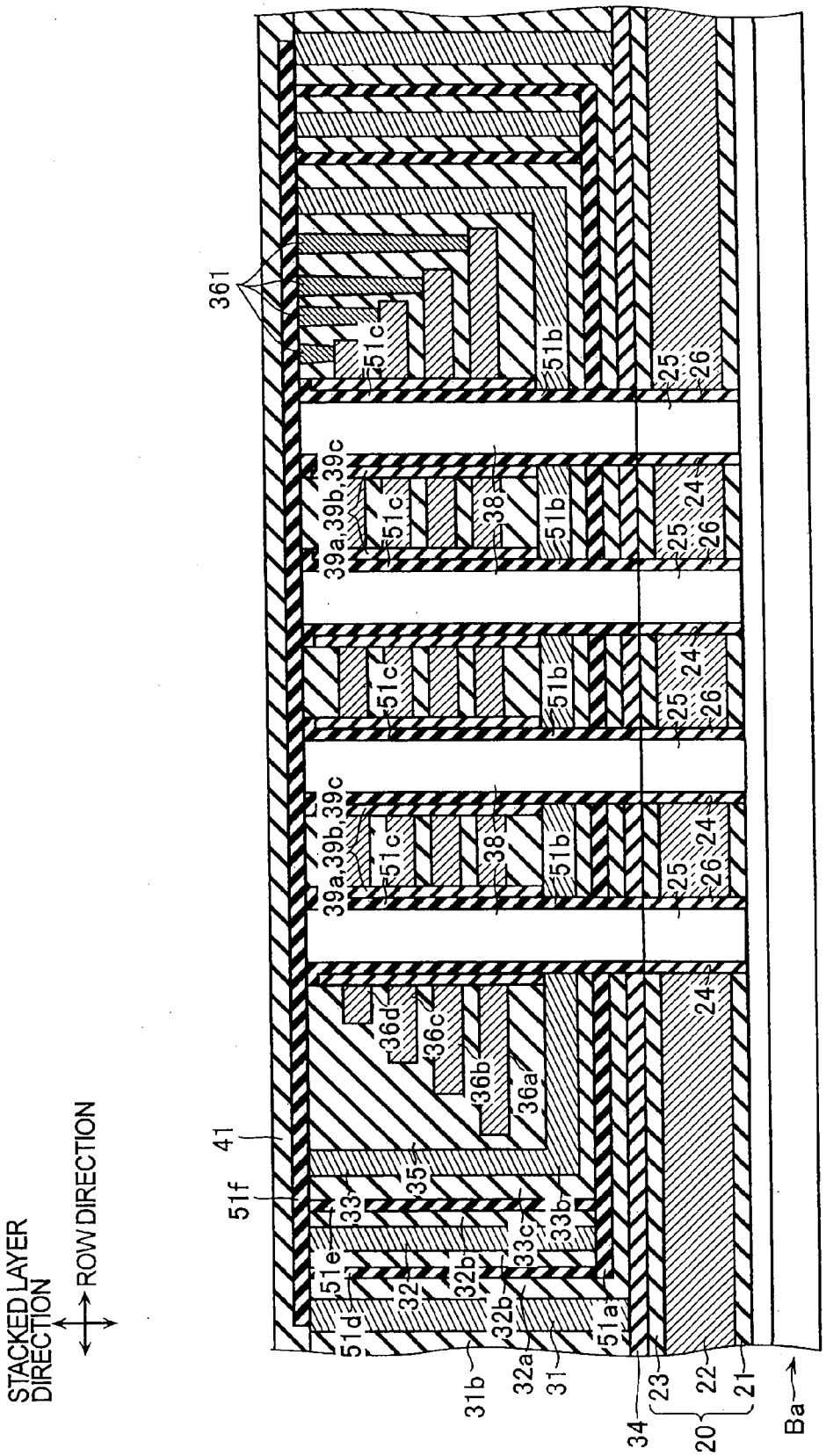

STACKED LAYER DIRECTION
ROW DIRECTION
361
41
51f
51c
51b
51e
51d
51a
39a,39b,39c
38
36a
36b
36c
36d
35
33
33b
33c
32
32b
31b
32a
31
34
23
22
21
20
Ba
25
26
24

FIG. 20

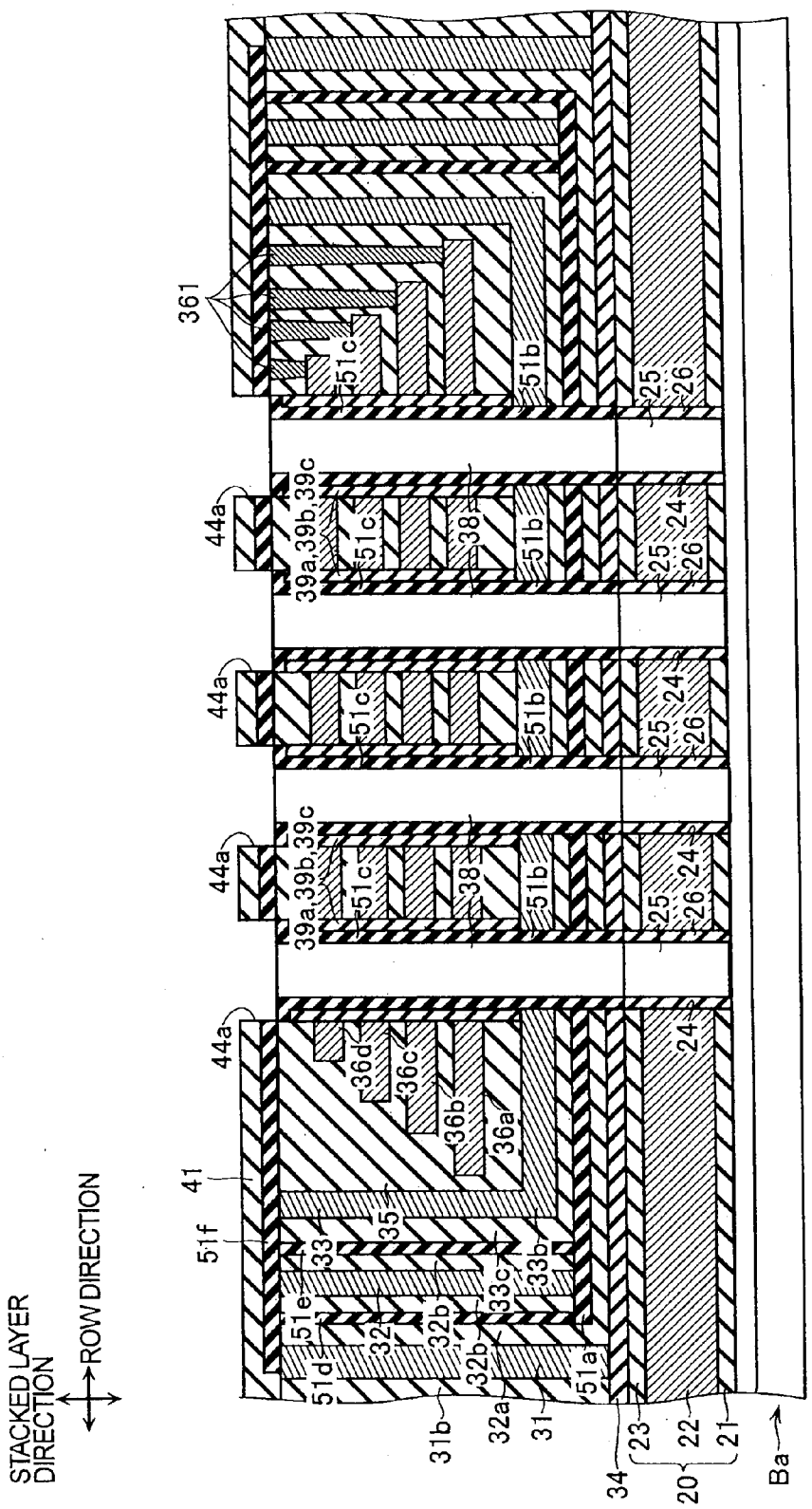

STACKED LAYER DIRECTION
ROW DIRECTION
361
51c
51b
25
26
44a
39a,39b,39c
38
24
41
51f
33
35
36d
36c
36b
36a
51e
51d
32
32b
33c
33b
51a
31b
32a
31
34
23
22
21
20
Ba

FIG. 21

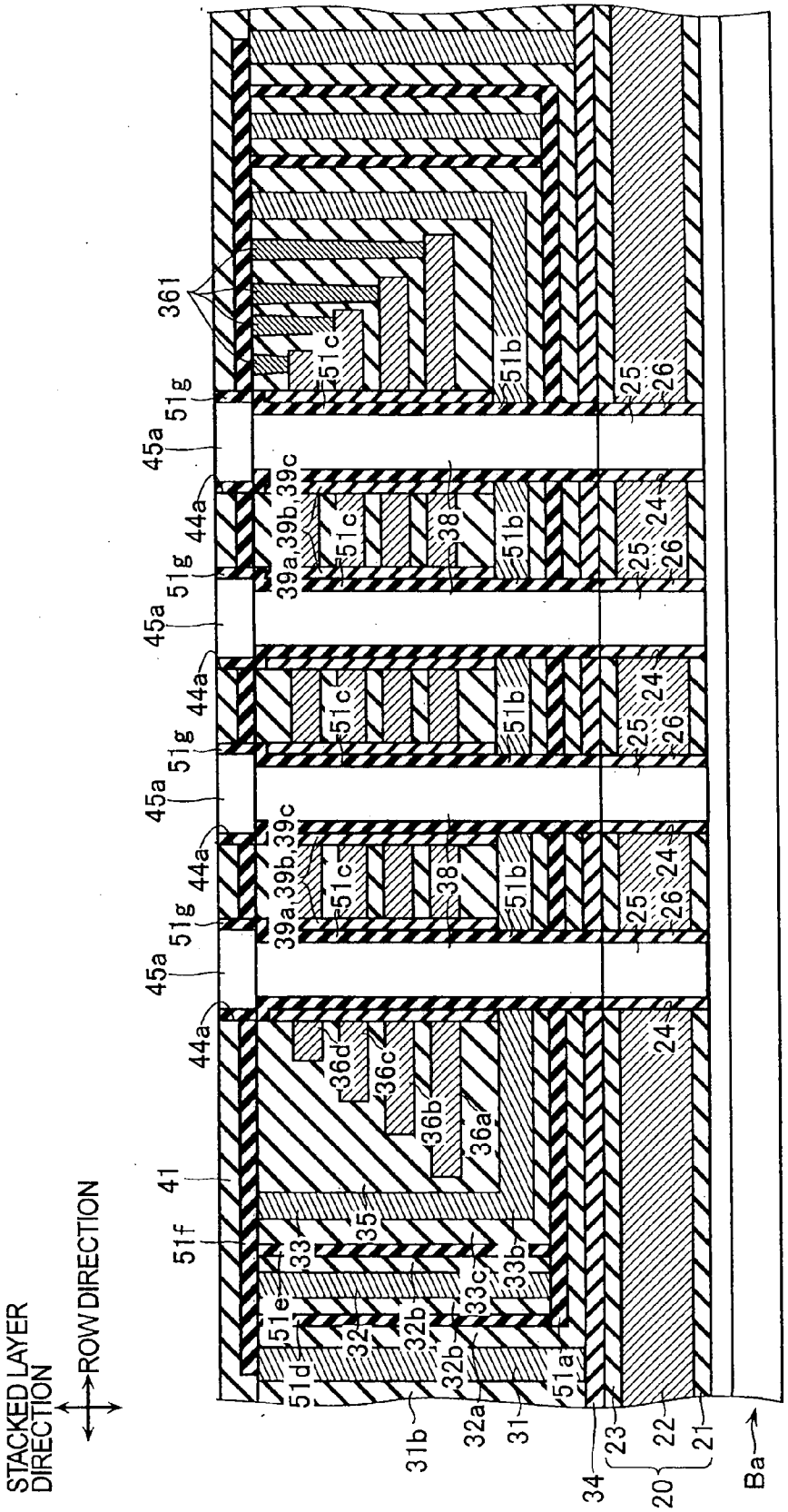

STACKED LAYER DIRECTION
ROW DIRECTION
361
51g
45a
44a
39a,39b,39c
51c
38
51b
25
26
24
41
51f
36d
36c
36b
36a
35
33
33c
33b
51e
32
32b
51d
51a
31b
32a
31
34
23
22
21
20
Ba

FIG. 22

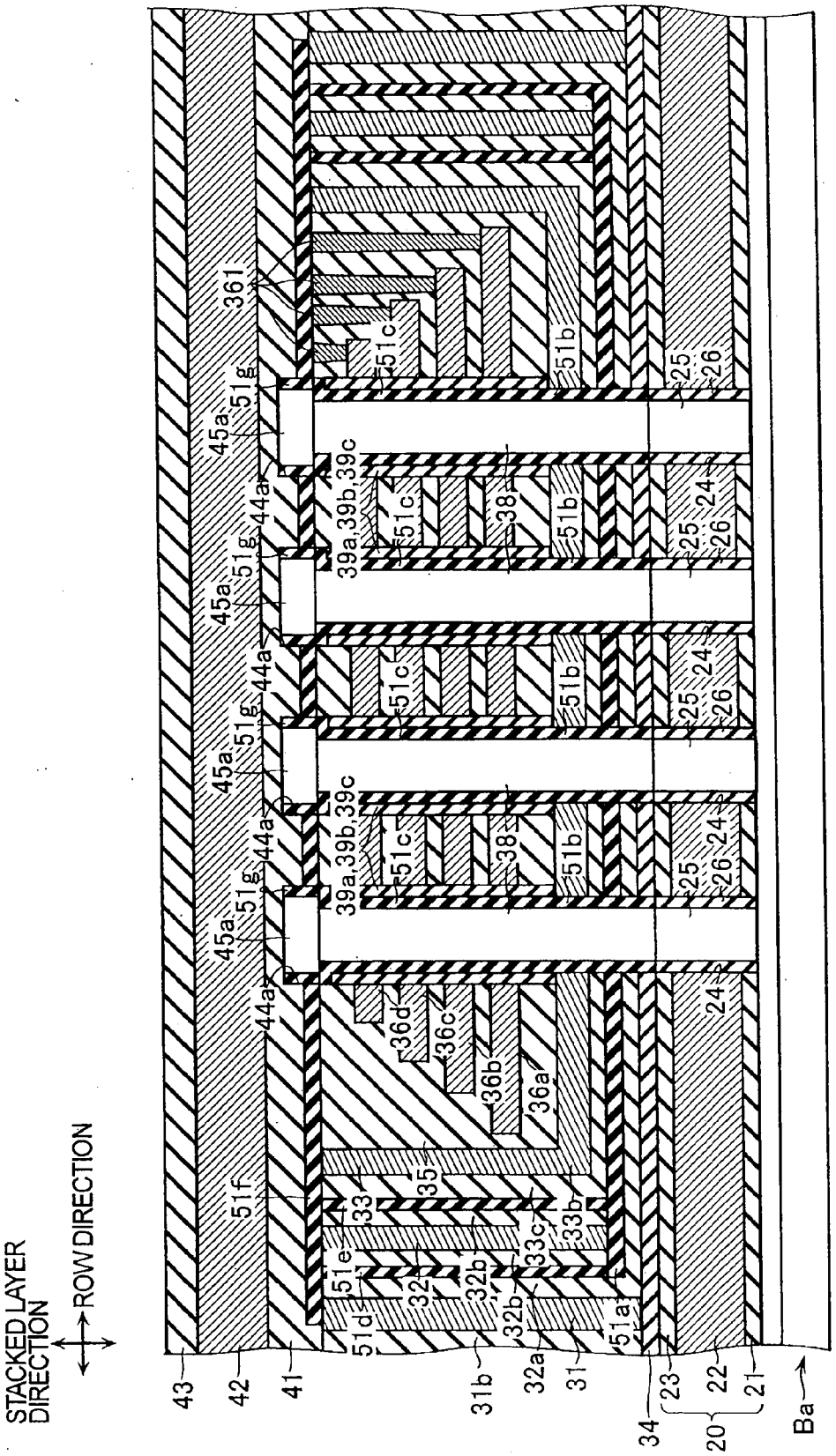

STACKED LAYER DIRECTION
ROW DIRECTION
43
42
41
31b
32a
31
34
23
22
21
20
Ba
51f
51e
51d
51a
32
32b
33
33c
33b
35
36a
36b
36c
36d
44a
45a
51g
39a,39b,39c
38
51c
51b
24
25
26
361

FIG. 23

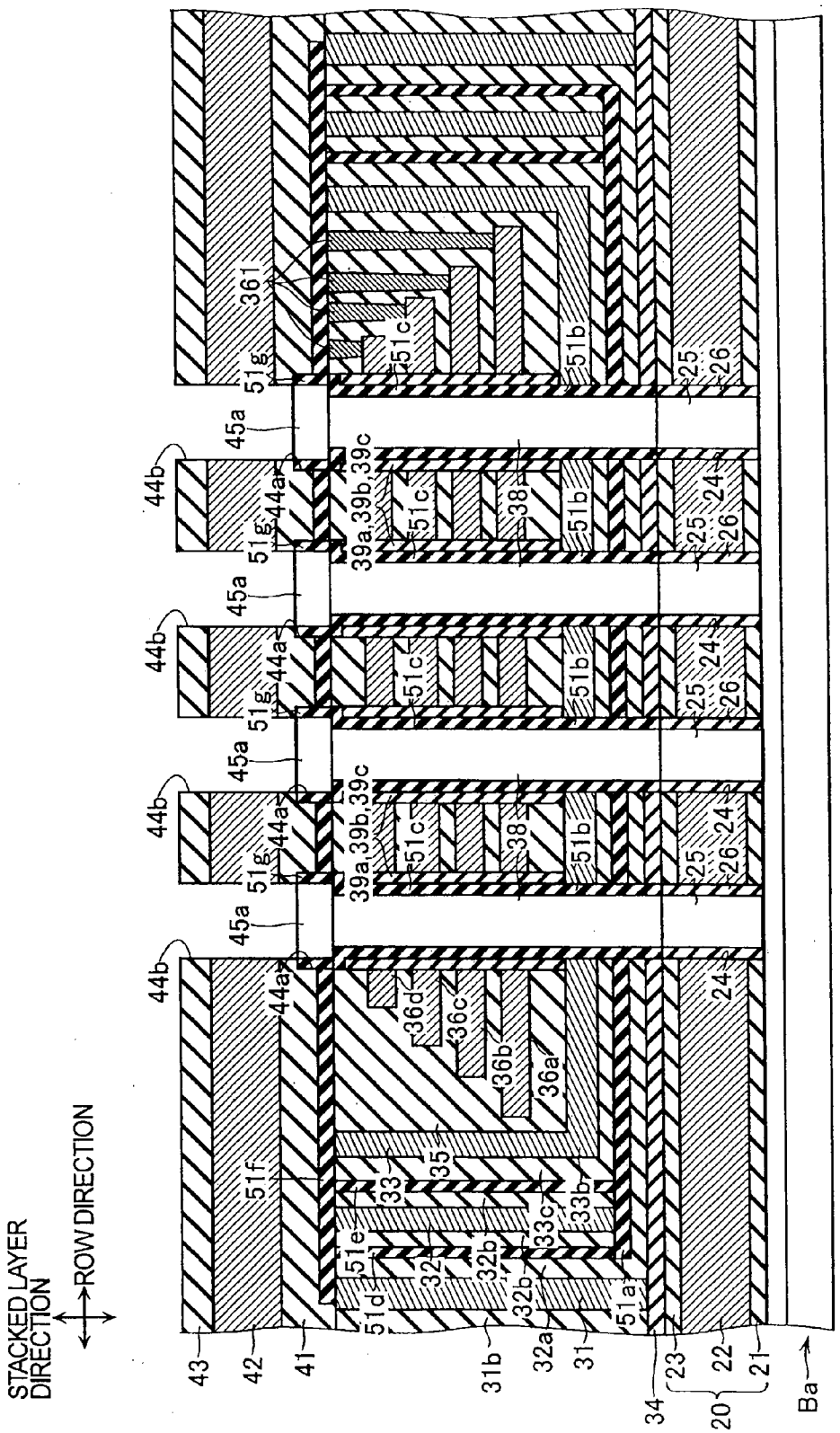

STACKED LAYER DIRECTION
ROW DIRECTION
43
42
41
31b
32a
31
34
23
22
21
20
Ba
51f
51e
51d
32
32b
33
33c
33b
35
36a
36b
36c
36d
44a
44b
45a
51g
51c
51b
39a,39b,39c
38
24
25
26
361

FIG. 24

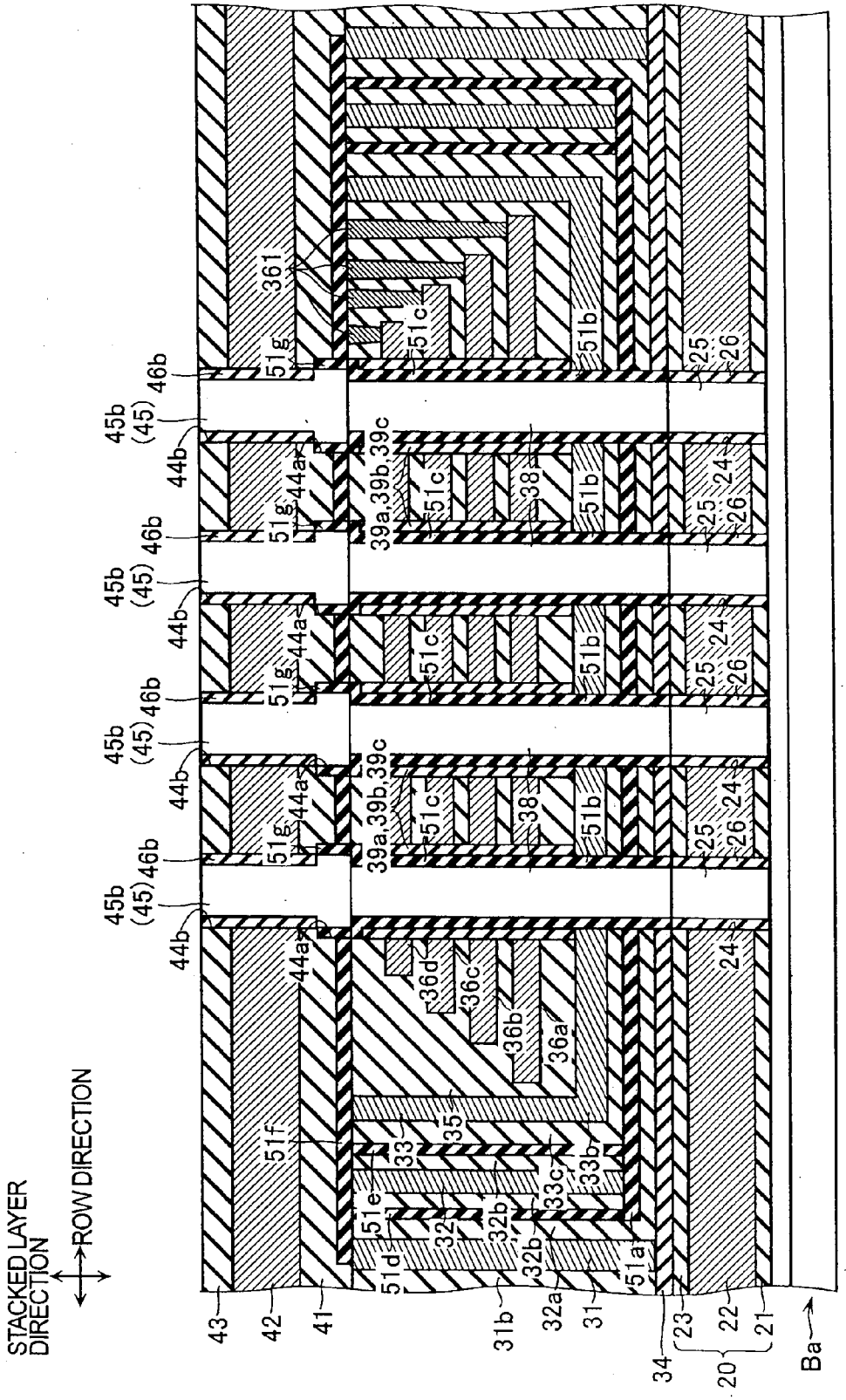

STACKED LAYER DIRECTION
ROW DIRECTION
43
42
41
31b
32a
31
34
23
22
21
20
Ba
51a
51d
51e
51f
51g
51b
51c
51d
51e
51f
51g
32
32b
33
33b
33c
35
36a
36b
36c
36d
44a
44b
45b
(45)
46b
39a,39b,39c
38
24
25
26
361

FIG. 25

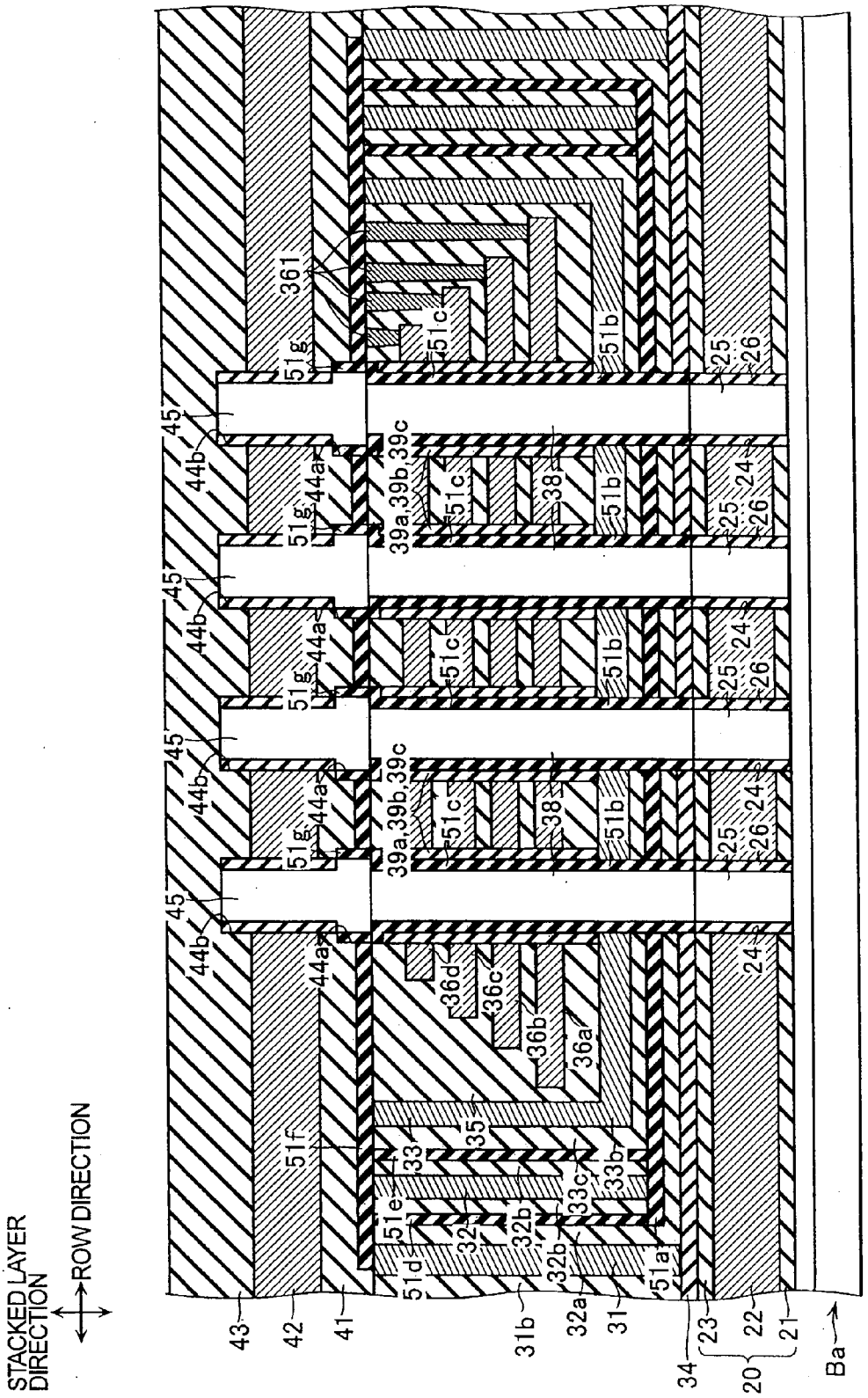

STACKED LAYER DIRECTION
ROW DIRECTION
43
42
41
31b
32a
31
34
23
22
21
20
Ba
51f
51e
51d
51a
33
32
32b
33c
33b
35
36a
36b
36c
36d
44a
44b
45
51g
361
51c
51b
39a,39b,39c
38
24
25
26

FIG. 26

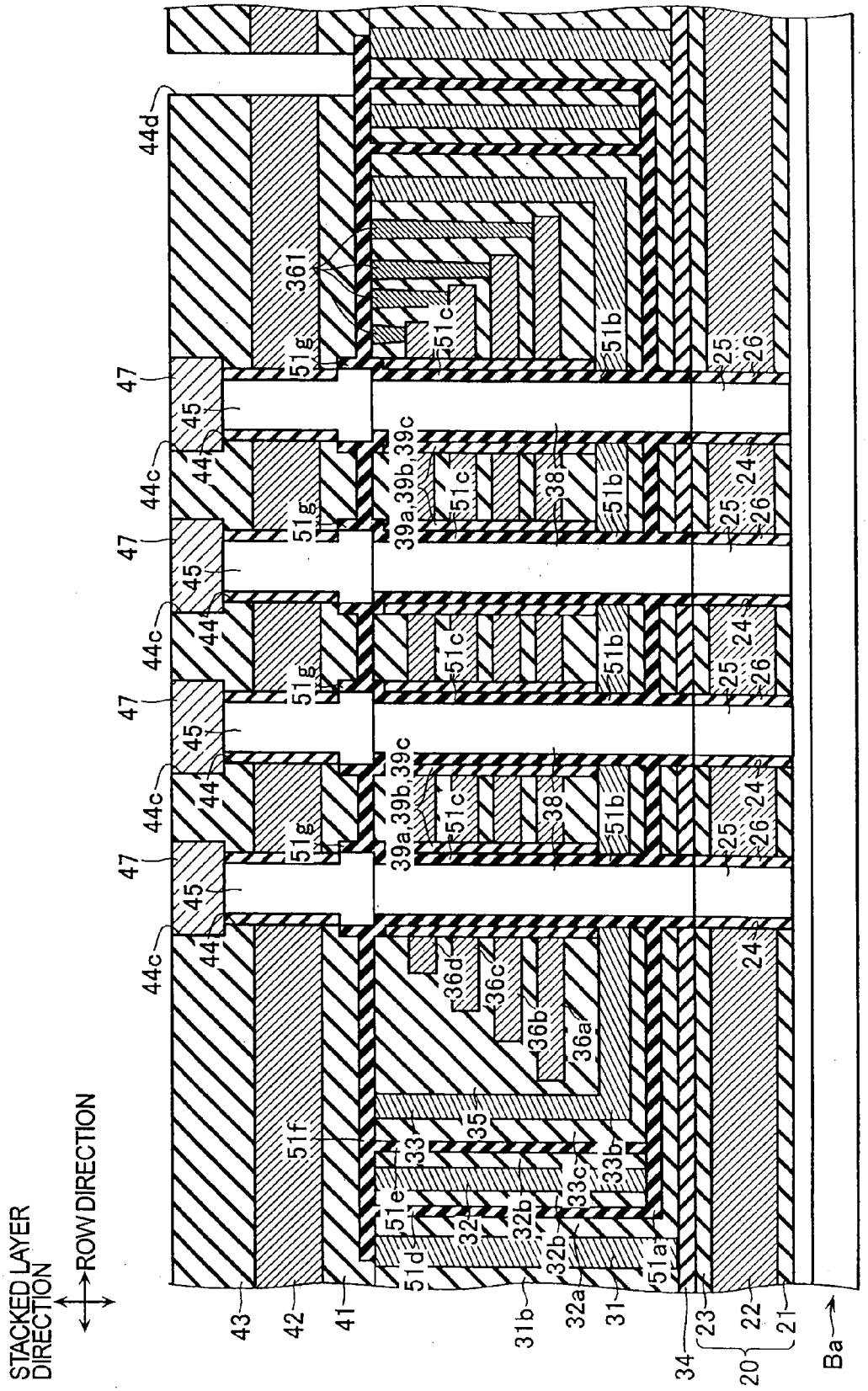

STACKED LAYER DIRECTION
ROW DIRECTION
44d
361
51g
51c
51b
25
26
47
45
44c
44
39a,39b,39c
38
24
51f
36d
36c
36b
36a
35
33
33b
33c
51e
51d
32
32b
32a
31
51a
43
42
41
31b
34
23
22
21
20
Ba

FIG. 27

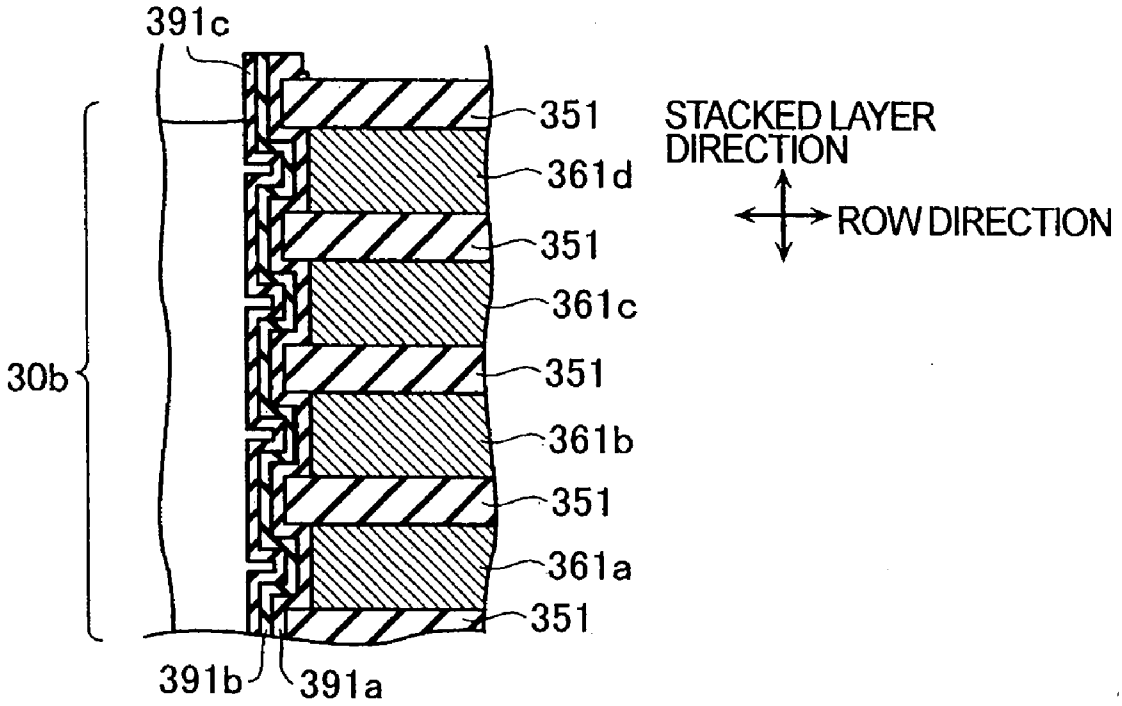

391c
351
361d
351
361c
351
361b
351
361a
351
30b
391b
391a
STACKED LAYER DIRECTION
ROW DIRECTION

FIG. 28

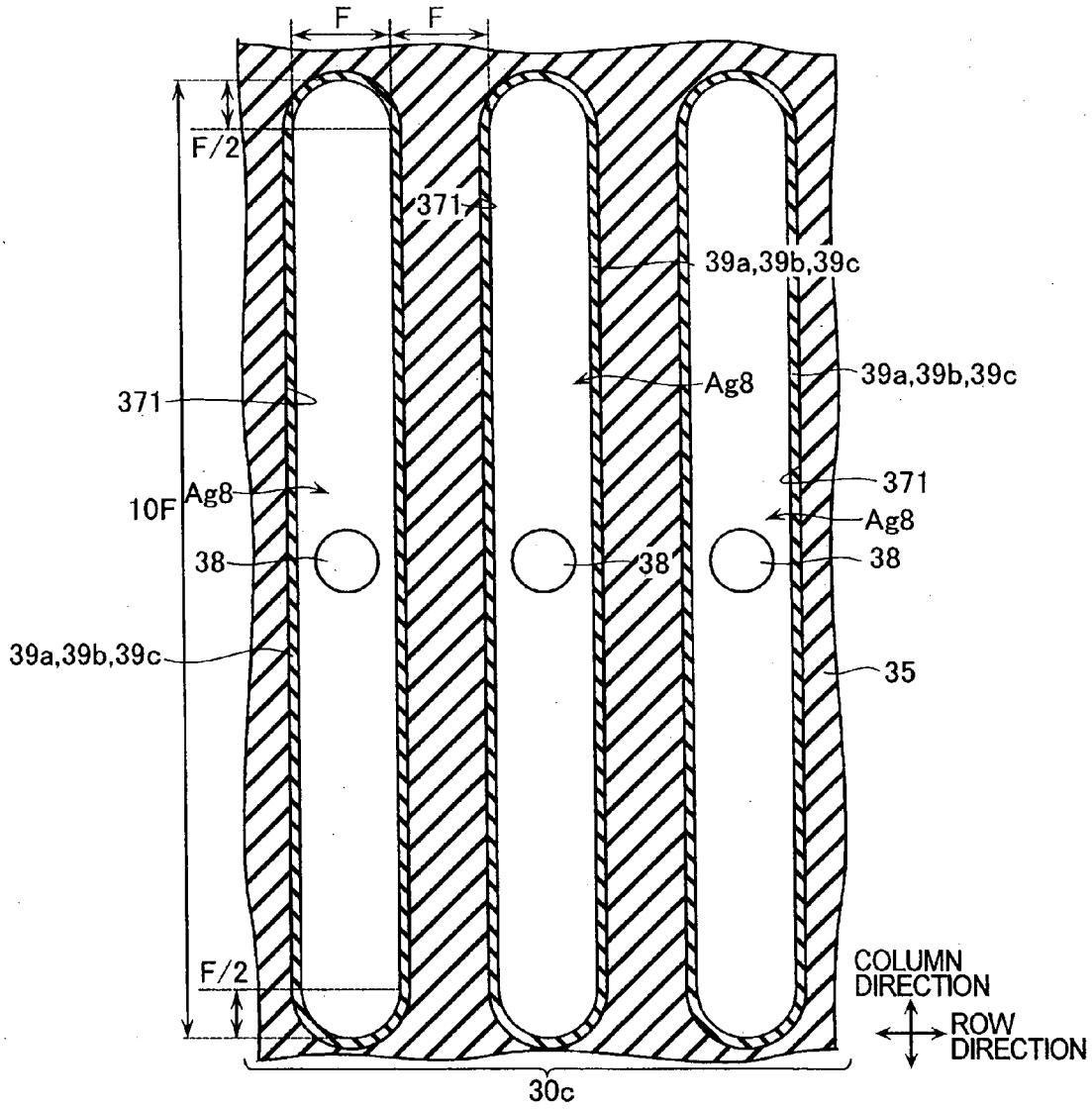

F
F
F/2
371
39a,39b,39c
Ag8
39a,39b,39c
371
371
Ag8
10F
Ag8
38
38
38
39a,39b,39c
35
F/2
COLUMN DIRECTION
ROW DIRECTION
30c

FIG. 29

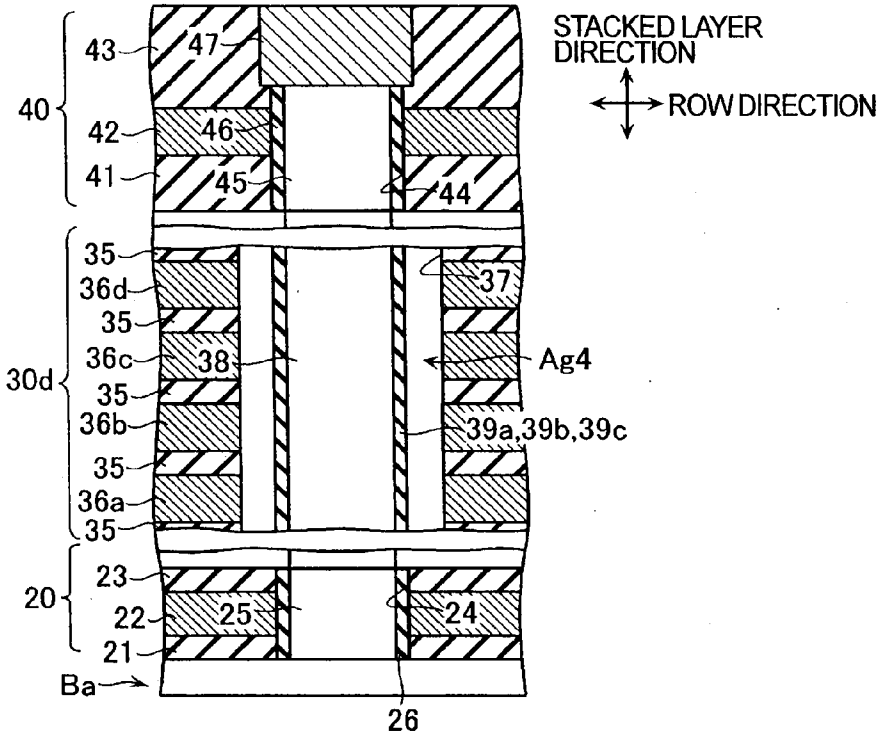

STACKED LAYER DIRECTION
ROW DIRECTION
40
43
47
42
46
41
45
44
30d
35
36d
37
36c
38
Ag4
36b
39a,39b,39c
36a
20
23
22
25
24
21
Ba
26

FIG. 30

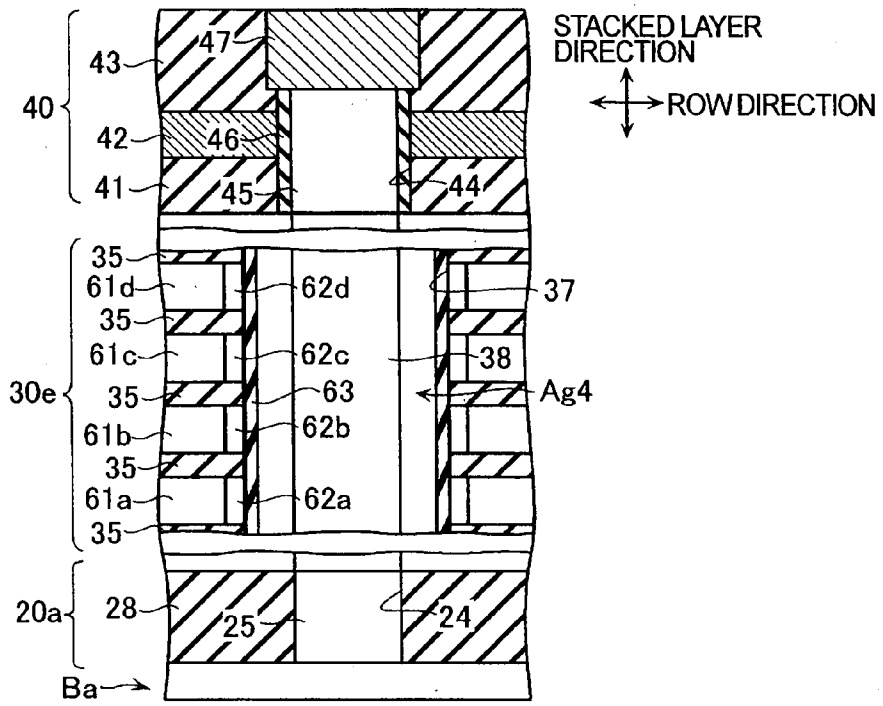

STACKED LAYER DIRECTION
ROW DIRECTION
40
43
47
42
46
41
45
44
30e
35
61d
62d
37
61c
62c
38
63
Ag4
61b
62b
61a
62a
20a
28
25
24
Ba

FIG. 31

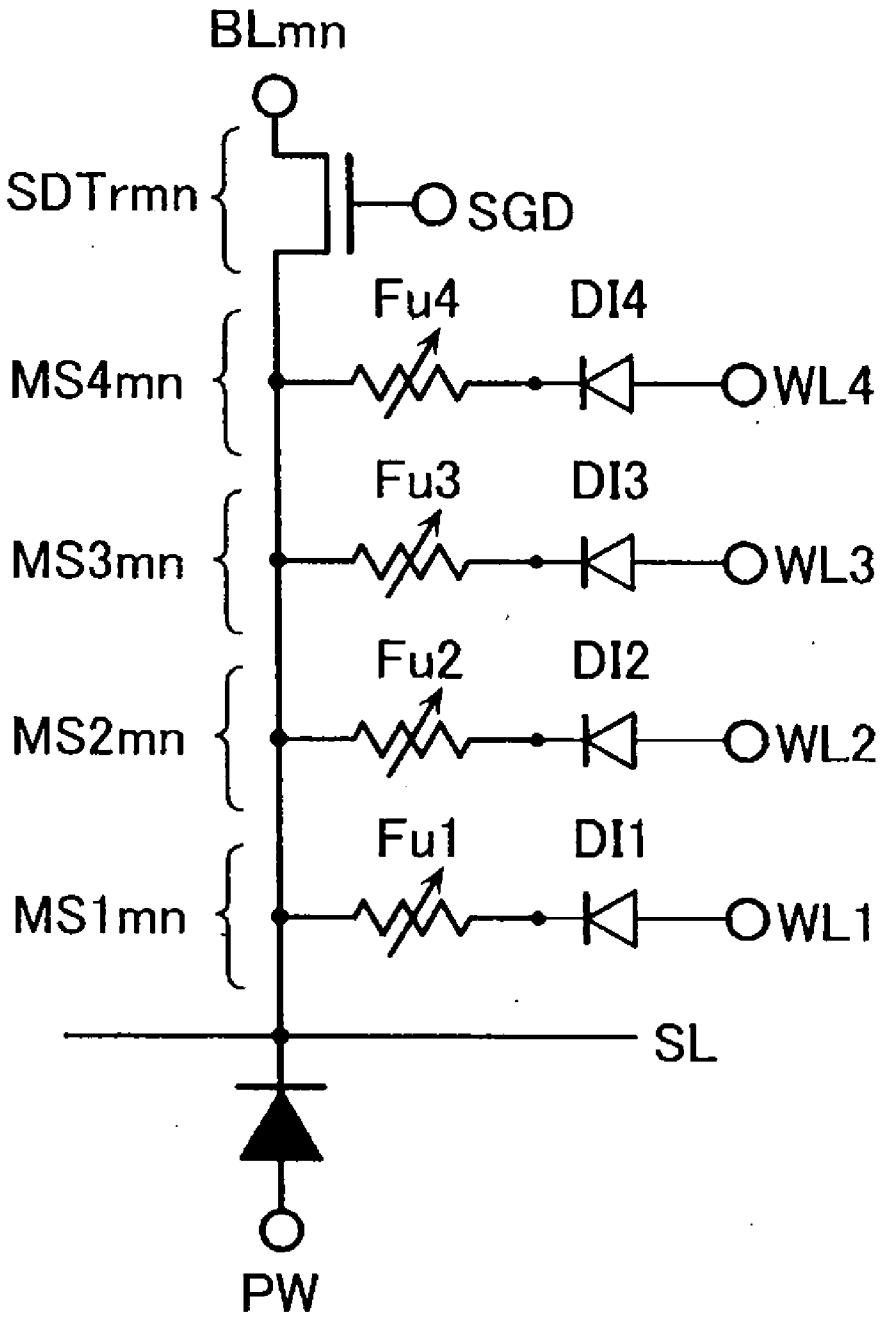

BLmn
SDTrmn
SGD
Fu4
DI4
MS4mn
WL4
Fu3
DI3
MS3mn
WL3
Fu2
DI2
MS2mn
WL2
Fu1
DI1
MS1mn
WL1
SL
PW

FIG. 32

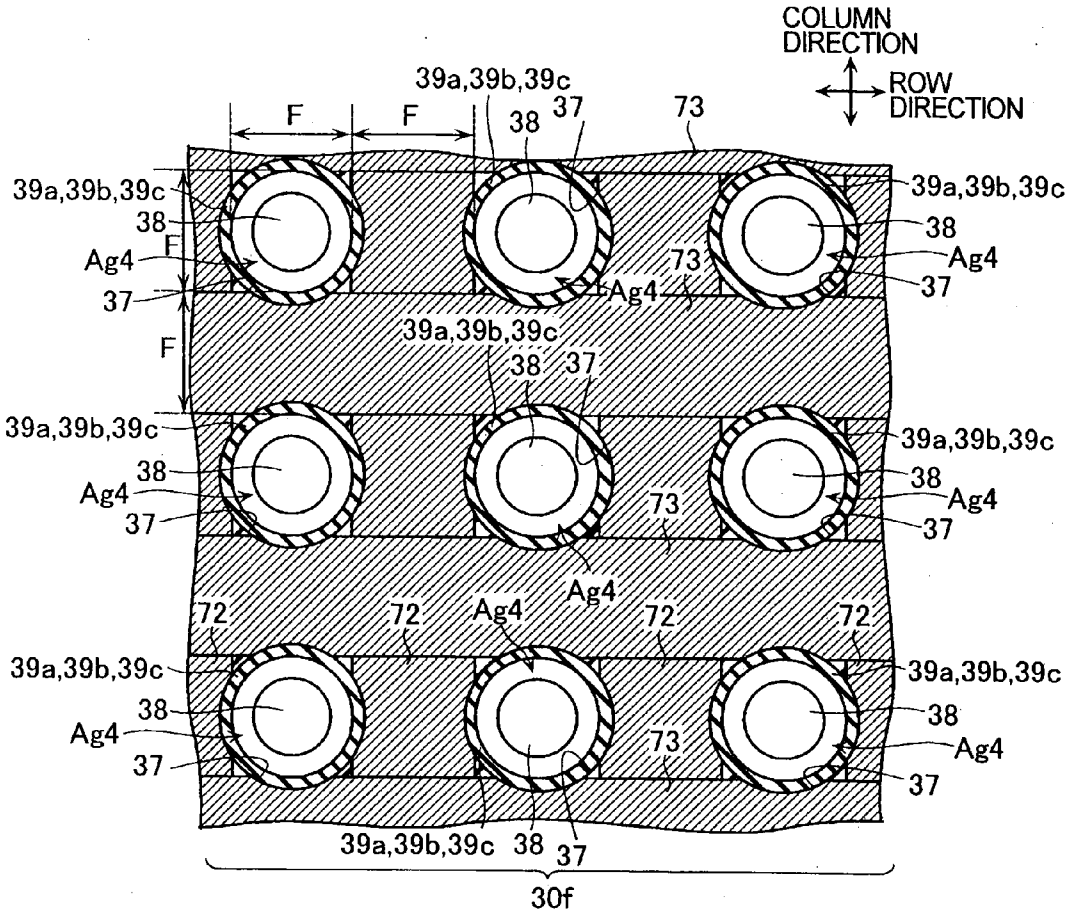

COLUMN DIRECTION
ROW DIRECTION
F
F
39a,39b,39c
38
37
73
Ag4
72
30f

FIG. 33

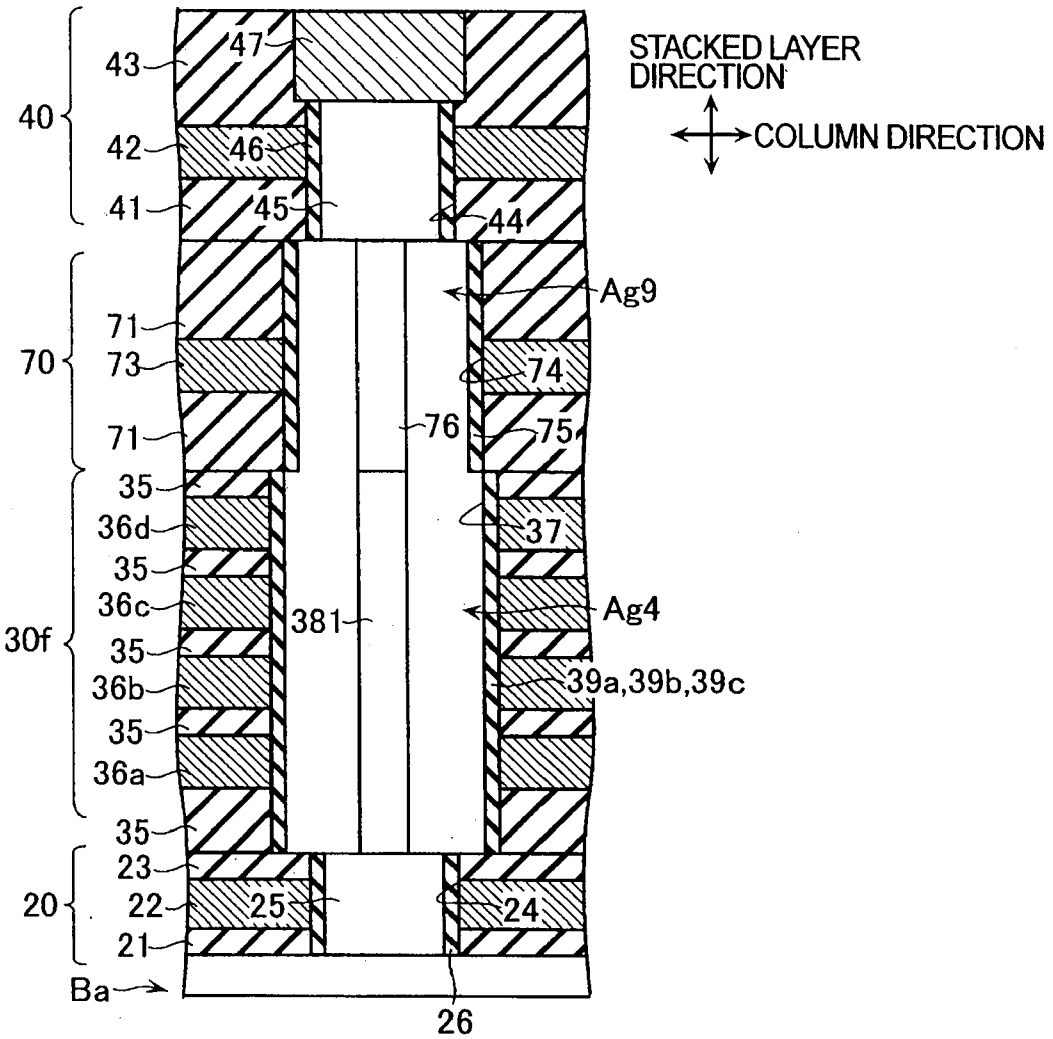

STACKED LAYER DIRECTION
COLUMN DIRECTION
40
43
47
42
46
41
45
44
70
71
73
71
76
74
75
Ag9
30f
35
36d
35
36c
35
36b
35
36a
35
381
37
Ag4
39a,39b,39c
20
23
22
25
21
24
Ba
26

FIG. 34

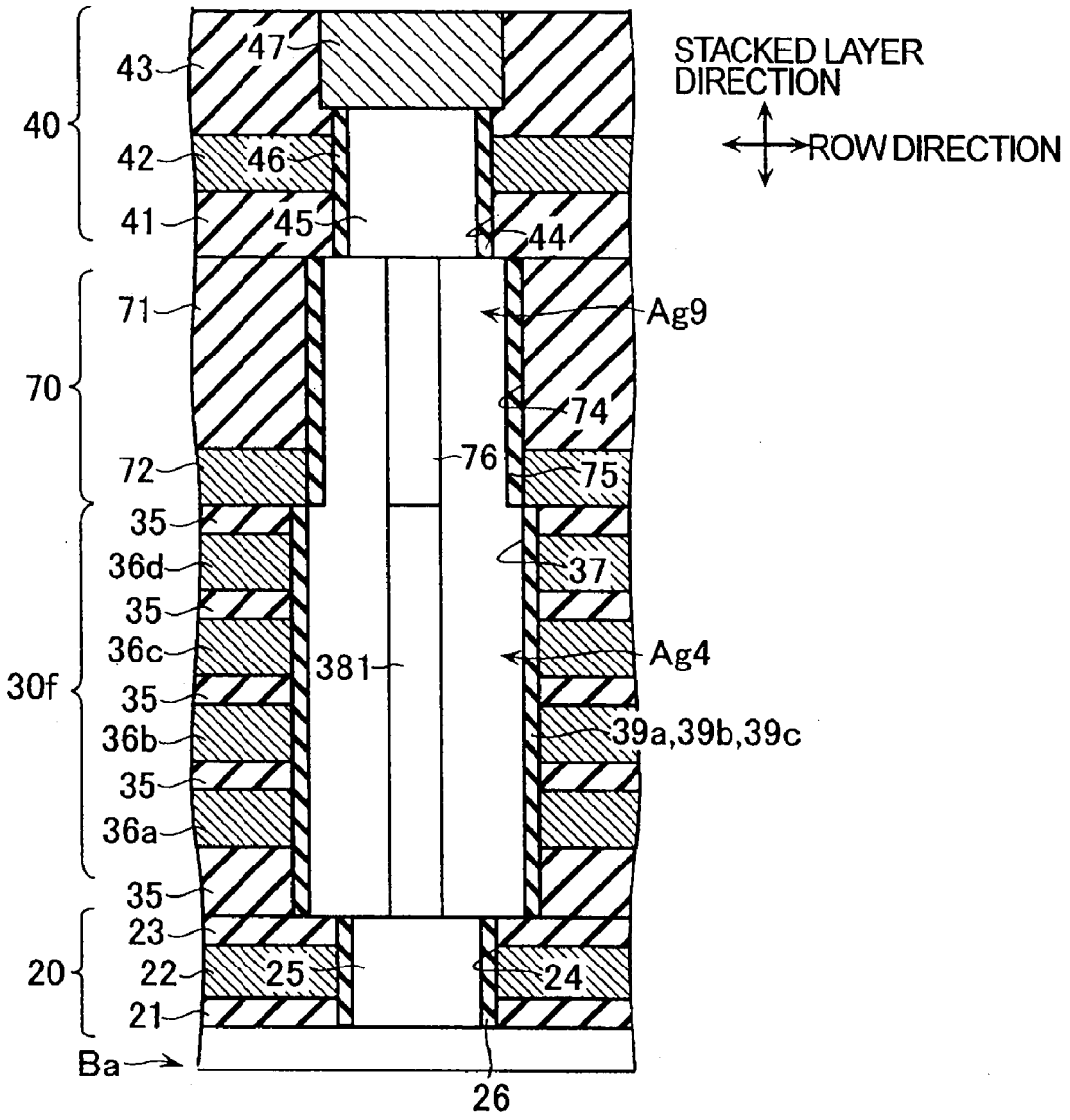

STACKED LAYER DIRECTION
ROW DIRECTION
40
43
47
42
46
41
45
44
70
71
Ag9
74
72
76
75
35
36d
37
35
36c
Ag4
381
30f
35
36b
39a,39b,39c
35
36a
35
20
23
22
25
24
21
Ba
26

FIG. 35

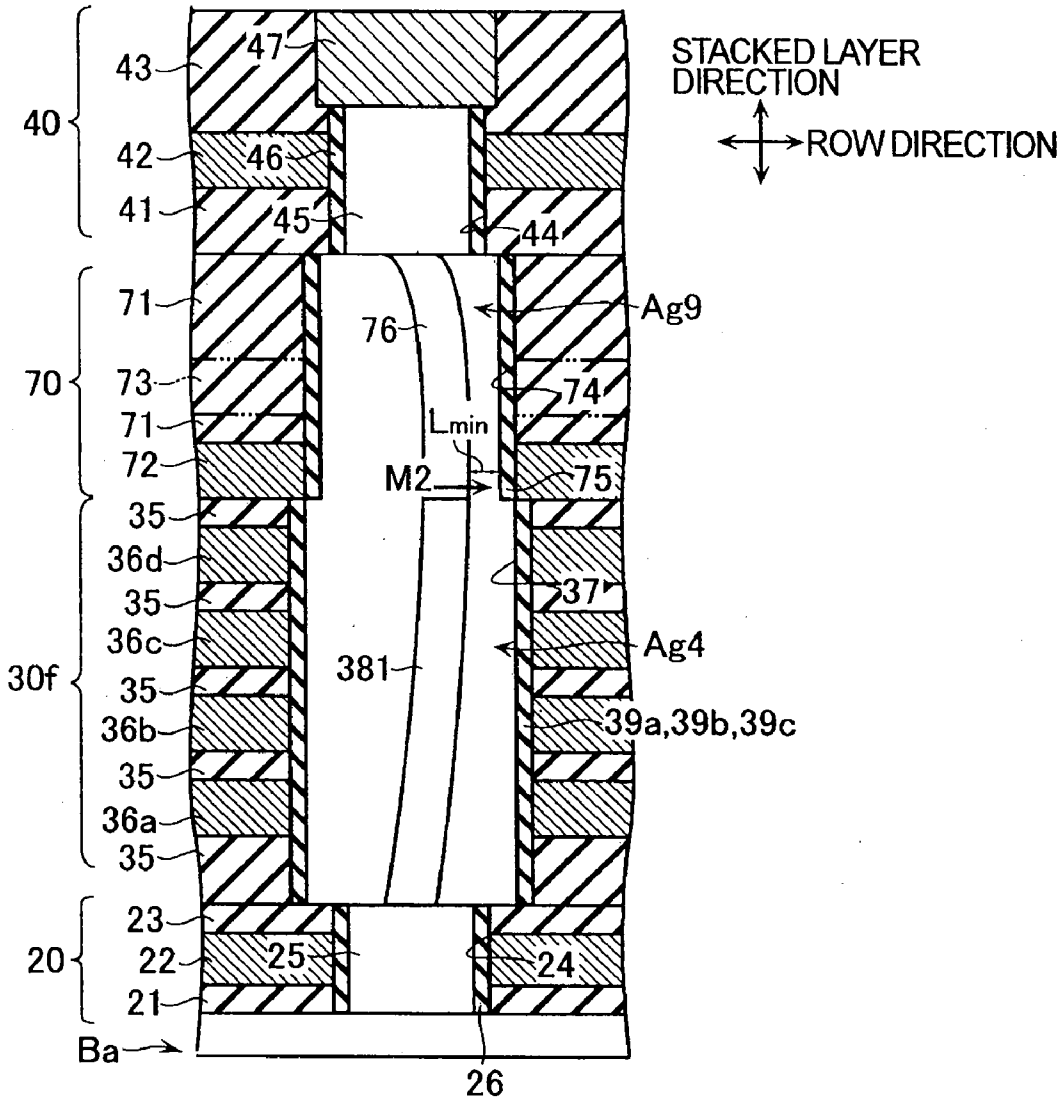

STACKED LAYER DIRECTION
ROW DIRECTION
40
43
47
42
46
41
45
44
70
71
76
Ag9
73
74
71
Lmin
72
M2
75
35
36d
37
35
36c
Ag4
30f
35
381
36b
39a,39b,39c
35
36a
35
20
23
22
25
24
21
Ba
26

FIG. 36

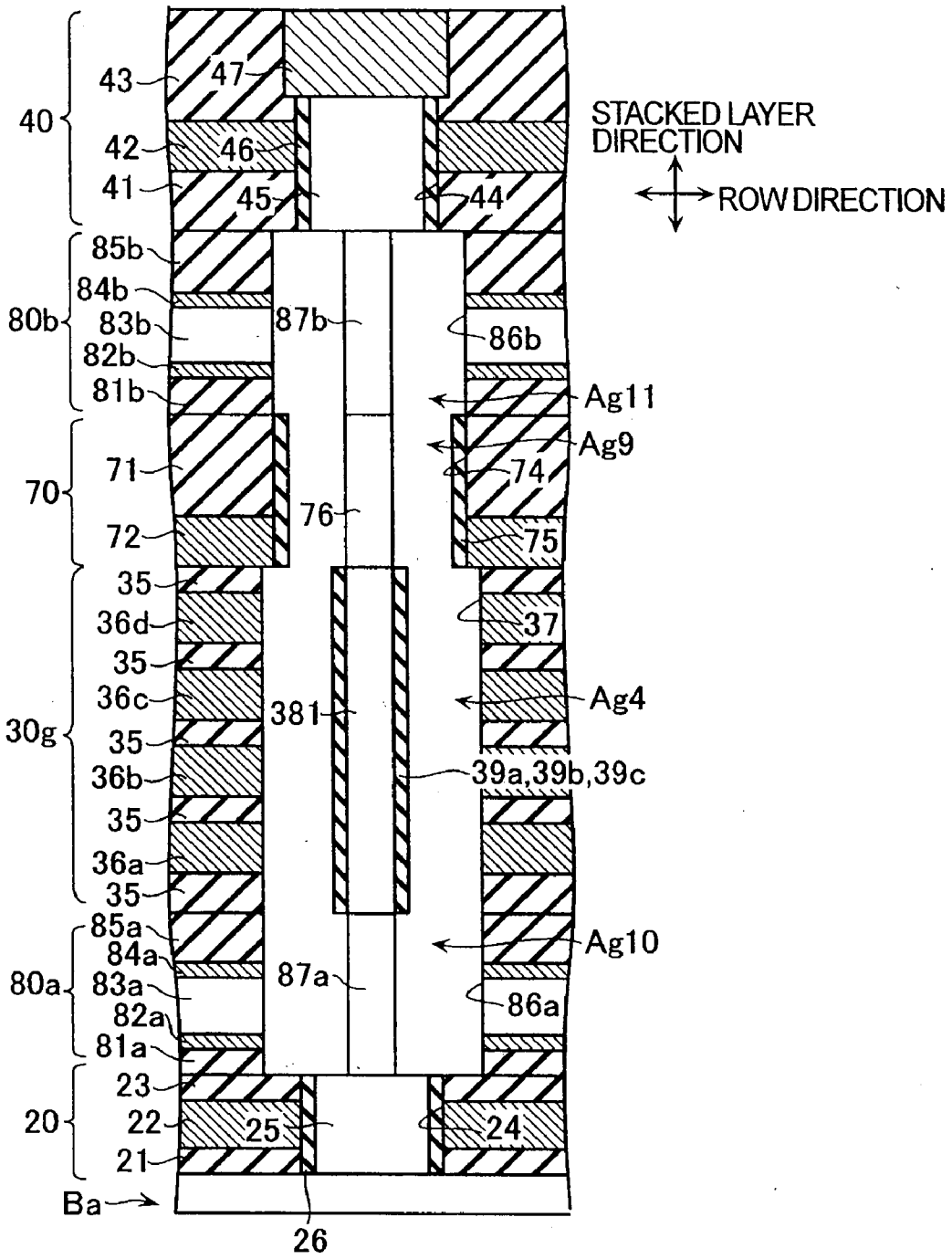

40
43
47
42
46
41
45
44
STACKED LAYER DIRECTION
ROW DIRECTION
80b
85b
84b
83b
82b
81b
87b
86b
Ag11
Ag9
70
71
74
72
76
75
30g
35
36d
37
36c
Ag4
381
36b
39a,39b,39c
36a
80a
85a
84a
83a
82a
81a
87a
Ag10
86a
20
23
22
25
24
21
Ba
26

FIG. 37

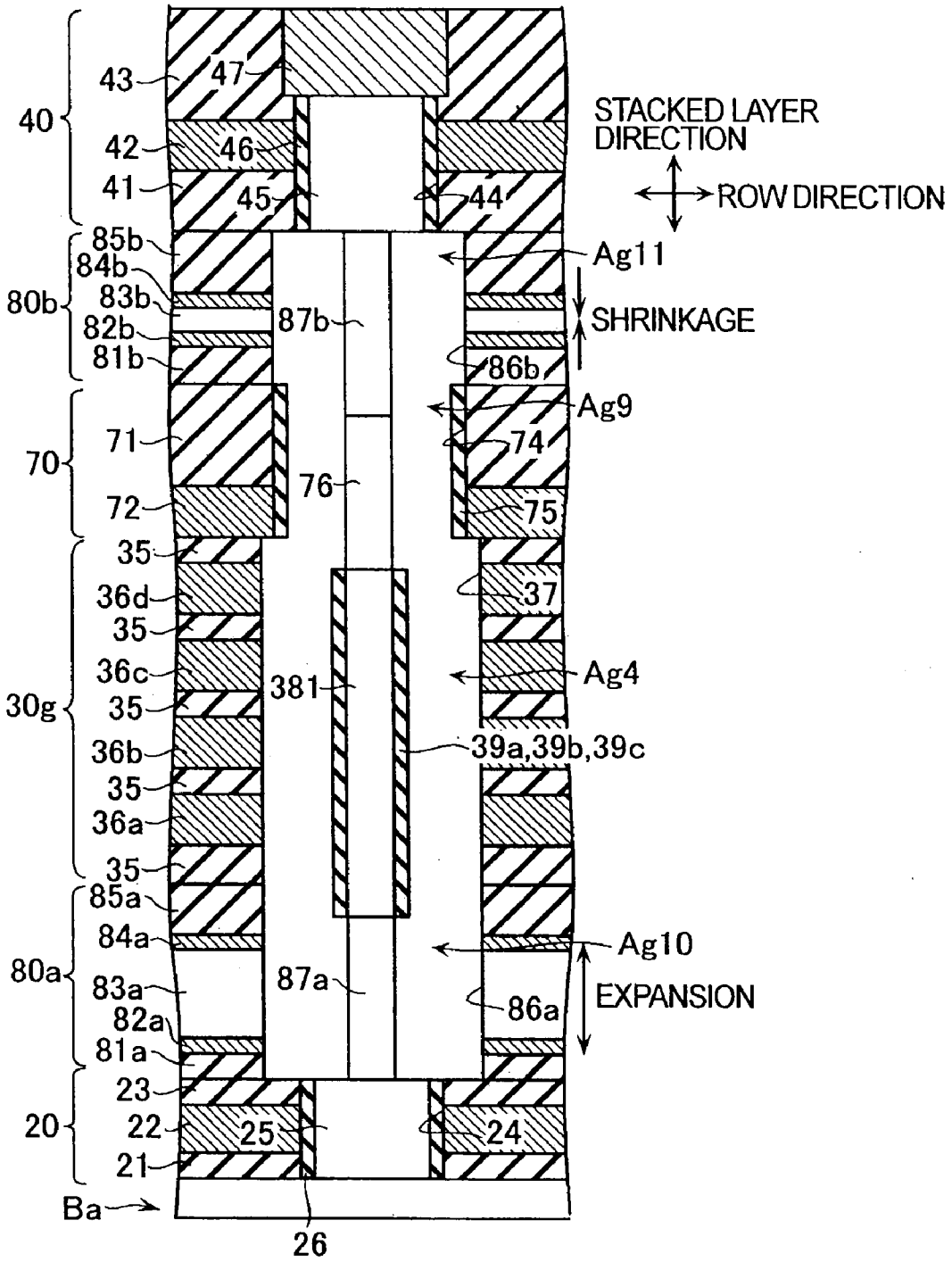

40
43
47
42
46
41
45
44
STACKED LAYER DIRECTION
ROW DIRECTION
85b
84b
83b
82b
81b
80b
87b
Ag11
SHRINKAGE
86b
Ag9
71
74
70
76
72
75
35
36d
37
35
36c
Ag4
381
30g
35
36b
39a,39b,39c
35
36a
35
85a
84a
Ag10
80a
83a
87a
EXPANSION
82a
86a
81a
23
20
22
25
24
21
Ba
26

FIG. 38

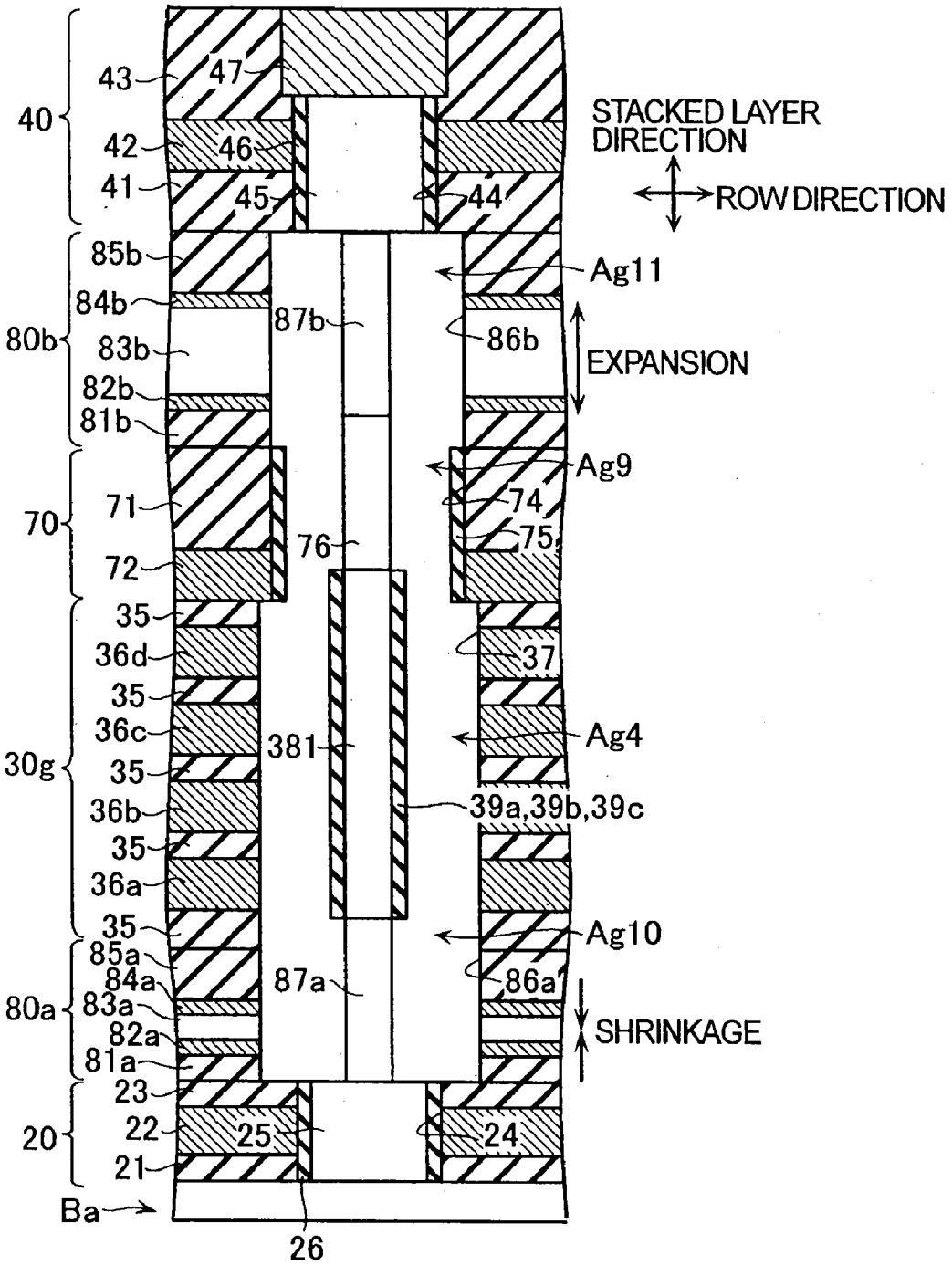

40
43
47
42
46
41
45
44
STACKED LAYER DIRECTION
ROW DIRECTION
85b
Ag11
84b
87b
86b
80b
83b
EXPANSION
82b
81b
Ag9
70
71
74
76
75
72
35
36d
37
35
36c
381
Ag4
30g
35
36b
39a,39b,39c
35
36a
35
Ag10
85a
84a
87a
86a
80a
83a
SHRINKAGE
82a
81a
23
20
22
25
24
21
Ba
26

FIG. 39

SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING SEMICONDUCTOR MEMORY DEVICE

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is based upon and claims the benefit of priority from the prior Japanese Application (No. 2007-311340, filed Nov. 30, 2007), the entire contents of which are incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to an electrically erasable semiconductor memory device and a method for fabricating the electrically erasable semiconductor memory device, and in particular, to a nonvolatile semiconductor memory device and the method for fabricating the nonvolatile semiconductor memory device.

DESCRIPTION OF THE BACKGROUND

[0003] Conventionally, electrical elements have been integrated in a two-dimensional plane of a semiconductor substrate or a semiconductor-on-insulator substrate to form an LSI. A dimension of the element has been miniaturized for increasing a memory capacity in a semiconductor memory device, however, the miniaturization has become increasingly difficult from view point of cost and technology. Therefore, an improvement of photolithography technology is desirable. However, it is anticipated that physical properties such as a breakdown voltage or the like reach to limitation without scaling driving voltage or the like level when the miniaturization is accomplished.

[0004] Recently, various approaches have been studied for highly integrating the semiconductor memory device. For example, employing a multiple-value technique, three-dimensionally stacking memory cells disclosed in Japanese Patent Publication (Kokai) No. 2003-078044, U.S. Pat. No. 5,599,724, U.S. Pat. No. 5,707,885, for example, using MEMS (Micro Electro Mechanical Systems) has been studied. However, it is necessary to overcome many problems for realization the approaches mentioned above. For example, in the case of three-dimensionally stacking memory cells, processing steps in a conventional method are largely increased layer by layer to increase the cost. Further, in a seek-scan type memory device using MEMS, an area of memory storage for retaining data on one bit is fixed by thermal stability or the like so as to limit the memory density.

SUMMARY OF INVENTION

[0005] According to an aspect of the invention, there is provided a nonvolatile semiconductor memory device, comprising a plurality of memory strings, each of the memory strings being constituted with a plurality of electrically erasable memory cells being serially connected each other, the memory strings comprising:

[0006] a columnar semiconductor layer perpendicularly extending for a substrate;

[0007] a plurality of conductive layers being formed in parallel with the substrate and including a first space between sidewalls of the columnar semiconductor layers; and

[0008] a characteristic change layer being formed on the sidewall of the columnar semiconductor layer faced to the first space or a sidewall of the conductive layer faced to the first space, the characteristic change layer changing characteristics accompanying with applied voltage;

[0009] wherein each of the conductive layers has a function as a relative movement to a prescribed direction for the columnar semiconductor layer.

[0010] Further, another aspect of the invention, there is provided a method for fabricating a nonvolatile semiconductor memory device, the nonvolatile semiconductor memory device comprising a plurality of memory strings, each of the memory strings being constituted with a plurality of electrically erasable memory cells being serially connected each other, comprising:

[0011] forming a source-side transistor layer on a semiconductor substrate;

[0012] depositing a silicon-nitride film, a silicon-oxide film, a germanium-silicon film, a silicon-oxide film and a silicon film to form an isolation insulator, a first protective layer, a first sacrifice layer, a second protective layer and a third frame bottom layer on the source-side transistor layer;

[0013] forming a first hole at a portion aligned with the source-side columnar semiconductor layer to pass through the third frame bottom layer, the second protective layer, the first sacrifice layer, the first protective layer and the isolation insulator;

[0014] forming a second sacrifice layer and a first columnar semiconductor layer on a sidewall of the first hole;

[0015] alternately forming a plurality of conductive layers and a plurality of first interlayer insulators on the first columnar semiconductor layer, the second sacrifice layer and the third frame bottom layer;

[0016] forming a second hole at a portion aligned with the first hole to pass through the plurality of the conductive layers and the plurality of the first interlayer insulators, constituting a memory hole with the first hole and the second hole;

[0017] forming the block insulation layer, the charge storage layer, the tunnel insulation layer, the third sacrifice layer and the second columnar semiconductor layer on a sidewall of the second hole in order, constituting a columnar semiconductor layer with the first columnar semiconductor layer and the second columnar semiconductor layer;

[0018] etching the first protective layer, the first sacrifice layer, the third frame bottom layer, the plurality of the conductive layers and the plurality of the first interlayer insulators to form into a shape of stairs;

[0019] forming a second interlayer insulator onto an upper surface of the columnar semiconductor layer;

[0020] forming a first groove onto au upper surface of the isolation insulator to pass through the interlayer insulator;

[0021] forming a second groove, a third groove and a fourth groove onto the first sacrifice layer to pass through the interlayer insulator to form a fourth sacrifice layer, a second frame layer and a fifth sacrifice layer in the second groove, the third groove, the fourth groove, respectively;

[0022] forming a fifth groove onto the third frame bottom layer to pass through the interlayer insulator to form a third frame in the fifth groove;

[0023] forming first-fourth holes by passing through the interlayer insulator onto an upper surface of an end in the row direction the plurality of the conductive layer and forming plug conductive layers in the first-fourth holes;

[0024] forming a sixth sacrifice layer on the first frame layer, a drain-side first insulation layer on the sixth sacrifice layer and first drain-side hole at a portion aligned with the memory hole.

[0025] forming a seventh sacrifice layer **51***g* and a drain-side first columnar semiconductor layer on a sidewall of the first drain-side hole;

[0026] forming a drain-side first insulation layer, a drain-side conductive layer and a drain-side second insulation layer on the drain-side first insulation layer;

[0027] forming a drain-side second hole at s portion aligned with the drain-side first hole to form a drain-side hole constituted with the drain-side first hole and the drain-side second hole;

[0028] forming a drain gate insulation layer and a drain-side second columnar semiconductor layer on a sidewall of the drain-side second hole to form a drain-side columnar semiconductor layer constituted with the drain-side first columnar semiconductor layer and the drain-side second columnar semiconductor layer;

[0029] forming a bit line layer at a portion aligned with the drain-side hole;

[0030] forming a drain-side third hole to a depth of the sixth sacrifice layer; and

[0031] removing the first-seventh sacrifice layers in the third drain-side hole by vapor atmosphere of ClF_3 so as to form a space.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] FIG. **1** is a structure diagram showing a nonvolatile semiconductor memory device according to a first embodiment of the present invention;

[0033] FIG. **2** is a part of a perspective schematic view showing the nonvolatile semiconductor memory device according to the first embodiment of the present invention;

[0034] FIG. **3** is a circuit diagram showing a memory string MS of the nonvolatile semiconductor memory device according to the first embodiment of the present invention;

[0035] FIG. **4** is a cross-sectional schematic view showing a structure of the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0036] FIG. **5** is a plan view showing a memory layer of the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0037] FIG. **6** is an enlarged view of FIG. **4**.

[0038] FIG. **7** is a part of a schematic plain view showing a memory hole of the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0039] FIG. **8**A-**8**B are a cross-sectional schematic view and a plan view showing a mechanism of the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0040] FIG. **9**A-**9**E are a cross-sectional schematic view and plan views showing the mechanism of the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0041] FIG. **10** is a cross-sectional schematic view showing processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0042] FIG. **11** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0043] FIG. **12** is a cross-sectional schematic view showing the processing steps for fabricating the first embodiment of the present invention;

[0044] FIG. **13** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0045] FIG. **14** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0046] FIG. **15** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0047] FIG. **16** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0048] FIG. **17** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0049] FIG. **18** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0050] FIG. **19** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0051] FIG. **20** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0052] FIG. **21** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0053] FIG. **22** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0054] FIG. **23** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0055] FIG. **24** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0056] FIG. **25** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0057] FIG. **26** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0058] FIG. **27** is a cross-sectional schematic view showing the processing steps for fabricating the nonvolatile memory semiconductor device according to the first embodiment of the present invention;

[0059] FIG. **28** is a partially enlarged cross-sectional schematic view showing a nonvolatile memory semiconductor device according to a second embodiment of the present invention;

[0060] FIG. **29** is a part of a plain schematic view showing a memory layer of a nonvolatile memory semiconductor device according to a third embodiment of the present invention;

[0061] FIG. **30** is a part of a cross-sectional schematic view showing a nonvolatile memory semiconductor device according to a fourth embodiment of the present invention;

[0062] FIG. **31** is a part of a cross-sectional schematic view showing a nonvolatile memory semiconductor device according to a fifth embodiment of the present invention;

[0063] FIG. **32** is a circuit diagram showing a memory string of the nonvolatile memory semiconductor device according to the fifth embodiment of the present invention;

[0064] FIG. **33** is a part of a plain schematic view showing a nonvolatile memory semiconductor device according to a sixth embodiment of the present invention;

[0065] FIG. **34** is a part of a cross-sectional schematic view showing the nonvolatile memory semiconductor device according to the sixth embodiment of the present invention;

[0066] FIG. **35** is a part of a cross-sectional schematic view showing the nonvolatile memory semiconductor device according to the sixth embodiment of the present invention;

[0067] FIG. **36** is a cross-sectional schematic view showing a mechanism of the nonvolatile memory semiconductor device according to the sixth embodiment of the present invention;

[0068] FIG. **37** is a part of a cross-sectional schematic view showing a nonvolatile memory semiconductor device according to a seventh embodiment of the present invention;

[0069] FIG. **38** is a cross-sectional schematic view showing a mechanism of the nonvolatile memory semiconductor device according to the seventh embodiment of the present invention;

[0070] FIG. **39** is a cross-sectional schematic view showing the mechanism of the nonvolatile memory semiconductor device according to the seventh embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0071] Embodiments of the present invention will be described below in detail with reference to the drawings mentioned above.

[0072] It is to be noted that the same or similar reference numerals are applied to the same or similar parts and elements throughout the drawings, and the description of the same or similar parts and elements will be omitted or simplified.

First Embodiment

[0073] First, according to a first embodiment of the present invention, a nonvolatile semiconductor memory device is explained device with reference to the drawings.

[0074] (A Structure of the Nonvolatile Semiconductor Memory Device)

[0075] FIG. **1** is a structure diagram showing a nonvolatile semiconductor memory device **100** according to a first embodiment of the present invention;

[0076] As shown in FIG. **1**, the nonvolatile semiconductor memory device **100** according to the first embodiment mainly includes a memory cell region **12**, a word line driving circuit **13**, a source-side selection gate line (SGS) driving circuit **14**, a drain-side selection gate line (SGS) driving circuit **15** and a sense amplifier **16**. The memory cell region **12** includes memory cells memorizing data. The word line driving circuit **13** controls voltage applied to a word line WL. The source-side selection gate line (SGS) driving circuit **14** controls voltage applied to the source-side selection gate line SGS. The drain-side selection gate line (SGS) driving circuit **15** controls voltage applied to a drain-side selection gate line (SGD). The sense amplifier **16** amplifies potential read out from the memory cells. Other than mentioned above, the nonvolatile semiconductor memory device **100** according to the first embodiment includes a bit line driving circuit (not illustrated) controlling voltage applied to a bit line BL and a source line driving circuit (not illustrated) controlling voltage applied to a source line SL (not illustrated).

[0077] Furthermore, in the nonvolatile semiconductor memory device **100** according to the first embodiment, the memory cells constituting the memory cell region **12** are formed by stacking a plurality of semiconductor layers in order. Further, each layer of the word lines WL is two-dimensionally extended in a prescribed area as shown in FIG. **1**. Each layer of the word lines WL has a plane structure of a single layer.

[0078] FIG. **2** is a part of a perspective schematic view showing the memory cell region **12** in the nonvolatile semiconductor memory device **100** according to the first embodiment.

[0079] In the first embodiment, the memory cell region **12** includes m×n numbers (m and n being counting numbers) of memory strings MS being constituted with memory cells MTr**1***mn*-MTr**4***mn*, source-side selection transistors SSTrmn and drain-side selection transistor SDTrmn. In FIG. **2**, m and n equals to three and four, respectively, as an example.

[0080] Each of the word lines WL**1**-WL**4** is connected to each gate of the memory cells MTr**1***mn*-MTr**4***mn* in each of the memory strings MS and each of the word lines WL**1**-WL**4** are formed of the same conductive layer and are common in plane each other. The memory cell MTr**1***mn* in each of the memory strings MS has a structure of a transistor and all gates of memory cells MTr**1***mn* are connected to a word line WL**1**. Further, all gates of memory cells MTr**2***mn* in each of the memory strings MS are connected to a word line WL**2**. Further, all gates of memory cells MTr**3***mn* in each of the memory strings MS are connected to a word line WL**3**. Further, all gates of memory cells MTr**4***mn* in each of the memory strings MS are connected to a word line WL**4**. In the nonvolatile semiconductor memory device **100** according to the first embodiment as shown in FIG. **1** and FIG. **2**, each of the word lines WL**1**-WL**4** is two-dimensionally extended in plane and has the plane structure like a board. Further, each of the word line WL**1**-WL**4** is configured nearly perpendicular to the memory strings MS.

[0081] Each of the memory strings MS includes columnar semiconductors CLmn on a p-well region Ba**1** formed in an n+region of a semiconductor substrate Ba. In FIG. **2**, for example, m equals from 1 to 3 and n equals from 1 to 4. Each of the columnar semiconductors CLmn are formed to perpendicular the semiconductor substrate Ba, and the columnar semiconductors CLmn are displaced like a matrix above the semiconductor substrate Ba and the word lines WL**1**-WL**4**. Thus, the memory strings MS are also displaced like a matrix in a plane perpendicular to the columnar semiconductors CLmn. An insulation layer (not illustrated) and a space (fourth space) Ag**4** are formed between the columnar semiconductors CLmn and the word lines WL**1**-WL**4**. Each of the columnar semiconductors CLmn may be a cylinder column

or a rectangular column. Further, the columnar semiconductor CLmn includes a columnar semiconductor with a shape of stairs.

[0082] Furthermore, as shown in FIG. **2**, the source-side selection gate line SGS constituting a source-side selection transistors SSTrmn is configured under the memory strings MS and contacting the columnar semiconductor CLmn and the insulation layer (not illustrated) via the columnar semiconductor CLmn and the insulation layer (not illustrated). The source-side selection gate line SGS is two-dimensionally extended in plane like the word lines WL**1**-WL**4** and has the plane structure like a board. Moreover, the columnar semiconductor layer CLmn is configured through the source-side selection gate line SGS. In the structure mentioned above, the source-side selection gate line SGS with the plane structure like a board, however, the source-side selection gate line SGS may be formed like a line as like a drain-side selection gate line SGD mentioned later.

[0083] Furthermore, as shown in FIG. **2**, the drain-side selection gate lines SGD constituting the drain-side selection transistor SDTrmn is configured upper the memory strings MS and contacting the columnar semiconductors CLmn and the insulation layer (not illustrated) via the columnar semiconductors CLmn and the insulation layer (not illustrated). In FIG. **2**, the drain-side selection gate lines SGD are illustrated as SGD**1**-SGD**4**. Each of the drain-side selection gate lines SGD is isolated each other. The drain-side selection gate line SGD is formed as a stripe which has a prescribed pitch to the column direction and extended to the row-direction as different for the word lines WL**1**-WL**4**. Furthermore, the columnar semiconductor layers CLmn is configured at a center in the width direction of the drain-side selection gate line SGD formed as the stripe so as to pass through the center. Further, the row-direction means parallel with the semiconductor substrate Ba and orthogonal to the stacked layers. On the other hand, the column direction is orthogonal to the row-direction.

[0084] Next, as reference to FIG. **2** and FIG. **3**, a circuit configuration and a mechanism of the memory strings MS according to the first embodiment are explained. FIG. **3** is a circuit diagram showing the memory strings MS in the nonvolatile semiconductor memory device according to the first embodiment.

[0085] In the first embodiment as shown in FIG. **2** and FIG. **3**, the memory string MS includes four memory cells MTr**1***mn*-MTr**4***mn*, the source-side selection transistors SSTrm and the drain-side selection transistor SDTrmn. These four memory cells MTr**1***mn*-MTr**4***mn*, the source-side selection transistors SSTrm and the drain-side selection transistor SDTrmn are serially connected each other as shown in FIG. **3**.

[0086] FIG. **4** is a cross-sectional schematic view showing a structure of the nonvolatile memory semiconductor device according to the first embodiment. As shown in FIG. **4**, in the first embodiment of the memory strings MS, the columnar semiconductor CLmn is formed on an n+-region formed in a p-type region (p-Well region) Ba**1** of a semiconductor substrate Ba. Thus, source line SL is connected to a source of the source-side selection transistors SSTrmn. The source means the n+-region formed in the p-well region Ba**1** of the semiconductor substrate Ba. Further, the bit line BL is connected to a drain of each of the drain-side selection transistor SDTrmn.

[0087] Each of the memory cells Mtrmn includes the columnar semiconductor CLmn, the insulation layer surrounding the columnar semiconductor CLmn via the space Ag**4** as shown in FIG. **2**, a charge storage layer (not illustrated in FIG. **2** and FIG. **3**) and the word line WL surrounding the insulation layer and the charge storage layer. An end portion of the word line WL contacting with the charge storage layer surrounded by the insulator act as a control gate of the memory cell Mtrmn. A source and a drain of each of the memory cells MTrmn are formed in each of the columnar semiconductors CLmn.

[0088] The source-side selection transistors SSTrmn includes the columnar semiconductor CLmn, the insulation layer surrounding the columnar semiconductor CLmn and the source-side selection gate line SGS surrounding the insulation layer. An end portion of the source-side selection gate line SGS contacting with the insulation layer acts as a control gate of the source-side selection transistors SSTrmn.

[0089] The drain-side selection transistors SDTrmn include the columnar semiconductors CLmn, the insulation layer surrounding the columnar semiconductor CLmn and the drain-side selection gate line SGD surrounding the insulation layer. An end portion of the drain-side selection gate line SGD contacting with the insulation layer acts as a control gate of each of the drain-side selection transistors SDTrmn.

[0090] The nonvolatile semiconductor memory device **100** being constituted with the above mentioned structure is controlled by the bit lines BL**1**-BL**3**, the drain-side selection gate line SGD, the word lines WL**1**-WL**4** and the source-side selection gate line SGS. Voltage of the source line SL is controlled by a bit line driving circuit (not illustrated), the drain-side selection gate line driving circuit **15**, the word line driving circuit **13**, the source-side selection gate line driving circuit **14**, a source line driving circuit (not illustrated) and the bit line driving circuit (not illustrated). Accordingly, reading out data, writing in data and erasing data are performed by controlling electrical charges of the charge storage layer in the prescribed memory cell. Thus, the drain-side selection gate line driving circuit **15**, the word line driving circuit **13**, the source-side selection gate line driving circuit **14**, the source line driving circuit and the bit line driving circuit have a function as control circuits controlling the memory strings MS.

[0091] (A Specific Configuration of the Nonvolatile Semiconductor Memory Device)

[0092] Next, as reference to FIG. **4** and FIG. **5**, a specific configuration of the nonvolatile semiconductor memory device **100** according to the first embodiment is explained.

[0093] As shown in FIG. **4**, the nonvolatile semiconductor memory device **100** (the memory cell strings MS) includes a source-side selection transistor layer **20**, a memory layer **30** and a drain-side selection transistor layer **40** in order from a lower layer towards an upper layer. The source-side selection transistor layer **20** acts as the source-side selection transistors SSTrmn. The memory layer **30** acts as the memory cells Mtrmn. The drain-side selection transistor layer **40** acts as the drain-side selection transistor SDTrmn.

[0094] Furthermore, a first actuator Ac**1** and a second actuator Ac**1** are configured a periphery portion of the memory cells MS. The first actuator Ac**1** and the second actuator Ac**1** are closely explained in FIG. **5**.

[0095] The source-side selection transistor layer **20** includes a first source-side insulation layer **21** formed on the source line layer (acting as the source line SL) of the semiconductor substrate Ba, a source-side conductive layer **22**

formed on the first source-side insulation layer **21** and a second source-side insulation layer **23** formed on the source-side conductive layer **22**.

[0096] Further, the source-side selection transistor layer **20** includes a source-side hole **24** passing through the first source-side insulation layer **21**, the source-side conductive layer **22**, the second source-side insulation layer **23** and a source-side columnar semiconductor layer **25**. A source-side gate insulation layer **26** is formed between a sidewall of the source-side columnar semiconductor layer **25** and the first source-side insulation layer **21**, the source-side conductive layer **22** and the second source-side insulation layer **2**. The source-side columnar semiconductor layer **25** is formed by an amorphous silicon film. The source-side gate insulation layer **26** is formed of silicon-dioxide.

[0097] FIG. **5** is a plan view showing a memory layer of the nonvolatile memory semiconductor device. As shown in FIG. **5**, the memory layer **30** includes a first frame layer **31**, a second frame layer **32** and a third frame layer **33**. The three frames with a rectangular column are formed from the periphery portion towards the memory cell region **12** in order from top view so as to surround the memory cell region **12**. The first frame layer **31**, the second frame layer **32** and the third frame layer **33** are formed of silicon.

[0098] As shown in FIG. **4**, the first frame layer **31** is formed on an isolation insulator **34** on the second source-side insulation layer **23**. As a result, the first frame layer **31** is fixed with the isolation insulator **34**. Further, a first protective layer **31***a* is formed on a sidewall of the first frame layer **31** and an isolation insulator **34***a* at a side of the memory cell region **12**. Further, a periphery insulation layer **31***b* is formed on a sidewall of the first frame layer **31** formed opposite to the memory cell region **12** and on the isolation insulator **34** to be successively formed on the first frame layer **31**. The first protective layer **31***a* and periphery insulation layer **31***b* is formed of silicon-dioxide (SiO_2).

[0099] As shown in FIG. **5**, the second frame layer **32** is connected to the first frame layer **31** via two pairs of first connection layers **32***a* being formed at both sides of the row direction and being extended to the column direction. As shown in FIG. **4**, the second frame layer **32** is configured by the two pairs of the first connection layer **32***a* via a first space Ag**1** formed towards the row direction and the column direction between the first protective layers **31***a*. Further, the second frame layer **32** is configured from the isolation insulator **34** to stacking direction via a second space Ag**2**. Namely, the second frame layer **32** is constructed to relatively move to row direction corresponding to the first frame layer **31** and the isolation insulator **34**. A second protective layer **32***b* is formed on a sidewall of the second frame layer **32**. A second protective layer **32***b* is formed of silicon-dioxide.

[0100] As shown in FIG. **5**, the third frame layer **33** is connected to the second frame layer **32** via two pairs of second connection layers **33***a* being formed at both sides of the row direction and being extended to the row direction. As shown in FIG. **4**, the third frame layer **33** is configured by the two pairs of the second connection layer **33***a* via a third space Ag**3** formed towards the row direction and the column direction between the second frame layers **32**. Further, third frame layer **33** is configured from the isolation insulator **34** to stacking direction via the second space Ag**2**. As shown in FIG. **4**, a third frame bottom layer **33***b* is formed on a bottom of a third frame layer **33** to be extended to an end of the third frame layer **33** in the row direction and the column direction. Namely, the third frame layer **33** is constructed to relatively move to the column direction corresponding to the second frame layer **32**. A third protective layer **33***c* is formed on a sidewall of third frame layer **33** and a lower surface of the third frame bottom layer **33***b*. The third protective layer **33***c* is formed of a silicon-dioxide.

[0101] An interlayer insulator **35** is formed on a top surface of the third frame bottom layer **33**. Further, first-fourth word line conduction layers **36***a*-**36***d* between the interlayer insulators **35** are formed. The first-fourth word line conduction layer layers **36***a*-**36***d* act as the word lines WL**1**-WL**4**. The first-fourth word line conduction layers **36***a*-**36***d* are two-dimensionally extended and an end of the word line conduction layers **36***a*-**36***d* in the row direction is formed as step by step. A plug conductive layer **361** is formed on an end in the row direction of a top surface of the first-fourth word line conduction layers **36***a*-**36***d* to be extended onto a top surface of the memory layer **30**. A wiring (not illustrated) connected to a top surface of a plug conductive layer **361** is put out to a periphery portion through a first connection layer **32***a* and a second connection layer **33***a*. The interlayer insulator **35** is formed of silicon-dioxide. The first-fourth word line conduction layers **36***a*-**36***d* is formed of poly-crystalline silicon.

[0102] As shown in FIG. **5**, the first actuator Ac**1** is configured between the first frame layer **31** and the second frame layer **3**. Further, the second actuator Ac**2** is configured between the second frame layer **32** and the third frame layer **33**. The first actuator Ac**1** forces to displace the second frame layer **32** to the row direction corresponding to the first frame layer **31**. The second actuator Ac**2** forces to displace the third frame layer **33** to the column direction corresponding to the second frame layer **32**. The first actuator Ac**1** and the second actuator Ac**2** is constituted as a comb-like electrostatic type. Further, the first actuator Ac**1** and the second actuator Ac**2** may be constituted with a piezo-type element or a thermal-expansion type element.

[0103] Further, a memory hole **37** is configured at a portion as aligning the source-side columnar semiconductor **25** to pass through the interlayer insulator **35**, the first-fourth word line conduction layers **36***a*-**36***d*, the third frame bottom layer **33***b*, the third protective layer **33***c*, the first protective layer **31***a* and the isolation insulator **34**. A memory **38** is formed at a portion as aligning the source-side columnar semiconductor **25** in the memory hole **37**. The memory **38** is formed of silicon. The fourth space Ag**4** is configured between the memory **38** and a block insulation layer **39***c* mentioned after. The memory **38** is fixed corresponding to the semiconductor substrate Ba.

[0104] FIG. **6** is an enlarged view of FIG. **4**. As shown in FIG. **6**, a block insulation layer **39***a*, a charge storage layer **39***b* and a tunnel insulation layer **39***c* are formed on sidewalls of the first-fourth word line conduction layers **36***a*-**36***d* in the memory hole **37** in order. The block insulation layer **39***a* is formed of silicon-dioxide. The charge storage layer **39***b* is formed of silicon-nitride (SiN). The tunnel insulation layer **39***c* is formed of silicon-dioxide.

[0105] FIG. **7** is a part of schematic plain view showing the memory layer **30** as shown FIG. **4**. As shown in FIG. **4** and FIG. **7**, a diameter of the memory hole **37** is formed to be larger than a diameter of the memory **38**. The fourth space Ag**4** is formed between the memory hole **37** and the memory **38**. For example, the diameter of the memory hole **37** is "F" and the shortest distance between the nearest memory holes **37** is "F". In this condition, R is expressed by $R=\pi F/4F^2\approx 0$.

79/F, where R is a ratio of the circular length of a charge storage layer per area corresponding to an area of the memory hole **37**.

[0106] In other word of the constitution of the memory layer **30**, the first-fourth word line conduction layers **36***a*-**36***d* are formed parallel to the semiconductor substrate Ba and includes the fourth space Ag**4** between the memories **38**. Further, the charge storage layer **39***b* is formed on a sidewall of the first-fourth word line conduction layers **36***a*-**36***d* faced to the fourth space Ag**4**.

[0107] As shown in FIG. **4**, the drain-side selection transistor layer **40** includes a first drain-side insulation layer **41** on the periphery insulation layer **31***b*, a drain-side conductive layer **42** on the first drain-side insulation layer **41**, and a second drain-side insulation layer **43** on the drain-side conductive layer **42**. Here, the drain-side selection transistor layer **40** (first drain-side insulation layer **41**) is formed on the memory layer **30** via a fifth space Ag**5**. The first drain-side insulation layer **41**, the drain-side conductive layer **42** and the second drain-side insulation layer **43** are formed as stripe patterns having a prescribe pitch to the column direction and extending to the row direction. An interlayer insulator is configured to column direction of the first drain-side insulation layer **41**, the drain-side conductive layer **42** and the second drain-side insulation layer **43** formed as stripe patterns (not illustrated). For example, the first drain-side insulation layer **41** and the drain-side second insulation layer **43** are formed of silicon-dioxide. The drain-side conductive layer **42** is formed of silicon. Further, one end of the drain-side conductive layer **42** acts as a control gate of the drain-side selection transistor SDTrmn mentioned above.

[0108] Further, the drain-side selection transistor layer **40** passes through the first drain-side insulation layer **41**, the drain-side conductive layer **42** and the second drain-side insulation layer **43**, to include a drain-side hole **44** and a drain-side columnar semiconductor layer **45** formed in the drain-side hole **44**. A drain-side gate insulation layer **46** is formed between a sidewall of the drain-side columnar semiconductor layer **45** and the first drain-side insulation layer **41**, the drain-side conductive layer **42** and the second drain-side insulation layer **43**. The drain-side columnar semiconductor layer **45** is formed of amorphous silicon. The drain-side gate insulation layer **46** is formed of silicon-dioxide.

[0109] A bit line layer **47** is formed at a portion being aligned with the drain-side columnar semiconductor layer **45** and an upper portion of the drain-side columnar semiconductor layer **45**. The bit line layer **47** acts as the bit line BL as shown in FIG. **2**.

[0110] (A Mechanism of the Nonvolatile Semiconductor Memory Device **100**)

[0111] Next, as reference to FIG. **8** and FIG. **9**, a mechanism of the nonvolatile semiconductor memory device is explained. FIG. **8**A is a cross-sectional schematic view showing the memory strings MS of the nonvolatile memory semiconductor device in normal state, and FIG. **8**A is a plan view showing the memory strings MS of the nonvolatile memory semiconductor device in normal state. FIG. **9**A is a cross-sectional schematic view showing the memory strings MS of the nonvolatile memory semiconductor device when the second frame layer **32** moves and FIG. **9**B-**9**E are plan views showing the memory strings MS of the nonvolatile memory semiconductor device when the second frame layer **32** moves. FIG. **9**B-**9**E show that the memory **38** is moved to approach at a prescribed portion of a sidewall in the opening. Four points in FIG. **9**B-**9**E is shown as an example, therefore, another point can be also applicable.

[0112] On the constitution mentioned above, the second frame layer **32** and a layer formed in the second frame layer **32**, and a layer formed in the third frame layer **33** and the third frame layer **33** are moved to the row direction by the first actuator Ac**1**. The third frame layer **33** and a layer formed in the third frame layer **33** are moved to the column direction by the second actuator Ac**2**.

[0113] As shown in FIG. **8**, in the normal state, the center of the memory **38** being constituted with the memory strings MS is corresponded to the center of the memory hole **37** by the first actuator Ac**1** and the second actuator Ac**2**.

[0114] On the other hand, the third frame layer **33** moves to the column direction and the row-direction (arrow M**1** illustrated in FIG. **9**B) by the first actuator Ac**1** and the second actuator Ac**2**, when writing in data and reading out data. Namely, first-fourth word line conduction layers **36***a*-**36***d* relatively move to the memory **38**. As shown in FIG. **9**A, in the memory string MS, the center of the memory **38** is moved from the center to an eccentric portion in the memory hole **37** accompanying with the movement. In other word, a part of the sidewall of the memory **38** approaches to a part of the charge storage layer **39***b*. Furthermore, as shown in FIG. **9**A, for example, when the fourth word line conduction layer **36***d* is applied to voltage, the memory **38** is performed to write in data into the approached portion of the charge storage layer **39***b* and read out data from the approached portion of the charge storage layer **39***b*. Here, a relative moving distance of the charge storage layer **39***b* corresponding to the memory **38** has a maximum value of approximately 10 nm. As shown in FIG. **9**B-**9**E, writing in data and reading data are performed at the four points of a circular of the charge storage layer **39***b* around the memory hole **37** (fourth space Ag**4**) by changing the moving direction of the first-fourth word line conduction layers **36***a*-**36***d* mentioned above. The portions are related to both the row-direction and the column direction. Furthermore, eight points, sixteen points and another case are also applicable. Data processing can be performed with effectively dividing the circular of the charge storage layer **39***b*.

[0115] (Method for Fabricating the Nonvolatile Semiconductor Memory Device **100** According to the First Embodiment)

[0116] Next, as reference to FIG. **10**-FIG. **26**, it is explained on processing steps for fabricating the nonvolatile semiconductor memory device **100** according to the first embodiment. First, as shown in FIG. **10**, the source-side transistor layer **20** is formed on the semiconductor substrate Ba.

[0117] As shown in FIG. **11**, a silicon-nitride film, a silicon-oxide film, a germanium-silicon (SiGe) film, a silicon-oxide film and a silicon film are deposited to form the isolation insulator **34**, the first protective layer **31***a*, the first sacrifice layer **51***a*, the second protective layer **33***c* and the third frame bottom layer **33***b*.

[0118] As shown in FIG. **12**, the first memory hole **37***a* is formed at a portion being aligned with the source-side columnar semiconductor layer **25** to pass through the third frame bottom layer **33***b*, the second protective layer **33***c*, a first sacrifice layer **51***a*, the first protective layer **31***a* and the isolation insulator **34**.

[0119] As shown in FIG. **13**, a germanium-silicon film and an amorphous silicon film are deposited on a sidewall of the first memory hole **37***a* in order, successively, the germanium-

silicon film and the amorphous silicon film are anisotropically etched to form a second sacrifice layer **51***b* and the first memory **38***a*.

[0120] As shown in FIG. **14**, a silicon-oxide film and a silicon film are alternately deposited on a top surface of the first memory **38***a*, a top surface of the second sacrifice layer **51***b* and a top surface of the third frame bottom layer **33***b*, to form the first-fourth word line conduction layers **36***a*-**36***d* and to form the interlayer insulator **35** on both surfaces of each of the first-fourth word line conduction layers **36***a*-**36***d*.

[0121] As shown in FIG. **15**, the second memory hole **37***b* is formed at a portion being aligned with the first memory hole **37***a* to pass through the first-fourth word line conduction layers **36***a*-**36***d* and the interlayer insulator **35** formed on both surfaces of each of the first-fourth word line conduction layers **36***a*-**36***d*. Further, the memory hole **37** is constituted with both the first memory hole **37***a* and the second memory hole **37***b*.

[0122] As shown in FIG. **16**, a silicon-oxide film, a silicon-nitride film, a silicon-oxide film, a germanium-silicon film and an amorphous silicon film are deposited on the sidewall of the second memory hole **37***b* in order. Subsequently by etching, the block insulation layer **39***a*, the charge storage layer **39***b*, the tunnel insulation layer **39***c*, a third sacrifice layer **51***c* and the second memory **38***b*. The memory **38** is constituted with both the first memory **38***a* and the second memory **38***b*.

[0123] As shown in FIG. **17**, each of the first protective layer **31***a*, the first sacrifice layer **51***a*, the third frame bottom layer **33***b*, the first-fourth word line conduction layers **36***a*-**36***d* and the interlayer insulator **35** are delineated to be formed into a shape of stairs.

[0124] As shown in FIG. **18**, a silicon-oxide film is deposited to a top surface of the memory **38** to form an interlayer insulator **52**.

[0125] As shown in FIG. **19**, a first groove **53***a* is formed onto the isolation insulator **34** to pass through the interlayer insulator **52**. The first groove **53***a* is formed as a rectangle frame surrounding the memory cell region **12** from top view. A silicon film is deposited on the first groove **53***a* to form the first frame layer **31**.

[0126] A second groove **53***b* is formed to pass through the interlayer insulator **52** to a top surface of the first sacrifice layer **51***a*. The second groove **53***b* is formed at nearer side as the memory cell region **12** than the first groove **53***a*, the shape of the second groove **53***b* from top view is formed as a rectangle surrounding the memory cell region **12**. A germanium-silicon film is deposited on the second groove **53***b* to form a fourth sacrifice layer **51***d*.

[0127] A third groove **53***c* is formed to pass through the interlayer insulator **52** to the upper surface of the first sacrifice layer **51***a*. The third groove **53***c* is formed at nearer side as the memory cell region **12** than the second groove **53***b*, the shape of the third groove **53***c* from top view is formed as a rectangle surrounding the memory cell region **12**. A silicon film is deposited on the third groove **53***c* to form the second frame layer **32**.

[0128] A fourth groove **53***d* is formed to pass through the interlayer insulator **52** to the upper surface of the first sacrifice layer **51***a*. The fourth groove **53***d* is formed at nearer side as the memory cell region **12** than the third groove **53***c*, the shape of the fourth groove **53***d* from top view is formed as a rectangle surrounding the memory cell region **12**. A germanium-silicon film is deposited on the fourth groove **53***d* to form a fifth sacrifice layer **51***e*.

[0129] A fifth groove **53***e* is formed to pass through the interlayer insulator **52** to an upper surface of the third frame bottom layer **33***b*. The fifth groove **53***e* is formed at nearer side as the memory cell region **12** than the fourth groove **53***d*, the shape of the fifth groove **53***e* from top view is formed as a rectangle surrounding the memory cell region **12**. A silicon film is deposited on the fourth groove **53***d* to form the third frame **33**.

[0130] Furthermore, each of first-fourth holes **53***f*-**53***i* is formed to pass through the interlayer insulator **52** to an end of each of first-fourth word line conduction layers **36***a*-**36***d* in the row-direction. A silicon film is deposited on the first-fourth holes **53***f*-**53***i* to form the plug conductive layer **361**.

[0131] As shown in FIG. **20**, a sixth sacrifice layer **51***f* is formed on the memory **38** and an upper surface of the first frame layer **31**. Subsequently, a silicon-oxide film is deposited on the sixth sacrifice layer **51***f* to form the drain-side first insulation layer **41**.

[0132] As shown in FIG. **21**, a first drain-side hole **44***a* is formed at a portion being aligned with the memory hole **37** to pass through the drain-side first insulation layer **41** and the sixth sacrifice layer **51***f*.

[0133] As shown in FIG. **22** a germanium-silicon film and a silicon film are deposited on a sidewall of the first drain-side hole **44***a* and the germanium-silicon film and the silicon are anisotropically etched to form a seventh sacrifice layer **51***g* and the drain-side first columnar semiconductor layer **45***a*.

[0134] As shown in FIG. **23**, the drain-side first insulation layer **41** is deposited, subsequently a silicon film and a silicon-oxide film deposited on the drain-side first insulation layer **41** to form the drain-side conductive layer **42** and the drain-side second insulation layer **43**.

[0135] As shown in FIG. **24**, a second drain-side hole **44***b* is formed at a portion being aligned with the drain-side first hole **44***a* to pass through the second drain-side insulation layer **43** and the drain-side conductive layer **42**. The drain-side hole **44** is constituted with both the drain-side first hole **44***a* and the drain-side second hole **44***b*.

[0136] As shown in FIG. **25**, a silicon-oxide film and a silicon film are deposited on a sidewall of the second drain-side hole **44***b* in order to form the drain gate insulation layer **46** and the second drain-side columnar semiconductor layer **45***b* by subsequent etching. The drain-side columnar semiconductor layer **45** is constituted with the drain-side first columnar semiconductor layer **45***a* and the second drain-side columnar semiconductor layer **45***b*.

[0137] As shown in FIG. **26**, a SiO_2 film on the second drain-side insulation layer **43** to further form the second drain-side insulation layer **43** to be thickened.

[0138] As shown in FIG. **27**, a bit line wiring groove **44***c* is formed at a portion being aligned with the drain-side hole **44** to pass through the second drain-side insulation layer **43**. Further, a d third rain-side hole **44***d* is formed to pass through the drain-side second insulation layer **43**, the drain-side conductive layer **42** and the first drain-side insulation layer **41** to a depth of the sixth sacrifice layer **51***f*. A poly-crystalline silicon film is deposited on the bit line wiring groove **44***c* to form the bit line layer **47**.

[0139] After processing steps shown in FIG. **27**, for example, the first-seventh sacrifice layers **51***a*-**51***g* is removed in the drain-side third hole **44***d* by a vapor atmosphere of

ClF_3, the structure of the nonvolatile semiconductor memory device **100** is formed as shown in FIG. **4**. Here, the second space Ag**2** is formed by removing the first sacrifice layer. The fourth space Ag**4** is formed by removing the second sacrifice layer **51***b* and the third sacrifice layer **51***c*. The first space Ag**1** is formed by removing the fourth sacrifice layer **51***d*. The third space Ag**3** is formed by removing the fifth sacrifice layer **51***e*. The fifth space Ag**5** is formed by removing the sixth sacrifice layer **51***f* and the seventh sacrifice layer **51***g*.

[0140] (Effect of the Nonvolatile Semiconductor Memory Device According to the First Embodiment)

[0141] Next, effects of the nonvolatile semiconductor memory device according to the first embodiment are explained. As mentioned above discussion, the nonvolatile semiconductor memory device according to the first embodiment has a capability of highly integrated structure. Further, the nonvolatile semiconductor memory device **100** having each layer of the memory cells MTrmn and the source-side selection transistors SSTrmn and each layer of the drain-side selection transistor SDTrmn can be fabricated by prescribed lithography processing steps without relations to a number of the layers on the word lines WL (word line conduction layer).

[0142] Further, the nonvolatile semiconductor memory device **100** is constituted to be written in data and read out data in a state where the first-fourth word line conduction layers **36***a*-**36***d* are relatively moved to arbitrarily two-dimensional direction (the row direction and the column direction) corresponding to the memory **38**. The nonvolatile semiconductor memory device **100** can execute writing in data and read out data at a plurality of portions on the charge storage layer **39***b*. Each of the portions is configured in the range of the row direction and the column direction. In other words, the nonvolatile semiconductor memory device **100** divides a part of the charge storage layer **39***b* on the circumference by the relative movement mentioned above to enlarge the memory density.

[0143] Further, as a relative movement distance of the charge storage layer **39***b* corresponding to the memory **38** is a maximum value of 10 nm, linearity control of the actuator is not necessary over a longer distance. Accordingly, the first actuator Ac**1** and the second actuator Ac**2** may be simple structures. As the structure can decrease a chip area occupied by the actuators and can lower a cost of the nonvolatile semiconductor memory device.

[0144] As mentioned above, the nonvolatile semiconductor memory device according to the first embodiment of the present invention has an effect of higher integration and lower cost on the nonvolatile semiconductor memory device.

Second Embodiment

[0145] (A Specific Configuration of a Nonvolatile Semiconductor Memory Device According to a Second Embodiment)

[0146] Next, as reference to FIG. **28**, a specific configuration of a nonvolatile semiconductor memory device according to a second embodiment is explained. FIG. **28** is a partially enlarged cross-sectional schematic view showing the nonvolatile memory semiconductor device according to the second embodiment. It is to be noted that the same or similar reference numerals in the second embodiment are applied to the same or similar parts and elements throughout the drawings as the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified.

[0147] The nonvolatile semiconductor memory device according to the second embodiment has difference with a configuration of a memory layer **30***b* as compared to the memory layer **30** in the first embodiment.

[0148] The memory layer **30***b* is different from the memory layer **30** in the first embodiment. A sidewall of first-fourth word line conduction layers **361***a*-**361***d* faced to the fourth space Ag**4** are formed as recesses corresponding to a side wall of an interlayer insulator **351**. Further, surfaces of a block insulation layer **391***a*, a charge storage layer **391***b* and a tunnel insulation layer **391***c* faced to the fourth space Ag**4** (not illustrated) are formed as a concavo-convex shape accompanying with the first-fourth word line conduction layer **361***a*-**361***d*.

[0149] (Effect of the Nonvolatile Semiconductor Memory Device According to the Second Embodiment)

[0150] Next, effects of the nonvolatile semiconductor memory device according to the second embodiment are explained. As mentioned above discussion, the nonvolatile semiconductor memory device according to the second embodiment has the same effects as the nonvolatile semiconductor memory device according to the first embodiment.

[0151] Further, the nonvolatile semiconductor memory device according to the second embodiment, the surfaces of the block insulation layer **391***a*, the charge storage layer **391***b* and the tunnel insulation layer **391***c* are formed as the concavo-convex shape. Thus, as compared to the first embodiment, a contact area between the first-fourth word line conduction layers **361***a*-**361***d* and the memory **38** is decreased. Accordingly, continuing closely contact by excess electrostatic force between the first-fourth word line conduction layers **361***a*-**361***d* and the memories **38** is suppressed to realize more stable relative-movement than the first embodiment.

Third Embodiment

[0152] (A Specific Configuration of a Nonvolatile Semiconductor Memory Device According to a Third Embodiment)

[0153] Next, as reference to FIG. **29**, a specific configuration of a nonvolatile semiconductor memory device according to a third embodiment is explained. FIG. **29** is a part of plain schematic view showing a memory layer of the nonvolatile memory semiconductor device according to the third embodiment. It is to be noted that the same or similar reference numerals in the third embodiment are applied to the same or similar parts and elements throughout the drawings in the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified.

[0154] The nonvolatile semiconductor memory device according to the third embodiment has difference with a configuration of a memory layer **30***c* as compared to the memory layer **30** in the first embodiment.

[0155] The memory layer **30***c* is different from the memory layer **30** in the first embodiment and has a memory hole **371**. The memory hole **371**, as same as the first embodiment, is configured in the first-fourth word line conduction layers **36***a*-**36***d* as shown in FIG. **30**. The memory hole **371** is formed like a slit which has the row-direction as lateral direction and the column direction as longitudinal direction from top view. Both ends of the row direction in the memory hole **371** are formed like a line. On the other hand, the column direction of the memory hole **371** is formed like a circular arc. As a result, an eighth space Ag**8** is configured between a sidewall of the memory hole **371** and a sidewall of the memory **38**. A perim-

eter length ratio R**1** per unit area of the charge storage layer **39***b* faced to the memory hole **371** equals to $(18+\pi)$ F/20F^2 and nearly equals to 1.06/F, where, for example, a length in the row direction of the both end of the memory hole **371** is "F", a length in the column direction of the both end of the memory hole **371** is "10F", the nearest length of the neighbor memory holes **371** is "F" and the diameter of the circular arc in the both end of the memory hole **371** is "F". Further, the ratio R equals to 0.79/F in the first embodiment as mentioned above, thus, the ratio R**1** of the nonvolatile semiconductor memory device according to the third embodiment is a higher value as compared to the ratio of the nonvolatile semiconductor memory device according to the first embodiment.

[0156] (Effect of the Nonvolatile Semiconductor Memory Device According to the Third Embodiment)

[0157] Next, effects of the nonvolatile semiconductor memory device according to the third embodiment are explained. As mentioned above discussion, the nonvolatile semiconductor memory device according to the third embodiment has the same effects as the nonvolatile semiconductor memory device according to the first embodiment.

[0158] Further, the perimeter length ratio R**1** per unit area of the charge storage layer **39***b* faced to the memory hole **371** can be larger than the ratio in the first embodiment by the memory hole **371** of third embodiment. As the perimeter length of the charge storage layer for necessary to stably memorize one bit is constant, the nonvolatile semiconductor memory device in the third embodiment can lead to higher packing memory density than that in the first embodiment by enlarging the perimeter length.

Fourth Embodiment

[0159] (A Specific Configuration of a Nonvolatile Semiconductor Memory Device According to a Fourth Embodiment)

[0160] Next, as reference to FIG. **30**, a specific configuration of a nonvolatile semiconductor memory device according to a fourth embodiment is explained. FIG. **30** is a part of a cross-sectional schematic view showing the nonvolatile memory semiconductor device according to the fourth embodiment. It is to be noted that the same or similar reference numerals in the fourth embodiment are applied to the same or similar parts and elements throughout the drawings in the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified.

[0161] The nonvolatile semiconductor memory device according to the fourth embodiment has difference with a configuration of a memory layer **30***d* as compared to the memory layer **30** in the first embodiment.

[0162] In the memory layer **30***d*, the tunnel insulation layer **39***c*, the charge storage layer **39***b* and the block insulation layer **39***a* are formed in order on a sidewall of the memory **38** instead of the sidewall of the memory hole **37** in the first embodiment.

[0163] (Effect of the Nonvolatile Semiconductor Memory Device According to the Fourth Embodiment)

[0164] Next, effects of the nonvolatile semiconductor memory device according to the fourth embodiment are explained. As mentioned above discussion, the nonvolatile semiconductor memory device according to the fourth embodiment has the same effects as the nonvolatile semiconductor memory device according to the first embodiment. Further, in the nonvolatile semiconductor memory device the fourth embodiment, the block insulation layer **39***a* is exposed to the fourth space Ag**4**. The tunnel insulation layer **39***c* has the thickness thereof being thinner than the thickness of the block insulation layer **39***a* and contacts with the memory **38**. Accordingly, the tunnel insulation layer **39***c* is not damaged accompanying with driving the third frame layer **33** whereas the tunnel insulation layer **39***c* contacts with the memory **38**. Hence, the nonvolatile semiconductor memory device according to the fourth embodiment can raise reliability as compared to that according the first embodiment.

Fifth Embodiment

[0165] (A Specific Configuration of a Nonvolatile Semiconductor Memory Device According to a Fifth Embodiment)

[0166] Next, as reference to FIG. **31**, a specific configuration of a nonvolatile semiconductor memory device according to a fifth embodiment is explained. FIG. **31** is a part of a cross-sectional schematic view showing the nonvolatile memory semiconductor device according to the fifth embodiment. It is to be noted that the same or similar reference numerals in the third embodiment are applied to the same or similar parts and elements throughout the drawings in the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified.

[0167] The nonvolatile semiconductor memory device according to the fifth embodiment has difference with a configuration of a source-side transistor layer **20***a* and a memory layer **30***e* as compared to the memory layer **30** in the first embodiment.

[0168] The source-side transistor layer **20***a* is different from that of the first embodiment. The source-side transistor layer **20***a* has not the source-side conductive layer **22**, on the other hand, has a structure which source-side columnar semiconductor layer **25** is deposited in the source-side hole **24** formed on the source-side fourth insulation layer **28**. In other word, the source-side selection transistors GS is not constituted with the source-side transistor layer **20***a*.

[0169] The memory layer **30***e* includes first-fourth p-type semiconductor layers **61***a*-**61***d* instead of the first-fourth word line conduction layers **36***a*-**36***d*. First-fourth n-type semiconductor layers **62***a*-**62***d* is configured on a sidewall of the first-fourth p-type semiconductor layers **61***a*-**61***d* at the memory hole **37** (fourth space Ag**4**) side. Further, a resistance-change layer **63** is formed to cover the first-fourth n-type semiconductor layers **62***a*-**62***d* and the interlayer insulator **34** formed on a sidewall of the memory hole **37**. The first-fourth p-type semiconductor layers **61***a*-**61***d* and the first-fourth n-type semiconductor layers **62***a*-**62***d* are formed of a poly-crystalline silicon film doped with impurities by plasma doping technique. The resistance-change layer **63** is constituted with titanium-oxide (TiO_2) or nickel-oxide (NiO).

[0170] Further, the resistance-change layer **63** may be constituted with silicon-nitride or silicon-dioxide. Moreover, the memory **38** is formed as an n-type semiconductor, the first-fourth p-type semiconductor layers **61***a*-**61***d* is formed faced to the memory hole **37** (fourth space Ag**4**) and the first-fourth n-type semiconductor layers **62***a*-**62***d* may be omitted. Furthermore, the memory **38** is formed as the p-type semiconductor, the first-fourth p-type semiconductor layers **62***a*-**62***d* is formed as a plane and faced to the memory hole **37** (fourth space Ag**4**) and the first-fourth n-type semiconductor layers **61***a*-**61***d* may be omitted.

[0171] FIG. **32** is a circuit diagram showing a memory string of the nonvolatile memory semiconductor device according to the fifth embodiment. As shown in FIG. **32**, in the nonvolatile semiconductor memory device according to the fifth embodiment, diodes DI**1**-DI**4** are constituted with first-fourth p-type semiconductor layers **61***a*-**61***d* and first-fourth n-type semiconductor layers **62***a*-**62***d*. Further, the resistance-change layer **63** contacting with the first-fourth n-type semiconductor layers **62***a*-**62***d* acts as the resistance-change elements Fu**1**-Fu**4** serially contacting with diodes DI**1**-DI**4**. The nonvolatile semiconductor memory device according to the fifth embodiment is constituted with memory cells MS**1***mn*-MS**4***mn* being connected with the resistance-change elements Fu**1**-Fu**4** and the diodes DI**1**-DI**4**. One end of the memory cell MS**4***mn* is connected to one end of the drain-side selection transistor SDTrmn. The nonvolatile semiconductor memory device according to the fifth embodiment performs reading out, writing in and erasing data by controlling the resistance of the resistance-change layer **63** constituting resistance-change elements Fu**1**-Fu**4** of the prescribed memory cells MS**1***mn*-MS**4***mn*.

[0172] (Effect of the Nonvolatile Semiconductor Memory Device According to the Fifth Embodiment)

[0173] Next, effects of the nonvolatile semiconductor memory device according to the fifth embodiment are explained. As mentioned above discussion, the nonvolatile semiconductor memory device according to the fifth embodiment has the same effects as the nonvolatile semiconductor memory device according to the first embodiment by using the resistance-change elements Fu**1**-Fu**4** as the memory element.

Sixth Fifth Embodiment

[0174] (A Specific Configuration of a Nonvolatile Semiconductor Memory Device According to a Sixth Embodiment)

[0175] Next, as reference to FIGS. **33**-**35**, a specific configuration of the nonvolatile semiconductor memory device according to the sixth embodiment is explained. FIG. **33** is a part of plain schematic view showing the nonvolatile memory semiconductor device according to the sixth embodiment. FIG. **34** is a part of a cross-sectional schematic view showing the nonvolatile memory semiconductor device according to the sixth embodiment. FIG. **35** is a part of a cross-sectional schematic view showing the nonvolatile memory semiconductor device. It is to be noted that the same or similar reference numerals in the sixth embodiment are applied to the same or similar parts and elements throughout the drawings in the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified.

[0176] As shown in FIGS. **33**-**35**, the nonvolatile semiconductor memory device according to the sixth embodiment has difference to a configuration of a memory layer **30***f* as compared to the memory layer **30** in the first embodiment. Further, the nonvolatile memory semiconductor device according to the sixth embodiment includes an electrostatic layer **70** at upper portion (drain-side transistor layer **40**) of the memory layer **30***f*.

[0177] As compared to the nonvolatile semiconductor memory device according the first embodiment, the first space Ag**1**, the second space Ag**2**, the third space Ag**3**, the fifth space Ag**5**, the first-third frame layers **31**-**33** and the third frame bottom layer **33***b* are not formed in the memory layer **30***f*, instead, the interlayer insulator is formed in the memory layer **30***f*. Thus, in the nonvolatile semiconductor memory device according to the sixth embodiment, the memory layer **30***f* does not include the first actuator Ac**1** and the second actuator Ac**2** which are included in the first-fifth embodiments as mentioned above. The memory layer **30***f* is fixed to the source-side transistor layer **20** and the drain-side transistor layer **40**. Further, the memory layer **30***f* includes a memory **381** with flexibility. The memory **381** according to the sixth embodiment has a smaller diameter than that of the first embodiment. Moreover, the memory **381** is constituted with a single-crystalline silicon film epitaxially grown or a germanium-silicon film. The memory **381** has flexibility by the structure mentioned above. The memory **381** may be constituted with another semiconductor with flexibility, for example, a carbon nano-tube with semiconductor properties or the like.

[0178] The electrostatic layer **70** includes a lower wiring layer **72** (as shown in FIG. **35**) and an upper wiring layer **73** (as shown in FIG. **34**) above the memory layer **30***f* via an interlayer insulator **71**. Moreover, the electrostatic layer **70** is formed to contact the drain-side first insulation layer **41** above the most upper portion of the interlayer insulator **71**. The lower wiring layer **72** is formed as a stripe configured by a prescribed pitch in the row-direction and extended in the column direction as shown in FIG. **33**. The upper wiring layer **73** is positioned upper layer than the lower wiring layer **72** as clearly shown in FIG. **33** and FIG. **35** and is formed as a stripe configured by a prescribed pitch in the column direction and extended in the row-direction. An electrostatic hole **74** is formed at a portion to align with the memory hole **37** in the electrostatic layer **70**. The electrostatic hole **74** is a smaller diameter than a diameter of the memory hole **37**. A sidewall insulation layer **75** made of poly-crystalline silicon is formed on a sidewall of the electrostatic hole **74**. Further, an electrostatic columnar semiconductor layer **76** is formed at an upper portion of the memory **381**. The electrostatic columnar semiconductor layer **76** is configured to form a ninth space Ag**9** between the electrostatic columnar semiconductor layer **76** and the sidewall insulation layer **75**. The electrostatic columnar semiconductor layer **76** has a diameter which nearly equal to a diameter of the memory **381**. The drain-side columnar semiconductor layer **45** is connected to the upper surface of the electrostatic columnar semiconductor layer **76**. The electrostatic columnar semiconductor layer **76** is constituted with a silicon single-crystalline film epitaxially grown or germanium-silicon (SiGe) film. The electrostatic layer **70** has a function deforming the memory **381** to a prescribed direction corresponding to the electrostatic columnar semiconductor layer **76** and the memory **381** by using electrostatic force.

[0179] (A Mechanism of the Nonvolatile Semiconductor Memory Device According to the Sixth Embodiment)

[0180] Next, as reference to FIG. **36**, a mechanism of the nonvolatile semiconductor memory device according to the sixth embodiment is explained. As shown in FIG. **36**, in the nonvolatile semiconductor memory device according to the sixth embodiment, electric field is generated on the sidewall insulation layer **75** by applying voltage to the lower wiring layer **72** and the upper wiring layer **73**. Electrostatic force is generated between a sidewall of the electrostatic columnar semiconductor layer **76** and a sidewall of the opposite sidewall insulation layer **75** by the voltage. Namely, a memory **381** (electrostatic columnar semiconductor layer **76**) is bended to prescribed row direction and column direction which is shown as an arrow M**2** in FIG. **36** by electrostatic

force accompanying with applied voltage between the lower wiring layer **72** and the upper wiring layer **73**. A distance between the column direction electrostatic columnar semiconductor layer **76** and the sidewall insulation layer **75**, and another distance between the memory **381** and the tunnel insulation layer **39***c* relatively becomes the shortest distance L_{min} as compared to other positions in the row direction and the column direction.

[0181] Successively applying voltage to the electrostatic layer **70**, voltage is applied to the word line being connected to memory cells for reading out and writing in. Here, the word line is set to the fourth word line conduction layer **36***d*. As the distance between the memory **381** and the tunnel insulation layer **39***c* is the shortest distance L_{min}, the memory **381** is further bended to the prescribed row direction and column direction constituting the shortest distance L_{min}'. Successively, voltage is applied to a third word line conduction layer **36***c*, a second word line conduction layer **36***b* and a first word line conduction layer **36***a* as same as a fourth word line conduction layer **36***d*. The memory **381** (electrostatic columnar semiconductor layer **76**) is bended to the prescribed row direction and column direction. By behavior mentioned above, the whole memory **381** is moved to the prescribed row direction and column direction. As shown in FIG. **36**, the charges in the charge storage layer **39***b* are controlled to perform writing in data, erasing data and reading out data in a state which the memory **381** is bended.

[0182] (Effect of the Nonvolatile Semiconductor Memory Device According to the Sixth Embodiment)

[0183] Next, effects of the nonvolatile semiconductor memory device according to the sixth embodiment are explained. As mentioned above discussion, the nonvolatile semiconductor memory device according to the sixth embodiment has the same effects as the nonvolatile semiconductor memory device according to the first embodiment. Further, the first actuator Ac**1** and the second actuator Ac**2** like as the first-fifth embodiments are not necessary in the nonvolatile semiconductor memory device according to the sixth embodiment. As the nonvolatile semiconductor memory device according to the sixth embodiment can be omitted the first-third frame layers **31-33** to be able to further highly integrate as compared to the first embodiment-fifth the embodiments.

[0184] Moreover, in the nonvolatile semiconductor memory device according to sixth the embodiment, each of the memories **381** can be bended by driving specific lower wiring layer **72** and upper wiring layer **73**. As a result, a problem of contact faulty between the memory **381** and the charge storage layer **39***b* can be suppressed. The faulty may be generated in a state, for example, which the memory **381** fully cannot approach to the charge storage layer **39***b* or the memory **381** is pressed to the charge storage layer **39***b* by excess forth. Further, the nonvolatile semiconductor memory device without the actuator and the frame layer according to the sixth embodiment can realize lower cost as compared to the first-fifth embodiments.

[0185] Further, in the nonvolatile semiconductor memory device according to the sixth embodiment, the memory **381** and the electrostatic columnar semiconductor layer **76** is constituted with a silicon single-crystalline film epitaxially grown or a germanium-silicon (SiGe) film. By the constitution, the memory **381** and the electrostatic columnar semiconductor layer **76** is formed to have comparatively uniform mechanical characteristics as compared to a constitution by a poly-crystalline body such as poly-crystalline silicon. Accordingly, the electrostatic layer **70** is driven as a lower voltage and the memories in the columnar semiconductor layer **381** and the electrostatic columnar semiconductor layer **76** are bended by high reliability.

Seventh Embodiment

[0186] (A Specific Configuration of a Nonvolatile Semiconductor Memory Device According to a Seventh Embodiment)

[0187] Next, as reference to FIG. **37**, a specific configuration of a nonvolatile semiconductor memory device according to a seventh embodiment is explained. FIG. **37** is a part of a cross-sectional schematic view showing the nonvolatile memory semiconductor device according to the seventh embodiment. It is to be noted that the same or similar reference numerals in the seventh embodiment are applied to the same or similar parts and elements throughout the drawings in the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified.

[0188] As shown in FIG. **37**, the nonvolatile semiconductor memory device according to the seventh embodiment has difference with a configuration of a memory layer **30***g* as compared to the memory layer **30** in the first embodiment. Further, the nonvolatile semiconductor memory device according to the seventh embodiment includes a lower driving layer **80***a* and an upper driving layer **80***b* in addition to the constitution of the sixth embodiment. The lower driving layer **80***a* is formed between the source-side transistor layer **20** and a memory layer **30***g*. The upper driving layer **80***b* is formed between the electrostatic layer **70** and the drain-side transistor layer **40**.

[0189] The memory layer **30***g* in which a tunnel insulation layer **39***c*, a charge storage layer **39***b* and a block insulation layer **39***a* are stacked in order is formed on a sidewall of the memory **381**, on the other hand, the memory layer is formed on the memory hole **37** in the sixth embodiment.

[0190] The lower driving layer **80***a* has an lower first insulation layer **81***a*, an lower first electrode layer **82***a*, a piezo element film **83***a*, a lower second electrode layer **84***a* and an lower second insulation layer **85***a* which are stacked on the source-side second insulation layer **23** in order. The lower second insulation layer **85***a* is formed to contact with the lowest interlayer insulator **35** in the memory layer **30***f*. The lower first electrode layer **82***a* and lower second electrode layer **84***a* are constituted with, for example, an Al film or a TiN film. The piezo element film **83***a* is constituted with, for example, (Pb, Zr)TiO3 or AlN.

[0191] A lower driving hole **86***a* is formed at a portion aligned with the source-side hole **24** in the lower driving layer **80***a* to pass through the lower second insulation layer **85***a*, the lower second electrode layer **84***a*, the piezo element film **83***a*, the lower first electrode layer **82***a* and the lower first insulation layer **81***a*. A lower columnar semiconductor layer **87***a* is formed in the lower driving hole **86***a*. The lower columnar semiconductor layer **87***a* has the same diameter as that of the memory **381**. An under surface of the lower columnar semiconductor layer **87***a* is formed to contact with an upper surface of the source-side columnar semiconductor layer **25**. An upper surface of the lower columnar semiconductor layer **87***a* is formed to contact with an under surface of the memory **381**. Further, a tenth space Ag**10** is formed between a sidewall of the lower driving hole **86***a* and a sidewall of the lower columnar semiconductor layer **87***a*.

[0192] The upper driving layer **80***b* includes an upper first insulation layer **81***b*, an upper first electrode layer **82***b*, a piezo element film **83***b*, an upper second electrode layer **84***b*, and an upper second insulation layer **85***b* which are stacked on the electrostatic layer **70** in order. The upper second insulation layer **85***b* is formed to contact to a lower portion of the drain-side first insulation layer **41**. The upper first electrode layer **82***b* and the upper second electrode layer **84***b* are constituted with, for example, an Al film or a TiN film. The piezo element film **83***b*, for example, is constituted with (Pb, Zr)TiO3 or AlN.

[0193] Further, an upper driving hole **86***b* is formed at a portion aligned with the electrostatic hole **74** in the upper driving layer **80***b* to pass through the upper second insulation layer **85***b*, the upper second electrode layer **84***b*, the piezo element film **83***b*, the upper first electrode layer **82***b*, and the upper first insulation layer **81***b*. The upper columnar semiconductor layer **87***b* is formed in the upper driving hole **86***b*. The upper columnar semiconductor layer **87***b* has the same diameter as that of the electrostatic columnar semiconductor layer **76**. An under surface of the upper columnar semiconductor layer **87***b* is formed to contact with an upper surface of the electrostatic columnar semiconductor layer **76**. An upper surface of the upper columnar semiconductor layer **87***b* is formed to contact with an under surface of the drain columnar semiconductor layer **45**. Further, an eleventh space Ag**11** is formed between a sidewall of the upper driving hole **86***b* and a sidewall of the upper columnar semiconductor layer **87**.

[0194] (A Mechanism of the Nonvolatile Semiconductor Memory Device According to the Seventh Embodiment)

[0195] Next, as reference to FIG. **38** and FIG. **39**, a mechanism of the nonvolatile semiconductor memory device according to the seventh embodiment is explained. As shown in FIG. **38**, piezo element film **83***a* is expanded by applying a prescribed voltage to the lower first electrode **82***a* and the lower second electrode **84***a*. On the other hand, the piezo element film **83***b* is shrinked by applying a prescribed voltage to the upper first electrode **82***b* and the upper second electrode **84***b* as shown in FIG. **38**. In this way, the word line conduction layers from the first word line conduction layer **36***a* to the fourth word line conduction layer **36***d* relatively move to upper side corresponding to the charge storage layer **39***b* and the memory.

[0196] As shown in FIG. **39**, the piezo element film **83***a* is shrinked by applying a prescribed voltage to the upper first electrode **82***a* and the upper second electrode **84***a*; on the other hand, piezo element film **83***b* is expanded by applying a prescribed voltage to the upper first electrode **82***b* and the upper second electrode **84***b*. In this way, the word line conduction layers from the first word line conduction layer **36***a* to the fourth word line conduction layer **36***d* relatively moved to lower side corresponding to the charge storage layer **39***b* and the memory **381**.

[0197] As shown in FIG. **38** or FIG. **39** mentioned above, the word line conduction layers from the first word line conduction layer **36***a* to the fourth word line conduction layer **36***d* are moved to lower side and upper side corresponding to the memory **381**, successively the memory **381** is bended as the same as the sixth embodiment. Namely, the word line conduction layers from the first word line conduction layer **36***a* to the fourth word line conduction layer **36***d* relatively move to the row-direction, the column direction, and the stacking direction corresponding to the charge storage layer **39***b*. Further, when the first-fourth word line conduction layers **36***a*-**36***d* are applied voltage, data are performed to be read out and to be written in the portion of the charge storage layer **39***b* approach to the first-fourth word line conduction layers **36***a*-**36***d*. Writing in data and reading out data are performed in a plurality of positions of the charge storage layer **39***b* around the memory hole **37** (fourth space Ag**4**) by changing the movement direction of the first-fourth word line conduction layers **36***a*-**36***d* and the bending direction of the memory **381**. The positions can be set at the row direction, the column direction and the stacking direction.

[0198] (Effect of the Nonvolatile Semiconductor Memory Device According to the Seventh Embodiment)

[0199] Next, effects of the nonvolatile semiconductor memory device according to the seventh embodiment are explained. As mentioned above discussion, the nonvolatile semiconductor memory device according to the seventh embodiment has the same effects as the nonvolatile semiconductor memory device according to the first embodiment. In the nonvolatile semiconductor memory device according to the seventh embodiment, the first-fourth word line conduction layers **36***a*-**36***d* have capability of relative movement to upper and lower direction in addition to the row direction and the column direction corresponding to charge storage layer **39***b*. In this way, in the nonvolatile semiconductor memory device according to the seventh embodiment, writing in data and reading out data can be performed in the plurality of the positions of the charge storage layer **39***b*. The positions can be set at the row-direction, the column direction and the stacking direction. The nonvolatile semiconductor according to the seventh embodiment memory device has a higher memory density by relative movement to upper and lower direction of the first-fourth word line conduction layers **36***a*-**36***d* as compared to the sixth embodiment.

Other Embodiments

[0200] Other embodiments of the present invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and example embodiments be considered as exemplary only, with a true scope and spirit of the invention being indicated by the claims that follow. The invention can be carried out by being variously modified within a range not deviated from the gist of the invention.

[0201] For example, in the first-seventh embodiments, word lines WL (first-fourth word line conduction layer **36***a*-**36***d*) are explained as a plane structure, however, the word lines WL are not limited as the plane structure. The word lines WL, for example, may be a stripe structure.

[0202] Further, in the first-seventh the embodiments, the memory layers is constituted with a stacked layer of the tunnel insulation layer (Oxide), the charge storage layer (Nitride) and the block insulation layer (Oxide) in order from the memory side, which is an ONO structure, however, an NO structure omitted the tunnel insulation layer (Oxide) may be applicable.

[0203] Further, in the sixth and seventh the embodiments, the memory layer **30***e* of the fifth embodiment can be applicable in stead of the memory layers **30***f*, **30***g*.

[0204] Further, in the sixth and seventh the embodiment, an space and an actuator is configured to relatively move the first-fourth word line conduction layers **36***a*-**36***d* to the row-direction and the column direction, so that the first-fourth word line conduction layers **36***a*-**36***d* can be moved to the row direction and the column direction

What is claimed is:

1. A nonvolatile semiconductor memory device, comprising a plurality of memory strings, each of the memory strings being constituted with a plurality of electrically erasable memory cells being serially connected each other, the memory strings comprising:

a columnar semiconductor layer perpendicularly extending for a substrate;

a plurality of conductive layers being formed in parallel with the substrate and including a first space between sidewalls of the columnar semiconductor layers; and

a characteristic change layer being formed on the sidewall of the columnar semiconductor layer faced to the first space or a sidewall of the conductive layer faced to the first space, the characteristic change layer changing characteristics accompanying with applied voltage;

wherein each of the conductive layers has a function as a relative movement to a prescribed direction for the columnar semiconductor layer.

2. The nonvolatile semiconductor memory device according to claim **1**,

wherein a surface of the characteristic change layer faced to the first space is formed as concavity and convexity.

3. The nonvolatile semiconductor memory device according to claim **1**,

wherein the first space is configured in each of the conductive layers and includes a hole formed as a slit shape from top view.

4. The nonvolatile semiconductor memory device according to claim **1**,

wherein the characteristic change layer is constituted with a resistance change layer or a charge storage layer, resistance of the resistance change layer being changed accompanying with the applied voltage, the charge storage layer storaging electric charges.

5. The nonvolatile semiconductor memory device according to claim **1**,

wherein the columnar semiconductor layer has flexibility and includes an electrostatic layer, the electrostatic layer deforming the columnar semiconductor layer to the prescribed direction by applying electrostatic force to the columnar semiconductor layer via the first space.

6. The nonvolatile semiconductor memory device according to claim **4**,

wherein the characteristic change layer is the charge storage layer formed on a sidewall of the conductive layer, and each of the memory cells includes the charge storage layer formed on the sidewall of the conductive layer and is serially connected in order.

7. The nonvolatile semiconductor memory device according to claim **6**, further comprising;

a source-side selection transistor and a drain-side selection transistor connected to the lower end and the upper end of the memory cells, respectively.

8. The nonvolatile semiconductor memory device according to claim **7**,

wherein the conductive layer acts as a control gate electrode, the sidewall of the conductive layer contacting with the memory cell, and the conductive layer act as a word line, one end portion of each of the conductive layers is formed into a shape of stairs.

9. The nonvolatile semiconductor memory device according to claim **8**, further comprising;

a word line driving circuit connecting to the word line and controlling voltage applied to the word line;

a source-side selection gate line driving circuit connecting to the source-side selection gate line and controlling voltage applied to the source-side selection gate line;

a drain-side selection gate line driving circuit connecting to the drain-side selection gate line and controlling voltage applied to the drain-side selection gate line;

a plurality of bit lines being connected to the memory strings; and

a sense amplifier connecting to the bit line and amplifying voltage read out from the memory cells.

10. The nonvolatile semiconductor memory device according to claim **1**, further comprising;

a first actuator relatively moving the plurality of the conductive layer to row direction for the columnar semiconductor layer; and

a second actuator relatively moving the plurality of the conductive layer to column direction for the columnar semiconductor layer.

11. The nonvolatile semiconductor memory device according to claim **10**,

wherein the first actuator and the second actuator are electrostatic capacity-type elements, piezo-type elements or thermal expansion-type elements.

12. The nonvolatile semiconductor memory device according to claim **10**, further comprising;

a memory cell region including the plurality of the memory cells;

a first frame layer being conductive and being formed as rectangular to surround the memory cell region;

a second frame layer being conductive and being formed as rectangular to surround the first frame layer;

a third frame layer being conductive and being formed as rectangular to surround the second frame layer;

a first connection layer being formed towards the column direction and electrically connecting with the first frame layer and the second frame layer;

a second connection layer being formed towards the row direction and electrically connecting with the second frame layer and the third frame layer;

a second space being formed between the first frame layer and the second frame layer via a first insulation film and a second insulation film; and

a third space being formed between the second frame layer and the third frame layer via a third insulation film and a fourth insulation film;

wherein the first actuator is constituted with the first frame layer, the first insulation film, the second space, the second insulation film and the second frame layer, and the second actuator is constituted with the second frame layer, the third insulation film, the third space, the fourth insulation film and the third frame layer.

13. The nonvolatile semiconductor memory device according to claim **12**,

wherein the first actuator and the second actuator are comb-like electrostatic capacity-type elements.

14. The nonvolatile semiconductor memory device according to claim **10**,

wherein the relative distance is below 10 nm.

15. The nonvolatile semiconductor memory device according to claim **3**,

wherein a longitudinal direction and a lateral direction of the slit hole are the column direction and the row direction, respectively.

16. The nonvolatile semiconductor memory device according to claim **4**,

wherein the characteristic change layer is constituted with the resistance change layer, the resistance change layer being formed at a conductive layer side via a diode formed on the sidewall of the conductive layer and electrically being connected to the conductive layer.

17. The nonvolatile semiconductor memory device according to claim **5**,

Wherein the electrostatic layer is formed on the plurality of the conductive layer via a fifth insulation film, the columnar semiconductor layer is extended corresponding to the electrostatic layer to be formed as an electrostatic columnar semiconductor layer, the first space is extended to be configured between the electrostatic layer and the electrostatic columnar semiconductor layer, the electrostatic layer is formed to have a sidewall insulation layer on the sidewall thereof, the electrostatic layer includes a lower wiring layer and an upper wiring layer, the upper wiring layer being formed on the lower wiring layer and being sandwiched by a sixth insulation film, the lower wiring layer being formed as a stripe shape with a prescribed pitch to the row direction and extending to the column direction, the upper wiring layer being formed as a stripe shape with a prescribed pitch to the column direction and extending to the row direction.

18. The nonvolatile semiconductor memory device according to claim **5**, further comprising;

a lower driving layer being formed between the conductive layer and the source-side selection transistor, the lower driving layer relatively moving the plurality of the conductive layer to the row direction corresponding to the columnar semiconductor layer by expanding and shrinking; and

an upper driving layer being formed between the drain-side selection transistor and the electrostatic layer, the upper driving layer relatively moving the plurality of the conductive layer to the row direction corresponding to the columnar semiconductor layer by expanding and shrinking.

19. The nonvolatile semiconductor memory device according to claim **18**, wherein

the lower driving layer includes a lower portion first insulation layer, a lower portion first electrode layer, a piezo element film, a lower portion second electrode layer and a lower portion second insulation layer in order;

the upper driving layer an upper portion first insulation layer an upper portion first electrode layer, the piezo element film, an upper portion second electrode layer and an upper portion second insulation layer in order;

the columnar semiconductor layer is extended corresponding to the lower portion driving layer to be formed as a lower portion columnar semiconductor layer, the electrostatic columnar semiconductor layer is extended corresponding to the upper portion driving layer to be formed as a upper portion columnar semiconductor layer; and

the first space is extended to be configured between the lower portion driving layer and the upper portion driving layer, and between the lower portion columnar semiconductor layer and the upper portion columnar semiconductor layer.

20. A method for fabricating a nonvolatile semiconductor memory device, the nonvolatile semiconductor memory device comprising a plurality of memory strings, each of the memory strings being constituted with a plurality of electrically erasable memory cells being serially connected each other, comprising:

forming a source-side transistor layer on a semiconductor substrate;

depositing a silicon-nitride film, a silicon-oxide film, a germanium-silicon film, a silicon-oxide film and a silicon film to form an isolation insulator, a first protective layer, a first sacrifice layer, a second protective layer and a third frame bottom layer on the source-side transistor layer;

forming a first hole at a portion aligned with the source-side columnar semiconductor layer to pass through the third frame bottom layer, the second protective layer, the first sacrifice layer, the first protective layer and the isolation insulator;

forming a second sacrifice layer and a first columnar semiconductor layer on a sidewall of the first hole;

alternately forming a plurality of conductive layers and a plurality of first interlayer insulators on the first columnar semiconductor layer, the second sacrifice layer and the third frame bottom layer;

forming a second hole at a portion aligned with the first hole to pass through the plurality of the conductive layers and the plurality of the first interlayer insulators, constituting a memory hole with the first hole and the second hole;

forming the block insulation layer, the charge storage layer, the tunnel insulation layer, the third sacrifice layer and the second columnar semiconductor layer on a sidewall of the second hole in order, constituting a columnar semiconductor layer with the first columnar semiconductor layer and the second columnar semiconductor layer;

etching the first protective layer, the first sacrifice layer, the third frame bottom layer, the plurality of the conductive layers and the plurality of the first interlayer insulators to form into a shape of stairs;

forming a second interlayer insulator onto an upper surface of the columnar semiconductor layer;

forming a first groove onto au upper surface of the isolation insulator to pass through the interlayer insulator;

forming a second groove, a third groove and a fourth groove onto the first sacrifice layer to pass through the interlayer insulator to form a fourth sacrifice layer, a second frame layer and a fifth sacrifice layer in the second groove, the third groove, the fourth groove, respectively;

forming a fifth groove onto the third frame bottom layer to pass through the interlayer insulator to form a third frame in the fifth groove;

forming first-fourth holes by passing through the interlayer insulator onto an upper surface of an end in the row direction the plurality of the conductive layer and forming plug conductive layers in the first-fourth holes;

forming a sixth sacrifice layer on the first frame layer, a first drain-side insulation layer on the sixth sacrifice layer and first drain-side hole at a portion aligned with the memory hole.

forming a seventh sacrifice layer **51***g* and a first drain-side columnar semiconductor layer on a sidewall of the first drain-side hole;

forming a first drain-side insulation layer, a drain-side conductive layer and a second drain-side insulation layer on the drain-side first insulation layer;

forming a second drain-side hole at s portion aligned with the first drain-side hole to form a drain-side hole constituted with the first drain-side hole and the second drain-side hole;

forming a drain gate insulation layer and a second drain-side columnar semiconductor layer on a sidewall of the drain-side second hole to form a drain-side columnar semiconductor layer constituted with the first drain-side columnar semiconductor layer and the second drain-side columnar semiconductor layer;

forming a bit line layer at a portion aligned with the drain-side hole;

forming a third drain-side hole to a depth of the sixth sacrifice layer; and

removing the first-seventh sacrifice layers in the third drain-side hole by vapor atmosphere of ClF_3 so as to form a space.

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