

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

Petitioner,

v.

MICRON TECHNOLOGY, INC.

Patent Owner.

Case IPR2025-00099

U.S. Patent No. 10,872,903

PETITION FOR *INTER PARTES* REVIEW

TABLE OF CONTENTS

	Page
EXHIBIT LIST	iii
TABLE OF ABBREVIATIONS	vi
LIST OF CHALLENGED CLAIMS	vii
I. INTRODUCTION	1
II. MANDATORY NOTICES	4
A. Real Party-in-Interest	4
B. Related Matters.....	5
C. Counsel and Service Information:.....	5
III. PAYMENT OF FEES	6
IV. REQUIREMENTS FOR INTER PARTES REVIEW	6
A. Grounds for Standing	6
B. Identification of Challenge	6
1. Specific Art on Which the Challenge Is Based	6
2. Statutory Grounds on Which the Challenge Is Based	7
V. '903 PATENT AND PROSECUTION HISTORY	7
A. '903.....	7
B. Prosecution History	9
VI. §325(d) AND §314(a) DISCRETION DOES NOT APPLY	10
A. §325(d)	10
B. §314(a).....	11
VII. LEVEL OF ORDINARY SKILL IN THE ART	11

VIII. CLAIM CONSTRUCTION	12
A. “cavity” limitations ([1.c]-[1.d], [17.l]-[17.o])	12
IX. GROUNDS OF UNPATENTABILITY.....	13
A. Ground 1: Ahn (Claims 1-3, 5, 7-9, 17-20) (§§102/103).....	13
1. Overview of Ahn.....	13
2. Claim Chart	15
B. Ground 2: Ahn in view of Ishikawa (Claims 7, 17).....	41
C. Ground 3: Fukuzumi (Claims 1-3, 7, 9, 17, 19-20) (§§102/103).....	44
1. Overview of Fukuzumi	45
2. Claim Chart	46
D. Ground 4: Fukuzumi in view of Ahn (Claims 5, 8, 18).....	80
X. SECONDARY CONSIDERATIONS	82
XI. CONCLUSION.....	83

EXHIBIT LIST

Exhibit No.	DESCRIPTION
1001	U.S. Patent No. 10,872,903 (“’903”)
1002	File History of U.S. Patent Application No. 16/716,177 (“’903FH”)
1003	Declaration of Dr. Kelin Kuhn in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,872,903 (“Kuhn”)
1004	Certified Translation of Korean Patent Application Publication No. 10-2010-0034612 (“Ahn”)
1005	Korean Patent Application Publication No. 10-2010-0034612
1006	U.S. Patent Application Publication No. 2009/0146190 (“Fukuzumi”)
1007	U.S. Patent Application Publication No. 2009/0283819 (“Ishikawa”)
1008	U.S. Patent No. 5,596,523 (“Endoh”)
1009	U.S. Patent No. 6,765,825 (“Scott”)
1010	U.S. Patent Application Publication No. 2010/0240205 (“Son”)
1011	U.S. Patent Application Publication No. 2009/0242967 (“Katsumata”)
1012	U.S. Patent Application Publication No. 2009/0310425 (“Sim”)
1013	U.S. Patent Application Publication No. 2010/0019310 (“Sakamoto”)
1014	Joint Claim Construction and Prehearing Statement (Patent Local Rule 4-3), <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 105 (N.D. Cal. August 19, 2024)

Exhibit No.	DESCRIPTION
1015	“Extended Data Retention Process Technology for Highly Reliable Flash EEPROMs of 10^6 to 10^7 W/E Cycles” by F. Arai et al. (1998)
1016	“A High-Endurance (>100K) BE-SONOS NAND Flash With a Robust Nitrided Tunnel Oxide/Si Interface” by S. Wang et al. (2010)
1017	“Flash Memory Reliability NEPP 2008 Task Final Report” by Y. Chen (2009)
1018	Counterclaim Plaintiff Micron Technology’s Disclosure of Asserted Claims and Infringement Contentions and Document Production Accompanying Disclosure (Patent Local Rules 3-1 and 3-2), <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL (N.D. Cal.)
1019	U.S. Patent Application Publication No. 2008/0116441A1 (Raghuram)
1020	“Growth characteristics and electrical resistivity of chemical vapor-deposited tungsten film” by I-Shun Chang (1998)
1021	Scheduling Order, <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 141 (N.D. Cal. Sept. 18, 2024)
1022	“Nitride Engineering and the Effect of Interfaces on Charge Trap Flash Performance and Reliability” by Sandhya C. (2008)
1023	Excerpts of “Polycrystalline Silicon for Integrated Circuits and Displays” by Ted Kamins (1998)
1024	Print-out of IEEE webpage (dated November 8, 2024)
1025	U.S. Patent No. 7,425,742 (Nazarian)
1026	U.S. Patent Application Publication No. 2007/0057328 (“Taniguchi”)

Exhibit No.	DESCRIPTION
1027	“Shrinking Possibilities” by B. Arnold (2009)

TABLE OF ABBREVIATIONS

Abbreviation	DESCRIPTION
'903	U.S. Patent No. 10,872,903 (Ex.1001)
'903FH	File History of U.S. Application No. 16/716,177 (Ex.1002)
Claims	Claims 1-3, 5, 7-9, 17-20 of U.S. Patent No. 10,872,903
IPR	<i>Inter Partes</i> Review
Kuhn	Declaration of Dr. Kelin Kuhn in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,872,903 (Ex. 1003)
Ahn	Certified Translation of Korean Patent Application Publication No. 10-2010-0034612 (Ex. 1004)
Fukuzumi	U.S. Patent Application Publication No. 2009/0146190 (Ex. 1006)
Ishikawa	U.S. Patent Application Publication No. 2009/0283819 (Ex. 1007)
Petitioner	Petitioner
PO	Patent Owner
POSITA	Person of Ordinary Skill in the Art
Board	Patent Trial and Appeal Board
NDCA Case	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc., et al.</i> , No. 3:23-cv-05792 (N.D. Cal.)

LIST OF CHALLENGED CLAIMS

[1.pre] An apparatus comprising:

[1.a] conductive pillars extending outward from a substrate;

[1.b] memory cell strings, each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars;

[1.c] a first control gate formed in a first device level, the memory cell strings including a memory cell string, the memory cell string including a first memory cell having a memory element formed in a cavity of the first control gate;

[1.d] a second control gate formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the second control gate; and

[1.e] a conductive channel extending between the first memory cell and the second memory cell and electrically coupled to a conductive pillar of the conductive pillars.

[2] The apparatus of claim 1, further comprising: a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material; and a second conductive region located on a second side opposite from the first side of the conductive pillar and separated from the conductive pillar by a second dielectric material.

[3] The apparatus of claim 2, wherein the first conductive region is coupled to the second conductive region.

[5] The apparatus of claim 2, wherein each of the first and second conductive regions comprises metal.

[7] The apparatus of claim 1, further comprising a data line coupled to the conductive channel, wherein the first and second memory cells are located between the data line and the substrate.

[8] The apparatus of claim 1, wherein the memory element comprises polysilicon.

[9] The apparatus of claim 1, wherein the memory element comprises a dielectric material.

[17.pre] An apparatus comprising:

[17.a] a first conductive pillar and a second conductive pillar extending outward from a substrate;

[17.b] a third conductive pillar and a fourth conductive pillars extending outward from the substrate;

[17.c] a region including a conductive material, the region coupled to the first, second, third, and fourth conductive pillars, the region located between substrate and the first, second, third, and fourth conductive pillars;

[17.d] a first memory cell string formed over the first conductive pillar;

[17.e] a second memory cell string formed over the second conductive pillar;

[17.f] a third memory cell string formed over the third conductive pillar;

[17.g] a fourth memory cell string formed over the fourth conductive pillar;

[17.h] a first data line coupled to the first and second memory cell strings, the first and second memory cell strings located between the first data line and the substrate;

[17.i] a second data line coupled to the third and fourth memory cell strings, the third and fourth memory cell strings located between the second data line and the substrate;

[17.j] a first control gate formed in a first device level;

[17.k] a second control gate formed in a second device level, wherein,

[17.l] the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate;

[17.m] the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate;

[17.n] the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate; and

[17.o] the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.

[18] The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises polysilicon.

[19] The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises a silicon nitride.

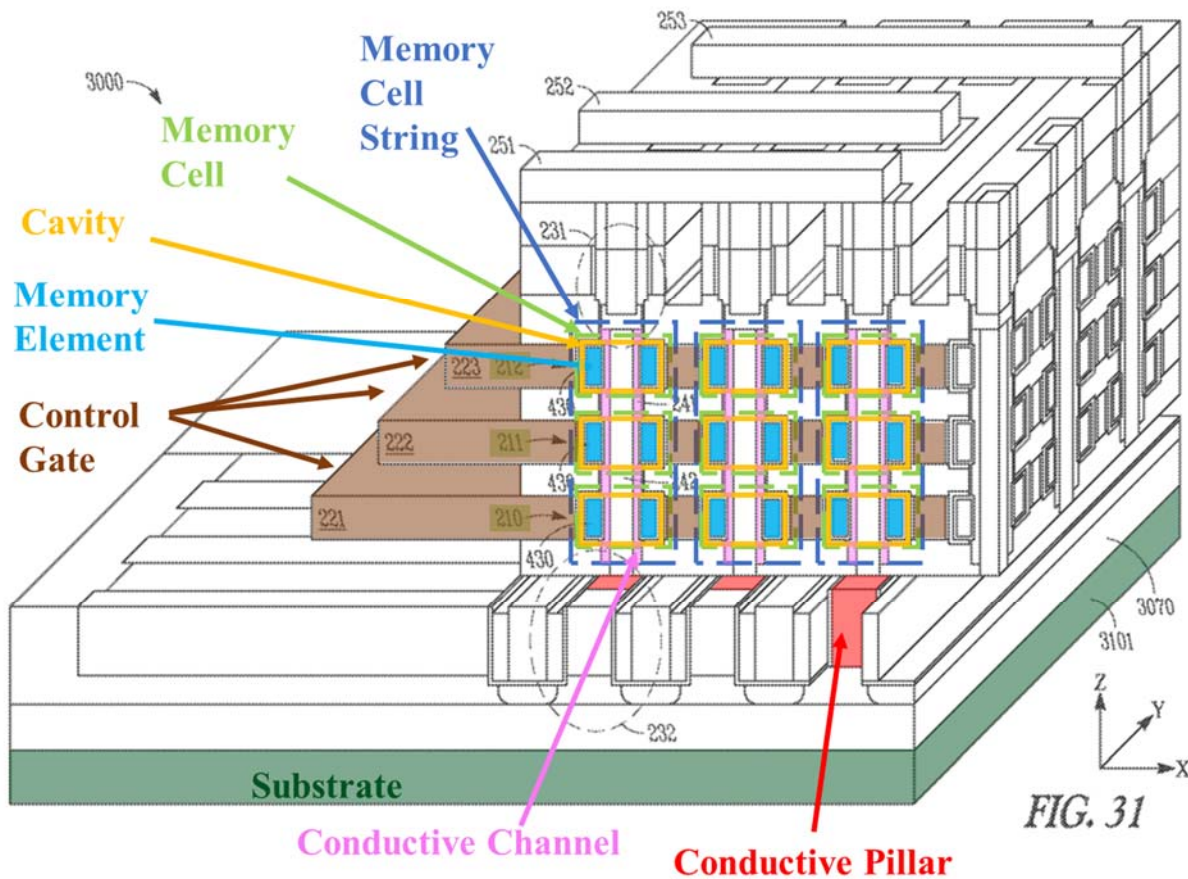
[20] The apparatus of claim 17, further comprising: a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells; a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells; a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells; and a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells.

Pursuant to §§311-319 and §42.1,¹ Petitioner petitions for *inter partes review* (“IPR”) of claims 1-3, 5, 7-9, 17-20 (“Claims”) of U.S. Patent No. 10,872,903 (“’903”) (Ex.1001), assigned to Patent Owner (“PO”). There is a reasonable likelihood—and it is highly likely—that at least one challenged claim is unpatentable as explained herein. Petitioner requests review of the Claims and judgment finding them unpatentable under §§102/103.

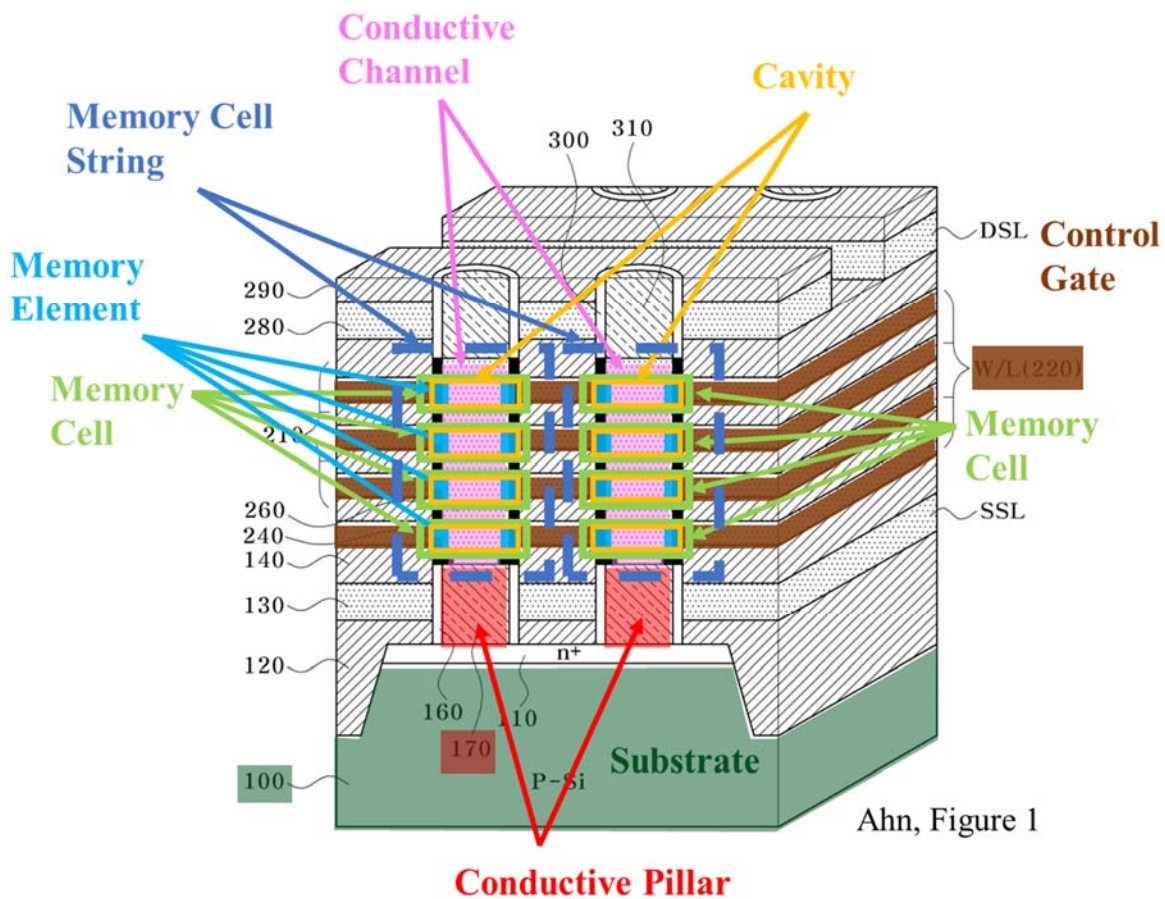
I. INTRODUCTION

The ’903 is generally directed to a non-volatile, three-dimensional memory device, with **memory cells** arranged in the X-, Y-, and Z-directions such that those in the Z-direction form a **memory cell string** above a **conductive pillar** formed on a **substrate**. ’903, 6:49-54, 11:17-41. Each **memory cell** includes a **conductive channel** and a **memory element** formed in a **cavity** of a **control gate**. ’903, 11:17-41, Fig. 4, 4:49-5:3, 12:46-51. Kuhn, ¶48.

¹ Section cites reference 35 U.S.C. (pre-AIA) or 37 C.F.R. as context indicates. All emphasis/annotations added unless noted. Figure annotations herein generally quote the Claims for reference. Citations herein are exemplary and not meant to be limiting.

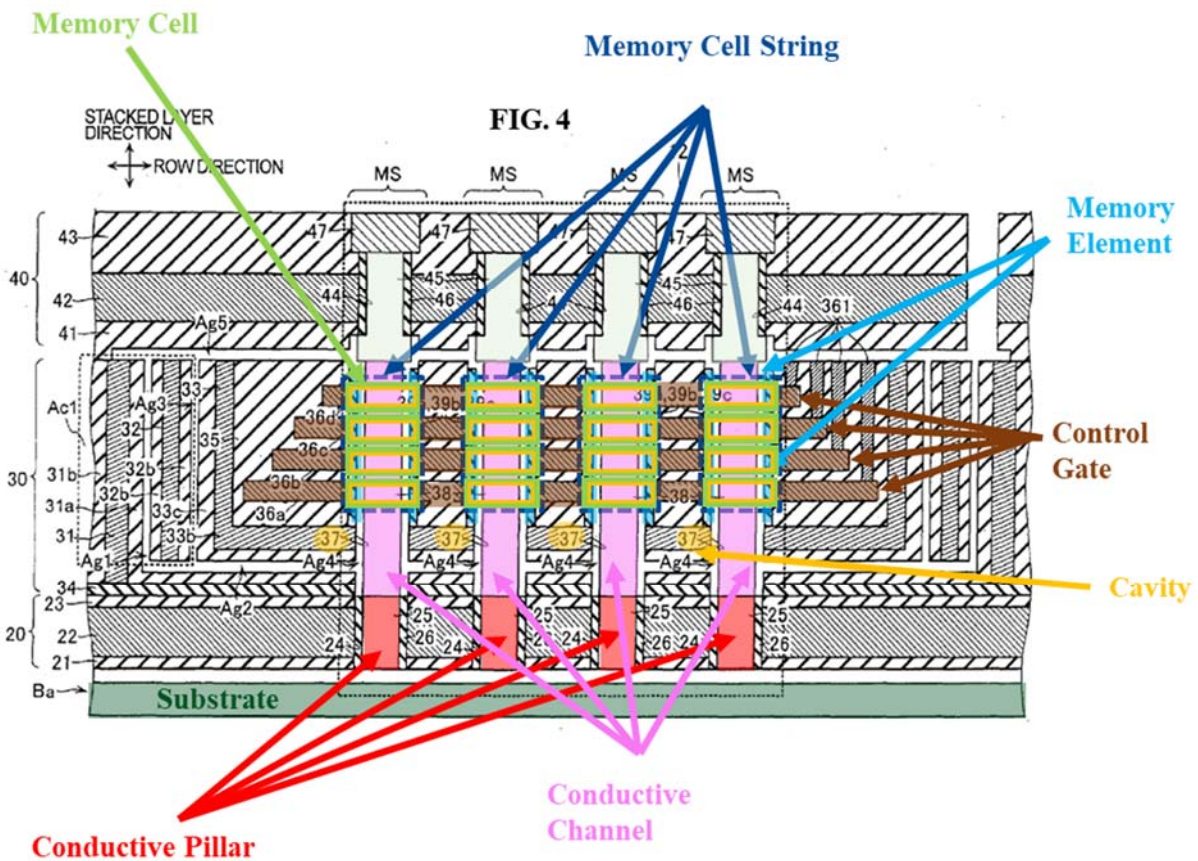


But these concepts were not new. Kuhn, ¶49. Ahn discloses a three-dimensional memory device, where **memory cells** arranged in a vertical direction form a **cell string** above **channel region (170)** formed on a **substrate 100**. Ahn, [0025]-[0028], Figure 1. Ahn's **memory cells** include **channel region (260)** formed inside **through hole (230)** penetrating through **conductive layers (220)**, and a **charge trap layer** formed inside **through hole (230)**. Ahn, [0037], [0040], [0043]. Kuhn, ¶50.



Ahn, Fig. 1.

Fukuzumi likewise discloses a three-dimensional matrix of **memory cells** **MTr1mn-MTr4mn** arranged in row- and column-directions, where a column of **memory cells** **MTr1mn-MTr4mn** forms a string above **source-side columnar semiconductor 25** formed on a **substrate**. Fukuzumi, [0079], [0081]. Each such memory cell **MTr1mn-MTr4mn** includes a **memory 38** formed in a **memory hole 37** penetrating through **word line conduction layers 36a-d**, and **charge storage layer 39b** formed inside **memory hole 37**. Fukuzumi, [0103]-[0104]. Kuhn, ¶51.



Fukuzumi, Fig. 4.

Accordingly, Petitioner requests that the Board institute trial and find the Claims unpatentable.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner is the real party-in-interest. No other parties had access to or control over the present Petition, and no other party funded or participated in preparation of the present Petition.

B. Related Matters

The '903 is the subject of the following co-pending civil action: *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc., et al.*, No. 3:23-cv-05792 (N.D. Cal.) (“NDCA Case”).

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Petitioner consents to electronic service of documents to the email addresses of the counsel identified above.

III. PAYMENT OF FEES

The undersigned authorizes the Office to charge the fee required by §42.15(a) and any additional fees that might be due to Deposit Account No. 18-1945, under Order No. 118880-0002-663.

IV. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Pursuant to §42.104(a), Petitioner certifies that the '903 is available for IPR. Petitioner and any real parties-in-interest are not barred or estopped from requesting IPR challenging the Claims on the Grounds identified herein.

B. Identification of Challenge

Pursuant to §§42.104(b)-(b)(1), Petitioner requests IPR of the Claims, and that the Board cancel the same as unpatentable.

1. Specific Art on Which the Challenge Is Based

Petitioner relies on the following prior art (Kuhn, ¶¶62-64):

Name	Ex.	Publication/Title	Filed	Published/ Issued	Prior art under at least
Ahn	1004- 1005	KR10-2010- 0034612	8/24/2008	4/1/2010	§102(a)
Fukuzumi	1006	U.S.2009/0146190	12/1/2008	6/11/2009	§102(b)
Ishikawa	1007	U.S.2009/0283819	3/20/2009	11/19/2009	§§102(a)/(e)

Each reference was published and/or filed before the '903's earliest claimed priority date of 6/28/2010.

2. Statutory Grounds on Which the Challenge Is Based²

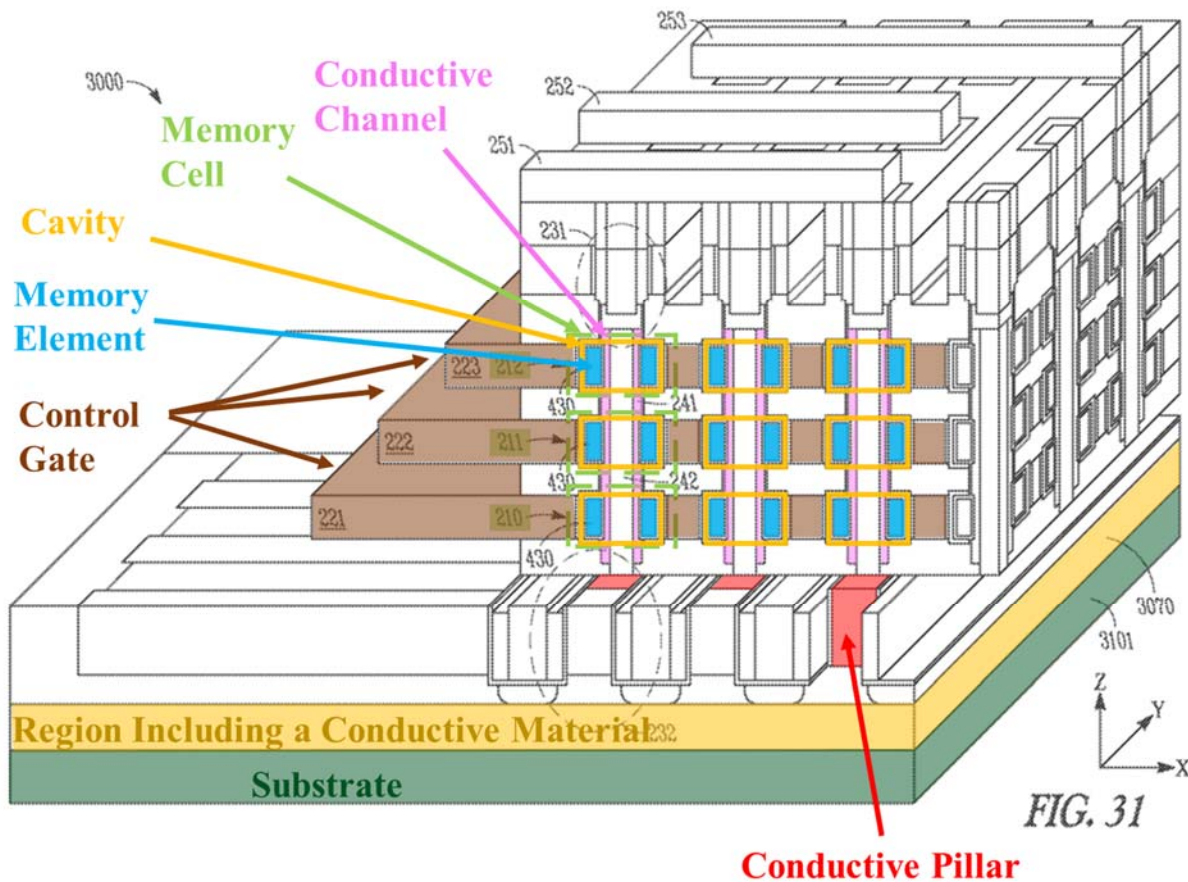
Ground	Claims	Basis	References
1	1-3, 5, 7-9, 17-20	§§102/103	Ahn
2	7, 17	§103	Ahn in view of Ishikawa
3	1-3, 7, 9, 17, 19-20	§§102/103	Fukuzumi
4	5, 8, 18	§103	Fukuzumi in view of Ahn

V. '903 PATENT AND PROSECUTION HISTORY

A. '903

The Claims recite a memory device. '903, 1:66-2:1; Kuhn ¶ 52. Fig. 31 shows an embodiment:

² See Kuhn, ¶¶62-64.



The device comprises a string of **memory cells 210-212** in the Z-direction, and **channels 241** extend in the Z-direction through ring-shaped **memory elements 430** of **memory cells 210-212**. '903, Fig. 31, 11:24-41. **Memory elements 430**, formed in **cavities** of **control gates 221-223**, store charge. '903, 5:4-19, 8:4-26, 12:46-51. By injecting p-type impurities into a top portion of **substrate 3101**, **common source 3070** is formed beneath **pillars**. '903, 10:63-65, 11:51-61, 11:26-30, 11:47-12:34. Kuhn, ¶¶53-54.

Pillars (e.g., pillar 705) are arranged in a matrix in the X- and Y-direction, coupled to and below **channels 241**. '903, Figs. 9 & 31, 3:36-38, 6:11-24, 6:45-49, 9:4-24, 11:27-34, 12:10-22. Kuhn, ¶55.

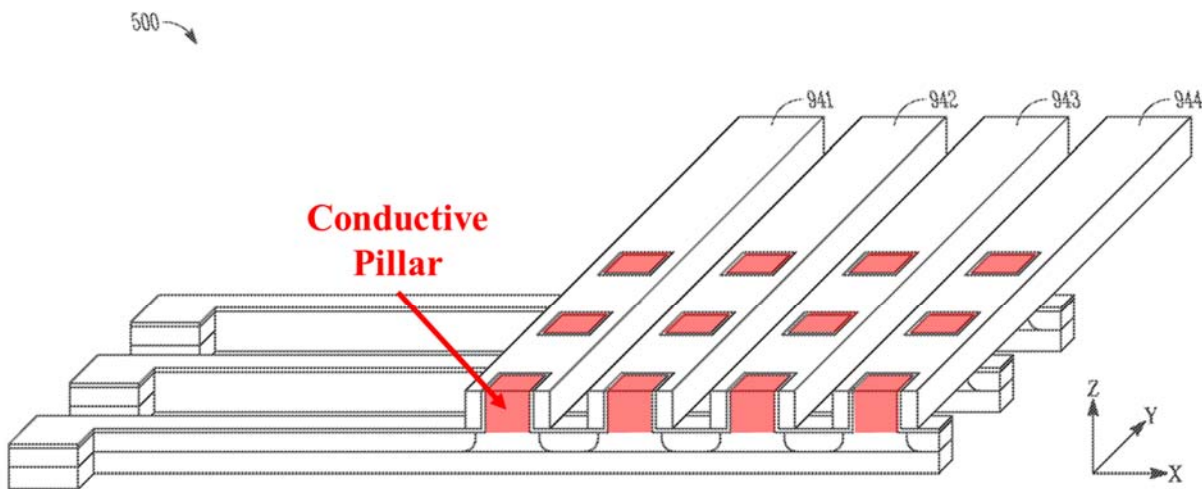


FIG. 9

'903, Fig. 9.

B. Prosecution History

U.S. Patent Application No. 16/716,177 matured into the '903 (filed 12/16/2019). Ex.1002, 213-221. During prosecution, after a double patenting rejection, Applicant cancelled all original claims and added the Claims. Compare Ex.1002, 46-50, with *id.*, 207-212. The Examiner allowed the Claims. Ex.1002, 213-221. Kuhn, ¶56.

VI. §325(d) AND §314(a) DISCRETION DOES NOT APPLY

A. §325(d)

Under the two-part *Advanced Bionics* framework, the Board should not exercise discretion.

This Petition’s grounds are not the same or substantially the same as the art or arguments raised during ’903’s prosecution. The Examiner did not consider **Fukuzumi** or **Ahn**, or art with the same or substantially the same disclosures as those herein. For example, the Claims require “conductive pillars,” which are not in the art of record, but are disclosed in **Ahn** and **Fukuzumi**. See §V.B. Though the Examiner considered **Ishikawa**, the Examiner did not consider **Ishikawa** in combination with **Ahn**. Ex.1002, 84, 193; *Sony v. MZ Audio Scis., LLC*, IPR2022-01544, Pap. 12, *7 (§325(d) discretion is improper where “Examiner did not consider the specific combination of references asserted”).

Even if the art or arguments were substantially the same, the Examiner erred in a manner material to the patentability of the Claims. Because the Examiner did not consider **Fukuzumi** and **Ahn** as prior art, “[i]t is...difficult, if not impossible, to discern...how the Examiner might have considered the arguments presented in the Petition, had they been presented to the Examiner.” *Bowtech, Inc. v. MCP IP, LLP*, IPR2019-00379, Pap. 14, *19-20 (declining to exercise §325(d) discretion where Petitioner did not “even attempt[] to explain how the Examiner

erred in any way”). Moreover, because the Examiner “did not expressly consider” **Ishikawa**, it is “impossible...to determine the consideration the Examiner gave” to this reference; “the absence of further evidence of the Examiner’s consideration of” the art demonstrates that “the Office erred in a manner material to patentability”—as confirmed by the strength of these references’ teachings. *See* §IX; *Ecobee Techs. v. Causam Enterprises, Inc.*, IPR2022-01339, Pap. 20, *20-21 (declining to exercise §325(d) discretion).

B. §314(a)

The PTAB should not exercise its §314(a) discretion where, as here, trial in the co-pending litigation (NDCA Case) is scheduled for 6/15/2026—after an expected FWD. EX.1021.

VII. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this Petition only, Petitioner assumes the Claims are entitled to the earliest claimed priority date of 6/28/2010. Kuhn, ¶58.

A POSITA at the time of the claimed invention would have had a Bachelor’s degree in electrical engineering, materials science, physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. A higher level of education might make up for less experience, and vice versa. Kuhn, ¶¶57-59.

VIII. CLAIM CONSTRUCTION

Claim terms subject to IPR are construed using *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). 37 C.F.R. §42.100(b). Only terms necessary to resolve the controversy need construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Because the prior art asserted herein discloses embodiments within the Claims’ indisputable scope, the Board need not construe the Claims’ outer bounds. Other than noted here, all claim terms should be construed according to their plain and ordinary meaning as would have been understood by a POSITA. Kuhn, ¶¶60-61.

A. “cavity” limitations ([1.c]-[1.d], [17.l]-[17.o])

In the NDCA Case, Petitioner proposes “[first-fourth] cavity of [first/second] control gate” should be construed as “a [first-fourth] hole with a larger diameter than holes in the layers immediately above and below the [first/second] control gate.” (“Petitioner’s Construction”). Ex.1014, Appendix B at 10-11. PO asserts those terms should be given their plain and ordinary meaning, without specifying the meaning (“PO’s Construction”). *Id.* The court in the NDCA Case has not construed the term, and the Board need not construe the term either. The prior art discloses this limitation both under PO’s Construction (*see, e.g.*, Grounds 1-2) and either party’s construction (*see, e.g.*, Grounds 3-4). *See* §§IX.A-D. Kuhn, ¶¶61.

IX. GROUNDS OF UNPATENTABILITY

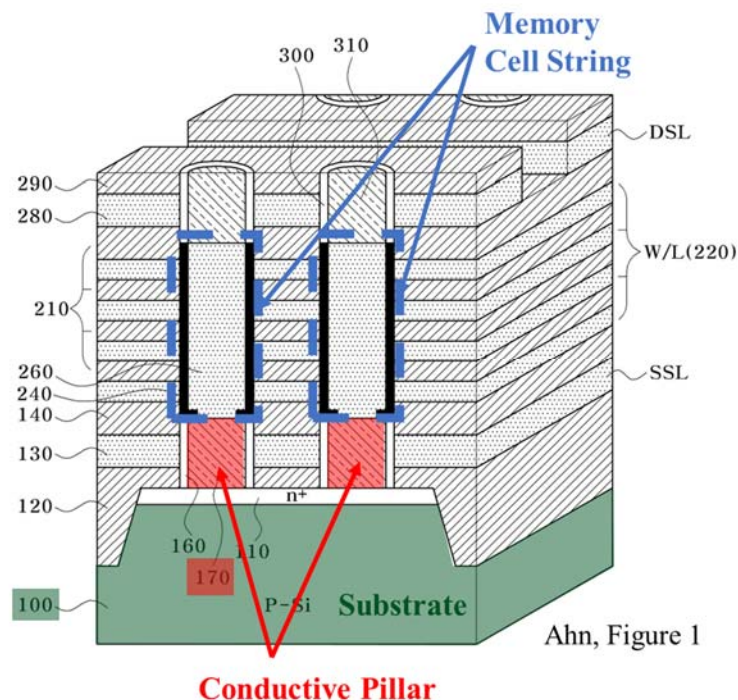
As explained below, the Claims are unpatentable as anticipated and obvious. Kuhn, ¶¶65-67, 291. This Petition is supported by the Declaration of Dr. Kuhn, which describes the prior art's scope and content at the time of and well before the '903. *See* Kuhn.

A. Ground 1: Ahn (Claims 1-3, 5, 7-9, 17-20) (§§102/103)

Ahn discloses and at least renders obvious the Claims, at least under PO's Construction of the "cavity" limitations. Kuhn, ¶¶71-72.

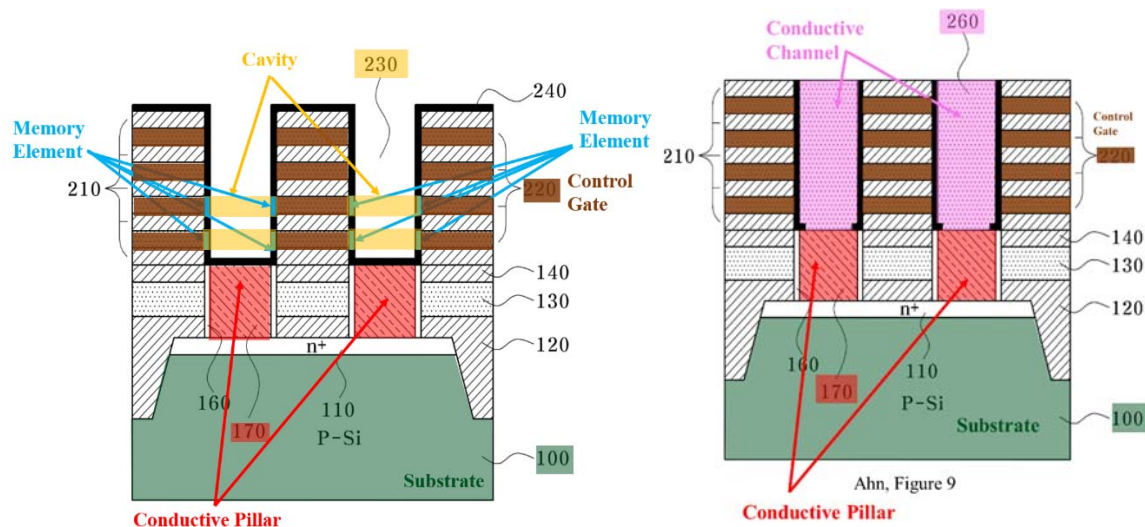
1. Overview of Ahn

Ahn discloses a three-dimensional memory device with memory cells to store data. Ahn, [0002], [0022], [0038]. Figure 1 shows an embodiment:

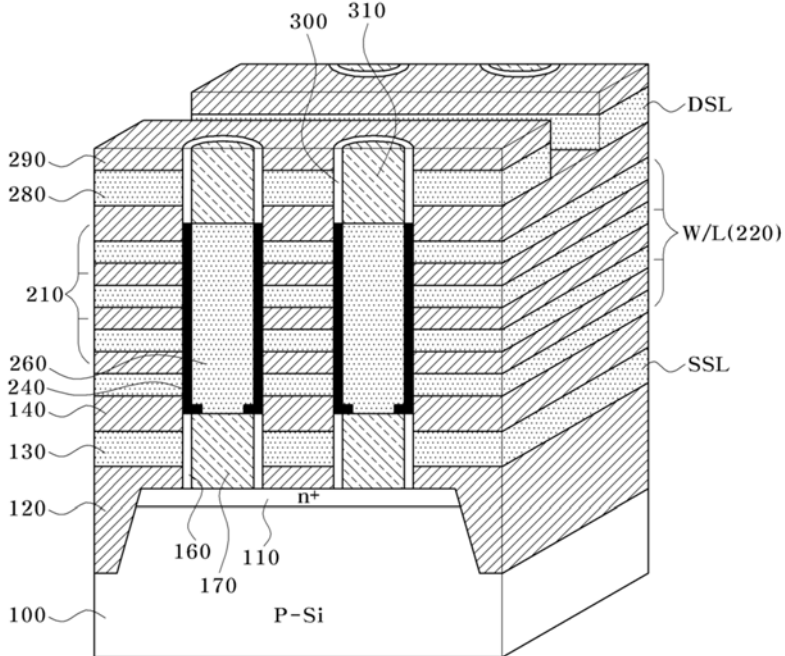


Ahn's memory device includes "cell strings[] arranged vertically on a substrate (100)," where each cell string includes "source select transistor, a plurality of memory cells, and a drain select transistor." Ahn, [0026]. Ahn's source select transistors include channel region (170) formed on the substrate (100). Ahn, [0027]. Kuhn, ¶¶68-69.

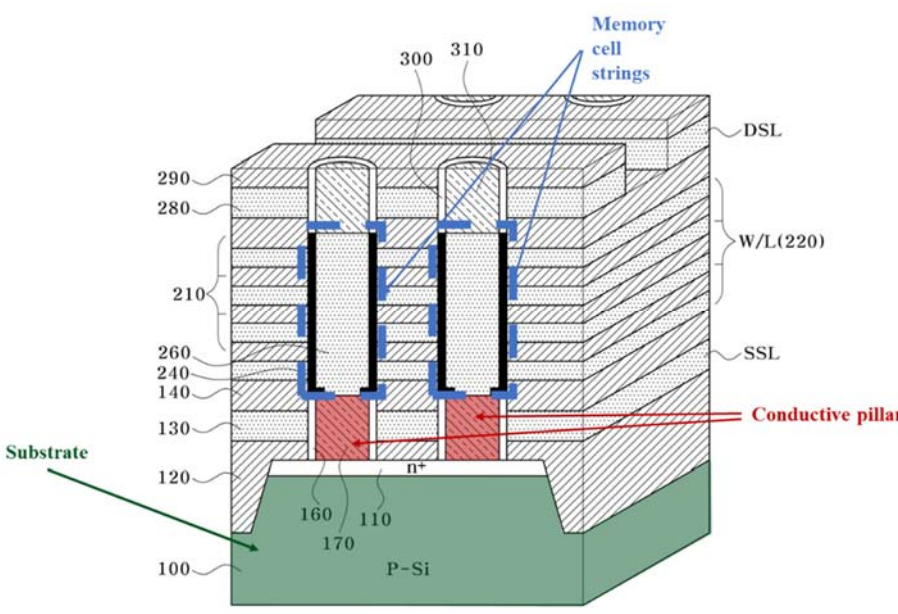
Ahn further discloses through holes (230) passing through conductive layers (220) (control gates), and exposing channel region (170) underneath, and charge trap layer "formed on the inner wall" of through hole (230) in each conductive layer (220). Ahn, [0036]-[0040]. Through holes (230) are filled to form channel region (260) of the memory cells. Ahn, [0043]. Kuhn, ¶70.



2. Claim Chart

'903	Ahn
[1.pre] An apparatus comprising:	To the extent the preamble is limiting, Ahn discloses an apparatus (e.g., “a flash memory device having a three-dimensional structure”). <u>E.g., Ahn:</u> Ahn discloses a “a flash memory device having a three-dimensional structure.” Ahn, [0001]. Kuhn, ¶¶73-75. • Figure 1  • [0001] (“The present invention relates to a method for manufacturing...<i>a flash memory device having a three-dimensional structure.</i>”) • See also [0007]
[1.a] conductive pillars extending	Ahn discloses conductive pillars (e.g., “channel region (170)”) extending outward from a substrate (e.g., “substrate (100)”).

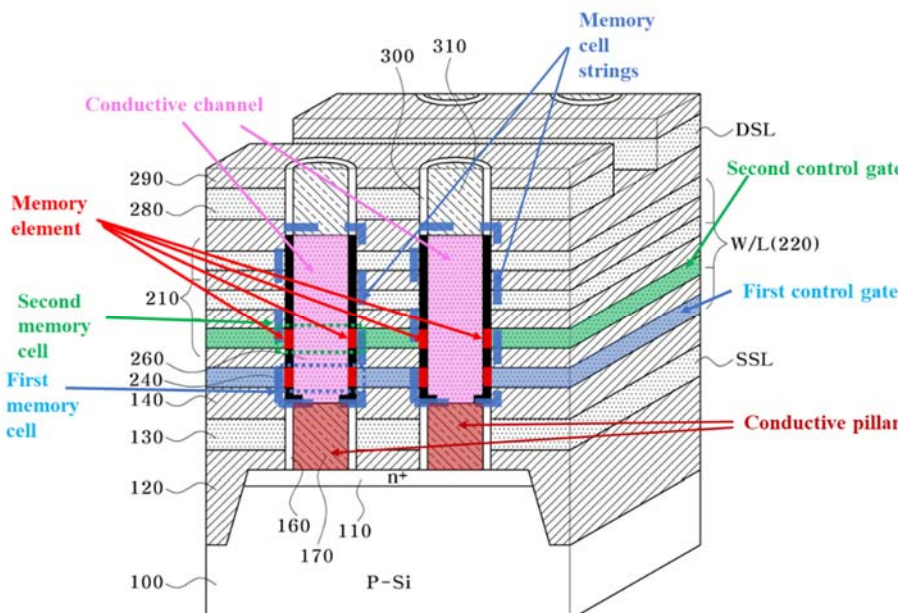
'903	Ahn
outward from a substrate;	<u>E.g., Ahn:</u> Ahn discloses channel region (170) formed on substrate (100). Ahn, [0027], Fig. 1. Kuhn, ¶¶76-78. - Figure 1 The diagram shows a cross-section of a semiconductor device. At the bottom is a green substrate (100) labeled 'P-Si'. Above it is a layer (110) labeled 'n+'. Two red rectangular regions (170) are embedded in the n+ layer, connected to a source (110) at the bottom. Above these are two vertical black bars representing conductive pillars (130). The pillars extend through several horizontal layers: 140, 240, 260, 210, 280, and 290. A bracket groups layers 210, 240, and 260 as 'SSL' (Source Select Layer). Another bracket groups layers 280 and 290 as 'W/L(220)' (Word Line). The topmost layer is labeled 'DSL' (Drain Select Layer). Two circular features (300 and 310) are shown on the top surface. A green arrow points from the label 'Substrate' to the bottom layer (100). [0027] (“The source select transistor consists of...<i>a channel region (170) formed to fill the through hole in which the above gate insulating layer is formed. The channel region is connected to a source (110) formed on the substrate....</i>”) - See also [0026], [0032]-[0033], [0035]
[1.b] memory cell strings, each of the memory cell strings is formed over a respective conductive pillar of the	Ahn discloses memory cell strings (e.g., “memory cells” of “cell strings”), each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars (e.g., “arranged vertically” over “channel region (170)”). <u>E.g., Ahn:</u> See [1.a]. Ahn further discloses “a plurality of cell strings,” each including “memory cells.” Ahn, [0026]. Ahn further discloses channel region (260) of the memory cells is formed

'903	Ahn
conductive pillars;	on channel region (170). Ahn, [0026], [0042]-[0043]. Kuhn, ¶¶79-82. - Figure 1  [0026] (“A source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string, and a plurality of such cell strings are arranged on the substrate (100).”). [0042] (“In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, charge trap layer, and blocking layer at the bottom of the through hole are etched to <i>expose the channel region (170) of the source select transistor. ...</i>”) [0043] (“...a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of the cell transistor....”)

'903	Ahn
	• See also [0025], [0036]-[0038]
[1.c] a first control gate formed in a first device level, the memory cell strings including a memory cell string, the memory cell string including a first memory cell having a memory element formed in a cavity of the first control gate;	Ahn discloses a first control gate formed in a first device level (e.g., lowest “conductive layer (220)”), the memory cell strings (e.g., “memory cells” of “cell strings”) including a memory cell string, the memory cell string including a first memory cell (e.g., “memory cell” at the lowest “conductive layer (220)” in Fig. 1) having a memory element (e.g., “charge trap layer”) formed in a cavity (e.g., “through hole (230)”) of the first control gate. <u>E.g., Ahn:</u> See [1.b]. Further, Ahn’s conductive layer (220) is a “control gate of the memory cell.” Ahn, [0036]. Ahn also discloses through hole (230) passing through conductive layers (220) and a charge trap layer “formed on the inner wall” of “through hole (230).” Ahn, [0037]-[0038]. Kuhn, ¶¶83-86. Conductive layer (220) “constituting the [] memory cell is repeatedly stacked as many times as the number of memory cells connected to one cell string” and the lowest conductive layer (220) in combination with the charge trap layer in Figure 1 forms a first memory cell. Ahn, [0028], [0036], [0040]. Kuhn, ¶86. • Figure 1

'903	Ahn
	Figure 7
	[0036] (“...on the resulting structure in which the source select transistor is formed, an interlayer

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	<i>insulating film (210) and a conductive layer (220) are repeatedly deposited several times....</i>The above conductive layer (220) can be repeatedly stacked.... <i>The above conductive layer (220) serves as a control gate of the memory cell....</i>") • [0038] ("...an ONO dielectric layer (240) for charge storage, i.e., a blocking layer, a charge trap layer, and a tunneling layer, are sequentially formed on the inner wall of the above through hole (230).") • See also [0026], [0028], [0037], [0040], [0042]-[0043]
[1.d] a second control gate formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the second control gate; and	Ahn discloses a second control gate formed in a second device level (e.g., second lowest "conductive layer (220)"), the memory cell string (e.g., "cell string") including a memory cell string, the memory cell string including a second memory cell (e.g., "memory cell" at the second lowest "conductive layer (220) in Fig. 1) having a memory element (e.g., "charge trap layer") formed in a cavity (e.g., "through hole (230)") of the second control gate. <u>E.g., Ahn:</u> See [1.b], [1.c]. Further, second lowest conductive layer (220) in combination with the charge trap layer in Figure 1 forms a second memory cell. Kuhn, ¶¶87-90. • Figure 1 (see [1.c]) • Figure 7 (see [1.c]) • See also [0026], [0028], [0036]-[0038], [0040], [0042]-[0043]
[1.e] a conductive channel extending between the first memory cell and the	Ahn discloses a conductive channel (e.g., "channel region (260)") extending between the first memory cell and the second memory cell (e.g., "memory cells" at the lowest and second-lowest "conductive layers (220)" in Fig. 1) and electrically coupled to a conductive pillar of the conductive

'903	Ahn
second memory cell and electrically coupled to a conductive pillar of the conductive pillars.	pillars (e.g., “connect[ed]” to “channel region (170)” below “channel region (260)”). <u>E.g., Ahn:</u> See [1.a]-[1.d]. Ahn further discloses channel region (260) passing through conductive layers (220), connecting the memory cells with (and thus electrically coupled to) channel region (170). Ahn, [0025], [0037], [0042]-[0043], Fig. 1. Kuhn, ¶¶91-94. - Figure 1  [0042] (“In order to connect the channel region of the source select transistor and the channel region of the memory cell, the protective film (250), tunneling layer, charge trap layer, and blocking layer at the bottom of the through hole are etched to expose the channel region (170) of the source select transistor....”) [0043] (“...a conductive material is deposited on the resulting material where the channel region of the source select transistor is exposed so that the above through hole is filled to form a channel region (260) of

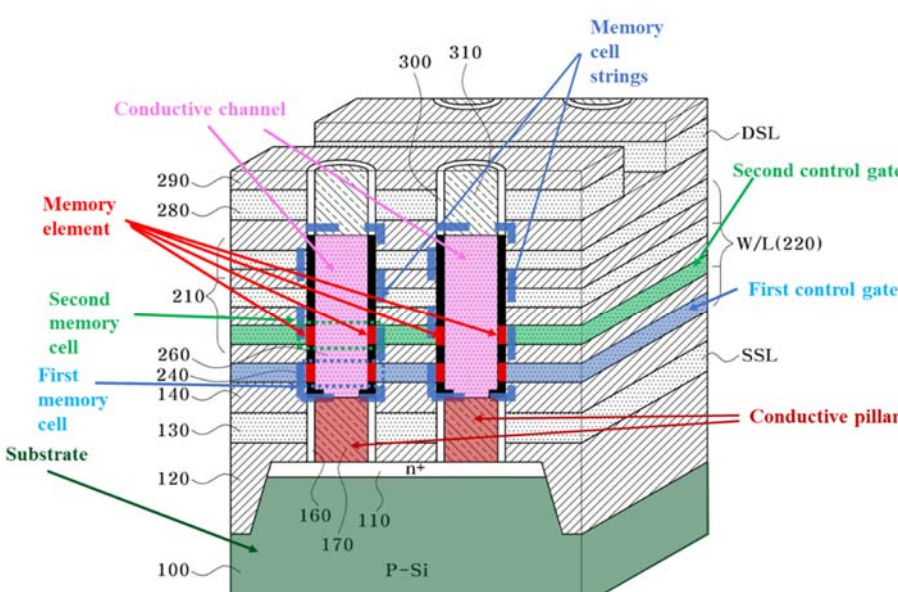
'903	Ahn
	<i>the cell transistor.</i> The channel region (260) of the above cell transistor can be formed of a polysilicon film or a conductive metal film doped with impurities....”) • See also [0025]-[0026], [0028], [0036]-[0038], [0040], Figure 9.
[2.a] The apparatus of claim 1, further comprising: a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material; and [2.b] a second conductive region located on a second side opposite from the first side of the conductive pillar and separated from the conductive pillar by a second dielectric material.	See [1]. Ahn discloses a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material; and a second conductive region located on a second side of the conductive pillar and separated from the conductive pillar by a second dielectric material (e.g., portions of “gate conductive layer (130) on the left and right sides of “channel region (170), respectively, and portions of “gate insulating layer (160)” respectively separate the left and right sides of “gate conductive layer (130)” from “channel region (170),” as shown in Fig. 1). <u>E.g., Ahn:</u> See [1.a], [1.e]. Ahn further discloses channel region (170) passes through gate conductive layer (130), such that regions of gate conductive layer (130) are on the left and right sides of channel region (170). Ahn, [0033], [0035]. Ahn further discloses gate insulating film (160) (a dielectric material) formed between gate conductive layer (130) and channel region (170), such that portions of gate insulating film (160) on the left and right sides of channel region (170) separate channel region (170) and respective regions of gate conductive layer (130). Ahn, [0034]. Kuhn, ¶¶95-102. Moreover, PO accuses the same structure in NDCA Case as satisfying this limitation. Ex.1018, Ex.D at 6-8. Kuhn, ¶103. • Figure 1

'903	Ahn
	• [0033] (“...the above conductive layer (130) and the insulating layer (140) in the region where the channel of the source select transistor is to be formed are etched to form a hole (150) that exposes the impurity layer (110) formed on the above substrate (100). The above hole (150) is a region in which a channel of a source select transistor is formed....”) • [0034] (“...a silicon oxide film is deposited on the side of the above hole...to form a gate insulating film (160) of a source select transistor....”) • [0035] (“...the interior of the hole where the gate insulating film (160) is formed is filled with a semiconductor layer such as single crystal silicon (Si). The above semiconductor layer ... becomes a channel region (170) of the select transistor....”) • See also [0032]
[3] The apparatus of claim 2, wherein the first conductive region is	See [2]. Ahn discloses the first conductive region (e.g., left portion of “gate conductive layer (130)” in Fig. 1) is coupled to the second conductive region (e.g., right portion of “gate conductive layer (130)” in Fig. 1).

'903	Ahn
[7] The apparatus of claim 1, further comprising a data line coupled to the conductive channel, wherein the first and second memory cells are located between the data line and the substrate.	See [1]. Ahn discloses a data line (e.g., bit line completing circuit on drain side of “cell strings”) coupled to the conductive channel (e.g., “channel region (260)” of cell transistors), wherein the first and second memory cells (e.g., “memory cells” at the lowest and second lowest “conductive layers (220)” in Fig. 1) are located between the data line and the substrate (e.g., “substrate (100)”). <u>E.g., Ahn:</u> See [1.a]-[1.e]. Furthermore, Ahn teaches data lines coupled to channel region (260). Ahn discloses its device is a “flash memory,” which a POSITA would have understood includes bit lines connected to the memory cells. Ahn, [0025]. Kuhn, ¶¶112-116. Moreover, Ahn’s memory cells store and erase data in a charge trap layer. Ahn, [0022], [0038]. Bit lines are used to perform these basic operations. Kuhn, ¶¶115-116.³ Ahn’s data line is located above channel region (310) of the drain select transistor such that the first and second memory cells are located between the data line and the substrate. Kuhn, ¶117. At the very least, POSITA would have found it obvious to form bit lines on top of the components explicitly taught by Ahn, as it obviates any modification of the manufacturing process or memory structure described in Ahn. In this regard, it was well-known in 3D flash memory to place bit lines over the memory cells.⁴ Kuhn, ¶118. Thus, a POSITA would have found it routine, straightforward and advantageous to place bit lines over Ahn’s flash memory, and would have known that applying bit lines to Ahn’s flash

³ Ex.1008, 1:44-60; Ex.1009, 1:60-2:9, 2:38-46, Fig. 5; Ex.1011, [0055].

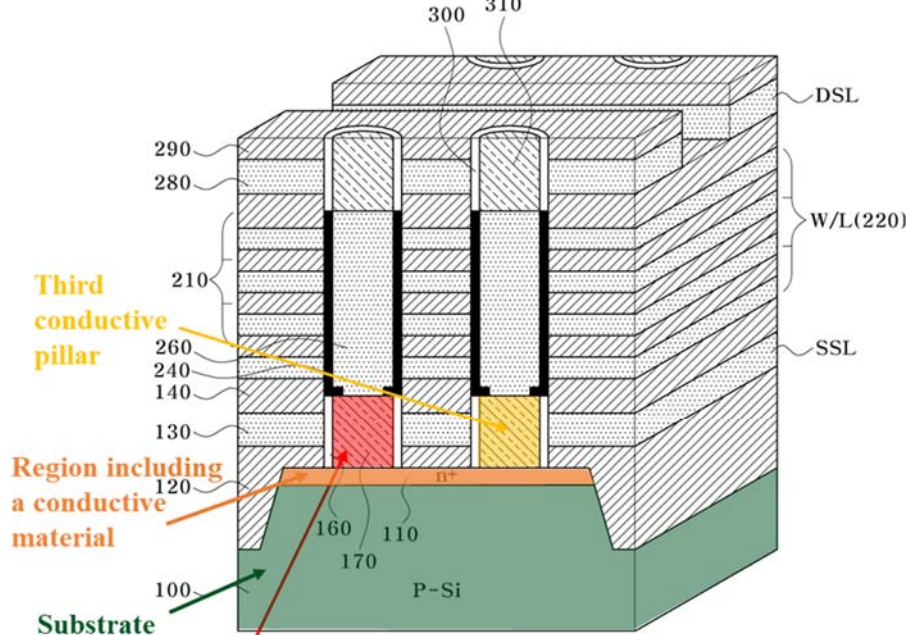
⁴ Ex.1010, [0039], [0053], Fig. 1; Ex.1011, [0047]-[0055], Fig. 2.

'903	Ahn
	memory (yielding the claimed limitations) would predictably work and provide the expected functionality. Kuhn, ¶119. - Figure 1  [0022] (“[B]y forming wells in vertically arranged memory cells, <i>data in the memory cells can be simultaneously erased</i> using the F-N tunneling method.”) [0025] (“Referring to Figure 1, a flash memory device having a three-dimensional structure according to one embodiment of the present invention includes <i>a source select transistor formed on a substrate (100), gate stacks (220) formed on the above source select transistor and repeatedly stacked to be separated by an insulating layer (210), a charge storage region (240) formed by a blocking layer, a charge trap layer, and a tunneling layer formed on a sidewall of a through hole penetrating the above gate stacks, memory cells formed by a channel region (260) formed to fill the above through hole, and a drain select transistor formed to be connected to the above memory cells.</i>”)

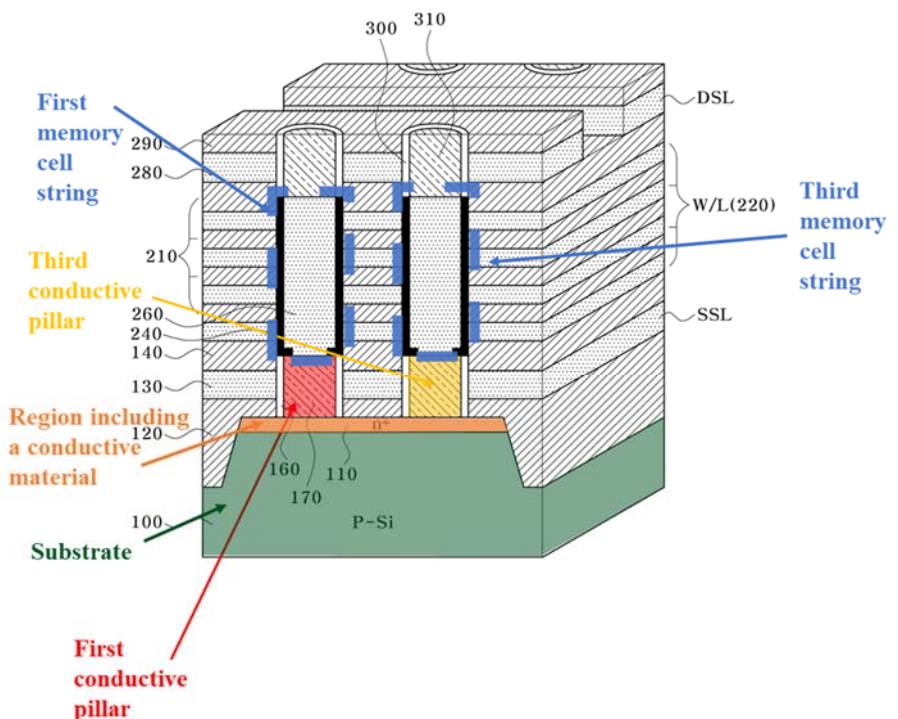
'903	Ahn
	See also [0026], [0037]-[0038], [0042]-[0044], [0046], [0048]-[0049]
[8] The apparatus of claim 1, wherein the memory element comprises polysilicon.	See [1]. Ahn discloses that the memory element (e.g., “charge trap layer”) comprises polysilicon (e.g., “polysilicon”). <u>E.g., Ahn:</u> See [1.c]. Ahn further discloses the “charge trap layer” is formed by depositing “a polysilicon film.” Ahn, [0040]. Kuhn, ¶¶120-122. [0040] (“...<i>a charge trap layer is formed by depositing...a polysilicon film....</i>”).
[9] The apparatus of claim 1, wherein the memory element comprises a dielectric material.	See [1]. Ahn discloses that the memory element (e.g., “charge trap layer”) comprises a dielectric material (e.g., “silicon-nitride”). <u>E.g., Ahn:</u> See [1.c]. Ahn further discloses the “charge trap layer” is formed of “a silicon nitride film,” a dielectric material.⁵ Ahn, [0040]. Kuhn, ¶¶123-126. [0040] (“...<i>a charge trap layer is formed by depositing...a silicon nitride film....</i>”).
[17.pre] An apparatus comprising:	See [1.pre]. Kuhn, ¶127.
[17.a] a first conductive	Ahn discloses a first conductive pillar (e.g., front-left “channel region (170)” in Fig. 1), a second conductive pillar

⁵ Ex.1019, [0071]

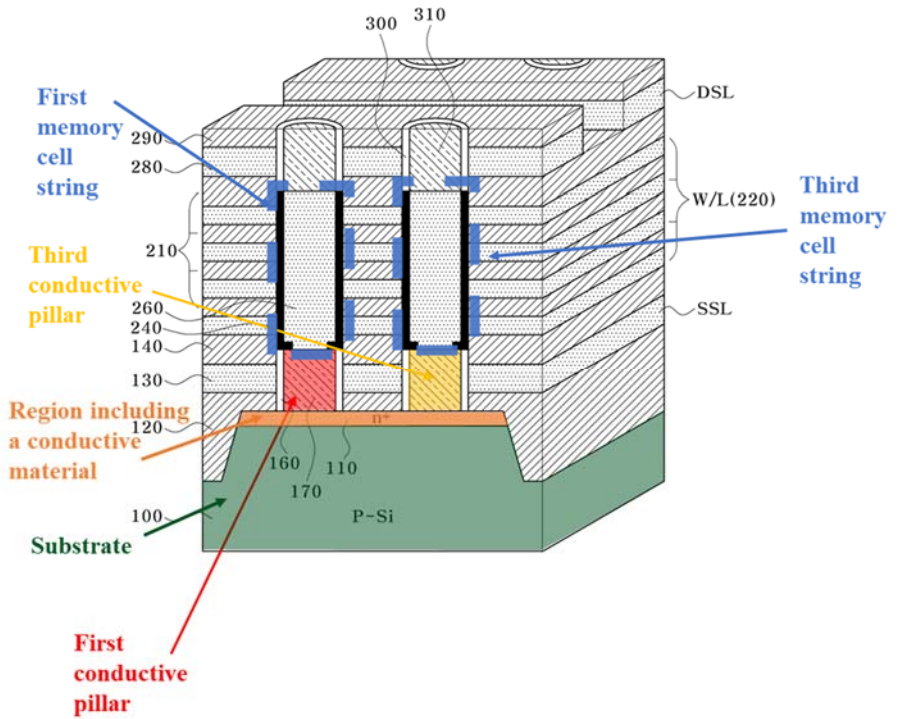
'903	Ahn
pillar and a second conductive pillar extending outward from a substrate; [17.b] a third conductive pillar and a fourth conductive pillars extending outward from the substrate;	(e.g., back-left “channel region (170)” in Fig. 1), a third conductive pillar (e.g., front-right “channel region (170)” in Fig. 1), and a fourth conductive pillars (e.g., back-right “channel region (170)” in Fig. 1) extending outward from the substrate (e.g., “substrate (100)”). <u>E.g., Ahn:</u> See [1.a]. Ahn further discloses cell strings “arranged on the substrate (100)” in a two-by-two matrix. Ahn, Fig. 1. As discussed in [1.a], each cell string includes a source select transistor, including a channel region (170). While only two cell strings of the front row are illustrated in Ahn’s figures (including first and third conductive pillars), a POSITA would have understood (and at least found obvious) two cell strings of the rear row (including second and fourth conductive pillars) are identical. Kuhn, ¶¶128-131. • Figure 1

'903	Ahn
	 • [0027] (“The source select transistor consists of...a channel region (170) formed to fill the through hole in which the above gate insulating layer is formed. The channel region is connected to a source (110) formed on the substrate...”) • See also [0004], [0026], [0032]-[0033], [0035]
[17.c] a region including a conductive material, the region coupled to the first, second, third, and fourth conductive pillars, the region located	Ahn discloses a region including a conductive material (e.g., “source 110” or “impurity layer (110)”), the region coupled to the first, second, third, and fourth conductive pillars (e.g., the four “channel regions (170)” of the source select transistor on “source 110,” as shown in Fig. 1), the region located between substrate (e.g., “substrate 100”) and the first, second, third, and fourth conductive pillars (e.g., channel regions (170)). <u>E.g., Ahn:</u>

'903	Ahn
between substrate and the first, second, third, and fourth conductive pillars;	See [1.a] and [17.a]-[17.b]. Ahn further discloses impurity layer/source (110), on substrate (100). Ahn, [0031]. Impurity layer (110) is “formed by ion-implanting impurities of the conductivity type opposite to that of the semiconductor substrate (100), for example, N type” and insulating film (120) “separate[s] the impurity layer from <i>other</i> conductive layers,” confirming impurity layer (110) is itself conductive. Ahn, [0031]. Ahn further discloses channel regions (170) formed on impurity layer (110) such that source (110) is coupled to channel regions (170) and located between channel region (170) and substrate (100) (see [17.a]-[17.b]). Ahn, [0027], [0031]-[0035]. Kuhn, ¶¶132-135. - Figure 1 - See also [0026]-[0027], [0031]-[0033], [0035]

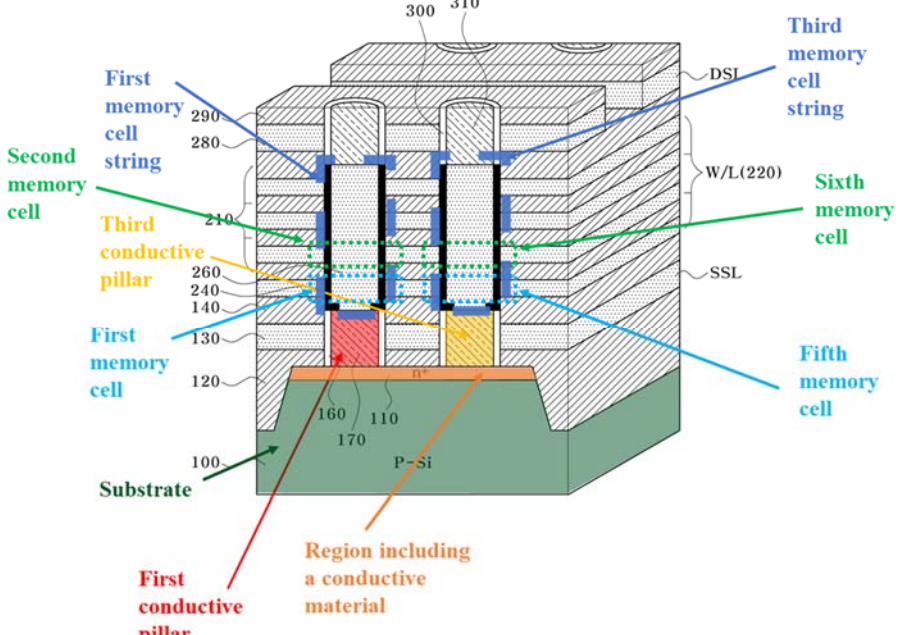
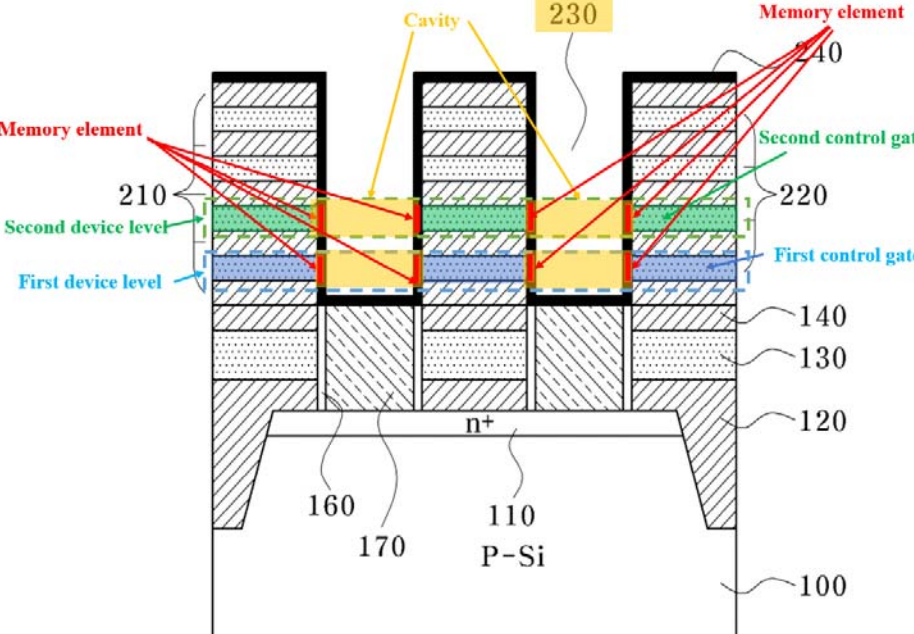
'903	Ahn
[17.d] a first memory cell string formed over the first conductive pillar; [17.e] a second memory cell string formed over the second conductive pillar; [17.f] a third memory cell string formed over the third conductive pillar; [17.g] a fourth memory cell string formed over the fourth conductive pillar;	Ahn discloses a first memory cell string formed over the first conductive pillar, a second memory cell string formed over the second conductive pillar, a third memory cell string formed over the third conductive pillar, a fourth memory cell string formed over the fourth conductive pillar (e.g., “memory cells” of “cell string” over four “channel region (170)” of Fig. 1—see [17.a]-[17.b]). <u>E.g., Ahn:</u> See [1.a]-[1.b], [17.a]-[17.c]. Ahn further discloses “source select transistor, a plurality of memory cells, and a drain select transistor are arranged vertically on a substrate (100) to form one cell string,” such that first-fourth sets of memory cells are respectively formed over first-fourth channel regions (170) illustrated in Figure 1, as identified in [17.a]-[17.b]. Ahn, [0026], [0042]-[0043], Fig. 1. Kuhn, ¶¶136-139. Figure 1 (front portion) 

'903	Ahn
	• See also [0025], [0026], [0036], [0037], [0038], [0042], [0043]
[17.h] a first data line coupled to the first and second memory cell strings, the first and second memory cell strings located between the first data line and the substrate; [17.i] a second data line coupled to the third and fourth memory cell strings, the third and fourth memory cell strings located between the second data line and the substrate;	Ahn discloses a first data line (e.g., line completing circuit on drain side of “cell strings”) coupled to the first and second memory cell strings (e.g., “memory cells” of front-left and back-left “cell strings” of Fig. 1), the first and second memory cell strings located between the first data line and the substrate (e.g., “substrate (100)”); a second data line (e.g., line completing circuit on drain side of “cell strings”) coupled to the third and fourth memory cell strings (e.g., “memory cells” of front-right and back-right “cell strings” of Fig. 1), the third and fourth memory cell strings located between the second data line and the substrate (e.g., “substrate (100)”). <u>E.g., Ahn:</u> See [7], [17.a]-[17.g]. As discussed in [7], a POSITA would have understood Ahn’s memory device includes bit lines (data lines) coupled to “channel region (260),” where memory cell strings are located between the bit lines and substrate (100). Kuhn, ¶¶140-145. To allow selection of individual memory cells, a POSITA would have further understood (or found it obvious) the bit lines are coupled to the cell strings in a direction perpendicular to drain select lines DSL. Each drain select line DSL is able to select one row of cell strings (e.g., the front or back row in Figure 1) and bit lines perpendicular to the drain select lines DSL are able to select one column of cell strings (e.g., the left or right column of cell strings), such that any pair of drain select line DSL and bit line would select a unique cell string. Kuhn, ¶144. In this arrangement, the front-left and back-left memory strings would be between one bit line and the substrate, and the front-right and back-right memory strings would be between another bit line and the substrate. A POSITA would have at least found it obvious to arrange bit lines perpendicular to drain select lines DSL in Ahn’s memory

'903	Ahn
	device to advantageously select cell strings. Moreover, this approach was well-known. Kuhn, ¶145.⁶ A POSITA would thus have found it routine, straightforward and advantageous to place bit lines over and perpendicular to Ahn's drain select lines, and would have known that applying bit lines to Ahn's flash memory (yielding the claimed limitations) in this manner would predictably work and provide the expected functionality. Kuhn, ¶145. - Figure 1  - See also [0022], [0025]-[0026], [0037]-[0038], [0042]-[0044], [0046], [0048]-[0049]

⁶ Ex.1010, [0039], [0053], Fig. 1; Ex.1011, [0047]-[0055], Fig. 2.

'903	Ahn
[17.j] a first control gate formed in a first device level; [17.k] a second control gate formed in a second device level, wherein,	See [1.c]-[1.d]. Kuhn, ¶146.
[17.l] the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate;	Ahn discloses that the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate (e.g., front-left “cell string” including “memory cells” at the lowest and second lowest “conductive layer (220)” in Fig. 1, with “charge storage layer” formed on the inner wall of “through hole (230)” in those layers—see [17.d]-[17.g]). <u>E.g., Ahn:</u> See [1.b]-[1.d], [17.d]-[17.g], [17.j]-[17.k]. Further, as discussed in [1.c]-[1.d], Ahn discloses each cell string includes multiple memory cells arranged vertically, each including a charge trap layer on the inner wall of through hole (230) in conductive layer (220). Ahn, [0028], [0036], [0040]. Kuhn, ¶¶147-150. In Figure 1, in the front-left memory string, the lowest conductive layer (220) in combination with the charge trap layer form a first memory cell, and the second lowest conductive layer (220) in combination with the charge trap layer form a second memory cell. Kuhn, ¶150. • Figure 1

'903	Ahn
	 - Figure 7  - See also [0025]-[0026], [0028], [0036]-[0038], [0040], [0042]-[0043]

'903	Ahn
[17.m] the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate;	Ahn discloses that the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate (e.g., back-left “cell string” including “memory cells” at the lowest and second lowest “conductive layer (220)” in Fig. 1, with “charge storage layer” formed on the inner wall of “through hole (230)” in those layers—see [17.d]-[17.g]) . <u>E.g., Ahn:</u> See [1.b]-[1.d], [17.d]-[17.g], [17.j]-[17.l]. Further, the same analysis provided for [17.l] applies for this limitation, except third and fourth memory cells are in the back-left memory string of Fig. 1. Kuhn, ¶¶151-154. • Figure 1

'903	Ahn
	Second Memory Cell String Fourth Memory Cell String 300 310 DSL W/L(220) SSL 290 280 210 260 240 140 130 120 Substrate 160 110 170 P-Si Region including a conductive material Figure 7

'903	Ahn
[17.n] the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate (e.g., front-right “cell string” including “memory cells” at the lowest and second lowest “conductive layer (220)” in Fig. 1, with “charge storage layer” formed on the inner wall of “through hole (230)” in those layers—see [17.d]-[17.g]).	Ahn discloses that the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate (e.g., front-right “cell string” including “memory cells” at the lowest and second lowest “conductive layer (220)” in Fig. 1, with “charge storage layer” formed on the inner wall of “through hole (230)” in those layers—see [17.d]-[17.g]).
<u>E.g., Ahn:</u>	<u>E.g., Ahn:</u>
See [1.b]-[1.d], [17.d]-[17.g], [17.j]-[17.l]. Further, the same analysis provided for [17.l] applies for this limitation, except fifth and sixth memory cells are in the front-right memory string of Fig. 1. Kuhn, ¶¶155-158.	See [1.b]-[1.d], [17.d]-[17.g], [17.j]-[17.l]. Further, the same analysis provided for [17.l] applies for this limitation, except fifth and sixth memory cells are in the front-right memory string of Fig. 1. Kuhn, ¶¶155-158.
	• Figure 1 (see [17.l]) • Figure 7 (see [17.l])

'903	Ahn
[17.o] the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.	Ahn discloses that the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and a eighth memory cell having a memory element formed in a fourth cavity of the second control gate (e.g., back-right “cell string” including “memory cells” at the lowest and second lowest “conductive layer (220)” in Fig. 1, with “charge storage layer” formed on the inner wall of “through hole (230)” in those layers—<i>see</i> [17.d]-[17.g]) . <u>E.g., Ahn:</u> <i>See</i> [1.b]-[1.d], [17.d]-[17.g], [17.j]-[17.l]. Further, the same analysis provided for [17.l] applies for this limitation, except seventh and eighth memory cells are in the back-right memory string of Fig. 1. Kuhn, ¶¶159-162. • Figure 1 (<i>see</i> [17.m]) • Figure 7 (<i>see</i> [17.m])
[18] The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises polysilicon	<i>See</i> [8], [17]. Kuhn, ¶163.
[19] The apparatus of claim 17, wherein the	<i>See</i> [9], [17]. Kuhn, ¶164.

'903	Ahn
memory element of each of the first, second, third, and fourth memory cells comprises a silicon nitride.	
[20.a] The apparatus of claim 17, further comprising: a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells; [20.b] a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells; [20.c] a third conductive channel coupled	See [17]. Ahn discloses a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells, a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells, a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells, and a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells (e.g., four “channel region (260)” formed over four “channel region (170)” of Fig. 1, extending between “memory cells” at the lowest and second-lowest “conductive layers (220)” —see [17.a]-[17.b], [17.l]-[17.o]). <u>E.g., Ahn:</u> See [1.e], [17.a]-[17.b], [17.d]-[17.g], [17.l]-[17.o]. Further, as discussed in [1.e] and [17.d]-[17.g], the first, second, third, and fourth cell strings each include channel region (260) formed over and coupled to first, second, third, and fourth channel regions (170), respectively. Kuhn, ¶¶165-168. • Figure 1

'903	Ahn
to the third conductive pillar and extending between the fifth and sixth memory cells; and [20.d] a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells.	See also [0025], [0026], [0028], [0036], [0037], [0038], [0040], [0042], [0043]

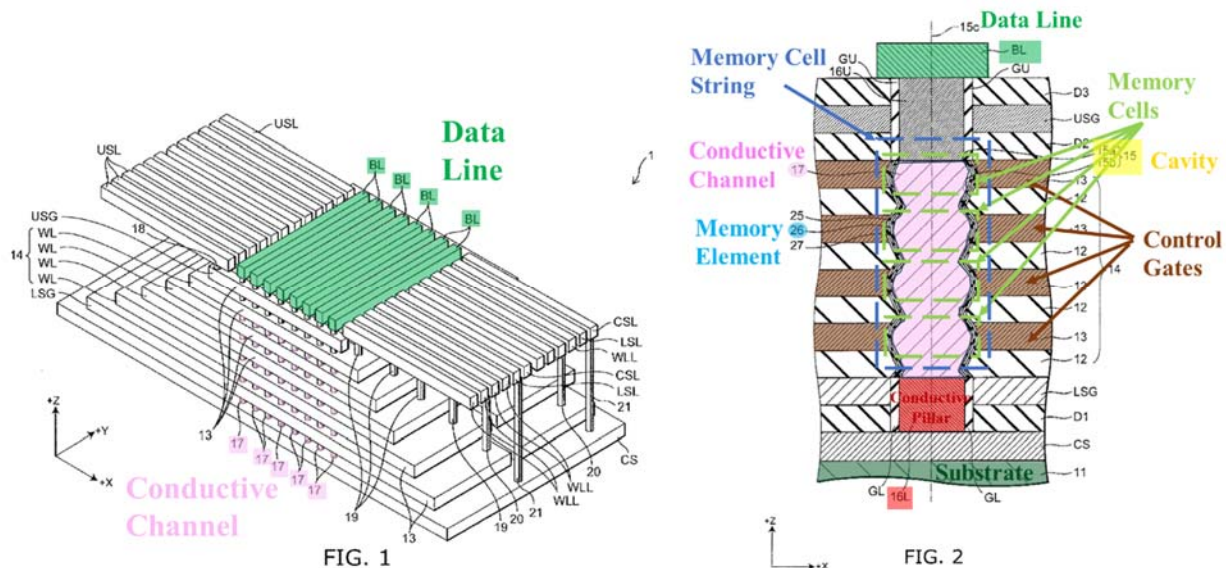
B. Ground 2: Ahn in view of Ishikawa (Claims 7, 17)

As discussed (§IX.A.2), Ahn teaches and at least renders obvious the “data line” limitations in claim 7 and [17.h]-[17.i]. Kuhn, ¶¶169-178.

To the extent additional disclosure is required for the “data line” limitations, Ishikawa discloses a data line (e.g., “bit interconnect BL”) coupled to a conductive channel (e.g., “semiconductor pillar 17”), wherein the first and second memory cells (e.g., “memory cells”) are located between the data line and the substrate (e.g., “substrate 11”) (claim 7); and a first data line (e.g., a first “bit

interconnect BL”) **coupled to first and second memory cell strings** (e.g., “memory strings” along the first bit interconnect BL), **the first and second memory cell strings located between the first data line and a substrate** (e.g., “substrate 11”) ([17.h]) and **a second data line** (e.g., a second “bit interconnect BL”) **coupled to third and fourth memory cell strings** (e.g., “memory strings” along the second bit interconnect BL), **the third and fourth memory cell strings located between the second data line and the substrate** (e.g., “silicon substrate 11”) ([17.i]). Kuhn, ¶170.

Ishikawa is directed to a three-dimensional nonvolatile semiconductor memory device. Ishikawa, [0003], [0007]-[0008].



In FIG. 1, **Ishikawa** discloses a plurality of **bit interconnects BL** extending in the Y direction, perpendicular to the upper select gate interconnects USL and

immediately above columnar electrode 16U of upper select gate USG. Ishikawa, [0033]-[0035], FIG. 2. As shown in FIG. 2, columnar electrode 16U is coupled to semiconductor pillar 17 underneath, which is formed above columnar electrode 16L (on substrate 11) and inside each through hole 15 of electrode films 13. Ishikawa, [0029], [0033]. Semiconductor pillar 17 is surrounded by dielectric layer 25, charge storage layer 26, and dielectric layer 27, forming a memory cell with electrode films 13 serving as control gates. Ishikawa, [0029]-[0030], [0033], [0050]. Kuhn, ¶¶171-172.

Ahn and Ishikawa are in the same field as the '903—which includes three-dimensional memory devices—and are reasonably pertinent to the problems addressed by '903, e.g., increasing density of memory devices. '903, 1:26-28; Ishikawa, [0005]-[0006]; Ahn, [0005]. Kuhn, ¶¶174-175.

A POSITA would have been motivated to apply Ishikawa's teachings of data lines to Ahn's memory device to advantageously read from, write to and erase individual memory cells. Kuhn, ¶¶173, 176. For example, Ishikawa discloses bit lines BL formed above upper select gates USG and perpendicular to upper select gate interconnects USL (i.e., drain select lines), such that “the X coordinate of a memory cell is selected by selecting a bit line BL” and “the Y coordinate can be selected by selecting an upper select gate USG,” allowing selection of a single memory cell string. Ishikawa, [0005], [0034], [0053]. Kuhn, ¶176. Combined with

selection of word line WL in the Z coordinate, this allows “one memory cell [to be] selected, and data is stored or erased by charge injection into or extraction” from each memory cell. Ishikawa, [0053]. Kuhn, ¶176. Accordingly, a POSITA would have been motivated to apply **Ishikawa’s** teachings of data lines to **Ahn’s** memory device, such that each data line is formed above drain select transistors and coupled to the cell strings underneath in a direction perpendicular to drain select lines DSL. Kuhn, ¶176.

A POSITA would have had a reasonable expectation of success applying **Ishikawa’s** teaching of data lines to **Ahn’s** memory device. As discussed (§IX.A.2, [7]), using data lines for data storage and erase was well-known in the art, and other than the minimal modification of adding data lines on top of **Ahn’s** memory device (to the extent not already there), no modification in Ahn’s manufacturing process would have been needed. Kuhn, ¶177.

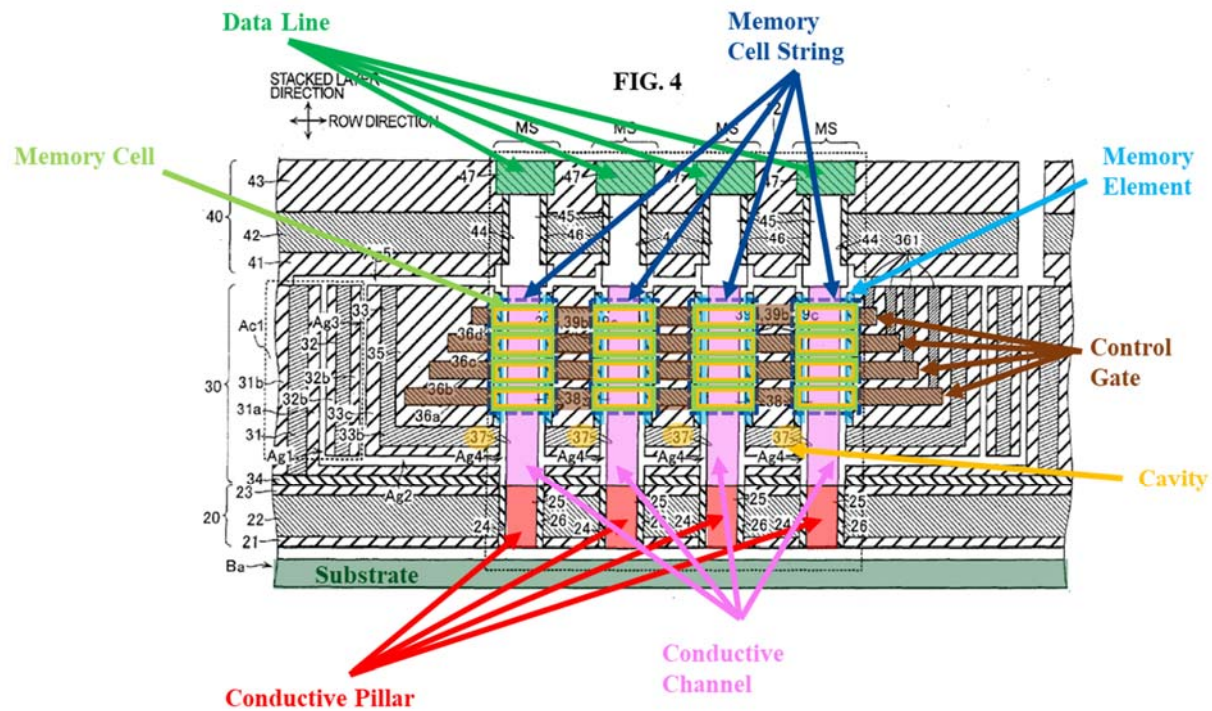
Thus, a POSITA would have found it routine, straightforward and advantageous to apply **Ishikawa’s** teaching of bit lines to **Ahn’s** memory device, and would have known such combination (yielding the claimed limitations) would predictably work and provide the expected resulting structure. Kuhn, ¶178.

C. Ground 3: Fukuzumi (Claims 1-3, 7, 9, 17, 19-20) (§§102/103)

Fukuzumi discloses and at least renders obvious the Claims, under both Petitioner’s and PO’s Constructions of the “cavity” limitations. Kuhn, ¶¶182-183.

1. Overview of Fukuzumi

Fukuzumi discloses a three-dimensional “nonvolatile semiconductor memory device.” Fukuzumi, [0002]-[0004]. FIG. 4 shows a cross-sectional view of an embodiment:



Fukuzumi, FIG 4.

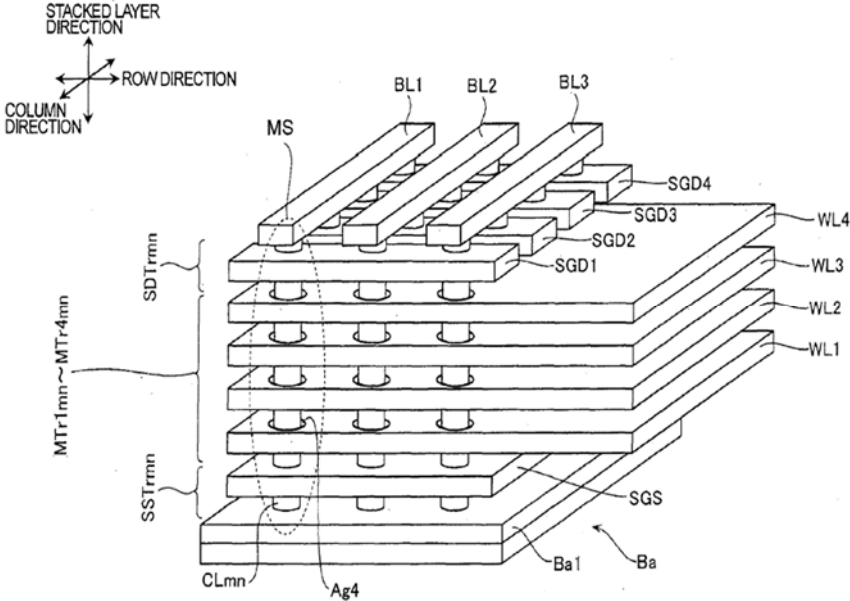
Fukuzumi’s memory device comprises a matrix of “memory strings MS” including **memory cells** **MTr1mn-MTr4mn**, where m and n indicate the **memory cells’** X- and Y-coordinates. Fukuzumi, [0079]. Each memory string MS includes columnar semiconductor CLmn comprising “**source-side columnar semiconductor layer 25**” formed on the “**substrate**,” “**memory 38**,” and “drain-

side columnar semiconductor layer 45” connecting **bit line layer 47** and **memories 38** along the column direction. Fukuzumi, [0086], [0088]-[0089], [0096], [0103], [0108]-[0109]. Kuhn, ¶¶179-180.

Memory cells MTr1mn-MTr4mn include **word lines WL1-WL4** (e.g., **word line conduction layer 36a-d**) “connected to each gate of the memory cells” and **charge storage layer 39b** formed on sidewalls of **word lines WL1-WL4** in **memory hole 37**. Fukuzumi, [0080], [0085]. Kuhn, ¶181.

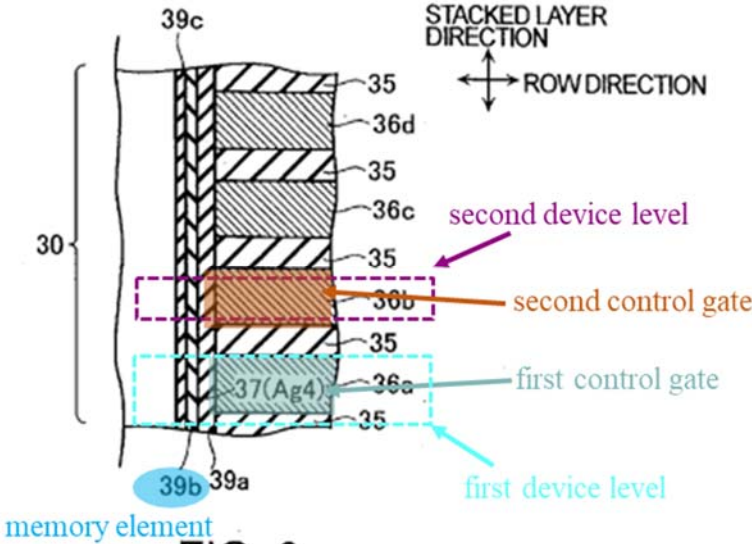
2. Claim Chart

'903	Fukuzumi
[1.pre] An apparatus comprising:	To the extent the preamble is limiting, Fukuzumi discloses an apparatus (e.g., “semiconductor memory device”). <u>E.g., Fukuzumi:</u> Fukuzumi discloses “nonvolatile semiconductor memory device.” Fukuzumi, [0093]. Kuhn, ¶¶184-186. • Figure 2

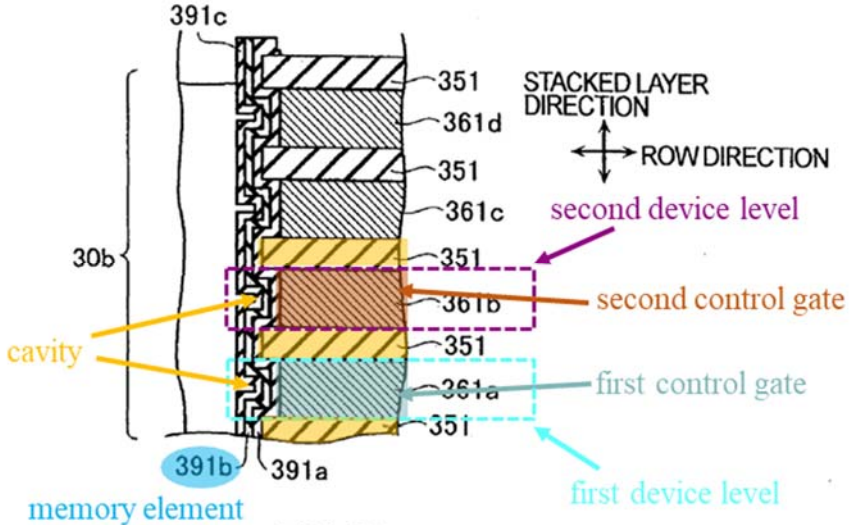
'903	Fukuzumi
	 • [0093] (“As shown in FIG. 4, <i>the nonvolatile semiconductor memory device 100</i>....”) • See also [0005], [0093]
[1.a] conductive pillars extending outward from a substrate;	Fukuzumi discloses conductive pillars (e.g., “source-side columnar semiconductor layer 25”; “source-side columnar semiconductor 25”) extending outward from a substrate (e.g., “formed to perpendicular the semiconductor substrate Ba”). <u>E.g., Fukuzumi:</u> Fukuzumi discloses source-side columnar semiconductor layers 25 extending perpendicular to (thus outward from) semiconductor substrate Ba. Fukuzumi, [0081], [0096], Fig. 4. Kuhn, ¶¶187-189. • Figure 2

'903	Fukuzumi
	FIG. 2 Figure 4

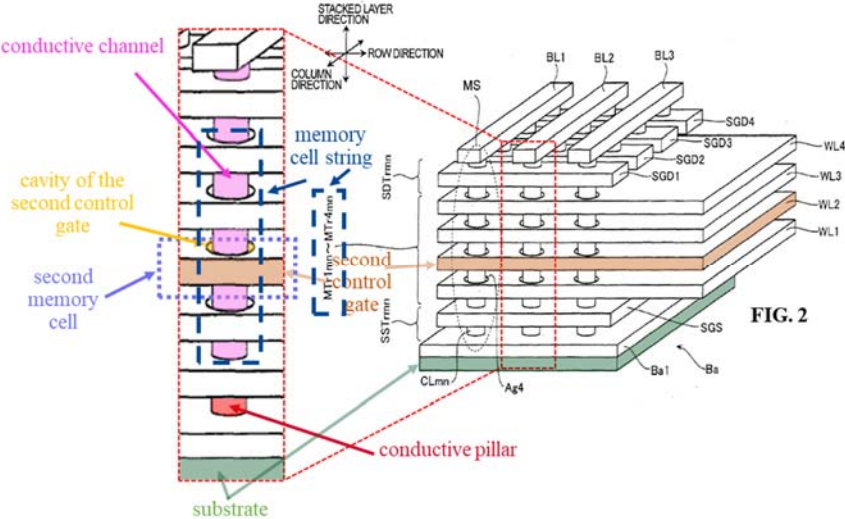
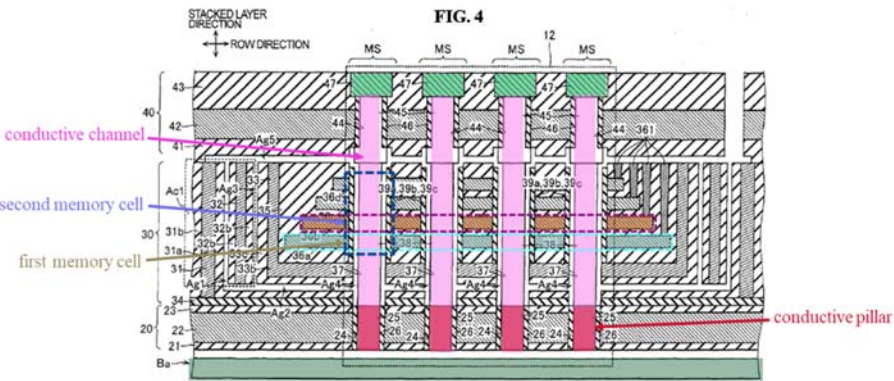
'903	Fukuzumi
	• [0079] (“...the memory cell region 12 includes $m \times n$ numbers (m and n being counting numbers) of memory strings MS being constituted with memory cells $MTr1mn-MTr4mn$....”) • [0081] (“Each of the memory strings MS includes columnar semiconductors $CLmn$ on a p-well region $Ba1$ formed in an n^+ region of a semiconductor substrate Ba. In FIG. 2, for example, m equals from 1 to 3 and n equals from 1 to 4....”) • [0103] (“Further, a memory hole 37 is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth word line conduction layers 36a-36d, the third frame bottom layer 33b, the third protective layer 33c, the first protective layer 31a and the isolation insulator 34. A memory 38 is formed at a portion as aligning the source-side columnar semiconductor 25 in the memory hole 37....”) • See also [0076]-[0078], [0080], [0085], [0093], [0104]
[1.c] a first control gate formed in a first device level, the memory cell strings	Fukuzumi discloses a first control gate formed in a first device level (e.g., “end portion” of “word line” $WL1$ “acts as a control gate”; “word line conduction layer” 36a), the memory cell strings including a memory cell string (e.g., “memory cells $MTr1mn-MTr4mn$”), the memory cell string including a first memory cell (e.g., “memory cell” at “word line” $WL1$) having a memory element (e.g., “charge storage layer” 39b)

'903	Fukuzumi
	 FIG. 6 [0079]: “...the memory cell region 12 includes $m \times n$ numbers (m and n being counting numbers) of memory strings MS being constituted with memory cells $MTr1mn$-$MTr4mn$....” [0080] (“Each of the word lines $WL1$-$WL4$ is connected to each gate of the memory cells $MTr1 mn$-$MTr4 mn$ in each of the memory strings MS and each of the word lines $WL1$-$WL4$ are formed of the same conductive layer and are common in plane each other. The memory cell $MTr1 mn$ in each of the memory strings MS has a structure of a transistor and all gates of memory cells $MTr1 mn$ are connected to a word line $WL1$. Further, all gates of memory cells $MTr2 mn$ in each of the memory strings MS are connected to a word line $WL2$....”) [0087] (“...An end portion of the word line WL contacting with the charge storage layer surrounded by the insulator act as a control gate of the memory cell $Mtrmn$....”) [0101] (“...The first-fourth word line conduction layer layers 36 a-36 d act as the word lines $WL1$-$WL4$....”)

'903	Fukuzumi
	• [0104] (“...a block insulation layer 39a, <i>a charge storage layer 39b</i> and a tunnel insulation layer 39c are <i>formed on sidewalls of the first-fourth word line conduction layers 36a-36d in the memory hole 37</i> in order....”) • See also [0090], [0103], [0114]. To the extent “cavity of the first control gate” requires the memory hole in the control gate to have a larger diameter than holes in the layers above and below the control gate, Fukuzumi’s second embodiment discloses “charge storage layer 391b” is formed as “a concavo-convex shape accompanying” word line conduction layer 361a. Fukuzumi, [0148]. In this embodiment, interlayer layers 351 above and below word line conduction layer 361a have holes with smaller diameters than memory hole in word line conduction layer 361a. While Figure 28 illustrating the second embodiment shows only the word line conduction layer 361, interlayer layers 351, and block insulation layer 391a, a charge storage layer 391b and a tunnel insulation layer 391c, Fukuzumi explains the omitted parts are “the same or similar” as the first embodiment discussed in the rest of this Ground. Fukuzumi, [0146]-[0151], Fig. 28. A POSITA would thus have understood (or at least found it obvious) that the analysis for other limitations relying on the first embodiment of Fukuzumi applies equally to Fukuzumi’s second embodiment. [0146]. Kuhn, ¶¶199-200. • Figure 28

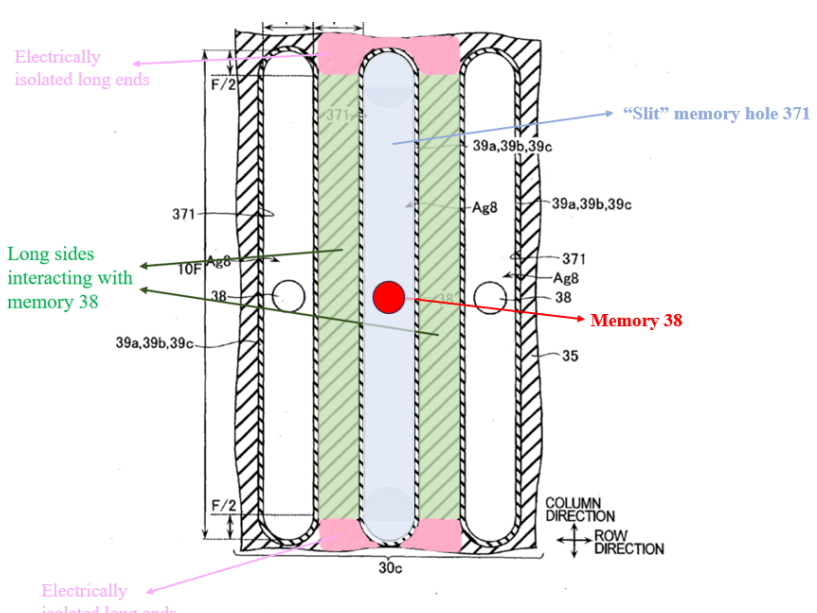
'903	Fukuzumi
	 FIG. 28 [0146] (“...FIG. 28 is a partially enlarged cross-sectional schematic view showing the nonvolatile memory semiconductor device according to the second embodiment. It is to be noted that the same or similar reference numerals in the second embodiment are applied to the same or similar parts and elements throughout the drawings as the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified.”) [0148] (“...A sidewall of first-fourth word line conduction layers 361a-361d faced to the fourth space Ag4 are formed as recesses corresponding to a side wall of an interlayer insulator 351. Further, surfaces of a block insulation layer 391 a, a charge storage layer 391 b and a tunnel insulation layer 391 c faced to the fourth space Ag4 (not illustrated) are formed as a concavo-convex shape accompanying with the first-fourth word line conduction layer 361a-361d.”) - See also [0200]
[1.d] a second control gate	Fukuzumi discloses a second control gate formed in a second device level (e.g., “end portion” of “word line” WL2 or “word

'903	Fukuzumi
formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the second control gate; and	line conduction layer” 36b “acts as a control gate”), the memory cell strings (e.g., “memory cells MTr1 <i>mn</i>-MTr4 <i>mn</i>”) including a memory cell string, the memory cell string including a second memory cell (e.g., “memory cell” at “word line” WL2) having a memory element (e.g., “charge storage layer” 39b) formed in a cavity (e.g., “memory hole 37”) of the second control gate. <u>E.g., Fukuzumi:</u> See [1.b]-[1.c]. Fukuzumi further discloses a second device level where second word line conduction layer 36b or WL2 is located, and a memory cell includes charge storage layer 39b formed on second word line conduction layer 36b in memory hole 37. Fukuzumi, [0080], [0101], [0103]-[0104]. Kuhn, ¶¶201-204. • Figure 2 (<i>see</i> [1.c]) • Figure 6 (<i>see</i> [1.c]) • <i>See also</i> [0079]-[0080], [0087], [0090], [0101], [0104], [0114] As explained in [1.c], to the extent “cavity of the second control gate” requires the memory hole in the control gate to have a larger diameter than holes in layers above and below the control gate, Fukuzumi discloses cavity meeting this definition. <i>See</i> [1.c]. Kuhn, ¶205.
[1.e] a conductive channel extending between the first memory cell and the second memory cell and electrically	Fukuzumi discloses a conductive channel (e.g., “memory 38”) extending between the first memory cell and the second memory cell (e.g., “memory cells” at “word lines” WL1 and WL2) and electrically coupled to a conductive pillar of the conductive pillars (e.g., formed on and “aligning the source-side columnar semiconductor 25” as illustrated in Fig. 4). <u>E.g., Fukuzumi:</u> See [1.a]-[1.d]. Fukuzumi further discloses silicon “memory 38[] formed at a portion aligning the source-side columnar

'903	Fukuzumi
coupled to a conductive pillar of the conductive pillars.	semiconductor 25 in the memory hole 37," which penetrates through the memory cells at word lines WL1 and WL2. Fukuzumi, [0103]. The memory cells (including memory 38 forming the conductive channel) and source-side selection transistors SSTrmn "are serially connected" such that memory 38 in the memory cells and source-side columnar semiconductor 25 in source-side selection transistors SSTrmn are electrically coupled. Fukuzumi, [0085]. Kuhn, ¶¶206-209. - Figure 2  FIG. 2 - Figure 4  FIG. 4 [0085] ("...<i>These four memory cells MTr1 mn-MTr4 mn, the source-side selection transistors SSTrm and the</i>

'903	Fukuzumi
	<i>drain side selection transistor SDtrmn are serially connected....”)</i> • [0086] (“...As shown in FIG. 4, in the first embodiment of the memory strings MS, the columnar semiconductor CLmn is formed on an n+-region formed in a p-type region (p-Well region) Ba1 of a semiconductor substrate Ba. Thus, source line SL is connected to a source of the source-side selection transistors SStrmn....”) • [0087] (“Each of the memory cells Mtrmm includes the columnar semiconductor CLmn....”) • [0103] (“...a memory hole 37 is configured at a portion as aligning the source-side columnar semiconductor 25 to pass through the interlayer insulator 35, the first-fourth wordline conduction layers 36a-36d....A memory 38 is formed at a portion as aligning the source-side columnar semiconductor 25 in the memory hole 37....”) • See also [0088]-[0089], [0104].
[2.a] The apparatus of claim 1, further comprising: a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material; and	See [1]. Fukuzumi discloses a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material, and a second conductive region located on a second side of the conductive pillar and separated from the conductive pillar by a second dielectric material (e.g., portions of “source-side conductive layer 22” located on the left and right sides of “source-side columnar semiconductor layer 25,” respectively, and portions of “source-side gate insulation layer 26” respectively separating the left and right sides of “source-side conductive layer 22” from “source-side columnar semiconductor layer 25,” as shown in Fig. 4). <u>E.g., Fukuzumi:</u> See [1.a]. Fukuzumi also discloses source-side hole 24 passing through source-side conductive layer 22, and source-side

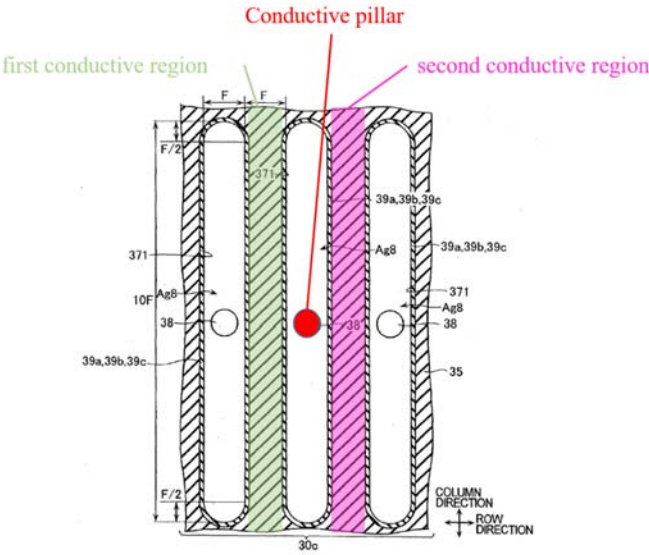
'903	Fukuzumi
[2.b] a second conductive region located on a second side opposite from the first side of the conductive pillar and separated from the conductive pillar by a second dielectric material.	columnar semiconductor layer 25 located in source-side hole 24, such that first and second regions of source-side conductive layer 22 are on the left and right sides of source-side columnar semiconductor layer 25, respectively, as shown in Fig. 4. Fukuzumi, [0096], Fig. 4. Kuhn, ¶¶210-213. Fukuzumi further discloses “source-side gate insulation layer 26[] formed between a sidewall of the source-side columnar semiconductor layer 25 and...the source-side conductive layer 22,” such that first and second portions of source-side gate insulation layer 26 separate the first and second regions of source-side conductive layer 22 from source-side columnar semiconductor layer 25. Fukuzumi, [0096]. Kuhn, ¶213. Moreover, PO accuses the same structure in NDCA Case as satisfying this limitation.. Ex.1018, Ex.D at 6-8. Kuhn, ¶214. - Figure 4 [0096] (“Further, the source-side selection transistor layer 20 includes a source-side hole 24 passing through the first source-side insulation layer 21, the source-side conductive layer 22, the second source-side insulation layer 23 and a source-side columnar semiconductor layer 25. A source-side gate insulation layer 26 is formed between a sidewall of the source-side columnar semiconductor layer 25 and the first source-side

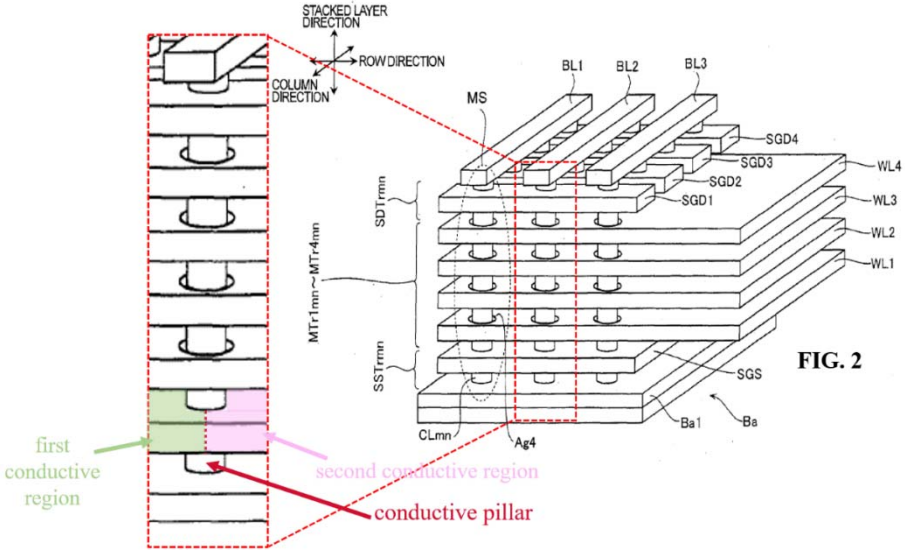
'903	Fukuzumi
	<i>insulation layer 21, the source-side conductive layer 22 and the second source-side insulation layer 2....The source-side gate insulation layer 26 is formed of silicon-dioxide.”)</i> To the extent “a second conductive region located on a second side opposite from the first side of the conductive pillar” requires the first and second conductive regions to be located on opposite sides of the conductive pillar, and otherwise electrically isolated from the pillar, Fukuzumi teaches (or at least renders obvious) the limitation. Kuhn, ¶215. For example, Fukuzumi’s third embodiment discloses a “slit” memory hole 371 where “both ends of the row direction in the memory hole 371 are formed like a line.” Fukuzumi, [0155], Fig. 29.  FIG. 29 As illustrated above, in this structure, word line conduction layers 36a-d on two opposite long sides of slit memory hole 371 electrically interact with memory 38, while portions of 36a-d at the long ends of slit memory hole 371 are electrically isolated

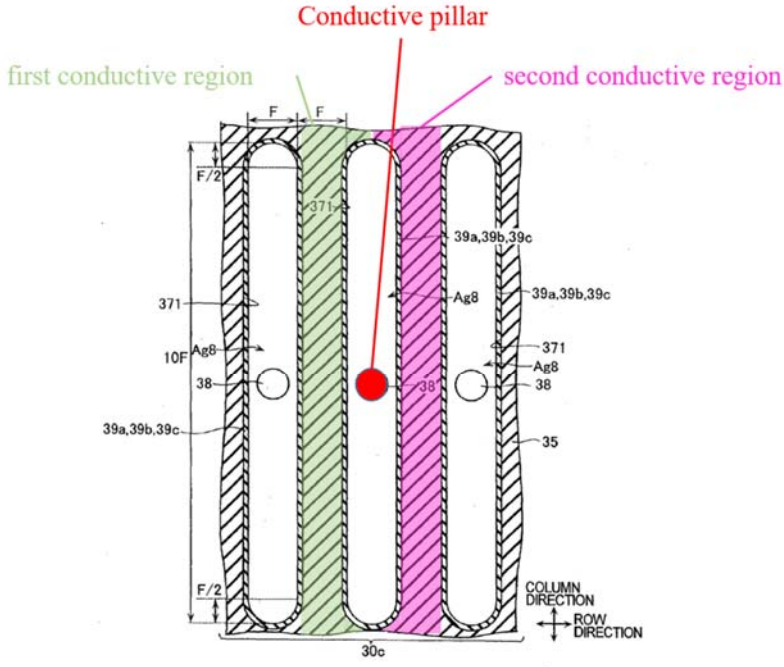
'903	Fukuzumi
	from and do not impact the operation of memory 38. Fukuzumi, [0155], Fig. 29. Kuhn, ¶¶215-217. A POSITA would have understood (or at least found it obvious) that the same “slit” structure would also be used for source-side hole 24, as illustrated below. Fukuzumi, [0153], [0200]. Kuhn, ¶218. The diagram illustrates a cross-sectional view of a memory string. A central vertical structure, labeled 'Source-side columnar semiconductor 25', passes through a 'Memory portion' and a 'Source-side selection transistor' region. A 'Slit memory hole 371' is formed in the memory portion, and a 'Source side hole 24' is formed in the source-side selection transistor. Both holes share the same vertical alignment and are part of a continuous structure. Labels with arrows point to 'Slit memory hole 371', 'Memory 38', 'Source side hole 24', and 'Source-side columnar semiconductor 25'. Brackets on the right indicate the 'Memory portion' and 'Source-side selection transistor' regions. Using the same slit memory hole structure for source-side hole 24 would advantageously allow the source-selection and memory transistors in a memory string to be formed using the same hole, thereby simplifying manufacturing.⁷ Kuhn, ¶219. In this implementation, portions of source-side gate insulation layer 26 separate the regions of source-side conductive layer 22 from source-side columnar semiconductor layer 25. Kuhn, ¶219. A POSITA would have had a reasonable expectation of success in applying “slit” hole structure to the source-side hole 24, as the use of such structure for source-side selection transistors was well-known in the art.⁸ Kuhn, ¶220. Fukuzumi explains parts other than the slit memory hole structure omitted in the third embodiment are “the same or similar” as the first embodiment discussed in the rest of this Ground. Fukuzumi, [0153], Fig. 29. A POSITA would thus

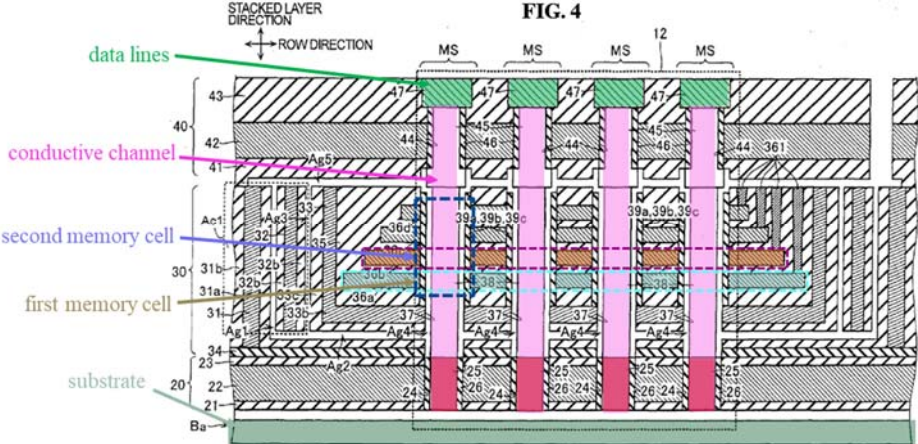
⁷ Ex. 1026, [0034], [0036], [0042]-[0043], [0062], [0066]-[0067], [0142].

⁸ Ex.1012, [0103]-[0106], Figs. 31, 36, 37.

'903	Fukuzumi
	have understood (or at least found it obvious) that the analysis for other limitations relying on the first embodiment of Fukuzumi applies equally to Fukuzumi's third embodiment modified to include "slit" source-side hole 24 structure. [0153]. Kuhn, ¶221. - Figure 29 (as applied to source-side selection transistor)  FIG. 29 [0153] (“...FIG. 29 is a part of plain schematic view showing a memory layer of the non-volatile memory semiconductor device according to the third embodiment. It is to be noted that the same or similar reference numerals in the third embodiment are applied to the same or similar parts and elements throughout the drawings in the first embodiment, and the description of the same or similar parts and elements will be omitted or simplified.”) [0155] (“The memory hole 371 is formed like a slit which has the row-direction as lateral direction and the column direction as longitudinal direction from top view. Both ends of the row direction in the memory hole 371 are formed like a line. On the other hand, the column

'903	Fukuzumi
	<i>direction of the memory hole 371 is formed like a circular arc....”).</i> • See also [0200]
[3] The apparatus of claim 2, wherein the first conductive region is coupled to the second conductive region.	See [2]. Fukuzumi discloses the first conductive region (e.g., left portion of “source-side conductive layer 22” in Fig. 4) is coupled to the second conductive region (e.g., right portion of “source-side conductive layer 22” in Fig. 4). <u>E.g., Fukuzumi:</u> See [2.a]-[2.b]. As explained in [2.b], Fukuzumi discloses (or at least renders obvious) source-side conductive layer 22 surrounding source-side columnar semiconductor layer 25, such that portions of source-side conductive layer 22 on the first and second sides of source-side columnar semiconductor layer 25 are coupled. Fukuzumi, [0096], [0155]; Figs. 2, 29. Kuhn, ¶¶222-225. PO accuses the same structure in NDCA Case as satisfying this limitation. Ex. 1018, Ex.D-2 at 8-9. Kuhn, ¶226. • Figure 2  FIG. 2 • Figure 29

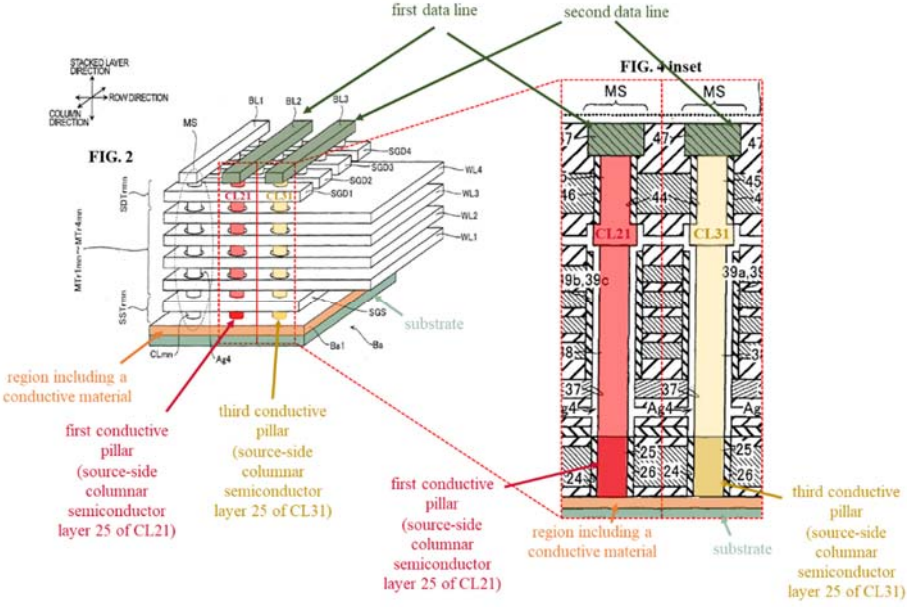
'903	Fukuzumi
	 FIG. 29 See also [0096], [0153], [0155].
[7] The apparatus of claim 1, further comprising a data line coupled to the conductive channel, wherein the first and second memory cells are located between the data line and the substrate.	See [1]. Fukuzumi discloses a data line (e.g., “bit line layer 47”) coupled to the conductive channel (e.g., coupled to “memory 38” through drain side columnar semiconductor layer 45), wherein the first and second memory cells (e.g., “memory cells” at “word lines” WL1 and WL2) are located between the data line and the substrate (e.g., between “bit line layer 47” and “substrate Ba”). <u>E.g., Fukuzumi:</u> See [1.a]-[1.e]. Fukuzumi also discloses bit line layers 47 formed on drain-side columnar semiconductor layer 45, which is located on memory 38 such that bit line layers 47 are coupled to memory 38 by drain-side columnar semiconductor layer 45. Fukuzumi, [0085], [0089], [0108]-[0109], Fig. 4. Moreover, the first and second memory cells located at WL1 and WL2 along

'903	Fukuzumi
	memory 38 are located between bit line layer 47 and substrate Ba. Fukuzumi, Fig. 4. Kuhn, ¶¶227-230. <u>See, e.g.:</u> - Figure 4  [0085] (“...<i>These four memory cells MTr1mn-MTr4mn, the source-side selection transistors SSTrm and the drain side selection transistor SDTrmn are serially connected each other....</i>”) [0089] (“<i>The drain-side selection transistors SDTrmn include the columnar semiconductors CLmn....</i>”) [0108] (“Further, <i>the drain-side selection transistor layer 40...include a drain-side hole 44 and a drain-side columnar semiconductor layer 45 formed in the drain-side hole 44....</i>”) [0109] (“A bit line layer 47 is formed at a portion being aligned with the drain-side columnar semiconductor layer 45 and an upper portion of the drain-side columnar semiconductor layer 45. The bit line layer 47 acts as the bit line BL as shown in FIG. 2.”) - See also [0081], [0083], [0086]-[0087], [0103]-[0104], Figs. 2-3.
[9] The apparatus of	See [1].

'903	Fukuzumi
claim 1, wherein the memory element comprises a dielectric material.	Fukuzumi discloses that the memory element (e.g., “charge storage layer 39b”) comprises a dielectric material (e.g., “silicon-nitride (SiN)”). <u>E.g., Fukuzumi:</u> See [1.c]. Fukuzumi further discloses charge storage layer 39b formed of silicon nitride, a dielectric material.⁹ Fukuzumi, [0104]. Kuhn, ¶¶231-234. • [0104] (“...The charge storage layer 39 b is formed of <i>silicon-nitride (SiN)</i>....”)
[17.pre] An apparatus comprising:	See [1.pre]. Kuhn, ¶235.
[17.a] a first conductive pillar and a second conductive pillar extending outward from a substrate; [17.b] a third conductive pillar and a fourth conductive pillars extending	Fukuzumi discloses a first conductive pillar, a second conductive pillar, a third conductive pillar, and a fourth conductive pillar (e.g., “source-side columnar semiconductor layer 25” of columnar semiconductors CL21, CL22, CL31, and CL32, respectively) extending outward from the substrate (e.g., “substrate Ba”). <u>E.g., Fukuzumi:</u> See [1.a]. Fukuzumi further discloses columnar semiconductors CL_m_n including source-side columnar semiconductor layers 25 at their lower ends “displaced like a matrix” on semiconductor substrate Ba—CL11 refers to the columnar semiconductor in the first column and first row, CL12 refers to the first column and second row, CL21 refers to the second column and first row, etc. Fukuzumi, [0081], [0088], [0096], [0103], Fig. 2; <i>see</i> [7]. For example, first and second source-side columnar semiconductor layers 25 at lower ends of CL21 and CL22 are arranged in the column-direction, as are third and fourth source-

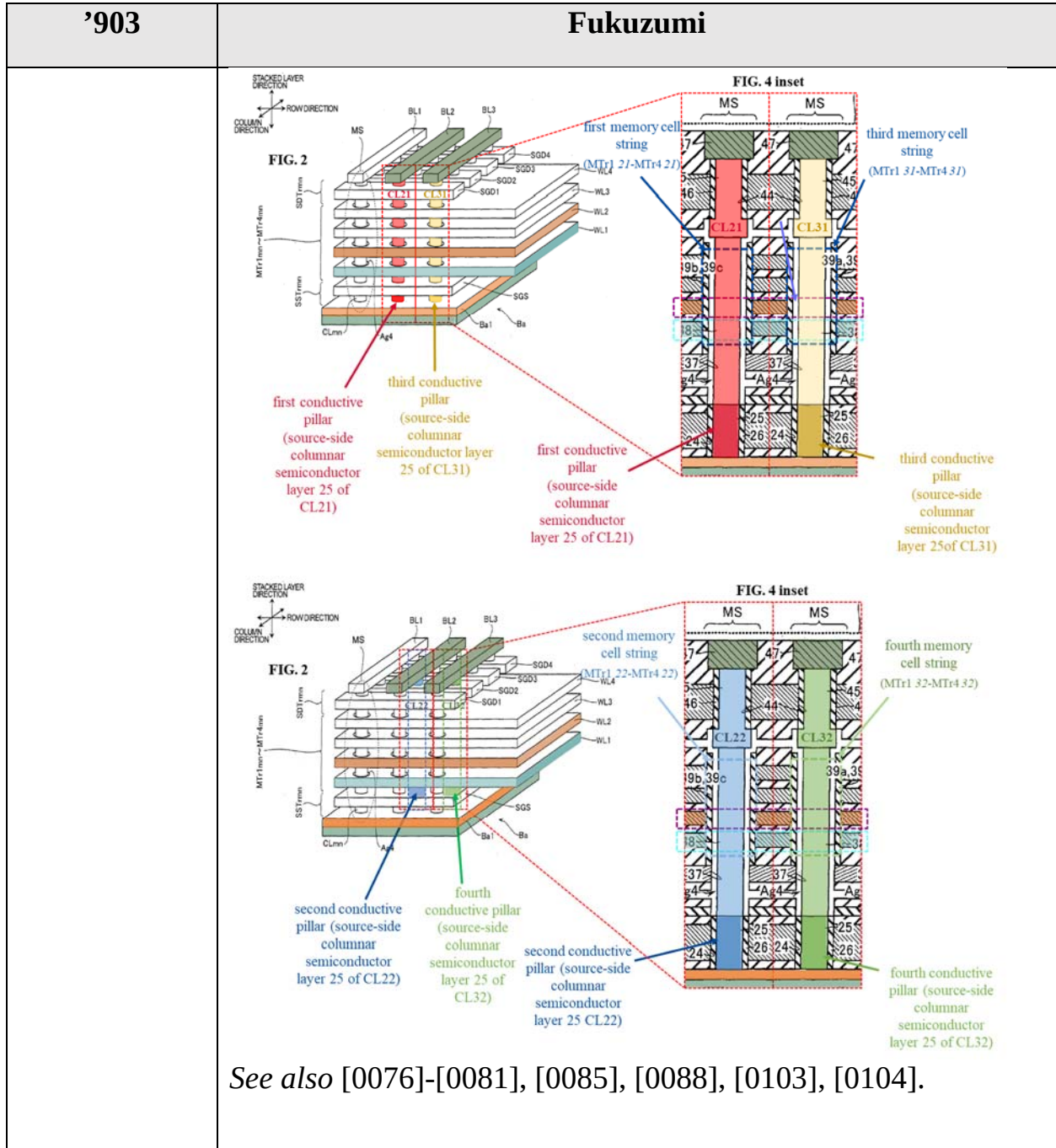
⁹ Ex.1019, [0071].

'903	Fukuzumi
outward from the substrate;	side columnar semiconductor layers 25 at lower ends of CL31 and CL32. Fukuzumi, Fig. 2. Kuhn, ¶¶236-239. - Figures 2&4 The diagrams illustrate a semiconductor device structure. FIG. 2 is a perspective view showing a stack of layers (WL1, WL2, WL3, WL4) on a substrate. Conductive pillars (CL21, CL31) are formed through the layers. FIG. 4 inset shows a cross-sectional view of the pillars, highlighting the source-side columnar semiconductor layers (25) at the base of the pillars. Labels include: first conductive pillar (source-side columnar semiconductor layer 25 of CL21), third conductive pillar (source-side columnar semiconductor layer 25 of CL31), second conductive pillar (source-side columnar semiconductor layer 25 of CL22), and fourth conductive pillar (source-side columnar semiconductor layer 25 of CL32). Other labels include MS, BL1, BL2, BL3, SOD1, SOD2, SOD3, SOD4, WL1, WL2, WL3, WL4, substrate, Ba1, Ba, Ag, and various numerical identifiers (e.g., 24, 25, 26, 37, 38, 39a, 39b, 39c, 44, 45, 46, 47). - See also Abstract, [0081], [0088], [0095], [0096], [0116].
[17.c] a region including a conductive	Fukuzumi discloses a region including a conductive material (e.g., “p-well region Ba1”), the region coupled to the first, second, third, and fourth conductive pillars (e.g., “source-

'903	Fukuzumi
material, the region coupled to the first, second, third, and fourth conductive pillars, the region located between substrate and the first, second, third, and fourth conductive pillars;	side columnar semiconductor layer 25” of columnar semiconductors CL21, CL22, CL31, and CL32 formed on “region Ba1”), the region located between substrate (e.g., “substrate Ba”) and the first, second, third, and fourth conductive pillars. <u>E.g., Fukuzumi:</u> See [1.a]. Fukuzumi further discloses a “p-well region Ba1” formed on semiconductor substrate Ba in an n+ region, where source-side columnar semiconductor layers 25, e.g., lower ends of CL21, CL22, CL31, CL32, are formed on Ba1. Fukuzumi, [0081], [0088], [0116]. Kuhn, ¶¶240-243. Figures 2&4  FIG. 2 is a perspective view of a semiconductor device. It shows a substrate (Ba) with a p-well region (Ba1) formed on its surface. A first conductive pillar (source-side columnar semiconductor layer 25 of CL21) and a third conductive pillar (source-side columnar semiconductor layer 25 of CL31) are formed on Ba1. A region including a conductive material is also shown. The device includes multiple layers: a first layer (WL1), a second layer (WL2), a third layer (WL3), and a fourth layer (WL4). A first data line (DL1) and a second data line (DL2) are formed on the top surface. A first conductive pillar (source-side columnar semiconductor layer 25 of CL21) and a third conductive pillar (source-side columnar semiconductor layer 25 of CL31) are formed on the substrate. A region including a conductive material is also shown. The device includes multiple layers: a first layer (WL1), a second layer (WL2), a third layer (WL3), and a fourth layer (WL4). A first data line (DL1) and a second data line (DL2) are formed on the top surface. FIG. 4 Inset is a cross-sectional view of the semiconductor device. It shows a substrate (Ba) with a p-well region (Ba1) formed on its surface. A first conductive pillar (source-side columnar semiconductor layer 25 of CL21) and a third conductive pillar (source-side columnar semiconductor layer 25 of CL31) are formed on Ba1. A region including a conductive material is also shown. The device includes multiple layers: a first layer (WL1), a second layer (WL2), a third layer (WL3), and a fourth layer (WL4). A first data line (DL1) and a second data line (DL2) are formed on the top surface. A first conductive pillar (source-side columnar semiconductor layer 25 of CL21) and a third conductive pillar (source-side columnar semiconductor layer 25 of CL31) are formed on the substrate. A region including a conductive material is also shown. The device includes multiple layers: a first layer (WL1), a second layer (WL2), a third layer (WL3), and a fourth layer (WL4). A first data line (DL1) and a second data line (DL2) are formed on the top surface.

'903	Fukuzumi
	FIG. 2 FIG. 4 inset first data line second data line region including a conductive material second conductive pillar (source-side columnar semiconductor layer 25 of CL22) fourth conductive pillar (source-side columnar semiconductor layer 25 of CL32) region including a conductive material fourth conductive pillar (source-side columnar semiconductor layer 25 of CL32) See also Abstract, [0081], [0088], [0095], [0096], [0116].

'903	Fukuzumi
[17.d] a first memory cell string formed over the first conductive pillar; [17.e] a second memory cell string formed over the second conductive pillar; [17.f] a third memory cell string formed over the third conductive pillar; [17.g] a fourth memory cell string formed over the fourth conductive pillar;	Fukuzumi discloses a first memory cell string formed over the first conductive pillar, a second memory cell string formed over the second conductive pillar, a third memory cell string formed over the third conductive pillar, a fourth memory cell string formed over the fourth conductive pillar (e.g. “memory cells” MTr1mn-MTr4mn over “source-side columnar semiconductor layer 25” of columnar semiconductors CL21, CL22, CL31, and CL32—see [17.a]-[17.b]). <u>E.g., Fukuzumi:</u> See [1.a]-[1.b], [17.a]-[17.c]. Fukuzumi further discloses each memory cell MTr1mn-MTr4mn in “memory hole 37” “formed at a portion as aligning” and above “source-side columnar semiconductor 25.” Fukuzumi, [0087], [0093], [0103]. Specifically, each memory cell MTr1mn-MTr4mn includes memory 38 of columnar semiconductor CLmn formed above and “aligning the source-side columnar semiconductor 25 in the memory hole.” Fukuzumi, [0087], [0103]-[0104], Fig. 2. For example, first memory string (MTr121-MTr421) is formed above first source-side columnar semiconductor layer 25 of columnar semiconductor CL21. Similarly, second (MTr122-MTr422), third (MTr131-MTr431), and fourth (MTr132-MTr432) memory strings are formed above source-side columnar semiconductor layers 25 of columnar semiconductors CL22, CL31, and CL32, respectively. Kuhn, ¶¶244-247. • Figures 2&4



'903	Fukuzumi
[17.h] a first data line coupled to the first and second memory cell strings, the first and second memory cell strings located between the first data line and the substrate; [17.i] a second data line coupled to the third and fourth memory cell strings, the third and fourth memory cell strings located between the second data line and the substrate;	Fukuzumi discloses a first data line (e.g., “bit line BL”) coupled to the first and second memory cell strings (e.g., “memory cells” MTr121-MTr421 and MTr122-MTr422), the first and second memory cell strings located between the first data line and the substrate (e.g., “substrate Ba”). Fukuzumi also discloses a second data line (e.g., “bit line BL”) coupled to the third and fourth memory cell strings (e.g., “memory cells” MTr131-MTr431 and MTr132-MTr432), the third and fourth memory cell strings located between the second data line and the substrate (e.g., “substrate Ba”). <u>E.g., Fukuzumi:</u> See [7], [17.a]-[17.g]. As discussed in [7], Fukuzumi discloses bit line layers 47 coupled to memory 38 of memory cells such that memory cells are located between bit line layers 47 and substrate Ba. Fukuzumi, [0085], [0109], Fig. 2. Kuhn, ¶¶248-251. Moreover, bit lines BL (bit line layers 47) extend in the column direction—one bit line BL is coupled to first (MTr121-MTr421) and second (MTr122-MTr422) memory strings, and a second bit line BL is coupled to third (MTr131-MTr431) and fourth (MTr132-MTr432) memory strings. Fukuzumi, Fig. 2. Kuhn, ¶251. • Figures 2&4

'903

Fukuzumi

first data line

second data line

FIG. 2

MS

BL1

BL2

BL3

SOD4

SOD3

SOD2

SOD1

WL3

WL2

WL1

SGS

substrate

CLnn

Ag4

Ba1

Ba

MT1 1m1-MT1 4m1

SS1 1m1-SS1 4m1

FIG. 3 Inset

MS

MS

first memory cell string (MT1 21-MT1 4 21)

third memory cell string (MT1 31-MT1 4 31)

CL21

CL31

47

46

45

44

39b

39c

38

37

36

35

34

25

26

24

Ag4

Ag

substrate

first data line

second data line

FIG. 2

MS

BL1

BL2

BL3

SOD4

SOD3

SOD2

SOD1

WL4

WL3

WL2

WL1

SGS

substrate

CLnn

Ag4

Ba1

Ba

MT1 1m1-MT1 4m1

SS1 1m1-SS1 4m1

FIG. 4 Inset

MS

MS

second memory cell string (MT1 22-MT1 4 22)

fourth memory cell string (MT1 32-MT1 4 32)

CL22

CL32

47

46

45

44

39b

39c

38

37

36

35

34

25

26

24

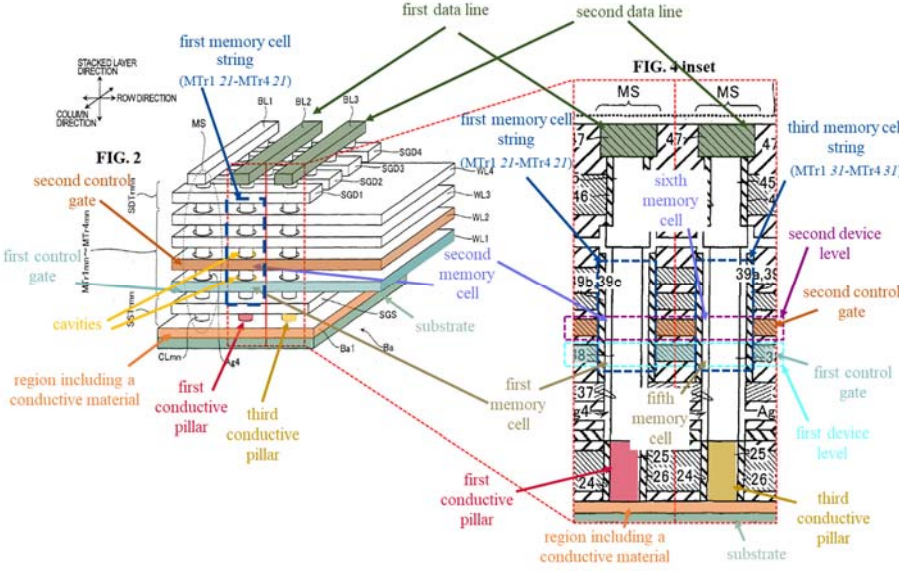
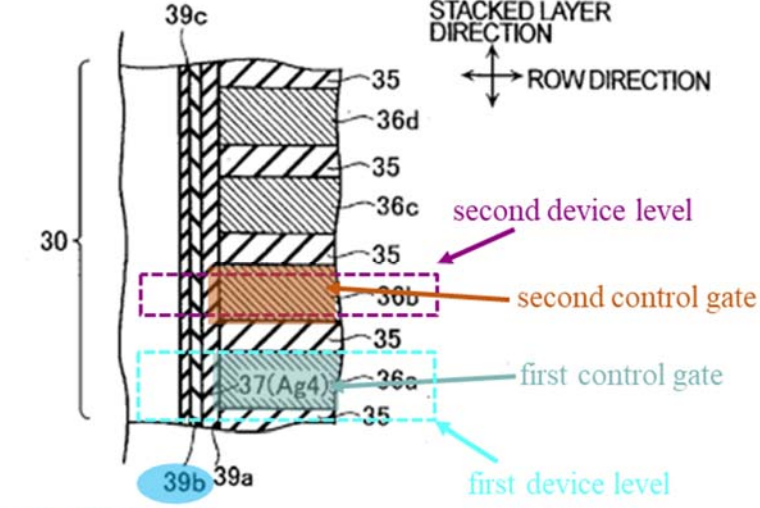
Ag4

Ag

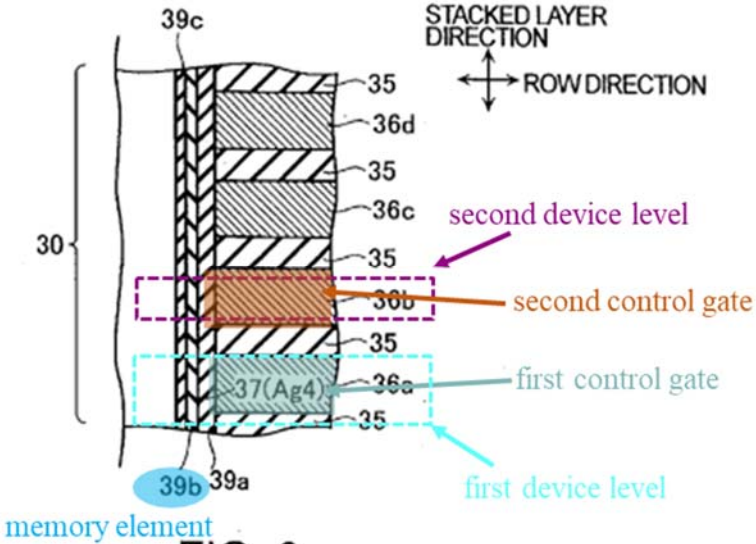
substrate

- See also [0081], [0083], [0085], [0086], [0087]-[0089], [0103]-[0104], [0108]-[0109].

'903	Fukuzumi
[17.j] a first control gate formed in a first device level; [17.k] a second control gate formed in a second device level, wherein,	See [1.c]-[1.d]. Kuhn, ¶252.
[17.l] the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate;	Fukuzumi discloses the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate (e.g., “memory cells” MTr121-MTr421 including “memory cells” MTr121 and MTr221 having “charge storage layer 391 b” formed in “memory hole 37” of “end portion” of “word line” WL1 and WL2, or “word line conduction layer” 36a and 36b, respectively). <u>E.g., Fukuzumi:</u> See [1.b]-[1.d], [17.d]-[17.g], [17.j]-[17.k]. As discussed in [1.c]-[1.d], Fukuzumi discloses each string of memory cells MTr1mn-MTr4mn includes memory cells with “charge storage layer 391b” in respective memory holes 37 of “end portion of the word line[s]” WL1-WL4. Fukuzumi, [0080], [0087], [0101]. Kuhn, ¶¶253-256. As further discussed in [1.c]-[1.d], this is also the case to the extent “cavity of the first control gate” requires the memory hole in the control gate to have a larger diameter than layers above and below the control gate. Kuhn, ¶257. For example, first memory string (MTr121-MTr421) includes first memory cell MTr121 at WL1 and second memory cell MTr221 at WL2 with “charge storage layer 391b” in

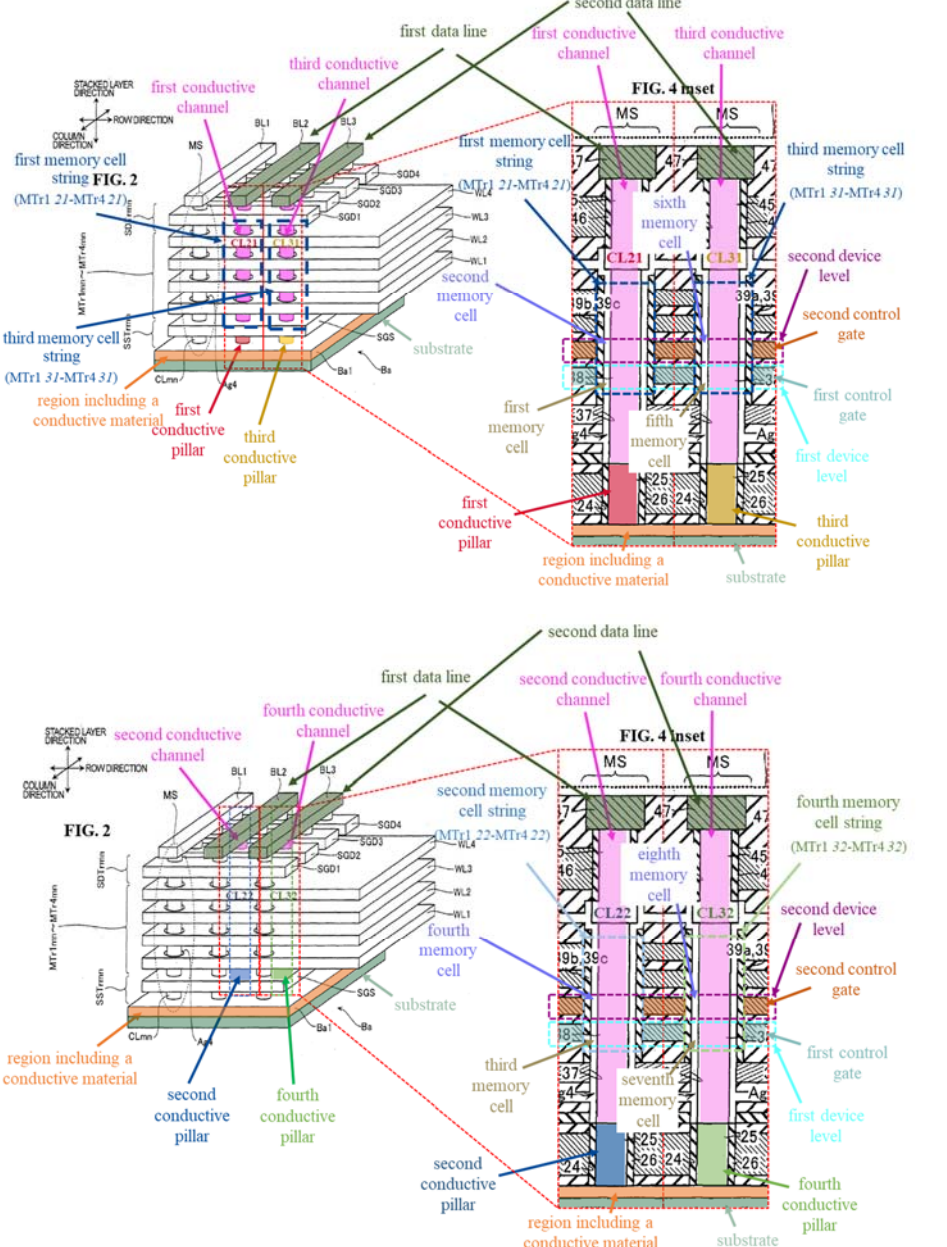
'903	Fukuzumi
	respective memory holes 37 of “end portion of the word line[s]” WL1-WL2. Kuhn, ¶256. - Figures 2&4  - Figure 6  FIG. 6 - See also [0079]-[0080], [0087], [0090], [0101], [0103]-[0104], [0114].

'903	Fukuzumi
[17.m] the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate (e.g., “memory cells” MTr122-MTr422 including “memory cells” MTr122 and MTr222 having “charge storage layer 391 b” formed in “memory hole 37” of “end portion” of “word line” WL1 and WL2, or “word line conduction layer” 36a and 36b, respectively).	Fukuzumi discloses that the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate (e.g., “memory cells” MTr122-MTr422 including “memory cells” MTr122 and MTr222 having “charge storage layer 391 b” formed in “memory hole 37” of “end portion” of “word line” WL1 and WL2, or “word line conduction layer” 36a and 36b, respectively). <u>E.g., Fukuzumi:</u> See [1.b]-[1.d], [17.d]-[17.g], [17.j]-[17.l]. The same analysis provided for [17.l] applies for this limitation, except third and fourth memory cells are MTr122 and MTr222. Kuhn, ¶¶258-261. - Figures 2&4 The diagram illustrates a multi-layered semiconductor structure. Key features include stacked layers (MS, SOD1-SOD4), word lines (WL1-WL3), and various pillars and gates. An inset provides a detailed view of the top layers, highlighting different levels, control gates, and memory cell strings. Labels such as BL1, BL2, BL3, CLns, Ba1, Ba, and Aa point to specific structural elements. Color-coded regions identify functional areas like conductive materials, pillars, cavities, and memory cells. - Figure 6

'903	Fukuzumi
	 FIG. 6
[17.n] the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second	Fukuzumi discloses that the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate (e.g., “memory cells” MTr131-MTr431 including “memory cells” MTr131 and MTr231 having “charge storage layer 391 b” formed in “memory hole 37” of “end portion” of “word line” WL1 and WL2, or “word line conduction layer” 36a and 36b, respectively). <u>E.g., Fukuzumi:</u> See [1.b]-[1.e], [17.d]-[17.g], [17.j]-[17.l]. The same analysis provided for [17.l] applies for this limitation, except fifth and sixth memory cells are MTr131 and MTr232. Kuhn, ¶¶262-265. • Figures 2&4 (see [17.l]) • Figure 6 (see [17.l])

'903	Fukuzumi
control gate; and	
[17.o] the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.	Fukuzumi discloses that the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and a eighth memory cell having a memory element formed in a fourth cavity of the second control gate (e.g., “memory cells” MTr132-MTr432 including “memory cells” MTr132 and MTr232 having “charge storage layer 391 b” formed in “memory hole 37” of “end portion” of “word line” WL1 and WL2, or “word line conduction layer” 36a and 36b, respectively). <u>E.g., Fukuzumi:</u> See [1.b]-[1.d], [17.d]-[17.g], [17.j]-[17.l]. The same analysis provided for [17.l] applies for this limitation, except seventh and eighth memory cells are MTr132 and MTr232. Kuhn, ¶¶266-269. • Figures 2&4 (see [17.m]) • Figure 6 (see [17.m])
[19] The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells	See [9], [17]. Kuhn, ¶270.

'903	Fukuzumi
comprises a silicon nitride.	
[20.a] The apparatus of claim 17, further comprising: a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells; [20.b] a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells; [20.c] a third conductive channel	See [17]. Fukuzumi discloses a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells, a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells, a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells, and a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells (e.g., “memory 38” extending between “memory cells” MTr1mn and MTr2mn, and coupled to “source-side columnar semiconductor layer 25” of columnar semiconductor CL21, CL22, CL31, and CL32—see [17.a]-[17.b], [17.l]-[17.o]). <u>E.g., Fukuzumi:</u> See [1.e], [17.a]-[17.b], [17.d]-[17.g], [17.l]-[17.o]. As discussed ([1.e], [17.d]-[17.g]), first, second, third, and fourth memory strings (MTr1mn-MTr4mn) are formed over and coupled to first, second, third, and fourth source-side columnar semiconductor 25 of columnar semiconductors CL21, CL22, CL31, and CL32, respectively, such that memory 38 (conductive channels) of the memory strings extend between memory cells of the memory strings and are coupled to respective source-side columnar semiconductors 25. Kuhn, ¶¶271-274. • Figures 2&4

'903	Fukuzumi
coupled to the third conductive pillar and extending between the fifth and sixth memory cells; and [20.d] a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells.	 FIG. 2 and FIG. 4 inset illustrate a memory array structure. FIG. 2 is a 3D perspective view showing a stack of memory cells (first, second, third, and fourth memory cell strings) and conductive pillars (first, second, third, and fourth conductive pillars) and channels (first, second, third, and fourth conductive channels). The structure includes a substrate, control gates, and various conductive layers. FIG. 4 inset is a cross-sectional view showing the detailed structure of the memory cells, including the first, second, third, and fourth memory cell strings, and the first, second, third, and fourth conductive pillars and channels. The structure includes a substrate, control gates, and various conductive layers. See also [0081], [0085]-[0089], [0103]-[0104].

D. Ground 4: Fukuzumi in view of Ahn (Claims 5, 8, 18)

As explained above (§IX.A.2), **Ahn** discloses the limitations of claims 5, 8 and 18. Kuhn, ¶275.

Fukuzumi and **Ahn** are in the same field as the '903—which includes three-dimensional memory devices—and are reasonably pertinent to the problems addressed by '903, e.g., increasing integration or density of memory devices. **Ahn**, [0005]; **Fukuzumi**, [0004]; '903, 1:26-28. Kuhn, ¶¶276-277.

Claim 5. A POSITA would have been motivated to apply **Ahn's** teachings of a metal conductive layer in a lower select gate to **Fukuzumi's** source-side selection transistor. **Fukuzumi** does not teach a particular material for source-side conductive layer 22 of source-side selection transistor SStrmn (*i.e.*, conductive layer on first and second sides of “source-side columnar semiconductor layer 25”), leaving selection of that material to a POSITA. *See generally* **Fukuzumi**. **Ahn** discloses a source-side selection transistor formed of “a conductive material,” and provides doped polysilicon and tungsten as examples. **Ahn**, [0032]. It was well-known in the art that high conductivity and high temperature resistance (including to withstand the high temperatures involved in fabrication) are important criteria for selecting gate materials, and that tungsten has these desired properties. Ex.1023, 195, 247; Ex.1020, 1. Thus, a POSITA would have been motivated to apply **Ahn's** teaching of using tungsten to form a source-side transistor gate to **Fukuzumi's** source-side

conductive layer 22 to advantageously enhance the conductivity and heat resistance of Fukuzumi's source-side selection transistor SStrmn. Ex.1020, 1. Kuhn, ¶¶278-282.

A POSITA would have had a reasonable expectation of success in applying **Ahn's** teachings of a metal conductive layer to **Fukuzumi's** source-side selection transistor. Use of metals for the conductive layer of the lower select gate was well-known in the art.¹⁰ Kuhn, ¶283. And, other than the minimal modification of using a metal layer for **Fukuzumi's** source-side selection transistor, no modifications in **Fukuzumi's** manufacturing process would have been needed because none of those steps depends on the composition of source-side transistor layer 20. Kuhn, ¶¶283-284. Indeed, **Ahn** teaches polysilicon and metal are interchangeable for a source-side selection transistor gate. Ahn, [0031]. Kuhn ¶284.

Claims 8 and 18. A POSITA also would have been motivated to apply **Ahn's** teachings of a polysilicon charge trap layer to **Fukuzumi's** charge storage layer. Ahn, [0040]. Kuhn, ¶¶285-289. **Fukuzumi** discloses using silicon nitride as the charge storage layer of its memory device. Fukuzumi, [0104]. But, a POSITA would have recognized polysilicon was commonly used for memory elements while the use of silicon nitride had known reliability issues. Ex.1010, [0080]; Ex.1025,

¹⁰ Ex.1010, [0046], [0073]; Ex.1013, [0050]

1:46-56, 5:26-50; Ex.1017, 3. Kuhn, ¶287. Further, a POSITA would have understood a polysilicon layer floating gate for charge storage to have better long-term data retention than silicon nitride. *Compare* Ex.1015, *with* Ex.1016; Ex.1022. Kuhn, ¶287.

A POSITA would have had a reasonable expectation of success applying **Ahn's** teachings of a polysilicon layer to **Fukuzumi's** 3D memory cells. Kuhn, ¶288. Indeed, **Ahn** discloses its charge trap layer inside the ONO layer is “formed by depositing, for example, a silicon nitride film or a polysilicon film,” noting the interchangeability of the two materials. Ahn, [0040]. Kuhn, ¶288.

A POSITA would have thus found it routine, straightforward and advantageous to apply **Ahn's** teachings of using a polysilicon memory element and a metal source side selection transistor gate to **Fukuzumi's** teachings of a memory device, and would have known such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality. Kuhn, ¶289.

X. SECONDARY CONSIDERATIONS

There is no evidence in the '903's prosecution history or elsewhere supporting secondary considerations. *See generally* Ex.1002. Kuhn, ¶290. Indeed, as demonstrated herein, any purported solutions to problems or unexpected results in the '903 were well-known. Kuhn, ¶290. Petitioner reserves the right to address any evidence of secondary considerations PO may raise.

XI. CONCLUSION

There is a reasonable likelihood that Petitioner will prevail as to the Claims.

Inter partes review of the Claims is accordingly requested.

Respectfully submitted,

Dated: November 18, 2024

By: /James L. Davis, Jr./
Name: James L. Davis, Jr.
Registration No. 57,325
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to §42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,872,903 contains, as measured by the word-processing system used to prepare this paper, 13,985 words. This word count does not include the items excluded by §42.24 as not counting towards the word limit.

Dated: November 18, 2024

By: /James L. Davis, Jr./
Name: James L. Davis, Jr.
Registration No. 57,325
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on November 18, 2024, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,872,903 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on Patent Center:

**73115 - SCHWEGMAN LUNDBERG &
WOESSNER/MICRON**
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UNITED STATES

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