UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00245
U.S. Patent No. 11,482,532
Issue Date: October 25, 2022

Title: JOINT OPENING STRUCTURES OF THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,482,532 PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42

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X. GROUND 1: **INDEPENDENT CLAIMS 1, 11, AND 18, AND DEPENDENT CLAIMS 2, 3, 13, 15-17, AND 20, ARE OBVIOUS OVER COSTA** 31

A. Claim 1: 31

1. [1.PRE] "A method of forming a joint opening structure in a three-dimensional (3D) memory device, comprising:" 31

2. [1.A] "forming a first stacked layer on a substrate;" 32

3. [1.B] "forming a first through hole penetrating the first stacked layer to expose the substrate;" 33

4. [1.C] "forming a first channel structure at a bottom of the first through hole and in contact with the substrate;" 36

5. [1.D] "forming a second channel structure in the first through hole and in contact with the first channel structure;" 37

6. [1.E] "forming a third channel structure above the first through hole and in contact with the second channel structure, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;" 40

7. [1.F] "forming a second stacked layer over the third channel structure;" 63

8. [1.G] "forming a second through hole penetrating the second stacked layer to expose the third channel structure;" 65

9. [1.H] "forming a fourth channel structure in the second through hole and in contact with the third channel structure; and" 68

10. [1.I] "forming a fifth channel structure above the second through hole and in contact with the fourth channel structure." 71

B. Claim 2: 79

1. [2.PRE] "The method of claim 1, wherein:" [2.A] "the first stacked layer includes a first number of oxide/nitride layer pairs; and" [2.B] "the second stacked layer includes a second number of oxide/nitride layer pairs." 79

C. Claim 3: 80

1. [3.PRE] "The method of claim 2, wherein:" [3.A] "the first number and the second number are not less than 32." 80

D. Claim 11: 80

1. [11.PRE] "A joint opening structure of a three-dimensional (3D) memory device, comprising:"..... 80

2. [11.A] "a first through hole penetrating a first stacked layer along a vertical direction;"..... 80

3. [11.B] "a first channel structure disposed at the bottom of the first through hole;" 81

4. [11.C] "a second channel structure in contact with the first channel structure disposed in the first through hole;" 81

5. [11.D] "a third channel structure in contact with the second channel structure disposed over the first through hole, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;" 81

6. [11.E] "a second stacked layer disposed on the third channel structure;" 81

7. [11.F] "a second through hole penetrating the second stacked layer along the vertical direction;"..... 81

8. [11.G] "a fourth channel structure in contact with the third channel structure disposed in the second through hole;" 82

9. [11.H] "a fifth channel structure in contact with the fourth channel structure disposed over the second through hole."..... 82

E. Claim 13: 82

1. [13.PRE] "The joint opening structure of claim 11, further comprising:" [13.A] "a first filling structure covering the surface of the second channel structure; and" 82

2. [13.B] "a second filling structure covering the surface of the fourth channel structure;" 85

3. [13.C] "wherein the first through hole is non-interconnected with the second through hole." 87

F. Claim 15: 89

1. [15.PRE] "The joint opening structure of claim 11, wherein:" [15.A] "the first stacked layer includes a first number of conductor/dielectric layer pairs;" [15.B] "the second stacked layer includes a second number of conductor/dielectric layer pairs; and" 89

2. [15.C] "the first number and the second number are not less than 32." 89

G. Claim 16: 90

1. [16.PRE] "The joint opening structure of claim 11, wherein:" [16.A] "a thickness of the third channel structure is in a range between 30 nm and 70 nm." 90

H. Claim 17: 90

1. [17.PRE] "The joint opening structure of claim 11, wherein:" [17.A] "a size difference between the top aperture and a bottom aperture of the first through hole is equal to or less than 30 nm; and" 90

2. [17.B] "a size difference between a top aperture and a bottom aperture of the second through hole is equal to or less than 30 nm." 91

I. Claim 18: 91

1. [18.PRE] "A joint opening structure of a three-dimensional (3D) memory device, comprising:" 91

2. [18.A] "a first stacked layer disposed on a substrate;" .. 91

3. [18.B] "a second stacked layer disposed on the first stacked layer; and" 92

4. [18.C] "a plurality of channel structures penetrating the first stacked layer and the second stacked layer;" 92

5. [18.D] "wherein each of the plurality of channel structures includes:" [18.E] "a first through hole penetrating the first stacked layer," 92

6. [18.F] "a first channel structure disposed at the bottom of the first through hole and in contact with the substrate," 93

7. [18.G] "a second channel structure disposed in the first through hole and in contact with the first channel structure," 93

8. [18.H] "a third channel structure disposed over the first through hole and in contact with the second channel structure, wherein a size of the third channel structure along a lateral direction is larger than a top aperture of the first through hole;" 93

9. [18.I] "a second through hole penetrating the second stacked layer," 93

10. [18.J] "a fourth channel structure disposed in the second through hole and in contact with the third channel structure, and" 93

11. [18.K] "a fifth channel structure disposed over the second through hole and in contact with the fourth channel structure." 94

J. Claim 20: 94

1. [20.PRE] "The joint opening structure of claim 18, wherein:" [20.A] "a thickness of the third channel structure is in a range between 30 nm and 70 nm." 94

XI. GROUND 2: INDEPENDENT CLAIMS 1, 11, AND 18, AND DEPENDENT CLAIMS 2, 3, 13, 15-17, AND 20, ARE OBVIOUS OVER COSTA IN VIEW OF OH 94

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II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Micron Technology, Inc., and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

On July 12, 2024, YMTC asserted the ’532 Patent and U.S. Patent Nos. 10,672,711, 10,879,164, 10,879,254, 10,886,291, 11,101,276, 11,145,666, 11,450,604, 11,568,941, 11,581,322, and 12,010,838 against Micron. On August 21, 2024, the litigation was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”). U.S. Patent Nos. 10,658,378, 10,861,872, 10,868,031, 10,937,806, 10,950,623, 11,468,957, 11,501,822, and 11,600,342 were asserted by Patent Owner in the first filed case, leading to a total of 19 patents-at-issue in the now consolidated Co-Pending Litigation.

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Patent	PTAB Proceeding	Wave
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	

XII. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See* generally Ex. 1002. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XIII. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

December 31, 2024

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