

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00117
U.S. Patent No. 10,672,711
Issue Date: June 2, 2020

Title: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL
MEMORY DEVICES AND FABRICATION METHODS THEREOF

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,672,711
PURSUANT TO 35 U.S.C. §§311-319 and 37 C.F.R. §42**

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LISTING OF EXHIBITS

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 10,672,711 to Zhu et al. (“the ’711 patent”)
1002	File History of U.S. Patent No. 10,672,711 (“the ’711 FH”)
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	<i>Curriculum Vitae</i> of Dr. Sanjay Banerjee
1005	U.S. Patent Publication No. 2012/0070944A1 to Kim et al. (“Kim”)
1006	Korean Patent No. 10-2015-0051841 to Park et al. (“Park”) including certified translation
1007	U.S. Patent Publication No. 2019/0067306A1 to Fang et al. (“Fang”)
1008	U.S. Patent Publication No. 2017/0294384A1 to Chen (“Chen”)
1009	Aritome, “NAND Flash Memory Technologies” (2016)
1010	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1011	Micheloni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1012	U.S. Patent Publication No. 2017/0117222A1 to Kim et al.
1013	Chang and Sze, “ULSI Technology” (1996)
1014	Orlowski et al., <i>Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy</i> , ECS Transactions Vo. 33, No. 6 (2010), 777-89
1015	U.S. Patent No. 9,728,547 to Ohsaki et al.
1016	U.S. Patent Publication No. 2017/0148677A1 to Shin

EXHIBIT NO.	DESCRIPTION
1017	U.S. Patent Publication No. 2013/0313627A1 to Lee et al.
1018	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1019	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1020	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.'s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1021	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 1:	
[1.PRE]	A semiconductor structure, comprising:
[1.A]	a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
[1.B]	a barrier layer disposed over a portion of the gate stack of the each step;
[1.C]	an etch-stop layer disposed on the barrier layer;
[1.D]	an insulating layer disposed on the etch-stop layer; and
[1.E]	a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.
Claim 2:	
[2]	The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the barrier layer and the high-k dielectric layer.
Claim 3:	
[3]	The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the etch-stop layer.
Claim 4:	
[4]	The semiconductor structure of claim 1, wherein the barrier layer comprises silicon oxide.

Ref. #	Listing of Challenged Claims
Claim 5:	
[5]	The semiconductor structure of claim 1, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.
Claim 6:	
[6]	The semiconductor structure of claim 1, wherein the each conductive structure directly contacts a corresponding one of the conductive layer of the each step.
Claim 7:	
[7]	The semiconductor structure of claim 1, wherein top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.
Claim 8:	
[8]	The semiconductor structure of claim 1, wherein the plurality of conductive structures comprise one or more of tungsten, cobalt, nickel, copper, and aluminum.
Claim 9:	
[9]	The semiconductor structure of claim 1, wherein the barrier layer is formed on side and top surfaces of the plurality of steps.
Claim 10:	
[10]	The semiconductor structure of claim 1, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.
Claim 11:	
[11]	The semiconductor structure of claim 1, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.

Ref. #	Listing of Challenged Claims
Claim 12:	
[12]	The semiconductor structure of claim 1, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.
Claim 13:	
[13.PRE]	A semiconductor structure, comprising:
[13.A]	a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
[13.B.]	an etch-stop layer disposed on a portion of the gate stack of the each step;
[13.C]	an insulating layer disposed on the etch-stop layer; and
[13.D]	a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer and the high-k dielectric layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.
Claim 14:	
[14]	The semiconductor structure of claim 13, wherein the etch-stop layer is formed on a side surface and a top surface of each step.
Claim 15:	
[15]	The semiconductor structure of claim 14, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.

Ref. #	Listing of Challenged Claims
Claim 16:	
[16]	The semiconductor structure of claim 13, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.
Claim 17:	
[17]	The semiconductor structure of claim 13, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.
Claim 18:	
[18]	The semiconductor structure of claim 13, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.
Claim 19:	
[19]	The semiconductor structure of claim 13, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.

I. INTRODUCTION

Petitioner Micron Technology, Inc. (“Petitioner”) respectfully requests *inter partes* review of claims 1-19 (the “Challenged Claims”) of U.S. Patent No. 10,672,711 (the “’711 patent”) assigned to Yangtze Memory Technologies Co., Ltd. (“YMTC” or “PO”). There is more than a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim.

The ’711 patent relates to a conventional “staircase structure on an alternating conductor/dielectric stack” (i.e., alternating stack of gate and dielectric layers). Ex 1001, 5:31-39. Such a staircase structure provides landing areas, i.e., steps, for the contacts (which the ’711 patent refers to as “conductive structures”) that physically connect to the gate layers. The ’711 patent alleges that etching the contact holes to the necessary different depths requires employing a fabrication technique that was either (1) costly or (2) prone to inadvertently punching through the target landing area. *Id.*, 5:47-6:3. The ’711 patent purports to solve this alleged issue by forming a barrier and an etch stop layer over the staircase landing areas:

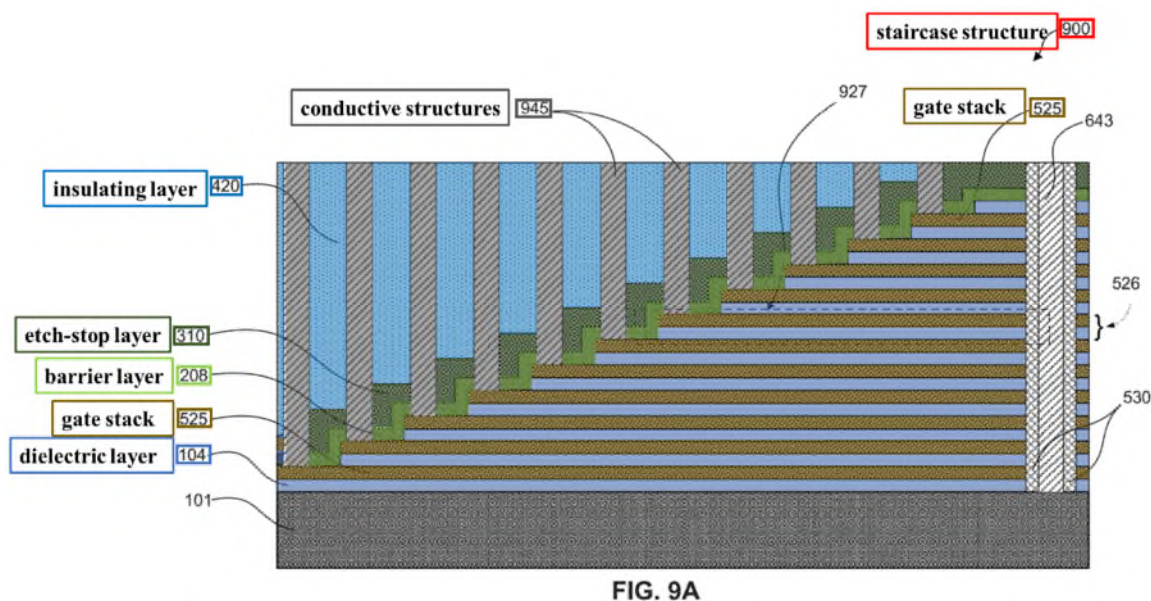
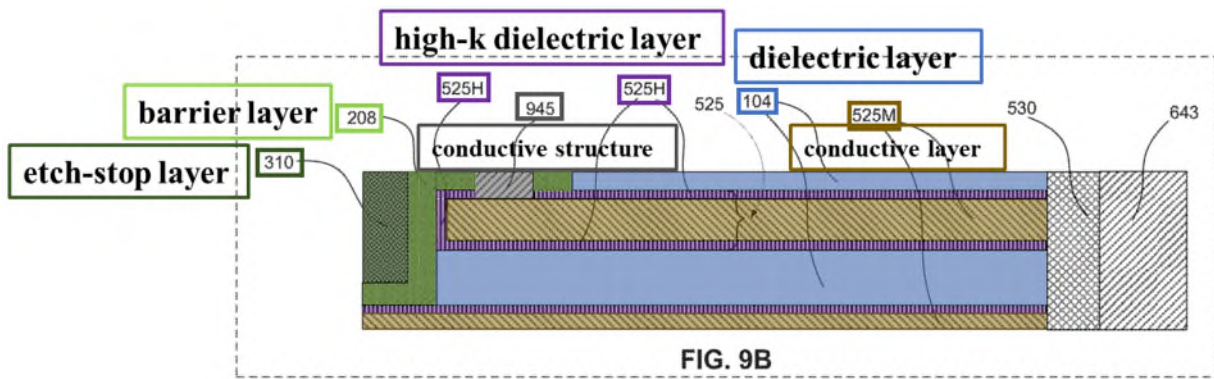


FIG. 9A

Id., Fig. 9A.¹

This alleged improvement, however, was no improvement at all, and the Examiner rejected the claims on the grounds that they were anticipated by two different prior-art references. In response, the Applicant amended the independent claims to require a high-k dielectric layer around the conductive (gate) layers of the stack. Ex. 1002, 152-57, 201-08. The Examiner allowed the amended claims. *Id.*, 239. The high-k dielectric layer is shown below in purple:

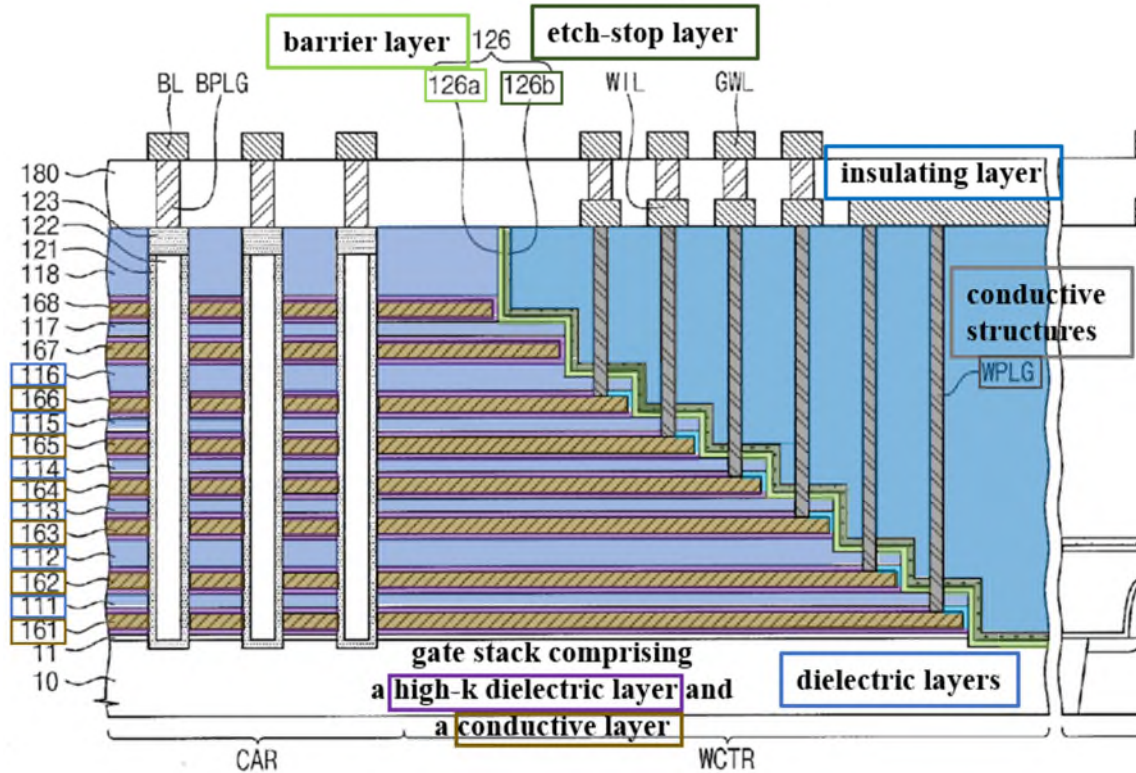
¹ All color annotations in this Petition are added except where noted otherwise.



Ex. 1001, Fig. 9B.

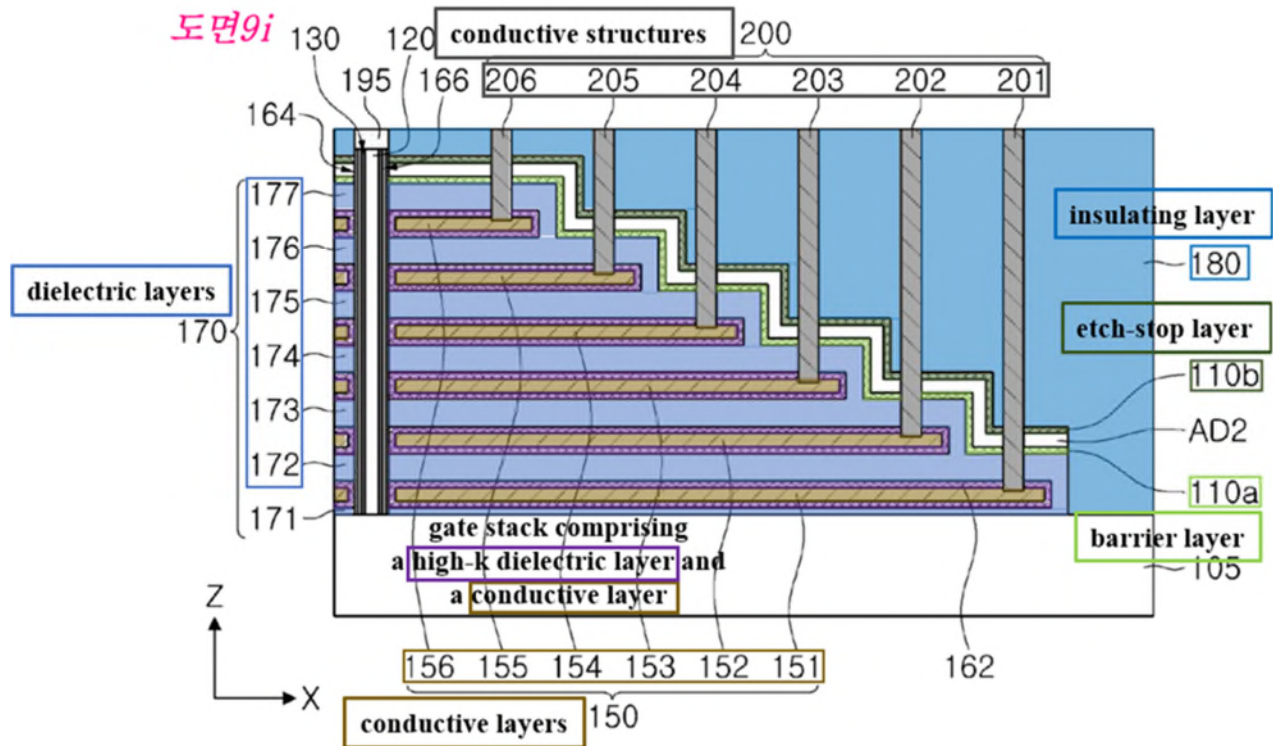
As this Petition demonstrates, the Examiner was incorrect in allowing the claims: forming a high-k dielectric layer around the gate layer was widely known in the art. The Petition relies on two primary references: Kim and Park. Neither reference was before the Examiner during prosecution. Notably, as shown below, both Kim and Park separately disclose a staircase structure with barrier and etch stop layers, as well as a high-k dielectric surrounding the gate layers.

Fig. 22A



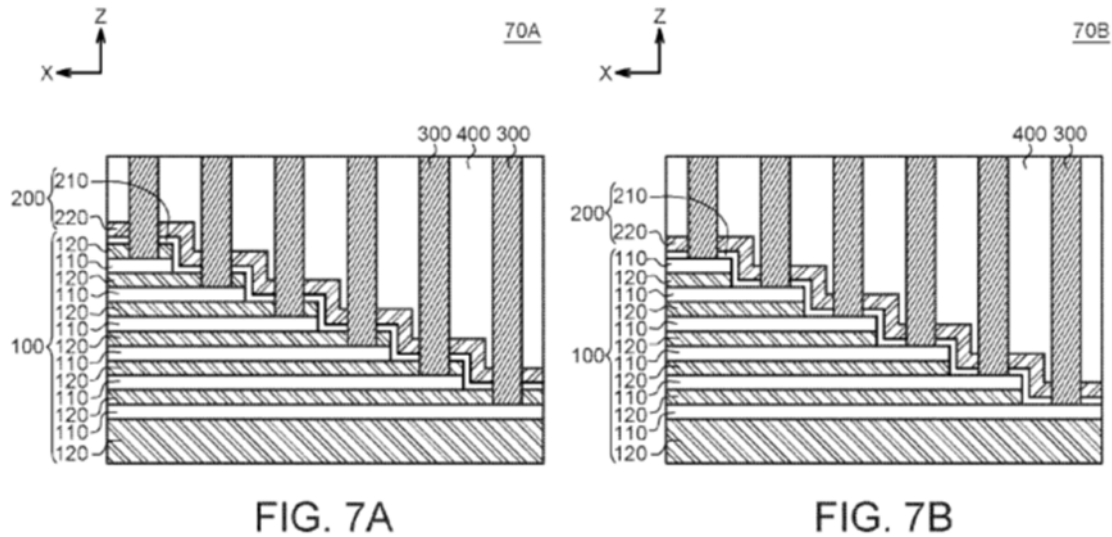
Ex. 1005 (Kim), Fig. 22A.²

² All Kim cross-sectional images shown herein omit a portion (the peripheral-circuit region) that is irrelevant to this Petition.



Ex. 1006 (Park), Fig. 9i.

Although the '711 patent illustrates a dielectric layer under the corresponding conductive layer at each step, whereas these figures from Kim and Park show the dielectric layer above the corresponding conductive layer at each step, that distinction is immaterial because Kim and Park also disclose having the conductive layer over the dielectric layer. Indeed, a POSITA would have known that both orders were conventional, as demonstrated by Chen:



Ex. 1008 (“Chen”), Fig. 7A (dielectric on top), Fig. 7B (conductor on top).

Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable under §103.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

According to USPTO assignment records, the '711 patent is currently assigned to YMTC. On July 12, 2024, YMTC asserted the '711 patent and U.S. Patent Nos. 10,879,164, 10,879,254, 10,886,291, 11,101,276, 11,145,666, 11,450,604, 11,482,532, 11,568,941, 11,581,322, and 12,010,838 against Micron (the “YMTC2 case”). On August 21, 2024, the litigation was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and*

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Micron Consumer Products Group, LLC, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”).

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Patent	PTAB Proceeding	Wave
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	
10,879,164	IPR2025-00118	Wave 3 Petitions
10,879,254	IPR2025-00034	
10,879,254	IPR2025-00119	
10,886,291	IPR2025-TBD	

Petition for *Inter Partes* Review of U.S. Patent No. 10,672,711

Patent	PTAB Proceeding	Wave
11,101,276	IPR2025-TBD	
11,145,666	IPR2025-TBD	
11,450,604	IPR2025-00035	
11,482,532	IPR2025-TBD	
11,568,941	IPR2025-TBD	
11,581,322	IPR2025-TBD	
12,010,838	IPR2025-TBD	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a).

C. Counsel, Service, and Fee Information

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PTABDocketJ3B3@orrick.com, PTABDocketJ1H1@orrick.com, and MICRON-

YMTC_OHS@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Petitioner certifies that the '711 patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Petitioner was served with a complaint alleging infringement of the '711 patent on July 12, 2024. This Petition was filed within one year of this date.

B. Identification of Challenge and Statement of Precise Relief Requested

Petitioner requests *inter partes* review of claims 1-19. This Petition discusses claim construction, explains why the claims are unpatentable, provides details regarding where the various claim limitations are found in the prior art, and is supported by the accompanying Declaration of Dr. Sanjay Banerjee (Ex. 1003, "Banerjee"), a leading expert in the 3D NAND field.

The '711 patent claims priority to a short CN application filed on August 31, 2017. Ex. 1001, Cover. For purpose of this Petition only, Petitioner assumes the '711 patent is entitled to that 2017 priority date.

Petitioner relies on the following primary references:

Petition for *Inter Partes* Review of U.S. Patent No. 10,672,711

(1) U.S. Patent Publication No. 2012/0070944A1 (Ex. 1005 or “Kim”). Kim was filed on September 13, 2011 and was published on March 22, 2012. Kim, Cover. Kim is prior art to the ’711 patent under 35 U.S.C. §§ 102(a)(1) and 102(a)(2).

(2) Korean Patent Publication No. 10-2015-0051841 (Ex. 1006 or “Park”). Park was filed on November 5, 2013 and was published on May 13, 2015. Park, Cover. Park is prior art to the ’711 patent under 35 U.S.C. §§ 102(a)(1) and 102(a)(2) (AIA).

Petitioner also relies on a secondary reference, U.S. Patent Publication No. 2019/0067306A1 (Ex. 1007 or “Fang”). Fang was filed on August 24, 2017 and was published on February 28, 2019. Fang, Cover. Fang is prior art to the ’711 patent under 35 U.S.C. § 102(a)(2).

Petitioner challenges the claims on the following grounds:

Ground 1: Claims 1-9, 11-16, and 18-19 are obvious over Kim in view of a POSITA’s knowledge;

Ground 2: Claims 10 and 17 are obvious over Kim in view of Fang;

Ground 3: Claims 1-6, 8-9, 11-16, and 18-19 are obvious over Park in view of a POSITA’s knowledge; and

Ground 4: Claims 7, 10, 15, and 17 are obvious over Park in view of Fang. Banerjee ¶¶ 63-64.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There are No Grounds for a § 314 Discretionary Denial in this Case

There is a pending district court action involving the '711 patent. The PTAB has explained that it “will not ... discretionarily deny institution in view of parallel district court litigation where a petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: the claims of the '711 patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”). In particular: the district court may stay the case, any potential trial will occur years from now, little district court work has occurred, Petitioner diligently prepared this Petition, and the Petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay of the district court proceeding if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome

would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Grp. – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”); *Fintiv* at 6-9, 12 (similar).

2. Proximity of the Court’s Trial Date

On September 18, 2024, the district court entered a scheduling order which set a trial date of June 15, 2026. *See* Ex. 1018. As a result, if IPR proceedings are instituted, they should be completed before the scheduled trial date. *See also* Ex. 1019 (statistics indicating that it takes on average 48.9 months to reach trial in the district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

Regarding the Co-Pending Litigation, to date, the parties and the district court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. *See* §II.B. Virtually no progress has been made on the Wave 3 patents (which includes the ’711 patent). The parties are approximately two weeks away from completing the exchange of contentions for the Wave 3 patents (from the YMTC2 case) and have not taken any depositions in the entire Co-Pending Litigation. Fact discovery is in its infancy. No claim-construction positions have been exchanged for the Wave 3 patents, no claim-construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment

motions have been filed. This weighs in favor of institution. *See Sand Revolution* at 10-11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv*, 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner and subsequently asserted 149 claims across those eleven patents. Ex. 1020. Petitioner proceeded with diligence, starting the filing of petitions covering each patent approximately three months after being served with the YMTC2 complaint. Ex. 1021. This Petition is being filed 4 months after YMTC first asserted it against Micron. This also weighs strongly in favor of institution.

4. Issue Overlap

Should the Board institute, Micron stipulates that it will not advance, in District Court, any ground asserted in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution*, 11-12.

5. Party Overlap

Both Petitioner and PO are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It

is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

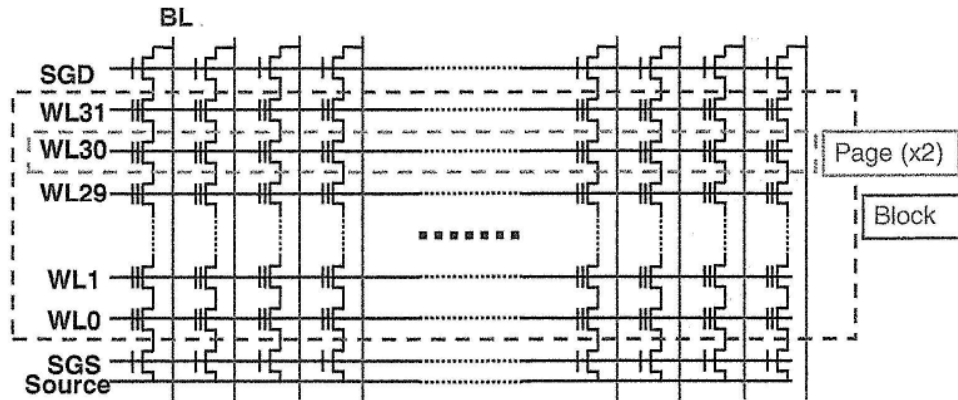
B. Denial Under §325(d) Would Be Inappropriate

The Examiner did not consider Kim, Park, or Fang, and thus denial under §325(d) would be inappropriate. Ex. 1001, Cover. Moreover, Kim and Park both disclose the alleged point of novelty in the specification (barrier and etch stop layers on the staircase structure) and the reason for allowance (a high-k dielectric around the gate layers). See §§VI, IX.A-IX.B.

V. TECHNOLOGY BACKGROUND

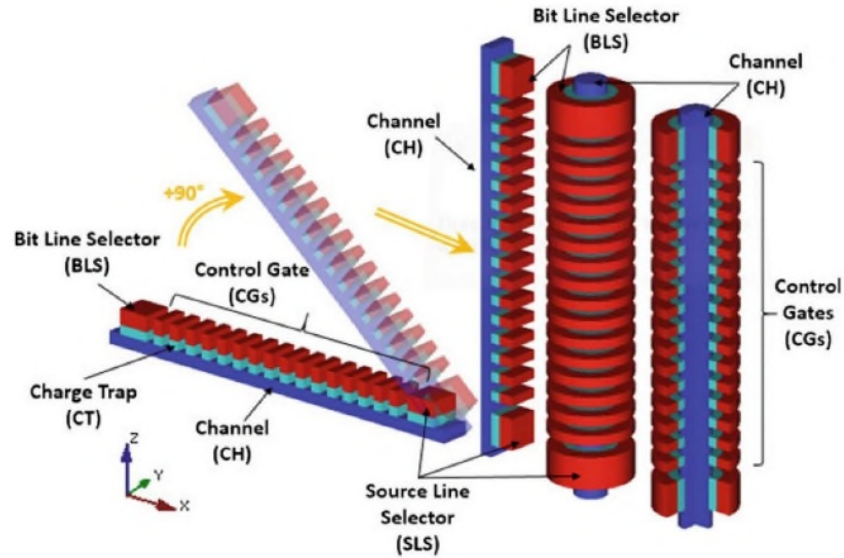
The '711 patent and the prior art discussed in this Petition relate to three-dimensional (3D) memory devices, *e.g.*, 3D NAND memory devices. Banerjee, ¶ 46.

At the core of NAND memory devices is a “memory cell,” which stores information as electrical charge. NAND cells are arranged in “strings” having multiple cells “connected in series.” Ex. 1009, 38. Early devices were formed as two-dimensional cell arrays on a substrate. *Id.*, 58; Banerjee ¶ 47.

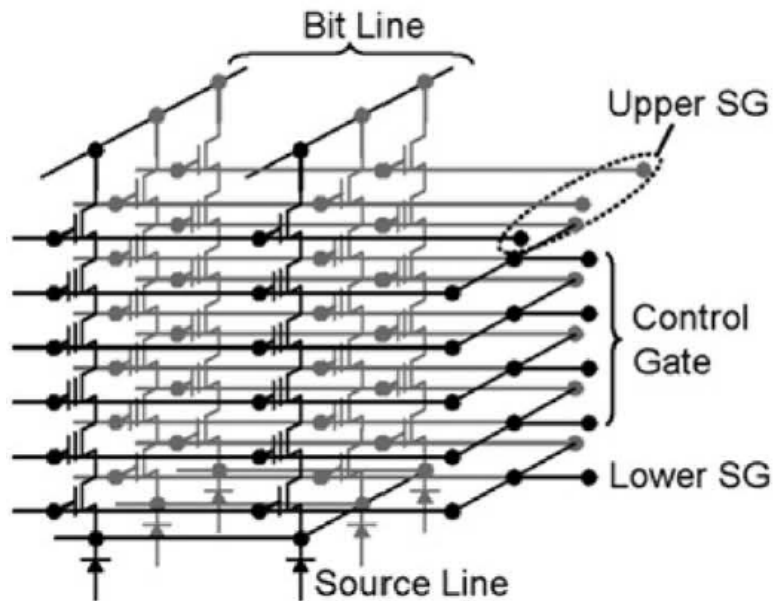


Ex. 1009, 40.

“[T]o further scale down the memory cell size,” “three-dimensional (3D) NAND flash cells” were developed. Ex. 1009, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1010, 3.



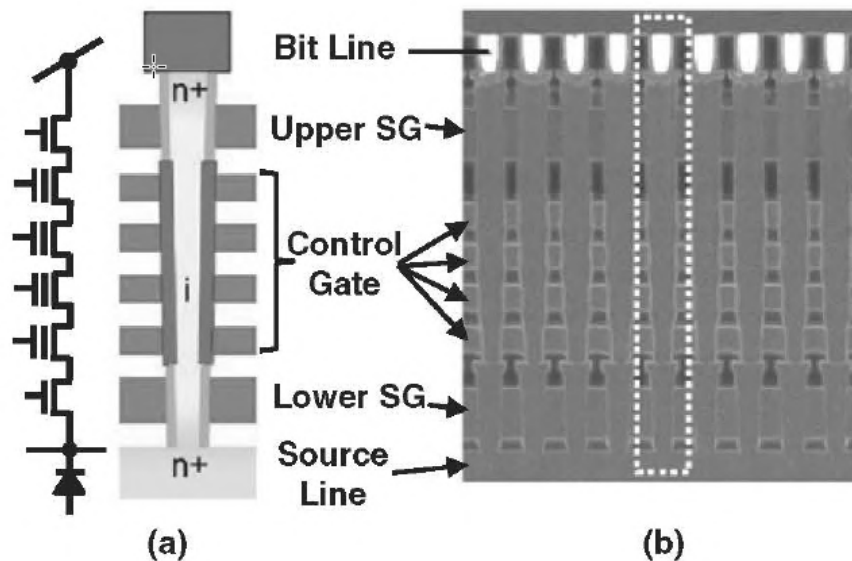
Ex. 1011, 122 (colors in the original). Multiple vertical channels are repeated in a three-dimensional array:



Ex. 1009, 296. A voltage applied on the control gate (also known as a word line) of each cell and the information stored in the cell (*e.g.*, binary 0 or 1) determine whether the cell turns on. Electrical current only flows through a string when all cells in the

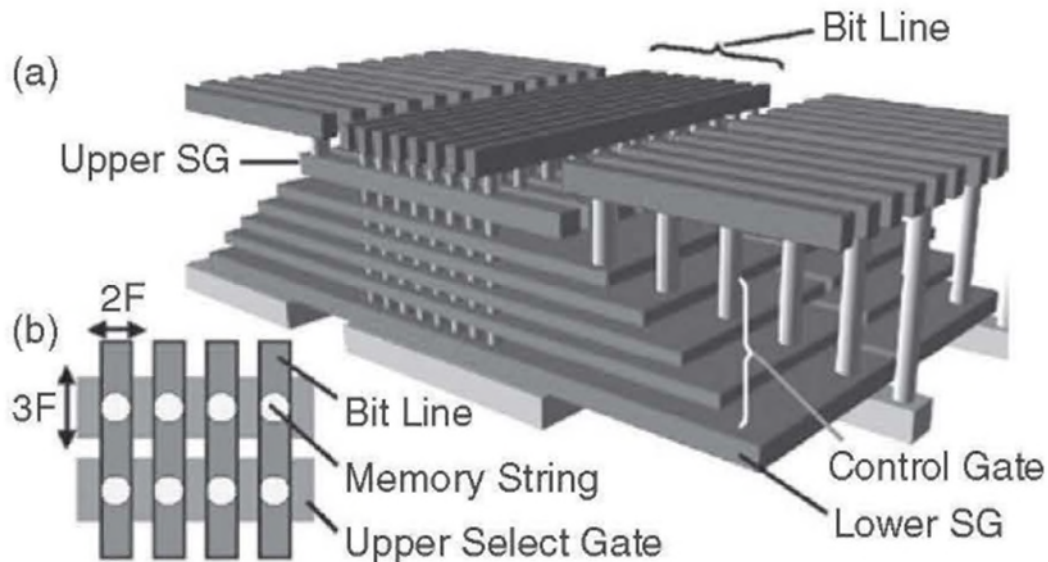
string are turned on. Thus, by applying a control-gate voltage sufficient to turn on all but one cell in a string and applying a suitable control-gate voltage to that one cell, the information stored in that cell may be determined via current flow, or the lack thereof, through the string. *Id.* This process is repeated by selecting a different cell in the next cycle, eventually retrieving the requested amount of information. Banerjee ¶ 48.

A particular vertical-memory-cell “string is selected by a bit line and an upper select gate (upper SG).” Ex. 1009, 295-296. A memory cell “is located in the intersection of a control gate plate” and the channel of the string. *Id.* The lowest layer is a “select gate (lower SG)” allowing the strings to connect to a lower “common source.” *Id.*, 295, 297. An example 3D vertical-memory-cell string is shown below:



Id., 296; Banerjee, ¶ 49.

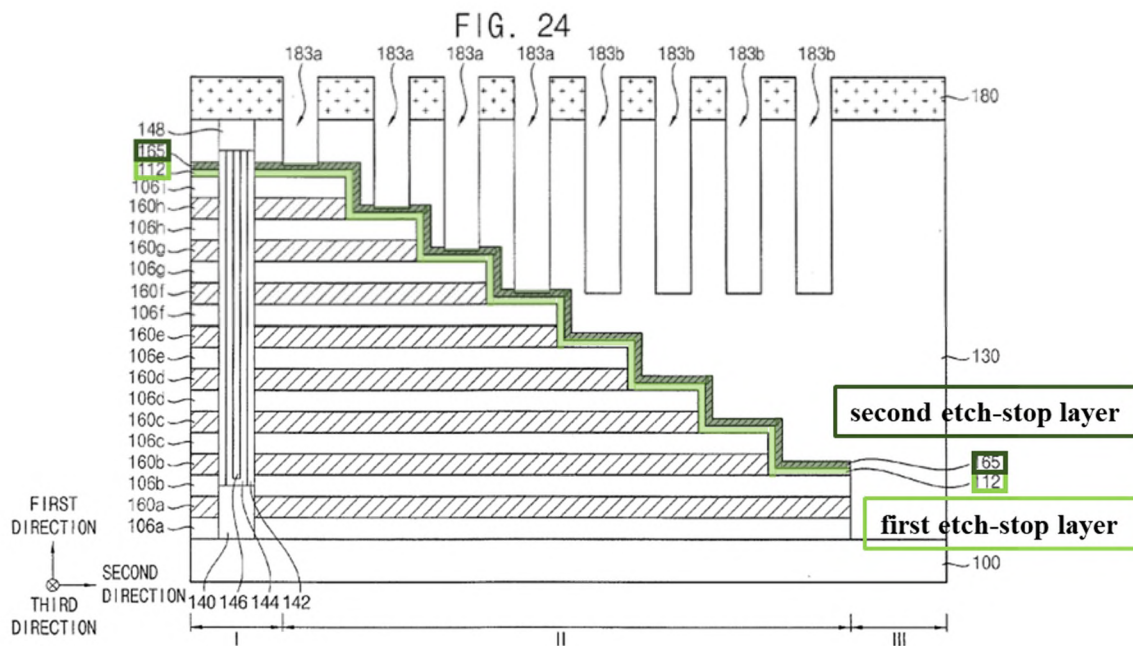
3D NAND includes “multi-stacked layers of [control] gate (plate)” material alternated with “dielectric” (*i.e.*, insulator) in a “[s]tack.” Ex. 1009, 294. A “through-hole[.]” channel (also known as a channel structure) “filled by memory film ... and channel poly-Si” passes through the layers to form the memory-cell string. *Id.*, 295. “Each” layer of “electrode plate acts as a control gate.” *Id.* “[T]he control gates ... are connected ... [in a] stair-like gate structure.” *Id.*, 295-97.

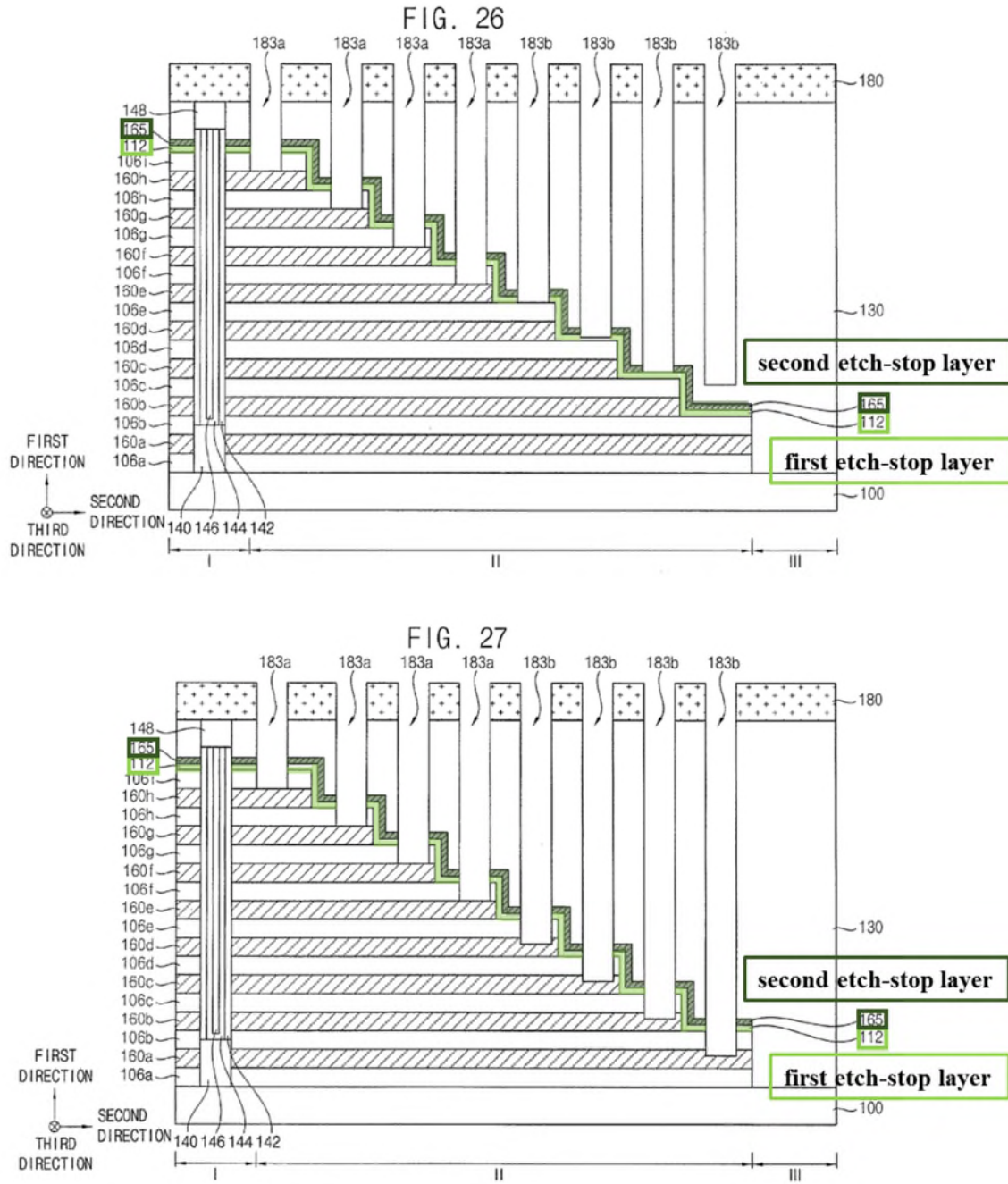


Id., 296 (Fig. 7.6). The staircase structure provides landing areas on the control gates for contacts with vertical conductive structures to couple the control gates to control voltages. *Id.*, 298; Banerjee ¶ 50.

As shown in the figure above, the vertical conductive structures contacting the different control-gate plates have various lengths. The '711 patent and the prior art address the challenge of fabricating these structures in a reliable and cost-effective manner. Banerjee ¶ 51.

Specifically, the vertical conductive structures are formed by etching holes through an insulating layer above the staircase structure and depositing a conductive material within. Because the conductive structures have different lengths and thus the holes need to be etched to different depths, techniques were developed to etch holes to their respective lengths. Ex. 1001, 5:51-53. One such technique is to place one or more etch-stop layers above the staircase structure. The etch-stop layers have a lower etching rate than the insulating layer for the etchant used to penetrate the insulating layer. Thus, upon reaching the etch-stop layers, etching slows down, protecting the underlying layers and preventing over-etching shallower holes while etching deeper holes. Park, [0045]-[0046]. This is illustrated by the following sequence of figures:





Ex. 1012, Figs. 24, 26-27; Banerjee ¶¶ 52-53.

More generally, a layer (“layer 2”) functions as an etch-stop layer when its etching rate is lower than that of the layer immediately above (“layer 1”).³ This is known as selective etching, based on the relative etch selectivity of materials in the layers. Ex. 1013, 220, 390, 593. Etch selectivity depends on the etchant: layer 1 may have a higher etching rate than layer 2 when one etchant is used, but a lower etching rate when a different etchant is used. These conventional processes were known as “selective etching” and “reverse selective etching.” Ex. 1014, 4, 6 (internal quotation marks omitted). Using different etchants allows greater flexibility in the choices of materials to use as an etch stop. Banerjee ¶¶ 54-55.

VI. THE ’711 PATENT AND ITS PROSECUTION HISTORY

The ’711 patent describes 3D memory structures and specifically relates to forming “word line contact structures” on a staircase structure. Ex. 1001, Abstract. As shown below, the word-line contact structure is the landing area in which a vertical conductive structure 945 contacts a particular step. The ’711 patent discloses a conventional staircase structure 900 with alternating gate stacks 525 and dielectric layers 104:

³ This implies that layers 1 and 2 cannot be the same material if layer 2 is to function as an etch-stop layer because the same material will have the same etching rate.

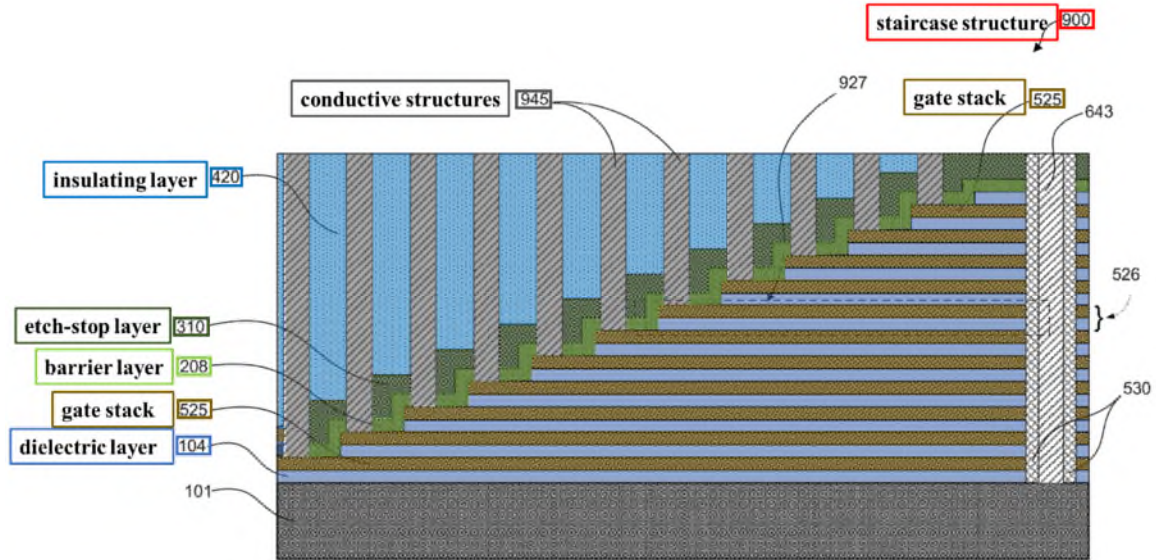


FIG. 9A

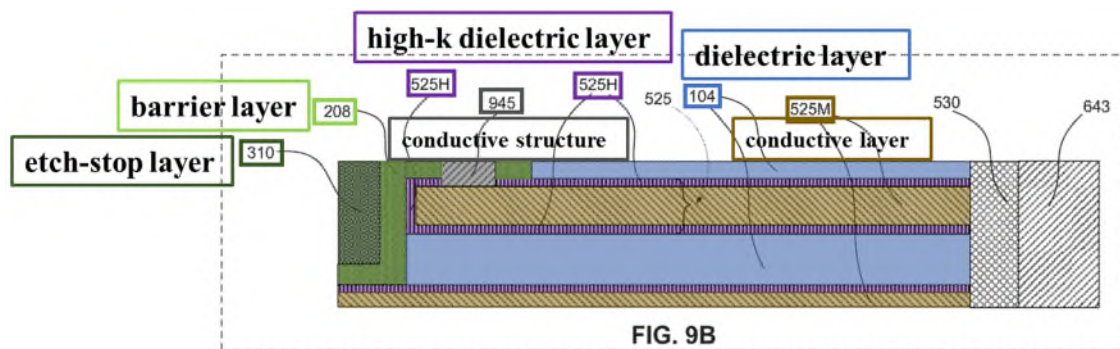
Id., Fig. 9A; 8:54-55. An optional barrier layer 208 and an etch-stop layer 310 cover the side surface and a portion of the top surface of each step. *Id.*, 5:54-65, 7:30-39, 7:56-58, 7:66-8:3. An insulating layer 420 is disposed on the etch-stop layer 310. Conductive structures 945 (*i.e.*, staircase contacts) penetrate the insulating layer 420, the etch-stop layer 310, and the barrier layer 208, and contact the gate stacks 525. *Id.*, 10:56-63, 11:14-19; Banerjee ¶ 56.

In this context, a barrier layer is simply an etch-stop layer by a different name. Banerjee ¶ 57. Consistent with the well-known principle explained above (§V), the '711 patent states that relative etch selectivity is what enables a layer to “function as an etch-stop layer,” *i.e.*, to slow down etching to protect the underlying layers. Ex. 1001, 6:62-67. The only statement in the '711 patent regarding the function of the barrier layer is that it serves as an etch-stop: “protecting the underlying structure during subsequent *etching* processes.” *Id.*, 7:36-39 (emphasis added). The patent

further discloses that “the second insulating layer 208 can be used as a barrier layer.” *Id.*, 7:35-39. Through the phrase “can be,” the patent implies that the second insulating layer 208 is not necessarily a barrier layer. Assuming the descriptions of insulating layer 208 nonetheless apply to the barrier layer, what the patent discloses confirms the understanding that, for the ’711 patent, a barrier layer is just another etch-stop layer. For example, the second insulating layer 208 and the etch-stop layer 310 are formed sequentially to the same step shape. *Id.*, 7:30-34, 7:56-58, 8:3-6. Their thickness characteristics are the same. *Id.*, 7:39-44, 8:6-10. Further, the barrier layer is optional, and, in its absence, the etch-stop layer would take its place in the structure. *Compare id.*, 7:67-8:6 with 7:30-34. Tellingly, when present, the barrier layer simply does what an etch-stop layer would do in its absence with respect to protecting the structure during etching. *Id.*, 8:56-64. Both layers comprise an insulating material. *Id.*, 7:51-52 (“the second insulating layer 208 can be made of similar material as the first insulating layer 104.”), 7:64-66 (“The etch-stop layer 310 can be made of any suitable insulating material that is different from the second insulating layer 208.”); §V (explaining that two adjacent layers must have different materials for the upper layer to function as an etch-stop layer). Both have an etching rate needed for etch stopping, *i.e.*, an etching rate lower than that of the layer immediately above. Ex. 1001, 9:60-62, 10:45-47; §V. Thus, both serve the same purpose, *i.e.*, to slow down the etching process to protect the underlying layers from

over-etching. Ex. 1001, 5:61-63 (“The etch-stop film protects underlying layers during etching processes that form contact VIAs.”), 7:36-39 (“the second insulating layer 208 can be used as a barrier layer for protecting the underlying structure during subsequent etching processes.”), 10:3-14; Banerjee ¶ 57.

In certain embodiments, each gate stack 525 comprises a conductive layer 525M at the core surrounded on three sides by a high-k dielectric layer 525H:



Ex. 1001, Fig. 9B, 8:65-9:4. The conductive structure 945 penetrates the high-k dielectric layer 525H in addition to (as shown in Figure 9A) the insulating layer 420, the etch-stop layer 310, and the barrier layer 208 and contacts the conductive layer 525M, thereby forming a contact to the control gate. *Id.*, 10:56-63, 11:14-22; Banerjee ¶ 58.

The '711 patent asserts that by using an etch-stop layer, the staircase contacts 945 may be formed simultaneously with a single lithography mask without reducing fabrication yields due to over-etching the shallower contact holes. Ex. 1001, 5:40-65. In other words, the '711 patent alleges that inadvertent punch-through of shallower holes, *i.e.*, inadvertently etching too far and into underlying layers, will

not occur. The '711 patent alleges that its etch-stop layer provides a lower-cost solution than the conventional method using multiple lithography masks. *Id.*, 5:51-53, 5:65-67; Banerjee ¶ 59.

During prosecution, the Examiner rejected various claims under §102(a)(1) as being anticipated by Oh (U.S. Patent Publication 2016/0358855A1) and by Matsuda (U.S. Patent Publication 2016/0020169A1). Ex. 1002, 152-56. The Examiner further rejected the remaining claims under §103 over Matsuda in view of Examiner's Official Notice. *Id.*, 156-57. The Applicant amended the independent claims, adding a high-k dielectric layer to the gate stack. *Id.*, 201-08. The Examiner then allowed the amended claims. *Id.*, 239; Banerjee ¶ 60.

What the Applicant failed to acknowledge in the specification or during prosecution, however, is that every aspect of its alleged invention, including the high-k dielectric layer that secured allowance, was conventional by the time of the application was filed, as this Petition demonstrates. Banerjee ¶ 61.

VII. CLAIM CONSTRUCTION

The Board in IPR proceedings applies the same *Phillips* claim-construction standard used in district-court cases. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). For purposes of institution, Petitioner submits that all terms of the '711 patent's claims may be afforded their plain and ordinary meaning. Banerjee ¶ 62.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '711 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts. Banerjee, ¶ 42.

IX. DESCRIPTION OF THE PRIOR ART

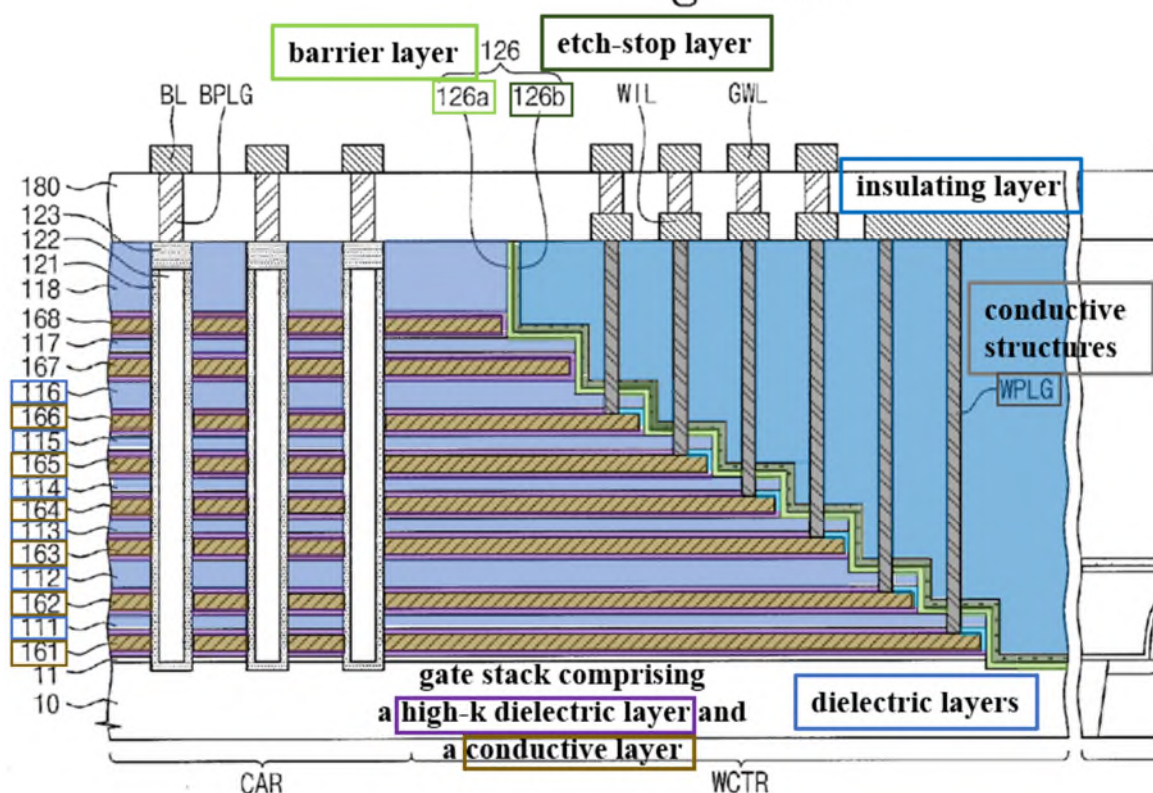
The prior art is analogous to the '711 patent, *e.g.*, they are in the same field of endeavor of improving 3D memory devices. Banerjee ¶ 65.

A. Kim

Kim discloses a 3D semiconductor memory device with a cell-array region, a peripheral-circuit region, and a word-line contact region WCTR disposed therebetween. Kim, Abstract, [0037]. Kim focuses on resolving the difficulty of planarizing the interlayer dielectric (analogous to the insulating layer of the '711 patent) between the regions. *Id.*, [0024]-[0025]; Banerjee ¶¶ 66-67.

Kim's descriptions of the word-line contact region WCTR render obvious the alleged invention of the '711 patent. This is readily apparent by comparing Kim's Figure 22A with Figures 9A-9B of the '711 patent in §VI above.

Fig. 22A



Kim, Fig. 22A; Banerjee ¶ 68.

Kim discloses embodiments in which a gate stack is disposed over a dielectric layer at each step, even though its figures show the opposite order. For example, after describing the layer ordering in its figures, Kim discloses that “[i]n other embodiments, each of top surfaces of the sacrificial layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word line contact region WCTR.” Kim, [0090]. Sacrificial layers SC1-SC8 are replaced with, and positionally correspond to, gate stacks in the fully formed device comprising gate-electrode layers and blocking layers. *Id.*, [0104]-[0105], [0198]-[0200]. More specifically, the edge portions of the sacrificial layers SC1-SC8 may

be exposed as the top surfaces of the steps. *Id.*, [0091], [0240]. That is, the edge portions of the gate stacks are directly below the first stop layer 126a. Banerjee ¶ 69. Accordingly, Kim discloses disposing a gate stack over a dielectric layer at each step. *Id.*

This Petition relies on Kim's Figures 17A-22B embodiment comprising an etch-stop layer and a barrier layer. Kim discloses other embodiments, *e.g.*, Figures 5A-14B.

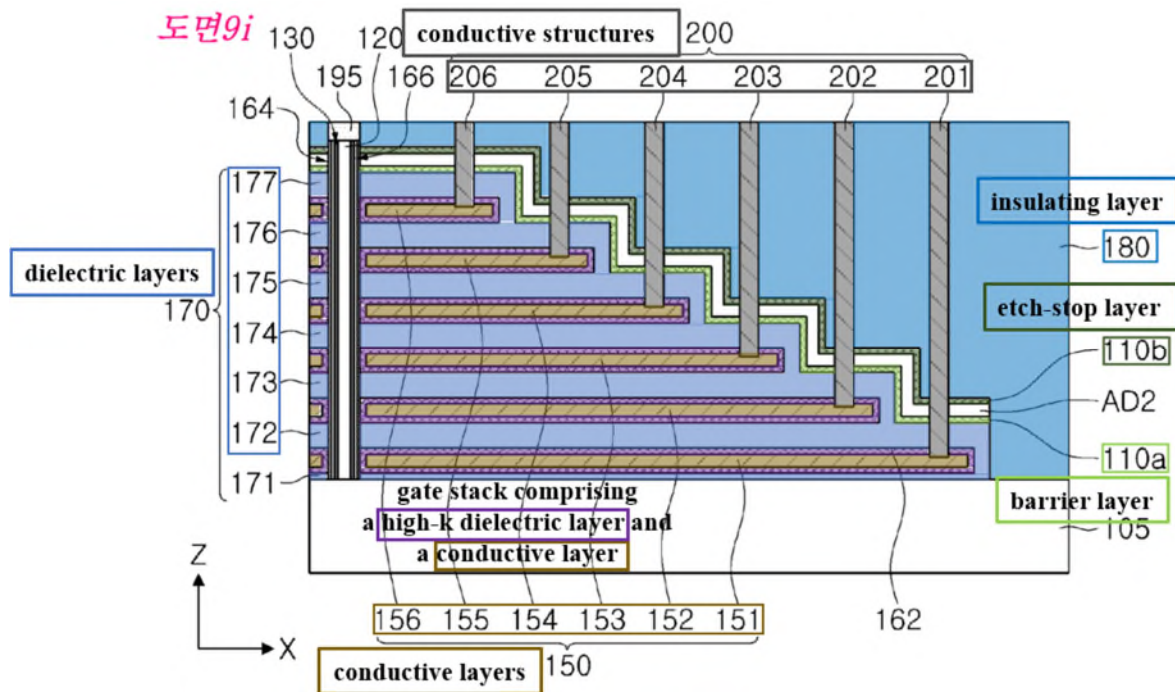
A POSITA would have understood that descriptions of one of Kim's embodiments apply to other embodiments except where the embodiments differ. Banerjee ¶¶ 70-71. Kim discloses closely related embodiments with many of the same elements denoted by the same reference numerals. Kim, [0184]. For example, the embodiments shown in Figures 5A-14B and in Figures 17A-22B are closely related. Thus, Kim states that overlapping descriptions of the same elements are omitted in the descriptions of Figures 17A-22B. *Id.* Further, the descriptions of Figures 17A-22B extensively reference Figures 9A-14B. *Id.*, [0183]-[0212]. Similarly, as another example, descriptions of Figures 26-27 refer to the two embodiments in Figures 17A-22A and 8A-11A. *Id.*, [0221], [0223]-[0224].

B. Park

Park is directed to solving the same alleged problem the '711 patent purports to solve, *i.e.*, preventing the so-called "bridge defects" caused by over-etching the

shallow contact holes when forming word-line contacts. Park, [0014], [0045]-[0046], [0050]-[0051]. What's more, Park's solution is the same as the '711 patent's: using a barrier and etch-stop layer and including a high-k dielectric layer around the gate layers. *Id.*, [0049]-[0051]; Banerjee ¶¶ 72-73.

That Park's descriptions of the word-line connection region disclose the alleged invention of the '711 patent is also readily apparent by comparing Park's Figure 9i with Figures 9A-9B of the '711 patent in §VI above.



Park, Fig. 9i; Banerjee ¶ 74.

Like Kim, Park discloses embodiments in which a gate stack is disposed over a dielectric layer at each step, even though its figures show the opposite order. For example, with respect to the Figure 9 embodiment, Park discloses that “a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad

regions (P1-P6).” Park, [0102]. This describes Figure 9a. Park, however, further discloses that “unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).” *Id.* Park teaches the same regarding a closely related Figure 4/8 embodiment. *Id.*, [0042]. Like Kim, Park’s sacrificial layers 140 are replaced with gate stacks. *Id.*, [0104]-[0105]. Accordingly, Park discloses disposing a gate stack over a dielectric layer at each step. Banerjee ¶ 75.

This Petition relies on the embodiment shown in Figures 5 (perspective view) and 9a-9j (cross-sectional views), comprising an etch-stop layer and a barrier layer. Park, [0100]. Park discloses other embodiments, *e.g.*, one illustrated in Figures 4 (perspective view) and 8a-8m (cross-sectional views). *Id.*, [0073].

A POSITA would have understood that descriptions of one of Park’s embodiments apply to other embodiments except where the embodiments differ. Banerjee ¶¶ 76-77. Park discloses closely related embodiments and teaches that “various embodiments may be combined,” and “elements indicated by the same symbols in the drawings are the same elements.” Park, [0017]. Further, most aspects of the Figure 5 embodiment “are the same as” the Figure 4 embodiment. *Id.*, [0049]. Thus, disclosures of Figures 4 and 8a-8m apply to Figures 5 and 9a-9j except where they differ.

C. Fang

Fang discloses a 3D semiconductor memory device with a staircase structure. Fang, [0002]. The structure comprises alternating dielectric layers and conductive layers. *Id.*, Abstract. The structure further comprises a silicon-nitride etch-stop layer and an oxide insulating layer. *Id.* Conductive word-line structures contacting the conductive layers are formed in openings through the insulating layer, the etch-stop layer, and the dielectric layers:

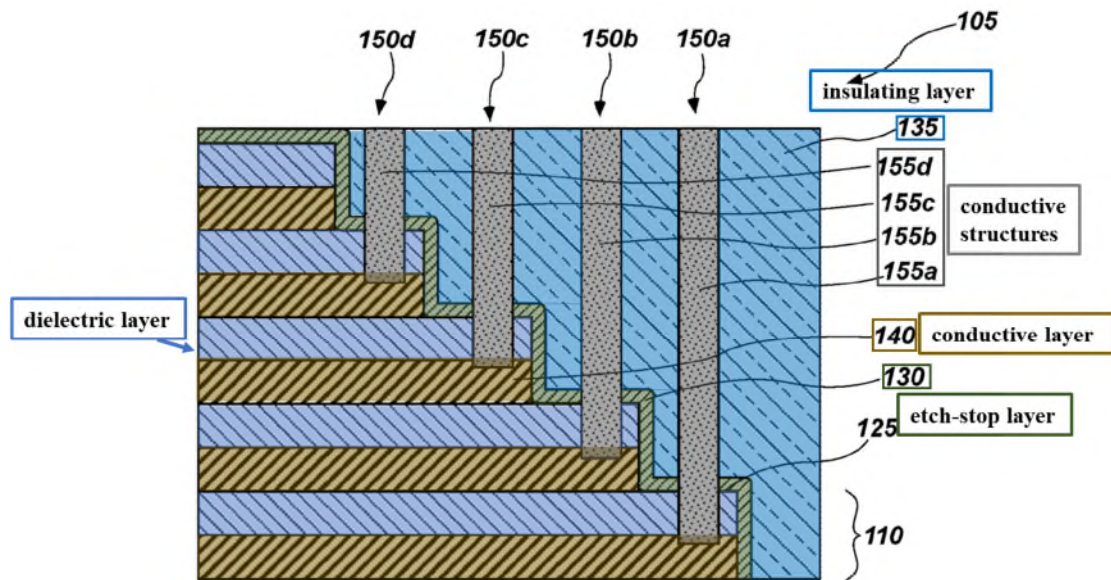


FIG. 6

Id., Fig. 6; Banerjee ¶¶ 78-79.

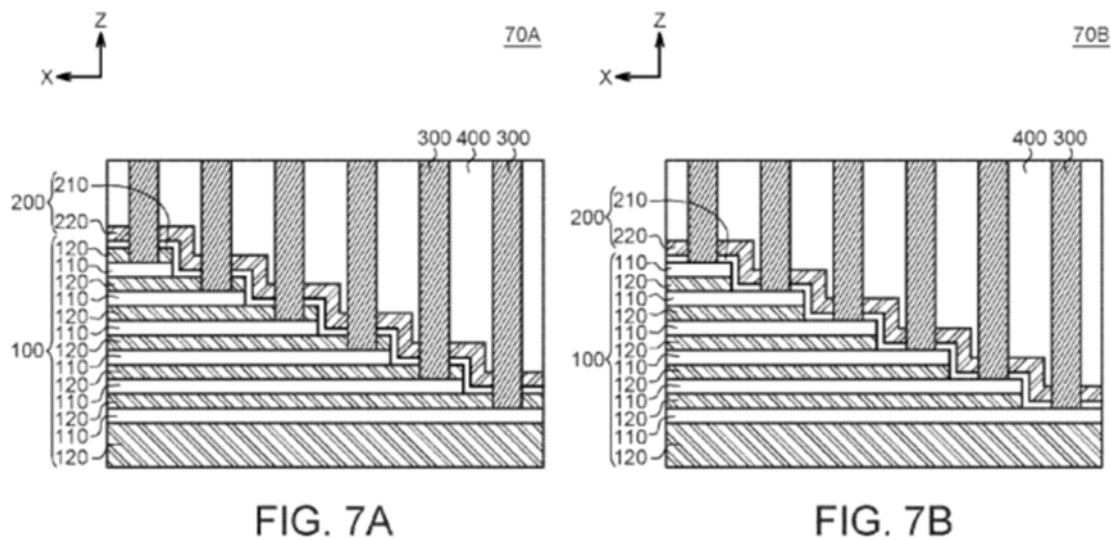
X. GROUND 1: KIM IN VIEW OF A POSITA'S KNOWLEDGE

A. Kim Discloses “a Gate Stack Disposed over a Dielectric Layer”

Kim discloses the gate-stack-on-top layer ordering even though its figures show the opposite order. §IX.A. This teaching of the gate-stack-on-top layer

ordering applies to the Figure 17A-22B embodiment. *Id.* (Kim’s descriptions apply to common aspects across embodiments); Banerjee ¶ 80. Kim’s teaching at least renders the limitation obvious. *Chamberlain Grp., Inc. v. Techtronic Indus. Co.*, 935 F.3d 1341, 1350 (Fed. Cir. 2019) (a reference invalidates if it enables a POSITA to “at once envisage” “the claimed arrangement”).

Additionally, a POSITA would have known that either order was a common alternative. For example, Chen discloses both orders side-by-side:



Chen, Figs. 7A (dielectric on top), 7B (conductor on top), [0044]-[0046]. A POSITA would have known that either order was routine, highly predictable, and would have had a reasonable expectation of success for implementing a gate-stack-on-top embodiment. Banerjee ¶ 81.

At a minimum, Kim’s teaching on reversing the order represents a “known technique” that is at least “a *suitable* option” for the Figures 17A-22B embodiment.

Retractable Techs., Inc. v. Becton, Dickinson & Co., 653 F.3d 1296, 1303 (Fed. Cir. 2011) (emphasis in original); Banerjee ¶ 82.

Below, Kim's figures are modified to show this gate-stack-on-top ordering. Based on Kim's express teaching and a POSITA's knowledge, a POSITA would have "at once envisage[d]" "the claimed arrangement." *Chamberlain Grp.*, 935 F.3d at 1350; Banerjee ¶ 83. For example, prior-art references with gate-stack-on-top configurations (two additional examples below) would have helped a POSITA visualize a Kim embodiment with gate stacks on top:

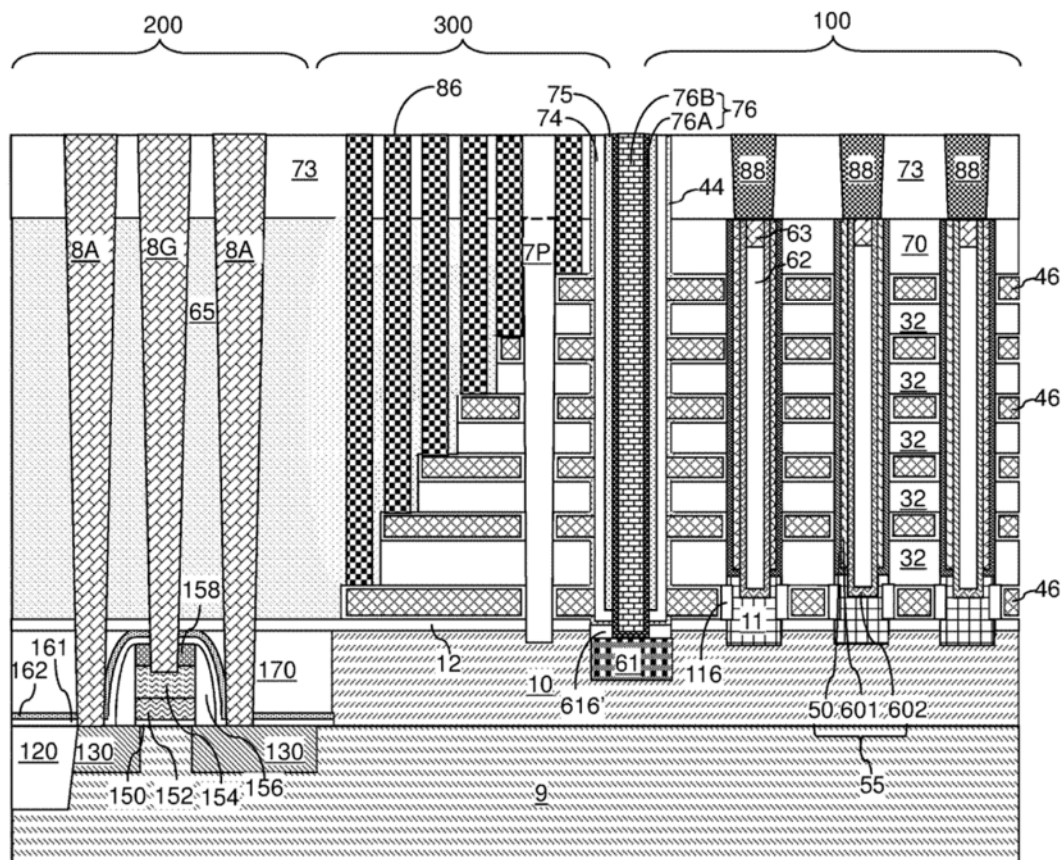
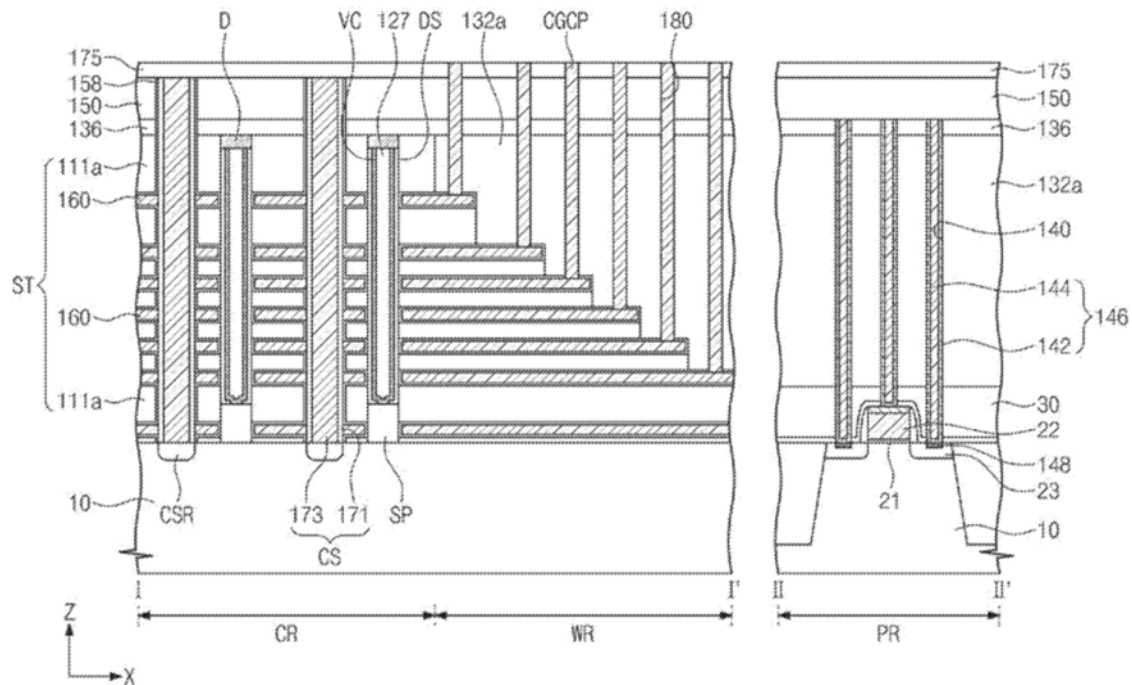


FIG. 13

Ex. 1015, Fig. 13.

FIG. 20



Ex. 1016, Fig. 20.

For clarity, the modified Kim figures are annotated with “Gate-Stack-on-Top.” Banerjee ¶ 84.

B. Claim 1:

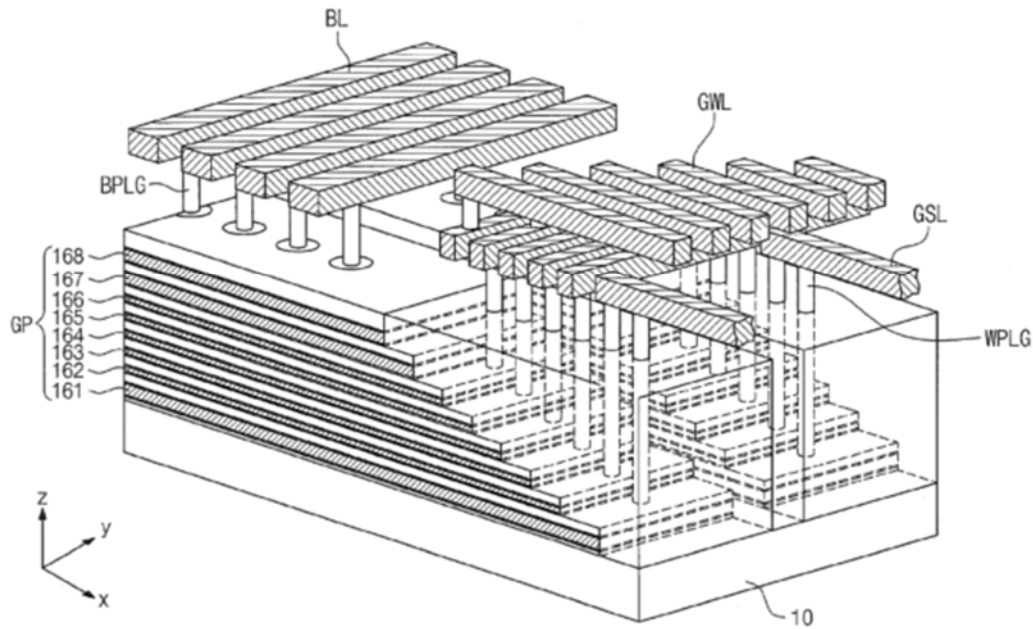
1. [1.PRE] “A semiconductor structure, comprising:”

Kim discloses *a semiconductor structure*, e.g., a 3D semiconductor device.⁴

Kim, Abstract.

⁴ Red italics in the claim-mapping sections denote claim language.

Fig. 4



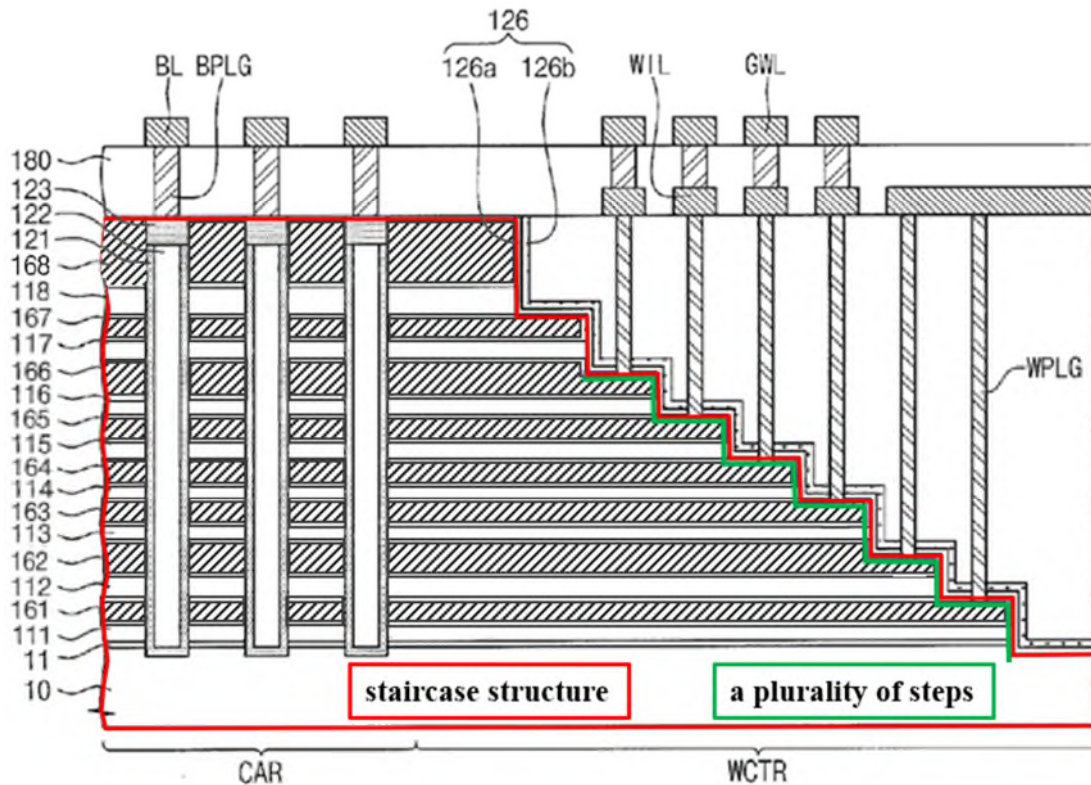
Id., Fig. 4.

2. [1.A] “a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;”

Kim at least renders this limitation obvious. Banerjee ¶ 86.

Kim’s 3D semiconductor device comprises *a staircase structure comprising a plurality of steps*:

Gate-Stack-on-Top Fig. 22A

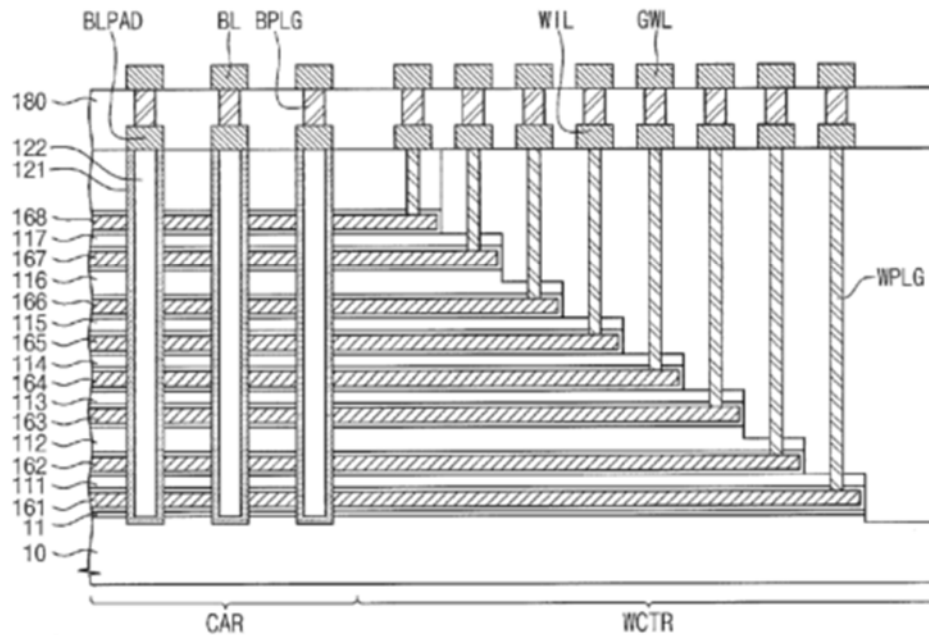


Kim, Fig. 22A, [0008], [0185] (“[a] stacked layer structure ST having the stepwise structure”), [0211]; Banerjee ¶ 87.

As an initial matter and as shown above, the *plurality of steps* may be the bottom six steps, which is relevant to limitation [1.E], because [1.E] requires “wherein each conductive structure is formed on the conductive layer of the each step.” The *plurality of steps* need not include all steps of the *staircase structure*, because the term *a staircase structure comprising a plurality of steps* permits additional steps given the use of *comprising*. Banerjee ¶ 88.

Additionally, it would have been understood, and certainly obvious, that there is a conductive structure that is not shown on the top steps, and the *plurality of steps* would then include all steps. This is because the channel structures are, in effect, a string of memory cells at the interface of the channel and the word lines (coupled to the conductive structures), and for various operations (*e.g.*, a read operation) targeting a memory cell in the middle of the string, it is necessary to turn on all memory cells above and below the target cell by applying a voltage (*e.g.*, pass voltage) to the memory cells through the word lines (*i.e.*, gates). §V. Put simply, the memory would not be able properly function without a contact to each gate layer. Indeed, usually the top gate layer is a select (to turn on the memory string) layer, *e.g.*, drain-select layer. Not surprisingly, it was thus conventional for a staircase structure to have a conductive structure on every step. Park, Fig. 9i; Fang, Fig. 17; Chen, Figs. 7A-7B. Indeed, Kim discloses such an embodiment, further demonstrating that it would have been understood, and obvious, to include a contact on the top steps:

Fig. 30

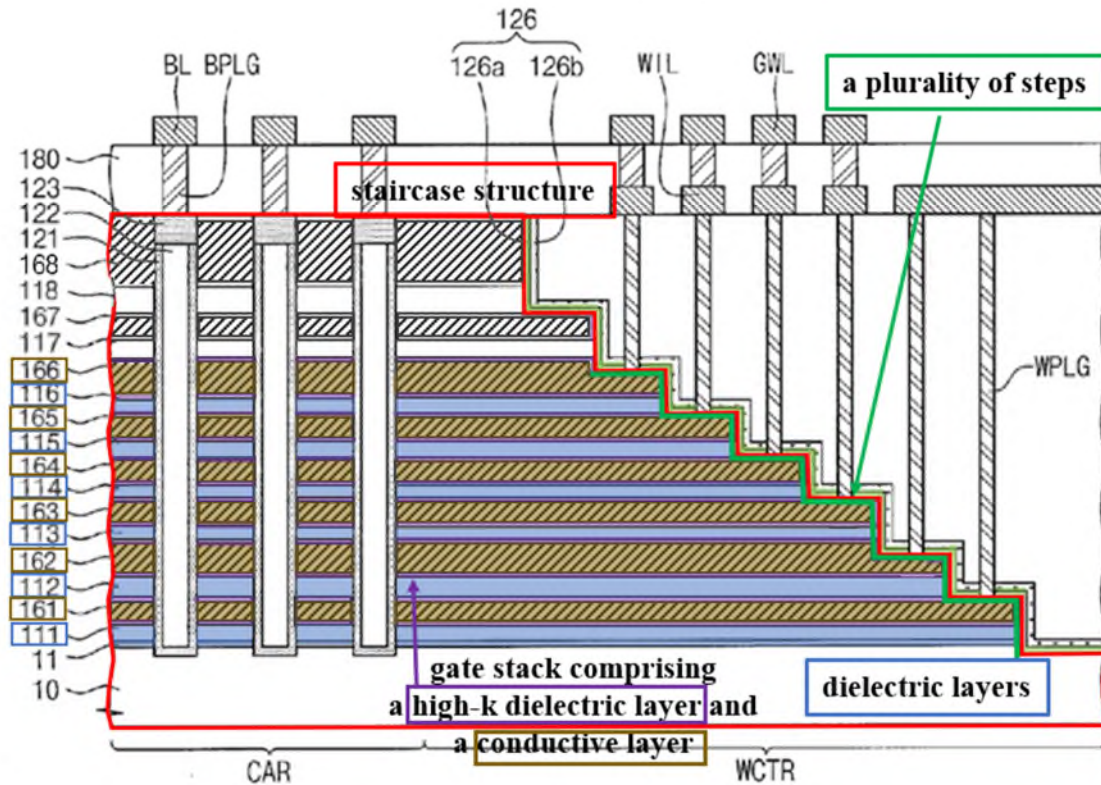


Kim, Fig. 30; Banerjee ¶ 89. While the figures do not annotate the top step, per the above, this Ground equally applies to including contacts on each step of the staircase.

In the gate-stack-on-top embodiment, *each step comprises a gate stack disposed over a dielectric layer* (one of “insulating layers” 111-116), *the gate stack comprising a high-k dielectric layer* (“blocking insulating layer 150c,” shown in purple, included in “data storing layer” 150⁵) *and a conductive layer* (one of “gate electrodes” 161-166):

⁵ 150 is shown in, *e.g.*, Figures 13A, 15A-D.

Gate-Stack-on-Top Fig. 22A



Kim, Fig. 22A, [0229] (“the stacked layer structure ST may include gate conductive layers 101 to 108 and the insulating layers 111 to 118 alternately stacked on the substrate 10.”); [0185]-[0186] (“stepwise structure ... [comprising] insulating layers 111 to 118....”), [0211], [0064], [0086]-[0087], [0202]. “The formation of the gate electrodes 161 to 168 may include forming a gate conductive layer....” *Id.*, [0202]; *id.*, [0157]; Banerjee ¶ 90.

Kim discloses “forming a data storing layer 150 and gate electrodes 161 to [166]” between insulating layers. Kim, [0200]. The data-storing layer 150 forms a conformal covering of the gate electrodes. *Id.*, [0202], Figs. 13A-13B. The data-

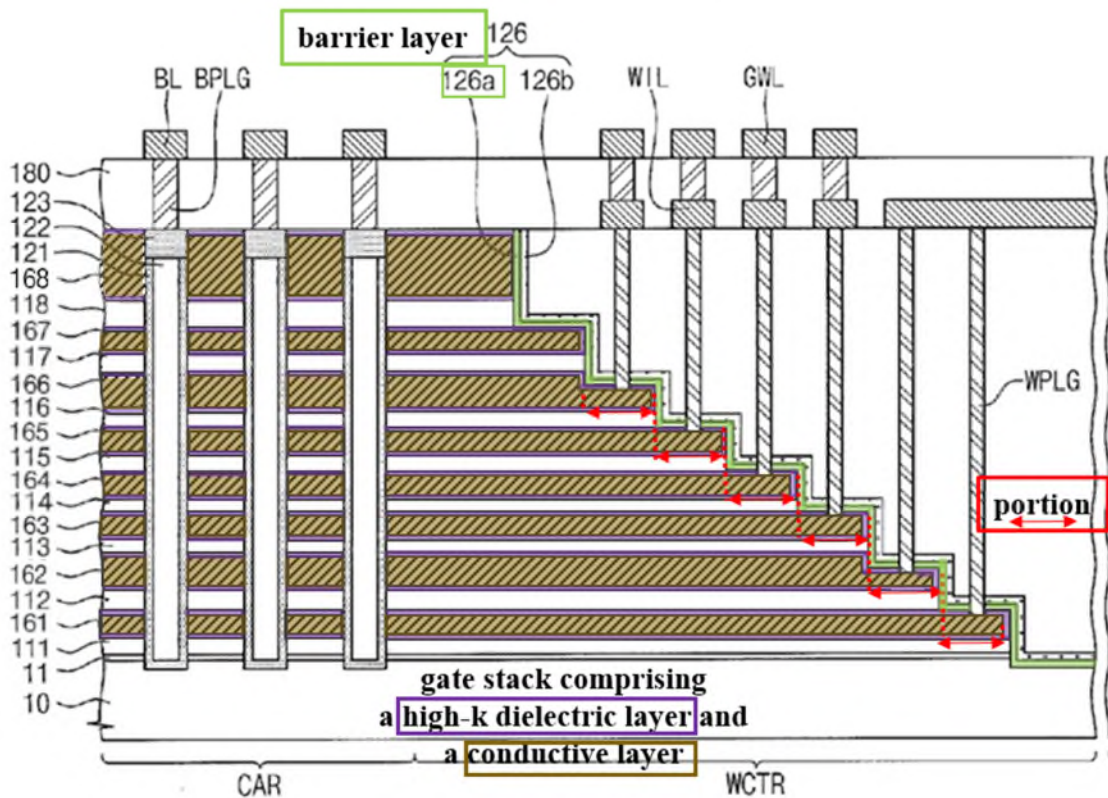
storing layer may include a blocking insulating layer 150c, which may comprise *a high-k dielectric*. *Id.*, [0148], [0151], Figs. 15B-15D; Banerjee ¶ 91.

3. [1.B] “a barrier layer disposed over a portion of the gate stack of the each step;”

Preliminarily, Kim’s disclosures of the first stop layer 125a and the second stop layer 125b apply to the layers labeled 126a and 126b in Figure 22A, respectively, for purposes of these claims. Banerjee, ¶ 92. The “stepwise etch stop pattern [comprising layers] 126[a and 126b]” is simply derived from removing the portions of the first stop layer 125a and the second stop layer 125b at the top surface of Kim’s staircase structure. Kim, [0201]; *compare id.*, Fig. 19A (showing 125a-125b) *with id.*, Fig. 20A (showing 126a-126b after the removal).

Kim discloses *a barrier layer* (“first stop layer” 126a) *disposed over a portion of the gate stack of the each step*:

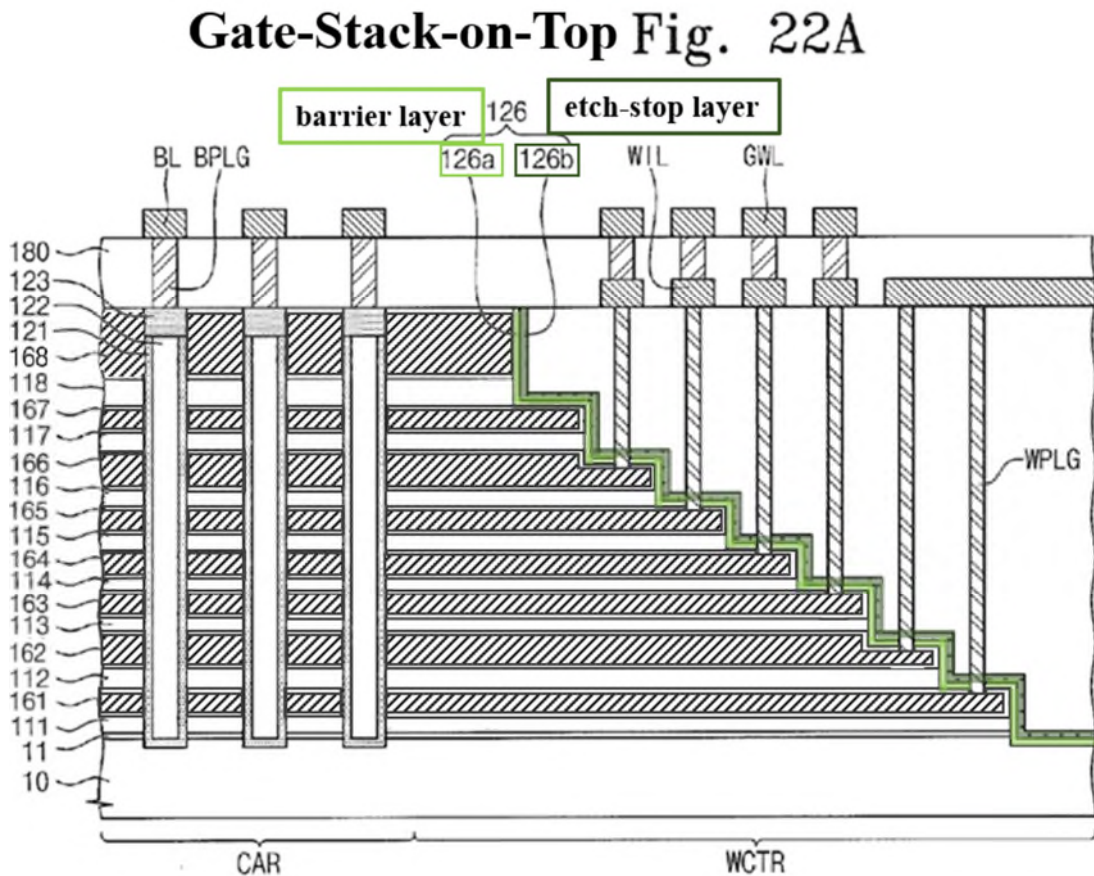
Gate-Stack-on-Top Fig. 22A



Kim, Fig. 22A. A POSITA would have understood the etch selectivity of the first stop layer to serve the purpose of preventing punch-through and protecting underlying structures. *Id.*, [0186]-[0187]; §VI (explaining that a barrier layer is just another etch-stop layer); Banerjee ¶ 93. The first stop layer 125a in Kim is “formed to conformally cover an exposed surface,” including a top surface of a step or, equivalently, *a portion of the gate stack*, of the staircase structure. Kim, [0187]; see also *id.*, [0185], [0213].

4. [1.C] “an etch-stop layer disposed on the barrier layer;”

Kim discloses *an etch-stop layer* (“second stop layer” 126b) *disposed on the barrier layer* (“first stop layer” 126a):



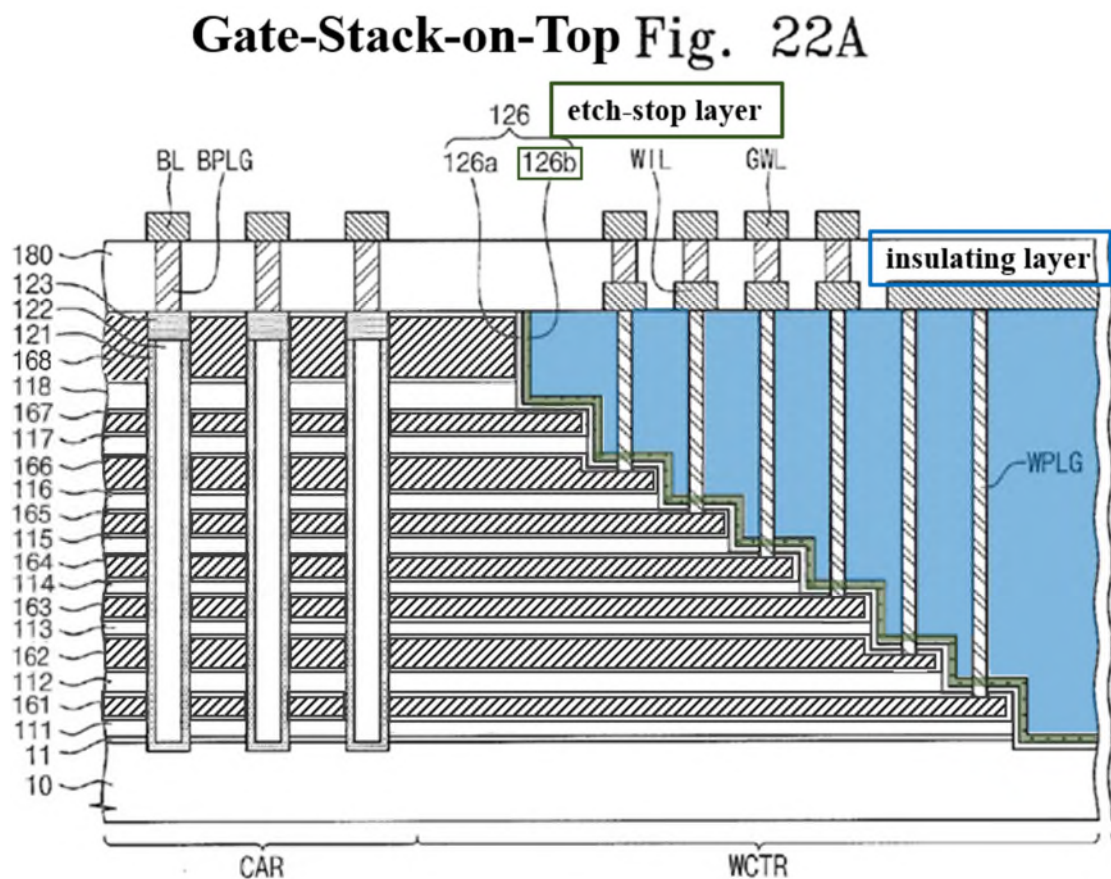
Kim, Fig. 22A, [0201]. A POSITA would have understood the etch selectivity of the second stop layer to serve the purpose of preventing punch-through and protecting underlying structures. *Id.*, [0186]-[0187]; Banerjee ¶ 94.

5. [1.D] “an insulating layer disposed on the etch-stop layer;
and”

Preliminarily, similar to the interchangeability of reference numerals 125 and 126 for purposes of these claims, Kim’s descriptions of the interlayer dielectric 130

apply to the interlayer insulating pattern 134 in Figure 22A. Banerjee ¶ 95. The interlayer insulating pattern 134 results from the interlayer dielectric 130 after a planarization process. Kim, [0193]; *compare id.*, Fig. 18A (showing the interlayer dielectric 130) with Fig. 19A (showing pattern 134 after planarization).

Kim discloses *an insulating layer* (“interlayer insulating pattern” 134) *disposed on the etch-stop layer* (“second stop layer” 126b):

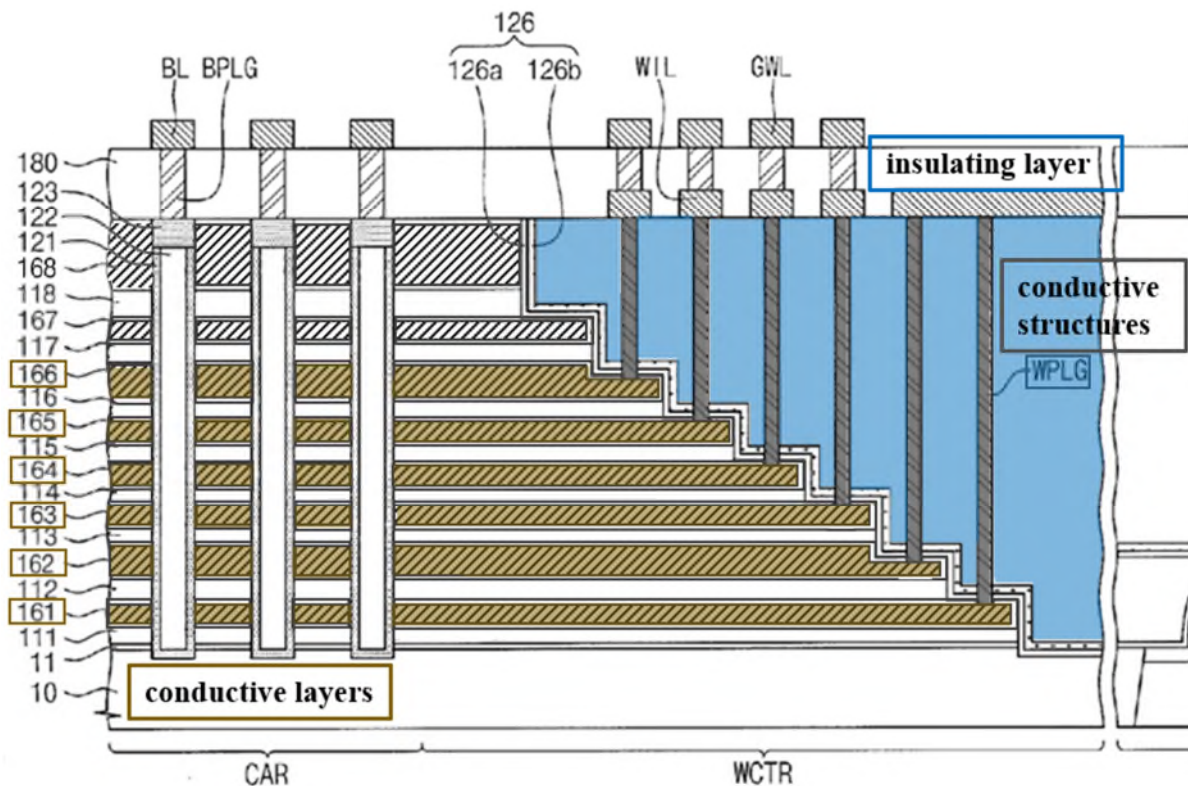


Kim, Fig. 22A, [0094], [0213] (“the interlayer dielectric 130 may be formed on the etch stop layer 125”), [0188] (same); Banerjee ¶ 96.

6. [1.E] “a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.”

Kim discloses *a plurality of conductive structures* (“word line contact plugs WPLG[s]”) *formed in the insulating layer* (“interlayer insulating pattern” 134), *wherein each conductive structure* (“WPLG”) *is formed on the conductive layer* (corresponding one of the “gate electrodes” 161-166) *of the each step*:

Gate-Stack-on-Top Fig. 22A

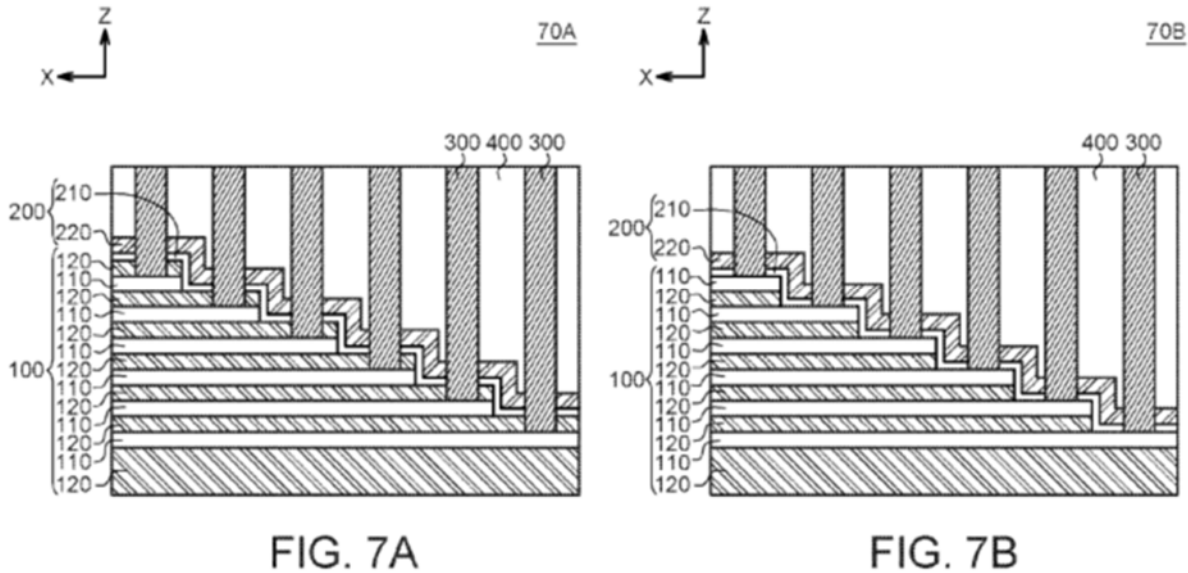


Kim, Fig. 22A, [0173]-[0174] (“the formation of word line contact plugs WPLG ... may include forming contact holes to penetrate the interlayer insulating pattern 134 ..., and filling the contact holes with a conductive material.”), [0210]-[0211]

(“WPLG may be formed to connect the global word lines GWL and the gate electrodes 161 to 168”); Banerjee ¶ 97.

When the gate stack is disposed over the dielectric layer at each step, the conductive structures WPLGs are still formed on the respective gate electrodes because the function of the WPLGs is to electrically connect the gate electrodes with global word lines GWL. Kim, [0175], [0210], [0251]-[0252]. Thus, it is unnecessary for the WPLGs to reach the lower layer (the dielectric layer). In other words, *each conductive structure* (“WPLG”) *is formed on the conductive layer* (corresponding one of the “gate electrodes” 161-166). Banerjee ¶ 98.

A POSITA would have known that the contact between the conductive word-line structures (*e.g.*, WPLGs) and the conductive layers remains the same, independent of the dielectric layer/gate stack ordering. For example, Chen discloses both orders:



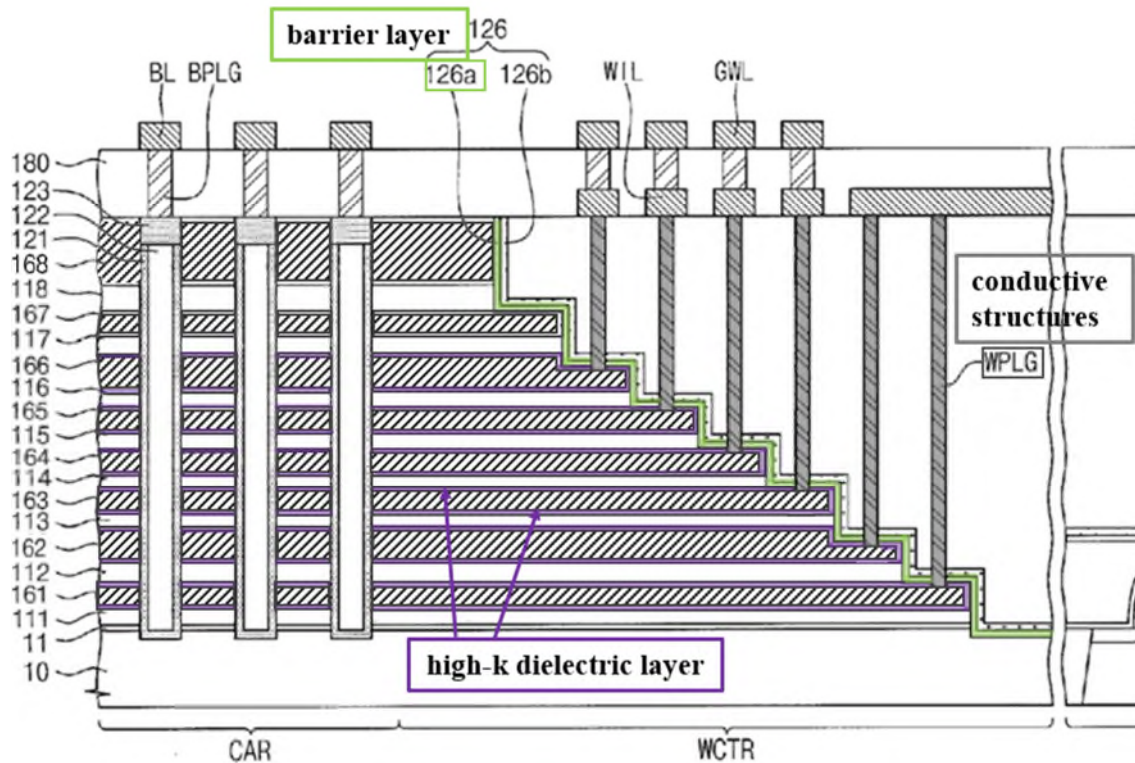
Chen, Figs. 7A (dielectric on top), 7B (conductor on top). In both embodiments, each conductive structure 300 is formed on, and contacts, a respective conductive layer 110. *Id.*, [0045]-[0046]. As discussed, this contact is needed for the functioning of the control gate. Banerjee ¶ 99.

C. Claim 2:

1. [2] “The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the barrier layer and the high-k dielectric layer.”

Kim discloses that *the plurality of conductive structures* (“WPLG[s]”) *extend[s] through the barrier layer* (“first stop layer” 126a) *and the high-k dielectric layer* (“blocking insulating layer” 150c):

Gate-Stack-on-Top Fig. 22A



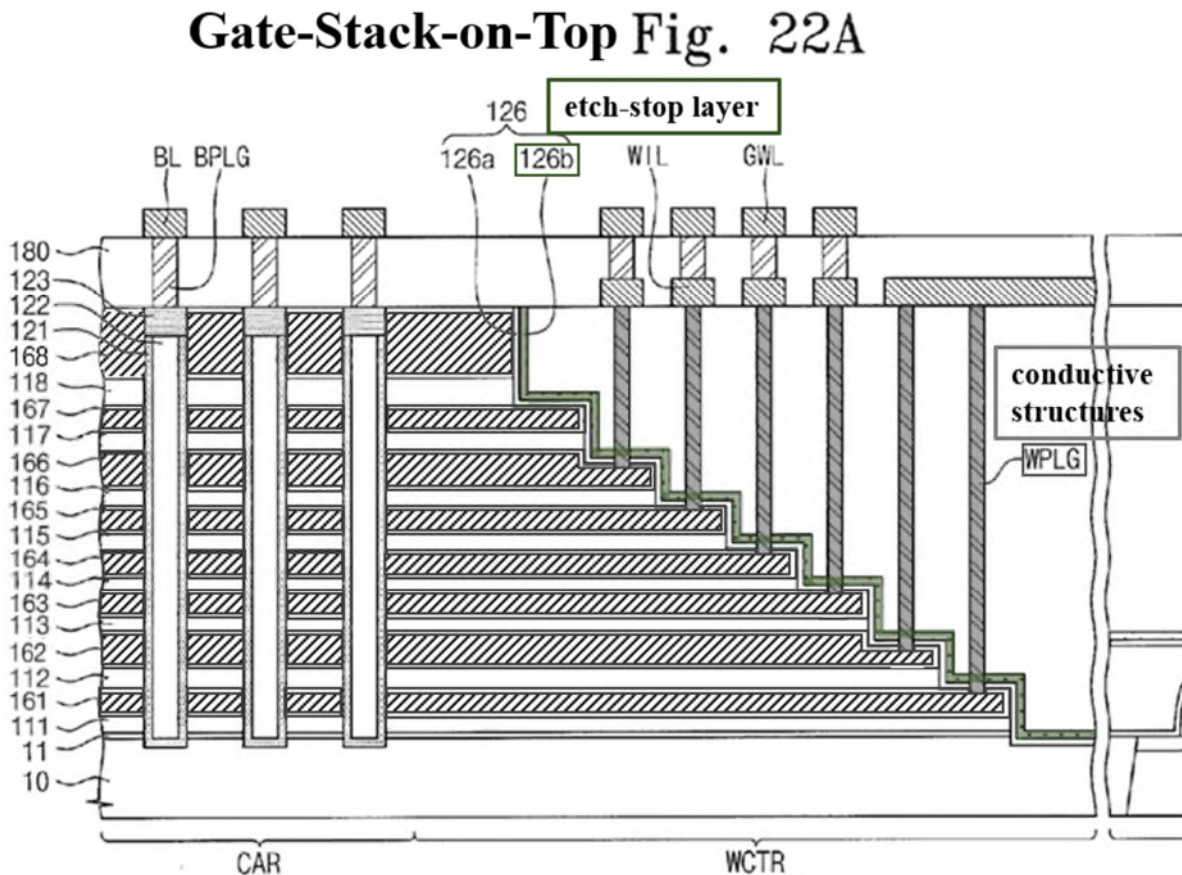
Kim, Fig. 22A, [0174] (“the word line contact plugs WPLG ... may be formed to penetrate ... the data storing layer 150...”), [0187] (addressing etch characteristic of the first stop layer).

The WPLG “connect[s] the global word lines GWL and the gate electrodes.” Kim, [0210]-[0211]. Thus, the WPLG must extend through the first stop layer and the blocking insulating layer to reach the gate electrodes regardless of the layer ordering. §§X.A, X.B.6 (a POSITA’s knowledge); Banerjee ¶¶ 100-101.

D. Claim 3:

1. [3] “The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the etch-stop layer.”

Kim discloses that *the plurality of conductive structures* (“WPLG[s]”) *extend[s] through etch-stop layer* (“second stop layer” 126b):



Kim, Fig. 22A, [0187] (addressing etch characteristic of the second stop layer); §X.C.1 (electrical-connection requirement); Banerjee ¶ 102.

E. Claim 4:

1. [4] “The semiconductor structure of claim 1, wherein the barrier layer comprises silicon oxide.”

Kim discloses that *the barrier layer* (“first stop layer” 125a/126a) *comprises silicon oxide*. Kim, [0187] (“the first stop layer 125a may be formed of silicon oxide....”); §X.B.3 (equivalence of 125a and 126a); Banerjee ¶ 103.

F. Claim 5:

1. [5] “The semiconductor structure of claim 1, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.”

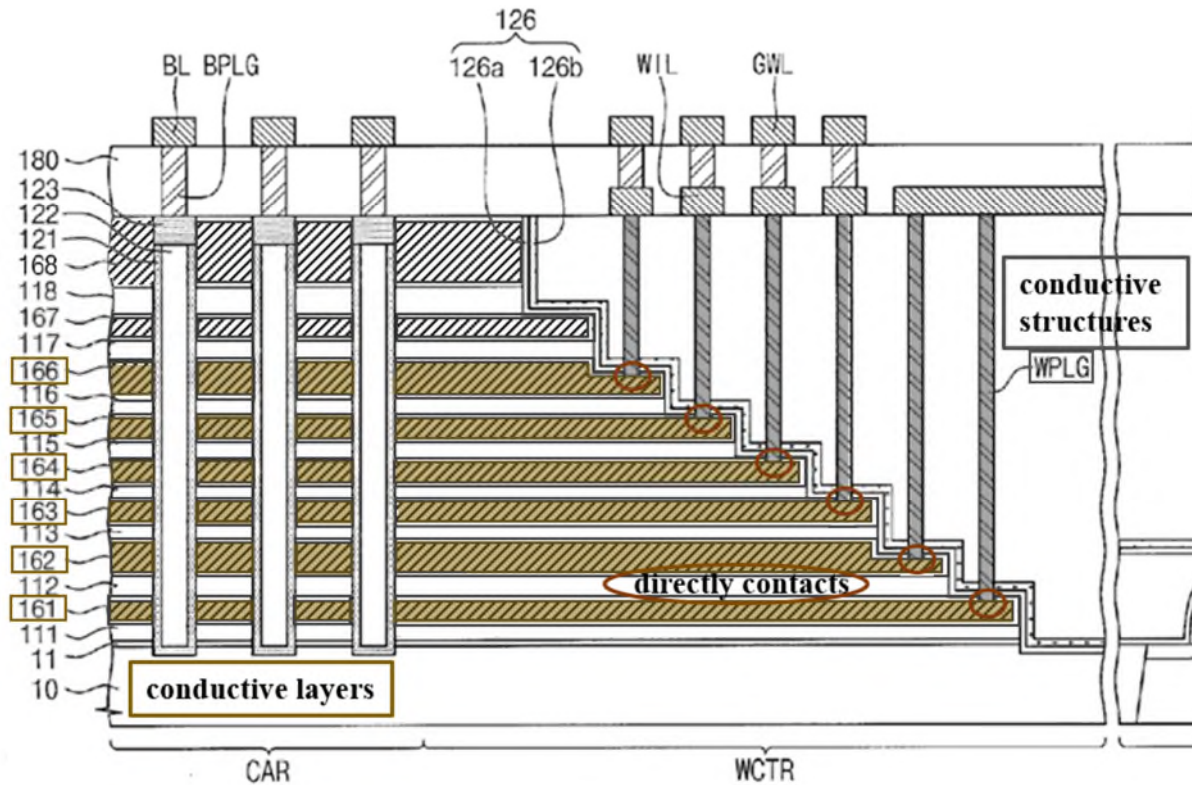
Kim discloses that *the etch-stop layer* (“second stop layer” 125b/126b) *comprises ... silicon nitride*. Kim, [0187] (“the second stop layer 125b may be formed of silicon nitride.”); §X.B.3 (equivalence of 125b and 126b); Banerjee ¶ 104.

G. Claim 6:

1. [6] “The semiconductor structure of claim 1, wherein the each conductive structure directly contacts a corresponding one of the conductive layer of the each step.”

Kim discloses that *the each conductive structure* (“WPLG”) *directly contacts a corresponding one of the conductive layer* (corresponding one of “gate electrodes” 161-166) *of the each step*:

Gate-Stack-on-Top Fig. 22A

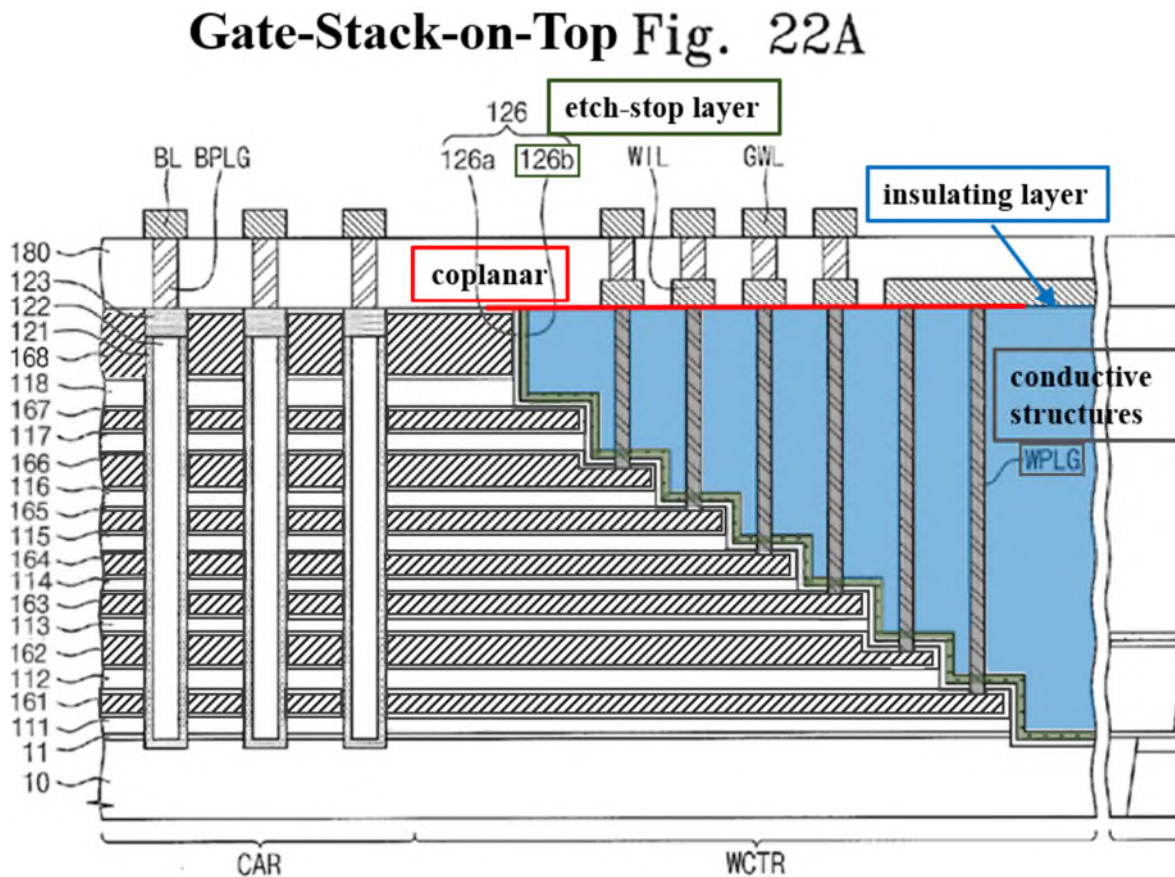


Kim, Fig. 22A. The WPLG “connect[s] the global word lines GWL and the gate electrodes.” *Id.*, [0210]-[0211]. The direct contacts between WPLGs and gate electrodes establish those connections. §§X.A, X.B.6 (a POSITA’s knowledge); Banerjee ¶ 105.

H. Claim 7:

1. [7] “The semiconductor structure of claim 1, wherein top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.”

Kim discloses that *top surfaces of the plurality of conductive structures* (“WPLG[s]”), *the insulating layer* (“interlayer insulating pattern” 134), and *a portion of the etch-stop layer* (“second stop layer” 126b) *are coplanar*:



Kim, Fig. 22A.

This coplanar surface is achieved through, *e.g.*, planarizing the interlayer dielectric 130, which can “expose the top surface of the [staircase structure]” and

result in “the interlayer insulating pattern 134 having a flat top surface.” Kim, [0103], [0193]; Banerjee ¶¶ 106-107.

The top surfaces of WPLG, the interlayer insulating pattern 134, and the second stop layer 126b, as shown in the figure above, meet the plain and ordinary meaning of “top surface” as a POSITA would understand from the ’711 patent. Banerjee ¶ 108.

I. Claim 8:

1. [8] “The semiconductor structure of claim 1, wherein the plurality of conductive structures comprise one or more of tungsten, cobalt, nickel, copper, and aluminum.”

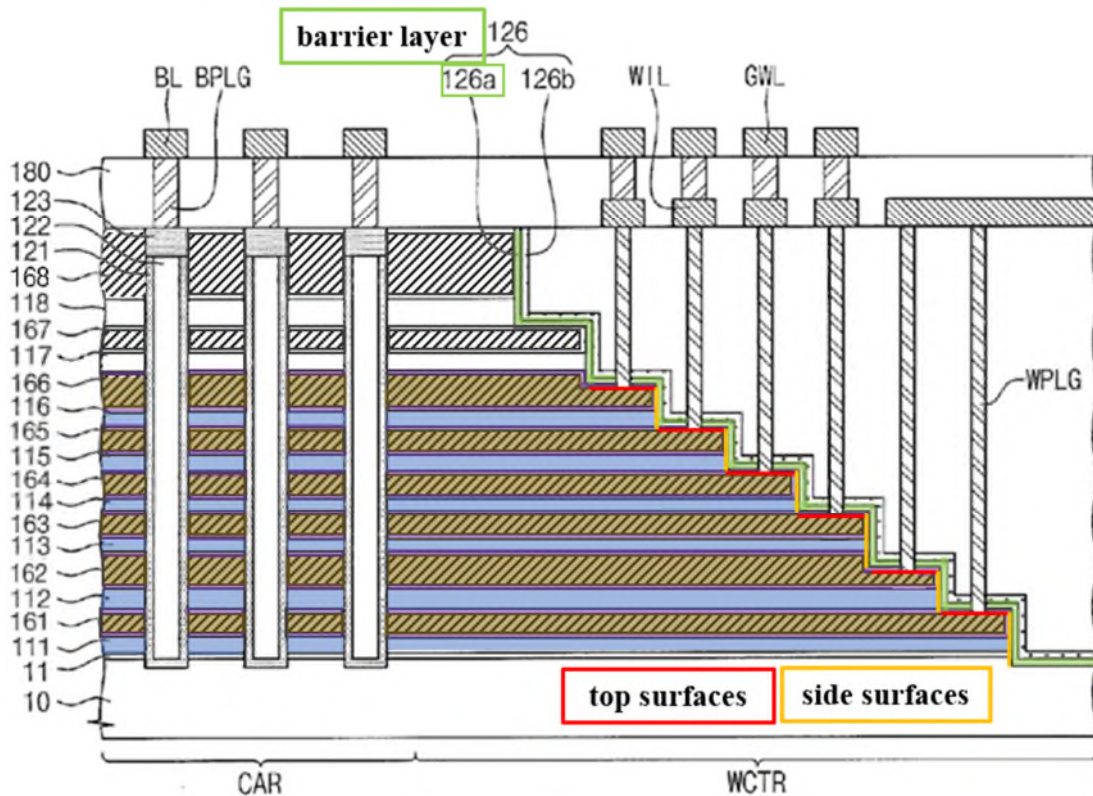
Kim discloses that *the plurality of conductive structures* (“WPLG[s]”) *comprise[s] ... tungsten*. Kim, [0173] (“the word line contact plugs WPLG ... may be formed of a metallic material (*e.g.*, tungsten).”); §IX.A (descriptions of Figures 5A-14B apply); Banerjee ¶ 109.

J. Claim 9:

1. [9] “The semiconductor structure of claim 1, wherein the barrier layer is formed on side and top surfaces of the plurality of steps.”

Kim discloses that *the barrier layer* (“first stop layer” 126a) *is formed on side and top surfaces of the plurality of steps*:

Gate-Stack-on-Top Fig. 22A



Kim, Fig. 22A. Kim discloses that “[t]he first stop layer 125a may be formed to conformally cover an exposed surface of the stacked layer structure ST.” *Id.*, [0187]. And Kim teaches that “a conformal layer has substantially the same shape as the surface it covers....” *Id.*, [0144]. Thus, Kim discloses that the first stop layer 125a/126a covers the risers (side surfaces) and treads (top surfaces) of the plurality of steps. *Id.*, [0185], [0213]; Banerjee ¶ 110.

K. Claim 11:

1. [11] “The semiconductor structure of claim 1, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.”

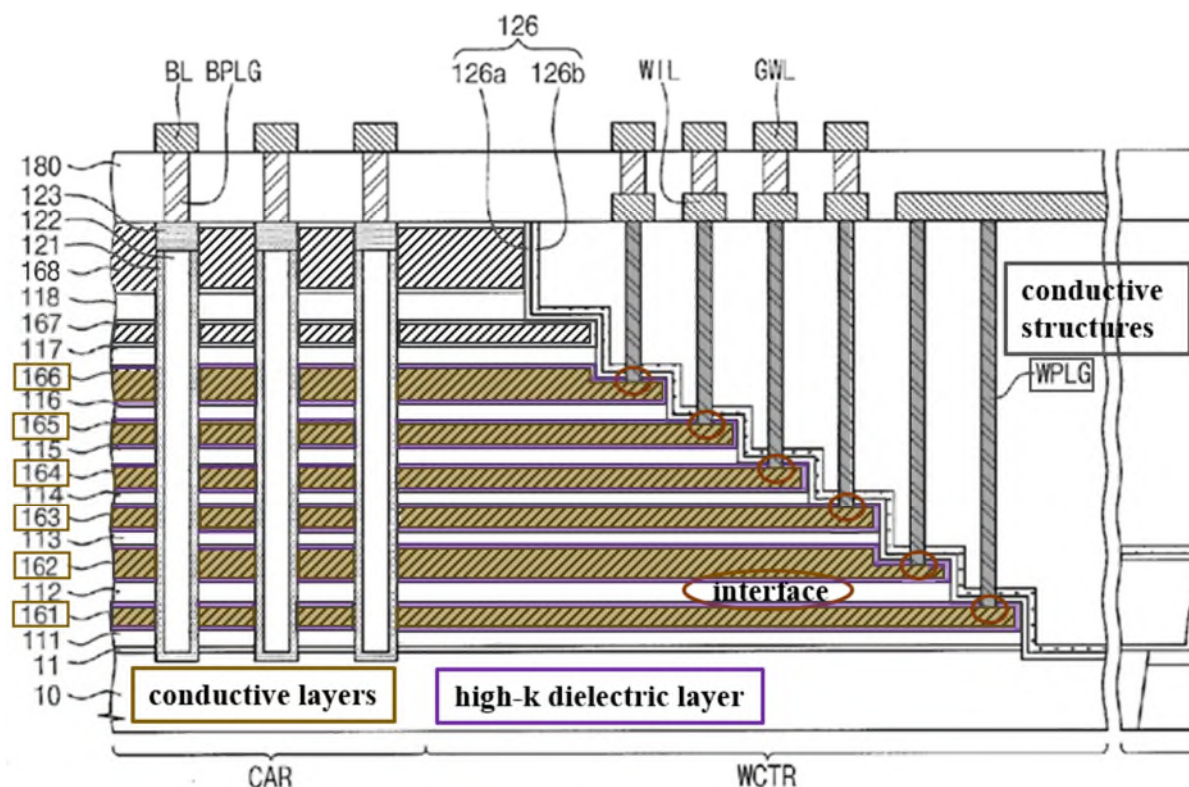
Kim discloses that *the high-k dielectric layer* (“blocking insulating layer” 150c) *comprises hafnium oxide, zirconium oxide, aluminum oxide, [or] tantalum oxide...* Kim, [0151] (“The blocking insulating layer 150c may include ... [a] high-k dielectric, ... *e.g.*, tantalum oxide, ... , hafnium oxide, zirconium oxide, [or] aluminum oxide....”); Banerjee ¶ 111.

L. Claim 12:

1. [12] “The semiconductor structure of claim 1, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.”

Kim discloses that *top and bottom surfaces and a sidewall of the conductive layer* (“gate electrodes” 161-166) *are covered by the high-k dielectric layer* (“blocking insulating layer” 150c), *except at an interface between the conductive layer and the conductive structure* (corresponding “WPLG”):

Gate-Stack-on-Top Fig. 22A



Kim, Fig. 22A; Banerjee ¶ 112.

More specifically, during the formation of the gate stack, “the data storing layer 150 [comprising blocking insulating layer 150c] may be formed to conformally cover ... the recess regions 142” between the insulating layers 111-116. Kim, [0200], [0202]. “Thereafter, the gate electrodes 161 to 16[6] may be formed in ... the [respective] data storing layer 150.” *Id.*, [0202]. Then an opening is etched through an interface in the blocking insulating layer 150c at the vertical opening (which after being filled becomes a WPLG) so that WPLGs “may be formed to

connect the global word lines GWL and the gate electrodes.” *Id.*, [0210]-[0211]; Banerjee ¶ 113.

A POSITA would have found it obvious that the layer ordering would not change the spatial relationship of gate electrodes and blocking insulating layer. Banerjee ¶ 114. For example, because the WPLG “connect[s] the global word lines GWL and the gate electrodes,” (Kim, [0210]-[0211]) the blocking insulating layer would not cover *an interface between the conductive layer* (“gate electrodes” 161-166) *and the conductive structure* (corresponding “WPLG”). §§X.A, X.B.6 (a POSITA’s knowledge).

M. Claim 13:

1. [13.PRE] “A semiconductor structure, comprising:”

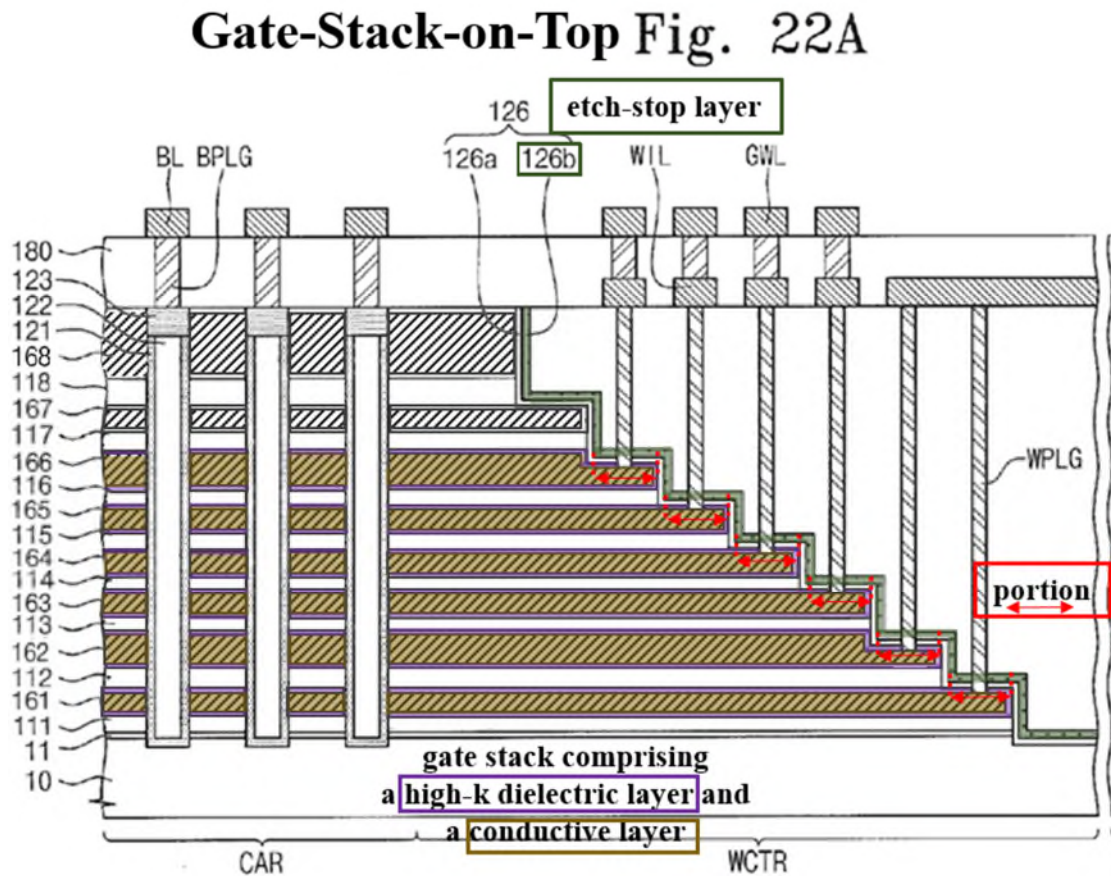
This preamble is identical to that of claim 1. Kim discloses it for the same reason as explained above. §X.B.1; Banerjee ¶ 115.

2. [13.A] “a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;”

This limitation is identical to [1.A]. Kim at least renders it obvious for the same reason as explained above. §X.B.2; Banerjee ¶ 116.

3. [13.B] “an etch-stop layer disposed on a portion of the gate stack of the each step;”

Kim discloses *an etch-stop layer* (“second stop layer” 126b) *disposed on a portion of the gate stack* (one of “gate electrodes” 161-166 and “blocking insulating layer” 150c) *of the each step*:



Kim, Fig. 22A.

Kim discloses limitation [13.B] because the '711 patent defines “on” to include both directly on something and indirectly on that something. Ex. 1001, 4:1-6; Banerjee ¶¶ 117-18.

4. **[13.C] “an insulating layer disposed on the etch-stop layer; and”**

This limitation is identical to [1.D]. Kim discloses it for the same reason as explained above. §X.B.5; Banerjee ¶ 119.

5. **[13.D] “a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer and the high-k dielectric layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.”**

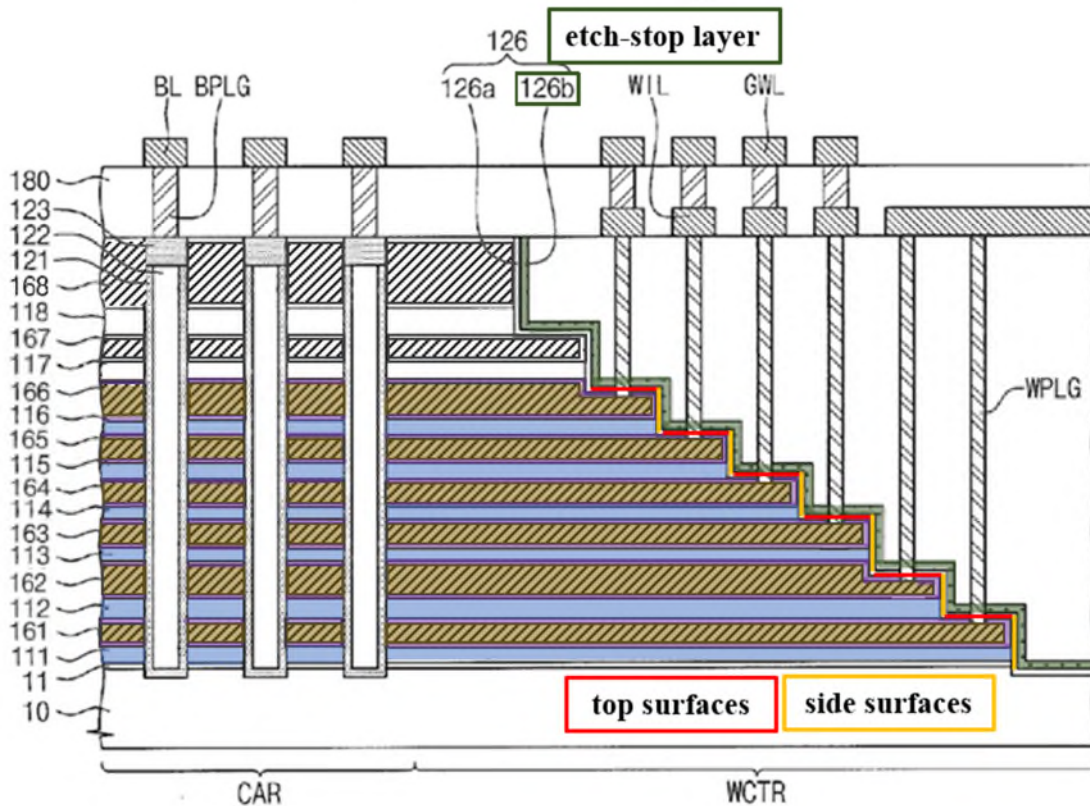
This limitation combines the requirements of limitation [1.E] and claims 2, 3, and 6. Kim at least renders it obvious for the same reason as explained above. §§X.B.6, X.C.1, X.D.1, X.G.1; Banerjee ¶ 120.

N. Claim 14:

1. **[14] “The semiconductor structure of claim 13, wherein the etch-stop layer is formed on a side surface and a top surface of each step.”**

Kim discloses that *the etch-stop layer* (“second stop layer” 126b) *is formed on a side surface and a top surface of each step:*

Gate-Stack-on-Top Fig. 22A



Kim, Fig. 22A.

Kim discloses that the first stop layer 125a (the barrier layer) is formed on side and top surfaces of the plurality of steps. §X.J.1. Kim further discloses that “the second stop layer 125b may be conformally formed on the first stop layer 125a.” Kim, [0187]. And “a conformal layer has substantially the same shape as the surface it covers....” *Id.*, [0144]. Thus, *the etch-stop layer* (second stop layer 126b) *is formed on a side surface and a top surface of each step.* *Id.*, [0256]; Ex. 1001, 4:1-6 (disclosing that “on” something includes both directly and indirectly on that something); Banerjee ¶¶ 121-22.

O. Claim 15:

- 1. [15] “The semiconductor structure of claim 14, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.”**

Kim discloses the additional limitation of claim 15.

Kim discloses that “the second stop layer 125b may be conformally formed on the first stop layer 125a.” Kim, [0187]. Further, “a conformal layer ... has substantially the same thickness throughout.” *Id.*, [0144]. Thus, *thicknesses of the etch-stop layer* (second stop layer 125b/126b) *is the same on the side and top surfaces of each step*. Banerjee ¶¶ 123-24.

P. Claim 16:

- 1. [16] “The semiconductor structure of claim 13, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.”**

The additional limitation of claim 16 is identical to that of claim 5. Kim discloses it for the same reason as explained above. §X.F.1; Banerjee ¶ 125.

Q. Claim 18:

- 1. [18] “The semiconductor structure of claim 13, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.”**

The additional limitation of claim 18 is identical to that of claim 11. Kim discloses it for the same reason as explained above. §X.K.1; Banerjee ¶ 126.

R. Claim 19:

1. **[19] “The semiconductor structure of claim 13, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.”**

The additional limitation of claim 19 is identical to that of claim 12. Kim discloses it for the same reason as explained above. §X.L.1; Banerjee ¶ 127.

XI. GROUND 2: KIM IN VIEW OF FANG

A. Claim 10:

1. **[10] “The semiconductor structure of claim 1, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.”**

Kim at least renders obvious claim 1. §X.B. Kim in view of Fang renders obvious dependent claim 10.

As an initial matter, as the Examiner took official notice, the claimed etch-stop layer thickness “[wa]s notoriously well known in the art.” Ex. 1002, 156. Further, the cited range—spanning three orders of magnitude—“lacks criticality.” *Id.* (citing the equivalent of Ex. 1001, 7:56-8:19); *compare* Ex. 1001 claim 10 with claim 17 (same thickness with or without a barrier layer). Where, as here, the “[d]ifferences between the prior art and the claimed invention[, if any, is merely] dimensional,” not resulting in “differences in performance,” the claim is not valid. *Gardner v. TEC Sys., Inc.*, 725 F.2d 1338, 1345-46 (Fed. Cir. 1984); Banerjee ¶¶ 128-29.

If more is required (it is not), Kim in view of Fang's etch-stop layer teaching renders claim 10 obvious. Fang discloses an analogous semiconductor structure with an etch-stop layer. Fang, Fig. 6, [0020]. To start, Kim's and Fang's etch-stop layers are similar. For example, both of their etch-stop layers may comprise silicon nitride. Kim, [0187]; Fang, [0022]. Fang's etch-stop layer "may be formed by conventional techniques...." Fang, [0020]. It would have been obvious that such conventional techniques are applicable to form Kim's etch-stop layer. Additionally, Fang's disclosed thickness range may be adjusted based on Kim's staircase structure. Fang's layer "may be formed over the stairs 125 at a thickness ranging from about 50 Å to about 1000 Å," or about 5 nm to 100 nm. *Id.*, [0021]. This etch-stop-layer thickness withstands etching of contact holes with depths "from about 1 μm to about 15 μm." *Id.*, [0030]. The height of Kim's staircase structure, and thus the approximate depth of its deepest contact hole, ranges from "about 10,000 Å to about 40,000 Å," or about 1 μm to about 4 μm. Kim, [0068]. Thus, a POSITA would have found it obvious that Fang's disclosed maximum thickness may be decreased proportionally to 26.7 nm (100 nm / 15 μm * 4 μm) to account for the shallower holes required for Kim's staircase structure when applying those teachings to specify Kim's etch-stop thickness. This thickness range of 5 to 26.7 nm overlaps with the claimed *range between 10 nm and 1000 nm*. Thus, Kim in view of Fang renders claim 10 obvious. Banerjee, ¶ 130.

To the extent the thickness of Fang’s etch-stop layer would need to be reduced to account for Kim’s extra etch-stop layer, *e.g.*, to maintain a total etch resistance, a POSITA would have found it obvious that the thickness would still overlap with the claimed *range between 10 nm and 1000 nm*. For example, a POSITA would have found it unnecessary to reduce the maximum range of 26.7 nm to below 10 nm (the reduction required to avoid any overlap with the claimed range) to account for one extra etch-stop layer. Banerjee ¶ 131. Thus, Kim in view of Fang renders obvious claim 7.

B. Claim 17:

1. [17] **“The semiconductor structure of claim 13, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.”**

The additional limitation of claim 17 is identical to that of claim 10. Kim in view of Fang renders it obvious for the same reason as explained above. §XI.A.1; Banerjee ¶ 132.

C. Motivation to Combine

A POSITA would have been motivated to apply Fang’s disclosure of the etch-stop-layer thickness on Kim’s staircase structure. Banerjee ¶ 133.

Kim focuses on resolving the difficulty of planarizing the interlayer dielectric to reduce the height difference between the cell-array region and the peripheral-circuit region. Kim, [0024]-[0025]. Accordingly, Kim does not detail certain aspects of the word-line contact region WCTR that were well-known in the art.

Fang, on the other hand, focuses on preventing over-etching shallower openings when etching openings for the word-line conductive structures. Fang, [0004], [0008]. A POSITA would have known that Fang's focus is an important consideration for manufacturing 3D memory devices and dovetails with Kim's focus to reduce or prevent damages to the device during manufacturing. Kim, [0027]. Further, a POSITA would have known that the thickness of an etch-stop layer is at least a necessary (but routine) design parameter and may be important to its purpose of preventing punch-through to underlying layers. Thus, a POSITA would have been motivated to adapt Kim's etch-stop layer in view of Fang's thickness range, since Kim does not specify a thickness. Banerjee ¶ 134.

A POSITA would have had a reasonable expectation of success in applying Fang's etch-stop-layer thickness to Kim because Fang's range (5-100 nm, or 5-26.7 nm adjusted) was reasonable. Banerjee ¶ 135. Further, a POSITA would have had a reasonable expectation of success because of similarities between Kim's and Fang's disclosures regarding the etch-stop layer. For example, Kim discloses that its "etch stop layer 125 may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130." Kim, [0213]. Fang discloses the same. Fang, [0020] ("The etch stop material 130 may also be substantially resistant to dry etch chemistries used to form openings 145 [through the insulating layer] (see FIG.

5).”). Kim discloses that its “second stop layer 125b may be formed of silicon nitride.” Kim, [0187]. So does Fang. Fang, [0020].

More generally, a POSITA would have had a reasonable expectation of success because both disclosures are directed to similar 3D memory devices with staircase word-line structures, *e.g.*, both comprising alternating conductive and dielectric layers at each step, an etch-stop layer and an insulating layer on the steps, and conductive structures penetrating various layers to form contacts with the conductive layers. Banerjee ¶¶ 136-37.

Were PO to argue against the combination by alleging Kim’s additional barrier layer somehow makes a difference to claims 10 and 17, PO would contradict the ’711 patent, which requires the same etch-stop-layer material and thickness for devices with or without the barrier layer. *Compare* Ex. 1001 claims 5, 10 *with* claims 16-17; Banerjee ¶ 138.

XII. GROUND 3: PARK IN VIEW OF A POSITA’S KNOWLEDGE

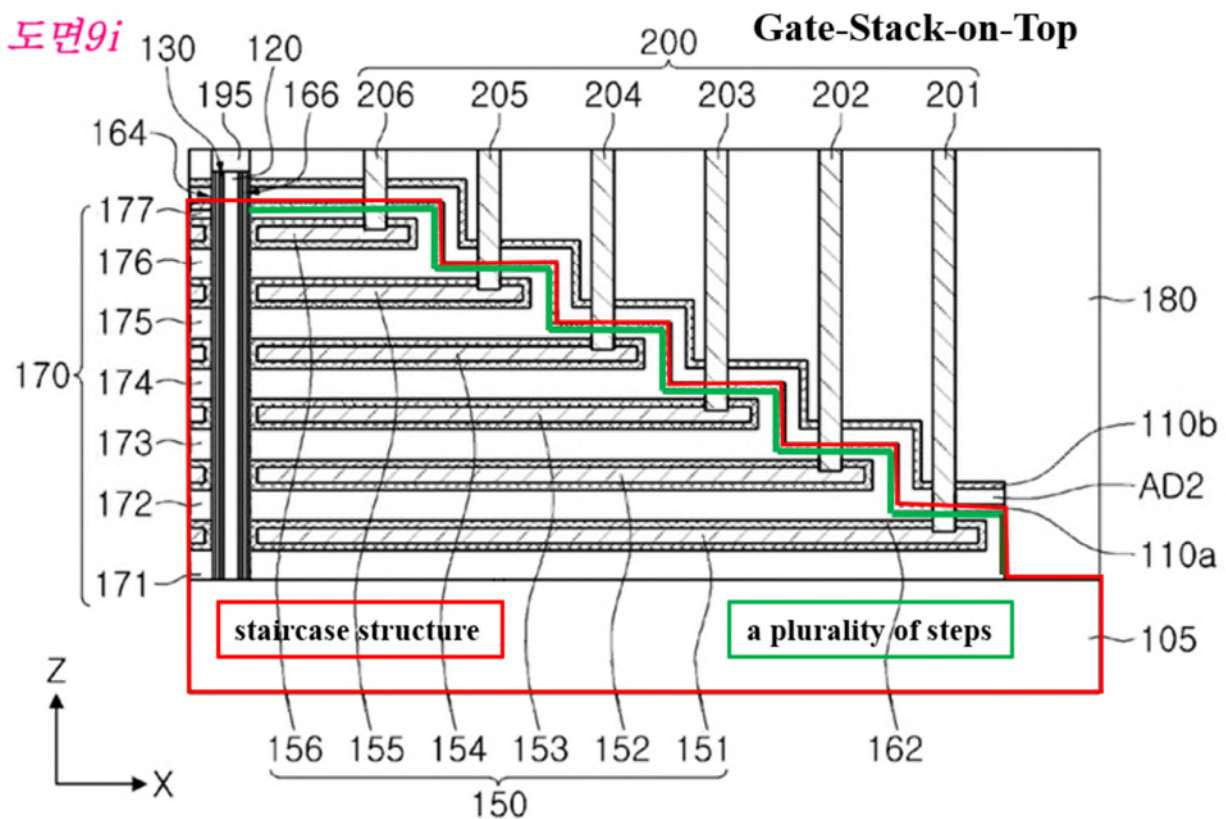
A. Park Discloses “a Gate Stack Disposed over a Dielectric Layer”

Park discloses a gate stack disposed over a dielectric layer even though its figures show the opposite order. §IX.B. In addition to Park’s express teaching, a POSITA would have known that either order was a common alternative. §X.A (citing Ex. 1008); Banerjee ¶ 139.

2. [1.A] “a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;”

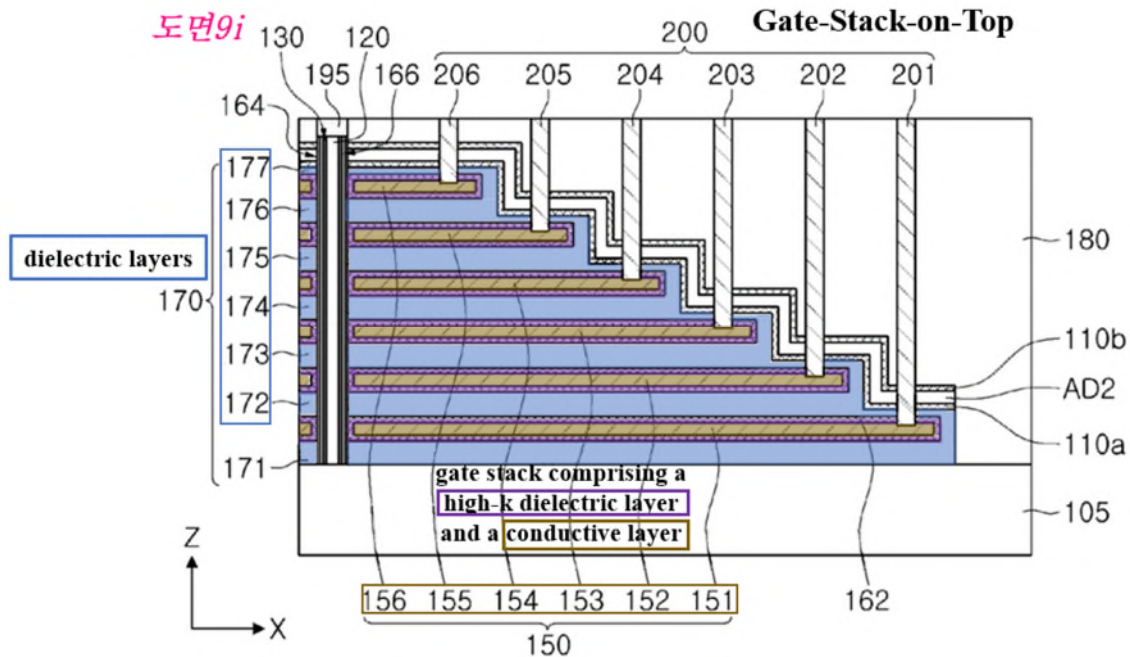
Park at least renders limitation [1.A] obvious.

Park’s nonvolatile memory comprises *a staircase structure comprising a plurality of steps*:



Park, Fig. 9i, [0102] (“Each of the plurality of insulating layers (170) and sacrificial layers (140) ... forms a step with respect to another insulating layers (170) and sacrificial layers (140).”); *id.*, Summary, [0004], [0036], [0042], [0081]; Banerjee ¶¶ 142-43.

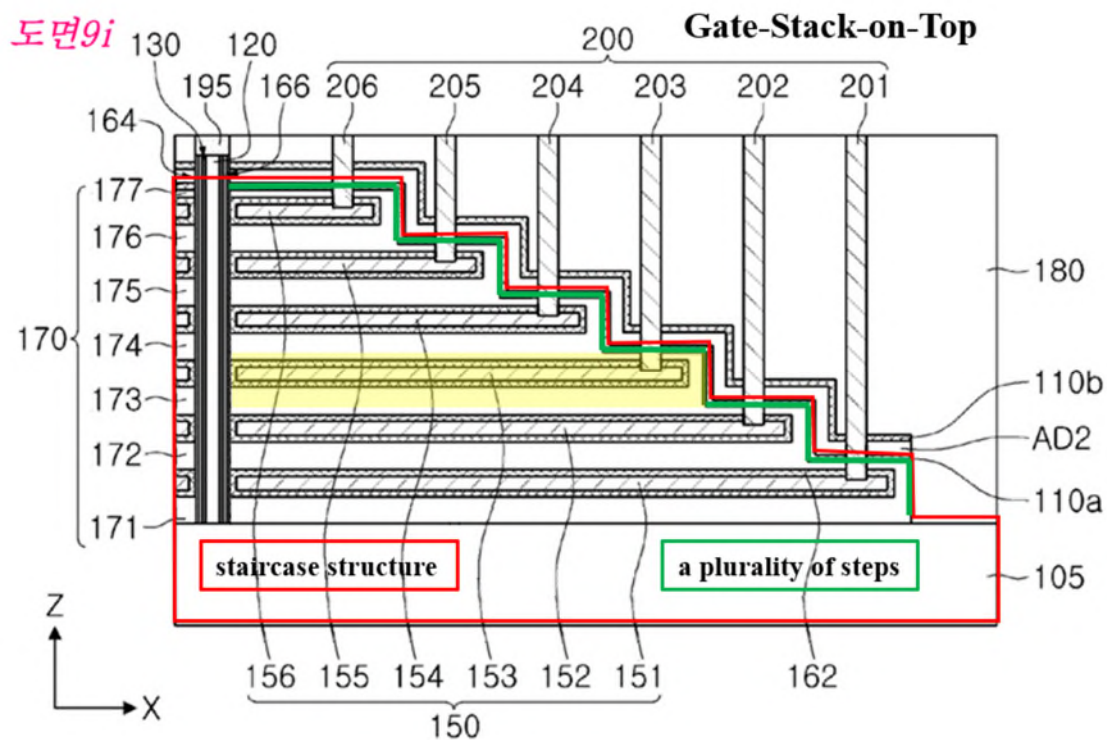
Park discloses that *each step comprises a gate stack disposed over a dielectric layer* (one of “insulating layers” 172-177). Further, *the gate stack compris[es] a high-k dielectric layer* (“blocking layer” 162) *and a conductive layer* (one of “gate electrode layers” 151-156):



Park, Fig. 9i, [0007] (“An insulating layer disposed between the plurality of gate electrode layers; and at least a portion of the plurality of gate insulating films may extend along the one direction to be disposed between the plurality of gate electrode layers and the insulating layer.”), [0033]; [0040]-[0041] (“the blocking layer (162) is disposed to surround the gate electrode layer (150).”). “[E]lectrically conductive materials forming the gate electrode layer (150).” *Id.*, [0106]. “The gate electrode layer (154) is surrounded by a blocking layer (162).” *Id.*, [0060]. “The blocking

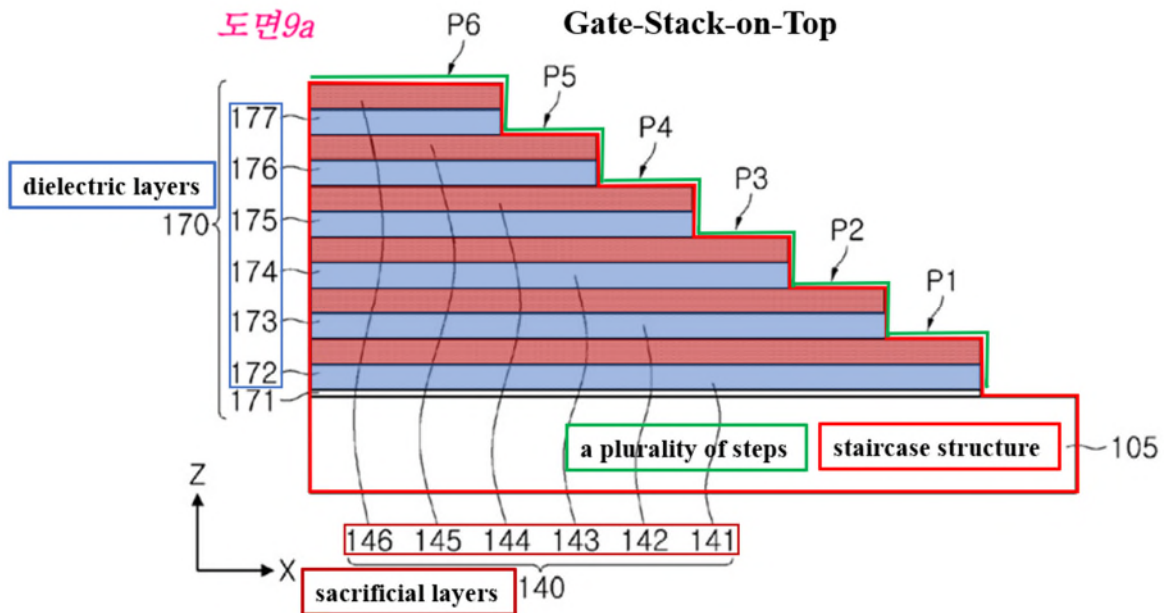
layer (162) may comprise ... a high-k dielectric material.” *Id.*, [0063]; Banerjee ¶ 144.

Were PO to argue that Park does not meet the “plurality of steps” limitation because its steps do not comprise a gate stack and a dielectric layer of the same width, PO would be wrong. First, nothing in the claim language requires that the gate stack and dielectric layer be the same width. Even assuming Park shows gate stack and dielectric layers of different widths, it still forms a staircase: it is obvious which gate stack and dielectric layer are paired to form a step (one shaded below):



Park, Fig. 9i. This ordinary understanding of “step” is consistent with the ’711 patent, which does not define a “step” to require two layers of the same length. See *generally* Ex. 1001; Banerjee ¶ 145.

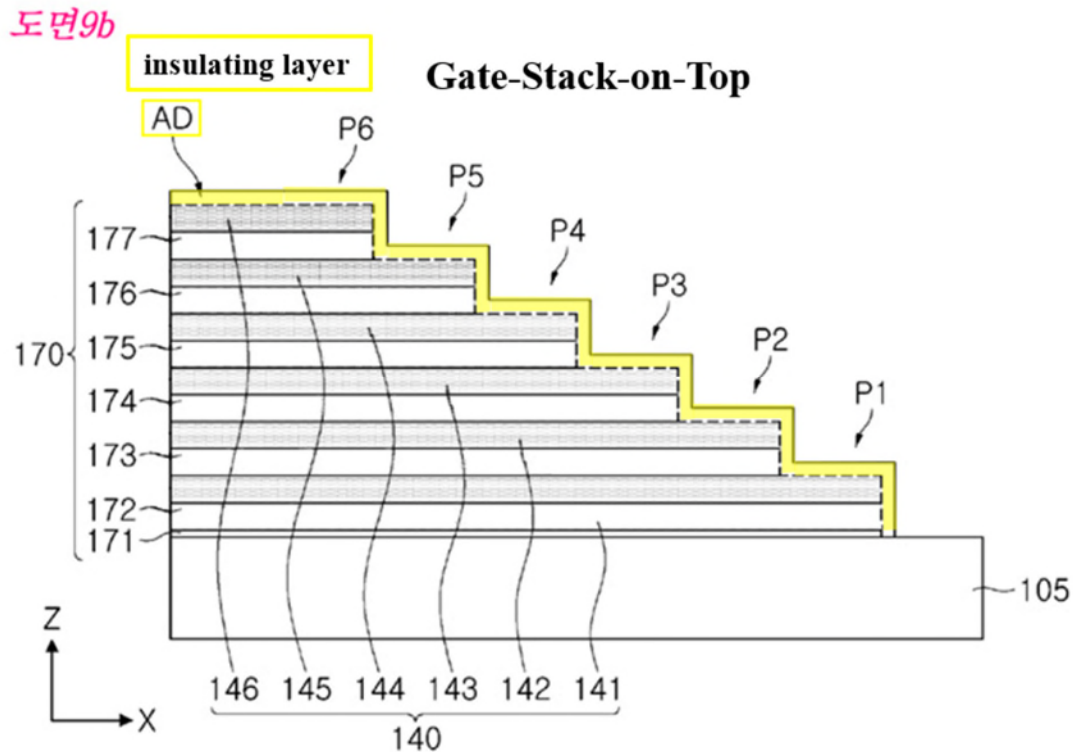
Regardless, Park plainly describes gate stacks and dielectric layers of the same width. The '711 patent explains that each step, including its lateral dimension, is configured by one cycle of an etch-and-trim process. Ex. 1001, 6:53-67, 7:13-22, 12:3-10. That matches exactly Park's process of forming the staircase structure:



Park, Fig. 9a, [0102]. As shown, each respective pair of dielectric layers 172-177 and sacrificial layers 141-146 has the same width after the etch-and-trim process, consistent with “step” of the '711 patent. Each sacrificial layer is subsequently replaced with a gate stack. *Id.*, Figs. 9f-9g, [0104]-[0105]; Banerjee ¶ 146.

That Park may deposit additional insulation (layer AD) onto the staircase, and thereby laterally extend the dielectric material, is irrelevant, because this limitation is a *comprising* limitation. That dielectric material may be added to the steps doesn't

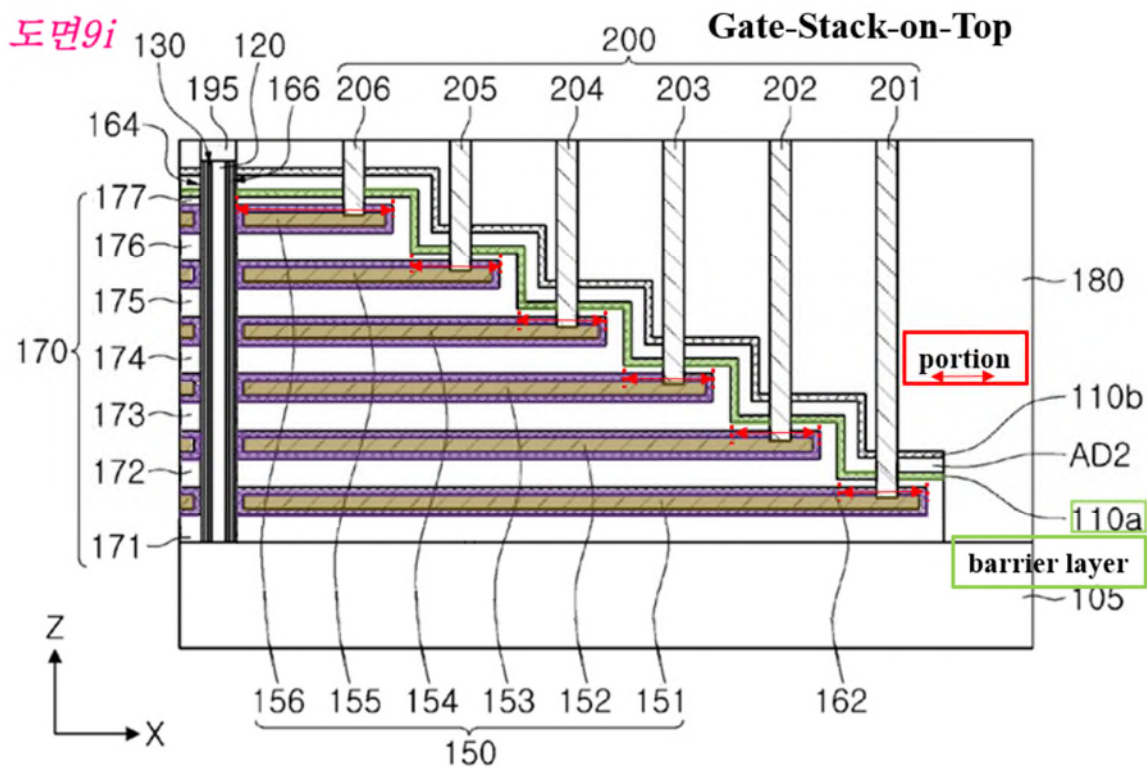
change the fact that the gate stacks and dielectric layers had the same width before layer AD was deposited.



Park, Fig. 9b, [0103]. Of course, nothing in Park says that layer AD must be deposited. To the contrary, Park explains that layer AD is optional. *Id.*, [0103] (“When multiple pad regions (P1-P6) are in place, an insulating layer (AD) *can* be further formed on the pad region (P1-P6).”) (emphasis added). By omitting this optional insulating layer, each step would comprise a gate stack and a dielectric layer of the same width (which, again, is not a claim requirement). Banerjee ¶ 147.

3. [1.B] “a barrier layer disposed over a portion of the gate stack of the each step;”

Park at least renders obvious *a barrier layer* (“etch-stop layer” 110a) *disposed over a portion of the gate stack of the each step*:



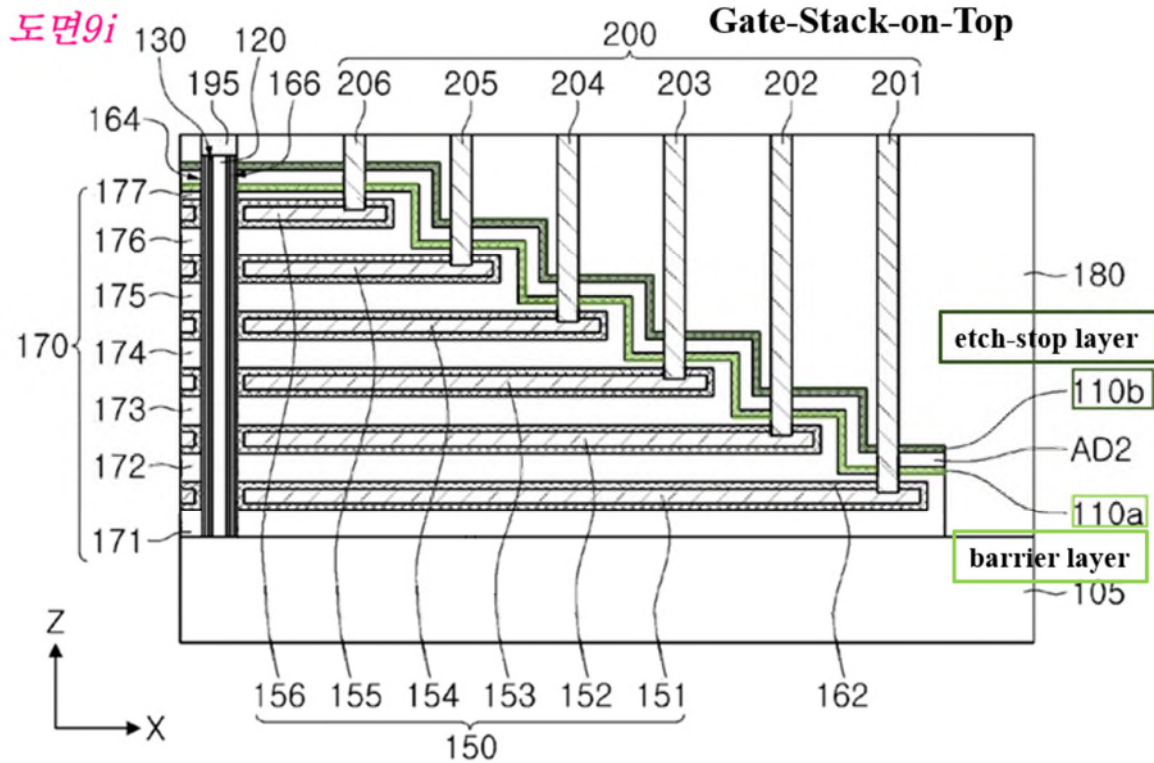
Park, Fig. 9i, [0049]. Specifically, “one or more etch-stop layers (110) may be formed on the gate electrode (150) in a plurality of pad regions.” *Id.*, [0046]; §VI (explaining that a barrier layer is another etch-stop layer). Like the barrier layer of the '711 patent, Park’s etch-stop layer 110a may comprise silicon oxide, silicon oxynitride, silicon nitride, or aluminum oxide. Ex. 1001, 7:50-52, 6:20-24 (disclosing that barrier layer may comprise the same material as the dielectric layer, which in turn may comprise one of the aforementioned materials); Park, [0124],

[0041], [0063] (disclosing that etch-stop layer 110a may comprise the same material as the blocking layer, which in turn may comprise silicon oxide, silicon nitride, silicon oxynitride, or a high-k dielectric material, including aluminum oxide). The etch-stop layer 110a “temporarily stop[s] or slow[s] down” the etching of vertical openings, “thereby preventing defects caused by penetration of the top gate electrode layer....” *Id.*, [0051]. Thus, etch-stop layer 110a functions as a barrier layer. Ex. 1001, 7:36-39. The *portion[s]* over which the barrier layer are disposed are pad regions P1-P6. Park, Figs. 9b-9c, [0046]; Banerjee ¶ 148.

The '711 patent discloses that “‘over’ something” includes directly on that something. Ex. 1001, 4:6-10. Thus, this limitation is met when the gate stack is above the dielectric layer. §X.B.3; Banerjee ¶ 149.

4. [1.C] “an etch-stop layer disposed on the barrier layer;”

Park discloses *an etch-stop layer* (“etch-stop layer” 110b) *disposed on the barrier layer* (etch-stop layer 110a):

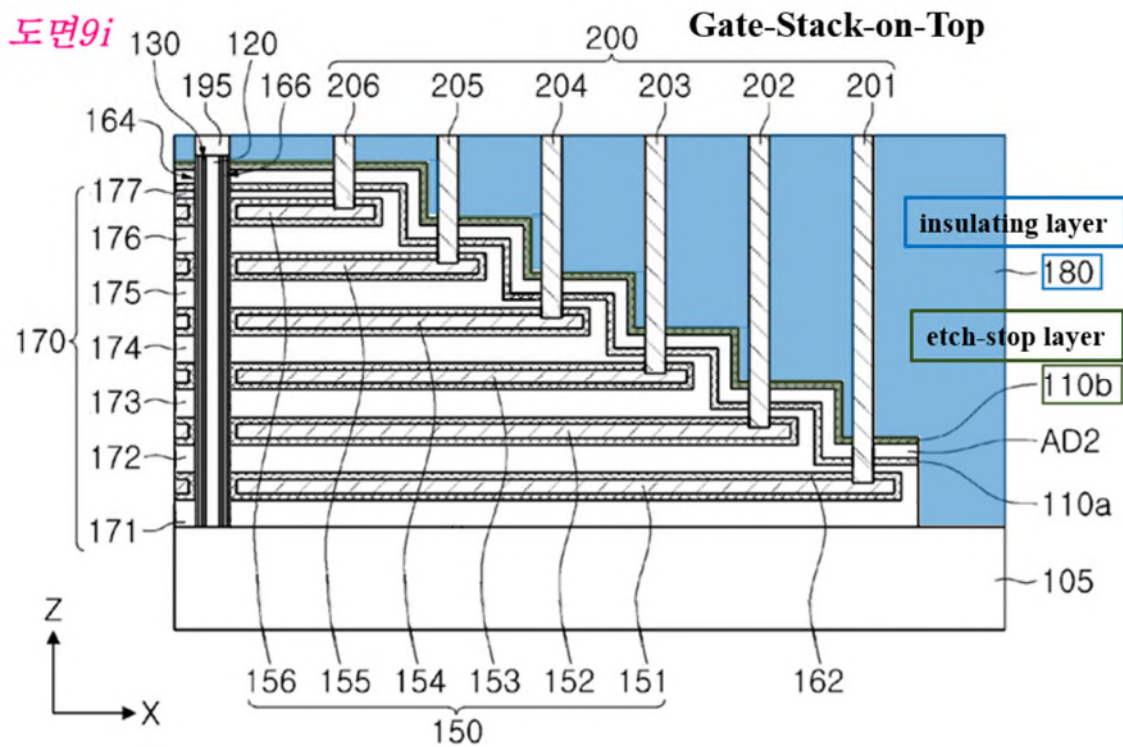


Park, Fig. 9i, [0049]. Like layer 110a, the etch-stop layer 110b “temporarily stop[s] or slow[s] down” the etching of vertical openings, “thereby preventing defects caused by penetration of the top gate electrode layer....” *Id.*, [0051]. That performs the function of an etch-stop layer of the ’711 patent. Ex. 1001, 5:61-63; Banerjee ¶ 150.

The ’711 patent discloses that X “on” Y means X is directly or indirectly on Y, *i.e.*, “an intermediate ... layer” may exist between X and Y. Ex. 1001, 4:1-6. Thus, this limitation is met even though an intermediate layer AD2 exists between etch-stop layers 110a and 110b. Banerjee ¶ 151.

5. [1.D] “an insulating layer disposed on the etch-stop layer;
and”

Park discloses *an insulating layer* (“connection region insulating layer” 180)
disposed on the etch-stop layer (“etch-stop layer” 110b):

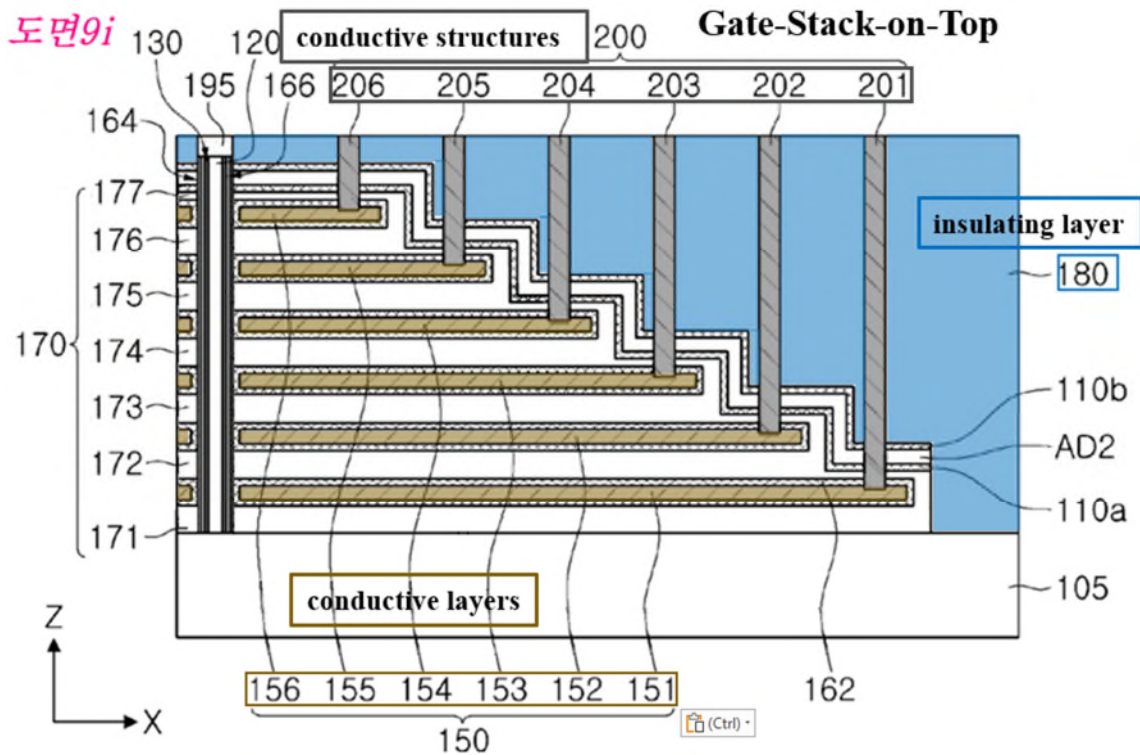


Park, Fig. 9i, [0103] (“a connection region insulation layer (180) can be applied onto the second etch-stop sacrificial layer (115b)...”); Banerjee ¶ 152.

6. [1.E] “a plurality of conductive structures formed in the
insulating layer, wherein each conductive structure is
formed on the conductive layer of the each step.”

Park discloses *a plurality of conductive structures* (“contact plugs” 201-206)
formed in the insulating layer (“connection region insulating layer” 180), *wherein*
each conductive structure (one of “contact plugs” 201-206) *is formed on the*

conductive layer (corresponding one of “gate electrode layers” 151-156) *of the each step*:



Park, Fig. 9i, [0050], [0108]-[0110] (describing an etching process “to prepare a plurality of vertical openings,” which are then “filled with an electrically conductive material” to form contact plugs “electrically connect[ed] [to] ... gate electrode layers....”); *id.*, [0043], [0045], [0049].

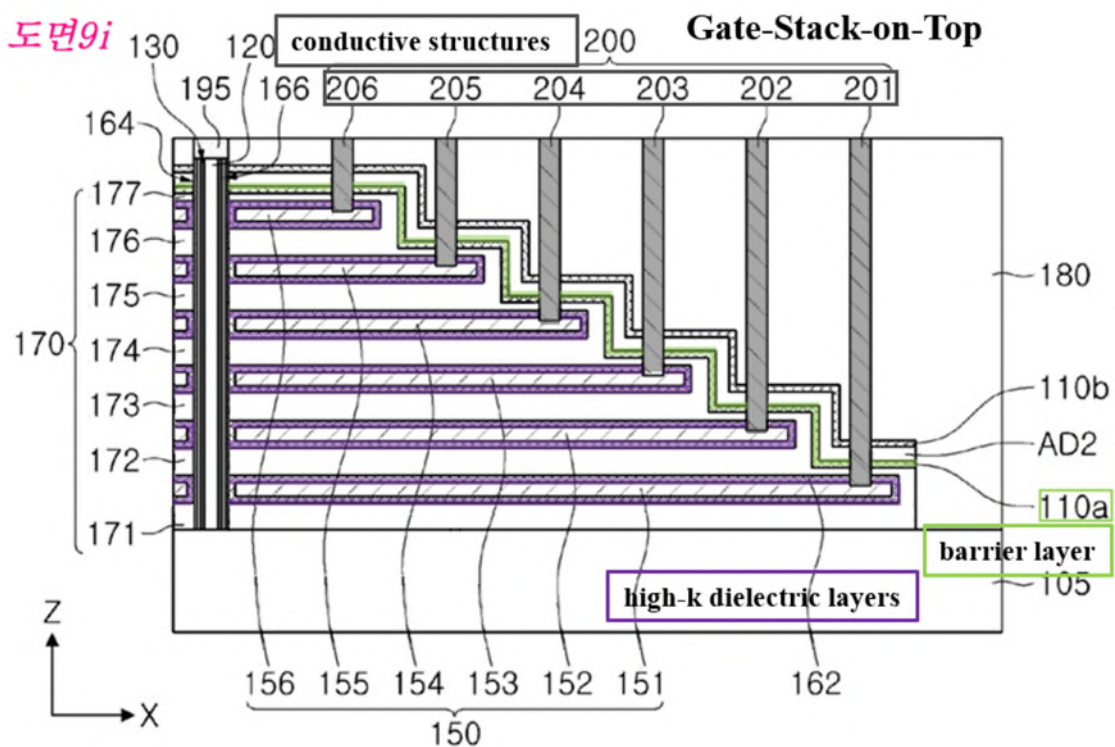
For the same reason explained in Ground 1, when the gate stack is disposed over the dielectric layer at each step, *each conductive structure* (“contact plugs” 201-206) is still *formed on the conductive layer* (corresponding one of “gate electrode layers” 151-156). §§X.A, X.B.6 (a POSITA’s knowledge); Park, [0110] (disclosing

electrical connection between gate electrodes and connecting lines through contact plugs); Banerjee ¶¶ 153-54.

C. Claim 2:

1. [2] “The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the barrier layer and the high-k dielectric layer.”

Park at least renders obvious that *the plurality of conductive structures* (“contact plugs” 201-206) *extend[s] through the barrier layer* (“etch-stop layer” 110a) *and the high-k dielectric layer* (“blocking layer” 162):



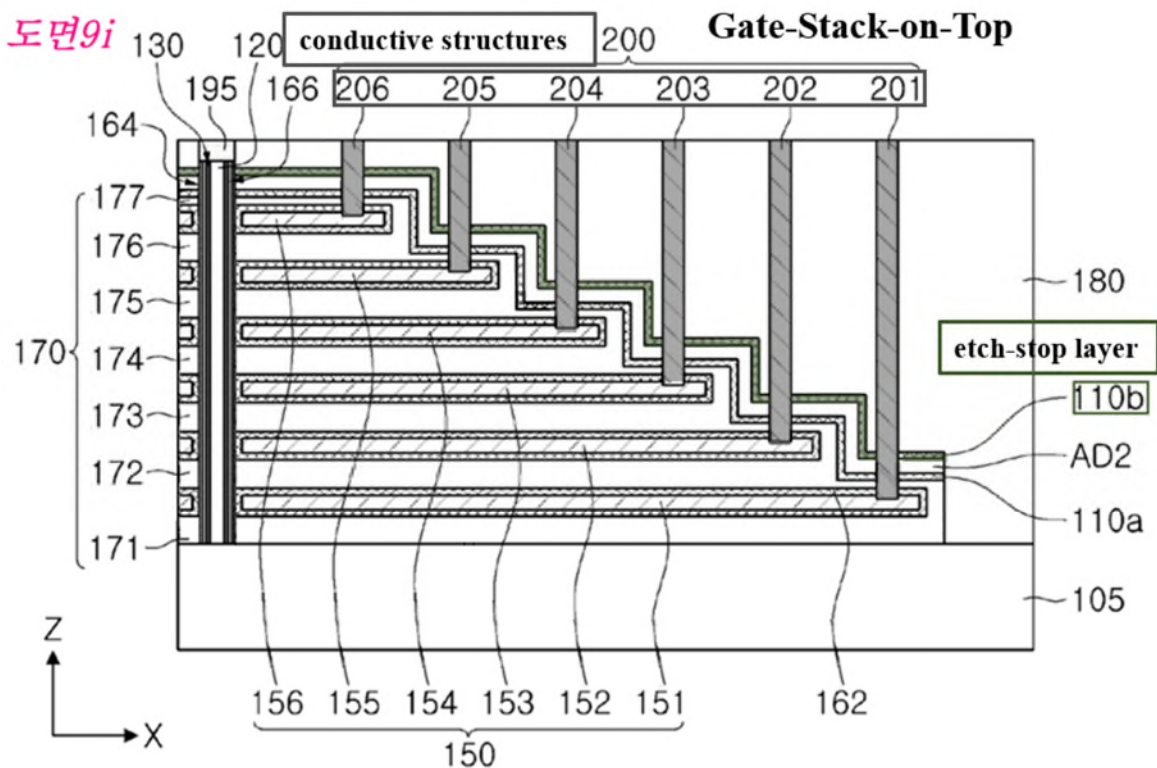
Park, Fig. 9i, [0049]-[0050] (“a vertical opening in which a contact plug (206) is formed in connection with a gate electrode layer (156)...”), [0110]; *id.*, [0056], [0125].

“[T]he plurality of connecting lines (220) must be electrically connected with the plurality of gate electrode layers (150) through the plurality of contact plugs (200).” *Id.*, [0110]. Thus, the contact plug must extend through the etch-stop layer 110a and the blocking layer to reach the gate electrode in the gate-stack-on-top configuration. Banerjee ¶¶ 155-56.

D. Claim 3:

1. [3] “The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the etch-stop layer.”

Park discloses that *the plurality of conductive structures* (“contact plugs” 201-206) *extend[s] through etch-stop layer* (“etch-stop layer” 110b):



Park, Fig. 9i, [0049]-[0050], [0110]; *id.*, [0056], [0125]. For the same reason that the conductive structures must penetrate through the barrier layer and the high-k dielectric layer, they must also penetrate through the etch-stop layer. §XII.C.1; Banerjee ¶ 157.

E. Claim 4:

1. [4] “The semiconductor structure of claim 1, wherein the barrier layer comprises silicon oxide.”

Park discloses that *the barrier layer* (“etch-stop layer” 110a) *comprises silicon oxide*. Specifically, Park discloses that the blocking layer 162 may comprise silicon oxide, and that etch-stop layer 110a may comprise an identical material. Park, [0063], [0105]; Banerjee ¶ 158.

F. Claim 5:

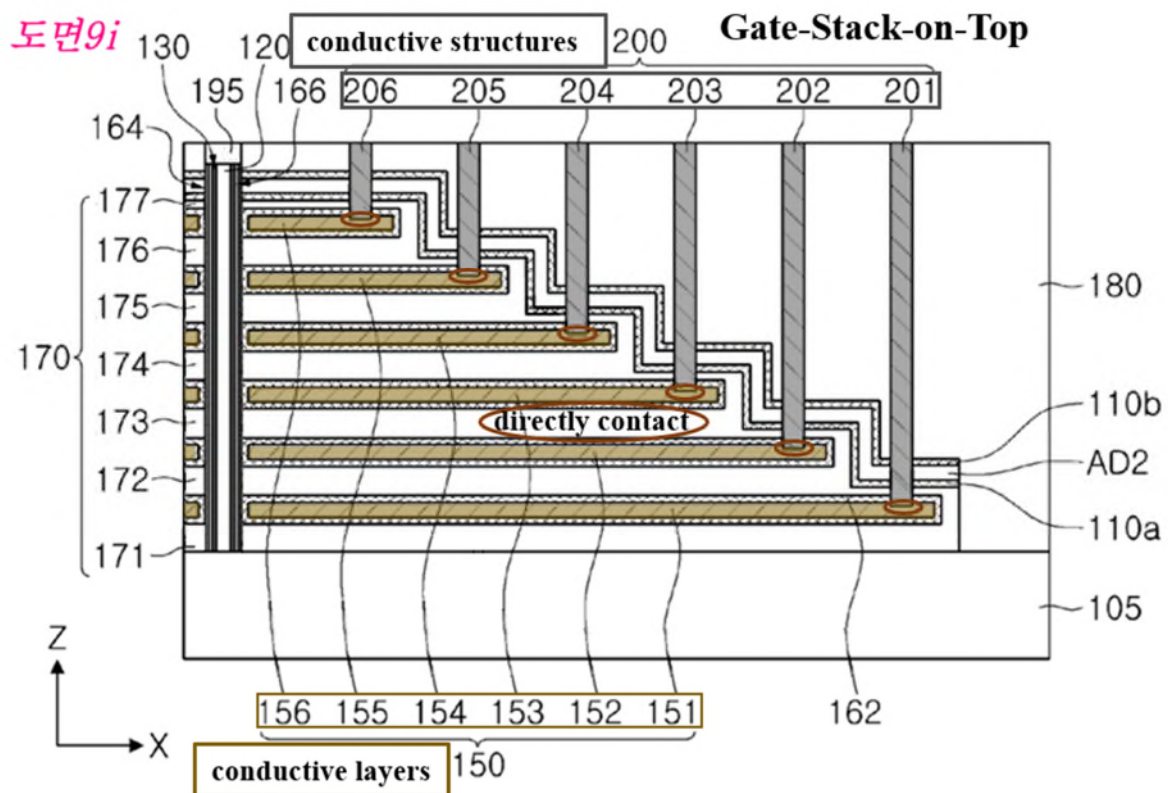
1. [5] “The semiconductor structure of claim 1, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.”

Park discloses that *the etch-stop layer* (“etch-stop layer” 110b) *comprises one or more of silicon nitride ... and a high-k dielectric*. Specifically, Park discloses that the blocking layer 162 may comprise silicon nitride (Si₃N₄) or a high-k dielectric, and that etch-stop layer 110b may comprise an identical material. Park, [0063], [0105]; Banerjee ¶ 159.

G. Claim 6:

1. [6] “The semiconductor structure of claim 1, wherein the each conductive structure directly contacts a corresponding one of the conductive layer of the each step.”

Park at least renders obvious that *the each conductive structure* (one of “contact plugs” 201-206) *directly contacts a corresponding one of the conductive layer* (corresponding one of “gate electrode layers” 151-156) *of the each step*:



Park, Fig. 9i, [0049]-[0050], [0110].

The direct contacts between contact plugs and gate electrode layers establish the required electrical connections. *Id.*, [0110]; §§XII.B.6, XII.C.1 (electrical-connection requirement); Banerjee ¶¶ 160-61.

H. Claim 8:

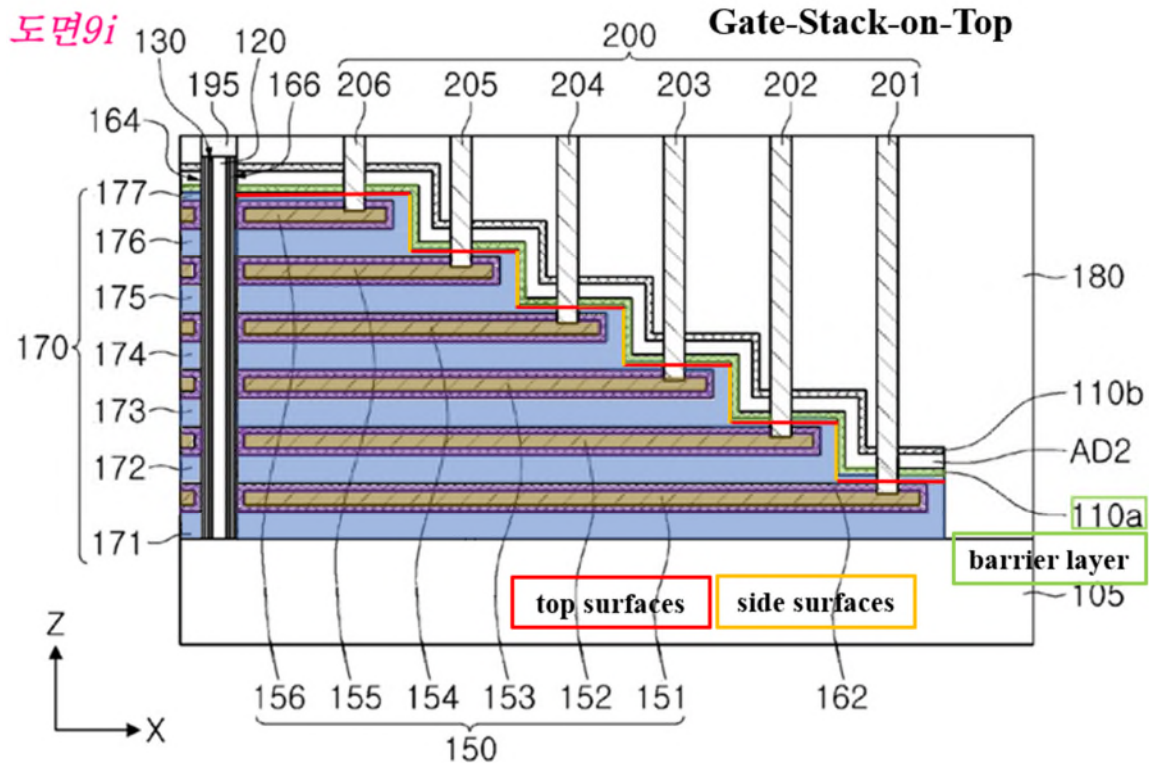
1. [8] “The semiconductor structure of claim 1, wherein the plurality of conductive structures comprise one or more of tungsten, cobalt, nickel, copper, and aluminum.”

Park discloses that *the plurality of conductive structures* (“contact plugs” 201-206) *comprise[s] ... tungsten*. Park, [0110] (“the plurality of vertical openings (210) may be filled with an electrically conductive material - for example tungsten (W) - to form a contact plug (201-206: 200).”); *id.*, [0099]; Banerjee ¶ 162.

I. Claim 9:

1. [9] “The semiconductor structure of claim 1, wherein the barrier layer is formed on side and top surfaces of the plurality of steps.”

Park discloses that *the barrier layer* (“etch-stop layer” 110a) *is formed on side and top surfaces of the plurality of steps*:



Park, Fig. 9i, [0049] (“a plurality of etch-stop layers (110a, 110b) is provided having a shape corresponding to a step arranged in the connection region (D).”); Banerjee ¶ 163.

J. Claim 11:

1. [11] “The semiconductor structure of claim 1, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.”

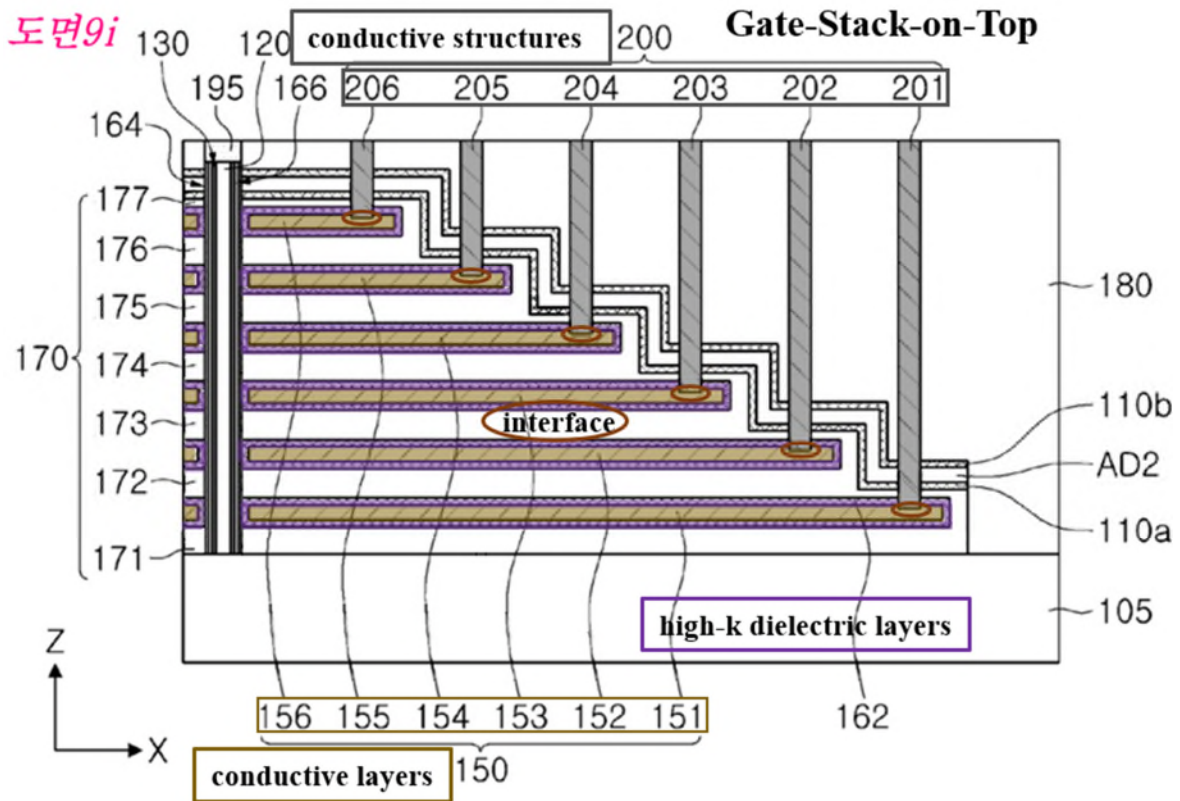
Park discloses that *the high-k dielectric layer* (“blocking layer” 162) *comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, [or] lanthanum oxide....* Specifically, Park discloses that the blocking layer 162 may comprise a high-k dielectric, and that “[t]he high-k dielectric material may be any

one of aluminum oxide (Al_2O_3), tantalum oxide (Ta_2O_3), ... zirconium oxide (ZrO_2), ... hafnium oxide (HfO_2), ... lanthanum oxide (La_2O_3)....” Park, [0063]; Banerjee ¶ 164.

K. Claim 12:

1. [12] “The semiconductor structure of claim 1, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.”

Park at least renders obvious that *top and bottom surfaces and a sidewall of the conductive layer* (one of “gate electrode layers” 151-156) *are covered by the high-k dielectric layer* (“blocking layer” 162), *except at an interface between the conductive layer and the conductive structure* (corresponding one of “contact plugs” 201-206):



Park, Fig. 9i, [0060] (“The gate electrode layer (154) is surrounded by a blocking layer (162).”); [0105] (“a gate electrode layer (150) may be formed ... within the block layer (162).”); *id.*, [0041]; §XII.C.1 (electrical-connection requirement); Banerjee ¶ 165.

For the reason explained in Ground 1 (§X.L.1), a POSITA would have found it obvious that the layer ordering would not change the spatial relationship of gate electrodes and blocking insulating layer. Banerjee ¶ 166; Park, [0110].

Were PO to argue that Park does not meet claim 12 because its high-k dielectric layer covers both sidewalls of the conductive layer, PO would be wrong. First, claim 12 is a comprising claim and is silent on the configuration at the second

sidewall. “The claim[] contain[s] no language requiring or even suggesting” that the conductive layer must *not* be covered by the high-k dielectric layer at the second sidewall. *Provisur Techs., Inc. v. Weber, Inc.*, No. 2021-1851, 2022 WL 17688071, at *3 (Fed. Cir. Dec. 15, 2022); Banerjee ¶ 167. Second, the ’711 patent discloses a sidewall isolation barrier layer, *e.g.*, insulating layer 530, covering the conductive layer at the second sidewall. Ex. 1001, 9:41-44, 12:42-48. Park’s high-k dielectric layer at the second sidewall amounts to such an isolation barrier layer. Banerjee ¶ 167. For example, the insulating layer 530 of the ’711 patent may comprise the same material as the etch-stop layer 310, which can be made of high-k dielectric films. Ex. 1001, 9:46-48, 8:10-14. That is the same material from which Park’s block layer 162 may be made. Park, [0063].

L. Claim 13:

1. [13.PRE] “A semiconductor structure, comprising:”

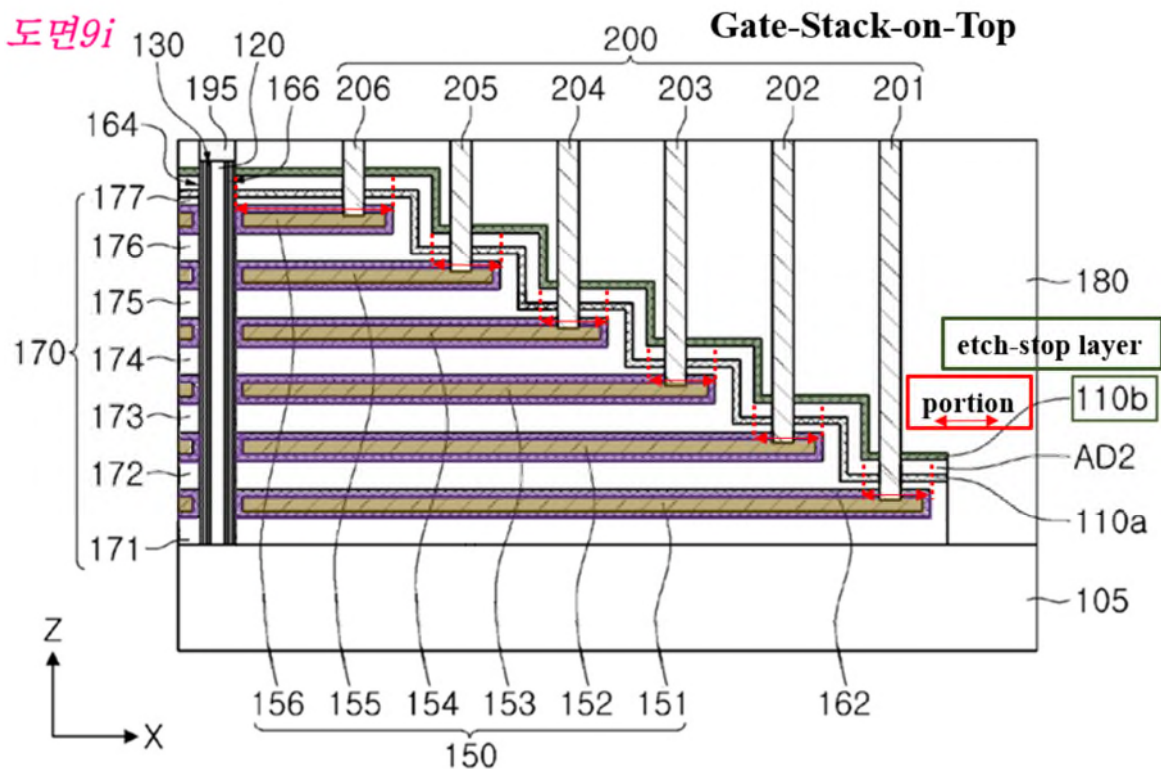
This preamble is identical to that of claim 1. Park discloses it for the same reason as explained above. §XII.B.1; Banerjee ¶ 168.

2. [13.A] “a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;”

This limitation is identical to [1.A]. Park at least renders it obvious for the same reason as explained above. §XII.B.2; Banerjee ¶ 169.

3. [13.B] “an etch-stop layer disposed on a portion of the gate stack of the each step;”

Park discloses *an etch-stop layer* (“etch-stop layer” 110b) *disposed on a portion of the gate stack* (one of “gate electrode layers” 151-156 and “blocking layer” 162) *of the each step*:



Park, Fig. 9i, [0049] (“a plurality of etch-stop layers (110a, 110b) is provided having a shape corresponding to a step”); §XII.B.3 (same but for the barrier layer).

Park satisfies limitation [13.B] even though intermediate layers exist between the etch-stop layer 110b and the gate stack. Ex. 1001, 4:1-6 (disclosing that “on” something includes both direct and indirectly on that something); Banerjee ¶¶ 170-71.

4. **[13.C] “an insulating layer disposed on the etch-stop layer; and”**

This limitation is identical to [1.D]. Park discloses it for the same reason as explained above. §XII.B.5; Banerjee ¶ 172.

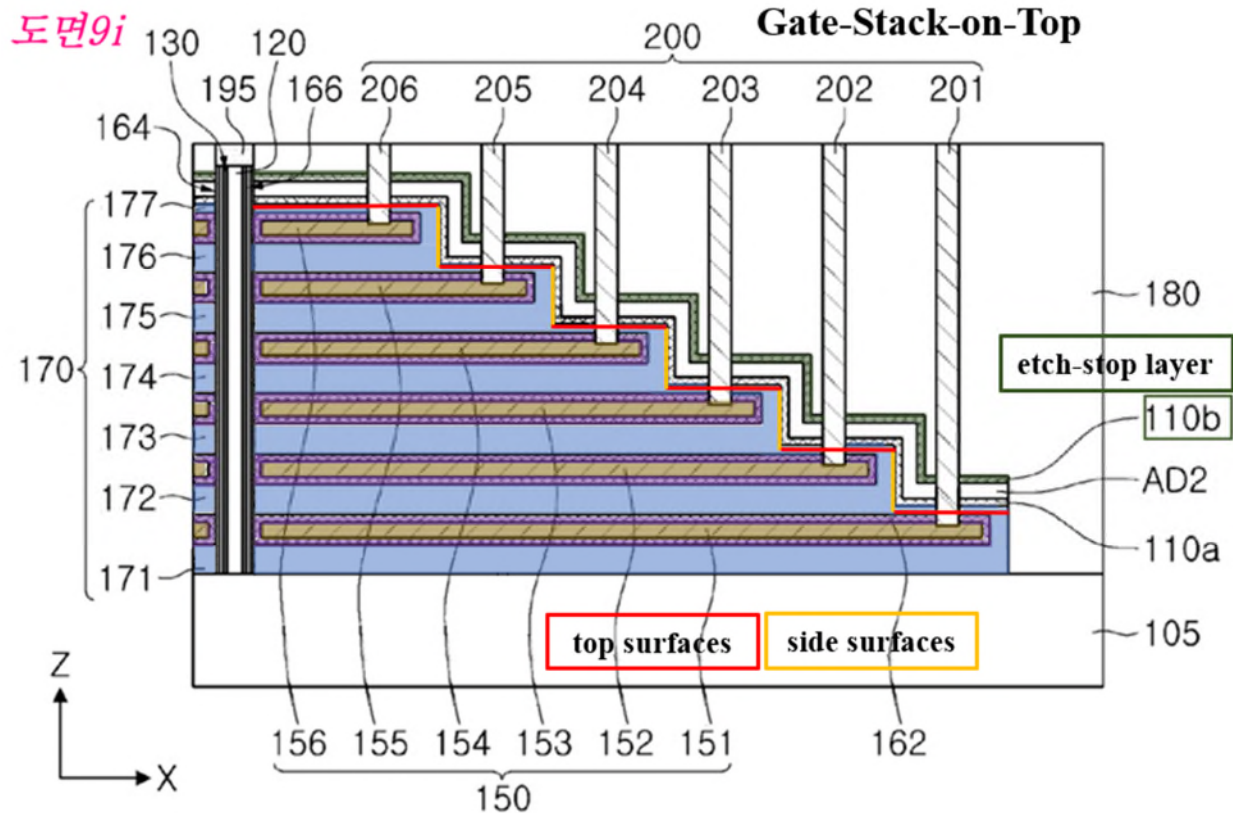
5. **[13.D] “a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer and the high-k dielectric layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.”**

This limitation combines the requirements of limitation [1.E] and claims 2, 3, and 6. Park at least renders it obvious for the same reason as explained above. §§XII.B.6, XII.C.1, XII.D.1, XII.G.1; Banerjee ¶ 173.

M. Claim 14:

1. **[14] “The semiconductor structure of claim 13, wherein the etch-stop layer is formed on a side surface and a top surface of each step.”**

Park discloses that *the etch-stop layer* (“etch-stop layer” 110b) *is formed on a side surface and a top surface of each step:*



Park, Fig. 9i, [0049] (“a plurality of etch-stop layers (110a, 110b) is provided having a shape corresponding to a step”), [0008]; *id.*, [0124]; Ex. 1001, 4:1-6 (disclosing that “on” something includes both directly and indirectly on that something); §XII.I.1 (virtually the same but for the barrier layer); Banerjee ¶ 174.

N. Claim 15:

1. [15] “The semiconductor structure of claim 14, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.”

Park at least renders obvious claim 15.

Park repeatedly refers to “*the* thickness of the etch-stop layer.” Park, [0006], [0060], [0067], [0070]-[0071]. A POSITA would have understood these references

to mean that the etch-stop layer has a single thickness. Thus, *thicknesses of the etch-stop layer* (“etch-stop layer” 110b) *is the same on the side and top surfaces of each step*. Banerjee ¶¶ 175-176.

This understanding of Park would have been supported by a POSITA’s knowledge. For example, it was known that an etch-stop layer of uniform thickness on all steps was desirable to achieve a uniform contact-hole depth below the etch-stop layer. Ex. 1017, [0042]. This prevents or reduces over-etching or under-etching. Banerjee ¶ 177.

O. Claim 16:

1. **[16] “The semiconductor structure of claim 13, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.”**

The additional limitation of claim 16 is identical to that of claim 5. Park discloses it for the same reason as explained above. §XII.F.1; Banerjee ¶ 178.

P. Claim 18:

1. **[18] “The semiconductor structure of claim 13, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.”**

The additional limitation of claim 18 is identical to that of claim 11. Park discloses it for the same reason as explained above. §XII.J.1; Banerjee ¶ 179.

Q. Claim 19:

1. **[19] “The semiconductor structure of claim 13, wherein top and bottom surfaces and a sidewall of the conductive layer**

are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.”

The additional limitation of claim 19 is identical to that of claim 12. Park discloses it for the same reason as explained above. §XII.K.1; Banerjee ¶ 180.

XIII. GROUND 4: PARK IN VIEW OF FANG

A. Claim 7:

- 1. [7] “The semiconductor structure of claim 1, wherein top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.”**

Park at least renders obvious claim 1. §XII.B. Park in view of Fang renders obvious claim 7. Banerjee ¶ 181.

Fang discloses that *top surfaces of the plurality of conductive structures* (“contacts” 155a-155d), *the insulating layer* (“another oxide material” 135), *and a portion of the etch-stop layer* (“etch stop material” 130) *are coplanar*:

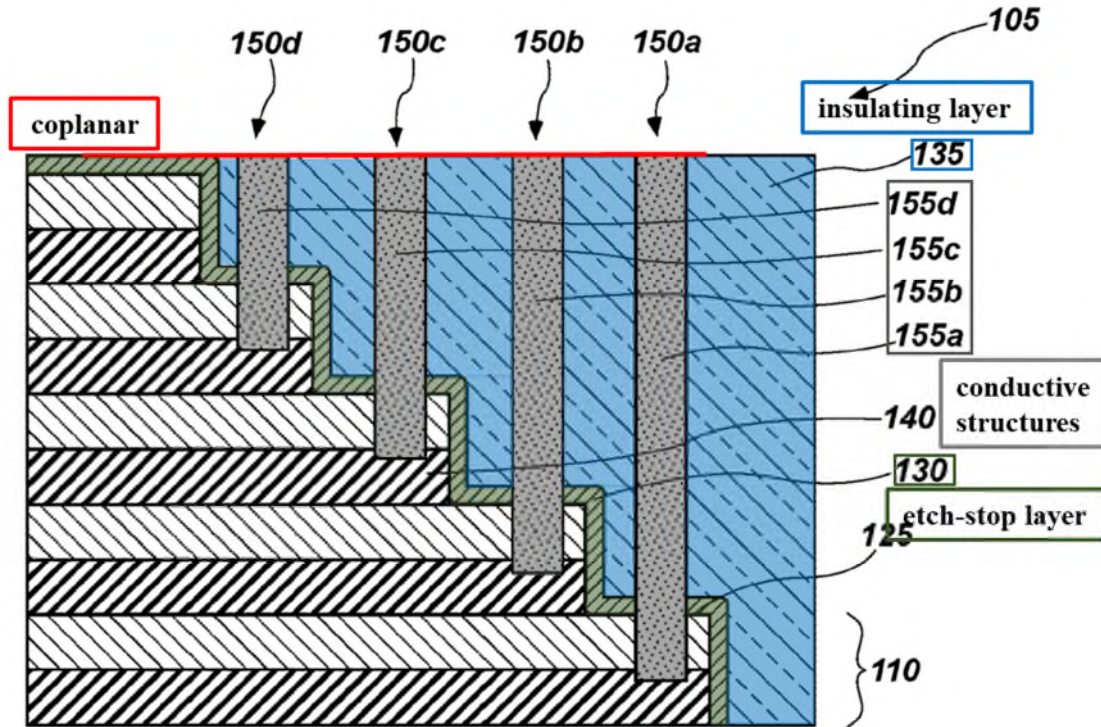
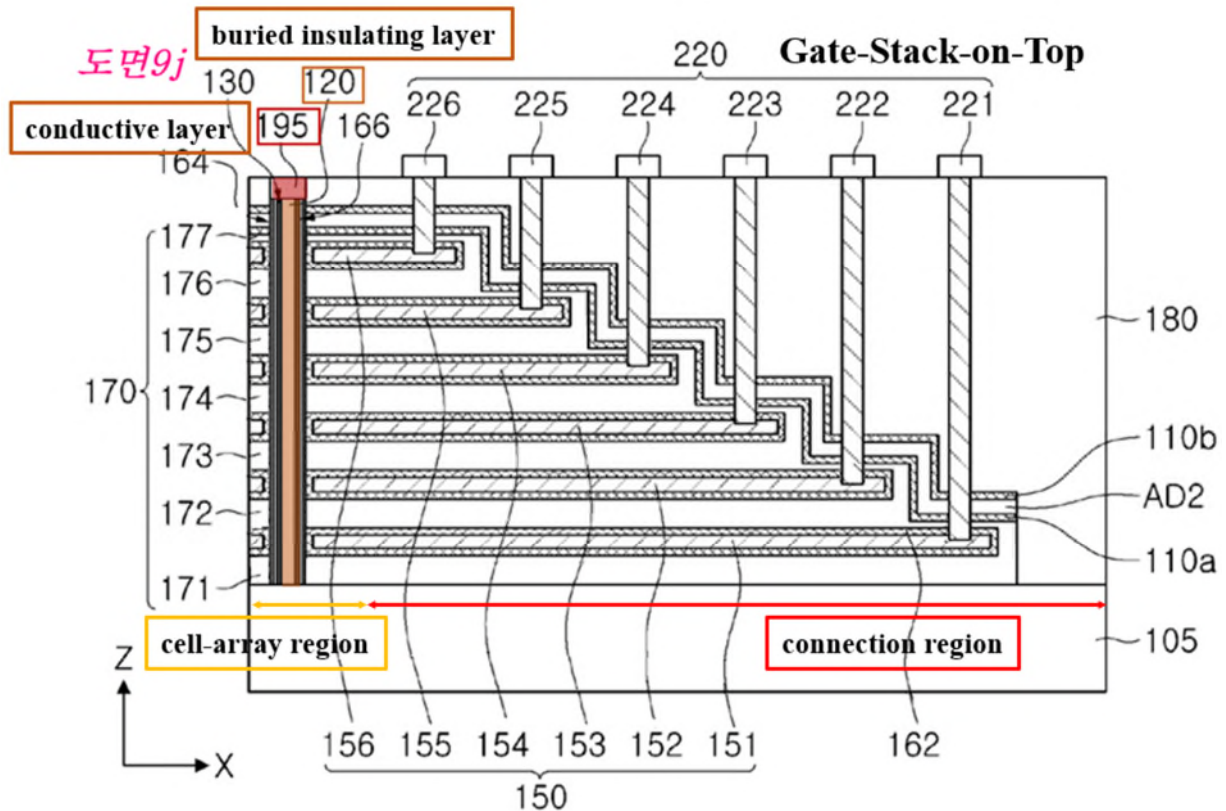


FIG. 6

Fang, Fig. 6, [0024]. This is achieved through a planarization process. *Id.*, [0024]; Banerjee ¶ 182.

Park also discloses planarizing the connection region insulating layer 180 to equalize the heights of the cell-array region C, where the channel is located, and the connection region D, where the staircase structure is located. Park, [0084].

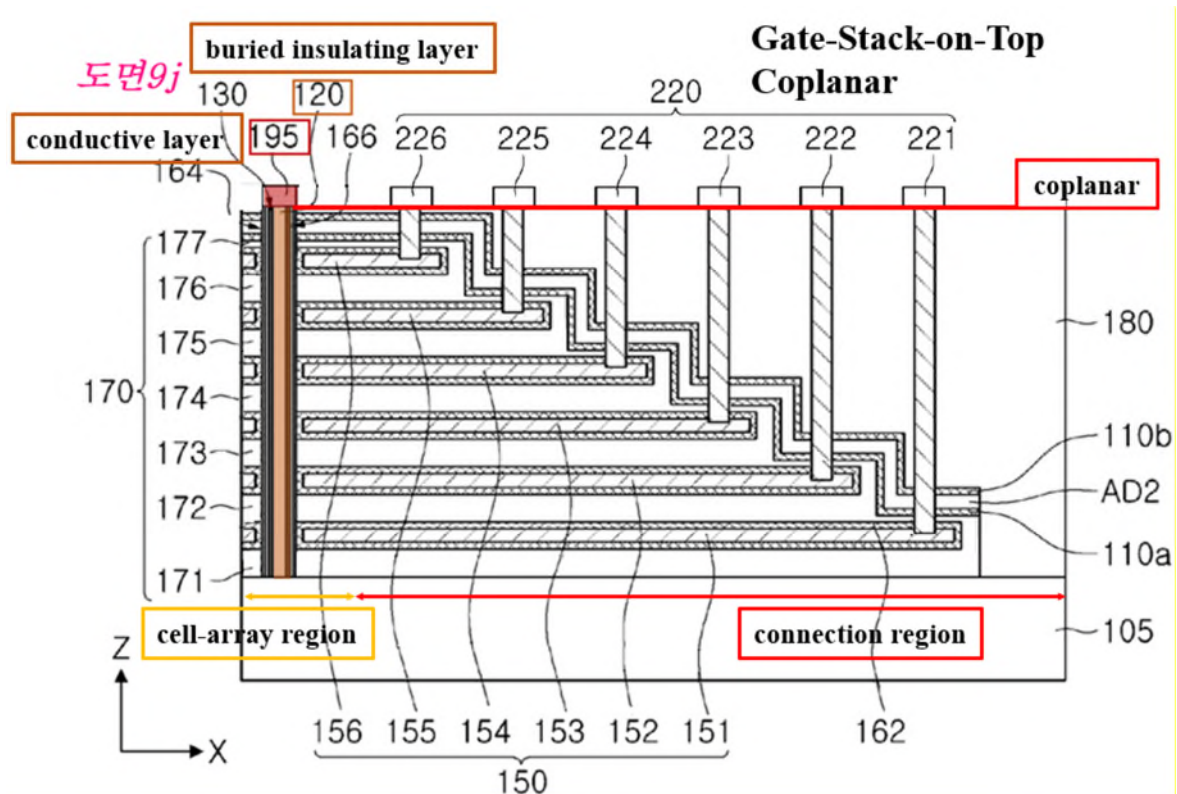


Id., Fig. 9j, [0089]. As shown, the top surfaces of Park's insulation layer and conductive structures are coplanar with the top surface of the conductive layer 195, but not the etch-stop layer 110b. Banerjee ¶ 183.

In view of Fang, a POSITA would have found it obvious to modify Park's planarization process such that *top surfaces of the plurality of conductive structures* ("contact plugs" 201-206), *the insulating layer* ("connection region insulating layer" 180), *and a portion of the etch-stop layer* ("etch-stop layer" 110b) *are coplanar*.
Banerjee ¶ 184.

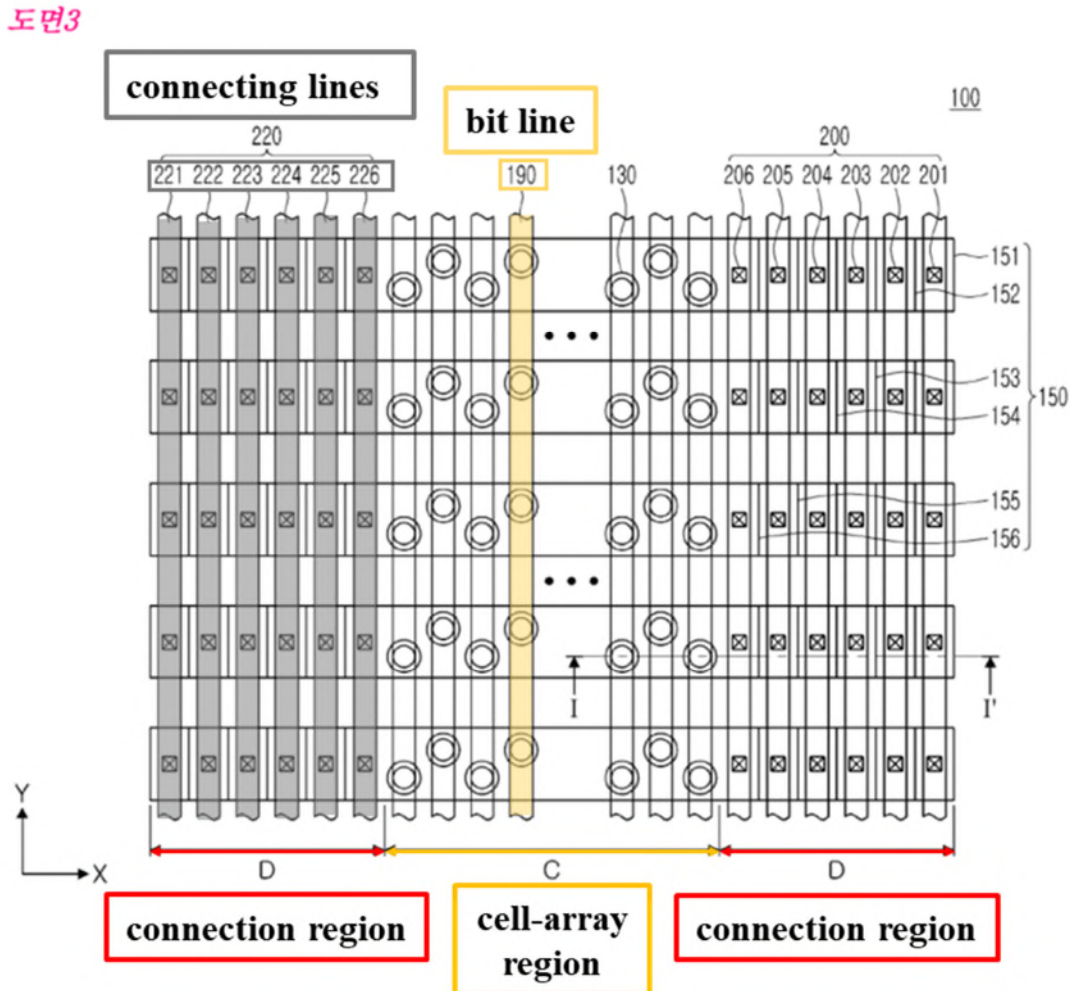
Park discloses planarizing the staircase structure “to remove unnecessary semiconductor material and insulating material covering the top connection region

insulating layer (180).” Park, [0089]. This occurs after forming the channel and before depositing the conductive layer 195, the conductive drain of the channel. *Id.*, [0088]-[0089]. In view of Fang, it would have been obvious that the materials above the top-surface plane of the etch-stop layer 110b is “unnecessary” and may be removed. *Id.*, [0089]. This would result in a device as shown below:



Id., Fig. 9j (coplanar, gate-stack-on-top modification). This configuration is compatible with Park’s disclosure. For example, when Fang’s coplanar configuration is applied on Park’s device, the connecting lines 221-226 would be lowered to roughly the same height as the conductive layer 195. This would not interfere with the device’s function. Specifically, the conductive layer 195 connects

the channel region 130 with a bit line 190. *Id.*, [0040]. The connecting lines 221-226 and bit lines 190 are parallel in the plan view in the x-and-y-axis direction:



Id., Fig. 3. Thus, lowering the connecting lines to the same height as the bit lines in the z-axis direction has no functional impact because parallel lines do not intersect whether they are at the same height in the z-axis direction. This permits the device to function as intended. Banerjee ¶ 185.

Indeed, Fang discloses but does not show select lines and access lines that electrically connect to gate electrodes through contacts 155a-155d. Fang, [0026],

[0040]. A POSITA would have understood these select lines and access lines to constitute Park's connecting lines. Banerjee ¶ 186. As such, Fang's select lines/access lines are at the same vertical height as its contacts 155a-155d, same as Park's modified configuration. Fang's configuration renders it obvious that the extra thickness in Park's connection region insulating layer above the plane of the etch-stop layer is unnecessary. Thus, applying Fang's coplanar configuration on Park's device represents nothing more than applying a known technique and a suitable option on a similar device. *Retractable Techs.*, 653 F.3d at 1303.

B. Claim 10:

1. **[10] “The semiconductor structure of claim 1, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.”**

Park at least renders obvious claim 1. §XII.B. Park in view of Fang renders obvious claim 10.

As explained, claim 10 is obvious over Park because the difference, if any, is merely dimensional not resulting in differences in performance. §XI.A.1; §XII.B (Park at least renders obvious claim 1); Banerjee ¶¶ 187-88.

If more is required (it is not), Fang discloses an analogous semiconductor structure with an etch-stop layer. Fang, Fig. 6, [0020]. The etch-stop layer of both Park and Fang may comprise silicon nitride. Park, [0124], [0060], [0067], [0063], §XII.F.1. Fang's etch-stop layer “may be formed by conventional techniques....”

Fang, [0020]. It would have been obvious that such conventional techniques, some of which Park already uses, may be used to form Park's etch-stop layer. Park, [0086]; Banerjee ¶ 189. Fang's etch-stop layer "may be formed over the stairs 125 at a thickness ranging from about 50 Å to about 1000 Å," or about 5 nm to 100 nm. Fang, [0021]. This range overlaps with the claimed *range between 10 nm and 1000 nm*. Thus, Park in view of Fang renders claim 10 obvious. Banerjee, ¶ 189.

To the extent the thickness of Fang's etch-stop layer would need to be reduced to account for Park's extra etch-stop layer, *e.g.*, to maintain a total etch resistance, a POSITA would have found it obvious that the thickness would still overlap with the claimed *range between 10 nm and 1000 nm*. For example, a POSITA would not have reduced Fang's etch-stop layer to below 10 nm (the reduction required to avoid any overlap with the claimed range) to account for Park's extra etch-stop layer. Banerjee ¶ 190.

Were PO to argue that this combination would not have been obvious because Park does not disclose the height of its staircase structure and thus the depths of contact holes, PO would be wrong. A POSITA would have understood that both Fang and the '711 patent include a broad range (20x and 100x, respectively) around "notoriously well[-]known" thicknesses for etch-stop layers. Ex. 1002, 156. A POSITA would have found it obvious that some subset of values within the range would work with an appropriate choice of etchant and relative etch selectivities. The

'711 patent is consistent with this understanding. The patent merely discloses the thickness of each dielectric layer or sacrificial/conductor layer (a range of 10 to 200 nm, a factor of 20x). Ex. 1001, 6:38-40. But the patent places no upper or lower limits on the number of steps in the staircase. Furthermore, it discloses that “a thickness of the SC layer 102 [*i.e.*, a step] can be different for each staircase level.” *Id.*, 6:40-41. Therefore, the height of the '711 patent staircase and thus the depths of its contact holes are completely unknown. Yet presumably the claimed range is adequate for an etch-stop layer for the staircase, regardless of the contact-hole depths. That being the case, a POSITA could have easily configured Park in view of Fang's teachings to have an etch-stop layer within the broad claimed thickness range. Banerjee ¶ 191.

C. Claim 15:

1. [15] **“The semiconductor structure of claim 14, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.”**

Park in view of Fang also renders obvious claim 15. See §XII.N.1.

Fang discloses that “[t]he thickness of the etch stop material 130 on the stairs 125 may be substantially uniform.” Fang, [0021]. In light of that, *thicknesses of the etch-stop layer* (“etch-stop layer” 110b) *is the same on the side and top surfaces of each step*. Banerjee ¶¶ 192-93.

A POSITA would have been motivated to apply Fang’s teaching with the knowledge that an etch-stop layer of uniform thickness on all steps was desirable. §XII.N.1. Further, a POSITA would have had a reasonable expectation of success because a uniform thickness is consistent with Park’s repeated references to “*the* thickness of the etch-stop layer.” Park, [0006], [0060], [0067], [0070]-[0071]; Banerjee ¶ 194.

D. Claim 17:

1. [17] **“The semiconductor structure of claim 13, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.”**

The additional limitation of claim 17 is identical to that of claim 10. Park in view of Fang renders it obvious for the same reason as explained above. §XIII.B.1; Banerjee ¶ 195.

E. Motivation to Combine

In addition to the reasons already stated (§§XIII.A.1, XIII.C.1), a POSITA would have been motivated to apply Fang’s disclosures of the coplanar configuration and the etch-stop-layer thickness on Park’s staircase structure and would have had a reasonable expectation of success in doing so. Banerjee ¶ 196.

Both Park and Fang are directed to reducing defects in 3D memory devices resulting from over-etching shallow openings when forming openings for the word-line conductive structures. Park, [0014], Fang, [0004]. A POSITA would have understood that Park and Fang have the same goal, *e.g.*, “improv[ing] reliability” of

a “high[ly] integrat[ed]” 3D memory device by reducing “processing ... , complexity, and cost” of the manufacturing process. Park, [0003]; Fang, [0004]. A POSITA would have known that such manufacturing processes involve many parameters and would have found Fang’s “specific details” useful to supply information, *e.g.*, thickness of the etch-stop layer, that Park does not specify. Fang, [0009]. Thus, a POSITA would have been motivated to consult Fang in addition to Park for a more complete combined teaching. Banerjee ¶ 197.

A POSITA would have known that Fang’s etch-stop-layer thickness was reasonable and thus would have had a reasonable expectation of success in adapting Park’s etch-stop layer to Fang’s disclosure. §§XIII.B.1-XIII.C.1; Banerjee ¶ 198.

Further, a POSITA would have had a reasonable expectation of success because of similarities between Park’s and Fang’s disclosures regarding the etch-stop layer. Banerjee ¶ 199. For example, Park discloses that its etch-stop layer may be formed of a material having an etch selectivity with respect to the connection region insulating layer through which vertical openings are formed. Park, [0050], [0108]. Fang discloses the same. Fang, [0020]. Park discloses that its etch-stop layer may be formed of silicon nitride. §XII.F.1. So does Fang. Fang, [0020].

Moreover, a POSITA would have had a reasonable expectation of success because Park’s and Fang’s disclosures are directed to similar 3D memory devices with staircase word-line structures, *e.g.*, both comprising alternating conductive and

dielectric layers at each step, one or more etch-stop layer and an insulating layer on the steps, and conductive structures penetrating the various layers to form contacts with the conductive layers. Banerjee ¶ 200.

A POSITA would have found it obvious that Fang's thickness range could be applied to Park's device and would have been motivated to do so to fill in a parameter that Park does not disclose. Banerjee ¶ 201. Although Park's embodiment relied on in this Petition discloses an additional barrier layer, Park also discloses an embodiment with a single etch-stop layer 110 like Fang. Park, Fig. 4, claim 1 (claiming one or more etch-stop layers). And Park makes no distinction regarding the thickness of its etch-stop layer based on the number of such layers in the embodiment. *See generally id.* This is consistent with a POSITA's understanding that the etch-stop thickness was flexible based on other parameters, *e.g.*, the choice of etchant. Thus, a POSITA would have found it obvious that Park's etch-stop layer could be adapted to Fang's thickness range.

Additionally, a POSITA would have been motivated to apply Fang's disclosure to make the top surface of the etch-stop layer coplanar with those of the insulating layer and conductive structure. First, Park itself teaches planarizing to remove unnecessary materials at the top of the staircase structure. Park, [0089]. In view of Fang, it would have been obvious that the materials above the top-surface plane of the etch-stop layer is unnecessary. §XIII.A. Thus, the extent to which they

are removed is simply a matter of design choice. Banerjee ¶ 202. In other words, partial or complete removal of the materials above the top-surface plane of the etch-stop layer are both suitable options for the design. And a suitable option by itself provides a motivation to combine. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023). Further, Fang's configuration reduces the overall height of the structure, reducing device size, which is desirable for memory devices. Banerjee ¶ 202.

A POSITA would have had a reasonable expectation of success to apply Fang's coplanar disclosure to Park's device. The modification simply extends Park's existing planarization process to remove a greater thickness of the same, unnecessary, materials in view of Fang. Banerjee ¶ 203. Additionally, this modification is compatible with Park's device. §XIII.A.1.

XIV. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See generally* Ex. 1002. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness. Banerjee ¶ 204.

XV. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Petition for *Inter Partes* Review of U.S. Patent No. 10,672,711

Respectfully submitted,

Dated: November 12, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the Petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,885 words.

Dated: November 12, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated documents and exhibits were caused to be served on November 12, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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Petition for *Inter Partes* Review of U.S. Patent No. 10,672,711

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